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TECHNICAL MANUAL

FLIGHT CONTROL COMPUTER

(500 Series Vehicles)

Prepared under Contract

NAS 8-14000

by

International Business Machines Corporation

Federal Systems Division

Huntsville, Alabama

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THE CONTENTS OF THE PRECEDING SECTIONS OF THIS MANUAL APPLY TO THE VEHICLE SPECIFIED ON THESE DATA SHEETS EXCEPT FOR THE FOLLOWING DIFFERENCES

Because of variations in vehicle flights the
filters may change from vehicle to vehicle; therefore, the filter information for each vehicle is located in
the Data Sheets. If a filter configuration in any Flight Control Computer is identical to a previously used filter, it will be referenced to the earlier configuration.

A technical description and electrical schematic for each filter will be found on the figure specified in the following listing:

S-IU-501 Filter	Figure No.	
$\Delta \phi \mathbf{Y} \text{ and } \Delta \phi \mathbf{P} \mathbf{S-IC}$	501-1	
$\Delta \phi \mathbf{Y}$ and $\Delta \phi \mathbf{P} \mathbf{S}$ -II	501-2	
$\Delta \phi \mathbf{Y}$ and $\Delta \phi \mathbf{P} \mathbf{S}$ -IVB	501-3	
$\Delta \phi \mathbf{R} \mathbf{S}$ -IC	501-4	
Δφ R S-II	501-5	
$\dot{\phi}$ Y and $\dot{\phi}$ P S-IC	501-6	
$\dot{\phi}$ Y and $\dot{\phi}$ P S-II	501-7	
$\dot{\phi}$ Y and $\dot{\phi}$ P S-IVB	501-8	
∮R S-IC	501-9	
∮RS-II	501-10	

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CIRCUIT DESCRIPTION

The $\Delta \phi Y$ and $\Delta \phi P$ S-IC filters are electrically and physically identical; therefore, the following description applies to both filters.

An amplified $\Delta \phi Y$ or $\Delta \phi P$ signal is applied to pins 7 and 8 of the filter during the S-IC burn mode. The amplified $\Delta \phi$ signal is coupled through the balanced, bridged H network consisting of R1 through R6 and C1 through C3. The attenuated and filtered $\Delta \phi$ signal is then coupled through the ladder network consisting of R11 through R19 and C4 through C8. The filter output is applied to pins 5 and 6. The bending mode frequencies (occurring between 1 Hz and 7 Hz) are shunted by C1 in the H network. For frequencies above 10 Hz the shunt effect of C1 is reduced by the bridge capacitors C2 and C3. The filter rolloff is then determined by the ladder network shunt capacitances C4 through C8. The overall response of the filter is such that both bending mode frequencies and higher frequencies are removed from the $\Delta \phi$ channel while the $\Delta \phi$ control signal (occurring at approximately 0.25 Hz) is not greatly reduced.

The control signal gain for the $\Delta \phi Y$ and $\Delta \phi P$ channels, an (expressed in degrees of engine movement per degrees of attitude error) is a stepped function which decreases with successive time intervals. The time intervals are established by the switchpoint signals from the IU Switch Selector which occur at T_1 +105 seconds (switchpoint 1) and at T_1 +120 seconds (switchpoint 2). For the $\Delta \phi$ channels, a₀ is 0.90 degree/degree from $T_1 + 0$ seconds to T_1 + 105 seconds, 0.45 degree/degree from T_1 + 105 seconds to $T_1 + 120$ seconds, and 0.32 degree/degree from $T_1 + 120$ seconds to the end of the S-IC burn mode. Within the $\Delta \phi$ filters, switchpoint 1 enters pin 1 and energizes K1. The normally-open contacts of K1 close, and the R7, R8 branch is added to the input of the ladder network. The addition of the R7, R8 shunt branch increases the signal attenuation within the filter and thus decreases the gain of the $\Delta \phi$ channel. Switchpoint 2 enters pin 3 of the filter and energizes K2. The normally-open contacts of K2 close, and the R9, R10 branch is added to the input of the ladder network. The addition of the R9, R10 shunt branch increases the signal attenuation of the filter to its maximum value and sets the $\Delta \phi$ channel gain to its minimum value during the S-IC mode of flight.

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CIRCUIT DESCRIPTION

The $\Delta \phi P$ and $\Delta \phi P$ S-II filters are electrically and physically identical; therefore, the following detail analysis applies to both filters.

An amplified $\Delta \phi Y$ or $\Delta \phi P$ signal is applied to pins 7 and 8 of the filter during the S-II burn mode. The amplified $\Delta \phi$ signal is routed through the series-parallel attenuation network consisting of resistors R1 through R11 to pins 5 and 6, where it is externally applied through a buffer amplifier to its associated 50 ma servo amplifier. At high frequencies capacitor C1 presents a low impedance shunt across the signal line. High frequency components of the $\Delta \phi$ signal are therefore prevented from reaching the 50 ma servo amplifiers. At 60 seconds after start of the S-II burn mode, relay K1 is energized by the switchpoint 3 signal (+28 Vdc) from the Switch Selector, and resistors R4 and R6 are shunted across the signal line. This reduces the amplitude of the signal developed across the signal line, and signal attenuation is thus increased. At 190 seconds after the start of the S-II burn mode, relay K2 is energized by the switchpoint 4 signal (+28 Vdc) from the Switch Selector, and resistor R7 is also shunted across the signal line. This causes further attenuation of the $\Delta\phi$ signal applied to the 50 ma servo amplifiers.

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Figure 501-2. $\Delta \phi Y, P S-II$ Filter (S-IU-501), Schematic Diagram

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The $\Delta \phi Y$ and $\Delta \phi P$ S-IVB filters are electrically and physically identical. Therefore, the following detail analysis applies to both types of filters.

During S-IVB burn mode, an amplified $\Delta \phi Y$ or $\Delta \phi P$ signal is applied between pins 8 and 6 of the filter. This amplified $\Delta \phi$ signal is routed via attenuating resistors R1 through R3 to pins 5 and

6 (pin 6 is common to the input and output). The $\Delta \phi$ signal is then routed to the associated 50 ma servo amplifiers. Capacitor C1 presents a low shunt impedance to ac components of the $\Delta \phi$ signal. Capacitor C3 bypasses voltage transients (as may be generated by relay switching action) to the Flight Control Computer power supply common bus (28 Vdc Return).

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through R10, to pins 5 and 6. The $\Delta \phi R$ output be-

Figure 501-4. △Ø R S-IC Filter (S-IU-501), Schematic Diagram



Figure 501-5. $\Delta \phi R$ S-II Filter (S-IU-501), Schematic Diagram

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CIRCUIT DESCRIPTION

The $\dot{\phi}$ Y or $\dot{\phi}$ P signal is applied between pins 7 and 8 of the filter during the S-IC burn mode. The $\dot{\phi}$ signal is coupled through a ladder network (comprised of R7 through R14, R23 through R26, R31 and R32, and C11 through C13) and two balanced, bridged H networks (comprised of R1 through R6, C1 through C5 and R15 through R22, C6 through C10) to the output pins 5 and 6. The frequency ranges which are rejected by the filter are from 1 Hz to 7 Hz (bending mode frequencies) and above 10 Hz. The control signal gain (expressed in degrees of engine movement per degrees of attitude error per second) of the $\dot{\phi}$ Y and $\dot{\phi}$ P channels is a stepped function with values of 0.69 degree/degree/second from T₁ +0 seconds until T₁ +105 seconds, 0.44 degree/degree/second from T₁ +105 seconds until T₁ +120 seconds, and 0.30 degree/degree/second from T₁ +120 seconds until the end of the S-IC burn mode. The gain switching occurs (at switchpoints 1 and 2) in the same manner as in the $\Delta\phi$ Y and $\Delta\phi$ P filters.

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CIRCUIT DESCRIPTION

An amplified $\dot{\phi}$ Y or $\dot{\phi}$ P signal is applied between pins 8 and 7 of the filter during the S-II burn mode. This $\dot{\phi}$ signal is routed through the seriesparallel resistor attenuation network comprised of resistors R1 through R7, and R10 through R13 to pins 5 and 6. The $\dot{\phi}$ signal across pins 5 and 6 is then routed through a buffer amplifier to the associated 50 ma servo amplifier. Capacitors C1 and C2 shunt the bending mode frequency components of the signal to resistor R10, while capacitor C3 shunts the high frequency components of the signal directly across the signal line. At 60 seconds after start of the S-II burn mode, relay K1 is energized by the switchpoint 3 signal (+28 Vdc) from the Switch Selector, and resistor R8 is shunted across the signal line. This reduces the amplitude of the signal developed across the signal line, and signal attenuation is then increased. At 190 seconds after the start of the S-II burn mode, relay K2 is energized by the switchpoint 4 signal (+28 Vdc) from the Switch Selector, and resistor R9 is also shunted across the signal line. This causes further attenuation of the ϕ signal applied to the 50 ma servo amplifiers.

Figure 501-7. $\dot{\phi}$ Y, P S-II Filter (S-IU-501), Schematic Diagram

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CIRCUIT DESCRIPTION

The $\dot{\phi}$ Y and $\dot{\phi}$ P S-IVB filters are electrically and physically identical, therefore, the following detail description applies to both filters.

During the S-IVB burn mode, an amplified $\dot{\phi}$ Y or $\dot{\phi}$ P signal is applied between pins 8 and 6 of the filter. The $\dot{\phi}$ signal is routed through resistor R1, the closed contacts of relay K1, inductor L1, and resistor R3 to pins 5 and 7. The signal is then routed through a buffer amplifier to the associated

50 ma servo amplifier. Inductor L1 and capacitor C2. connected in a parallel LC configuration, present a high series impedance to ac components of the $\dot{\phi}$ signal. Capacitors C1, C3, C4, and C5 provide a low impedance shunt for ac components of the signal. At 270 seconds after the start of the second S-IVB burn mode, relay K1 is energized by the switchpoint 5 signal from the Switch Selector. With relay K1 energized, resistor R2 is placed in the signal path, and $\dot{\phi}$ signal attenuation is increased.

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An amplified ϕR signal is applied between pins 8 and 7 of the ϕR S-IC filter during the S-IC burn mode. The ϕ signal is routed through the series attenuation network consisting of resistors R1 through R8 and R11 through R14 to pins 5 and 6. The ϕ signal between pins 5 and 6 is then externally routed through a buffer amplifier to the 50 ma servo

amplifiers. Capacitors C1 and C4 shunt the bending mode frequency components of the signal to resistors R9 and R10. Capacitors C2, C3, C5, C6, and C7 provide a low impedance shunt across the signal line for the high frequency components of the $\dot{\phi}$ signal.

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Figure 501-9. ØR S-IC Filter (S-IU-501), Schematic Diagram



An amplified $\dot{\phi}R$ signal is applied between pins 8 and 7 of the $\dot{\phi}R$ S-II filter during the S-II burn mode. The $\dot{\phi}$ signal is routed through series-parallel attenuating resistors R1 through R5 to pins 5 and 6. The signal between pins 5 and 6 is then externally

routed through a buffer amplifier to the 50 ma servo amplifiers. Capacitors C1 and C2 provide a low impedance shunt across the signal line for the high frequency components of the signal.

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Figure 501-10. $\dot{\phi}$ R S-II Filter (S-IU-501), Schematic Diagram

THE CONTENTS OF THE PRECEDING SECTIONS OF THIS MANUAL APPLY TO THE VEHICLE SPECIFIED ON THESE DATA SHEETS EXCEPT FOR THE FOLLOWING DIFFERENCES:

Because of variations in vehicle flights the
filters may change from vehicle to vehicle; therefore, the filter information for each vehicle is located in the Data Sheets.

The S-IU-502 filters are identical to the S-IU-501 configurations. The list below indicates the figure in the S-IU-501 Data Sheets that describes each S-IU-502 filter. Refer to the specified figure for a technical description and an electrical schematic of the filter.

S-IU-502 Filter	Figure No.
$\Delta \phi \mathbf{Y}$ and $\Delta \phi \mathbf{P} \mathbf{S}$ -IC	501 - 1
$\Delta \phi \mathbf{Y}$ and $\Delta \phi \mathbf{P} \mathbf{S}$ -IVB	501-3
$\Delta \phi R S-IC$	501-4
ΔφRS-II	501-5
$\dot{\phi}$ Y and $\dot{\phi}$ P S-IC	501-6
ϕ Y and ϕ P S-II	501-7
ϕ Y and ϕ P S-IVB	501-8
ϕ R S-IC	501-9
φRS-II	501-10

The Switching Control Circuit in the S-IU-502 Flight Control Computer has been modified as shown
in Figures 502-1 and 502-2 to accept a new method for latching the Flight Control Computer into S-IC burn mode. These figures show only the circuitry affected by the modification. The complete switching circuit functional block diagram is shown in Figure 2-40, and the complete switching circuit schematic diagram is shown in Figure 2-44 sheet 6.

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Figure 502-1. Switching Circuit, Functional Block Diagram - S-IU-502 Modification



CIRCUIT DESCRIPTION

A new connection and 3 diodes have been added to provide a satisfactory method for latching the Flight Control Computer into the S-IC burn mode. The new design prevents the possibility of overloading the S-IC Burn Mode Substitute Signal from the GSE or the First Motion Signal from the Switch Selector (when either is present at J129-34 and J129-33) by conduction through J24-28 and J24-30 of Switching Circuit "C" to the +28 Vdc bus, thus holding all the S-IC mode relays energized when the IU +28 Vdc supply is removed from the Flight Control Computer. The S-IC Test Signal from the GSE is also protected from a similar overload.



THE CONTENTS OF THE PRECEDING SECTIONS OF THIS MANUAL APPLY TO THE VEHICLE SPECIFIED ON THESE DATA SHEETS EXCEPT FOR THE FOLLOWING DIFFERENCES

Because of variations in vehicle flights the
filters may change from vehicle to vehicle; therefore, the filter information for each vehicle is located in the Data Sheets.

Filters (S-IU-503) which DO NOT CHANGE from the S-IU-501 or S-IU-502 configuration are listed below, and the figure indicated is located in the S-IU-501 Data Sheets. Refer to the specified figure for a technical description and an electrical schematic of the filter.

S-IU-503 Filter	Figure No.
∆øY and ∆øP S-IC	501-1
$\Delta \phi \mathbf{Y}$ and $\Delta \phi \mathbf{P} \mathbf{S}$ -II	501-2
∆¢ R S-IC	501-4
∆¢ R S-II	501-5
$\dot{\phi}$ Y and $\dot{\phi}$ P S-IC	501-6
ĠR S-II	501-10

A technical description and electrical schematic for each filter that DOES CHANGE from the S-IU-501 or S-IU-502 configuration will be found on the figure specified in the following listing:

S-IU-503 Filter	Figure No.
$\Delta \phi \mathbf{Y} \text{ and } \Delta \phi \mathbf{P} \mathbf{S}$ -IVB	503-1
$\dot{\phi}$ Y and $\dot{\phi}$ P S-II	503-2
$\dot{\phi}$ Y and $\dot{\phi}$ P S-IVB	503-3
őR S-IC	503-4

The Switching Control Circuit in the S-IU-503 Flight Control Computer has been modified in the same manner as the S-IU-502 Flight Control Computer. This modification is described in change number 2 of the S-IU-502 Data Sheets.

In its present configuration, it has been determined that damage could result to the spacecraft if one of the outboard engines should malfunction during the S-IC burn phase of the mission. In order to reduce the probability of damage, an S-IC engine bias circuit has been added to the S-IU-503 Flight Control Computer to provide an electrical cant signal that will cause the S-IC gimballed engines to cant outward during the major portion of the S-IC burn mode. The outward cant of the engines will reduce the moment produced about the center of mass of the vehicle if an engine malfunction should occur. Reduction of the moment will also reduce the forces applied to the spacecraft; therefore, damage to the spacecraft is less probable. The engine cant signal is applied to the Flight Control Computer at liftoff +20 seconds and will remain applied until the start of S-II burn mode. The outward cant of each engine will be approximately 2 degrees and is achieved by retracting the pitch and yaw actuators of each engine by approximately 1.41 degrees.

The engine cant circuit is shown in Figure 503-5 and depicts its impact on the Saturn V Control System components. (This figure is part of Figure 2-1, Sheet 2. Only the affected areas are shown.) The engine cant circuit is also shown in Figure 503-6 and depicts its impact on the S-IU-503 S-IC and S-II burn modes within the Flight Control Computer. (This figure is part of Figure 2-2. Only the affected areas are shown.) The schematic diagram of the engine cant circuit, including ramp generator J36, is shown in Figure 503-7. (This figure is a simplified version of Figure 2-44, Sheet 4. Only the affected circuitry is shown.)

In the S-IU-503 Flight Control Computer, rate gyro filtering circuits (also called spatial filtering circuits) have been added to the triple-redundant pitch, yaw, and roll attitude rate channels. This filtering is used during the S-IVB modes of flight. The S-IVB Burn Mode, Functional Block Diagram is changed as shown in Figure 503-8. (This figure is part of Figure 2-3. Only the affected areas are shown.) The S-IVB Coast Mode, Functional Block Diagram , is changed as shown in Figure 503-9. (This figure is part of Figure 2-4. Only the affected areas are shown.)

The ϕ yaw and ϕ pitch rate gyro filtering is used only during the S-IVB coast mode, while the ϕ roll rate gyro filtering is used during S-IVB burn and coast modes. The ϕ yaw and ϕ pitch rate gyro filtering circuits are physically comprised of a rate gyro filter module and part of the dc amplifier scaling boards associated with the ϕ yaw and ϕ pitch dc amplifiers. The ϕ roll rate gyro filtering circuits are located on redesigned dc amplifier modules. Flt Cont Cmptr (500), Sect. IV

The rate gyro filtering removes an 18 Hz component (a result of vehicle shell mode vibrations) from the attitude rate signals. The 18 Hz component reaches amplitudes of 1.75 degrees/second, while the average attitude rate signals are nearly 0 degrees/ second. The effect of the 18 Hz component is most serious in the APS control system. During S-IVB burn mode, it significantly reduces the sensitivity of the APS roll control channel, thus allowing large attitude errors to develop before the APS can make the necessary correction. In the S-IVB coast mode, the problem is also present in the yaw and pitch APS channels. The rate gyro filtering circuits remove the 18 Hz component from the attitude rate signals and thus eliminate these problems.

Figure 503-10 shows the rate gyro filtering for the $\dot{\phi}$ roll channels. (This figure is a simplified version of the Flight Control Computer, Schematic Diagram, Figure 2-44, showing only the affected circuitry.)

Figures 503-11, 503-12, and 503-13 show the rate gyro filtering for the ϕ yaw and ϕ pitch channels during the S-IVB coast mode. (These figures are simplified versions of the Flight Control Computer, Schematic Diagram, Figure 2-44. Only the affected circuitry is shown.)

Rate gyro filter module J39, shown in Figure 503-11, processes both ϕ yaw and ϕ pitch tripleredundant signals, and it forms a part of the rate gyro filtering which takes place in the dc amplifier scaling boards A and B. Each of the rate gyro filter channels is a low-pass filter with series resistance and shunt capacitance which attenuates the 18 Hz component of the ϕ yaw and ϕ pitch signals.

Figure 503-12 shows the rate gyro filtering circuitry for the triple-redundant $\dot{\phi}$ yaw signals during the S-IVB coast mode. Scaling board A, J92, is shown in detail.

Figure 503-13 shows scaling board B, J118, in detail. This scaling board processes the ϕ pitch S-IVB coast signals in the same manner that scaling board A processes the ϕ yaw S-IVB coast signals.

5 The S-IU-503 Flight Control Computer has three redesigned dc amplifier scaling boards, J35, J50, and J51, for the $\Delta \phi$ yaw, $\Delta \phi$ roll, and $\Delta \phi$ pitch attitude error signal channels. The new scaling boards provide a gain-switching capability for the $\Delta \phi$ channels when the spacecraft attitude control inputs are used. The dc amplifiers in the attitude error channels provide a channel gain of 3.75 for the IU Guidance System inputs which have a scale factor of 0.8 volt/degree of attitude error. Because the scale factor for the Spacecraft Guidance System is only 0.3 volt/degree, the attitude error channels in the Flight Control Computer must have a gain of 10 in order to maintain control system stability. The channel gain is set by the amount of feedback coupled through the dc amplifier scaling boards.

Figure 503-14 shows the scaling board circuitry which performs the gain switching.

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CIRCUIT DESCRIPTION

The $\Delta \phi Y$ and $\Delta \phi P$ S-IVB filters are electrically and physically identical. Therefore, the following detail analysis applies to both types of filters.

During S-IVB burn mode, an amplifier $\Delta \phi Y$ or $\Delta \phi P$ signal is applied between pins 8 and 9 of the filter. This amplified $\Delta \phi$ signal is coupled through attenuating resistors R1, R3, R5, and R2, R4, R6 to pins 5 and 6. The $\Delta \phi$ signal is then routed to the associated 50 ma servo amplifiers. Capacitor C1 represents a low shunt impedance to ac components of the $\Delta \phi$ signal. At T₆+577 seconds, switchpoint 5 (see note 2 above) is applied at pins 3 and 10, energizing K1 and causing the normally-closed contacts of K1 to open. At this time, R7 and R8 are added to the circuit increasing the attenuation and decreasing the gain, a₀, from 0.81 degree/degree to 0.22 degree/degree.

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CIRCUIT DESCRIPTION

An amplified $\dot{\phi}$ Y or $\dot{\phi}$ P signal is applied between pins 8 and 7 during the S-II burn mode. This $\dot{\phi}$ signal is routed through the series-parallel resistor attenuation network comprised of R1 through R14 to pins 5 and 6. The $\dot{\phi}$ signal at pins 5 and 6 is then routed through a buffer amplifier to the associated 50 ma servo amplifier. The resistor and capacitor network comprised of C1 through C4, and R6 shunts the bending mode frequency components of the signal, while C5 and C6 shunt the high frequency components of the signal, while C5 and C6 shunt the high frequency components directly across the signal line. At 60 seconds after the start of the S-II burn mode, relay K2 is energized by the switchpoint 3 signal (+28 Vdc) from the Switch Selector, and resistor R16 is shunted across the signal line. This reduces the amplitude of the signal across pins 5 and 6, thus increasing signal attenuation. At 190 seconds after the start of the S-II burn mode, relay K1 is energized by the switchpoint 4 signal (+28 Vdc) from the Switch Selector, and resistor R15 is also shunted across the signal line. This causes further attenuation of the $\dot{\phi}$ signal applied to the 50 ma servo amplifiers.

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CIRCUIT DESCRIPTION

The ϕ Y and ϕ P S-IVB filters (S-IU-503) are electrically and physically identical; therefore, the following detail description applies to both filters. During the S-IVB burn mode, an amplified $\phi \dot{Y}$ or $\phi \dot{P}$ signal is applied between pins 8 and 9 of the filter. The signal is coupled through R3 through R6, the normally-closed contacts of relay K2, the normallyclosed contacts of relay K1, the tank circuit coils L1 and L2, and R7 and R8 to pins 5 and 6. The signal is then routed through a buffer amplifier to the associated 50 ma servo amplifier. Inductor L1 and capacitor C2 form a resonant tank circuit which is in series with the signal path, and presents a high impedance to ac components of the signal. Capacitor C1 shunts the ac components directly across the signal lines. Inductor L2 and capacitor C3 form a tank circuit which is identical to L1 and C2 on the opposite signal

line. Capacitor C4 provides a shunt across the signal lines for the very small ac component which passes through the tank circuits.

At T₆ +577 seconds, relay K1 is energized if the switchpoint 5 signal (see note 2 above) is applied from the Switch Selector. When the contacts of relay K1 open, resistors R9 through R14 are added in series with the signal line, and the signal attenuation is increased. This causes the channel gain, a_1 , to decrease from 0.97 degree/degree/second to 0.23 degree/degree/second.

At T₆ +718 seconds, relay K2 is energized if the switchpoint 6 signal (see note 3 above) is applied from the Switch Selector. When the contacts of relay K2 open, resistors R1 and R2 are added in series with the signal line, and the signal attenuation is increased. This causes the channel gain, a₁, to decrease from 0.97 degree/degree/second to 0.70 degree/degree/second.

Figure 503-3. • Y, P S-IVB Filter (S-IU-503), Schematic Diagram

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CIRCUIT DESCRIPTION

An amplified ϕR signal is applied between pins 7 and 8 of the ϕR S-IC filter during the S-IC burn mode. The ϕ signal is routed through the series attenuation network consisting of resistors R1 through R3, and R5 through R13 to pins 5 and 6. The signal between pins 5 and 6 is then externally routed through a buffer amplifier to the 50 ma servo amplifiers. The high frequency components of the signal are shunted directly across the signal lines by capacitors C2, C6, C7, C8, and C9. The ac component of the signal associated with the bending mode frequency is shunted across resistor R4 by capacitors C1, C3, C4, and C5.

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S-IU-503 Modification

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Figure 503-6. S-IC and S-II Burn Modes, Functional Block Diagram - S-IU-503 Modification

CIRCUIT DESCRIPTION

The engine cant signal is shown entering the Flight Control Computer at connector J3, pins W and V and connector J8, pin L. The J3 inputs are 28 Vdc applied from the IU Switch Selector through the IU Control Distributor. (The IU Switch Selector outputs are triple-redundant, but two-out-of-three voting occurs in the IU Control Distributor so that either one or two engine cant signals are applied to the Flight Control Computer.) The J8 input is 28 Vdc applied from the GSE for test purposes. The engine cant inputs are coupled through connector J37, pins E, F, and G to the ramp generator.

The ramp generator establishes a stable reference voltage to charge a resistance-capacitance integrator network. The integrator network produces an output voltage which rises as a function of time. This output voltage provides the cant bias which is applied to each of the yaw and pitch 50 ma servo amplifiers. In addition, the ramp generator provides for relay switching to ensure that the cant bias is applied only during the S-IC mode of flight. Further relay switching serves as a backup to ensure that the cant bias cannot be applied to the servo amplifiers during the S-IVB mode of flight.

Within the ramp generator J36, the 28 Vdc cant signals present at pins 7, 8, or 9, as applicable, are coupled through isolation diodes CR1, CR2, or CR3 to resistor R5 and are applied across the series zener diodes CR6 and CR7 to the 28 Vdc return at pin 5. Each zener diode drops 9 volts; therefore, the voltage at the top of CR6 is maintained at a constant 18 volts. This constant 18-volt potential is used to charge the integrator network comprised of R6, R7 and C1, C2. The integrator output voltage is taken across C1, C2 and applied to the integrator load. The output voltage is a DC ramp which starts at 0 volts and approaches a positive 9.2 volts as a function of time according to the time constant of the integrator.

It is necessary for the engine cant signal to be smoothed in this manner so that the cant voltage which is applied to the 50 ma servo amplifiers will not change at a rate which could cause the engine actuator drive signals to change at an excessive rate.

The integrator output voltage from C1, C2 is coupled through the normally-closed contacts of K1 and through the normally-open contacts of K2 (K2 is energized during S-IC burn mode), through R10, R11 to the output pins 4 and 2. The ramp generator output is applied through two series 200K resistors to a pair of 200-turn input signal windings at pins 6 and D of each 50 ma servo amplifier. The same polarity is. applied to each servo amplifier input (pin 6 is positive in respect to pin D) so that each engine actuator drive signal will be affected in the same manner. (All engine actuators are caused to retract.)

The S-IC burn mode signal is applied from switching control circuit J129, pins 33 and 34, through J37-D to the ramp generator at pin 6. This 28 Vdc signal is coupled through CR4 and applied across R1 and R3. The positive voltage developed across R3 is applied to the base of transistor Q1 which is half of a Darlington-connected relay driver. The positive base voltage applied to Q1 causes it to turn ON and drive the base of transistor Q3. Transistor Q3 is then turned ON and draws its collector current from the 28-volt source through the relay coil of K2. This causes K2 to energize and remain energized during S-IC burn mode.

The S-IVB burn mode signal is applied from J129, pins 8 and 9, through J37-A to the ramp generator at pin 1. This is a backup signal to the S-II burn mode signal (which should remove the S-IC burn mode signal and turn OFF relay K2, opening the ramp generator output path). The 28 Vdc S-IVB burn mode signal is applied to a relay driver circuit which is identical to the circuit described for the S-IC mode relay driver. When the S-IVB burn mode signal is applied, relay K1 is energized, and its normallyclosed contacts open the ramp generator output path. Both the S-II and the S-IVB burn mode signals cause the removal of cant voltage from the servo amplifiers. The redundant operation is used to improve reliability.

S-IU-503 Data Sheet

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Flight Control Computer, Schematic Diagram (Sheet 4) - S-IU-503 Modification

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Figure 503-8. S-IVB Burn Mode, Functional Block Diagram - S-IU-503 Modification

S-IU-503 Data Sheet

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Figure 503-9. S-IVB Coast Mode, Functional Block Diagram - S-IU-503 Modification

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IBM AG

CIRCUIT DESCRIPTION

The triple-redundant ϕ roll signals are applied to the rate gyro filtering circuits in dc amplifier scaling boards J35, J50, and J51. The circuitry within these scaling boards is identical; therefore, only J50, which processes the ϕ roll reference channel, is discussed.

The ϕ roll reference signal is applied to pins 4 and 2 of J50. The signal is coupled through R1,

R5 and R4, R6 to pins 3 and B, the filter output. The ϕ roll reference signal is amplified by the associated DC amplifier, and the amplified signal is applied back to pins C and D of the scaling board. (The signal is inverted in the dc amplifier so that the feedback is degenerative.) Within the scaling board, the feedback signal is coupled through R2 and R3 to summing points between R1, R5 and R4, R6. The circuit capacitances shunt the input lines (C1) and the feedback lines (C2, C3 and C10, C11) in order to reduce the higher frequency components of the ϕ roll signal. (The 18 Hz component is high compared to the ϕ roll control frequencies, which are less than 1 Hz).

Figure 503-10. Rate Gyro Filtering for $\dot{\phi}$ Roll S-IVB Channels

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IBM AG

CIRCUIT DESCRIPTION

The ϕ yaw signals are applied to pins 3 and 4, C and D, and 5 and E. Since these inputs lead to identical circuitry (except for reference designators), only the ϕ yaw reference channel will be discussed.

The ϕ yaw reference signal is coupled from pins 5 and E, through R19 and R23 to pins M and 13, the scaling board output. The signal is then amplified and inverted by the associated dc amplifier, and the amplified signal is coupled back to pins N and P of the scaling board as a degenerative feedback. Within the scaling board, mode switching relays K3 and K6 couple the feedback signal through R24 and R17 to summing points at the scaling board inputs. Circuit capacitances C13 through C18 couple more of the feedback for high frequencies into the scaling board output, thus eliminating the undesirable effects of the 18 Hz component. The back-to-back zener diodes, CR9 and CR10, between the scaling board output pins, M and 13, protect the dc amplifier input stage from any transient pulses greater than approximately 5 volts; a transient pulse of 6 volts could damage the dc amplifier.

Figure 503-12. Scaling Board A and Associated DC Amplifiers

503-16

Figure

503-13.

Scaling

Board

В

and

OP STANDBY S-IVB COAST INPUT OP ACTIVE S-IVB COAST INPUT **ØP REFERENCE S-IVB COAST INPUT** ΔφR S-IC/S-II INPUT ΔΦP S-IC/S-II INPUT $\Delta \phi \mathbf{Y}$ S-IC/S-II INPUT S-IC/S-II S-IVB 28 VDC BURN BURN MODE +28 VDC RET MODE ŤΕ ŶD 5 12 14 C Î9 î II 3 6 8 B A z 4 CRI CR2 R8 250K 15W ±1% 15W±1 RI2 RI3 RI5 **500K** 15W 15W ±1% ±1% **500K** 1250K RI6 250K RI7 250K 15W±.1% RI9 R20 R22 47K 500K 500K 15W 15W ±1% ±1% R24 250K R23 47K .15W±.1% ±1% ±1%)R25 C4 C16 CI CIO C13 C7 R26 10K 0.1UF 0.IUF O.IUF 0.1UF 0.1UF 0. IUF 100V 1000 C2IF CI4 C17, C5,1 C816 CIL Da 0. IUF O.IUF O.IUF 0. ÎUF 0.1UF 0. IUF 2N910 1000 100V CR9 CRT CR5 CR3 7 RI4 500K KI RIO 500K 15₩ ±1% R21 RI8 C31 R2 LC6 1.001UF 0R6 500K 15W ±1% .00IUF 1.001UF .00IUF 500K 500K 500K T.OOIUF 15W K2 ±1% К3 Raz TK6 K6 K6 2N2034 K4] CR8 K5] K5 K6 K3 K5. KA KI K4 K5] CRG K4 CRIO K2 K3 K3 K3 KI K2)R31 TK2 K2 R32 IOK. CR4 PN91 SCALING BOARD B J118 N M 13 P 21/2 10 K G н F 7 J 4 5 4 4 5 5 DC AMPLIFIER DC AMPLIFIER DC AMPLIFIER $\Delta \phi$ ROLL S-IC/ $\Delta \phi$ PITCH S-IC/ $\Delta \phi \, \text{YAW S-IC}/$ NOTE: S-II BUFFER S-II BUFFER S-II BUFFER **ØPITCH S-IVB ØPITCH S-IVB** Ø PITCH S-IVB ZENER DIODES CR5 THROUGH COAST "C" COAST "B" COAST "A" CR10 ARE S1N749A. AMPL J115 AMPL J116 AMPL J117 6 7 6 7 CHANGED AREA L IBM S-IVB COAST OUTPUTS THROUGH SWITCHING CIRCUIT A1 TO SPATIAL AMPLIFIERS AG

S-IU-503 Data Sheet Flt Cont Cmptr (500), Sect.

VI

Associated DC Amplifiers

Added 1 August 1968

Anomist 1968

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CIRCUIT DESCRIPTION

Since the yaw, pitch, and roll channels are identical (except for reference designators) only the vaw channel is discussed. The $\Delta \phi$ yaw attitude error signal is applied from Switching Circuit A2 to pins 5 and 7 of the scaling board. The signal is coupled through R7 and R8 to pins 6 and E, the scaling board output. The signal is then applied to an associated dc amplifier where it is amplified, inverted, and coupled back to the scaling board as a degenerative feedback. The feedback is applied to pins F and G of the scaling board. Under IU guidance control, the feedback is applied directly to R6, C3 and R9, C4, and through normally-closed contacts of K1 to R5, R10. The negative feedback signal is coupled through the parallel RC networks and is summed with the $\Delta \phi$ yaw signal at the scaling board output, reducing the input to the dc amplifier and decreasing the gain of the ${\Delta \varphi}$

yaw channel. Under spacecraft guidance control, the spacecraft control signal is applied to pin P of the scaling board and is coupled through CR1 and the voltage divider of R23 and R24 to the 28 Vdc return at pin A. At the junction of R23 and R24, a positive voltage is developed which is applied to the base of transistor Q1, part of a Darlington-connected relay driver. Transistor Q1 is turned ON by the positive voltage applied to its base, and its emitter current drives transistor Q2. When Q1 and Q2 are turned ON, their collector current is drawn from the 28-volt source at pin 1 of the scaling board through relays K1, K2, and K3, causing these relays to energize. When K1 energizes, it opens its normally-closed contacts in series with R5 and R10 in the $\Delta \phi$ yaw feedback network, removing these resistors from the circuit. The removal of R5 and R10 decreases the amplitude of the feedback signal, and less degeneration occurs in the $\Delta \phi$ yaw channel. Thus, the channel gain is increased during the time of spacecraft control.

Figure 503-14. Spacecraft Control Gain Switching Capability

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THE CONTENTS OF THE PRECEDING SECTIONS OF THIS MANUAL APPLY TO THE VEHICLE SPECIFIED ON THESE DATA SHEETS EXCEPT FOR THE FOLLOWING DIFFERENCES

The Switching Control Circuit (J132 in S-IU-504, J129 in S-IU-503) in the S-IU-504 Flight Control Computer has been modified to accept a new method for latching the Flight Control Computer into the S-IC burn mode. Figures 504-1, 504-2, and 504-3 show the circuit changes made by the modification. The complete switching circuit functional block diagram is shown in Figure 2-40, and the complete switching circuit schematic diagram is shown on Figure 2-44 sheet 6. The complete switching circuit control schematic diagram is shown in Figure 2-57.

The purpose of the S-IU-504 Switching Control Modification is to prevent the possibility of overloading the S-IC Burn Mode Substitute Signal from the GSE or the First Motion Signal from the Switch Selec-

tor (when either is present at J132-34 and J132-33) by conduction through J24-28 and J24-30 of Switching Circuit "C" to the +28 Vdc bus, thus holding all the S-IC mode relays energized when the IU +28 Vdc supply is removed from the Flight Control Computer. The S-IC Test Signal from the GSE is also protected from a similar overload.

Because of variations in vehicle flights the filters may change from vehicle to vehicle; therefore, the filter information for each vehicle is located in the Data Sheets.

Filters (S-IU-504) which DO NOT CHANGE from previous configurations are listed below, and the figures indicated are located in preceding Data Sheets. Refer to the specified figure for a technical description and an electrical schematic of the filter.

S-IU-504 Filter	Figure No.
$\Delta \phi \mathbf{Y} \text{ and } \Delta \phi \mathbf{P} \mathbf{S-IC}$	501-1
$\Delta \phi \mathbf{Y} \text{ and } \Delta \phi \mathbf{P} \mathbf{S-II}$	501-2
$\Delta \phi \mathbf{Y} \text{ and } \Delta \phi \mathbf{P} \mathbf{S}$ -IVB	503-1
$\Delta \phi R S-IC$	501-4
$\Delta \phi $ R S-II	501-5
ϕ Y and ϕ P S-IC	501-6
ϕ Y and ϕ P S-II	503-2
ϕ Y and ϕ P S-IVB	503-3
φ̈́R S-IC	503-4
φ̈́R S-II	501-10

The S-IC cant circuit has been added to the S-IU-504 Flight Control Computer. See change number 3 in the S-IU-503 Data Sheets for details of the change.

The rate gyro filtering circuits have been added to the S-IU-504 Flight Control Computer. See change number 4 in the S-IU-503 Data Sheets for details of the change.

5 The spacecraft attitude control gain-switching capability has been added to the S-IU-504 Flight Control Computer. See change number 5 in the S-IU-503 Data Sheets for details of the change.

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Figure 504-1. Switching Circuit, Functional Block Diagram - S-IU-504 Modification

Changed 1 August 1968

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Figure 504-3. Switching Control, Schematic Diagram - S-IU-504 Modification