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D. Vankovich

THE 'BRAID' TRANSFORMER MEMORY by

INSTITUTE OF TECHNOLOGY

MASSACHUSETTS

GUIDANCE

R. L. Alonso W. H. Aldrich September 1965





GUIDANCE AND NAVIGATION

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R-498 THE 'BRAID' TRANSFORMER MEMORY

ABSTRACT

This report describes a read-only digital computer memory which utilizes a loom to "braid" information into a wire harness. The memory is called a braid memory and is a variation on the type of transformer memory first described by T. L. Dimond. Such memories are useful when permanence of information is desirable.

Braids for the memory described in this report were made at the rate of 2¹⁵ bits/hour including connections. The use of a loom makes braid manufacture both a fast and an economical process.

A number of trade-offs between speed, capacity, and component count exist; hence, braid memories with many different characteristics can be made. The memory described in this report has a capacity of 16,384 words of 16 bits each. Its semiconductor count is 194 transistors, 244 integrated logic gates, and 1024 diodes. It also employs 256 ferrite transformer cores. The memory has a cycle time of $2 \mu s$ and consumes less than 3.5 watts of power.

by R.L. Alonso W. H. Aldrich September 1965

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I. INTRODUCTION

1.1 Prior Work

Transformer memories are read-only memories (ROM) which make use of magnetic coupling, linear or non-linear, between a set of interrogation lines and a set of sense lines. Modern interest in transformer memories dates back to (at least) Dimond's article [1]. Further background in ROM technology is available in Taub's review [2]. The appeal of such memories is based on the permanence of the information, which is of advantage in control systems, and on the intuitive feeling that it should be possible to build large (about 10^6 bits), fast (about 1μ sec cycle time), fixed memories at a cost substantially below that of equivalent core storage. Such a memory must be inexpensive indeed to compete with the rapidly dropping cost of core storage. Transformer memories have a further advantage in size because they can be made very compact. System densities of about 1000 bits/in³ have been realized with another type of transformer memory [14] and would be a factor in a number of circumstances.

In this paper we present a particular variant of the transformer memory, which we call "braid" and which exploits weaving with a loom as a means of manufacture, thereby giving some substance to the intuitive feelings that a transformer memory should be cheap to make. The experimental system, although short of the size and speed stated above, is large enough to give confidence in the practicality of this type of read-only memory.

1.2 Transformer Memory Principles

The particular type of transformer memory dealt with here uses linear transformer material (as opposed to non-linear magnetic cores, [7], [10]), and is sometimes called a Dimond switch [1] [4] [5] [6] [11]. The transformer cores are shown in Figure 1-1 as heavy vertical lines (Karnaugh mirror notation, [12]); the presence and polarity of the winding through the transformer is shown by the direction of the slash mark which intersects the core and wire.

A transformer memory consits of an array of transformer cores threaded by a number of word lines. The word lines either thread or bypass each transformer so that, when a particular word line is pulsed, energy is transferred to the appropriate secondaries (called sense windings). Each bit of information is stored in the topological fact of a word line either threading or not threading a transformer. In Figure 1-1, for example, word lines thread cores as marked by the slash marks. Word line 1 threads cores 1, 3, ..., K, and bypasses 2; word line N threads 1, 3, bypasses 2, K. The



Fig. 1-1 Basic Transformer Memory

name "word line" is derived from the fact that pulsing such a line causes an entire word of K bits to be read out, with "ones" (i.e., e.m.f. at the sense windings) appearing at threaded cores and "zeros" (i.e., no e.m.f. at the sense windings) elsewhere.

The cores may be toroidal and provide a closed path for the flux, as in [4], [11] and [13], and the memory described in this article, or they may be just rods of magnetic material as in [5], [6], [9]. The reasons for and against each choice will be discussed in a later section. Figure 1-2 shows an exploded view of a section of the memory.



Fig. 1-2 Braid Transformer Memory Construction

The aggregate of all the word lines is called a braid. The electrical properties and design problems of the braid memory are determined in large part by the method of construction. The word lines are thin wires (as in [5], but as opposed to [6], [11], which use a thin Mylar sheet with a conductor deposited on it). The word lines form a tight bundle of 2^{10} wires (figure 1-3).



Fig. 1-3 1000 Wire Braid

1.3 Method of Braid Construction

The braid can be made with a loom. Shown in Figure 1-4 is a side view of the process. Each wire passes through a feeder which can be moved up or down. Steps in the process consist of selecting the proper wires, separating them with a shuttle-like temporary separator, and forming the (square) braid. Termination of the wires to proper terminals is an important phase of construction which is also done with the aid of the loom (see section III). Making the braid in this way results in "writing speeds" of as many bits per pick as there are wires in the loom. A 64-wire loom has been made and operated, and a 1024-wire loom is under development.



Fig. 1-4 Principle of Braid Construction

II. EXPERIMENTAL BRAID MEMORY SYSTEM

2.1 System Description

The experimental system is a fixed memory of about 16,000 words of 16 bits each (2¹⁸ bits). A summary of its characteristics is shown in Table 2-1. The memory, including its sensing and inhibiting circuits (but not its drivers) is shown in Figure 2-1. Figure 2-2 shows a close-up where the core caps which close the flux path have been removed from the cores, as well as a section of the 1024 wire braid. The uncapped U-shaped cores are shown threading the 30-turn sense winding.

The braid lines are selected by means of a 32 x 32 selection matrix. There is additional circuitry, described below, which can be used to inhibit the output of all but a single group of 16 cores. Since there are 256 cores threaded by the word lines, and since the desired output is a 16-bit word, selection of a word also implies selection of one out of 16 groups (of 16 cores each), which is left uninhibited. The inhibiting and sensing elements are commercially available integrated circuits (RTL NOR gates); Figure 2-3 shows the arrangement for combining the output of 16 cores, only one of which is uninhibited. Inhibition is accomplished by shorting the sense winding with a transistor. It was convenient in our case to use integrated circuits for this function; the collector resistor of these units, which would normally be connected to +3V, was connected to ground thereby providing a low impedance across the sense winding. Figure 2-4 shows an inhibit position, i.e., all those cores which share a single inhibiting signal.

Other inhibiting schemes were also tried. One system suppressed the output of cores by passing a current (through groups of 16 cores) so as to oppose any word-line current that might flow. The core outputs were then a positive pulse for a "one", and either no pulse or a negative pulse for a "zero", depending on the possible combinations of inhibiting and word-line currents. This system proved very noisy because of the loop currents it generated.

A third inhibiting system used a diode switch instead of a transistor to inhibit cores. This system was also not as satisfactory as the transistor inhibiting system described above.

The overall arrangement of the 256 cores is shown in stylized form in Figure 2-5. The address field is interpreted as follows:

Bits 1 - 4	Inhibit group selection
Bits 5 - 9	Transmitter selection
Bits 10 - 14	Receiver selection.



Fig. 2-1 Experimental Braid Memory System







Fig. 2-3 Single Bit Position Showing Inhibiting Circuits IHO through IH15 are inhibiting signals. At next one of these is "zero" at any given time.



Fig. 2-4 Single Inhibit Position

IH15 Drives 16 Inhibiting Gates



Fig. 2-5 Overall Memory Organization

The word-line selection system follows a more or less conventional double-ended system, as shown in Figure 2-6.

The receivers are somewhat different from those often used in a coincident current system in that they connect the receiver bundle (i.e., the common point of 32 word lines at that end) either to ground, when the receiver is selected, or to +E (Figure 2-7a). The transmitter switches are shown in Figure 2-7b. In series with the transmitter switches is a common current limiter (Figure 2-7c), which is used to regulate the rise time and final amplitude of the input current pulse.

Capacity	16,384 words of 16 bits each (2^{18} bits)
Word lines	1024
Diodes	1024
U cores	256
Sensing gates	96 cans (3-input NOR gates)
Inhibiting gates	128 cans (Dual 2-input NOR gates)
Receiver switches	32
Transmitter switches	32
Access time	$1 \ \mu \ \text{sec}$
Cycle time	2 µsec
Sensing turns	30 T
Power consumption	< 3.5 W (calculated)
Power supplies	+ 10 V + 25 V + 3 V

Table 2-1. Summary of Braid Memory Characteristics

2.2 System Performance

In order to discuss the electrical performance of the braid it is necessary to define a number of currents and locations within the braid. The basic definitions are shown in Figure 2-8. The variable x identifies a location along the braid, by core number. For our experimental system x = 0 identifies the first core and hence the beginning of the braid. The middle of the braid corresponds to x = 127, and the end of the braid, where the currents exit, corresponds to x = 255. The definitions are:

- I_d : current delivered by the regulated driver; not a function of x.
- $I_t(x)$: total current along the braid. $I_t(x)$ is not the same everywhere along the braid because of stray capacitances to ground.
- $I_1(x)$: current along the selected line. Ideally, $I_1(x) = I_d$.
- $I_0(x)$: current along all other wires of the braid. $|I_0(x)| > 0$ in our experimental system because of loop and shunt currents. $I_t(x) = I_1(x) + I_0(x)$.



Fig. 2-6 Double Ended Selection System



Fig. 2-7a Receiver Circuit



Fig. 2-7b Transmitter Circuit



Fig. 2-7c Current Limiter



Definitions of: $I_1(x)$, $I_o(x)$, $I_e(x)$, $I_e(x)$, $I_t(x)$, V, (x). x is the core position number along the braid. True: $I_t(x) = I_e(x) + I_e(x) = I_1(x) + I_o(x)$.

Fig. 2-8 Definitions of Currents and Voltages within Braid

- $I_{e}(x)$: total current through the xth core.
- $I_{o}(x)$: total current bypassing the xth core.

 $I_{e}(x) + I_{e}(x) = I_{t}(x).$

- I_r: current emerging from the braid along the 32 lines which share a common receiver circuit. When that receiver is active, i.e., when it is selected, the I_r includes I₁ (255).
- V_s(x): voltage appearing across the loaded 30-turn sensing winding of core x, i.e., core output voltage.
- $V_1(x)$: voltage along the selected line, to ground. $V_1(x) V_1(x+1)$ is the drop per core.
- $V_1(255)$: voltage at the selected receiver.
- $V_r(x)$: average voltage of all those lines which share a common receiver, except $V_1(x)$.
- $V_0(x)$: average voltage along all those lines which do not share a common receiver.

As a practical matter, V_1 , V_r , and V_0 are measured only at x = 0 and x = 255. $V_s(x)$ can be measured at each core.

The braid used in the experimental system was made from an existing 16,384word program (for the Apollo guidance computer), and thus it is considered typical, meaning really that there are no glaring pathological information patterns. The braid is identified in this report as "information braid J" to distinguish it from two other braids (Y and S) which were made for investigating certain noise generating processes. All three braids are described in some detail in Appendix A.

The performance of the braid and its associated electronics can be discussed in terms of the various currents defined above. The ratio $I_1(x)/I_0(x)$ is a good measure of signal to noise, and also a measure of how the braid length affects performance. The ratio is not only a function of x, but a function of time. Unfortunately, the complicated nature of the braid makes simple and rigorous analysis of these currents difficult, and for that reason this section will be primarily descriptive, leaving analyses for the appendices.

Figure 2-9 shows I_r during the entire memory cycle. The first peak of nearly 200 mA occurs during the .5 μ sec following the turn-on of the receivers before the transmitters and drivers are turned on, and it represents the discharging of 32 lines associated with the selected receiver (called a receiver bundle). The word lines are all at +E initially. The capacity of 32 lines to all other lines is about $6300 \,\mu\mu$ f in the present instance. (This and other physical facts are listed in Table A-1 of Appendix A.) The



Fig. 2-9 Receiver Currents, Address 22522 $(I_r (255); 0.5 \mu \text{sec/div}; 50 \text{ mA/div.})$



Fig. 2-10 Envelopes of V_s (x). 0.2 μ sec/div; 5/div (Top: V_s (1) Bottom: V_s (238)

drive current $I_1(255)$ is the second peak (150 mA); I_1 must not be started until the initial discharge current has decreased sufficiently. The negative current spike shows the recharging of the receiver bundle, when the bundle is disconnected from ground and connected to +E. Appendix D treats the particulars of currents induced during receiver switching.

The cycle shown in Figure 2-9 is an isolated cycle, with the next cycle some time away. For fast operation the discharging of one receiver bundle can overlap the recharging of another one, if the second address uses a different receiver from the first address. It is nevertheless evident that the double-ended selection increases both access and cycle times, and that a selection system which uses a switch per word line could be much faster.

The range of core outputs can be seen in Figure 2-10. The top trace shows $V_s(1)$, where V_s is the voltage appearing across the input to the sense amplifier. The noise preceding the "one" or "zero" output is due to receiver discharge (or charge) currents. The noise during signal time is the superposition of shunt and loop currents, and the ringing currents set up by receiver switching. The bottom trace shows $V_s(238)$. The signal and noise levels, although still usable, are somewhat worse than earlier in the braid. The degradation of signal to noise, $I_1(x)/I_0(x)$, due to shunt and loop currents, which are due to capacitance between word lines, Appendix B discusses loop currents, which are due to magnetic coupling between lines and inter-line capacitance. Both shunt and loop currents can result in noise (undesired $V_s(x)$), and the possible size and speed of a braid memory system is strongly influenced by those currents.

The core outputs $V_g(x)$ are a fairly good measure of the currents $I_e(x)$, if one takes into account the nonlinearity introduced by the sensing gate. The matter is dicussed in Appendix E.

An overall view of the memory operation is shown in Figure 2-11. The top trace is the drive current I_d , inverted. The second trace is $V_s(x)$ for x in the first half of the braid, over a large number of addresses. The third trace shows the envelope of sense amplifier outputs, before strobing. The fourth trace shows the strobing signal. In trace 2, the second set of V_s outputs does not appear because of the consecutive address scanning employed. The core inhibit signals are functions of the low order bits of the address; consequently, if a core is addressed one time without inhibiting it will be inhibited for the next fifteen cycles, assuming a normal progression of addresses. The associated sense amplifier shows outputs at that time because it also receives inputs from fifteen other cores, one of which will be uninhibited.

The currents $I_e(x)$ are shown in Figure 2-12 for x = 31 and x = 238 both with and without receiver switching. Charging and discharging of receiver bundles causes ringing currents which are superimposed onto the drive current. The envelop of currents $I_e(x)$



Fig. 2-ll Overall Memory Operation 0.5 $\mu \sec/div$.



Fig. 2-12a I_e (31) Address 142XX; 50 mA/div; 0.2 μ sec/div. No Receiver Switching.



Fig. 2-l2b $~I_{\rm e}$ (31); 0.2 $\mu \rm sec/div;$ 50 mA/div. Receiver Switching



Fig. 2-12c, d I_e (233) 0.2 µsec/div; 50 mA/div. Address 243XX - No Inhibits or Sensing Top: Receiver Switching Bottom: Receiver not Switching



Fig. 2-12e I_e (238) 0.2 μsec/div; 50 mA/div. No Inhibits or Sensing. No Receiver Switching



Fig. 2-12f I $_{\rm e}$ (238) 0.2 μ sec/div; 50 mA/div. No Inhibits or Sensing. Receiver Switching

generated with no receiver switching (Figure 2-12a, c, e) is obtained by interrogating all those word lines which share a receiver. Note the similarity between I_e(x) and $V_s(x)$. Figure 2-12d shows a case where loop currents aid I₁ (i.e., makes the "zeros" larger), and Figure 2-12e shows a case where the loop currents oppose I₁; either case is possible. In one system the lowest observed ration of I_1/I_0 is approximately 10:1, for braid J at peak signal time.

The loop currents discussed in Appendix C get potentially worse as the number of wires increases. In the present case, and for the present dimensions of the braid, the 1024-wire braid provides moderate loop currents (about one-tenth of the word-line currents, at worst), indicating that these would not have been observed for a few hundred wires, and that they are possibly overwhelming for four to eight thousand wires and up. Again, the physical length of the braid has a direct effect on the size of these currents.

The speed penalty incurred by using the double-ended selection system is directly dependent on the capacitance between a receiver bundle and the rest of the braid. A physically smaller braid, or one with fewer cores, or fewer wires in each receiver bundle will all result in smaller receiver discharge currents. For a high-speed system, however, it seems clear that a switch per line is preferable. Such a system may not be as prohibitive as it first appears because the cost of some transistors is now comparable to the cost of word-line diodes.

2.3 Design Conclusion

There are several conclusions to be drawn from our experience. The most important of these is that the design should endeavor to minimize the voltage drop along a word line. To do this it is first necessary to keep the area enclosed by the word lines as small as possible by having the receiver bundles (or their continuation) return along the braid, thereby reducing the word-line's self inductance. Second, the sensing circuit of each core should have a very low input impedance, which, when reflected back to the primary, will result in a very small voltage drop for each core (we have found it useful to think of cores as current transformers, rather than voltage transformers). Our choice of a logic gate as sensing element put certain limitations on the maximum number of secondary turns for a given word-line current because of the need to provide both a threshold voltage and a minimum current for the sensing gate (Appendix E). Clearly, a more elaborate sensing circuit can be made if even lower secondary impedances are desired.

A clear additional conclusion is that the physical size of the braid, i.e., its length, should be kept to a minimum for a given number of cores.

An interesting question raised by the efforts of Butcher [5] and Pick et al [6][9] is the relative superiority of closed versus open magnetic paths for the "core." Butcher in particular reported first trying the closed flux path method, and abandoning it in favor of rods because of the mechanical problems involved in closing the flux path [16]. The

rod scheme seems to us to cause electrical problems in place of the mechanical ones it solves because of the relatively lower ratio of core (or rod) flux to air flux.

A relatively surprising finding was that the capacitance shunt currents, which were studied in detail by Kington and Taub [11] for a multilayered conductor transformer memory, were relatively small for the multiwire braid and not as important as loop currents. These shunt currents are essentially proportional to the drop along a word line and to the capacitance from one wire to the rest of the braid (Appendix B); this last capacitance was apparently much higher for Kington and Taub (89 pf per core) than for the braid (about 2 pf per core), possibly for reasons of the physical dimensions of the two systems. There is clearly much to be gained by making the system physically small.

III. BRAID MANUFACTURE

The economic potential of the braid memory is dependent on the ease with which braids can be made. Interest in the electrical properties of the braid followed, rather than preceded, what seemed like good ideas for manufacturing. The original suggestion to use a loom was made by W. Bard Turner, a member of this laboratory. Those manufacturing ideas, developed by Turner and others (see the acknowledgements) are now at the point where they bear describing.

The working braids manufactured to date have been made on 64-wire looms. Braid J was made with the device shown in Figure 3-1, a primitive affair which used toy motors to operate the individual wire picks. Sixteen separate braids of 64-wires grouped into two braids of 512 wires each (see Appendix A).

A second 64-wire loom was built to test certain mechanical selection techniques. The end product of that loom is also a 64-wire braid (Figure 3-2) where the wires are terminated individually at one end, and in two bundles of 32 wires at the other end. This second loom can be seen in Figure 3-3. The mechanism for selecting the individual lines is at the top of the picture. The work area, where the separators are inserted, can be seen at the far end of the table. The selection mechanism is solenoid operated (Figure 3-4), and uses a system of coincident holes for selecting the dropping rods. Details of the mechanism can be seen in Figures 3-5 and 3-6. The 64 vertical rods are initially set in the up position. The tape control mechanism then steps along, allowing selected rods to fall by providing coincident holes at both rows and columns. The wire separator (Figure 3-7) is inserted when all the wires have been selected.

The 64-wire system described in these pictures can step along doing four picks per minute. The overall manufacturing speed, including terminations and continuity testing, is one 64-wire section of 256 holes (2^{16} bits) every two hours. Terminations are greatly aided by the inherent identifying process; the tape which controls the selection of wires has an initial section in which the wires are selected in a sequence which corresponds to the sequence of terminals on the connector. Thus there is no need to tag wires individually, and only the 64-wire braid as a whole need be tagged. The braid shown in Figure 3-8, which contains 2^{18} bits, was made by the above process; it is similar to Braid J in that it was made from a typical computer program.

A third loom system, under development, will pick 2¹⁰ wires at a time. The loom uses a Jacquard lift mechanism, which is a 160-year-old system in which punched cards

were first used (Figure 3-9). In a standard Jacquard system the choice of thread is controlled by a punched card "read" by a device at the upper right-hand part of the lift. We are presently developing a tape-controlled equivalent of the punched card which will permit arbitrary selection of wires.

A 2^{10} wire braid is not as simple to handle mechanically as a 2^6 wire braid in that a fairly elaborate procedure must be followed to provide proper separation of "ones" and "zeros". The prize, however, seems well worth the effort since such a loom will be capable of producing well over 2^{20} bits per 8 hours, or from four to ten times more than our present 64-wire loom.



Fig. 3-1 Original 64-Wire Loom



Fig. 3-2 64-Wire Braid Section



Fig. 3-3 64-Wire, Coincident Hole Loom



Fig. 3-4 Selection Mechanism of 64-Wire Loom



Fig. 3-5 Closeup of Selection Mechanism



Fig. 3-6 Lift Mechanism in Place Over Selection System for 64-Wire Loom



Fig. 3-7 Insertion of Separators Between Selected and Unselected Wires



Fig. 3-8 Jacquard Loom for Simultaneous Handling of 2^{10} Wires

APPENDIX A

BRAID CHARACTERISTICS

Three different braids were constructed for breadboard tests. Two of them, the straight braid, "S", and the forked braid, "Y", were made to study certain noise mechanisms. Braid "J" was made to contain actual binary information and was operated in a breadboard of the entire memory system. The important characteristics of the braids are summarized in the following tables.

Table A-1

Braid J Characteristics

Construction:

Two 512-wire braids on separate sets of bobbins, ground returns bundled on "zero" side (see also Figure 2-2).



Fig. A-1 Cross Section

Wire Size:

Word lines #38 (nylon, polyurethane insulation, O.D. = 0.140 mm); Gnd returns #36 (nylon, polyurethane insulation, O.D. = 0.178 mm)

Braid Length: 2.85 meters

Measured $C_{512-512}$: .0087 μ f (Top half to bottom half)

.017 μ f (1st and 3rd quarters to 2nd and 4th)

Measured C_{1-Braid}: 440 pf mean (low 410 pf, high 465 pf)

Measured $C_{32-Braid}$: .0063 μ f mean (low .0049 μ f, high .0075 μ f)

Calculated L_{32-Braid}: 3.32 μ mean (low 2.16 μ h, high 5.17 μ h)

Calculated $L_{1-Braid}$ all "ones": 5.62 μ h in free air, 12.46 μ h in array

Calculated L_{1-Braid} 15/16 "zeros": 4.25 μ h in free air, 5.28 μ h in array

Measured L_{1-Braid} all "ones": $\sim 14 \ \mu h$ in array

Measured L_{1-Braid} 15/16 "zeros": ~7 μ h in array

Table A-2

Braid S Characteristics

Type Construction:	Straight bundle 1024 wires
Wire Size:	#36 (nylon, polyurethane insulation, O.D. = 0.178 mm)
Braid Length:	2.74 meters
Measured C ₅₁₂₋₅₁₂ :	0.069 µf
Measured C ₁ -Braid:	450 pf
Measured C _{32-Braid} :	0.018 µf
Calculated L ₃₂ -Braid	1.85 µh
Calculated L ₁ -Braid	4.2 μ h mean

Table A-3

Braid Y Characteristics

Construction:

Straight bundle, 1056 lines





Wire Size:

#38 (nylon polyurethane insulation, O.D. = 0.14 mm)

Measured $C_{512-512}$: 0.026 μf

Calculated L₅₁₂₋₅₁₂:

1.10 μh (calculated from dimensions for forked position. See Appendix C.)

APPENDIX B

NOISE DUE TO SHUNT CURRENTS

Each word line has capacitance to the unselected wires of the braid. All unselected lines are at a-c ground because the receiver circuits connect the receiver bundles to either +E or to ground, through a saturated transistor (Figure 2-7a). When a current pulse passes down the selected line some of the current is capacitively shunted to unselected wires because of the self-inductance of the selected line as shown below.



Fig. B-1 Shunt Current Noise Mechanism

In reality, the inductance and capacitance are functions of the geometry of the selected line and hence the information in the memory. If the line threads a core it will have high inductance at that position because it is then farther from its return path and because coupling between the line and core secondary is not perfect. If, on the other hand, the line does not thread a core its inductance will be lower, but not negligible, and the capacitance will be higher. The worst case, that is, for maximum $[I_1(0) - I_1(255)]$, occurs when the line threads as many cores as possible, the line being nearly uniform.

Potentially, all of the current $[I_1(0) - I_1(255)]$ may flow through an uninhibited core not threaded by the selected line and thus produce noise. Consequently, we are interested in placing an upper bound on this current. Kington and Taub (11) have derived a solution for a worst-case pattern of information for their system, which differs somewhat from the braid system. This appendix gives an approximate solution for the shunt current in the interest of producing both a worst-case upper bound and a simple model to aid understanding.

The upper-bound calculation is based on two assumptions which lead to a larger shunt current than that which actually occurs. The first assumption is that the unselected lines in the bundle remain at ground potential along their entire length, thus neglecting mutual inductive coupling. The second assumption is that the voltage at any given time is a linear function of x as shown below.



Fig. B-2 V_1 as a Function of x and t

This is a conservative assumption because in reality the voltage of a constantfrequency sine wave will decrease exponentially with distance on a uniform line. If we imagine the voltages on the line to have a spectrum such that all components are attenuated at nearly the same rate (i.e., the line is distortionless for the signals involved) then the actual $V_1(x, t)$ will be less than that given by:

$$V_1(x, t) = V_1(0, t) - \left[\frac{V_1(0, t) - V_1(m, t)}{m}\right] x.$$

Letting C be the total shunt capacitance of the line, the current, ${\rm i}_{_{\rm S}}$, through C is less than i, where:

$$i_s = I_1(0) - I_1(255)$$
,

$$i = \int_{0}^{m} \frac{C}{m} \frac{\partial}{\partial t} \left[V_{1}(0, t) - \frac{V_{1}(0, t) - V_{1}(m, t)}{m} \right] dx ,$$

$$i = \frac{1}{2} C \dot{V}_1(0, t) + \frac{1}{2} C \dot{V}_1(m, t)$$

where

$$\dot{V}_1(x, t) = \frac{\partial}{\partial t} V_1(x, t).$$

A more convenient form is:

$$i = \frac{1}{2} C [\dot{V}_{1}(0, t) - \dot{V}_{1}(m, t)] + C \dot{V}_{1}(m, t)$$
$$i = \frac{1}{2} C L_{11} \ddot{I}_{1}(m, t) + C \dot{V}_{1}(m, t).$$

 L_{11} is the total line self inductance and I_1 is the current which passes through that inductance and is measured as $I_1(255)$.

The toal shunt current has been observed in two breadboard systems, braids S and J. For the shunt-current experiment, with braid S, all lines are grounded at the far end and the current through the driven line is compared with the current in all the other lines which are open-circuited at the drive end and which carry i. In this case, $V_1(m, t)$ equals zero, hence,

$$i = \frac{1}{2} L_{11} C \ddot{I}_{1} (m, t).$$

Figures B-3 and B-4 compare \mathbf{i}_{s} and \mathbf{I}_{1} for braid S with two different rise times for I.

In the top picture, the equation gives a calculated peak value of 49.14 ma for i. In the second picture the first peak of i is calculated to be 10.6 ma. As can be seem from the figures, these values are too high by about fifty percent of the actual values.

Figure B-5 shows the same measurement for the information braid, "J". Using the measured values in Appendix A for $L_{1-Braid}$ and $C_{1-Braid}$, we calculate i to be between 22.6 and 13.5 ma. at peak value when I first starts from zero. The measured peak is approximately 5 ma.

A more accurate expression for the current i can be written if the effect of mutual coupling is taken into account. The assumptions that the voltage on the unselected portion of the braid varies linearly with x and is due only to mutual coupling lead to the expression:

$$i = \frac{1}{2} (L_{11} - L_{21}) C \ddot{I}_1 (m, t) + C \dot{V}_1 (m, t),$$

where L_{21} is the mutual inductance between the selected line and the unselected bundle.

The value of L_{21} appears in Appendix C and its use for the case illustrated in Figure B-5 gives maximum calculated value for i to lie between 14.9 and 9.6 ma. In both cases, the waveforms agree in form with those observed. This is most apparent in Figures B-3 and B-4.



Fig. B-3 Comparison of Shunt Current, i_s, and Word Line Current.







Fig. B-5 Comparison of Shunt Current, i, and Word Line Current for Braid J

APPENDIX C

NOISE DUE TO LOOP CURRENTS

The loop-current noise mechanism arises because there is mutual inductance between the driven line and the remainder of the braid and because the capacitance from one section of the braid to another may cause a closed loop which can carry current. The worst case is illustrated below.



Fig. C-1

The magnitude and frequency of the loop currents can be calculated for the worst case once the parameters are known. Given the dimensions of the loop portion of the braid, the self and mutual inductances may be calculated by assuming that current is evenly distributed in the bundle and that the volume surrounding the braid is magnetically isotropic. The latter assumption approaches reality only when the cores are strongly inhibited, thus the solution is only valid during inhibit time and to the extent that the uninhibited cores and leakage flux can be neglected.

If the assumptions are satisfied and m is the length of the loop portion of the braid in meters, we calculate, as in [15], the mutual inductance

$$l_{21} = \frac{\mu m}{2\pi} \ln \left[\frac{D+r}{r} \right]^2$$

Similarly, the self inductance of the braid loop

$$l_{22} = \frac{\mu m}{4\pi} + \frac{\mu m}{\pi} \ln \frac{D}{r}$$

The capacitance, $C_{512-512}$, is the capacitance of half the conductors in the braid to the other half. This value is not a linear extrapolation of the single wire to bundle capacity and its value for the "Y" braid is given in Table A-3.

The equivalent circuit we are interested is in then given by Figure C-2.



Fig. C-2

$$e_{2} = l_{2_{1}} \frac{di_{1}}{dt} - l_{22} \frac{di_{2}}{dt} ;$$

$$e_{2} = \frac{1}{C} \int i_{2} dt, \text{ where } C = C_{512-512} .$$

Letting $i_1 = Mt$, i.e., a ramp with slope M amperes per second, and initial conditions $e_2 = 0$, $i_1 = 0$, $i_2 = 0$, we find

$$l_{2} = \frac{l_{21}}{l_{22}} \quad M \quad \sqrt{l_{22}C} \sin \left(\frac{1}{\sqrt{l_{22}C}} t \right)$$

For the "Y" braid with spacing such that D = 4r, and m = 1.37, we estimate

$$l_{21} = 1.08 \times 10^{-6}$$
 henry,
 $l_{22} = 1.10 \times 10^{-6}$ henry.

With M = 0.31×10^6 ampere second, we calculate that i_2 attains a maximum value of 50.18 ma. The frequency is calculated to be 0.97 mc as long as the ramp continues. The actual circuit response is shown in Figure C-3. The variations in i_2 are due to the fact that a number of memory cycles are superimposed and this involves the selection of different lines. None of these lines follows the worst-case path; their paths are a function of the information and of the wire position in the bundle. Figure C-3 shows a maximum current of 30 ma and a frequency during the "up" ramp of about 0.7 mc.



Fig. C-3 Comparison of Loop Current, i2, and Drive Current.

The effect of i_2 on the output voltage seen by the sense amplifier would be in the direction to decrease the amplitude of "one" outputs if the braid were in the sense shown in Figure C-1. Figure C-4 shows a possible orientation of the braid in which i_2 flows so as to enhance "one" outputs and make "zero" outputs larger than they should be.



Fig. C-4

Figure C-5 shows envelopes of the output voltage $V_s(255)$ for various cases of loop currents. The envelopes of Figure C-5 were obtained first with the information braid "J" only (case b) and then with both braids "J" and "Y" mounted on the core array. Envelopes c, d, and e show the effect upon the normal signals of a loop current which opposes (and thus decreases) both "ones" and uninhibited "zeros" and also the effect of a loop current which increases both "ones" and uninhibited "zeros." (As is discussed in Appendix D the envelopes of V_s are very nearly proportional to envelopes of I_1 .)



- a. Inhibited '0's.
- b. Normal Uninhibited '0's.
- c. Uninhibited '0's, Y Braid as in Fig. II-1.
- d. Uninhibited '0's, Y Braid Inverted in Last Bit Positions (Cores 240-255).
- e. '1' Outputs. Lowest Correspond to Case c, Highest to Case d, and Middle to Case b.

Fig. C-5 Output Voltage, Core 255

APPENDIX D

NOISE DUE TO RECEIVER SWITCH DISCHARGE

The selection of a receiver switch requires the discharge of the capacitance formed by the 32 word-lines, one of which is to be fully selected by sending drive current down it, and the rest of which should carry no current at drive time. Consequently, the discharge transient must be completed before drive time and cannot be started before the start of a cycle. Therefore, rapid operation requires that the discharge be done as fast as possible, the speed being limited by the parameters of the line formed by the half-selected wires and the rest of the braid.

This line can exist in a great number of configurations ($\sim 2^{2^{13}}$) depending on the information in the memory. However, each configuration is not greatly different electrically from others which differ only in a few bit positions. Empirical data on the range of variation found for a braid memory of 2^{18} bits appear in Appendix A, Table A-1. The parameters of interest are $C_{32-Braid}$ and $L_{32-Braid}$. Because we are interested in a reasonably wide range of parameter variation and a simple description of the switching problem, the line is approximated by a lumped L-C model with the receiver switch approximated by a SPDT switch and associated resistors and diodes. The model parameters are chosen to mimic the line at the receiver end in the vicinity of critical damping. Figure D-1 is used in the explanation of the receiver switching problem.

The capacitor, C, is chosen to hold the same charge as the actual receiver bundle and is, hence, the value which is measured on a low-frequency bridge. Because the inductance, L, carries all of I_r in the equivalent circuit, it must be smaller than the inductance arrived at by dimensional considerations, which does not carry the entire current I_r . An experimental evaluation of L can be done by making R_{on} very small and observing the ringing frequency.

The receiver switches may be in one of two states, clamping the 32 associated word lines either to +V or to ground (see Figure 2-7a). When a receiver is unselected, it clamps the 32 lines to +V. Selection of the receiver corresponds to putting the switch in the ground position, charging C through R_{on} . If the switch is thrown at t = 0,

$$I_{r} = \frac{V}{L} \left(\frac{\sin \beta t}{\beta}\right) \exp \left(\frac{-R_{on}t}{2L}\right)$$

where

$$\beta = \left(\frac{1}{LC} - \frac{R_{on}^2}{4L^2}\right)^{1/2}$$

This case is shown for the experimental straight braid S in Figure D-2. In general, it is desirable to make β zero or imaginary ($R \ge 2\sqrt{\frac{L}{C}}$) because the time of the switching transient is to be minimized. The most desirable case is that of critical damping ($\beta = 0$); however, in practice it is difficult to obtain exactly this case because the parameters of each receiver will vary somewhat. An underdamped response is undesirable because it will cause noise current to flow through the half-selected diodes represented by d when $V_c < 0$ In addition, it is possible for the receiver bundle to remain at a voltage below ground for a long time after the initial transient because the switch is not strictly bipolar. This is because the line will lose more charge than CV on the first half-cycle and then become overdamped when I_r attempts to change direction.

Uninhibited cores which are linked by I_r tend to cause overdamping to occur because they increase R and L linearly by the number of cores linked. This can be readily seen by noting that the condition for overdamped operation is:

$$\frac{R^2}{L} > \frac{4}{C}$$

but for n-unihibited cores, and R \approx 20 Ω , L = 1.9 μ h,

$$\frac{\left(R + nR_{c}\right)^{2}}{L + nL_{c}} > \frac{R^{2}}{L}$$

because $R_c \approx 0.7$ and $L_c \approx 0.07 \times 10^{-6}$. If, however, the cores linked are inhibited, R_c decreases to about .01 ohm and L_c remains the same; the result being that the circuit tends toward underdamping for increasing n below 256. Comparison of these two cases is shown in Figure D-3.

The receiver switch must necessarily be designed so as to connect unselected receiver bundles to + E because, otherwise, the initial potential V_c is strictly a function of past addressing history. In fact, V_c for a given receiver bundle can greatly exceed + E. Returning all receiver bundles to + E guarantees that they are at a known potential at the beginning of each memory cycle.





Fig. D-1 Receiver Switching and Equivalent Circuit



Fig. D-2 I_r for Braid "S" Using Ideal Switch



 Fig. D-3 Effect of Inhibits on Receiver Change. "Y" Braid, Receiver Bundle Threads 112 Successive Cores, Rest of Braid Threads No Cores.
 Top: Inhibits Constantly On. Bottom: Inhibits Constantly Off.

APPENDIX E

CORE RESPONSE

Because it is desirable to keep the voltage drop along a word line small, the cores must act as step-up transformers to enable the output of a sense winding to overcome the high (~0.7 Volt) threshold of the sensing gate. Once the gate has had its threshold exceeded, the sense winding must produce sufficient current to hold the gate on until its output is strobed. A convenient way to look at the cores is as a current transformer whose output voltage is directly proportional to the net current through the core. The conditions which give this mode of operation can be found from the following analysis.

First consider the case of two coupled coils where one of them is driven by a current source, and the other has a resistive load.



Fig. E-1

$$l_{21} \frac{di_1}{dt} = l_{22} \frac{di_2}{dt} - i_2 R_2.$$

Letting K = coefficient of coupling

N₁ = turns on driven coil

 N_2 = turns on secondary coil

 ϕ/i = ratio of flux to current in a single turn coil.

then

$$l_{21} = K N_1 N_2 \phi/i$$
,
 $l_{22} = N_2^2 \phi/i$

In the complex frequency domain:

$$i_{2}(s) = i_{1}(s) \frac{s l_{21}/l_{22}}{s + R_{2}/l_{22}}$$
$$e_{2}(s) = i_{1}(s) \frac{s k (N_{1}/N_{2}) R_{2}}{s + R_{2}/(N_{2}^{2} \phi/i)}$$

In order to take into account energy losses in the core material, R_2 must be the parallel combination of the secondary resistance and a resistance give by:

$$R_{\text{core loss}} = N_2^2 \frac{A}{\langle \ell \rangle} \frac{4\pi \times 10^{-7} \times \mu_r}{\tau}$$
[17]

where A = core cross sectional Area.

< l > = mean magnetic flux path length.

 μ_r = relative permeability in the region of zero magnetic field.

au = relaxation time constant of Magnetization.

Core loss may be neglected, of course, if $R_{core \ loss} >> R_{secondary}$. For the cores in the described system $R_{core \ loss} = 4990$ ohms.

For the particular case where $i_1(t) = Mt$ for t > 0, we find:

$$e_{2}(t) = M K N_{1}N_{2} \phi/i \left[1 - \exp\left(-\frac{R_{2}t}{N_{2}^{2} \phi/i}\right) \right]$$
$$\frac{de_{2}}{dt} = M K \frac{N_{1}}{N_{2}} R_{2} \exp\left[-\frac{R_{2}t}{N_{2}^{2} \phi/i}\right]$$
$$t \ll \frac{N_{2}^{2} \phi/i}{R_{2}}$$

If

Hence

then $e_2 \approx M K \frac{N_1}{N_2} R_2 t$ which is exactly proportional to the input current.

Note that increasing the secondary turns will cause the output voltage to decrease, as long as the coefficient of coupling, K, remains relatively constant.

The nature of the current transformer approximation can be seen from Figure E-2. Letting e_2 approximate V_s , we get very good agreement between calculations and the measured response of Figure E-2. For this system, K = 0.88 and $\phi/i = 0.33 \times 10^{-6}$ henry.



Fig. E-2 Observed Core Response

APPENDIX F

U CORE VERSUS E CORE

The braid memory discussed in this report is based on the use of a U-shaped core. An alternative is to use an E-shaped core (more properly, a double U), with the sense windings wound around the middle leg. The braid slips along the middle leg (see Figure F-1) so that the current along the selected word line goes through one or the



Figure F-1

Top View of E Cores with Braid

other window of the E core, depending on the information content. The advantage of such a system lies in the bipolar nature of the output emf. While in a U core the ones and zeros are roughly as in Figure F-2a, in an E core they appear as in Figure F-2b.







Figure F-2b E-Core Outputs The bipolar signals result in a much higher effective signal-to-noise ratio which can, in turn, be used to speed up the memory operation. The amplitude of the output signal, however, will be smaller for the E-shaped core provided the same drive current is employed. This result follows readily from the expressions in Appendix E if we make up the E core from two U cores. The output voltage for the E-core case becomes:

$$e_2(S) = i_1(S) \frac{1}{2} \frac{SK(N_1/N_2)R_2}{S + \frac{R_2}{2N_2^2 \phi/i}}$$

If $i_1(t) = Mt$ for $t \ge 0$

$$e_{2}(t) = MKN_{1}N_{2} \phi/i \left[1 - exp(\frac{-R_{2}}{2N_{2}^{2} \phi/i})\right].$$

The main disadvantage of E cores is the approximate doubling of the volume required for the memory. This fact is a consequence of the way the memory is laid out. The expansion to E cores causes an approximate doubling of the dimension along the bit-position axis in Figure 2-5. This effective decrease in memory density by a factor of two is a high price to pay in space and military applications where volume and weight are at a high premium.

A final disadvantage of the E core is the fact that the sense windings and all braids must be placed on the center leg, whereas both legs of the U core can be used for sense windings and braids.

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