

DWG NO.
6000124

A

REVISIONS

CHK	ENGRG NOTICE	LTR	DESCRIPTION	DATE	APPROVED
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DWG CHK <i>O. Bailey 10-29-65</i>		TITLE UNIT LOGIC DEVICE TYPES 322, 323, 324, DISCRETE INPUT (DIB), DESIGN AND PERFORMANCE FOR	
DSGN APPROVAL <i>8/3/65 R. A. Throck</i>		SIZE A	CODE IDENT NO. 03640
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SCALE		WT	SHEET 1 of 10

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UNIT LOGIC DEVICE TYPES 322, 323, AND 324, DISCRETE INPUT (DIB), DESIGN AND PERFORMANCE FOR

1. SCOPE

1.1 PURPOSE - This specification defines the design and performance characteristics of the Discrete Input (DIB), Unit Logic Device (ULD) Types 322, 323, and 324.

2. APPLICABLE DOCUMENTS

2.1 The following documents shall form a part of this specification to the extent specified herein. In case of conflict between this specification and the referenced documents, this specification shall have precedence.

2.2 IBM SPECIFICATIONS

6701130

Electronic Measurement Standards

2.3 IBM DRAWINGS

6000043

Transistor-Silicon NPN

6000047

Diode-Silicon

6000322

Unit Logic Device, Type 322

6000323

Unit Logic Device, Type 323

6000324

Unit Logic Device, Type 324

3. REQUIREMENTS

3.1 DISCRETE INPUT - The Discrete Input (DIB) provides an output signal compatible with LVDA logic circuitry. The input signal is characterized by a switch which is either closed to ground or open. The circuit provides a logical inversion of the input signal.

3.2 LOGIC BLOCK DIAGRAM

3.2.1 System Block Diagram - Refer to Figure 1.

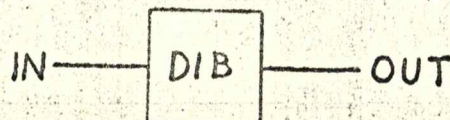


FIGURE 1

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3.2.1 ULD Interconnection Block Diagram - Refer to Figure 2.

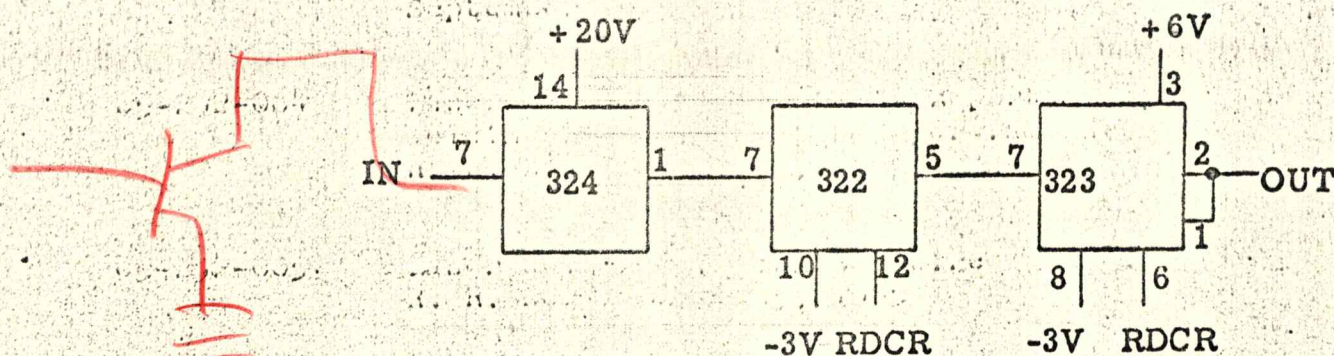


FIGURE 2

3.3 SCHEMATIC - Refer to Figure 3.

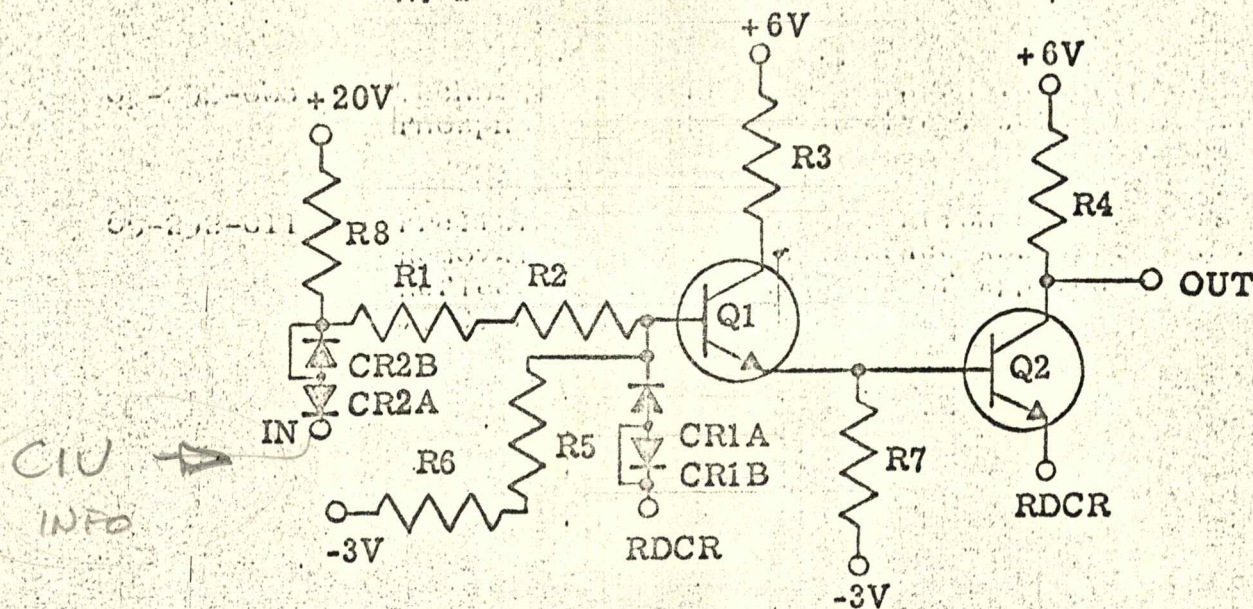


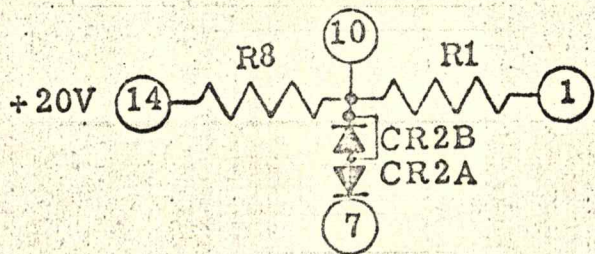
FIGURE 3

DO

1st
c/p

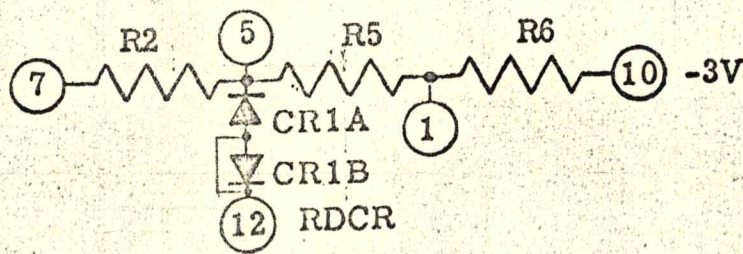
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3.3.1 ULD Schematic - Refer to Figures 4, 5 and 6.



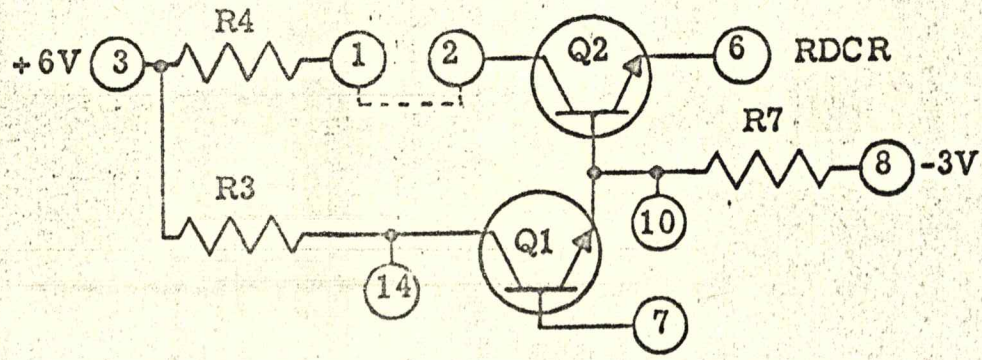
ULD TYPE 324

FIGURE 4



ULD TYPE 322

FIGURE 5



ULD TYPE 323

FIGURE 6

3.4 OPERATING TEMPERATURE LIMITS - Maximum junction temperature of any semiconductor device is 100°C. Minimum junction temperature of any semiconductor device is 10°C.

3.5 COMPONENTS

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3.5.1 Discrete Components. Refer to Table I.

TABLE I
UNIT LOGIC DEVICE

<u>Type Number</u>	<u>IBM Part Number</u>
322	6000322
323	6000323
324	6000324

3.5.2 Deposited Components in ULD Types 322, 323, and 324.
Refer to Tables II through IV.TABLE II
TRANSISTORS

<u>REF DES</u>	<u>IBM Drawing</u>
Q1	6000043
Q2	6000043

TABLE III
RESISTORS

<u>REF DES</u>	<u>Resistive Value</u>	<u>Wattage Rating</u>	<u>EOL Tolerance</u>
R8	8K	51MW	+5%
R1	10K	18MW	+5%
R2	8K	20MW	+5%
R3	5.2K	55MW	+5%
R4	6K	17MW	+5%
R5	8.25K	20MW	+5%
R6	8.25K	20MW	+5%
R7	10K	21MW	+5%

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TABLE IV

DIODE SETS

<u>REF DES</u>	<u>IBM Drawing</u>
CR1 A	6000047
CR1 B	6000047
CR2 A	6000047
CR2 B	6000047

3.6 COMPONENT OPERATING CONDITIONS

3.6.1 ULD Dissipation - Refer to Table V.

TABLE V

UNIT LOGIC DEVICE

<u>Type Number</u>	<u>Average Power Dissipation During Worst Case Steady State Conditions</u>
322	6.3MW
323	17MW
324	72MW

3.6.2 Deposited Components in ULD Types 322, 323 and 324.
Refer to Tables VI through VIII.

TABLE VI

TRANSISTORS

<u>REF DES</u>	<u>Parameter</u>	<u>Peak</u>	<u>Average During Worst Case Steady State Conditions</u>
Q1	Collector to Emitter Voltage	6.4V	6.4V
	Inverse Base to Emitter Voltage	0V	0V
	Collector Current	1.15MA	1.15MA
	Power Dissipation	1.15MW	1.15MW
Q2	Collector to Emitter Voltage	6.12V	6.12V
	Inverse Base to Emitter Voltage	1.7V	1.7V
	Collector Current	8.45MA	8.45MA
	Power Dissipation	1.7MW	1.7MW

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TABLE VII

DIODE SETS

<u>REF DES</u>	<u>Peak Forward Current</u>	<u>Peak Reverse Voltage</u>	<u>Maximum Switching Rate</u>
CR2B	NA		
CR2A	3.02MA	21.7V	1KC
CR1A	0.243MA	2V	1KC
CR1B	NA		

TABLE VIII

RESISTORS

<u>REF DES</u>	<u>Peak Voltage</u>	<u>Average Power Dissipation During Worst Case Steady State Conditions</u>
R8	23V	52MW
R1	8.0V	6.7MW
R2	6.5V	5.3MW
R3	5.5V	6.2MW
R4	5.9V	6.2MW
R5	2.6V	0.8MW
R6	2.6V	0.8MW
R7	3.96V	1.7MW

3.7 POWER SUPPLY REQUIREMENTS - Refer to Table IX.

TABLE IX

CURRENT LOAD PER SUPPLY

<u>DC Voltage</u>	<u>Tolerance</u>	<u>Maximum Current Output Up</u>	<u>Output Down</u>
+20V	+2%	3.02MA	1.58MA
+6V	+2%	Negligible	2.32MA
-3V	+2%	+ .07MA	.67MA

3.7.1 Duty Cycle -100 percent.

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3.7.2 Voltage Application Sequence - None.

3.8 SIGNAL INPUT REQUIREMENTS

3.8.1 Signal Input Levels

	Minimum	Maximum
Up Level	+8V OR Open Circuit	+35V Or Open Circuit
Down Level	-3V	+3V

3.8.2 Input Currents

	Minimum	Maximum
Input at +0V	-2.60MA	-2.16MA
Input at +23V	0MA	0MA

3.8.3 Input Switching Requirements

	Minimum	Maximum
Rise Time	10NSEC	500USEC
Fall Time	10NSEC	500USEC

3.9 OUTPUT SPECIFICATIONS - Output specifications are predicated upon worst-case signal and power inputs and worst case end-of-life component characteristics. End-of-life resistor tolerance is $\pm 5\%$.

3.9.1 Maximum Resistive Load - The output may drive a minimum resistance of 790 ohms returned to +6V.

	Load Current	
	Minimum	Maximum
Output Up	0	-100UA
Output Down	NA	-7.75MA

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3.9.2 Output Signals Levels - Steady State

	<u>Minimum</u>	<u>Maximum</u>
Output Up	5.25V	6.12V
Output Down	0V	0.37V

3.9.3 Maximum Capacitive Load - Maximum load capacitance including stray capacitance is 100 PF

3.9.4 Output Delay

3.9.4.1 Output Rise Delay

	<u>Minimum</u>	<u>Maximum</u>
Rise Delay	20USEC	300USEC

3.9.4.2 Output Fall Delay

	<u>Minimum</u>	<u>Maximum</u>
Fall Delay	5USEC	200USEC

3.9.5 Output Response Times

3.9.5.1 Fall Time

	<u>Minimum</u>	<u>Maximum</u>
Fall Time	1USEC	25USEC

3.9.5.2 Rise Time

	<u>Minimum</u>	<u>Maximum</u>
Rise Time	1USEC	30USEC

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3.10 INSTALLATION REQUIREMENTS

3.10.1 Grounding - Not applicable.

3.10.2 Packaging - The three ULD types 322, 323, and 324 forming DIB are to be adjacent.

4. QUALITY ASSURANCE PROVISIONS - Not applicable.

5. PREPARATION FOR DELIVERY - Not applicable.

6. NOTES

6.1 ABBREVIATIONS

NSEC	Nanosecond
PF	Picofarad
NA	Not Applicable.
EOL	End-of-Life
RDCR	Regulated DC Return

6.1.2 All voltages are DC unless otherwise specified.

6.2 MEASUREMENTS - Refer to Electronics Measurement Standards, IBM Specification 6701130.