

GENERAL  ELECTRIC

APOLLO
SUPPORT
DEPARTMENT

ACE-S/C OPERATOR COURSE STUDY GUIDES

CONTRACT NASw-410

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ACCEPTANCE CHECKOUT EQUIPMENT – SPACECRAFT

FOR TRAINING PURPOSES ONLY

ACE-S/C OPERATOR COURSE
STUDY GUIDES

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Apollo Support Department
Missile and Space Division
General Electric Company
Daytona Beach, Florida

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INTRODUCTION TO ACE-S/C

OBJECTIVES

To familiarize the student with ACE-S/C concepts and requirements.

INTRODUCTION

The development of new manned spacecraft systems has increased the complexity of tasks relating to integrated acceptance testing and preflight checkout of complex spacecraft systems and subsystems. The magnitude of the Apollo spacecraft checkout requirements precludes the use of conventional testing methods. The initiation of test stimuli and the analysis of the resulting test data by conventional test equipment and methods would be time consuming, costly, and would reduce the reliability of the test effort because of possible human error.

To minimize these problems, an advanced, integrated checkout and display system, which provides for centralized programmed control of spacecraft checkout operations, was developed. This advanced checkout system is called Acceptance Checkout Equipment - Spacecraft (ACE-S/C). The ACE-S/C ground station can accommodate independent subsystem and/or integrated system testing in either manual, semiautomatic, or automatic operational modes. Large quantities of test data can be processed and displayed in real time as well as recorded for post-test analysis.

ACE-S/C PROGRAM OBJECTIVES

The objectives of the ACE-S/C program are to:

- a. Provide advanced checkout and display equipment for MSC. *c/o*
- b. Provide universal checkout equipment.
- c. Provide optimum man-machine interface.
- d. Provide continuity into future programs.
- e. Insure spacecraft and checkout equipment compatibility.

LOCATIONS OF ACE-S/C EQUIPMENT

ACE-S/C ground stations are installed at the following locations for the purposes indicated:

- a. Merritt Island Launch Area (MILA), Merritt Island, Florida - ACE-S/C will be utilized to conduct the complete range of subsystem and integrated system *KSC*

testing from receipt of the spacecraft modules through spacecraft/launch vehicle mating and final prelaunch checkout.

- b. Manned Spacecraft Center (MSC), Houston, Texas - ACE-S/C will be utilized in the testing of spacecraft and astronauts in simulated space and lunar environments. Reliability assessment data will be derived from extended spacecraft operations at MSC.
- c. Grumman Aircraft Engineering Corporation (GAEC) Facility, Bethpage, New York - ACE-S/C will be utilized for subsystem and integrated system testing of the Lunar Excursion Module (LEM) during the various stages of factory assembly and checkout.
- d. North American Aviation Corporation (NAA) Facility, Downey, California - ACE-S/C will be utilized for subsystem and integrated system testing of the Command Module (CM) and Service Module (SM) during the various stages of factory assembly and checkout.

ACE-S/C SYSTEMS REQUIREMENT

The ACE-S/C ground station operates in conjunction with the spacecraft during checkout via the Digital Test Command System (DTCS) and the Digital Test Measurement System (DTMS). The DTCS receives, decodes, and converts digital test commands from the ACE-S/C ground station and the DTMS codes and multiplexes the response of the spacecraft subsystems to digital commands for transmission to the ACE-S/C ground station for processing.

The ACE-S/C ground station is divided into three primary areas: the computer room, the control room, and the terminal facility room. The computer room contains the data acquisition subsystem, the computer subsystem, and data transmission equipment. The control room (Figure 1) contains consoles, data display system, and part of the command generation equipment. The terminal facility room contains patching facilities, parts of the command and data display subsystems, and timing equipment.

Specifically the ACE-S/C ground station can perform the following functions:

- a. Provide the control, display, data processing, and recording required to control spacecraft stimuli equipment.
- b. Receive, process, display, and record spacecraft parameter data derived from spacecraft ground and flight telemetry systems.
- c. Provide self-check and calibration capacity for itself and related equipment.

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Figure 1. ACE-S/C Control Room

FEATURES OF ACE-S/C

The ACE-S/C system was developed to check out a broad range of complex spacecraft. In its present application ACE-S/C is being utilized to perform the complete range of spacecraft testing from factory checkout to launch. In accomplishing its assigned task in the Apollo program, the ACE-S/C system:

- a. Completely tests integrated systems and independent subsystems.
- b. Provides any desired degree of test automation.
- c. Processes large quantities of data for real-time display.
- d. Adapts to any system or test mode by means of software changes.

The following additional advantages are accrued through the utilization of ACE-S/C:

- a. Provides for astronaut participation and launch control.
- b. Tests across system interfaces.
- c. Uses flight telemetry equipment.
- d. Minimizes cabling by serial transmission of commands and data.
- e. Has built-in self-check capability.

PROGRAM AND INTERFACE REQUIREMENTS

To generate the required command and display computer programs and the appropriate decommutator programs, computer programmers must be provided with detailed information concerning the specific command functions assigned to various control consoles, measurement limits, and display devices to be used for the various measurements. This information is provided to the programmers in the Test Operation Programing Requirements document. This document takes the form of punched cards and defines the configuration of the ACE-S/C equipment and the content of the computer and decommutator programs.

Upon receipt of the programing requirements, the programmers generate an assembly program. This assembly program is used to assemble the test operation program by calling up existing routines and subprograms from the master file or program library tape.

A central program library of official ACE-S/C computer programs, subprograms, and subroutines is maintained. The program library contains a master card file for each program. This file is reproduced into master program magnetic tape, and from these tapes, a working library tape is prepared.

The library tape contains all programs, subprograms, and subroutines in common use at a specific ACE-S/C facility. Provisions are made to replace, insert, or delete routines from the library tapes during all phases of operation including test preparation, checkout, and spacecraft test operations.

PERSONNEL REQUIREMENTS

Operator personnel will be supplied by the using agency to man the various operational consoles. These operator personnel will initiate the various tests to be performed by the spacecraft and in turn will evaluate the test results by monitoring the display devices located in the control room.

POSITIONAL NOTATIONAL NUMBERING SYSTEMS

OBJECTIVES

1. To review decimal, binary, and octal numbering systems.
2. To teach method of converting from one system to another.

INTRODUCTION

As man emerged from a totally primitive state, his progress was paced by the development of alphabets and number systems. Of the many number systems developed, probably the most commonly used base, or radix, was ten - which you recognize as the basis of the familiar decimal system. Possibly this radix was selected because man has ten fingers and ten toes and it was a natural and familiar concept on which to base a number system.

For the purposes of this course, we will be concerned with three numbering systems: (1) decimal, (2) binary, and (3) octal, having base numbers of 10, 2, and 8, respectively. Emphasis will be placed on the binary system, since its base of two admits only two digits, and this fact adapts it ideally to electronic computational devices.

The history of computing devices goes back several centuries, but it is only in recent years that electronic component development made possible the tremendous speeds and capacity of modern computers. The greatest contributions to this effect were the development of the transistor and the refinement of pulse and digital techniques.

The development of complex computing machines was greatly enhanced by Boolean algebra principles. This practice enabled engineers to mathematically analyze new circuitry prior to fabrication.

Since the decimal numbering system is used by all of us daily, it is very familiar. It consists of ten symbols (0 through 9) and, therefore, has a radix of 10. In a positional, notational system such as the decimal system, each digit of the number is recognized by the position that it occupies. The positional value of the first order in the decimal system is 1; the second is 10; the third is 100, etc. The first-order digit, which has the lowest value, is considered the least significant digit (LSD). The digit that has the

highest value is the most significant digit (MSD). In the decimal number 23, the LSD is represented by the symbol 3 and the MSD by the symbol 2. When counting in a number system, two rules apply. First, each time a count of 1 takes place, the symbol in the first order changes to the next symbol in a repetitive sequence. By adding a 1 to 4 in the decimal system, the symbol changes to 5. Second, each time an order of a number changes from the highest symbol in the system to 0, a count of 1 is sent to the next highest order. For example, adding a 1 to a 9 in the decimal system changes the first order to 0 and adds 1 to the second order, giving numerical 10. Thus, when the positional value that is attached to each decimal order is known, the exact value of each digit in a decimal number can be determined. The procedure, for the decimal number 40,811 is as follows:

$$\begin{array}{rclcl}
 1 \times 10^0 & = & 1 \times & 1 & = & 1 \\
 1 \times 10^1 & = & 1 \times & 10 & = & 10 \\
 8 \times 10^2 & = & 8 \times & 100 & = & 800 \\
 0 \times 10^3 & = & 0 \times & 1000 & = & 0000 \\
 4 \times 10^4 & = & 4 \times & 10000 & = & \underline{40000} \\
 & & & & & 40811
 \end{array}$$

In summary, the decimal numbering system represents numbers which are a sum of the powers of 10 with each position weighted by a digit between 0 and 9. There are many other numbering systems besides the decimal system. Two of these, the octal and binary, are of special importance because of their application in computational devices.

EXPLANATION

In digital computers the binary system is most commonly used. Binary digits are referred to as "bits." Since only two symbols are used, the radix of the binary system is two. Thus, the binary system represents quantities as a sum of the powers of 2, where each order of 2 is weighted by either the digit 0 or 1. A binary number is interpreted from the least significant digit (LSD) to the most significant digit (MSD) in increasing powers of 2. In binary counting the rotating sequence is 0, 1, 0, 1, 0, ... etc. Thus, a binary word (number) will appear as a series of 1's and 0's where the highest

order will be larger than other 1's added together. An example of a simple binary count with decimal equivalents is as follows:

<u>Decimal</u>	<u>Binary</u>
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
10	1010

The decimal number 7 is 0111 in binary. If the LSD (the extreme right-hand bit) is equal to 2 to the 0 power, the second bit is equal to 2 to the 1st power, the third equal to 2 to the 2nd power, and the fourth is equal to 2 to the 3rd power (e.g., 0111_2 can be evaluated as follows:

$$1 \times 2^0 = 1$$

$$1 \times 2^1 = 2$$

$$1 \times 2^2 = 4$$

$$0 \times 2^3 = \underline{0}$$

$$\text{Sum} = 7$$

therefore, 0111_2 is equal to 7_{10} .

It may be seen now how the highest order 1 is larger than the other 1's added together. If it is desired to know the decimal value of a large binary word, it is necessary only to add the values of the bits where a 1 is present. For example:

Position Value	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Binary	0	1	1	0	1	1	1	0	1	0	1
Decimal	0	512	256	0	64	32	16	0	4	0	1

Thus, the binary word 01101110101 represents the decimal equivalent 885.

Whereas the binary system is used in the computer itself, the octal system is generally used for writing data for insertion into the computer. The great advantage of the octal system is the ease with which conversion may be made from and to binary numbers. The octal system is directly related to the binary system, as it represents the sum of the powers of 8, and 8 is the decimal number 2 to the third power (2^3). In the octal system there are eight symbols: 0, 1, 2, 3, 4, 5, 6, and 7. In octal counting, the rotating sequence is 0, 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, ... etc. Each time the order changes from 7 to 0, the next higher order receives a count of 1. For example, $7 + 1 = 10$ in the octal system. The symbols 8 and 9 have no significance in the octal system, as seen in the following chart.

<u>Decimal</u>	<u>Octal</u>	<u>Decimal</u>	<u>Octal</u>
1	1	11	13
2	2	12	14
3	3	13	15
4	4	14	16
5	5	15	17
6	6	16	20
7	7	17	21
8	10	18	22
9	11	19	23
10	12	20	24

The use of coded binary in data processing is simpler from a design and cost standpoint and is generally used. Note that the binary number 1010101010 has little significance until it is converted to either a decimal or an octal number. In octal coded binary the 12 bits are broken down into groups of three (101-010-101-010) and then read directly as an octal number (5-2-5-2). This is the octal representation of the binary number and is used to denote addresses, instructions, and operands.

This guide will be concerned with the following three categories of numerical conversions:

- Conversion of octal and binary numbers to their decimal equivalents.
- Conversion of decimal numbers to either their octal or binary equivalents.
- Conversion of octal numbers to binary and binary numbers to octal.

For the first two categories, first the general rules are described; then the rules are applied to the octal and binary systems. (Refer to the rules while following the examples.) The third category is a special condition and the two conversions of this category are described, followed by application and explanation.

Conversion of Octal and Binary Numbers to Their Decimal Equivalents

To convert any nondecimal number to its equivalent, carry out the following steps:

- Arrange the digits of the number vertically, with the least significant digit at the top of the column and the most significant digit at the bottom.
- Note the radix of the nondecimal number and write the radix next to each of the digits of the number.
- To each of the radix numbers of step b, apply the decimal exponents 0, 1, 2, 3, etc.
- Expand the powers of step c.
- In each order multiply the digit of the number together with the expanded powers of step d to obtain the positional value for that digit.
- Add all the positional values to obtain the equivalent decimal number.

Following the above rules, the octal number 51043 is converted to its decimal equivalent as follows:

<u>Step a</u>		<u>Steps b and c</u>		<u>Step d</u>	<u>Step e</u> (Step a x Step d)
LSD	3	8^0	=	1	3
	4	8^1	=	8	32
	0	8^2	=	64	0
	1	8^3	=	512	512
MSD	5	8^4	=	4096	<u>20480</u>
51043					Decimal 21027 (Step f)

Again following the rules, the binary number 1101011 is converted to its decimal equivalent as follows:

<u>Step a</u>		<u>Steps b and c</u>	<u>Step d</u>	<u>Step e</u> (Step a) x (Step d)
LSD	1	2^0	1	1
	1	2^1	2	2
	0	2^2	4	0
	1	2^3	8	8
	0	2^4	16	0
	1	2^5	32	32
MSD	1	2^6	64	<u>64</u>
Decimal				107 (Step f)

Conversion of Decimal Numbers to Either Their Binary or Octal Equivalent

To convert a decimal number to its octal or binary equivalent, carry out the following steps:

- Write the decimal number to be converted.
- Write the decimal radix of the system to which the decimal number is to be converted.
- Divide the decimal number by the radix. This division will result in a quotient and a remainder. Write the quotient below the decimal number and write the remainder to the right of the quotient. The first remainder is the least significant digit of the new number.
- Divide the quotient of step c by the radix to obtain a second quotient and a remainder. Place the new quotient beneath the quotient obtained in step c and place the new remainder below the remainder obtained in step c. This remainder is the second order digit of the new number.
- Repeat step d over and over again until the quotient of a division is 0. The remainder obtained for this division is the most significant digit of the new number. This completes the conversion.

Following the above rules, the decimal number 21027 is converted to its octal equivalent as follows:

<u>Step b</u>	<u>Step a</u>	<u>Step e</u>
8	21027	3 LSB step c (step a divided by step d)
	2628	
	328	4
	41	0
	5	1
	0	5 MSD; the octal equivalent is 51043

Following the above rules, the decimal number 107 is converted to its binary equivalent as follows:

<u>Step b</u>	<u>Step a</u>	<u>Step e</u>
2	107	
	53	1 LSD step c (step a divided by step d)
	26	1
	13	0
	06	1
	03	0
	01	1
	0	1 MSD; the binary equivalent is 1101011

Conversion of Binary to Octal/Octal to Binary

If the first eight binary numbers have been memorized, the binary-to-octal and octal-to-binary conversions are very easily carried out. To convert a binary number to its octal equivalent, carry out the following steps:

- Arrange the binary number in groups of three digits, starting from the rightmost digit. These groups are referred to as triads.
- For each triad, write the octal equivalent (which is also the decimal equivalent), treating each triad as if it were an octal order. This gives

the octal equivalent. Using these steps, the binary number 110011101 converted to its octal equivalent as follows:

Step a:	110	011	101	Binary
Step b:	6	3	5	Octal Equivalent

To convert an octal number to its binary equivalent, the above steps are carried out in reverse as follows:

Step a:	5	3	6	Octal
Step b:	101	011	110	Binary

To show all possible cases, the binary 111, 110, 101, 100, 011, 010, 001, 000 is converted to its octal equivalent as follows:

Step a:	111	110	101	100	011	010	001	000
Step b:	7	6	5	4	3	2	1	0

The four basic arithmetic operations are addition, subtraction, multiplication, and division. In general, all arithmetic operations involve three numbers. One number is the one that is being operated upon. This is generally referred to as the operand. The second number is the one that operates on the operand. This is generally referred to as the operator. The third number is the one produced by the operation. This is called the resultant. For each of the four arithmetic operations there are specific expressions for the general terms operand, operator, and resultant. These, together with the conventional way of writing, are as follows:

General Term	Specific Term			
	<u>Addition</u>	<u>Subtraction</u>	<u>Multiplication</u>	<u>Division</u>
Operand:	Augend	Minuend	Multiplican	Dividend
Operator:	Addend	Subtrahend	Multiplier	Divisor
Resultant:	Sum	Difference	Product	Quotient

In practice, the term "operand" is generally used to refer to all of the above. Arithmetic operations are carried out in computers with binary numbers. Each of the four arithmetic operations is discussed in turn.

Binary Addition

Binary addition table:

	0	1	10
0	0	1	10
1	1	10	11
10	10	11	100

To add binary 1101 to 1001, the table is used in the following manner:

- a. Arrange the numbers for addition -

$$\begin{array}{r} 1001 \text{ augend} \\ +1101 \text{ addend} \end{array}$$

- b. Take the first order. From the table it can be seen that its sum is 10X. The first order of the sum is 0 and the carry is 1.

$$\begin{array}{r} \downarrow \\ + \text{carry} \\ 1001 \\ +1101 \\ \hline 0 \end{array}$$

- c. Take the second order. The sum of the second order is 1 with no carry to the third order.

$$\begin{array}{r} \downarrow \\ 1001 \\ +1101 \\ \hline 10 \end{array}$$

- d. Take the third order. The sum is 1 with no carry.

$$\begin{array}{r} \downarrow \\ 1001 \\ +1101 \\ \hline 110 \end{array}$$

- e. Take the fourth order. The sum is 10. The fourth order sum is 0 with a 1 carry to the 5th order.

$$\begin{array}{r} \downarrow \\ 1001 \text{ augend} \\ +1101 \text{ addend} \\ \hline 10110 \text{ sum} \end{array}$$

When an addition table is not available, the following rules will be helpful.

1. $0 + 0 = 0$
2. $1 + 0 = 1$
3. $1 + 1 = 0$ and a 1 to carry to the next highest order.

Binary Subtraction

The subtraction of one binary number from another, 10110 from 11000101, for example, is carried out in the following manner:

- a. Arrange the numbers for subtraction -

$$\begin{array}{r} 11000101 \text{ minuend} \\ - \quad 10110 \text{ subtrahend} \\ \hline \end{array}$$

- b. Take the first order. Because the first order minuend is a 1 and the first order subtrahend is a 0, their difference is 1.

$$\begin{array}{r} \downarrow \\ 11000101 \\ - \quad 10110 \\ \hline 1 \end{array}$$

- c. Take the second order. Note that because the minuend is a 0 while the subtrahend is a 1, borrowing is required. In the binary system a special rule for borrowing is as follows:

1. Add 10 to the minuend in the order in which borrowing is required (in this case the second order) and then subtract. The result is:

$$\begin{array}{r} \downarrow \\ \quad 10 \\ 110001\cancel{0}1 \\ \quad 10110 \\ \hline \quad 10 \end{array}$$

2. Then consider the next higher order minuend. The rule is to change the number (if it is a 1, change it to a 0, and if it is a 0, change it to a 1). Note that, in the latter case, borrowing is done from a 0 to the next higher order, which is impossible; therefore the borrowing process must continue to successive higher orders of the minuend until a 1 is reached. This case is considered in the fourth step. Because the minuend of the next higher order (the third order) is a 1, change it to a 0. The result is then as follows. (Note that no further subtraction can be performed until this is done):

$$\begin{array}{r} \quad 010 \\ 1100\cancel{0}\cancel{0}1 \\ \quad 10110 \\ \hline \quad 11 \end{array}$$

- d. Take the third order. As in the second order, borrowing is required.

Therefore, add 10 to the third order and subtract; the result is as follows:

$$\begin{array}{r}
 \downarrow \\
 1010 \\
 11000\cancel{0}1 \\
 \underline{10110} \\
 111
 \end{array}$$

Consider the next higher order, the fourth order. But note that, in this case, because the number is a zero, it is impossible to borrow from the fourth order. Therefore, change the 0 to a 1 and go on to the next higher, or fifth order. As in the fourth order, the number is a 0; therefore, it is necessary to change the 0 to 1 of this order and of the succeeding orders until a 1 is reached. In this example, a 1 exists in the seventh order. Now change that 1 to a 0; the borrowing process is thus complete and the result is then as follows:

$$\begin{array}{r}
 \downarrow \\
 0 \ 1 \ 1 \ 1 \ 10^{10} \\
 1 \ \cancel{1} \ \cancel{0} \ \cancel{0} \ \cancel{0} \ \cancel{1} \ 1 \quad \text{minuend} \\
 \quad \quad \quad 1 \ 0 \ 1 \ 1 \ 0 \quad \text{subtrahend} \\
 \hline
 1 \ 0 \ 1 \ 0 \ 1 \ 1 \ 1 \quad \text{difference}
 \end{array}$$

The result can readily be checked by adding the subtrahend to the difference. This addition should equal the minuend.

Complements

The analog of the 10's complement in the binary system is called the 2's complement. This is generated by subtracting the number to be complemented from a power of binary 10. The analog of the 9's complement in the binary system is called the 1's complement. This can be generated by subtracting the number to be complemented from a series of 1's. In practice, the process of generating the 1's complement is very simple. Each bit (binary digit) of the binary number is inverted; each 1 becomes a 0, and each 0 becomes a 1. This is a very easy operation to carry out in computers, and is one of the great advantages of the 1's complement. In computers, the 2's complement is formed by adding a 1 to the 1's complement.

To carry out binary subtraction using complements (example: 11010 subtracted from 101101), perform the following steps:

- a. Arrange the numbers for subtraction:

$$\begin{array}{r}
 101101 \quad \text{minuend} \\
 - \underline{11010} \quad \text{subtrahend}
 \end{array}$$

- b. Obtain the 1's complement of the subtrahend by changing each 0 to a 1 and each 1 to a 0. Then add 1 to the 1's complement to obtain the 2's complement.

$$\begin{array}{rcl}
 011010 & \text{subtrahend} & \\
 100101 & \text{1's complement of subtrahend} & \\
 + \quad 1 & & \\
 \hline
 100110 & \text{2's complement of subtrahend} &
 \end{array}$$

- c. In the subtraction arrangement, replace the subtrahend with its 2's complement and carry out binary addition.

$$\begin{array}{rcl}
 101101 & \text{minuend} & \\
 +100110 & \text{2's complement of subtrahend} & \\
 \hline
 1010011 & &
 \end{array}$$

- d. Drop the extreme left-hand digit 1, the end carry, to obtain the true difference.

$$\begin{array}{rcl}
 1010011 & & \\
 \downarrow & & \\
 10011 & \text{difference} &
 \end{array}$$

- e. Check that this is the correct difference by adding this difference to the original subtrahend. The sum obtained in this manner is equal to the original minuend.

$$\begin{array}{rcl}
 10011 & \text{difference} & \\
 11010 & \text{subtrahend} & \\
 \hline
 101101 & \text{minuend} &
 \end{array}$$

Binary Multiplication

The binary multiplication table is presented here:

$$\begin{array}{r|l}
 & 0 \ 1 \\
 0 & 0 \ 0 \\
 1 & 0 \ 1
 \end{array}$$

The multiplication of binary 1101 by binary 1011 is carried out in the following manner:

- a. Arrange the numbers for multiplication:

$$\begin{array}{rcl}
 1101 & \text{multiplicand} & \\
 \times 1011 & \text{multiplier} &
 \end{array}$$

- b. Carry out the multiplication of the multiplicand by the first-order multiplier. Since the multiplier is 1, there are no carries and the multiplicand need only be transferred to provide the first-order product.

$$\begin{array}{rcl}
 \downarrow & & \\
 1101 & \text{multiplicand} & \\
 1011 & \text{multiplier} & \\
 1101 & \text{first-order product} &
 \end{array}$$

- c. Carry out the multiplication of the multiplicand by the second-order multiplier. Since the second multiplier order contains a 1, all that is required is that the multiplicand be transferred and shifted one place to the left to provide a second-order product.

↓

1101	multiplicand
<u>1011</u>	multiplier
1101	second-order product

- d. Carry out the multiplication of the multiplicand by the third-order multiplier. Since this order contains a 0, and the multiplicand is not transferred, the resulting order product is 0. Note that, for step e, however, the shift must be accounted for.

↓

1101	multiplicand
<u>x1011</u>	multiplier
1101	first-order product
1101	second-order product
0000	third-order product

- e. Carry out the multiplication of the multiplicand by the fourth-order multiplier. Since this order contains a 1, the multiplicand is transferred and shifted to provide the fourth-order product. Note that the third-order shift is also included. (Note that, in a digital machine, only two numbers are added together at any one time; the third number is added to the resulting sum of the first two.)

1101	multiplicand
<u>1011</u>	multiplier
1101	first-order product
1101	second-order product
0000	third-order product
1101	fourth-order product

- f. Add the order products to get the final product.

1101	first-order product
1101	second-order product
0000	third-order product
<u>1101</u>	fourth-order product
10001111	final product

In binary multiplication, carries do not arise. The order of multiplication is either by a 0 or by a 1. If it is by a 0, the order product is also 0. If it is by a 1, the order product is the same as the multiplicand. Besides this, all that is necessary in binary multiplication is that each order product be shifted one place to the left. After the order products are suitably shifted, their sum provides the desired final product. The operation of binary multiplication is an add and shift operation.

Binary Division

In binary division note that, in general, there are only two possible cases. Either the divisor will go into the dividend or it will not. If the first case is true, enter a 1 in the quotient. If the second case is true, enter a 0. The next step is to subtract the divisor from the MSB side of the dividend. The resulting difference is then divided again by the divisor, and the appropriate entry is made in the quotient. The above steps are repeated until the desired accuracy is obtained.

The following problem illustrates the paper and pencil method of doing binary division. Divide 11110 by 101 using the following method:

- a. Arrange the numbers for division

$$\begin{array}{r} \text{quotient} \\ 101 \overline{) 11110} \\ \text{divisor} \quad \text{dividend} \end{array}$$

- b. Divide the dividend by the divisor and make the appropriate entry in the quotient.

$$\begin{array}{r} 1 \\ 101 \overline{) 11110} \end{array}$$

- c. Subtract the divisor from MSB side of dividend:

$$\begin{array}{r} 1 \\ 101 \overline{) 11110} \\ \underline{101} \\ 10 \end{array}$$

- d. Bring down the next bit from the dividend:

$$\begin{array}{r} 1 \\ 101 \overline{) 11110} \\ \underline{101x} \\ 101 \end{array}$$

- e. Repeat steps 2, 3, and 4 until the remainder is zero or until the desired accuracy is achieved.

$$\begin{array}{r} 110 \\ 101 \overline{) 11110} \\ \underline{101xx} \\ 101 \\ \underline{101} \\ 0 \end{array}$$

- f. The answer may be checked by multiplying the quotient and divisor to obtain the dividend.

$$\begin{array}{r} 101 \text{ divisor} \\ \underline{110} \text{ quotient} \\ 1010 \\ \underline{101} \\ 11110 \text{ dividend} \end{array}$$

Ordinarily in a digital computer, division is accomplished by sequentially subtracting and shifting. The quotient is then formed by evaluating the difference that is obtained for each subtraction. The machine method will be further developed during the Data Processing Course.

TABLE OF POWERS OF 2

2^n	n	2^n
1	0	1.0
2	1	0.5
4	2	0.25
8	3	0.125
16	4	0.062 5
32	5	0.031 25
64	6	0.015 625
128	7	0.007 812 5
256	8	0.003 906 25
512	9	0.001 953 125
1 024	10	0.000 976 562 5
2 048	11	0.000 488 281 25
4 096	12	0.000 244 140 625
8 192	13	0.000 122 070 312 5
16 384	14	0.000 061 035 156 25
32 768	15	0.000 030 517 578 125
65 536	16	0.000 015 258 789 062 5
131 072	17	0.000 007 629 394 531 25
262 144	18	0.000 003 814 697 265 625
524 288	19	0.000 001 907 348 632 812 5
1 048 576	20	0.000 000 953 674 316 406 25
2 097 152	21	0.000 000 476 837 158 203 125
4 194 304	22	0.000 000 238 418 579 101 562 5
8 388 608	23	0.000 000 119 209 289 550 781 25
16 777 216	24	0.000 000 059 604 644 775 390 625
33 554 432	25	0.000 000 029 802 322 387 695 312 5
67 108 864	26	0.000 000 014 901 161 193 847 656 25
134 217 728	27	0.000 000 007 450 580 596 923 828 125
268 435 456	28	0.000 000 003 725 290 298 461 914 062 5
536 870 912	29	0.000 000 001 862 645 149 230 957 031 25
1 073 741 824	30	0.000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0.000 000 000 465 661 287 307 739 257 812 5
4 294 967 296	32	0.000 000 000 232 830 643 653 869 628 906 25
8 589 934 592	33	0.000 000 000 116 415 321 826 934 814 453 125
17 179 869 184	34	0.000 000 000 058 207 660 913 467 407 226 562 5
34 359 738 368	35	0.000 000 000 029 103 830 456 733 703 613 281 25
68 719 476 736	36	0.000 000 000 014 551 915 228 366 851 806 640 625
137 438 953 472	37	0.000 000 000 007 275 957 614 183 425 903 320 312 5
274 877 906 944	38	0.000 000 000 003 637 978 807 091 712 951 660 156 25
549 755 813 888	39	0.000 000 000 001 818 989 403 545 856 475 830 078 125

OCTAL-DECIMAL INTEGER CONVERSION TABLE

		0	1	2	3	4	5	6	7
0000	0000	0000	0001	0002	0003	0004	0005	0006	0007
to	to	0010	0008	0009	0010	0011	0012	0013	0014
0777	0511	0020	0016	0017	0018	0019	0020	0021	0022
(Octal)	(Decimal)	0030	0024	0025	0026	0027	0028	0029	0030
		0040	0032	0033	0034	0035	0036	0037	0038
		0050	0040	0041	0042	0043	0044	0045	0046
		0060	0048	0049	0050	0051	0052	0053	0054
		0070	0056	0057	0058	0059	0060	0061	0062
Octal	Decimal								
10000	4096								
20000	8192								
30000	12288								
40000	16384								
50000	20480								
60000	24576								
70000	28672								

		0	1	2	3	4	5	6	7
0400	0256	0257	0258	0259	0260	0261	0262	0263	
0410	0264	0265	0266	0267	0268	0269	0270	0271	
0420	0272	0273	0274	0275	0276	0277	0278	0279	
0430	0280	0281	0282	0283	0284	0285	0286	0287	
0440	0288	0289	0290	0291	0292	0293	0294	0295	
0450	0296	0297	0298	0299	0300	0301	0302	0303	
0460	0304	0305	0306	0307	0308	0309	0310	0311	
0470	0312	0313	0314	0315	0316	0317	0318	0319	
0500	0320	0321	0322	0323	0324	0325	0326	0327	
0510	0328	0329	0330	0331	0332	0333	0334	0335	
0520	0336	0337	0338	0339	0340	0341	0342	0343	
0530	0344	0345	0346	0347	0348	0349	0350	0351	
0540	0352	0353	0354	0355	0356	0357	0358	0359	
0550	0360	0361	0362	0363	0364	0365	0366	0367	
0560	0368	0369	0370	0371	0372	0373	0374	0375	
0570	0376	0377	0378	0379	0380	0381	0382	0383	
0600	0384	0385	0386	0387	0388	0389	0390	0391	
0610	0392	0393	0394	0395	0396	0397	0398	0399	
0620	0400	0401	0402	0403	0404	0405	0406	0407	
0630	0408	0409	0410	0411	0412	0413	0414	0415	
0640	0416	0417	0418	0419	0420	0421	0422	0423	
0650	0424	0425	0426	0427	0428	0429	0430	0431	
0660	0432	0433	0434	0435	0436	0437	0438	0439	
0670	0440	0441	0442	0443	0444	0445	0446	0447	
0700	0448	0449	0450	0451	0452	0453	0454	0455	
0710	0456	0457	0458	0459	0460	0461	0462	0463	
0720	0464	0465	0466	0467	0468	0469	0470	0471	
0730	0472	0473	0474	0475	0476	0477	0478	0479	
0740	0480	0481	0482	0483	0484	0485	0486	0487	
0750	0488	0489	0490	0491	0492	0493	0494	0495	
0760	0496	0497	0498	0499	0500	0501	0502	0503	
0770	0504	0505	0506	0507	0508	0509	0510	0511	

		0	1	2	3	4	5	6	7
1000	0512	0512	0513	0514	0515	0516	0517	0518	0519
to	to	1010	0520	0521	0522	0523	0524	0525	0526
1777	1023	1020	0528	0529	0530	0531	0532	0533	0534
(Octal)	(Decimal)	1030	0536	0537	0538	0539	0540	0541	0542
		1040	0544	0545	0546	0547	0548	0549	0550
		1050	0552	0553	0554	0555	0556	0557	0558
		1060	0560	0561	0562	0563	0564	0565	0566
		1070	0568	0569	0570	0571	0572	0573	0574
		1100	0576	0577	0578	0579	0580	0581	0582
		1110	0584	0585	0586	0587	0588	0589	0590
		1120	0592	0593	0594	0595	0596	0597	0598
		1130	0600	0601	0602	0603	0604	0605	0606
		1140	0608	0609	0610	0611	0612	0613	0614
		1150	0616	0617	0618	0619	0620	0621	0622
		1160	0624	0625	0626	0627	0628	0629	0630
		1170	0632	0633	0634	0635	0636	0637	0638
		1200	0640	0641	0642	0643	0644	0645	0646
		1210	0648	0649	0650	0651	0652	0653	0654
		1220	0656	0657	0658	0659	0660	0661	0662
		1230	0664	0665	0666	0667	0668	0669	0670
		1240	0672	0673	0674	0675	0676	0677	0678
		1250	0680	0681	0682	0683	0684	0685	0686
		1260	0688	0689	0690	0691	0692	0693	0694
		1270	0696	0697	0698	0699	0700	0701	0702
		1300	0704	0705	0706	0707	0708	0709	0710
		1310	0712	0713	0714	0715	0716	0717	0718
		1320	0720	0721	0722	0723	0724	0725	0726
		1330	0728	0729	0730	0731	0732	0733	0734
		1340	0736	0737	0738	0739	0740	0741	0742
		1350	0744	0745	0746	0747	0748	0749	0750
		1360	0752	0753	0754	0755	0756	0757	0758
		1370	0760	0761	0762	0763	0764	0765	0766

		0	1	2	3	4	5	6	7
1400	0768	0769	0770	0771	0772	0773	0774	0775	
1410	0776	0777	0778	0779	0780	0781	0782	0783	
1420	0784	0785	0786	0787	0788	0789	0790	0791	
1430	0792	0793	0794	0795	0796	0797	0798	0799	
1440	0800	0801	0802	0803	0804	0805	0806	0807	
1450	0808	0809	0810	0811	0812	0813	0814	0815	
1460	0816	0817	0818	0819	0820	0821	0822	0823	
1470	0824	0825	0826	0827	0828	0829	0830	0831	
1500	0832	0833	0834	0835	0836	0837	0838	0839	
1510	0840	0841	0842	0843	0844	0845	0846	0847	
1520	0848	0849	0850	0851	0852	0853	0854	0855	
1530	0856	0857	0858	0859	0860	0861	0862	0863	
1540	0864	0865	0866	0867	0868	0869	0870	0871	
1550	0872	0873	0874	0875	0876	0877	0878	0879	
1560	0880	0881	0882	0883	0884	0885	0886	0887	
1570	0888	0889	0890	0891	0892	0893	0894	0895	
1600	0896	0897	0898	0899	0900	0901	0902	0903	
1610	0904	0905	0906	0907	0908	0909	0910	0911	
1620	0912	0913	0914	0915	0916	0917	0918	0919	
1630	0920	0921	0922	0923	0924	0925	0926	0927	
1640	0928	0929	0930	0931	0932	0933	0934	0935	
1650	0936	0937	0938	0939	0940	0941	0942	0943	
1660	0944	0945	0946	0947	0948	0949	0950	0951	
1670	0952	0953	0954	0955	0956	0957	0958	0959	
1700	0960	0961	0962	0963	0964	0965	0966	0967	
1710	0968	0969	0970	0971	0972	0973	0974	0975	
1720	0976	0977	0978	0979	0980	0981	0982	0983	
1730	0984	0985	0986	0987	0988	0989	0990	0991	
1740	0992	0993	0994	0995	0996	0997	0998	0999	
1750	1000	1001	1002	1003	1004	1005	1006	1007	
1760	1008	1009	1010	1011	1012	1013	1014	1015	
1770	1016	1017	1018	1019	1020	1021	1022	1023	

OCTAL-DECIMAL INTEGER CONVERSION TABLE

	0	1	2	3	4	5	6	7
2000	1024	1025	1026	1027	1028	1029	1030	1031
2010	1032	1033	1034	1035	1036	1037	1038	1039
2020	1040	1041	1042	1043	1044	1045	1046	1047
2030	1048	1049	1050	1051	1052	1053	1054	1055
2040	1056	1057	1058	1059	1060	1061	1062	1063
2050	1064	1065	1066	1067	1068	1069	1070	1071
2060	1072	1073	1074	1075	1076	1077	1078	1079
2070	1080	1081	1082	1083	1084	1085	1086	1087
2100	1088	1089	1090	1091	1092	1093	1094	1095
2100	1096	1097	1098	1099	1100	1101	1102	1103
2120	1104	1105	1106	1107	1108	1109	1110	1111
2130	1112	1113	1114	1115	1116	1117	1118	1119
2140	1120	1121	1122	1123	1124	1125	1126	1127
2150	1128	1129	1130	1131	1132	1133	1134	1135
2160	1136	1137	1138	1139	1140	1141	1142	1143
2170	1144	1145	1146	1147	1148	1149	1150	1151
2200	1152	1153	1154	1155	1156	1157	1158	1159
2210	1160	1161	1162	1163	1164	1165	1166	1167
2220	1168	1169	1170	1171	1172	1173	1174	1175
2230	1176	1177	1178	1179	1180	1181	1182	1183
2240	1184	1185	1186	1187	1188	1189	1190	1191
2250	1192	1193	1194	1195	1196	1197	1198	1199
2260	1200	1201	1202	1203	1204	1205	1206	1207
2270	1208	1209	1210	1211	1212	1213	1214	1215
2300	1216	1217	1218	1219	1220	1221	1222	1223
2310	1224	1225	1226	1227	1228	1229	1230	1231
2320	1232	1233	1234	1235	1236	1237	1238	1239
2330	1240	1241	1242	1243	1244	1245	1246	1247
2340	1248	1249	1250	1251	1252	1253	1254	1255
2350	1256	1257	1258	1259	1260	1261	1262	1263
2360	1264	1265	1266	1267	1268	1269	1270	1271
2370	1272	1273	1274	1275	1276	1277	1278	1279

	0	1	2	3	4	5	6	7
2400	1280	1281	1282	1283	1284	1285	1286	1287
2410	1288	1289	1290	1291	1292	1293	1294	1295
2420	1296	1297	1298	1299	1300	1301	1302	1303
2430	1304	1305	1306	1307	1308	1309	1310	1311
2440	1312	1313	1314	1315	1316	1317	1318	1319
2450	1320	1321	1322	1323	1324	1325	1326	1327
2460	1328	1329	1330	1331	1332	1333	1334	1335
2470	1336	1337	1338	1339	1340	1341	1342	1343
2500	1344	1345	1346	1347	1348	1349	1350	1351
2510	1352	1353	1354	1355	1356	1357	1358	1359
2520	1360	1361	1362	1363	1364	1365	1366	1367
2530	1368	1369	1370	1371	1372	1373	1374	1375
2540	1376	1377	1378	1379	1380	1381	1382	1383
2550	1384	1385	1386	1387	1388	1389	1390	1391
2560	1392	1393	1394	1395	1396	1397	1398	1399
2570	1400	1401	1402	1403	1404	1405	1406	1407
2600	1408	1409	1410	1411	1412	1413	1414	1415
2610	1416	1417	1418	1419	1420	1421	1422	1423
2620	1424	1425	1426	1427	1428	1429	1430	1431
2630	1432	1433	1434	1435	1436	1437	1438	1439
2640	1440	1441	1442	1443	1444	1445	1446	1447
2650	1448	1449	1450	1451	1452	1453	1454	1455
2660	1456	1457	1458	1459	1460	1461	1462	1463
2670	1464	1465	1466	1467	1468	1469	1470	1471
2700	1472	1473	1474	1475	1476	1477	1478	1479
2710	1480	1481	1482	1483	1484	1485	1486	1487
2720	1488	1489	1490	1491	1492	1493	1494	1495
2730	1496	1497	1498	1499	1500	1501	1502	1503
2740	1504	1505	1506	1507	1508	1509	1510	1511
2750	1512	1513	1514	1515	1516	1517	1518	1519
2760	1520	1521	1522	1523	1524	1525	1526	1527
2770	1528	1529	1530	1531	1532	1533	1534	1535

2000 1024
to to
2777 1535
(Octal) (Decimal)

Octal Decimal
10000 4096
20000 8192
30000 12288
40000 16384
50000 20480
60000 24576
70000 28672

	0	1	2	3	4	5	6	7
3000	1536	1537	1538	1539	1540	1541	1542	1543
3010	1544	1545	1546	1547	1548	1549	1550	1551
3020	1552	1553	1554	1555	1556	1557	1558	1559
3030	1560	1561	1562	1563	1564	1565	1566	1567
3040	1568	1569	1570	1571	1572	1573	1574	1575
3050	1576	1577	1578	1579	1580	1581	1582	1583
3060	1584	1585	1586	1587	1588	1589	1590	1591
3070	1592	1593	1594	1595	1596	1597	1598	1599
3100	1600	1601	1602	1603	1604	1605	1606	1607
3110	1608	1609	1610	1611	1612	1613	1614	1615
3120	1616	1617	1618	1619	1620	1621	1622	1623
3130	1624	1625	1626	1627	1628	1629	1630	1631
3140	1632	1633	1634	1635	1636	1637	1638	1639
3150	1640	1641	1642	1643	1644	1645	1646	1647
3160	1648	1649	1650	1651	1652	1653	1654	1655
3170	1656	1657	1658	1659	1660	1661	1662	1663
3200	1664	1665	1666	1667	1668	1669	1670	1671
3210	1672	1673	1674	1675	1676	1677	1678	1679
3220	1680	1681	1682	1683	1684	1685	1686	1687
3230	1688	1689	1690	1691	1692	1693	1694	1695
3240	1696	1697	1698	1699	1700	1701	1702	1703
3250	1704	1705	1706	1707	1708	1709	1710	1711
3260	1712	1713	1714	1715	1716	1717	1718	1719
3270	1720	1721	1722	1723	1724	1725	1726	1727
3300	1728	1729	1730	1731	1732	1733	1734	1735
3310	1736	1737	1738	1739	1740	1741	1742	1743
3320	1744	1745	1746	1747	1748	1749	1750	1751
3330	1752	1753	1754	1755	1756	1757	1758	1759
3340	1760	1761	1762	1763	1764	1765	1766	1767
3350	1768	1769	1770	1771	1772	1773	1774	1775
3360	1776	1777	1778	1779	1780	1781	1782	1783
3370	1784	1785	1786	1787	1788	1789	1790	1791

	0	1	2	3	4	5	6	7
3400	1792	1793	1794	1795	1796	1797	1798	1799
3410	1800	1801	1802	1803	1804	1805	1806	1807
3420	1808	1809	1810	1811	1812	1813	1814	1815
3430	1816	1817	1818	1819	1820	1821	1822	1823
3440	1824	1825	1826	1827	1828	1829	1830	1831
3450	1832	1833	1834	1835	1836	1837	1838	1839
3460	1840	1841	1842	1843	1844	1845	1846	1847
3470	1848	1849	1850	1851	1852	1853	1854	1855
3500	1856	1857	1858	1859	1860	1861	1862	1863
3510	1864	1865	1866	1867	1868	1869	1870	1871
3520	1872	1873	1874	1875	1876	1877	1878	1879
3530	1880	1881	1882	1883	1884	1885	1886	1887
3540	1888	1889	1890	1891	1892	1893	1894	1895
3550	1896	1897	1898	1899	1900	1901	1902	1903
3560	1904	1905	1906	1907	1908	1909	1910	1911
3570	1912	1913	1914	1915	1916	1917	1918	1919
3600	1920	1921	1922	1923	1924	1925	1926	1927
3610	1928	1929	1930	1931	1932	1933	1934	1935
3620	1936	1937	1938	1939	1940	1941	1942	1943
3630	1944	1945	1946	1947	1948	1949	1950	1951
3640	1952	1953	1954	1955	1956	1957	1958	1959
3650	1960	1961	1962	1963	1964	1965	1966	1967
3660	1968	1969	1970	1971	1972	1973	1974	1975
3670	1976	1977	1978	1979	1980	1981	1982	1983
3700	1984	1985	1986	1987	1988	1989	1990	1991
3710	1992	1993	1994	1995	1996	1997	1998	1999
3720	2000	2001	2002	2003	2004	2005	2006	2007
3730	2008	2009	2010	2011	2012	2013	2014	2015
3740	2016	2017	2018	2019	2020	2021	2022	2023
3750	2024	2025	2026	2027	2028	2029	2030	2031
3760	2032	2033	2034	2035	2036	2037	2038	2039
3770	2040	2041	2042	2043	2044	2045	2046	2047

OCTAL-DECIMAL INTEGER CONVERSION TABLE

[illegible]

OCTAL-DECIMAL INTEGER CONVERSION TABLE

	0	1	2	3	4	5	6	7
6000	3072	3073	3074	3075	3076	3077	3078	3079
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6040	3104	3105	3106	3107	3108	3109	3110	3111
6050	3112	3113	3114	3115	3116	3117	3118	3119
6060	3120	3121	3122	3123	3124	3125	3126	3127
6070	3128	3129	3130	3131	3132	3133	3134	3135
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6110	3144	3145	3146	3147	3148	3149	3150	3151
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6130	3160	3161	3162	3163	3164	3165	3166	3167
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6150	3176	3177	3178	3179	3180	3181	3182	3183
6160	3184	3185	3186	3187	3188	3189	3190	3191
6170	3192	3193	3194	3195	3196	3197	3198	3199
6200	3200	3201	3202	3203	3204	3205	3206	3207
6210	3208	3209	3210	3211	3212	3213	3214	3215
6220	3216	3217	3218	3219	3220	3221	3222	3223
6230	3224	3225	3226	3227	3228	3229	3230	3231
6240	3232	3233	3234	3235	3236	3237	3238	3239
6250	3240	3241	3242	3243	3244	3245	3246	3247
6260	3248	3249	3250	3251	3252	3253	3254	3255
6270	3256	3257	3258	3259	3260	3261	3262	3263
6300	3264	3265	3266	3267	3268	3269	3270	3271
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6340	3296	3297	3298	3299	3300	3301	3302	3303
6350	3304	3305	3306	3307	3308	3309	3310	3311
6360	3312	3313	3314	3315	3316	3317	3318	3319
6370	3320	3321	3322	3323	3324	3325	3326	3327

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6420	3344	3345	3346	3347	3348	3349	3350	3351
6430	3352	3353	3354	3355	3356	3357	3358	3359
6440	3360	3361	3362	3363	3364	3365	3366	3367
6450	3368	3369	3370	3371	3372	3373	3374	3375
6460	3376	3377	3378	3379	3380	3381	3382	3383
6470	3384	3385	3386	3387	3388	3389	3390	3391
6500	3392	3393	3394	3395	3396	3397	3398	3399
6510	3400	3401	3402	3403	3404	3405	3406	3407
6520	3408	3409	3410	3411	3412	3413	3414	3415
6530	3416	3417	3418	3419	3420	3421	3422	3423
6540	3424	3425	3426	3427	3428	3429	3430	3431
6550	3432	3433	3434	3435	3436	3437	3438	3439
6560	3440	3441	3442	3443	3444	3445	3446	3447
6570	3448	3449	3450	3451	3452	3453	3454	3455
6600	3456	3457	3458	3459	3460	3461	3462	3463
6610	3464	3465	3466	3467	3468	3469	3470	3471
6620	3472	3473	3474	3475	3476	3477	3478	3479
6630	3480	3481	3482	3483	3484	3485	3486	3487
6640	3488	3489	3490	3491	3492	3493	3494	3495
6650	3496	3497	3498	3499	3500	3501	3502	3503
6660	3504	3505	3506	3507	3508	3509	3510	3511
6670	3512	3513	3514	3515	3516	3517	3518	3519
6700	3520	3521	3522	3523	3524	3525	3526	3527
6710	3528	3529	3530	3531	3532	3533	3534	3535
6720	3536	3537	3538	3539	3540	3541	3542	3543
6730	3544	3545	3546	3547	3548	3549	3550	3551
6740	3552	3553	3554	3555	3556	3557	3558	3559
6750	3560	3561	3562	3563	3564	3565	3566	3567
6760	3568	3569	3570	3571	3572	3573	3574	3575
6770	3576	3577	3578	3579	3580	3581	3582	3583

6000 3072
to to
6777 3583
(Octal) (Decimal)

Octal Decimal
10000 4096
20000 8192
30000 12288
40000 16384
50000 20480
60000 24576
70000 28672

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7000	3584	3585	3586	3587	3588	3589	3590	3591
7010	3592	3593	3594	3595	3596	3597	3598	3599
7020	3600	3601	3602	3603	3604	3605	3606	3607
7030	3608	3609	3610	3611	3612	3613	3614	3615
7040	3616	3617	3618	3619	3620	3621	3622	3623
7050	3624	3625	3626	3627	3628	3629	3630	3631
7060	3632	3633	3634	3635	3636	3637	3638	3639
7070	3640	3641	3642	3643	3644	3645	3646	3647
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7110	3656	3657	3658	3659	3660	3661	3662	3663
7120	3664	3665	3666	3667	3668	3669	3670	3671
7130	3672	3673	3674	3675	3676	3677	3678	3679
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7150	3688	3689	3690	3691	3692	3693	3694	3695
7160	3696	3697	3698	3699	3700	3701	3702	3703
7170	3704	3705	3706	3707	3708	3709	3710	3711
7200	3712	3713	3714	3715	3716	3717	3718	3719
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7230	3736	3737	3738	3739	3740	3741	3742	3743
7240	3744	3745	3746	3747	3748	3749	3750	3751
7250	3752	3753	3754	3755	3756	3757	3758	3759
7260	3760	3761	3762	3763	3764	3765	3766	3767
7270	3768	3769	3770	3771	3772	3773	3774	3775
7300	3776	3777	3778	3779	3780	3781	3782	3783
7310	3784	3785	3786	3787	3788	3789	3790	3791
7320	3792	3793	3794	3795	3796	3797	3798	3799
7330	3800	3801	3802	3803	3804	3805	3806	3807
7340	3808	3809	3810	3811	3812	3813	3814	3815
7350	3816	3817	3818	3819	3820	3821	3822	3823
7360	3824	3825	3826	3827	3828	3829	3830	3831
7370	3832	3833	3834	3835	3836	3837	3838	3839

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7400	3840	3841	3842	3843	3844	3845	3846	3847
7410	3848	3849	3850	3851	3852	3853	3854	3855
7420	3856	3857	3858	3859	3860	3861	3862	3863
7430	3864	3865	3866	3867	3868	3869	3870	3871
7440	3872	3873	3874	3875	3876	3877	3878	3879
7450	3880	3881	3882	3883	3884	3885	3886	3887
7460	3888	3889	3890	3891	3892	3893	3894	3895
7470	3896	3897	3898	3899	3900	3901	3902	3903
7500	3904	3905	3906	3907	3908	3909	3910	3911
7510	3912	3913	3914	3915	3916	3917	3918	3919
7520	3920	3921	3922	3923	3924	3925	3926	3927
7530	3928	3929	3930	3931	3932	3933	3934	3935
7540	3936	3937	3938	3939	3940	3941	3942	3943
7550	3944	3945	3946	3947	3948	3949	3950	3951
7560	3952	3953	3954	3955	3956	3957	3958	3959
7570	3960	3961	3962	3963	3964	3965	3966	3967
7600	3968	3969	3970	3971	3972	3973	3974	3975
7610	3976	3977	3978	3979	3980	3981	3982	3983
7620	3984	3985	3986	3987	3988	3989	3990	3991
7630	3992	3993	3994	3995	3996	3997	3998	3999
7640	4000	4001	4002	4003	4004	4005	4006	4007
7650	4008	4009	4010	4011	4012	4013	4014	4015
7660	4016	4017	4018	4019	4020	4021	4022	4023
7670	4024	4025	4026	4027	4028	4029	4030	4031
7700	4032	4033	4034	4035	4036	4037	4038	4039
7710	4040	4041	4042	4043	4044	4045	4046	4047
7720	4048	4049	4050	4051	4052	4053	4054	4055
7730	4056	4057	4058	4059	4060	4061	4062	4063
7740	4064	4065	4066	4067	4068	4069	4070	4071
7750	4072	4073	4074	4075	4076	4077	4078	4079
7760	4080	4081	4082	4083	4084	4085	4086	4087
7770	4088	4089	4090	4091	4092	4093	4094	4095

7000 3584
to to
7777 4095
(Octal) (Decimal)

OCTAL-DECIMAL FRACTION CONVERSION TABLE

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
000	000000	100	125000	200	250000	300	375000
001	001953	101	126953	201	251953	301	376953
002	003906	102	128906	202	253906	302	378906
003	005859	103	130859	203	255859	303	380859
004	007812	104	132812	204	257812	304	382812
005	009765	105	134765	205	259765	305	384765
006	011718	106	136718	206	261718	306	386718
007	013671	107	138671	207	263671	307	388671
010	015625	110	140625	210	265625	310	390625
011	017578	111	142578	211	267578	311	392578
012	019531	112	144531	212	269531	312	394531
013	021484	113	146484	213	271484	313	396484
014	023437	114	148437	214	273437	314	398437
015	025390	115	150390	215	275390	315	400390
016	027343	116	152343	216	277343	316	402343
017	029296	117	154296	217	279296	317	404296
020	031250	120	156250	220	281250	320	406250
021	033203	121	158203	221	283203	321	408203
022	035156	122	160156	222	285156	322	410156
023	037109	123	162109	223	287109	323	412109
024	039062	124	164062	224	289062	324	414062
025	041015	125	166015	225	291015	325	416015
026	042968	126	167968	226	292968	326	417968
027	044921	127	169921	227	294921	327	419921
030	046875	130	171875	230	296875	330	421875
031	048828	131	173828	231	298828	331	423828
032	050781	132	175781	232	300781	332	425781
033	052734	133	177734	233	302734	333	427734
034	054687	134	179687	234	304687	334	429687
035	056640	135	181640	235	306640	335	431640
036	058593	136	183593	236	308593	336	433593
037	060546	137	185546	237	310546	337	435546
040	062500	140	187500	240	312500	340	437500
041	064453	141	189453	241	314453	341	439453
042	066406	142	191406	242	316406	342	441406
043	068359	143	193359	243	318359	343	443359
044	070312	144	195312	244	320312	344	445312
045	072265	145	197265	245	322265	345	447265
046	074218	146	199218	246	324218	346	449218
047	076171	147	201171	247	326171	347	451171
050	078125	150	203125	250	328125	350	453125
051	080078	151	205078	251	330078	351	455078
052	082031	152	207031	252	332031	352	457031
053	083984	153	208984	253	333984	353	458984
054	085937	154	210937	254	335937	354	460937
055	087890	155	212890	255	337890	355	462890
056	089843	156	214843	256	339843	356	464843
057	091796	157	216796	257	341796	357	466796
060	093750	160	218750	260	343750	360	468750
061	095703	161	220703	261	345703	361	470703
062	097656	162	222656	262	347656	362	472656
063	099609	163	224609	263	349609	363	474609
064	101562	164	226562	264	351562	364	476562
065	103515	165	228515	265	353515	365	478515
066	105468	166	230468	266	355468	366	480468
067	107421	167	232421	267	357421	367	482421
070	109375	170	234375	270	359375	370	484375
071	111328	171	236328	271	361328	371	486328
072	113281	172	238281	272	363281	372	488281
073	115234	173	240234	273	365234	373	490234
074	117187	174	242187	274	367187	374	492187
075	119140	175	244140	275	369140	375	494140
076	121093	176	246093	276	371093	376	496093
077	123046	177	248046	277	373046	377	498046

OCTAL-DECIMAL FRACTION CONVERSION TABLE

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
000000	000000	000100	000244	000200	000488	000300	000732
000001	000003	000101	000247	000201	000492	000301	000736
000002	000007	000102	000251	000202	000495	000302	000740
000003	000011	000103	000255	000203	000499	000303	000743
000004	000015	000104	000259	000204	000503	000304	000747
000005	000019	000105	000263	000205	000507	000305	000751
000006	000022	000106	000267	000206	000511	000306	000755
000007	000026	000107	000270	000207	000514	000307	000759
000010	000030	000110	000274	000210	000518	000310	000762
000011	000034	000111	000278	000211	000522	000311	000766
000012	000038	000112	000282	000212	000526	000312	000770
000013	000041	000113	000286	000213	000530	000313	000774
000014	000045	000114	000289	000214	000534	000314	000778
000015	000049	000115	000293	000215	000537	000315	000782
000016	000053	000116	000297	000216	000541	000316	000785
000017	000057	000117	000301	000217	000545	000317	000789
000020	000061	000120	000305	000220	000549	000320	000793
000021	000064	000121	000308	000221	000553	000321	000797
000022	000068	000122	000312	000222	000556	000322	000801
000023	000072	000123	000316	000223	000560	000323	000805
000024	000076	000124	000320	000224	000564	000324	000808
000025	000080	000125	000324	000225	000568	000325	000812
000026	000083	000126	000328	000226	000572	000326	000816
000027	000087	000127	000331	000227	000576	000327	000820
000030	000091	000130	000335	000230	000579	000330	000823
000031	000095	000131	000339	000231	000583	000331	000827
000032	000099	000132	000343	000232	000587	000332	000831
000033	000102	000133	000347	000233	000591	000333	000835
000034	000106	000134	000350	000234	000595	000334	000839
000035	000110	000135	000354	000235	000598	000335	000843
000036	000114	000136	000358	000236	000602	000336	000846
000037	000118	000137	000362	000237	000606	000337	000850
000040	000122	000140	000366	000240	000610	000340	000854
000041	000125	000141	000370	000241	000614	000341	000858
000042	000129	000142	000373	000242	000617	000342	000862
000043	000133	000143	000377	000243	000621	000343	000865
000044	000137	000144	000381	000244	000625	000344	000869
000045	000141	000145	000385	000245	000629	000345	000873
000046	000144	000146	000389	000246	000633	000346	000877
000047	000148	000147	000392	000247	000637	000347	000881
000050	000152	000150	000396	000250	000640	000350	000885
000051	000156	000151	000400	000251	000644	000351	000888
000052	000160	000152	000404	000252	000648	000352	000892
000053	000164	000153	000408	000253	000652	000353	000896
000054	000167	000154	000411	000254	000656	000354	000900
000055	000171	000155	000415	000255	000659	000355	000904
000056	000175	000156	000419	000256	000663	000356	000907
000057	000179	000157	000423	000257	000667	000357	000911
000060	000183	000160	000427	000260	000671	000360	000915
000061	000186	000161	000431	000261	000675	000361	000919
000062	000190	000162	000434	000262	000679	000362	000923
000063	000194	000163	000438	000263	000682	000363	000926
000064	000198	000164	000442	000264	000686	000364	000930
000065	000202	000165	000446	000265	000690	000365	000934
000066	000205	000166	000450	000266	000694	000366	000938
000067	000209	000167	000453	000267	000698	000367	000942
000070	000213	000170	000457	000270	000701	000370	000946
000071	000217	000171	000461	000271	000705	000371	000949
000072	000221	000172	000465	000272	000709	000372	000953
000073	000225	000173	000469	000273	000713	000373	000957
000074	000228	000174	000473	000274	000717	000374	000961
000075	000232	000175	000476	000275	000720	000375	000965
000076	000236	000176	000480	000276	000724	000376	000968
000077	000240	000177	000484	000277	000728	000377	000972

OCTAL-DECIMAL FRACTION CONVERSION TABLE

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
000400	000976	000500	001220	000600	001464	000700	001708
000401	000980	000501	001224	000601	001468	000701	001712
000402	000984	000502	001228	000602	001472	000702	001716
000403	000988	000503	001232	000603	001476	000703	001720
000404	000991	000504	001235	000604	001480	000704	001724
000405	000995	000505	001239	000605	001483	000705	001728
000406	000999	000506	001243	000606	001487	000706	001731
000407	001003	000507	001247	000607	001491	000707	001735
000410	001007	000510	001251	000610	001495	000710	001739
000411	001010	000511	001255	000611	001499	000711	001743
000412	001014	000512	001258	000612	001502	000712	001747
000413	001018	000513	001262	000613	001506	000713	001750
000414	001022	000514	001266	000614	001510	000714	001754
000415	001026	000515	001270	000615	001514	000715	001758
000416	001029	000516	001274	000616	001518	000716	001762
000417	001033	000517	001277	000617	001522	000717	001766
000420	001037	000520	001281	000620	001525	000720	001770
000421	001041	000521	001285	000621	001529	000721	001773
000422	001045	000522	001289	000622	001533	000722	001777
000423	001049	000523	001293	000623	001537	000723	001781
000424	001052	000524	001296	000624	001541	000724	001785
000425	001056	000525	001300	000625	001544	000725	001789
000426	001060	000526	001304	000626	001548	000726	001792
000427	001064	000527	001308	000627	001552	000727	001796
000430	001068	000530	001312	000630	001556	000730	001800
000431	001071	000531	001316	000631	001560	000731	001804
000432	001075	000532	001319	000632	001564	000732	001808
000433	001079	000533	001323	000633	001567	000733	001811
000434	001083	000534	001327	000634	001571	000734	001815
000435	001087	000535	001331	000635	001575	000735	001819
000436	001091	000536	001335	000636	001579	000736	001823
000437	001094	000537	001338	000637	001583	000737	001827
000440	001098	000540	001342	000640	001586	000740	001831
000441	001102	000541	001346	000641	001590	000741	001834
000442	001106	000542	001350	000642	001594	000742	001838
000443	001110	000543	001354	000643	001598	000743	001842
000444	001113	000544	001358	000644	001602	000744	001846
000445	001117	000545	001361	000645	001605	000745	001850
000446	001121	000546	001365	000646	001609	000746	001853
000447	001125	000547	001369	000647	001613	000747	001857
000450	001129	000550	001373	000650	001617	000750	001861
000451	001132	000551	001377	000651	001621	000751	001865
000452	001136	000552	001380	000652	001625	000752	001869
000453	001140	000553	001384	000653	001628	000753	001873
000454	001144	000554	001388	000654	001632	000754	001876
000455	001148	000555	001392	000655	001636	000755	001880
000456	001152	000556	001396	000656	001640	000756	001884
000457	001155	000557	001399	000657	001644	000757	001888
000460	001159	000560	001403	000660	001647	000760	001892
000461	001163	000561	001407	000661	001651	000761	001895
000462	001167	000562	001411	000662	001655	000762	001899
000463	001171	000563	001415	000663	001659	000763	001903
000464	001174	000564	001419	000664	001663	000764	001907
000465	001178	000565	001422	000665	001667	000765	001911
000466	001182	000566	001426	000666	001670	000766	001914
000467	001186	000567	001430	000667	001674	000767	001918
000470	001190	000570	001434	000670	001678	000770	001922
000471	001194	000571	001438	000671	001682	000771	001926
000472	001197	000572	001441	000672	001686	000772	001930
000473	001201	000573	001445	000673	001689	000773	001934
000474	001205	000574	001449	000674	001693	000774	001937
000475	001209	000575	001453	000675	001697	000775	001941
000476	001213	000576	001457	000676	001701	000776	001945
000477	001216	000577	001461	000677	001705	000777	001949

ACE-S/C FUNCTIONAL DESCRIPTION

OBJECTIVES

To familiarize the student with:

- a. ACE-S/C system data flow.
- b. Major subsystem identification.
- c. Function and interface relationships of various equipment.
- d. Operating characteristics.

INTRODUCTION

The ACE-S/C Operator's Manual contains a functional description of the ACE-S/C. The student should read Chapter 1 of the ACE-S/C Operator's Manual and study the ACE-S/C system block diagram wall chart.

ACE-S/C PHYSICAL DESCRIPTION

OBJECTIVES

To familiarize the student with the physical identification and layout of the Acceptance Checkout Equipment - Spacecraft.

INTRODUCTION

GENERAL

The ACE-S/C equipment is divided into four physical areas: the control room, the computer room, the terminal facility room (usually shared by two or more ground stations), and the launch emplacement area or spacecraft test area. This arrangement provides for logical equipment grouping and separation of personnel concerned with different aspects of system operation. Certain subsystems, of necessity, cut across these physical boundaries. Portions of these subsystems will, therefore, be found in more than one of the four areas.

CONTROL ROOM EQUIPMENT

The control room contains the primary controls and displays of the ACE-S/C station. These are arranged in a series of consoles, grouped according to functional spacecraft systems, providing a central location for stimulating and monitoring the performance of each spacecraft system.

The system consoles are arranged in the following groups: (Not all groups may be used in any given ground station.)

- a. Test Conductor Console (TC).
- b. Instrumentation Console (Inst).
- c. Communications Console (Comm).
- d. Environmental Control System Console (ECS).
- e. Fuel Cell and Cryogenics Console (FC and C).
- f. Power and Sequential Console (Pwr and Seq).
- g. Guidance and Navigation Console (G&N).
- h. Stabilization and Control (Stab and Cont).
- i. Propulsion and Reaction Control System Console (Prop and RCS).

- j. Aeromedical System Console.
- k. Thermostructures Facility Console.

COMPUTER ROOM EQUIPMENT

The computer room contains the Digital Acquisition and Decommuration Equipment (DADE), the command and display computer complex, the DTVC's, a roll-chart recorder group (at some stations this may be located in the terminal facility room), magnetic tape recorders, time interface units, and the ACE-S/C station checkout equipment.

The computer complex includes two computer consoles, two compute modules (the command and display computers), three auxiliary memory modules, three auxiliary input modules, and associated peripheral equipment.

The ACE-S/C checkout equipment includes a PCM simulator, an event recorder, and several analog recorders. The computer complex console contains START modules, displays, and controls employed in ACE-S/C station checkout as well as for monitoring system performance. An event distribution, recording, and patching unit is provided to drive the computer room event displays.

Wall clocks, displaying real and countdown time, and voice communication equipment are also provided in the computer room.

TERMINAL FACILITY ROOM EQUIPMENT

The terminal facility room provides a flexible interface between the remote spacecraft test areas and the ACE-S/C stations. It also provides certain support and interfacing functions within the stations.

The terminal facility room contains the terminal patch facility, the timing group, certain alphanumeric display system units, the CUE unit, and voice communication units.

The terminal patch facility serves as the external interface for all ACE-S/C station input and output data lines. It also permits the ACE-S/C control rooms and computer rooms to be cross-patched from one system to another. (Normally, the ACE-S/C stations will operate independently of each other; however, by means of cross-patching within the terminal facility room, any computer room can operate with any control room.)

The timing group is composed of a time code generator, which drives various real-time displays in the stations, and countdown generators (one for each station), which drive countdown displays.

The SGS unit and (at locations where it is required) the DCCU are located in the terminal facility room. This equipment provides an interface between the display computer in the computer room and the CRT displays in the control room.

SPACECRAFT AND SPACECRAFT TEST AREA EQUIPMENT

The spacecraft and spacecraft test area contain the interface equipment that completes the checkout loop between the spacecraft and the ACE-S/C station. The interface equipment consists of Digital Test Command Systems (DTCS) and Digital Test Measurement Systems (DTMS).

The carry-on DTCS is physically located near the spacecraft and consists of a receiver-decoder, baseplates, and relay and DAC modules. The external DTCS and the Service Equipment (S/E) DTCS are physically located adjacent to the spacecraft. CARRY-ON
The S/E DTCS interfaces with ground support equipment in the vicinity of the spacecraft to provide remote control of command/service module or lunar excursion module. EXTERNAL

The carry-on DTMS is physically located in the spacecraft and consists of three signal conditioning and sampling units and one pulse code modulation subsystem. The S/E DTMS system is physically located adjacent to the spacecraft and consists of the external signal conditioning unit and service equipment adapter. The data interleaver is located adjacent to the spacecraft.

ACE-S/C PHYSICAL CONFIGURATION AT NORTH AMERICAN AVIATION, INC., DOWNEY, CALIFORNIA

Three ACE-S/C ground stations are installed in Building 290 at North American Aviation, Inc., to accomplish acceptance checkout of the Apollo command and service modules. The equipment locations at these stations is shown in Figure 1.

ACE-S/C PHYSICAL CONFIGURATION AT GRUMMAN AIRCRAFT ENGINEERING CORPORATION, BETHPAGE, NEW YORK

Two ground stations are located at Grumman Aircraft Engineering Corporation to test the lunar excursion module. Figure 2 shows the equipment location at this installation.

ACE-S/C PHYSICAL CONFIGURATION AT NASA MANNED SPACECRAFT CENTER, HOUSTON, TEXAS

Two ACE-S/C ground stations are installed at MSC, Houston to support the command, service, and lunar excursion modules in simulated lunar missions. These stations are installed in Building 32. The equipment layout is shown in Figure 3.

ACE-S/C PHYSICAL CONFIGURATION AT MERRITT ISLAND LAUNCH AREA, FLORIDA

Five ACE-S/C stations are located in the O&C Building at MILA to accomplish receiving and launch readiness checkout of the command, service, and lunar excursion modules. Figure 4 shows the equipment layout at this location.

UNIT	DRAWING	TITLE
18 & 23	63C507781G1	INSTRUMENTATION SYSTEM - LOW CABINETS*
19 & 20	63C507671G1	COMMUNICATION SYSTEM - LOW CABINETS
11 & 17	63C507646G1	ENVIRONMENTAL CONTROL SYSTEM - LOW CABINETS
1	63C507720G1	ENVIRONMENTAL CONTROL SYSTEM - HIGH CABINETS
12	63C507644G1	FUEL CELL AND CRYOGENICS - LOW CABINETS
2	63C507654G1	FUEL CELL AND CRYOGENICS - HIGH CABINETS
8	63E907543G1	FUEL CELL AND CRYOGENICS - HIGH CABINETS
13	63C507641G1	POWER AND SEQUENTIAL SYSTEM - LOW CABINETS
3	63C507710G1	POWER AND SEQUENTIAL SYSTEM - HIGH CABINETS
7	63E907525G1	POWER AND SEQUENTIAL SYSTEM - HIGH CABINETS
14	63C507640G1	GUIDANCE AND NAVIGATION - LOW CABINETS
4	63C507709G1	GUIDANCE AND NAVIGATION - HIGH CABINETS
15	63C507643G1	STABILIZATION AND CONTROL SYSTEM - LOW CABINETS
5	63C507652G1	STABILIZATION AND CONTROL SYSTEM - HIGH CABINETS
16	63C507648G1	PROPULSION SPS AND RCS SYSTEMS - LOW CABINETS
6	63C507679G1	PROPULSION SPS AND RCS SYSTEMS - HIGH CABINETS
10	63C507677G1	TEST CONDUCTOR CONSOLE
21 & 24	63C507658G1	EVENT STORAGE AND DISTRIBUTION UNIT/ DECOMMUTATOR DIST.
29		REAL AND COUNTDOWN WALL TIME DISPLAY
30		REAL AND COUNTDOWN WALL TIME DISPLAY
31		REAL AND COUNTDOWN WALL TIME DISPLAY

*CONTROL ROOM NO. 1 - UNIT 18 CONSISTS OF 18A1, 18A2, 18A3.
CONTROL ROOM NO. 2 - UNIT 18 CONSISTS OF 23A1, 18A1, 18A2
CONTROL ROOM NO. 3 - UNIT 18 CONSISTS OF 23A1, 18A1, 18A2

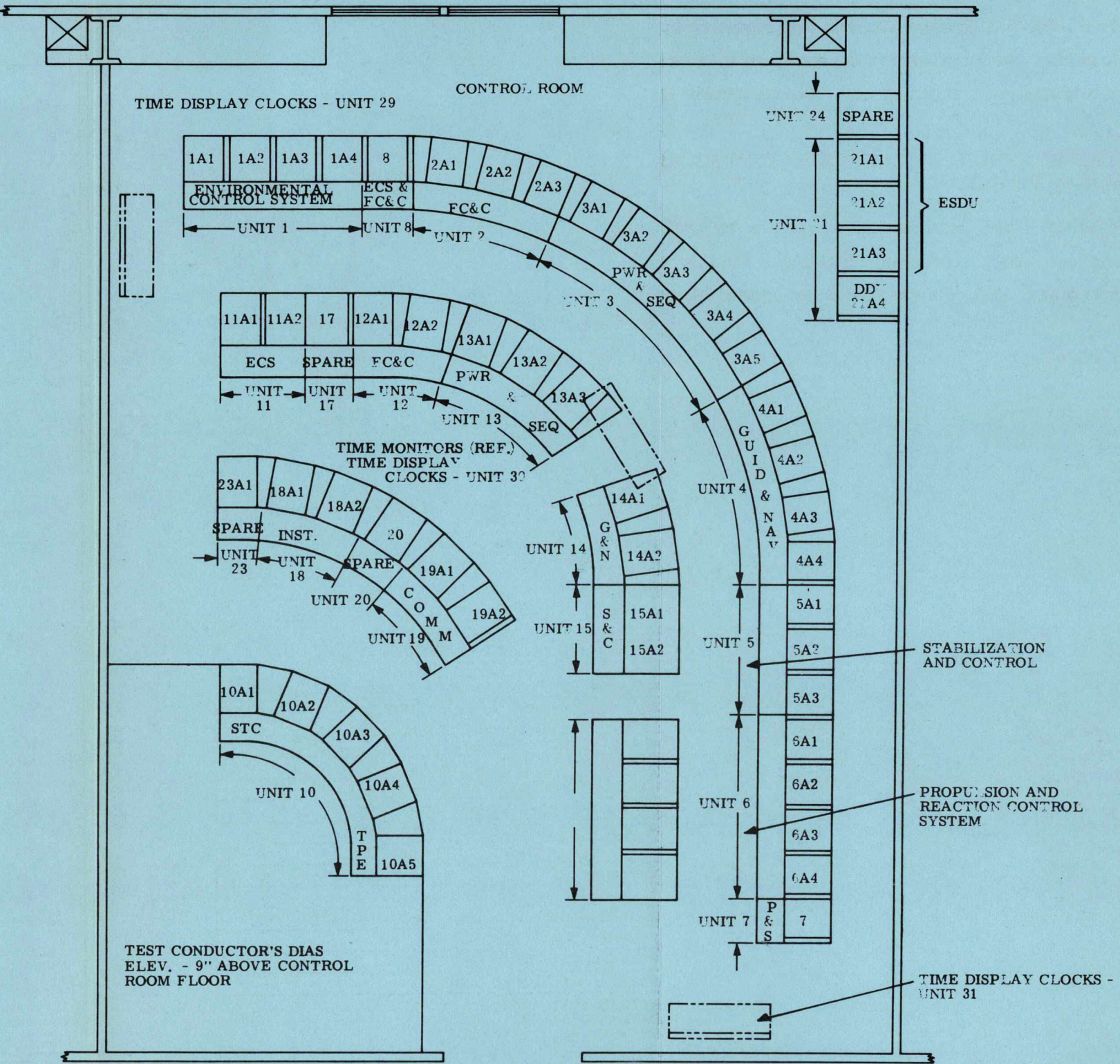
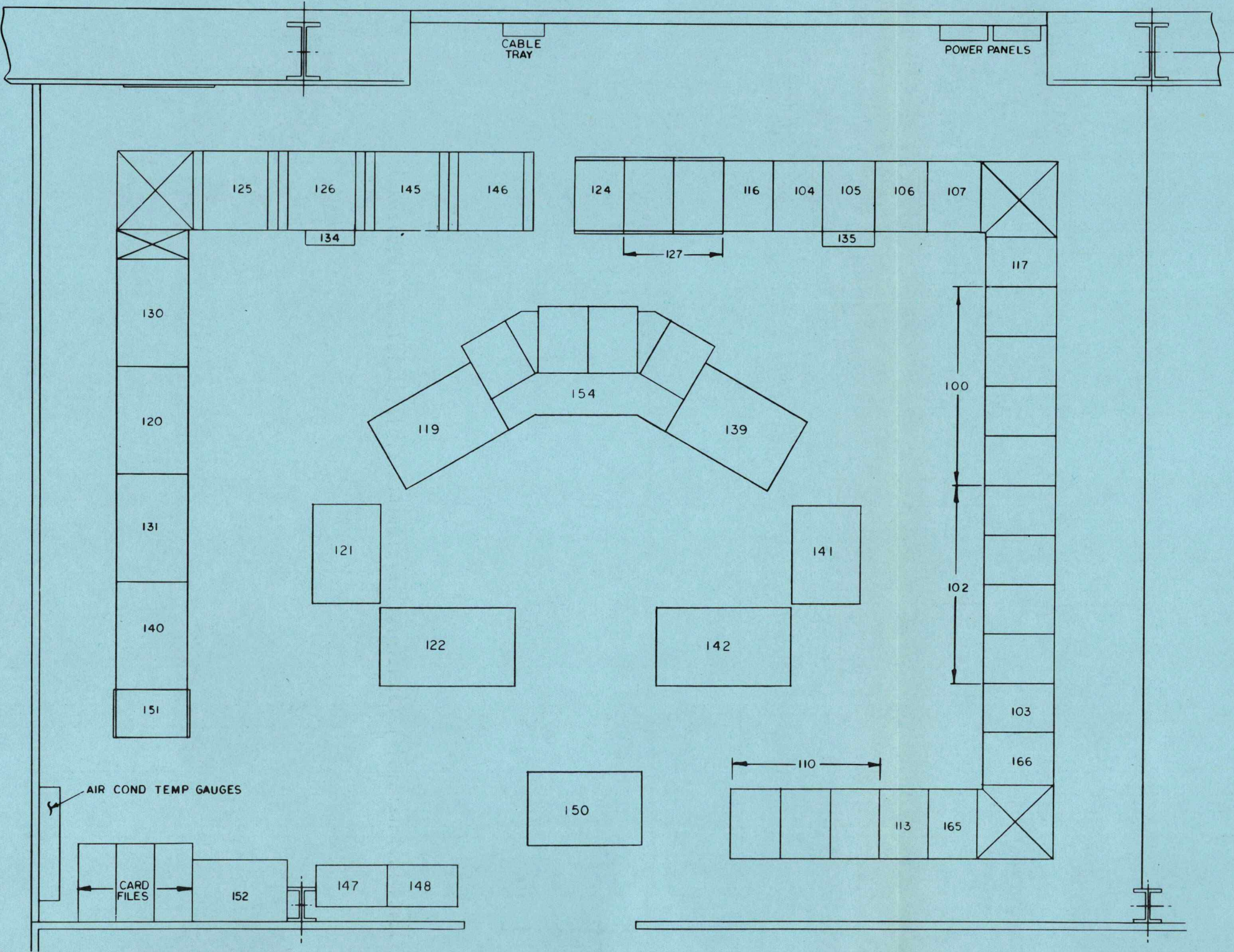
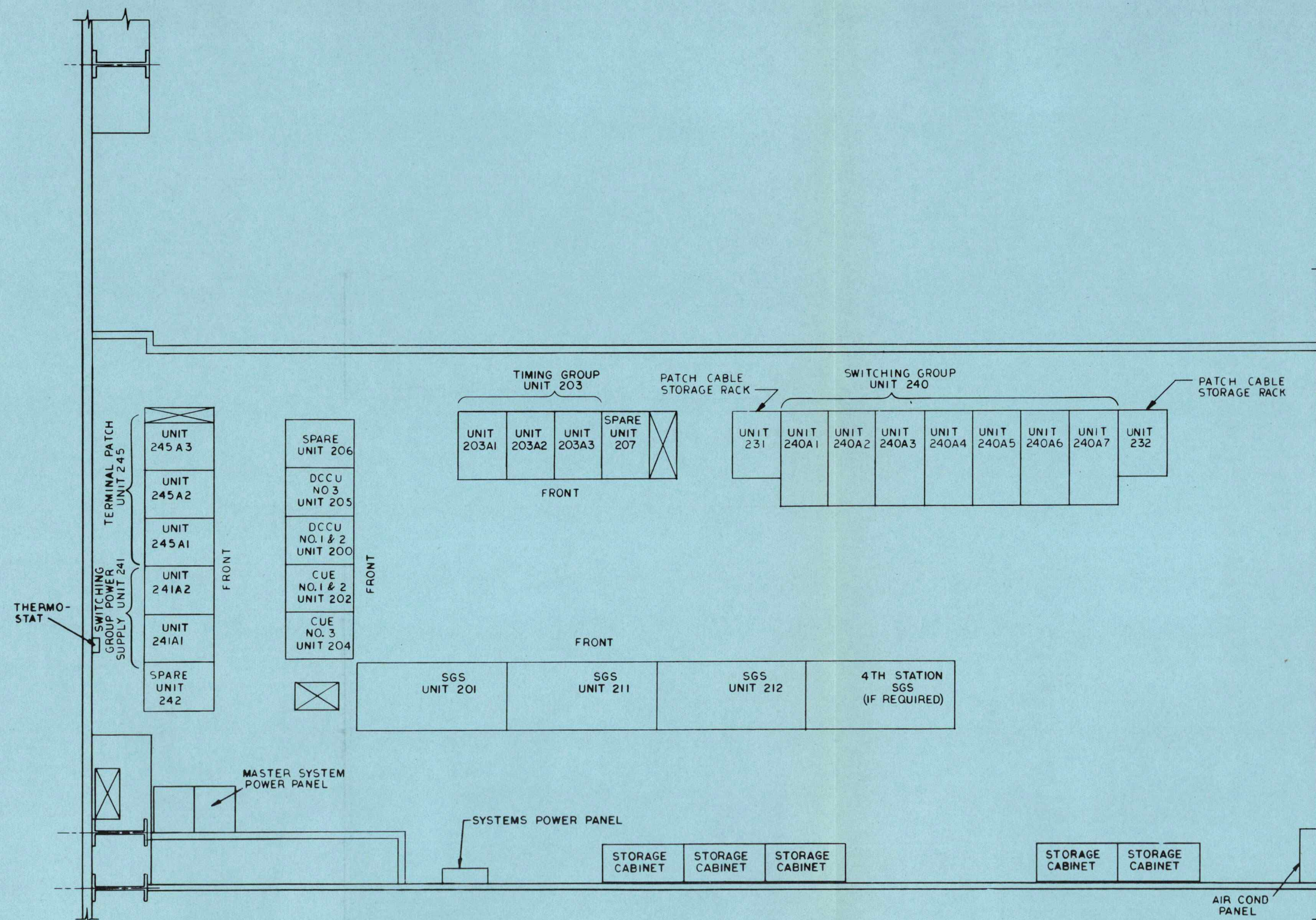


Figure 1. ACE-S/C Control Room Equipment Layout at NAA, Downey, Calif. (Sheet 1 of 3)



NO.	NO. OF ENCLOSURES	DESCRIPTION
100	4	DIGITAL ACQ. & DECOM. EQUIP. #1 & SIMULATOR
102	4	DIGITAL ACQ. & DECOM. EQUIP. #2
103	1	SPARE CABINET
104	1	VIDEO DISTRIBUTION & TAPE TRANSPORT CONTROL UNIT
105	1	MAGNETIC TAPE RECORDER/REPRODUCER
106	1	MAGNETIC TAPE RECORDER/ REPRODUCER
107	1	MAGNETIC TAPE RECORDER/REPRODUCER
110	3	ANALOG RECORDER
113	1	EVENT DISTRIBUTION RECORDING AND PATCHING
116	1	TAPE RECORDER/COMP TIME DECODER & SEARCH UNIT
117	1	COUNTDOWN GENERATOR COMPUTER INTERFACE
119	1	COMPUTER CONSOLE
120	1	COMPUTER MODULE
121	1	TYPEWRITER
122	1	CARD READER
124	1	MAGNETIC TAPE CONTROLLER
125	1	MAGNETIC TAPE TRANSPORT
126	1	MAGNETIC TAPE TRANSPORT
127	2	D. T. V. C.
130	1	INPUT/OUTPUT UNIT (3 MODULES)
131	1	MEMORY UNIT (3 MODULES)
134	1	REAL & COUNTDOWN WALL TIME DISPLAY
135	1	REAL & COUNTDOWN WALL TIME DISPLAY
139	1	COMPUTER CONSOLE
140	1	COMPUTER MODULE
141	1	TYPEWRITER
142	1	CARD READER
145	1	MAGNETIC TAPE TRANSPORT
146	1	MAGNETIC TAPE TRANSPORT
147	1	X-Y PLOTTER
148	1	X-Y PLOTTER
150	1	LINE PRINTER
151	1	PUNCH CONTROL & MAGNETIC TAPE CONTROLLER
152	1	CARD PUNCH
154	4	COMPUTER COMPLEX CONSOLE
165	1	F. M. DISCRIMINATOR UNIT
166	1	FM CALIBRATION UNIT



NOTE:
 1. 4TH STATION CUE WILL FIT INTO UNIT 204 IF REQUIRED.
 2. 4TH STATION DCCU WILL FIT INTO UNIT 206 IF REQUIRED.

Figure 1. ACE-S/C Terminal Facility Room Equipment Layout At NAA, Downey, Calif. (Sheet 3 of 3)

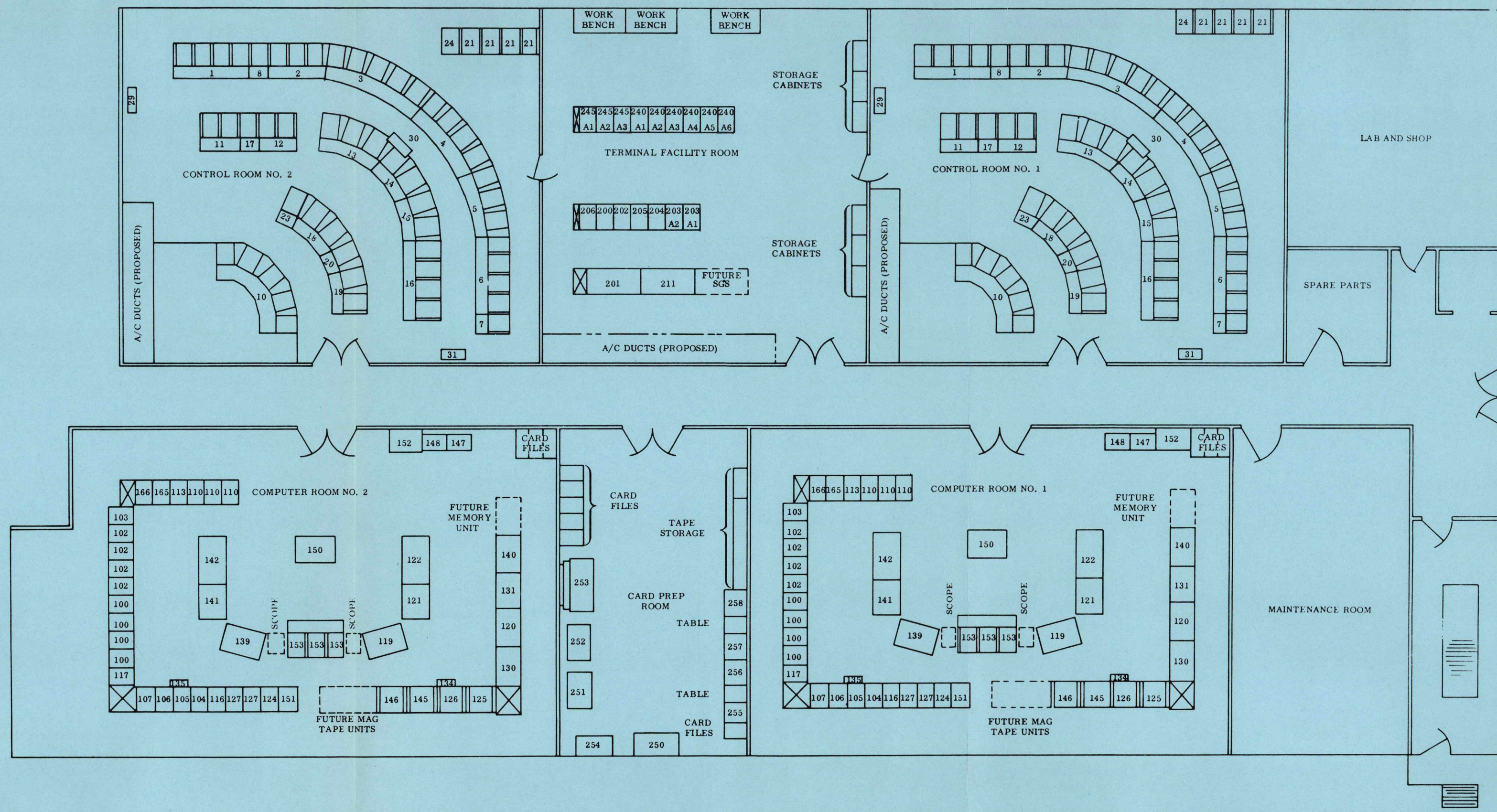


Figure 2. ACE-S/C Equipment Layout at GAEC, New York

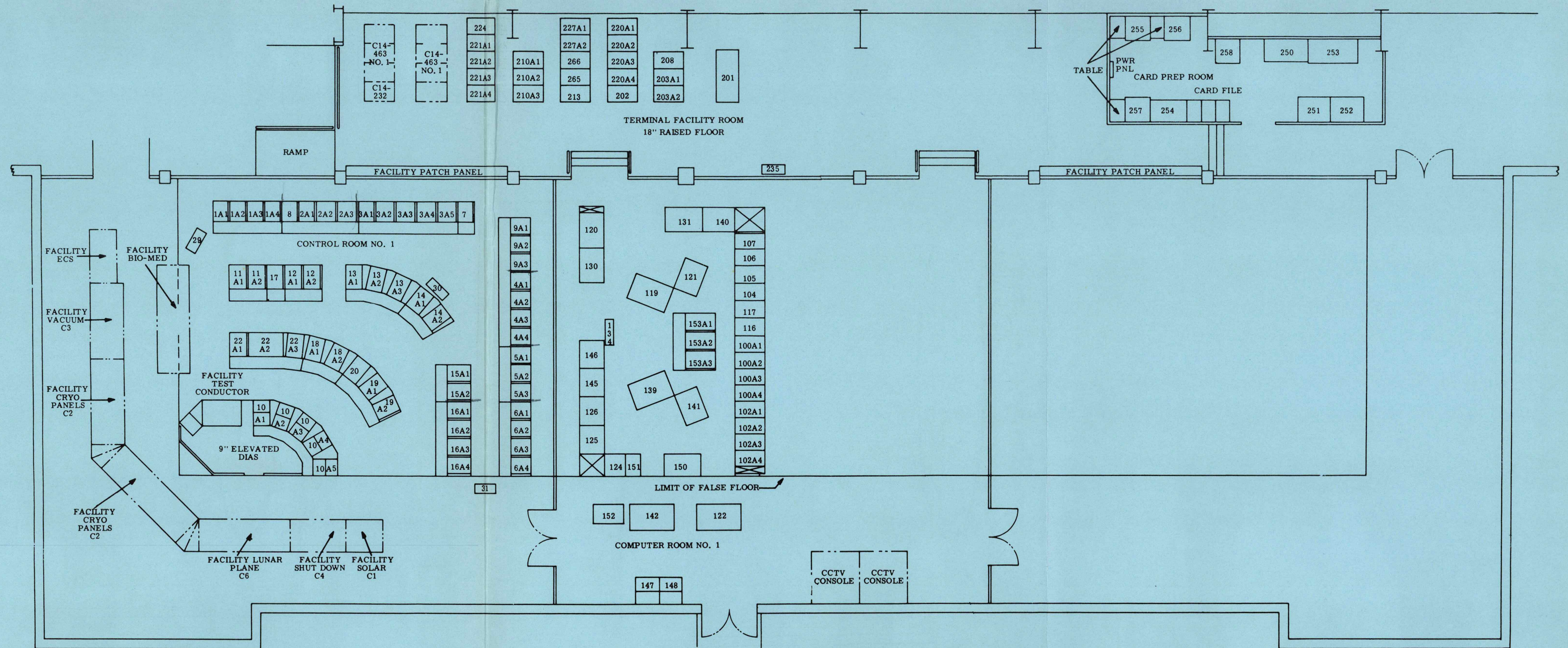


Figure 3. ACE-S/C Equipment Layout at MSC Houston, Texas

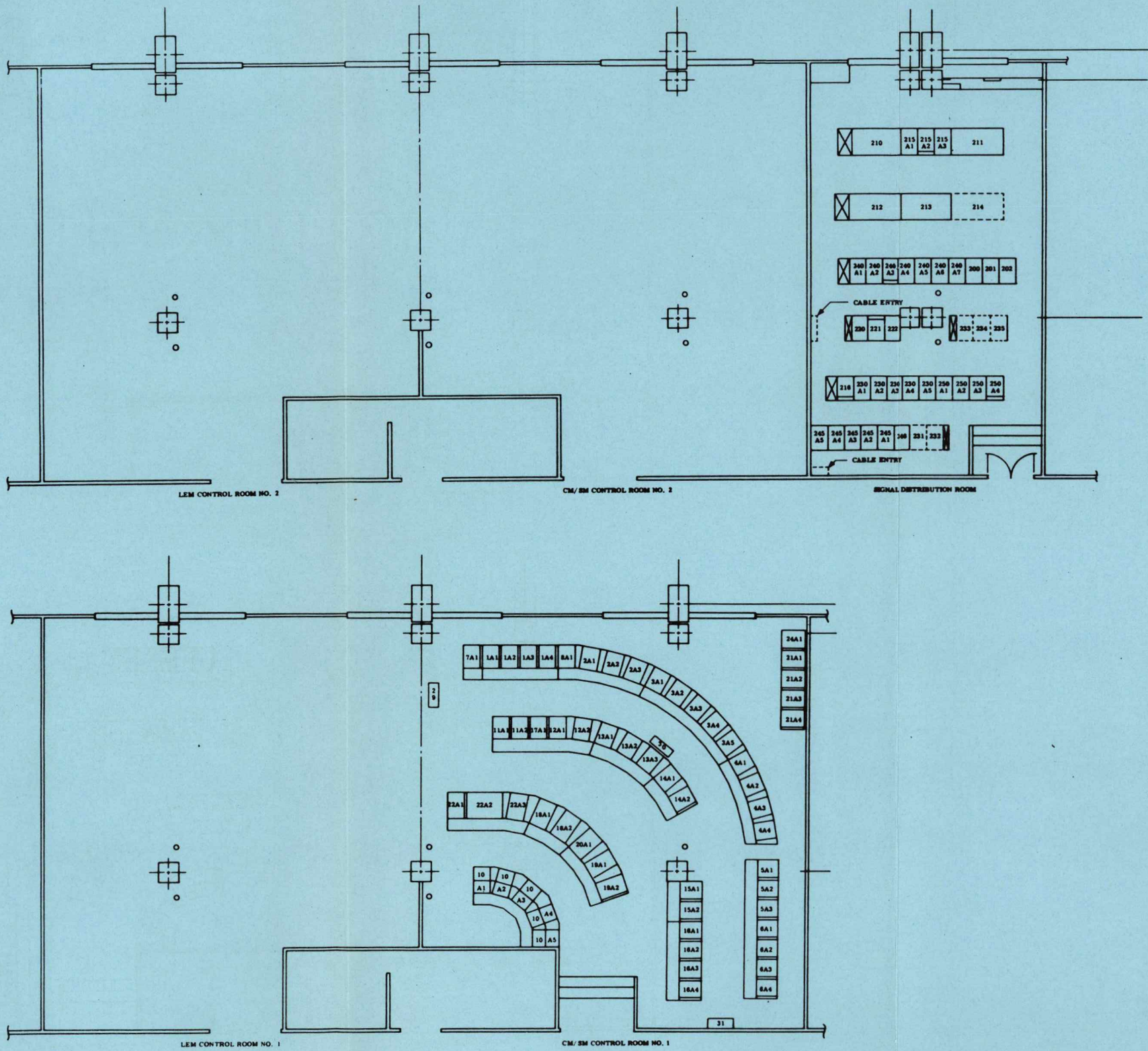


Figure 4. ACE-S/C Equipment Layout at Merritt Island Launch Area, Florida (Sheet 1 of 2)

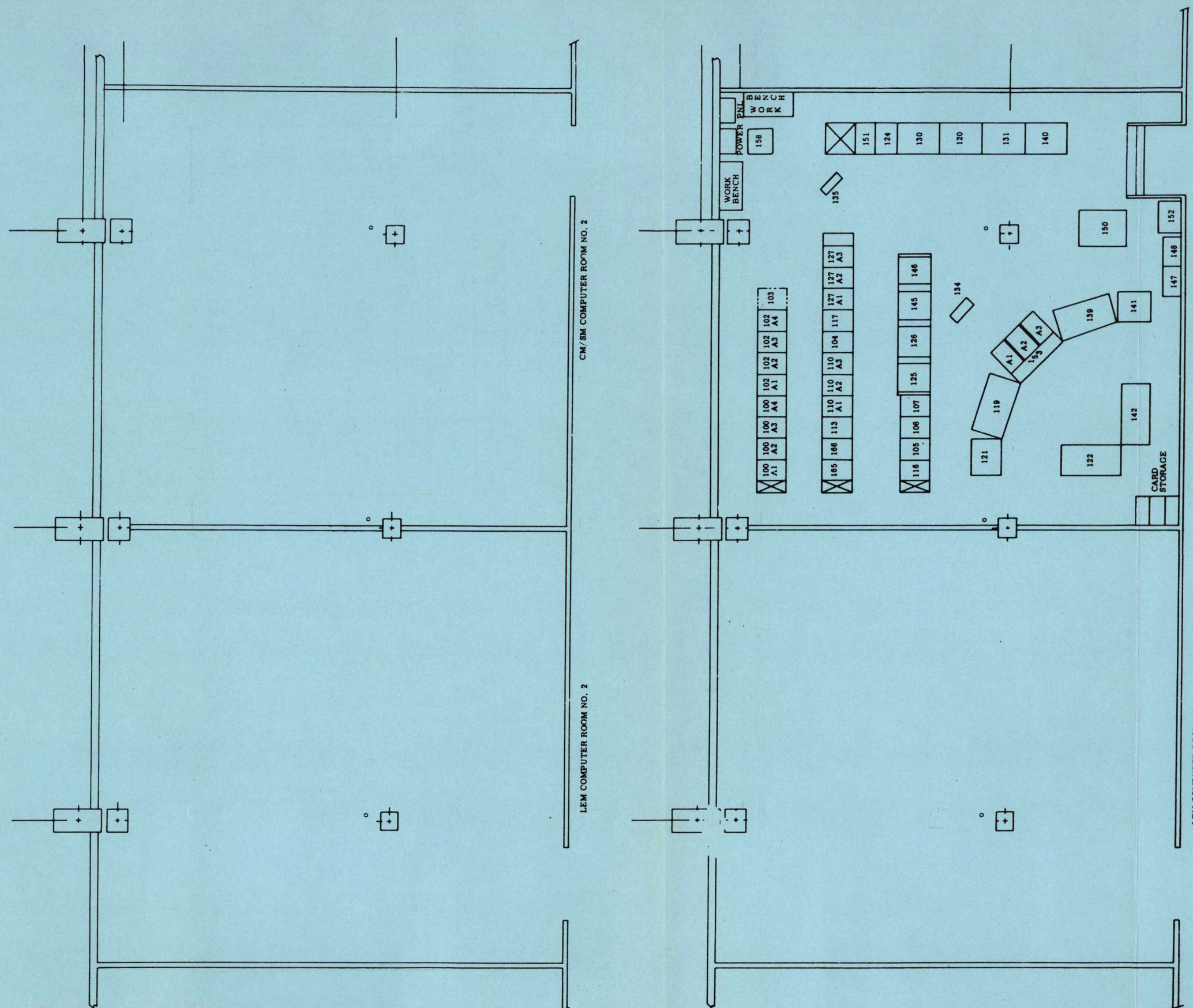


Figure 4. ACE-S/C Equipment Layout at Merritt Island Launch Area, Florida (Sheet 2 of 2)

DATA ENTRY EQUIPMENT

OBJECTIVES

To familiarize the student with:

- a. Modes of operation.
- b. Data entry/computer interface.
- c. Theory of operation (block diagram).
- d. Controls displays.
- e. Confirmation codes.

INTRODUCTION

The data entry equipment is an integral part of the uplink loop and serves as a communications link between the test operator and the ACE-S/C computer complex. This equipment permits the simultaneous initiation of individual data and/or test commands to the computer. The computer processes these inputs, generates and transmits the test commands to the Digital Test Command System (DTCS), and returns the status of the test commands to the data entry equipment for display and operator evaluation.

The data entry equipment consists of six basic units:

- a. Communications Unit Executor (CUE).
- b. Junction Box (J-Box).
- c. Relay Start (R-START).
- d. R-START (Enclosure).
- e. Computer Communications Start (C-START).
- f. Keyboard Start (K-START).

The Selection To Activate Random Testing (START) modules are mounted in the control room consoles and are connected to CUE by means of J-Boxes, which are also located in the consoles. The data entry equipment operates under program control of the uplink computer. The CUE is the heart of the data entry equipment and serves as the interface between the START modules and the computer. The CUE can be selected for any one of four modes of operation by the uplink computer. The CUE normally operates in the manual mode; whereby, the operator manually inserts a test command into a START module. The START module is then executed, the CUE interrupts the

computer main program, and then transfers the START module information into the computer memory. The remaining three modes of operation are identified as automatic mode, where the information is prestored in the START modules, and the computer interrogates specific START modules under program control; maintenance mode, where the computer can communicate with the Command Monitor Unit (CMU) via the CUE; and the standby mode, which is defined as the idling mode of the CUE.

EXPLANATION

GENERAL

The data entry equipment makes it possible for a plurality of operators to initiate, simultaneously, test commands for the uplink computer to process. The subsystem is configured as shown in Figure 1, with the various START modules being the most basic item to the system. As shown in the diagram, each J-Box can service sixteen START modules in two groups of eight each. In a similar fashion, the CUE services sixteen J-Boxes also in two groups of eight each, so that the system can accommodate a total of 256 START modules.

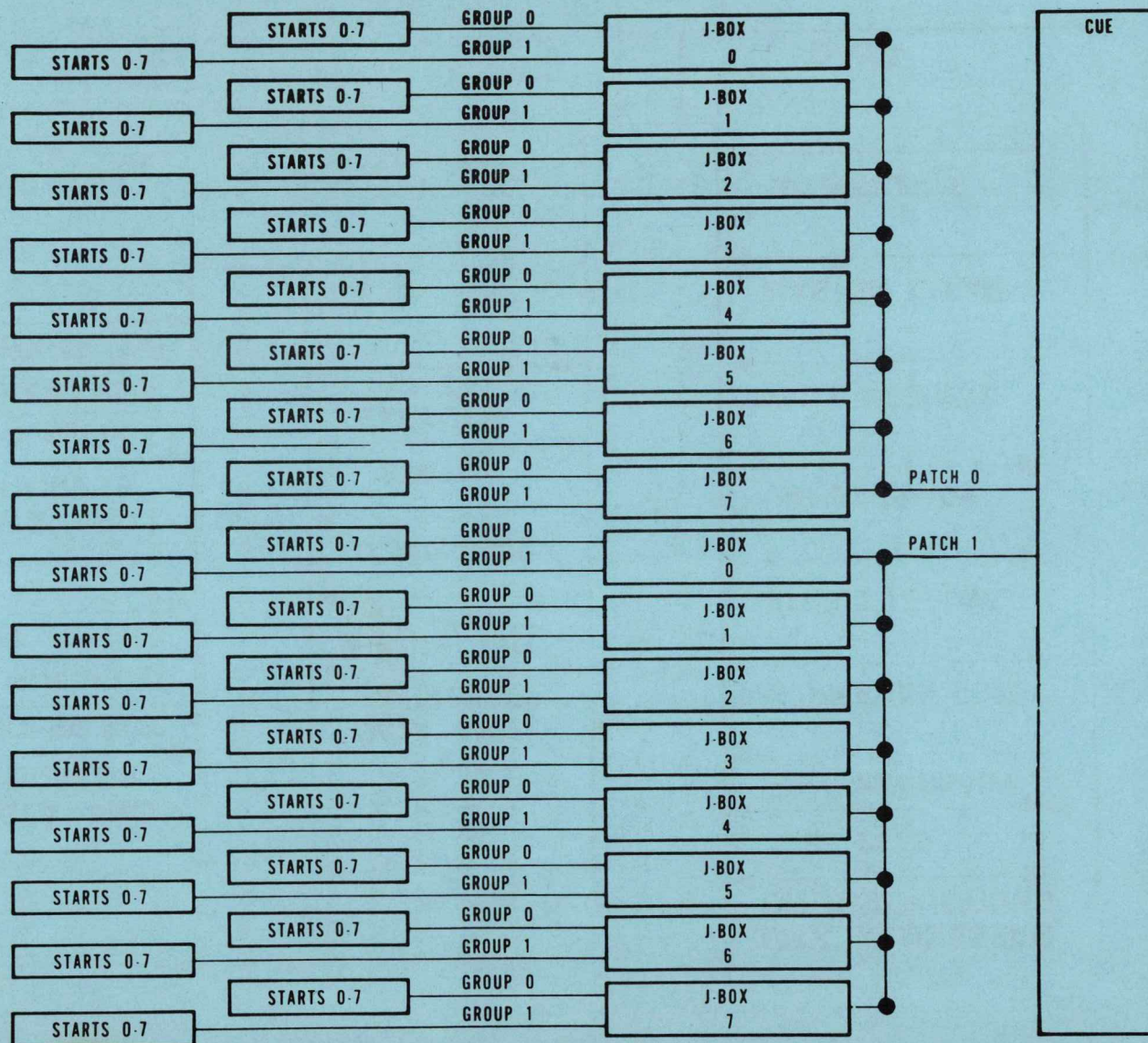
There are three distinct types of START modules: R-START modules, which provide for manual control of discrete events or for subroutine callup; C-START modules, which provide for manual selection of computer subroutines and the parameters required by the subroutines; and a single K-START module, which provides manual and automatic means of inserting information into the Apollo Guidance Computer (AGC). Refer to Section 1 of the ACE-S/C Operator's Manual for detailed operating instructions.

Figure 2 is a functional block diagram of the data entry equipment, which illustrates the functional relationships between the various components making up the data entry equipment. This figure also shows the control signal and data flow that exists between the CUE and the uplink computer.

R-START

Each R-START module provides the operator with a means of manually initiating test commands that control individual relay action in subgroups of four at a time. In other words, there is a one-to-one correspondence between a given function switch and a relay in the sensor stimulation equipment of the DTCS. The operator sets the status of the relays under his control by depressing the proper combination of function switches on the R-START modules (see Figure 3). The lower half of the back-light, split-legend

SIMPLIFIED DATA ENTRY ADDRESSING DIAGRAM



FOR TRAINING PURPOSES ONLY

FOR TRAINING PURPOSES ONLY

410-0(105)

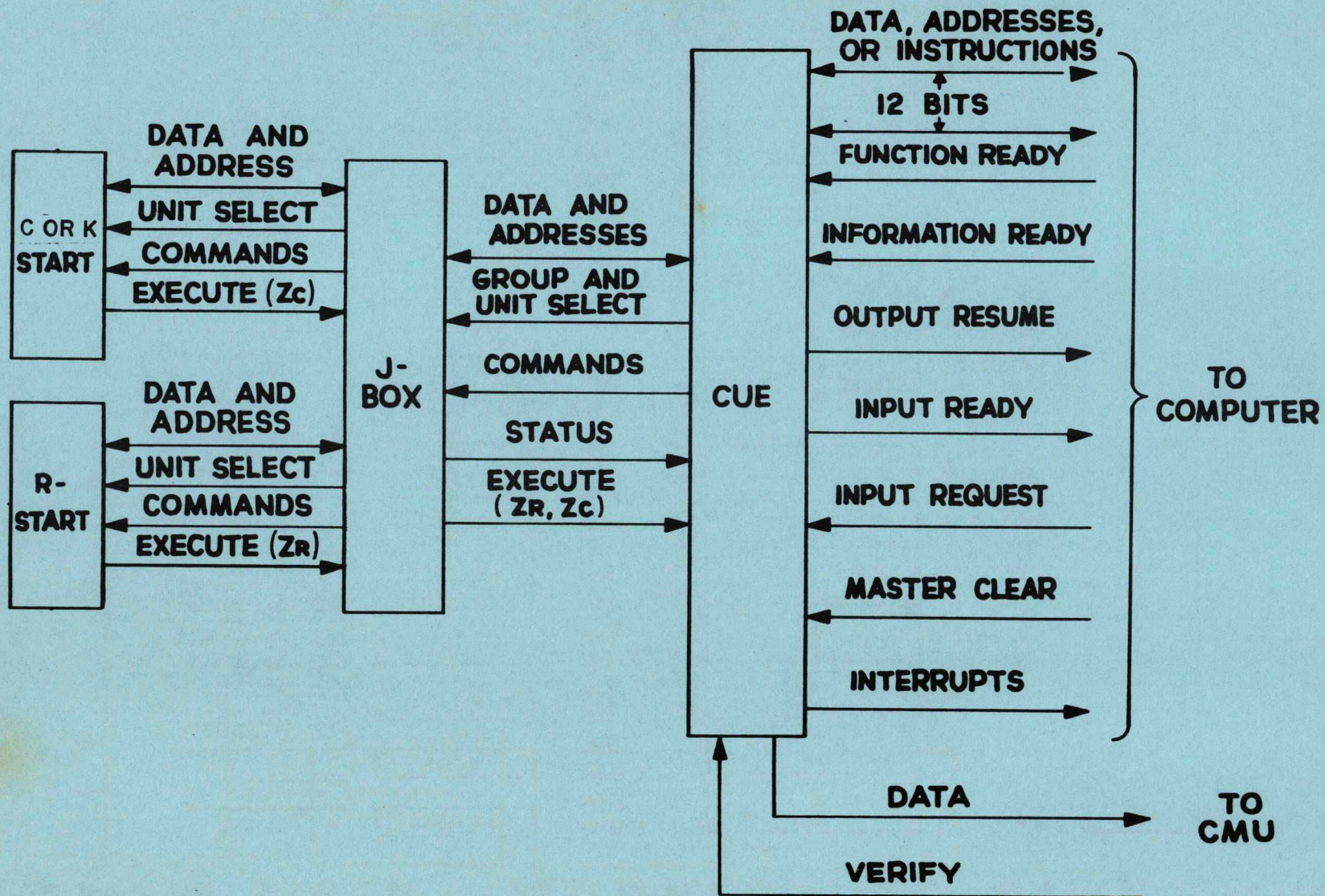


Figure 2. Data Entry Functional Block Diagram

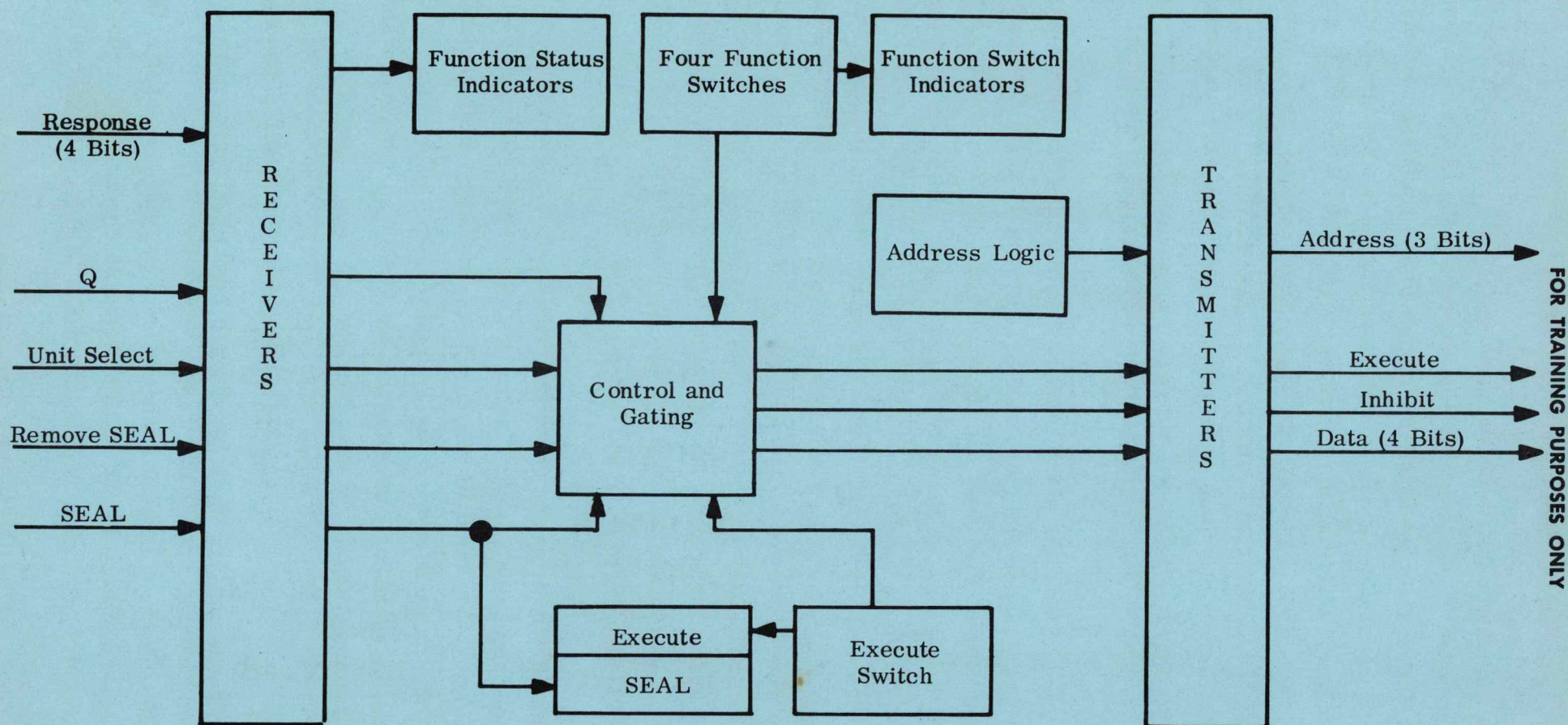


Figure 3. R-START Block Diagram

function switches illuminates to provide the operator with a visual indication of the test command just inserted. The operator then depresses the XEQ switch sending a signal to the CUE that inhibits any C-START modules from being executed until all executed R-START modules have been serviced (see Figure 3). Group and unit transmitters in the CUE generate an enabling signal that permits the R-START to transmit an execute signal to the CUE. This execute signal performs three basic functions:

- a. Stops the CUE scanner on the address of the R-START.
- b. Gates the setting of the four function switches and the three least significant bits of the module address to the J-Box.
- c. Causes the CUE to generate an Interrupt 30 to the uplink computer.

The J-Box adds the next four bits of address and the CUE adds the last or most significant bit. The four function bits from the R-START and the eight-bit scanner address are combined into a 12-bit word that is transferred to the computer on its command. Normally the response of the system to an execute will be the illumination or nonillumination of the upper half of the function switches, matching them to the state that had been set manually by the operator. The correspondence between the upper and lower portions of the function switches indicate to the operator that his command was successfully transmitted and accepted by the DTCS equipment. In response to certain predetermined conditions, the START modules may be logically isolated or SEALED from the system by commands originating in the computer. The Select Extend Allocate Lockout (SEAL) command causes the lower position of the XEQ switch to illuminate, informing the operator of the SEAL condition.

Figure 4 illustrates the relationship of the R-START module to the remainder of the data entry equipment and also shows the signal and data flow between the START modules and the computer. The input control signals to the START modules originate in the computer. Their function is described as follows:

- a. SEAL - This signal inhibits the addressed START module from transmitting an execute signal to CUE.
- b. REMOVE SEAL - The REMOVE SEAL signal is used in two ways: to either reset the CUE or to gate a confirming response to the START module.
- c. UNIT SELECT - This signal is generated when the scanner count is the same as the address for a particular START module.
- d. Q - This signal is transmitted when the data entry equipment is in the automatic mode of operation and enables preselected patterns of digital information in the R-START to be transmitted to the CUE for subsequent transfer to the computer.

FOR TRAINING PURPOSES ONLY

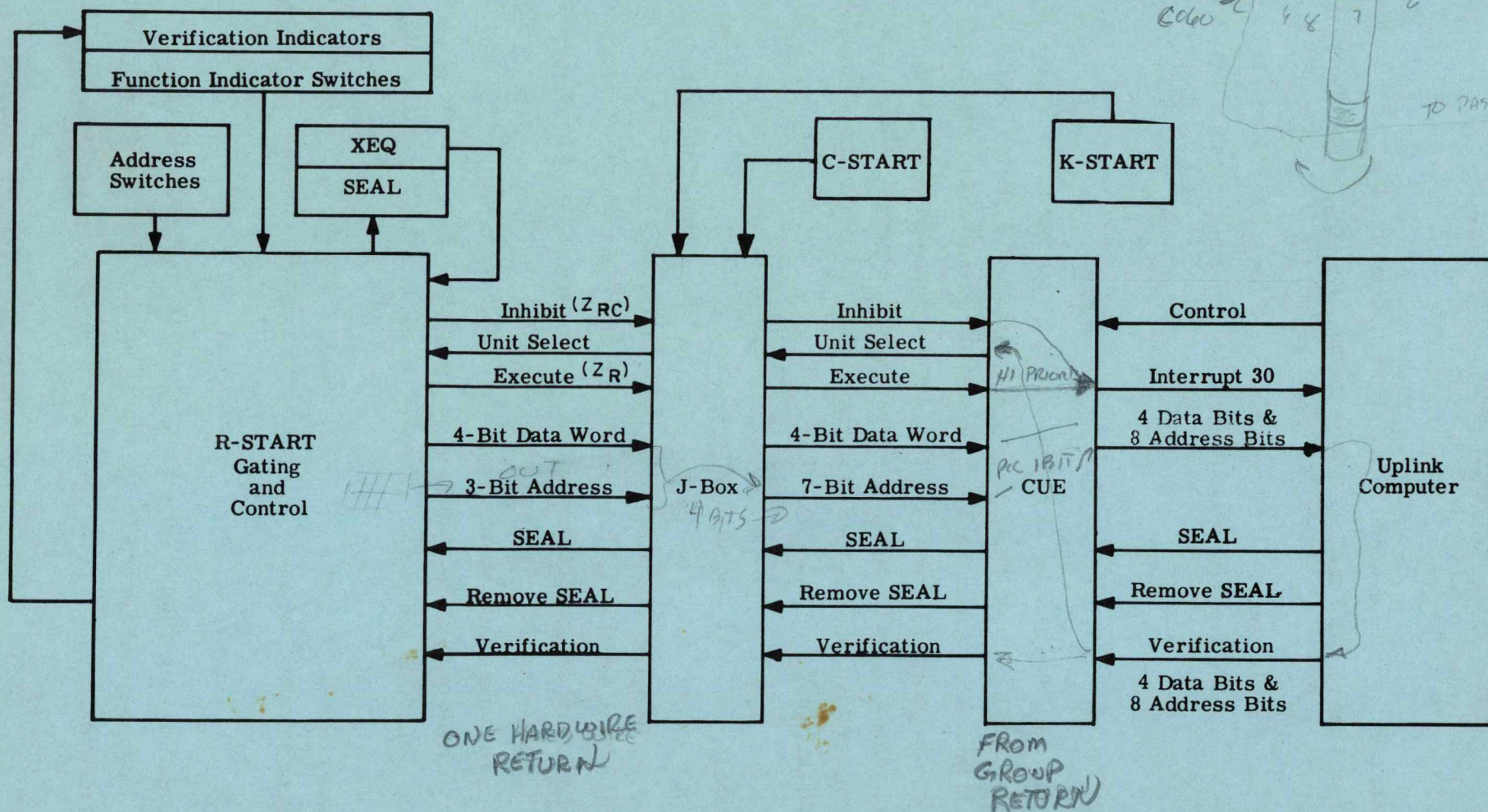


Figure 4. R-START/Data Entry Functional Diagram

4 BIT WORD 8 BIT ADDRESS

410-0(105)

- e. Four response code bits, F1 through F4, light the corresponding upper halves of the indicators when the relays are latched.

The four data bits from the computer via CUE are fanned into the four-bit receiver section of the addressed START module and are gated to the storage unit by the remove SEAL signal. From there the data bits are gated to the function light latches. In other words, the status of the upper half of the function switches always indicates the condition of the relays which they control. A lighted indicator corresponds to a relay latch condition.

C-START MODULE

The C-START panel contains ten 12-position selector switches, ten displays which indicate the selector switch settings, an XEQ switch indicator, Power On indicator, and four function indicator lights. Each individual switch position provides a four-bit binary-coded-decimal (BCD) (8-4-2-1) code for transmission to the computer. Thus, the command output of a C-START module is a 40-bit message. This output is used for setting discrete voltages in the D/A converters of the DTCS and to modify preprogrammed subroutines.

The sequence of C-START operation is as follows:

- a. The operator sets up a predetermined code by means of the selector switches and verifies his selection by observation of the display on the C-START panel.
- b. When he is satisfied that the correct sequence of characters has been selected, he enters them into the computer by depressing the XEQ switch, which causes illumination of the upper half of the XEQ switch.
- c. The response of the system to a C-START execute will be to extinguish the upper half of the XEQ switch and to illuminate the four function lamps into codes that indicate various responses to the C-START command.

Figure 5 is a block diagram of a C-START module. As seen in the diagram, it is composed of function select switches, BCD converters, project indicators, and logic gating circuits.

Figure 6 illustrates the relationships of the C-START module to the remainder of the data entry equipment and also shows the signal and data flow between the START modules and the computer.

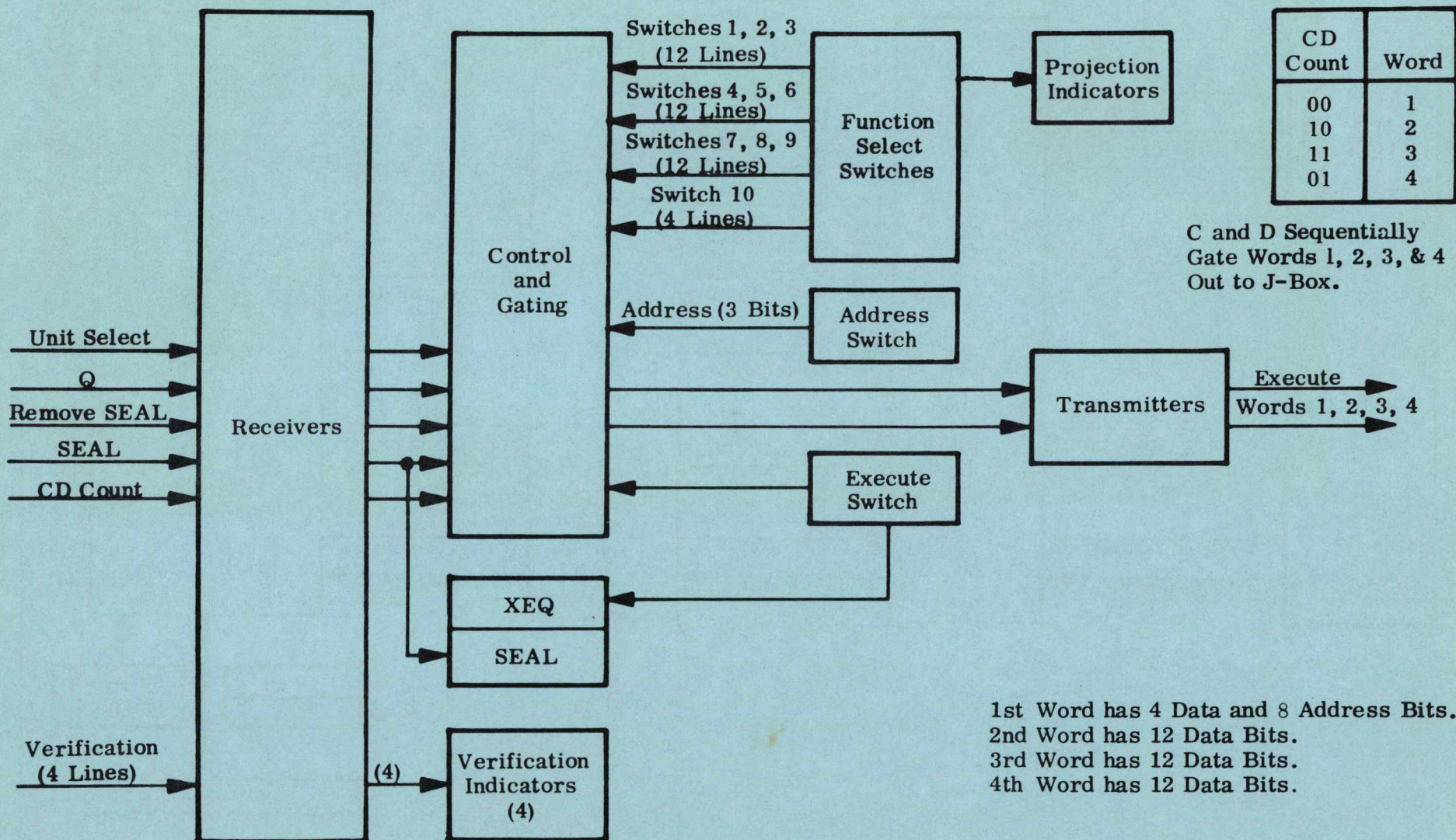


Figure 5. C-START Block Diagram

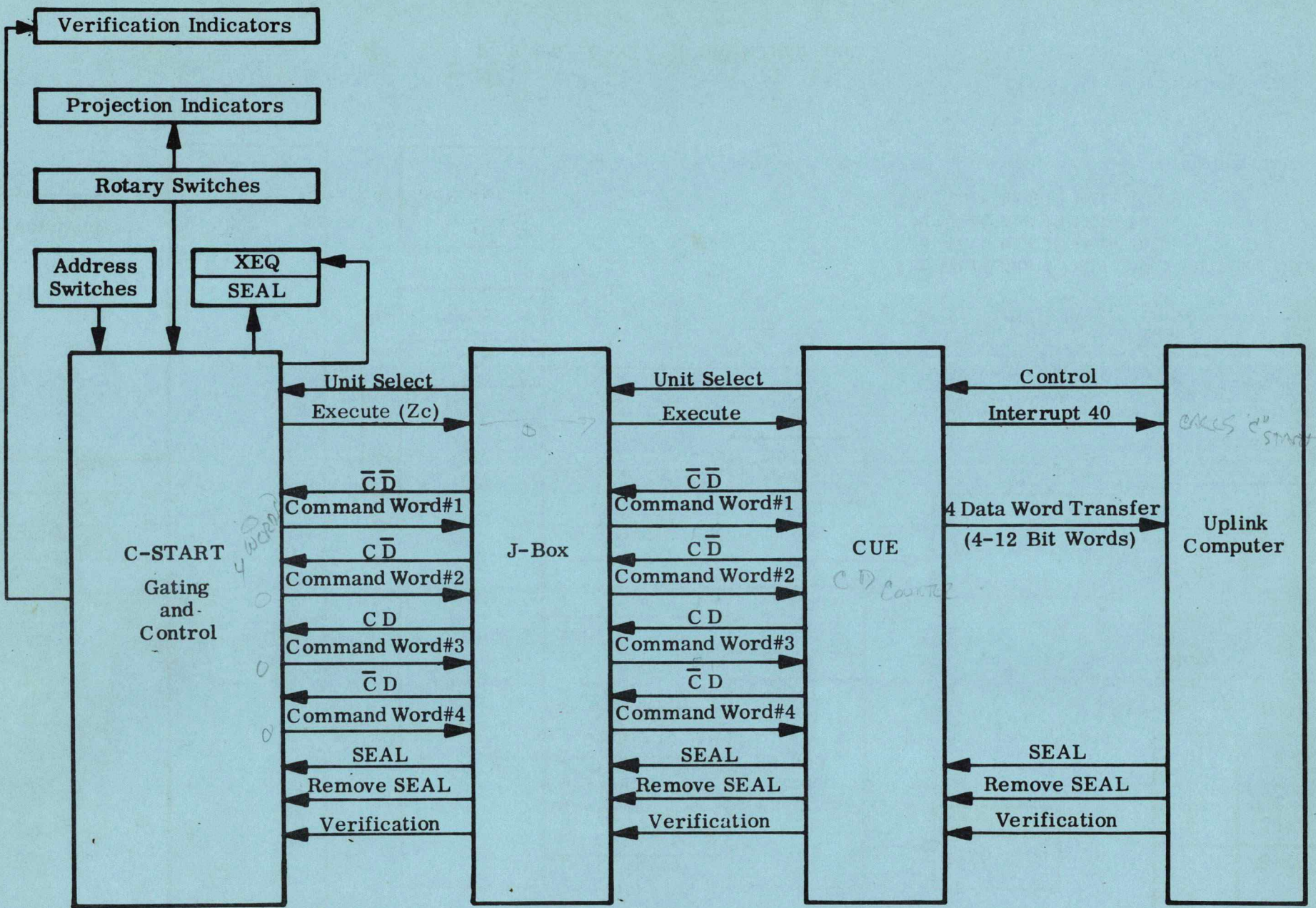


Figure 6. C-START/Data Entry Functional Diagram

The logic involved in the operation of the C-START module is analogous to the R-START. An execute signal is generated by depression of the XEQ switch and is gated out of the module by the unit select enable signal from the CUE scanner. Whereas the R-START module produces only one 12-bit word, the C-START module generates four 12-bit words for each execute. Word transmission is controlled by the "C" and "D" word selection signals. The execute signal is used to gate the 40 data bits and the three least significant digits of the address out of the C-START module and into the appropriate J-Box.

Normally, module selection is on a first-come-first-served basis. However, priority logic inhibits the selection of C-START modules until all waiting R-START units have been serviced.

Unlike R-START modules, verification of a C-START is a function of the computer program and indicates to the operator, through the four function lights on the C-START panel, various combinations of lights with each defining a separate or distinct condition. The C-START verification codes are illustrated in Figure 7.

The SEAL, remove SEAL, unit select, and Q signals perform the same function as in the R-START.

K-START MODULE

The K-START module is a digital input device that supplies information to the computer from manually operated keyboard switches or automatically from a paper tape reader when selected by the operator. The K-START panel contains a pushbutton keyboard, six tape control switches, a tape input display, three status displays, and a bank of 24 AGC event displays. Figure 8 is a functional block diagram of a K-START module.

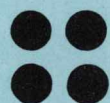
The data transmitted consists of four 12-bit words. The first word contains the 8-bit address of the K-START and a bit indicating whether the input is from key or tape. The second word contains the 5-bit data word, the stop and skip bits for tape input, and an odd parity bit, which indicates odd parity for the five data bits. The third and fourth words are all zeros. Table 1 shows the configurations of the 5-bit data words when using keyboard control. Table 2 shows the four-bit words as they are transmitted when using the tape input, and Table 3 shows the four 12-bit words that are transmitted when using the keyboard input.

K-START
Key Board
6 TAPE
CONTROL
SWITCH
TAPE INPUT
DISPLAY
3 STATUS
DISPLAY
24 AGC
EVENT
DISPLAY

BINARY
COUNT

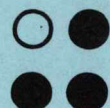
12

0



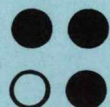
NOT USED

1



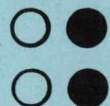
CSR INDICATES ERROR

7

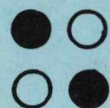


DAC IN USE

5

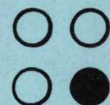
INVALID CONTROL
(SUB-PROGRAM) CODE

6

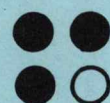


VOLTAGE EXCEEDS LIMITS

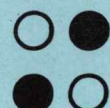
9

FREQUENCY OR PULSE/SEC
EXCEEDS LIMITSBINARY
COUNT

8

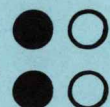
ILLEGAL SEQUENCE
REQUESTED

9



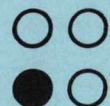
ILLEGAL DATA ENTRY

10

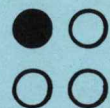


ILLEGAL DAC ASSIGNMENT

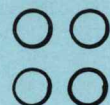
11

TOO MANY
ANALOGS REQUESTED

14

CAN NOT COMPLETE
SEQUENCE

15



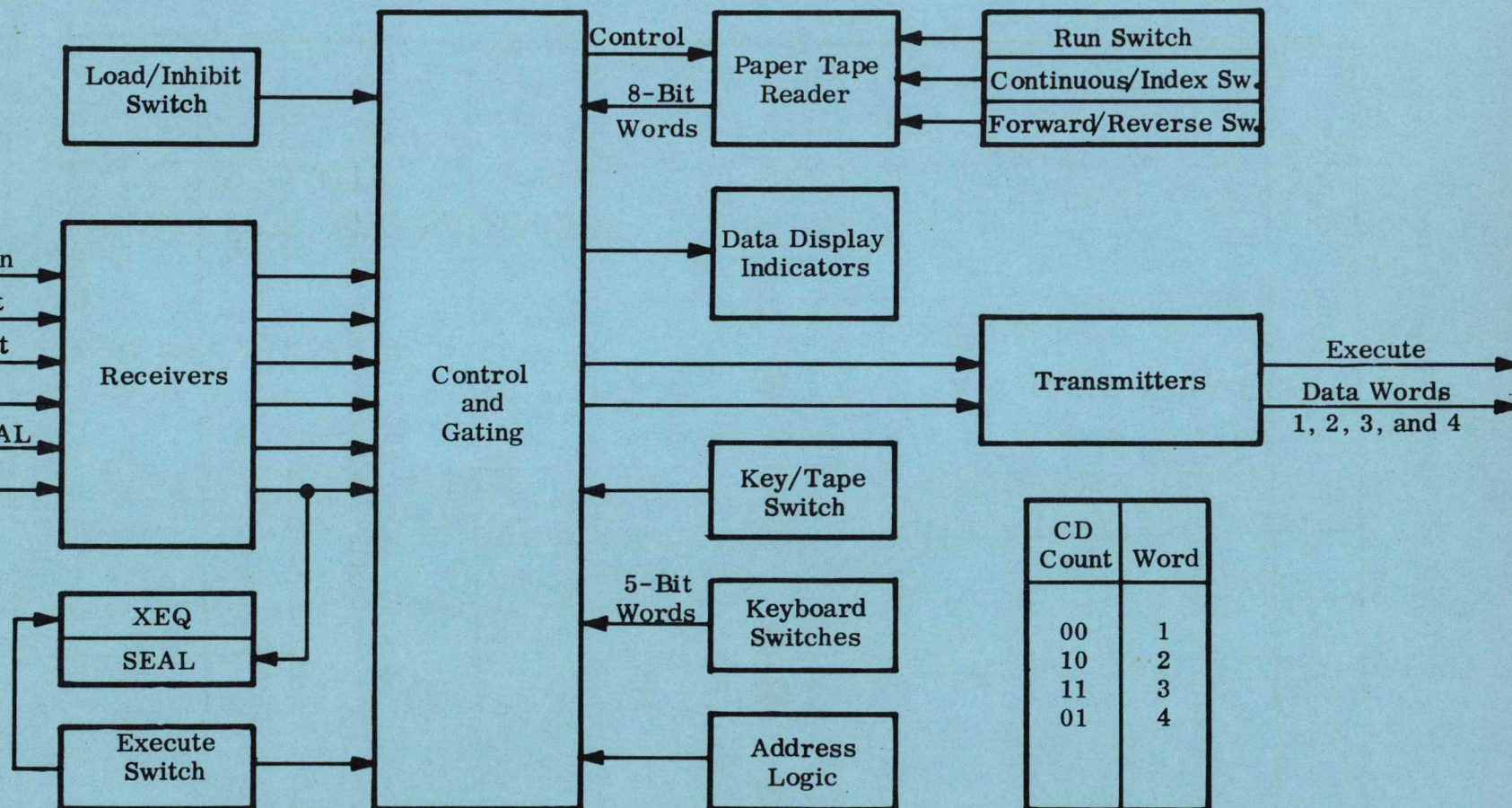
ALL GOOD-GO

○ LIT

● OUT

Figure 7. C-START Verification Indicator Codes

FOR TRAINING PURPOSES ONLY



C and D Sequentially Gate
Words 1, 2, 3, & 4 To J-Box

Figure 8. K-START Block Diagram

8 bits ADDRESS —

Table 1
K-START Keyboard Word Format

Key Codes	Data Bits	Parity Bit (Odd)
0	1 0 0 0 0	0
1	0 0 0 0 1	0
2	0 0 0 1 0	0
3	0 0 0 1 1	1
4	0 0 1 0 0	0
5	0 0 1 0 1	1
6	0 0 1 1 0	1
7	0 0 1 1 1	0
8	0 1 0 0 0	0
9	0 1 0 0 1	1
Verb	1 0 0 0 1	1
Noun	1 1 1 1 1	0
+	1 1 0 1 0	0
-	1 1 0 1 1	1
Enter	1 1 1 0 0	0
Clear	1 1 1 1 0	1
Release	1 1 0 0 1	0
Error Reset	1 0 0 1 0	1

Table 2
K-START Tape Input Word Format

Data to CUE	Bit											
	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Word 1	Y	Y	Y	Y	Y	Y	Y	Y	0	0	0	1
Word 2	0	0	0	0	W	X	X	X	X	X	X	X
Word 3	0	0	0	0	0	0	0	0	0	0	0	0
Word 4	0	0	0	0	0	0	0	0	0	0	0	0
Y = Address X = Data W = Parity												

Table 3
Word Format, Key

Data to CUE	Bit												
		2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Word 1		Y	Y	Y	Y	Y	Y	Y	Y	0	0	0	0
Word 2		0	0	0	0	W	0	0	X	X	X	X	X
Word 3		0	0	0	0	0	0	0	0	0	0	0	0
Word 4		0	0	0	0	0	0	0	0	0	0	0	0

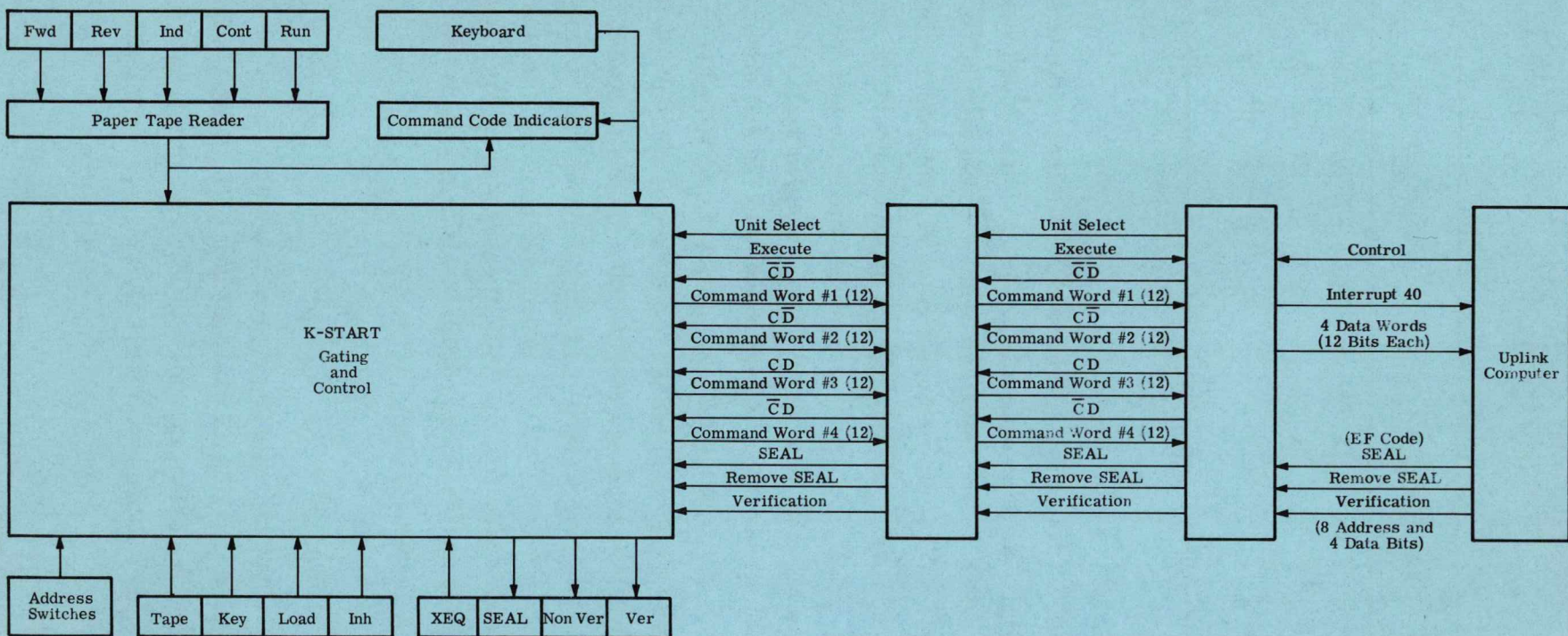
TAPE INPUT

When the K-START module is in the Tape Input Mode, the tape reader delivers one 8-bit word to the K-START (Figure 9) and halts until it is commanded to read the next character word. Figure 10 shows the tape format and channel allocations. Channels 4 through 8 contain the five data bits used as the command. Channel 1 contains the parity punch for odd parity recognition of the five data bits. Channel 2 is the skip punch that, when punched, causes the tape reader to ignore that frame and to move to the next frame. Channel 3 contains the stop punch that, when punched, causes the tape motion to halt at that particular frame. A hole in the stop channel also causes the LOAD/INH switch to be set to the INH position, the TAPE/KEY switch to be set to the KEY position, and the indicator lamps (Figure 11) to display the 8-bit data word that is read from the tape. A hole in both the stop and skip channels causes the tape to travel to the next frame.

When the 8-bit word is delivered to the K-START from the paper tape reader, the word is then reassembled in the manner shown in Table 2. The resultant four 12-bit data words are then transmitted to the CUE.

KEY INPUT

In the key mode, the 5-bit character words are generated as a result of the depression of the keyboard switches on the K-START control panel. The 5-bit word configurations with the resultant parity bit are shown in Table 1. The transfer of the data words and the exchange of control signals between the K-START module and the CUE is the same as the tape input operation.



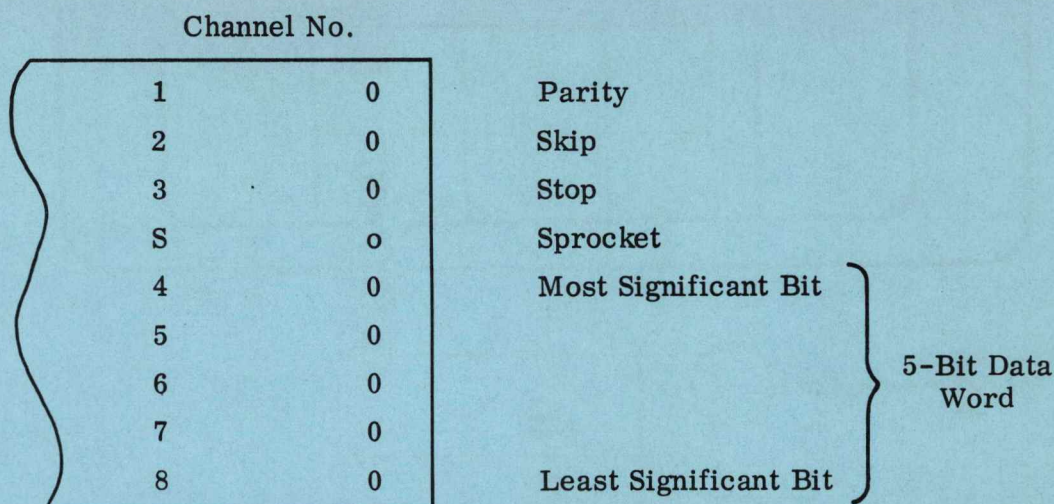


Figure 10. Tape Format

Depressing a given key automatically transmits the four 12-bit data words to the CUE. The K-START module encodes the key code output to eight bits, as in the case in the tape input mode. However, the skip and stop bits are zeros in the key mode of operation.

J-BOX (Figure 12)

The sixteen J-Boxes provide the interface between the START modules and CUE. Each J-Box supplies power to the two groups of eight modules associated with it. Each J-Box generates the 16 unit select signals (Figure 13), which are transmitted to the START modules associated with the J-Box by ANDing eight unit select and two group select signals. Also, each J-Box has a BCD switch that generates the three bits of the J-Box address, which is inserted in the address portion of the 12-bit data transfer from the START to the CUE. The J-Box also decodes a group "0" or "1" bit to be inserted. The CUE will generate the patch "0" or "1" bit.

COMMUNICATIONS UNIT EXECUTOR

The CUE serves as a central addressing and control unit between the START modules and the 160G computer. This unit controls the two-way communications path over which pass the START module data and/or test commands and the computer responses.

- a. Scanning - A scanning counter, located within the unit, sequentially interrogates all 256 START addresses. If the presence of a START execute signal is sensed, the scanning ceases and an interrupt is sent to the computer. CUE causes the contents of the START module, as well as its address, to be gated to the computer.

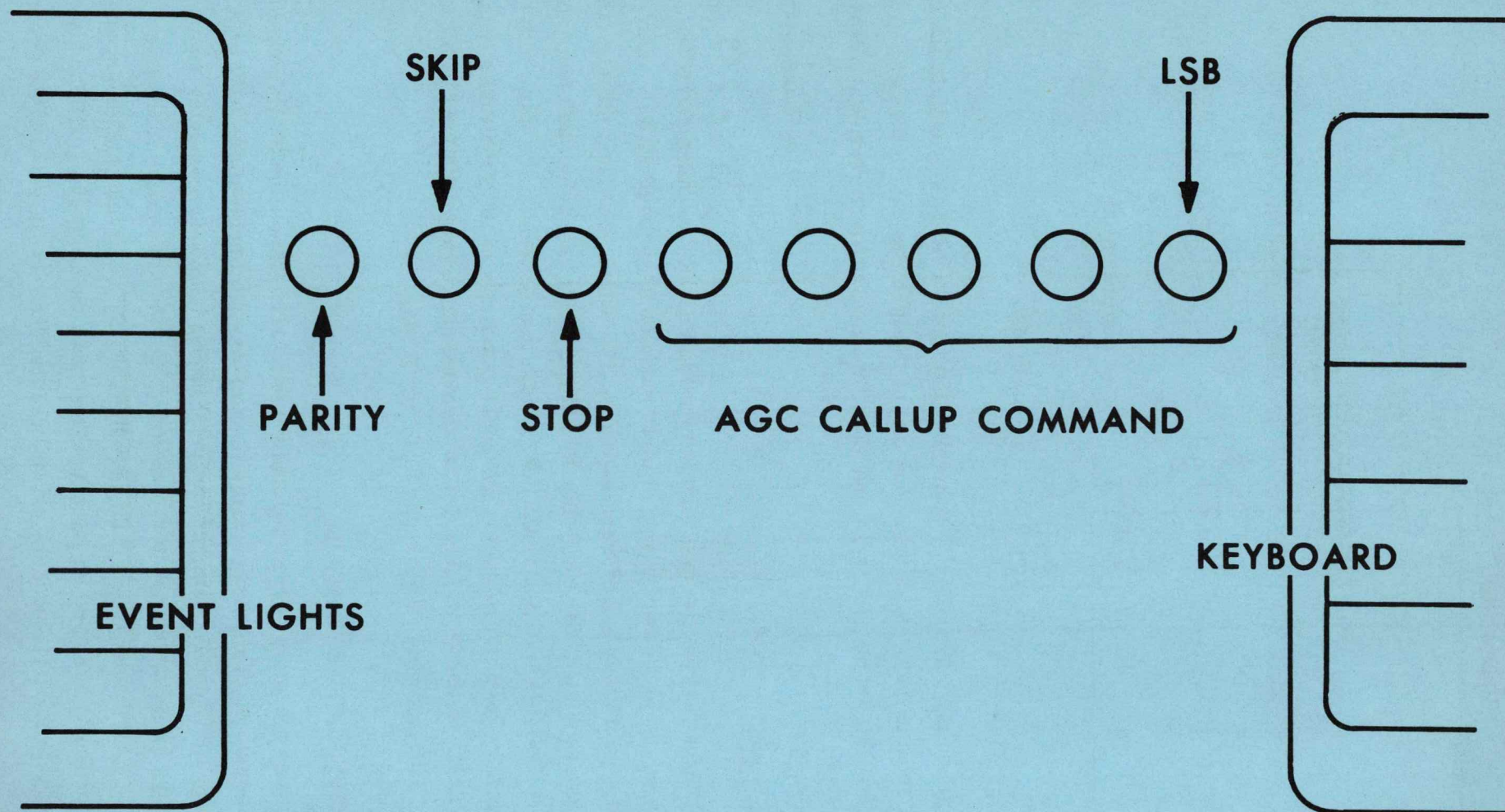


Figure 11. K-START Character Bit

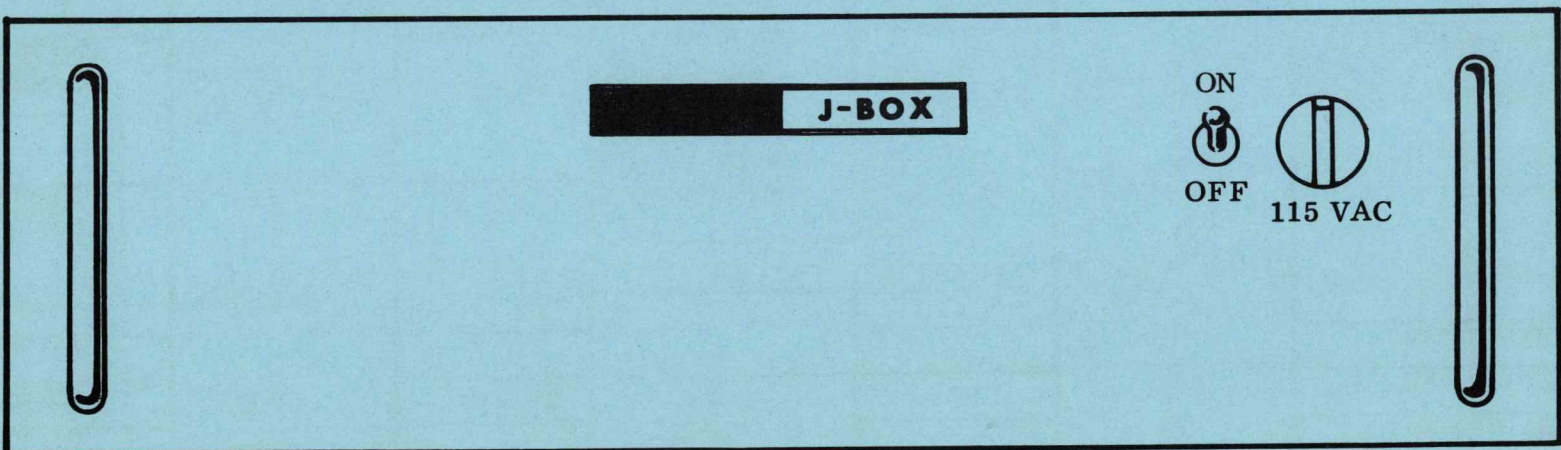


Figure 12. J-Box

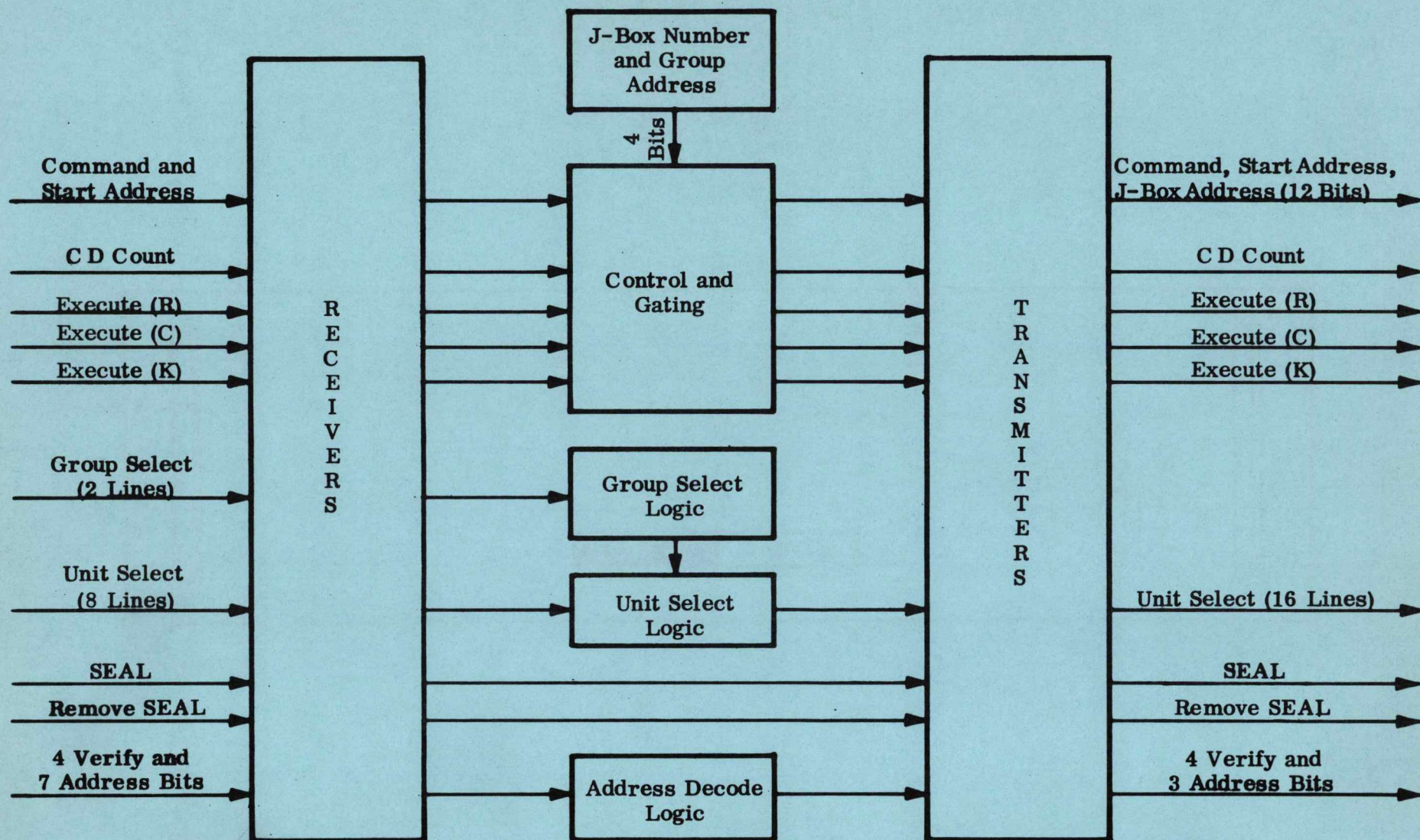


Figure 13. J-Box Block Diagram

- b. Command Encoding - CUE encodes commands for introduction to the computer, such as START module data and address bits and status response codes. It determines which interrupt signal is to be generated and transmits it to the computer. It decodes the computer instructions (external function codes) into proper timing and operating sequences.
- c. When in the maintenance mode of operation the CUE allows the computer to communicate with the Command Monitor Unit (CMU).

Figure 14 is a block diagram of the CUE. This unit is composed of timing, scanner, unit and group translators, a control section, decode logic, and transmit/receive electronics. A self-contained power supply provides the dc voltage necessary to the logic operation.

The CUE scanner, which is used to generate sequential START module addressing, consists of a three-stage, gray code counter followed by an eight-stage binary counter. The three-stage, gray code counter receives its inputs from a 100 kc oscillator. The gray code counter counts down the clock pulses and in turn drives the binary counter. The output of the binary counter is utilized to develop the addresses of the various START modules in the data entry system. The most significant bit (2^7) of the scanner address is used to define patch 1 or patch 0 of the CUE. Bits 2^3 through 2^6 are used to decode the group selection and bits 2^0 through 2^2 decode the unit selection. As the scanner counts, it sequentially interrogates each START module looking for an execute signal.

COMPUTER GENERATED FUNCTION CODES

General

The CUE interprets and reacts to the following External Function (EF) codes from the computer. All EF codes are in octal notation, and the CUE is selected by a code of the form 37 XY. The 37 determines that the computer selected CUE. XY defines specific functions to be performed.

External Function Codes

The following are external function codes:

- a. 3700 Status Request - On request of this instruction, CUE transmits a status response code to the computer. Table 4 contains the status response codes for the data entry equipment.

Handwritten note:
Hello
Type
Message

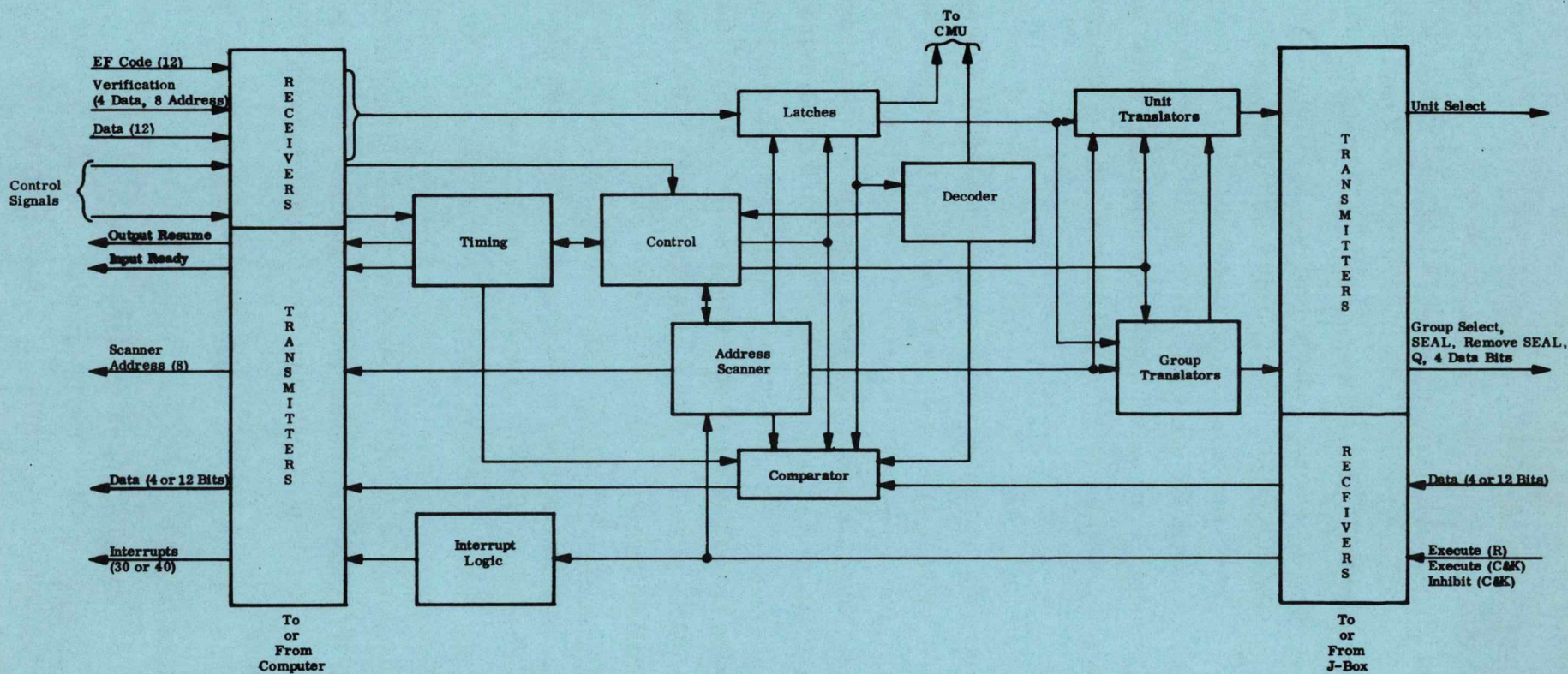


Figure 14. CUE Functional Block Diagram

- b. 3701 SEAL - A response is not returned to the computer if the remote device takes too much time in processing the data, the computer issues a SEAL command. This command isolates or inhibits the use of that START module.
- c. 3702 Select Standby Mode - The standby mode is the idling mode of operation; however, CUE will not generate interrupts.
- d. 3703 Select Manual Mode - The manual mode is the normal working mode of operation for the CUE. The CUE is capable of transmitting data and/or commands in this mode of operation.
- e. 3704 Remove SEAL - The remove SEAL instruction is used in two ways: to remove the SEAL condition in a particular START module or to gate a confirming response to the START module.
- f. 3705 Compare - The logic of the CUE contains compare circuitry by which the address is checked for errors occurring during transmission between the CUE and the computer. It is used only if the original test data is of a critical nature.
- g. 3706 Input Request - The computer selects the CUE for input by using the input instruction. This enables one or four 12-bit data words to be transmitted to the computer.
- h. 3707 Select Maintenance Mode - This mode of operation allows the computer to transmit two 12-bit words of data via the CUE to the CMU for display and operator evaluation.
- i. 3710 Select Automatic Mode - The selection of the automatic mode of operation permits the computer to select a particular START unit and to select which particular data word it wishes to interrogate.
- j. 3711 Read Scanner Address - The computer under program control can at any time issue a read scanner address instruction. Upon receipt of this command, the CUE automatically transmits the 8-bit address currently generated by the address scanner logic to the computer.

The 160G computer communicates with the CUE via external function codes and control signals (see Figure 15). The CUE will receive, decode, and act upon these external function codes. If the computer requests a status reply, the CUE will transfer a status word to the computer, which indicates a specific condition as described in the preceding listing.

Table 4
Status Response Codes

Bit Position	Description
2^0	Terminal Fault
2^1	Manual Mode
2^2	Address Compares
2^3	CMU Filled
2^4	Data Compares
2^5	Standby Mode
2^6	Spare
2^7	Spare
2^8	Spare
2^9	Interrupt 30
2^{10}	Interrupt 40
2^{11}	CUE Generated Interrupt

COMMAND MONITOR UNIT

The CMU displays malfunction information pertaining to the DTCS, the computer peripheral equipment, and the data entry equipment. The data, which represents the nature of the malfunction, is generated by the ACE-S/C uplink computer and transferred to the CMU via the CUE for display (see Figure 16). The status information depicted by the CMU provides a means for operating personnel in the computer room to correlate digital test command malfunctions with the data entry equipment in the ACE-S/C control room, and also to take the appropriate action pertaining to computer peripheral equipment malfunctions. Only the equipment malfunctions that can be detected and handled by the computer will be displayed on the CMU. In the event of a data entry malfunction (CUE and START), the CUE scanner address will be displayed indicating the point during the scanning process the malfunction occurred.

The CMU is located in the computer complex console (Unit 154) in the computer room.

The command monitor unit has the capability to display the status of 16 computer peripheral equipments (see Figure 17). Each peripheral has an assigned indicator and will be lighted by data from the computer room upon the detection of a malfunction in that area. The indicator will only depict that a malfunction has occurred and not

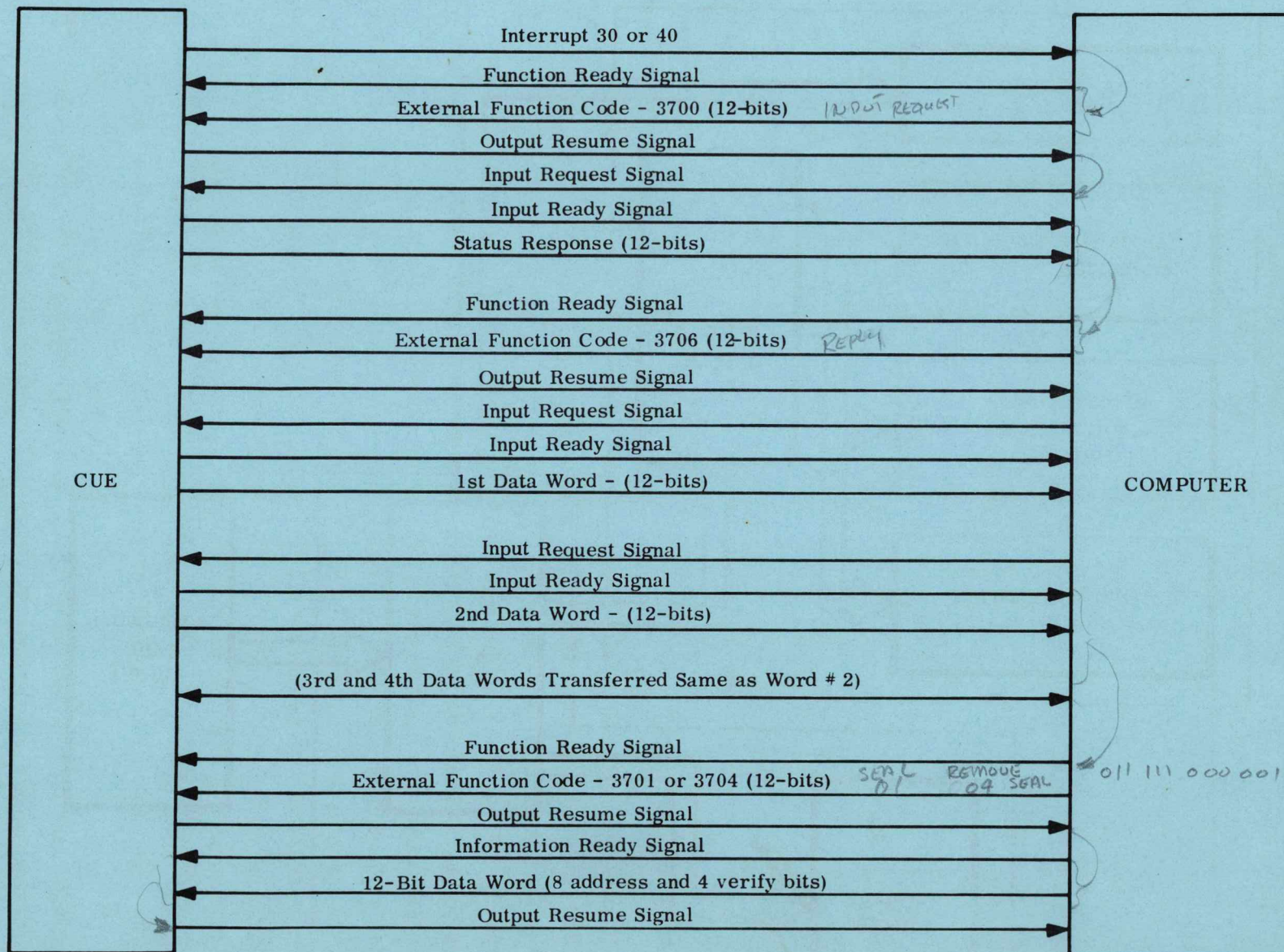


Figure 15. CUE/Computer Interface Signals

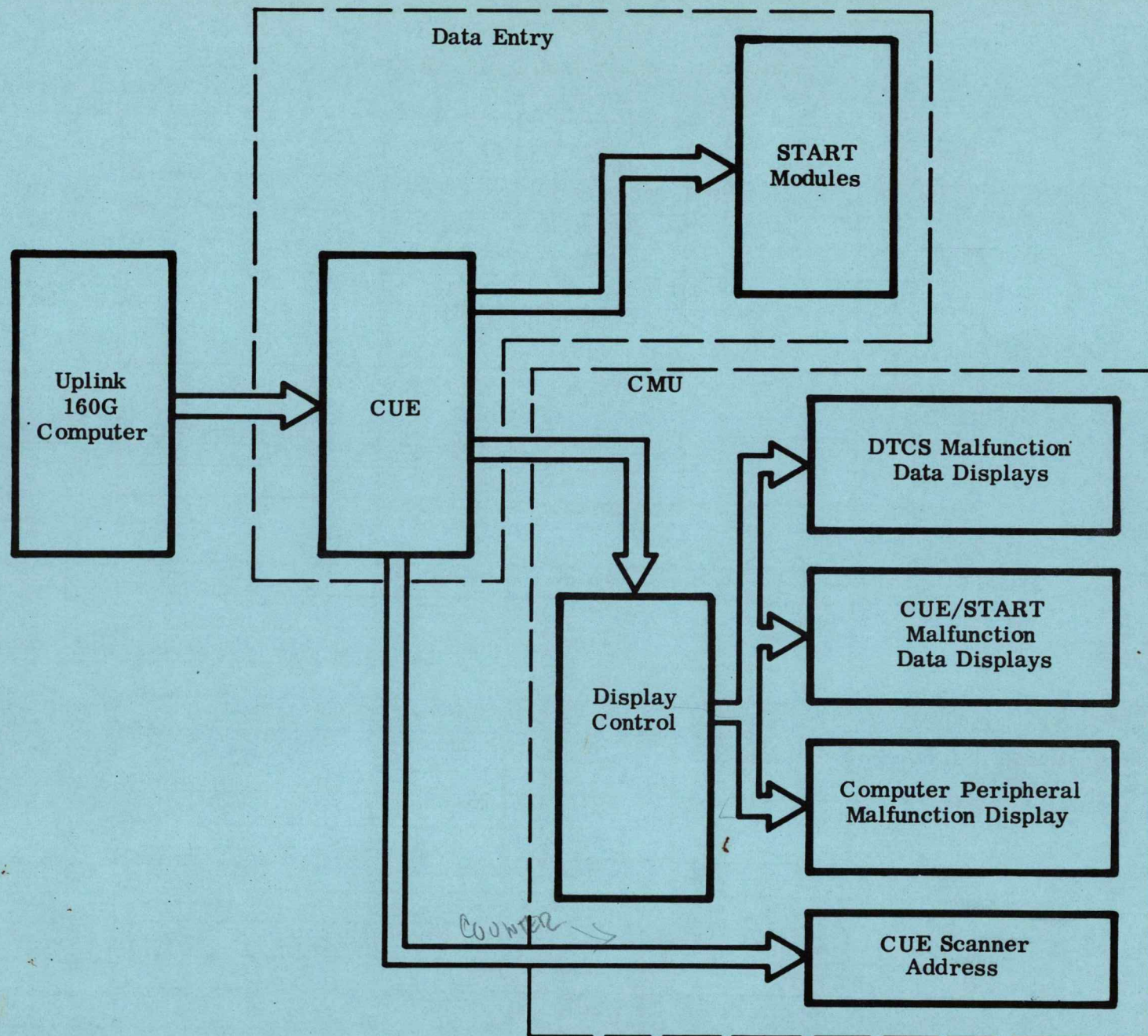


Figure 16. CMU/CUE Interface

DTCS Malfunction					CUE/START Malfunction					
	Group	Base-plate	Module	Sub-Group Code		START Address		Code		
Reset ☐	1	8	3	A 4		3	7	7	6 2	Reset ☐
☐	5	0	0	2		2	2	4	9 5	☐
☐	2	1	4	C 1		1	3	6	4 1	☐
☐	4	6	2	D 5		1	4	5	2 3	☐
☐	3	4	1	B 3		0	2	3	2 0	☐

CUE Scanner Address

1 4 6

STATUS- (WHEN BAD)

Peripheral			Equipment			Status	

Figure 17. CMU Indicators

the nature of the malfunction. The types of peripheral equipment that can be monitored and displayed are listed as follows:

Uplink Peripherals

- a. 1 typewriter.
- b. 3 data transmitter and verification converters.
- c. 2 magnetic tape transports.
- d. 1 card reader.

Downlink Peripherals

- a. 1 typewriter.
- b. 1 data transmitter and verification converter.
- c. 2 magnetic tape transports.
- d. 1 line printer.
- e. 2 X-Y plotters.
- f. 1 card punch.
- g. 1 card reader.

DATA PROCESSING

OBJECTIVES

To familiarize the student with:

- a. The overall operation of the 160G computing system.
- b. Computer system programing.
- c. Operation of the 169G-3 memory unit.
- d. Operation of the 171G-3 input/output unit and associated peripheral devices.

PART I - COMPUTER FUNCTIONAL DESCRIPTION

The Acceptance Checkout Equipment - Spacecraft (ACE-S/C) ground station contains a data processing system that consists of two general-purpose Control Data Corporation 160G digital computers and associated peripheral and data transmission equipment. The two 160G computers are identical and are identified by their assigned function within the overall ACE-S/C system. Basically, the ACE-S/C system is divided into two functional loops: (1) the uplink or command loop and (2) the downlink or display loop. The uplink computer processes commands received from the data entry equipment, i.e., R-START, C-START, and K-START modules, which interface with the computer through the CUE. After the commands are processed, the uplink computer transmits them to the receiving equipment in the test bay via a data transmission system. The spacecraft's reactions to the commands are monitored by sensors and the resulting signals are commutated on a PCM telemetry carrier and returned to the decommutation equipment located in the computer room. The downlink data is then presented to the second 160G computer for tolerance checks, conversion to engineering units, and distribution to the downlink data transmission system for routing to the display equipment. This computer can also cause the data to be recorded for post-test analysis.

To fully understand the functional operation of the 160G computing system, it is necessary to first understand basic computer concepts. A general-purpose digital computer consists of four major sections: (1) memory, (2) arithmetic, (3) control, and (4) input/output. Any functional part of a general-purpose digital computer can be included in one of these major sections. Figure 1 is a block diagram of a general-purpose digital

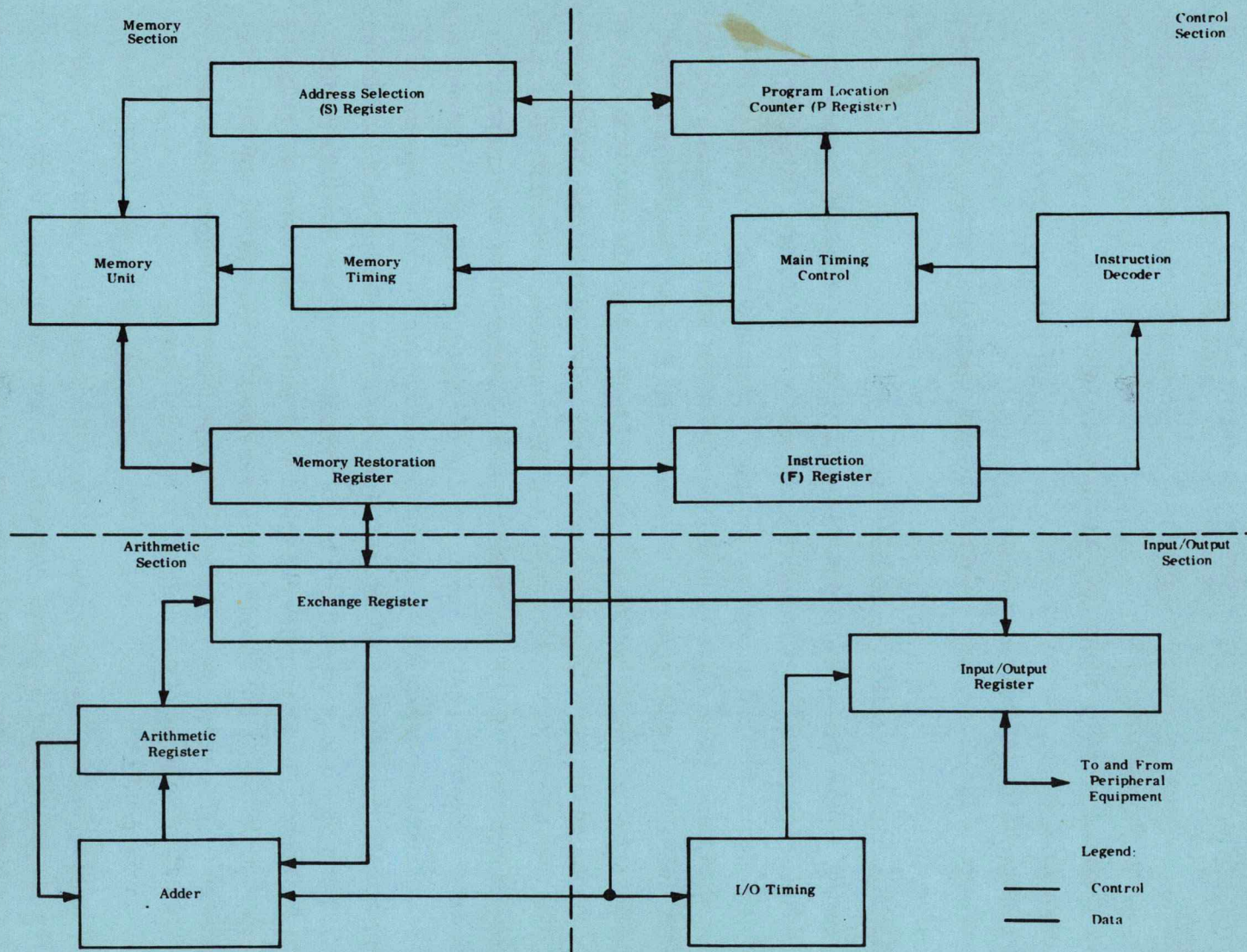


Figure 1. Digital Computer Block Diagram

computer showing these major sections. The following paragraphs present a functional description of each major section and its relationship to the other sections.

MEMORY

The memory section of a computer is composed of an array of permanent or semi-permanent storage devices as its primary element. In modern high-speed computers, this device has generally been the ferrite core. The ferrite core has the capability of retaining information in one of two magnetic states, making it capable of storing one bit (binary digit) of information (see Figure 2A). The magnetic properties of the core allow it to maintain a magnetic state without the application of power (see Figure 2C) and enable this state to be changed upon the application of a magnetic field of the proper intensity and direction. The core can be switched from one magnetic state to the other very rapidly, approximately 1 to 2 microseconds. Since the cores are small in size (30 mils or so in outside diameter), a memory containing 100,000 cores or more can be built into a package not much larger than a textbook.

128
A common configuration for a core memory has 4096 cores mounted in a 64 by 64 matrix on each of a number of planes; the number of planes will be equal to the number of bits (length) of the word to be stored. Each plane stores one bit of the data word in any one of 4096 locations, as determined by the address associated with that data word. A memory composed of 13 planes of 4096 cores each then could store 4096 13-bit data words. The complete memory for a computer would be made up of one or more of these banks of memory.

Each core in a plane is threaded by four wires: a horizontal drive line, a vertical drive line, a sense line, and an inhibit line. For each plane of the memory described there are 64 horizontal drive lines, each threading 64 cores; 64 vertical drive lines, each threading 64 cores; a single sense line, threading all 4096 cores; and an inhibit line threading all 4096 cores. To complete the wiring of the memory, the corresponding horizontal drive lines of each plane are connected together in series electrically, and the corresponding vertical drive lines of each plane are connected together in series.

A given memory address, specifying a single core in each of the 13 planes, is selected by translation of the output of the address S register to select one horizontal drive line and one vertical drive line. Only one core in each plane is threaded by the selected horizontal and vertical drive lines and is, therefore, the core selected by that memory

FERRITE CORES

MATRIX

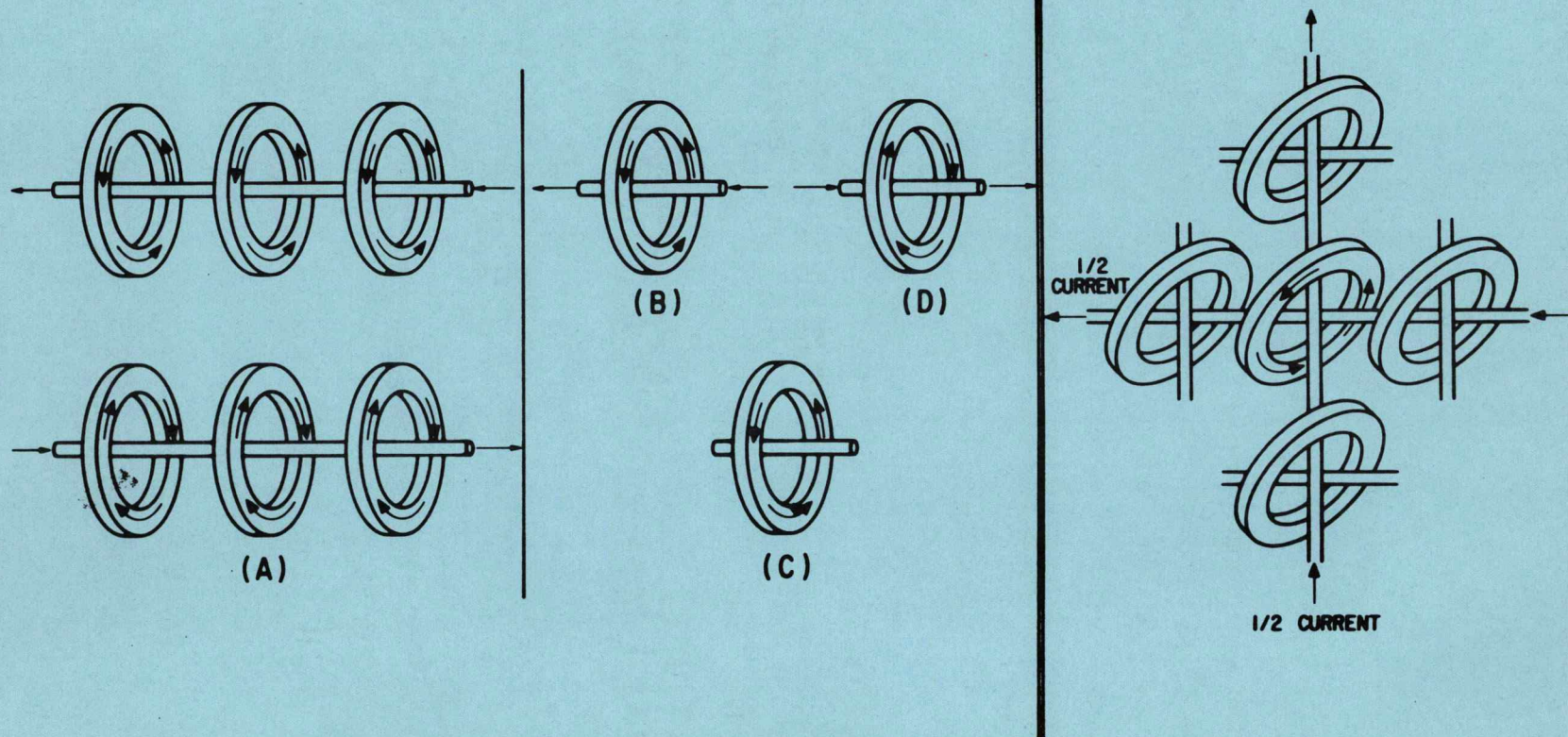


Figure 2. Memory Section of a Computer

address. When information is to be stored in memory or read out of memory, a half current (a current having only approximately one-half the amplitude required to switch a core) is applied to the selected drive lines.

All the cores that are threaded by only one of these wires will be disturbed by a current that is not sufficiently large to switch the cores, while the single core on each plane that is threaded by both of these wires will be disturbed by a current that is of sufficient amplitude to switch the magnetic state of the core.

During the readout of information from the memory, the magnetic state of each of the selected cores is switched to the zero state. If the selected core was initially in the one state, a voltage will be induced in the sense line when the core is switched to the zero state. If the selected core was initially in the zero state, it remains in that state and virtually no voltage is induced in the sense line. Therefore, by examining the sense line at an appropriate time after the drive lines are energized, it can be determined whether the selected core contains a zero or a one. The voltage pulses on the sense lines are amplified, shaped into standard logic pulses, and gated into the Z (data) register from whence they are transmitted to the other sections of the computer as needed. This method of reading the information from a core memory is known as destructive readout.

In a memory with destructive readout, the circuitry associated with the memory automatically takes the word from the Z register after readout and restores it in the selected cores in memory during the write portion of the memory reference. During the write operation, the direction of current through the selected horizontal and vertical drive lines is in a direction opposite to that during the read operation. Thus the selected core on each plane will be set to a one state unless an inhibit current equal to a half current and in a direction opposite to that of the write current is applied to the inhibit winding of the plane. The inhibit current is controlled by the contents of the Z register, and, therefore, a zero is written into memory for those data bits of Z that are a zero.

For a computer operation which is to write new information into memory, the memory again goes through both a read and a write cycle. During the read cycle, however, the transfer of information from the sense amplifiers to the Z register is inhibited. Instead, the Z register is set by a transfer of data from the computer or an input/output chassis to the Z register. During the write portion of the memory reference, then, the new information is written into the selected memory location.

The selection of the horizontal and vertical drive lines is controlled by the address associated with the word. Six address bits are necessary to select one of the 64 horizontal drive lines, and six address bits are necessary to select one of the 64 vertical drive lines. The time from the initiation of a memory reference cycle until the information is in the Z register is known as the access time of the memory; the time required for the complete memory reference is known as the memory cycle time.

A typical computer memory is constructed of a number of these 4096-word banks of memory. The address is then composed of more than 12 bits. The upper bits are decoded to determine the bank of memory to be referenced, while the lower 12 bits specify the location in the selected memory bank.

In summary, the memory section requires only three things from the control section of the computer. These are:

- a. A transfer into the memory address register of the number indicating which word in memory is to be selected.
- b. An indication of the direction of the transfer of the word, either into or out of the memory.
- c. A signal to start the memory cycle, which in turn will energize the appropriate selection and drive signals to perform the transfer.

ARITHMETIC

The arithmetic section contains the circuitry necessary to perform mathematical and logical calculations on information. For this purpose, it has several registers to hold numbers and wired-in logic to allow the mathematical and logical manipulations of the numbers. The operation of any digital circuitry follows a pre-arranged set of logical steps. The logical operations of the arithmetic section of the computer are simple combinations of these logical steps, while the arithmetic operations are more complicated combinations of these basic steps. The shifting of an operand left or right in a register is one of the simpler applications of these basic steps.

The arithmetic section obtains the timing signals necessary to perform its various functions from the control section and, also, obtains the information on which it performs its various functions from the memory section. The results of its functional operations are generally transferred back to the memory section for storage in core memory.

The heart of most computers is the adder. Arithmetic, as previously mentioned, is one of the more difficult operations to perform with the basic logical steps available in a digital computer. The adder, which performs an addition (or, by an inversion of one operand, a subtraction) in a near minimum time and with a near minimum of active components, is an optimum combination of these basic logical functions. It so happens that if certain control signals are not activated as two operands flow through the adder, various logical combinations of the two operands result; various logical instructions come essentially free, if the adder is in the arithmetic section. Multiply, divide, and shift instructions also make use of this adder portion of the arithmetic section.

CONTROL

The words stored in the memory of a computer can be classified as either instruction words or data words. The program of a computer consists of one or more series of instruction words; the control section of the computer reads these instruction words one by one and executes the instruction specified. If by mistake, a data word is read by the control section instead of an instruction word, the computer has no way of knowing that it is not an instruction word; the control interprets the bits of the word as an instruction and executes whatever instruction is specified. (This is why the operation code 00 is interpreted as a stop instruction in many computers; if the program jumps by mistake to a section of memory which has neither data nor instructions in it, the program will stop.)

The control section has the primary function of providing timing signals for the various internal information transfers. It provides these timing signals by translating or decoding the numerical computer instruction which it receives from the memory core storage. The instruction (word or words) is held in an instruction register, frequently referred to as the F register, while the translation and execution is taking place. The control section has its own register to determine the location in memory where each instruction is to be found. This register is called the program address register, abbreviated as P register. Since the computer instructions are found in sequential memory locations, the P register is incremented each time an instruction is executed. In some computers the incrementing is done by using the adder, and, in others, special circuitry is provided for this purpose.

The control section requires a signal from the computer operator to start; once this is done, it relies on instruction information from the core memory to determine which of

the control and timing signals it should generate. These signals regulate the the flow of information at all times within the computer and also control the initiation of information transfer external to the computer.

INPUT/OUTPUT

The Input/Output (I/O) section provides the temporary storage facility for information being transferred into or out of the computer. Incoming information is retained by the I/O section until that information has been stored in core memory. Outgoing information is retained by the I/O section until the receiving device is able to accept it. The timing for information transfers is provided from within the I/O section, but it is initiated by the control section. A primary function of the I/O section is one of compensating for the vastly different information flow rates found in the computer and external peripheral devices. It enables a computer, operating at transfer rates of several hundred thousand words per second, to communicate with peripheral devices operating as slowly as several words per second.

COMPUTER PROGRAMING

At the present state of the art, the term "Electronic Brain" for a general-purpose digital computer is a complete misnomer. Research is progressing on how to build a computer that will "think," but computers currently available are incapable of doing anything which could be called, by any stretch of the imagination, thinking. They merely work out what has already been thought of beforehand by the designer and supplied to them in the form of instructions.

The current digital computer, therefore, is capable of doing only those operations which the programmer tells it to do. It is safe to say that any problem whose solution can be described, step by step, before the solution is begun, can be programmed for a digital computer. It immediately follows that the best person to program a mathematical problem is a mathematician, the best person to program an engineering problem is an engineer, and the best person to program a medical problem is a doctor (unless the engineer or doctor can reduce his problem to one of solving equations, in which case a mathematician is better qualified to program the problem).

Three significant advantages of a digital computer are:

- a. The computer is orders of magnitude faster than a human being in solving a problem.

- b. A computer does not make errors.

These advantages make it sound as if a digital computer is nothing but a super adding machine; it is this, but much more. A third advantage makes the digital computer considerably more than a super adding machine:

- c. The ability to make (preprogramed) decisions.

The programing of a digital computer is composed of the following three basic steps:

- (1) Analyzing the problem.
- (2) Reducing the problem to separate simplified portions for ease of handling.
- (3) Writing instructions that will solve each portion and combining these.

An obvious means of translating these steps into the instructions which the computer uses is for the programmer to program the problem directly in the machine's language. Machine-language coding, also known as absolute coding, can give a program of maximum efficiency - the resulting program will run in a minimum length of time. Unfortunately, a program written in machine language takes an unreasonable amount of computer time to check out; fewer and fewer programs are being written in machine language.

One interesting attempt to simplify the job of programing is through the use of compilers. A compiler is a computer program that allows the programmer to write his program in a series of steps which are easily understood by him, but which have little or no relation to the machine-language instructions. The compiler then translates the program so written into machine instructions. Many of these compiler languages are so independent of machine language that they can be used on a variety of computers. (A separate computer program has to be written for each computer.) An example of a compiler is FORTRAN (a contraction of FORMula TRANslation), which uses a formula-type language to program the problem.

There are, for example, FORTRAN compilers written for the Control Data 1604 and the IBM 7090. The same problem, written in FORTRAN, can be computed to be run on either computer by using the appropriate compiler. A major advantage of compilers is this independence of the specific computer; a major disadvantage is that the programs written in compiler language will not run at the maximum speed because of the divorcement of the compiler language from the computer language. A compiler-generated program, assuming a well-written compiler and a computer well suited to the compiler language, will run 10 to 15 percent slower than if the program had been

written in machine language. FORTRAN, ALGOL, and COBOL are examples of well-known compilers.

Between the two extremes of machine-language coding and compilers come assemblers. An assembler is like a compiler in that it puts a machine program between the writing of the program and the generation of the machine-language instructions. Strictly speaking, an assembler contains only pseudo-instructions which correspond, one to one, with the machine-language instructions. Actually, most assemblers have some pseudo-instructions which go beyond the instruction list of the computer and, hence, are simple compilers. Writing in assembly language is essentially writing in machine language with the corresponding advantage that programs so written will run at the maximum possible speed. The advantage of using an assembler is that it relieves the programmer of a considerable amount of drudgery, helps in debugging the program, and saves machine time. Assemblers are obviously not independent of the machine they are to be run on. Examples are OSAS, written for the CDC 160A, and GASS, written for the CDC 160G.

160G COMPUTING SYSTEM

The 160G computer module and its associated maintenance and operator console make up the basic 160G computer, but it can be expanded into a much larger system with the addition of 169G memory and 171G input/output modules. The following paragraphs present a general description of the 160G compute, 169G memory, and 171G input/output modules. Figure 3 depicts a block diagram of the 160G compute module.

160G COMPUTE MODULE

Memory Section

The memory section of the 160G computer module provides a means of storing program instructions, data words, and various constants utilized in the spacecraft checkout. The heart of the 160G computer module (see Figure 3) memory section is the 8192, 14-bit magnetic core stack. The 160G computer utilizes a basic 13-bit instruction with the 14th bit being a parity bit. The memory restoration register (Z), a 14-bit register, temporarily holds data being transferred to and from the magnetic core memory. The Z register has associated with it, parity circuitry which generates a parity bit for each stored word during a write operation and then checks this parity bit when a read operation is performed.

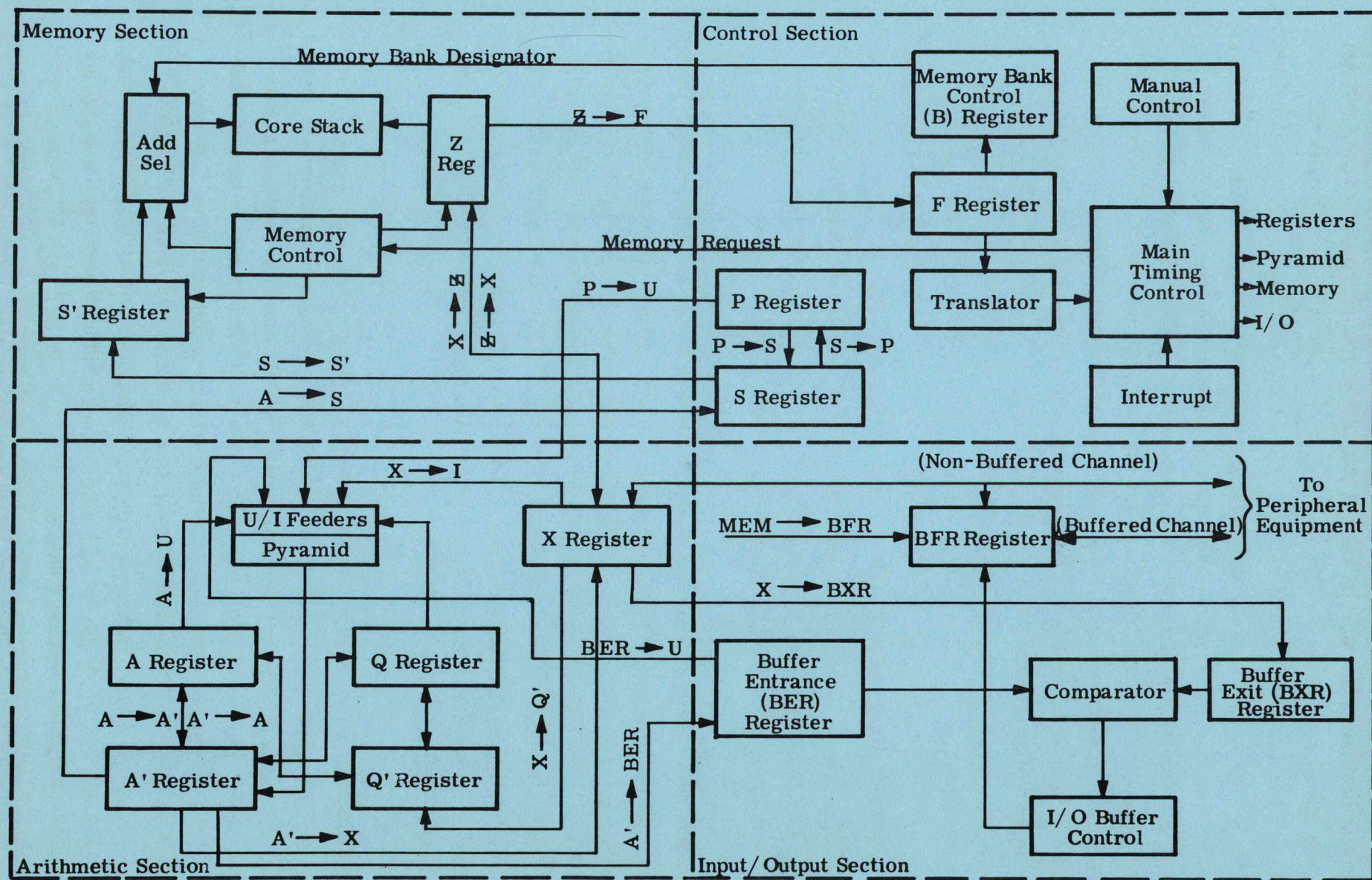


Figure 3. 160G Compute Module Block Diagram

A memory plane in the 160G compute module consists of four quadrants, each quadrant contains 4096 (64 by 64) ferrite cores. Each memory stack is composed of seven planes forming an 8192 word bank of memory. In the 160G computer system, the banks are numbered 0, 2, 4, 6, 10, etc., with bank 0 being located in the compute module. The first 4096 words of the bank are obtained by selection of a bit from each of two quadrants of the seven plane stack; the second 4096 words utilize the other two quadrants of the planes. The S' register, a 13-bit register, contains the address of the memory location currently being referenced in a specific bank. The least significant 12 bits specify the address in the pair of quadrants, while the most significant bit specifies the pair of quadrants.

Registers

Internal Memory Address Register (S')

When a memory reference is made to internal memory, the current memory address in the S register is placed in the S' register. The S' register provides outputs that condition the address selection logic to reference the correct address.

Memory Restoration Register (Z)

The 14-bit Z register operates with core memory. All data entering or leaving core memory is stored temporarily in the Z register. Data to be written into core memory is placed in the Z register and then written into the correct location. Data read from core memory is placed in the Z register. After this data has been transferred to another register, the data is gated from Z back into the same memory location. Thus, Z permits a memory reference to be nondestructive. The 14th bit of the Z register is a parity bit.

Memory Operation

Each 160G compute module contains a memory section of 8192 storage locations, which is the internal memory. Memory sections located in 169G memory modules are external memories. The physical arrangement of the core storage and method of read-out, write-in, and address selection of the internal memory is practically identical with an external memory. The major differences lie in the access channels. The 160G memory section cannot be accessed by other 160G compute or 171G input/output modules; whereas, the 169G may be accessed by any combination of 160G compute or 171G input/output modules that total nine or less. Therefore, the 160G memory section does not need a scanning device.

A maximum of 14 bits can be stored in a given memory location. Thirteen bits comprise the data or instruction word, and the 14th bit is a parity bit. The parity bit allows a malfunction of the memory to be detected.

The storage function, within a memory section, is controlled by a delay line for timing the Z and S' registers to effect directly a memory reference to a specific location. Control of readout and write-in within the memory section is accomplished by pulsing the delay line once each time a memory reference is made.

The control section of the 160G places a memory request, a select code, and a read, write, or partial-write command on the lines to all accessible memory modules including the internal memory. When the internal memory senses its select code and memory request, the following events occur:

- a. Transfer of the address from S to S'.
- b. Set the busy flip-flop to lock out other memory references for the remainder of the cycle.
- c. Set the gate, read drive, and discharge drive flip-flops to enable read currents to flow through the selected X and Y drive lines of the memory stack.
- d. Start a pulse down the delay line to time each function in the memory reference cycle.
- e. Clear the Z register in preparation for a transfer of 1's.

A mode command places the memory section in the write, read, or partial-write mode of operation.

In the write mode, the control section places data for a specific address into the X register. When the write gate is enabled, the data is transferred into the Z register of the memory section and stored in the core memory during the write portion of the memory reference.

In the read mode, the data from the memory address selected by the S' register appears on the outputs of the sense amplifiers during the read portion of the memory reference. When the read transfer occurs, the data is transferred into the Z register of the memory section. The output of the memory section Z register is then gated to the computer. The data word read from memory during the read portion of the memory reference is restored in memory during the write portion of the memory reference cycle. In the partial-write mode, both the read and write functions are employed in

one memory cycle. The upper seven bits of the 13-bit word are processed in the read mode, and the lower six bits plus parity are processed in the write mode. The result is that the lower six bits of the word are changed in the partial-write mode while the upper seven bits are not affected.

Address Selection

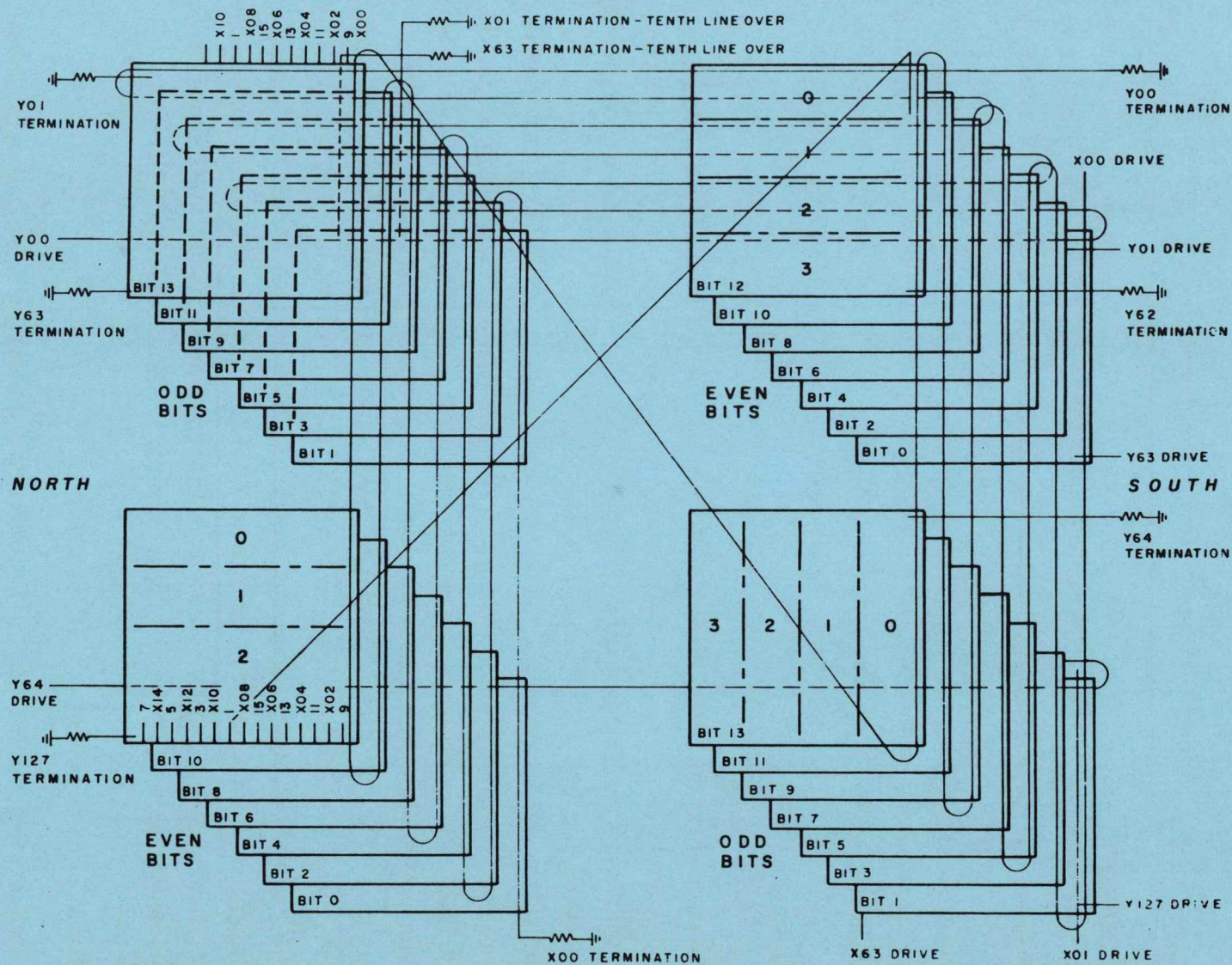
In order to accommodate a 14-bit word in a seven plane memory stack, two bits must be stored on each plane. This is done by dividing a plane into two banks, each consisting of one odd quadrant and one even quadrant. Bits 00, 02, through 12 are stored in the even quadrants of seven successive planes in a bank, and bits 01, 03 through 13 are stored in the odd quadrant of the same seven planes in the same bank. Storage across the seven planes of the other bank uses the remaining odd and even quadrant of each plane. Since a quadrant contains a 64 by 64 matrix of cores and two quadrants are used to store a word, each bank effectively accommodates 14-bit words in 4096 storage locations.

Since a memory stack contains two banks, $4096 \times 2 = 8192$, storage locations are available in a memory stack. For addressing purposes, the X drive lines run through the even quadrants of bank 00, continue through all the planes on the south side through the transposition plane and down through all the planes on the north side, and return to termination through the odd quadrant of bank 00, Figure 4. Therefore, 64 X drive lines thread all cores in all four quadrants of all seven planes in a memory stack. In the Y axis, 64 Y drive lines run through both quadrants of all seven planes and terminate. A second set of 64 Y drive lines thread through the odd and even quadrants of the seven planes of the 01 bank. Therefore, both banks are energized along the X axis and only one bank is energized along the Y axis so the Y drive lines serve to select the 00 or 01 bank. Addressing consequently energizes one of 64 lines in the X axis and one of 128 lines in the Y axis. The energized X line crosses the energized Y line once in the odd quadrant and once in the even quadrant of the seven planes of a selected bank. The drive lines are energized by turning on line-drive transformers, Figure 5.

Memory Arrangement

The maximum number of bits that can be stored in a given memory location is 14 bits, 13 bits contain information and 1 bit is used for parity checking. Information access time for the memory and its associated control and sensing circuits is approximately 0.5 microsecond, and the time for a complete memory reference cycle is 1.35 microseconds. Figure 4 shows the quadrants, planes, and X and Y drive lines arranged to

15



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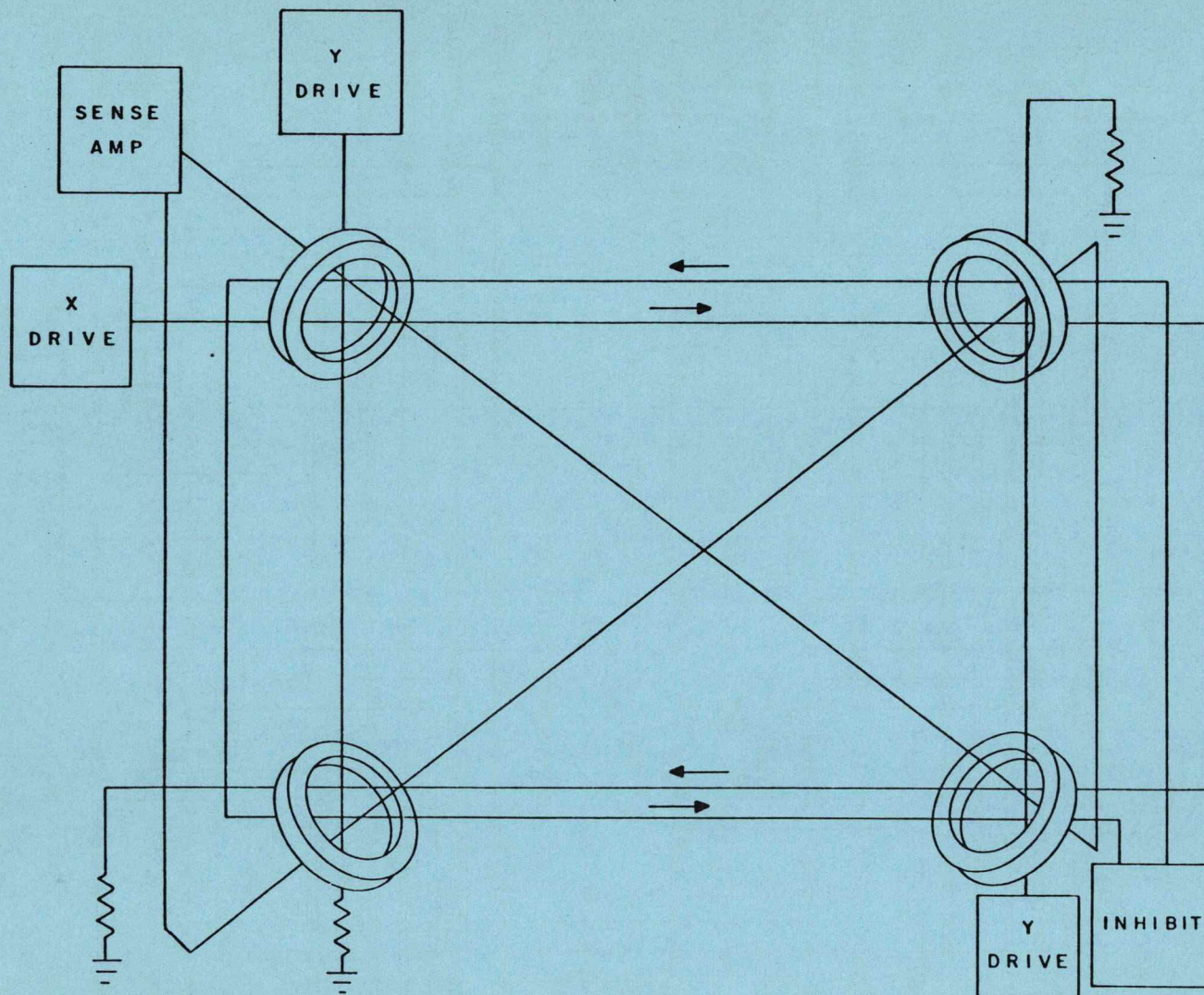


Figure 5. Core Matrix, Functional Brief

form a memory stack. Figure 5 shows a functional brief of memory cores with the drive lines, inhibit line, and sense line threaded through a set of four cores. All cores are wired in the same manner. The following paragraphs describe the circuits that are directly connected to these drive lines and effect storage, location, and removal of bits stored in the memory stack.

Core Storage

The memory operates in the coincident current mode, using currents of one direction to read, and the opposite direction to write.

Each core is threaded by four wires (see Figure 4), X and Y half-current drive lines, an inhibit line, and a sense line. When information is written into a core, the core is switched to the 1 state by two coincident currents on the X and T drive lines. Similarly, when information is read from a core, it is switched to the 0 state by two coincident currents of the opposite polarity. The inhibit line carries a current parallel to one of the drive lines, but in a direction opposite to the half-write current. If the inhibit current is flowing during a write phase, it cancels the effect of one of the half currents and, thereby, prevents any core through which the inhibit current passes from being switched from a 0 to 1 state. If the drive currents were not inhibited during the write phase, all cores would be switched to a 1 state. If the write coincident X and Y currents act to switch a core from 0 to 1, and if that core is already a 1, it remains a 1. Conversely, if the read coincident X and Y drive currents act to switch a core from 1 to 0, and if that core is already a 0, it remains a 0. The sense line is connected to a differential sense amplifier. When a core switches state in either direction, the sense amplifier produces an output; however, this output is sampled only during the memory read phase.

The memory core material has an approximately rectangular hysteresis loop. The high residual magnetization of the core enables it to function as a memory element. The magnetic properties of a core are represented in Figure 6 by its hysteresis loop in which magnetic flux density B is plotted as a function of field intensity H . If sufficient current flow to cause a field intensity of $+H_m$ is applied to the core, the flux density increases to saturation $+B_s$. When current is removed, the flux drops to residual value $+B_r$ and remains there. Sufficient current flow in the opposite direction to cause a field intensity of $-H_m$ reverses the flux density to $-B_s$. When current is removed, the flux density drops to the residual value $-B_r$.

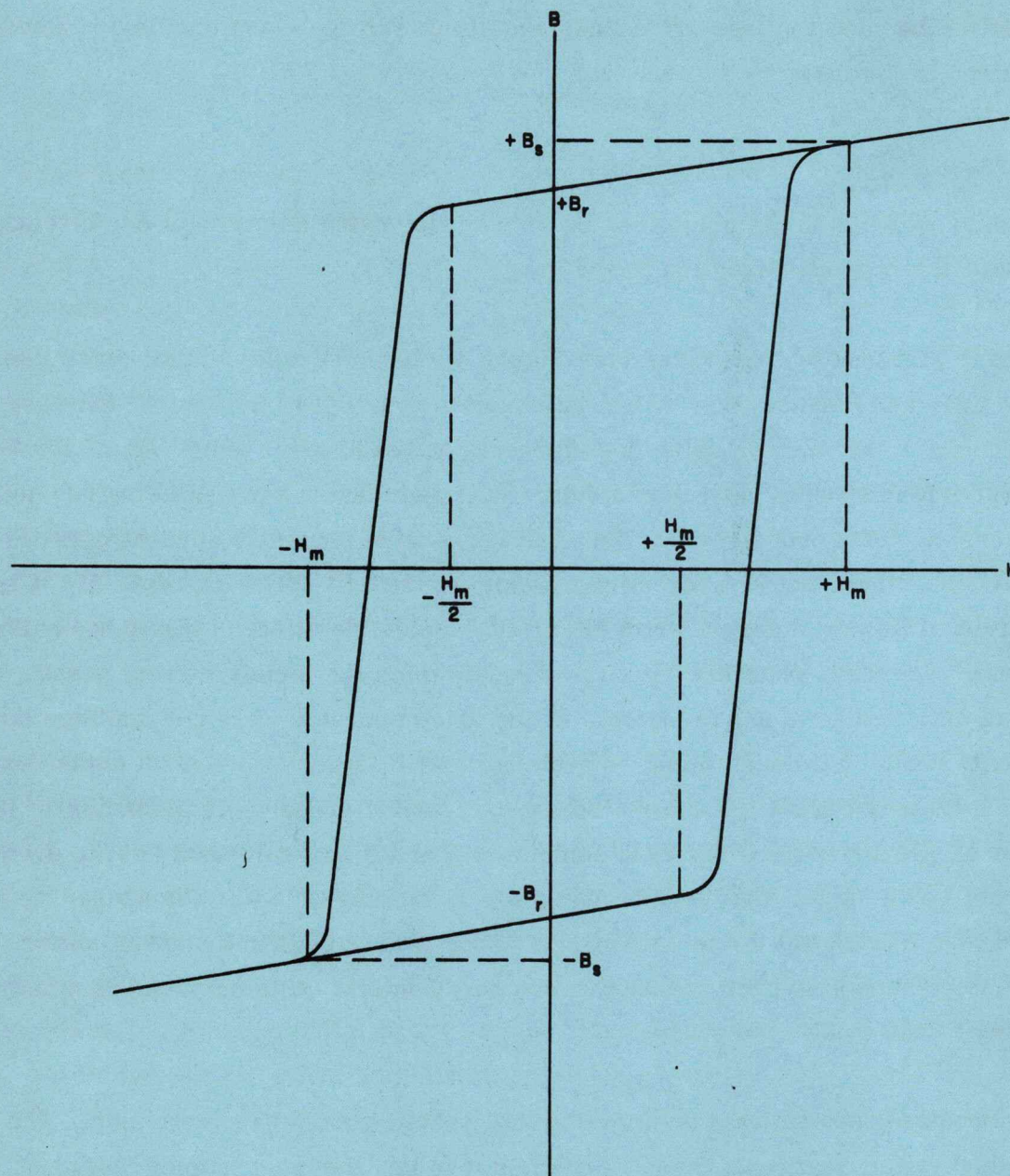


Figure 6. Typical Hysteresis Loop

The basic memory cycle consists of half-current pulses capable of producing a field intensity of $H_m/2$. A half-current pulse is insufficient to switch a core; however, the coincidence of two half currents produces a net field intensity that is sufficient to switch the core.

Inhibit Circuits

Whenever an address is selected and the read drive is on, coincident currents are present on each core of that address. These currents attempt to switch all cores. Cores magnetized in the direction resulting from a previous 1 storage are switched, and cores magnetized in the direction resulting from a previous 0 are not switched. Inhibit currents are not used during read, those cores that switch are allowed to switch. If a core is switched, a small voltage is induced in the sense line threaded through that core and a pulse appears along the sense line (see Figure 4). The read-out process switches every core containing a 1 to a 0; this is a destructive readout and the memory must be restored. The output of the sense line is amplified and gated into the memory register as 1's. During the write drive the information is written back into memory; at the end of the memory reference cycle, the contents of the particular selected address is restored.

Whenever an address is selected and the write drive is on, two coincident currents are present on each storage bit of that address. Unless the effect of one of these drive currents is cancelled out, every core in that address is switched to a 1. Because of the effect of the inhibit lines during the write phase of the memory cycle, only those bits which were 1's are switched back to 1's. In order to prevent core-switching in cores that are not to store a 1, a current flowing in opposition to one of the drive currents is generated to cancel the effect of this drive current, thereby inhibiting a core from being switched. This function is performed by the inhibit circuits consisting of inhibit generators and inhibit lines.

Sense Circuits

Each sense circuit consists of the sense line threaded through all cores of a quadrant of a plane, and the sense amplifier which is tied to the two ends of the sense line. Whenever a core is switched, a pulse of about 35 millivolts appears on the sense line. This pulse may be either positive-going or negative-going depending on the direction the core was switched. The sense amplifier consists of a differential voltage amplifier and a discriminator. Regardless of the pulse polarity at the sense amplifier input, the output is always a positive-going pulse.

Parity Circuit

Bit 13 in each memory location is used to provide a comparison bit for parity checking. Bit 13 is generated by the parity logic and placed into the Z register before a word is written into memory.

The number of 1's contained in the Z register determines whether a parity bit should be generated by the parity logic as a 1 or 0. The parity check on the 160G memory operates on an odd-parity basis; that is, the word which is read out of or written into memory must contain an odd number of 1's. If the number of 1's in the operand is odd, a parity bit 0 is generated. If the number of 1's in the operand is even, a parity bit 1 is generated.

Memory Timing

The select code, mode command, address, data word, and memory request to a specific memory bank are originated by the computer to start a memory reference cycle. After a memory bank is selected, address transferred, and mode command received, a timing pulse starts down the delay line in the memory section. At this time, temporary control of the read, write, or partial-write reference is held by the memory section. The computer main timing control is inhibited until released by the memory section. At the end of the memory cycle, the memory section returns to its quiescent state until receipt of another memory request. The computer cannot make more than one memory reference at a time on one memory bank. However, several different memory banks may be in operation simultaneously.

Arithmetic Section

The arithmetic section (see Figure 3) contains an exchange register (X) which is used in most operations where data is transferred to or from the Z register. It is also used as an exchange path for many other transfers within the compute module. The arithmetic register (A) is used for nearly all arithmetic, logical, and shifting operations. In addition to the A register, the auxiliary arithmetic register (Q) is used to provide an extension to the A register. The two are connected to form a 26-bit AQ register in multiply, divide, and certain shifting operations. The auxiliary arithmetic register (A') is the receiver of all adder computations, and a secondary auxiliary arithmetic register (Q') provides a 13-bit second-rank Q in shifting a transfer operation.

The actual arithmetic element is the adder. The adder has inputs from the A, Q, X, Q', P, and buffer entrance (BER) registers, and also has a standard +1 and +2 input. The input from the X register can be either the contents of X or the complement of the contents. If the positive contents of X are energized into one side of the adder and the contents of A into the other side, the result (which goes to A') will be $(X) + (A)$ where the parentheses are read as "the contents of X" and "the contents of A." If the complemented contents of X are energized into one side of the adder and the contents of A into the other, the result will be $(A) - (X)$. The +1 input is used in replace-add-one instructions and in advancing the program control register (the P register). The constant +2 is added to (P) in some instructions.

Control Section

The first functional element of the control section (see Figure 3) to be considered is the P register. This 13-bit register contains the address of the instruction being executed. The P register is updated through the adder; the contents of the P register are gated into one adder input and +1, +2, or input from the X register (for relative addressing) is used as the other input. The memory address register (S) holds the address of every memory reference. It has inputs from A', P, and X and outputs to P, S', or the external S' register in the 169G memory modules.

The function register (F) is a 13-bit register that holds 13 bits of the instructions being executed. It receives its inputs from the Z register and procedures its outputs to the translator, which performs the instruction translation and sends the proper signals to control the required operations. The F' register, an extension of F, is a 5-bit register and is used with the lower 5 bits of F as a decreasing counter in multiply, divide, and some shifting operations.

The main timing control issues commands to all sections of the compute module and governs all functions performed therein. One input to the main timing control is from the interrupt logic.

Certain internal and external conditions arise that make it necessary for the main program to be notified of their presence. An interrupt is the program signal that transfers control to some fixed location in memory without losing the information needed to return to the main program.

A signal, on any of the interrupt lines into the interrupt logic, results in a signal to the control logic that interrupts the routine presently being performed except under conditions where the interrupt function has been locked out. Upon interruption of the present routine, program control is transferred to the routine which services the active interrupt. Regardless of the type of interrupt, the same general procedure is followed. The compute module stores the address of the next instruction to be executed in the routine that has been interrupted and reads the instruction contained in the special storage location associated with the active interrupt. At the completion of the interrupt routine, the next instruction in the interrupted routine is read from memory and program control is returned to the interrupted routine.

Each compute module (Command and Display) has an associated control console. The console, consisting of a display panel and a switch panel, contains the controls and indicators necessary for maintenance and operation of the computer. The display panel contains three status indicator displays and four 13-bit register displays. The switch panel is a row of pushbuttons that are used to exercise manual control over the computer.

Input/Output Section

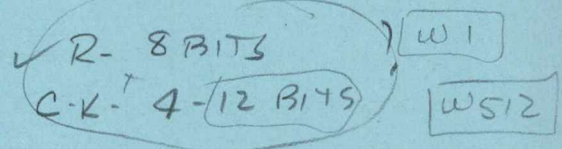
The input/output section utilizes two different types of information transfer: buffered transfer and nonbuffered transfer. A nonbuffered input/output transfer is one in which the execution of program instructions is halted while information is transferred between the computer memory and some external device. In this type of input/output operation, all the computer high-speed calculating and logic capabilities cease for as long as it takes to complete the information transfer. This method of transfer is efficient in transferring a few words of data at a time (it is most efficient when the transfer is performed at the rate of one word at a time). The nonbuffered input/output transfer uses the X register as an input/output register and uses the compute module main timing control to control the transfer.

A buffered input/output transfer interrupts the execution of computer instructions if the transfer is being made into or out of the same (8192 word) bank of memory in which the program is being run. If the same bank of memory is being utilized, a word transferred out of the computer memory takes one memory cycle from the computer program; on input, the time taken from the program is between one and two memory cycles. If difference memory banks are being used, no cycles are taken from the computer program on output, but one cycle is taken on input. (Note that these subtractions

from the computer program are only for the buffered channel of the compute module - for the other buffered channels, the times are one and one if the program and input/output channel are using the same memory module and zero and zero if they are not.)

To perform a buffered transfer of data, the input/output channel must be informed of two things:

- The complete address of the first data word.
- The complete address of the last data word.



The numbers identifying these two quantities are placed into two special registers prior to starting the information transfer. The first register is called the buffer entrance register (BER); it holds the memory address of the work currently being transferred.

BER
BUFFER
ENTRANCE

Each time another word is transferred, the number in this register is automatically incremented by one count. The second register is called the buffer exit register (BXR); the number it holds is the memory address of the last word to be transferred plus one. A buffer operation has been completed when the number in the BER has been incremented to a value that makes it equal to the number in the BXR. A special comparator in the I/O section senses for this condition of equality and generates a buffer termination signal when the condition appears.

7
BXR
BUFFER
EXIT

In any buffer operation, the data being transferred is handled by a register called the buffer data register (BFR). This register holds the data until the external device can recognize it and set itself up to process it (for an output transfer) or until the compute module can be accessed (for an input transfer).

BFR
BUFFER
DATA
REGISTER

169G MEMORY MODULE

128x64

Each 169G external memory module contains 8192 (8k) words. The total memory cycle time of the 169G is the same as that of the internal memory (1.36 microseconds). Up to 15 external memory modules may be controlled by one compute module giving a maximum of 131,072 memory locations per compute module. Each memory module contains nine access channels, which may service either compute or input/output modules.

Figure 7 illustrates a block diagram of the 169G memory module. It contains circuitry for core storage address and bank selection, scanner, read-write, and parity. The

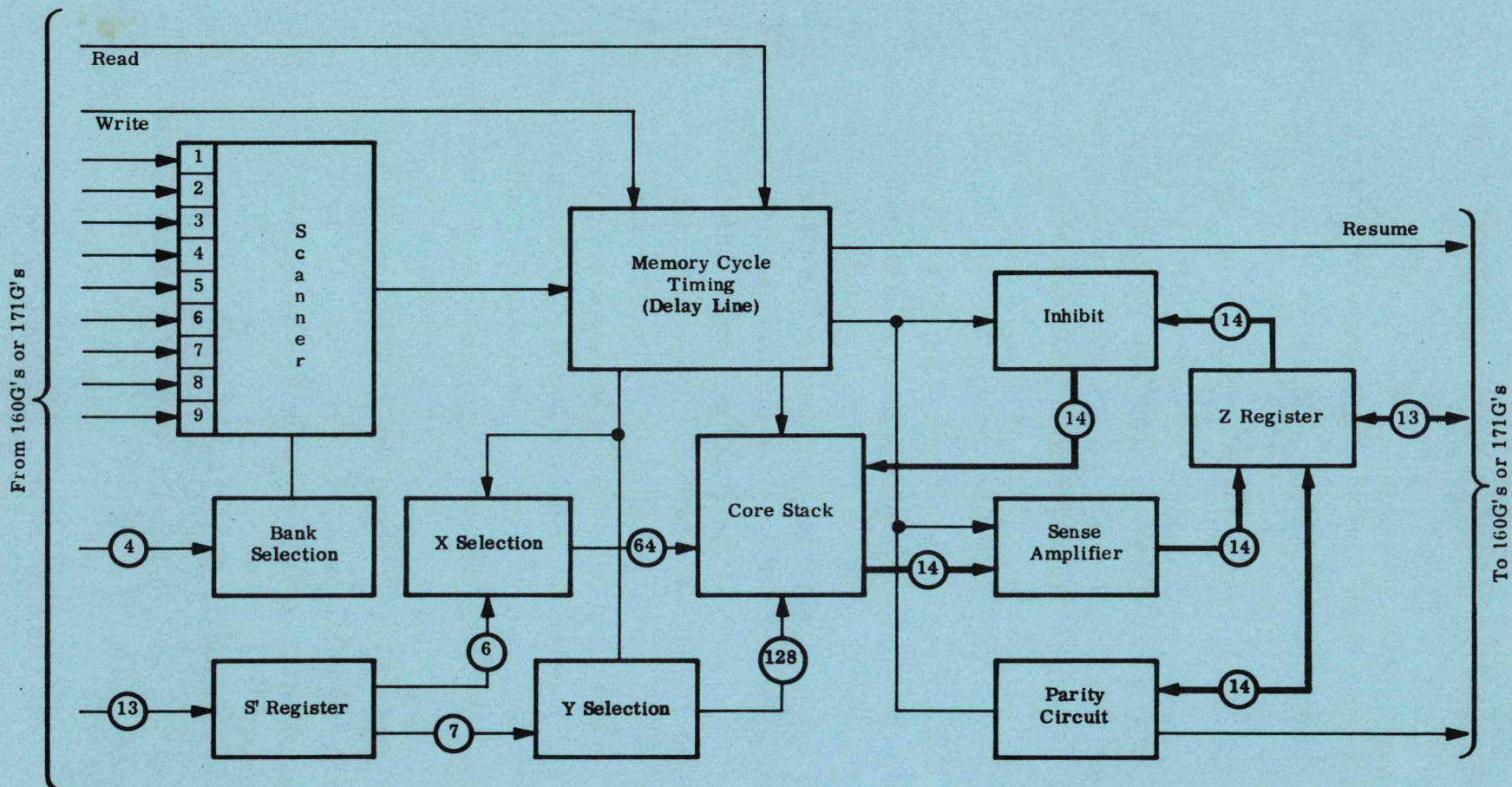


Figure 7. 169G Memory Module Block Diagram

operation of these sections is explained in the following paragraphs. The core stack used in the 169G is the same as that used in the compute module. Address selection is accomplished by translation of the output of the address selection register (S') to select one X and one Y drive line of the core memory. This register receives its inputs from either the S register in the compute module or the buffer entrance register in the I/O module. The 13-bit address is divided into an upper 7 bits, which select one of 128 Y drive lines through the core stack and a lower 6 bits, which select one of 64 X drive lines through the stack. Since the X drive line threads all four quadrants in a plane, and the Y drive line selects two of the four quadrants in a plane, two cores are selected per plane. Thus, two data bits are stored per plane in the memory.

The memory module also contains a 4-bit bank selection circuit to differentiate each module from the 14 other modules and the internal memory that can be selected by the computer. The compute or I/O module transmits a 4-bit number to select one of the 15 external memory modules and this number, together with the 13-bit address, completely specifies any one of the maximum of 131,072 memory locations in the system.

A scanner sequentially examines each of the access channels to determine which channel has requested a memory reference. When a request is present, the scanner stops on that channel to process the request. Toward the end of the ensuing memory cycle, the scanner restarts from the point at which it stopped, thereby examining the next channel in sequence upon starting. The operation of the scanner is of the sequential rather than the return-to-start type; this prevents one access channel from hopping the scan.

When the scanner recognizes a request, it sends a signal to the memory cycle control, which starts the requested memory cycle. The memory cycle gates the address selection and read-write circuitry and then issues a resume signal to the computer or I/O module that requested the reference.

For a read operation from memory, the data is transferred from memory to the Z register (the data restoration register) by setting those bits of Z that receive a one from the sense amplifier during the read portion of the memory cycle. For a write into memory, data is transferred into the Z register during the read portion of the memory cycle from either the X register of the compute module or the BFR register of an input/output module. During the write portion of a memory cycle, the Z register controls the inhibit current to the core memory and, thereby, controls whether a one or zero is stored at the selected address.

The parity circuit monitors the 13 bits of Z in a write operation and writes a 14th bit such that the word stored in memory always contains an odd number of one bits (odd parity). In a read operation, the 14 bits are checked for odd parity, and should an error be detected, a signal is sent to the compute or input/output module that is being serviced at the time to inform it of the erroneous readout.

171G INPUT/OUTPUT MODULE

The 171G I/O module contains two buffered bidirectional data channels, each having its own control and interrupt circuitry. A maximum of three I/O modules may be controlled by a single compute module. The compute module has control of the I/O modules in the setting up and initiating of any I/O action. After the action has been initiated, control is maintained by the I/O module, and all data interchange is with memory modules. Each channel has the ability to perform an I/O operation independently with the use of a time-sharing memory request circuit for the two channels.

Figure 8 illustrates a block diagram of the 171G I/O module. It can be seen from this diagram that the interface connections between the 171G and the compute and memory modules are common to both channels of the 171G module.

The 171G and 160G interface consists of 13 bidirectional data lines. These lines are used to transmit function codes to the I/O module and response codes to the compute module. These are also used by the compute module in setting up the control registers in the 171G. There are also 26 control and indication lines used for channel selection, interrupt, and other control functions.

The 171G and 169G interface contains 13 bidirectional data lines that are used to transfer input and output data between the two modules. There are also 17 address selection lines (13-bit address, 4-bit bank) from the 171G to the 169G modules. Six control lines used for requests, resumes, etc., form the control portion of the interface between the two modules. These interface connections are time-shared by both channels within each 171G module.

The other circuitry contained in each channel is quite similar to that contained in the buffered channel of the compute module. Each channel contains a 13-bit BFR, BXR, BER, and a 4-bit buffer bank control register (BBC). The channels also contain control, comparison, and interrupt circuitry.

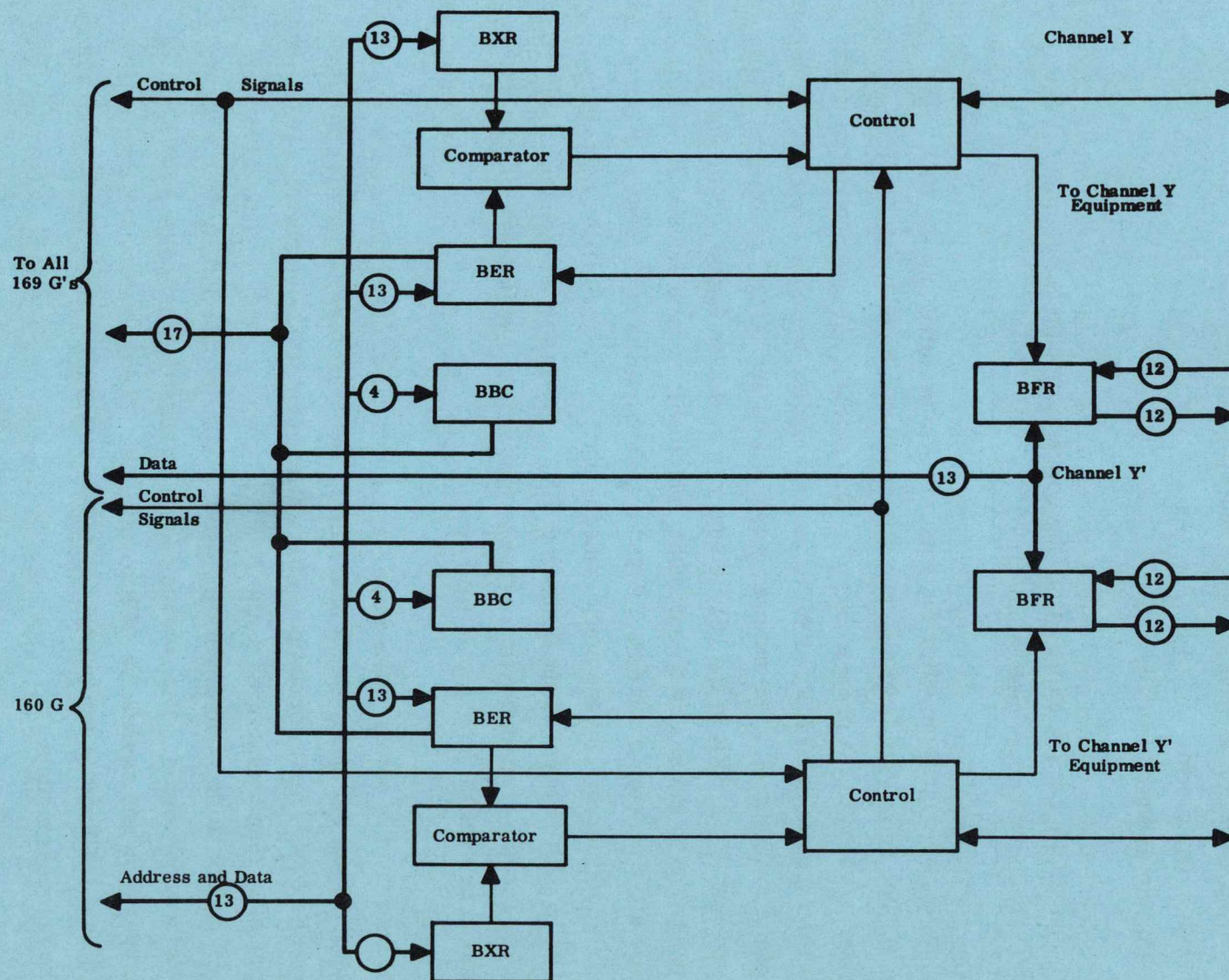


Figure 8. 171G External Input/Output Module Block Diagram

Since a channel in the 171G module is quite similar to the buffered channel of the compute module, its operation is also similar. The basic input/output process includes the following steps:

- a. Request and check status.
- b. Set up BER, BXR, BBC.
- c. Select equipment.
- d. Initiate action.

All these operations are the same as for the compute module buffer channel except that an I/O channel number must be specified.

On a typical output operation, after the equipment is selected and the BER, BXR, and BBC are set up, an initiate buffer output command will combine with the channel selection number to activate the proper channel. Once started, the I/O channel circuitry will gate the contents of BER and BBC to the appropriate memory along with a memory request and a read signal. The memory word will be read from the selected memory and transmitted to the BFR in the 171G along with a resume signal. This data will then be passed on to the selected equipment, which will issue a resume back to the I/O module after receipt of the data. This resume from the equipment will cause the BER register to increase by one count, and the entire process will be repeated until the number in BER is equal to the number of BXR. At this time, a signal (BER=BXR) from the I/O module terminates the operation and causes a buffer termination interrupt signal to be sent to the compute module.

The input operation is set up in the same way as the output operation except that an initiate buffer input command starts operation. The 171G takes control and immediately sends a request for information to the selected external equipment. Data from the equipment is then transferred to the BFR along with a ready signal to the 171G I/O control. Data is then gated from BFR to the selected 169G along with a memory request and a write signal. The resume issued by the 169G indicates completion of the write operation and causes the BER to advance. The operation will then repeat until the signal (BER=BXR) terminates control and the buffer termination interrupt is sent to the compute module.

In addition to the input and output buffering capabilities that the 171G has, it also is able to provide the data path and control signals to transfer information between 169G memory modules. This transfer enables entire blocks of information to be exchanged

between two 169G memory modules or within the same memory modules. The operation involves an input buffer on one channel and an output buffer on the other channel of a 171G I/O module. Figure 9 depicts the assignment of the various peripheral equipment to each of the input/output channels.

PROGRAMING

A digital computer, such as the Control Data Corporation (CDC) 160G, is incapable of performing useful operations on its own. To accomplish any operation or series of operations that the machine is capable of performing, the computer must be told, step by step in a language it is capable of understanding, exactly what to do and the order in which it is to do it. This process of telling the computer what to do is referred to as programing. Emphasis will be placed on data transfer and addressing rather than on specific instructions. For programing purposes, there are two types of information stored in memory, operands and instructions. The operand is the information that is acted upon (add, subtract, shift, etc.) and the instruction contains all information (command and address) necessary to perform the action.

OPERATING MODES

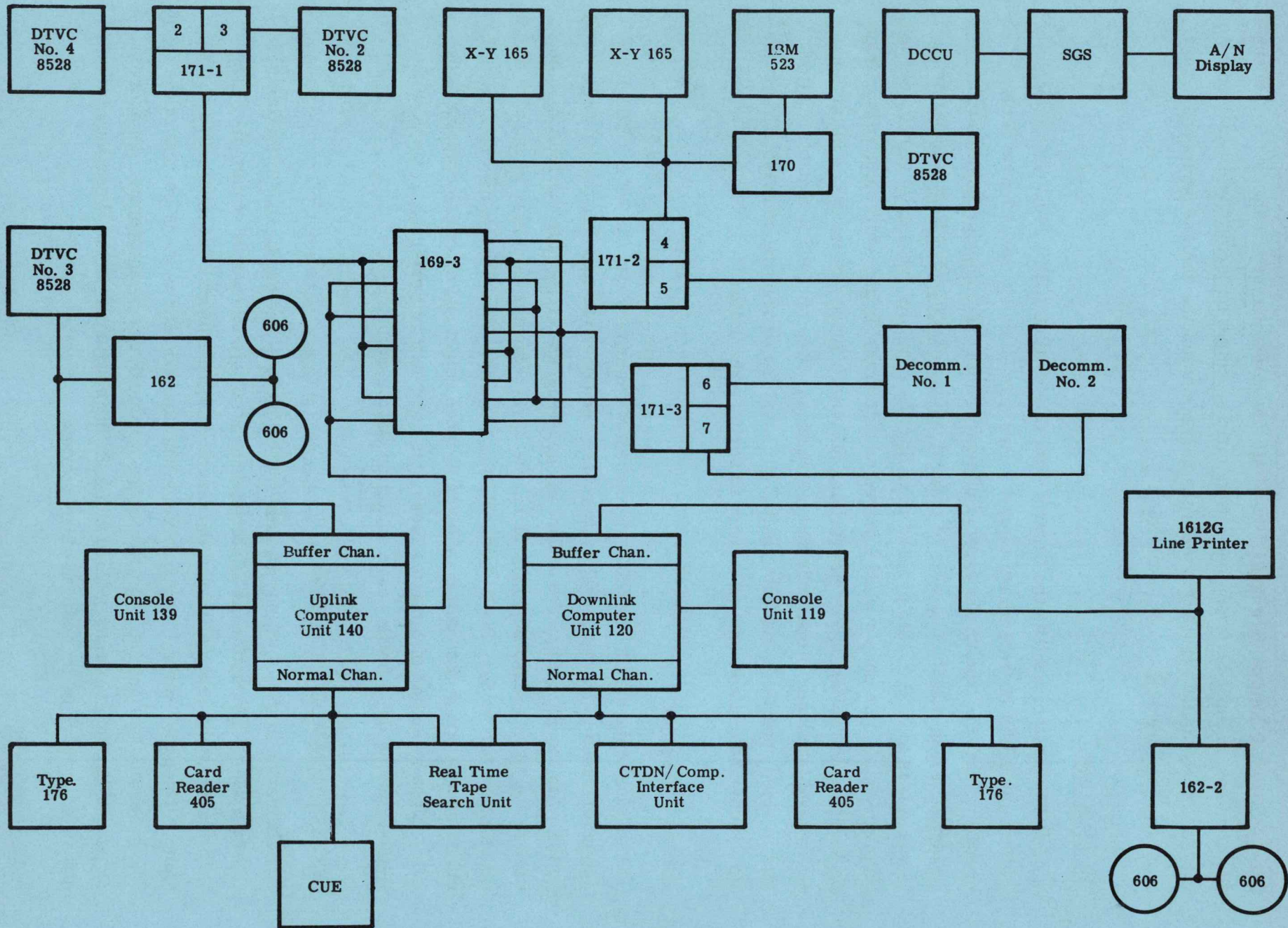
The original computer in the CDC 160 series of computers was the 160A. The 160G computers used in the ACE-S/C system have been designed and constructed to be compatible with the 160A computer. That is, any program written for the 160A may be used in the 160G without change. Thus, the 160G computer is said to be capable of operating in two modes, the A-mode and the G-mode. The A-mode may be selected either by a program instruction or by an A-mode select switch on the computer console. Upon execution of a master clear, the computer automatically reverts to the G-mode unless the A-mode select switch is depressed.

INSTRUCTION WORD FORMAT

An instruction in the 160G may be either 13 or 26 bits (see example). If the instruction is a 26-bit instruction, it is stored sequentially in two words of memory. The format of a 13-bit instruction and the format of word 1 of a 26-bit instruction are the same. The upper seven bits constitute a function code and is the F portion of the word. The lower six bits are the E portion of the word and may be an operand, an address, or part of the function code. Word 2 of a 26-bit instruction is the G portion of the instruction and may be an address or an operand.

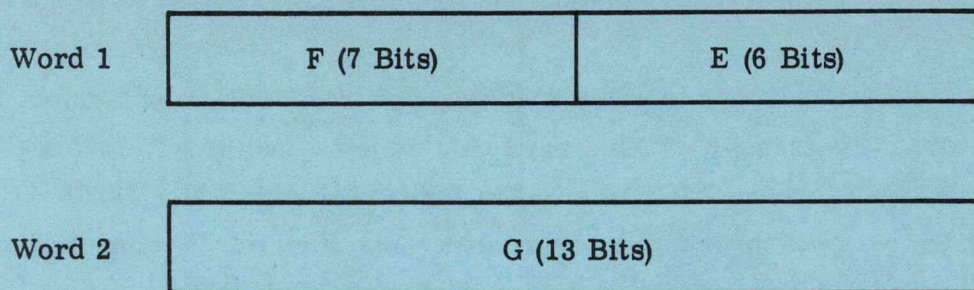
FIG 9

FOR TRAINING PURPOSES ONLY



FOR TRAINING PURPOSES ONLY

Figure 9. Data Processing I/O Channel Assignment



STORAGE CONTROLS

A 160G compute module may address up to 15 banks of external memory. These, plus the internal bank, add up to 131,072 words of storage that the 160G may address directly. For a memory of this size, the compute module must provide a 17-bit address to specify uniquely any particular word in memory. To provide the additional bits necessary to give a 17-bit address, the storage bank control register is used.

STORAGE BANK CONTROL

A reference to memory may be classified as one of four types:

- To input or output information on a buffer I/O channel.
- To read in instructions or to locate a constant or counter that is associated with a program.
- To read or store an operand or data.
- To update an index register, an index register reading, or an address reference for indirect addressing.

The 20-bit storage bank control register is divided into four groups of five bits each. Each group is assigned to one and only one of the four types of memory reference. The 160G then automatically classifies each memory reference into one of the four types and uses the appropriate part of the storage bank control register to complete the 17-bit address. The four types of memory reference are referred to by the following names: Type 1 reference is the buffer bank; Type 2, the relative bank; Type 3, indirect bank; and Type 4, direct bank.

ADDRESSING MODES

The 160G has 14 basic data handling instructions. Each of these basic instructions may have as many as 12 variations or addressing modes.

INPUT/OUTPUT

The purpose of the I/O circuitry is to permit the transfer of data between memory and external equipment. This transfer of data may be either a normal or buffered operation. Normal data transfer completely ties up the compute module while a buffered operation allows the compute module to be free most of the time for other operations. When the compute module communicates with external equipment, it executes an External Function (EF) code which is a 12-bit code that is read from memory into the X register.

READ NEXT INSTRUCTION (RNI) AND ADVANCE P SEQUENCES

The RNI and advance P sequences are important because they are the part of each instruction that enables the computer to step sequentially from instruction to instruction. Since P contains the address of the current instruction and S contains the address of the next instruction, the usual flow of instruction addresses will be from S to P. The only exceptions to this flow are on an enter instruction, the initial instruction of a program, a Buffer 2 operation, and an output buffer operation.

The RNI sequence performs two important operations:

- a. A memory reference cycle is initiated and the instruction in the memory address given by the S register is transferred to the X and F registers.
- b. The P and S registers are updated.

At the end of an RNI:

- a. The E portion of the instructions is in the X register.
- b. The instruction is in the F register.
- c. $P + 1$ is in the A' register.

COMPUTER PERIPHERALS

There are several standard peripherals associated with the CDC 160G computers.

They are:

- a. 4-606 Magnetic Tape Transports.
- b. 2-162G Magnetic Tape Synchronizers.
- c. 1-162G High Speed Printer.
- d. 2-165G X-Y Plotters.
- e. 2-176G Monitor Typewriters.
- f. 2-405/177G Card Readers.
- g. 1-IBM 523/170 Card Punch.

Peripherals are extensions of the computer - the voice and ears of the system. They are the only means available input information (programs and subroutines) efficiently into the computer and to record processed data from the computer. Some of the peripherals may be both input and output devices, and some are limited to either input or output operations, but not both.

606/162G MAGNETIC TAPE SYSTEMS

The magnetic tape transport (606) provides a high-speed medium for recording and retaining information or for delivering information to the computer. Information is read or written by passing the magnetic tape over read/write heads.

Information is written on the magnetic tape by using seven individual write heads. All seven heads write information simultaneously across the tape so that each frame of data is composed of a 6-bit character and a vertical parity bit. Tracks 0 through 5 contain the data, and track 6 contains a parity bit. These frames are formed into groups called records (program controlled) and at the end of each record a check character is written. This character is made up of seven longitudinal (horizontal) parity bits, one for each channel. Thus, parity is checked vertically, frame by frame, and horizontally, channel by channel.

A non-return-to-zero (NRZ), change on ones, recording method is used. For this method, a binary one is recorded by changing the magnetic flux direction on the tape. If, in a certain time period, the magnetic field does not change directions, a binary zero is indicated.

The magnetic tape synchronizer (162G) provides communications between the computer and the tape transports. The synchronizer can also provide communications between the tape transports and the high speed printer in an off-line condition. The 162G, controlled by EF codes from the computer:

- a. Controls the magnetic tape transports.
- b. Transfers information between the computer and the magnetic tape transports.
- c. Converts the data to a usable form.

Figure 10 shows the major communications between the 160G computer and its associated peripherals.

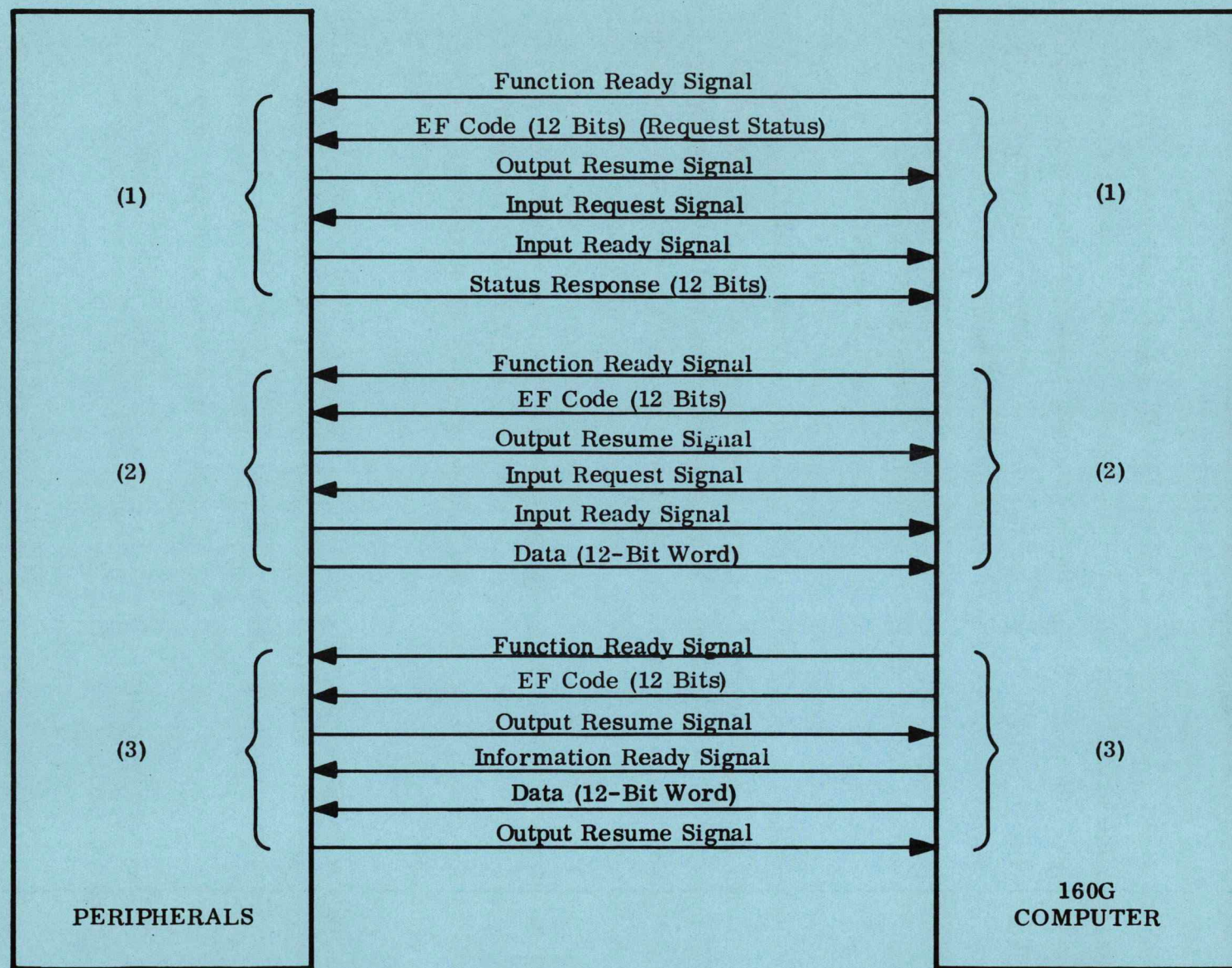


Figure 10. Signal Transfers Between 160G and Peripherals

1612G HIGH SPEED PRINTER

The 1612 high speed printer is a computer output device. The computer may transfer data to it for presentation, but it cannot input data to the computer.

The high speed printer accepts Binary-Coded-Decimal (BCD) information from the computer and prints the information out on fan-fold forms for observation and recording purposes. The 1612G can print up to 1000 lines per minute with each line containing 120 characters. A choice of 64 different characters, or symbols, are available on the print drum for selection.

Since the high speed printer cannot be used as a computer input device, only the signal transfers indicated in Groups (1) and (3) of Figure 10 will be utilized.

165G X-Y PLOTTER

The 165G X-Y plotter is a high-speed, two-axis recorder that can trace a visible plot of one variable against another. The plot is accomplished by means of a carriage-mounted ballpoint pen, writing on paper placed on a bi-directional recording drum. The paper feed and take-up mechanism handles paper rolls 100 feet long and 12 inches wide. Recording drum sprocket teeth engage sprocket holes in the paper in order to drive the paper past the pen. The control section of the plotter provides the interface between the computer and the plotter mechanism.

Since the X-Y plotter is only a computer output device, the signal exchanges in Groups (1) and (3) of Figure 10 are applicable.

176G MONITOR TYPEWRITER

The 176G typewriter serves as both an input and an output device for the computer. A manual input to the computer may be accomplished from the keyboard, or a typewritten copy of specific computer memory locations may be derived by automatic computer instruction at a rate of about 10 characters per second. The typewriter is normally used to type out operator instructions when manual intervention is needed during a program.

Since the 176G may be used as an input and an output device, the signal transfers indicated in Groups (1), (2), and (3) of Figure 10 are applicable.

405/177G CARD READER AND CONTROLLER

The 405 card reader and controller provides a fast and efficient source of information to the computer. It can read up to 1200, 80-column cards or 1600, 50-column cards per minute. (Eighty-column cards are used in the ACE-S/C system.)

The card reader supply tray and primary receiving tray have capacities of 4000 cards. The secondary receiving tray, used as a limited sorter or to store rejected cards, has a capacity of 240 cards. The cards contain binary or Hollerith coded information, and the data is read from the cards by means of a photoelectric read station.

The card reader acts as an interface unit between the CDC 160G computer and the CDC 405 card reader. It provides the necessary control logic to transfer data from the 405 to the 160G and, upon computer instruction, tells the 405 what operation to perform (such as, read card binary, read card Hollerith, continuous read, single-cycle read, etc.). When the card reader is instructed to read binary data, the 177G transfers the information column (12 bits) by column to the computer as the computer requests an input. When the card reader is instructed to read Hollerith coded data, the 177G translates a Hollerith column (12 bits) to 6-bit BCD, temporarily stores the data, translates the next Hollerith column to 6-bit BCD, and then transmits the 12-bit word containing two BCD characters and representing two columns of information on the card to the computer. This process is known as "packing." A binary card may usually be recognized by the punch configuration in the first column. If rows 7 and 9 in the first column are both punched, the card contains binary information. If either row 7 or row 9 is not punched in the first column, the card may contain Hollerith coded information.

The 405/177G can only be used as a computer input device. Therefore, the signal exchanges indicated in Groups (1) and (2) of Figure 10 are applicable.

IBM 523/170 CARD PUNCH AND CONTROLLER

The IBM 523 card punch mechanically punches cards at a rate of 100 cards per minute. These cards are the 80-column type, but as many columns as desired, up to 80, may be punched on any one card.

The CDC 170G card punch controller interfaces the 160G to the 523. The controller provides the necessary signals, translations, and transfers for the computer to provide program instruction for the card punch. The controller provides temporary storage

for data from the computer to be punched onto cards. It also controls the transfer of data from the computer to the card punch. The 523/170G is strictly a computer output device, and, therefore, the signal exchanges shown in Groups (1) and (3) of Figure 10 are applicable.

PART II - SYSTEM PROGRAMING

In previous study guides, the command or uplink loop was discussed in terms of hardware functions. These discussions embraced the operation of the data entry equipment and the 160G Control Data Corporation computer and the functional relationship between these two entities. Since the command computer is a stored program processor, it now becomes necessary to discuss the command loop operation in light of the various programs that are stored in the computer's memory. In addition to discussing the functional aspects of the programs, it is necessary to understand the functional aspects of the programs, it is necessary to understand the general programing requirements, program structure, program preparation and verification, and a general understanding of the many terms utilized in conjunction with the programing effort. To enable the operator to understand program application in the ACE-S/C system, a working knowledge of the various terms used in describing program operation is necessary. A list of these terms follow:

ABSOLUTE CODING: Coding written in numeric language acceptable to the machine without further modification.

ACCESS, RANDOM: Access to storage under conditions in which the next position from which information is to be obtained is independent of the previous one.

ACCESS TIME: The time interval between the call for a unit of information from a storage device and the delivery of that information.

ADDER: A device capable of forming the sum of two quantities.

ADDRESS: A label, name, or number identifying a register, a storage location, or a device from which information is received or to which it is transmitted.

ADDRESS, ABSOLUTE: The label(s) assigned by the machine designers to a specific storage location.

ADDRESS, BASE: A number that appears as an address in a computer instruction, but which is to be modified; e.g., by adding the contents of one or more index registers before it is used.

ADDRESS, DIRECT: An address in a computer instruction that indicates the location where the referenced operand is to be found or stored.

ADDRESS EFFECTIVE: A modified address; the address actually used in a particular execution of a computer instruction.

ADDRESS, INDIRECT: An address in a computer instruction that indicates a location where the address of the referenced operand is to be found.

ADDRESS, RELATIVE: A number of the form of an address that specifies the position of a storage location with respect to some base address. The absolute address of the storage location is obtained by adding the relative address to the base address.

ADDRESS, SYMBOLIC: A label chosen to identify a particular work, function, or other information in a routine, independent of the location of the information within the routine.

ALPHANUMERIC: Characters that may be either letters of the alphabet, numerals, or special symbols.

ARITHMETIC UNIT: The part of a computer where logical and arithmetic operations are performed.

ASSEMBLY PROGRAM: A computer program that produces machine instructions from symbolic input.

BANK: A unit of core storage with provisions for storing 4096 or 8192 words. The use of more than one bank permits increasing the storage capacity of a computer without increasing the word length implicitly necessary to extend the range of storage addresses. In the 160A or the 160G, this address is effectively increased by set storage bank control instructions which determines which banks will be used during the program.

BCD: Binary Coded Decimal.

BINARY CODED DECIMAL: Representation of alphanumeric characters by combinations of binary digits.

BLOCK: A group of words considered or transported as a unit; in flow charts, an assembly of boxes, each box representing a logical unit of programing, usually requiring transfer to and from the high-speed storage.

BOOTSTRAP: The coded instructions at the beginning of an input medium (tape or cards), together with instructions inserted by switches or buttons into the computer, which are used to read programs into memory.

BREAK-POINT: A point in a routine at which special action is taken, such as a stop or a transfer, either as the result of the insertion of a special instructions or the setting of a console switch. Usually used in debugging.

BUFFER: A device in which data is stored temporarily in the course of transmission from one point to another.

BUFFERED (INPUT/OUTPUT): A term indicating that the computer may carry on high-speed computation at the same time it is exchanging data with a peripheral device.

BUG: A mistake in a routine; an equipment malfunction.

BYTE: A group of binary digits usually operated upon as a unit.

C-START: Computer communications START module.

CALLING SEQUENCE: A set of characters identifying a subroutine and containing information concerning parameters to be inserted in the subroutine, information to be used in generating the subroutine, or information related to the operands; a call-word when exactly one word is filled.

CHANNEL: A transmission path (e.g., one connecting the computer to external equipment).

CHARACTER: One of a set of symbols, usually restricted to a member of a specific alphabet or appropriate to a particular computer. The symbols may include the letters A through Z, digits 0 through 9, punctuation marks, operation symbols, or any other symbols which a computer may read, store, or write, more precisely, the coded computer representation of a symbol drawn from its alphabet (e.g., one might represent the symbol "A" as the character 100001 in a specific computer alphabet).

CHECK SUM: A check in which groups of digits are summed, usually without regard to overflow, and that sum checked against a previously computed sum to verify accuracy, also, the previously computed sum.

CLEAR: To reset a register by placing every stage in the "0" state.

CODE: (Verb) To perform that part of the programmer's job that involves the writing down of the sequence of instructions that make up a computer program.

COLLATE: To merge items from two or more similarly sequenced files into one sequenced file without necessarily including all items from the original files.

COMMAND: A signal that performs a unit operation, such as transmitting contents of one register to another, shifting a register, setting a flip-flop.

COMPILER: A computer program that translates instructions written in a technical or problem-oriented language into machine language. Usually more than one machine instruction results from each symbolic instruction.

COMPLEMENT: See One's Complement or Two's Complement.

CONTENT: The quantity or word held in a register or storage location.

CORE: A small ferromagnetic toroid used as the bi-stable device for storing a bit in a memory plane.

COUNTER: A device, register, or storage location for storing integers, permitting these integers to be increased or decreased by unity or by an arbitrary integer, and capable of being reset to zero or to an arbitrary integer.

CRT: Cathode Ray Tube.

CSR: Check Status Reply.

CUE: Communications Unit Executor.

DATA REDUCTION: The process of transforming masses of raw test or any experimentally obtained data, usually gathered by instrumentation, into useful, ordered, and simplified intelligence.

DCCU: Digital Communications and Control Unit.

DEBUG: To isolate and remove all malfunctions from a device or all mistakes from a computer program.

DENSITY, PACKING: The number of units of useful information contained within a given linear dimension, usually expressed in units per inch, e.g., the number of bits stored on tape per linear inch on a single track by a single head.

DIGITIZE: To convert an analog measurement of a physical variable to a numerical value, expressing the quantity in digital form.

DIAGNOSTIC PROGRAM: See Maintenance Program.

DOWNLINK CONTROL PROGRAM: A computer program that receives, processes, and displays, in real time, telemetry data from the spacecraft.

DTCS: Digital Test Command System.

DTVC: Digital Transmission and Verification Converter.

DUMP: To copy the contents of part or all of some storage medium into another storage or display medium.

EBM: Execute DTCS buffer memory.

EDITOR: A routine to insert, delete, replace, or rearrange data.

END-AROUND BORROW: A borrow that is generated in the highest order stage of an accumulator or counter and sent directly to the lowest-order stage.

ENTER: To place manually a quantity into a register.

EXECUTION ADDRESS: Most often used to specify the storage address of an instruction or operand. Sometimes used as the operand.

EXTERNAL FUNCTION CODE: A 12-bit code used to select and specify that an external device; e.g., a printer or tape is to perform some specific function.

FLIP-FLOP: A bi-stable storage device.

FUNCTION CODE: See Operation Code.

GASS: A general assembly system for the Control Data Corporation 160G computer system. GASS operates within MASS.

HANG UP: An unplanned computer stop or delay in problem solution, e.g., inability to escape from a loop.

HOUSEKEEPING: Operations in a routine that do not directly contribute to the solution of the problem at hand, but which are made necessary by the method of operation of the computer.

INDEX REGISTER: A register that contains a quantity, which may be used to automatically modify addresses (and for other purposes) under direction of the control section of the computer.

INITIALIZE: To set program variables, such as addresses, counters, etc., to the condition required in a routine prior to its use.

INPUT/OUTPUT: A collective designation for all communication facilities of a computer.

INSTRUCTION: A set of characters that, as a unit, cause a computer to perform one of its operations. Instructions may contain one or more addresses according to the number of references to operands in storage contained in the instruction.

INTERRUPT: A signal (or class thereof) that, when received and recognized by the computer, forces the computer to forestall its current operation and jump to a subroutine, the starting address of which is determined by the class of the interrupt.

I/O: Input/Output.

JUMP: An instruction or signal that, conditionally or unconditionally, specifies the location of the next instruction and directs the computer to that instruction.

K-START: Keyboard START module.

LBM: Load DTCS buffer memory.

LIBRARY: An ordered set or collection of standard and proven programs and subroutines used for data processing applications and the solution of problems.

LOAD: To bring information into memory from an external storage medium and to place a quantity from storage into the A register.

LOCATION: A storage position in internal or shared memory.

LOCKOUT: Any function (usually of machine logic) that inhibits an action that would normally occur if the lockout were not imposed.

LOGICAL OPERATIONS: The computer operations that are logical in nature, such as logical and, or, extract, and decisions. This is in contrast to the arithmetic operations, such as add, subtract, multiply, and divide.

LOOP: A given sequence of instructions operated upon repeatedly (normally, until a specified condition occurs).

MACRO: A symbolic instruction representing a frequently used sequence of machine language instructions.

MAINTENANCE PROGRAM: A diagnostic program to determine the operational readiness of any piece of computer or peripheral equipment and to isolate any malfunctions that occur.

MANAGEMENT INFORMATION AND CONTROL PROGRAM: A program that performs checking, processing, and/or analysis of data to furnish management with information for evaluation, control, and operation of activities for which it is responsible.

MASK: A prearranged pattern or configuration of bits in a computer word generally used for logical or bit manipulations.

MASS: A monitor and assembly system for the Control Data Corporation 160G computer system.

MICROSECOND: A millionth part of a second.

MILLISECOND: A thousandth part of a second.

MNEMONIC OPERATION CODES: Operation codes in symbolic notation, which are easier to remember than the actual operation codes of the machine.

MONITOR: A program that exercises supervisory control over some other programs or collections of programs. Also called executive routine or master routine.

NANOSECOND: A billionth part of a second.

OBJECT PROGRAM: A machine language program that is the final output of an assembly system.

OCTAL: Pertaining to the number base of eight.

OFF-LINE: Pertaining to the operation of devices that are under direct control of the computer.

ON-LINE: Pertaining to the operation of devices that are under direct control of the computer.

ONE'S COMPLEMENT: With reference to a binary number, it is that number which results from subtracting each bit of the given number from the bit "1."

OPERAND: Usually refers to the quantity specified by the execution address. This quantity is operated upon in the execution of the instruction.

OPERATION CODE: That part of an instruction designating the operation to be performed.

OSAS-A: A general assembly system for the Control Data Corporation 160A computer system.

OVERFLOW: The condition in which the capacity of a register is exceeded.

PARALLEL TRANSFER: A system of data transfer in which elements of information are transferred simultaneously over a set of lines.

PARAMETER: A quantity to which values may be assigned; used in subroutines and generators to specify item size, decimal point, block arrangement, field length, sign position, etc.

PARITY CHECK: A redundancy check technique based on an odd or even number of binary ones in some grouping of binary digits. In the binary representation of a character, a parity bit is made either zero or one, whichever is required to make the number of ones in the character an even number for even or an odd number for odd parity.

PARTIAL ADD: An addition without carries.

PROGRAM: A sequence of instructions that causes a data processing system to process a specific application; a plan for the solution of a problem.

PSEUDO INSTRUCTION: A symbolic representation of information to a compiler or interpreter; a group of characters having the same general form as a computer instruction, but never executed by the computer as an actual instruction.

PYRAMID, BORROW: A network of inverters that senses borrow conditions and produces borrow signals.

✓ R-START: Relay selection START modules.

RAW DATA: Data that has not been processed; may or may not be in machine-sensible form.

READ: To copy, usually from one form of storage to another, particularly from external or secondary storage to internal storage; to sense the presence of information on a recording medium.

REAL-TIME PROCESS: A process where the computer exists on-line in an environment that cannot be made subservient to computer control. Usually a continuous physical process is involved.

RECORD: A group of related facts or field of information that is treated as a unit.

RELOCATE: To move a routine from one portion of internal storage to another and, in so doing, to automatically adjust the address references so that the routine can be executed in its new location.

RETURN JUMP: A jump instruction that enables program control to be returned to the original sequence upon transfer to and completion of a second sequence of instructions.

ROUTINE: Essentially synonymous with "program," although generally restricted to describing single-purpose programs.

SEAL: To lockout; in a START module, to inhibit transmission of information to the computer.

SEGMENTATION: Division of a routine into parts, one segment being the "main program" and other segments being subprograms. The segments are linked together by CALL-type statements and may be compiled and debugged separately.

SERIAL TRANSFER: A system of data transfer in which elements of information are transferred in succession over a single line.

SGS: Symbol Generator System.

SHIFT: To move the bits of a quantity right or left.

SIGN BIT: The bit in the highest-order stage of the register (in registers where a quantity is treated as signed by use of ones complement notation). If the bit is "1," the quantity is negative; if the bit is "0," the quantity is positive.

SIGN EXTENSION: The duplication of the sign bit in the highest-order stages of a register.

SOURCE PROGRAM: A program coded in other than machine language that must be translated into machine language to be executed by a computer.

SPACECRAFT TEST PROGRAM: A computer program package containing the control programs, TEX's, etc., required to describe a single spacecraft test.

START: Selections To Activate Random Testing.

STATUS: The condition of an external device, as reflected in the response given a status interrogation by the computer.

The condition of a device, such as a computer, as shown by visual displays on its console.

STORAGE: Any device into which units of information can be copied, which will hold this information, and from which the information can be obtained at a later time.

STORAGE, TEMPORARY: Internal storage locations reserved for intermediate and partial results.

SUBPROGRAM: A segment of a larger program capable of being compiled and debugged by itself.

SUBROUTINE: The set of instructions necessary to direct the computer to carry out a well-defined mathematical or logical operation; a subunit of a routine.

SUBROUTINE, CLOSED: A subroutine not stored in the main path of the routine. Such a subroutine is entered by a jump operation with provision made to return control to the main routine at the end of the operation.

SUBROUTINE, OPEN: Has been, in general, replaced by the term "Macro Instruction." It is a subroutine inserted directly into the main path of the routine, not entered by a jump. Such a subroutine must be re-copied at each point that it is needed.

SUPERVISORY EXECUTIVE PROGRAM (SEP): The monitor program that exercises supervisory control over the use of spacecraft test programs during real-time testing of spacecraft.

SYMBOLIC CODING: Any coding system in which symbols other than machine addresses and machine language are used.

TABLE LOOKUP: A coding technique or an instruction that locates the word in a table corresponding to a specified word, and usually obtains some other word that corresponds to the word located.

TEST EXECUTIVE (TEX): A computer program or subprogram written specifically to meet spacecraft system test sequence requirements for real-time operation.

TEST FILE: One or more spacecraft test programs on magnetic tape, limited only by length of tape.

TWO'S COMPLEMENT: The two's complement may be formed by complementing each bit of the given number and then adding one to the result, performing the required carries.

UPLINK CONTROL PROGRAM: A computer program that generates commands to the DTCS to provide stimuli to the spacecraft according to information received from the CUE.

UTILITY PROGRAM: A program normally used to assist in the operation of a data processing system (e.g., memory dump, card to tape, etc.).

WORD: A set of characters which occupies one storage location and is treated by the computer circuits as a unit. Ordinarily, a word is treated by the control unit as an instruction and by the arithmetic unit as a quantity.

WRITE: To transfer information to an output medium; to copy, usually from internal storage to external storage; to record information in a register, location, or other storage device or medium.

Figures 11 and 12 illustrate the various program and system flow chart symbols that are utilized in the programming effort for ACE-S/C. An understanding of the flow chart symbology will make it easier for the reader to understand the program flow charts included in this document.

PROGRAMMING REQUIREMENTS

Table 1 depicts the general programming requirements for a typical ACE-S/C configuration. The requirements are broken down into seven distinct areas. The Downlink Data Processing and Display area involves the inputting of the PCM analog and event data words from the decommutation equipment and the selection or stripping out of the input words that are to be processed. In addition, the computer must be alerted as to the type of processing required so that the proper checks, conversions, formatting, and outputting routines can be accommodated. Downlink data processing will be discussed in more detail in a subsequent study guide. The Uplink Command Generation and Verification area involves the interrupt handling routines, command interpretation,

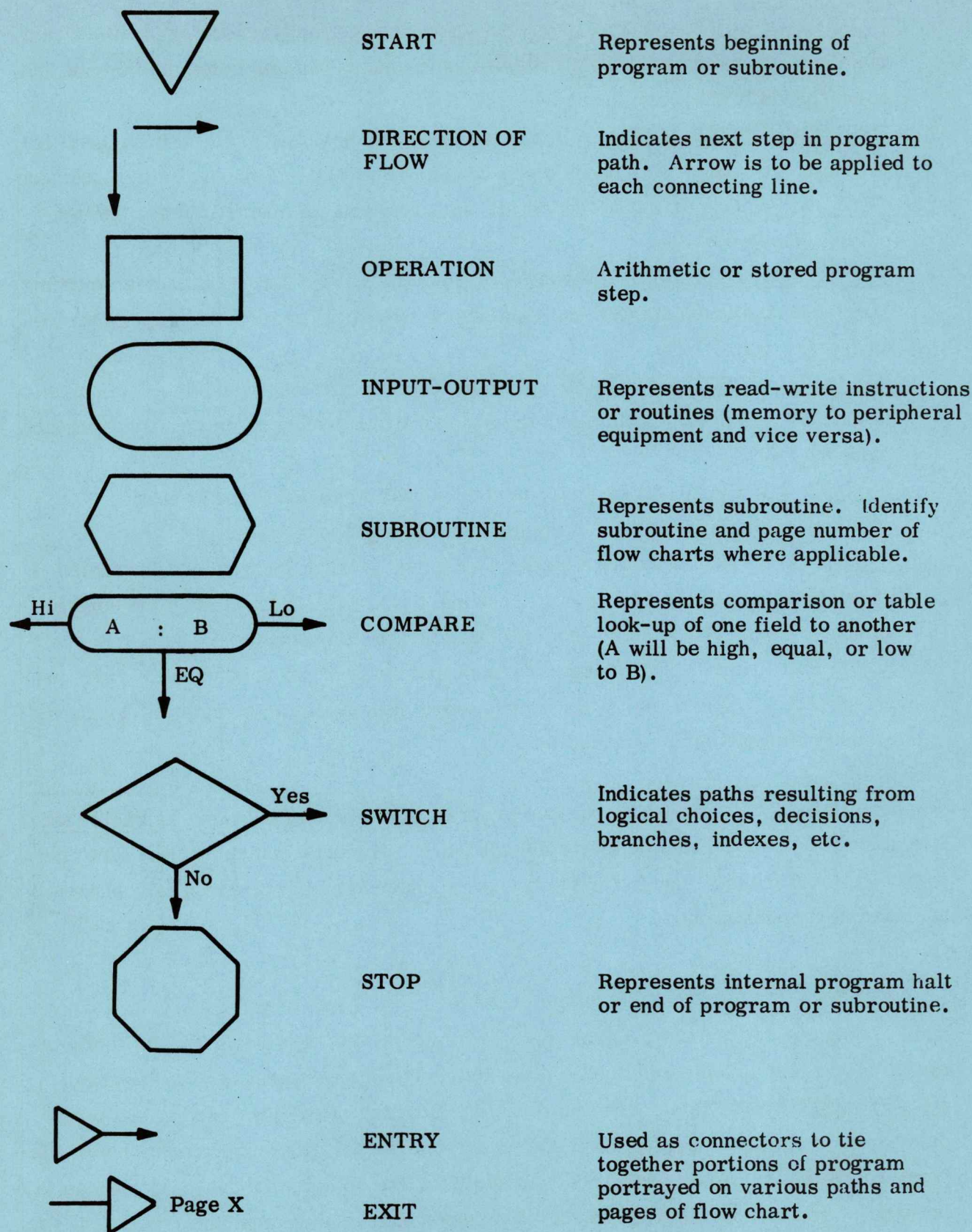


Figure 11. Program Flow Chart Symbols

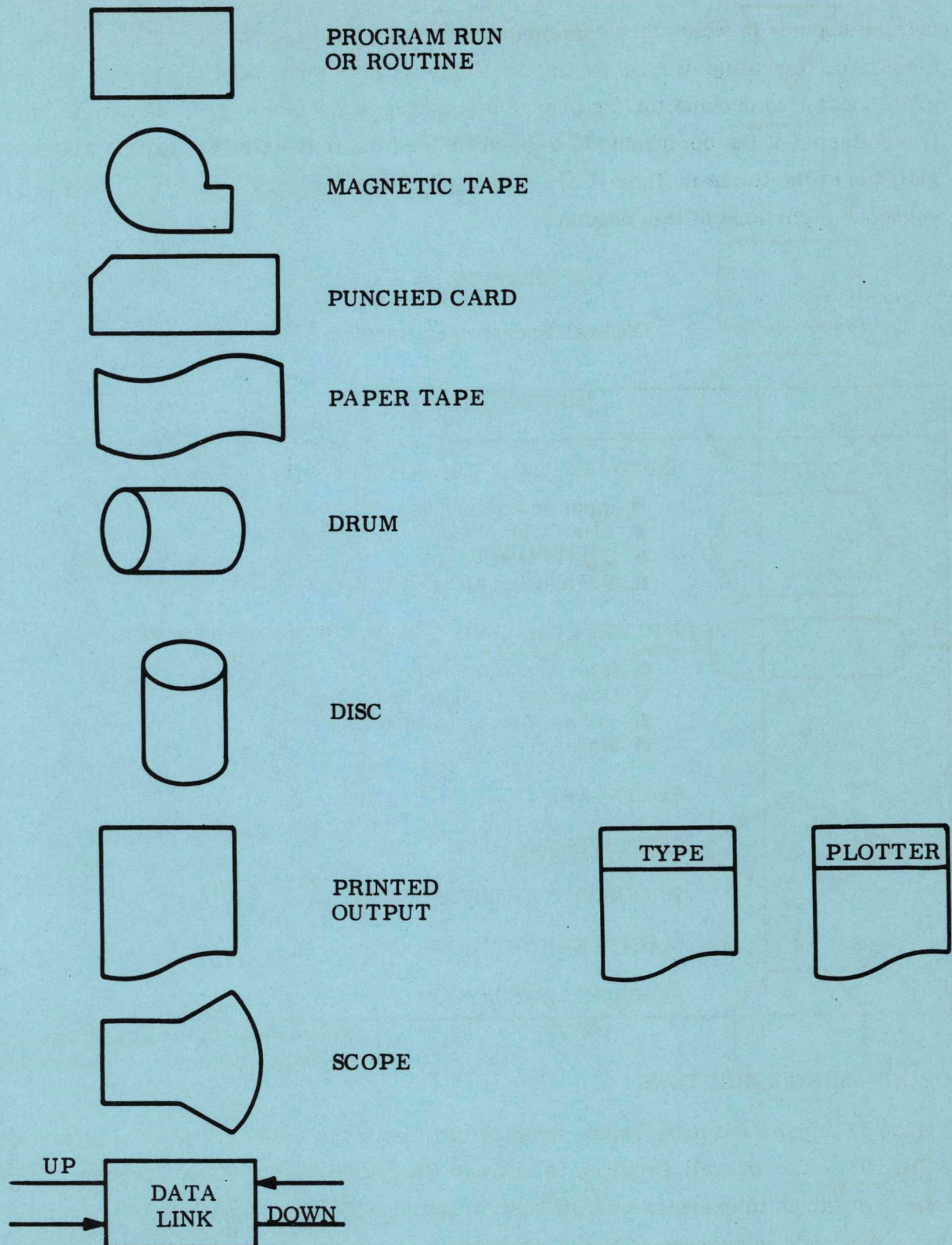


Figure 12. System Flow Chart Symbols

and the manner in which these commands are to be handled; for example, a relay closure or the callup of a subroutine that may initiate some other function. The program must also provide for the proper formatting of the commands and also for the transmission of the commands to the proper location in the test bay area. The remainder of the items in Table 1 are self-explanatory and they also will be covered in subsequent portions of this document.

Table 1
General Programing Requirements

No.	Program Requirements
1	DOWNLINK DATA PROCESSING AND DISPLAY ■ Input and Selection ■ Limit Checks and Adjustment ■ Conversion ■ Formatting and Outputting
2	UPLINK COMMAND GENERATION AND VERIFICATION ■ Interrupt Handling ■ Command Interpretation and Handling ■ Formatting and Outputting ■ Status Keeping
3	SELF-TEST
4	SUPERVISORY PROGRAMS
5	PROGRAM VERIFICATION
6	MAINTENANCE PROGRAMS
7	LIBRARY MAINTENANCE

PROGRAMING STRUCTURE

Figure 13 depicts the programing structure utilized in the conduct of spacecraft testing by ACE-S/C. The overall program is entitled Supervisory Executive Program (SEP). SEP is designed to exercise overall control and provide a means of rapidly changing computer loads to support ACE-S/C stations in all phases of operation. The function of this program is to locate the proper file on the test file tape and load the uplink program, uplink parameters, and the downlink program. It also loads the scope annotations, downlink parameters, calibration address tables, and the calibration data.

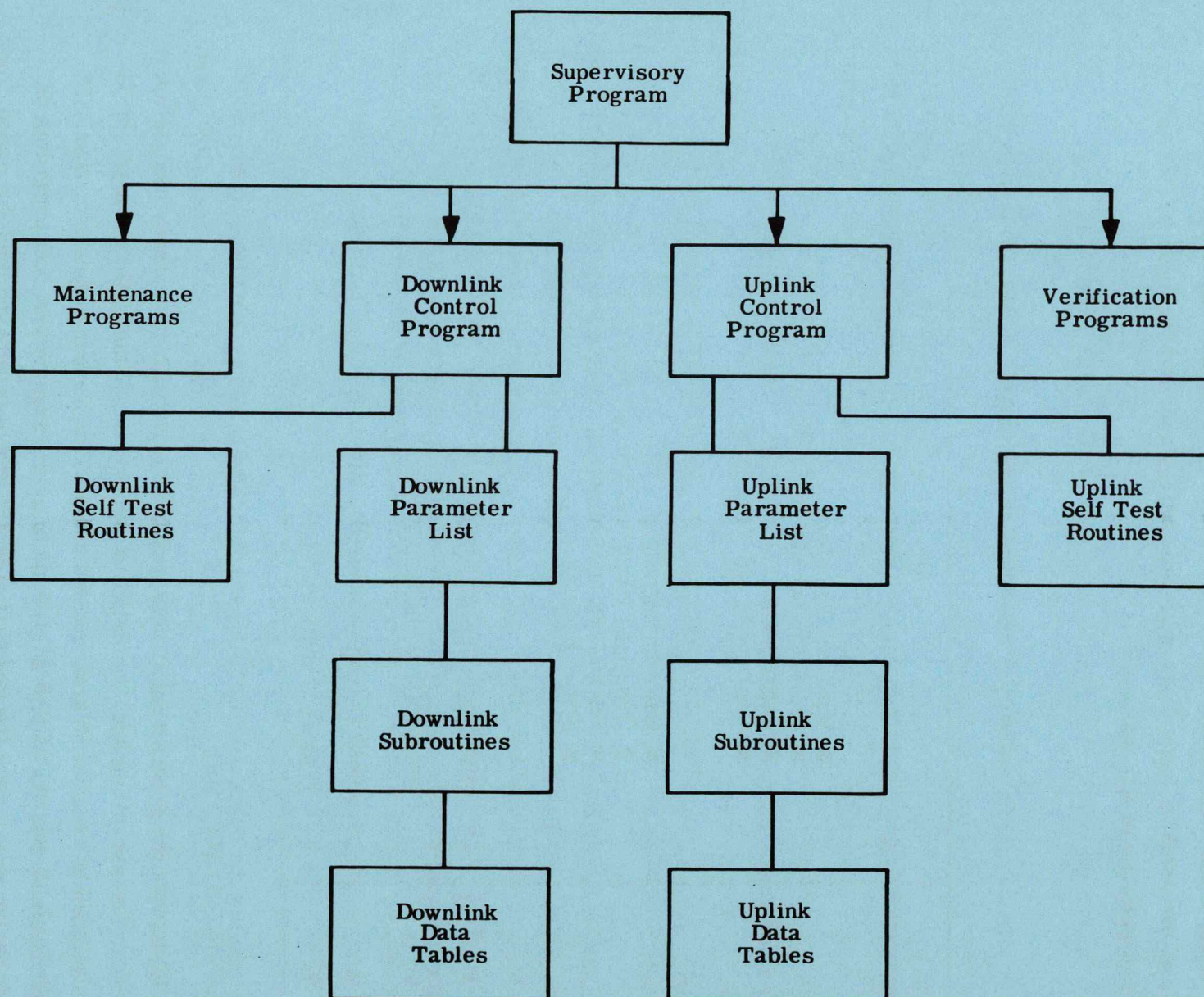


Figure 13. Programing Structure

When changes are called for in the course of operations, this program permits three types to be initiated by a single specified C-START. These three changes are as follows:

- a. Load an entire test.
- b. Load a new annotation into the entire SGS memory and load its associated downlink parameters.
- c. Change the engineering limits in a specified downlink parameter.

The SEP is loaded in the memory of the downlink computer. A test file tape is loaded with the SEP and the loading instructions being the first file on the magnetic tape. After the tape has begun loading the program, the uplink computer is started by the operator. The system is now fully automatic for the loading process and is under the control of SEP operating in the downlink computer. Unless errors (requiring operator intervention) occur, all further commands to the program are via SEP C-START. Further information concerning the operation of the SEP can be obtained from the ACE-S/C computer program document, Volume 5.

PROGRAM PREPARATION AND VERIFICATION (Figures 14 and 15)

The Programing Standards Manual, Part 4, Bulletin 2, defines the procedure to be followed in the preparation and verification of spacecraft test programs. This procedure is used to verify that each ACE-S/C test program and/or spacecraft test tape meets specified requirements and can be certified for use as an operational program to be incorporated into the official ACE-S/C computer program library. The spacecraft contractor submits to the General Electric Company a block specification which details the various parameters to be processed, sampling rates, parameter limits, type of processing and the page format for the alphanumeric display system.

After receiving the block specification, the information is analyzed for proper understanding and then the initial write-up and flow charts are developed. These flow charts are reviewed by the spacecraft contractor and NASA to insure the proper translation of the requirements. Upon the completion of the review, detailed flow charts are developed and then all real-time test programs are written in mnemonic language. The General Assembly System (GASS) will be used for the assembly of test programs on the CDC 160G computer. After the test program has been flow charted and coded, the debugging procedure is accomplished.

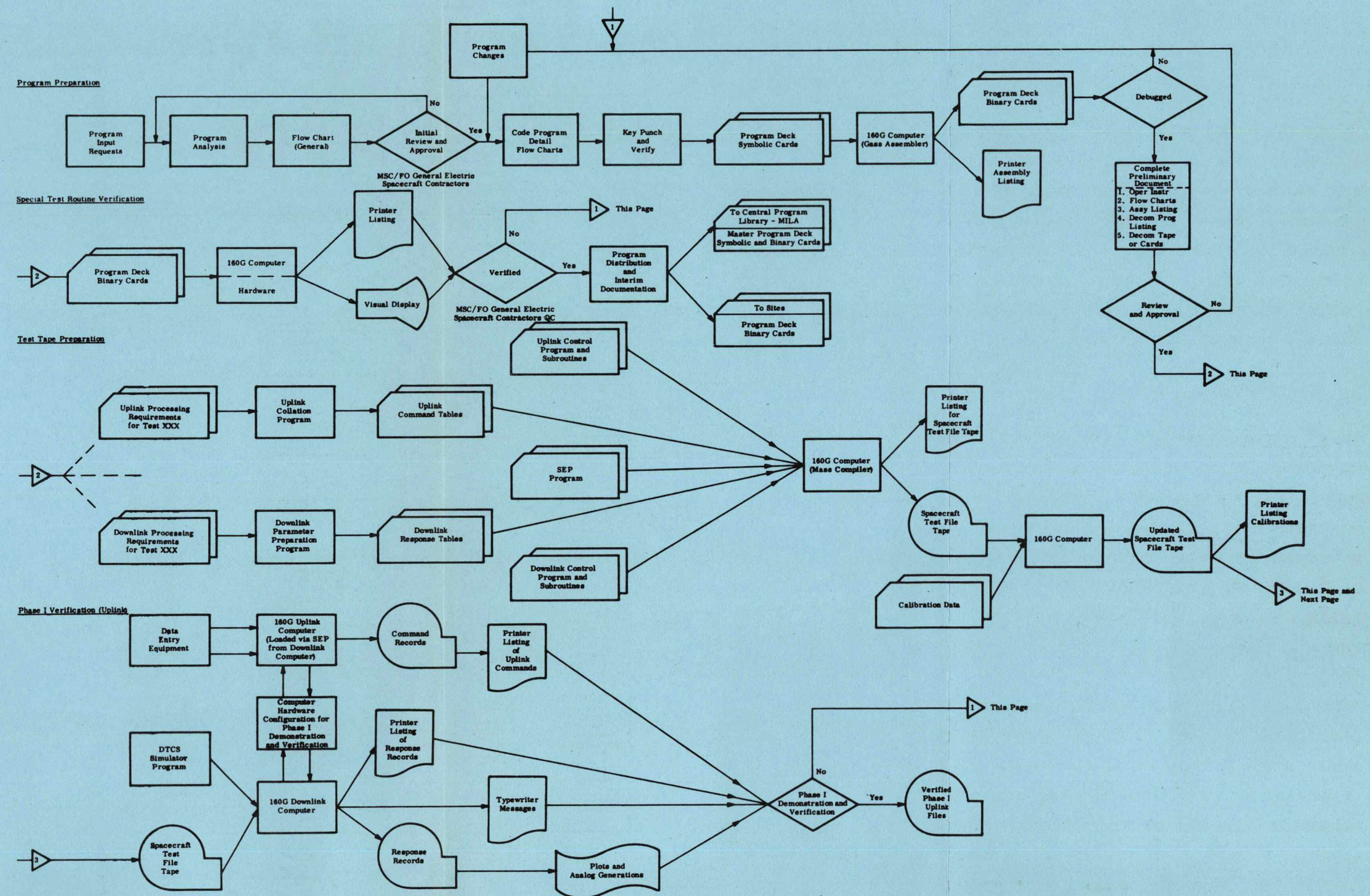


Figure 14. Spacecraft Test Programs - Program Preparation and Verification

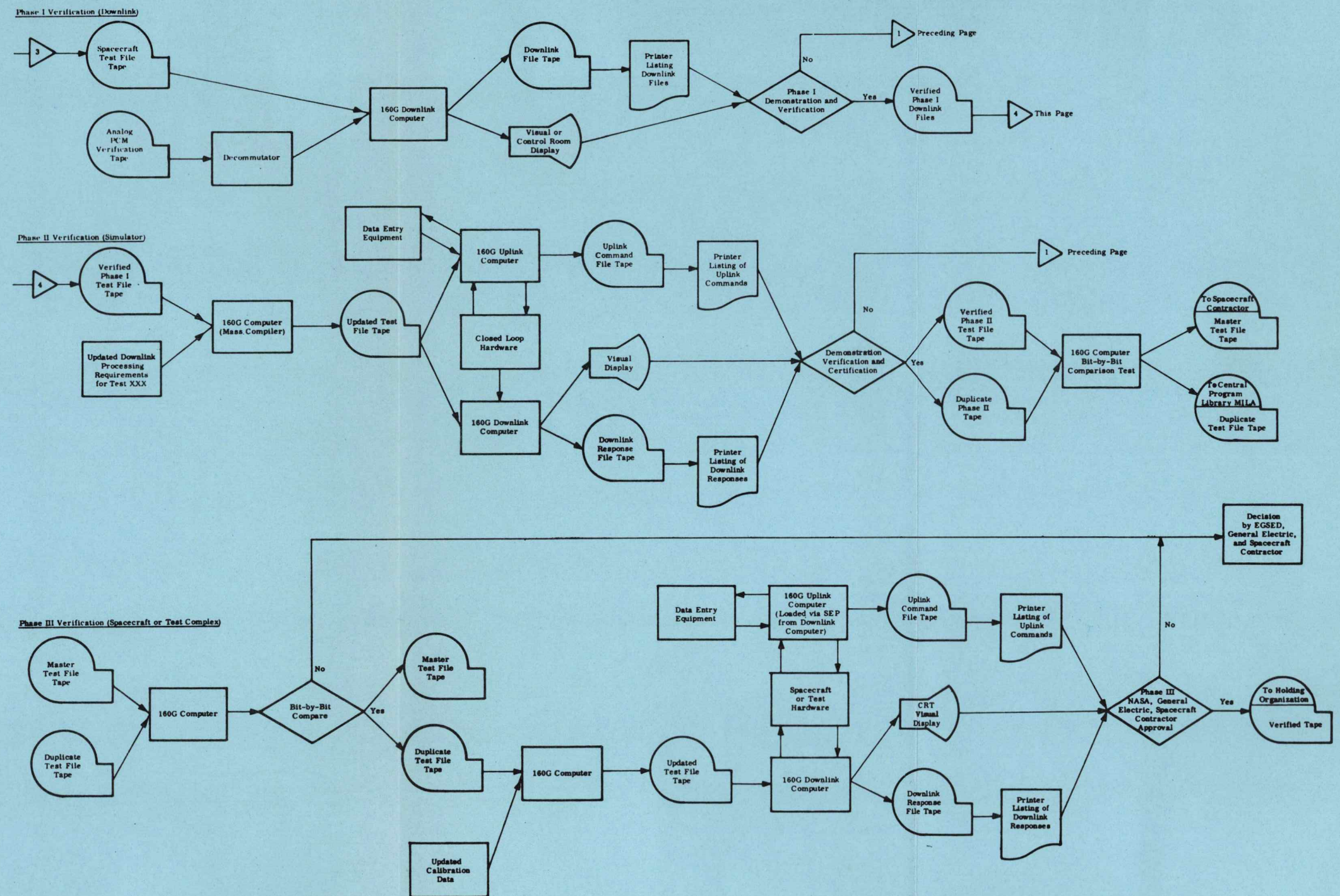


Figure 14. Spacecraft Test Programs - Program Preparation and Verification (Cont.)

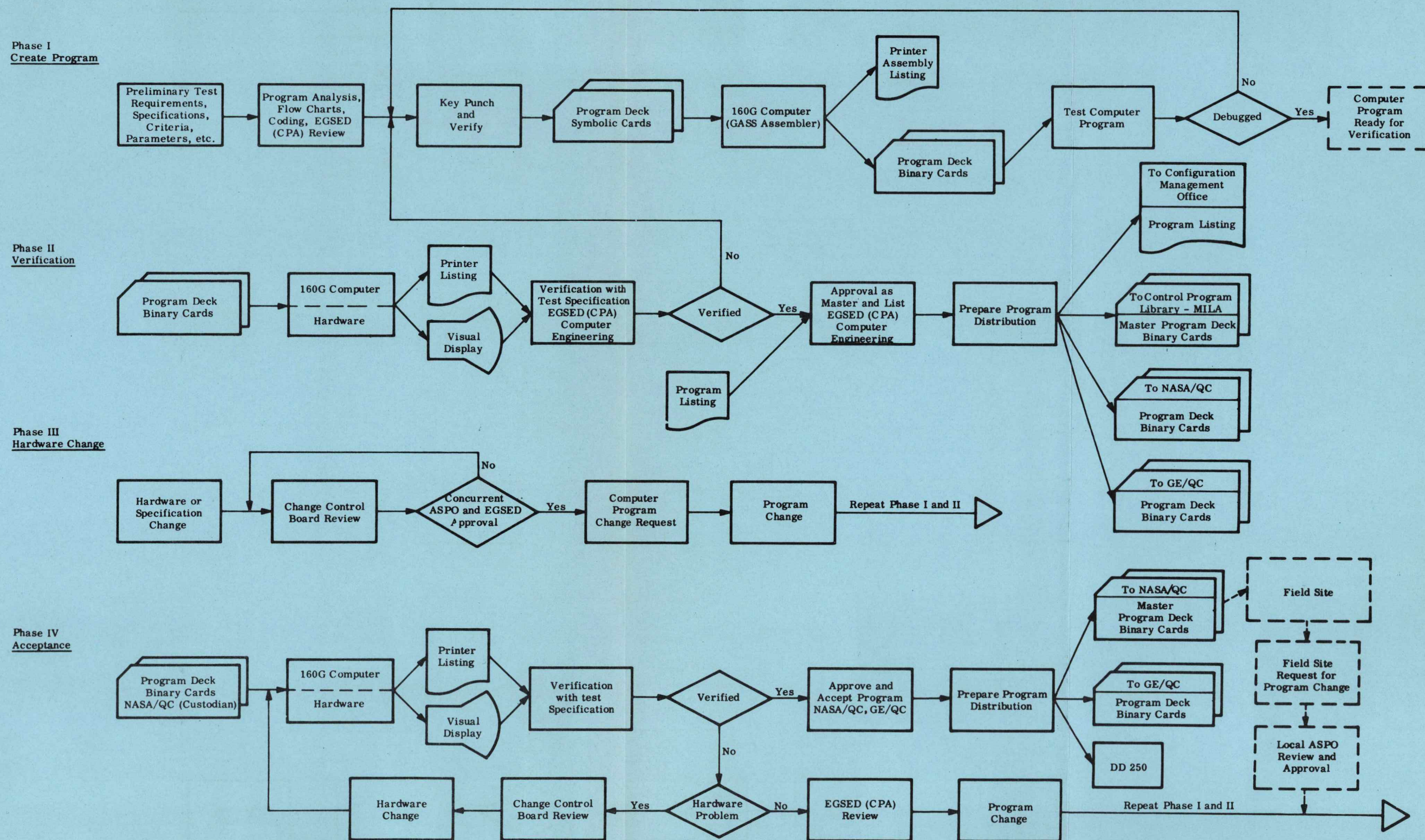


Figure 15. Acceptance Test Programs - Program Preparation, and Verification

After completion of the program preparation sequence, the verification phase is initiated. Figure 16 illustrates the general equipment configuration utilized during the verification phase of test program checkout. The uplink configuration will be as follows - Hardware configuration will remain standard from the START modules through the uplink computer and through the input to the assigned uplink Data Transmission and Verification Converter (DTVC). The output of the uplink DTVC will be disconnected from the Digital Test Command System (DTCS) and patched to the DTVC of the downlink computer.

The software configuration will be as follows:

- a. Load test program to be verified from the spacecraft test tape into the uplink computer.
- b. Load DTCS simulator program into the downlink computer.
- c. Mount usable tapes on other tape units of both computers.

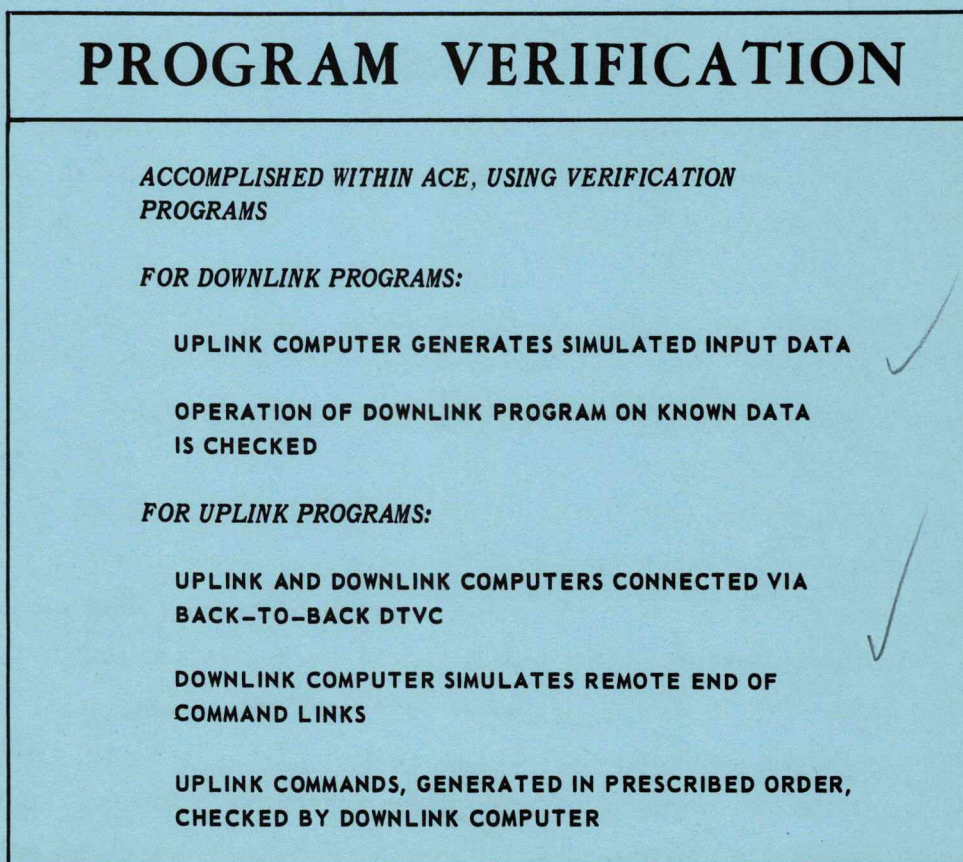


Figure 16. Program Verification

UPLINK PROGRAM ANALYSIS (Figure 17 - Main Uplink Control Program)

The command computer time is occupied by two separate types of operations that may be described as nonpriority and priority operations. The nonpriority operation is controlled by the executive program that maintains a logic flow of low-priority (nontime critical) processing tasks. These tasks serve the dual purpose of performing important maintenance and housekeeping functions while efficiently using the computer's spare time between priority operations. The priority operation may be best described as the handling of test operation request interrupts from the CUE. The priority operation is controlled by interrupt handling routines. The various interrupts are the key to the priority operation. The priority operation consists of processing these interrupts to determine what action is necessary to satisfy a test operation request.

The nonpriority computer operation consists of two main operations that are best termed initialization and housekeeping. During the initialization operation, normal command equipment operation is prevented while the computer receives parameters that are arranged into tables. The tables are then assembled, and the computer selects the operating status for external equipment. After this is accomplished, normal operation of the command equipment group is enabled, and the computer systematically performs low-priority information transfers and real-time maintenance checks. The housekeeping operation may be temporarily halted at any time by interrupts from the DTVC or CUE. When this occurs, the computer breaks into a priority operation.

The initialization operation begins when punched cards containing table parameters are read into the computer. The computer assembles these parameters into three unique tables (according to program control) and stores them in allocated memory locations. These tables are termed clock table, R-START table, and C-START table. The clock table is associated with timed interrupts to the computer from the tape recorder/computer time decoder and search control. The clock table is used to interpret these interrupts, call up the subroutine requiring attention, and set the clock for the next controlled interrupt. The R-START table is associated with Interrupt 30 from the CUE. This table is used to associate each R-START module with a group, baseplate, and module of the receiver-decoder. The R-START table is also used to control SEAL requests or reference an appropriate preroutine address. Additional information with respect to function switch status of the current R-START module is added to the data determined by the R-START table. The C-START table performs the same function as the R-START table insofar as it associates each C-START module with a group, baseplate, and module of the receiver-decoder. The C-START

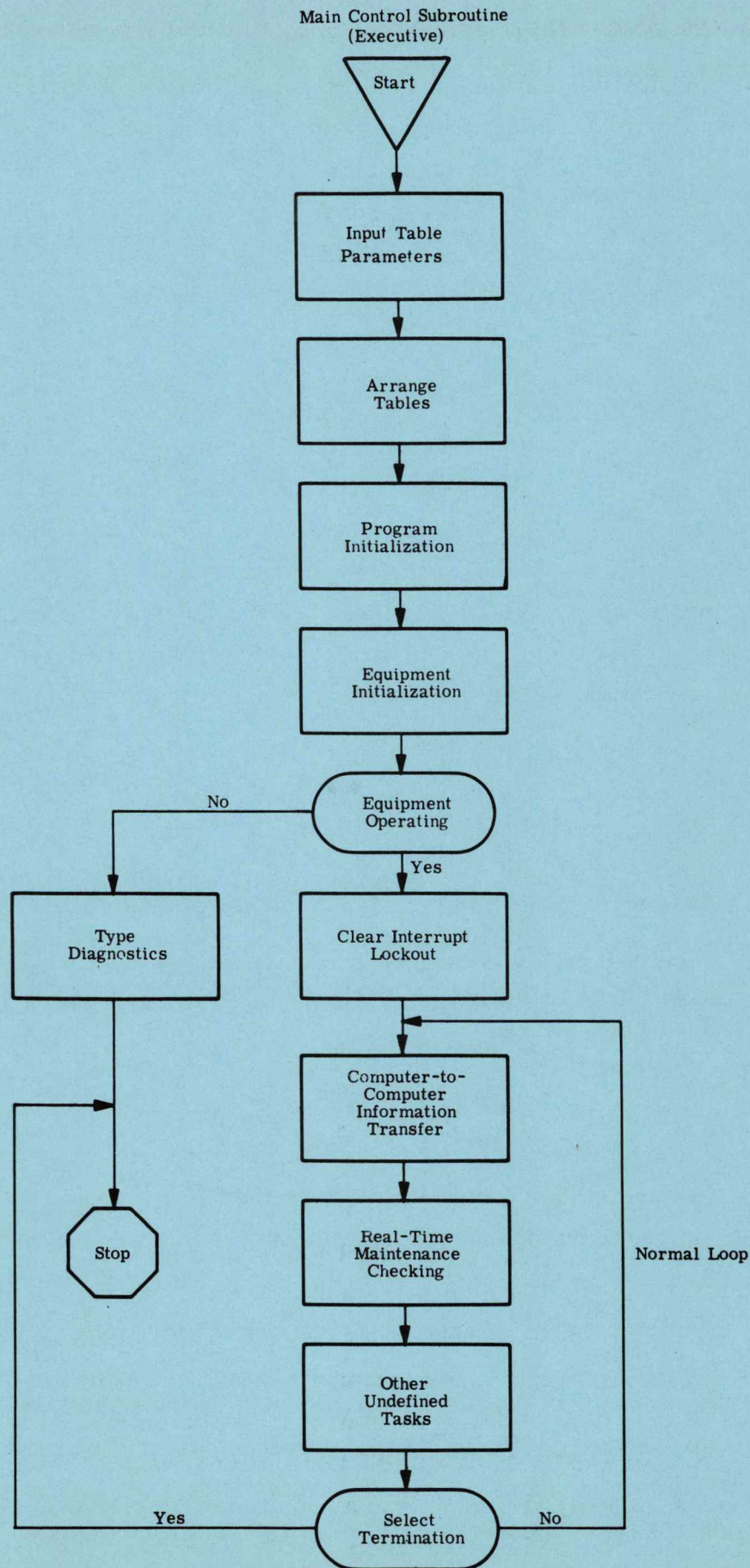


Figure 17. Uplink Control Program

table also controls SEAL request or references appropriate preroutine memory address for special analog functions. After the tables have been assembled, the computer initializes all equipment used during normal operation. This is accomplished by verifying that all peripheral equipment is ready and selecting the proper operating mode for each. If this cannot be accomplished, the computer types out an appropriate message and halts. After equipment initialization is completed, the computer sets all programmed flags to their normal state, releases the lockout interrupt, and begins the housekeeping operation.

The housekeeping operation is actually a wait operation that efficiently uses the computer time to perform nonpriority tasks while the computer is waiting for priority operation requests. During this operation, the computer may perform a number of various operations that are designated by the program. Examples of these operations are the transfer of information between computers through shared memory or the performance of routine maintenance checks. The housekeeping operation can be interrupted at any time to perform priority operations. After the priority operation is completed, the housekeeping operation begins again at the point where the interruption occurred.

A priority operation is the functioning of the computer as a translator interface between the CUE and the DTCS. This operation begins as the result of an interrupt received from the CUE. After an interrupt occurs, the computer receives an input from the START module that generated the interrupt. The computer reads the START module input and generates one or more commands to be sent to the DTVC. The DTVC transmits the command from the computer to the DTCS. The DTCS performs a validity check on the command and returns a Check Status Reply (CSR) word to the DTVC. The DTVC relays the check status reply word to the computer, which uses it to determine the success or failure of the transmission. If the transmission was successful, the START module that originated the command is notified by a confirm or a SEAL from the computer. The confirm allows the START to enter new commands to the computer. The SEAL prevents further action from being initiated by that particular START until the preset command has been executed. If three transmissions of the command are unsuccessful, the computer will notify the CUE and diagnose the malfunction.

The computer is switched from housekeeping operation by interrupt signals from the external command equipment. During normal operation, these interrupts consist of Interrupt 30 and Interrupt 40 signals. The Interrupt 30 signal is applied to the computer by either an R-START module or a DTVC. The Interrupt 40 signal is applied to

the computer by a C-START, K-START, DTVC, or one of the I/O synchronizers. Either interrupt will cause the I (interrupt) flag to be set and the computer to respond in the same manner.

When an Interrupt 30 is sent to the computer, the first action performed is to save the accumulator contents so it may be used when housekeeping operations are resumed by the computer. The I flag is cleared so that the housekeeping operation may resume after the interrupt has been answered. Finally, the computer checks a series of routing flags to determine if the DTVC generated the interrupt. If none of the routing flags is set, the computer checks the status of the CUE. If the CUE did not generate the interrupt, the computer assumes the interrupt was generated by the DTVC and starts a priority operation by initiating a DTVC routine.

When an Interrupt 40 is sent to the computer, it reacts in the same way as it does when the Interrupt 30 is received. The only difference is a few additional steps are performed to determine if the interrupt came from the tape recorder/computer time decoder and search control. After the computer has determined which external unit has generated an interrupt, it will start a priority operation, which may be one of several routines. The routine will be determined by the equipment that generated the interrupt.

The R-START routine causes the computer to accept a coded R-START command word from the CUE, interpret the command word, and transmit commands to the DTCS via a DTVC.

If a command generated by the R-START module requires relay action only, the computer checks the DTVC for availability. If the DTVC is available for transmission, the command words are set into the output buffer and control is transferred to the DTVC output routine. If the DTVC is not available, the computer begins nonpriority operation until the DTVC is available. In either case, the appropriate routing flags are set to the proper state.

If a command generated by the R-START module is for a special function, the required special subroutine is recalled from memory and recorded on magnetic tape. The computer then returns the CUE to interrupt mode and clears the interrupt lockout logic. It then replaces the housekeeping operation with the special subroutine. The computer then runs the special subroutine and answers interrupts just as though it was performing the housekeeping operation. When the special subroutine has been completed, the

computer returns control to the R-START routine, which returns the computer to normal housekeeping operations.

The C-START routine causes the computer to accept four coded command words from the CUE, interpret the command words, and transmit commands to the DTCS via the DTVC. The C-START command words will contain up to ten decimal digits of parametric information to add to the uplink commands. The parametric information is added to one of three general subroutines that are called up by the first C-START input word. The subroutine can generate commands to apply stimuli and control relay closure sequence in the DTCS. This is accomplished through the sequence of computer operation described in the following paragraphs.

If the C-START input is for a normal function, the computer generates commands using the onboard addresses and other data contained in the input words. The computer then checks DTVC for availability. If the DTVC is not available for transmission, the computer returns to housekeeping operations until the DTVC is available. If the DTVC is ready to transmit, the command words are placed in the output buffer and computer control is transferred to the DTVC routine. In either case, appropriate routing flags are set the proper state.

If the C-START input is for a special function, the computer derives the test area equipment address and appropriate preroutine from the C-START table. The computer then loads the test area address into the A register and makes a return jump to the preroutine. After the preroutine has run, the A register contains the address of the routine that will perform the special function. This address is placed in the clock table. Then the initial interrupt time is calculated, and also placed in the clock table opposite the address. If this is the first entry in the clock table, the computer requests the first interrupt from the clock. Thereafter, this condition is handled by the clock servicing routine. The command is recorded on magnetic tape, and the CUE write mode is selected. This releases the scanner and returns the CUE to interrupt mode. After this, the computer returns to normal housekeeping operations.

The computer switches to the K-START routine from a C-START routine. This routine causes the command computer to interpret K-START inputs and generate command signals to be sent to the spacecraft Airborne Guidance Computer (AGC). The command computer receives four 12-bit words from the K-START module. The first word contains the unique address of the K-START module and a flag bit that indicates whether

the input originated at the K-START keyboard or at the paper tape reader. Words three and four are dummy words to make the K-START input format compatible with the C-START input.

The purpose of the DTVC routine is to transmit commands to the DTCS via a DTVC. This routine causes the computer to send Load Buffer Memory (LBM) words and Execute Buffer Memory (EBM) words to the DTVC for transmission. CSR words are received from the DTCS by the DTVC. The CSR words cause the DTVC to send an Interrupt 30 to the computer if the transmission was successful, and an Interrupt 40 if the transmission was unsuccessful. The DTVC will not transmit a command until the CSR of a previous command has been received.

The computer determines which DTVC is to be used to transmit from the START input, then stores the command in a rotating table. This table is large enough to control the largest backlog of command anticipated. The computer also stores the first word from the CUE and the previous function switch settings in the table. These are required in the event the transmission fails. In this case, the CUE word and the fail CSR word will be sent to the CUE maintenance panel, and the previous function switch settings will be sent to the requesting START module. After the command has been stored, the computer checks the DTVC status. If the DTVC is not busy, the computer moves data from the rotating table to the output block for transmission to the DTCS. After transmission, the computer converts the command from a load DTCS buffer memory to an execute DTCS buffer memory. When the I/O module buffer interrupt indicates the LBM has been transmitted, and when the CSR has been received, the computer will allow the EBM to be transmitted. When the I/O module indicates the EBM has been transmitted, the computer will select the DTVC to recognize the CSR word and generate an Interrupt 30 or 40 to indicate success or failure of the transmission. The computer performs interrupt operations between the steps explained previously to make efficient use of time required for the actual transmission. Success or failure of the transmission is determined by the DTVC. After reception of the CSR, the DTVC will generate an Interrupt 30 or 40 depending on the success or failure of the transmission. If the transmission has been a failure, an Interrupt 40 will be generated and the CSR will be inputted to the computer. The computer will check to determine if this is the third failure of this command. If it is, the computer will call up a maintenance routine. If not, transmission will be tried again. If an Interrupt 30 is generated by the DTVC indicating success of transmission, the computer will release the CUE to scan. The computer will also send a function code to the START module that originated

the command to light the upper half of the function switch pushbuttons. The computer then checks the rotating table for a backlog of commands. If a backlog exists, the DTVC routine will be called up. If a backlog does not exist, the DTVC will be set to "not busy."

The purpose of the clock servicing routine is to maintain a check on the special function routines. This is accomplished with clock interrupts that assure transfer of these routines at the appropriate time.

When the computer transfers control to the clock servicing routine, time is inputted from the real-time decoder. The computer applies this time to the clock table to find the routine that requires attention. If this function has output its last iteration, the computer clears this routine from the clock table and returns to normal housekeeping operation. If the routine is still available to be called, the computer updates the clock table and sets the clock for the next interrupt. Then it makes a return jump to the special subroutine that requires attention. After running the special subroutine, the computer checks to determine if the last iteration has been outputted for this function. If this was the last iteration, the routine is made unavailable for the next "call." The computer then checks the DTVC for availability. If the DTVC is not available for transmission, the computer returns to normal housekeeping operations. If the DTVC is available, the contents of the special routine storage locations are transferred into the output buffer, and control is transferred to the DTVC output routine. In either case, the computer sets the appropriate routine flags to their proper positions.

The purpose of the exit routine is to return the computer operation to the point in the housekeeping routine where the interrupt occurred.

After the last required transmission is completed, the computer clears the E (error flag). If an interrupt has occurred during transmission of a command, the computer transfers control to the appropriate routine. (The clock servicing routine has first priority in this return.) If there are no routines that require processing, the I (interrupt) flag is checked. Then the computer sets the accumulator with the housekeeping data that was present when the interrupt occurred. Finally, the computer clears the interrupt lockout and makes a return jump to the housekeeping routine.

DATA TRANSMISSION AND VERIFICATION CONVERTER

OBJECTIVES

To familiarize the student with:

- a. Modes of operation.
- b. Theory of operation (block diagram).
- c. DTVC/computer interface.

INTRODUCTION

The Data Transmission and Verification Converter (DTVC) is an interconnecting communications device that provides long-distance serial data transfer between the computer and various remote units. Data flow between the computer and the remote units is maintained by a sequence of control signals. There are four DTVC units utilized in the ACE-S/C system, three in the uplink or command loop and one in the downlink or display loop. The DTVC's in the command loop relay the various commands from the computer to the stimuli generators located in the test bays. The commands are verified for correctness, and verification signals are then routed back from the test bay area to the command computer via the DTVC's. The selected DTVC accepts 12-bit parallel words from the computer, converts to serial format, and transmits as a 24-bit serial word over the hardlines. The DTVC receives a 24-bit serially coded word from the remote unit, assembles, and stores the first 12 bits, and then the DTVC performs a bit-by-bit check of the second 12 bits with the first 12 bits. The DTVC then presents a 12-bit, parallel-coded word to the computer whether correct or in error. When an error is detected, interrupt and status signals will be made available to the computer.

EXPLANATION

FUNCTIONAL DESCRIPTION

The DTVC operates under program control of a digital computer and communicates in parallel mode with the computer over a standard input/output communications channel. The DTVC communicates with other DTVC's or similar devices in serial mode over a long-distance communications link. Serial data is transmitted with 100-percent redundancy for verification by the receiving unit. The DTVC has three modes of operation,

select transmit, select receive, and select interrupt. The unit remains in the monitor or receive mode until the computer is ready for a transmission. The DTVC operates under program control of a digital computer. The computer can select the DTVC to operate in any one of the following three modes:

- a. Select Transmit - Prepares the equipment to receive 12-bit parallel words from the computer and transmit 24 serial bits for each word received on one of the available channels. The equipment remains in this mode until an interblock null is detected. After detection of the interblock null, the DTVC enters the monitor mode.
- b. Select Receive - Prepares equipment to receive 24-bit words in serial mode on one channel, assemble and verify 12-bit words, and present the words in parallel to the computer. The monitor mode differs from the select receive in that the receive data will not be transferred to the computer until the select receive is enabled.
- c. Select Interrupt - Prepares the equipment to monitor data on one channel and compares the upper six bits of the first word with the positions of a predetermined selection of six switches. If the two match and no error is detected, an interrupt signal is transferred to the computer.

In the transmit mode, data is received as a 12-bit parallel word and is transmitted as a 24-bit redundant serial word. Each word is placed in a register and the contents of consecutive stages of that register are transmitted over a preselected serial communications channel. When all 12 bits of the word have been transmitted, the contents of the register will be retransmitted to provide 100-percent redundancy with no delay between transmissions.

The DTVC in the receive mode receives a serial 24-bit word. The first 12 bits of each 24-bit word are loaded into a register. Each of the second 12 bits, as they are received, will be compared with the corresponding bit of the assembled word to verify the accuracy of the transmission. Upon detection of an error, an interrupt signal will be made available to the computer. All 12-bit words will be presented to the computer whether correct or in error. If insufficient bits are received to form a 12-bit word, the word shall be completed by the addition of 0's and presented to the computer.

TRANSMIT CYCLE

Figure 1 shows the DTVC operating in conjunction with the computer, acting as a communication link between the computer and the DTCS. In order for the computer

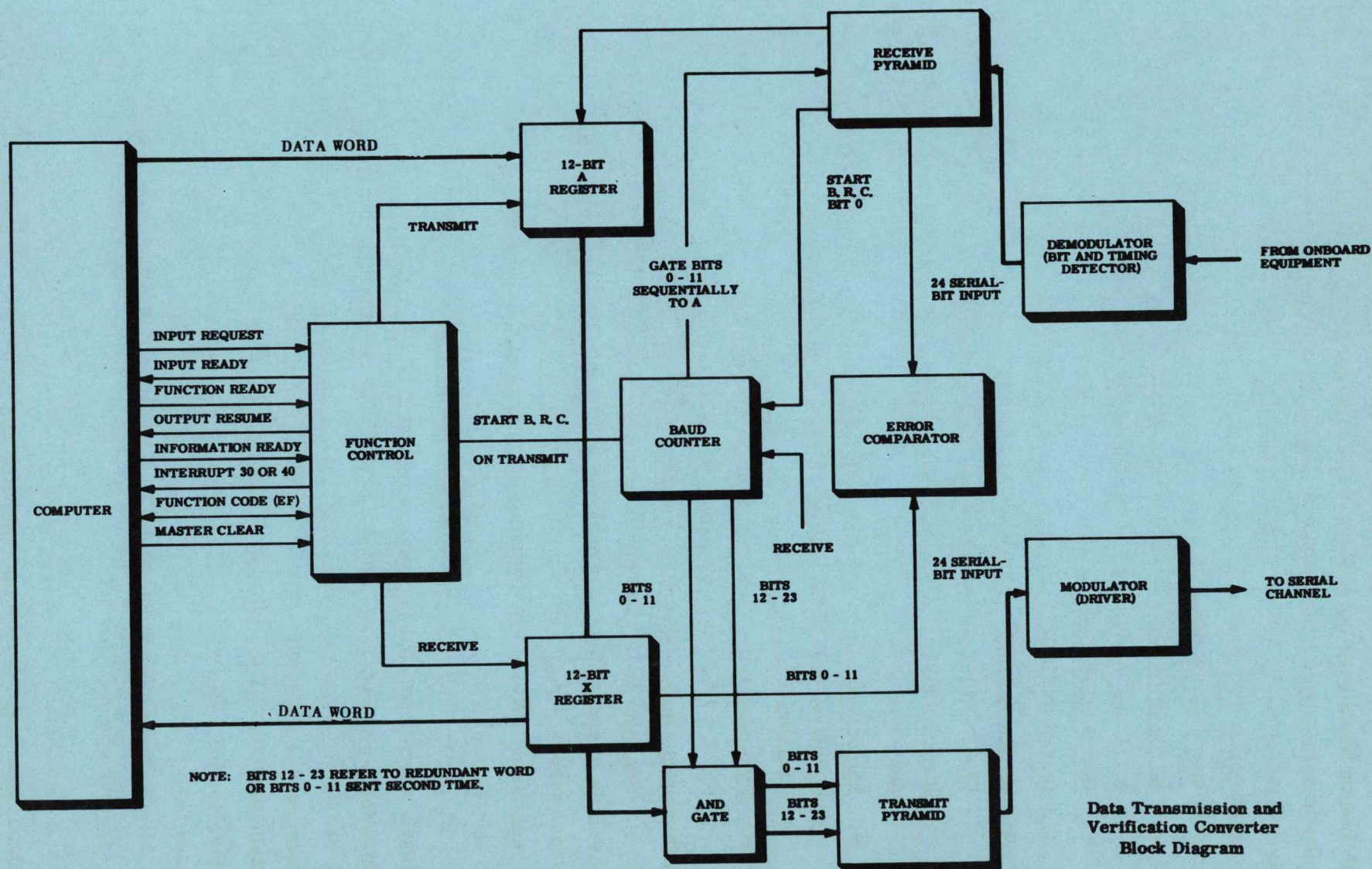


Figure 1. DTVC Functional Block Diagram

to provide data flow to the DTVC, preliminary conditions (channel selection, etc.), must be established between the two items of equipment and the DTVC must be placed in the transmit mode. This condition is attained through the use of control signals, which are essentially the raising or lowering of line voltages. Prior to entering a presentation on data flow and time-sequenced events, it is necessary that the following control signals be established:

- a. Function Ready - This signal is generated by the computer indicating that an external function code is available for translation.
- b. Information Ready - This signal is generated by the computer and is transferred to the DTVC indicating that a data word is available for transmission.
- c. Output Resume - This signal is generated by the DTVC and is a response to receiving the function ready or information ready signals and indicating to the computer that the word has been accepted and the DTVC is ready for another word.
- d. Input Ready - This signal is generated by the DTVC and is transferred to the computer indicating that the DTVC has a Check Status Reply (CSR) for the computer.
- e. Input Request - This signal is generated by the computer and is transferred to the DTVC specifying that the computer is ready for an input word.
- f. Interrupt - This signal is generated by the DTVC and is transferred to the computer indicating the status of the transmission. It causes the computer to interrupt the main program and to take action on the incoming word.
- g. Master Clear - This signal is generated by the computer and is transferred to the DTVC to establish initial operating conditions.

If the computer has information to be transmitted over the serial communications channel, the computer must select the proper DTVC and determine which one of several serial channels is to be utilized. To facilitate this, the computer generates a 12-bit external function code, the most significant 6 bits select the proper DTVC, and the least significant 6 bits select the proper channel within the DTVC and the operation required. The following sequential steps indicate how the computer and the DTVC communicate to effect the proper conditions for a data word transmission (see Figure 2):

- a. The computer transmits a 12-bit External Function (EF) code to the DTVC over the data lines.
- b. A function-ready signal is transmitted to enable the DTVC to recognize the input function code.

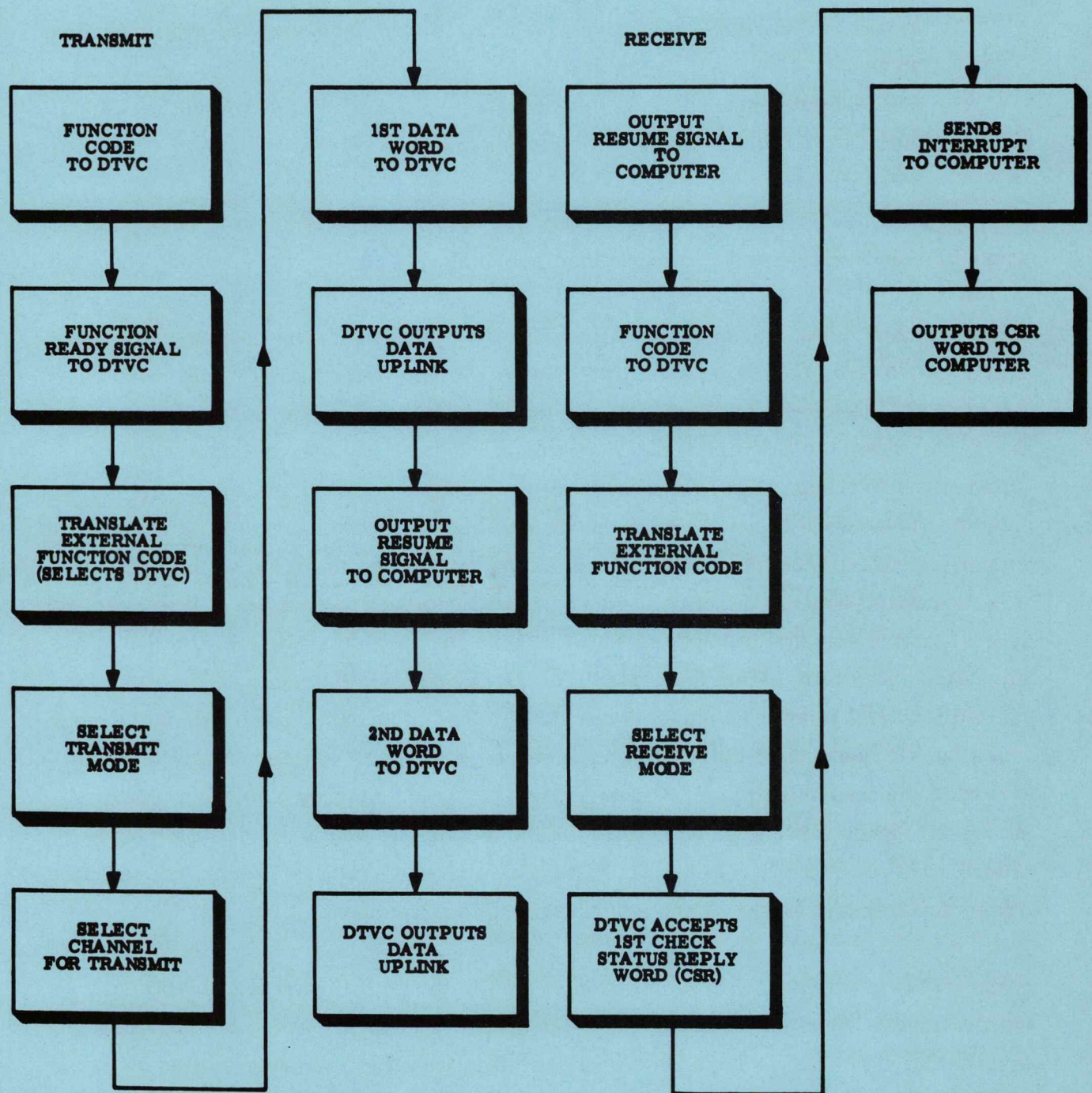
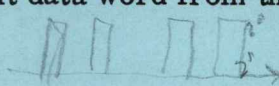


Figure 2. Data Transmission and Verification Converter Operational Flow Chart

- c. The translation of the EF code places the DTVC into the select-transmit mode and selects the serial data channel to be utilized.
- d. An output resume signal is then transmitted to the computer to indicate that the DTVC is ready to receive the data word. The output-resume signal removes the function-ready signal, which, in turn, removes the output-resume signal.
- e. The computer generates an information-ready signal indicating to the DTVC that a 12-bit data word is available for transmission.

The DTVC is now in the condition to accept the 12-bit data word from the computer for transmission over the serial data channel selected.



The computer, after transmission of the EF code, places a 12-bit parallel data word on the output lines (see Figure 1). DTVC control logic (information ready) enables 12 parallel gates in the transmit gates in the transmit loop to facilitate the data transfer to the Assembly (A) register. The contents of the A register are immediately gated to the Exchange (X) register in parallel format. Upon completion of this transfer, the 12-bit word is now ready to be transmitted. The transmit or timing enable signal is sent from control to the timing unit to gate clock pulses out to the counter. The counter, a chain of flip-flops, sequentially gates the contents out of the X register, e.g., the contents of register No. 1 at time "1," register No. 2 at time "2," etc. By sequentially gating the contents of the 12-bit register, the parallel word is shifted to serial form. To perform the 100-percent redundancy required, the counter gates out the contents of the X register a second time. The serialized data is transferred to the transmit pyramid. The function of the transmit pyramid is to convert the 24-bit digital input to a split-phase modulated signal containing the intelligence transferred out of the X register. The output split-phase data is transferred to a line driver for transmission over the serial communications channel.

If the DTVC is utilized for transmission of data to the DTCS, then four 12-bit data words must be transferred out of the computer for transmission. In the previous discussion, a 12-bit word has been transferred to the DTVC and transmitted as a 24-bit redundant word. As the last bit is being gated out of the X register, the A and X register are cleared. The DTVC at this time generates an output-resume signal to the computer. This signal indicates to the computer that the first 12-bit word has been serialized, that redundancy has been performed, that the word was transmitted to the DTCS, and that the DTVC is ready for another 12-bit word. The computer

generates an information-ready signal indicating to the DTVC that another data word is on the lines for transmission. For the second transmission the same steps will be repeated.

RECEIVE CYCLE

After the transmit cycle, the DTVC will, after an interword null, return to the monitor mode ready to receive data over the last channel selected; however, no data will be transferred to the computer until the select-receive circuit has been enabled. Prior to entering the receive cycle, the computer must transmit a 12-bit function code to the DTVC containing a select-receive instruction.

The split-phase data containing the information from the remote equipment is received by the bit and timing detector circuitry, which changes the incoming serial waveform to digital information and provides timing for word assembly and error detection. The output serial data is fed to the receive pyramid. Timing, a resultant of the first detected bit, is fed to the counter to start the gating cycle to transfer the serial data from the receive pyramid sequentially into stages number 1 to 12 of the A register. Each incoming bit causes the counter to change one step; therefore, bit No. 1 is gated into stage No. 1, bit No. 2 is gated into stage No. 2, etc., until all 12 stages have been set. This action converts the serial data to parallel data. The data is immediately gated into the X register as 12 parallel bits.

Bits number 12 to 24, that is, bits numbered 1 to 12 of the redundant portion of the 24-bit word, are gated into the error comparator to be compared with the 12 bits now contained in the X register. To expedite the data transfer, the contents of the X register are gated into the error comparator as the tenth bit of the redundant word is gated into the comparator. After comparison is made and no error is detected, the DTVC will generate an interrupt 30 indicating to the computer that the redundancy checked. If redundancy failed, the DTVC will generate an interrupt 40 indicating to the computer that an error was detected.

GOOD
DTVC
interrupt
30

BAD
DTVC
interrupt
40

As bit No. 12 is gated into the A register, the DTVC generates a control signal to the computer indicating that data is on line. If the computer is ready to receive data, an input-request signal will be generated by the computer to the DTVC. During the exchange of control signals between the computer and the DTVC, the transfer from the A to X register is effected. The contents of the X register will now be gated out to the computer by the receive enable from DTVC control.

A complete transmit and receive cycle has now been completed. Should the computer desire to transmit another word and/or words, an exchange of control signals will be initiated.

DIGITAL TEST COMMAND SYSTEM

OBJECTIVES

The objective of this study guide is to familiarize the student with:

- a. Modes of operation.
- b. Theory of operation (block diagram).
- c. Spacecraft/DTCS interface.
- d. Application of stimuli.

INTRODUCTION

The basic function of the digital test command system (DTCS) is to receive serial-digital command data from a DTVC, decode the command data, convert the command data into stimuli and command signals, and route the commands and stimuli to the various systems under test. An additional function is to perform internal checks in decoding and selection to prevent double interrogation of equipment and to inform the ACE-S/C uplink computer of the status of the command transmission. The functional operation of each DTCS, external, carry-on, and ground service is the same; therefore, no specific one will be discussed.

A single DTCS consists of a receiver-decoder, baseplates, relay modules, analog modules, and a guidance and navigation buffer unit. The function of the receiver-decoder is to receive, format, time, and check the redundant serial command from the ACE-S/C uplink data transmission equipment. The baseplates house the relay and/or analog modules, and the baseplate logic performs decoding for baseplate selection. The relay modules provide relay closure outputs to the spacecraft or service equipment. The analog module is basically a digital-to-analog converter that produces an analog stimulus in accordance with the uplink test command.

DTCS CONFIGURATION

A single DTCS in its maximum configuration will contain one receiver-decoder, thirty-two baseplates, and one guidance and navigation buffer unit. The thirty-two baseplates are divided into four groups of eight baseplates each. Each baseplate can contain four plug-in type modules. The plug-in modules provide system capability to be expanded or contracted to meet particular checkout requirements. Figure 1 shows the various

DTCS SIGNAL FLOW

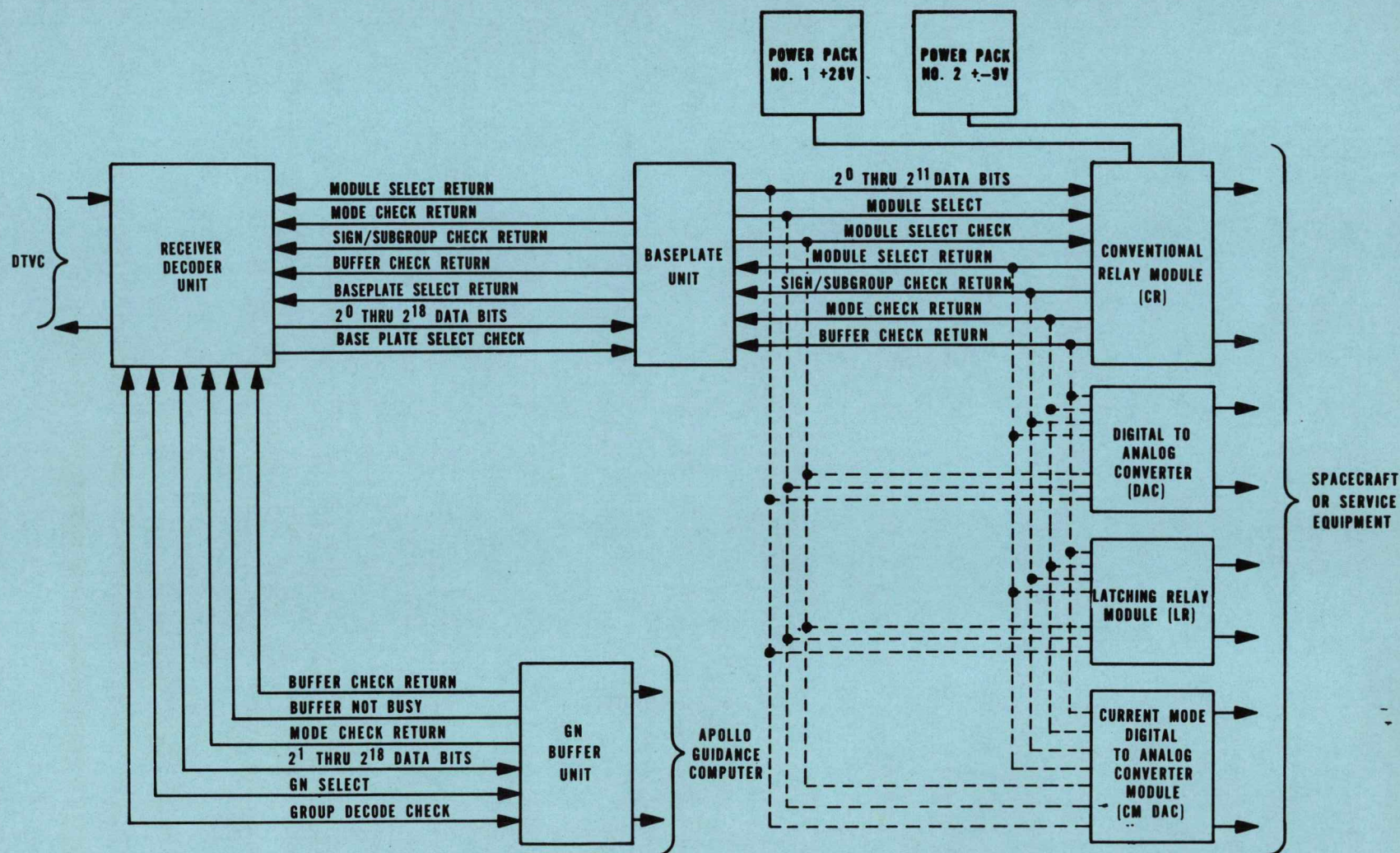


Figure 1. DTCS Signal Flow

modules that operate with the baseplate units. Conventional relay and latching relay modules provide programmable relay closures. Voltage mode digital-to-analog converter (VMDAC) modules provide programmable voltages. Current mode digital-to-analog converter (CMDAC) modules provide programmable currents. Each analog module contains one digital-to-analog converter, while each relay module contains sixteen relays.

The equipment within the DTCS is organized into various types of equipment groups. The various types include: receiver groups, baseplate groups, and command stimuli groups. The equipment groups designated here denote groupings of equipment associated with various types of enclosure units. (See Figure 2.)

The receiver group incorporates a receiver-decoder baseplate enclosure unit which houses a receiver-decoder, baseplate, and four modules. Each interconnected DTCS equipment configuration requires only one receiver group.

The baseplate groups incorporate a dual baseplate enclosure which houses two baseplate units and eight plug-in modules. The baseplate units in all enclosure units are connected in parallel to the receiver-decoder. The baseplate groups (either I, II, III, or IV) can accommodate a maximum of eight baseplates.

The command stimuli group consists of a baseplate unit and four standard modules, two of which must always be CR modules.

The command stimuli group has special stimuli equipment modules which include a 28-volt power supply module (power pack No. 1) a 9-volt power supply module (power pack No. 2), and a resistor bank module.

The principal types of stimuli outputs are:

- a. Selectable precision reference resistances.
- b. +28 vdc.
- c. ± 9 vdc.
- d. Precision currents.

DTCS FUNCTIONAL DESCRIPTION

A DTVC interconnects with each DTCS receiver-decoder to transmit serial commands to the test bay. Each command sent to the receiver-decoder will contain 48 bits and

POSSIBLE DTCS EQUIPMENT CONFIGURATION

4

410-0(108)

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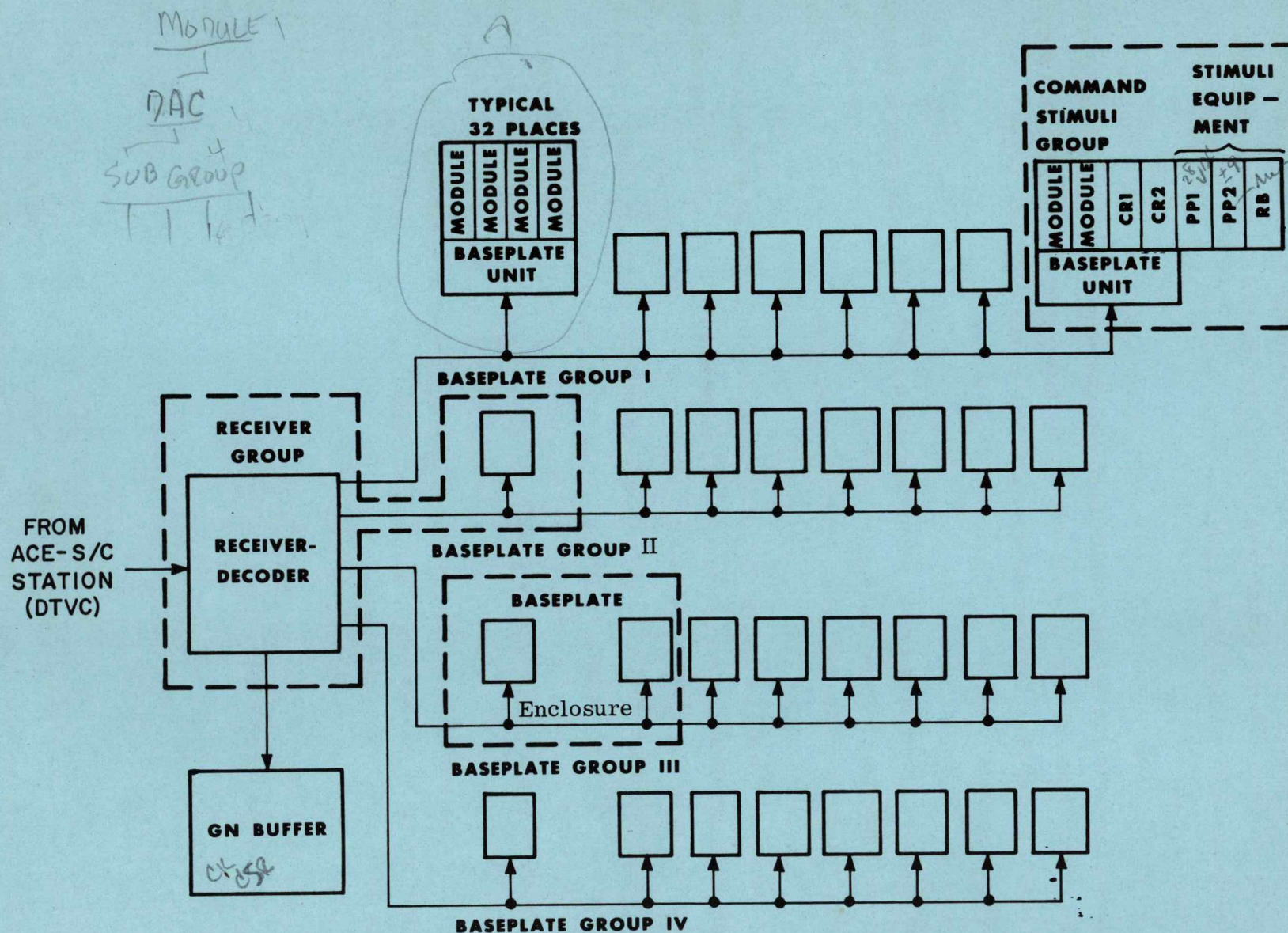


Figure 2. Possible DTCS Equipment Configuration

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will consist of two words of 24 bits each. The first 12 bits of each word are repeated in the second half of that word to provide 100-percent redundancy in the message structure. Each 48-bit message therefore contains 24 bits of information (see Figure 3). The two 24-bit words are transmitted uplink a minimum of 4 microseconds apart and a maximum of 25 microseconds apart.

Upon receipt of the first word, the receiver-decoder gates 12 of the 24 bits into a register and checks for redundancy with the remaining 12 bits. The second word, transmitted approximately four microseconds later, is processed by the receiver-decoder in a similar manner. The command word is now in a 24-bit parallel format.

There are three different formats for the 24-bit command word. The type format depends upon the unit or module selected to supply an output to the spacecraft or ground service equipment. The data formats are:

- a. RELAY DATA FORMAT - Used by the latching or conventional relay module. Generally this command is initiated by an R-START.
- b. ANALOG DATA FORMAT - Used by the DAC module. This command is used for generating constant or varying analog signals. A C-START is generally used to initiate this command.
- c. GUIDANCE AND NAVIGATION BUFFER DATA FORMAT - Used by the GN buffer unit. This command is initiated only by a K-START module.

Figure 4 shows the formats and functional assignments of each of the 24 bits to be decoded. Figure 5 shows where the bits are decoded for equipment or mode selection and indicates the various codes for particular functions. The following is an explanation of the use of the data bits in the various configurations.

CONFIGURATION FOR A RELAY COMMAND

Reserved Bit - Bit 23 is reserved and will always be a logical "1". ✓

Baseplate Group Select Bits - Bits 19 through 22 are used to determine the legal baseplate group address. ✓

✓ Baseplate Select Bits - Bits 15 through 18 are used by the baseplate translation logic to select the appropriate baseplate.

Module Select Bits - Bits 12 through 14 are used to select the appropriate module.

Mode Select Bits - Bits 10 and 11 are used to select the mode of operation. The modes of operation for the relay module are the load buffer memory mode (LBM) and the execute buffer memory mode (EBM). Normally, two 48-bit words are transmitted from

TYPICAL 48 BIT TRANSMITTED WORD

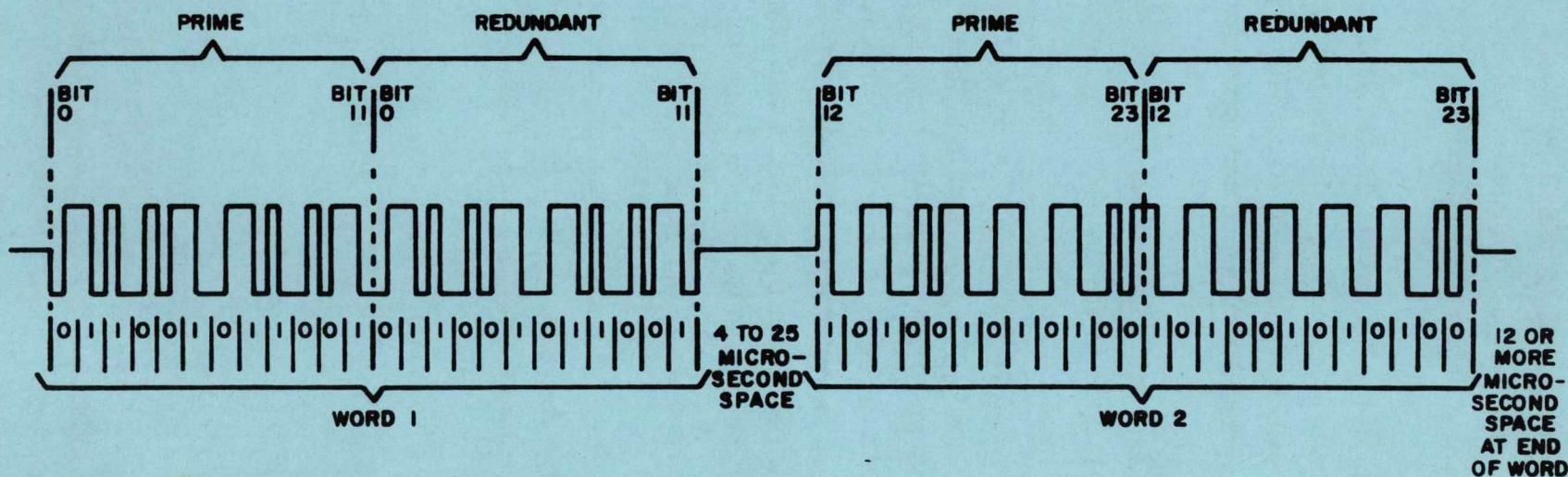


Figure 3. Typical 48 Bit Transmitted Word

COMMAND MESSAGE FORMATS

G&N			RELAY			DAC		
2 ⁰	NOT USED	TRANSLATED IN G&N COMPUTER BUFFER UNIT	2 ⁰	NOT USED	TRANSLATED IN RELAY MODULE	2 ⁰	LBM/EBM/ DATA	TRANSLATED IN ANALOG MODULE
2 ¹	LBM / EBM		2 ¹	<i>R⁰ START</i> RELAY STATE SELECT (ON-OFF DATA)		2 ¹	<i>1⁰ START</i> ANALOG OUTPUT OF DAC	
2 ²			2 ²			2 ²		
2 ³	2 ³		2 ³					
2 ⁴	2 ⁴		2 ⁴					
2 ⁵	2 ⁵		2 ⁵					
2 ⁶	G&N DATA 16 BITS		2 ⁶	RELAY SUBGROUP SELECT		2 ⁶		
2 ⁷			2 ⁷			2 ⁷		
2 ⁸			2 ⁸			2 ⁸		
2 ⁹			2 ⁹	2 ⁹				
2 ¹⁰			TRANSLATED IN RCVR/DECODER	2 ¹⁰	LBM / EBM	2 ¹⁰	MODULE SELECT (1 OF 4)	TRANSLATED IN BASEPLATE
2 ¹¹	2 ¹¹			2 ¹¹				
2 ¹²	2 ¹²			2 ¹²				
2 ¹³	2 ¹³	2 ¹³						
2 ¹⁴	2 ¹⁴	2 ¹⁴						
2 ¹⁵	2 ¹⁵	2 ¹⁵						
2 ¹⁶	2 ¹⁶	2 ¹⁶						
2 ¹⁷	2 ¹⁷	2 ¹⁷						
2 ¹⁸	2 ¹⁸	2 ¹⁸						
2 ¹⁹	TRANSLATED IN RCVR/DECODER	2 ¹⁹		BASEPLATE GROUP & G&N SELECT	2 ¹⁹	TRANSLATED IN RCVR/DECODER		
2 ²⁰		2 ²⁰			2 ²⁰			
2 ²¹		2 ²¹	2 ²¹					
2 ²²		2 ²²	2 ²²					
2 ²³		2 ²³	2 ²³					

Figure 4. Data Format

IN DTCS

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FOR TRAINING PURPOSES ONLY

PROGRAMMING DIAGRAM

FOR TRAINING PURPOSES ONLY

FOR TRAINING PURPOSES ONLY

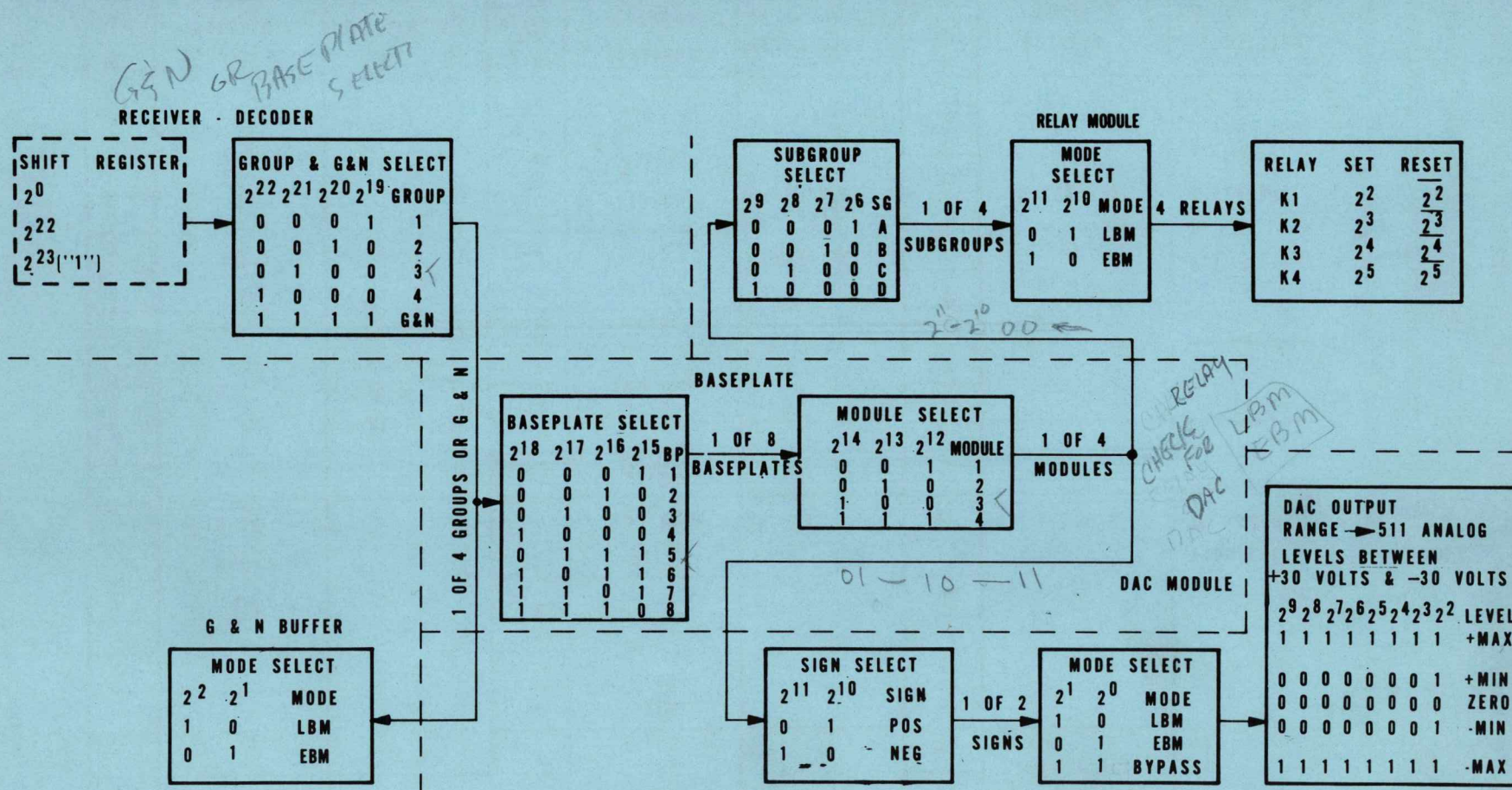


Figure 5. Programming Diagram

the DTVC for each sequence of operations. The first transmission is called the LBM command. After receipt, this transmission is checked and loaded into a buffer memory register. The second transmission of data is called the EBM command. This transmission is checked against the LBM message previously transmitted. If the two transmissions compare, the command stored in the buffer memory register is executed.

Relay Subgroup Select Bits - Bits 6 through 9 are used to select the appropriate subgroups, each of which contains four relays.

Relay State Select Bits - Bits 2 through 5 are used to energize or de-energize the appropriate latching or conventional relays.

CONFIGURATION FOR AN ANALOG COMMAND WORD

Note

An analog command word will be checked and decoded in the same manner as a relay command up to and including module selection.

Sign Select Bits - Bits 10 and 11 are used to determine whether the analog function is to be of a positive or negative polarity.

Analog Output Bits - Bits 2 through 9 represent the output voltage or current from the analog module.

Mode Select Bits - Bits 0 and 1 are used to select the mode of operation. The modes of operation are the load buffer memory mode (LBM), execute buffer memory mode (EBM) and the bypass buffer memory mode (BBM). In the LBM mode, data is loaded into a DAC buffer register. In the EBM mode the contents of the buffer register are checked against the LBM message. If the transmission compares, the DAC will provide an analog output. The BBM mode is used to provide an analog output immediately in direct response to a single command message. The function of this mode is to allow a higher rate of command words to be executed within a DAC to increase the frequency of an analog stimuli when generating a sine wave.

CONFIGURATION FOR GUIDANCE AND NAVIGATION COMPUTER WORD

Reserved Bit - Bit 23 is a reserve bit and will always be a logical "1".

G&N Select Bit - Bits 19 through 22 are used to select the GN buffer unit.

GN Data Bit - Bits 3 through 18 of the GN data format are transferred to the Apollo guidance computer.

Mode Select Bits - Bits 0 and 1 are used to select the mode of operation. The modes of operation are the LBM and the EBM modes. In the LBM mode the data bits are loaded in parallel into the buffer register. In the EBM mode the second data bit format is compared with the contents of the buffer register. If comparison is made, the contents in the buffer register are shifted serially into the Apollo guidance computer.

Figure 1 shows the flow of various return signals that are fed back to the receiver-decoder to indicate that legitimate bit transmission and equipment selection have been accomplished. The receiver-decoder encodes the return signals and produces a 12-bit check reply word which is sent redundantly to the DTVC. The check reply indicates that transmission and selection proceeded without error or, if an error occurred, the type of error is indicated. The error word codes are indicated in Table 1. Bit zero (2^0) of the check reply word is used to give a gross indication of command transmission success or failure. In addition, if an error does occur, bits 2^1 through 2^5 are coded to indicate the specific malfunction that caused the malfunction condition. Bits 2^6 through 2^{11} comprise a code word used by the DTVC.

Table 1
Check Reply Format

2^5	2^4	2^3	2^2	2^1	2^0	
0	0	0	0	0	0	Check Circuitry Error
0	0	1	1	1	0	Transmission Error
0	1	0	1	1	0	Group G&N Select Error
1	0	0	1	1	0	Baseplate Select Error
1	1	0	1	0	0	G&N Buffer Busy
1	1	1	0	0	0	Module Select Errors
0	1	1	1	0	0	Subgroup Select or DAC Sign Select Error
0	1	1	0	1	0	Mode Select Error (LBM-EX)
1	0	1	0	1	0	Buffer Check Error
1	1	1	1	1	1	No Error

2^{11} through 2^6 shall be fixed as follows (ICW)

2^{11}	2^{10}	2^9	2^8	2^7	2^6
1	1	0	1	0	1

RECEIVER-DECODER UNIT

The receiver-decoder (R/D) receives the serially-transmitted, 48-bit word from the DTVC, places 24 of the bits in a staticizing register, communicates with the GN buffer unit and baseplate units, presents a parallel output of data bits to a selected baseplate unit or the GN unit, and redundantly transmits 12-bit serial status words back to the DTVC. The operation of the R/D is described in the following paragraphs. A simplified block diagram of the receiver-decoder is shown in Figure 6.

The bit detector and timing circuit senses each cycle of the input serial data and determines whether the cycle represents a "1" or "0" and whether the "1" or "0" bit is in the first 24-bit pulse train (word 1) or the second 24-bit pulse train (word 2) of the 48-bit transmission. In addition, the bit detector can detect the absence of data bits so that missing bits in the pulse train result in an error indication.

When all 48 bits have been received or when an error in the 48-bit format is detected, the control and clearing circuitry generates the enable signal for transmitting an error word and for clearing circuits to permit subsequent data bit reception.

The control and clearing logic contains the necessary circuitry for detecting a format error caused by either a missing bit or by an improper inter-word space (message window). The inter-word space detector determines that the space between pulse trains (word 1 and word 2) is what is programmed. The circuitry contains a variable delay network that is adjusted according to the amount of time programmed between the last pulse of word 1 and the first pulse of word 2. The time can vary between four microseconds and 25 microseconds. word
counting
4-25ms

The control and clear circuitry also contains logic for detecting the end of word 1 and end of word 2. Detection of end of word 1 is necessary in format error detection and to implement proper routing of the bit detector outputs depending on whether word 1 or word 2 is being received. At the end of word 2 the baseplate group or GN selection circuitry is enabled.

The staticizing register is a 24-bit exchange register that stores the actual message content of the 48-bit command. The redundant bits are not stored. The first 12 bits of word 1 are stored in one 12-bit section of the register. The next 12 bits of redundant data are compared bit-by-bit with the contents of the register. If the redundancy check fails, a transmission error signal is generated which is applied to the check status

RECEIVER DECODER

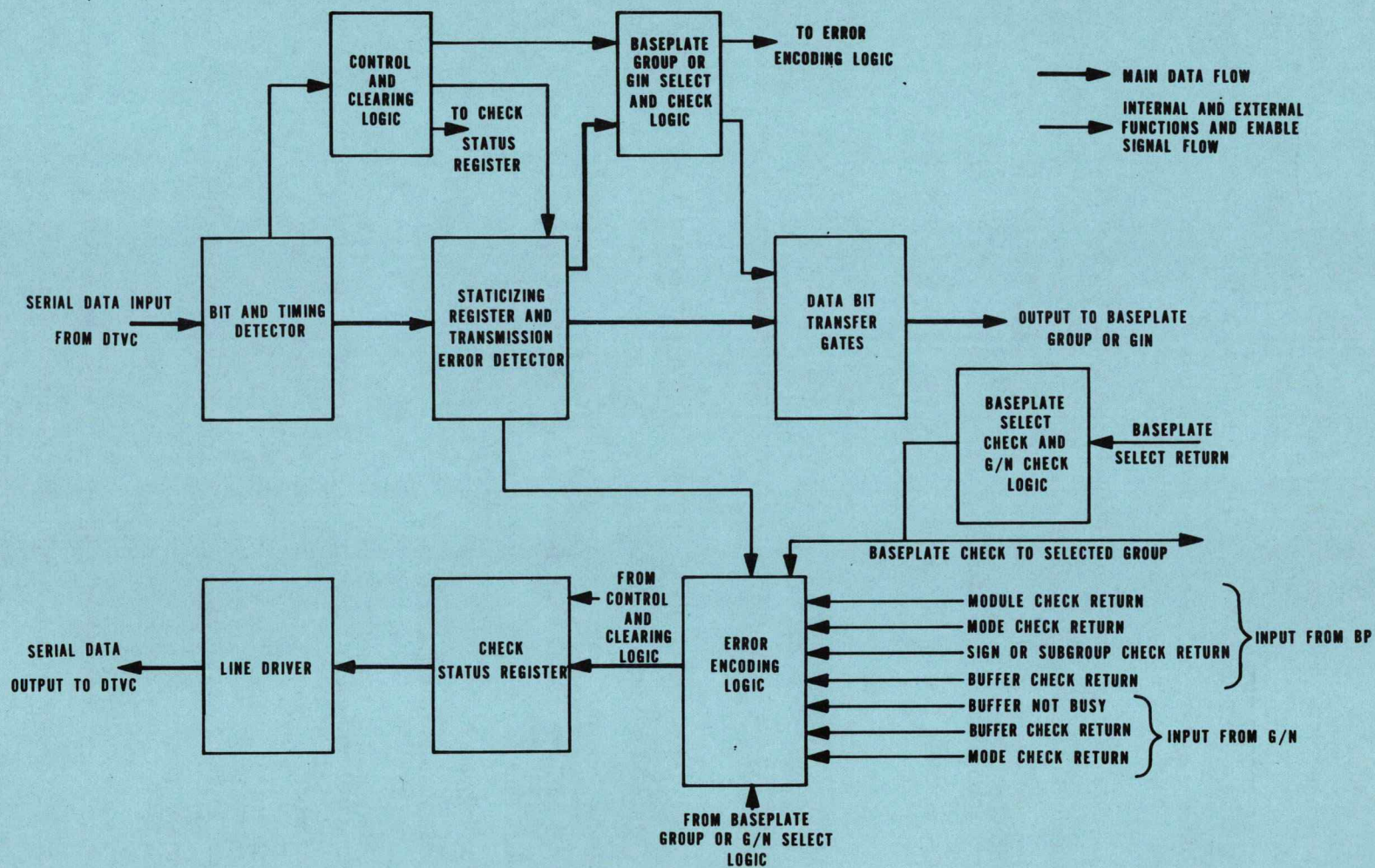


Figure 6. Receiver Decoder

register. If there is no error, the next 12 bits are stored in the second 12-bit section of the staticizing register and compared with the 12 redundant bits in the same manner. If an error is detected in the redundancy check of the second word, a transmission error signal is generated and an error code is transmitted to the DTVC. If no error is detected, an enable signal allows the R/D operation to continue as follows: Upon receiving enable signals from the control and clearing circuitry (end of word two) and the transmission error detector (NO ERROR) the baseplate group or GN select circuit decodes bits 19 through 22 and enables the baseplate group or GN select circuit to select a baseplate group or the GN unit. If only one selection is made by the baseplate group or GN select, the group check signal is produced and no error is indicated. Data bits 0 through 18 are furnished to a baseplate group or data bits 1 through 18 and their complements are furnished to the GN buffer.

The check word encoder encodes the various error signals, (buffer check return, mode check return, sign/subgroup check return, module select return, buffer not busy, baseplate select check, group check, transmit go) to provide a coded digital indication of no error or the type of error if an error occurs. The check word is registered in the check status register.

Checks to assure that one and only one of the 32 possible baseplates has been selected are performed by the baseplate select check and G/N select check logic. This logic monitors the outputs of the select decoders in all 32 baseplates. If more than one baseplate is selected, an error signal is sent to the error encoding logic to transmit an error code to the DTVC. If no error is detected, an enable signal (select check) is sent to the eight baseplates in the selected baseplate group.

The check status register ^{CSR} (CRS) receives the error/no error signals from the check word encoder and sends a check reply word to the DTVC. The check reply is transmitted as a 12-bit word with redundant transmission in bi-phase form. Six of the 12 bits are of fixed format and the remaining six bits (Table 1) comprise the error. The CSR circuitry contains its own timing. A 1-Mc clock (not shown) is enabled by termination of a command message. The clock output triggers a 12-bit counter which causes the CSR to serially output the check reply word.

BASEPLATE UNIT

The baseplate unit receives, decodes, and checks a portion of the data it receives from the receiver-decoder and gates the remaining data to the modules. The status check information is returned to the receiver-decoder. A simplified block diagram of the baseplate is shown in Figure 7.

The function of the baseplate select decoder is to determine if that baseplate has been addressed by the receiver-decoder. When a baseplate has been addressed, the baseplate select decoder circuit sends a return signal to the receiver-decoder and generates an enable signal to other circuits in the baseplate unit. Bits 15 through 18 are used for baseplate selection.

The module select decoder translates bits 12 through 14 into one of four possible combinations for one of four module selections. In addition to receiving the module select code, a baseplate select check signal from the receiver-decoder and an enable from the baseplate select decoder must also be received. Upon receipt of the required enabling signals and a valid module select code the module select decoder generates a select signal on one and only one of the output lines.

When the selected module receives the select signal it sends a select return signal to the module select check circuit. This circuit determines that one and only one module has responded to the select signal (has been selected). If the circuit is satisfied, a module select return signal is sent to the CSR encoder in the R/D indicating that no error was detected in module decoding, and a module select check signal is sent to all modules in the baseplate. If the circuit is not satisfied, an error signal is sent to the CSR encoder and a signal is sent to all modules in the baseplate to inhibit module operations.

After receiving the module select check signal the selected module will perform the operations described in the sections on the various types of modules. Status check signals from each module in the baseplate are received by the check return circuits in the baseplate. These circuits determine if one and only one module in the baseplate has performed the required operations (that is, selecting a subgroup or sign, selecting a mode, etc.). As the status check signals are received from the modules, the sign/subgroup check return, mode check return, and buffer check return signals are sent to the receiver-decoder.

BASEPLATE UNIT

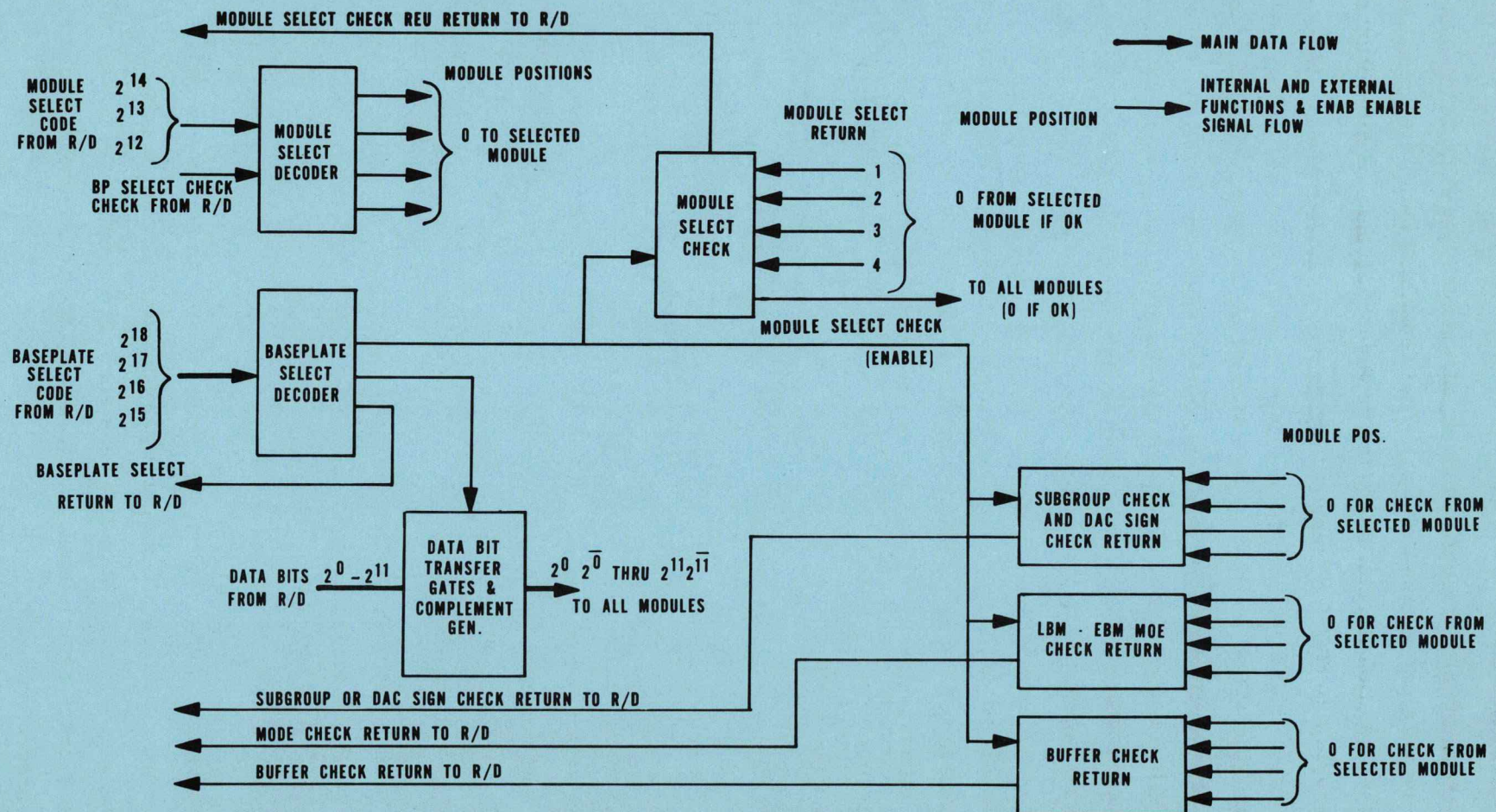


Figure 7. Baseplate Unit

RELAY MODULE

The relay modules provide relay closure outputs to the spacecraft or service equipment. The output may be a voltage from a power source in a system of GSE, from a DAC, or from a power supply in the DTCS. Each relay module contains four subgroups of relays. As pointed out earlier in this study guide, there are two types of relay modules, latching relay modules (LR) and conventional relay modules (CR). Each subgroup, whether LR or CR, contains four single-pole/double-throw type relays. The LR contacts remain closed after the voltage has been removed from the relay coils. The CR contacts remain closed only while voltage is applied to the relay coil. The relay module also contains circuitry to perform subgroup select, mode select, subgroup check, mode check, buffer, and buffer check circuitry. Diagrams of a CR relay module and a LR relay module are shown in Figures 8 and 9 respectively.

CONVENTIONAL RELAY (see Figure 8.)

The conventional relay module is selected to respond to input data bits when the associated baseplate unit furnishes a module select input. In response to the module select signal, the conventional relay module supplies a module select return to the baseplate. The module select return signal is used by the baseplate unit to check module selection. If two or more modules were erroneously selected, the baseplate unit would receive two or more module select return signals and determine that module selection was improper. If module selection proceeds properly, a module select check is received by the selected module from the baseplate. Upon receipt of both the module select and the module select check signals, decoding of the subgroup select bits proceeds. Then the decoding of subgroup select bits is complete and a subgroup check return signal is furnished to the baseplate unit indicating proper subgroup selection. This signal also enables the following subgroup action to continue. The conventional relay module has a load buffer memory (LBM) mode of operation and an execute buffer memory (EBM) mode of operation: LBM/EBM mode data bit decoding is performed to select one of the modes of operation. After a mode is selected and checked for one and only one mode, a mode check return signal is furnished to the baseplate indicating proper mode selection. The check signal is also used to enable the comparison of the relay state select bits with the corresponding bits in the load buffer memory. If the LBM mode was selected, the relay state select bits are loaded into the buffer memory when the mode check signal is generated.

CONVENTIONAL RELAY MODULE

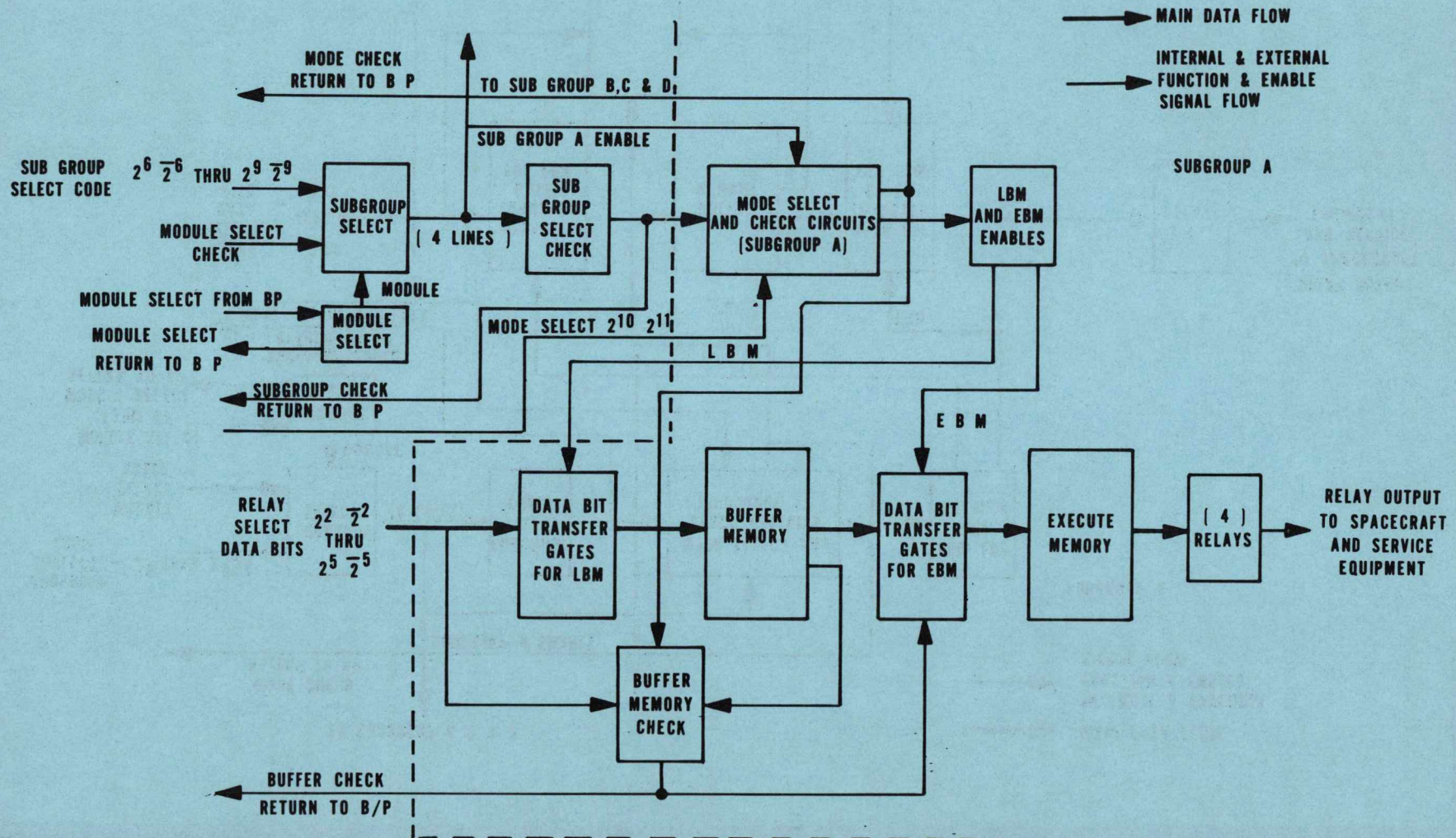


Figure 8. Conventional Relay Module

LATCHING RELAY MODULE

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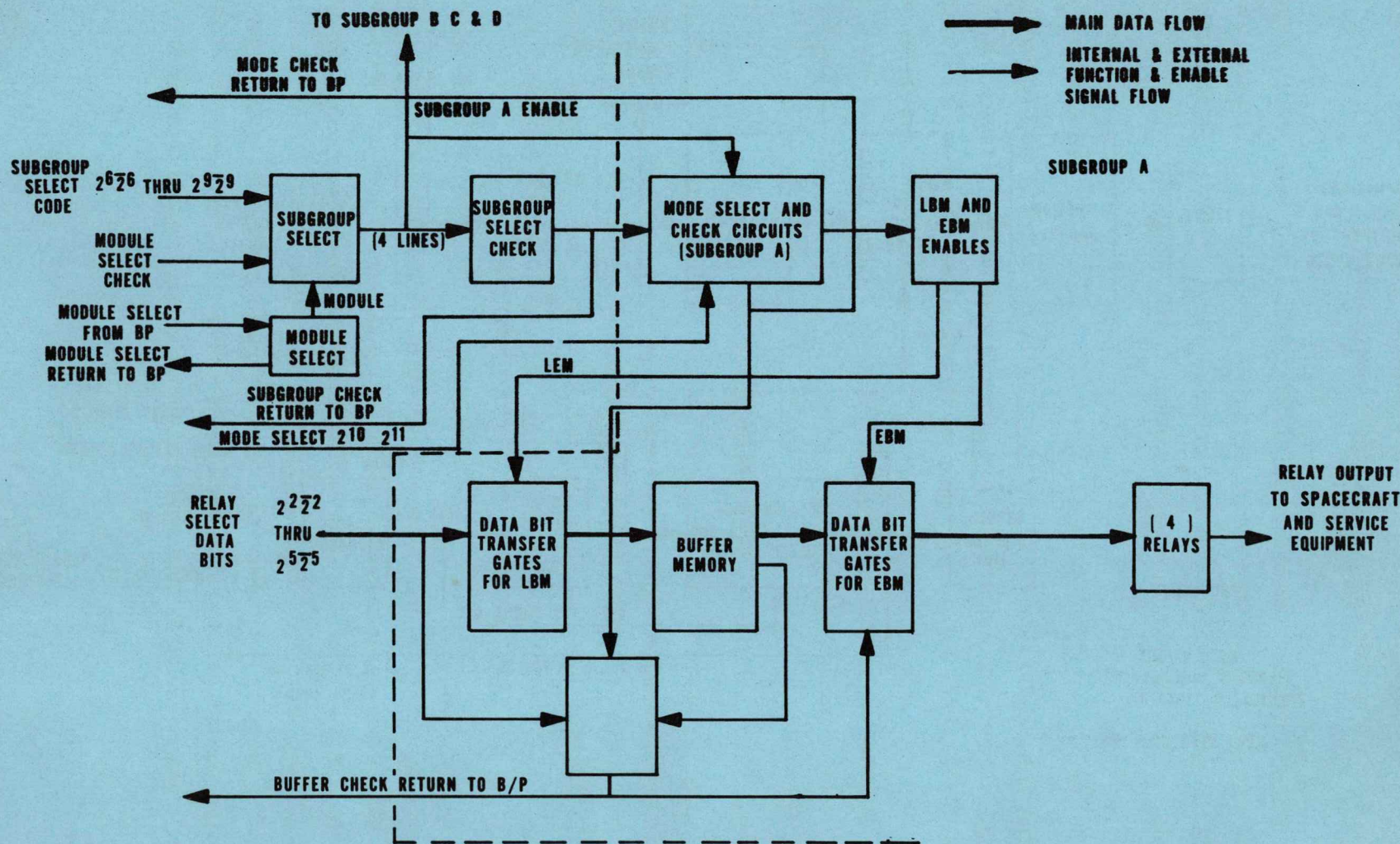


Figure 9. Latching Relay Module

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If the input relay state select bits are the same configuration as bits being held in the buffer memory a buffer check signal is produced. The buffer check return signal is applied to the baseplate indicating a buffer comparison.

In the EBM mode, the data bits in the buffer memory are loaded into the execute memory via the transfer gates if the relay select bits of the EBM word correspond with the bits held in the buffer memory. The configuration of bits loaded in the execute memory determines relay energization configuration and thus relay closure output configuration.

LATCHING RELAY (see Figure 9.)

The operation of the LR module is similar to the operating of the CR module. In the load buffer memory, the data bits are loaded into the buffer memory. In the execute mode, the data bits in the buffer memory determine energization of latching relays if the relay select bits of the LBM word correspond with the bits held in the buffer memory. The bits determining the relay energization configuration determine the relay closure output configuration.

DIGITAL-TO-ANALOG CONVERTER MODULE

The voltage mode digital-to-analog converter (DAC) converts eight data bits plus two sign bits into one of 511 different voltage levels between -30 and +30 volts. The current mode digital-to-analog converter (CMDAC) converts eight data bits plus two sign bits into one of 511 different current levels, consisting of 256 current levels between 0 and 300 milliamperes at 0 to +10 vdc and 256 current levels between 0 and 300 milliamperes at 0 to -10 vdc.

A block diagram of the DAC module is shown in Figure 10. The logic circuitry is identical for both types of digital-to-analog converters. Each type of converter is capable of three modes of operation. In the load buffer mode (LBM), the incoming data is loaded into the buffer memory. In the execute mode (EBM), the data stored in the buffer memory is transferred to the execute memory, and is then converted into an analog voltage or current in the VMDAC or CMDAC output section. When the bypass buffer memory (BBM) is selected, the incoming data is gated directly into the execute memory.

VMDAC DAC OR CURRENT MODE DAC MODULE

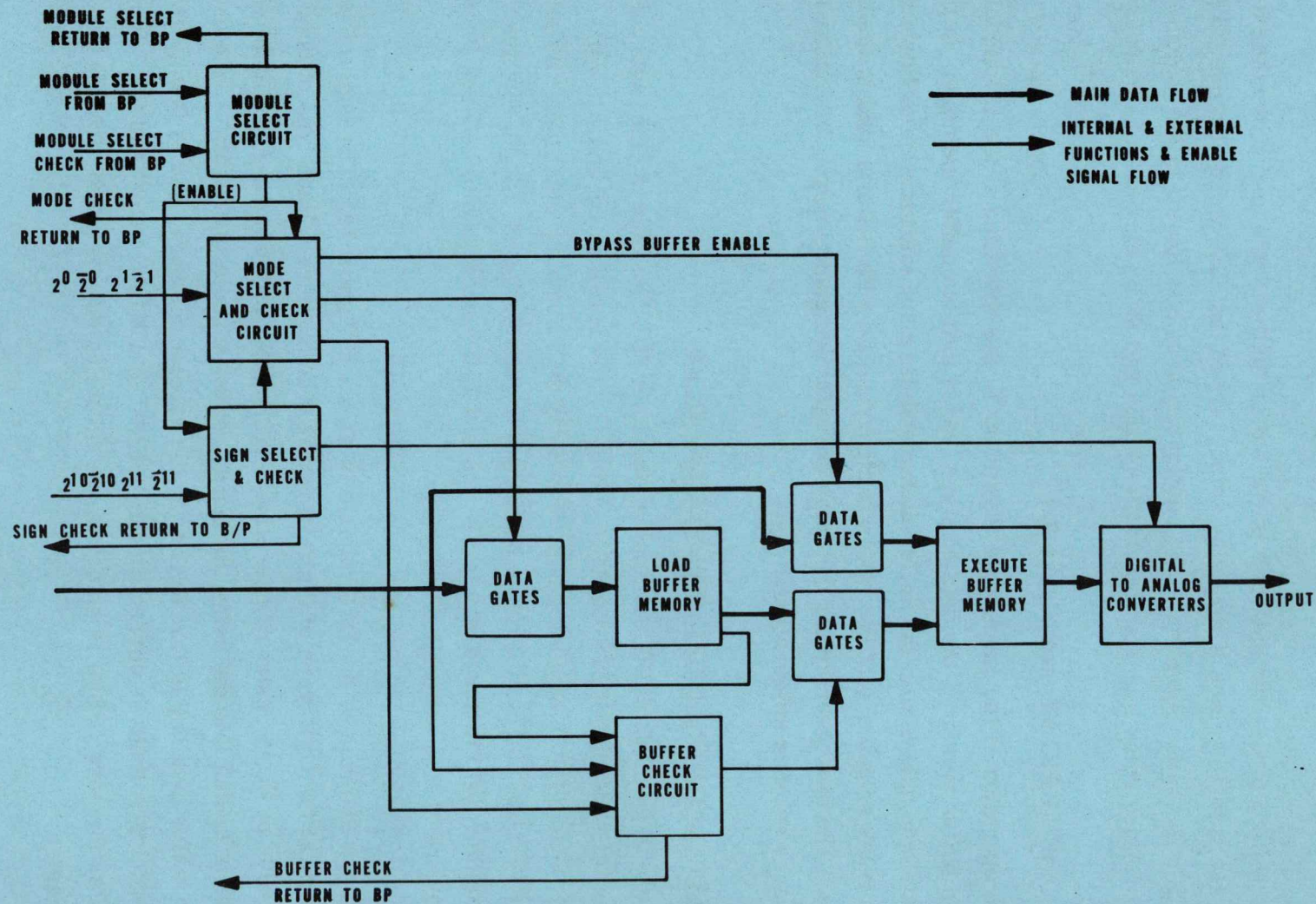


Figure 10. VMDAC DAC or Current Mode DAC Module

GUIDANCE AND NAVIGATION BUFFER UNIT

The guidance and navigation (GN) buffer receives data from the receiver-decoder in parallel form, stores the data, then changes the format of the data to serial form and sends it to the Apollo guidance computer (AGC).

The GN buffer unit receives the LBM word and the EBM word from the R/D unit. Data bits 3 through 18 of the LBM word are loaded into the buffer memory register. The EBM word causes the data bits to be shifted serially into the AGC. Data bits 1 and 2 are used for mode selection (LEM or EBM). The operation of the GN buffer is described in the following paragraphs. A simplified block diagram of the GN buffer unit is shown in Figure 11.

When the receiver-decoder unit selects the GN buffer, the buffer-not-busy circuit determines whether the GN buffer is shifting data into the AGC, or whether the GN buffer has completed the data shift-out and is ready to receive additional data from the receiver-decoder (buffer not busy).

Comparison is performed before the data is loaded into the buffer memory, so the buffer-check-return signal may or may not be generated. In either case, the incoming data will be loaded into the buffer memory. During the EBM word, the incoming data must be the same as the data stored in the buffer memory. If the incoming data is not the same as the stored data, then an error has occurred and no buffer-check-return signal is generated.

The execute control circuit determines when the GN buffer is ready to shift data into the AGC, then starts and controls the data shift-out. At the end of the EXC word, the 16 data bits stored in the GN buffer memory are shifted serially into the AGC. The shift-out is performed at the 1-kc rate, and lasts 16 milliseconds. At the end of this time, the execute control circuit is cleared.

The function of the counter is to determine when all the data has been shifted out of the buffer memory. The counter counts 16 shift-out pulses, then clears the execute control circuit. During shift-out the execute control circuit sends a buffer signal to the buffer-not-busy check circuit.

GN BUFFER UNIT

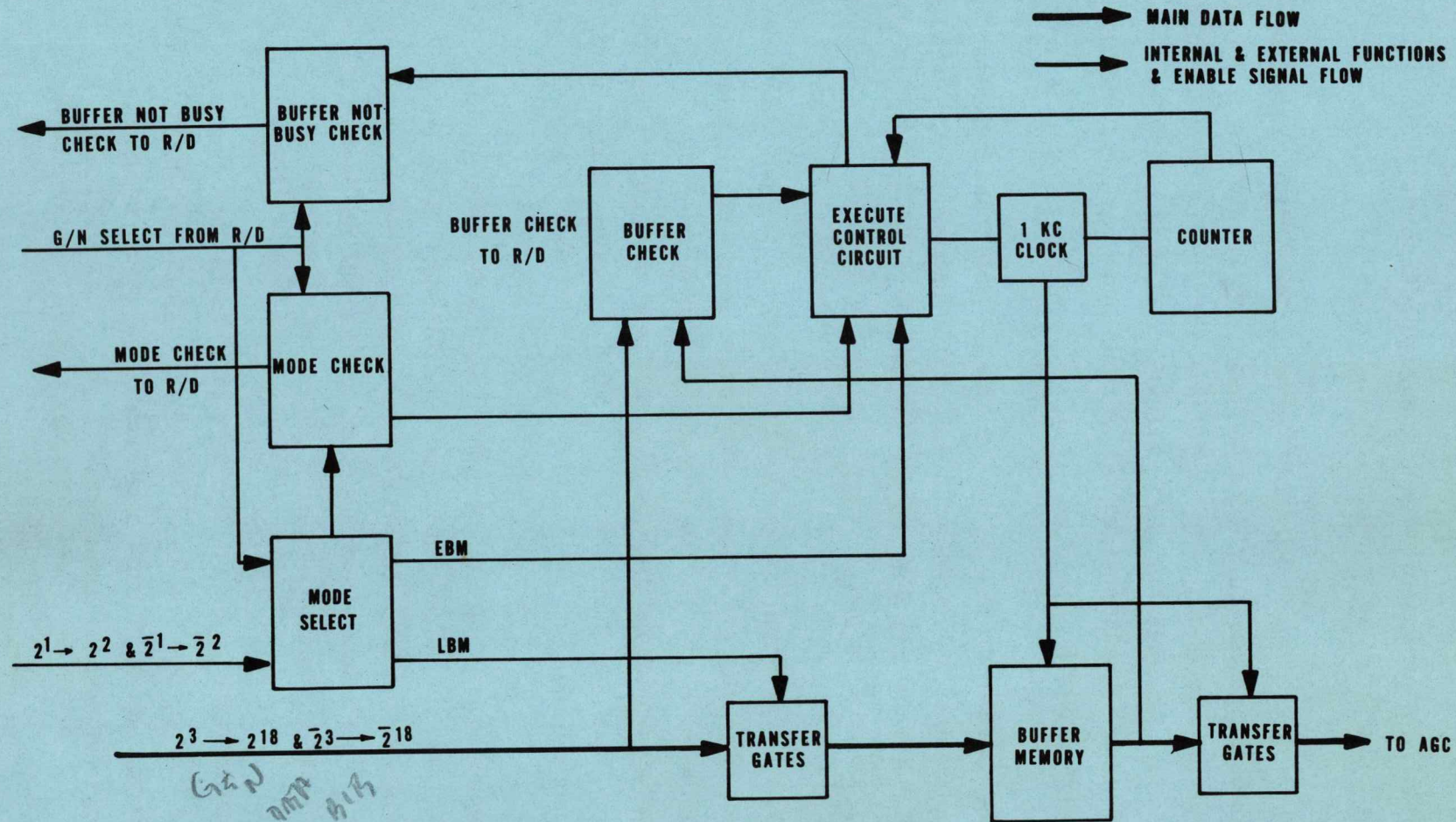


Figure 11. GN Buffer Unit

DIGITAL TEST MEASUREMENT SYSTEM

OBJECTIVES

To familiarize the student with:

- a. Apollo PCM telemetry formats.
- b. Apollo/DTMS interfaces.
- c. Theory of operation (block diagram).
- d. Interleaver/ACE-S/C ground station interfaces.

INTRODUCTION

The primary purpose of the digital test measurement system (DTMS) is to acquire, condition, digitize, and interleave spacecraft and ground service equipment data and then to transmit this data over hard lines to the ACE-S/C ground station processing and display equipment. The DTMS is divided into four major equipment groups:

- a. Airborne (A/B) response system.
- b. Carry-on (C/O) response system.
- c. Servicing equipment (S/E) response system.
- d. Data - Interleaving system.

Each response system contains commutating, encoding, and digital multiplexing equipment which is necessary to convert spacecraft and service equipment sensor outputs into a serial PCM signal. The three response systems outputs (airborne, carry-on, and service equipment) are fed to an interleaver that combines the three separate PCM input signals into a single interleaved (I/L) serial PCM output at a rate of 204.8 kilobits per second. The A/B PCM signal in addition to being interleaved with the other PCM inputs is also transmitted intact (at its original rate of 51.2 kilobits per second) to the ACE-S/C ground station. Figure 1 shows a simplified diagram of the digital test measurement system.

Note

Grumman Aircraft Engineering Corporation uses the generic prefix S92 when identifying DTMS equipment by model number instead of the C14 prefix used by North American Aviation, Inc. Therefore, the identification number of any unit

DIGITAL TEST MEASUREMENT SYSTEM

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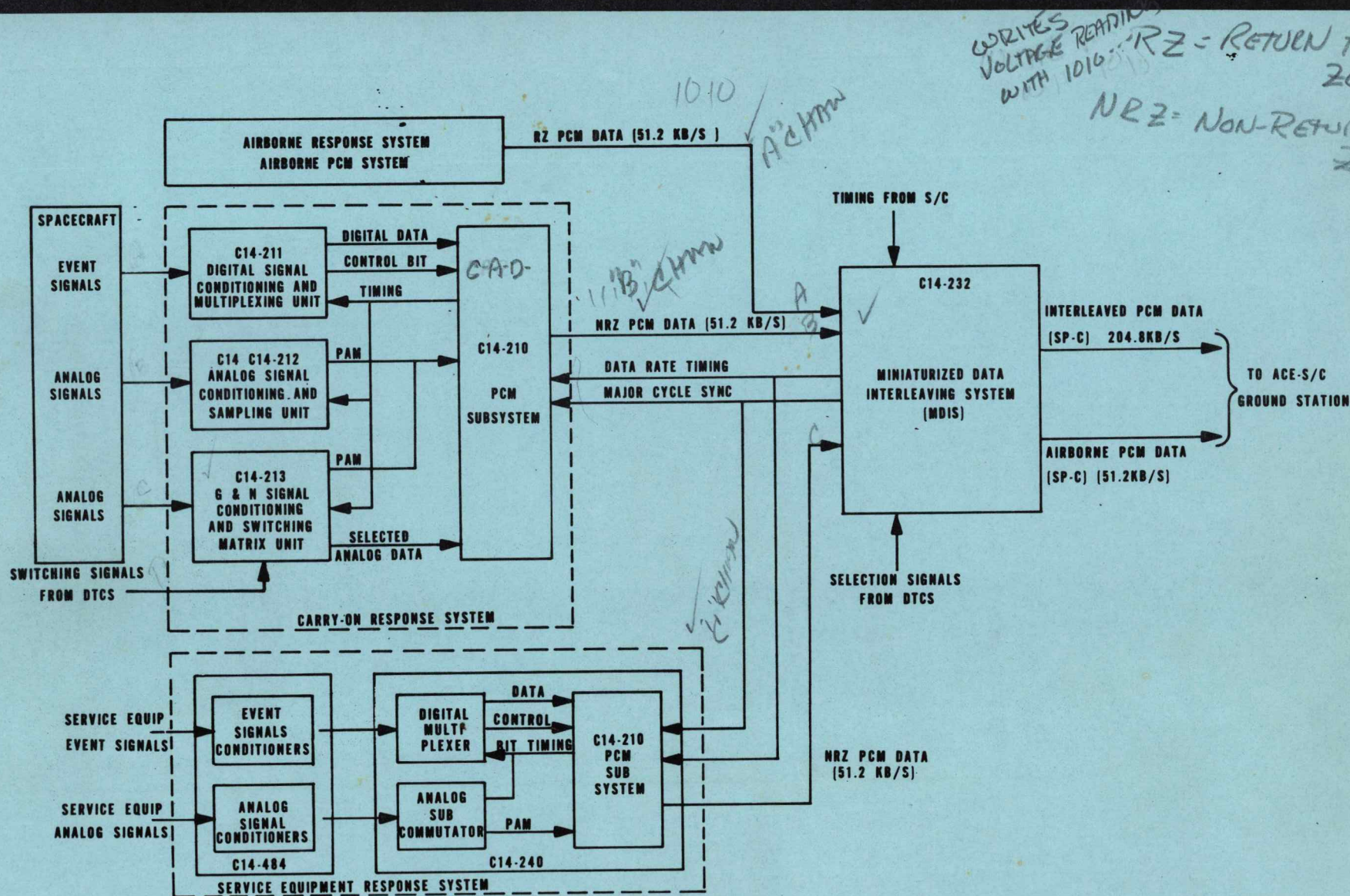


Figure 1. Digital Test Measurement System

8 BITS = 1 WORD = $\begin{cases} 8 \text{ EVENTS} \\ 1 \text{ ANALOG} \end{cases}$

described in this publication can be changed from the North American designation as used, by substituting S92 in front of the hyphenated three-number designator.

$\begin{cases} 1 \text{ WORD} = \\ 8 \text{ EVENTS} \\ 1 \text{ ANALOG} \end{cases}$

The PCM bit stream output of the DTMS to the ACE-S/C ground station contains two types of data words - analog and event. The A/B and I/L PCM organization and formats are shown in Figure 2. Each data word, whether analog or event, contains eight data bits. An analog word represents only one analog measurement; that is, one sensor output is represented by a combination of eight PCM bits ("ones" and "zeros"). An event word, however, represents eight separate events, a "one" representing the occurrence of the event and a "zero" indicating the event has not occurred. For some given events, the opposite condition exists.

Each response system (airborne, carry-on, or service equipment) commutates the transducer output data at a rate of 50 prime frames per second and transmits the data at a rate of 51.2 kilobits per second with 128 words (analog or event) per prime frame. The output of each response system is applied to the interleaver and is commutated into a single serial bit train of 50 prime frames at 204.8 kilobits per second, with 512 words per prime frame. Thus, the interleaver commutates and transmits the PCM data to the ACE-S/C ground station at four times the input bit rate. The interleaver data is bi-phase modulated before transmission to the ACE-S/C ground station.

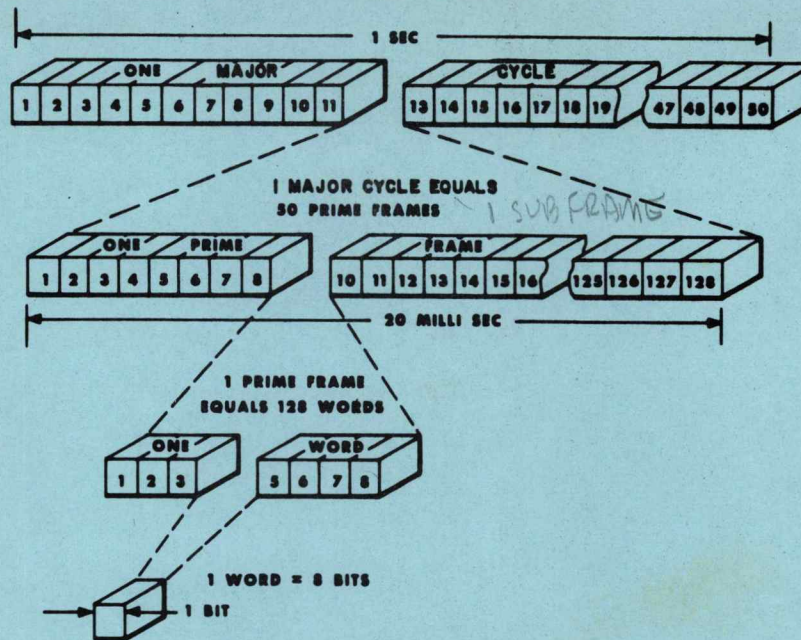
CARRY-ON RESPONSE SYSTEM

The carry-on response system consists of a digital signal conditioner and multiplexer, an analog signal conditioner, a guidance and navigation analog signal conditioner, and a pulse code modulation system. The output format of the carry-on response system is 50 prime frames per major cycle - 128 words being equal to one prime frame at a rate of the 51.2 kilobits per second.

DIGITAL SIGNAL CONDITIONER AND MULTIPLEXER UNIT (C-14-211)

The digital signal conditioner and multiplexer unit time shares eight output lines from up to 320 digital input lines. The multiplexer divides the input lines into 40 groups of eight event inputs per group. Each group of eight events is referred to as an event word. The multiplexer samples the inputs, one word at a time in a time ordered sequence and sends the word on eight parallel lines to the PCM system.

A/B PCM FORMAT



I/L PCM FORMAT

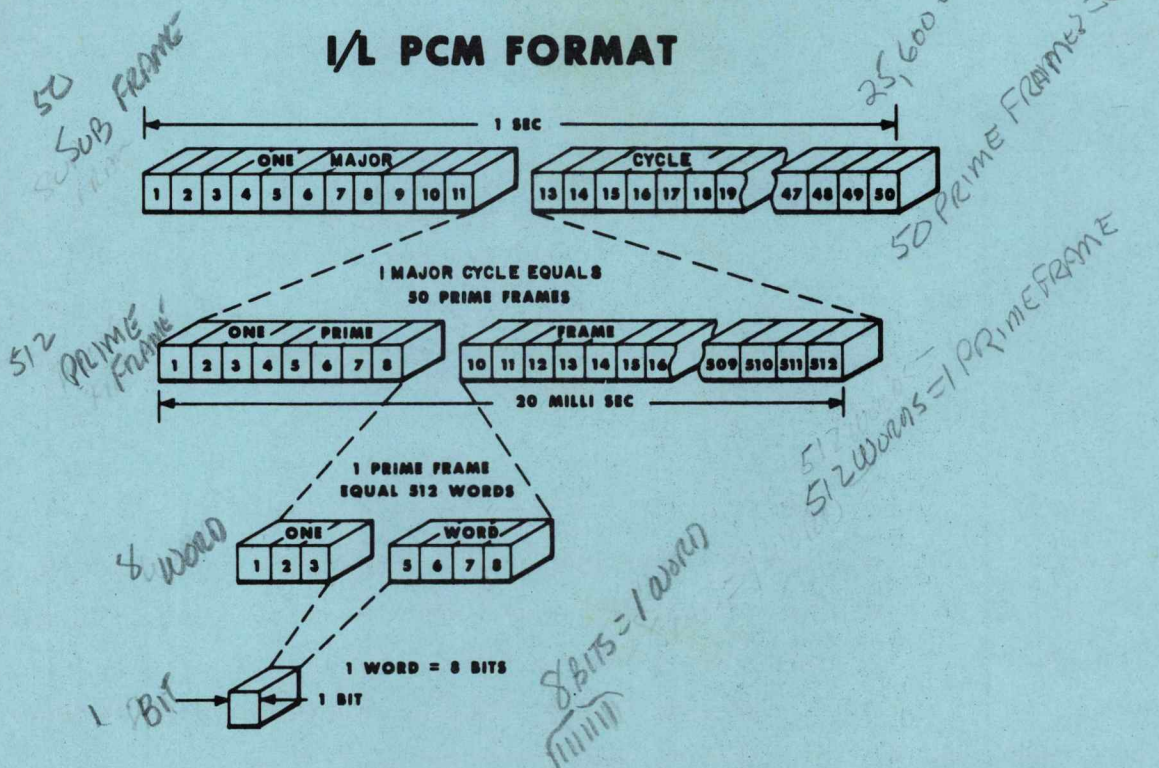


Figure 2. A/B and I/L PCM Format

Figure 3 shows a simplified block diagram of the digital signal conditioner and multiplexer unit. The counter and control bit network perform two independent functions. The counter will sequence through 50 unique states once per second to provide 50 prime frame timing signals. The word select logic generates enable signals representing selected word slots within selected prime frames to cause sampling of one of the forty 8-bit input words. The word select logic is controlled by the counter and by the sampling rate gates. The word select logic connects to the multiplexer gates to enable 8-bit words to be routed through the signal output network to the PCM system.

The signal output network contains the sampling rate gates, sync word and digital word standard logic, and the signal output logic. The sampling rate gates identify the primary gate control times during which the multiplexer may sample digital inputs. Sampling rate gates may be selected to cause the unit to sample event data at one sample per second, ten samples per second, 50 samples per second, 100 samples per second, and 200 samples per second. The 50, 100, and 200 per second gates are presently not used, but are available for future expansion of the multiplexer. The sampling rate gates are driven by the primary gate control timing signal from C14-210 unit.

The digital word standard and sync word logic provide an 8-bit word with a fixed pattern for test purposes. This word will be inserted in word slot 121 of each prime frame. The circuit is also capable of providing a sync word in word slot one of each prime frame.

sync
word
slot
121
of
prime
frame

GUIDANCE AND NAVIGATION SIGNAL CONDITIONER AND SWITCHING UNIT (C14-213)

The guidance and navigation signal conditioner unit accepts up to 150 analog input signals from the guidance and navigation system. The unconditioned input signals are converted to a voltage level from 0 to 5 vdc that is proportional to the input signal. The conditioned signals are then subcommutated by three 50-channel subcommutators. In addition, 32 of the conditioned signals are applied to a switching matrix. The switching matrix provides a means of selecting conditioned analog signals, one at a time, to be sent directly to the PCM subsystem (C14-210). The switching matrix is controlled by commands that select a particular channel. These commands are developed by relays in the digital test command system. The output of the switching matrix is applied to the carry-on PCM system (C14-210) for high-speed sampling. Figure 4 shows a simplified diagram of the G&N signal conditioner and switching matrix unit.

DIGITAL SIGNAL CONDITIONER AND MULTIPLEXER UNIT

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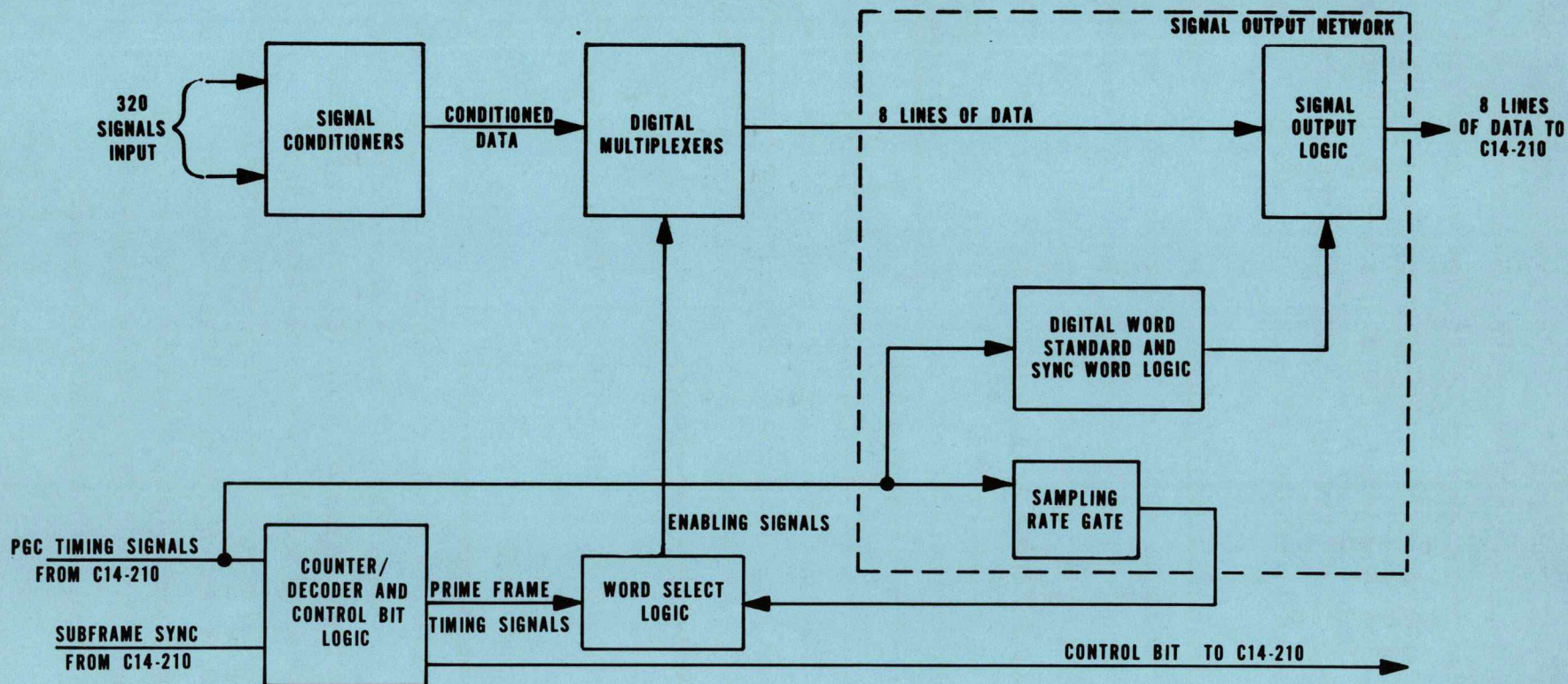


Figure 3. Digital Signal Conditioner and Multiplexer Unit

G&N SIGNAL CONDITIONING AND SWITCHING UNIT

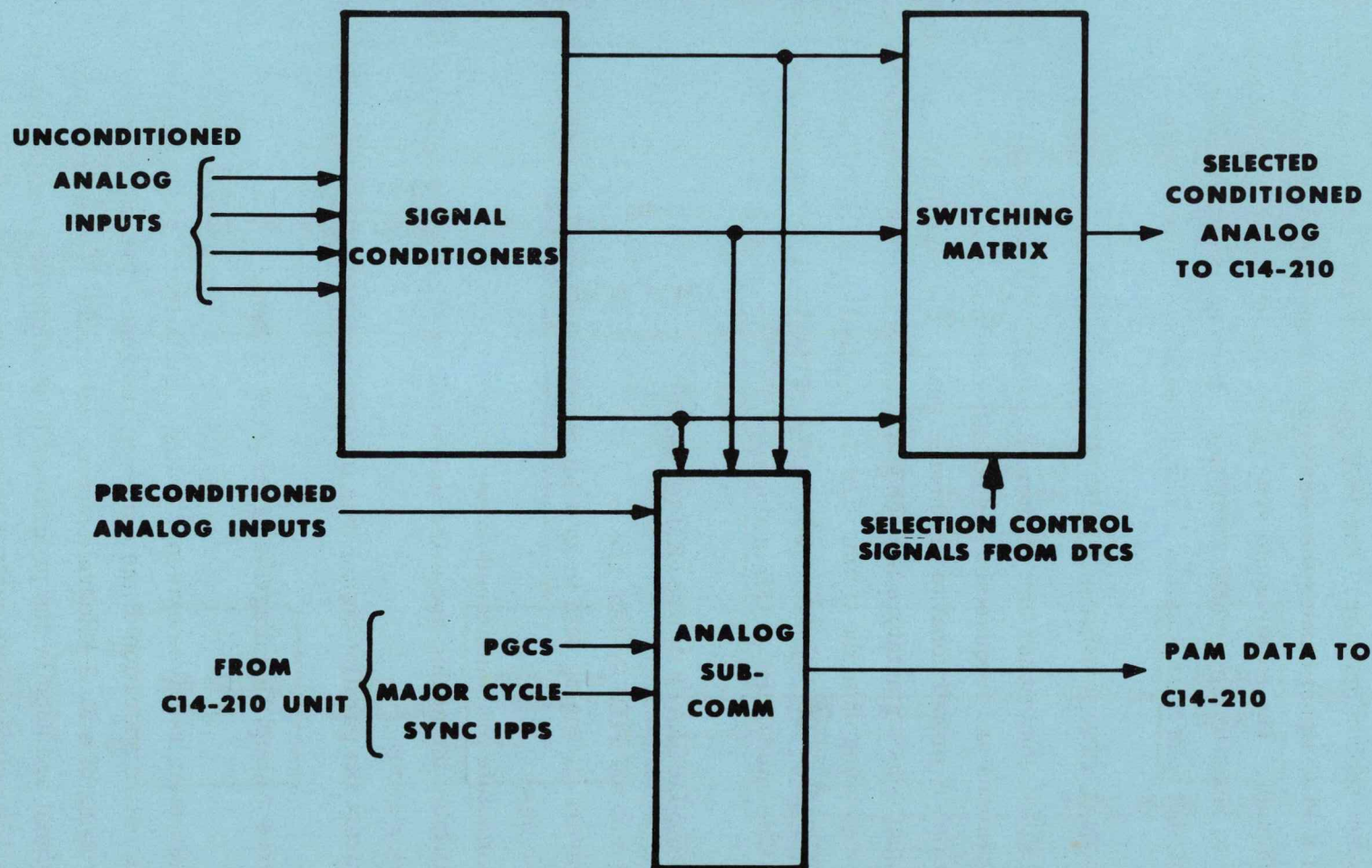


Figure 4. Guidance and Navigation Signal Conditioner and Switching Matrix Unit (C14-213)

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Each subcommutator can accept 50 analog channels in the 0- to 5-volt range and samples each channel sequentially upon receipt of an external timing signal, Primary Gate Control (PGC), from the PCM system (C14-210). Figure 5 shows a simplified diagram of a 50-channel subcommutator. The PGC inputs are fed to a ten input OR gate. The presence of a PGC signal causes the counter to advance to the next channel and sample that input channel. The major cycle sync pulse applied to the subcommutator causes the counter to reset to the channel 1 position. Each channel is normally sampled once each second, but it is also possible to sample each sample ten times each second.

ANALOG SIGNAL CONDITIONER (C14-212)

The analog signal conditioner unit (Figure 6) accepts up to 200 analog input signals of various amplitudes and frequencies and conditions them into a voltage level of zero to five volts which is proportional to the input signal. The signals are then applied to four 50-channel subcommutators for subcommutation at rates of one or ten samples per second depending upon the timing signals supplied by the PCM subsystem (C14-210). The output of each of the subcommutators is a serial train of nonreturn-to-zero (NRZ) pulse-amplitude-modulated (PAM) analog data that is routed to the PCM subsystem.

PULSE CODE MODULATION SYSTEM (C14-210)

The functions of the PCM system are to:

- a. Convert all analog data to an 8-bit digital word representative of the parameter input.
- b. Commutate preconditioned analog data.
- c. Multiplex the analog and event words into specific word locations within a major cycle.
- d. Convert the parallel digital data to a serial bit train for input to the interleaver.

Figure 7 shows a simplified diagram of the PCM system.

The PCM subsystem receives external timing signals from the data interleaver that regulates the entire operation of the carry-on response system. The external timing signals consisting of a 51.2-kilocycle square wave and a 1-pulse-per-second major cycle sync signal are used by the programmer to develop 128 primary gate control pulses. The 128 primary gate control pulses are time coincident with 128 data words to make up a prime frame of data. The major cycle sync pulse occurs at the beginning of each major cycle to provide a zero time reference.

50-CHANNEL SUBCOMMUTATOR

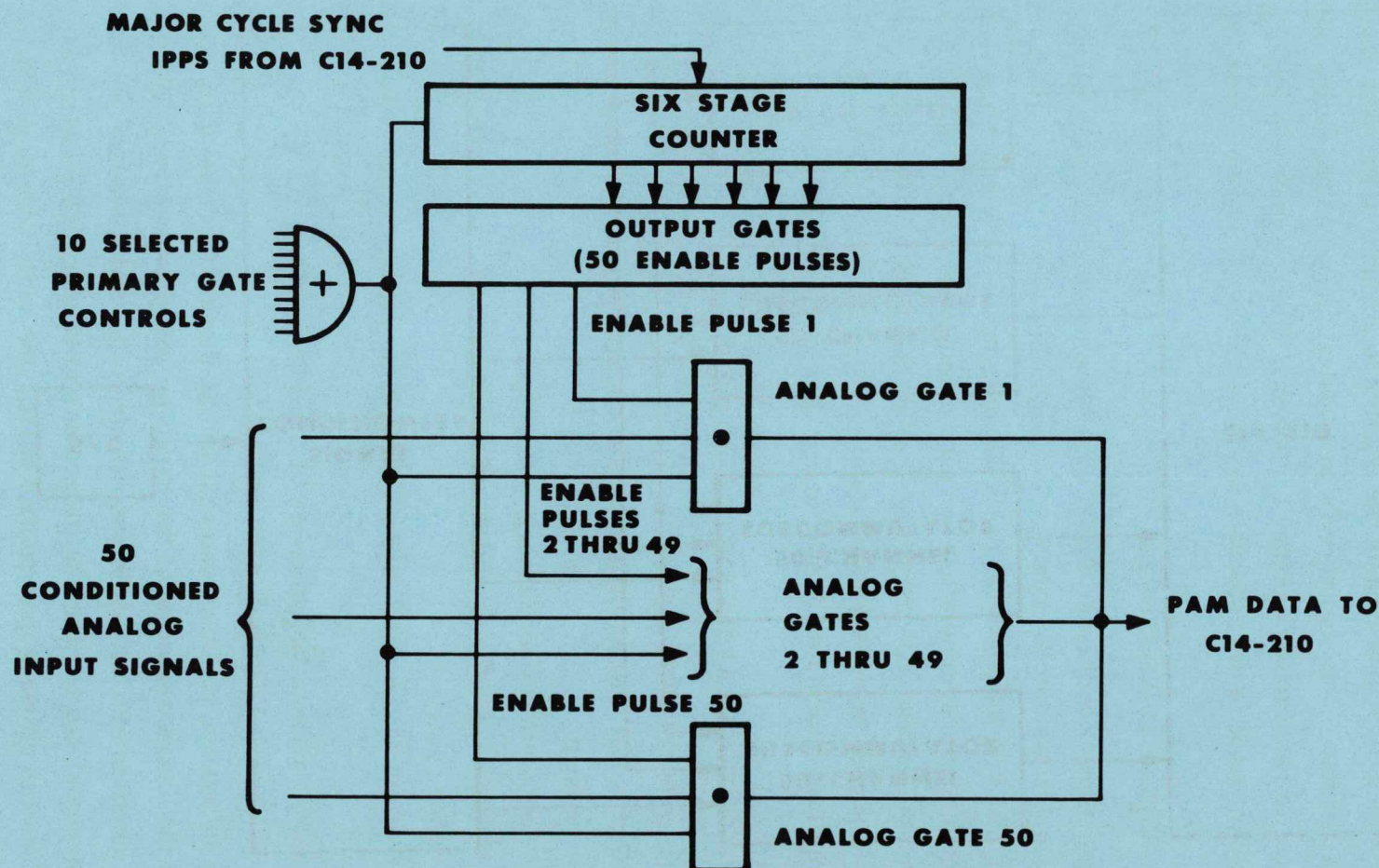


Figure 5. 50-Channel Subcommutator (Simplified)

ANALOG SIGNAL CONDITIONER GROUP C14-212

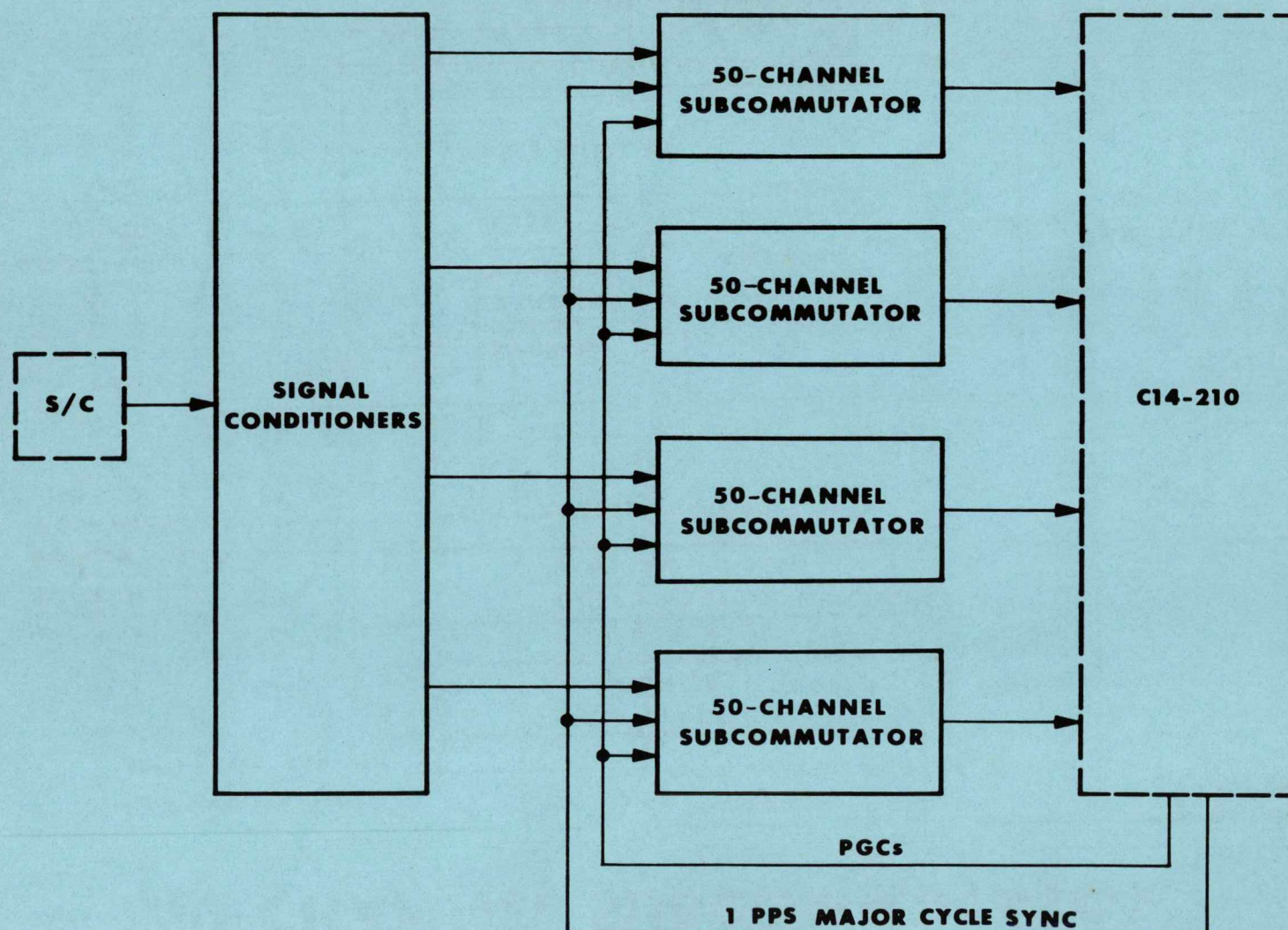


Figure 6. Analog Signal Conditioner Group (C14-212)

PCM SYSTEM

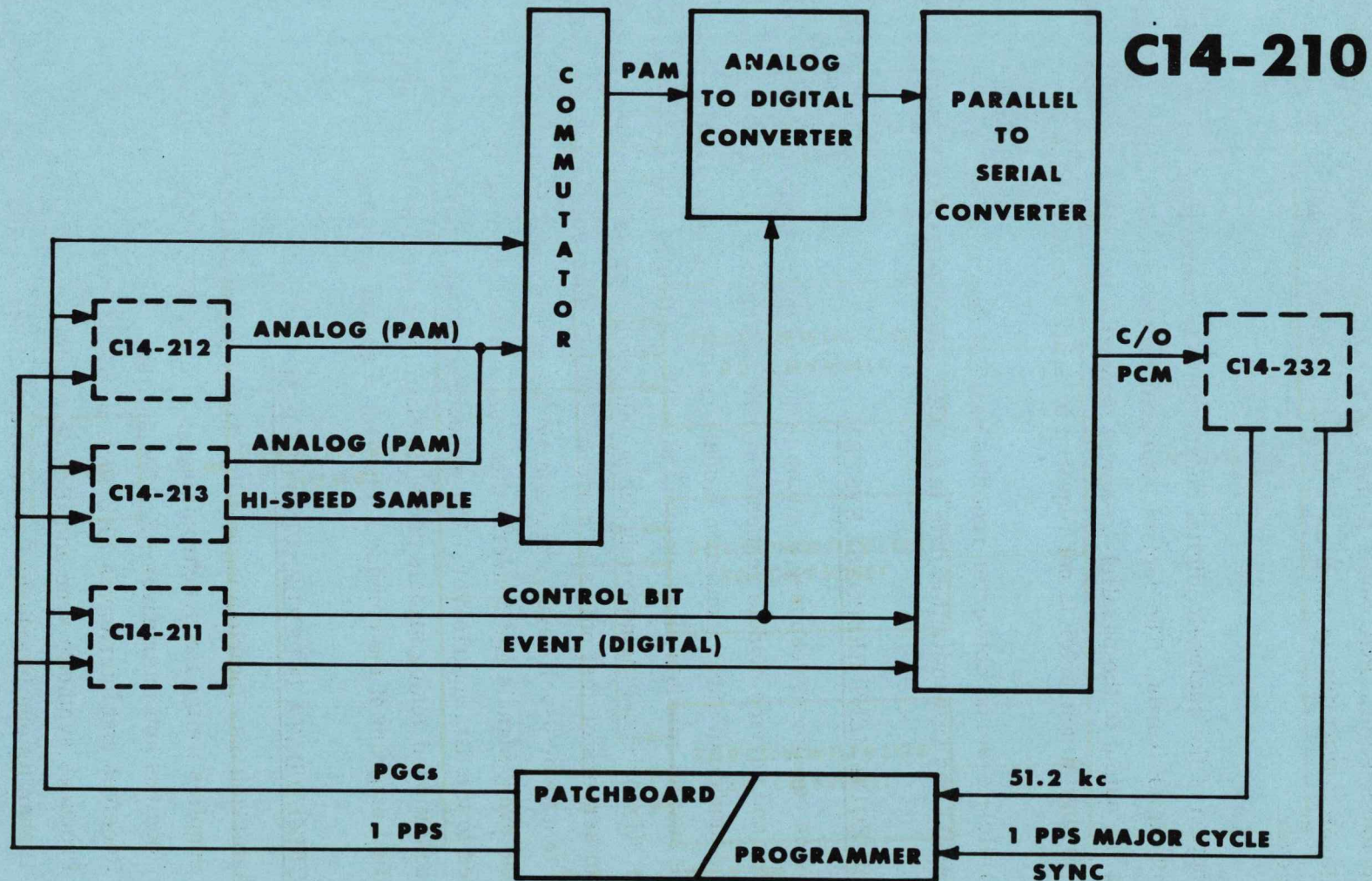


Figure 7. PCM System (C14-210)

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The patchboard receives the 128 PGC's from the programmer and forwards only those channels allocated in the PCM format for the operation and proper output of the carry-on response system. PGC No. 1 is used as a sync word enable pulse in the digital multiplexer. PGC 121 is used as a digital standard enable pulse in the digital multiplexer.

The function of the analog-to-digital converter is to convert the applied PAM data into eight-bit digital words. The control bit signal received from the digital multiplexer inhibits the output to the parallel-to-serial converter during those times when the analog-to-digital converter is not required to digitize analog data.

The parallel-to-serial converter receives parallel data from the A/D converter or unit C14-211 and transmits this data in an NRZ serial PCM train to the data interleaver.

SERVICE EQUIPMENT RESPONSE SYSTEM

The service equipment response systems performs the same functions for the service equipment and service module response signals as the carry-on system does for the command module or lunar excursion module response signals. The service equipment response system consists of an external signal conditioning unit and a spacecraft adapter. The external signal conditioning unit conditions analog signal voltages received from sensors or test points to a proportional 0- to 5-volt level, and event signal voltages to a 0- or 6-volt level. The spacecraft adapter receives the conditioned analog and event signals and converts these signals into a serial PCM format which is forwarded to the data interleaver. The spacecraft adapter has the capability of accepting 200 conditioned analog signals and 992 conditioned event signals. Figure 8 shows a simplified diagram of the service equipment response system.

MINIATURIZED DATA INTERLEAVING SYSTEM

The miniaturized data interleaving system (MDIS) performs the following functions:

- a. Supplies timing for synchronizing up to eight NRZ PCM systems.
- b. Receives and interleaves RZ PCM inputs. *A/B 51.2*
- c. Receives and interleaves NRZ PCM inputs. *C/D 3/1.6 ANALOG 204.6*
- d. Produces synthetic sync and ID code words.
- e. Transmits one interleaved serial output at 204.8 kilobits per second (bi-phase modulated).
- f. Transmits the two RZ inputs serially at 51.2 or 1.6 kilobits per second (bi-phase modulated). *A/B*

RESPONSE SYSTEM SERVICE EQUIPMENT

C14-240

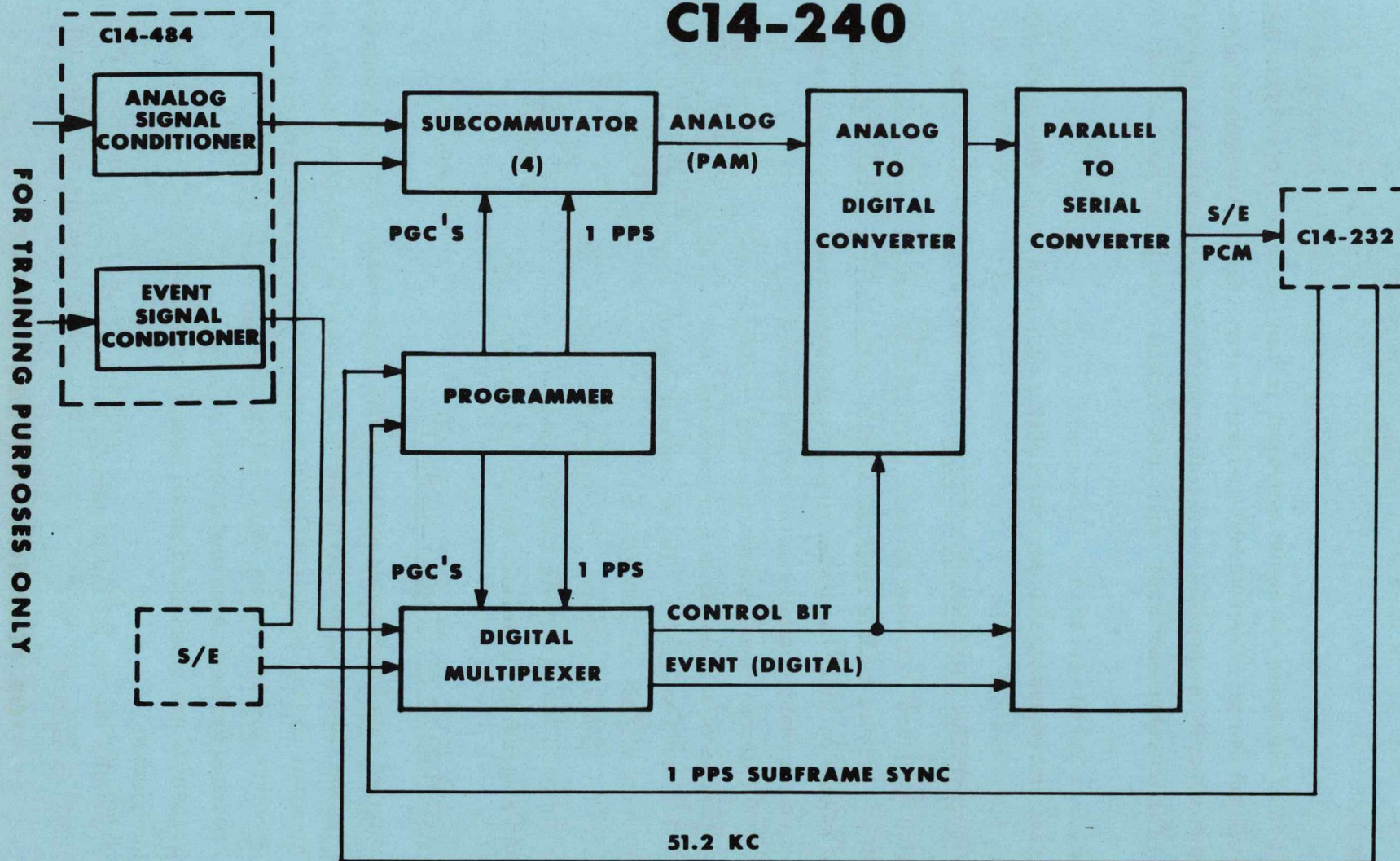


Figure 8. Service Equipment Response System

Figure 9 shows a simplified diagram of the data interleaver. In the Apollo application, only three of the possible ten inputs are used. The A/B PCM data feeds one of the two RZ inputs. The C/O PCM and S/E PCM data constitute two of the eight NRZ inputs.

Timing signals from the central timing equipment or airborne PCM system can be used to drive the internal timing circuits. In the event that neither of the external timing signals is used, or if the selected timing source fails, a phase-locked oscillator will provide the timing signals by operating as a free-running, crystal-controlled oscillator. Selection of input PCM signals and the timing signal source is made by a switching matrix. This matrix is normally controlled by remote switching via a DTCS; however, front panel manual switches are available for local control.

The programmer receives the timing and enabling signals from the input circuitry and generates the necessary timing and control pulses for use within the MDIS. The programmer also supplies data rate timing (51.2 kc) and major cycle sync (1 pps) via the output circuitry to each of the eight possible NRZ PCM data sources. In the present configuration the timing signals are applied to the carry-on response system and the service equipment response system.

by ABC B, A, C
ABC A
The digital data to be interleaved is first conditioned and subinterleaved into four serial data trains. The data interleaver receives the data from the input circuitry and interleaves this data into a composite serial train. The interleaver also receives synthetic sync words to replace that normally supplied by a response system input if for some reason the data input has been deselected by the switching matrix. If the airborne or alternate RZ channel is open, it will be necessary to generate a synthetic sync word and a synthetic ID word. Figure 10 shows the input and output format of the interleaver. Only the first four sync words and the first ID word of the interleaver output are required by the decommutator in the ACE-S/C ground station.

The data outputs of the MDIS are converted to bi-phase formats in synchronism with timing signals from the programmer. The bi-phase data is then conditioned by the line drivers for transmission by coaxial cable to the ACE-S/C ground station where it will be processed and displayed for spacecraft test engineer evaluation.

SUMMARY

The DTCS equipment that is described in Study Guide 410-0 (108) and the DTMS equipment covered by this study guide are frequently grouped together and referred to as the

DATA INTERLEAVER SIMPLIFIED BLOCK DIAGRAM

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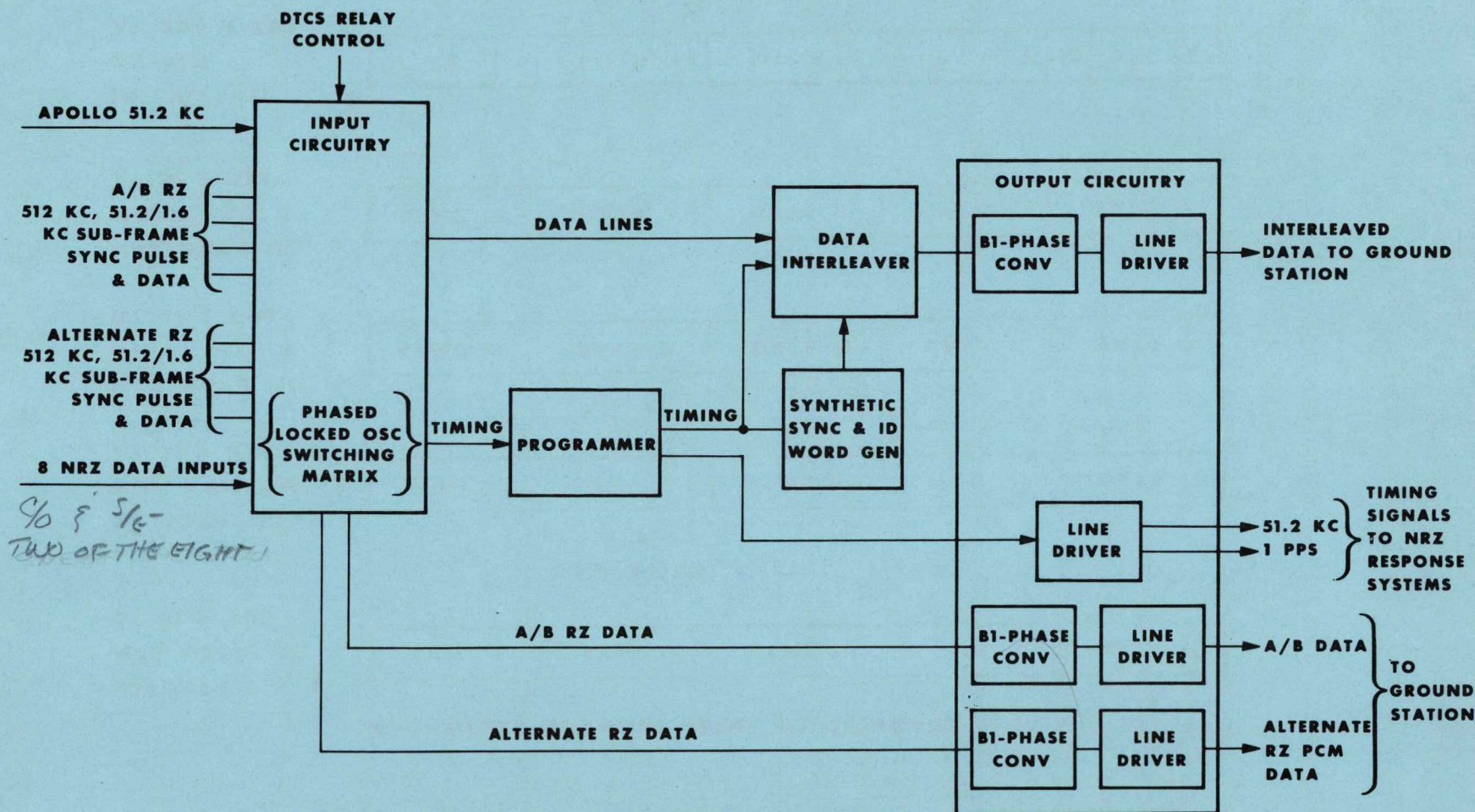


Figure 9. Data Interleaver Simplified Block Diagram

MDIS DATA INPUT & OUTPUT FORMATS

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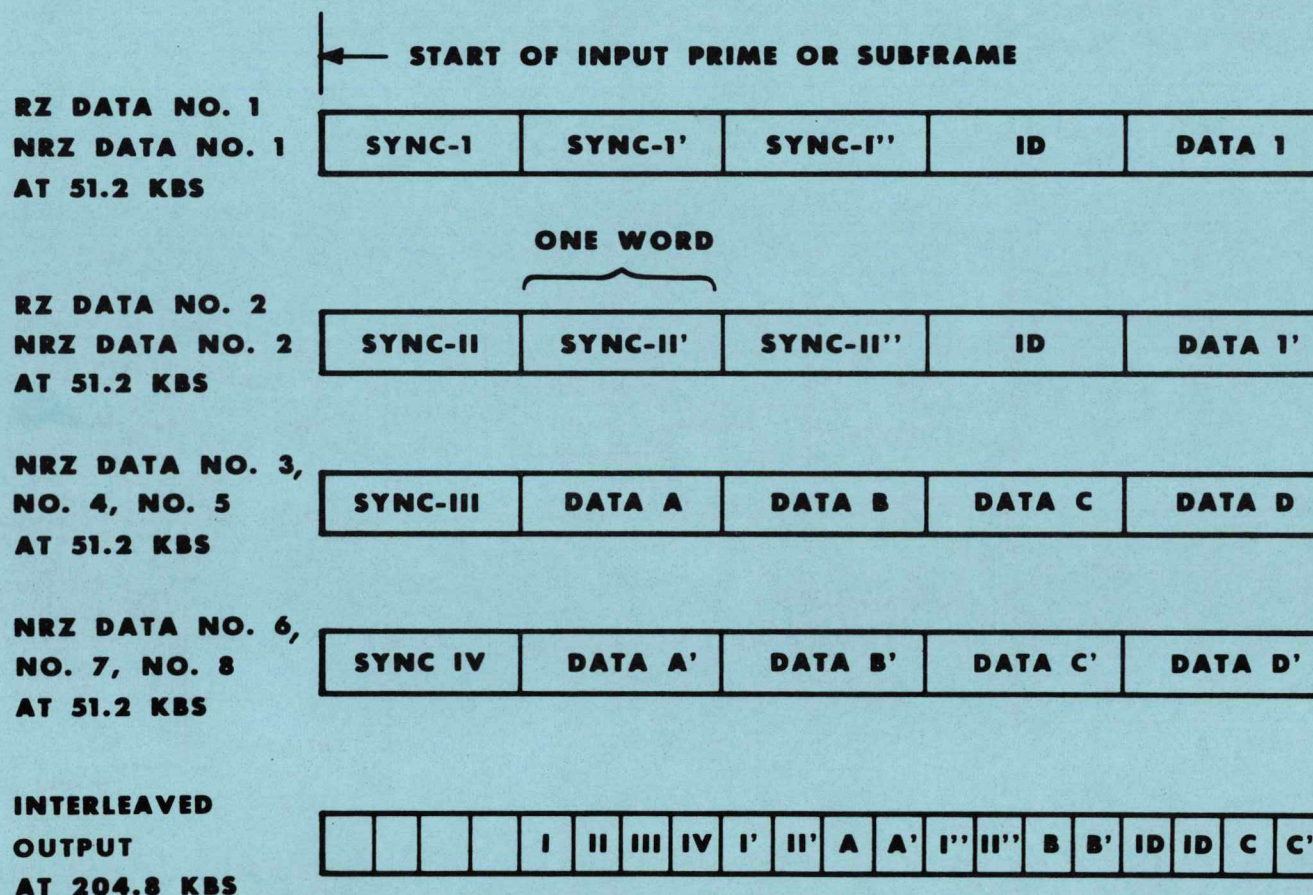


Figure 10. MDIS Data Input and Output Formats

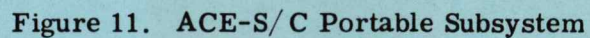
ACE-S/C portable subsystem. Refer to Figure 11 which is a block diagram of the ACE-S/C portable subsystem illustrating the manner in which these systems interface with the ACE-S/C ground station, the Apollo spacecraft (S/C block) and to ground service equipment (service equipment block).

The ACE-S/C ground station interfaces are shown on the left side of the diagram. DTVC No. 1 outputs 24-bit serial commands via the terminal patch facility (not shown) to the C/O DTCS which converts the command into a stimulus and applies it to the addressed test point via the J-Box. The spacecraft response is routed through the J-box to the appropriate checkout signal conditioner which outputs the conditioned response to the checkout PCM unit where the conditioned response is digitized (if necessary) and commutated into the C/O PCM input to the MDIS.

The interface between the ACE-S/C portable subsystem and the ACE-S/C ground station is shown at the bottom left of the diagram. The I/L PCM and A/B PCM outputs of the MDIS are routed through the terminal patch facility (again not shown). The function of the terminal patch facility is to allow a given ACE-S/C ground station to service one of several spacecraft test bays. The video output signals (I/L PCM and A/B PCM) of the MDIS from the terminal patch facility are fed to a video distribution and tape transport control unit (VDTTC) located in the computer room of the ACE-S/C ground station. These two PCM signals along with the FM signal constitute the inputs to the data recording and display system. In subsequent lessons, this system will be described and analysed at a functional block diagram level.

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DATA ACQUISITION

OBJECTIVES

To familiarize the student with:

- a. Video distribution and tape transport control.
- b. Magnetic tape recorder/reproducer.
- c. PCM decommutators.
- d. FM/FM group.
- e. Direct access computer interface (DACI).

INTRODUCTION

The Data Acquisition and Decommuration Equipment (DADE) provides for the recording, synchronizing, decommutating, processing of programmed data, and distributing of the data transmitted from the spacecraft vicinity. Three data lines (A/B PCM, I/L PCM, and FM/FM) are routed to this equipment through a terminal patch facility. The DADE group is made up of the video distribution and tape transport control unit, magnetic tape transports, FM/FM equipment, and PCM decommutators. Figure 1 is a block diagram of the DADE.

The video distribution and tape transport control unit is the receiver and distributor of all incoming test data from the spacecraft test area. Three types of test data are received over separate transmission hardlines: (1) interleaved serial PCM digital words, (2) airborne PCM digital words, and (3) FM signals. The distribution of the received test data is accomplished by means of video distribution and tape transport control unit patch-panel assemblies and the appropriate patch-panel coaxial jumper connections. The distribution of the received data is as follows:

- a. Airborne PCM test data to one of the decommutators and to a recording channel on one of the three wideband magnetic tape recorders.
- b. Interleaved PCM test data to the other decommutator and to a recording channel on one of the tape recorders.
- c. FM test data to the FM discriminator and to a recording channel on one of the recorders.

The decommutator units synchronize with the PCM data they receive, decommutate it, perform limit checks, floating point checks, event transition checks, and convert it to several output forms that are then sent to the analog and event display units and to the display computer.

The FM discriminator unit separates the test data contained in the FM signals it receives and it converts the data to analog voltages that are sent to the analog and event display units. The magnetic tape recorder units provide a permanent record of all test data received by the ACE-S/C system. The data recorded on magnetic tape can be played back as required. The playback PCM data is routed to the video distribution and tape transport control unit patch panels and is continuously distributed to the decommutator units. The playback FM data is also routed to the patch panels, but requires special patching connections to be sent on to the FM discriminator unit. The PCM test data received from the spacecraft test area via the terminal patch facility contains information obtained from sensors that are permanently installed in the spacecraft, from carry-on equipment that is removed prior to launch, and from ground service equipment. A composite signal containing all sensor information is developed by units in the spacecraft vicinity and is received at the input to the data acquisition and decommutation units as interleaved PCM test data. The test data obtained from the permanently installed spacecraft sensors also is received as a separate (second) PCM input and is called airborne PCM test data. Certain test data (e.g., outputs of vibration sensors), which is required in a raw form, is received in the form of FM signals.

VIDEO DISTRIBUTION AND TAPE TRANSPORT CONTROL UNIT

VIDEO DISTRIBUTION AND TAPE TRANSPORT CONTROL UNIT FUNCTIONS

The video distribution and tape transport control unit provides:

- a. The means to distribute selectively all incoming raw test data from the spacecraft test area, refined test data generated within the ACE-S/C system, and the support signals (time codes, voice, etc.) generated by the support equipment.
- b. The means to condition certain selected signals prior to their being recorded on magnetic tape.
- c. A magnetic tape recorder remote control switching capability.

The selective routing of test data signals is facilitated by patch panels. The signal mixer and reference mixer/oscillator subassemblies contained in the video distribution and tape transport control unit are used to modify certain selected signals prior to recording them on magnetic tape. The outputs of these subassemblies are routed to the magnetic tape recorders via the patch panels. The signal separator is used to process certain magnetic tape recorder playback signals prior to their distribution

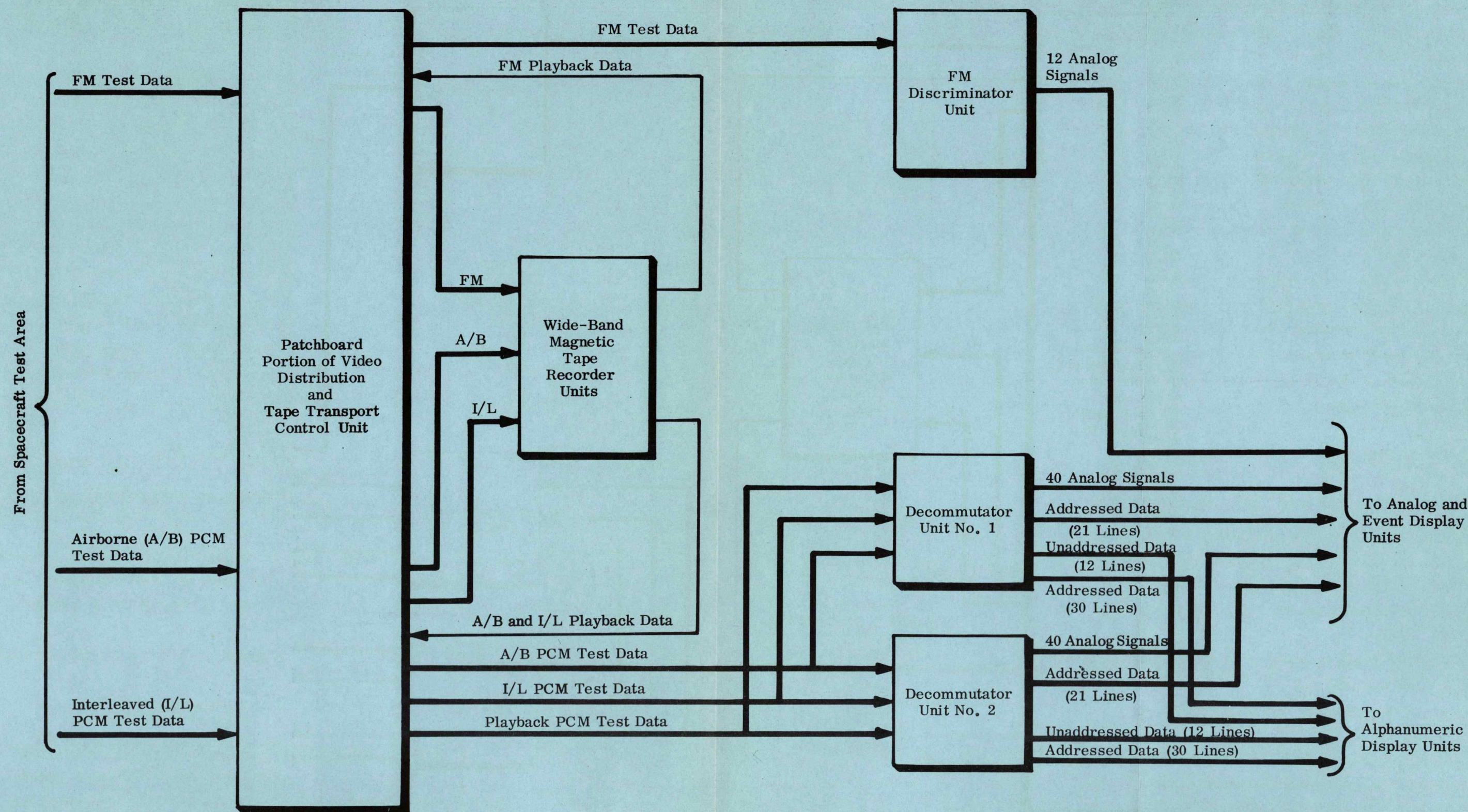


Figure 1. Data Acquisition and Decommulation Equipment Functional Block Diagram

by the patch panels. The magnetic tape recorder relay control unit provides a means by which the magnetic tape recorder transport control unit may be remotely controlled from the computer complex console or from the tape search unit. This unit also is used to route the current status indications of the magnetic tape recorders to the computer complex console and to the tape search unit.

VIDEO DISTRIBUTION AND TAPE TRANSPORT CONTROL UNIT DESCRIPTION

The video distribution and tape transport control unit is composed of five physically identical patch panels. The routing of the signals available at the patch panel is accomplished by means of coaxial jumper cables. Some signals are available on more than one patch-panel connector, e.g., interleaved PCM test data. This availability is accomplished by means of T-connectors on the rear of the patch panel. The exact patch-panel jumper connections to be used are dependent upon specific test program needs and are not given here. With respect to maintenance, the patch panels provide a convenient and centrally located means to monitor many of the signals passed through the units of the ACE-S/C computer room.

The signal mixer, signal separator, reference oscillator/mixer, and magnetic tape recorder relay control units are functionally part of the magnetic tape recording equipment.

MAGNETIC TAPE RECORDER AND REPRODUCER UNITS

MAGNETIC TAPE RECORDER FUNCTIONS

There are three identical magnetic tape recorder units located in the computer room of an ACE-S/C system. They are used to record selected test data resulting from a spacecraft testing sequence. The recorded data is a permanent record of incoming PCM test data, FM test data, reconstructed decommutator PCM data, time code signals, and voice signals. The data stored on the magnetic tapes may be reproduced (played back) at any time to facilitate data reduction, ACE-S/C system preoperation checkout, and maintenance test procedures.

Each magnetic tape recorder is capable of recording and reproducing up to seven discrete channels of data. Each channel may record and reproduce data in either of two ways: Direct Record/Reproduce or Wide Bank Frequency Modulation (WBFM). The recorders are of modular construction and are designed for field modification to fourteen channels should greater capability be required at a later date.

MAGNETIC TAPE RECORDER INPUTS (See Figure 2)

All data signals to be recorded on magnetic tape are routed through the patch panels of the video distribution and tape transport control unit to the magnetic tape recorder units. Certain data, such as airborne PCM test data, is routed through the patch panels directly to a magnetic tape recorder. Other data, such as timing codes and voice, is first patched to a signal mixer unit (located in the video distribution and tape transport control unit), processed, and then patched to a magnetic tape recorder unit.

Each recorder also receives control signals from remote control units. The computer complex console contains three remote control units, one for each magnetic tape recorder unit. A tape search control unit (located in the tape recorder/computer time decoder and search control unit) also supplies remote control signals to the magnetic tape recorders. All remote control signals are fed to the magnetic tape recorders via a magnetic tape recorder switching control unit located in the video distribution and tape transport control unit. The switching function of the magnetic tape recorder switching control unit is controlled by the operator of the computer complex console.

MAGNETIC TAPE RECORDER OUTPUTS (See Figure 2)

All data signals reproduced (played back) by the magnetic tape recorder units are routed to the appropriate units of the ACE-S/C system by the patchboards of the video distribution and tape transport control unit. Certain test data (e.g., PCM test data) is routed through the patch panels directly to the appropriate ACE-S/C units. Some data (e.g., timing codes, voice, etc.) are first patched to a signal separator (located in the video distribution and tape transport control unit), processed, and then patched to an appropriate ACE-S/C unit.

MAGNETIC TAPE RECORDER DESCRIPTION

Each magnetic tape recorder provides seven channels for recording and reproducing wideband signal data. The tape used with the magnetic tape recorder is 0.5-inch wide, 1.0-mil thick, mylar-base magnetic tape on 14-inch reels. (For 14-channel operation, 1-inch tape is used.) The recorders have four record/reproduce speeds: 15, 30, 60, and 120 inches per second. Direct record frequency response is from 400 cps to 1.5 megacycles. Wideband FM record frequency response is 0 to 400 kilocycles. The basic components of the tape recorder are a precision four-speed tape transport, a control section to control the tape transport, and the record and reproduce signal circuits.

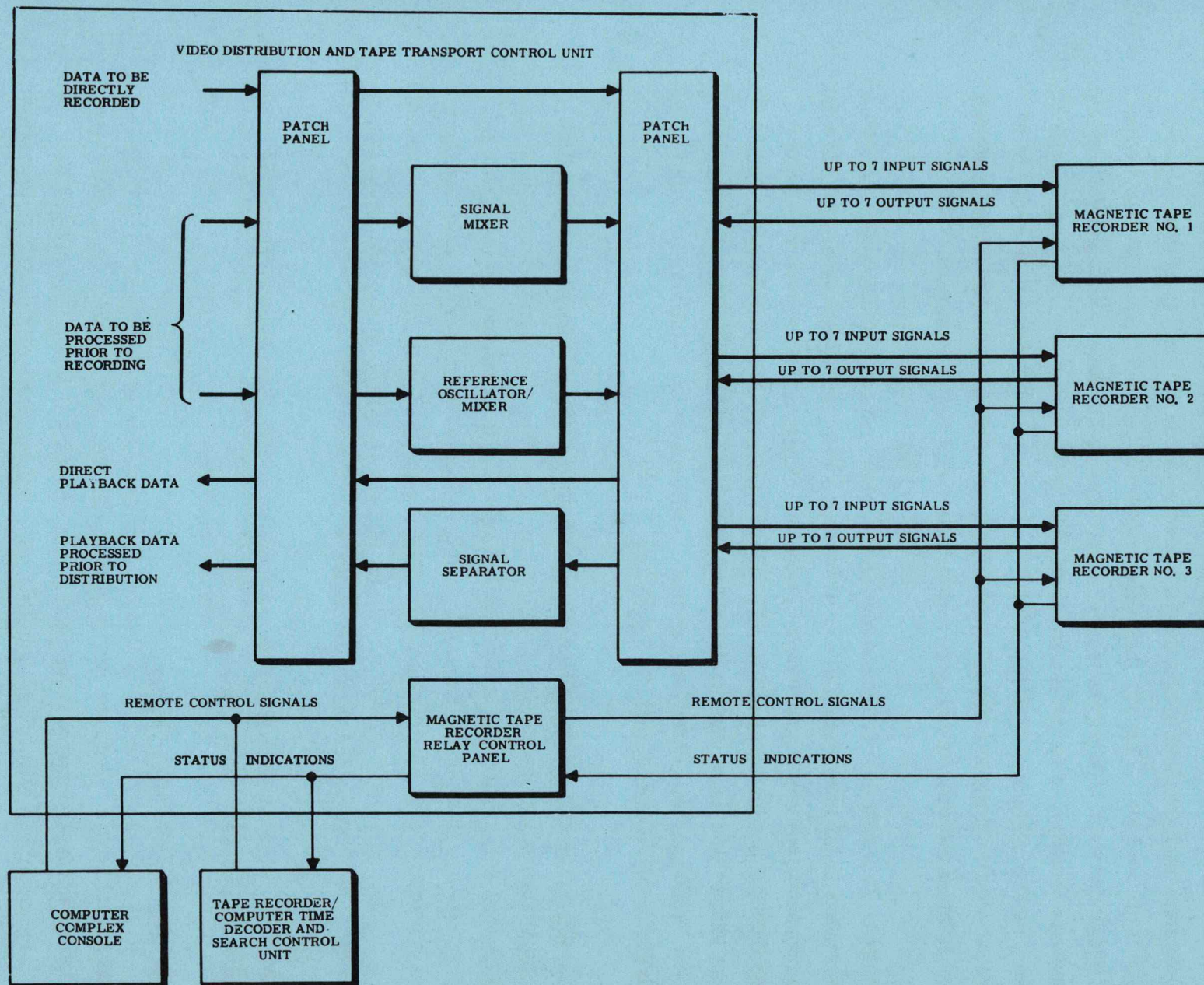


Figure 2. Magnetic Tape Recorder Input/ Output Functional Block Diagram

FM GROUP

GENERAL

The telemetry system used to transmit FM data over an RF link is of the frequency-division multiple type. That is, the radio-frequency carrier is modulated by a group of subcarriers, each of a different frequency. Each subcarrier is frequency modulated in a manner determined by the intelligence to be transmitted. One or more of the subcarriers can be modulated by a frequency-division multiplex scheme in order to increase considerably the number of individual data channels available in the system. The modulation technique used in this system is frequency modulation.

Multiplexing is a scheme of communication system organization whereby many independent channels of information are combined on a noninterfering basis into a common frequency band, for subsequent transmission over a band. In frequency division multiplexing, each individual channel occupies only a designated part of the band rather than the entire band as in time division multiplexing. Available within one carrier band are 18 subcarrier center frequencies, each capable of containing information up to a predetermined band limit.

The FM discriminator group is used in the detection of the FM signals transmitted from the spacecraft to the ACE-S/C ground station. The FM signal is routed to the magnetic tape recording units and to the FM groups simultaneously (see Figure 3). The recorded raw data on the magnetic tape unit is used for playback after testing and for the preservation of FM test data. During a spacecraft test, the received raw data is detected by the FM group, and the output signals representative of the input modulation frequency are recorded on analog paper recorders.

The FM group also contains a subcarrier oscillator and a frequency counter for check-out and alignment of the FM discriminators.

FM DISCRIMINATOR FUNCTIONS

The FM discriminator separates the incoming FM test data received from the video distribution and tape transport control unit and converts it to analog voltages that are sent to the analog and event display units. The unit contains 12 subcarrier discriminators. The inputs of seven of the discriminators are tied in parallel and receive a composite FM signal containing seven subcarrier frequencies from the spacecraft test area or a magnetic tape recorder via the video distribution and tape transport

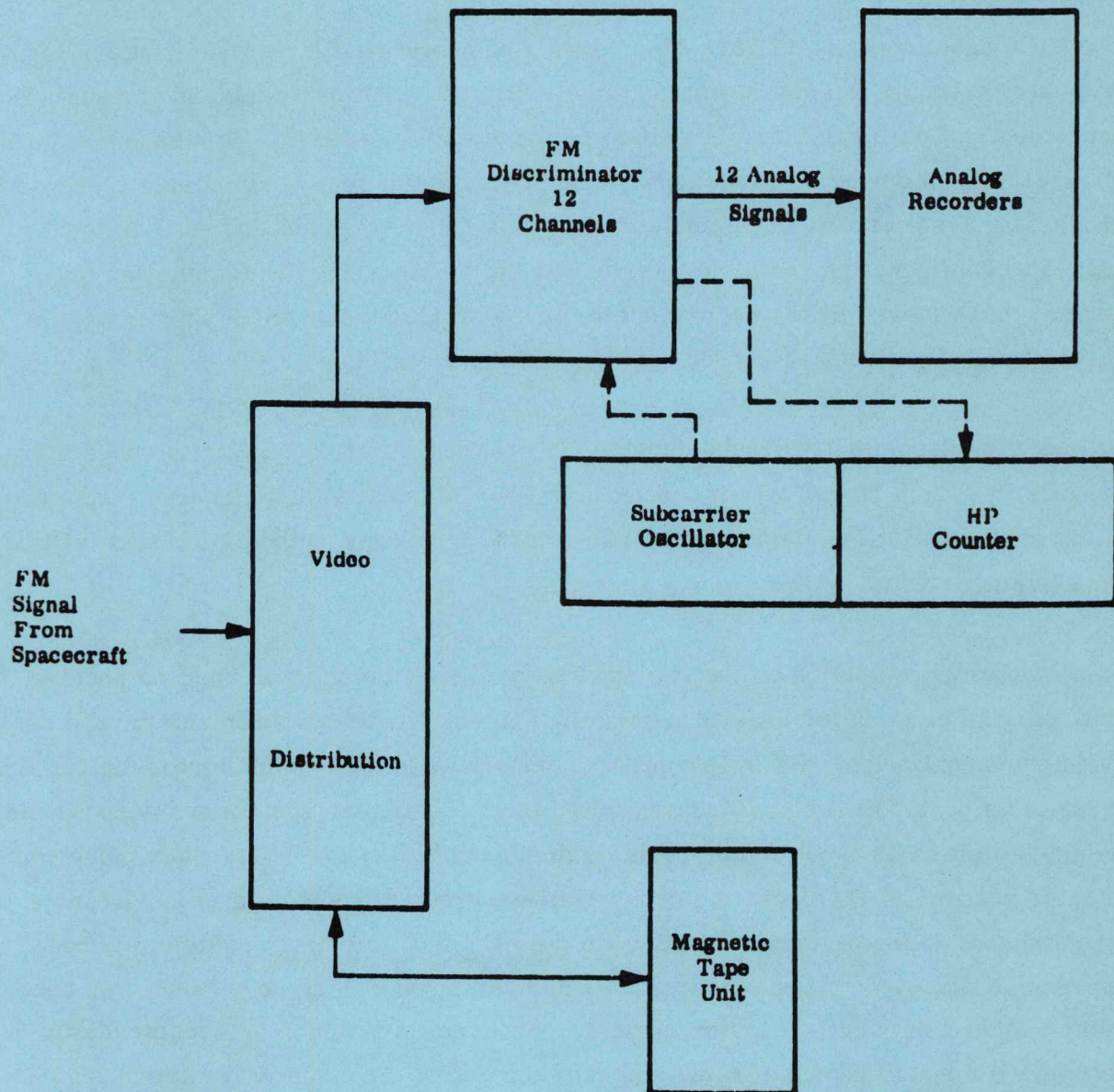


Figure 3. FM Group

control unit. The inputs of the remaining five discriminators are also tied in parallel and receive a composite FM signal containing five subcarrier frequencies from the signal separator assembly located in the video distribution and tape transport control unit. These signals received from the ACE-S/C system are AMR B-1, IRIG B, countdown time, voice, and a recorder reference signal.

PCM DECOMMUTATOR

The PCM decommutator (Figure 4) is capable of operating over a wide range of input telemetry data and can also accept a variety of types of PCM coding and various arrangements of parameter data specified by the telemetry system. To meet the demands of versatility in operating range and the requirements of recording, display, and data processing systems, the decommutator operates under program control. In the ACE-S/C configuration, both the interleaved and the airborne decommutation programs can be stored by the decommutator memory simultaneously. This gives the capability of rapid acquisition for each type of input available.

Although the decommutators are capable of versatility, only the operation pertaining to the ACE-S/C application will be mentioned. The interleaved and airborne inputs are of the configurations explained in the paragraphs pertaining to the digital test measuring system.

To obtain synchronization on the incoming data, the decommutator must be programmed with the criteria for bit synchronization, prime frame synchronization, and major cycle synchronization. Bit synchronization exists when the decommutator defines the exact same period of time as was generated by the telemetry system and decodes the weighted digit in its true form. Prime frame synchronization exists when the decommutator recognizes the beginning of a repetitive group of coded bits which divide a given amount of time into equal parts. In the ACE-S/C telemetry system this code appears 50 times per second; therefore, the system divides a one-second time span into 50 equal parity units. Major cycle synchronization is when the decommutator recognizes a specific prime frame and can then define the same real-time second as generated by the telemetry system. After completing these three steps of synchronization the decommutator memory is synchronous with the input data; therefore, the decommutation process can be initiated.

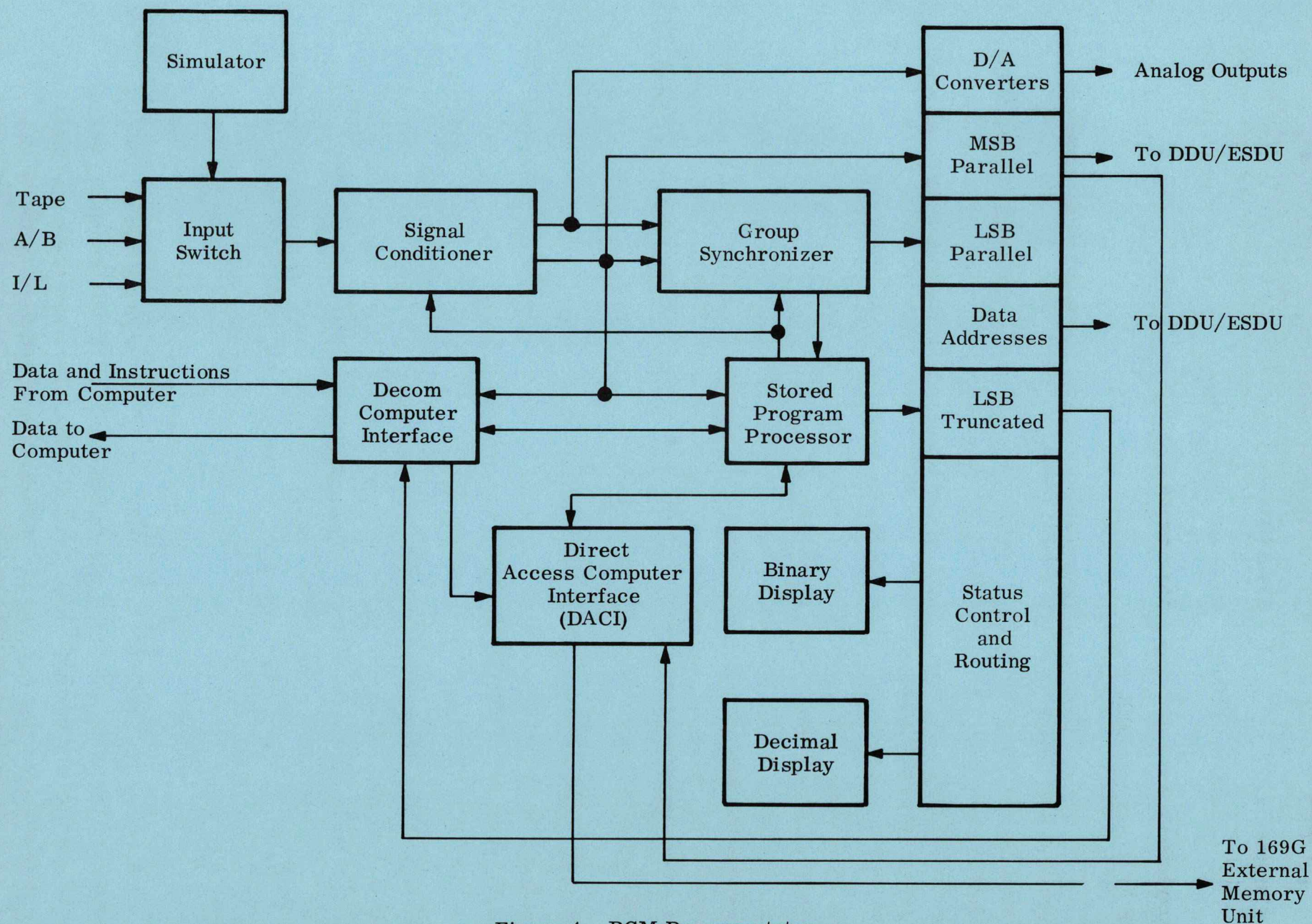


Figure 4. PCM Decommutator

The basic parts of the decommutator are the signal conditioner, the group synchronizer, the stored program processor (memory), the output rack, and the decom/computer interface (normal and DACI). All operate under program control of the particular program in operation.

SIGNAL CONDITIONER

The PCM signal conditioner (Figure 5) accepts the incoming split-phase pulse code modulated telemetry signal, conditions the pulses, and synchronizes with each bit to control the decommutator timing. The signal conditioner acts upon the incoming PCM signal to restore the data to a ground level and provide a stable output for the entire decom. This is performed to enable more efficient decommutation by the remaining sections of the decommutator.

Decommutation of the incoming PCM data can only be performed if the decommutator timing is synchronized with the bit rates of the commutation processes. Therefore, various time slots containing discrete words can be processed or decommutated to reproduce the exact data used in modulation during the commutation of the spacecraft parameters. The input signal to the decommutator when used in the ACE-S/C capacity is split, phase-C PCM data. This input signal is then converted to NRZ-C and RZ-M with the NRZ-C being sent to the frame synchronizer.

The signal conditioner consists of three principal subsystems:

- a. A dc restorer.
- b. A bit synchronizer.
- c. A bit detector.

The dc restorer accepts the serial data train as an input and supplies level-restorer signal to the bit synchronizer and bit detector. The bit synchronizer outputs are a clock at the bit rate of the data and timing signals from the system. The bit detector accepts the clock timing signals from the bit synchronizer and the data train from the dc restorer. It then produces reconstructed serial NRZ-C digital data as an output. Thus, the bit detector performs the basic decision of whether a binary "one" or "zero" exists for each bit.

For split-phase data, the clock defines only the carrier frequency although the bit location is subject to an ambiguity. The bit detector resolves this ambiguity, locates the bit position, and makes the bit polarity decision. The phase decision is made on the basis of several bits to reduce the probability of an error as a result of noise and

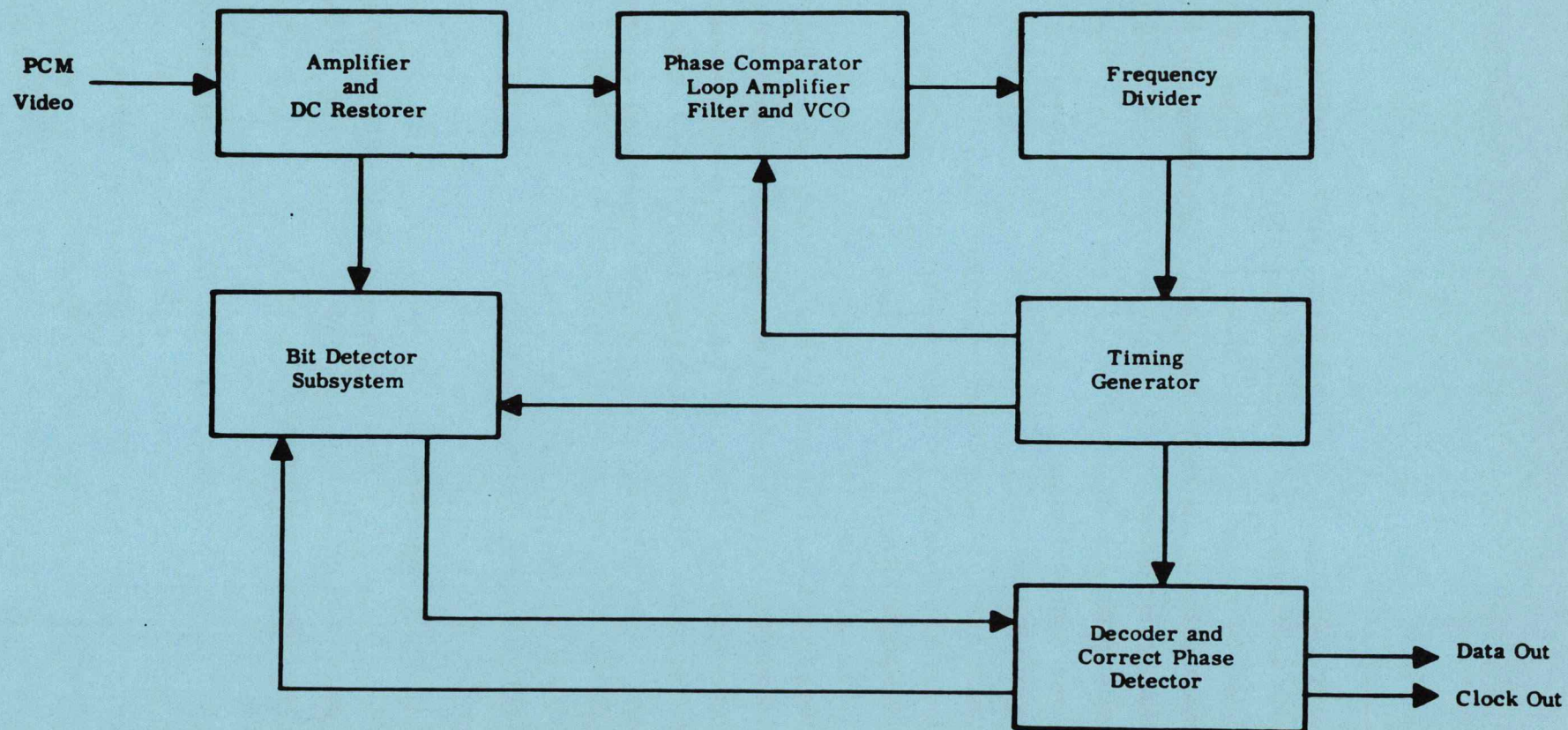


Figure 5. PCM Signal Conditioner

uses as criteria the definition of SP-C data where two adjacent half cycles of a bit period are never equal.

GROUP SYNCHRONIZER

The group synchronizer performs two different types of synchronization. First, it must establish prime frame synchronization and then major cycle or ID synchronization. The information used as criteria to perform these functions must be programmed in memory and callup as instruction for the synchronizer as follows:

- a. Prime frame length.
- b. Prime frame pattern.
- c. ID counts up or down.
- d. Location of ID word.
- e. Number of errors accepted in synchronization.
- f. Number of prime frames to be checked.
- g. ID MSB/LSB first.

The serial data from the signal conditions is shifted through a shifter register (accumulator) of the frame synchronizer (Figure 6) where a bit-by-bit comparison of the input data is made with the pattern and length placed in storage after memory callup. When the pattern of the prime frame sync word (32 bits in ACE-S/C) matches the stored pattern, a first prime frame sync signal is generated and enables the check mode of operation. Heretofore, the synchronizer has been in the search mode looking for a correlating pattern. This first prime frame sync signal not only enables the check mode but informs memory that a pattern has been found. Since it is highly possible that a sync pattern can be found any place in a prime frame with an arbitrary group of data bits, memory must instruct the frame synchronizer where the next pattern is located. To do this, it generates a signal call operative which enables a prime frame sync pulse to be checked the next time it should appear. If the first sync pulse was a valid one, then the next prime frame sync pulse should fall within the operative; however, if the first sync pulse was invalid, it is extremely unlikely that at the same time in the next frame an arbitrary group of 32 bits will match the pattern and generate a sync pulse; therefore, the pulse would not fall within the operative and would generate an error. If this exceeds the number of errors allowed, then the system returns to the search mode to obtain the proper sync word.

After the proper sync word is obtained and the check mode entered, the synchronizer checks the sync word with the pattern a predetermined number of times to establish

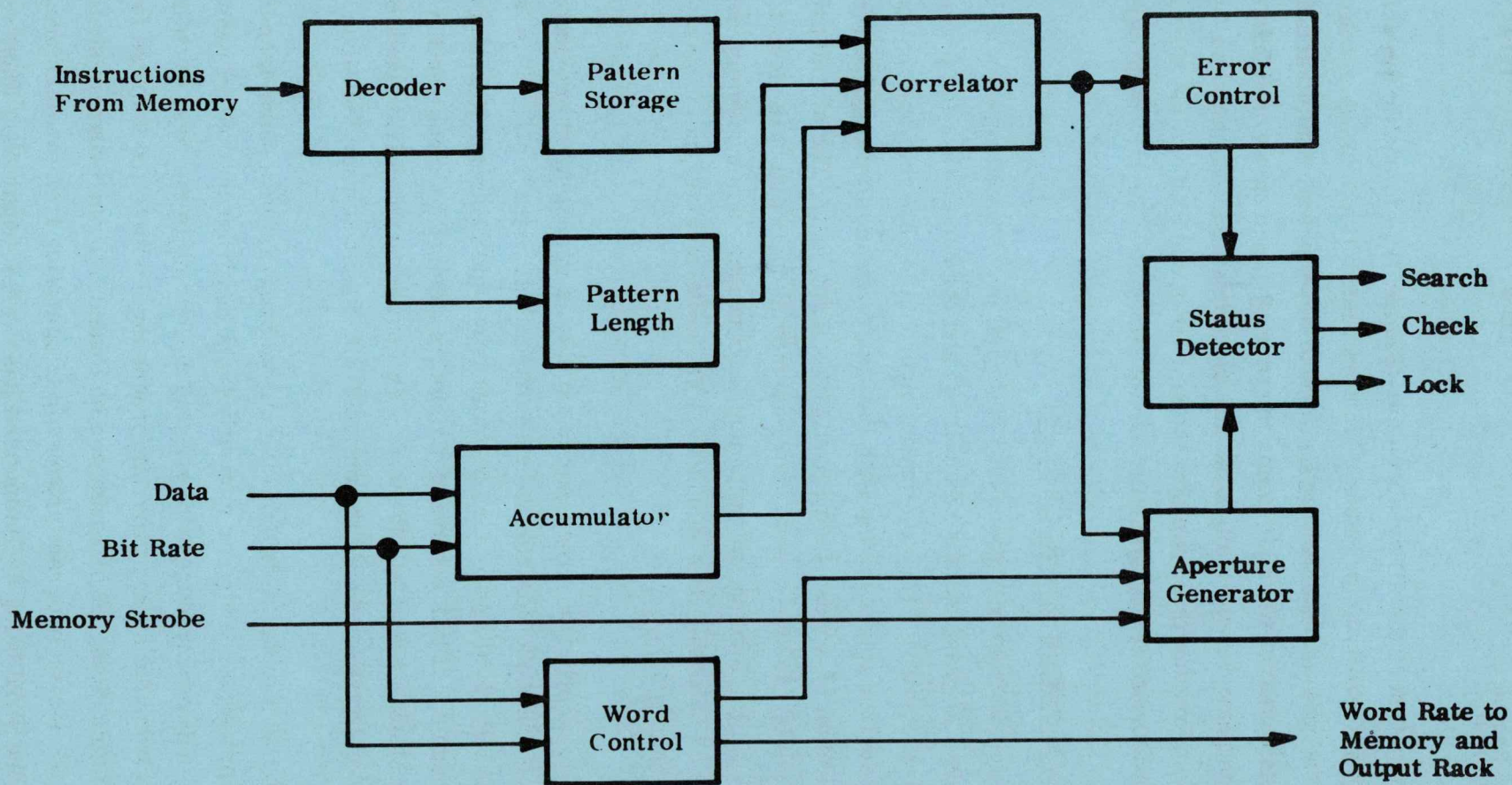


Figure 6. Prime Frame Synchronizer

that proper synchronization has been obtained. After this mode, the ID synchronizer is enabled.

The function of the ID synchronizer (Figure 7) is to enable the unit to begin decommutation as readily as possible. Memory instructs the group synchronizer where the ID word occurs and enables the ID word to be detected. This detected word is sent to memory control where it jumps the memory sequence to the prime frame detected. At this point, major cycle sync has been obtained. Each prime frame contains an ID word and during this time slot the new ID is checked against the updated contents of the synchronizer. If these two do not correlate, the ID synchronizer returns to search.

STORED PROGRAM PROCESSOR

The stored program processor (Figure 8) provides storage for key instruction words used by the group synchronizer DACI and the output rack for processing data under program control. It also stored synchronized code information that enables the group synchronizer to get in step with the data train and to reacquire synchronization with a minimum of words of synchronization being lost. The stored program processor consists of random-access, core-memory, input/output devices for formatting, control logic for loading and unloading instructions, and a memory control panel for entering or selecting data manually. The core-memory has a storage capability for 8192, 40-bit words.

The stored program processor is capable of operating on one decommutation program while loading another into the memory on a priority basis. This is accomplished by arbitrarily dividing the core memory into eight program stored sections designated 1 through 8. If this arbitrary division is adhered to, each section of memory is capable of storing 1024, 40-bit words. Of course, it is entirely possible to have only one or two programs take up the entire 8192, 40-bit storage locations.

A program can be loaded into the stored program processor from a digital computer, the paper tape reader, or manually from the program control panel. For the program entry, a three-bit address for starting the loading is the first word in a given program. Thereafter, the stored program processor modifies the address for sequential loading of memory slots. A program can be loaded into one program section of memory, while the stored program processor is operating from another program section, provided the word being decommutated has a word length of at least seven bits.

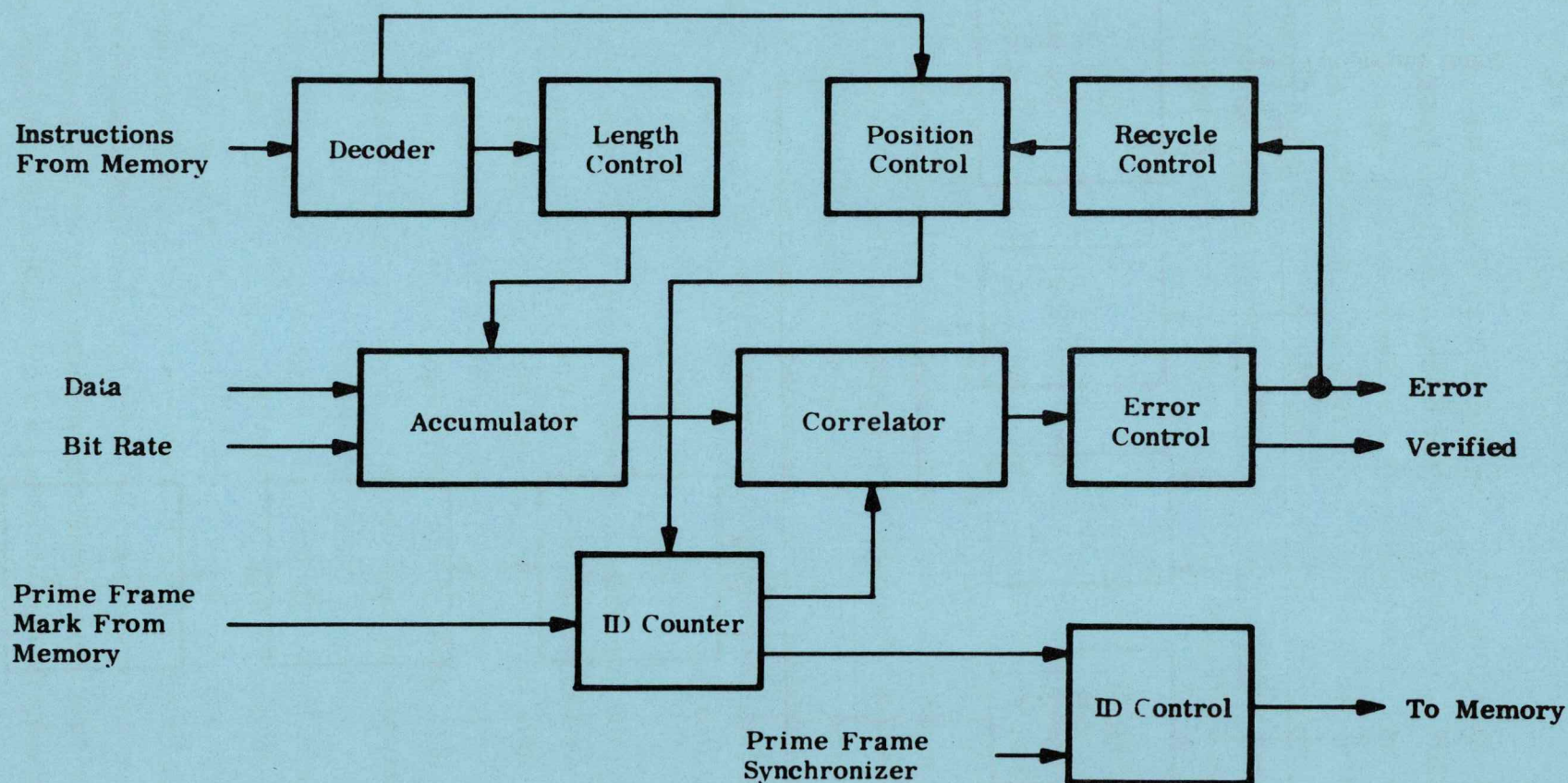


Figure 7. ID Synchronizer

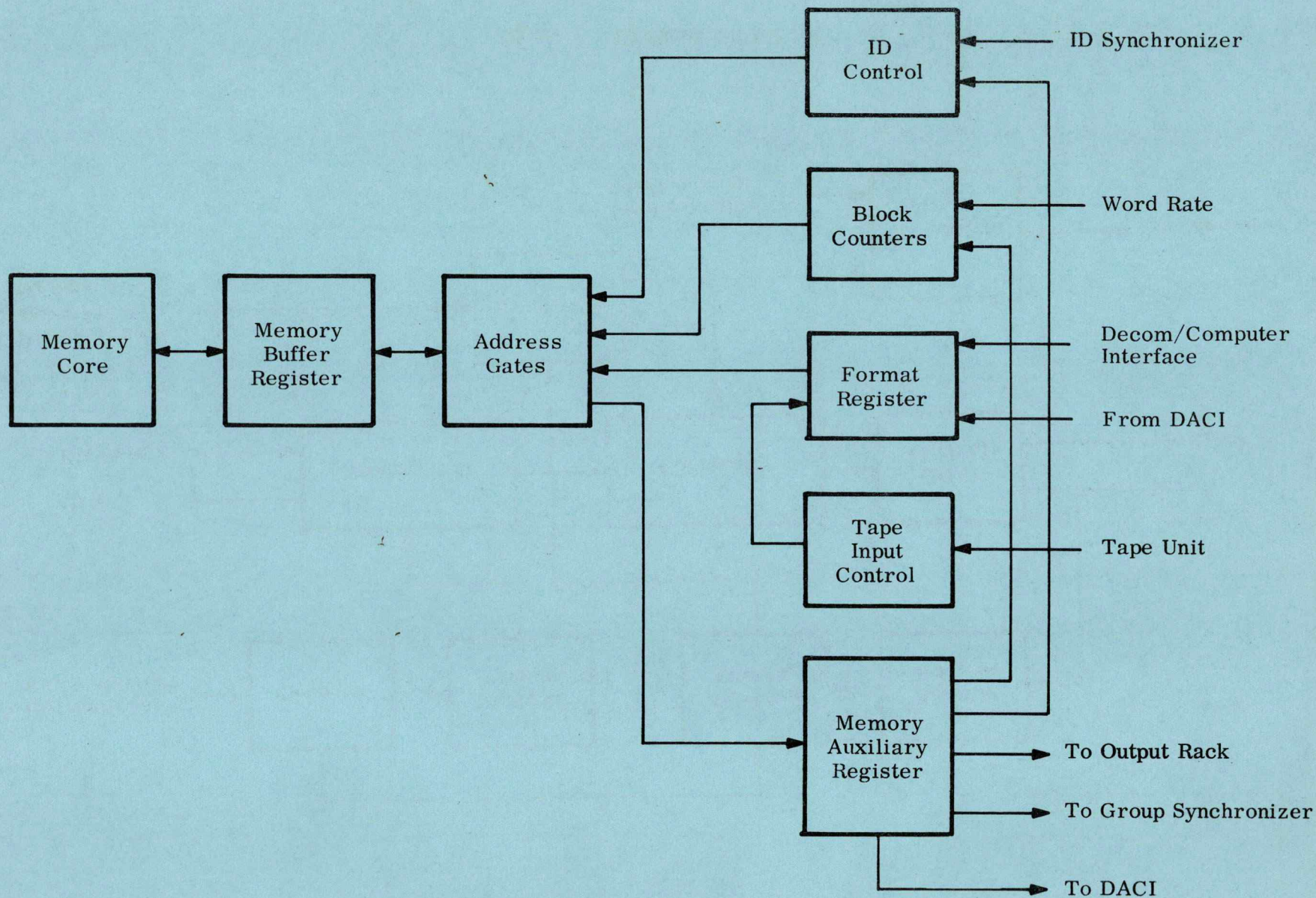


Figure 8. Stored Program Processor

Program instruction words from a computer and the paper tape reader are formatted into the instruction word format used by the stored program processor. If the instruction word is from a computer, it is furnished in the form of four words or characters, one 4-bit and three 120-bit words or characters. The words or characters are formatted into a 40-bit word by the formatting gates and the 40-bit word is loaded into the data register. Word formatting is controlled by the format counter and decoder. This functional area pulses the correct set of formatting gates based upon the number of words or characters transferred. For the first four-bit word or character transferred from the computer, the format counter pulses the first four most significant bit formatting gates. It notes the fact that a word has been transferred and when another word is ready, pulses the next set of formatting gates (corresponding to the 12 next most significant bits of the instruction word). Upon completion of word formatting, the word is transferred to the core-memory register by the master load gates. The word is subsequently stored in the address designated by the program. When this word is stored, the computer sends another instruction word, load/unload counter modifies the address, and another word is stored in the next sequential address of the memory. The process continues until a complete program is loaded.

A similar process is required for loading instruction words from the paper tape reader. The starting address for program loading is the first word on the tape. The tape reader furnishes input words in the form of one four-bit word or character and six 6-bit words or characters. These input words are formatted and stored in the memory by the same process described for computer inputs. The process continues until a completed program is loaded. Instruction words entered from the program control panel do not require formatting. The starting address for storing the words is manually entered at the program control panel. Thereafter, the load/unload counter modifies the address for sequential loading of the memory. No manual loading can be performed during decommutation; however, the address of stored instruction words can be changed using controls on the program control panel.

During the entire loading process, each 40-bit word is checked for parity and if an odd number of "ones" exists in the formatted word, a "one" is added in bit position zero. Thus, the stored program processor incorporates "even ones" parity.

The stored program processor operates in two basic modes - preacquisition and decommutation. In the preacquisition mode, all the criteria is called out of memory and is the criteria for memory control in the same manner discussed in the synchronizer.

Memory is controlled during the decommutation process by block counters which are jammed to the starting addresses of the data contained in prime frame one and prime frame two of the telemetry input format for a particular program. These block counters fall into two categories, ID and control and routing (Figure 9). When the ID word is verified, the ID block counters cause the block counters used for control and routing to be jammed to the address of the prime frame when major cycle synchronization is found. At this time, the exact location of every word is known in the major cycle.

The control and routing format contain instructions for memory control and the formatting process performed by the output rack. The next block instruction causes the block counters to access the next memory location applicable to the incoming data word. The instructions contained in a memory location are for the next incoming word. Therefore, the decommutator operates one word time ahead of the incoming data.

OUTPUT RACKS

The output format devices (Figure 10) are used to convert the NRZ-C data into the proper format determined by the equipment to receive the data word. The gating of the data words into the proper output register is determined by the program in the stored program processor. The output format control unit receives serial reconstructed NRZ-C data from the output of the PCM signal conditioner, timing from the group synchronizer, and program control instructions from the memory. The output format control unit provides analog and digital data outputs to the external units. Parallel binary and binary-coded-decimal (BCD) data are also provided to data displays on the system control panel, which gives the operator the capability of displaying any incoming data word in its time binary or decimal value.

The outputs of the digital-to-analog converter circuit are routed to the event distribution and recorder patching unit to be distributed to the analog recorders located in the computer room. The data routed to the downlink computer comes from the least significant bit truncated register and DACI where they are transferred as 12-bit and 30-bit parallel data words respectively. The data transmitted to the decommutator distribution and event storage and distribution unit, in the control room, are routed through the MSB parallel register. The addresses (from memory) applied to the data of the MSB parallel register are routed through the data address register. The remaining output devices are not used in the application with ACE-S/C.

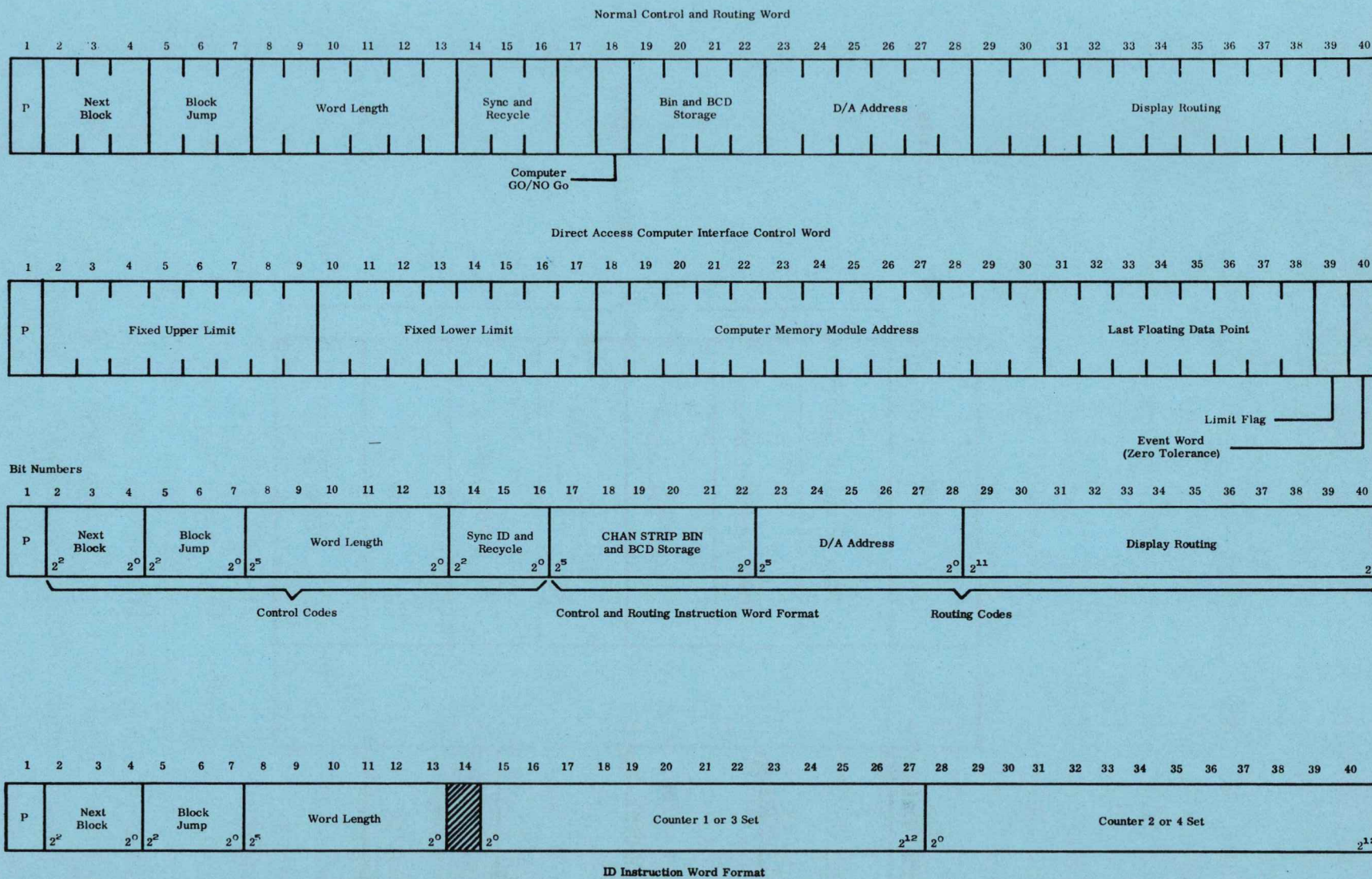


Figure 9. Program Word Formats

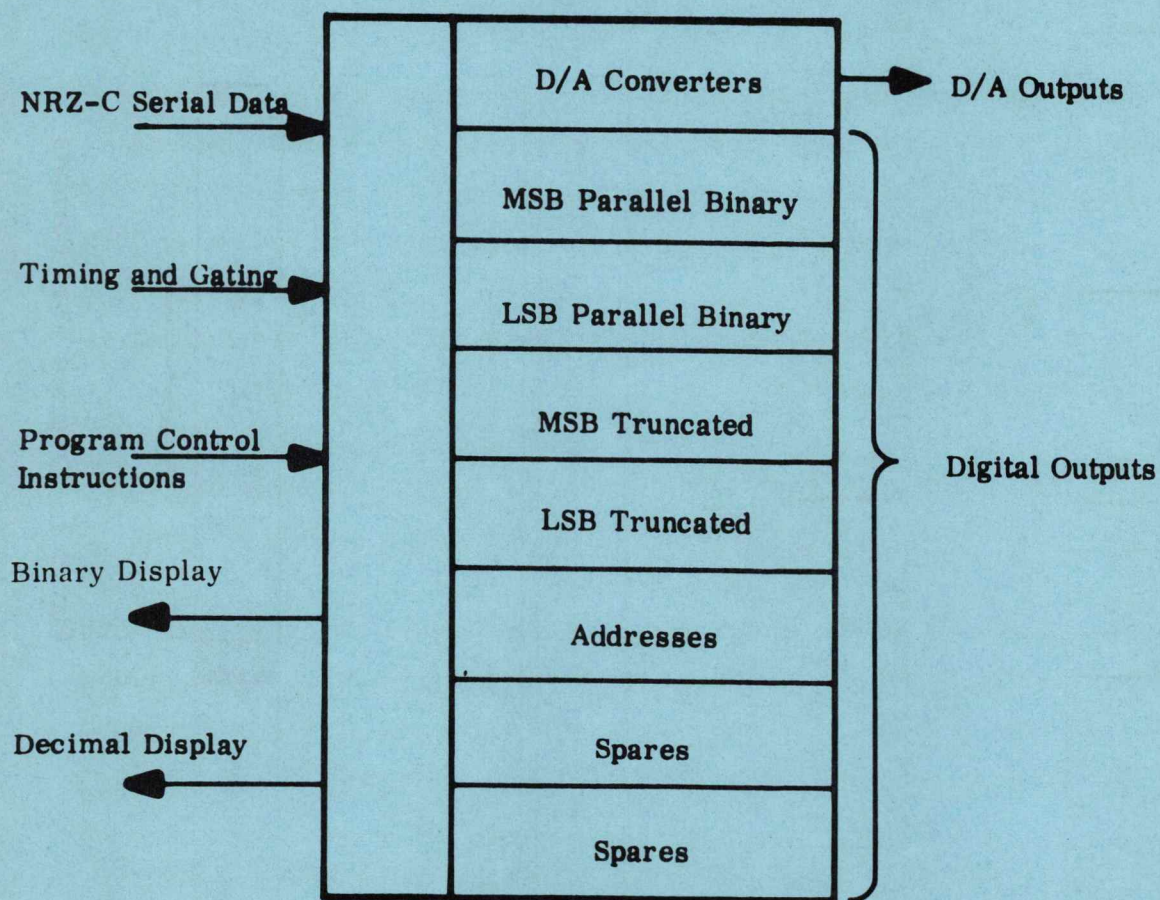


Figure 10. Output Devices

DIGITAL-TO-ANALOG CONVERTERS

The digital-to-analog (D/A) converters convert the incoming digital data to analog voltages to be distributed to the event distribution and recorder patching unit. The decommutator contains a total of 60 D/A converters of which 40 are used in the transmission of data to the recording and patch unit. The D/A converters are selected by the stored program processor. The memory instruction performs three functions in controlling the D/A devices:

- a. Controlled designation of which D/A will convert the incoming data word.
- b. When the D/A will be selected.
- c. Synchronization of gating the incoming data into the converter.

MSB/LSB PARALLEL OUTPUTS

The function of this group is to provide as an output all data words in both MSB and LSB first formats at the same time. Any data word may be from 4 to 64 bits long. The different conditions under which the registers can accept data are:

- a. No parity or word synchronization code bits in the data word and either MSB or LSB first.
- b. Parity and word synchronization code bits present in the data word either at the beginning or the end of the word and either MSB or LSB first.

The program of the system being monitored dictates the mentioned conditions. The data is serial when received and is converted to parallel by a formatting process.

After the entire word has been formatted, the down data word is shifted left the number of places corresponding to the number of parity and word synchronization code pulses contained in the word. The action takes place if word parity and word sync are used. In the ACE-S/C application, word parity and word sync are not used.

The MSB formatting and parallel registers are composed of 33 stages while the LSB formatting and parallel registers are composed of 64 stages. The reason for this is that it is only necessary to acquire one more MSB bit than half the word length to determine the value of the measurand while the entire word in LSB form must be gathered to determine which bits are the MSB of the word.

Also contained in the MSB/LSB parallel registers logic is the 12-bit display address register which feeds the ESDU and the console control logic circuits. This address

with a read pulse is gated out in parallel with the contents of the MSB/LSB parallel registers.

MSB/LSB TRUNCATED OUTPUTS

Truncate means to cut up or cut off. Truncation circuitry is used when the decommutator operates in conjunction with 160G computer. If the incoming data word is too large, the truncated output will be in characters whose lengths are compatible with the computer input. This allows the decommutator to maintain its versatility and still allow the remaining units of the ACE-S/C system to function at their specific capability. The MSB/LSB truncated unit operates basically identical to the MSB/LSB parallel unit with the exception of a calculator which divides the incoming word by a factor of two until a remainder is obtained. This remainder is outputted as the first truncated character which will vary in length with varying lengths of incoming data. However, the remaining characters will all be the same dependent upon the initial size of the incoming data word.

The ACE-S/C application utilizes the least significant truncated circuits and outputs the data words to the decommutator/computer interface unit.

DECIMAL AND BINARY DISPLAYS

Three decimal displays and one binary display provide the capabilities for selecting and displaying the decimal and binary values of words from registers in the output racks.

The three decimal displays operate independently; that is, all three can be used concurrently to select and display one word or three different words. Any word in the data train up to octal 7777 (decimal 4095) can be selected on any one display. The decimal displays are wired for word values up to 999,999; however, the displays only contain modules for word values up to 999.

The binary display provides the capabilities for selecting and displaying any of 4095 data words. A 64-bit word plus parity can be displayed. In addition, word synchronization is also displayed.

The decimal and binary displays function identically, except for the fact that the decimal displays must decode the BCD inputs. The decoding operation performed for decimal displays can be ignored when evaluating the operation of the binary display.

DECOMMUTATOR/COMPUTER INTERFACE

The computer interface unit is designed so that a free interchange of data and instructions can be carried on between the Radiation Series 540 PCM acquisition and stored program decommutation system and a digital computer. The unit converts the logic level of the computer to that required by the computer. The unit also decodes the various instructions from the computer and causes the decommutator to comply with them. In addition, the unit provides a path through which a complete program can be inserted into the decommutator memory or an existing program can be modified or checked. All interchange between the computer and the computer interface unit is performed by parallel transfer.

The decommutator sends two types of words to the computer through the computer interface unit. Both types of words are sent upon request of the computer. The two types are truncated data words (characters) with a maximum of 12 bits per character and a status word. The truncated characters are routed from the decommutator LSB truncated character register through the computer interface unit which converts the logic levels to be compatible with that required by the computer. The status word is partially generated within the decommutator and tells the computer the status of the decommutator at the time of receiving the request from the computer.

All data transferred into the computer memory from the decommutator and all data transferred from the computer into the decommutator memory must be under the direct and complete control of the computer program. The decommutator can be synchronized on the incoming data train and, in effect, to the entire decommutation process. However, no data is transferred through the interface unit until requested by the computer. Initiation of this transfer is effected by control words and control functions generated by the computer.

DIRECT ACCESS COMPUTER INTERFACE (DACI)

The DACI is essentially in parallel with the decommutator normal interface circuitry (Figure 11) and enables the ACE-S/C decommutator to input addressed data directly into the 169G external memory unit. The decommutator output circuitry (normal or DACI) will be selected by the preacquisition block of the decom program. The DACI is then enabled by the 160G downlink computer. The decommutator control and routing

words defines which PCM words are to be transferred to the 169G. The information transfer from DACI to the 169G will be as follows:

- a. 17 address bits: 4 Memory bank select
13 Memory address
- b. 13 data bits: 8 Data
2 Blank
3 Flags

The decommutator also has the capability to perform parameter limit checks, floating point checks, and event transition checks (Figure 12). The limit checks are performed on the upper and lower parameter values for each PCM word determined by the loaded decommutator program. The values for the upper and lower limits are predetermined and are preprogrammed into the decommutator memory prior to testing. Thus, the values provide unique checking for each telemetry word input into the PCM decommutator system.

The floating point check is performed on those parameters where the change is of significance rather than the exact upper or lower values. In this capability the last known value of a parameter is used as the next point of reference, thus the floating point technique. The event transition checking is performed in the same manner as the floating point technique in that the last event word input from the telemetry system is used as the next reference.

A flag is sent to the computer as part of the data word (Figure 13 bits 10, 11, 12) to tell the computer any time the limit check or floating point check was out of tolerance.

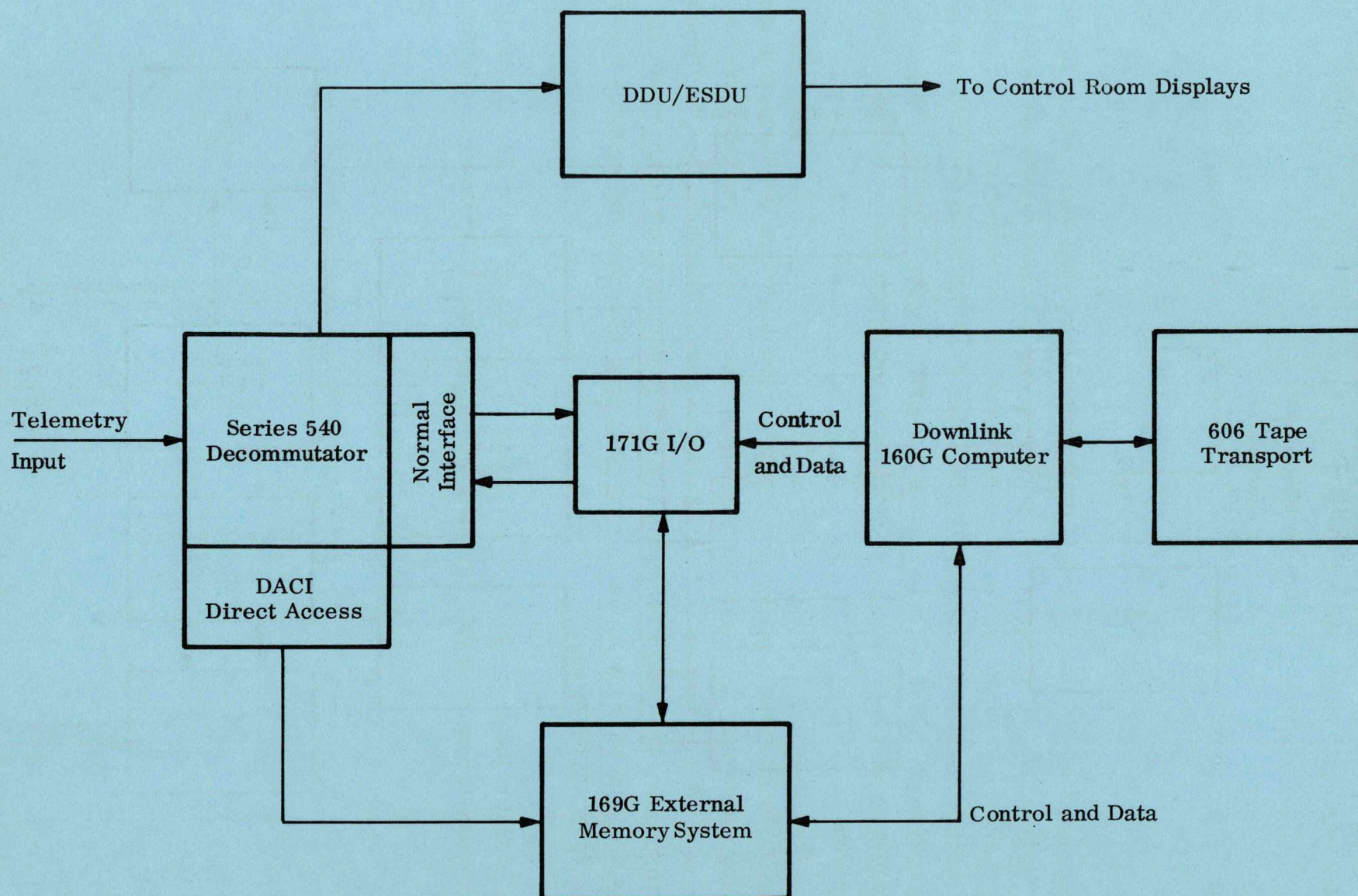


Figure 11. Interconnection Diagram

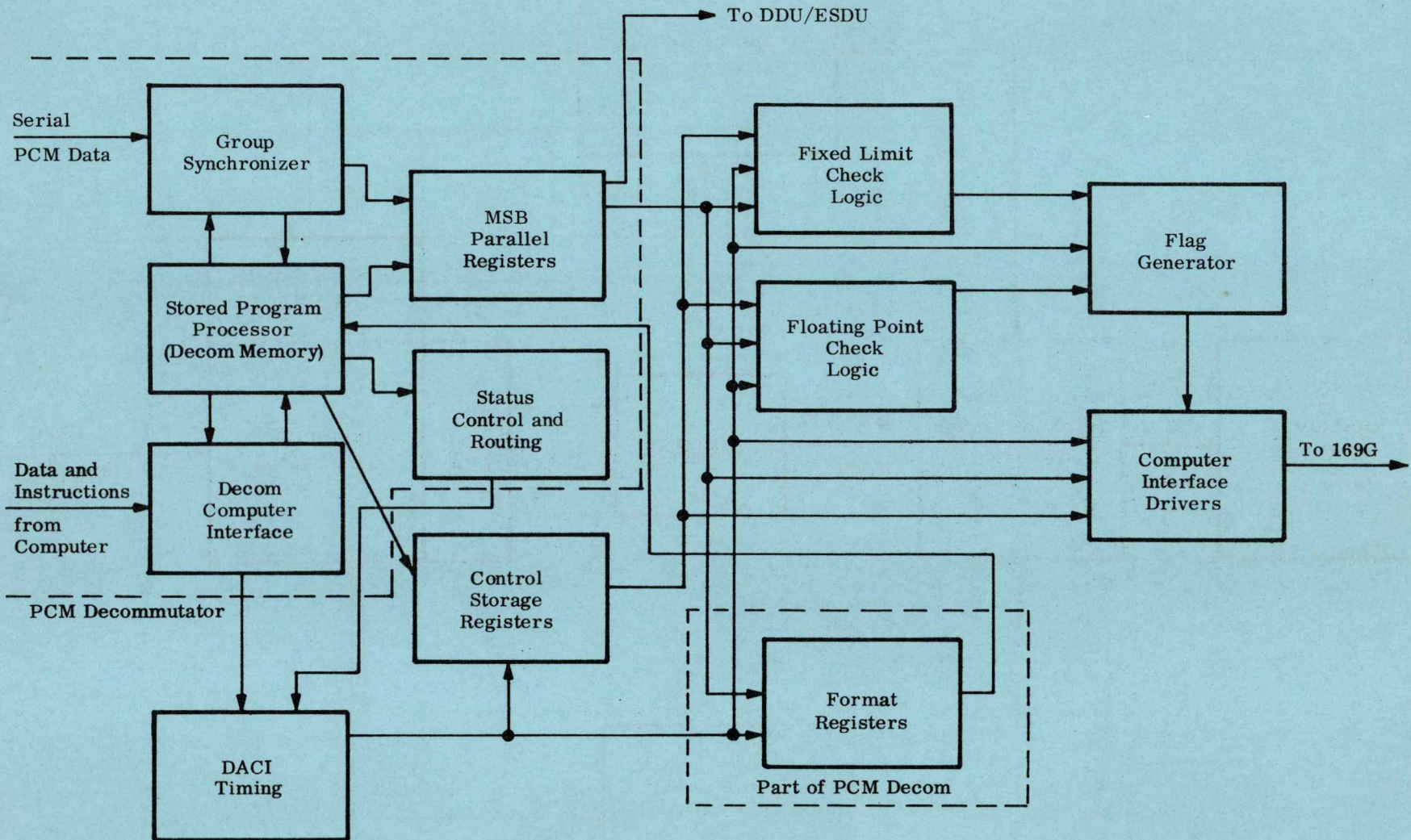


Figure 12. DACI/Decommutator Interface

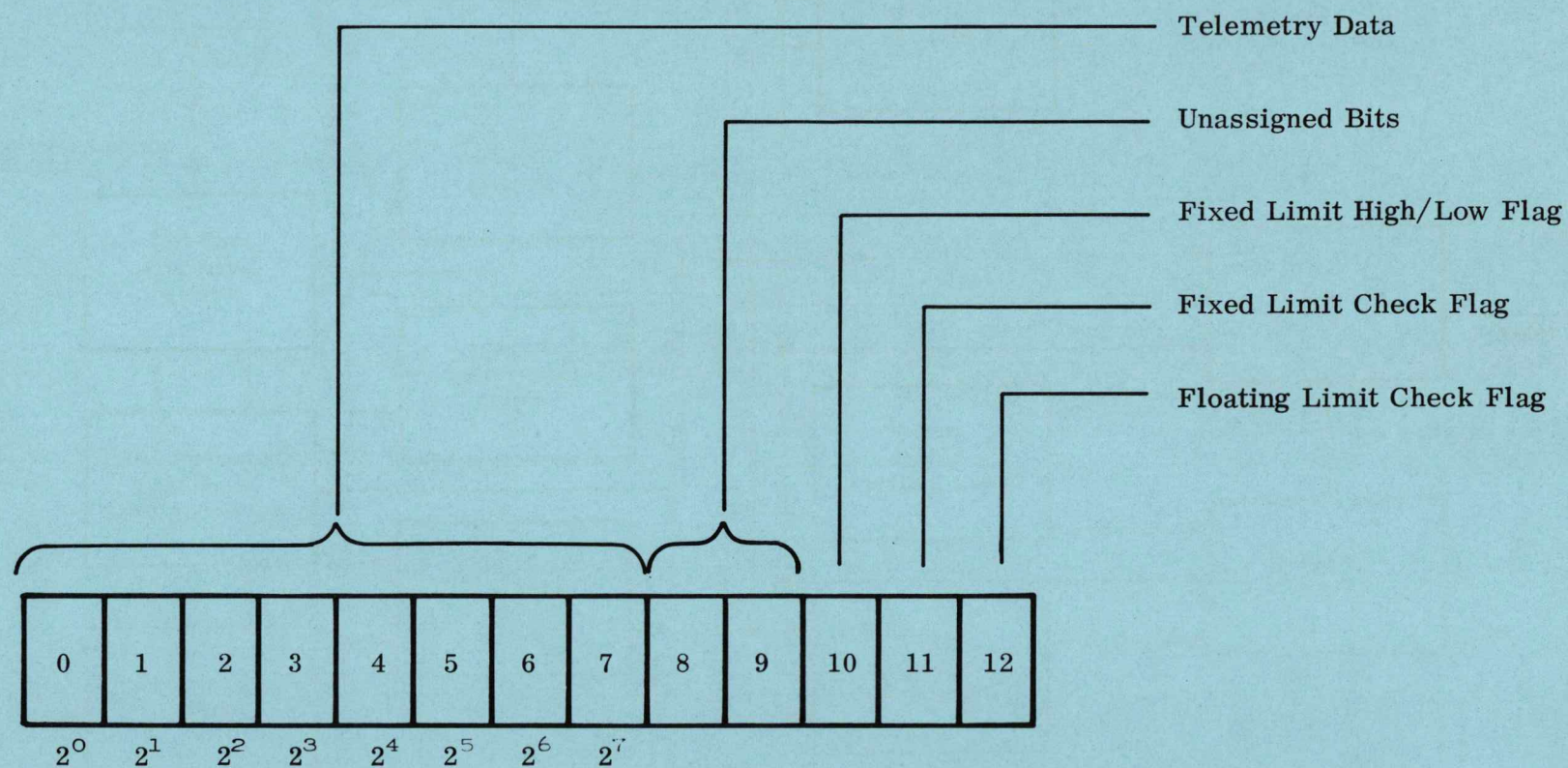


Figure 13. Computer Word Format

DISPLAY COMPUTER

OBJECTIVES

To familiarize the student with:

- a. Data inputs.
- b. Limit comparison.
- c. Generation of engineering units.
- d. Problem solving.
- e. Programing.
- f. Downlink programs.

INTRODUCTION

The display computer is a stored-program, high-speed, single-address, parallel-operation, modular, electronic data processor that has the same operating characteristics as the uplink or command computer. The primary functions of the display computer are data reduction, analysis, and preparation for display of test data derived from spacecraft tests.

The display computer receives raw data in the form of event and analog words from the decommutator units via a 171G input/output module. The computer performs the following functions in processing this data:

- a. Formatting of the data for processing.
- b. Comparison of words with programed values to determine whether the data is within predetermined limits.
- c. Conversion to engineering units.
- d. Comparing event status with previous status.
- e. Preparing and formatting processed data for display.

After the input data has been processed and formatted, the display computer selects the downlink DTVC and then transfers the parallel data words to the DTVC for transmission to the Symbol Generator and Storage (SGS) Unit. The local DTVC operates in conjunction with a Digital Communications and Control Unit (DCCU) to provide a data transmission path to the display producing unit. The processed data received by

the DCCU is then transferred to the SGS. The SGS stores the incoming data and converts the data into alphanumeric characters for display on the requesting CRT modules.

The incoming PCM test data is stored in computer memory and is then processed in preparation for display on an alphanumeric CRT display unit. Processing of the incoming PCM data includes:

- a. Selection of specific data from the incoming data.
- b. Comparison to determine whether the measurement represented by a digital word is within preprogramed limits.
- c. Conversion to engineering units.
- d. Conversion and formatting test data for display.
- e. Storage of selected parameters for trend analysis, etc.

In addition to driving the alphanumeric CRT displays, the display computer also supplies a number of peripheral units with processed data. The peripheral units include a high-speed printer, an X-Y plotter, tape unit, card punch, and a typewriter. These units can be used for the setup and checkout of the computer complex in preparation for a spacecraft testing sequence, as well as to provide a display and recording capability during the actual test operations. The general functions and operations of the display computer are best described in terms of the computer program.

The Supervisory Executive Program (SEP) organizes the display computer (as well as the command computer) program in preparation for processing test data. The SEP is recorded on a test file tape, along with certain common programs (such as ACE-S/C self-test programs), and all display executive programs that are part of a test series, spacecraft test subroutines, and test parameters. The test file tape may be placed on a command computer tape unit. The command computer then interrupts the display computer by means of a SEP bridge punched card placed in the display computer card reader. The SEP portion of the test file tape then selects a display computer executive program and loads its appropriate subroutines and parameters into the display computer memory. Prior to or during loading, any display computer parameter on the test file tape may be changed by using change cards. Changes called for by the change cards are not limited to load time but may be made at any point during the test sequence.

An ACE-S/C self-check program, included as part of the SEP, is readily accessible to the display computer. This self-check program provides the assurance that the

required ACE-S/C subsystems are in the ready mode prior to the actual test run and that they have the proper operational status while a test is in progress. Indications of a no-go nature are provided by this program, along with sufficient additional information to enable program callup of selected diagnostics for prompt decision as to corrective actions.

It is the purpose of the executive routine to control the sequence of data processing by the display computer. This routine may be divided into three major sections:

- a. Primary initialization.
- b. Subroutine linkage.
- c. Summary filing.

Primary initialization insures that all registers, counters, and other indexes used by the display computer executive routine are cleared and reset to the start conditions. This prepares the display computer for an interrupt from the decommutator units to commence the loading of PCM test data for subsequent processing. The subroutine linkage portions of the executive routine consist of fixed sets of instructions that control the exit from one subroutine and the entry to the next subroutine. By using the subroutine linkage instructions, the processing order is flexible and is easily changed, since only the linkage routines need to be rearranged to create a new and different subroutine processing order. Before the entry to a subroutine, the subroutine linkage instructions supply the new subroutine with the address of the first parameter for the data word to be processed by that particular subroutine. Upon exit from the subroutine, the linkage routine determines if there are any more data words to be processed by the subroutine and will cause the subroutine to repeat if necessary. Processed data, derived from display computer subroutine operations, is stored and transmitted to the appropriate peripheral units under the control of the summary filing portions of the executive routine.

In the following paragraphs, thumbnail sketches of some typical display computer subroutines are given. It is not the intent to list and describe every subroutine available in detail, but rather to demonstrate the function of the display computer in relationship to the alphanumeric display equipment and the overall ACE-S/C system.

The purpose of the PCM telemetry data subroutine is to allow the entry of PCM digital test data from the decommutator units into the display computer for processing (see figure 1). The data input sequence is initiated by an interrupt signal from the PCM

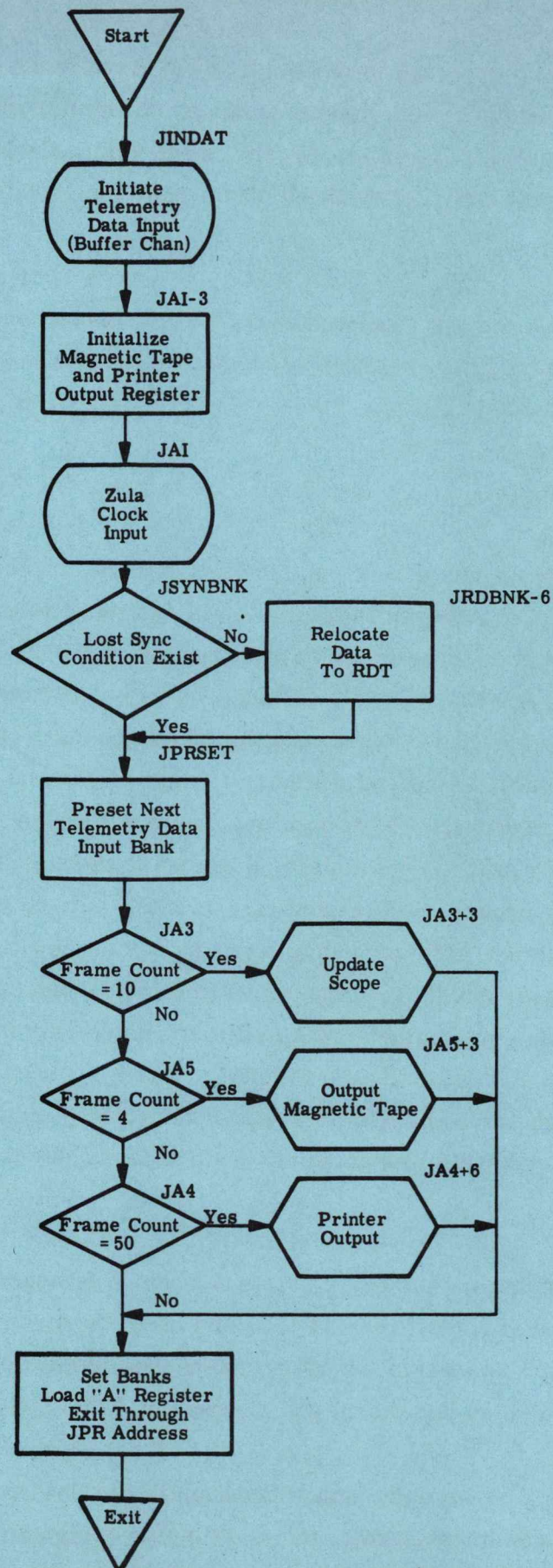


Figure 1. Buffer in Data Subroutine

decommutator equipment. The incoming PCM data, in the form of 8-bit parallel event and analog words, is buffered into two separate areas of auxiliary memory. One prime frame of PCM data (512 eight-bit words) is read in at a time. There are 50 such prime frames to be read in each second. The following steps are required for a typical read-in process:

- a. Read first prime frame of 512 words into memory area number 1.
- b. Begin read-in of second prime frame of 512 words into memory area number 2 and start processing data in memory area number 1.
- c. Begin read-in of odd-numbered prime frames of data into memory area 1 and start processing data in memory area 2.
- d. Input process continues, inputting 50 prime frames per second alternately into areas 1 and 2.

This switching type of buffer allows time to transfer selected data to be processed, from one input area to a relocatable data table, while filling the other input area. Identification of data to be transferred is based primarily on the PCM data prime frame count. This program subroutine tests for synchronization in the last input area to receive test data. If an in-sync condition exists, all data to be processed is transferred to a relocatable data table. If a lost-sync condition exists, the relocation of data is bypassed and a flag is set. A real-time clock reading is stored in the computer so that a specific time can be related to each data prime frame received.

The engineering units subroutine converts the received PCM test data to the proper engineering units, determining analog percentages, and make limit checks. The data is processed in one of three ways:

- a. Type A - the average of every Nth point.
- b. Type B - process every Nth point.
- c. Type C - process on significant change.

Prior to read-in of any PCM test data, all the necessary information required to convert the incoming PCM test data associated with a specific measurement will be read from magnetic tape and stored by the display computer. This information consists of a polynomial (or appropriate degree), the coefficient constants of the polynomial, the location of the binary points of the coefficients, the binary point of the upper and lower limits, and the specific upper- and lower-limit values. The polynomial and its associated coefficients are the mathematical expression for a curve to which the PCM data

is fitted. The general polynomial form is given as:

$$A_0 + M\{A_1 + M[A_3 + M(A_4 + A_5 M)]\}$$

where A_0 through A_5 are the coefficients and M is the 8-bit PCM data word associated with the measurements.

The display computer solves the polynomial expression and generates one 12-bit word. This 12-bit word is a solution to the polynomial expression and is in engineering units. The engineering units are appropriate for the measurement that was represented by PCM test data input. The engineering unit value for the measurement is stored and can be transmitted to the SGS for display on a CRT.

Following the conversion to the appropriate engineering unit value, the display computer may check this value against preprogramed limit tolerances. As previously stated, the specific upper-limit and lower-limit values of each measurement to be processed are read into the display computer prior to acceptance of any PCM test data. First, the measurement value is compared with the upper-limit value and then the lower-limit value. If the measurement value is within the tolerance limits, no further computations are made. If an out-of-tolerance condition is indicated, the display computer will flag the measurement value and cause this value to blink when displayed on a CRT.

Certain PCM data words are converted to engineering units and then only checked for an in-limits or out-of-limits indication. These measurement values are compared with the maximum and minimum values of operational limits in percent of full scale. The measurement values are compared, each time they are received, with the previous value to determine if they are going out of limits or coming into limits. Each time a measurement value changes status (goes out of limits or comes into limits), it is stored for transmission to the SGS and then to a CRT display.

The purpose of the event status check subroutine is to extract specific event information from certain incoming PCM test data words and to determine its state and disposition. Based on the bit position of the event, the display computer extracts the bit from the PCM data word. The computer then compares the state of this bit with the previous subframe state. If a transition has occurred, the present state (on/off condition), the time of transition, and a flag indicating that a transition has occurred are stored for output to magnetic tape recording and printout. The programmer also can

cause the present on/off condition to be sent to the SGS and then to a CRT display. If a transition has not occurred, the present state of the event will not be updated on the CRT display since the previous state is still valid.

The purpose of the output data for CRT display subroutine is to output (via an external buffer) the information required to update the SGS memory and thus the CRT displays. This subroutine is required for one of the following types of CRT displays:

- a. A display of the engineering units of a measurement.
- b. A display of a measurement requiring only an in-limits or out-of-limits indication.
- c. A display of an event requiring only an on/off or open/closed type of indication.
- d. The display of an event and the time of a transition of state occurred.
- e. The display of decommutator loss of sync or its removal.
- f. Any other display of parameters deemed necessary by the programmer to fulfill the current test requirements.

The data that the display computer has identified and processed is stored in the common output area of memory for scope updating as required. By means of a parameter table look-up, the stored parameters are identified fully and the CRT character code and positioning codes are prepared. The display will output the stored parameter values, CRT positioning codes, and any other instructions necessary for proper CRT displays as blocks of data. The blocks of data are groups of sequentially outputted 12-bit parallel words.

The purpose of the store information for periodic output subroutine is to store the processed data and its associated time codes, in/out limit indications, CRT display X and Y coordinates, status, and engineering unit values. This data is converted to a form appropriate for printing or plotting and is stored in a common output area. The data is also stored in the common output memory area in an unprocessed form for output to magnetic tape recorders. This data is transmitted to the appropriate peripheral units at the end of each prime frame (i.e., at the completion of processing 50 subframes), which occurs once every second.

The callup alternate CRT display data subroutine is used after each subframe is processed when a check is made by the display computer to see if a callup of alternate display data has been requested. When a callup has been requested and is recognized by the display computer, the time of callup is determined and is used to search for

the alternate displays requested. At the completion of the read-in of the alternate displays and the associated parameters and data, the new CRT character display codes are stored and transmitted to the SGS in the same manner as normal processed data.

Figure 2 contains flow charts of the downlink control program illustrating the various functions that are performed during the data input and processing cycles. Figure 1 contains a typical example of one of the subroutines utilized in the downlink data processing cycle.

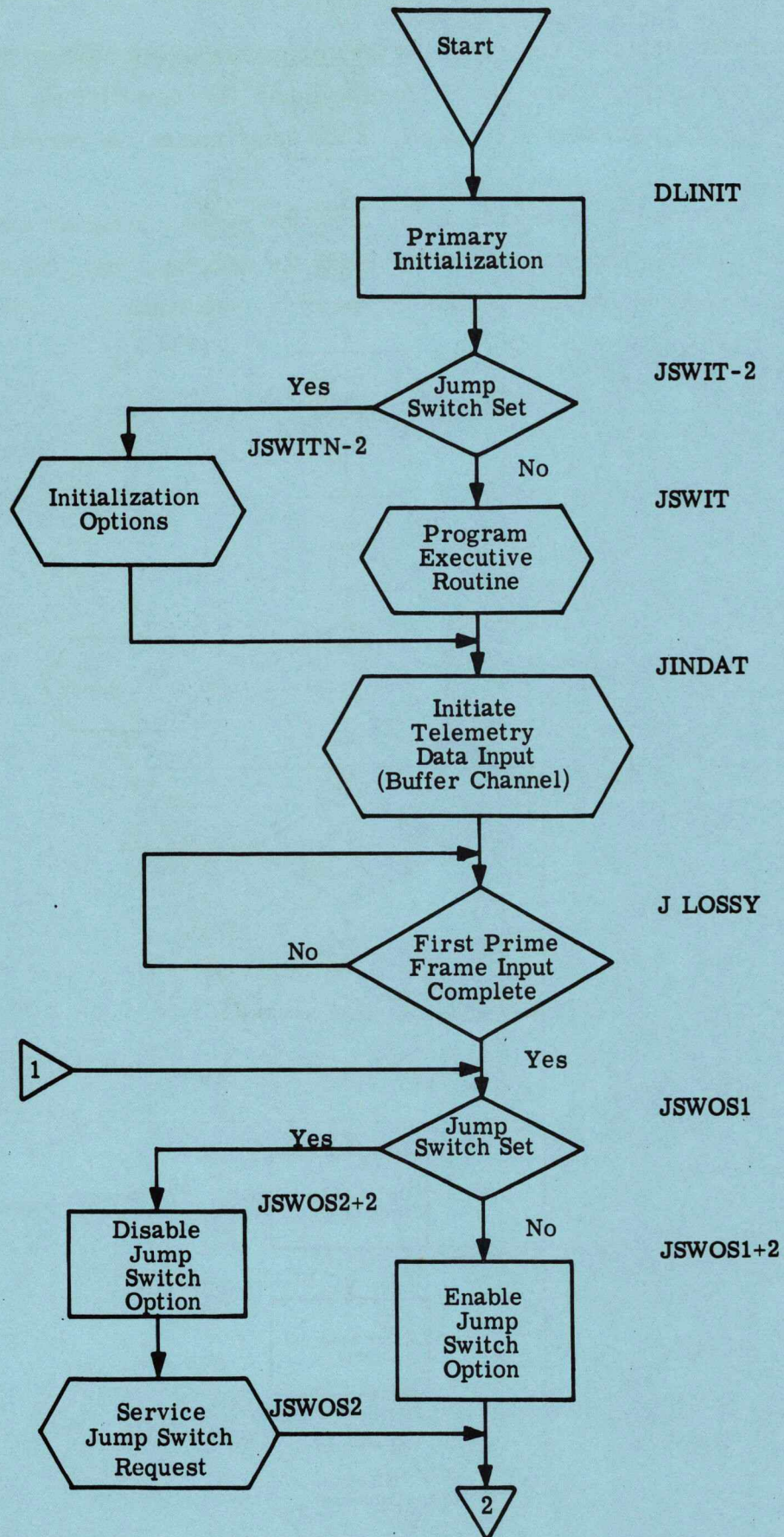


Figure 2. Downlink Control Program
(Sheet 1 of 2)

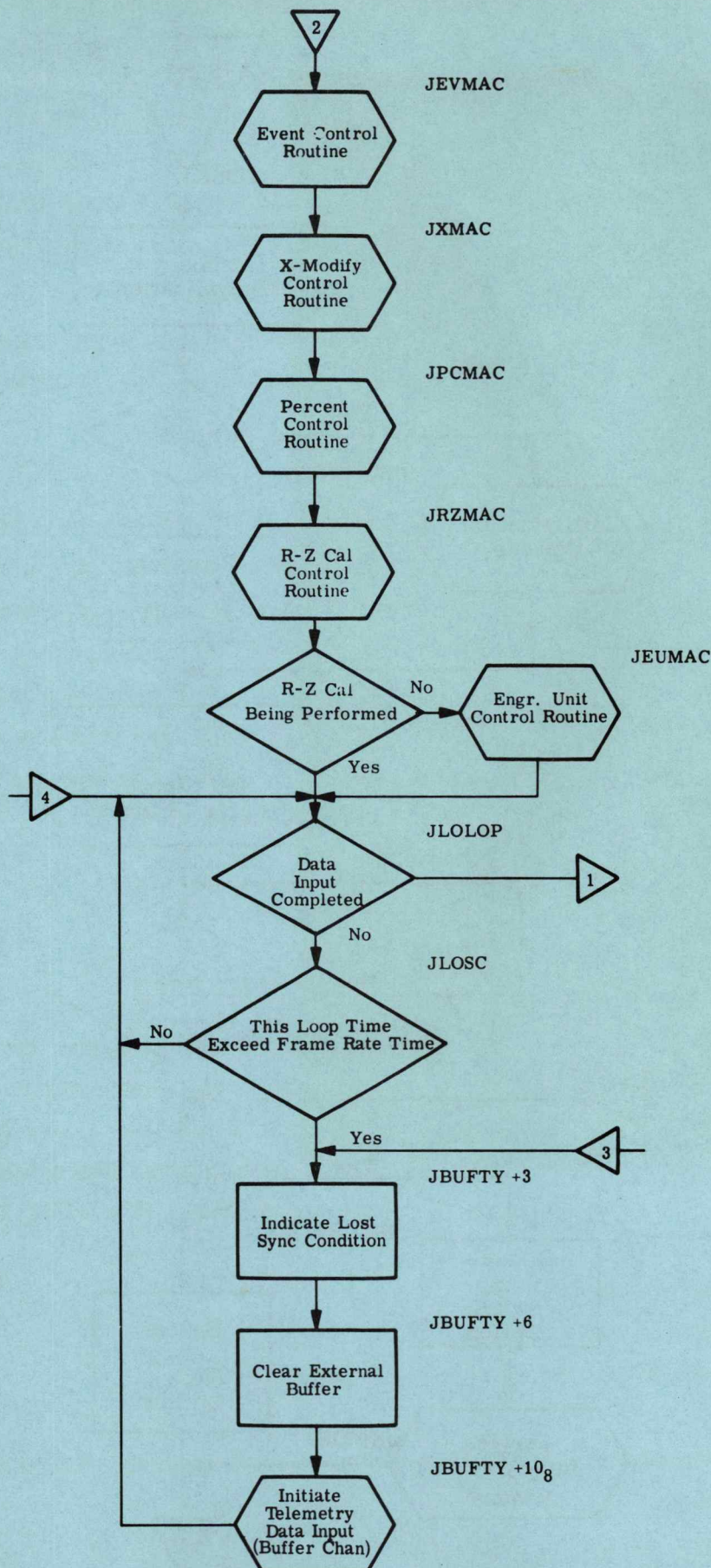


Figure 2. Downlink Control Program
(Sheet 2 of 2)

DATA TRANSMISSION DIGITAL COMMUNICATIONS AND CONTROL UNIT

OBJECTIVES

To familiarize the student with the Digital Communications and Control Unit (DCCU) and review the Data Transmission and Verification Converter (DTVC).

INTRODUCTION

The downlink data transmission system consists of a DTVC and a DCCU. This equipment facilitates the data transmission between the downlink computer and the Symbol Generator and Storage (SGS) Unit. The DCCU (Figure 1) is composed of a DTVC and a control unit adapter. The DCCU enables the downlink computer to communicate directly with the SGS via the serial data channel. By providing a 160G computer interface for the SGS and adapting it directly to the DTVC, it eliminates the need for a remote computer at stations where only input/output operations are being handled. In the case of the SGS, only input operations are affected.

EXPLANATION

DATA TRANSMISSION AND VERIFICATION CONVERTER

The DTVC operates under program control of a digital computer and communicates in parallel mode with a computer over a standard input/output communications channel. The DTVC communicates with other DTVC's or similar devices in serial mode over a long-distance communications link. Serial data is transmitted with 100-percent redundancy for verification by the receiving termination. The DTVC has three modes of operation:

- a. Select transmit.
- b. Select receive.
- c. Select interrupt.

The DTVC remains in the monitor or receive mode until the computer is ready for a transmission.

DIGITAL COMMUNICATIONS AND CONTROL UNIT

The downlink computer communicates with the DCCU (Figure 1) via the local DTVC utilizing control functions and control words. The control functions constitute the function-ready, output-resume, information-ready, input-ready signals, etc. The control words are the External Function (EF) codes transmitted over the data lines and perform the function of unit selection, mode selection, and channel selection.

The local DTVC remains in the monitor mode during all idle periods and the control unit adapter maintains the remote DTVC in the select-receive and interrupt mode. The local DTVC transmission loop always communicates with the remote DTVC/ adapter receiver loop; therefore, from the aspect of data transmission, the two DTVC's are back to back.

The first 12-bit word transmitted out of the downlink computer is an external function code to address the local DTVC and select the proper operation. The following sequential steps perform this function:

- a. The downlink computer transmits a 12-bit external function code over the data lines to the local DTVC.
- b. The computer simultaneously transmits a function-ready signal, allowing the local DTVC to decode the EF code.
- c. The DTVC translates the EF code word and enables select transmit and the correct serial channel.
- d. The local DTVC transmits an output-resume signal to the computer, which in turn removes the function-ready signal, which in turn removes the output-resume signal.

The local DTVC is now in the proper mode to communicate with the remote DTVC/ adapter via the selected serial channel. The next word to be transmitted by the computer is another EF code; however, to the local DTVC this EF code is treated as a data word. This word is now converted to serial format and transmitted over the hardlines to the remote DTVC. As previously stated, the remote DTVC is in the select-receive and interrupt mode. The remote DTVC utilizes the interrupt-code-word method to determine what type of operation the control unit adapter is to perform.

The upper six bits of the incoming EF code designate the interrupt word for the DTVC/adapter combination. These six bits of information must match the setting of

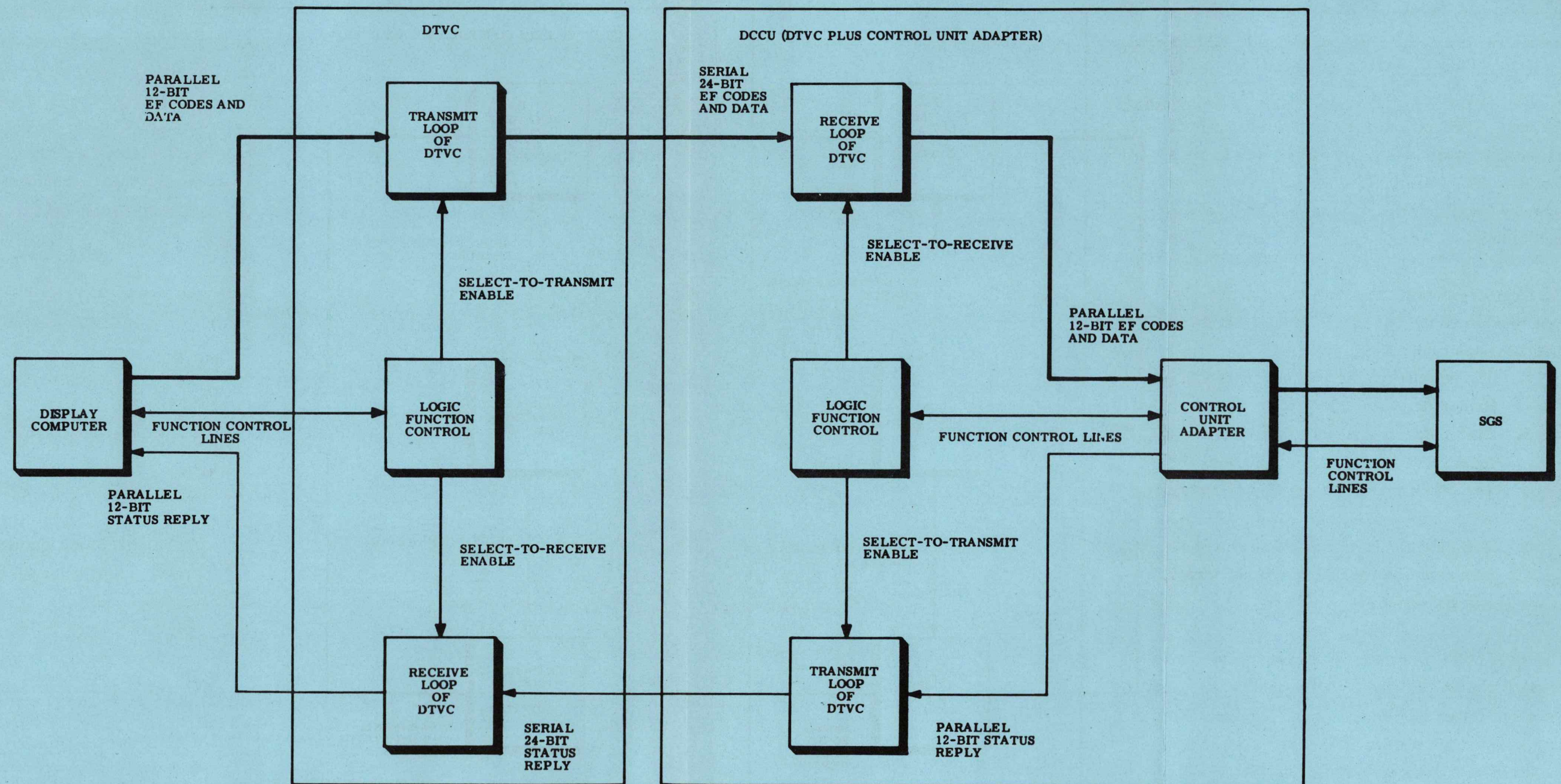


Figure 1. DTVC/DCCU Transmission Link Functional Block Diagram

six switches that have been preset to a particular configuration. The lower six bits of the incoming EF code designate the command requested for the adapter/SGS operation.

After the DTVC/adapter has been set up for an output operation to the SGS, the third 12-bit word from the display computer is transmitted over the serial channel. The DTVC/adapter treats this word as a function code for the SGS and will transmit this word out simultaneously with a function-ready signal. The function-ready signal allows the SGS to accept and translate the function code. The SGS translates the EF code and returns an output-resume signal to the control unit adapter. The DTVC/control unit adapter will transmit all subsequent words to the SGS until an interblock null is detected or until an error is detected.

In detecting an interblock null, the control unit adapter returns to the monitor mode and awaits another EF code from the computer, and if another block of data is to be transferred to the SGS, the cycle will be repeated.

If during transmission an error in a control word or data word is detected, a "hold" will be generated by the control unit adapter, thereby preventing any erroneous data from being transferred to the external equipment. After an interblock null is detected, the adapter places the DTVC in the select-transmit mode and transmits a coded 12-bit word to the computer indicating status and error. The computer decodes the adapter word, determines the status and/or error, and then retransmits the block of data a predetermined number of times.

If for each time the display computer retransmits the block of data, the DCCU returns the same status and/or error indicating code, the display computer enters into a programmed maintenance routine in an attempt to determine the exact nature of the problem.

ALPHANUMERIC DISPLAY SYSTEM

OBJECTIVES

To familiarize the student with:

- a. Inputs.
- b. Theory of operation.
- c. Display.
- d. Updating.
- e. CRT controls.

GENERAL

The alphanumeric display system provides a readout of results of exercises performed within the spacecraft. The display system receives formatted data and instructions from a digital computer, translates, stores, and displays this data in real time on cathode ray tubes (CRT). The data is displayed in alphanumeric form. The operator monitoring the CRT has the capability of choosing specific pages of data for display on his scope and also has available those controls necessary for individual comfort, i.e., focus, brightness, etc.

COMPONENTS

The alphanumeric cathode ray tube display system contains the following equipment:

- a. Symbol Generator and Storage Unit (SGS) - This unit incorporates a high-speed, magnetic-core memory and control logic, symbol generators, position generator, central timing logic, page selection circuits, and maintenance panel.
- b. Cathode Ray Tube and Callup Module - Up to twenty each, independent modules, containing a ten-inch diameter cathode ray tube with a raster size measuring 6 by 6 inches. Each module has switches allowing the operator to call up a full page of data at a time.

EXPLANATION

SYMBOL GENERATOR AND STORAGE UNIT (See Figure 1)

This unit receives 12-bit digital words from a digital computer. The 12-bit words are decoded and data words are stored in specific locations in memory according to logic performed on received-instruction words. The entire contents of memory is scanned at a rate sufficient to refresh all 20 cathode ray tubes at a minimum update rate of 30 cps. The unit receives and acts upon commands from the individual CRT callup keyboards in order to select page formatted data to be presented on the cathode ray tubes. The character repertoire of the SGS allows display of all alphanumeric characters together with a set of special symbols. A code to cause characters to blink or not to blink (at a rate that will be varied manually at the SGS maintenance panel) is incorporated. All characters stored in memory between the start-blink code and the no-blink code will be displayed in a blinking manner. The blinking indicates an out-of-tolerance condition. The initial page format is as follows:

- a. Each page consists of 1024 characters displayed in 24 lines of 40 characters each.
- b. One 32-character line at the top of the display.
- c. One 32-character line at the bottom of the display.

A half-page consists of either top or bottom half of the preceding format. A display character requires 6 bits from core memory. All numeric characters available for display can be received by the SGS in either binary coded decimal (BCD) or octal form. Word entry to the SGS will be 12 bits in length; two octal-coded display characters or three BCD-coded display characters are contained in one word of input data. When in the BCD mode, the SGS automatically converts BCD characters to octal characters for memory storage.

HIGH-SPEED MAGNETIC CORE MEMORY AND CONTROL LOGIC

The memory located in the SGS is a core stack of 2048- by 60-bit words. The recycle time of the memory (read-write cycle) is 6.4 microseconds. The memory also includes the necessary horizontal and vertical drivers as well as sense circuitry. The memory allocation for half-page formats is shown in Figure 2. A very convenient means of determining the address of any character position in any of the 20 pages of data in the SGS is illustrated by comparing Figure 2 with Figure 3.

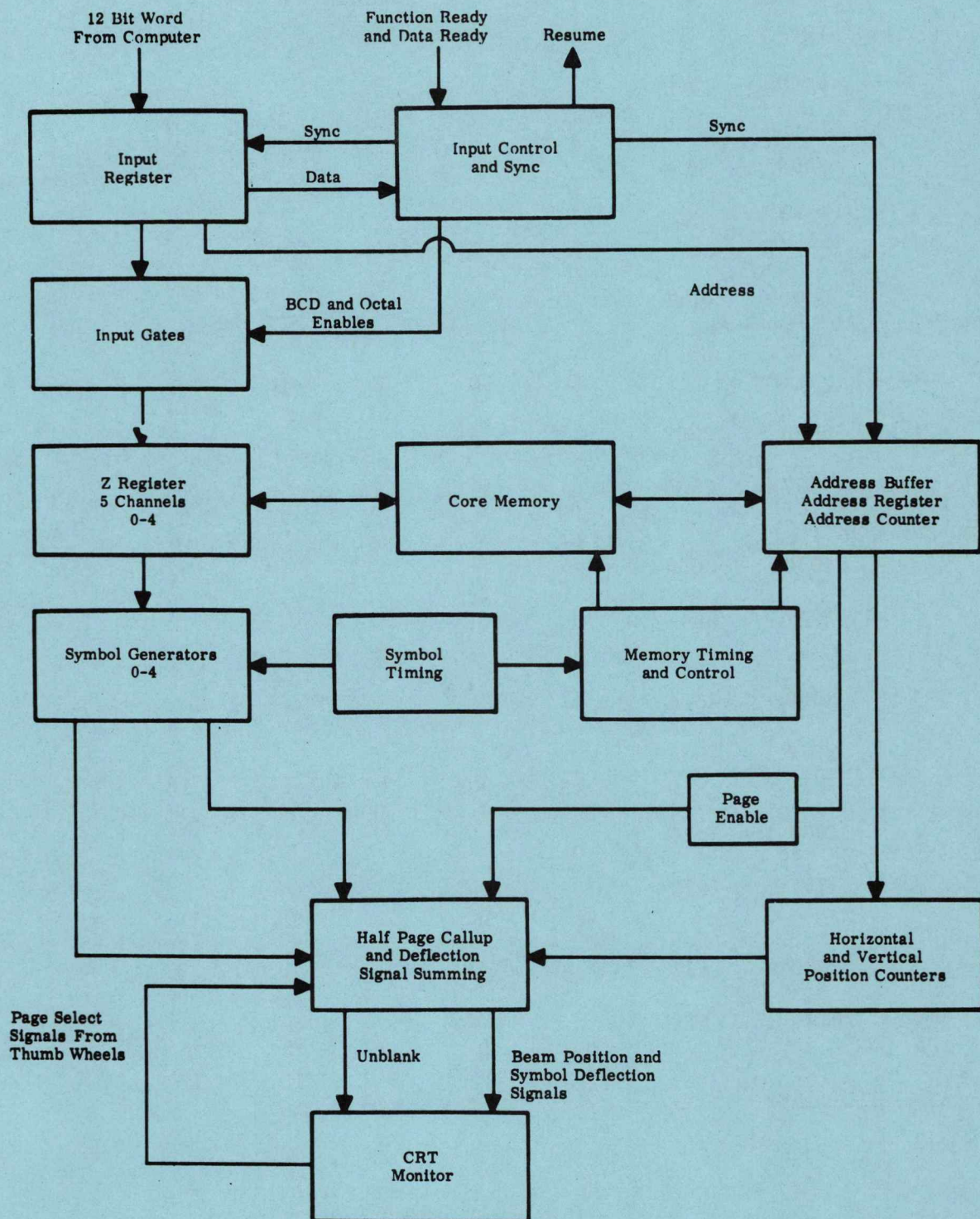


Figure 1. A/N Display System Simplified Block Diagram

Octal	Decimal	Memory Address				
		Channel				
		0	1	2	3	4
7777	4095	B	B	B	B	B
		4	8	12	16	20
7000	3584					
6777	3583	T	T	T	T	T
		4	8	12	16	20
6000	3072					
5777	3071	B	B	B	B	B
		3	7	11	15	19
5000	2650					
4777	2559	T	T	T	T	T
		3	7	11	15	19
4000	2650					
3777	2047	B	B	B	B	B
		2	6	10	14	18
3000	1536					
2777	1535	T	T	T	T	T
		2	6	10	14	18
2000	1024					
1777	1023	B	B	B	B	B
		1	5	9	13	17
1000	512					
0777	511	T	T	T	T	T
		1	5	9	13	17
0000	0					
		0	1	2	3	4
To Symbol Generators						

Figure 2. Memory Layout (Top- and Bottom-Half Pages)

0000	1 2 3 4 5 6 7	0010	1 2 3 4 5 6 7	0020	1 2 3 4 5 6 7	0030	1 2 3 4 5 6 7		
0040		0050		0060		0070		0100	1 2 3 4 5 6 7
0110		0120		0130		0140		0150	
0160		0170		0200		0210		0220	
0230		0240		0250		0260		0270	
0300		0310		0320		0330		0340	Upper
0350		0360		0370		0400		0410	1/2
0420		0430		0440		0450		0460	Page
0470		0500		0510		0520		0530	
0540		0550		0560		0570		0600	
0610		0620		0630		0640		0650	
0660		0670		0700		0710		0720	
0730		0740		0750		0760		0770	
1000	1 2 3 4 5 6 7	1010	1 2 3 4 5 6 7	1020	1 2 3 4 5 6 7	1030	1 2 3 4 5 6 7	1040	1 2 3 4 5 6 7
1050		1060		1070		1100		1110	
1120		1130		1140		1150		1160	
1170		1200		1210		1220		1230	
1240		1250		1260		1270		1300	Lower
1310		1320		1330		1340		1350	1/2
1360		1370		1400		1410		1420	Page
1430		1440		1450		1460		1470	
1500		1510		1520		1530		1540	
1550		1560		1570		1600		1610	
1620		1630		1640		1650		1660	
1670		1700		1710		1720		1740	1 2 3 4 5 6 7
1740	1 2 3 4 5 6 7	1750	1 2 3 4 5 6 7	1760	1 2 3 4 5 6 7	1770	1 2 3 4 5 6 7		

Pages 1, 5, 9, 13, 17, use as is. Pages 2, 6, 10, 14, 18, add 2000. Pages 3, 7, 11, 15, 19, add 4000.
Pages 4, 8, 12, 16, 20, add 6000.

Figure 3. SGS Raster to Address Conversion Chart

The SGS memory, upon receipt of an instruction and address, loads sequentially in a channel until receipt of a new instruction and address. In this manner, the computer is able to update any portion of any or all lines by changing the stored data.

There are four distinct types of words from the computer to the SGS. They are as follows: (Refer to Figure 4)

- a. External-Function-Select Word - This word is used by the computer to uniquely select the display system for transfer of data. The octal code for the external function word is 0100.
- b. SGS Control Word - This word selects either the BCD or octal-coded format, determines whether to write or not write over stored period-character codes, and selects the channel number.

The SGS control word will always be followed by a 12-bit address word. The most significant 6 bits of the control word will always be octal-code 75. Thus, the control word will be uniquely specified. The eighth bit from the Most Significant Bit (MSB) of the control word specifies the coding of the data words following the control word. There are two types of data words, BCD-coded and octal-coded. The ninth bit from the MSB of the control word is used to ascertain whether to write over period-character codes that may or may not be stored in addresses specified by the block input following the control word. If the ninth bit is a zero, the contents of the selected initial address and of all sequential addresses will be tested for the presence of a period code. If the address contains a period-character code, the new information is received into the next sequential address containing no period code. If the ninth bit is present, period-character codes are written over with new information.

- c. Address Word - This word always follows the SGS control word and always specifies the address, in the selected channel, that the computer will begin loading. The memory assigned to the selected channel will then be sequentially loaded until such time as the next control word is recognized.
- d. Data Word - An address word will always be followed by one or more data words. Depending on the code identified in the control word, the data words will either contain three BCD-coded display characters or two octally coded display characters. (See Tables 1 and 2.)

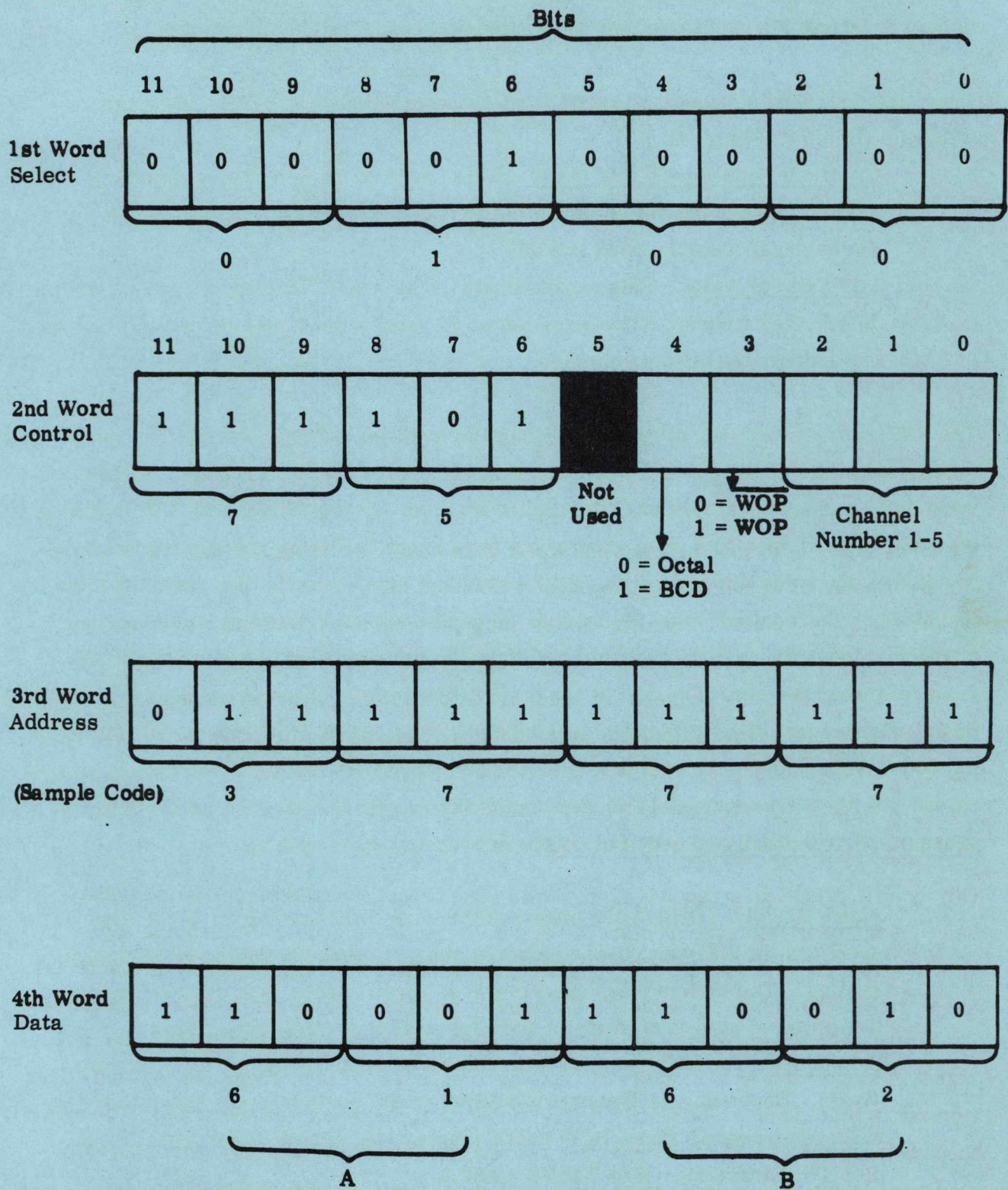


Figure 4. Computer Words to Symbol Generator and Storage Unit (SGS)

Table 1
BCD Character Display Codes

BCD Code	Character
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	0
1011	*
1100	Space
1101	Blink
1110	No Blink
0000	Skip

A typical example of loading the SGS from the computer utilizing all four types of previously discussed words is as follows:

- a. 0100 - (External Function Code) computer selects A/N display system.
- b. 7511 - Octally coded character mode write over period, channel 1.
- c. 2004 - Starting address for load, fifth character, page 6, channel 1.
- d. 4561 - Load octal code for N in address 2004, load octal code for A in address 2005.

SYMBOL AND POSITION GENERATORS

The symbol generators receive 12-bit octal codes from the SGS memory and transform these codes into synchronized X- and Y-deflection signals. An unblank signal is also developed to unblank the CRT's during the generation of the required character(s). Each symbol generator receives 12-bit octal codes from a specific memory channel. Thus, each symbol generator generates the 4096 characters required to fill four full pages. The characters are generated as sequential locations of memory are read out. The memory is read out as 60-bit words; thus, five symbol generators are required. The symbol generator drives with sufficient power so that any or all 20 CRT's may select the same page or half page for display with no apparent degradation in quality of displayed data.

A position generator is incorporated in the SGS. This generator produces the analog-deflection signals for positioning the characters on each page and are summed with the

Table 2
Octal Character Display Codes

Octal Code	Character	Octal Code	Character
12	0	26	W
01	1	27	X
02	2	30	Y
03	3	31	Z
04	4	60	+
05	5	40	-
06	6	13	=
07	7	14	(space)
10	8	73	.
11	9	21	/
61	A	52	%
62	B	77	(Degree)
63	C	00	(Skip)
64	D	36	(Delta)
65	E	34	(Theta)
66	F	17	(Omega)
67	G	32	(Gamma)
70	H	57	(Mu)
71	I	53	(Sigma)
41	J	35	(Phi)
42	K	76	(Psi)
43	L	37	(Omega)
44	M	74	(Lambda)
45	N	72	(Angle)
46	O	33	(Comma)
47	P	54	(Asterisk)
50	Q	15	Start Blink
51	R	16	No Blink
22	S	55	Arrow
23	T	56	Arrow
24	U		
25	V		

character-deflection signals in the deflection signal summing networks. The page format is preset by logic in the position generator.

HALF-PAGE CALLUP

The half-page callup receives the half-page command signals from the CRT callup keyboard. Upon receiving these signals, the switching logic selects the correct symbol generator(s) and the correct half pages (top and bottom) from memory for transmission to the requesting CRT module. It is possible to select any of 20 top half pages and any of 20 bottom half pages from any 20 CRT callup keyboards utilizing the central switching logic. (Refer to ACE-S/C Operator's Manual, for details of CRT module operation.)

Figure 5 is a simplified block diagram that illustrates character forming and positioning circuits to the alphanumeric cathode ray tube display.

CHARACTER FORMING AND POSITIONING CIRCUITS

The display on the face of the CRT consists of 26 lines of characters. The top and bottom lines of the page format contain 32 characters each. The other 24 lines contain 40 characters each.

In order to perform this operation, the positioning circuits operate so as to move the dot across the face of the scope as shown in Figure 6. Starting at the top left hand corner, the Y register will be cleared and the X register will step 32 counts horizontally.

The CRT will be unblanked at each stop. During the stop the character-forming network will cause the dot to move in such a manner as to paint a character on the face of the CRT.

At the end of the first line, the X register is cleared and the Y register advances one count. The X register now counts 40 steps across the face of the CRT and again the characters are painted at each step. This process is continued to the bottom line. At the count of 32 in the X register, both the X and Y registers will be cleared and the operation will be repeated starting at the upper left-hand corner.

Figure 5 shows the channels for moving the beam across the face of the scope. Also shown are the character forming circuits. The output of the character forming circuits

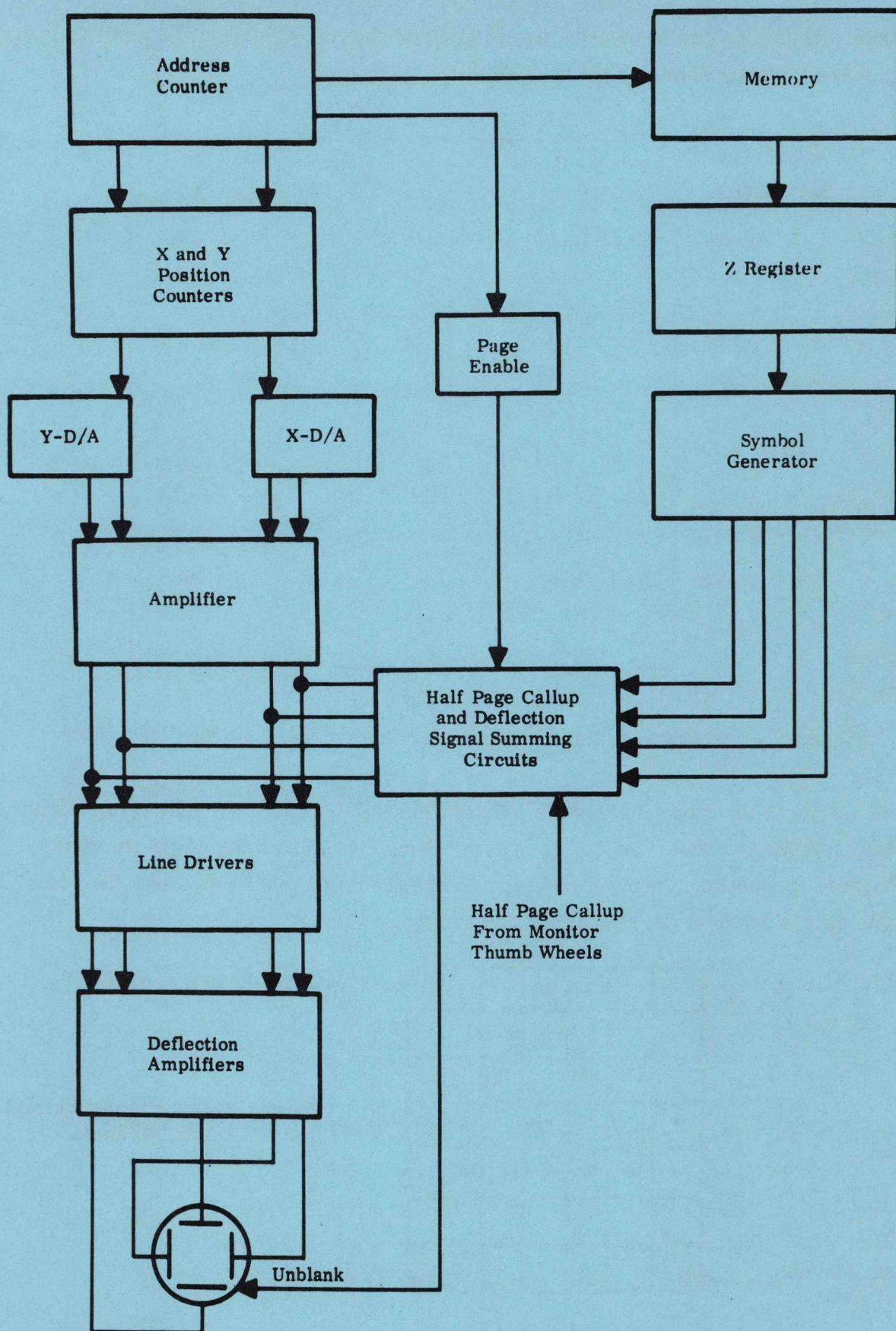


Figure 5. Character Forming and Positioning Circuits Simplified Block Diagram

is mixed with the X- and Y-positioning voltages on the lines between the amplifier and line driver blanks as shown in the diagram.

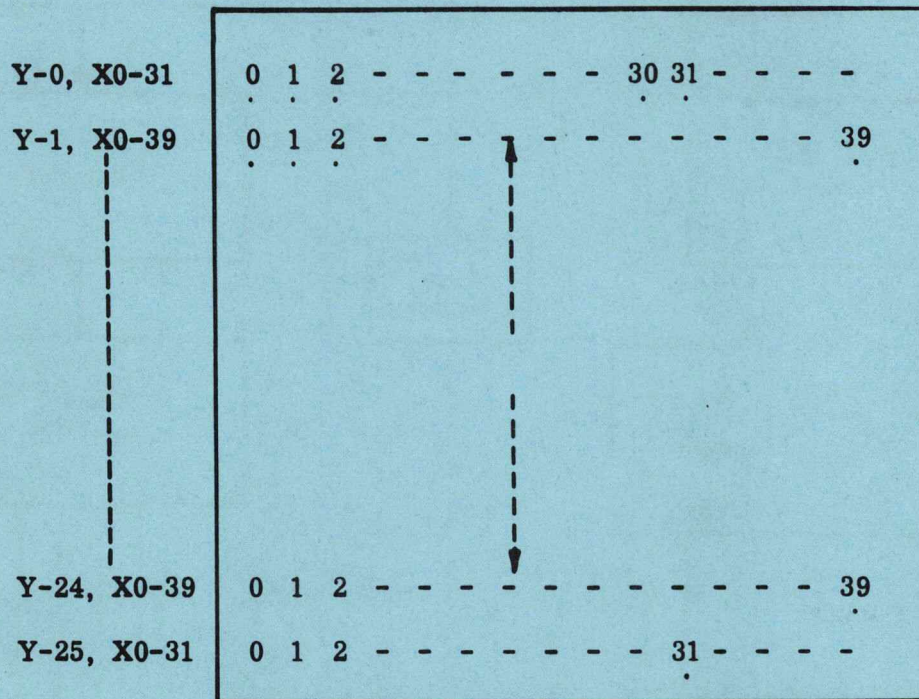


Figure 6. Movement of Dot Across Alphanumeric Cathode Ray Tube Face

Figure 7 depicts the steps involved in printing the letter "A" on the face of the alphanumeric cathode ray tube. After the preset voltage has moved the dot to the lower left corner, the moved voltages are gated through the diode matrix to move the beam in steps as indicated on the blank dots on the Figure 7.

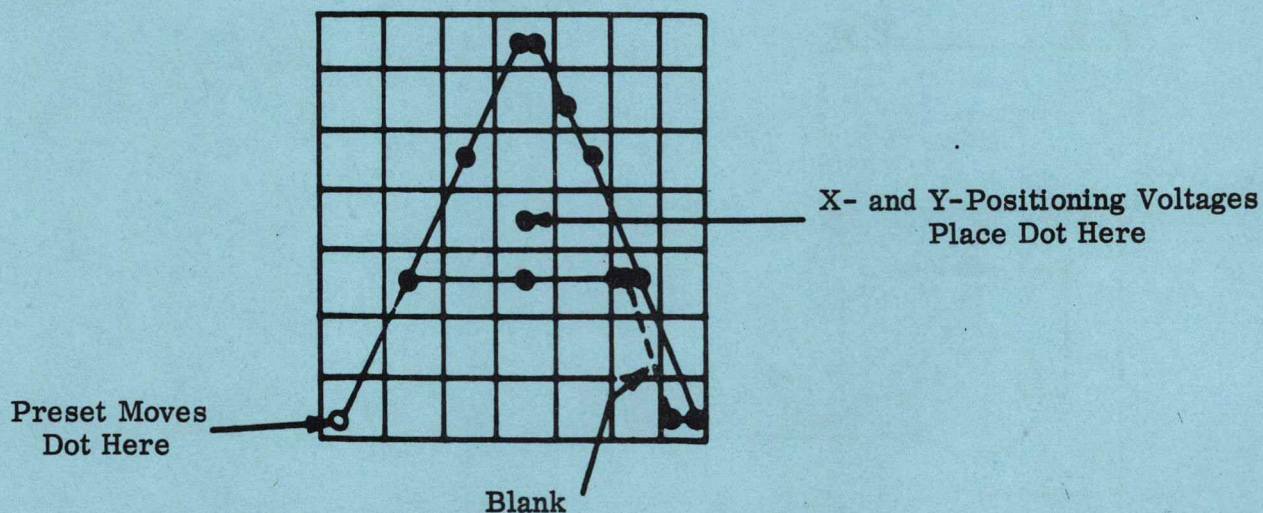


Figure 7. Letter "A" Printed on Alphanumeric Cathode Ray Tube Display Surface

The inputs to the character forming inverters and line drivers consist of AND gates where the data for a page is gated through to the monitor from which the callup signals are arriving. There are 20 of these circuits, one for each monitor in the system.

SPECIAL DISPLAY AND RECORDING EQUIPMENT

OBJECTIVES:

To familiarize the student with:

- a. Pulsed Integrating Pendulum Accelerometer (PIPA).
- b. Cardiograph.
- c. Digital cardiometer.

INTRODUCTION

The ACE-S/C system incorporates various special display devices utilized to process, record, and display designated parameters and certain astronaut physical information, such as heartbeat. The following paragraphs describe those displays and equipment which perform unique or special-purpose functions.

EXPLANATION

PULSED INTEGRATING PENDULUM ACCELEROMETER

The Pulsed Integrating Pendulum Accelerometer (PIPA) display equipment is located in the Guidance and Navigation System Console. The PIPA display equipment consists of a Hewlett-Packard 120B oscilloscope, a variable 0- to 360-degree resolver, a low-pass filter, a divide-by-64 frequency divider, an equalization circuit, and an amplifier. This equipment is used to evaluate the phase shift of the three PIPA signal generators which are part of the airborne guidance system located in the spacecraft test area. The phase shift is displayed as a Lissajous pattern by comparing one of the PIPA signal generator outputs with a 3.2-kc reference signal on the PIPA oscilloscope located in the Guidance and Navigation System Console. The PIPA oscilloscope is equipped with a self-contained Polaroid camera and camera housing. Thus, photographic recording with simultaneous viewing is provided.

Figure 1 is a block diagram of the PIPA display equipment. By means of a command from an R-START module located in the Guidance and Navigation System Console, one of the PIPA signals (X, Y, Z, or 3.2-kc calibration) at the spacecraft test area is selected. Any one of these signals is available for display on the PIPA oscilloscope by means of a hardline link to the Systems Patch Terminal Unit. The selected PIPA signal

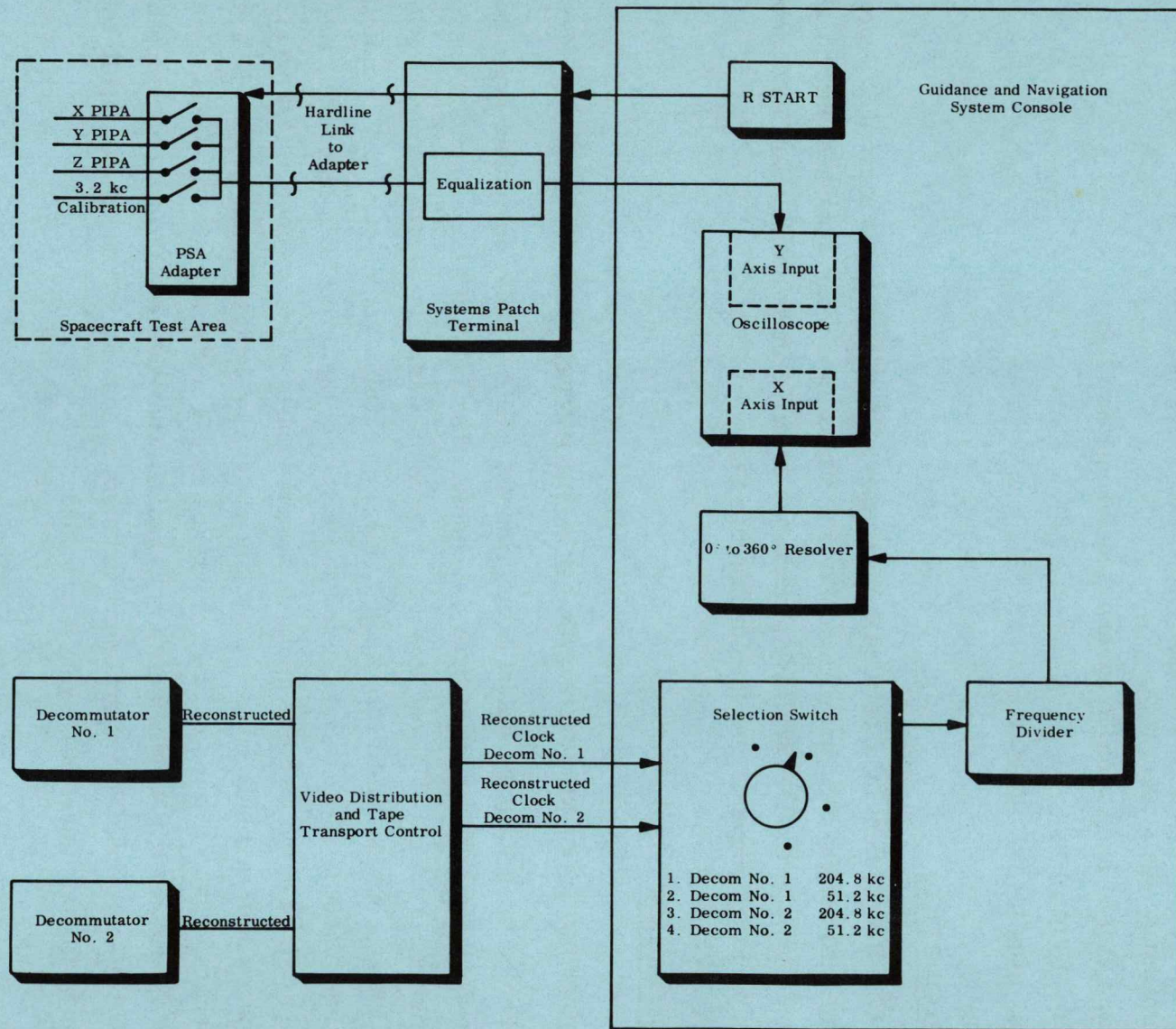


Figure 1. PIPA Simplified Diagram

is applied to a line equalization circuit contained in the Systems Patch Terminal Unit. The equalization circuit provides uniform gain and phase characteristics at a frequency of 3.2-kc. The axis of the PIPA oscilloscope is located in the Guidance and Navigation System Console.

In order to display the PIPA Lissajous pattern which takes the shape of a butterfly, a second 3.2-kc reference signal is applied to the X-axis input. The reference signal is established by frequency division of either the 204.8-kilobit (kb) or the 51.2-kilobit reconstructed clock signal output of PCM Decommulator. The reconstructed clock signals from both decommutators are routed through the Video Distribution and Tape Transport Control Unit and the Systems Patch Terminal Unit to a panel-mounted selector switch located on the Guidance and Navigation System Console.

The reconstructed clock signal is applied to a frequency divider. The panel-mounted selector switch permits the reconstructed clock signals to be applied to various stages of a frequency divider. When a 204.8-kilobit reconstructed clock signal is to be processed, the switch is set to route the clock signal through the stage, resulting in a division by 64. When a 51.2-kilobit reconstructed clock signal is to be processed, the switch is reset to route the signal to the stage that divides by 16. Thus, the reference signal output of the frequency divider will always be 3.2-kc regardless of the reconstructed clock signal frequency.

The 3.2-kc reference signal output from the frequency divider is converted to a sine wave and is applied to a resolver containing a quadrature winding. The resolver permits the reference signal phase angle to be adjusted from 0 to 360 degrees by means of a front-panel-mounted dial. In addition, the front panel contains a two-position 45° INCREMENT switch. When the switch is placed in the IN position, the quadrature winding of the resolver is connected providing a fixed phase shift of 45 degrees. When the switch is in the OUT position, the quadrature winding is disconnected.

The PIPA display equipment will have a test capability whereby the 51.2- and 204.8-kilobit signals can be generated from a source within the ACE-S/C ground station.

CARDIOGRAPH (MILA Only)

The Cardiograph located in the Aeromedical Console is a high-precision, direct-writing device used to provide a permanent record of astronaut heart-rate information. The Cardiograph is functionally similar to the eight-channel Analog Recorder. However,

there are certain physical differences between the two. For example, the Cardiograph has chart speeds 50 percent lower than the Analog Recorder, the local remote switch is not available on the Cardiograph, and the Cardiograph uses a horizontally-mounted oscillograph as differentiated from the vertical oscillograph contained on the eight-channel Analog Recorder.

DIGITAL CARDIOMETER (MILA Only)

The astronaut's pulse rate is displayed to the Aeromedical Representatives by the Digital Cardiometer (Figure 2). To recognize rapid changes in pulse rate, the heartbeats are counted during either a 10-second or 15-second period and the resulting count is converted to a figure that represents pulses per minute.

This figure is displayed on projection-type numeric indicators located on the front panel of the Cardiometer located on the Aeromedical Console. Front panel controls are provided for selecting one of two signal inputs, resetting the internal counting circuits to zero, and for adjusting the instrument to trigger reliably from the input electrocardiogram signal. The input select control also allows selection of a calibrate test signal.

The circuits of the Cardiometer (Figure 2) may be divided into five major groups for purposes of discussion:

- a. Heart beat pulse generator.
- b. Sample gate generator.
- c. Pulse rate conversion counter.
- d. Display storage.
- e. Display conversion matrix.

In addition to the above, there are circuits for controlling the sample rate, resetting the instrument to zero, and displaying the pulse rate.

Electrocardiogram wavetrain signals are applied to the heart rate pulse generator circuits from the digital-to-analog converter circuits in the ACE-S/C Aeromedical Console. Because the wavetrain is not suitable for operating the counting circuits, the heartbeat pulse generator is used to generate the required uniform pulses to drive the counters. The heartbeat pulse generator circuits also contain the THRESHOLD ADJUST control permitting adjustment of the Cardiometer so that it operates on the proper peak of the wavetrain.

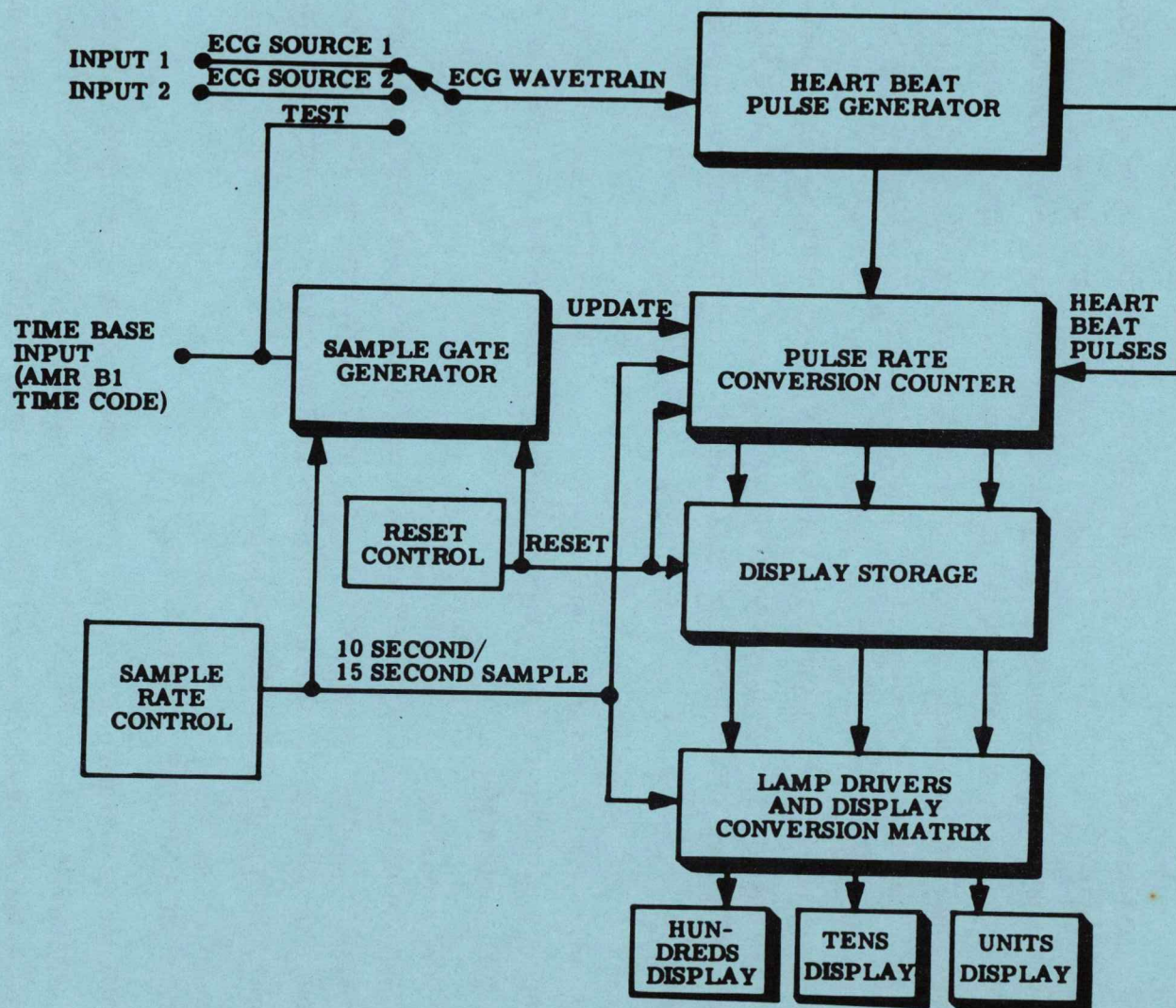


Figure 2. Digital Cardiometer Simplified Block Diagram

To display a figure representing pulses per minute after counting the heart beat for only a 10-second or 15-second period, the pulses are multiplied by a factor of four or six. This conversion by multiplication is performed by a Pulse Rate Conversion Counter. For example, when the 10-second period is selected by the operator, the number of heart beats is multiplied by a factor of six. Thus, 11 heart beats would be converted to 66, a figure that represents the pulse-per-minute average. When the 15-second period is selected the heart beats are multiplied by a factor of four.

The operator selects the sample period by setting the front panel SAMPLE PERIOD control to either the 10 SECOND or 15 SECOND position. The time base for the Cardiometer is derived from the AMR B-1 time code by the sample gate generator. The AMR B-1 time code is composed of 1-pps pulses of varying widths. These 1-pps pulses are counted by the sample gate generator circuits to provide an update pulse every 10 or 15 seconds, depending on the setting of the SAMPLE RATE control.

The update pulse controls the pulse rate conversion counter and the display storage circuits. Each occurrence of the update pulse causes the content of the pulse rate conversion counter to be shifted to display storage and the count in the conversion counter to reset to zero.

The count in the display storage circuits is converted to decimal (10-line code) form by the display conversion matrix. This 10-line code is used by the lamp drivers to operate the numeric display.

The operator can reset the Cardiometer to zero by depressing the RESET pushbutton, thus causing the restart of the operation at any time. Depressing the RESET pushbutton causes the reset of the sample gate generator counters, the pulse rate conversion counter, and the display storage circuits.

CRT SWITCHING UNIT (MSC Only)

The CRT Switching Unit permits three of the alphanumeric display outputs from the SGS Unit to be switched between six console CRT modules. Three of the CRT modules are located in the Thermo Structures Facilities Console, while the remaining three CRT modules are individually located in the Service Propulsion and Reaction Control Console, the Stabilization and Control Console, and the Guidance and Navigation System Console. One of the CRT modules located in the Thermo Structures Facilities Console will be used to drive a slave CRT in the Solar Simulator Console.

The CRT Switching Unit (Figure 3) can be patched to provide alphanumeric display signals to the above-mentioned consoles, thereby denying alphanumeric display signals to the three CRT modules located in the Thermo Structures Facilities Console. The patching configuration can be rearranged to provide alphanumeric display signals to any or all of the CRT modules located in the Thermo Structures Facilities Console at the expense of denying such signals to the CRT modules in the consoles mentioned previously. The patch configuration to be employed will be established by the program test requirements.

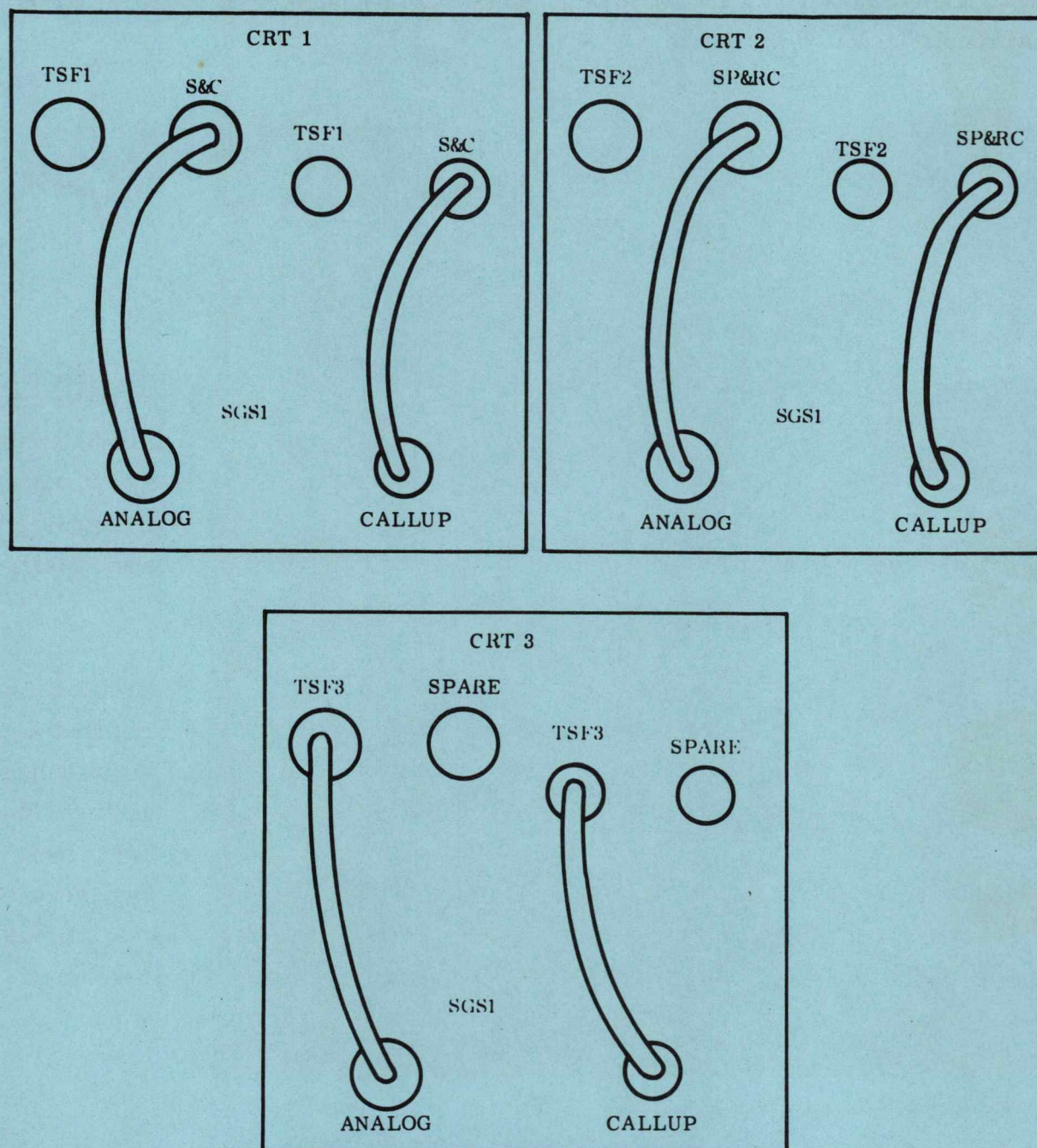


Figure 3. CRT Switching Unit Panel at MSC
FOR TRAINING PURPOSES ONLY

ANALOG AND EVENT DISTRIBUTION

OBJECTIVES

To familiarize the student with:

- a. Decommutator Distribution Unit.
- b. Event Storage and Distribution Unit.
- c. Digital-to-Analog converters.
- d. Recorders.
- e. Event modules and meter modules.
- f. Event and analog select panel.

INTRODUCTION

Units of the ACE-S/C system utilized to process, display, and record the addressed digital test data outputs of the decommutator units are shown in Figure 1. The Decommutator Distribution Unit (DDU) receives addressed digital test data from both decommutators via transmission hardline connections (one line per bit). Fan-out amplifiers within the DDU distribute the received test data word to the Event Storage and Distribution Unit (ESDU) and control consoles.

Within the ESDU, the test data event words are identified (by address recognition) and are routed to storage registers. The outputs of the storage registers, representing on-off event functions, are distributed to recording and/or display units (event indicators) mounted in the control consoles. Analog data words from the DDU are identified in a manner similar to that used for event data words and are stored by digital logic circuits contained within the control consoles. In this case, the storage register outputs are fed to Digital-to-Analog (D/A) converters. The resultant analog signals are routed, via a patchboard, to appropriate recording and/or display units (meter modules) mounted in the control consoles.

EVENT DATA DISPLAY FUNCTIONS

Event data words are selected from intermixed analog and event data words received from the decommutator distribution circuits in the event storage and distribution section of the DDU/ESDU. This selection (by address recognition) and the storage location

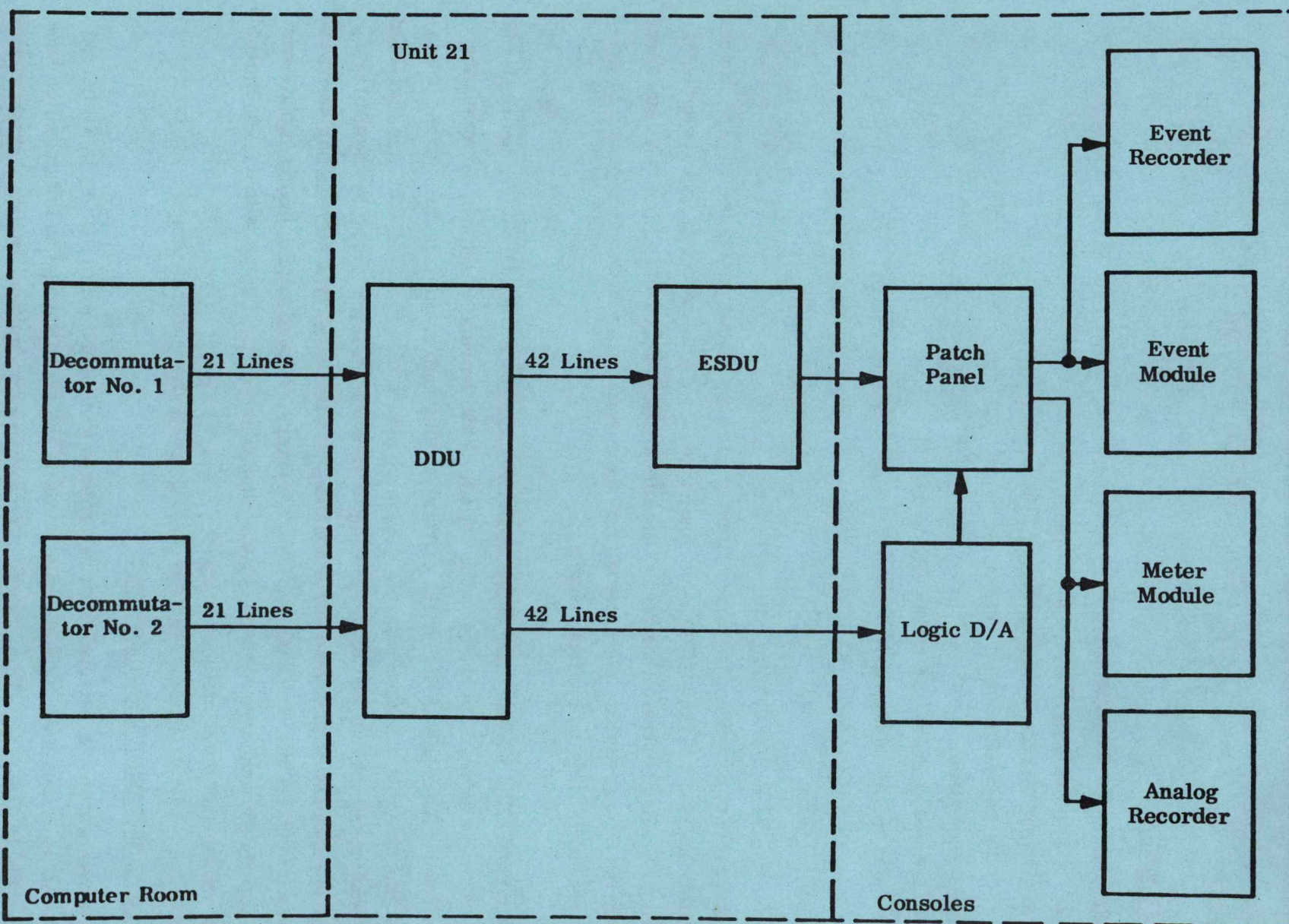


Figure 1. Analog and Event Data Distribution and Display

of each event bit is predetermined by the selection and arrangement of plug-in logic modules within the event storage and distribution circuits.

The ESDU will select and store 150 event words, each of which consists of eight discrete event functions (a total of 1200 events). The event words are gated into registers within the ESDU. The output of each bit position in a register represents the status of a specific event (whether it has or has not occurred).

The outputs of the storage registers are routed to a patch facility in the DDU/ESDU. The patching at this point determines the distribution of each event function to the various consoles and permits routing any specific event function to multiple locations. The outputs of the ESDU are fed to event recorders and/or lamp drivers (in the consoles), which cause event lamps to light.

Event modules are located on the various system control consoles. The front panel of an event module contains 24 lights arranged in three vertical rows of eight lights each. Each light is equipped with a colored lens engraved to identify the event function. These lenses are replaceable if it is necessary to change the display. A lamp test switch on the module tests the function of all lamps simultaneously.

Event recorders are utilized to provide permanent records of events where the time and/or duration of events are desired. Two types of event recorders are used: a 32-channel recorder providing a continuous-write, deflection-type presentation and a 100-channel recorder providing a write/no-write indication of event status. Both recorders have paper speed controls and each includes time recording channels.

ANALOG DATA DISPLAY FUNCTIONS

The intermixed analog and event data words from the decommutator distribution circuits of the DDU/ESDU are routed to all system control consoles. Each control console has address selection circuits that select the analog data words to be displayed at the particular console. The division between decommutator output and the selection of addresses that will be accepted is predetermined by the selection and arrangement of plug-in logic modules in each control console.

These address logic circuits decode the address portion of analog data words to gate the data portion of the word into a storage register. The storage register is connected to a D/A converter that operates a meter and/or a pen on an analog recorder. In some

consoles, the data to be displayed on a particular indicator can be selected from as many as four different addresses. This address selection is controllable by means of a selector switch on the console front panel.

DECOMMUTATOR DISTRIBUTION UNIT FUNCTIONS

The DDU simultaneously receives addressed digital test data words from the two PCM decommutators located in the computer room. The circuits of the DDU are identical for both decommutator inputs and provide the following functions:

- a. Sample the incoming data rate.
- b. Switch decommutator inputs in the event of a read pulse failure.
- c. Distribute the test data word received to the ESDU and various control consoles.

Each test data word received from the decommutators is in parallel format. Each word is composed of 12 binary bits representing the address, 8 binary bits representing data, and an associated read pulse. To receive a test data word, 21 lines are required, one for each bit of the word. Either analog or event information can be represented by the incoming test data words and they arrive at the DDU input in an intermixed form.

The test data words are routed from the decommutators through the terminal patch facility to the DDU via 42 hardlines (see Figures 1 and 2). Twenty-one of these lines carry Decommutator No. 1 data and 21 carry Decommutator No. 2 data. Each line is terminated at the DDU input and is applied to a set of switch gates. All switching gate circuits are identical. Each of the 42 switching gates receives a Decommutator No. 1 input line and a Decommutator No. 2 input line. Each read pulse line (one from each decommutator) is also fed to a read pulse detection circuit. The outputs of each read pulse detection circuit are switching signals used to control the status of their associated switching gates.

Half of the switching gates will normally pass Decommutator No. 1 test data words while the remaining half will normally pass Decommutator No. 2 test data words. This will be the case as long as both decommutators are supplying a read pulse to the DDU. If, for any reason, a decommutator ceases to supply a read pulse, the output of the read pulse detection circuit, associated with that particular decommutator, will change state. This change of state in the read pulse detection circuit output will cause the status of the associated switching gates to change. As a result, the switching gates associated with the nonoperative decommutator will pass the test data still being

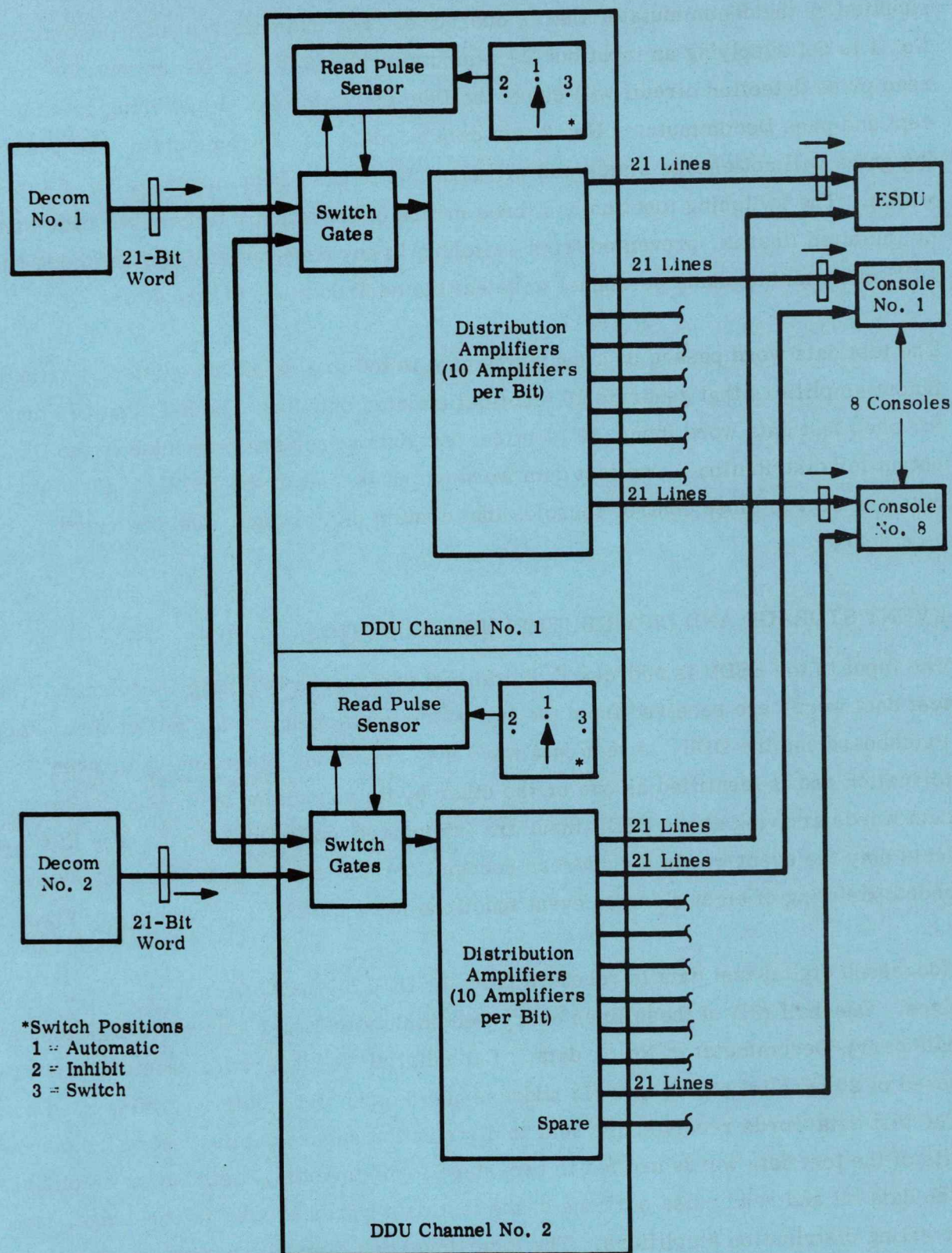


Figure 2. Analog and Event Distribution

supplied by the decommutator that is operative. For example, assume Decommulator No. 1 is not supplying an input but Decommulator No. 2 is, the Decommulator No. 1 read pulse detection circuit will cause the Decommulator No. 1 switching gates to accept and pass Decommulator No. 2 test data words. The Decommulator No. 2 switching gates will not change status and will continue to pass Decommulator No. 2 test data words. The switching function has three modes of operation: fully automatic, manual, or inhibited (that is, prevented from switching at any time) switching. Switches on the DDU allow maintenance personnel to select the desired mode of operation.

The test data word passed by a switching gate is fed to a set of associated distribution fanout amplifiers that generate 10 identical isolated outputs. The net result is that, for each test data word input, 10 identical test data words are presented to the DDU output for distribution. One test data word output is sent to the ESDU, eight of the outputs are sent to those control consoles that contain digital logic, and one output is used as a spare.

EVENT STORAGE AND DISTRIBUTION UNIT FUNCTIONS

The input to the ESDU is addressed digital test data words in a parallel format. These test data words are received from the two decommutator units via the Terminal Facility Patchboard and the DDU. A test data word may represent either analog or event information and is identified as one or the other by its associated address. The test data words arriving at the ESDU input are intermixed analog and event. The ESDU selects only the event words (by address recognition) and stores up to 150 such words, each consisting of eight discrete event functions for a total of 1200 events (see Figure 3).

Addressed digital test data is received from the DDU by the ESDU via 42 parallel data lines. One-half (21) of these lines carry Decommulator No. 1 data while the remaining half carry Decommulator No. 2 data. Each digital test data word received is composed of 20 parallel binary bits (12 address and 8 data) and a delayed timing read pulse. The test data words received are sent to distribution subassemblies where the address bits of the test data words are fed to two-stage logic-inverting distribution amplifiers. The data bit and read pulse portions of the test data words are fed to one-stage, logic-inverting distribution amplifiers. The logic-inverting distribution amplifiers are identical for both decommutators.

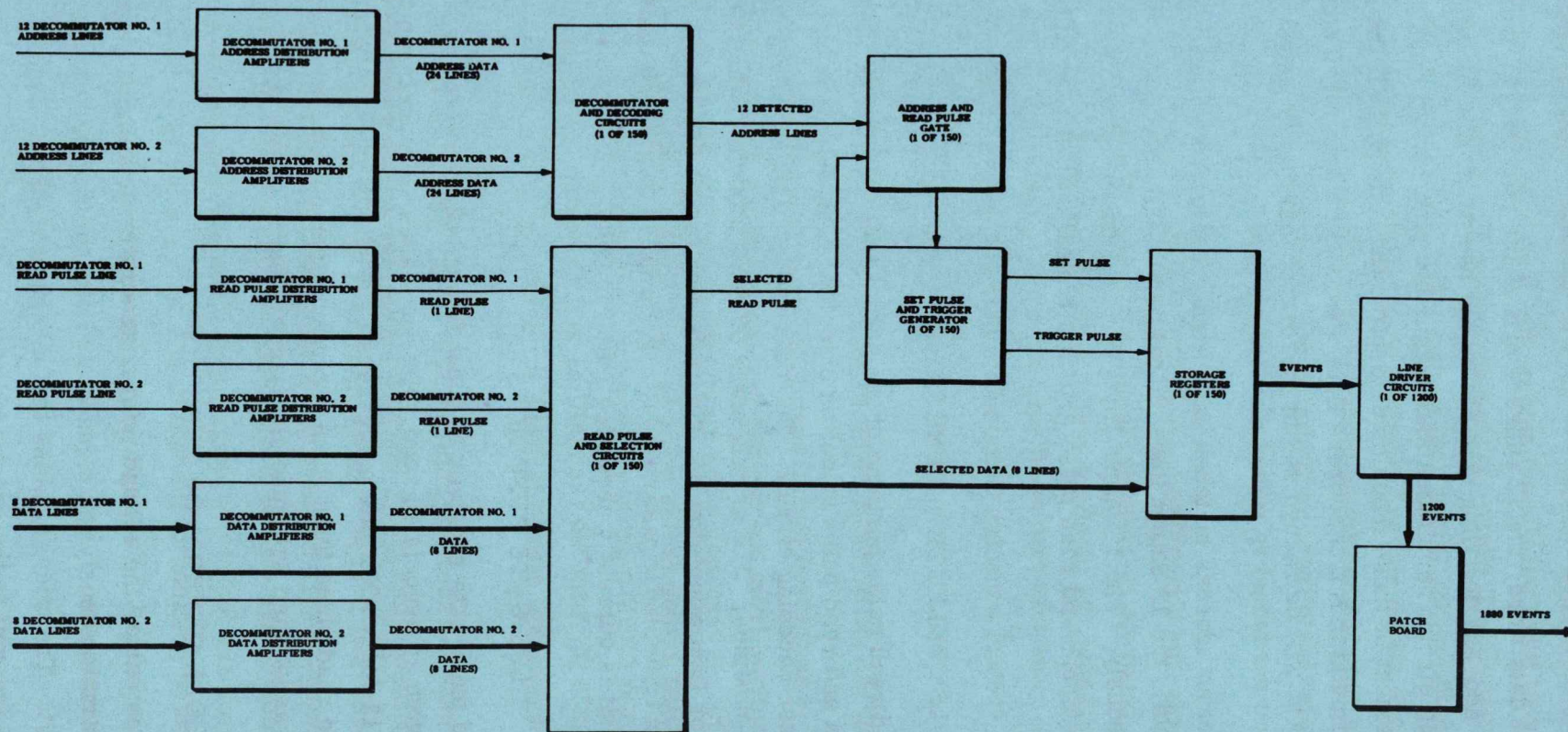


Figure 3. ESDU Block Diagram

ADDRESS DECODING FUNCTIONS

Upon receipt of a test data word, the 12 address bits of the word and their complements are fanned out to 150 address decoding circuits by the two-stage distribution amplifiers. Each address decoding circuit comprises four selectable plug-in logic modules. The selection and arrangement of these modules determine the following (1) the Decommulator No. 1 or Decommulator No. 2 address lines that will be monitored and (2) the 12-bit address code that will be recognized in the form of four binary-coded octal digits.

When the bit content of an address matches one of the preselected address codes set into the decoding circuit, the 12 output lines of that particular decoding circuit all will be a logic 0 simultaneously. The 12 output lines of each address decoding circuit are fed to an associated address and read pulse gate. A typical address decoding circuit is shown in Figure 4.

DATA AND READ PULSE SELECTION FUNCTIONS

The eight data bits and read pulse portions of the digital test data words received are distributed to 150 data and read pulse selection circuits. One selection circuit is associated with each address decoding circuit. The data and read pulse selection circuits consist of two jumper modules. The arrangement of these modules selects either the Decommulator No. 1 or Decommulator No. 2 data bits and read pulse to be passed. The decommutator input selected to pass is always the same as that which the associated address decoding circuit is currently accepting (see Figure 5).

ADDRESS AND READ PULSE GATE FUNCTIONS

Each address and read pulse gate receives 13 input lines: 12 representing a preselected octal address from an associated read pulse and data-selection circuit. The circuit functions as a 13-input AND gate and generates a "display" pulse whenever its associated address and read pulse input lines are simultaneously at logic 0. The display pulse is fed to an associated set pulse and trigger generator circuit.

SET PULSE AND TRIGGER GENERATOR FUNCTIONS

Upon receiving a display pulse, the set and trigger generator develops a set pulse. The set pulse is sent simultaneously to an associated storage register and to a trigger-pulse generating circuit. The trigger pulses that are generated are slightly delayed from the set pulse and are sent to the associated storage register.

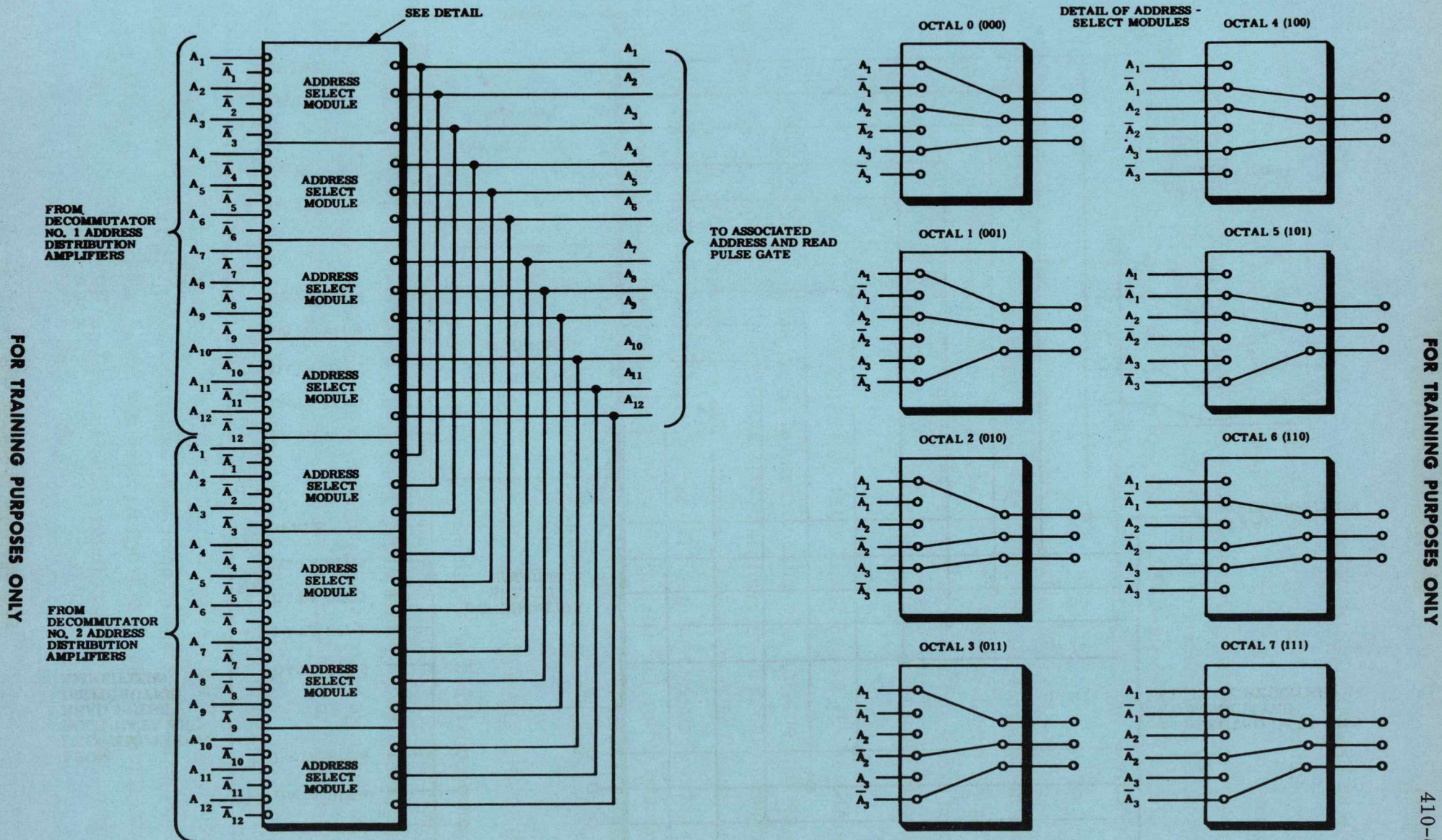


Figure 4. Typical Address Decoding Circuit

FROM
DECOMMUTATOR
NO. 1 DATA AND
READ PULSE
DISTRIBUTION
AMPLIFIERS

FROM
DECOMMUTATOR
NO. 2 DATA AND
READ PULSE
DISTRIBUTION
AMPLIFIERS

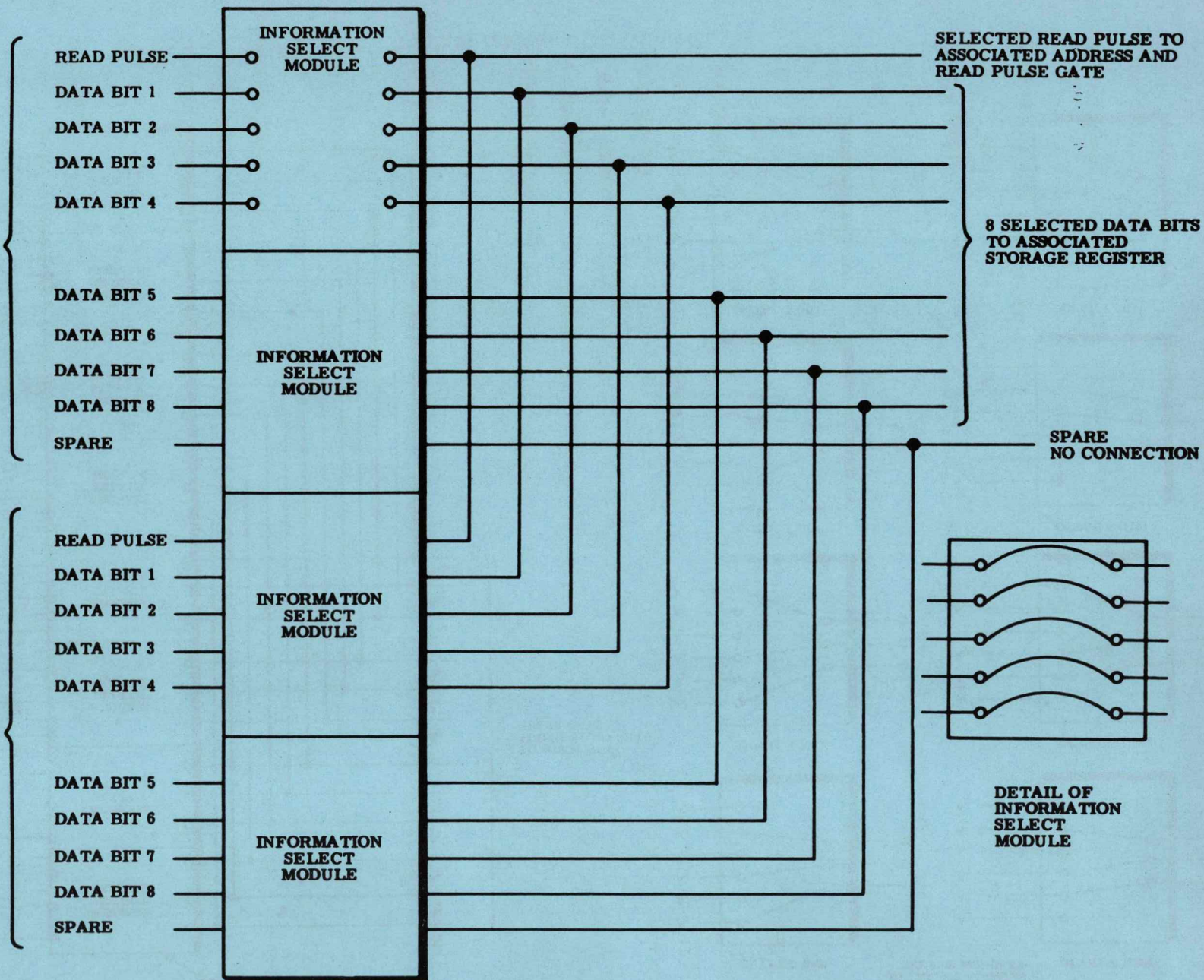


Figure 5. Typical Data and Read-Pulse Selection Circuit

STORAGE REGISTER FUNCTIONS

The ESDU contains 150 storage registers, one for each addressed data word that can be recognized and processed by the ESDU. Each storage register is composed of eight flip-flops (bistable multivibrators), one for each data bit of a selected word. Each flip-flop receives a set pulse, trigger pulse, and one of eight selected data lines. Upon receipt of a set pulse, all flip-flops of the storage register are cleared of past data. After being cleared, the trigger pulse and any selected data present are ANDed at the input of each flip-flop and are loaded into the storage register. The output of each flip-flop represents one discrete on-off event. A logic 0 indicates the event has occurred, while a logic 1 indicates the event has not occurred or has ceased.

LINE DRIVER FUNCTIONS

The "false" output of each storage register flip-flop is applied to the input of a logic inverting line driver and then to the distribution patchboard. The purpose of the line drivers is to provide (1) the capability to drive relatively long cables and (2) signal isolation prior to distribution by the patchboard. Since there are 150 storage registers supplying eight event outputs each, there are 1200 line drivers. It should be noted that because of inversion by the line drivers, the signals received by the patchboard will be the complement of the storage register output signals.

PATCHBOARD FUNCTIONS

The patchboard contained in the ESDU provides a flexible means to selectively distribute the event signals to appropriate control consoles. The patchboard can be removed and programed as required. The input to the patchboard is 1200 separate events. Each event is coupled to the output of the patchboard by means of plug-in jumper connections. To change the distribution of an event, the patchboard is removed from the ESDU and the appropriate jumper connections are made. After completing the necessary jumper changes, the patchboard is returned to the ESDU.

By means of branching connectors (commoning blocks or squids), a single event input may be coupled to the several patchboard output connections. Each patchboard output pin is connected via hardline to predesignated control consoles.

CONTROL CONSOLE FUNCTIONS

Figure 6 is a block diagram for a typical control console. The inputs to the console are (1) Events from the ESDU and (2) addressed data (event and analog intermixed)

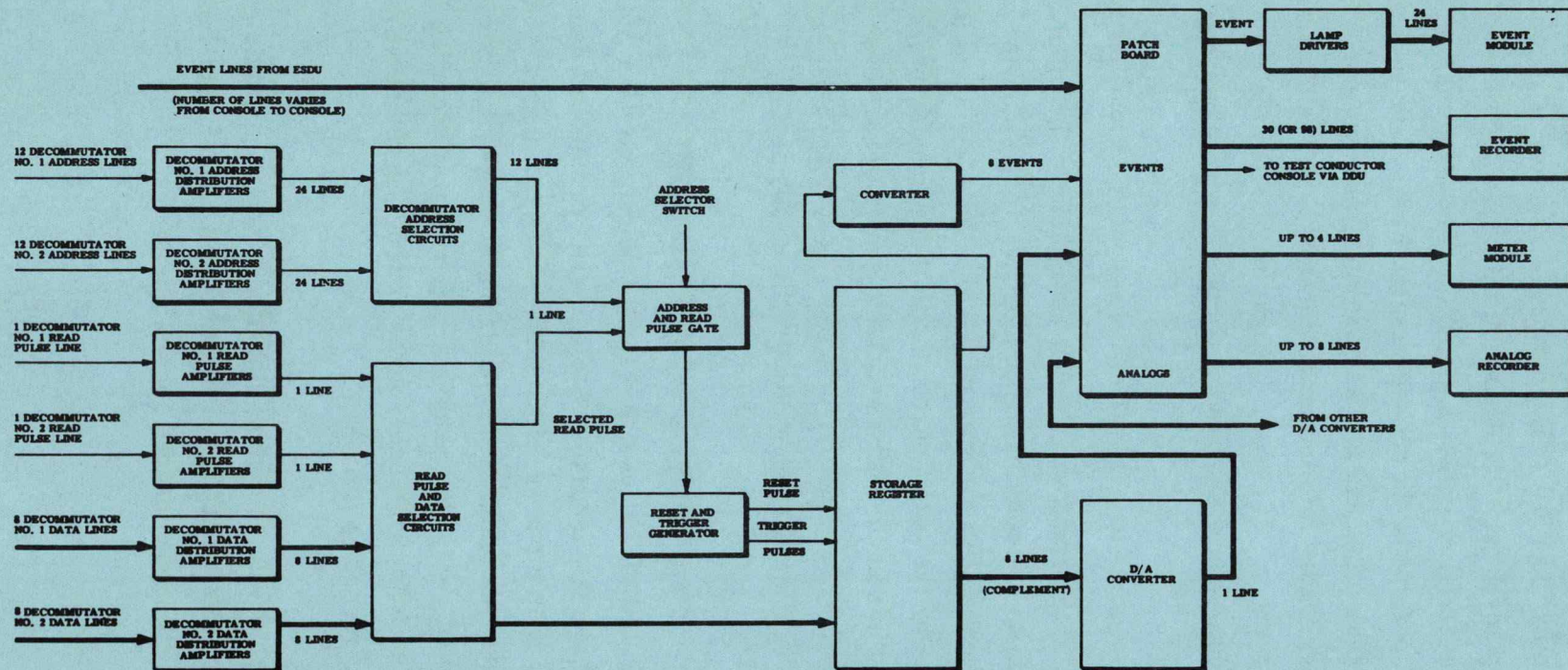


Figure 6. Typical Control Console Block Diagram

from the DDU. Each incoming event line is fed to a console patchboard. From the patchboard each event is routed to an associated lamp driver and/or event recorder channel for display. The analog words that are contained in the inputs from the DDU are recognized and stored. The recognition and storage process of analog data is the same as that used for event words in the ESDU. The exact number of analog words that can be accepted varies from console to console. The output of each storage register is applied to a D/A converter. All D/A converter outputs are fed to a console patch panel, which routes the analog signals to the appropriate meter module and/or analog recorder.

DIGITAL-TO-ANALOG CONVERTER

Each D/A converter receives eight binary bits from an associated storage register. A D/A converter is composed of eight voltage divider networks so connected as to form a resistive ladder (see Figure 7). Switching transistors control the input to each voltage divider network. The switching action is such that a logic 0 will cause -5 volts to be applied to a voltage divider and a logic 1 will ground the input to the voltage divider. The output of the D/A converter is taken across the entire resistive ladder. The voltage developed across the ladder will depend upon the bit combination received from the storage register. All "zeros" from the storage register will cause -5 volts to be developed across the ladder. This is the maximum voltage the D/A converter will produce.

CONVERTER CIRCUITS

The converter assemblies are special purpose and exist only in two of the control consoles, Power and Sequential System Console and the Communications Console. Each converter assembly contains eight identical converter circuits. Each converter circuit is composed of a NOR gate and a power inverter module. A typical converter circuit is illustrated in Figure 8.

As illustrated in Figure 8, the converter NOR gate monitors the "1" side of the three most-significant-bit flip-flops of an associated storage register. Whenever the input to the storage register is greater than 31 (00011111), at least one of the inputs to the NOR gate will be a logic 1. In this case, the NOR gate output will be a logic 0 that will be sent to the associated Power Inverter (PI) module. The PI module output then will be a logic 1 indicating that the parameter being monitored is above 12 percent of full scale (32 divided by 256). When the parameter being monitored is below 12 percent, the NOR gate output will be a logic 1 and the PI module output will be a logic 0.

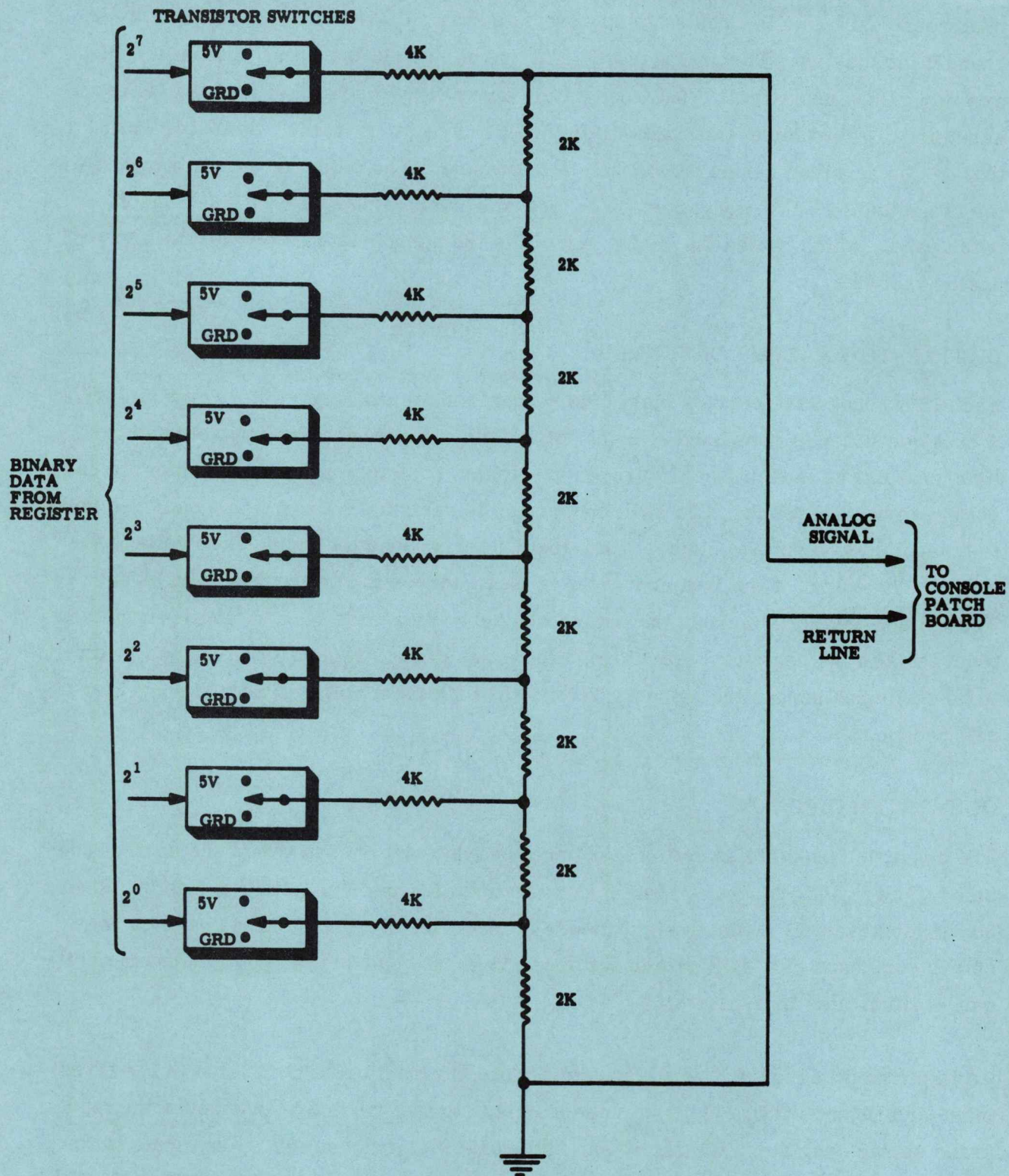


Figure 7. Typical D/A Converter Circuit

STORAGE REGISTER

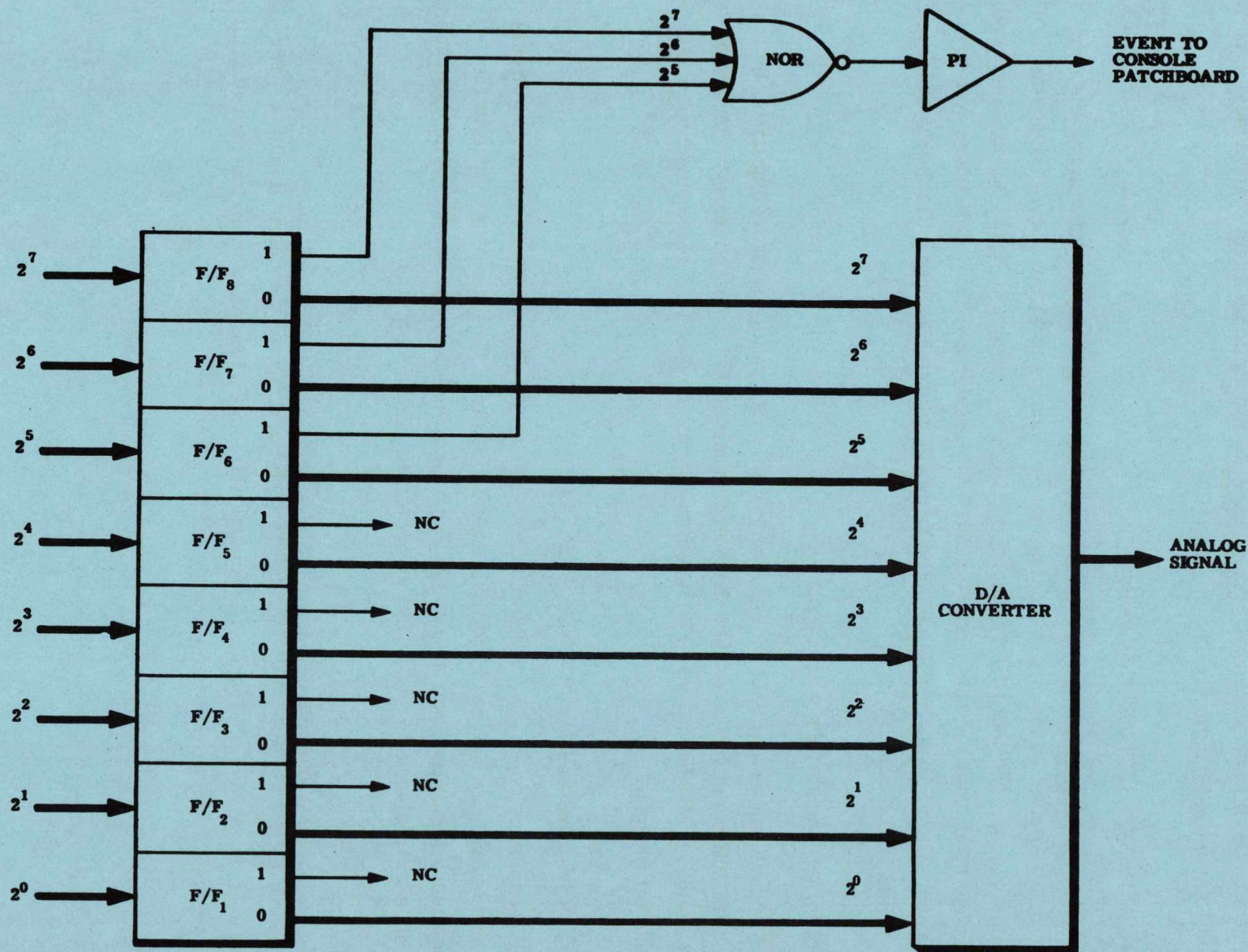


Figure 8. Typical Converter Circuit

The output of each converter circuit is treated as an event signal and is fed directly to the control console patchboard. At this point, the converter event signal is sent to an event module on that particular control console and/or to an event display device on the Test Conductor Console (TCC).

32-CHANNEL EVENT RECORDER

The 32-channel event recorder provides a means of permanently recording the time and duration of an event. It will accept and record up to 32 channels of event data simultaneously. In the ACE-S/C configuration, two channels (1 and 32) are reserved for time code data. All data is recorded in a continuous-write, deflection-type presentation. Chart speed can be selected from 12 available speeds. Useful frequency response is 100 cps.

100-CHANNEL EVENT RECORDER

The 100-channel event recorder is a write/no-write recorder providing on-off indicators for 100-event inputs (two of these are reserved for timing signals). Recording is done electrically on specifically sensitized paper. Maximum response time is 1.25 milliseconds.

8-CHANNEL ANALOG RECORDER

Selected analog data is recorded on eight-channel analog recorders. Two additional channels are provided for recording time code data. The record provided is the continuous-write, deflection variety. The recorders will operate at any of 12 speeds. Frequency response is flat to 75 cps and useful to 200 cps.

EVENT AND METER MODULES

Refer to ACE-S/C Operator's Manual for the operation of the meter modules. Section 1 of the ACE-S/C Operator's Manual will supply information on the operation of the various recorders located in the control room.

SUPPORT EQUIPMENT

OBJECTIVES

To familiarize the student with:

- a. Switching equipment function.
- b. Timing group equipment function.
- c. MILA related equipment function.
- d. Computer peripheral equipment function.

INTRODUCTION

This document will attempt to relate the various pieces of support equipment to the overall operation of the ACE-S/C ground station. The discussion on the support equipment will be broken down into four general areas:

- a. Automatic switching equipment.
- b. Timing group equipment.
- c. Merritt Island Launch Area (MILA) peculiar equipment.
- d. Computer peripherals.

EXPLANATION

SWITCHING EQUIPMENT

The ACE-S/C switching system is an addition to the ACE-S/C ground station designed to provide fast, accurate, reliable switchover of the various major components of the ground station. It provides easy access of any control room to any computer room and any computer to any one of ten test areas. In addition, it allows for the association of any CUE or DCCU to any control or computer room.

The switching system consists of a switching group, a power group, and a patching group. Figure 1 is a block diagram of the ACE-S/C switching system.

Switching Group

The switching group permits four discrete groups of cables, from as many as five separate ACE-S/C ground stations to be properly connected within a station or

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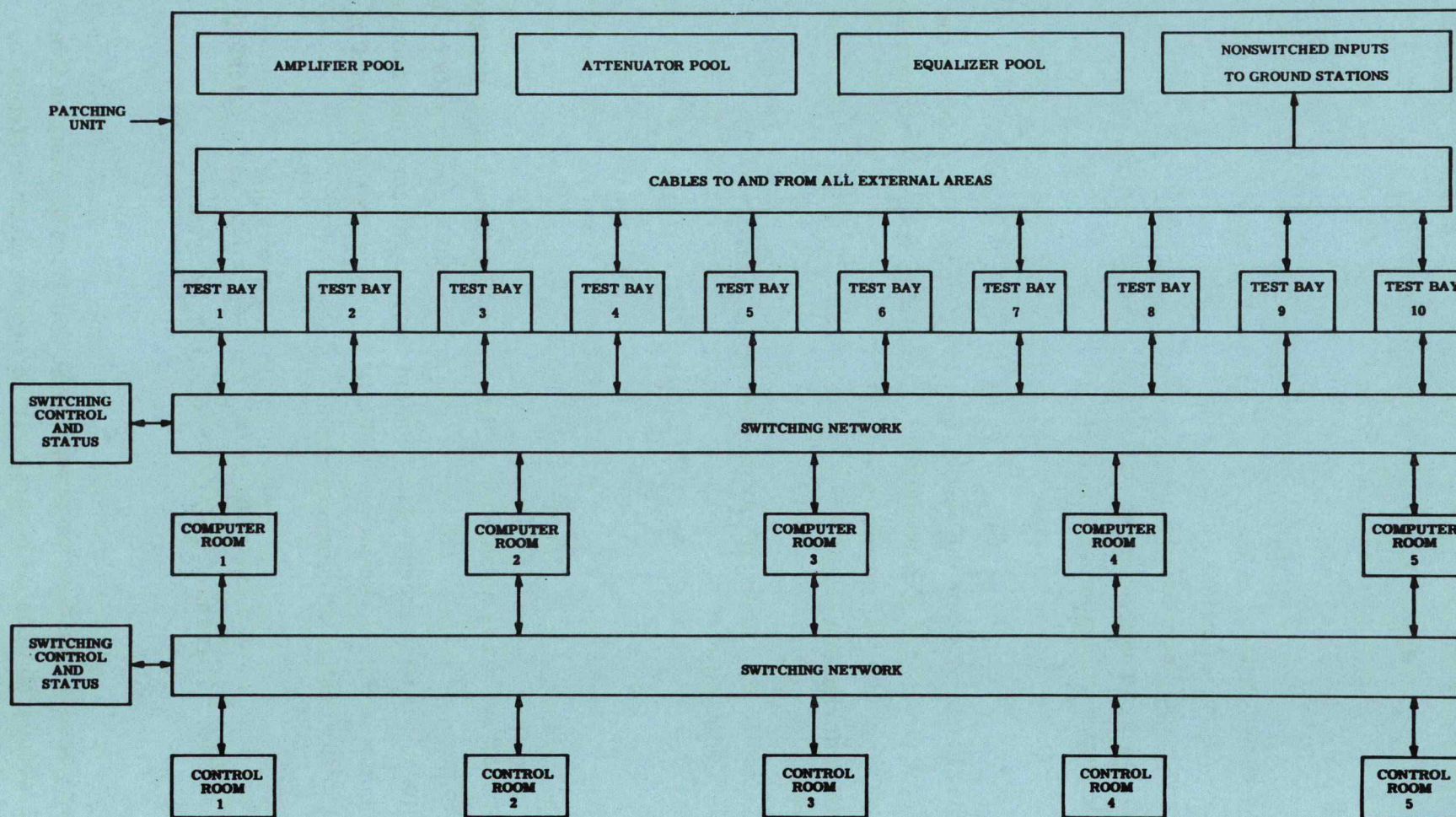


Figure 1. ACE-S/C Switching Facility, Block Diagram

cross-connected between stations. Each group of cables is connected by means of a pushbutton control panel that activates reed relay switches. The following four functional cable groups may be connected to the appropriate termination points within an ACE-S/C station or cross-connected to similar terminations at any of four other ACE-S/C stations:

- a. Cables that carry signals to and from spacecraft test areas and are routed between the Systems Patch Terminal Unit and the ACE-S/C Station Computer Room.
- b. Cables that link an ACE-S/C Control Room to an ACE-S/C Computer Room.
- c. Cables that insert a selected CUE unit between a previously selected computer/control room combination.
- d. Cables that insert a selected DCCU between a previously selected computer/control room combination.

There are four control unit panels located on the switching unit (240): one for each of the four switched cable groups. Each control unit panel contains pushbutton switches arranged in a matrix format to permit selection of any switching arrangement of the respective cable group.

Figure 2 illustrates the computer room to control room control unit panel pushbutton matrix. The panel contains 25 pushbuttons arranged in rows and columns of five each (5 by 5). Each pushbutton contains a two-digit number to indicate the switching configuration that may be achieved by depressing that pushbutton. The first digit on each pushbutton indicates the control room selected while the second digit designates the computer room to which the other end of the cable group will be terminated. This two-digit nomenclature is a standard switching matrix designation where the first digit always represents the row and the second digit denotes the column.

As an example, the top row of pushbuttons, as illustrated in Figure 2, permits a control room designated as number one to be connected to any one of five possible computer rooms. It should be noted that the left column of pushbuttons permits the computer room, designated as number one, to be connected to any one of five possible control rooms.

The test area to computer room control unit panel contains a 5 by 10 pushbutton matrix (Figure 3). This is provided to facilitate switching ten groups of spacecraft test area signal cables from the Systems Patch Terminal Unit to as many as five ACE-S/C

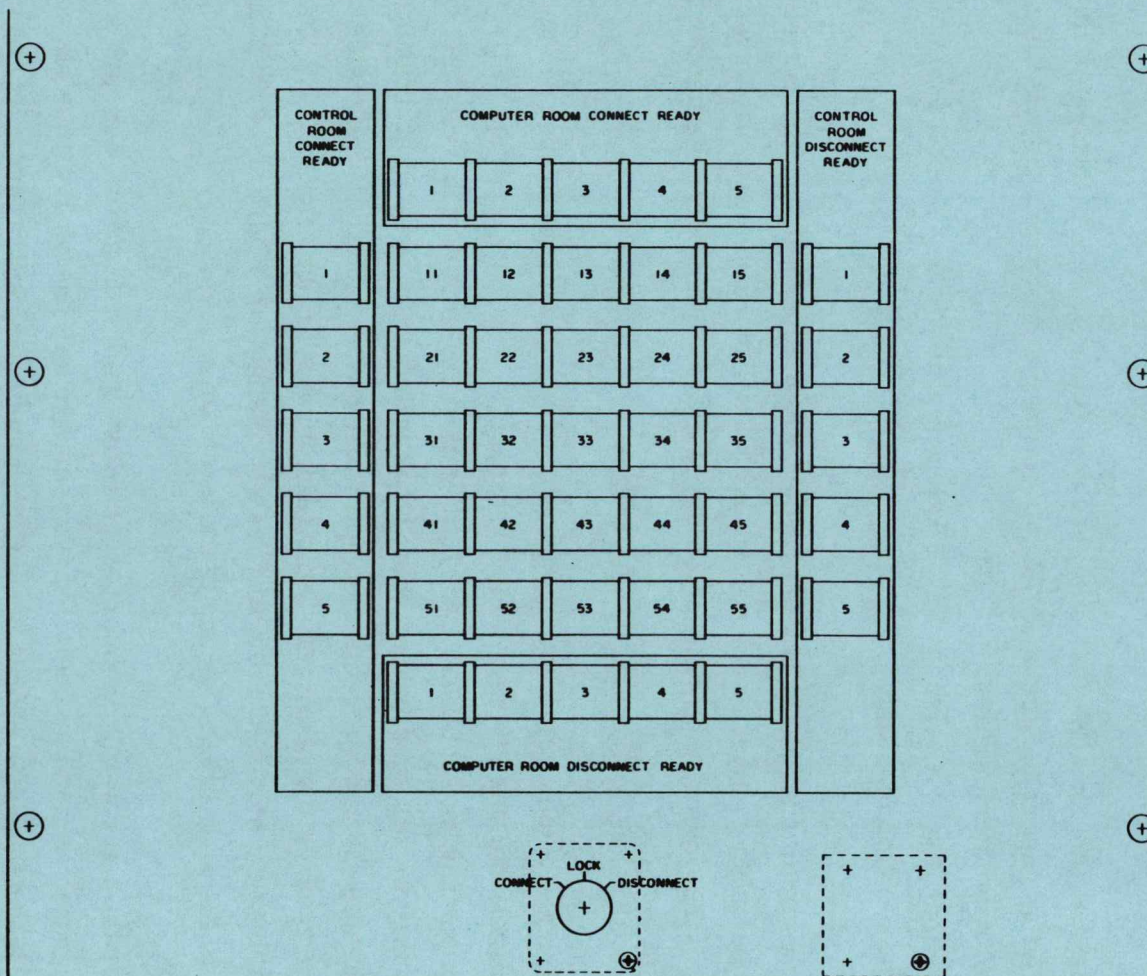


Figure 2. Computer Room to Control Room Control Unit Panel Pushbutton Matrix

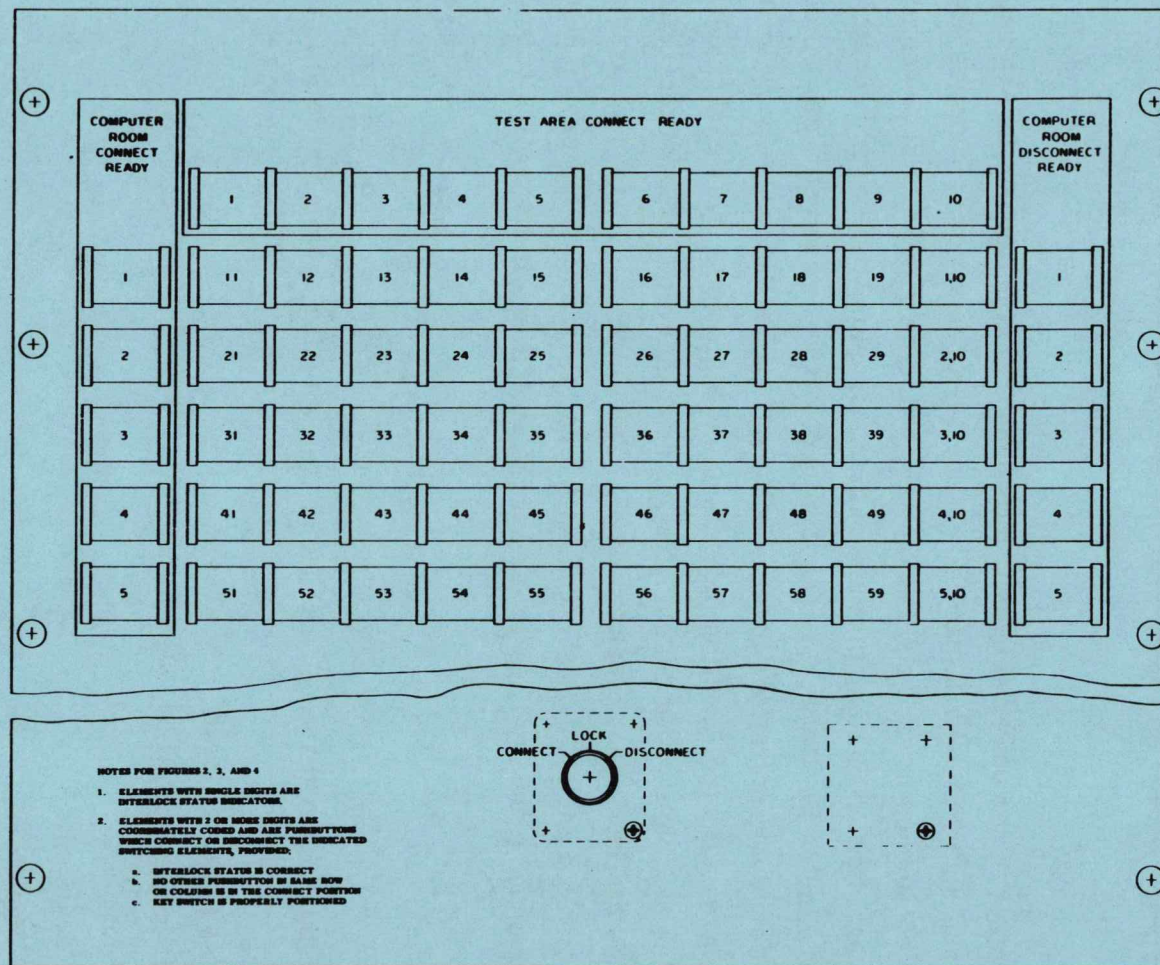


Figure 3. Test Area to Computer Room Control Unit Panel Pushbutton Matrix

computer rooms. The principles of a 5 by 10 switching matrix are similar to those of a 5 by 5 matrix except that there are ten columns of five switches each instead of just five columns.

Control unit panels are also provided to permit the switching of various combinations of CUE's and DCCU's with the control room and computer room selections. These control unit panels contain 5 by 5 pushbutton matrixes as illustrated in Figure 4.

Power Group

The power group provides power supplies, nickel-cadmium batteries, inverters, and power control and status indication panels. Three 50-ampere power supplies provide the worst case continuous power required for the switching group. Nickel-cadmium batteries, through diode isolation, provide continuous, automatic power backup for a minimum of 30 minutes for the worst case continuous power requirements, which includes five complete configurations made, continuous operation, constant relay board status indication, and control function indication and operation. This backup duration increases rapidly as these worst case conditions are removed. An additional benefit of reed relays is the low "must break" voltage. This further increases the configuration operate time on a backup status. The inverters operate from battery dc supply or battery backup and provide all ac power for the amplifiers in the switch unit and patch group.

Patching Group

The patching group increases the flexibility of the switching system in the following manner:

- a. Accepts inputs from the test areas.
- b. Conditions these inputs as required.
 - (1) Amplifies.
 - (2) Equalizes.
 - (3) Attenuates.
 - (4) Matches impedance.
- c. Splits inputs to more than one recipient if required.
- d. Makes possible the inputting of like signals from more than one test area to one ground station.

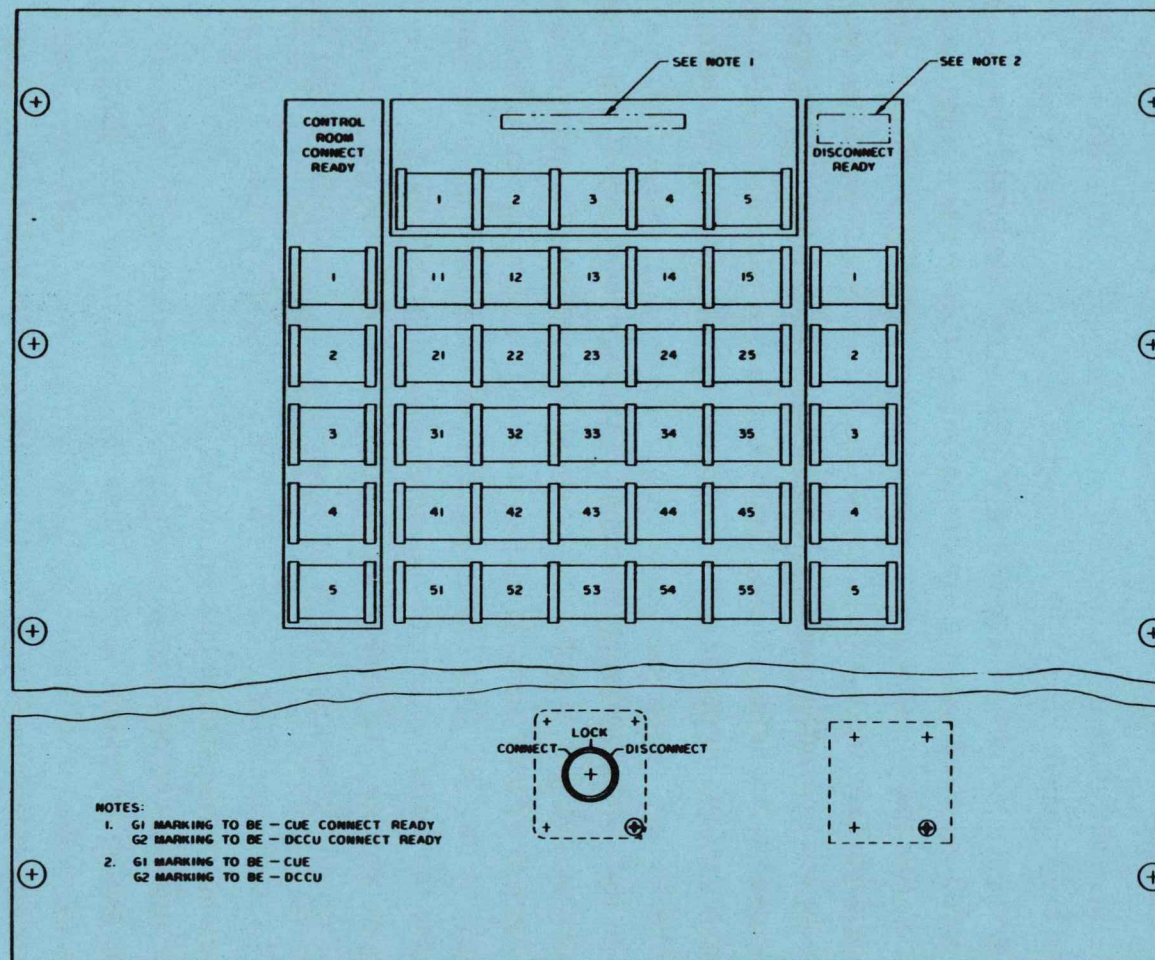


Figure 4. Control Room to DCCU or CUE Control Unit Panel Pushbutton Matrix

The operational usage of the equipment is as follows:

- a. To connect a control room to a computer room (reference Figure 2).
 - (1) The test conductor determines that the control room is operational. He then activates the "control room connect ready" circuit by depressing the "connect ready initiate" switch on the test conductor console.
 - (2) The computer console operator determines that the computer room is ready to go "on line."

He then activates the "computer room connect ready" circuit by depressing the "connect ready initiate" switch on the computer complex console.
 - (3) Once steps (1) and (2) are completed and upon command from the test conductor, the switching system operator inserts a key in the control room/computer room control panel, moves it to the "connect" position and depresses the switch in the matrix to connect the specified control room and computer room. He then moves the key back to the lock position and removes it. The configuration is then established and interlocked.
- b. To connect a CUE or DCCU to the computer room/control room combination (Figure 4):
 - (1) The test conductor must have given a connect ready signal that is combined in the control logic with a signal generated by the control room/computer room crosspoint being made. This combination actuates a light on the CUE (DCCU) control panel entitled "control room ready."
 - (2) Once the maintenance man has determined that the CUE (DCCU) is ready to go "on line," he depresses a switch on the CUE (DCCU) rack that actuates a light on the control panel entitled "CUE (DCCU) connect ready."

These are most likely operational status indications that will normally indicate ready with no special action.
 - (3) Once these two lights are lit and upon command from the test conductor, the switching system operator inserts the key in the CUE (DCCU) control panel, moves it to the connect position, and actuates the required matrix crosspoint to connect the specified CUE (DCCU) and control room. The other side of the CUE (DCCU) is automatically configured to the computer room connected to that control room by the control logic. He then moves the key to the lock position and removes it.
- c. To connect a test area to a computer room (Figure 3). Prerequisites are as follows:
 - (1) Control room/computer room connected.
 - (2) CUE connected (verified via intercom).

- (3) DCCU connected (verified via intercom).
- (4) Computer room programed and ready to accept data.

Once the prerequisites are met, the computer console operator actuates the "computer room connect ready" light on the computer room/test area control panel by depressing the "test area connect ready" switch on the computer complex console.

Once the switching operator completes and checks the patch unit connections for the test configuration, he actuates the "test area connect ready" light on the computer room/test area control panel by depressing the proper test area connect ready switch on the patch unit.

This test area connect ready signal indicates operational status and may be normally "on" for extended periods of time.

Once these two lights are lit and upon command from the computer console operator, the switching system operator inserts the key in the computer room/test area control panel, moves it to the connect position and actuates the crosspoint to connect the specified test area and computer room. He then moves the key to the lock position and removes it.

This describes the connection for one ACE-S/C ground station. It is now so configured and interlocked that no one can remove any component of the system without the test conductor's permission. Depressing any matrix crosspoint pertaining to any component that has been configured in this discussion will cause nothing to happen.

The following steps are required to disconnect a test configuration:

- a. To disconnect a test area -
 - (1) Upon receipt of verbal instruction from the test conductor, the computer console operator actuates the "computer room disconnect ready" light on the computer room/test area control panel by depressing the "test area disconnect ready" switch on the computer console.
 - (2) The switching system operator then inserts the key, moves it to the disconnect position and actuates the matrix crosspoint, thereby disconnecting it.
- b. To disconnect a CUE or DCCU -
 - (1) The test conductor actuates the "control room disconnect ready" light on the control room/computer room, control room/CUE, and control

room/DCCU panels by depressing the "control room disconnect ready" switch on the test conductor's console.

- (2) The switching system operator then inserts the key, moves it to the disconnect position and actuates the matrix crosspoint, thereby disconnecting the respective CUE or DCCU only.

The CUE and DCCU can also be automatically disconnected by procedure c.

- c. To disconnect a control room or computer room -

- (1) The test conductor extends a "control room disconnect ready" light.
- (2) The computer console operator extends a "computer room disconnect ready" light.
- (3) The switching system operator then inserts the key in the control room/computer room control panel, moves it to the disconnect position and depresses the matrix crosspoint, thereby disconnecting the control/computer room plus the associated CUE and DCCU if they are not already disconnected.

The following steps are required to replace a defective CUE or DCCU while maintaining the operational integrity of the ACE-S/C ground station.

- a. The test conductor extends a "disconnect ready" signal that appears on the control room/computer room, control room/CUE and control room/DCCU control panels.

Note

The control room/computer room control panel is still interlocked since no disconnect ready signal has been received from the computer console operator.

- b. The switching system operator then uses the key and disconnects the matrix crosspoint.
- c. The test conductor then extends a connect ready signal.
- d. If it is not already on, the maintenance man extends a connect ready from the new CUE or DCCU to be used after he determines that it is operational.
- e. The switching system operator then operates the key and depresses the matrix crosspoint to connect the new CUE or DCCU into the circuit. He then removes the key and the new test configuration is operational, after validation of the new component.

TIMING GROUP EQUIPMENT

The acceptance checkout equipment - spacecraft (ACE-S/C) timing equipment consists of a time code generator, a countdown generator, a universal tape search system, and

a countdown time input/output synchronizer. The universal tape search system also contains a synchronizer that is utilized as a real-time input/output synchronizer. The primary function of timing equipment in the ACE-S/C ground station is the correlation of command data, spacecraft test data, and operational test sequences.

Three time codes are generated by the timing equipment:

- a. AMR "B-1" time code.
- b. IRIG Format "B" time code.
- c. ACE-S/C Countdown time code.

Also available within the ACE-S/C is a special time code that can be utilized during special testing and maintenance testing.

Although both real-time and countdown-time codes are necessary in the correlation of data, no central time unit is needed to facilitate the generation and transfer of commands or the transfer and processing of test data.

The time code generator generates Inter-Range Instrumentation Group (IRIG) Format "B" time code and the AMR "B-1" time code (see Figure 5). The IRIG code is used for data correlation on the high-speed recorders, and the AMR time code is used for data correlation on the slow paper recorders. The countdown generator generates the ACE-S/C countdown time code that is used for test correlation and can also be used to correlate test data in respect to real time. The universal tape search system electrically positions a magnetic tape transport to a predetermined point on the test tape for playback of test data. The input/output synchronizer performs the function of making available to the uplink and downlink computers real time and countdown time on an as-required basis.

The IRIG "B" real time is sent to wall clocks to display in decimal form the time of year to one second and to the consoles as range time to display also in decimal form the time of year to one second. The IRIG "B" is sent to a time code distribution unit where it is disseminated to the following equipment:

- a. Oscillograph recorder.
- b. Video distribution and tape transport control.
- c. Tape recorder/computer time decoder and search unit.

During a magnetic tape playback operation the IRIG "B" time code distributed to the tape recorder/computer time decoder and search unit to be used by the universal tape

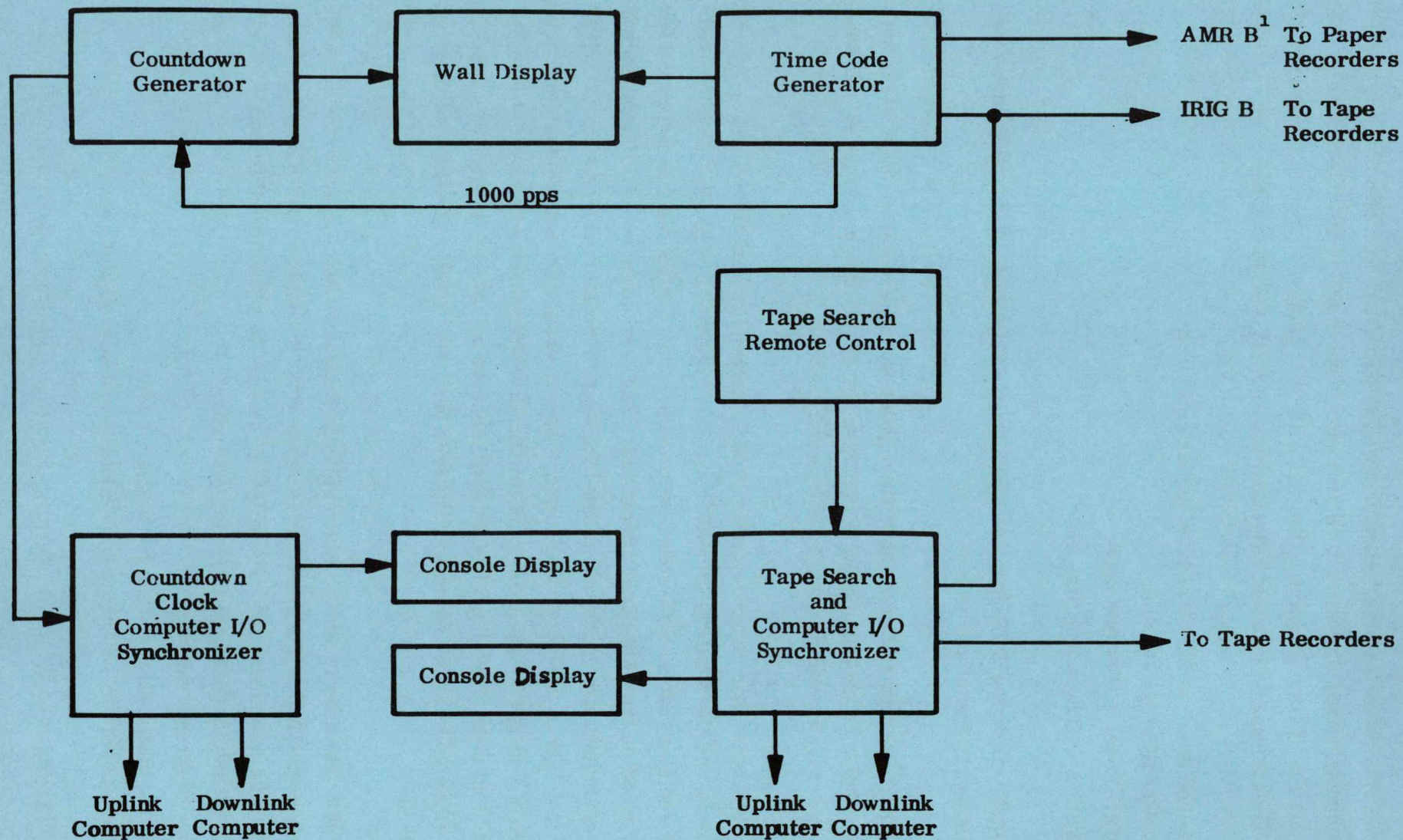


Figure 5. Timing System Block Diagram

search system in positioning the magnetic tape transport, to the input/output synchronizer for computer real/playback time and to the consoles as range/playback time.

The Time Code Generator, Model 6190, is located in the terminal facility room and is used to synchronize the countdown generator. In a two-station configuration only one time code generator is utilized. It synchronizes the countdown generators for both stations to an on-time accuracy of one millisecond. The countdown generator generates AMR "B-1" and the IRIG Format "B" time codes.

The Countdown Generator, Model 6350, also located in the terminal facility room, is physically a part of the two-station time generation equipment. The synchronization of the countdown generator to the time code generator is performed automatically; however, the start and stop of the generator is performed manually by either local or remote controls. The remote controls are located on the test conductor console and all countdown time functions during spacecraft tests are performed by the test conductor. The ACE-S/C countdown time code is a modified IRIG Format "B" time code.

The Countdown Time Input/Output Synchronizer, Model 6580, located in the computer room, is designated Countdown/Computer Interface/Translator, Unit 177. It is the function of this unit to make available to the ground station's uplink and downlink computers countdown time in binary form and at any time so designated by the computers. The countdown input/output synchronizer receives time from the countdown generator.

The Universal Tape Search System (UTSS), Model 6222, located in the computer room, is designated the Tape Recorder/Computer Time Decoder and Search Control Unit No. 116. The UTSS also contains a real time input/output synchronizer, which has the function of making available to the ground station's uplink and downlink computers real time in binary form and at any time so designated by the computer. The tape search system interfaces with the Ampex analog magnetic tape recorders and is used to position the tape to a designated prerecorded point for playback operations. The system uses IRIG "B" real-time information to perform the search positioning function and during playback modes the IRIG "B" real time previously recorded on the tape is displayed on the test conductors console as range time.

The time code generator is the basis for the ACE-S/C timing equipment and may (depending upon the requirement) be in synchronization with WWV or some Government time standard. The output of the generator consists of the following time

codes: AMR "B-1" and IRIG "B." The system generates the time by the use of Decimal Counting Units (DCU) and displays the contents in decimal form via "nixie" displays. The IRIG "B" time code is available in BCD and straight binary; BCD indicates time of year to a second and straight binary indicates time of day to a second. The AMR "B-1" time code is available only in straight binary and indicates time of day to a second.

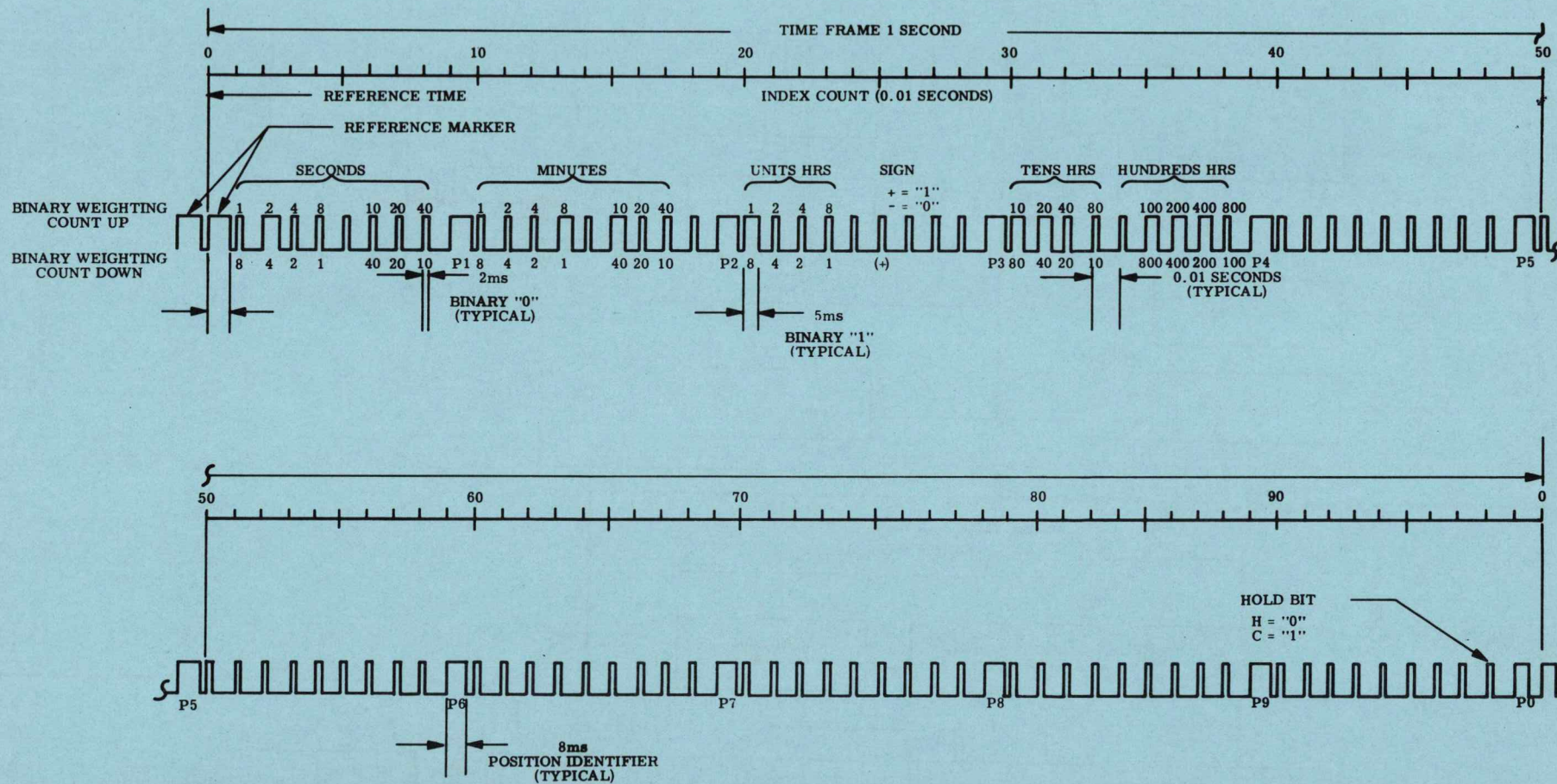
The basic counting devices in the time code generator are the decimal counting units. These counters are connected in cascade form and are called minor, major, and days time counter. The minor time counter produces one pulse each second at the output for each 100,000 input pulses. The major counter produces one pulse each day with a one pulse-per-second input signal. The days counter counts the days pulses.

The Countdown (C/D) Generator generates the ACE-S/C countdown time code as shown in Figure 6. It also generates the countdown time displayed on the wall displays and console displays. The countdown time is synchronized to the time code generator by a 1-kc square-wave signal. The countdown generator generates time data from minus 999 hours, 59 minutes, and 59 seconds to plus 999 hours, 59 minutes, and 59 seconds.

It also generates a sign to distinguish between countdown time and countup time. During any moment that the time is disabled, a "hold" indication will replace the + or - sign.

The Computer Countdown Time Input/Output Synchronizer is a time-sharing device that provides the uplink and downlink computers with countdown time. The synchronizer transfers time to the computer upon request, and upon coincidence of countdown time and a preset time, it will interrupt the computer to enable a preprogrammed subroutine to be performed. The input/output synchronizer receives the ACE-S/C countdown serial-modulated time code from the countdown generator, decodes, and translates the incoming signal to produce a binary word for use by the computer (see Figure 7).

The uplink computer uses countdown time to time-tag commands, which are recorded on magnetic tape. Therefore, time must be available for transfer from the synchronizer to the computer at all times during testing. The binary information representing hours, minutes, and seconds is transferred to the computer as two 12-bit parallel words. Word one contains the current seconds and minutes, and word two contains the current hours and the sign denoting countup time or countdown time. To request and



The ACE Countdown Time Code is a modification of the standard IRIG-Format B. Countdown time in Sec., Min., Hr. is represented in BCD, 8-4-2-1 form. Two formats are actually used - during count up (+) the format is scanned least significant bit first for each sub-word. In the count down (-) mode the format is scanned most significant bit first in each sub-word.

Figure 6. ACE-S/C Countdown Time Code Format

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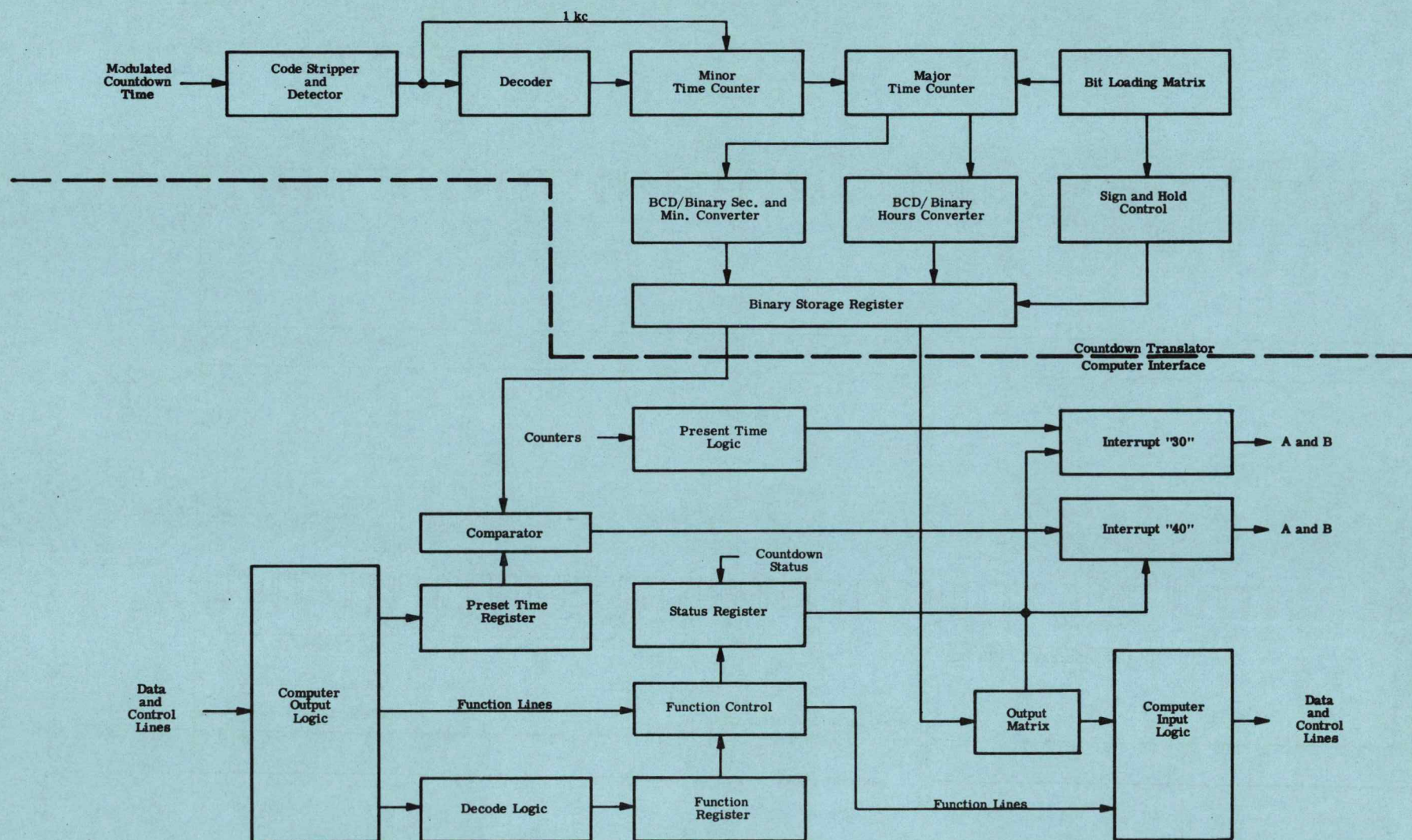


Figure 7. Input/Output Synchronizer

transfer the time, the computer (whether uplink or downlink) must use the external function control-word and control-line method to effect the transfer.

A second function of the input/output synchronizer is to interrupt the computer when countdown time corresponds to a preset time. This can be performed either by manually inserting into the synchronizer the preset time or from the computer through preprogramed routines. Both methods can be used during a countdown or a test. If countdown time corresponds to the manually preset time, an Interrupt 30 will be generated by the synchronizer, and if countdown time corresponds to the preset time specified by the computer, then an Interrupt 40 will be generated.

The Model 6580-600 Countdown Time Input/Output Synchronizer consists of two separate units: (1) a countdown time code translator and (2) an input/output synchronizer for two CDC 160G general-purpose computers. The two units are housed together for reasons of power supply and interface economy.

The UTSS receives serial time code information from a magnetic tape unit. The tape search unit compares the current time value recorded on the tape with a preset value of time and issues appropriate control signals to a magnetic tape transport unit. The control signals issued are used to start, stop, and control the search and playback drive of a tape transport. Thumbwheel switches are available on the tape search control unit to preset the desired playback start/stop time values. The search time resolution provided by the thumbwheel switches is days, hours, minutes, and seconds. The tape search control unit compares the time code preset into the thumbwheel switches with the time code recorded on a magnetic tape and instructs the tape transport to search in a forward or reverse direction for the location of the start time. When the start time is located, the tape search control unit instructs the tape transport to playback in the forward direction until the stop time is reached.

A tape search control unit mode selector switch is provided to select any one of four operating modes.

- a. Recycle Mode - In the recycle mode, the tape search control unit will cause a tape transport to search in the conventional manner to the preset start time and then automatically reproduce (play back) to the preset stop time. This process will continue until a new control instruction is set into the tape search control unit.

- b. Single-Cycle Mode - In the single-cycle mode, the tape search control unit functions the same way as in the recycle mode except that it halts the tape transport being controlled when the preset stop time is reached.
- c. Search-to-Start Mode - The search-to-start mode is similar to the single-cycle mode except that the tape transport being controlled is halted when the preset start time is reached. To cause the tape transport to commence playback operation toward the preset stop time, the unit must be placed in the playback mode.
- d. Playback Mode - In the playback mode the tape unit starts and plays back the tape until the end of the tape is reached.

The UTSS contains an I/O synchronizer for use by the computers (uplink and downlink) during a tape playback operation. The I/O synchronizer gives IRIG "B" real time to either computer upon request. During a normal operation, i.e., when the Ampex tape recorders are in a record mode, the IRIG "B" real time is not made available to the computers.

The input/output synchronizer in the UTSS operates in the same manner as the countdown time Input/Output Synchronizer, Model 6580-600. However, the synchronizer in the UTSS obtains time from the time code generator and does not have the preset digital switches available to the operator for manual interrupt time.

The UTSS also contains circuitry for developing a serial time code of variable frame lengths to be used by the operator in special tests and various specific applications primarily during equipment maintenance operations.

The time codes generated by the timing equipment (AMR "B-1," IRIG "B," and ACE-S/C countdown time) are distributed to various equipment in ACE-S/C as shown in Figure 5. The input/output synchronizer performs the function of making available to the uplink and downlink computers real time and countdown time on an as-required basis.

IRIG "B" Real-Time Distribution

The IRIG "B" real time is sent to wall clocks to display in decimal form the time of year to one second and to the consoles as range time to display also in decimal form

the time of year to one second. The IRIG "B" is sent to a time code distribution unit where it is disseminated to the following equipment:

- a. Oscillograph recorder.
- b. Video distribution and tape transport control.
- c. Tape recorder/computer time decoder and search unit.

IRIG "B" Playback Time Distribution

During a magnetic tape playback operation the IRIG "B" time code is distributed to the tape recorder/computer time decoder and search unit to be used by the UTSS in positioning the magnetic input/output synchronizer for computer real/playback time and to the consoles as range/playback time.

AMR "B-1" Real-Time Distribution

The AMR "B-1" time code is disseminated to the following units to be recorded for data correlation:

- a. Strip chart recorders.
- b. Analog recorders.
- c. Video distribution and tape transport control.
- d. Oscillograph recorder.

AMR "B-1" playback time, that time recorded on the magnetic tape recorders, is distributed to the following units:

- a. Strip chart recorders.
- b. Analog recorders.
- c. Oscillograph recorder.

ACE-S/C countdown time code is displayed on wall clocks indicating countdown time to one second and is distributed to the following units to be used in data and test correlation:

- a. Computer input/output synchronizer.
- b. Magnetic tape transports.
- c. Test conductor console.
- d. Computer complex console.

ACE-S/C countdown time code is distributed to the following units during a playback operation:

- a. Test conductor console.
- b. Computer input/output synchronizer.

- c. Computer complex console.
- d. FM discriminators.

The ACE-S/C system employs five wall clock display units, three in the control room and two in the computer room and two console clocks. Each wall clock contains two sets of in-line decimal display of real time (actual or range time) and one set for the display of countdown time. The console clocks display either real or countdown time.

The real-time wall clock displays always show the current time of day or range time, never playback real time. The real-time wall clock display units consist of nine decimal in-line indicators: three for day, two for hours, two for minutes, and two for seconds.

The countdown time wall clock displays always show current countdown time, never playback countdown time. The countdown wall clock display units consist of eight in-line decimal indicators: two for seconds, two for minutes, three for hours, and one to indicate plus, minus, or hold.

Both the computer complex console and the test conductor console contain front panel mounted real and countdown clock display subassemblies. The console real-time clock display units are capable of showing either current range time or the playback range time depending upon the present ACE-S/C operational mode. In like manner, the console countdown time clock display units are capable of showing either the current countdown time or playback time. The same number and type of indicating device as are used in the console clocks are used in the wall clock displays.

MERRITT ISLAND LAUNCH AREA PERIPHERAL EQUIPMENT

The following description paragraphs are applicable only to the ACE-S/C ground stations that are installed at the Merritt Island Launch Facility.

The ACE-S/C has the functional responsibility of performing a checkout of the entire Apollo spacecraft. Because of the complexity of the testing and the total number of parameters to be processed from each subsystem, the spacecraft is functionally divided into two categories for checkout operations - Command/Service Module (CM/SM) and Lunar Excursion Module (LEM). Two ACE-S/C stations are provided to perform this checkout function.

The Saturn launch vehicle checkout is performed simultaneously with the spacecraft checkout, utilizing a different type of system. The checkout philosophy of the launch vehicle is different and the degree and complexity somewhat less than that of the spacecraft. The launch vehicle is of a standard booster configuration designed to boost a given spacecraft on a given mission. The Apollo spacecraft is designed for a particular mission and therefore must be man-rated to perform that mission, thus, the different philosophy and complexity of checkout.

However different, the checkout of the two vehicles must be integrated and highly coordinated during the final stages of prelaunch testing.

Blockhouses 34 and 37, Launch Control Center (LCC) 39, and the Operational and Control (O&C) Building contain the equipment necessary to perform the checkout integration of the launch and spacecraft vehicles.

During final prelaunch testing and countdown, the two ACE-S/C ground stations will be performing their separate functions of CM/SM and LEM checkout. These systems will be integrated and coordinated by the equipment remoted in the blockhouse. This integration must function in this manner because each ground station is operating under a different internal program control designed to check out two unrelated functional spacecraft subsystems. Additionally, during prelaunch testing and countdown, one of the ACE-S/C ground stations will be in direct communication with the launch vehicle checkout computer to perform programed coordination activities such as milestones and various selected event data. The functional relationship here is to coordinate the spacecraft and launch vehicle checkouts within milestone events, thereby resulting in a more highly integrated prelaunch test rather than coordination of subsystem Go/No Go status.

These methods of integration and coordination between the spacecraft checkout systems and the launch vehicle checkout system provide for a more unified checkout of the equipment as a system, thereby producing a more capable and more reliable vehicle to perform mission objectives (see Figure 8).

There is a direct link between the ACE-S/C (MILA) ground stations in the O&C Building and the peripheral equipment in Blockhouses 34 and 37 and LCC 39. Both Command/Service Module and Lunar Excursion Module checkout data will be transmitted and displayed simultaneously within the capacities of the transmission equipment (see Figure 9).

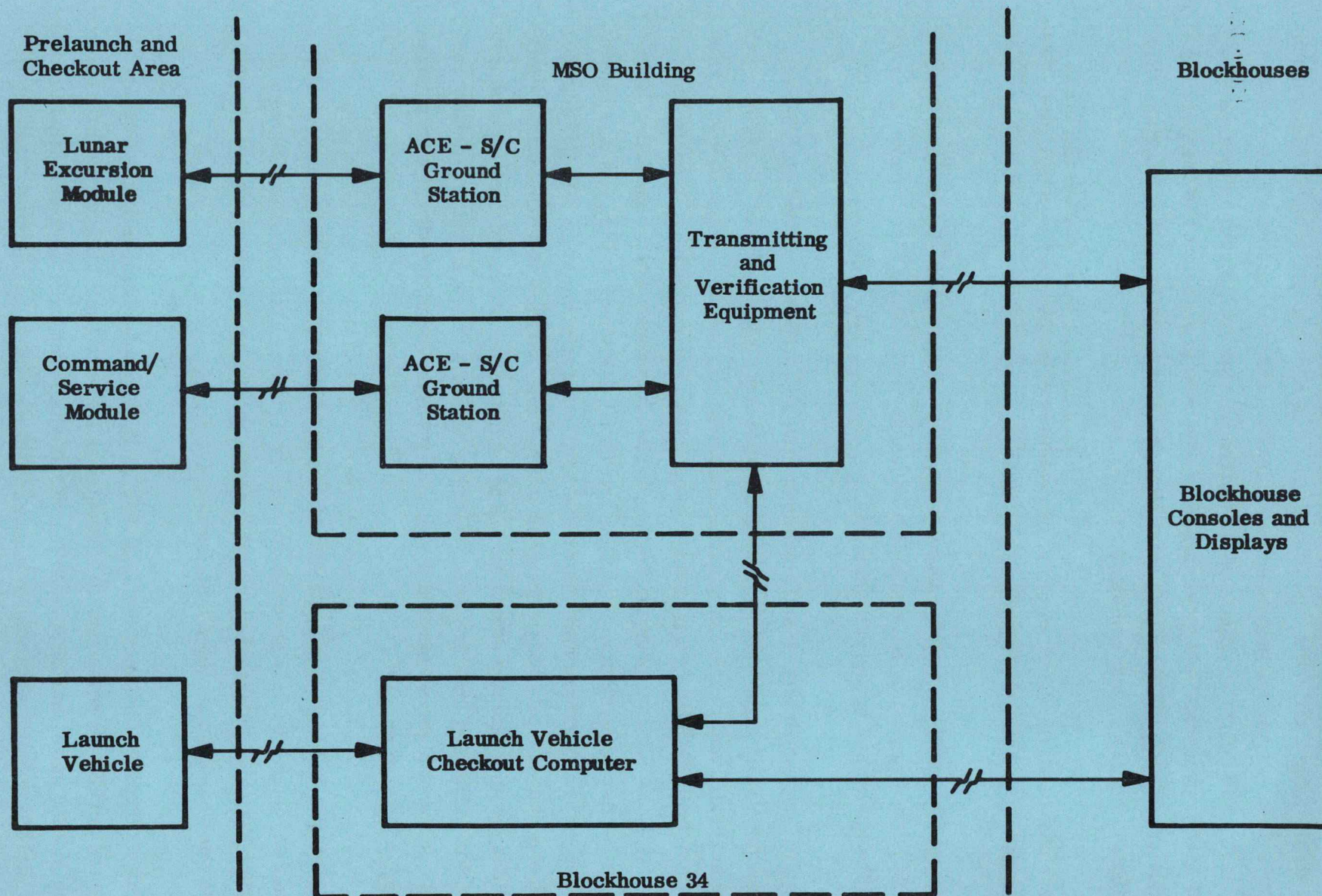


Figure 8. MILA/ACE-S/C Interface

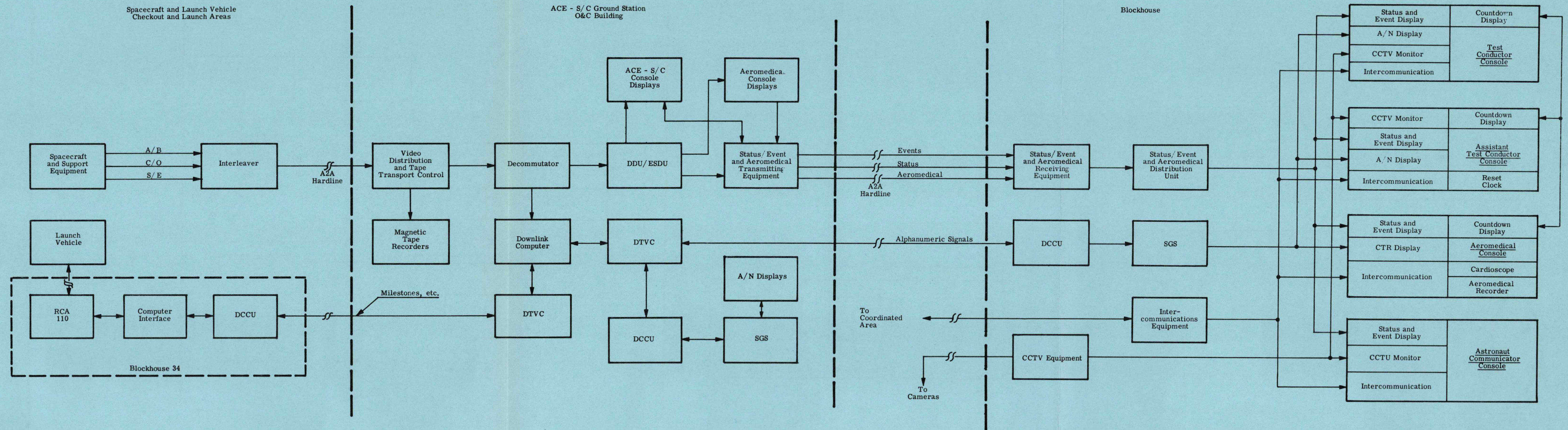


Figure 9. MILA Peripheral Interconnection

The ACE-S/C MILA peripheral equipment in Blockhouse 37 will be functionally identical to that in Blockhouse 34. The LCC 39 system differs from Blockhouse 34 and 37 by the addition of one low-silhouette console to the Test Conductor's Console, containing one self-contained clock and one countdown time control.

Additional equipment is installed in the MILA O&C Building to provide data transmission facilities for the MILA peripheral equipment. This equipment will serve Blockhouses 34 and 37 and LCC 39. This equipment will also transmit status and event signals from the ACE-S/C control rooms.

Within the ACE-S/C ground stations, parallel outputs provide the necessary signals that are transmitted to the blockhouses. These signals are displayed in the blockhouse simultaneously with the data being displayed in the ACE-S/C control room. The ACE-S/C ground station computer rooms will have additional transmission and verification equipment to facilitate a bidirectional flow of milestone and event data between the spacecraft checkout computer and the launch vehicle checkout computer.

TEST CONDUCTOR'S CONSOLE

The test conductor will utilize a console that provides a means of monitoring the status of all the spacecraft systems (CM/SM and LEM). An additional monitoring of milestone events, closed-circuit television presentations, countdown time, and alphanumeric summary test data enables the test conductor to be cognizant of all spacecraft checkout functions, thereby providing a highly functional spacecraft/launch vehicle integration task.

In addition to a monitoring function, the test conductor has the capability of controlling the arming and safe control of the CSM and LEM pyrotechnics.

ASSISTANT TEST CONDUCTOR'S CONSOLE

The assistant test conductor has the capability of monitoring closed-circuit television, intercommunications, countdown time, and alphanumeric test data. Utilizing the aforementioned displays, the assistant test conductor has the functional responsibility of controlling closed-circuit television presentation, countdown time, and alphanumeric test data, thus adding in the coordination of the overall integration.

AEROMEDICAL REPRESENTATIVE CONSOLE

The aeromedical representative utilizes the displays provided by the aeromedical console to monitor alphanumeric summary test data, system status, milestone events, and astronaut aeromedical functions. The aeromedical functions are pneumograph (respiration) and electrocardiogram (heart rate). With the astronaut aeromedical functions and other system test data, the aeromedical representative can coordinate the systems' Go/No Go status with that of the astronauts.

ASTROCOMMUNICATOR CONSOLE

The astrocommunicator utilizes the display devices on the astrocommunicator console for monitoring spacecraft communications and mission milestones.

DIGITAL COMMUNICATION AND CONTROL UNIT (DCCU)

The DCCU communicates via the A2A hardline with a MILA ACE-S/C ground station downlink computer and feeds alphanumeric data to the SGS. The DCCU allows the computer (Downlink 160G) to perform input/output operations at a remote location under local computer control. It also performs error verification of data transmissions.

SYMBOL GENERATOR AND STORAGE UNIT

The SGS receives digital words from the ACE-S/C downlink computer via a DCCU. As outputs, the SGS provides alphanumeric data to the CRT display monitors. Each CRT monitor is capable of controlling data callup from the SGS. The SGS utilized in the blockhouse control room is basically the same as that incorporated in the ACE-S/C ground station; however, it is limited to eight display units.

SIGNAL TRANSMISSION EQUIPMENT

This equipment, located in the O&C Building, facilitates the transmission of aeromedical, status, and event data to the remote consoles located in the blockhouse. The transmitting equipment utilizes both the frequency modulation and frequency-shift techniques in the transmission of data.

SIGNAL RECEIVING EQUIPMENT

This unit is the receiving terminal for status, event, and aeromedical analog data. As such, it consists primarily of tone receivers for demodulating frequency-shift transmissions and discriminators for demodulating frequency-modulated transmission.

These components provide the capability to process status and event signals and aeromedical analog signals transmitted from the O&C Building via telephone lines and the distribution of these signals to console displays.

STATUS/EVENT AND AEROMEDICAL DATA DISTRIBUTION UNIT

This unit is patched to all the blockhouse consoles to provide data for respective display devices.

GLOSSARY OF TERMS

GLOSSARY OF TERMS

FOREWORD

This Glossary of Terms includes those terms and abbreviations commonly used in the ACE-S/C program.

ABSOLUTE CODING: Coding written in numeric language acceptable to the machine without further modification.

ACCESS RANDOM: Access to storage under conditions in which the next position from which information is to be obtained is independent of the previous one.

ACCESS TIME: The time interval between the call for a unit of information from a storage device and the delivery of that information.

ACCUMULATOR: A unit containing a register that stores a quantity when a second quantity is delivered to the unit (frequently only a storage register).

✓ **ACE-S/C:** Acceptance Checkout Equipment - Spacecraft.

ADDEND: A number or quantity to be added to another.

ADDER: A device capable of forming the sum of two quantities.

ADDRESS: A label, name, or number identifying a register, a storage location, or a device from which information is received or to which it is transmitted.

ADDRESS, ABSOLUTE: The label(s) assigned by the machine designers to a specific storage location.

ADDRESS, BASE: A number that appears as an address in a computer instruction, but which is to be modified; for instance, by adding the contents of one or more index registers before it is used.

ADDRESS, DIRECT: An address in a computer instruction that indicates the location where the referenced operand is to be found or stored.

ADDRESS, EFFECTIVE: A modified address; the address actually used in a particular execution of a computer instruction.

ADDRESS, INDIRECT: An address in a computer instruction that indicates a location where the address of the referenced operand is to be found.

ADDRESS, RELATIVE: A number of the form of an address that specifies the position of a storage location with respect to some base address. The absolute address of the storage location is obtained by adding the relative address to the base address.

ADDRESS, SYMBOLIC: A label chosen to identify a particular work, function, or other information in a routine, independent of the location of the information within the routine.

ALPHANUMERIC: Characters that may be either letters of the alphabet, numerals, or special symbols. ✓

AMR: Atlantic Missile Range.

ANALOG-TO-DIGITAL CONVERSION: A process by which a sample of analog information is transformed into a digital code.

ANALOG-TO-DIGITAL CONVERTER: A device to convert analog information to digital by means of coded information.

ANALOG VOLTAGE: A voltage that varies in a continuous fashion in accordance with the magnitude of a measured variable.

AND: A logical operation.

AND GATE: A circuit with two or more inputs which produces one output if all input signals are coincident and are of the correct, predetermined polarity.

ARITHMETIC OPERATIONS: Fundamental operations of arithmetic; that is, addition, multiplication, division, and subtraction.

ARITHMETIC UNIT: That portion of the hardware of an automatic computer in which arithmetic and logical operations are performed.

ASD: Apollo Support Department.

ASPO: Apollo Spacecraft Project Office (NASA-MSC - Houston, Texas).

ASSEMBLY PROGRAM: A computer program that produces machine instructions from symbolic input.

AUXILIARY STORAGE: A device (other than the main memory unit) with the capability of holding large amounts of information.

BANK: A unit of core storage with provisions for storing 4096 or 8192 words. The use of more than one bank permits increasing the storage capacity of a computer without increasing the work length implicitly necessary to extend the range of storage addresses. In the 160A or the 160G, this address is effectively increased by set storage bank control instructions which determine which banks will be used during the program.

BINARY: A mathematical system in which the base "2" numerical structure is used. It is used in computer logic because it is much easier to work with than the decimal system which is based on ten numbers.

BINARY NUMBER: A group of digits, written in binary code (utilizing the base "2" numbering system), representing a specific number in the decimal system.

BINARY CODED DECIMAL (BCD): Decimal notation in which the individual decimal digits are represented by some binary code; for example, in the 8-4-2-1 coded decimal notation, the number twelve is represented as 0001 0010 for 1 and 2, respectively. Whereas, in pure binary notation, it is represented as 1100.

BIT: A unit of information that is carried by an identifiable character, and that can exist in either of two states - a "one" or a "zero." (An abbreviation of binary digit.)

BIT RATE: The frequency derived from the period of time required to transmit one bit.

BLANK: The character which results in memory when an input record is read - such as the hole in a card.

BLOCK: A group of words transported as a unit.

BOOTSTRAP: The coded instructions at the beginning of an input medium (tape or cards), together with instructions inserted by switches or buttons into the computer, which are used to read programs into memory.

BREAK-POINT: A point in a routine at which special action is taken, such as a stop or a transfer, either as the result of the insertion of a special instruction or the setting of a console switch. Usually used in debugging.

BUFFER: A device in which data is stored temporarily in the course of transmission from one point to another.

BUFFERED (INPUT/OUTPUT): A term indicating that the computer may carry on high-speed computation at the same time it is exchanging data with a peripheral device.

C-START: Computer communications START module. ✓

CALLING SEQUENCE: A set of characters identifying a subroutine and containing information concerning parameters to be inserted in the subroutine, information to be used in generating the subroutine, or information related to the operands; a call-word when exactly one word is filled.

CARRIER: A wave suitable for being modulated to transmit intelligence.

CCTV: Closed-circuit television.

CDC: Control Data Corporation (computer manufacturer).

CHANNEL: A transmission path; for instance, one connecting the computer to external equipment.

CHARACTER: One of a set of symbols, usually restricted to a member of a specific alphabet or appropriate to a particular computer. The symbols may include the letters A through Z, digits 0 through 9, punctuation marks, operation symbols, or any other symbols which a computer can read, store, or write; more precisely, the coded computer representation of a symbol drawn from its alphabet (one might represent the symbol "A" as the character 100001 in a specific computer alphabet).

CHECK SUM: A check in which groups of digits are summed, usually without regard to overflow. That sum is then checked against a previously computed sum to verify accuracy; also, the previously computed sum.

CLEAR: To reset a register by placing every stage in the "0" state.

CLOCK, MASTER: Central source of standard signals required for computer operations.

CLOCK PULSE: A pulse used for timing purposes. In PCM systems, a timing pulse that occurs at the bit repetition rate.

CLOSED-LOOP TELEMETRY: A telemetry system used as the indicating portion of a remote-control system. A system to check out a vehicle without radiation of RF energy.

✓ **CM or C/M:** Command Module.

CODE: A system of symbols and their use in representing rules for handling the flow or processing of information.

COMMAND: A signal that performs a unit operation, such as transmitting contents.

COMMUTATION: Sequential sampling, on a repetitive time sharing basis, of multiple data sources for transmitting and/or recording on a single channel.

COMMUTATION FRAME PERIOD: Time required for sequential sampling of all input signals. This period would correspond to one revolution of a single multi-contact rotary switch.

COMMUTATION RATE: Number of commutation inputs sampled per second.

COMMUTATOR: A device used to accomplish time division, multiplying by repetitive sequential switching.

COMPILER: A computer program that translates instructions written in a technical or problem-oriented language into machine language. Usually more than one machine instruction results from each symbolic instruction.

COMPLEMENT: A quantity that is derived from a given quantity and which represents the negative of the given quantity.

CONDITIONAL JUMP: A "jump" instruction which occurs only if a certain condition is present in the computer at the time the instruction is executed.

CONTENT: The quantity or word held in a register or storage location.

CONVERSION: Changing the form of representation of information.

CONVERTER: A unit that changes the language of information from one form to another.

CORE, MAGNETIC: A magnetic material capable of assuming and remaining at one of two or more conditions at magnetization, thus providing storage.

CORE STORAGE: High-speed storage in which information is represented by the magnetization of ferromagnetic cores.

COUNTER: A device, register, or storage location for storing integers, permitting these integers to be increased or decreased by unity or by an arbitrary integer, and capable of being reset to zero or to an arbitrary integer.

CSR: Check Status Register.

CUE: Communications Unit Executor.

CYCLE: A set of operations repeated as a unit.

D/A or DAC: Digital-to-Analog converter.

DADE: Data Acquisition and Decommuation Equipment. ✓

DATA REDUCTION: The process of transforming masses of raw test or any experimentally obtained data, usually gathered by instrumentation, into useful, orderly, and simplified intelligence.

DCCU: Digital Communications and Control Unit.

DDI: Data Display, Inc.

DDS: Data Display Subsystem.

DDU: Decommulator Distribution Unit.

DEBUGGING: The process of determining the correctness of a computer routine and locating errors in a program.

DENSITY, PACKING: The number of units of useful information contained within a given linear dimension, usually expressed in units per inch; for example, the number of bits stored on tape per linear inch on a single track by a single head.

DECODING: Operation by which a unit or equipment determines the meaning of the operation code of an instruction.

DECOMMUTATION: Equipment for separation, demodulation, or demultiplexing commutated signals.

DEVIATION: In frequency modulation, the peak difference between the instantaneous frequency of the modulated wave and the carrier center frequency.

DIGIT, BINARY: A whole number in the binary scale of notations, either a "one" or a "zero."

DIGITAL: Expressing value in terms of numbers. Measurable in discrete, discontinuous steps.

DIGITAL MAGNETIC TAPE RECORDING: The method of recording binary coded information using two discrete flux levels.

DIGITAL OUTPUT: A transducer output that represents the magnitude of the measurement and in the form of a series of discrete quantities coded in a system of notation.

DIS: Data Interleaving System.

DISCRIMINATOR, FM: A device that converts variations in frequency to proportional variations in voltage or current.

DOWNLINK: That part of the ACE-S/C system that receives, processes, and displays the return data from the spacecraft.

DTCS: Digital Test Command System

DTMS: Digital Test Measurement System.

DTVC: Data Transmission and Verification Converter.

EBM: Execute Buffer Memory.

ECS: Environmental Control System.

EDITOR: A routine to insert, delete, replace, or rearrange data.

EPS: Electrical Power System.

ESDU: Event Storage and Distribution Unit.

ELS: Earth Landing System.

EXECUTION (XEQ): Performance of an instruction in which the steps are carried out by the code of the instruction.

EXTERNAL FUNCTION CODE: A 12-bit code used to select and specify that an external device, for example, a printer or tape, is to perform some specific function.

FIXED POINT: System of arithmetic where the quantities are expressed by a predetermined number of digits with the decimal point located at some predetermined position.

FLIP-FLOP (FF): A bistable device capable of storing a bit of information or of controlling gates.

FM: Frequency Modulation.

FM DISCRIMINATOR: A device that converts frequency variations to proportional variations in the amplitude of an electrical signal.

FM/FM: Frequency modulation of a carrier by a subcarrier which is frequency modulated by information.

FORMAT: The predetermined arrangement of characters.

(EXTERNAL) FUNCTION CODE (EF): An external function code is a digital word used in addressing and selecting operating modes of equipment external to the computer. This code is generated by the computer.

FUNCTION READY: A signal transmitted by the computer, or such devices operating in a computer capacity, to external equipments to indicate that a function code is available.

GAEC: Grumman Aircraft Engineering Corporation.

G & N: Guidance and Navigation.

GASS: The generalized assembly system for the Control Data 160G Computer system.

GATE: A circuit with the ability to produce an output dependent upon a specified type and coincidence of inputs.

GFE: Government Furnished Equipment.

GSE: Ground Support Equipment.

INDEX REGISTER: A register that contains a quantity which may be used to automatically modify addresses (and for other purposes) under direction of the control section of the computer.

INDIRECT ADDRESSING: A second level of addressing - the address part of an instruction is the location in memory where the address of the operand may be formed or is stored.

INITIALIZE: To set all units, etc., to the desired initial values.

INFORMATION READY: A signal transmitted by the computer to an external piece of equipment indicating data is available.

INPUT READY: A signal transmitted to the computer by external equipment indicating that data is available to the computer.

INPUT REQUEST: A signal transmitted to external equipment by the computer requesting data.

INSTRUCTION: A set of characters which define an operation, together with one or more addresses.

I/O: Input/Output - in reference to the computer.

IRIG: Inter-Range Instrumentation System.

JUMP: An instruction specifying the location of the next instruction and directing the computer to that instruction.

K-START: Keyboard START Module.

LBM: Load Buffer Memory.

LCC: Launch Control Center (MILA).

LEM: Lunar Excursion Module.

LES: Launch Escape System.

LIBRARY: An ordered set or collection of standard and proven programs and sub-routines used for data processing applications and the solution of problems.

LINE-PRINTING: Printing an entire line of characters across a page as the page feeds in one direction past a type bar.

LOAD: To bring information into memory from an external storage medium and to place a quantity from storage into the A register.

LOC: Launch Operation Center (Cape Kennedy).

LOCATION: A storage position in internal or shared memory.

LOCKOUT: Any function (usually of machine logic) that inhibits an action that would normally occur if the lockout were not imposed.

LOGIC CIRCUIT: A complex of "go/no-go" type circuitry arranged in such a pattern or matrix as to perform the various arithmetic functions on demand.

LOGICAL OPERATIONS: The computer operations that are logical in nature, such as logical AND, OR, extract, and decisions. This is in contrast to the arithmetic operations, such as add, subtract, multiply, and divide.

LOOP: A given sequence of instructions operated upon repeatedly (normally, until a specified condition occurs).

LV or L/V: Launch Vehicle.

MACRO: A symbolic instruction representing a frequently used sequence of machine language instructions.

MAINTENANCE PROGRAM: A diagnostic program to determine the operational readiness of any piece of computer or peripheral equipment and to isolate any malfunctions that occur.

MASK: A prearranged pattern or configuration of bits in a computer word generally used for logical or bit manipulations.

MASS: A monitor and assembly system for the Control Data Corporation 160G computer system.

MEMORY: Internal storage.

MESSAGE: A group of words transported to a unit specifying an operation.

MICROSECOND: A millionth part of a second.

MILA: Merritt Island Launch Area (Cape Kennedy).

MILLISECOND: A thousandth part of a second.

MIT: Massachusetts Institute of Technology.

MITRE: The research division of the Massachusetts Institute of Technology.

MNEMONIC: The art of programming to improve the efficiency of the computer memory.

MNEMONIC OPERATION CODES: Operation codes in symbolic notation which are easier to remember than the actual operation codes of the machine.

MODULATION: The process of impressing information on a carrier for transmission.

MONITOR: A program that exercises supervisory control over some other programs or collections of programs. Also called executive routine or master routine.

MSC: Manned Spacecraft Center, Houston, Texas.

MULTIPLEXING: The simultaneous transmission of two or more signals within a single channel. The three basic methods of multiplexing involve the separation of signals by time division, frequency division, and phase division.

NASA: National Aeronautics and Space Administration.

OCTAL: Pertaining to the number base of eight.

OFF-LINE: Peripheral equipment not under direct computer control.

ONE: The representation of a binary digit; that is, a condition exists.

ONE'S COMPLEMENT: With reference to a binary number, that number which results from subtracting each bit of the given number from the bit 1. A negative number is expressed by the one's complement of the corresponding positive number.

ON-LINE: Peripheral equipment under direct computer control.

OPERAND: Any one of the quantities entering or arising in an operation. An argument, a result, a parameter, or an indication of the location of the next instruction.

OSAS-A: A general assembly system for the Control Data Corporation 160A computer system.

OVERFLOW: The generation of a quantity beyond the capacity of a register.

PARALLEL TRANSFER: A system of data transfer in which elements of information are transferred simultaneously over a parallel set of lines.

PARAMETER: Measurand, a physical or electrical quantity which is measured.

PARITY BIT: A bit added to a binary code to facilitate a parity check.

PARITY CHECK: A self-checking code employing binary digits in which the total number of "ones" or "zeros" in each permissible code expression is always even or always odd. A check may be made for either even or odd parity.

PARTIAL ADD: An addition without carries.

PCM: Pulse Code Modulation (PCM) is the pulse modulation of a carrier by coded information. In PCM telemetry, information transmission is by means of a code representing a finite number of values of the information at the time sampling.

PERIPHERAL: Off-line devices concerned with the transfer of data. Usually under control of the computer.

PHASE-LOCK LOOP: An electrical servo system used either as a tracking filter or as a frequency discriminator.

PRIME CHANNELS: The channels which are sequentially sampled by the basic commutator of the system.

PRIME FRAME: A group of words resulting from a complete sampling of the prime channel.

PROGRAM: A sequence of instructions that causes a data processing system to process a specific application; a plan for the solution of a problem.

PSEUDO INSTRUCTION: A symbolic representation of information to a compiler or interpreter; a group of characters having the same general form as a computer instruction, but never executed by the computer as an actual instruction.

PYRAMID, BORROW: A network of inverters that senses borrow conditions and produces borrow signals.

R-START: Relay selection START modules.

RAW-DATA: Data that has not been processed; it may or may not be in machine-sensible form.

READ: To copy, usually from one form of storage to another, particularly from external or secondary storage to internal storage; to sense the presence of information on a recording medium.

REAL-TIME PROCESS: A process where the computer exists on line in an environment that cannot be made subservient to computer control. Usually a continuous physical process is involved.

RECORD: A group of related facts or a field of information that is treated as a unit.

RECORD HEAD: An electromagnetic transducer used during the recording process for inducing magnetic patterns into the magnetic tape.

REGISTER: A device for storing one or more computer words.

RELOCATE: To move a routine from one portion of internal storage to another and, in so doing, to automatically adjust the address references so that the routine can be executed in its new location.

REPRODUCE HEAD: An electronic transducer that converts the remanent flux patterns in a magnetic tape into electrical signals.

ROUTINE: Essentially synonymous with "program," although generally restricted to describing single-purpose programs.

ROUTINE, EXECUTIVE: A set of coded instructions designed to process and control other sets of coded instructions.

SCS: Stabilization and Control System.

✓ **SEAL:** Select Extend Allocated Lockout.

SEGMENTATION: Division of a routine into parts, one segment being the "main program" and other segments being subprograms. The segments are linked together by CALL-type statements and may be compiled and debugged separately.

SENSE: To examine, particularly relative to a criterion; to determine the present arrangement of some element of hardware, especially a manually set switch.

SERIAL TRANSFER: A system of data transfer in which elements of information are transferred in succession over a single line.

SERIAL RECORDING, PCM: The technique of recording a train of bits on a single magnetic tape track.

SGS: Symbol Generator and Storage Unit.

SHIFT: To move the bits of a quantity right or left.

SIGN BIT: The bit in the highest-order stage of the register (in registers where a quantity is treated as signed by use of one's complement notation). If the bit is "1," the quantity is negative; if the bit is "0," the quantity is positive.

SIGN EXTENTION: The duplication of the sign bit in the highest-order stages of a register.

SKEW: Tape motion characterized by an angular velocity between the gap centerline and a line perpendicular to the tape centerline.

✓ **SM or S/M:** Service Module.

SOURCE PROGRAM: A program coded in other than machine language that must be translated into machine language to be executed by a computer.

SPACECRAFT TEST PROGRAM: A computer program package containing the control programs, TEX's, etc., required to describe a single spacecraft test.

✓ **START:** Selection to Activate Random Testing.

STATUS: The condition of an external device, as reflected in the response given a status interrogation by the computer.

STORAGE: Memory.

SUBCARRIER: A carrier which is applied as a modulating wave to modulate another carrier or an intermediate subcarrier.

SUBROUTINE: The set of instructions necessary to direct the computer to carry out a well-defined mathematical or logical operation.

SUBROUTINE, CLOSED: A subroutine not stored in the main path of the routine. Such a subroutine is entered by a jump operation with provision made to return control to the main routine at the end of the operation.

SUBROUTINE, OPEN: Has been, in general, replaced by the term "Macro Instruction." It is a subroutine inserted directly into the main path of the routine, not entered by a jump. Such a subroutine must be recopied at each point at which it is needed.

SUPERVISORY EXECUTIVE PROGRAM (SEP): The monitor program that exercises supervisory control over the use of spacecraft test programs during real-time testing of spacecraft.

SUBCOMMUTATION: Commutation of additional channels with output applied to individual channels of the primary commutator.

SUBCOMMUTATION FRAME: In PCM systems, a recurring integral number of subcommutator words which includes a single subcommutation frame synchronization word.

SUBPROGRAM: A segment of a larger program capable of being compiled and debugged by itself.

SUPERCOMMUTATION: Commutation at higher rate by connection of single data input source to equally spaced contacts of the commutator.

SYMBOLIC CODING: Any coding system in which symbols other than machine addresses and machine language are used.

TABLE LOOKUP: A coding technique or an instruction that locates the word in a table corresponding to a specified word, and usually obtains some other word that corresponds to the word located.

TAPE, MAGNETIC: A tape or ribbon of some material impregnated or coated with magnetic material on which information can be placed in the form of magnetically polarized spots.

TAPE SPEED ERRORS: Any variation of the tape speed from its nominal speed over the record or reproduce head regardless of cause.

TELEMETRY (T/M): The science of measuring a quantity of quantities, transmitting the results to a distant station, and there interpreting, indicating, and/or recording the quantities measured.

TEST EXECUTIVE (TEX): A computer program or subprogram written specifically to meet spacecraft system test sequence requirements for real-time operation.

TEST FILE: One or more spacecraft test programs on magnetic tape, limited only by the length of the tape.

TIMING SIGNAL: Any signal recorded simultaneously with data to provide a time index.

TRACKS: A portion of a magnetic tape the width and position of which on the magnetic tape is specified. A track extends throughout the entire length of a reel of tape and always exists regardless of its state of magnetization.

TWO'S COMPLEMENT: The two's complement may be formed by complementing each bit of the given number and then adding one to the result, performing the required carries.

UPLINK CONTROL PROGRAM: A computer program that generates commands to the DTCS to provide stimuli to the spacecraft according to information received from the CUE.

UTILITY PROGRAM: A program normally used to assist in the operation of a data processing system (memory dump, card-to-tape, etc.).

VDTTC: Video Distribution and Tape Transport Control Unit.

VIDEO RECORDING: The method of recording information having a bandwidth in excess of 500 kilocycles on a single track.

WORD: An ordered set of digits processed as a unit.

WOW and FLUTTER: Terms derived from disc and motion picture sound recording often used in reference to speed change errors in magnetic recording.

WRITE: To transfer information to an output recorder; to copy, usually from internal storage to external storage; to record information in a register, location, or other storage device.

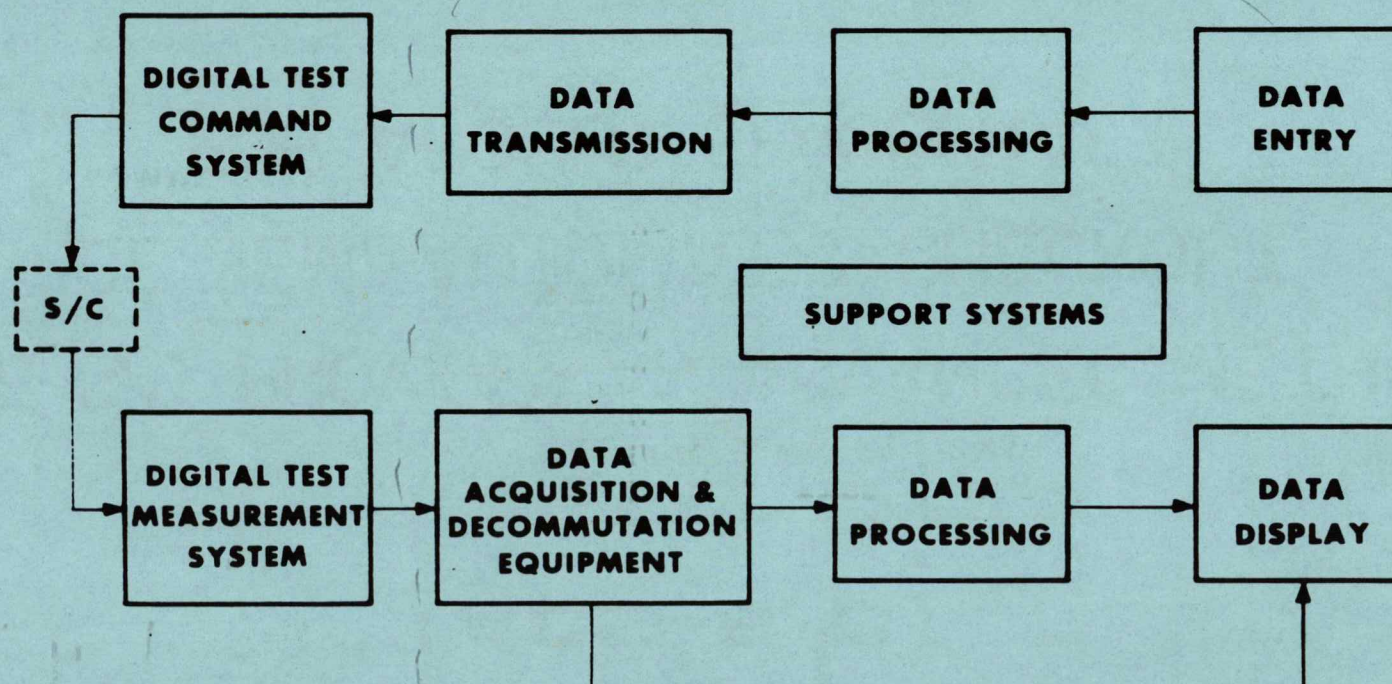
SUPPLEMENTS

**ACCEPTANCE CHECKOUT
EQUIPMENT-SPACECRAFT
(ACE-S/C)**

**ACE-S/C PROVIDES AN ADVANCED METHOD
OF SEMI-AUTOMATIC CHECKOUT
FOR APOLLO SPACECRAFT**

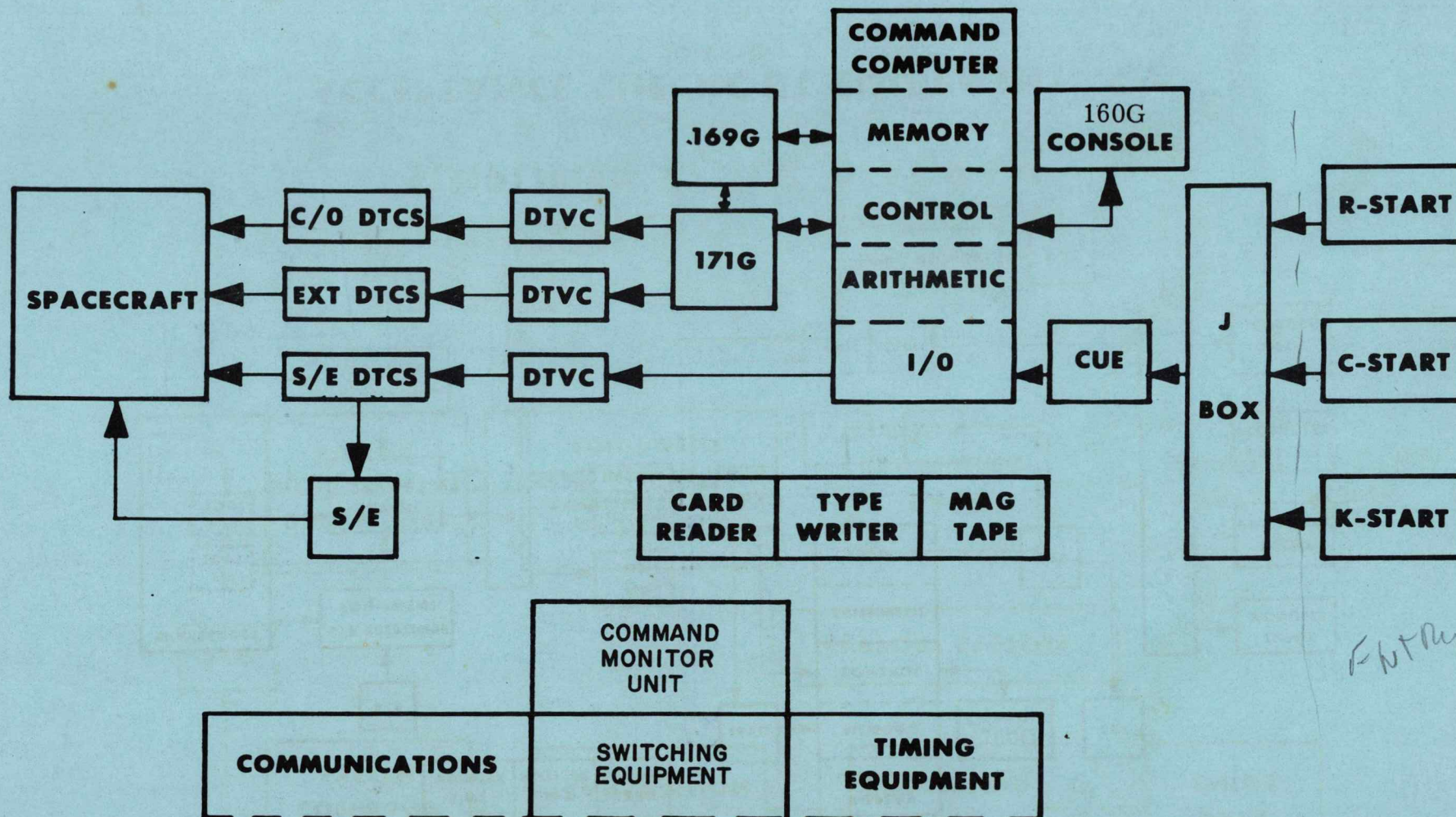
FOR TRAINING PURPOSES ONLY

FOR TRAINING PURPOSES ONLY



ACCEPTANCE CHECKOUT EQUIPMENT - S/C
SIMPLIFIED BLOCK DIAGRAM

FOR TRAINING PURPOSES ONLY

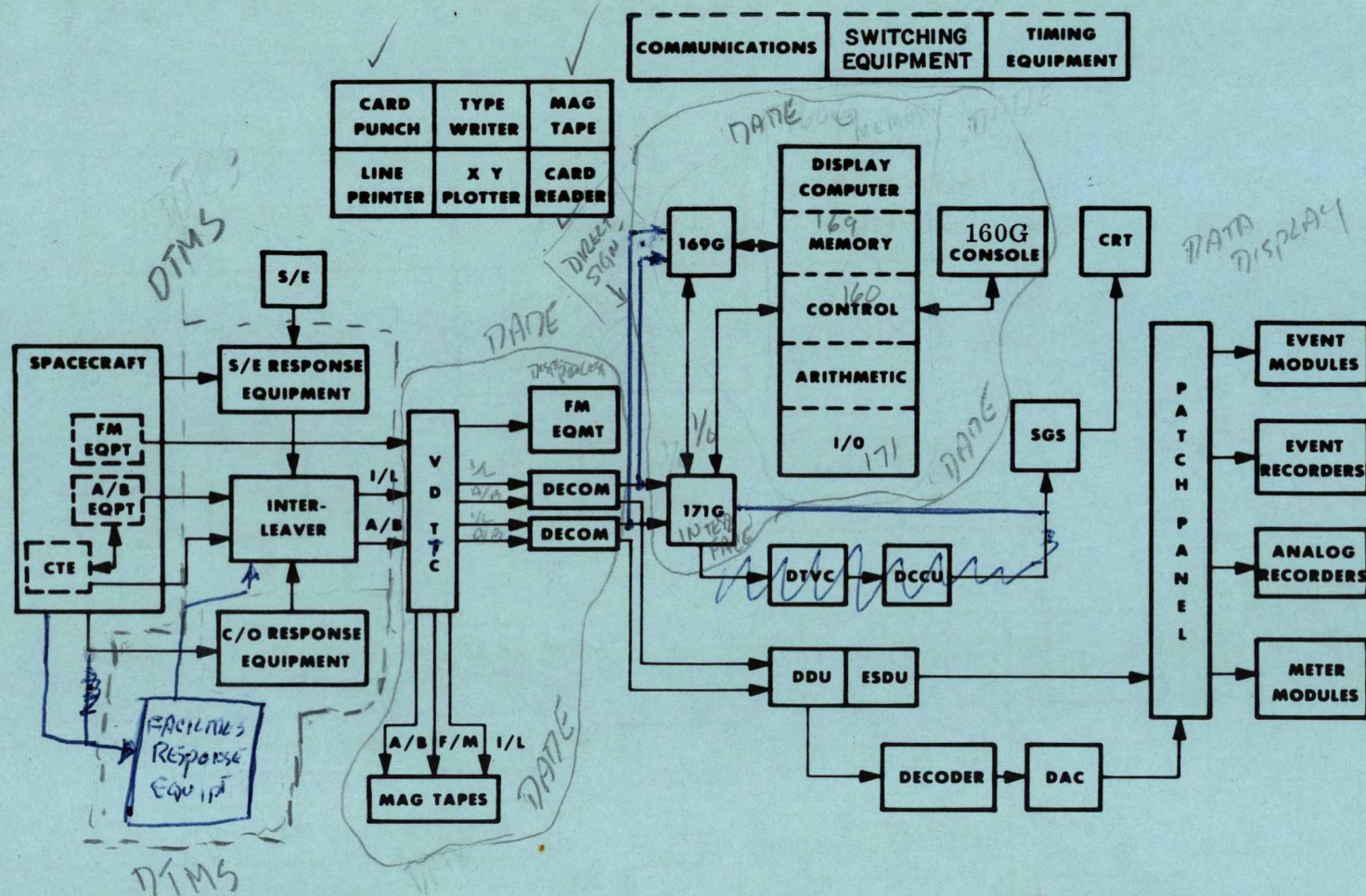


FOR TRAINING PURPOSES ONLY

ACCEPTANCE CHECKOUT EQUIPMENT -S/C

(UPLINK)

FOR TRAINING PURPOSES ONLY



ACCEPTANCE CHECKOUT EQUIPMENT -S/C
(DOWNLINK)

FOR TRAINING PURPOSES ONLY

DTCS ADDRESS CODES FOR CMU

GROUP ADDRESS

 $\underline{2^{11}}$ $\underline{2^{10}}$ $\underline{2^9}$ (WORD NO. 2)

0	0	1	GROUP NO. 1
0	1	0	GROUP NO. 2
1	0	0	GROUP NO. 3
0	0	0	GROUP NO. 4
1	1	1	GROUP NO. 5 (G & N)

BASEPLATE ADDRESS

 $\underline{2^5}$ $\underline{2^4}$ $\underline{2^3}$ $\underline{2^2}$ (WORD NO. 1)

0	0	0	1	BASEPLATE NO. 1
0	0	1	0	BASEPLATE NO. 2
0	1	0	0	BASEPLATE NO. 3
1	0	0	0	BASEPLATE NO. 4
0	1	1	1	BASEPLATE NO. 5
1	0	1	1	BASEPLATE NO. 6
1	1	0	1	BASEPLATE NO. 7
1	1	1	0	BASEPLATE NO. 8

MODULE ADDRESS

 $\underline{2^8}$ $\underline{2^7}$ $\underline{2^6}$ (WORD NO. 2)

0	0	1	MODULE NO. 1
0	1	0	MODULE NO. 2
1	0	0	MODULE NO. 3
1	1	1	MODULE NO. 4

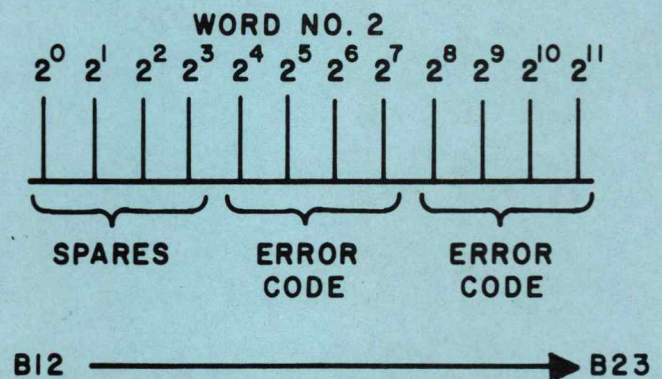
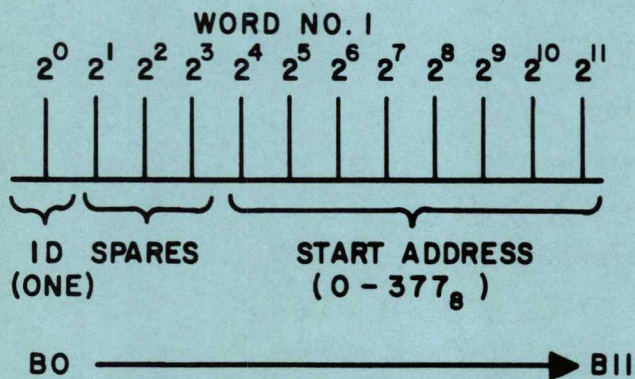
SUBGROUP ADDRESS

 $\underline{2^5}$ $\underline{2^4}$ $\underline{2^3}$ (WORD NO. 2)

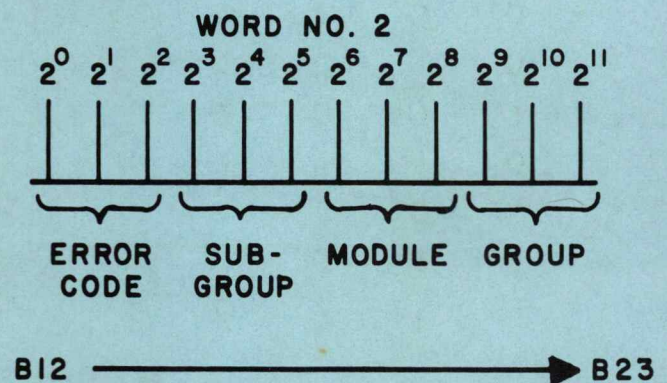
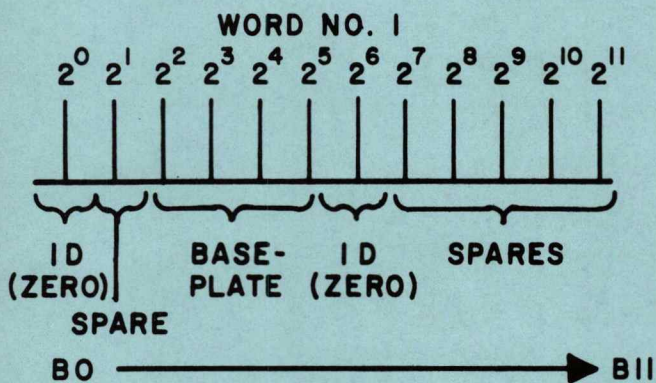
0	0	1	SUBGROUP A
0	1	0	SUBGROUP B
1	0	0	SUBGROUP C
0	0	0	SUBGROUP D

CMU DATA WORDS INPUTS

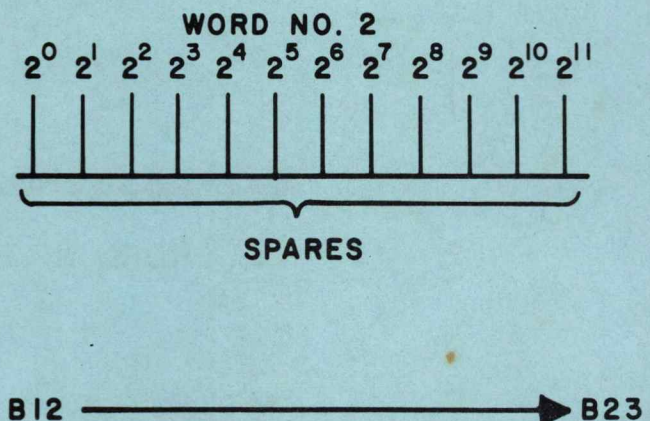
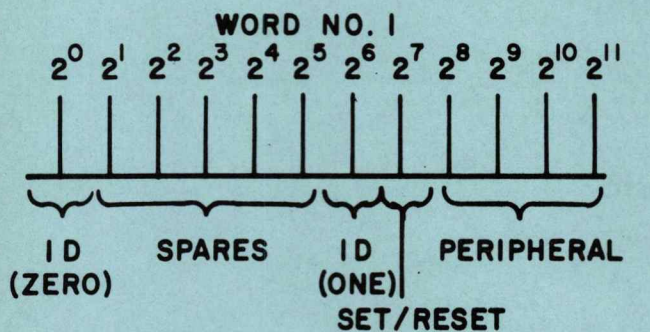
CUE/START STATUS WORDS



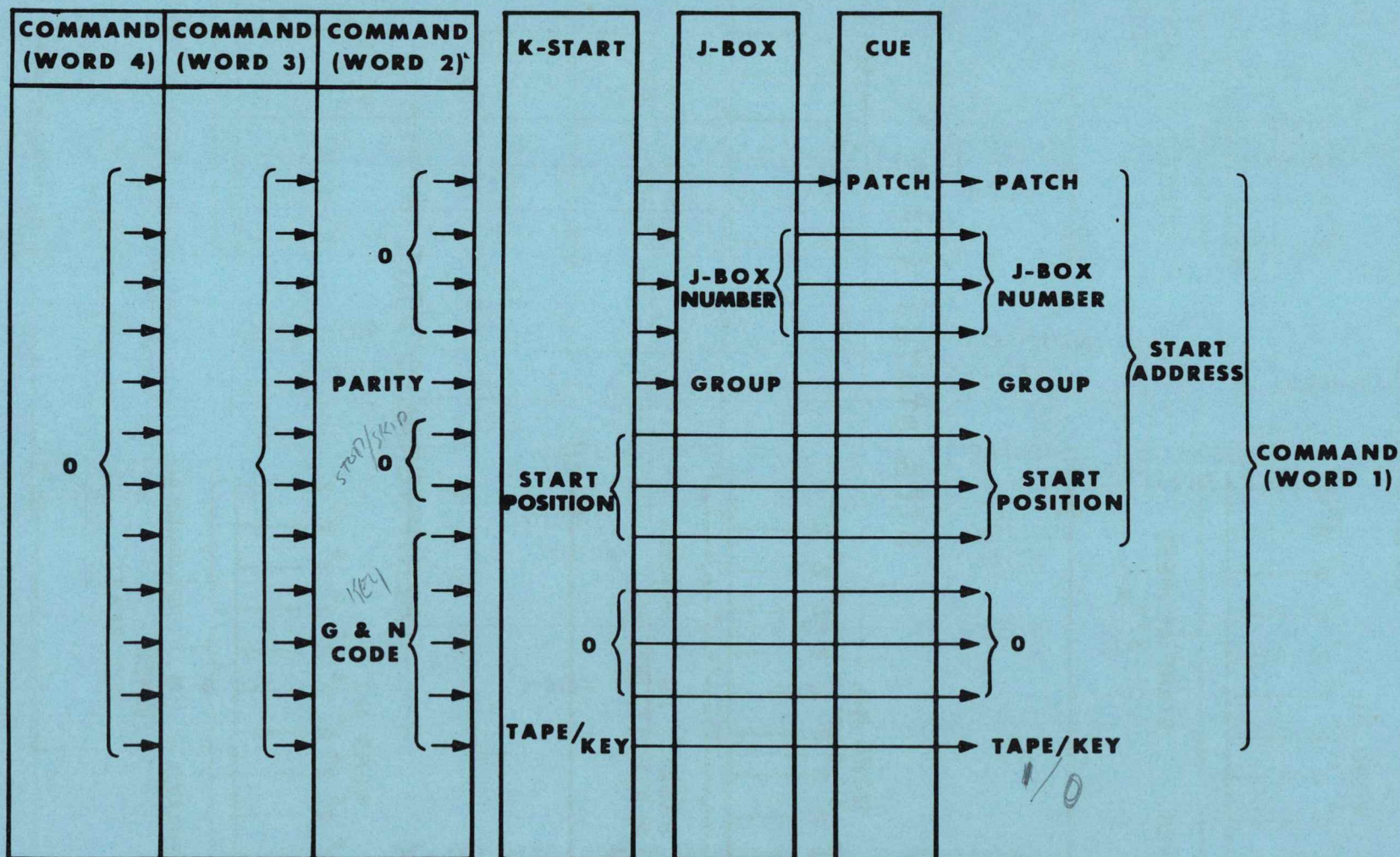
DTCS STATUS WORDS



PERIPHERAL STATUS WORDS



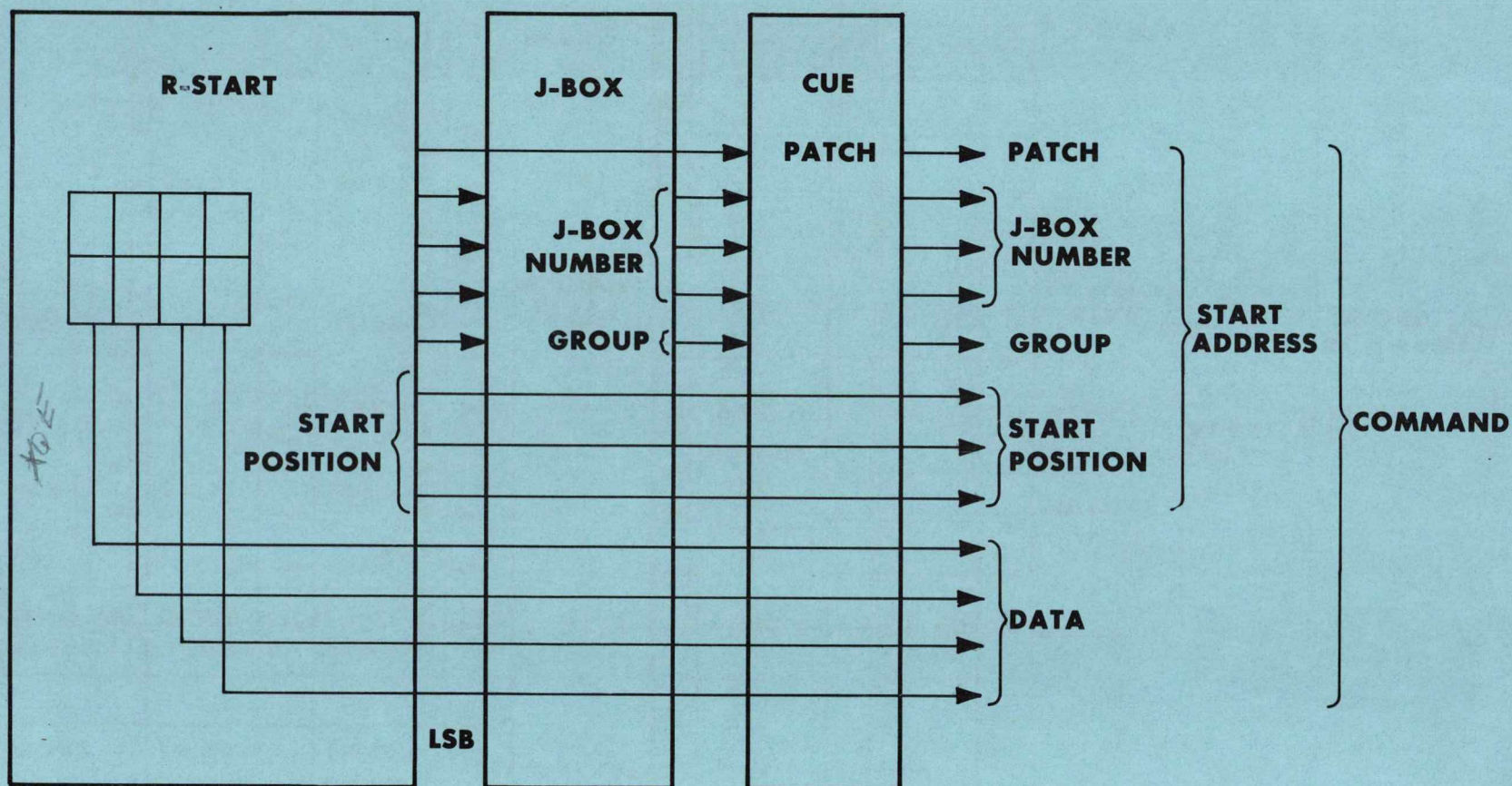
K-START COMMAND FORMAT



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FOR TRAINING PURPOSES ONLY

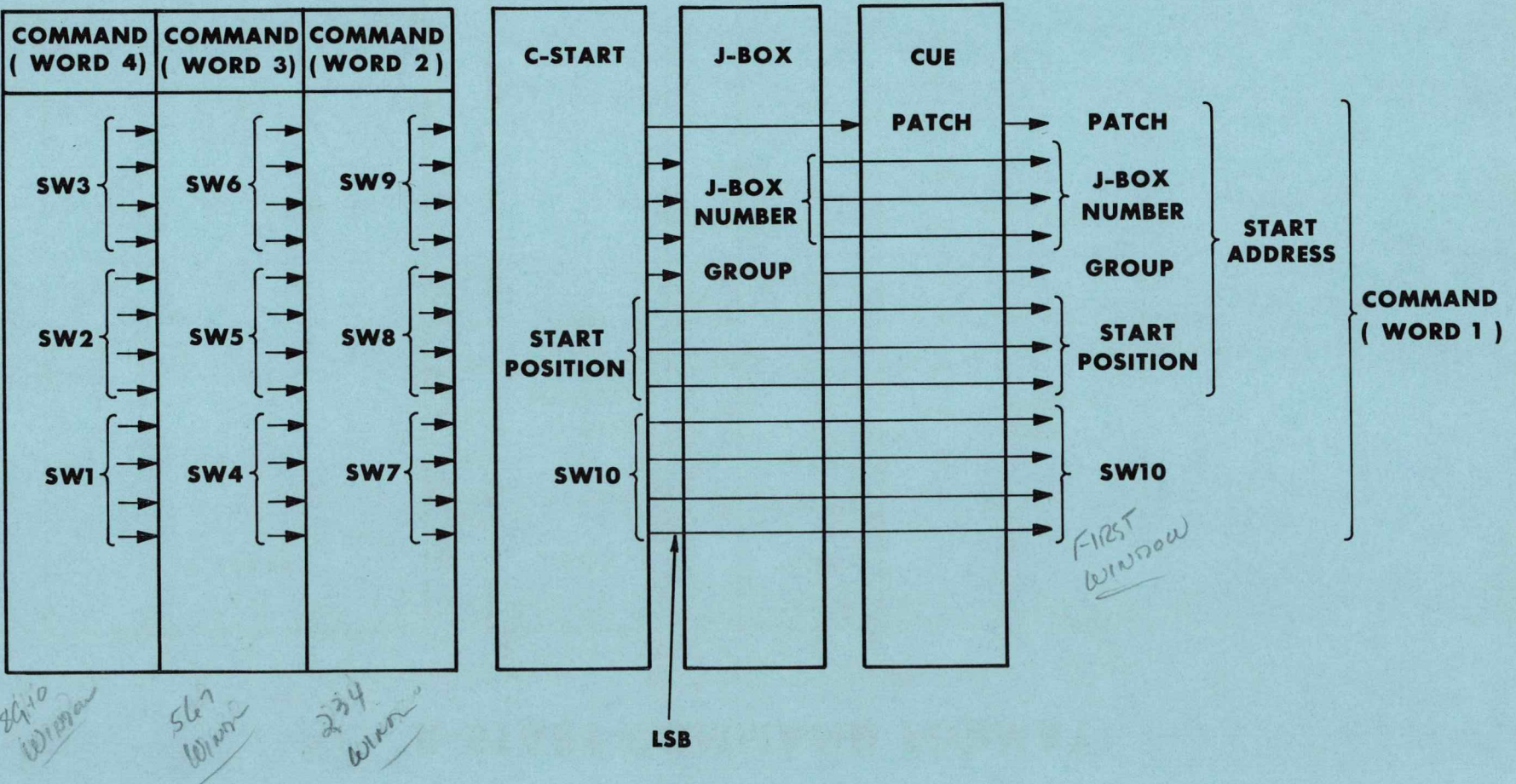
R-START COMMAND FORMAT



FOR TRAINING PURPOSES ONLY

FOR TRAINING PURPOSES ONLY

C-START COMMAND FORMAT



FOR TRAINING PURPOSES ONLY

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PROGRAMING REQUIREMENTS

**DOWNLINK DATA REDUCTION
& DISPLAY**

UPLINK COMMAND GENERATION

AUTOMATIC LIMIT ADJUSTMENT

ACE SELF-TEST

ACE DIAGNOSTICS

PROGRAM VERIFICATION

SUPERVISORY PROGRAM

LIBRARY MAINTENANCE

FOR TRAINING PURPOSES ONLY

FOR TRAINING PURPOSES ONLY

PROGRAM VERIFICATION

*ACCOMPLISHED WITHIN ACE, USING
VERIFICATION PROGRAMS*

FOR DOWNLINK PROGRAMS:-

UPLINK COMPUTER GENERATES SIMULATED INPUT DATA

OPERATION OF DOWNLINK PROGRAM ON KNOWN DATA
IS CHECKED

FOR UPLINK PROGRAMS:-

UPLINK & DOWNLINK COMPUTERS CONNECTED VIA
BACK-TO-BACK DTVC

DOWNLINK COMPUTER SIMULATES REMOTE END OF
COMMAND LINKS

UPLINK COMMANDS , GENERATED IN PRESCRIBED ORDER ,
CHECKED BY DOWNLINK COMPUTER

UPLINK CARD 1 FORMAT

FOR TRAINING PURPOSES ONLY

FOR TRAINING PURPOSES ONLY

SUPERVISORY PROGRAM

SUPI-002 - GASS SYMBOLIC ASSEMBLER

SUPI-003 - MASS SYST-MONITOR

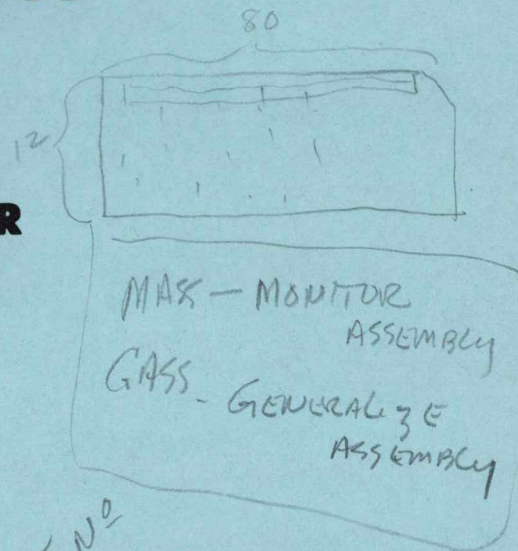
004 - SUPERVISOR EFFECTIVE
(OVERALL) PROGRAMMER

007 MASS / GASS CARD Assy Package
(COMBINE 002-003)

005 - UPLINK Control Program
(CARDS 1 & 2)

CDC INSTIGATED
C
D
C

- a. FIELD 1 - STIMULUS NUMBER
- b. FIELD 2 - CHANGE CODE
- c. FIELD 3 - DESCRIPTION
- d. FIELD 4 - CONSOLE
- e. FIELD 5 - START MODULE
- f. FIELD 6 - DTCS ADDRESS
- g. FIELD 7 - SUBPROGRAM
- h. FIELD 8 - TEST IDENTIFICATION
- i. FIELD 9 - RESERVED FOR GE
- j. FIELD 10 - MULTIPLE STIMULI LISTING
- k. FIELD 11 - CARD NUMBER



START NO.

CYRATIC LEVEL

FIELD = 1 OR MORE Column

GE

UPLINK CARD 2 FORMAT

- a. FIELD 12 - STIMULUS NUMBER
- b. FIELD 13 - CHANGE CODE
- c. FIELD 14 - C-START INSERT
- d. FIELD 15 - R-START INSERT
- e. FIELD 16 - REMARKS — OCT - ETC
- f. FIELD 17 - TEST IDENTIFICATION LTA-
- g. FIELD 18 - RESERVED FOR GE
- h. FIELD 19 - MULTIPLE STIMULI LISTING
- i. FIELD 20 - CARD NUMBER

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FOR TRAINING PURPOSES ONLY

DOWNLINK CARD 1 FORMAT

- a. FIELD 1 - MEASUREMENT ID
- b. FIELD 2 - MEASUREMENT ID LINK
- c. FIELD 3 - MULTI-DISPLAY
- d. FIELD 4 - MEASUREMENT DESCRIPTION
- e. FIELD 5 - FIRST PRIME FRAME ✓
- f. FIELD 6 - TIME SLOT ✓
- g. FIELD 7 - WORD FRAGMENT ✓
- h. FIELD 8 - RATE ✓
- i. FIELD 9 - PRIME FRAME INCREMENT ✓
- j. FIELD 10 - OFF STATE
- k. FIELD 11 - MODULE
- l. FIELD 12 - RECORDER
- m. FIELD 13 - CHANGE CODE
- n. FIELD 14 - CARD NUMBER

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FOR TRAINING PURPOSES ONLY

DOWNLINK CARD 2 FORMAT

- a. FIELD 15 - MEASUREMENT ID
- b. FIELD 16 - MEASUREMENT ID LINK
- c. FIELD 17 - MULTI-DISPLAY ✓
- d. FIELD 18 - SCOPE READOUT DISPLAY ✓
- e. FIELD 19 - ENGINEER UNITS ✓
- f. FIELD 20 - PAGE
- g. FIELD 21 - LINE
- h. FIELD 22 - DIGIT CONFIGURATION
- i. FIELD 23 - SCOPE FORMAT ID

DOWNLINK CARD 2 FORMAT

- j. FIELD 24 - FILING REQUIREMENTS**
- k. FIELD 25 - TEST ID**
- l. FIELD 26 - LIMITS**
- m. FIELD 27 - CATEGORY**
- n. FIELD 28 - OBSOLETE**
- o. FIELD 29 - SPECIAL**
- p. FIELD 30 - CHANGE CODE**
- q. FIELD 31 - CARD NUMBER**

FOR TRAINING PURPOSES ONLY

FOR TRAINING PURPOSES ONLY

DOWNLINK CARD 3 FORMAT

- a. FIELD 32 - MEASUREMENT ID
- b. FIELD 33 - MEASUREMENT ID LINK
- c. FIELD 34 - MULTI-DISPLAY
- d. FIELD 35 - LABELING INFORMATION ✓
- e. FIELD 36 - NOT USED
- f. FIELD 37 - METER SCALING ✓
- g. FIELD 38 - METER SCALE CODE ✓
- h. FIELD 39 - SECOND MODULE/RECORDER
- i. FIELD 40 - ADDITIONAL MODULES CODE ✓
- j. FIELD 41 - RESERVED FOR G.E.
- k. FIELD 42 - CHANGE CODE
- l. FIELD 43 - CARD NUMBER

DOWNLINK CARD 4 FORMAT

- a. FIELD 44 - MEASUREMENT ID
- b. FIELD 45 - MEASUREMENT ID LINK
- c. FIELD 46 - MULTI-DISPLAY
- d. FIELD 47 - MODULE/RECORDER ✓
- e. FIELD 48 - MODULE/RECORDER ✓
- f. FIELD 49 - REMARKS
- g. FIELD 50 - CHANGE CODE
- h. FIELD 51 - CARD NUMBER

FOR TRAINING PURPOSES ONLY

FOR TRAINING PURPOSES ONLY

DOWNLINK CARD 5 FORMAT

- a. FIELD 52 - MEASUREMENT 1D**
- b. FIELD 53 - MEASUREMENT 1D LINK**
- c. FIELD 54 - MULTI-DISPLAY**
- d. FIELD 55 - ADDITIONAL REMARKS**
- e. FIELD 56 - CHANGE CODE**
- f. FIELD 57 - CARD NUMBER**

LIMIT CHANGE CARD 1 FORMAT

- a. FIELD 1 - MEASUREMENT ID**
- b. FIELD 2 - MEASUREMENT ID LINK**
- c. FIELD 3 - MULTI-DISPLAY**
- d. FIELD 4 - NOT USED**
- e. FIELD 5 - LIMIT VALUE 1**
- f. FIELD 6 - LIMIT VALUE 2**
- g. FIELD 7 - NOT USED**
- h. FIELD 8 - DIGIT CONFIGURATION**
- i. FIELD 9 - REMARKS**
- j. FIELD 10 - VEHICLE ID**
- k. FIELD 11 - CHANGE CODE**

FOR TRAINING PURPOSES ONLY

FOR TRAINING PURPOSES ONLY

SEPARATOR CARD 2 FORMAT

- a. FIELD 12 - SEPARATOR I.D.**
- b. FIELD 13 - REMARKS**

FOR TRAINING PURPOSES ONLY

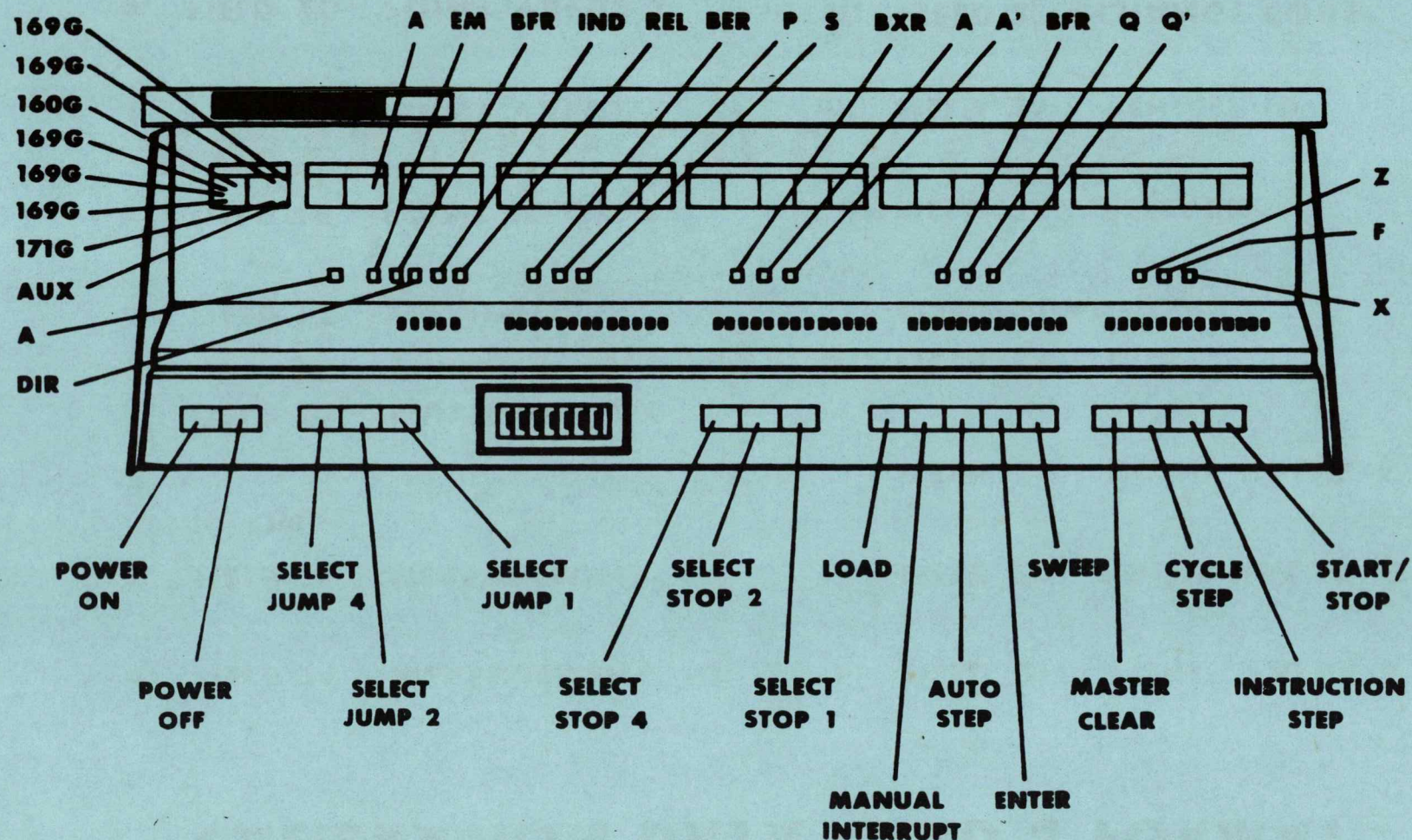
FOR TRAINING PURPOSES ONLY

CALIBRATION DATA CARD 3 FORMAT

- | | |
|--------------------------------------|--------------------------------------|
| a. FIELD 14 - MEASUREMENT ID | h. FIELD 21 - POINT VALUE 4 |
| b. FIELD 15 - MEASUREMENT
ID LINK | i. FIELD 22 - POINT VALUE 5 |
| c. FIELD 16 - MULTI-DISPLAY | j. FIELD 23 - POINT VALUE 6 |
| d. FIELD 17 - SEGMENTS | k. FIELD 24 - DIGIT
CONFIGURATION |
| e. FIELD 18 - POINT VALUE 1 | l. FIELD 25 - REMARKS |
| f. FIELD 19 - POINT VALUE 2 | m. FIELD 26 - VEHICLE ID |
| g. FIELD 20 - POINT VALUE 3 | n. FIELD 27 - CHANGE CODE |

FOR TRAINING PURPOSES ONLY

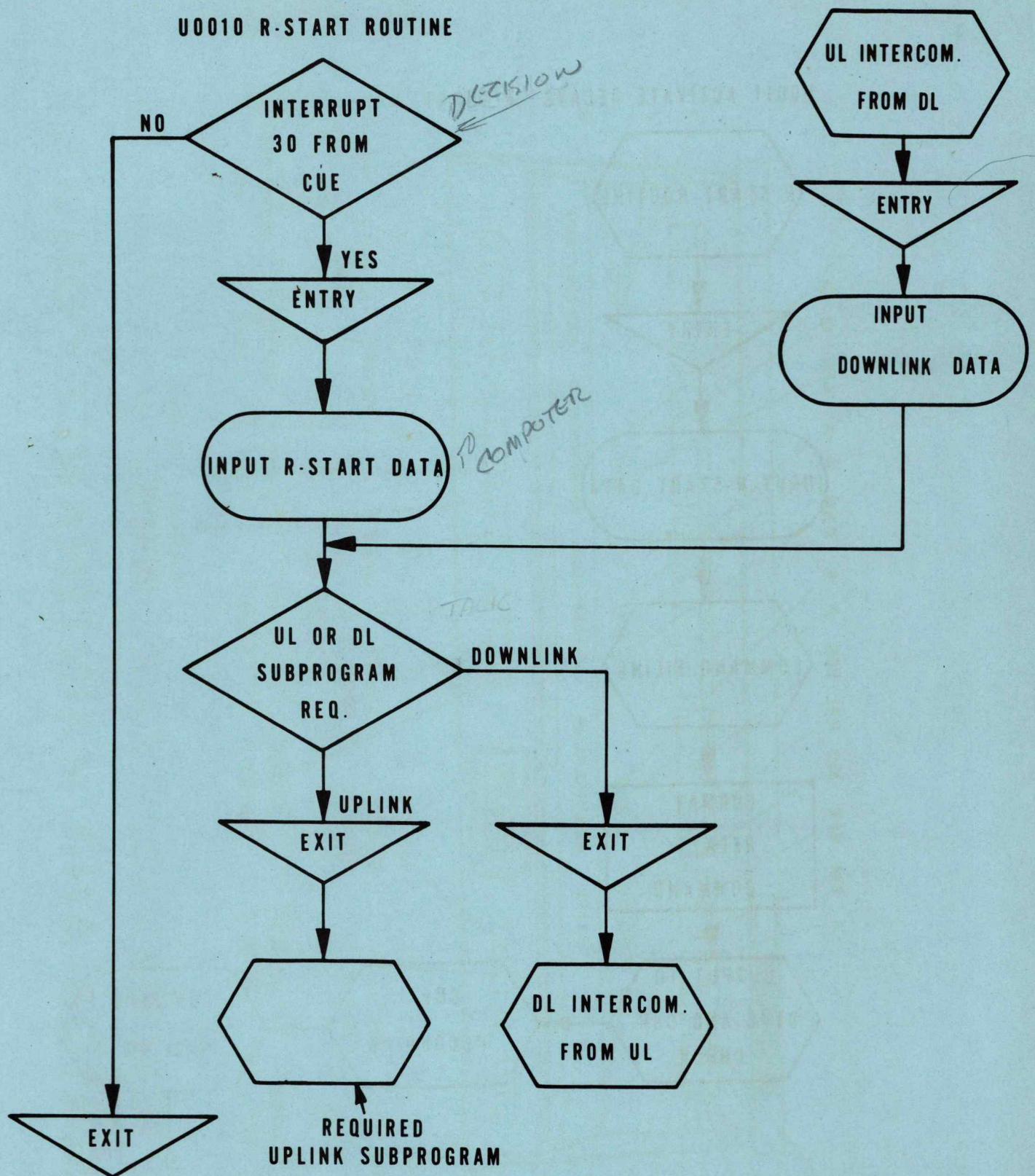
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OPERATOR AND MAINTENANCE CONSOLE

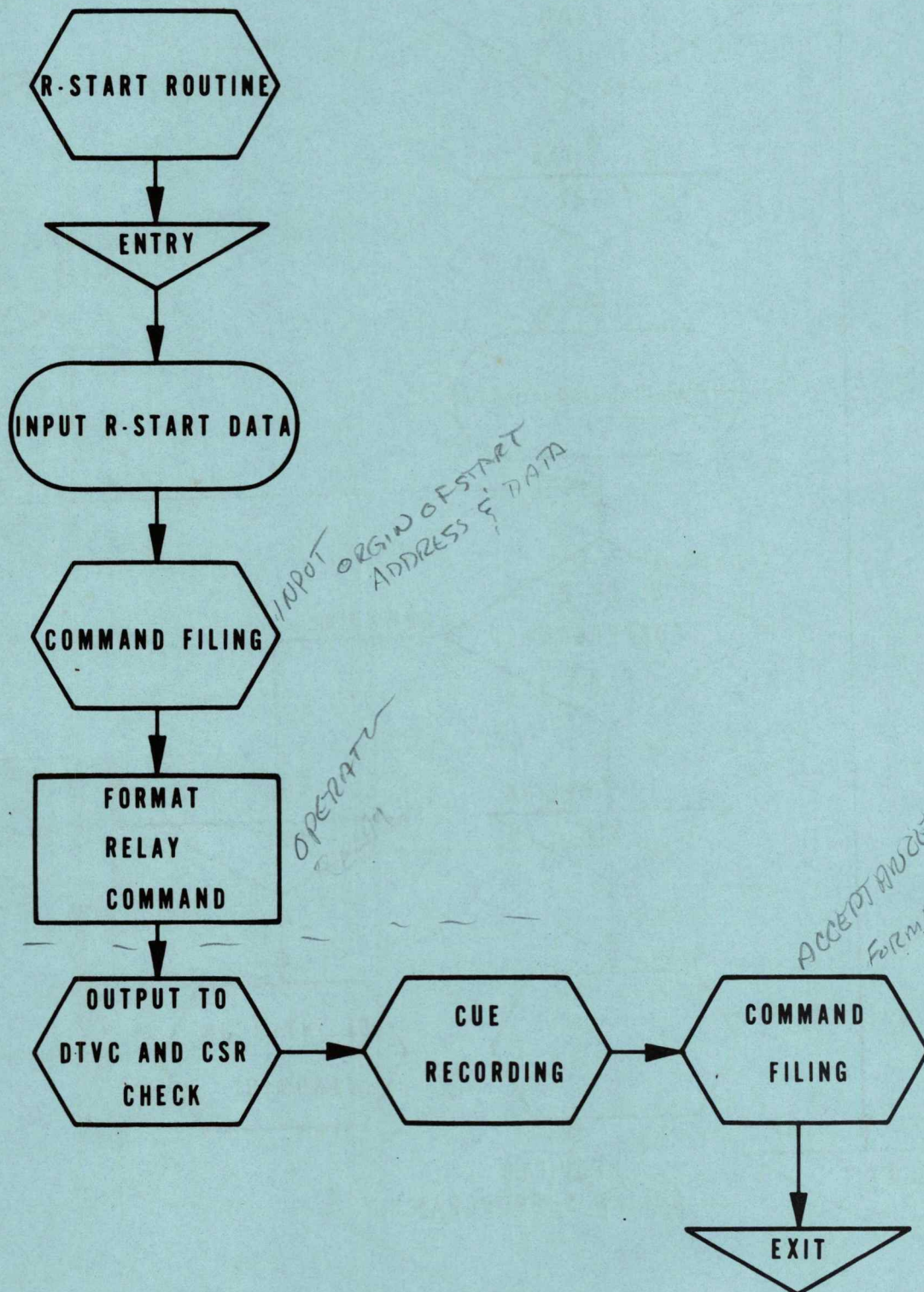
SYMBOLS IDENT ON 410-0106 Pg 46

U0010 R-START ROUTINE

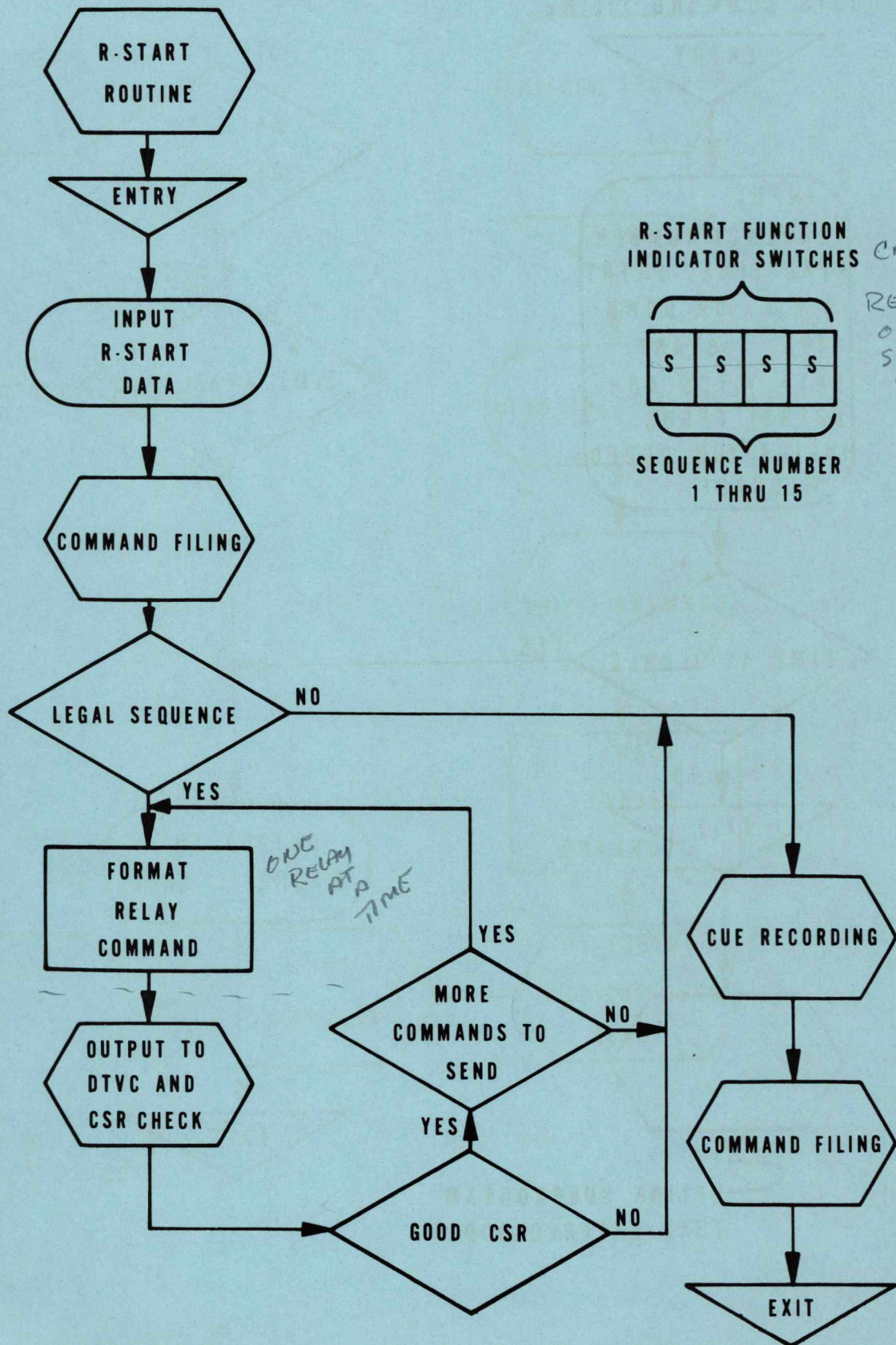


UPLINK - DOWNLINK CHECK
TALK TOGETHER THRU ?
169 & MEMORY LINK 3-15

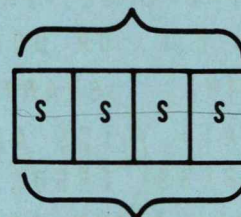
U0011 ACTIVATE RELAYS (R-START)



U0012 ACTIVATE RELAY SEQUENCE (R-START)



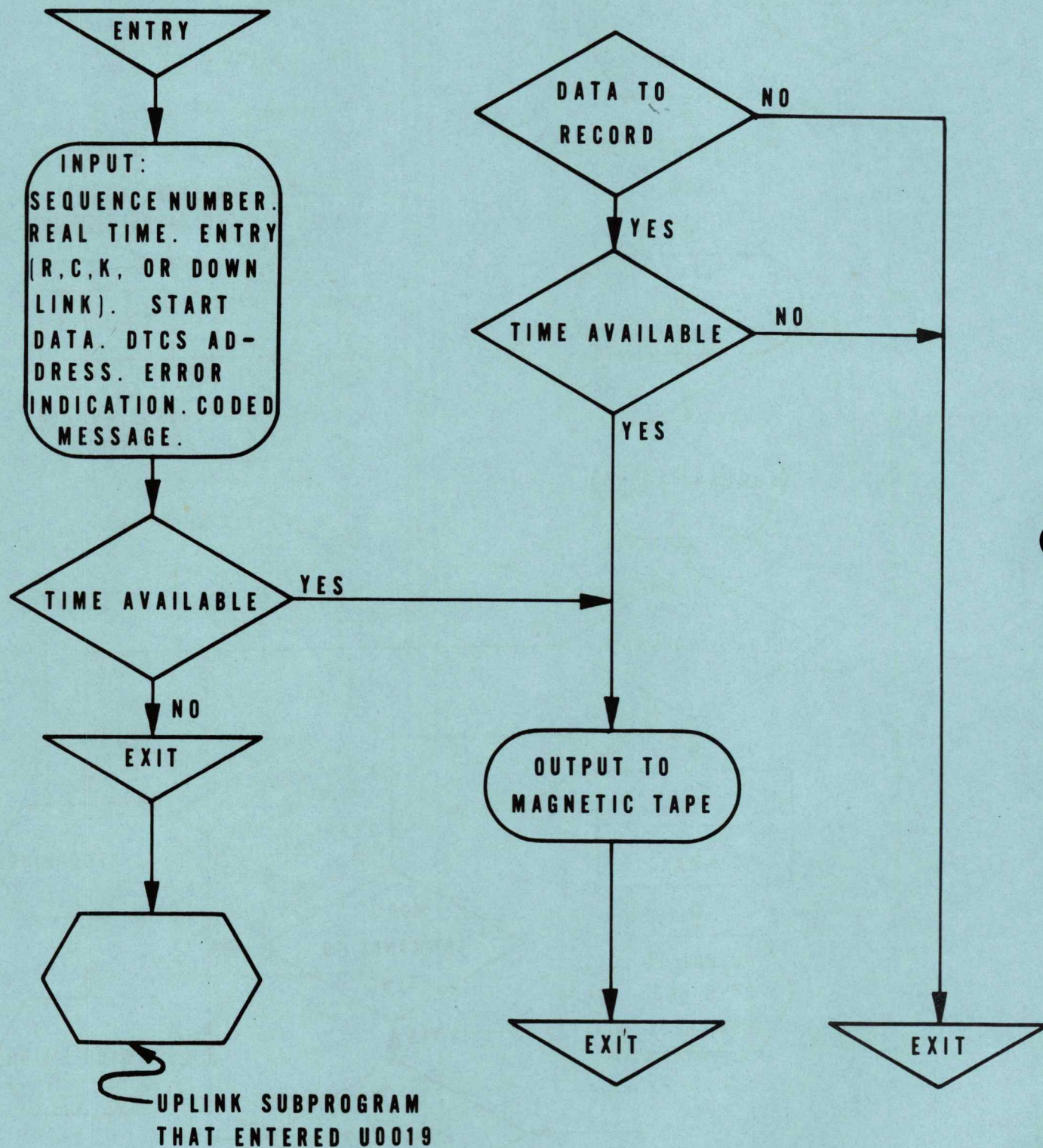
R-START FUNCTION
INDICATOR SWITCHES



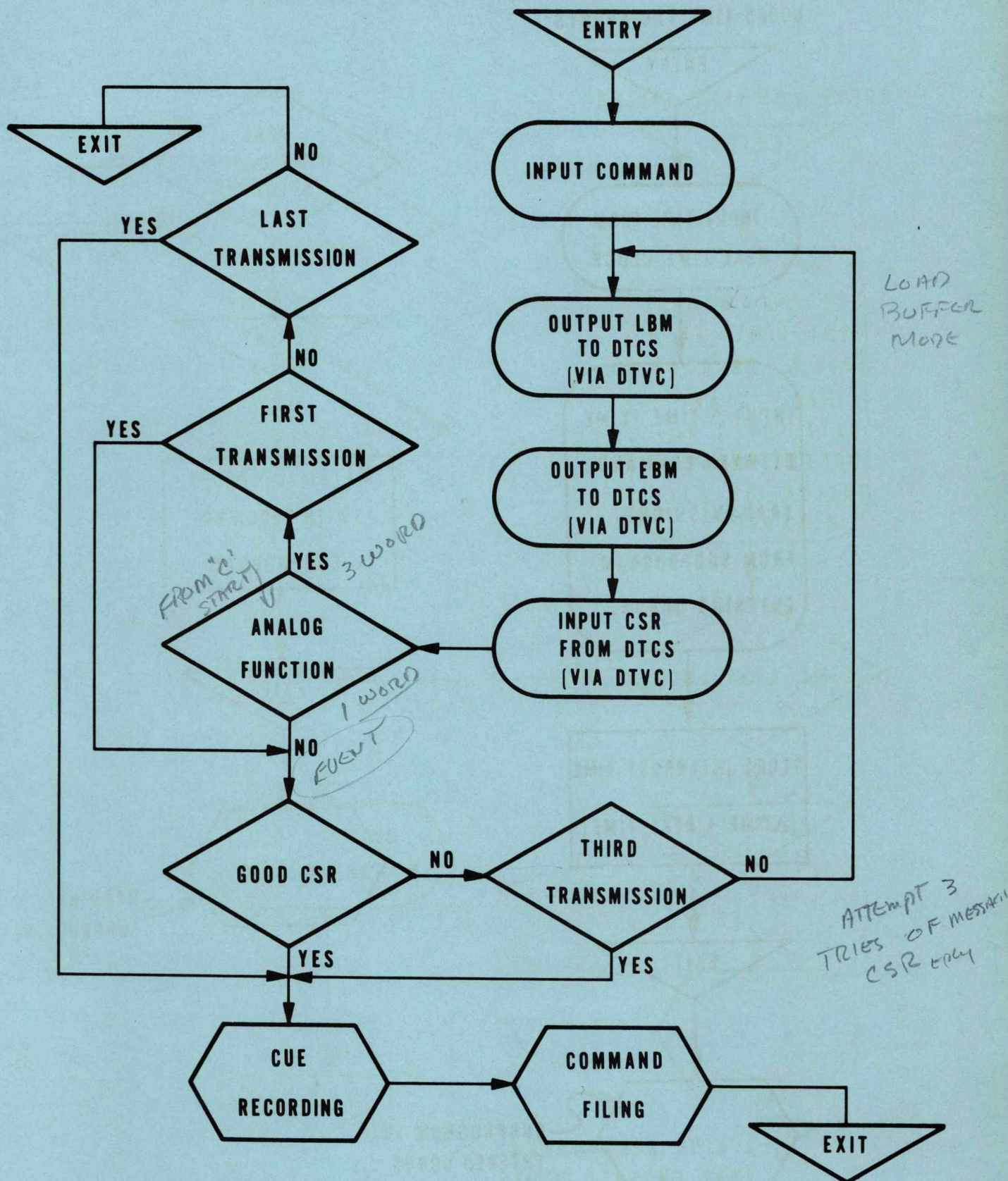
SEQUENCE NUMBER
1 THRU 15

*CAN
MEAN
RELAY START
OR
SEQUENCE
START*

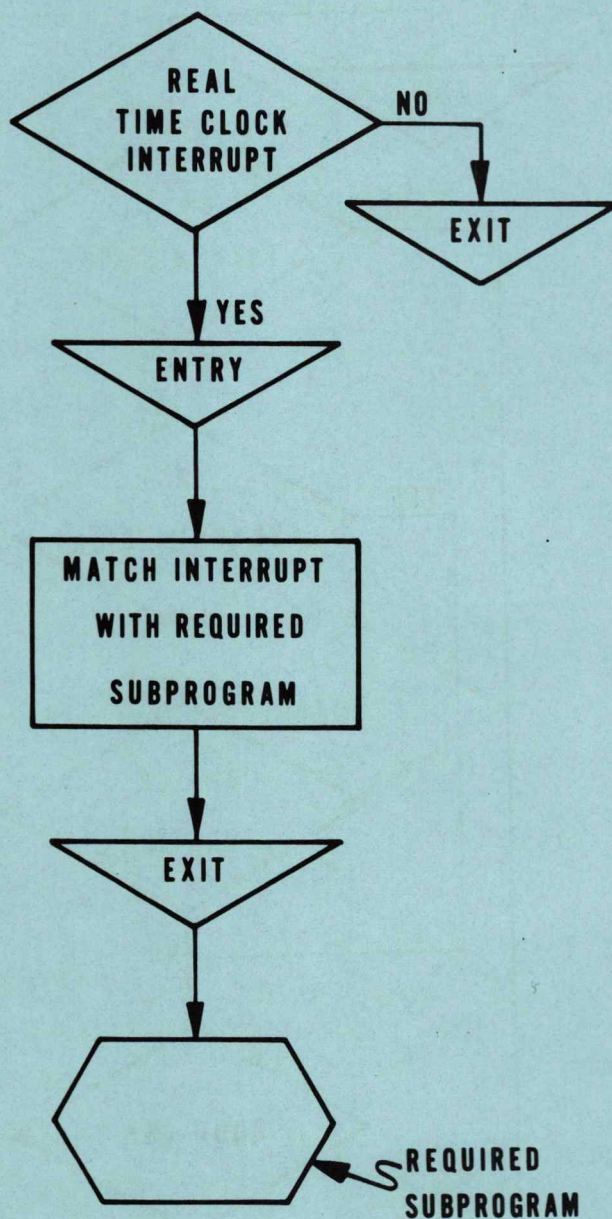
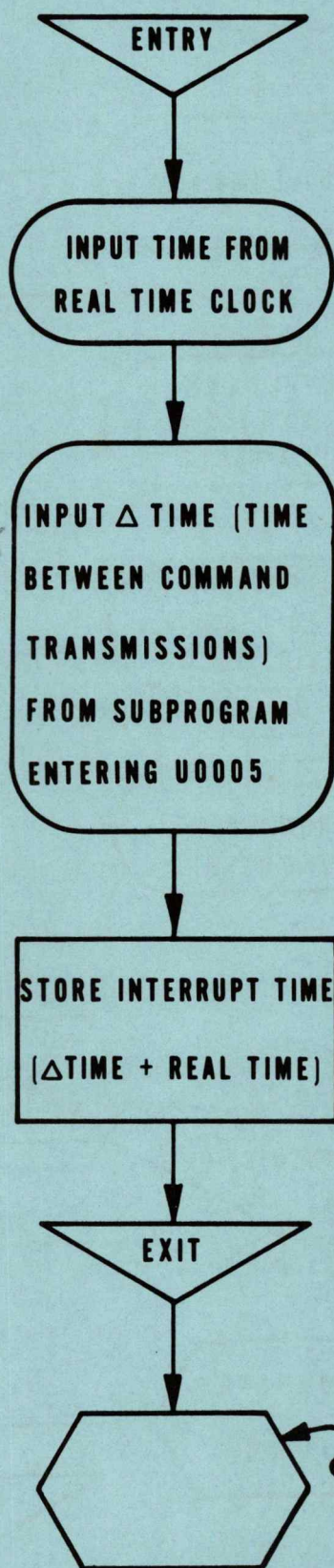
U0019 COMMAND FILING



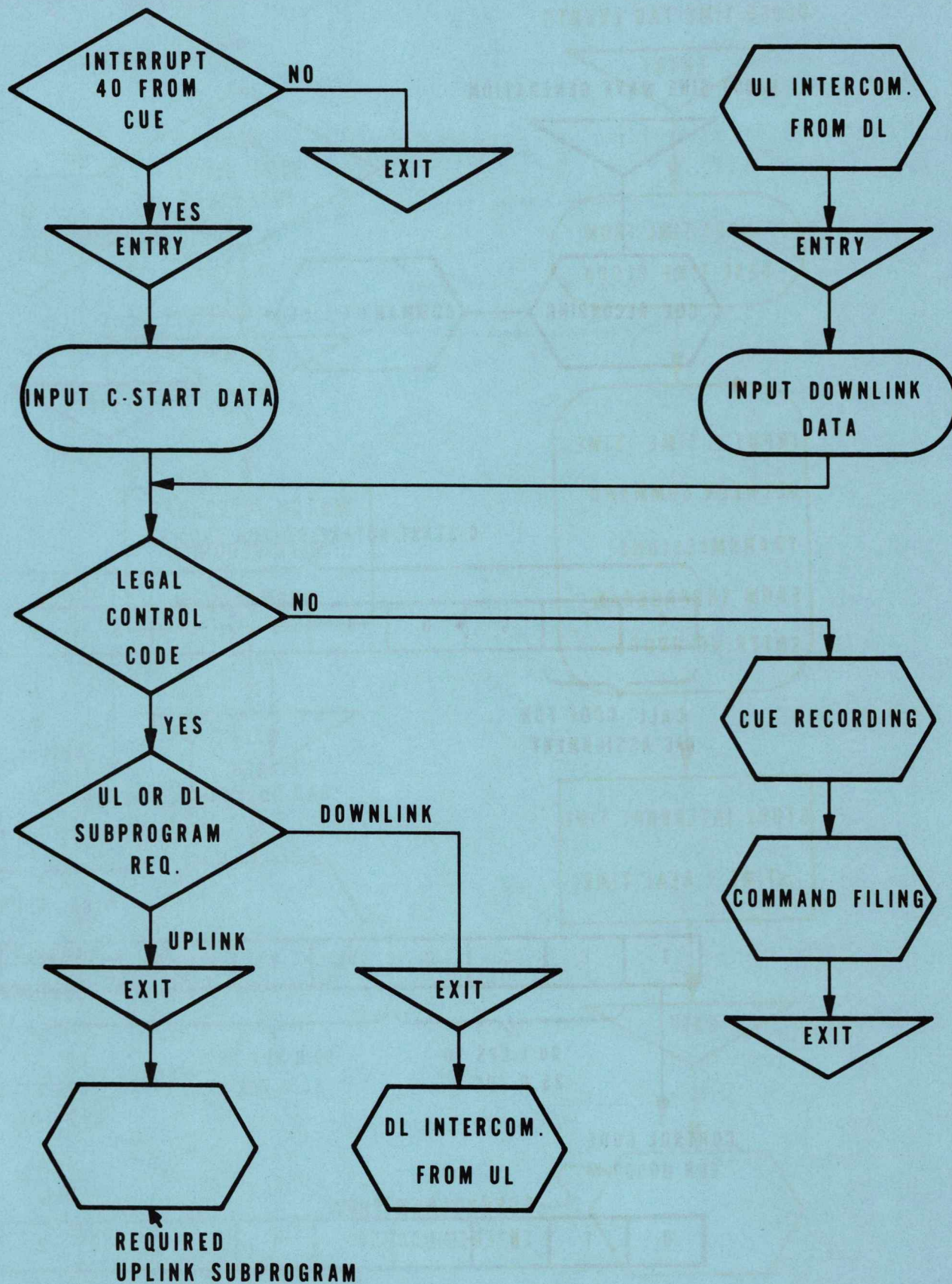
U0016 OUTPUT TO DTVC AND CSR CHECK



U0005 TIME TAG EVENTS

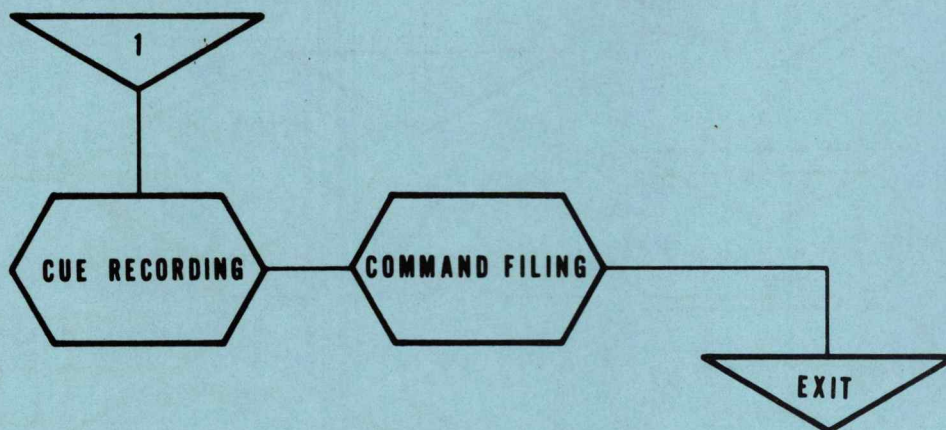


U0002 C-START ROUTINE

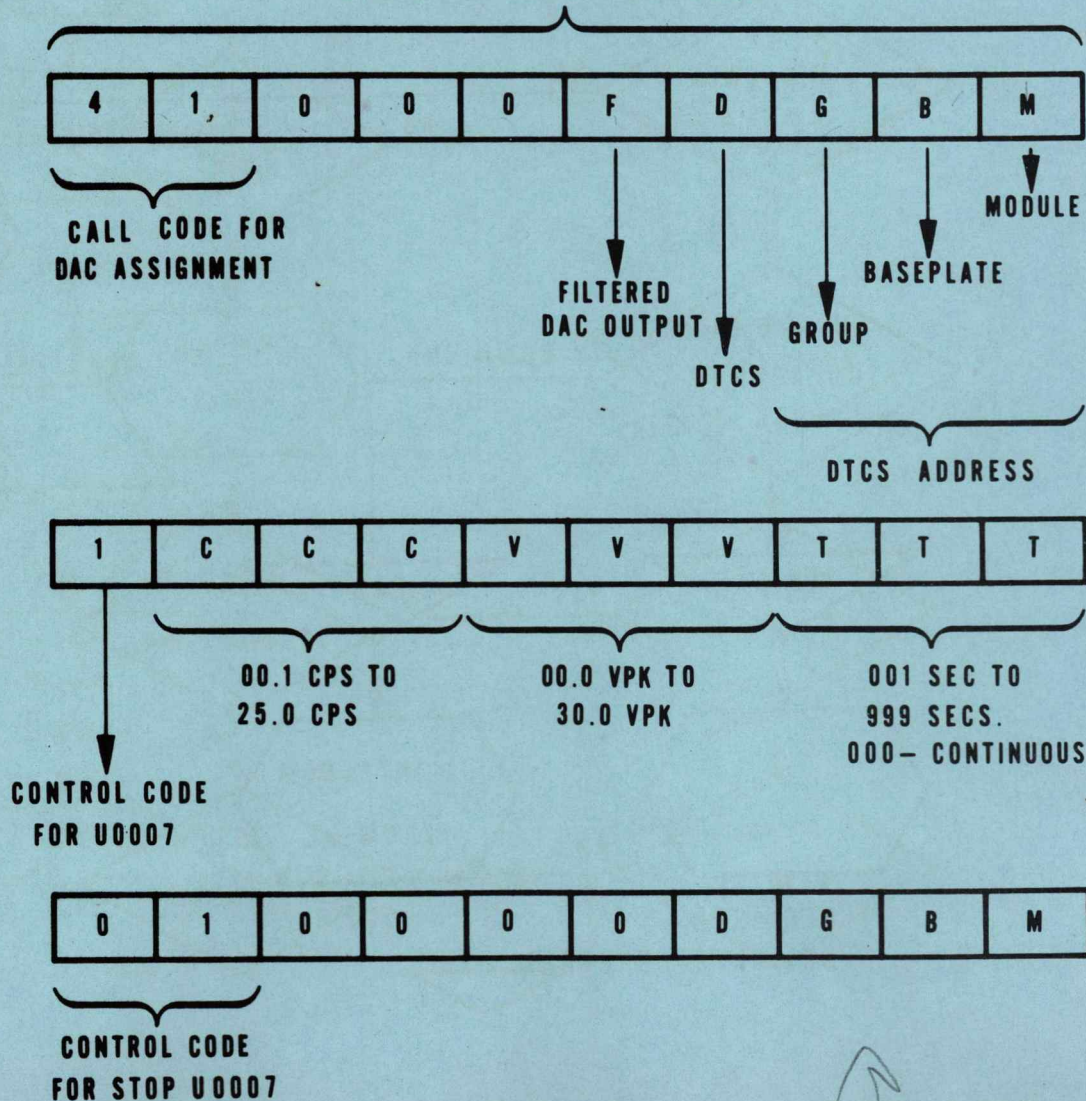


"C" START

U0007 SINE WAVE GENERATION

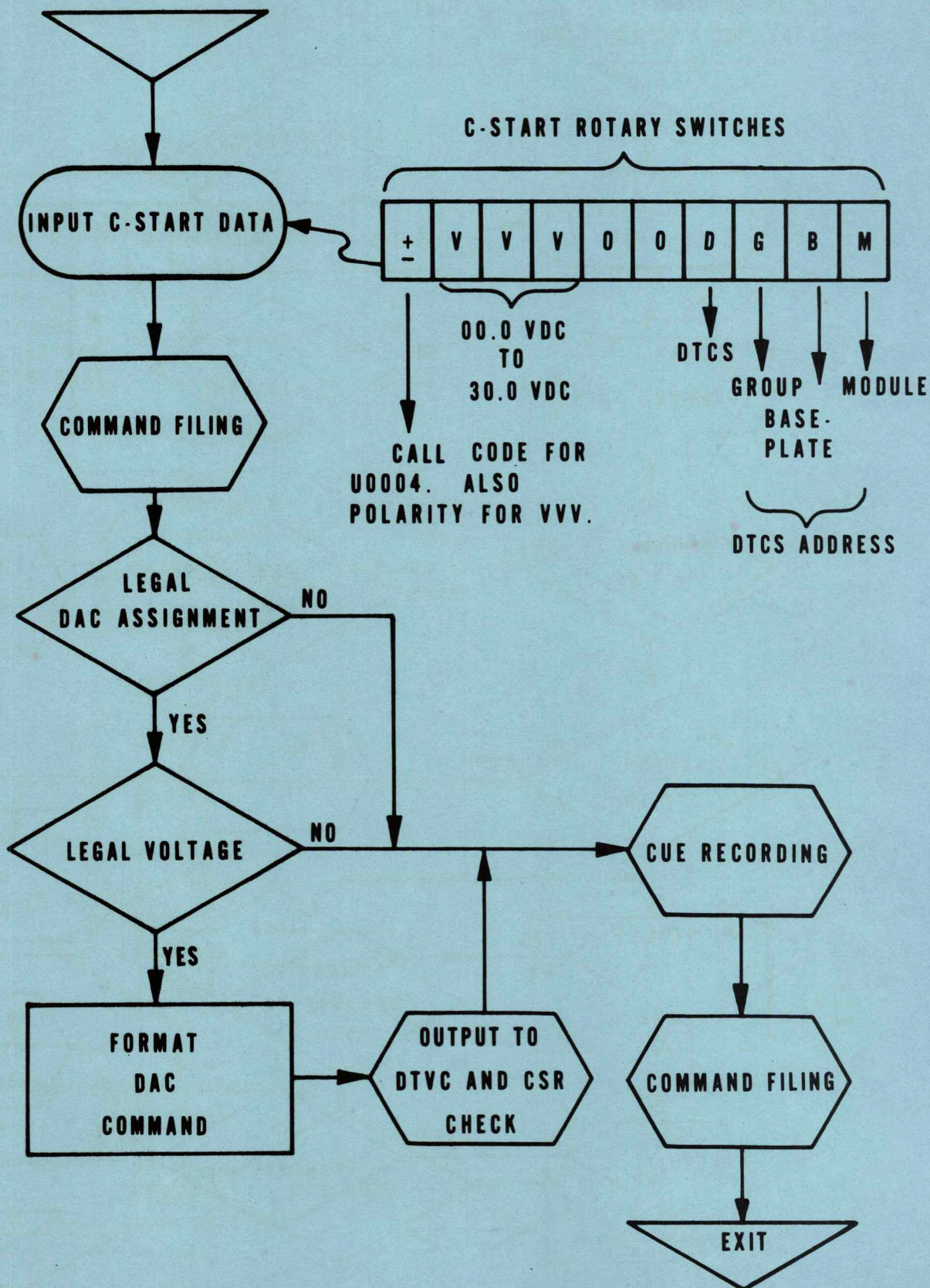


C-START ROTARY SWITCH FORMAT

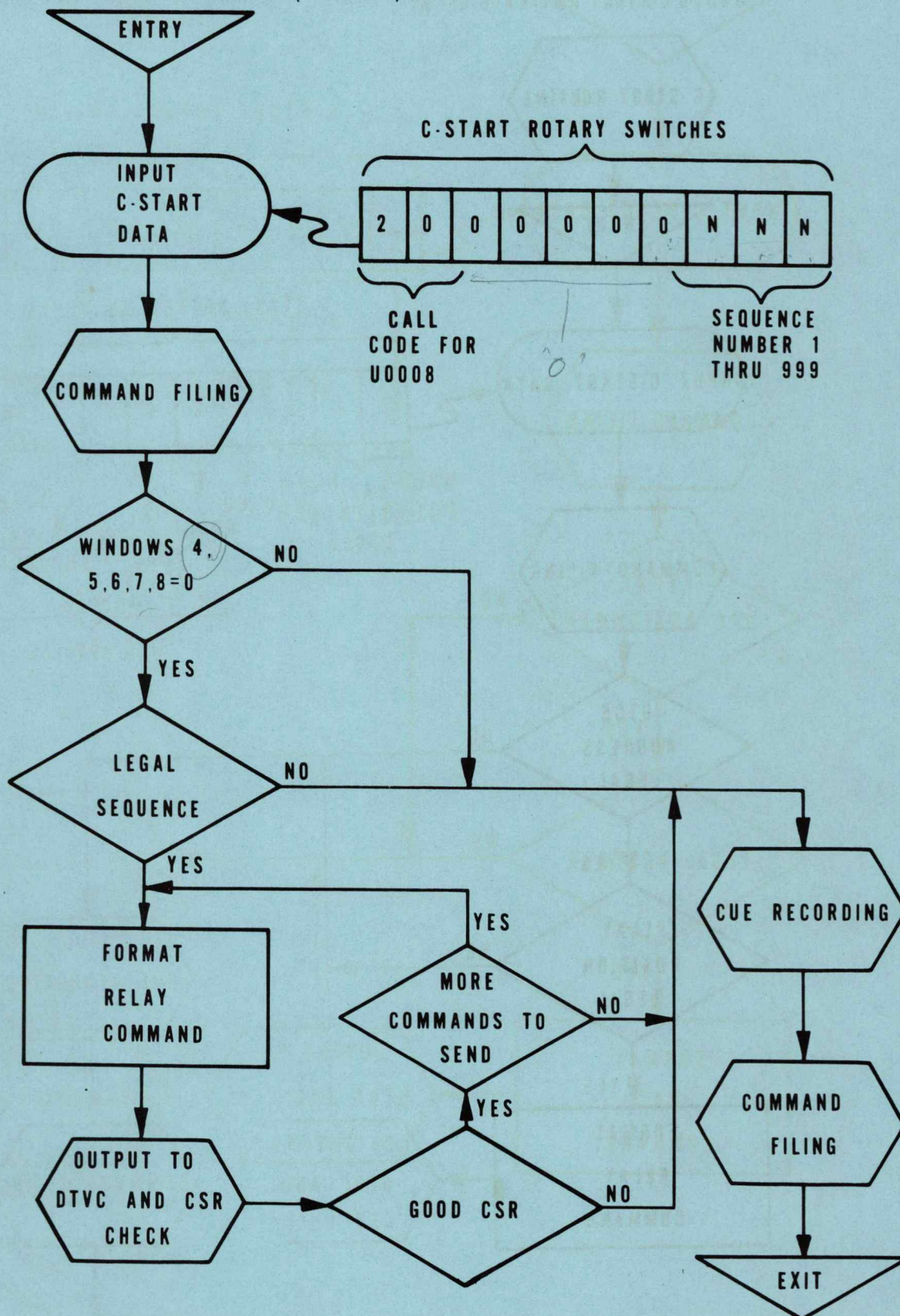




U0004 CONSTANT LEVEL DAC

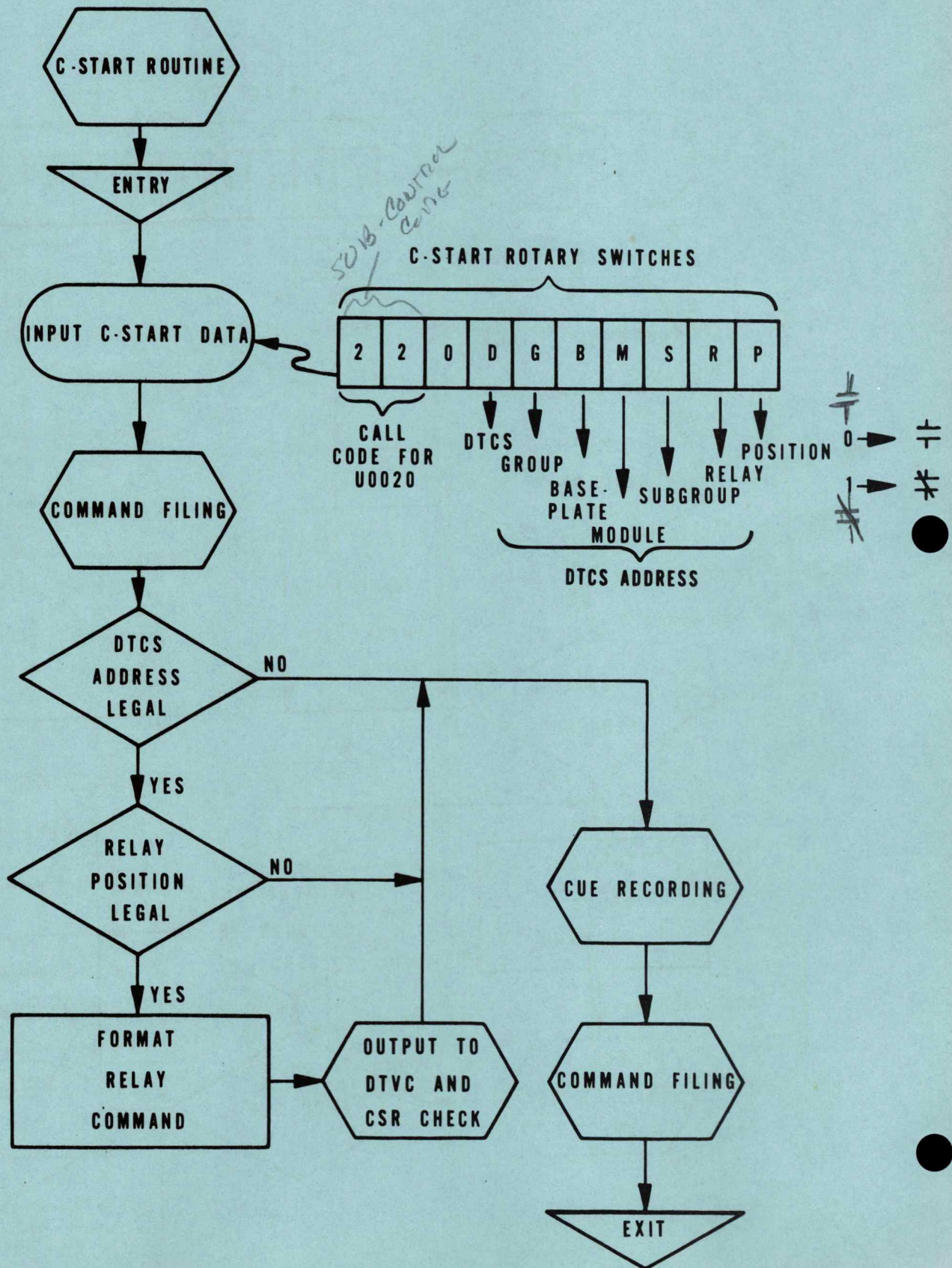


U0008 SEQUENTIAL CONTROL (C-START)

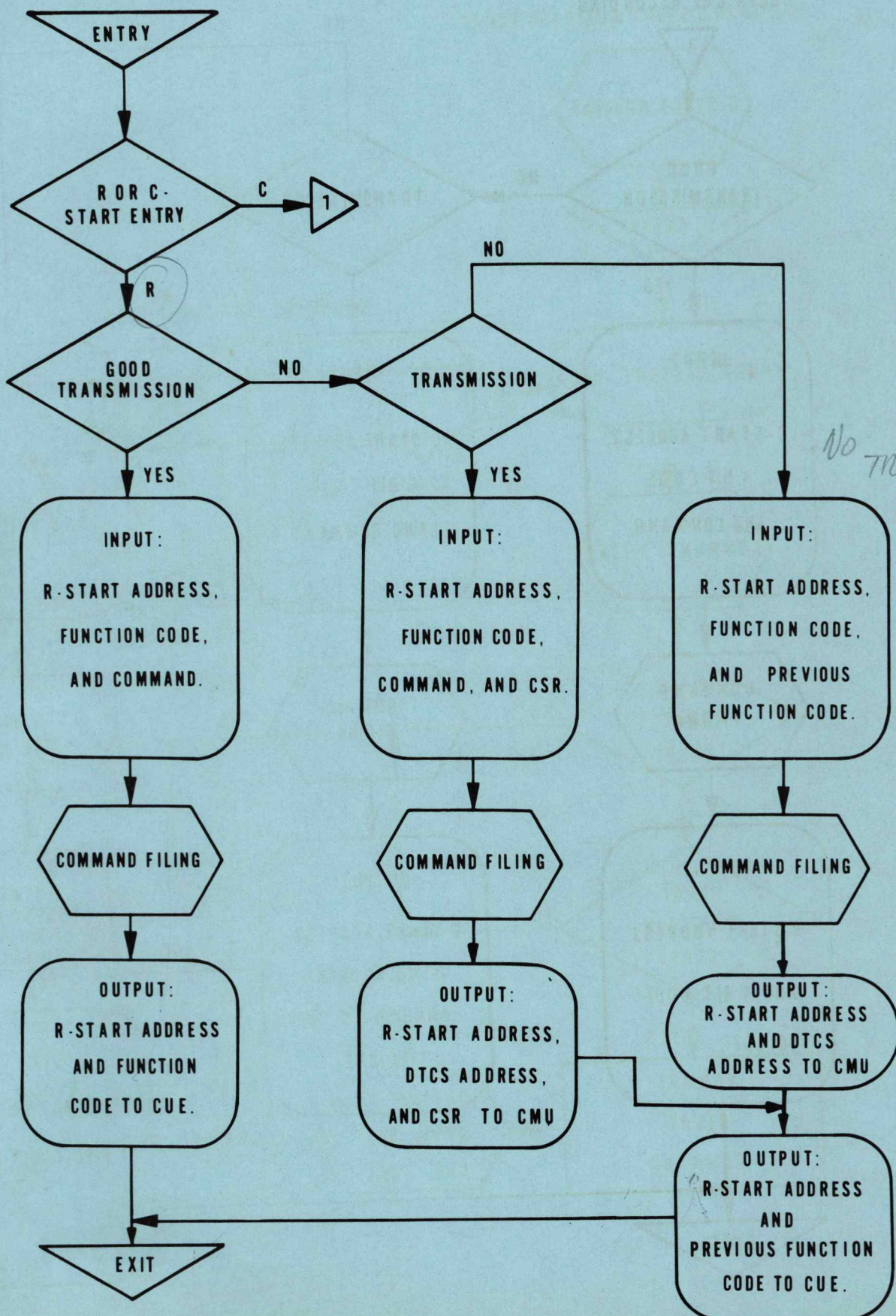


LEGAL CONTROL CODE

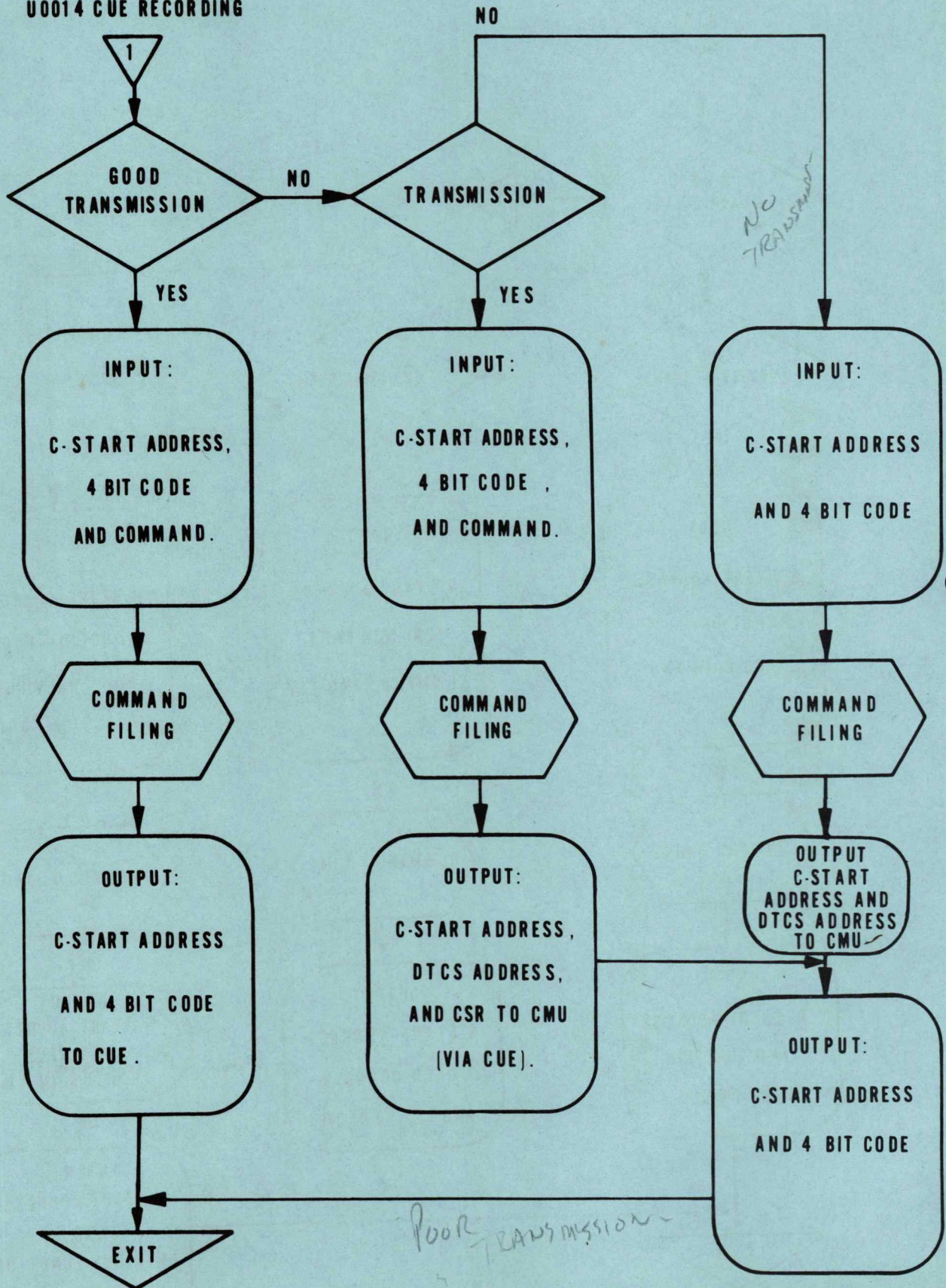
U0020 C-START ACTIVATE RELAY



U0014 CUE RECORDING



U0014 CUE RECORDING



LEM TEST AREA

CARRY-ON EQUIPMENT

410-92200 } DTCS
410-92201 }

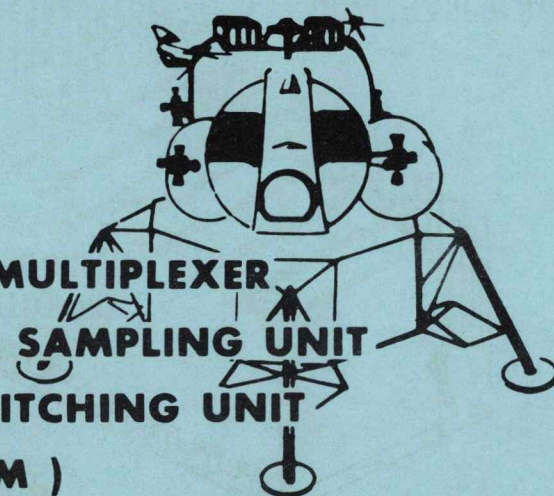
410-92210 PCM SUBSYSTEM

410-92211 DIGITAL SIGNAL CONDITIONING & MULTIPLEXER

410-92212 ANALOG SIGNAL CONDITIONING & SAMPLING UNIT

410-92213 G&N SIGNAL CONDITIONING & SWITCHING UNIT

ACE-S/C PECULIAR CARRY-ON EQUIPMENT (LEM)

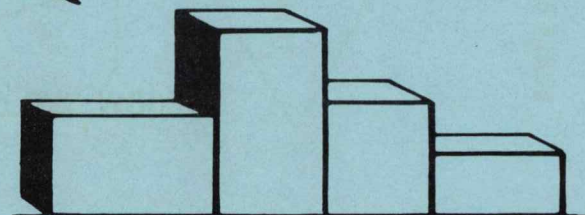


410-92241 S/E DTCS

410-92484 EXTERNAL SIGNAL CONDITIONER

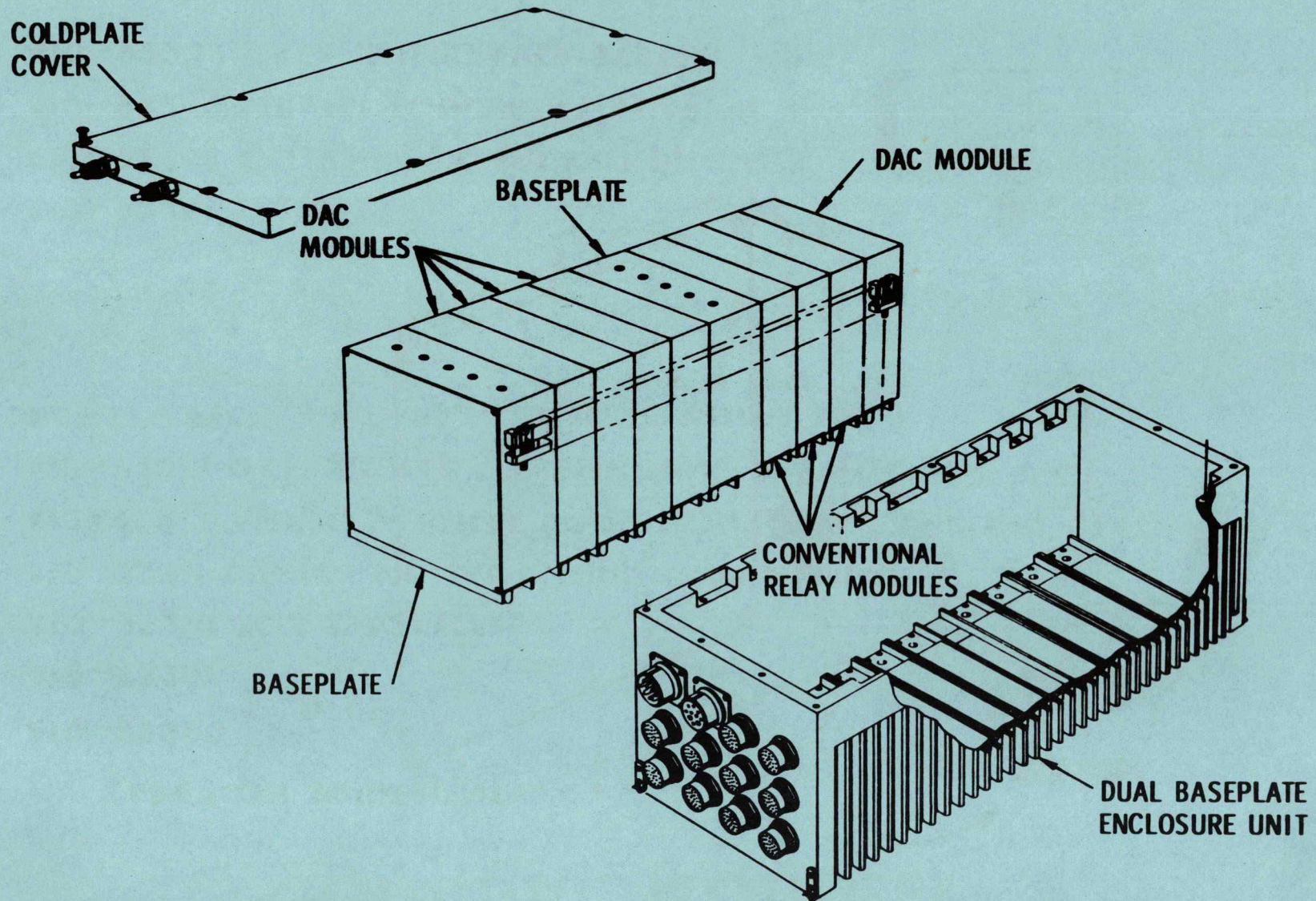
410-92240 SERVICE EQUIPMENT ADAPTER

410-92232 DATA INTERLEAVER SYSTEM (MDIS)



BASEPLATE GROUP

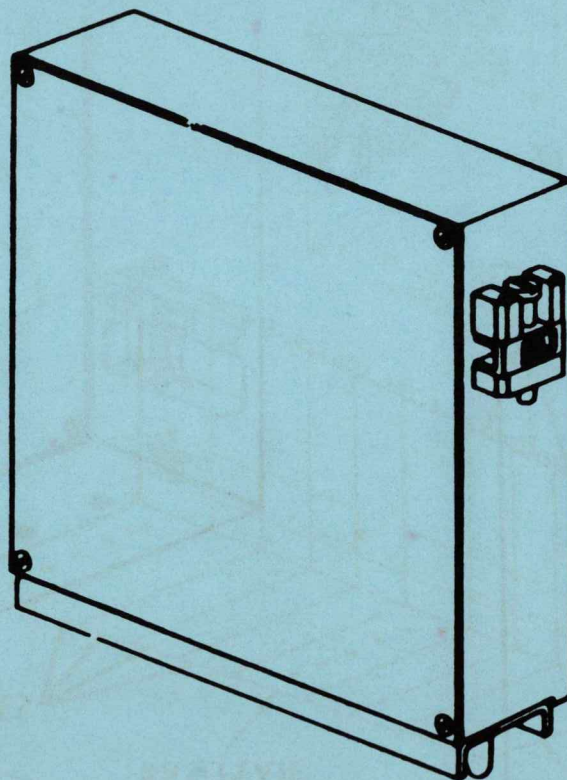
4-2



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LATCHING, CONVENTIONAL RELAY AND DAC MODULES

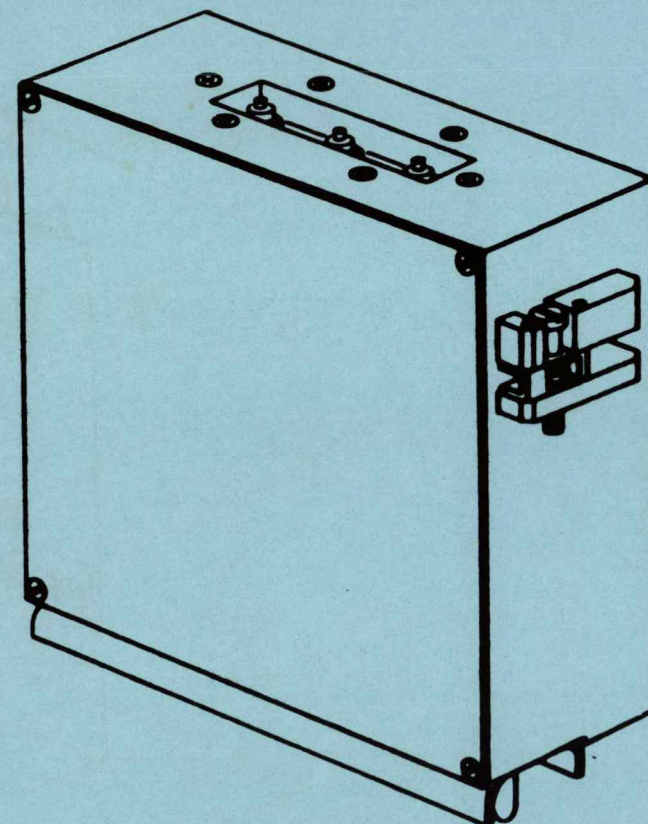
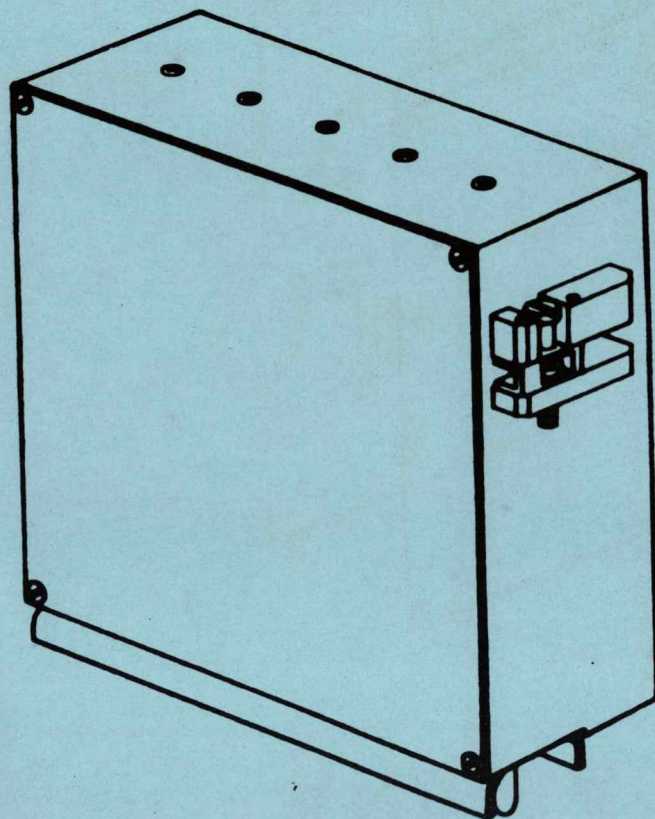


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BASEPLATE UNIT

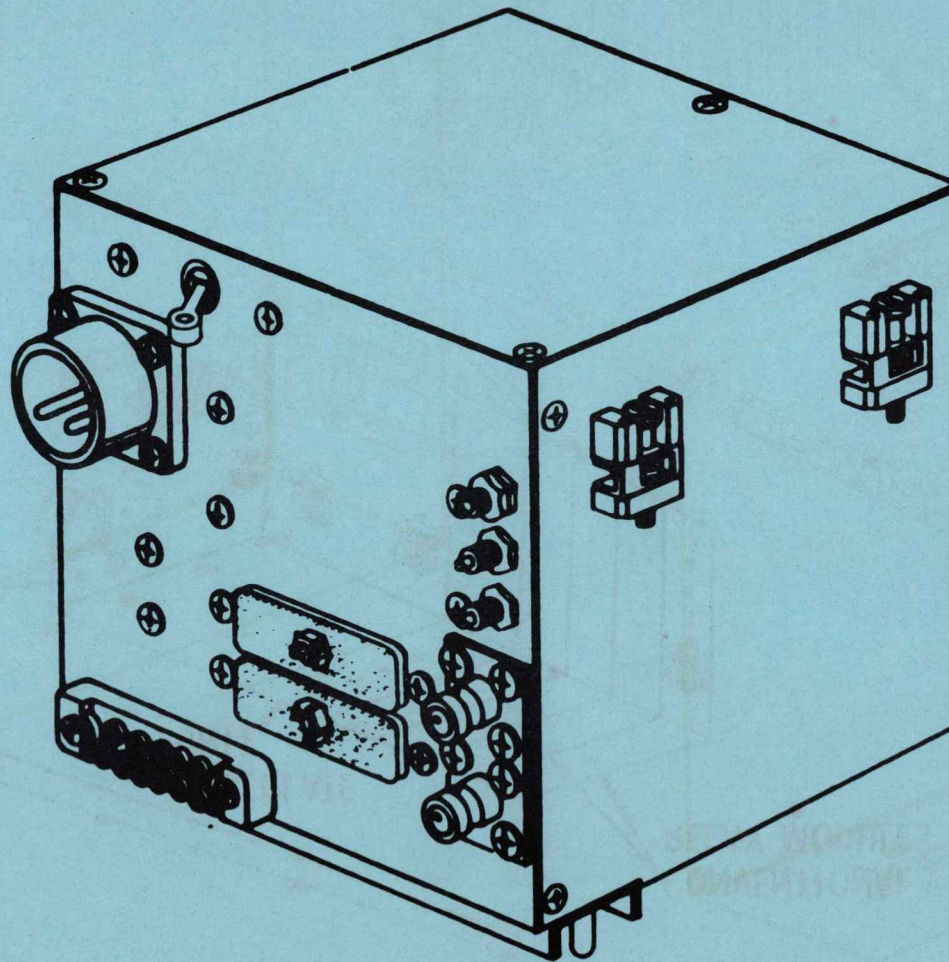
RESISTOR BANK



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FOR TRAINING PURPOSES ONLY

RECEIVER-DECODER UNIT



FOR TRAINING PURPOSES ONLY

FOR TRAINING PURPOSES ONLY

RECEIVER GROUP

4-6

COLDPLATE
COVER

CONVENTIONAL
RELAY MODULES

BASEPLATE
UNIT

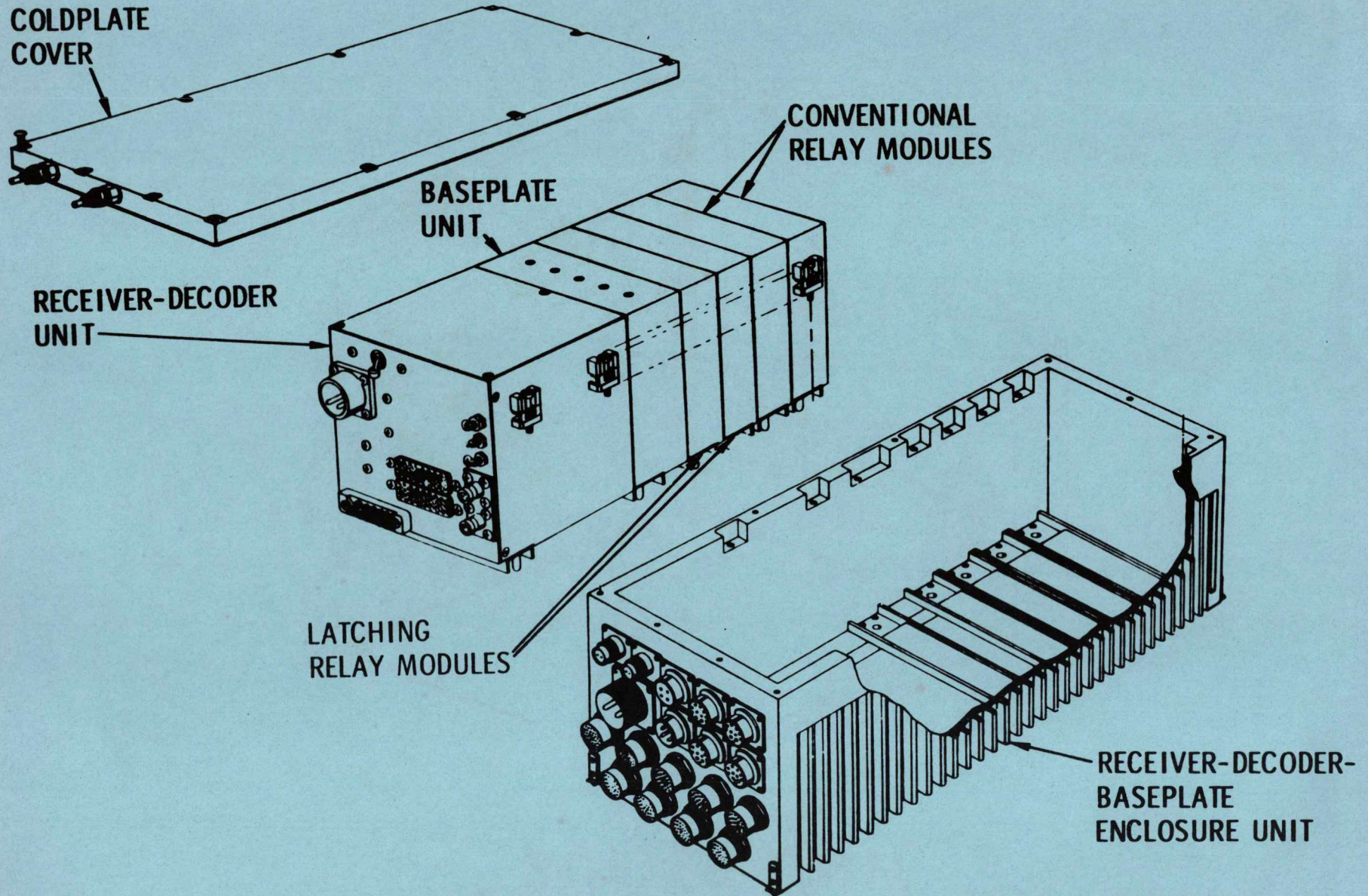
RECEIVER-DECODER
UNIT

LATCHING
RELAY MODULES

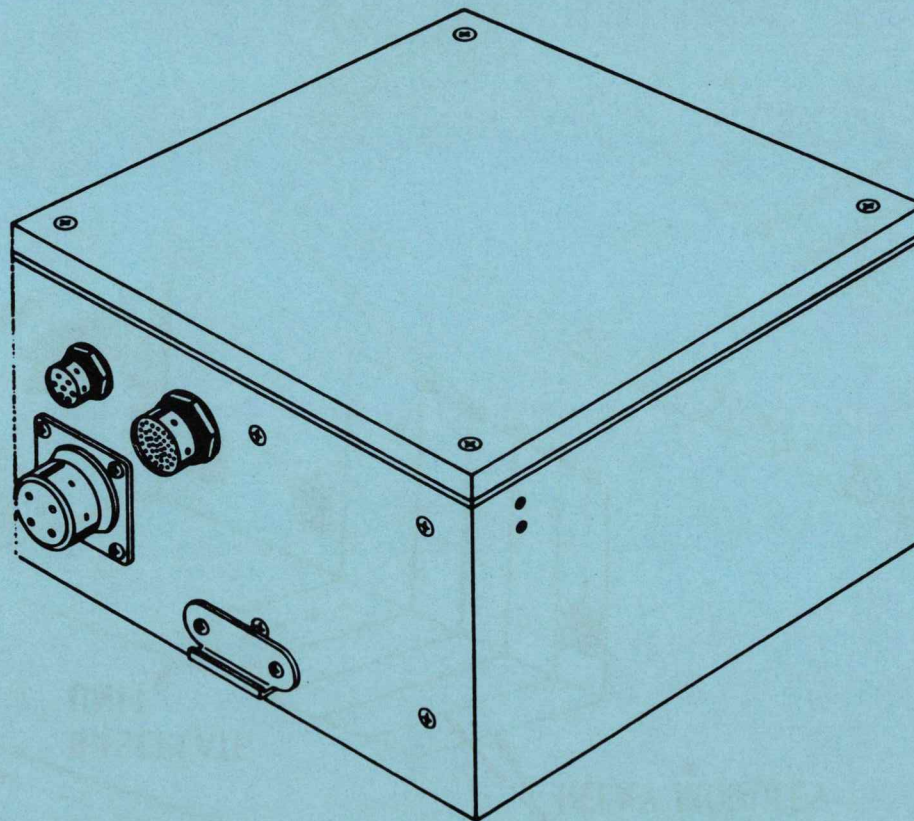
RECEIVER-DECODER-
BASEPLATE
ENCLOSURE UNIT

FOR TRAINING PURPOSES ONLY

FOR TRAINING PURPOSES ONLY



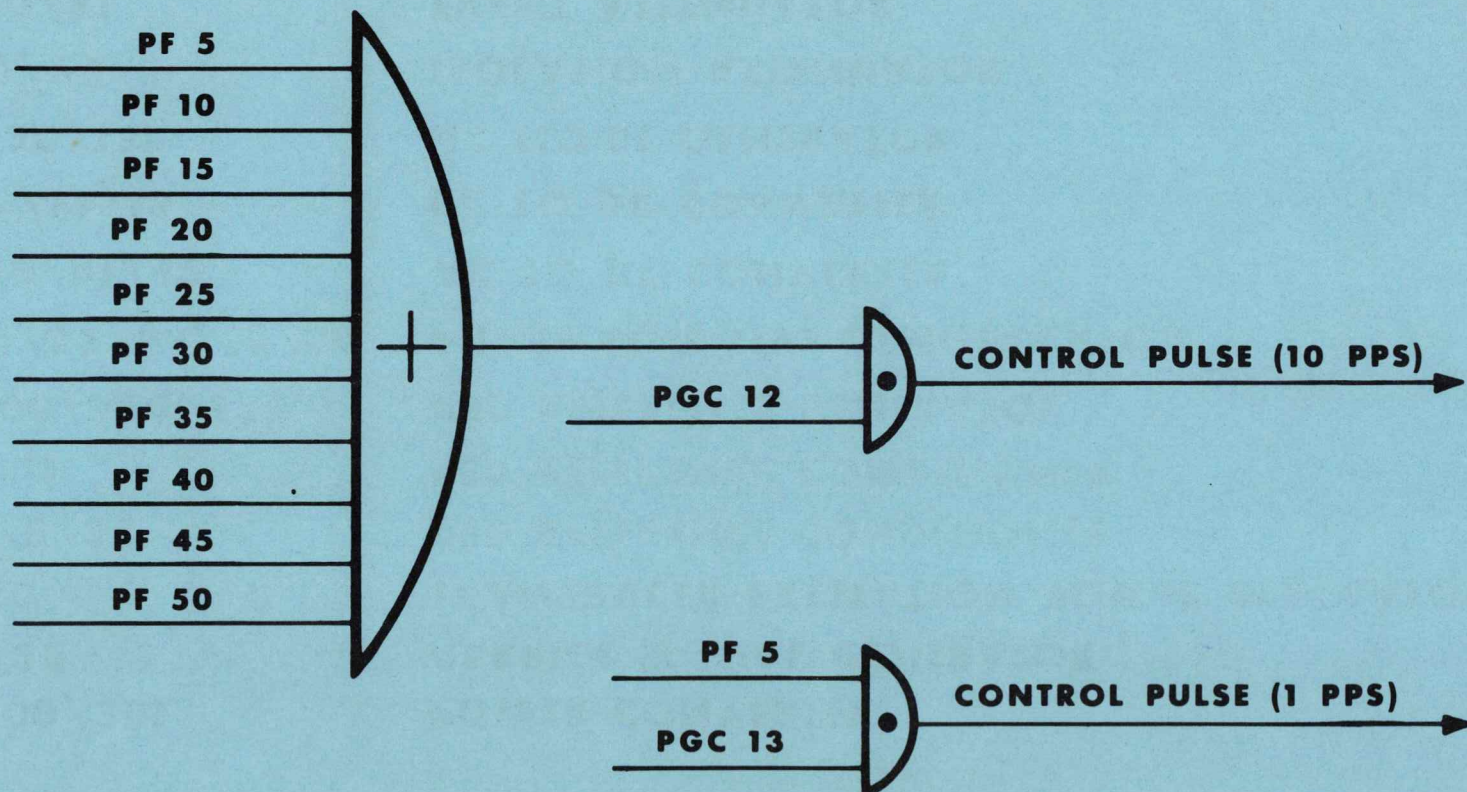
GUIDANCE AND NAVIGATION BUFFER UNIT



FOR TRAINING PURPOSES ONLY

FOR TRAINING PURPOSES ONLY

WORD SELECT SIMPLIFIED



FOR TRAINING PURPOSES ONLY

FOR TRAINING PURPOSES ONLY

C14-212 ANALOG SIGNAL CONDITIONER MODULES

FOR TRAINING PURPOSES ONLY

PVR 200/201

CAG 220

TER 210

REC 4/8/32

REC 25.6

REG 800/3200/25.6

PSD 51/52/53/55/56

ACD 40/41/42

DCD 11/12/13

ANC 130/131

ISA 20/22

EVA 70/71

ASR 230

FRD 60

DCA 02

VRD 30

POWER CONVERTER

CARRIER SIGNAL GENERATOR

TRANSDUCER EXCITATION POWER REGULATOR

PSD REFERENCE CONDITIONER

PSD REFERENCE CONDITIONER

PSD REFERENCE GENERATOR

PHASE SENSITIVE DEMODULATOR

AC TO DC CONVERTER

DC TO DC CONVERTER

AC NOISE GENERATOR

ISOLATION ATTENUATOR

EVENT ATTENUATOR

ANALOG STANDARD REGULATOR

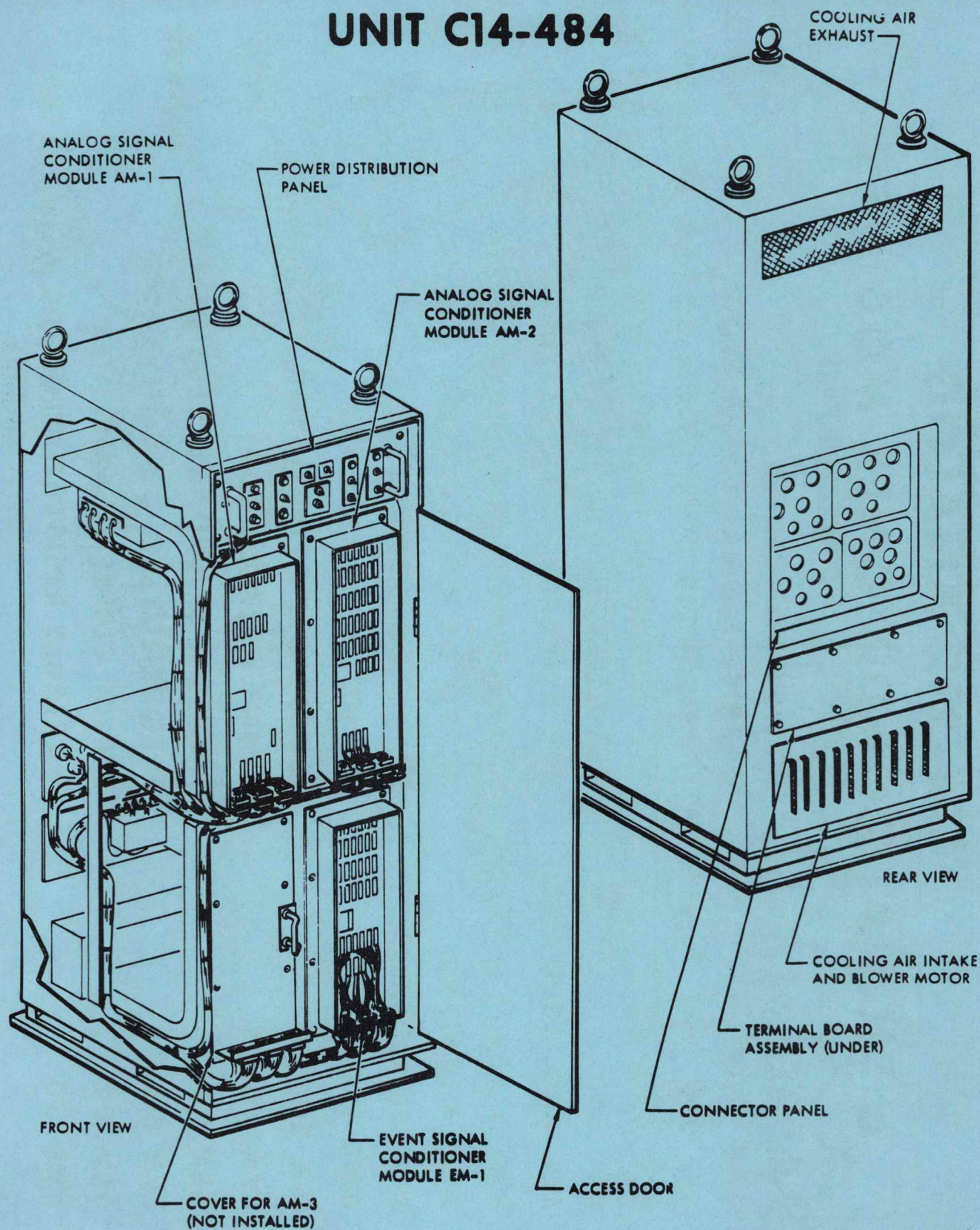
FREQUENCY TO DC CONVERTER

DIRECT CURRENT AMPLIFIER

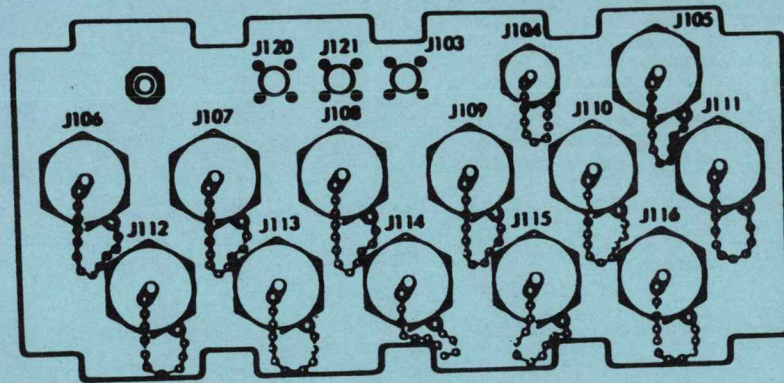
VARIABLE RESISTANCE TO DC CONVERTER

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EXTERNAL SIGNAL CONDITIONING UNIT C14-484



MDIS ENCLOSURE



CONNECTOR PANEL

VIEW A

PHASE LOCKED
OSCILLATOR

POWER
CONVERTER

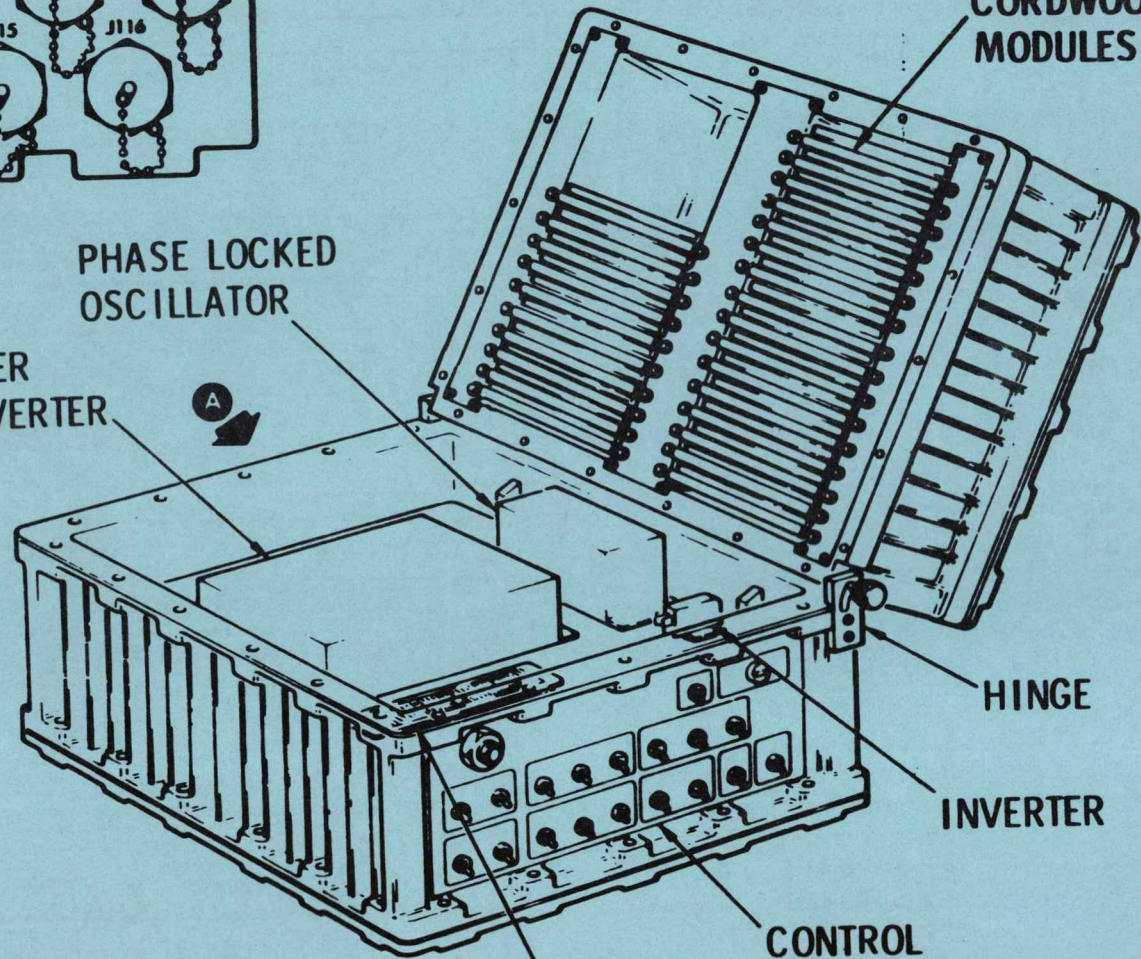
CORDWOOD
MODULES

HINGE

INVERTER

CONTROL
PANEL

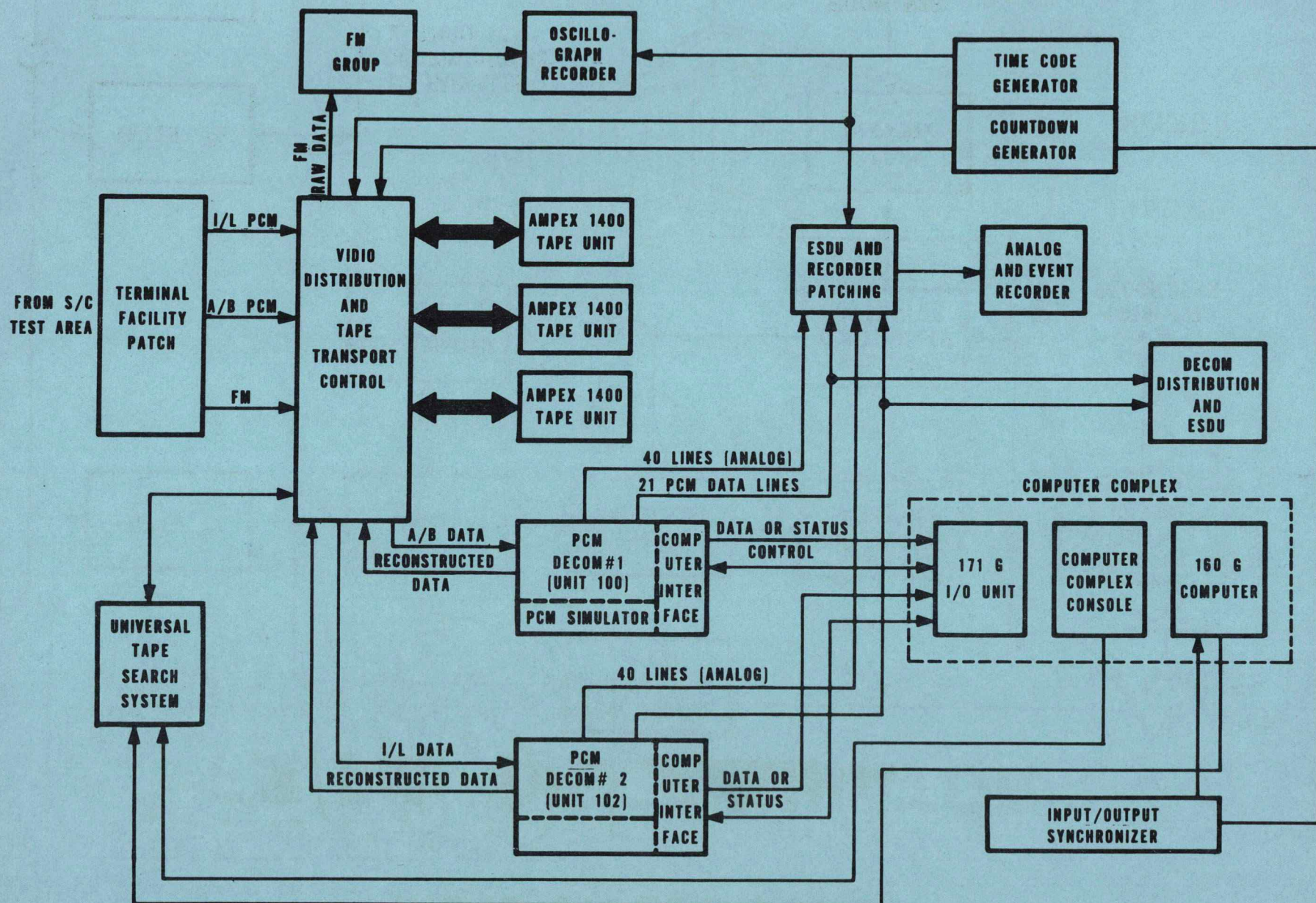
TERMINAL
MODULE



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FOR TRAINING PURPOSES ONLY

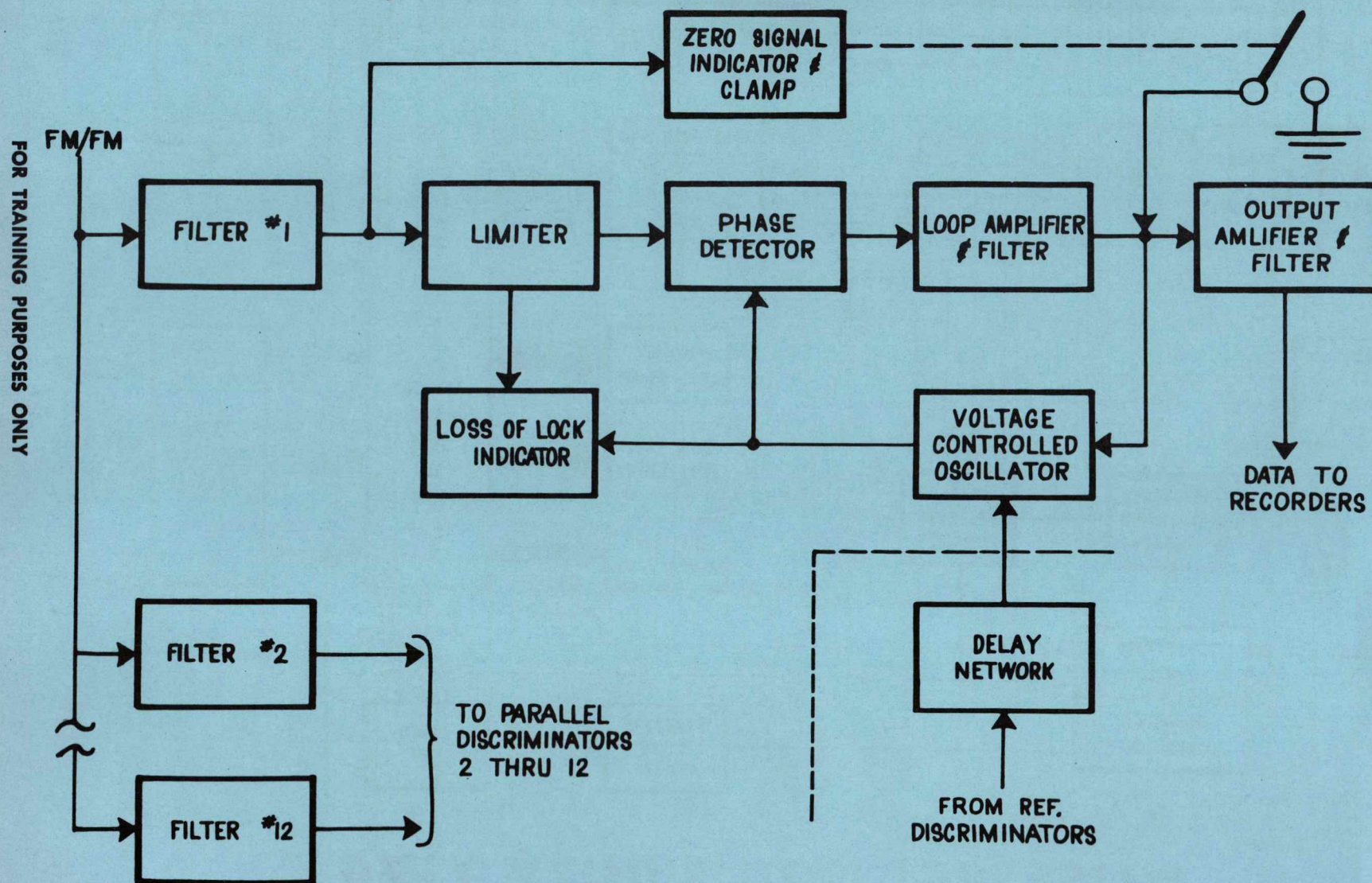
DATA ACQUISITION SUBSYSTEM



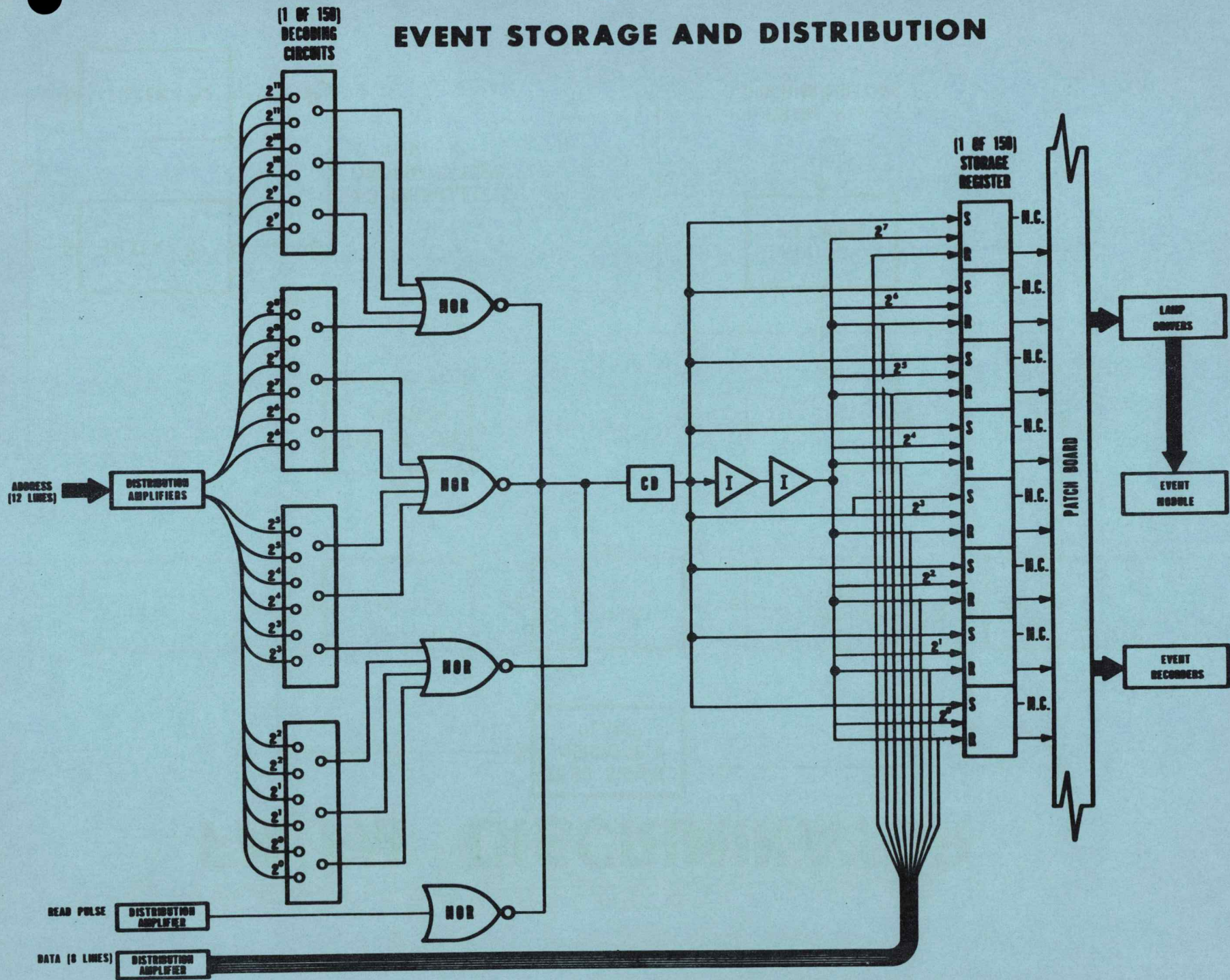
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FM/FM DISCRIMINATOR



EVENT STORAGE AND DISTRIBUTION



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DISPLAY SCOPE CHART FORMATS

DISPLAY SCOPE SPACING CHART										PROJECT		TEST				
										VEHICLE		PAGE				
										SYSTEM		DATE				
LINE	FIELD I				FIELD II						FIELD III		FIELD IV			
1	S	Y	S	P	G	O	L	O	S							
2	← 1 3 →				→											
3																
4																
5																
6																
7	M	E	A	S	N	O	M E A S . D E S C R I P T I O N				D A T A		U N I T			
8	← 6 →				← 2 1 →						← 8 →		← 4 →			
9																
10																
11																
12																
13	M	E	A	S	N	O	M E A S . D E S C R I P T				D A T A		D A T A		U N I T	
14	← 6 →				← 1 4 →						← 7 →		← 8 →		← 4 →	
15																
16																
17																
18	M	E	A	S	N	O	M E A S D E S		D A T A		D A T A		D A T A		U N I T	
19	← 6 →				← 7 →		← 7 →		← 7 →		← 8 →		← 4 →			
20																
21																
22																
23	D E S C R		P T I O N		D A T A		D E S C R I P		I O N		D A T A					
24	← 4 →		← 6 →		← 1 4 →		← 6 →									
25																
26	P A G E		R R O R		S Y S		P G N O		P A G E		E R R O R					

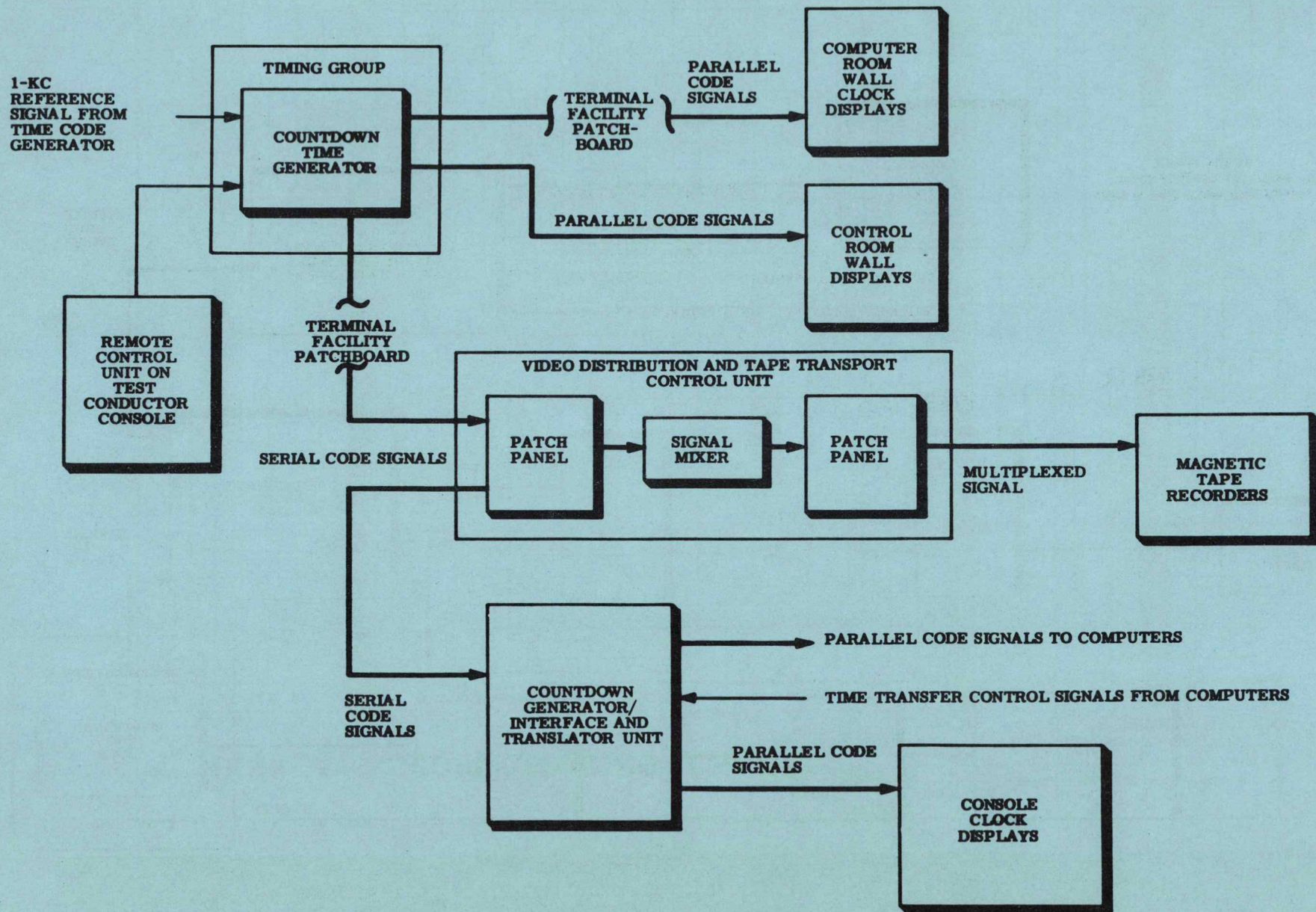
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DISPLAY SCOPE SPACING CHART GIVING AN EXAMPLE OF DOUBLE MEASUREMENT PER LINE

DISPLAY SCOPE SPACING CHART										PROJECT APOLLO		TEST 6.4																
										VEHICLE AF 11		PAGE 3																
										SYSTEM RCS		DATE 5 FEBRUARY 1964																
LINE	FIELD I					FIELD II										FIELD III				FIELD IV								
TOP HALF PAGE	1	R	C	S	P	G	2	L	O	S																		
	2																											
	3	C	R	0	0	0	1	H	E	P	R	E	S	S														
	4	C	R	0	0	0	3	H	E	T	E	M	P															
	5	C	R	0	0	0	7	F	U	E	L	Q	U	A	N	T	I	T	Y									
	6	C	R	0	0	1	3	O	X	I	D	I	Z	E	R	Q	U	A	N	T								
	7	C	R	0	5	0	2	H	E	R	E	G	O	U	T													
	8						S	E	V	I	C	E	M	O	D	-	R	C	S									
	9	S	R	5	0	0	1	H	E	P	R	E	S	S														
	10	S	R	5	0	0	5	H	E	T	E	M	P															
BOTTOM HALF PAGE	11	S	R	5	0	1	3	F	U	E	L	Q	U	A	N	T	I	T	Y									
	12	S	R	5	0	2	5	O	X	I	D	I	Z	E	R	Q	U	A	N	T								
	13	S	R	5	0	6	5	E	N	G	I	N	E	P	A	C	K	A	G	E								
	14																											
	15	T	D	0	1	8	5	T	W	R	P	Y	R	O	B	U	S											
	16	C	D	0	2	0	0	L	E	S	L	O	G	I	C	B	U	S										
	17	C	D	0	2	0	5	A	D	A	P	T	E	R	P	Y	R	O										
	18	T	D	0	0	0	5	L	E	S	P	Y	R	O	B	U	S											
	19	C	D	0	2	1	2	E	L	S	A	R	M															
	20	C	D	0	2	1	4	E	L	S	S	A	F	E														
	21	C	D	0	2	0	7	M	A	I	N	B	U	S														
	22	C	D	0	2	0	9	T	W	R	P	Y	R	O	B	U	S											
	23	C	D	0	2	1	6	L	E	S	L	O	G	I	C	B	U	S										
	24	C	D	0	2	1	8	A	D	A	P	T	E	R	P	Y	R	O										
	25																											
	26		1	2	3	4	5	7	8	9	0	L	E	S	P	G	0	4	1	2	3	4	5	6	7	9	0	

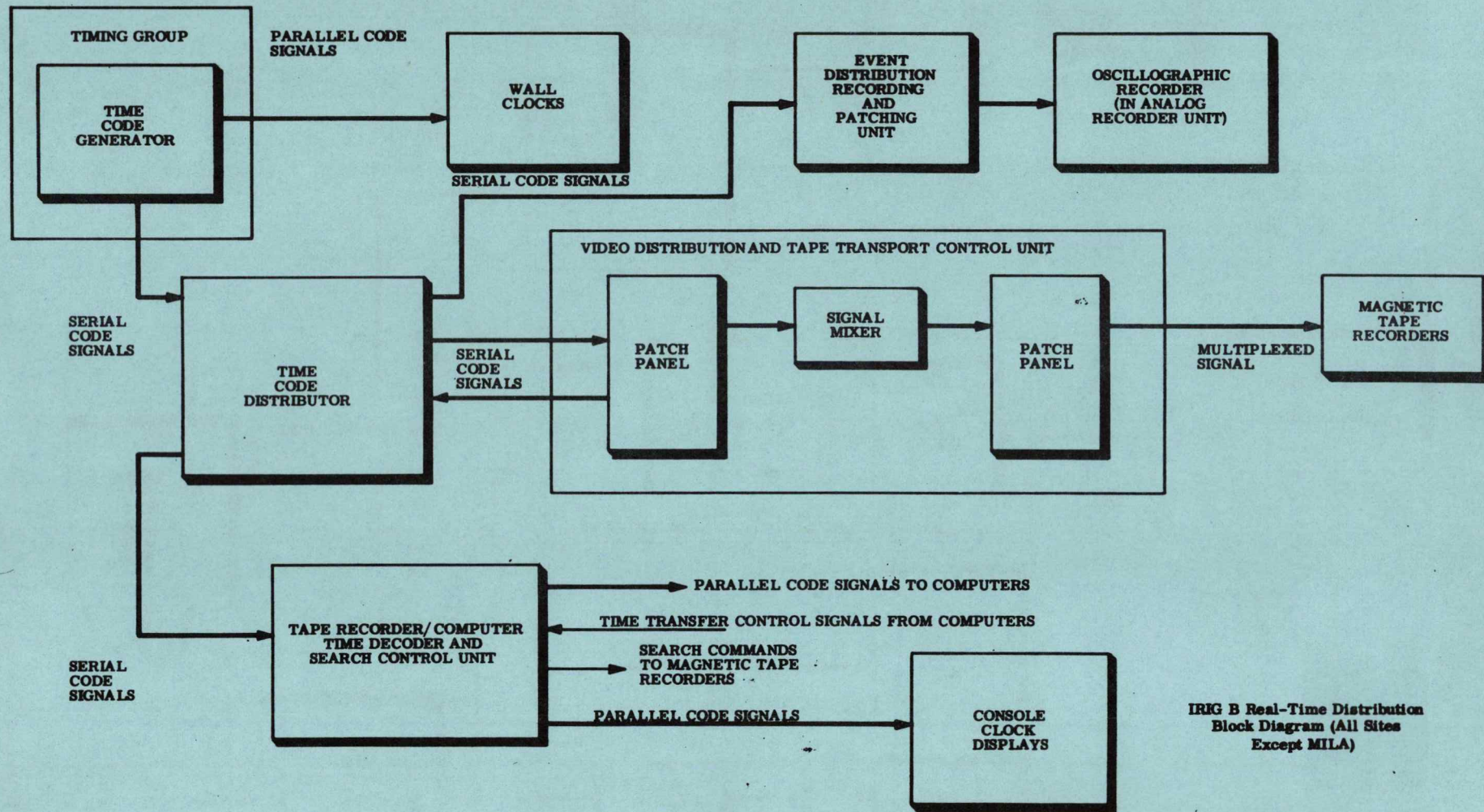
FOR TRAINING PURPOSES ONLY



FOR TRAINING PURPOSES ONLY

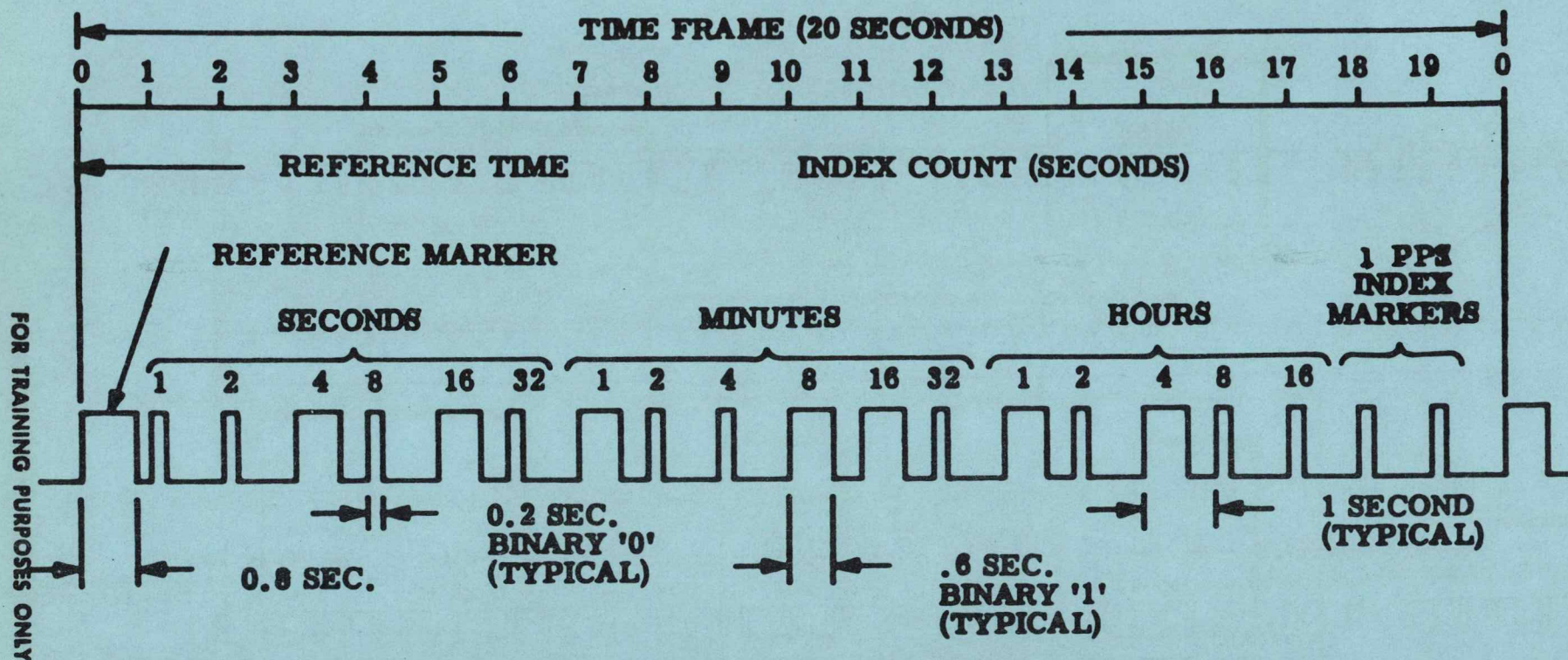
Real Countdown-Time Distribution Block Diagram (All Sites Except MILA)

FOR TRAINING PURPOSES ONLY



IIRIG B Real-Time Distribution
Block Diagram (All Sites
Except MILA)

FOR TRAINING PURPOSES ONLY



THE AMR B-1 TIME CODE IS A 17-DIGIT WIDTH MODULATED CODE. THE CODE IS COMPOSED OF A REFERENCE MARKER, THREE SUB-CODE WORDS OF SECONDS, MINUTES AND HOURS AND INDEX MARKERS. EACH SUB-CODE WORD IS WEIGHTED IN BINARY FASHION.

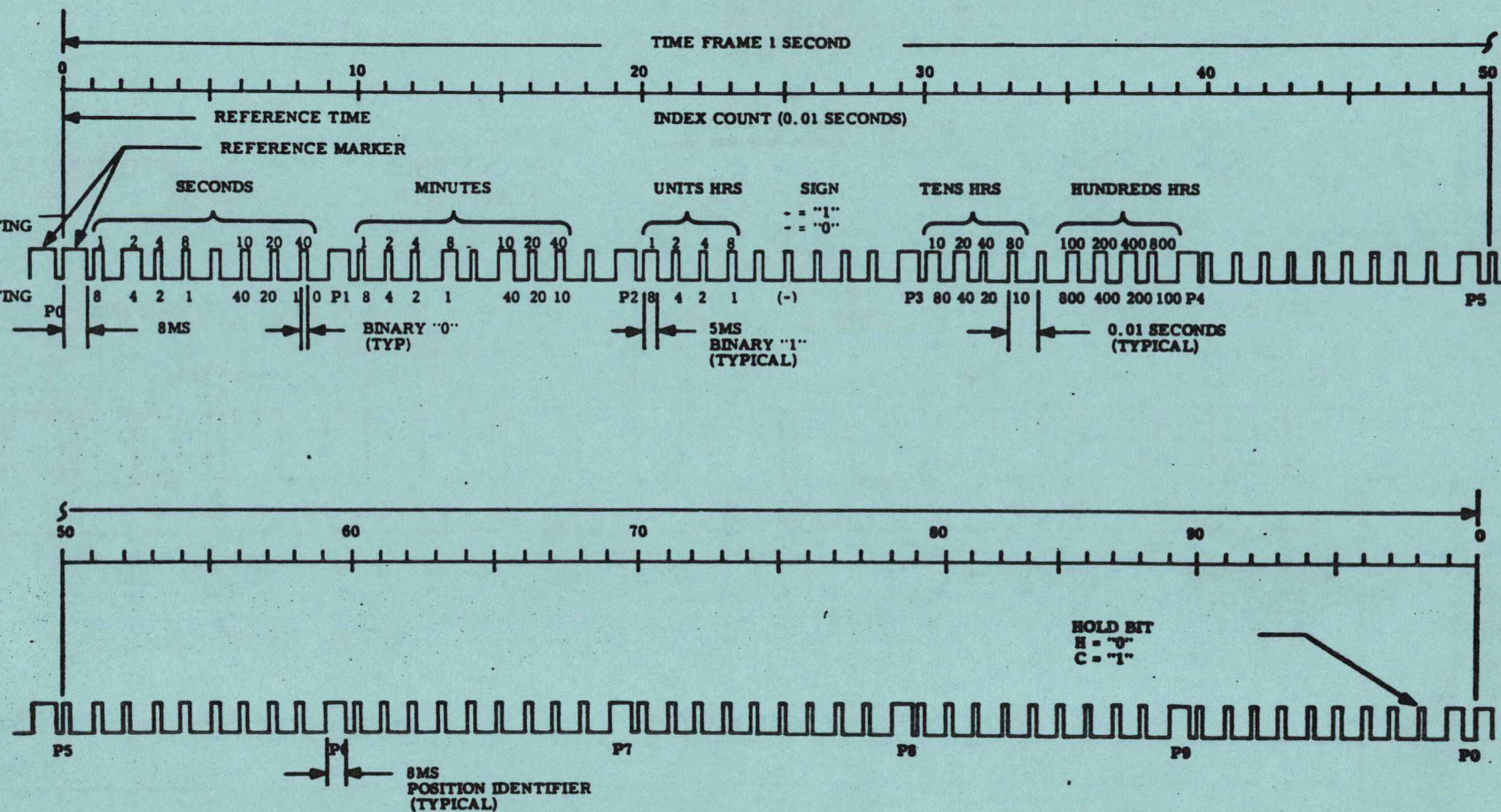
THE LEADING EDGES OF ALL PULSES ARE PRECISELY SPACED AT 1-SECOND INTERVALS.

THE CODE TIME FRAME IS 20 SECONDS. THE SUM OF THE CODED TIME REFERS TO THE LEADING EDGE OF THE CODE WORD REFERENCE MARKER.

THE CODE MAY BE USED TO AMPLITUDE MODULATE A SINE WAVE CARRIER. FREQUENCY SHOULD BE SPECIFIED. 1000 CPS OR 100 CPS IS RECOMMENDED. THE CODE FORMAT IS THEN REFERRED TO AS AMR B-2.

AMR B-1 Time Code Format

FOR TRAINING PURPOSES ONLY

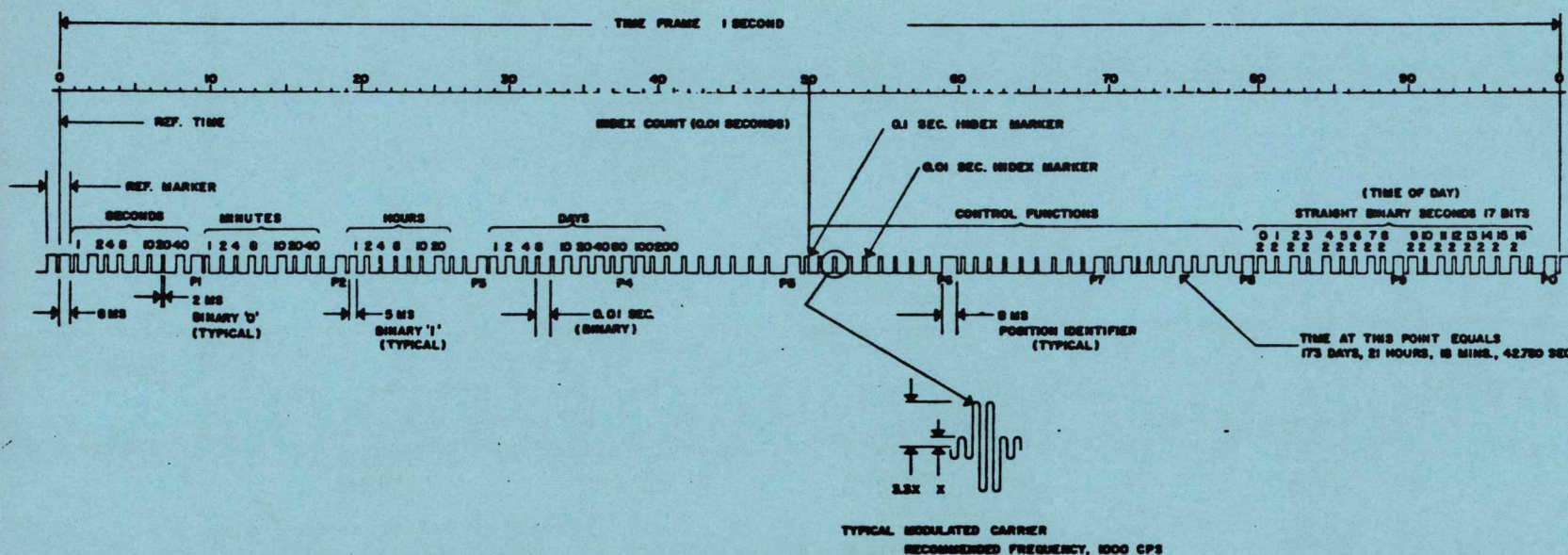


ACE-S/C Countdown-Time Code Format

FOR TRAINING PURPOSES ONLY

IRIG B TIME STANDARD CODE

FOR TRAINING PURPOSES ONLY



FOR TRAINING PURPOSES ONLY

