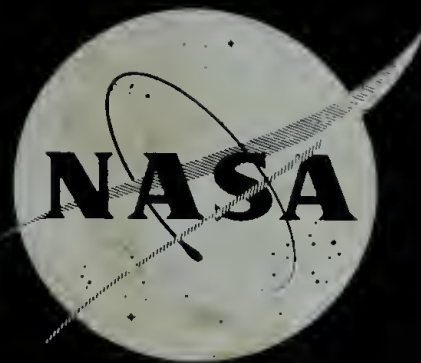


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VOLUME I



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MILWAUKEE, WISCONSIN



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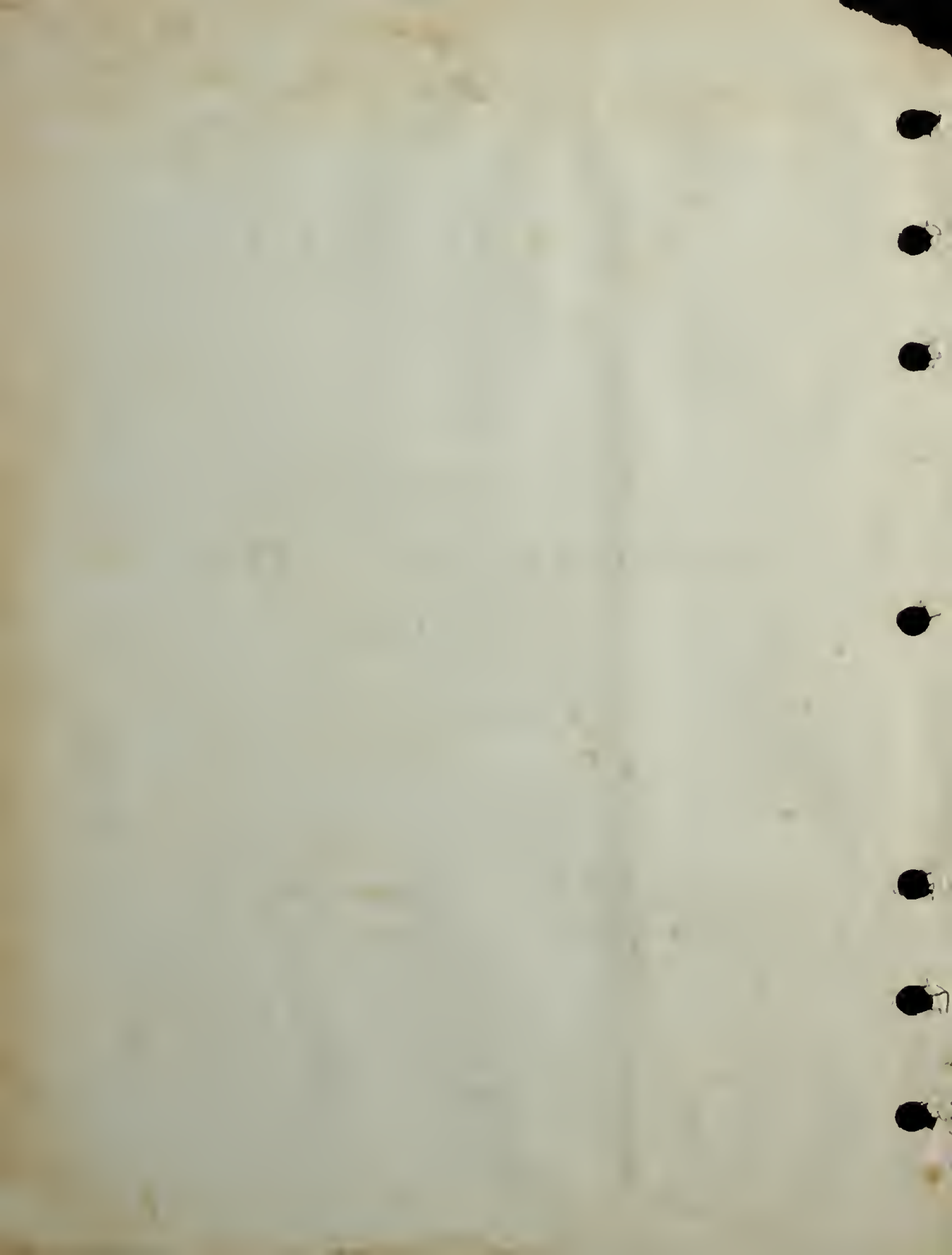
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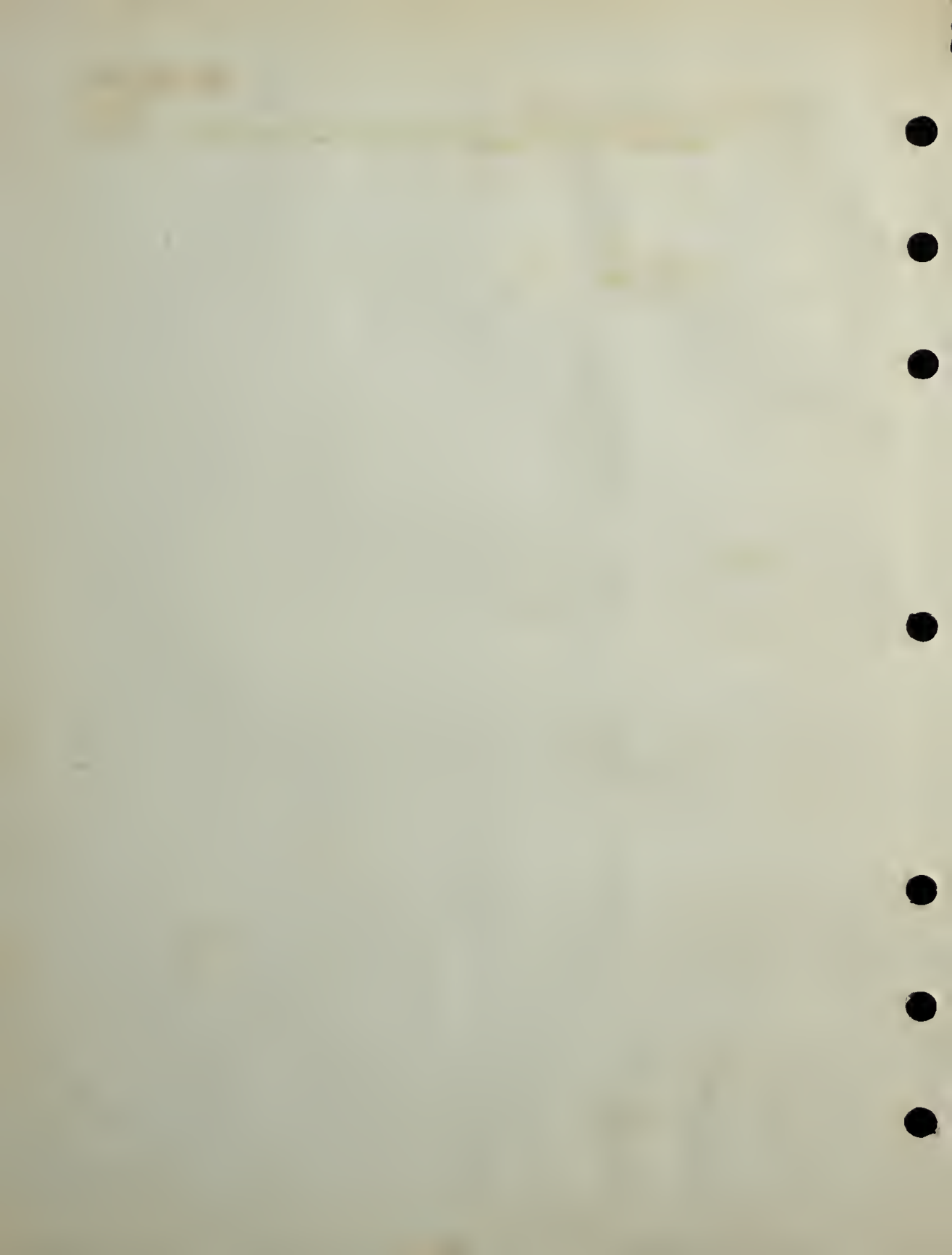
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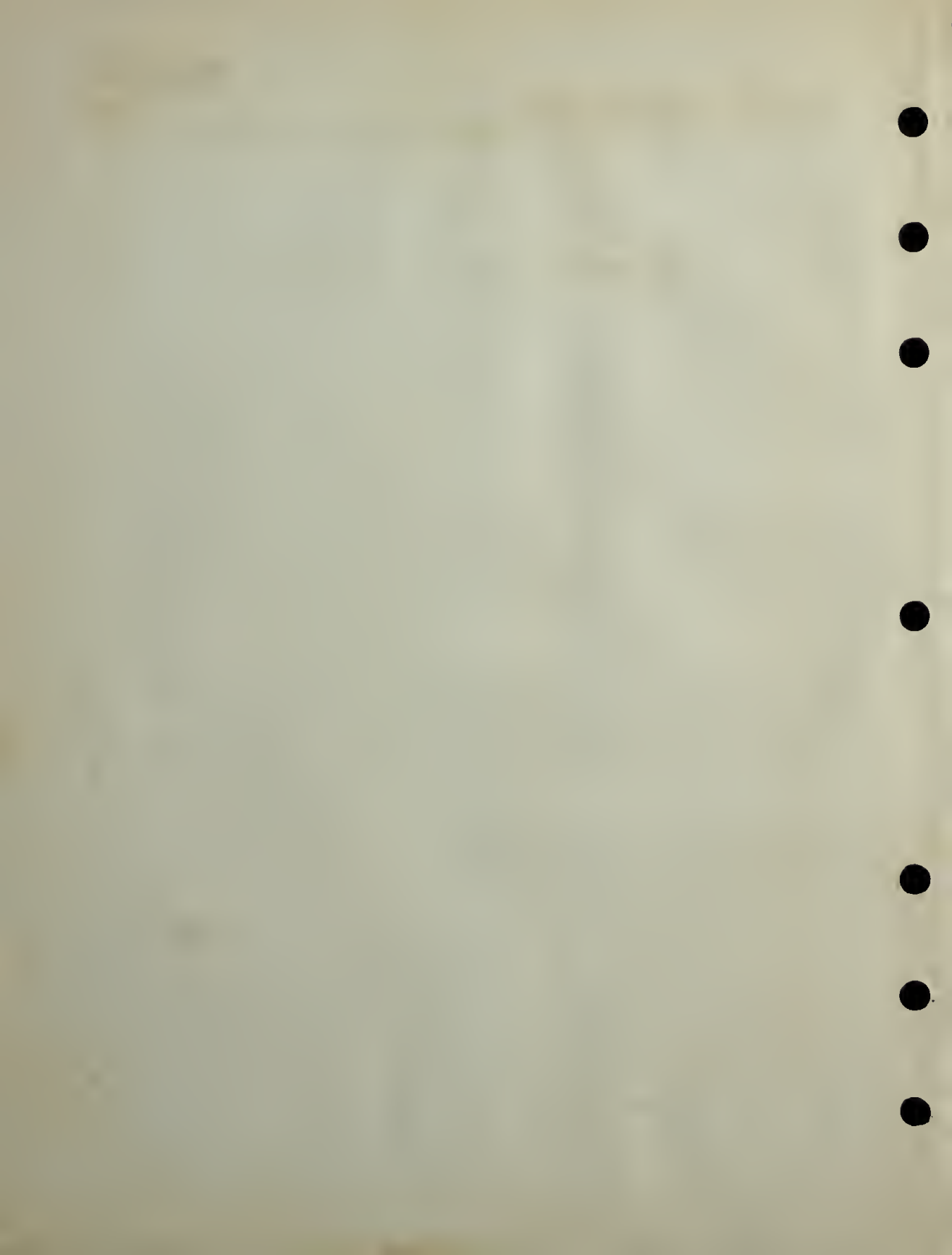
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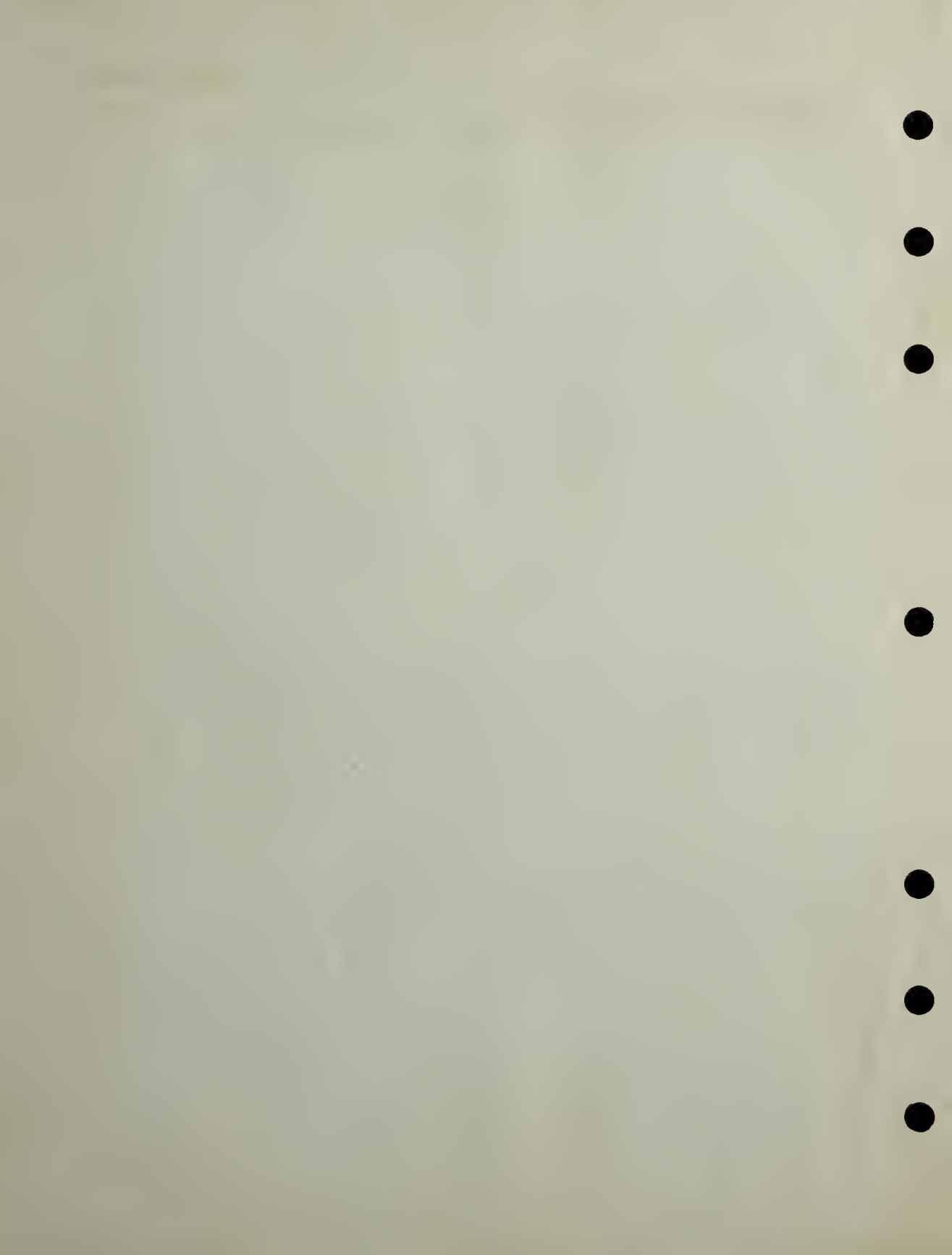
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LIST OF RELATED MANUALS

ND-1021038	Packing, Shipping and Handling Manual
ND-1021039	Auxiliary Ground Support Equipment Manual
ND-1021040	Bench Maintenance Ground Support Equipment Manual





## INTRODUCTION

This manual is intended to be used with its Job Description Cards (JDC's) for the checkout, maintenance, and repair of the Apollo Guidance and Navigation System (G and N system), figure 1-1, in the guidance and navigation laboratories and stock rooms located at North American Aviation (NAA) and Merritt Island Launch Area (MILA) for the Block I Series 100 program. The manual is also intended for use as a familiarization manual and introduction to the G and N system.

This manual provides a functional analysis, detailed theory of operation, component description, system tie-in, and a description of flight operations. The manual lists support equipment required for the JDC procedures and provides tabular and diagram references to the JDC's to insure that the preparation for checkout, checkout analysis, and repair and replacement procedures are performed in sequence and conform to all program requirements.

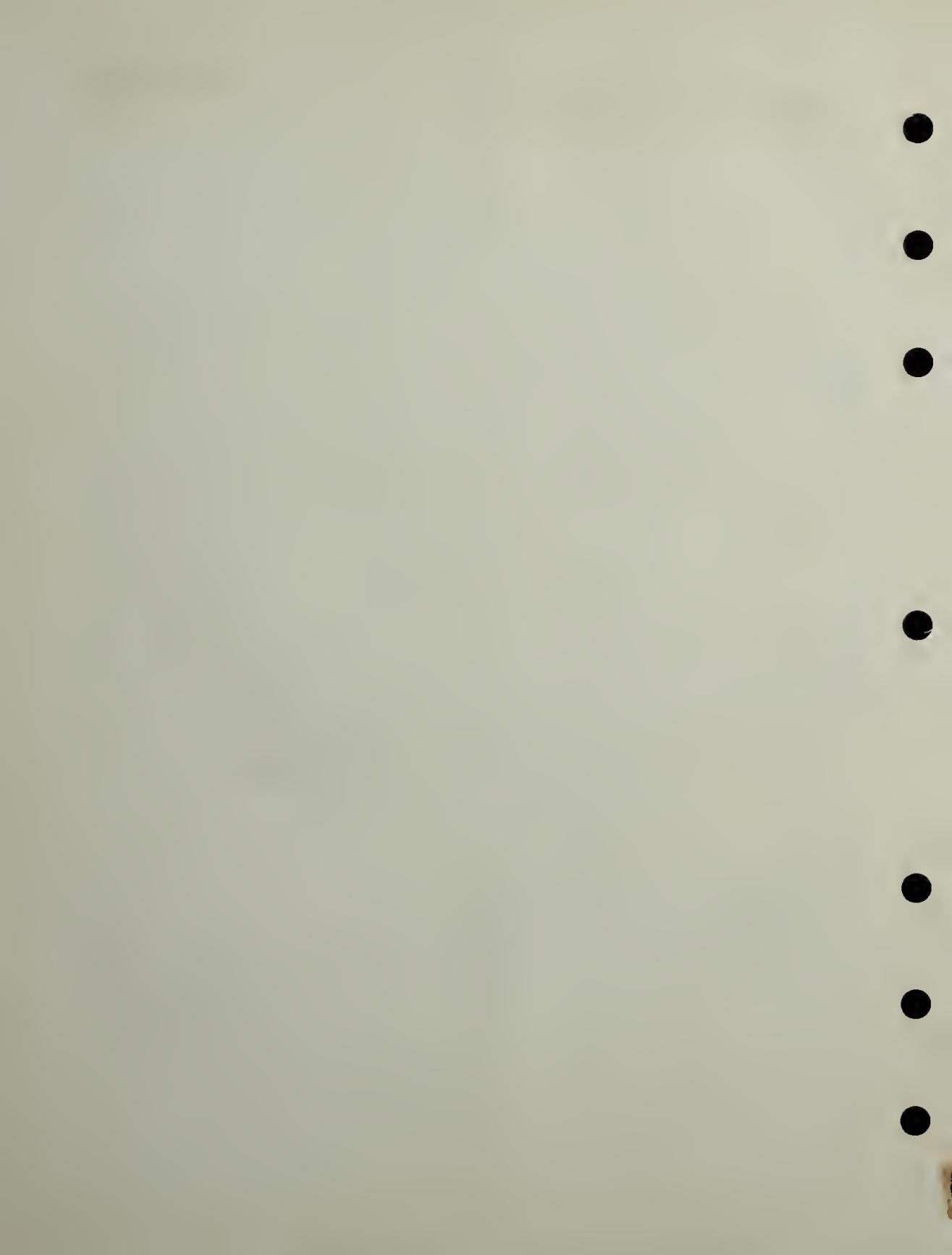
Information available as of 1 July 1965 was used in the preparation of this manual and covers Apollo G and N system, part number 1015000-101.

The manual is prepared in accordance with E-1087 Documentation Handbook in compliance with National Aeronautics and Space Administration (NASA) contract NAS 9-497, exhibit D.

Appendix A contains a listing of technical terms and abbreviations used in the manual, appendix B explains the functions and relationship of the System Identification Data List (SIDL) and the Aperture card system to the manual, and appendix C contains the logic symbols used in the discussion of the computer logic diagrams. All JDC's referenced in this manual are contained in the Apollo Guidance and Navigation System Job Description Card binders and are also available through the aperture card system.

Use the Technical Data Change Request (TDCR) form to request changes to this manual. Send the original TDCR to:

Apollo Field Service Publications, Department 38-01  
AC Electronics  
Division of General Motors  
P.O. Box 371  
Milwaukee, Wisconsin 53201



## Chapter 1

## SYSTEM TIE-IN

## 1-1 SCOPE

This chapter presents the concepts of the Apollo mission. The chapter also describes the functional interface between the guidance and navigation system (G and N system) and the other spacecraft systems.

## 1-2 APOLLO MISSION AND PROGRAM

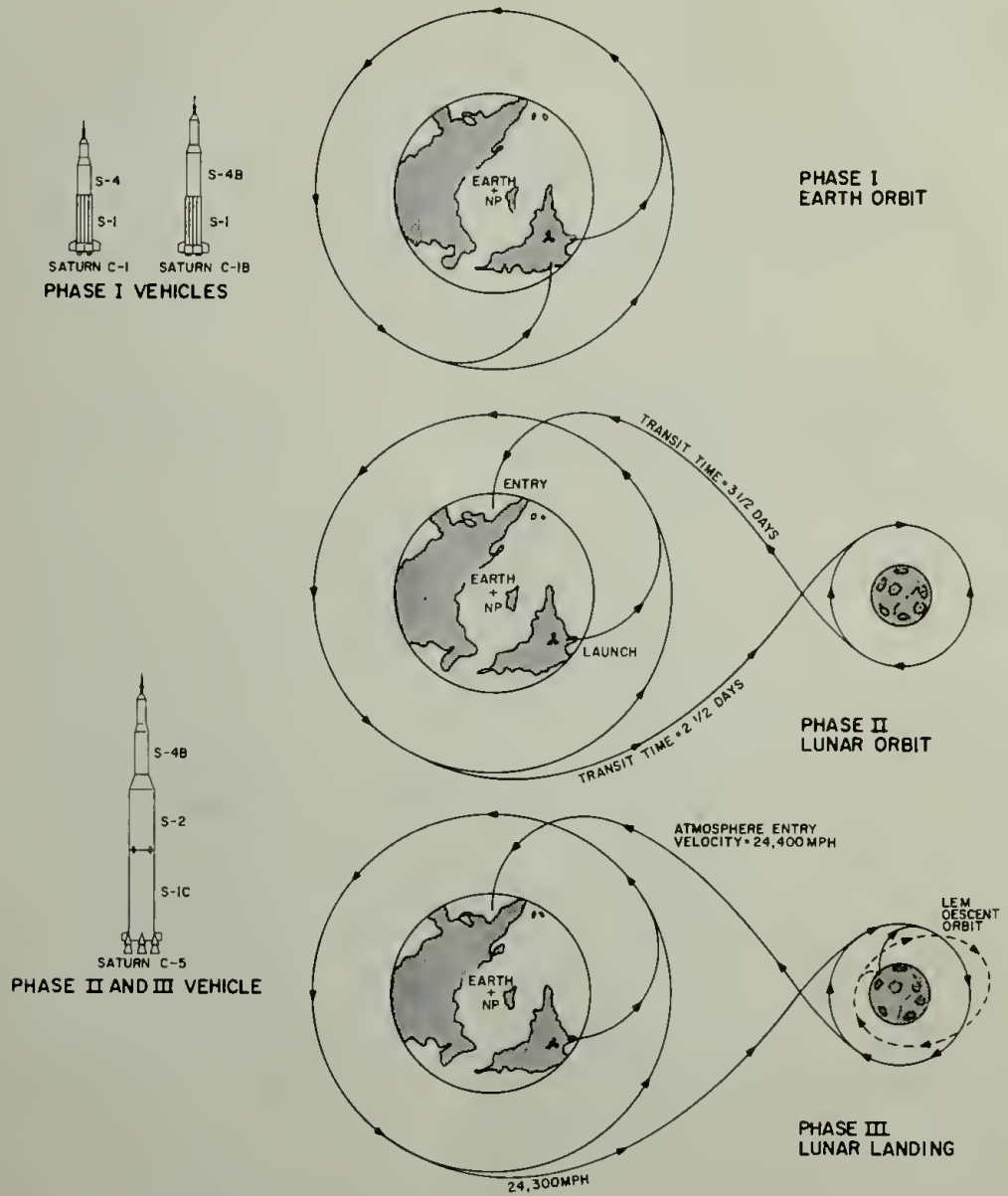
The purpose of the Apollo program is to land astronauts on the moon and return them safely to earth. Before a lunar landing is attempted, the spacecraft hardware must be proven, the astronauts must be trained, and a capability for extended space flight must be demonstrated. To obtain these objectives the Apollo program has been divided into three phases (figure 1-2).

1-2.1 EARTH ORBITAL FLIGHTS. Phase I of the Apollo program will consist of earth orbital flights. The first flights will be unmanned and will test the performance and interface of the spacecraft systems during flight. Later earth orbital flights will be manned, and the astronauts will practice techniques of navigation, rendezvous, and entry.

Rendezvous will be practiced in earth orbit using the Apollo spacecraft (figure 1-3) and the lunar excursion module (LEM), a two man vehicle which will land on the moon in the phase III mission. The astronauts will practice LEM separation and docking techniques which will be used in the lunar landing mission.

Entry, a critical part of earth orbital flights, will be even more critical at the higher entry speeds reached in phase II and III flights. To approach these speeds for practice during phase I entry, the spacecraft will be accelerated from earth orbit into a parabolic entry trajectory. Earth landing for all Apollo flights will be by parachute descent of the command module (figure 1-3).

Two launch vehicles will be used during phase I. The two stage Saturn C-1 will be capable of placing the spacecraft and a three man crew into earth orbit. The larger two stage Saturn C-1B will be required to orbit the spacecraft and LEM simultaneously. Physical characteristics of the Apollo vehicles are given in table 1-1.



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Figure 1-2. Three Phases of Apollo

APOLLO GUIDANCE AND NAVIGATION SYSTEM

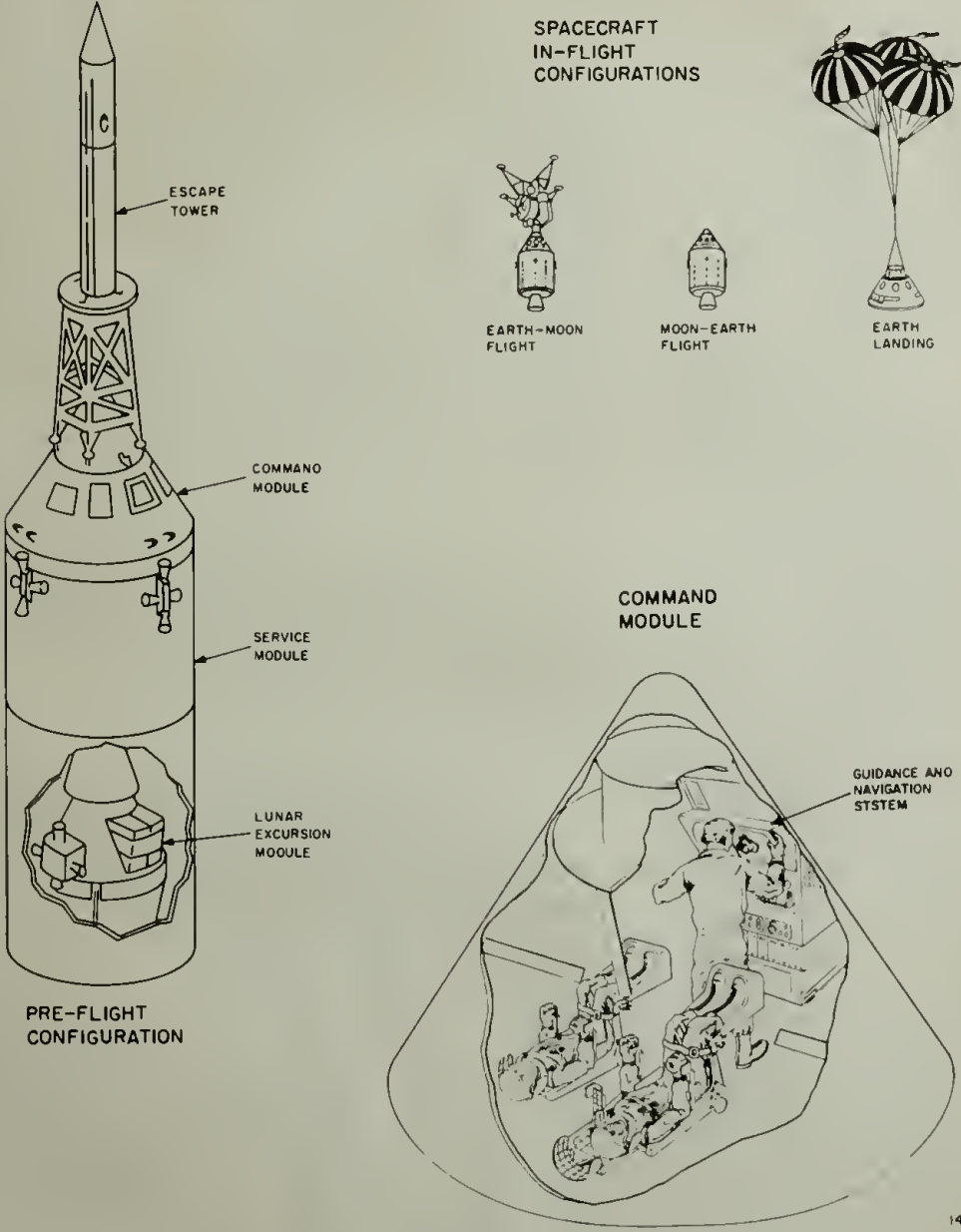


Figure 1-3. Apollo Spacecraft

Table 1-I. Spacecraft and Launch Vehicle Physical Characteristics

Vehicle	Stage	Nominal Thrust (pounds)	Propellants and Oxidizers	Height (feet)	Diameter (feet)
Spacecraft	Command module	N/A	Aerozine 50 Nitrogen te- troxide	12	13
	Service module	21,900	Aerozine 50 Nitrogen te- troxide	23	12.8
	LEM	10,000 on landing 4,000 on takeoff	Aerozine 50 Nitrogen te- troxide	17	10
Saturn C-1	First (S-1)	1,500,000	Kerosene Liquid oxygen	81.6	21.6
	Second (S-4)	90,000	Liquid hydrogen Liquid oxygen	40	18
Saturn C-1B	First (S-1)	1,500,000	Kerosene Liquid oxygen	81.8	21.6
	Second (S-4B)	200,000	Liquid hydrogen Liquid oxygen	60	22
Saturn C-5	First (S-1C)	7,500,000	Kerosene Liquid oxygen	138	33
	Second (S-2)	1,000,000	Liquid hydrogen Liquid oxygen	82	33
	Third (S-4B)	200,000	Liquid hydrogen Liquid oxygen	60	22

APOLLO GUIDANCE AND NAVIGATION SYSTEM

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1-2.2 LUNAR ORBITAL MISSION. The phase II objective will be manned flight around the moon and return to earth. This flight will require about six and one half days and will employ techniques of navigation and entry practiced during the phase I flights. The astronauts will make scientific observations during the lunar voyage, and will view the lunar landscape from a relatively close position. These observations will be combined with astronomical and lunar probe findings to determine a suitable landing site for the phase III mission.

The launch vehicle for phase II will be a 335 foot-high Saturn C-5. This three stage vehicle also will be used to launch the phase III mission.

1-2.3 LUNAR LANDING MISSION. The phase III mission will have the following primary objectives:

- (1) Land two astronauts and scientific equipment on the moon and return the astronauts safely to earth.
- (2) Perform scientific experiments on the moon and, within the restrictions of limited spacecraft payload, return lunar samples to earth.

This flight will take about eight days. Landing on the moon will be accomplished by separating the LEM from the spacecraft and deorbiting the LEM to a predetermined lunar landing site. Two astronauts will descend in the LEM and one astronaut will remain in the spacecraft, which will continue to orbit the moon. Rendezvous techniques perfected in phase I will be applied when the LEM returns to lunar orbit and the two astronauts transfer to the spacecraft. The spacecraft then will be injected into a trans-earth trajectory.

### 1-3 APOLLO SPACECRAFT

The spacecraft (figure 1-3) consists of a command module and a service module. The LEM is attached to the rear of the service module, and a launch escape system is mounted on the command module. Solid fuel motors in the launch escape system inject the command module into an escape trajectory if an abort occurs during launching. The launch escape system is jettisoned shortly after a satisfactory launching and only the spacecraft and the LEM are inserted into earth orbit. After the spacecraft is injected from earth orbit into a lunar trajectory, the LEM, a spacecraft itself, is separated from the service module and docked on the command module. The LEM is carried to lunar orbit where it is detached for lunar landing.

1-3.1 COMMAND MODULE. The command module contains crew accommodations, all controls and displays which the astronauts use to control the spacecraft, and systems for spaceflight and earth entry. The G and N system is located in the command module lower equipment bay and is designed to calculate the position of the spacecraft, and to control spacecraft attitude and velocity changes. The G and N system performs these functions by:

- (1) Periodically establishing an inertial reference for measurements and computations.

- (2) Providing a means of aligning the inertial reference by precise optical measurements.
- (3) Providing a means of calculating the position and velocity of the spacecraft by optical or inertial techniques.
- (4) Generating attitude control and thrust commands to maintain the spacecraft on a satisfactory trajectory.
- (5) Displaying pertinent data about the status of guidance problems.

1-3.2 SERVICE MODULE. The service module houses a propulsion system, reaction control system, radar, fuel cells, and other gear and supplies that do not need to be pressurized. Until separation occurs just prior to entry, the service module provides the spacecraft with thrust, attitude control, and electrical power.

#### 1-4 SPACECRAFT SYSTEMS

There are essentially seven spacecraft systems. The functional interface between the G and N system and the other systems is shown in figure 1-4. Descriptions and sources of the interface signals are provided in table 1-II. Four spacecraft systems have direct interface with the G and N system and two systems have indirect interface with G and N system.

1-4.1 GUIDANCE AND NAVIGATION SYSTEM. The G and N system performs two basic functions: inertial guidance and optical navigation. The astronaut plays an active part in both functions.

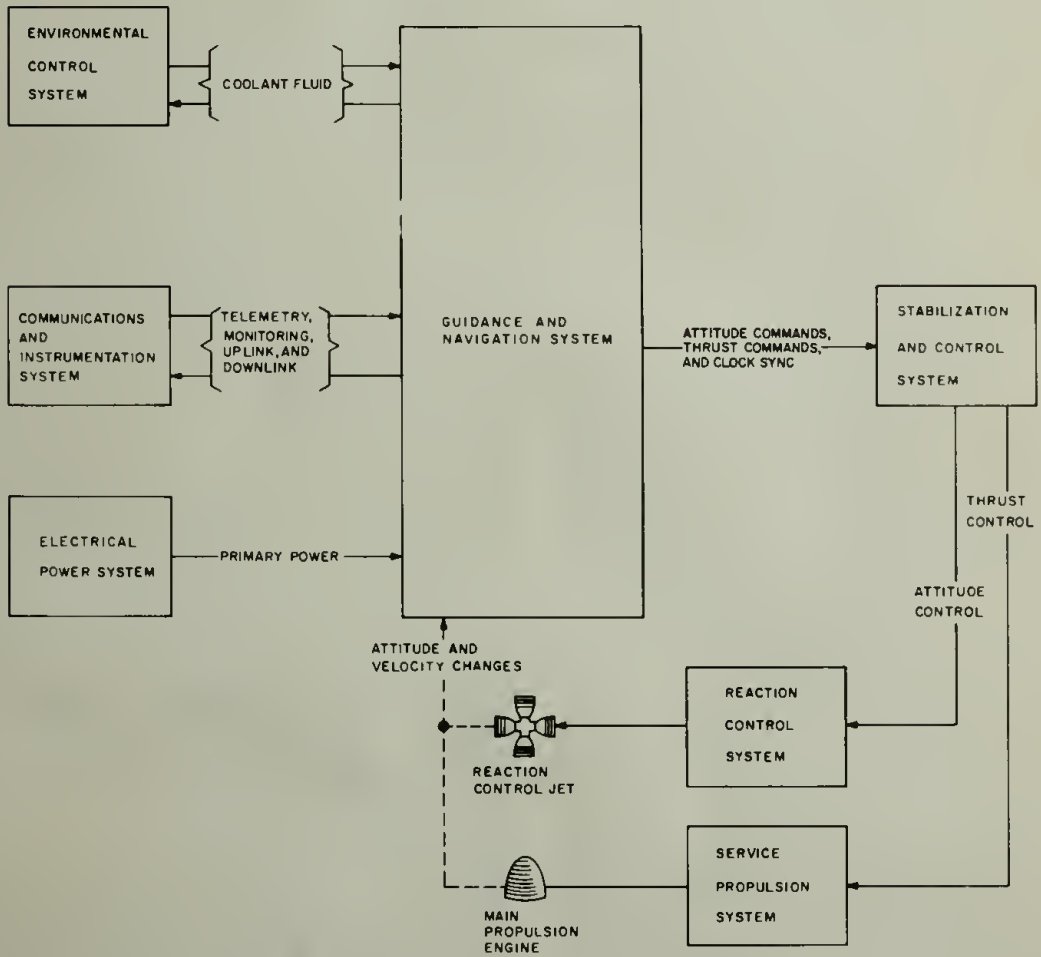
For inertial guidance the G and N system employs an inertial measuring unit (IMU) using accelerometers mounted on a gyroscopically stabilized, gimbal mounted platform. The G and N system senses velocity and attitude changes and provides steering and thrust control signals to the stabilization and control system (SCS).

For optical navigation a scanning telescope and sextant are used to take sightings on celestial bodies and landmarks. A star tracker and a horizon photometer convert light into electrical signals to lock the sextant on a star and to provide a signal to a digital computer indicating landmark position. The sightings are used to determine spacecraft position and velocity, and to establish proper alignment of the stable platform. Communications with ground tracking stations also provide information for spacecraft navigation.

A digital computer (Apollo guidance computer) in the G and N system serves as the primary spacecraft data processing element. The Apollo guidance computer (AGC), which contains a catalog of celestial objects, is programmed to calculate thrust and steering commands using information obtained from optical sightings. Data on gravitational fields and celestial movements are used in the AGC to calculate future position and velocity of the spacecraft.



APOLLO GUIDANCE AND NAVIGATION SYSTEM



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Figure 1-4. G and N System Functional Interface, Block Diagram

Table 1-II. Description of Interface Signals

Signal Name	Source	Description
Stabilization and Control System (SCS) and G and N System Interface		
Engine on-off	AGC (Apollo guidance computer)	Provides pulse train that lasts as long as the engine is required to fire. The time at which the signal terminates takes into account electronic delays within the SCS and tail-off characteristics of the engines.
Discrete signal carrier	AGC	Provides continuous pulse train to the SCS to be switched back to the AGC.
G and N system attitude control (or SCS attitude control)	SCS	Provides power to an attitude control switch on the G and N system.
Minimum impulse enable	G and N system	Disables all three attitude channels simultaneously and supplies voltages to an attitude control switch on the G and N system.
Minimum impulse + and - pitch, yaw, and roll	SCS	Provides six signals to the G and N system for hand controller operation.
Minimum impulse pitch, yaw, and roll	G and N system	Provides the capability to initiate spacecraft attitude changes in the G and N system attitude control mode or the SCS attitude control mode. These changes will be initiated by discrete minimum impulses.
Pitch error body offset and body axis	G and N system	Provides pitch attitude error signal to the SCS.
Yaw error body offset axis	G and N system	Provides yaw attitude error signal to the SCS during G and N system entry mode.
Yaw error body axis	G and N system	Provides yaw attitude error signal to the SCS during normal G and N system operating modes.
Roll error body offset axis	G and N system	Provides roll attitude error signal to the SCS during G and N system entry mode.

(Sheet 1 of 3)

Table 1-II. Description of Interface Signals (cont)

Signal Name	Source	Description
Roll error body axis	G and N system	Provide roll attitude error signal to the SCS during normal G and N system operating modes.
IMU 28V 800 cps (demodulator reference)	G and N system	Provides an 800 cps, synchronous, in-phase voltage from the G and N system.
IMU sin AIG 1X, IMU cos AIG 1X, IMU sin AMG 1X, IMU cos AMG 1X, IMU sin AOG 1X, and IMU cos AOG 1X	G and N system	Provide total attitude signals to the SCS.
Electrical Power System (EPS) and G and N System Interface		
+28 vdc AGC bus A and bus B	EPS	Provide power to the AGC.
+28 vdc optics bus A and bus B	EPS	Provide power to the optics subsystem.
+28 vdc IMU bus A and bus B	EPS	Provide power to the IMU.
+28 vdc standby bus A and bus B	EPS	Provide IMU temperature control power.
115V 400 cps	EPS	Provides power for all G and N system 6 volt lamps.
Communication and Instrumentation System and G and N System Interface		
DLNK sync	AGC	Synchronizes data transferred from the AGC to the communications and instrumentation system.

(Sheet 2 of 3)

Table 1-II. Description of Interface Signals (cont)

Signal Name	Source	Description
DLNK end	AGC	Permits two AGC words to be transferred from the AGC to the communications and instrumentation system. Stops the AGC and the transmission of data from the AGC to the communications and instrumentation system.
DLNK start	AGC	Provides pulse signal that occurs at the beginning of every data transmission to the communications and instrumentation system. Sets flip-flop in AGC that enables 5 stage downlink counter.
DLNK data	AGC	Initiated by DLNK start, stopped by DLNK end, and consists of a 40 bit telemetry word (two AGC words and an 8 bit telemetry word order code).
ULNK 1	AGC	Transmitted to the uplink counter in the AGC. Adds one to uplink counter and shifts the counter one increment.
ULNK 0	AGC	Transmitted to the uplink counter in the AGC. Shifts uplink counter one increment.

(Sheet 3 of 3)

1-4.2 STABILIZATION AND CONTROL SYSTEM. The SCS, which is located in the command module, can sense and control spacecraft attitude and velocity changes during flight. The SCS is a medium by which astronaut inputs, service propulsion system, reaction control systems, G and N system, and spacecraft are made compatible. The SCS provides the following spacecraft capabilities:

- (1) Rate stabilization of command module during an abort after spacecraft separation from the booster and stabilization of the command module after escape tower jettison and during entry.
- (2) Attitude and stabilization control about three axes in response to either manual or automatic rotation commands.
- (3) Translational control along three axes in response to manual commands for ullage maneuvers, transposition, and docking.

## APOLLO GUIDANCE AND NAVIGATION SYSTEM

- (4) Translational control along three axes in response to manual commands as a backup mode to the LEM-controlled rendezvous and docking operation.
- (5) Translational control along three axes in response to manual commands for small changes in velocity.
- (6) Thrust vector control for the service propulsion system.
- (7) Manual service propulsion system engine thrust on-off functions.
- (8) Displays for visual indication of control parameters.

The SCS consists of a rate gyro package, attitude gyro and accelerometer package, attitude gyro coupler unit, electronic control assemblies, and various displays and controls. The SCS can hold the spacecraft to a local vertical attitude during earth or lunar orbit by using orbital rates, or to a specific attitude by using reference gyros mounted on the spacecraft body. Information about spacecraft attitude and rate of attitude change is displayed to the astronaut. Steering and thrust signals from the G and N system are processed and conditioned by the SCS and used to operate the reaction control and service propulsion systems.

1-4.3 SERVICE PROPULSION SYSTEM. The service propulsion system (SPS) provides thrust to control spacecraft velocity. The SPS normally is operated by the G and N system through the SCS, but can be operated manually through the SCS in emergencies.

The SPS is utilized for mission abort, midcourse velocity corrections, and orbital injections. The SPS is located in the rear of the service module and consists of helium, fuel, and oxidizer tanks; gimbaled thrust chamber; propellant control valves; and propellant distribution system.

1-4.4 REACTION CONTROL SYSTEMS. Two reaction control systems (RCS) are used for attitude control and stabilization of the spacecraft. One RCS is required for the service module and the other for the command module. Both systems can be operated by the G and N system through the SCS or directly by the SCS. Each RCS consists of helium, fuel, and oxidizer tanks; propellant control valves; fixed thrust chambers; and distribution subsystem.

Spacecraft attitude, rate of rotation, and small translational velocity changes are normally controlled by an automatic RCS loop, but also may be controlled by a direct RCS loop. Each RCS fuel valve and oxidizer valve contains one solenoid winding controlled by the automatic RCS loop, and a second solenoid winding controlled by the direct RCS loop.

The automatic RCS loop is activated by signals from the G and N system or by signals from hand controllers. The RCS jets fire to rotate the spacecraft and, when the rotational command is removed, jets are automatically fired in the opposite direction to stop the spacecraft rotation.

The direct RCS loop bypasses the automatic circuits to provide direct astronaut control of the RCS jets. After the hand controller is released, the spacecraft continues to rotate until the astronaut commands an opposite rotation.

1-4.4.1 Service Module Reaction Control System. The service module RCS provides thrust to control spacecraft attitude during all phases of flight except launch and entry. The service module RCS consists of four hypergolic-propellant-pressurized reaction jet subsystems. The subsystems are mounted in the forward section of the service module and are located 90 degrees apart. Eight of the 16 nozzles are used for roll control, four for pitch, and four for yaw. Each nozzle produces a nominal thrust of 100 pounds in space.

1-4.4.2 Command Module Reaction Control System. The command module RCS is used only during entry after separation of the command and service modules. The RCS of the command module consists of two independent subsystems, each utilizing 6 nozzles. The two subsystems operate simultaneously and provide three axis control of the command module. In the event one subsystem fails, the remaining reaction jet subsystem is capable of providing the control necessary for safe entry.

1-4.5 ELECTRICAL POWER SYSTEM. The primary power required to operate the G and N system is supplied by a hydrox fuel cell in the service module and is used during all mission phases except entry and recovery. Three zinc-silver oxide storage batteries in the command module furnish power for entry and recovery.

The hydrox fuel cell contains three independent modules operating in parallel and capable of producing a 27 to 31 volt dc output. In an emergency any two fuel cell modules could meet all power requirements. Three solid state inverters change the fuel cell output into 115 volt, 400 cycle power. The fuel cell dc output and the inverter ac output both are used to provide power for normal G and N system operation.

Each fuel cell module contains 31 fuel cell units. The fuel cells utilize hydrogen and oxygen as reactants and potassium hydroxide as an electrolyte. The reactants are stored in tanks furnished as a part of the environmental control system. The water formed by operating the fuel cells is collected and delivered to the environmental control system, for potable water.

1-4.6 ENVIRONMENTAL CONTROL SYSTEM. An environmental control system (ECS) is used to sustain life in space by providing breathable atmosphere, acceptable temperatures, humidity and pressure control, water, and waste disposal. In addition, a water-glycol coolant fluid is circulated about temperature sensitive components of the G and N system to aid in maintaining constant operating temperatures. The fluid temperature at the input to the G and N system is 45 degrees Fahrenheit and is circulated at a rate of 33 pounds per hour. The ECS includes oxygen tanks and space radiators in the service module, and a distribution system, connections for spacesuit oxygen lines, sensors, regulators, cabin blowers, and heat exchangers in the command module.

APOLLO GUIDANCE AND NAVIGATION SYSTEM

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1-4.7 COMMUNICATIONS AND INSTRUMENTATION SYSTEM. The Apollo communications and instrumentation system provides voice, television, and telemetry communication with the earth; voice communication among crew members; tracking radar; and communication between the spacecraft and LEM. A closed loop television system permits viewing external sections of the spacecraft during flight.

Data can be transmitted to earth or received from earth by Apollo telemetry. Telemetry data can be stored when direct communication with the earth is not possible because of the location of earth stations or because the spacecraft is behind the moon. Earth stations can determine spacecraft position and transmit this information through telemetry to the G and N system AGC to supplement information obtained from the G and N system. Critical signals of the G and N system, and other spacecraft systems, are conditioned and supplied to pulse code modulated (PCM) equipment for transmission to ground stations.

After earth landing, a recovery beacon in the command module transmits a VHF signal to direct aircraft and ships to the landing area.





## Chapter 2

## SYSTEM AND SUBSYSTEM FUNCTIONAL ANALYSIS

## 2-1 SCOPE

This chapter provides functional descriptions of the guidance and navigation (G and N) system and the three subsystems which comprise the G and N system. The chapter describes how the three subsystems perform G and N system operations.

## 2-2 GUIDANCE AND NAVIGATION SYSTEM

The G and N system performs two basic functions: inertial guidance and optical navigation.

For inertial guidance, the G and N system employs an inertial measuring unit (IMU) containing accelerometers mounted on a stabilized, gimbal mounted platform. The IMU, IMU control panel, three coupling display units (CDU's), display and control (D and C) electronics, portions of the power and servo assembly (PSA), and portions of the control electronics form the inertial subsystem (ISS) of the G and N system.

For optical navigation, the G and N system employs an optical unit assembly (OUA) consisting of a scanning telescope (SCT), sextant (SXT), horizon sensor, and star tracker. The OUA, navigation base (nav base), two CDU's, and portions of the PSA, portions of control electronics, portions of the D and C electronics, tracker X and Y assembly, and G and N indicator control panel form the optical subsystem (OSS) of the G and N system.

The Apollo guidance computer (AGC) is a digital computer which serves as the primary data processing element of the G and N system. The AGC, main panel display and keyboard (DSKY), and the navigation panel DSKY form the computer subsystem (CSS) of the G and N system.

Figure 2-1 illustrates the signal flow and interface between the three G and N subsystems.

## 2-3 AXES

Apollo spacecraft and G and N axes are illustrated in figure 2-2. The axes in each set illustrated and discussed are orthogonal.

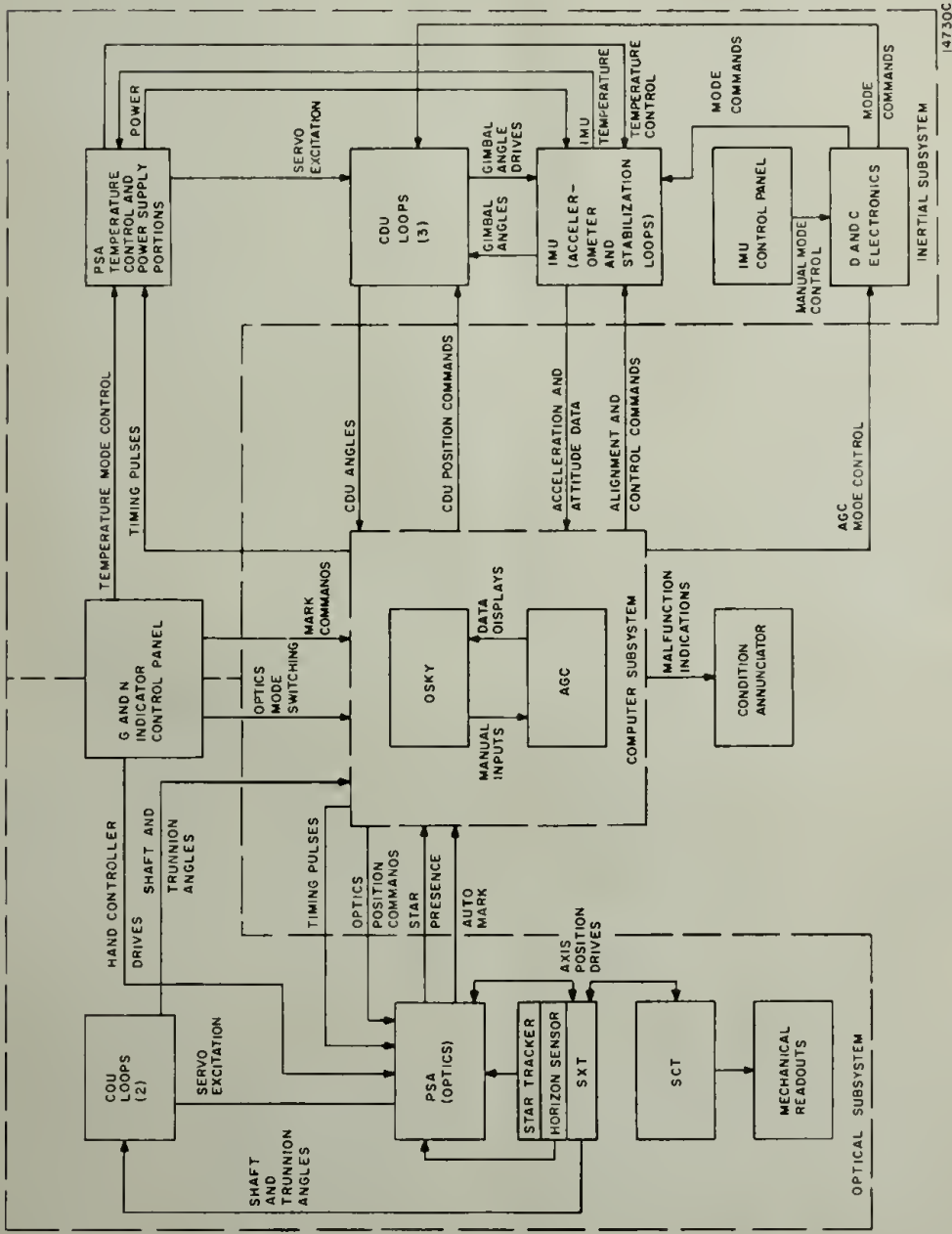
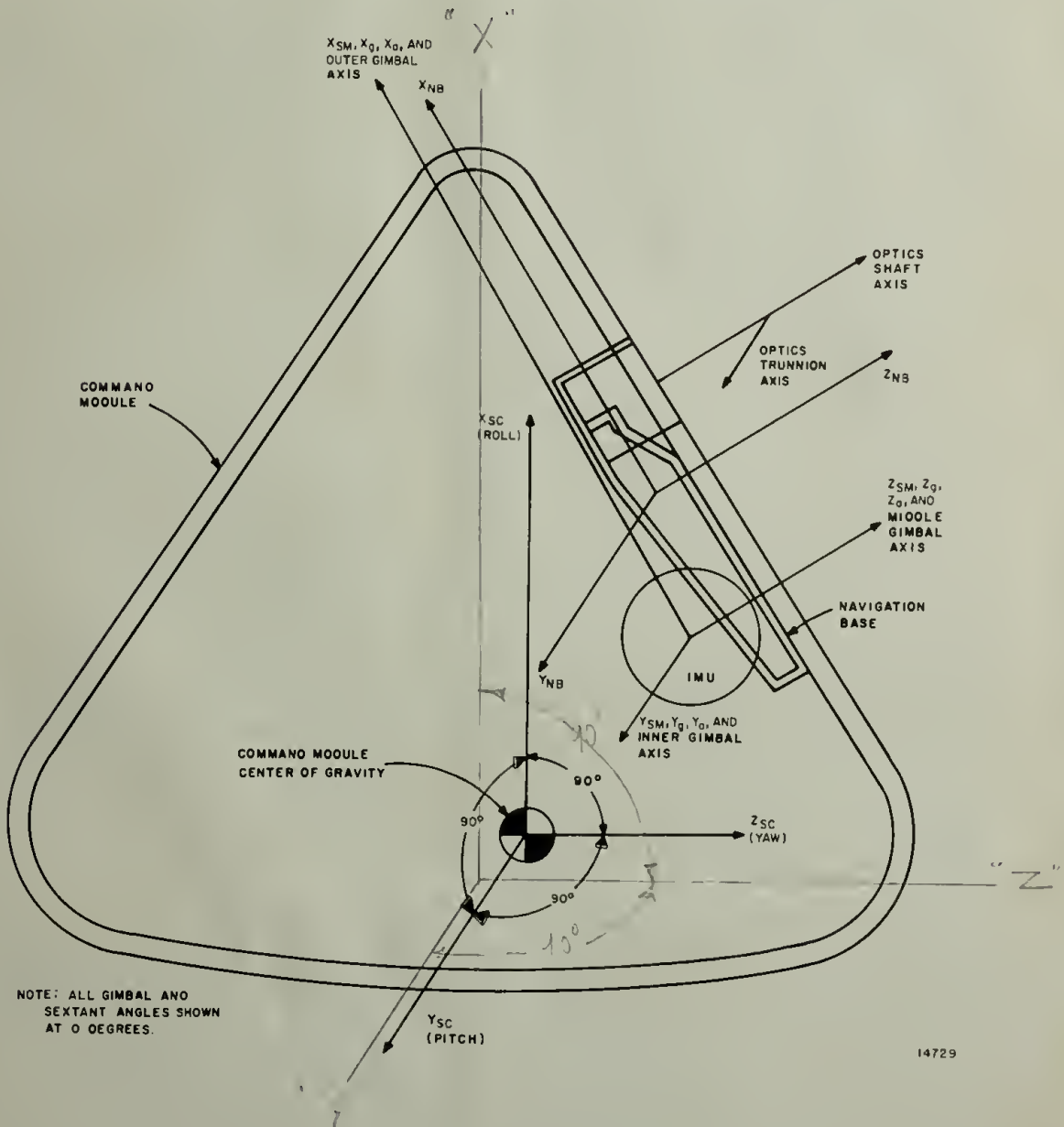


Figure 2-1. G and N System, Functional Block Diagram



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Figure 2-2. Orientation of Command Module and G and N System Axes

2-3.1 SPACECRAFT AXES. The spacecraft axes have two functions: they provide a reference for all other sets of Apollo axes and they define the point about which attitude maneuvers are completed. These two functions are accomplished with definition of the spacecraft symmetry axes and the spacecraft body axes. The spacecraft symmetry axes ( $X$ ,  $Y$ ,  $Z$ ) have a fixed relationship to the spacecraft. The  $X$  symmetry axis passes from the geometric center of the command module circular base through the apex of the command module. The  $Y$  and  $Z$  symmetry axes are perpendicular to one another and lie in the plane of the command module base. The  $Z$  axis points toward the downrange centerline of the spacecraft. The spacecraft body axes ( $X_{SC}$ ,  $Y_{SC}$ ,  $Z_{SC}$ ) are parallel to the symmetry axes and are located at the spacecraft center of gravity. Rotation about the  $X_{SC}$ ,  $Y_{SC}$ , and  $Z_{SC}$  axes (attitude changes or corrections) is defined as roll, pitch, and yaw respectively.

The spacecraft center of gravity is a movable point. It depends on the amount of fuel consumed, the astronauts' locations in the command module, and the stages of the Apollo spacecraft attached to the command module. The center of gravity must be determined for accurate attitude maneuvers.

2-3.2 NAVIGATION BASE AXES. The nav base axes ( $X_{NB}$ ,  $Y_{NB}$ ,  $Z_{NB}$ ) are references for spacecraft navigational operations. The nav base provides a rigid support for the IMU and OUA. The nav base also provides a mount for the IMU and OUA to the spacecraft structure. The  $X_{NB}$  axis is parallel to the conical surface of the command module and is displaced 33 degrees from the  $X_{SC}$  (roll) axis. The  $Y_{NB}$  axis is parallel to the  $Y_{SC}$  (pitch) axis. The  $Z_{NB}$  axis is perpendicular to the conical surface of the command module and is displaced 33 degrees from the  $Z_{SC}$  (yaw) axis.

2-3.3 INERTIAL AXES. The inertial axes provide references for measuring changes in velocity and attitude. The inertial axes are parallel to the nav base axes at zero degrees. The  $G$  and  $N$  system senses changes in the alignment of the inertial axes in order to determine the relationship of the inertial axes to the nav base axes and the spacecraft axes during flight. Comparison of the alignment of the inertial axes to that of the nav base axes and the spacecraft axes is used in calculating spacecraft attitude corrections.

2-3.3.1 Stable Member Axes. The stable member axes ( $X_{sm}$ ,  $Y_{sm}$ ,  $Z_{sm}$ ) provide a reference for aligning the inertial components and for defining the angular orientation of the inertial axes during flight.

2-3.3.2 Gyro Axes. The gyro axes ( $X_g$ ,  $Y_g$ ,  $Z_g$ ) define the positive input axes of the gyros and are parallel to the stable member axes. If the attitude of the stable member is changed with respect to space, the gyro senses the change along the gyro input axes and the circuitry associated with the gyros realigns the stable member to its original position.

APOLLO GUIDANCE AND NAVIGATION SYSTEM

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2-3.3.3 Accelerometer Axes. The accelerometer axes ( $X_a$ ,  $Y_a$ ,  $Z_a$ ) are the positive input axes of the accelerometers and are parallel to the stable member axes. Velocity changes are measured along the accelerometer input axes. The velocity data is used to determine spacecraft position and velocity.

2-3.3.4 Gimbal Axes. The gimbal axes (outer, inner, middle) are the axes of the movable gimbals. The gimbal angles are zero when the gimbal axes and the stable member axes are parallel. The attitude of the spacecraft with respect to the stable member is measured by gimbal resolvers.

2-3.4 OPTICAL AXES. The optical axes (figure 2-3) provide a reference for measuring the position of the command module and for aligning the IMU. The shaft axes ( $X_s$ ,  $Y_s$ ,  $Z_s$ ) and the trunnion axes ( $X_t$ ,  $Y_t$ ,  $Z_t$ ) are parallel to the nav base axes when the shaft angle ( $A_s$ ) and the trunnion angle ( $A_t$ ) are at zero degrees. The shaft drive axis (SDA) is coincident with the  $Z_s$  axis and the trunnion drive axis (TDA) is coincident with the  $Y_t$  axis. The  $Z_s$  axis is always parallel to  $Z_{NB}$  axis and the  $Y_t$  axis is parallel to  $Y_{NB}$  axis only at zero degrees shaft angle. The  $Z_s$  axis is used to direct the optics line of sight (LOS) toward landmark targets; therefore, the  $Z_s$  axis is also referred to as the landmark LOS (LLOS). The  $Z_t$  axis is used to direct the optics LOS toward star targets; therefore, the  $Z_t$  axis is also referred to as the star LOS ( $S_t$ LOS).

## 2-4 INERTIAL SUBSYSTEM

The ISS performs three functions: measures changes in spacecraft attitude, assists in generating steering commands, and measures spacecraft velocity changes due to thrust. To accomplish these functions, the IMU provides an inertial reference consisting of a stable member gimbaled in three degrees of freedom and stabilized by three integrating gyros.

The ISS is aligned to a predetermined reference each time the ISS is energized and during prolonged use. Realignment during use may be necessary since the gyros that maintain the space referenced member may drift and generate errors in the flight calculations.

Once the ISS is energized and aligned, any rotational motion of the spacecraft is essentially about the gimbaled stable member, which remains fixed in space. Resolvers, mounted on the gimbal axes to act as angular sensing devices, measure the attitude of the spacecraft with respect to the stable member. These angular measurements are sent to the AGC and displayed on CDU's to the astronaut.

The AGC calculates the gimbal angles necessary to change spacecraft attitude and sets the calculated gimbal angles in the CDU's. The difference between the angles set into the CDU's and the actual gimbal angles generates attitude error signals in the ISS. The error signals are sent to the stabilization and control system to change spacecraft attitude.

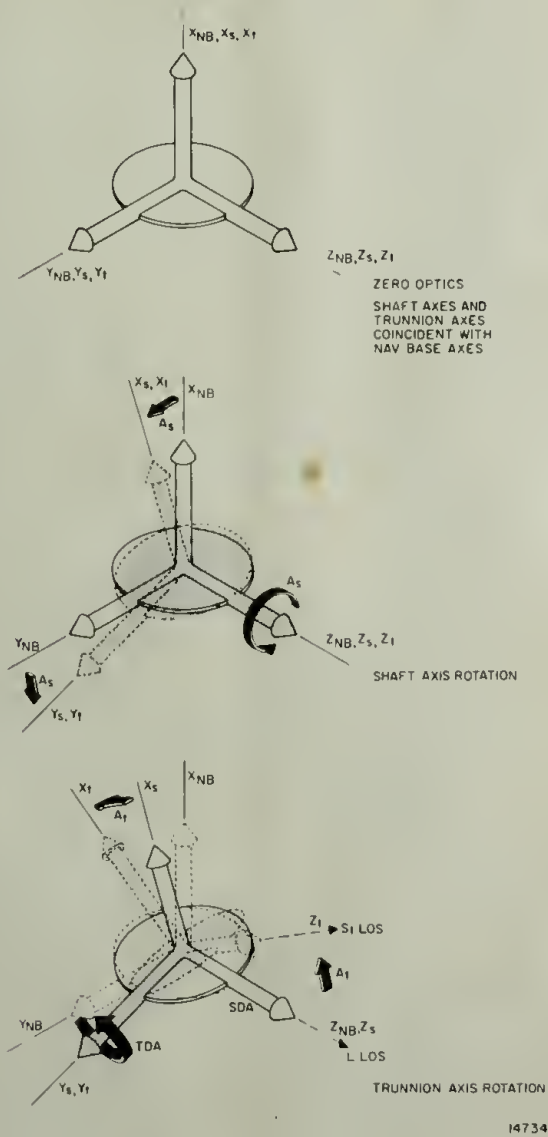


Figure 2-3. Orientation of Optical Axes to Nav Base Axes

Three pendulous accelerometers mounted on the stable member detect changes in velocity along the axes of the IMU stable member and supply incremental velocity data to the AGC. The AGC uses the incremental velocity data to calculate spacecraft total velocity.

For explanation purposes, the ISS is divided into functional blocks as shown in figure 2-4.

2-4.1 STABILIZATION LOOP. The three stabilization loops (figure 2-5) maintain the stable member in a specific spatial attitude so that the three mutually perpendicular 16 pulsed integrating pendulums (16 PIP's) can measure the proper components of spacecraft acceleration with respect to inertial space. An input to the stabilization loops is created by any change in spacecraft attitude with respect to the spatial attitude of the stable member. A change in spacecraft attitude is transmitted to the stable member through a three-degree-of-freedom gimbal system which couples the stable member to the spacecraft structure. This change tends to produce a change in stable member attitude which is sensed by the stabilization gyros and angular differentiating accelerometers (ADA's). When the gyros experience an input, they issue error signals which are amplified, resolved, if necessary, into appropriate components, and applied through a servo amplifier to the gimbal torque motors. The signals from the ADA's are amplified and applied to the servo amplifier where they are summed with the gyro signals. The gimbal torque motors then drive the gimbals until the stable member regains its original spatial orientation. The stabilization loops also align and maintain the stable member in a specific earth referenced orientation prior to flight.

The stabilization loop consists of three 25 inertial reference integrating gyros (25 IRIG), three ADA's, three IRIG preamplifiers, three ADA preamplifiers, a gyro error resolver, three gimbal servo amplifiers, six gimbal torque motors, three gimbals, and circuitry associated with these components. The inner gimbal is the stable member upon which the three stabilization gyros are mounted. Movement of any gimbal always results in a movement of the stable member and rotation about the input axis of one or more of the stabilization gyros.

The stabilization loop contains three parallel channels. Each channel starts with a stabilization gyro (X, Y, and Z), and terminates in a gimbal torque motor. Completion of the loop is mechanical, since driving the gimbals results in a movement of the stable member and a movement of the stabilization gyros. When movement of the IMU support gimbal or case tends to displace the stable member from its erected position, one or more of the stabilization gyros sense the movement and issue error signals. The phase and magnitude of the 3,200 cps gyro error signal represents the amount and direction of rotation experienced by the gyro about its input axis. The error signal is fed from the gyro signal generator ducosyn to the associated IRIG preamplifier. All three IRIG preamplifiers are packaged in a single module mounted on the stable member. The amplification is required to achieve a high signal-to-noise ratio through the gimbal slip rings.

The amplified gyro error signals also represent motion of the stable member about its axes since the stable member axes ( $X_{sm}$ ,  $Y_{sm}$ , and  $Z_{sm}$ ) and the gyro axes ( $X_g$ ,  $Y_g$ , and  $Z_g$ ) are parallel with respect to one another. If the middle and outer gimbal axes remain parallel with the stable member axes, then movement of the outer gimbal (roll movement of IMU case) is sensed by only the X gyro and movement of the middle gimbal (yaw movement of IMU case) is sensed by only the Z gyro. Movement of the stable member about the inner gimbal axis ( $Y_{sm}$ ), however, changes the relationship of the X and Z gyro input axes to the outer and middle gimbal axes and as a result, a movement of the middle gimbal and/or the outer gimbal is sensed by both the X and the Z gyros. The input required by the servo amplifiers to drive the gimbals and move the stable member back to its original position must be composed of components from both the X and Z gyros. The required gimbal error signals are developed by the gyro error resolver. The gyro error signals  $E(X_g)$  and  $E(Z_g)$  are applied to the two stator windings of the resolver. The two rotor windings are connected to the inputs of the outer and middle gimbal servo amplifiers. Movement of the stable member about the inner gimbal axis (pitch) changes the position of the resolver rotor relative to the resolver stator. This change corresponds electromagnetically to the change in the relationship of the stable member axes to the gimbal axes. The outputs taken from the rotor are the required middle and outer gimbal error signals ( $E_{mg}$  and  $E_{og}$ ). Since the inner gimbal torque motor axis and the Y axis of the stable member are the same axis, the Y gyro error signal  $E(Y_g)$  is equal to the inner gimbal error ( $E_{ig}$ ) and is fed directly to the inner gimbal servo amplifier.

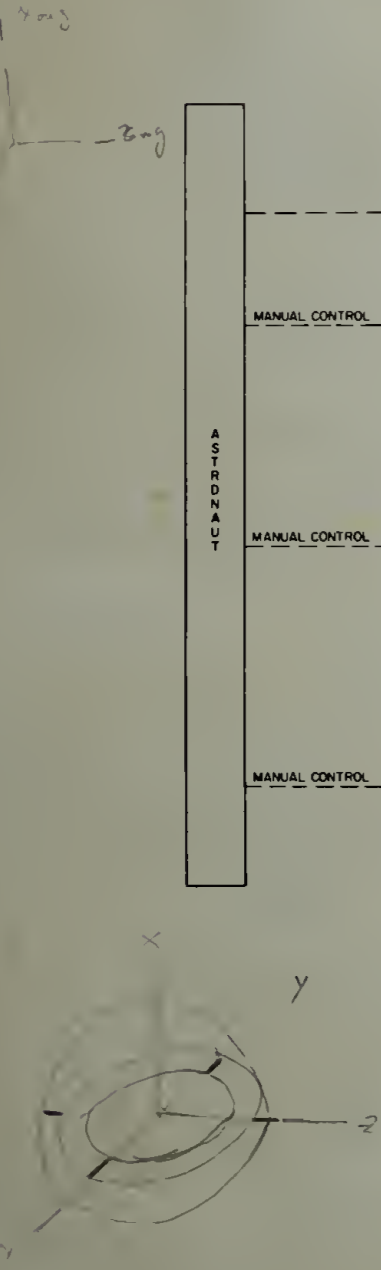
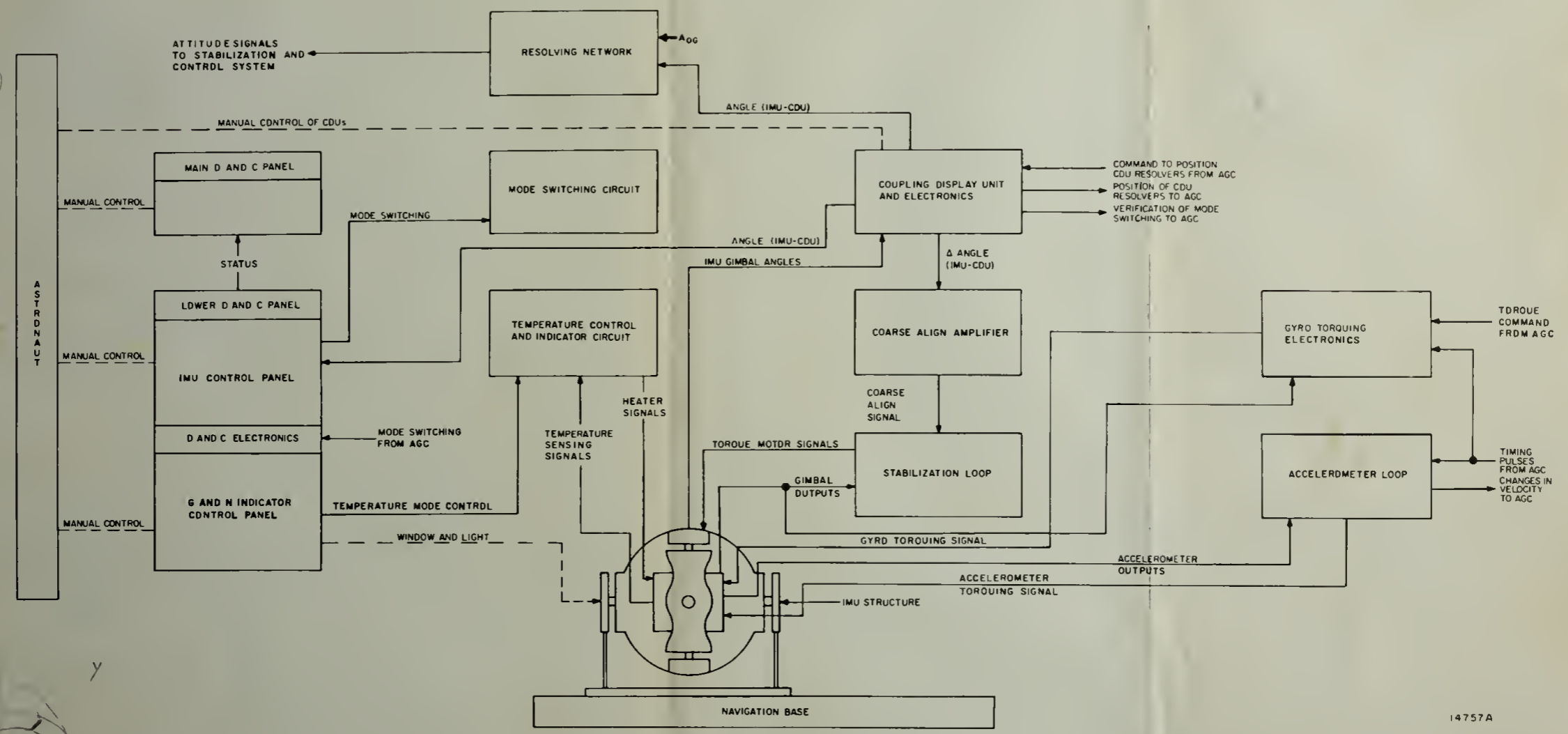
The three identical servo amplifier modules are located in the PSA and contain an ADA filter and decoupling network, a demodulator, and a stabilization amplifier. The stabilization amplifier consists of a dc amplifier and a torque drive amplifier. The demodulator circuit converts the 3,200 cps, zero or pi phase, gimbal error signals into a representative positive or negative dc current which is applied to the dc amplifier stage of the stabilization amplifier. At this stage, the gimbal error signals are summed with the outputs of the ADA's.

The use of the ADA's in the stabilization loop improves the dynamic response characteristics of the loop. The ADA is a fluid damped, torsional pendulum with a rotor winding which generates a voltage proportional to the angular velocity of the pendulum relative to the permanent magnet field fixed to the case. One ADA, mounted on the stable member, is positioned to sense rotational motion about the inner gimbal axis. The remaining two ADA's are mounted on the middle gimbal; one is positioned to sense rotational motion of the middle gimbal and the other is positioned to sense rotational motion of the outer gimbal. The output from the ADA's is amplified by the ADA preamplifiers. One ADA preamplifier module is mounted on the stable member and the other two are mounted on the middle gimbal. The output of the ADA preamplifier is filtered by the ADA filter and decoupling network in the servo amplifiers and then is applied to the summing junction of the dc amplifier. The output of the dc amplifier is applied to the torque drive amplifier which develops the current to drive the torque motors. The torque motors are mounted on opposite ends of each gimbal axis and operate in parallel. Two-motor operation halves the total armature resistance and doubles the maximum torque that may be



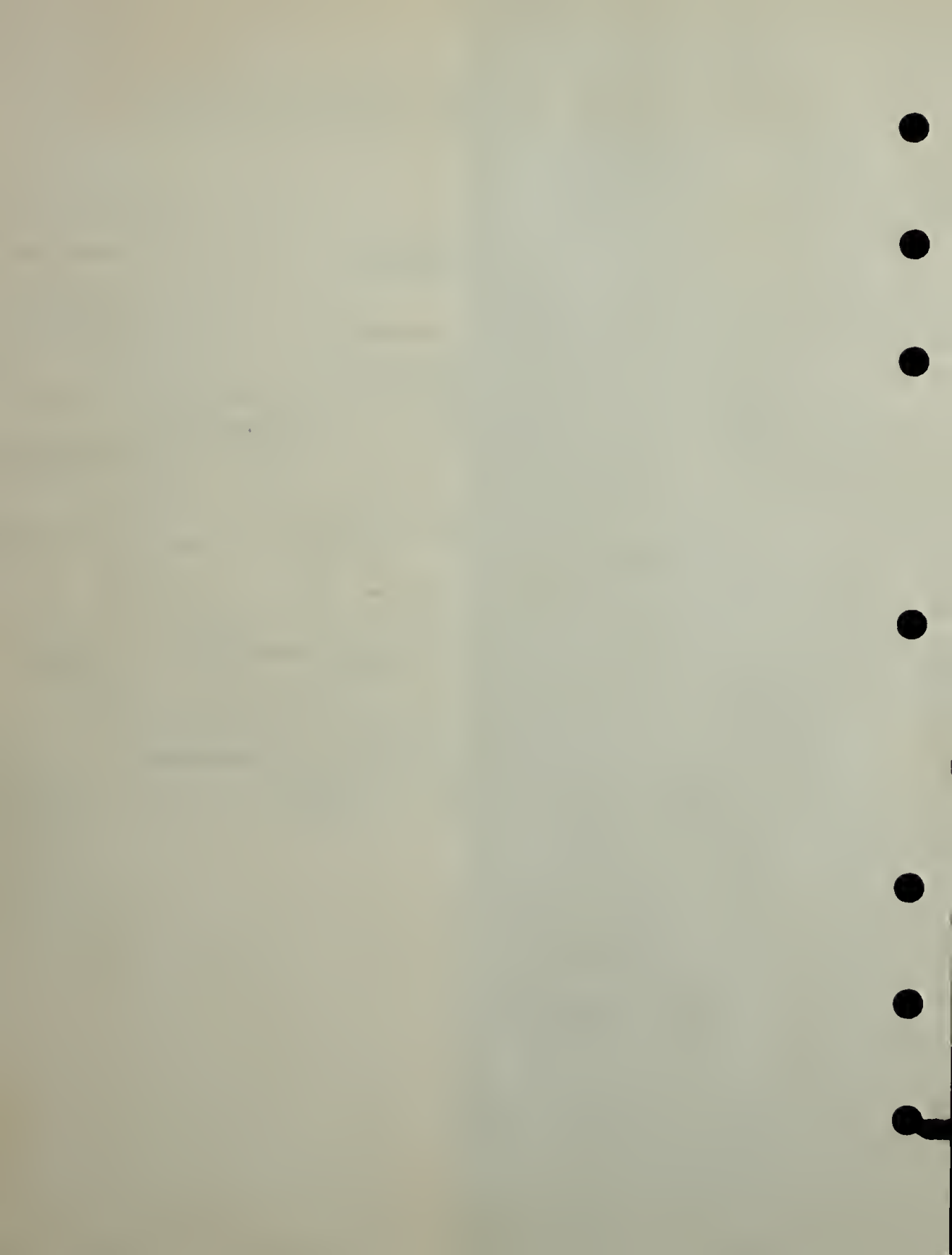
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Figure 2-4. ISS, Block Diagram



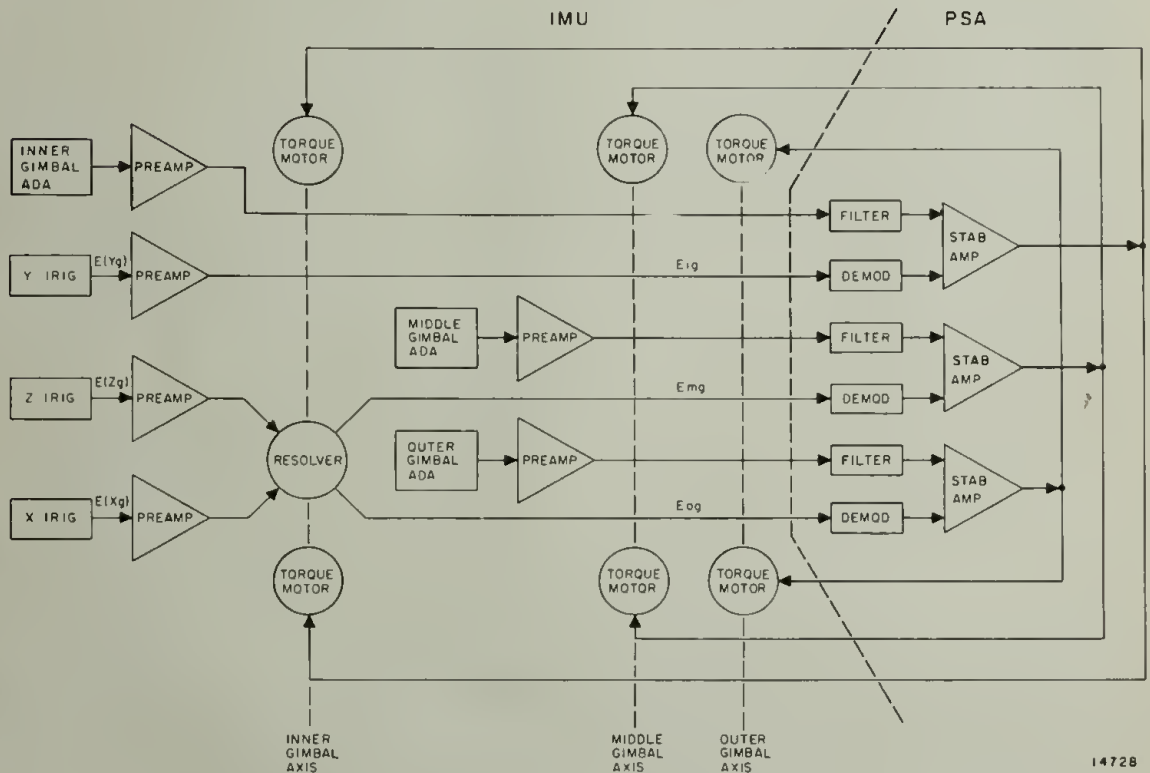
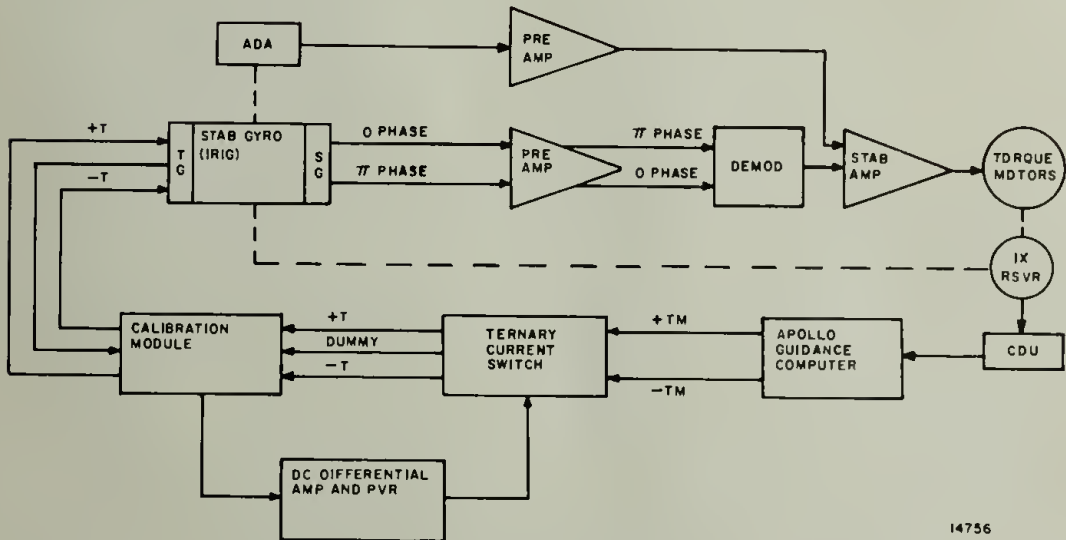


Figure 2-5. Stabilization Loop, Block Diagram

developed. Each torque motor pair has a resistor network connected in series with it to develop feedback which is applied to the input of the servo amplifier. The amount of feedback required for each loop differs to account for the differences in gimbal inertia. The proper feedback resistance value is selected by the connections to the servo amplifier module and gives each loop the proper gain.

2-4.2 GYRO TORQUING LOOP AND CALIBRATION CIRCUIT. The three gyro torquing loops (figure 2-6) can control the orientation of the stable member by pulsing the 25 IRIG torque generator ducosyns.

The three torquing loops consist of three stabilization loops, three CDU's, AGC, three ternary current switches, three calibration modules, three dc differential amplifiers, and three precision voltage references (PVR's).



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Figure 2-6. Gyro Torquing Loop, Block Diagram

During gyro torquing the CDU's are slaved to the gimbals and transmit the gimbal angles to the AGC.

The AGC calculates the number of plus or minus pulses necessary to bring the stable member to the desired alignment and pulses the ternary current switch with the torque commands (TM). (AGC calculations are based on optical measurements, known gimbal angles, and IRIG scale factors.)

The ternary current switch (figure 2-7) located in the PSA contains bistable multivibrators and current switches. The ternary current switch permits plus and minus torque commands (TM) from the AGC to apply dc current pulses to the 25 IRIG torque generator windings. The +TM input pulse to the ternary current switch is applied to a flip-flop or bistable multivibrator which biases the +T current switch to an on condition. With the +T current switch on, a constant dc signal is passed through +T current switch as a 120 milliamper nominal signal. The flip-flop remains in a set condition after a +TM set pulse has been received until the flip-flop is reset by a reset pulse from the AGC. In the reset condition, the zero outputs from the flip-flop are applied through an and gate to activate a dummy current switch which passes a constant dc signal to the scale factor network of the calibration module. The operation of a negative TM pulse (supplying -T output current) in the ternary current switch is the same as the operation of a positive TM set pulse.

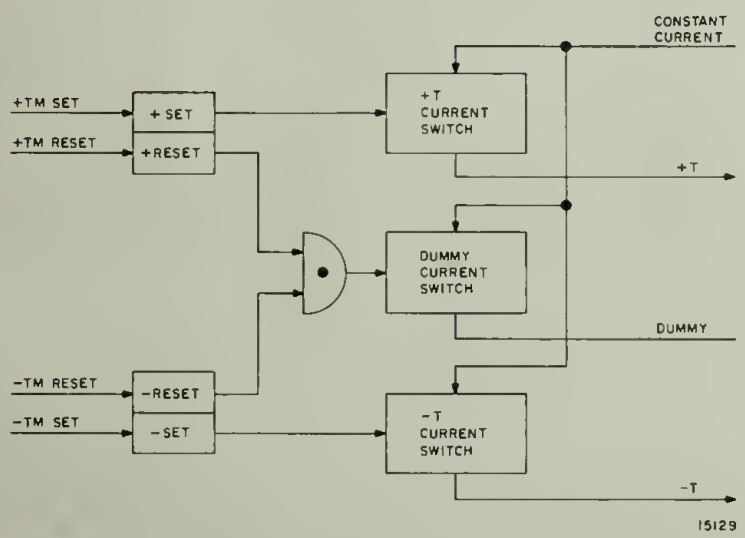


Figure 2-7. Ternary Current Switch, Block Diagram

The calibration module (figure 2-8) also provides a compensation network that tunes the torque generator windings to a resistive load for the +T or -T current pulses received from the ternary current switch. The +T 120 milliamperere dc pulse is applied to the odd numbered torque generator windings and the -T 120 milliamperere dc pulse is applied to the even numbered torque generator windings. When no torque signal is present, the dummy current switch current is on, completing the dc loop for a no-signal condition. The 120 milliamperere current is regulated by the dc differential amplifier which continuously compares the scale factor voltage of the calibration module with the output of the PVR.

The calibration circuit pulses the torque generator the required amount depending on the +T and -T pulses received from the ternary current switch.

The pulses supplied to the torque generator change the position of the 25 IRIG float. This change in position induces an error signal output from the 25 IRIG signal generator. The error signal is applied to the stabilization loop to change position of the IMU gimbal angles and the stable member. The change in gimbal angles is sensed by the CDU's and transmitted to the AGC by the CDU encoders.

**2-4.3 ACCELEROMETER LOOP.** The three accelerometer loops measure the acceleration of the stable member along three mutually perpendicular axes and integrate this data to determine velocity. The velocity data is used by the AGC to compute the spacecraft velocity vector. Figure 2-9 is a functional diagram of an accelerometer loop.

The accelerometer loops contain three 16 PIP's, three PIP preamplifiers, three ac differential amplifiers, three interrogators, three binary current switches, three calibration modules, and associated electronics.

The three mutually perpendicular 16 PIP's measure the components of acceleration of the stable member.

When an acceleration is sensed along the input axis of a 16 PIP, the pendulum rotates from a null (dead zone) position. The pendulum rotation induces an electrical signal in the signal generator. The 2 volt rms, 3200 cps, 1 phase, signal generator excitation voltage is synchronized with the AGC clock. The signal generator output consists of a zero or pi phase, amplitude-modulated signal. This output signal is proportional to the rotation of the pendulum about its output axis. The preamplifier mounted on the stable member provides a 45 degree phase shift from the reference excitation. The output of the preamplifier is supplied to a high gain ac differential amplifier. The amplifier signals are sent to the interrogator. The interrogator (figure 2-10) provides +T set outputs for zero phase inputs and -T set outputs for pi phase inputs.

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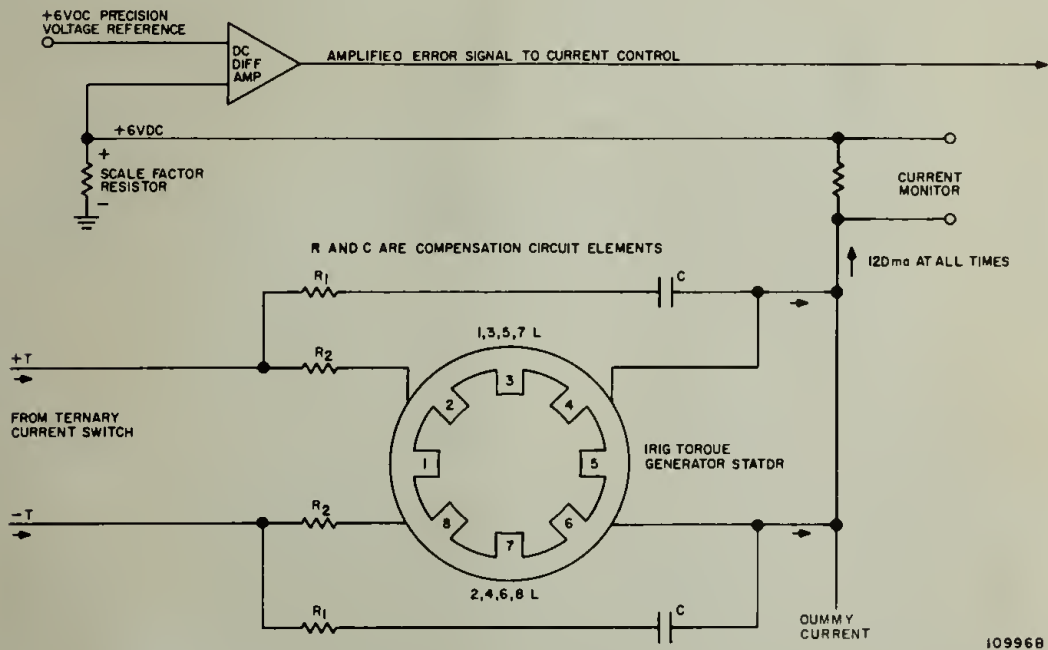


Figure 2-8. Calibration Circuit, Block Diagram

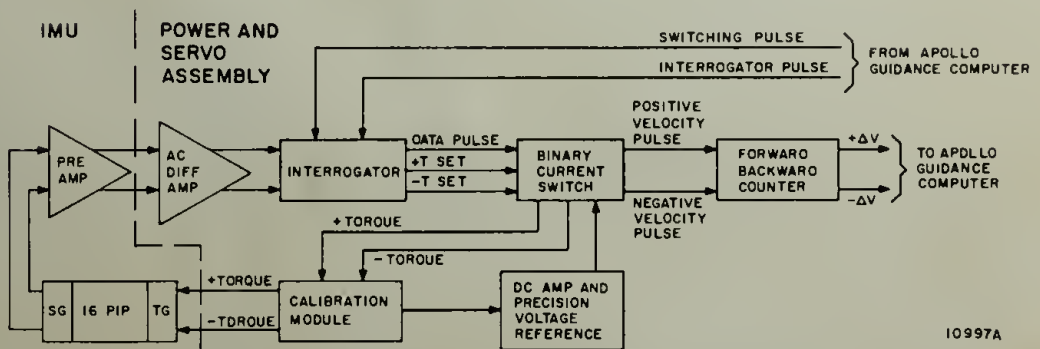


Figure 2-9. Accelerometer Loop, Block Diagram

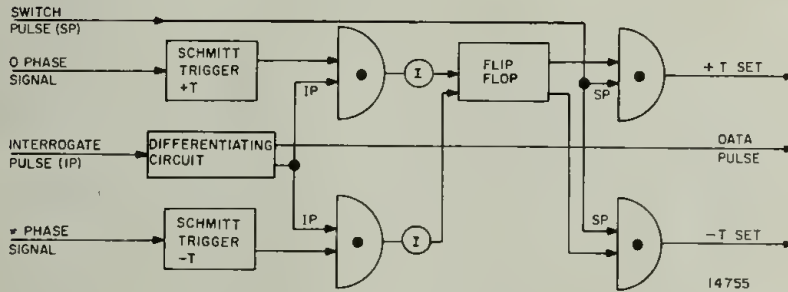


Figure 2-10. Interrogator, Block Diagram

The interrogator is located in the PSA and contains a schmitt trigger, differentiating circuit, bistable multivibrator, and and gates.

The amplified signals from the ac differential amplifier are applied to schmitt triggers within the interrogator. One trigger is driven by the zero phase signal while the other is driven by the pi phase signal. When the threshold of the trigger is exceeded, the voltage output level switches abruptly from a zero voltage to some positive voltage value. The width of the trigger output pulses is determined by the time during which the input voltage to the schmitt trigger exceeds the threshold level. The output of each schmitt trigger is applied to separate and gates.

Interrogate pulses (IP) are received by the interrogator from the AGC. An interrogate pulse is a three microsecond pulse occurring at 3200 cps and timed to occur 135 degrees after the positive zero crossing of the reference excitation. The interrogate pulse therefore occurs in the middle of the +T trigger pulses if the pendulum angle is positive and in the middle of the -T trigger pulses if the pendulum angle is negative.

The interrogate pulses are anded with the outputs of the triggers. The gated outputs are inverted and sent to the flip-flop as set or reset pulses. The outputs of the flip-flop are routed to two and gates. The flip-flop enables only one output gate at any switch pulse time. The outputs of the and gates are called +T set pulses and -T set pulses. The other output of the interrogator, the data pulse, is formed by the differentiation of the interrogate pulse. The outputs from the interrogator are routed to the binary current switch.



The binary current switch (figure 2-11) is located in the PSA and contains bistable multivibrators, current switches, and and gates. The +T set and -T set pulses from the interrogator are used to turn on the plus and minus current switches. The binary current switch uses the interrogator outputs to generate 16 PIP torquing current and positive or negative velocity pulses if acceleration is sensed.

The +T set and -T set pulses from the interrogator are the inputs to a bistable or flip-flop multivibrator. If the flip-flop is already in the + set condition, further application of +T set pulses to the flip-flop does not change its condition. The + set condition persists until the pendulum angle decreases to zero and goes negative. At this point the interrogator generates a -T set pulse which causes the flip-flop to go to the - set condition. The flip-flop outputs control transistors within the current switches which close the path to provide torquing current to the 16 PIP +T or -T torquing coils. The condition of the flip-flop determines which torquing coil is energized.

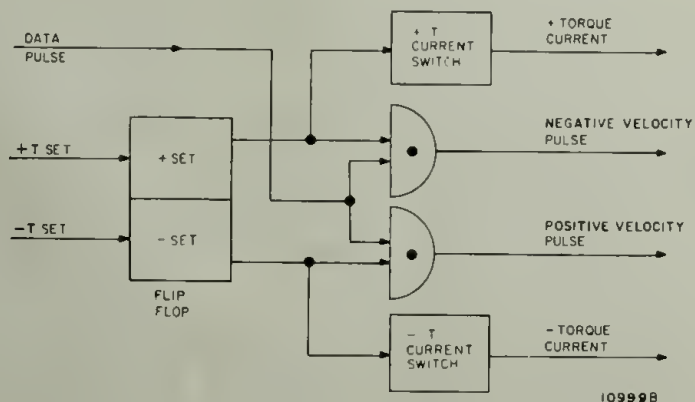


Figure 2-11. Binary Current Switch, Block Diagram

The outputs of the flip-flop also go to two and gates where they are anded with the data pulses from the interrogator. This anding produces pulses (P or N) representing positive or negative velocity. Each pulse represents an increment of velocity and is defined by the loop scale factor in terms of centimeters-per-second-per-pulse. The velocity pulses go to the forward-backward counter.

The +T and -T outputs of the binary current switch are sent to the calibration module. The calibration module compensates for the inductive load of the 16 PIP torque generator ducosyns and regulates the balance of the plus and minus torques. The calibration module consists of two load compensation networks in parallel with the torquing coils of the 16 PIP. The torquing coils, along with the compensation network, appear as a resistive load to the output of the binary current switch. Variable resistors regulate and balance the amount of torque developed by the torquing coils. This balancing insures that for a given torquing current an equal amount of torque is developed in either direction. A feedback signal from the calibration module to the dc amplifier and the precision voltage reference regulates the torquing current supplied by the binary current switch.

The dc differential amplifier and PVR maintain the current through the torquing coils of the torque generator ducosyn at a constant value necessary to maintain the PIP loop scale factor at the proper value. The PVR is supplied with regulated 32 volt dc excitation and, through the use of precision circuits, develops a precise 6 volts for use as a reference. The 6 volts developed by the PVR is compared with the 6 volts developed across the scale factor resistor in the calibration module. This comparison is made by the dc differential amplifier. This error voltage controls a series current regulator from the 120 volt dc source. Thus, controlled current can be maintained in the torquing coils.

The forward-backward counter (figure 2-12) is driven by the P and N pulses from the current switch. During operation of the 16 PIP loop with no acceleration input, the loop operates at a rate of 3 P pulses and then 3 N pulses. The counter counts forward on the P pulses and then backward on the N pulses. The counter continues this operation and generates no  $\Delta V$  pulses to the AGC. However, with an acceleration input to the 16 PIP, the loop no longer operates on the 3:3 ratio and the counter exceeds its capacity and reads out  $\Delta V$  pulses to the AGC.

2-4.4 CDU LOOP. The mechanization of the CDU loop for the ISS is shown in figure 2-13. In this mechanization, the sixteen speed (16X) and the single speed (1X) CDU resolvers function as receivers and the 16X and 1X resolvers mounted on the IMU in the inter-gimbal assemblies serve as transmitters. The one-half speed (1/2X) resolver is used only to zero the CDU. The outputs of these three resolvers provide inputs to the selector circuit. The 1X resolver also provides an input to the coarse align amplifier and the spacecraft attitude control loop, depending on the mode of operation. The output of the IMU outer gimbal 1X resolver is also routed to the outer gimbal CDU 16X resolver and the output of the CDU 16X resolver is routed to the stabilization and control system during the entry mode. The selector circuit consists of four pairs of diodes. The 16X and 1X IMU-CDU resolvers each use one pair of diodes and the 1/2X uses two pairs.

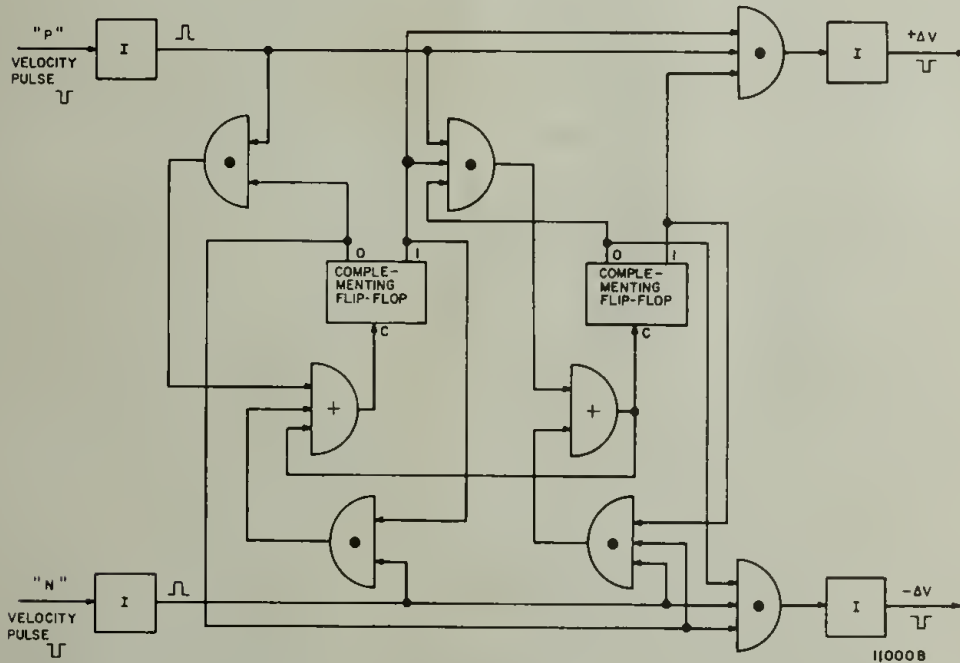


Figure 2-12. Forward-Backward Counter, Block Diagram

The diodes in the 1X resolver and 1/2X resolver circuits are selected so that the input to the motor drive amplifier (MDA) is cut off when the voltage drops below a certain level. The diodes in the 16X resolver circuit are selected so that the resolver output is limited at a certain level. This combination of diodes determines which of the resolvers supplies the control input to the CDU MDA and, therefore, the coarse-fine control of the IMU-CDU loop in the zero encoder and fine align modes.

The MDA can also receive inputs from the slew switch or the digital to analog converter (DAC) as well as a feedback signal from the motor-tachometer. The inputs to the MDA are first amplified and then, through the use of two integrated choppers, any input quadrature voltage is rejected. This signal is again amplified to provide an output to drive the CDU motor. The encoder electronics, as used in the ISS mechanization, generates one pulse per gear tooth. Each pulse represents approximately 40 arc-seconds of rotation of the 1X CDU resolver shaft. The pulse has a maximum repetition rate of approximately 2,200 pps. Malfunctions in the CDU loop are identified on the condition annunciator. A signal denoting the malfunction is transmitted to the AGC.

2-4.5 MODES OF OPERATION. The ISS has six major modes of operation which can be manually controlled at the IMU control panel by six pushbuttons. The modes of operation are: zero encoder, coarse align, manual CDU, fine align, attitude control, and entry. Two additional switches are provided on the IMU control panel: a pushbutton for initiating manual alignment of the IMU using the CDU's and a transfer switch to select either manual or computer control of the IMU.

The mechanization of the ISS switching is shown in figure 2-14. The relays, diodes, and 100 second time delay are contained in the D and C electronics. The method of controlling the mode switching circuits depends upon the setting of the transfer switch: manual or computer. With the transfer switch in the manual position, relays K8 through K13 are used as latching relays to hold relays K1 through K5 energized after the mode pushbutton is released. Modes can be selected in any sequence. The selection of a new mode deenergizes the presently latched-in relay. The only ISS bistable relay is K13, used to prevent a change of state due to a momentary power failure in the critical entry mode. Since K13 is bistable, a reset K13 command must be generated when entering each of the other five modes. During computer control, the mode relays K1 through K5 are held energized by a continuous signal applied by the AGC.

2-4.5.1 Standby Mode. During this mode, 28 volt dc prime power is applied to the 3200 cps, 1 percent power supply and the 3200 cps square wave supply. These power supplies provide excitation for the temperature control circuits, the gyro and the accelerometer ducosyns, and the temperature control electronics. All the ISS mode switching relays are deenergized with relay K13 either set or reset.

2-4.5.2 IMU Turn-on Mode. When the ISS is switched into the operate mode, prime power is applied to all the ISS power supplies. The 100 second time delay starts its timing cycle (see figure 2-14) and the IMU DELAY lamp on the condition annunciator is lighted through contacts of energized relay K7. The ISS also enters coarse align through contacts of energized relay K2. The purpose of the coarse align mode is to slave the IMU gimbals to the CDU's for 100 seconds after power is applied to the gyro wheels to prevent torquing the gyros until the gyro wheels have obtained proper speed. After a 100 second interval, relay K6 is energized by the 100 second time delay circuit. When energized, relay K6 deenergizes relays K7 and K2, removing power from the IMU DELAY lamp and switching the ISS from the coarse align mode. If the ISS was in the entry mode, relay K13 is set and the ISS returns to the entry mode. Otherwise, all the relays except K6 and K12 are deenergized placing the ISS in the attitude control mode. This condition continues until one of the six modes is selected.

2-4.5.3 Zero Encoder Mode. The purpose of this mode is to drive the CDU shaft angle to a zero position utilizing the CDU's 16X and 1/2X shaft resolvers. The zero encoder mode is selected manually by pressing the zero encoder pushbutton S5 (figures 2-14 and 2-15), which energizes relay K8. Relay K8 is latched in by a ground routed through switches S9, S5, S6, S7, S8, and S10; deenergized relays K13, K11, K10, and K9; and energized relay K8. If the system is in manual control and has been turned on for at least 100 seconds, then relay K1 (zero encoder relay) and relay K4 (fine align relay) are energized. Relays K1 and K4 are energized by a ground routed through energized

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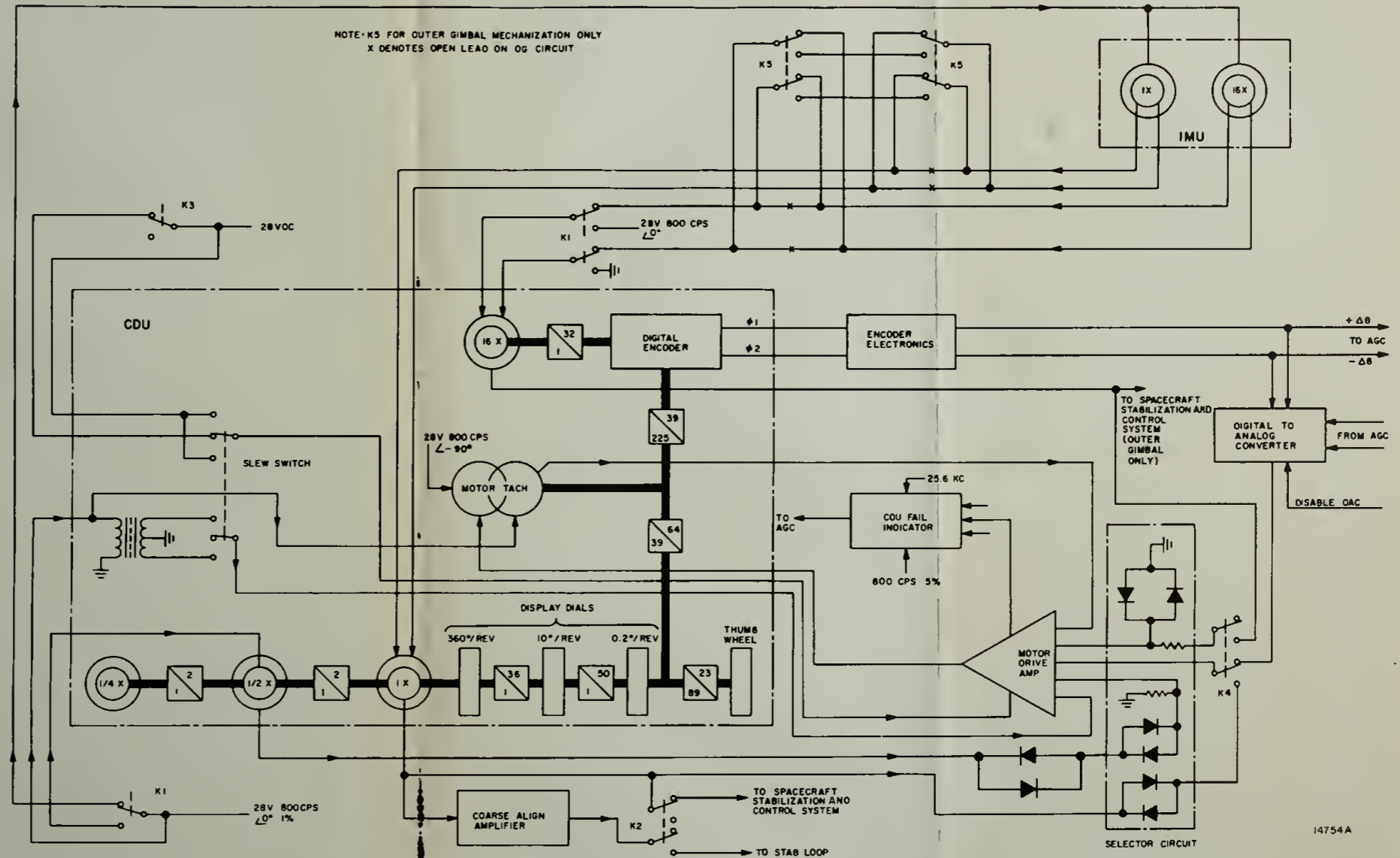
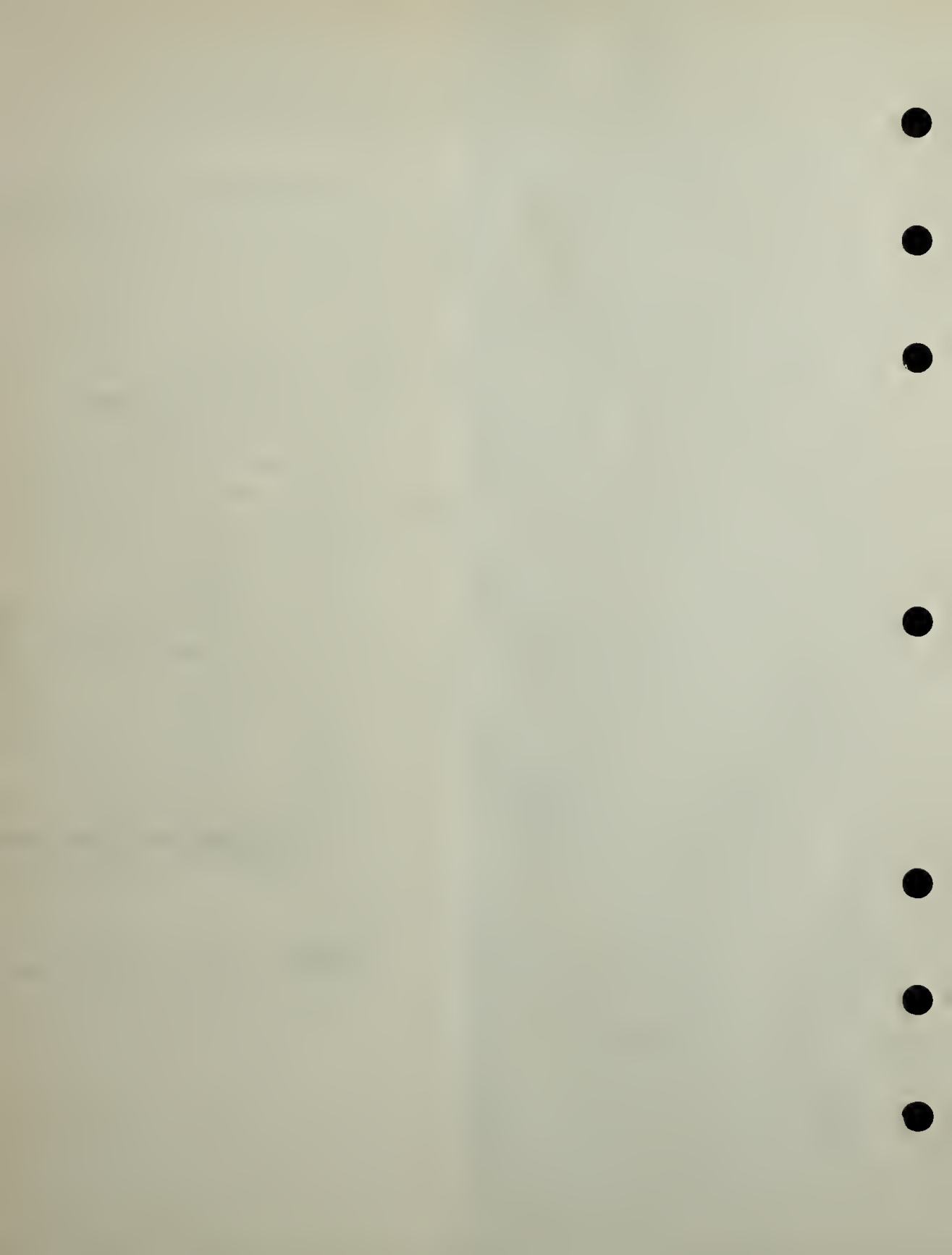
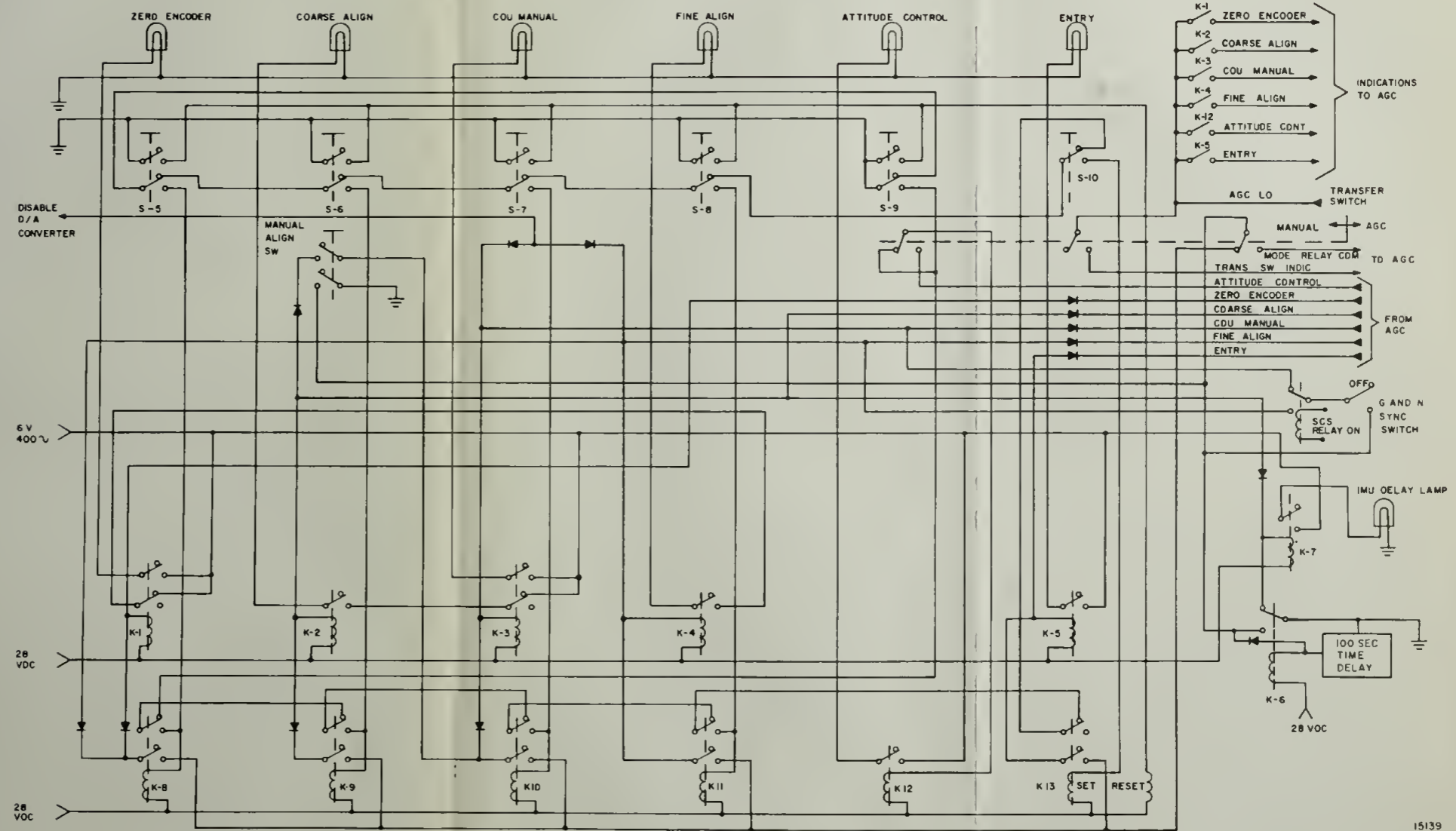


Figure 2-13. CDU Loop Mechanization

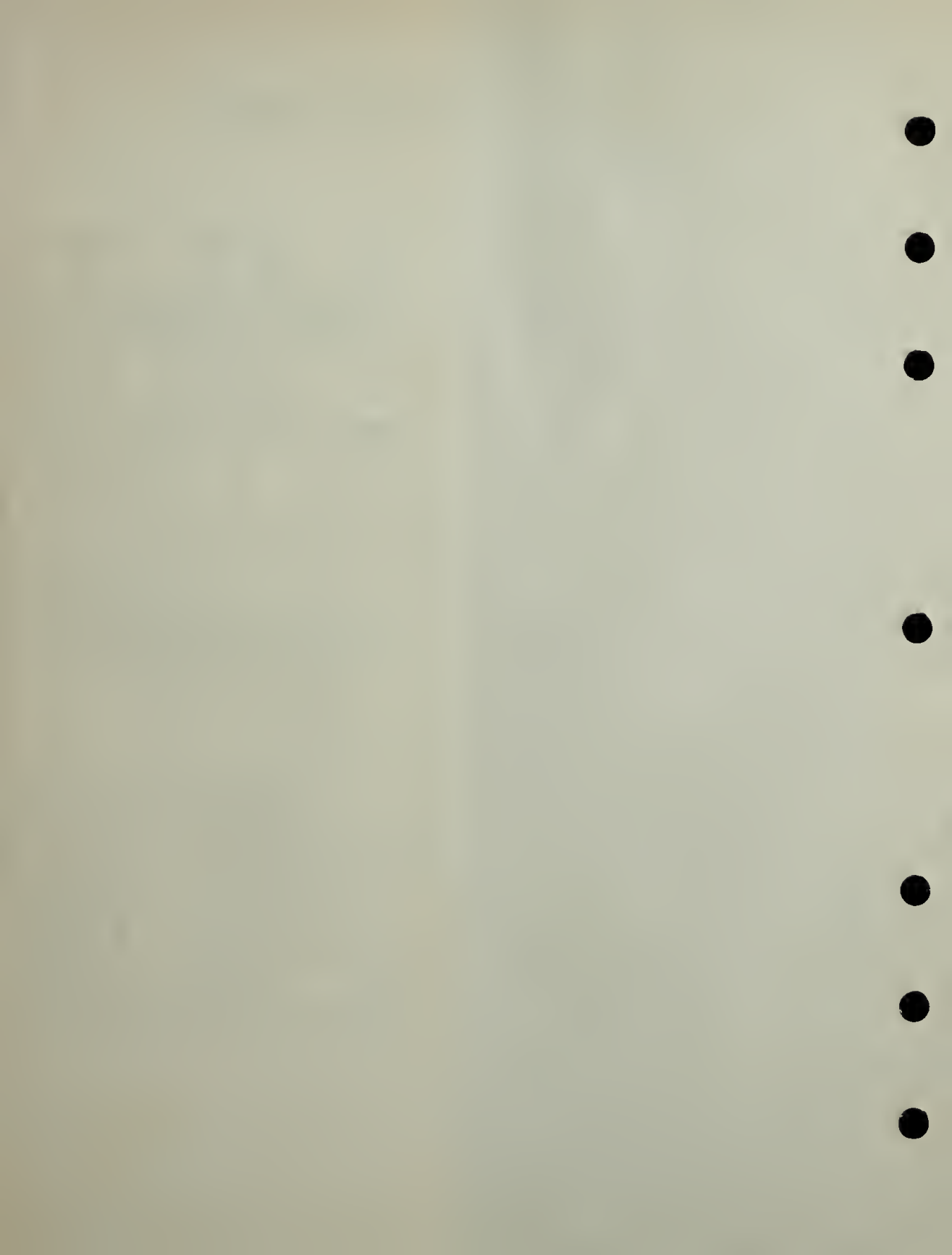


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Figure 2-14. ISS Mode Switching Diagram





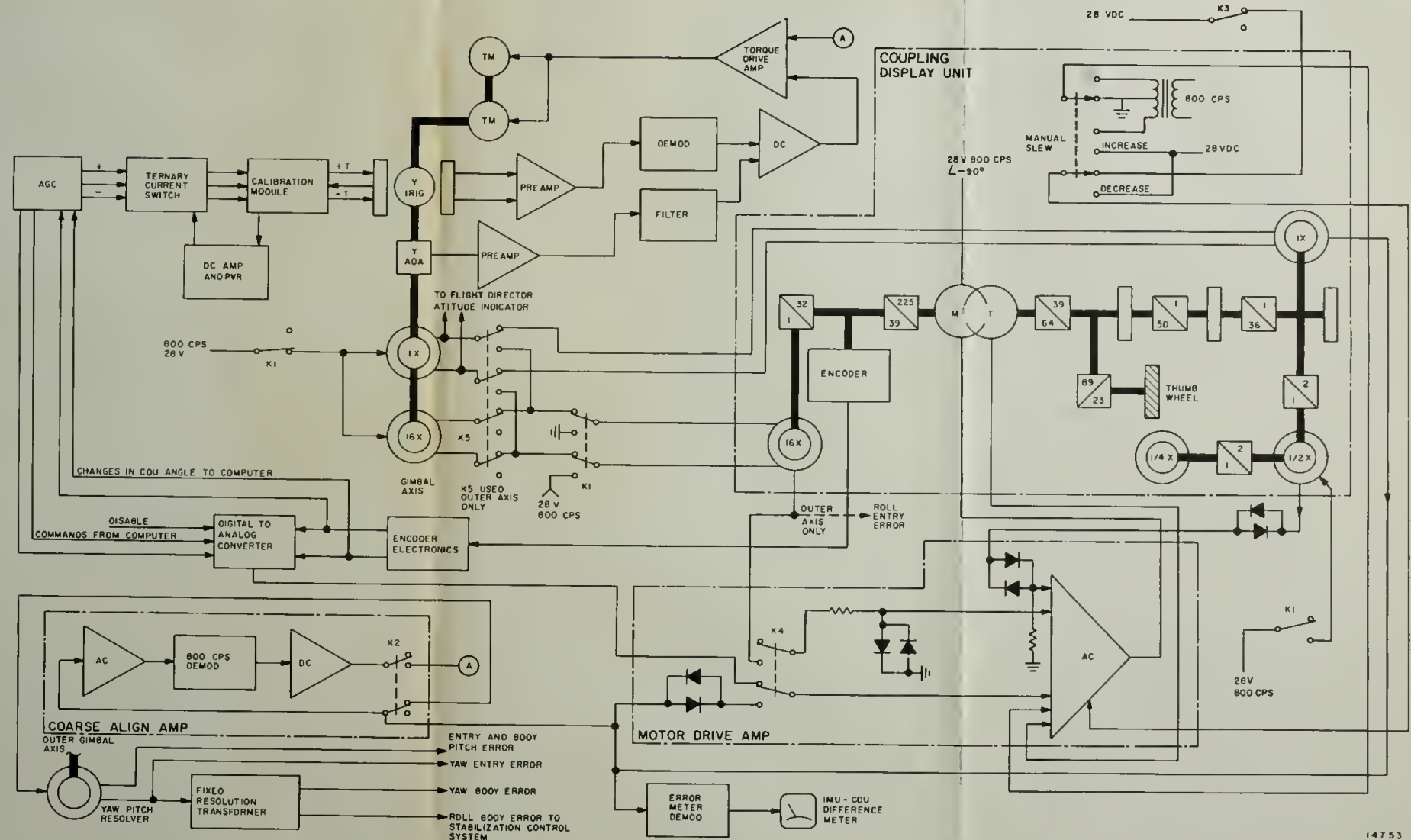
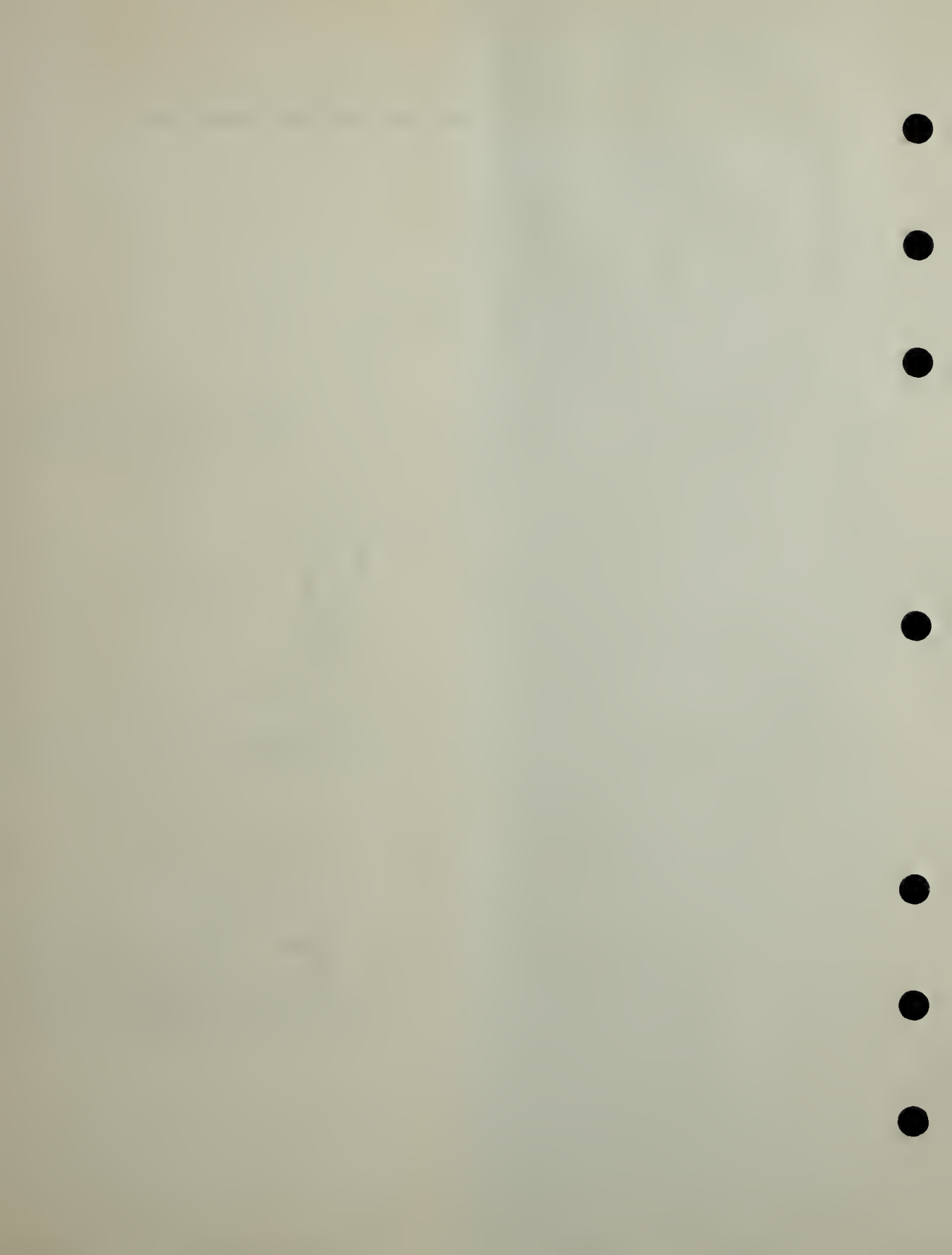


Figure 2-15. IMU-CDU Interface, Block Diagram



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relay K6; through the transfer switch, in the manual position; and through energized relay K8. The zero encoder lamp lights and the fine align lamp is disabled when relay K1 energizes. Relay K4 being energized prevents the DAC from driving the CDU. If the system is in computer control, a command which holds relays K1 and K4 energized is received from the AGC and the latch-in relay K8 is not required. A discrete is sent to the AGC by contacts on relays K1 and K4 to indicate that they are energized. The AGC then modes the system from zero encoder to fine align, attitude control, and back to fine align. This moding prevents null ambiguity between the IMU and CDU's in the fine align mode.

In the loop used to drive the CDU's to zero, an 800 cps reference signal is applied through relay K1 to the stator winding of the 16X and 1/2X CDU resolvers. The 16X resolver rotor output is switched by relay K4 into the MDA while the 1/2X CDU resolver is wired directly into the MDA. The MDA output is applied as the control signal to the CDU servo motor which drives the CDU geartrain and positions the resolvers. The sine winding of the 16X and 1/2X resolver rotors is used since the sine function goes to zero at a zero shaft angle. The IMU is not disturbed during the zero encoder mode of operation. Maximum time required for zeroing is approximately 30 seconds.

**2-4.5.4 Coarse Align Mode.** The purpose of this mode is to slave the IMU gimbal angles to the CDU angles. The mode is entered by one of four means: pressing of the coarse align pushbutton with the ISS in manual control, AGC command of coarse align mode with the system in computer control, IMU turned on for less than 100 seconds, or system in manual CDU mode and the manual align pushbutton pressed.

If the mode is entered by pressing the coarse align pushbutton, relay K9 is energized by a ground routed through switches S6, S5, and S9. Relay K9 is held energized after the coarse align pushbutton is released by a ground routed through switches S9, S5, S6, S7, S8, and S10; through deenergized relays K13, K11, and K10; and through energized relay K9. With relay K9 energized, the system in manual control, and the IMU turned on for at least 100 seconds, then relay K2 is energized by a ground routed through energized relay K6, through the transfer switch, and through energized relay K9. The three other methods of entering coarse align mode energize relay K2 directly. With relay K2 energized, the coarse align lamp lights unless the system is in manual CDU mode. Relay K2 permits a discrete signal to be sent to the AGC indicating the system mode of operation.

The mechanization of the coarse align mode is shown in figures 2-14 and 2-15. Positioning of the CDU is performed by pulses from the AGC sent to the DAC. When the AGC is used to position the IMU gimbals, a 3,200 pps signal is applied to the DAC gated at 1/12 second interval. The three DAC's receive pulses sequentially, requiring 1/4 second to supply all the DAC's with an input. The cycle is repeated until the required number of pulses have been issued by the AGC. For a small angle of shaft rotation, the DAC provides an 800 cps output proportional in amplitude to the number of pulses received. The output goes to the MDA via relay K4 (fine align relay) and drives the CDU shaft. The CDU encoder electronics provides feedback to the AGC and supplies an input to the DAC proportional to the CDU shaft rotation. Each pulse is equal to approximately

40 arc seconds of rotation of the 1X resolver. Theoretically, one pulse out of the AGC to the DAC should cause the encoder to generate one pulse of feedback to the AGC and DAC. The pulse input from the AGC to the DAC and the feedback from the encoder should cancel each other in the AGC when CDU shaft angle equals the AGC commanded angle.

The input signal to the coarse align amplifier is received from the CDU 1X resolver which has been positioned to the desired IMU gimbal angle. The stator of the gimbal 1X resolver is excited with an 800 cps reference signal routed through relay K1. The rotor of the IMU and CDU 1X resolvers are connected through deenergized relay K5. When the two rotor angles differ, an error signal proportional to the sine of the angular difference is picked off the CDU resolver rotor and applied to the coarse align amplifier. The signal is amplified, demodulated, and sent through the coarse align relay, K2, (one in each of the three coarse align amplifiers) to the torque drive amplifier. The output of the torque drive amplifier is the control signal for the gimbal torque motors which drive the gimbals until the gimbal 1X resolver angular position equals the CDU 1X resolver angle. The error signal from the CDU 1X resolver is also applied to the IMU-CDU difference meter on the IMU control panel. A demodulator circuit is provided to change the 800 cps signal to a dc signal to drive the meter.

2-4.5.5 Manual CDU Mode. This mode is used in conjunction with the manual align mode as a backup for IMU alignment to establish coarse alignment of the IMU. The manual CDU mode is entered by one of three methods: by pressing the manual CDU pushbutton with the ISS in manual control, by AGC command of the manual CDU mode when the system is in computer control, or by turning on the G and N sync switch on the main display and control panel with the HOLD/FOLLOW switch set to HOLD.

The mechanization of the manual CDU mode is shown in figures 2-14 and 2-15. If the mode is entered by pressing the manual CDU pushbutton, relay K10 is energized by a ground routed through switches S9, S5, S6, and S7. Relay K10 is held energized after the manual CDU pushbutton is released by a ground routed through switches S9, S5, S6, S7, S8, and S10; through deenergized relays K13 and K11; and through energized relay K10. If the system is in manual control and the IMU has been turned on for at least 100 seconds, then relay K3 is energized by a ground routed through energized relay K6, through the transfer switch, and through energized relay K10. When relay K3 energizes, the manual CDU lamp lights, a discrete indicating the mode of operation is sent to the AGC, and the DAC is disabled. With relay K10 energized, the manual align pushbutton is activated and when pressed, energizes the coarse align relay, K2. The coarse align lamp does not light since relay K9 is deenergized. The G and N sync switch on the main display and control panel energizes relay K3 independently of computer or manual control. The switch is used during the attitude control mode to lock the CDU's and hold the spacecraft at a preferred orientation obtained by maneuvering the spacecraft with the attitude control stick. Relay K3 removes the 28 volt dc signal from the CDU MDA to prevent the output from positioning the CDU's. The slew switch can drive the CDU by restoring the 28 volts dc and applying 800 cps signal to the MDA.

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2-4.5.6 Fine Align Mode. The purpose of this mode is to bring the stable member to fine alignment by pulsing the torque duocosyns and to slave the CDU's to the IMU gimbal angles. The number of required pulses is calculated and issued by the AGC based on optical alignment measurements. The mode is entered by one of three methods: pressing of the fine align pushbutton with the ISS in manual control, application of fine align commands from AGC with the ISS in computer control, or turning on the G and N sync switch on the main display and control panel with the HOLD/FOLLOW switch set to FOLLOW. If the mode is entered manually, relay K11 is energized by a ground routed through switches S9, S5, S6, S7, and S8. (See figure 2-14.) Relay K11 is held energized after the fine align pushbutton is released by a ground routed through switches S9, S5, S6, S7, S8, and S10, through deenergized relay K13, and through energized relay K11. The fine align relay, K4, is energized, after relay K11 energizes, by a ground routed through energized relay K6, through the transfer switch, and through energized relay K11. Energizing relay K4 provides power to light the fine align lamp and provides a discrete to the AGC indicating the mode of operation. When the G and N sync switch is turned on and the HOLD/FOLLOW switch is set to FOLLOW, relay K4 is energized. Two conditions are required to energize the stabilization and control system relay: the stabilization and control system must be in the attitude control mode, and the spacecraft attitude must be controlled by use of the attitude control stick. With these conditions satisfied, the CDU's are slaved to the IMU gimbal angles and, when a new attitude is established, the CDU angles provide the reference for holding the spacecraft's new orientation.

The fine align mode (see figure 2-14) performs two tasks: torquing of the gyro floats so the stabilization loops reposition the stable member, and driving the CDU's to repeat the IMU gimbal angles. The torquing is accomplished by the AGC plus and minus torquing pulses at a rate of 3,200 pps applied to the ternary current switch. The switch output pulses displace the stabilization gyro float from a null and generate error signals in the stabilization loop. The error signal in the stabilization loop causes the torque motors to drive the gimbals to position the stable member. Since relay K4 is energized, the CDU's follow the gimbal angles. The angular difference between the IMU and CDU 1X and 16X resolvers generates a CDU resolver rotor error signal proportional to the sine of the angular difference. The signal is sent through relay K4 to the MDA. The MDA output excites the control winding of the CDU drive motor and drives the CDU shaft until the IMU and CDU angles are equal. Upon completion of the fine align mode, the stable member is fine aligned to a reference coordinate system and the CDU readouts indicate the gimbal angles.

2-4.5.7 Attitude Control Mode. In this mode velocity steering or attitude control signals are generated so that the IMU gimbal angles and CDU shaft angles remain equal. The attitude of the spacecraft is controlled by the position of the CDU's. The mode can be entered by one of two methods: pressing of the attitude control pushbutton with the ISS in manual control, and by AGC attitude control commands with the ISS in computer control. Attitude control does not have a separate mode relay but is mechanized by deenergizing all the mode relays, K1 through K5. (See figure 2-14.) Relay K12, which is latched in by the other mode pushbuttons and relays, lights the mode lamp and sends a discrete to the AGC indicating the mode of operation. If any of the other five modes are entered, relay K12 is deenergized.

In the attitude control mode (see figure 2-14), all the mode relays are deenergized. The error signal which is used for attitude control and velocity steering is generated by the 1X CDU receiving resolver and is sent to the stabilization and control system through the coarse align relay (K2), pitch-yaw resolver, and fixed resolution transformer. The error signal results from the difference between the angular position of the IMU and CDU 1X resolvers. While in attitude control, the CDU resolver can be positioned automatically by the AGC as described in the coarse align mode, paragraph 2-4.5.4. If velocity steering is being performed, the AGC drives the CDU's to control the direction of the thrust vector and the CDU error signal is used to position the service propulsion engine.

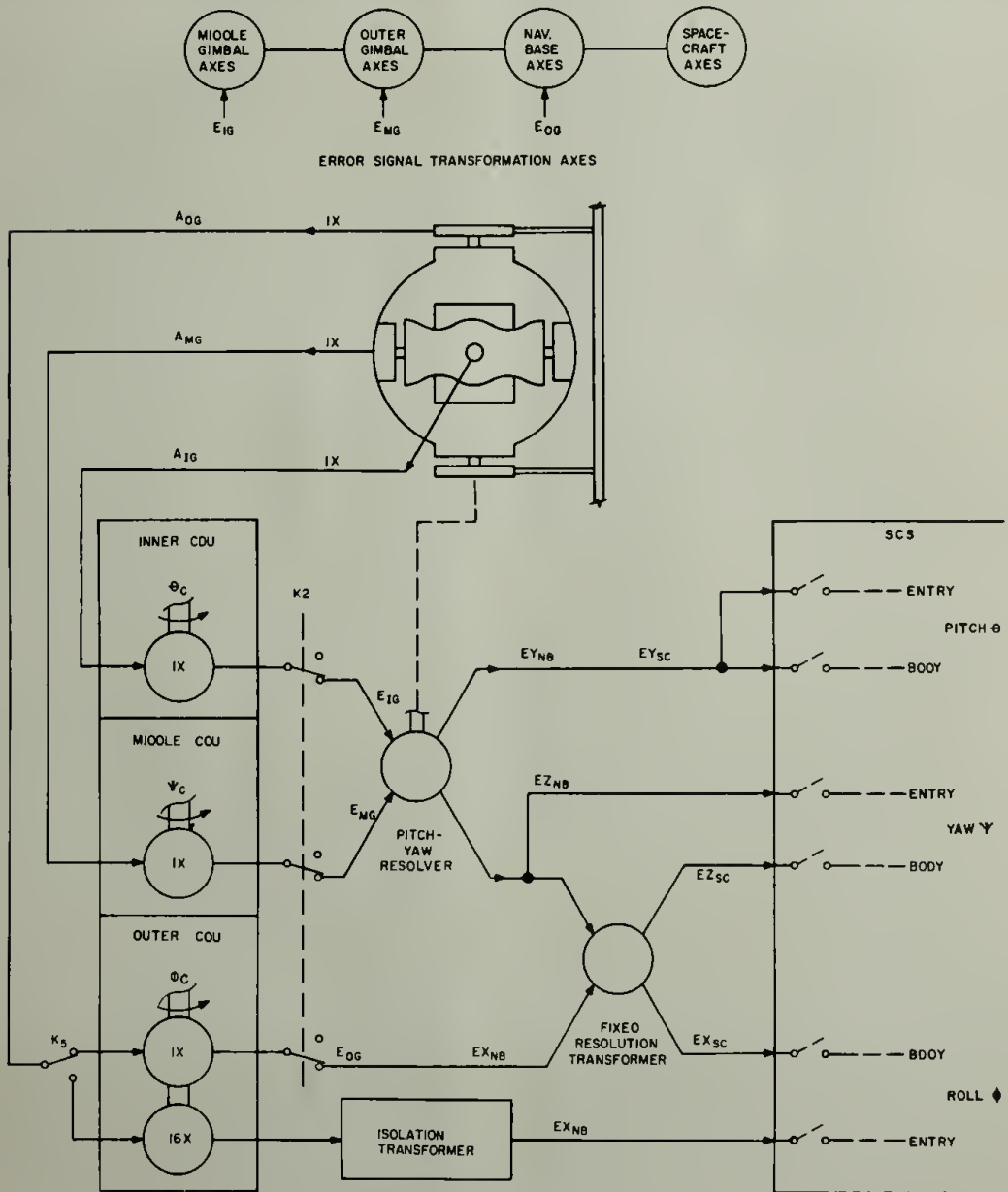
The stable member is held fixed with respect to inertial space by the stabilization loop. In essence, the spacecraft rotates about the stable member. A signal from the gimbal transmitter resolvers ( $A_{ig}$ ,  $A_{mg}$ ,  $A_{og}$ ) indicates any change in the orientation of the spacecraft with respect to an inertial frame defined by the stable member axes. The desired gimbal angles are sent into the inner, middle, and outer gimbal CDU's and are designated  $\theta_c$ ,  $\psi_c$ ,  $\phi_c$ , respectively. When the CDU angles and IMU angles are not equal, error signals  $E_{ig}$ ,  $E_{mg}$ ,  $E_{og}$  are generated. Before these error signals can be supplied to the stabilization and control system to re-orient the spacecraft, two resolutions are completed. See figure 2-16. The inner and middle gimbal error signals ( $E_{ig}$  and  $E_{mg}$ ) are resolved about the outer gimbal axis by the pitch-yaw resolver located between the outer gimbal and gimbal case. The error signals are then resolved by the fixed resolver to transform them from the nav base axes to the spacecraft axes. Once the error signals are resolved into spacecraft axes and supplied to the reaction control jets on the service propulsion engine, the motion of the spacecraft is resolved back into gimbal axes by kinematics, thus completing the attitude control loop.

**2-4.5.8 Entry Mode.** The purpose of this mode is to reduce the response time required for generating an attitude error signal in the outer CDU which controls the roll of the command module during the entry phase.

The mode is entered by one of two methods: pressing the entry pushbutton with the ISS in manual control, or AGC commanding the entry mode with the ISS in computer control. If the entry mode is entered manually, bistable relay K13 is set and holds the ISS in entry mode until reset. Whenever any other mode pushbutton is pressed, a reset command is issued. With relay K13 set, the ISS in manual control, and the IMU turned on for at least 100 seconds, relay K5 is energized and routes power to the entry lamp and issues a discrete to the AGC.

Mechanization of the entry mode is similar to machanization of the attitude control mode except that output of the IMU outer gimbal 1X resolver is switched by relay K5 to the outer CDU 16X resolver. The roll command to the stabilization and control system during entry is supplied by the outer 16X resolver. By connecting the 1X IMU resolver to the 16X CDU resolver the amount of angular rotation of the CDU shaft for a given IMU angle is reduced by a factor of 16. Therefore, when the AGC commands a roll maneuver of X degrees, the CDU is positioned at X degrees/16. This decreases the response time for roll commands. Figure 2-16 illustrates the mechanization for transforming the three CDU attitude errors into spacecraft entry axes.

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1100BA

Figure 2-16. Attitude Error Transformation

2-4.6 TEMPERATURE CONTROL SYSTEM. The temperature control system (figure 2-17) has four modes of operation to maintain the IRIG's and PIP's within their required temperature limits. The four modes of operation are auto-override, proportional, backup, and emergency. The temperature control system also contains indicating circuitry which provides monitoring signals to the telemetry.

The indicating circuitry monitors the IRIG and PIP temperatures and provides alarm indications if the temperatures exceed the allowable limits. The alarm circuit is actuated by either of two indicating bridge magnetic amplifiers and a temperature alarm magnetic amplifier.

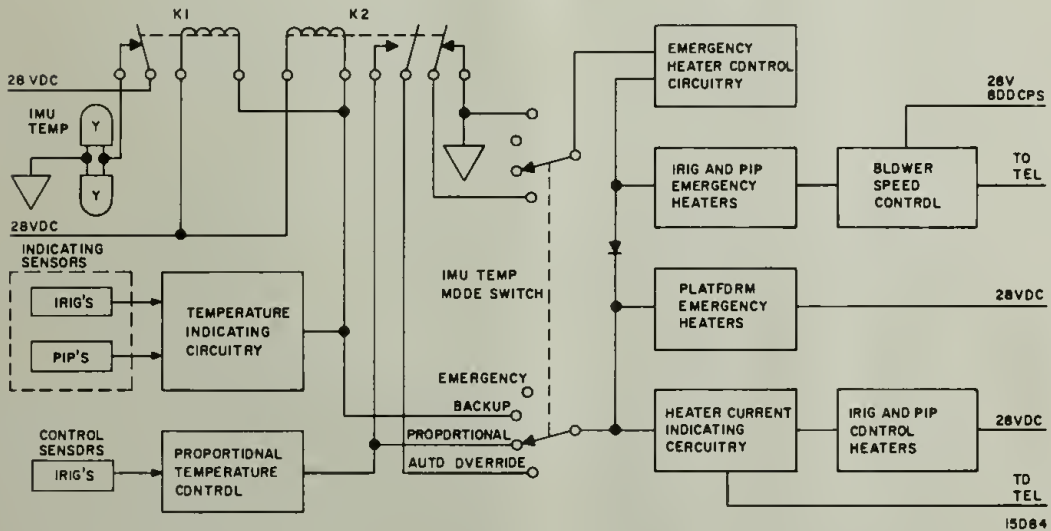


Figure 2-17. Temperature Control, Block Diagram

2-4.6.1 Auto-override Control. In auto-override, the IRIG control sensors provide heater current regulation, as long as the temperature is within tolerance. During this mode, the control heaters and emergency heaters operate in parallel to maintain the temperature. The blower speed is controlled as an inverse function of heater current



(as heater current increases, blower speed decreases). The temperature indicating sensors and circuitry provide a dc low to relays K1 and K2 (relays energized) as long as the temperature remains within tolerance. Relay K1 controls operation of the IMU FAIL light on the condition annunciator and relay K2 controls operation of the emergency heater control circuitry. When the temperature goes out of tolerance and the relays deenergize, the failure indicator lights and control of temperature is switched to the emergency heater control circuitry.

2-4.6.2 Proportional Control. Proportional control is the normal mode of operation. It functions the same as auto-override mode except that relay K2 is not in the loop to switch to the emergency mode if the temperature goes out of tolerance.

2-4.6.3 Backup Control. The backup temperature control system is less accurate than the proportional control circuit and is used only if the proportional control circuit fails. The backup mode eliminates the temperature control circuitry from the loop and uses the indicating sensors for temperature control sensors. The temperature indicating circuitry is modified so that when the temperature is below the upper temperature limit, the temperature indicating circuitry output is always a dc low. This output signal is applied to the heater control circuitry. The emergency heater control circuitry then controls the temperature regulation.

2-4.6.4 Emergency Control. The emergency control circuit is used during alarm conditions until the nature of the malfunction can be determined. The emergency control can be either automatically or manually activated. The emergency mode uses only the emergency heater and control circuitry to maintain temperature. The sensing element of the emergency temperature control circuit is a mercury thermostat located on the IMU stable member. The emergency temperature control circuit provides on-off control to the IRIG and PIP emergency heaters.

## 2-5 OPTICAL SUBSYSTEM

The OSS allows direct visual sightings to be made and precision measurements to be taken on celestial objects by means of the SCT and SXT. The angular data developed is transferred by CDU's into the AGC, which uses this data to calculate spacecraft position and trajectory. In addition, the results obtained are used to align the IMU to a star framework.

Establishment of an LOS to selected celestial targets generally requires use of the SCT and/or SXT together with spacecraft positioning controls. The astronaut changes spacecraft attitude to direct the optics field of view toward the celestial target area. Direct viewing through the wide 60 degree field of the SCT enables target search and recognition. The SXT is then used to take precise measurements. The OSS also incorporates automatic optical tracking circuitry which relieves the astronaut of maintaining star target acquisition after he has originally acquired it. The astronaut completes his measurements by obtaining landmark target acquisition.

After target acquisition the optical angular measurements and the time of sighting are transferred to the AGC. Data pertaining to the location of targets and programs for navigational calculations stored in the AGC are then compared. The results of the comparisons are used to align the IMU and determine spacecraft position and trajectory.

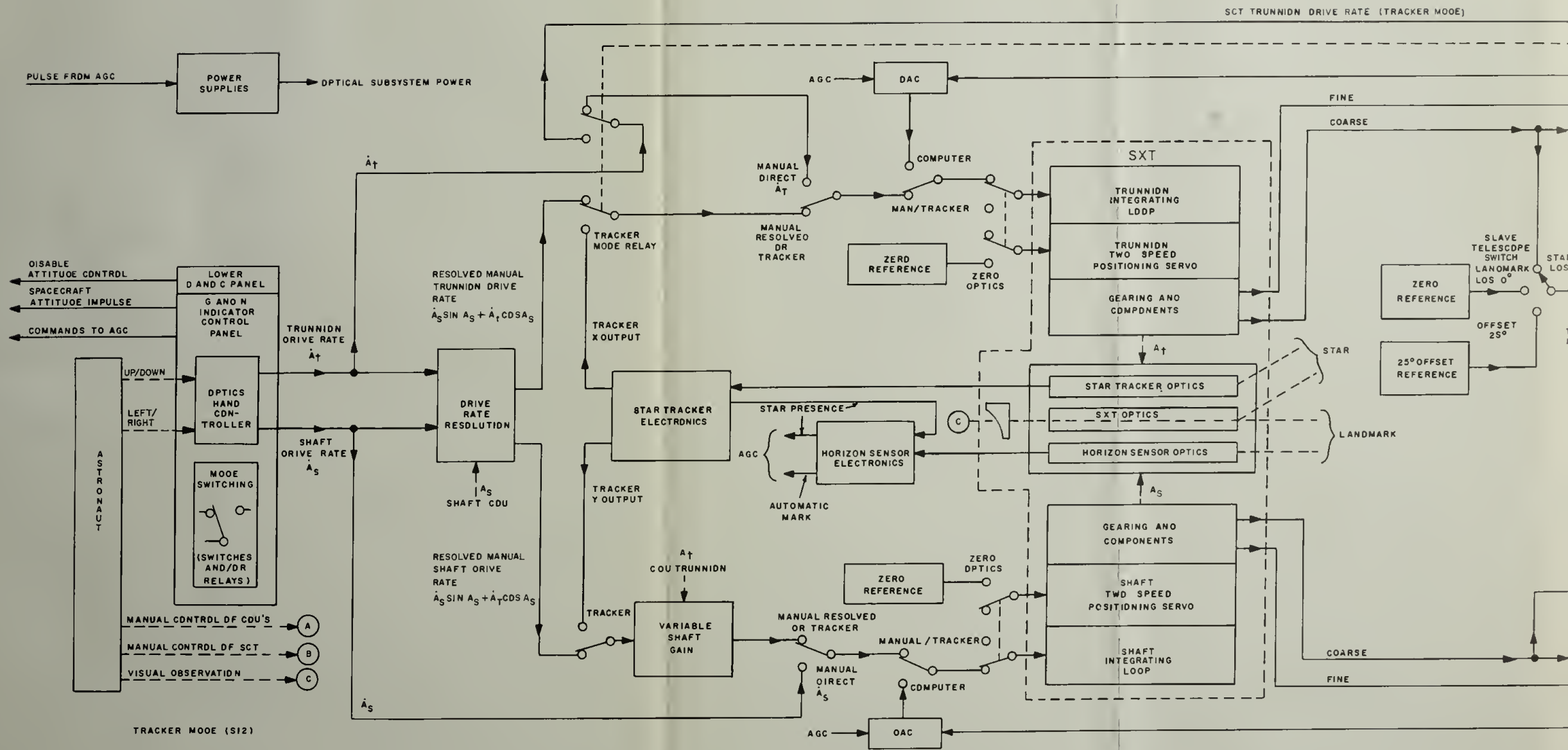
In case of a failure in the optics electronics, the astronaut can operate the SCT manually with a universal tool and read the angles off the SCT counters. In such emergencies the astronaut will calculate, with possible assistance from the ground, a navigational fix to determine position and required velocity corrections.

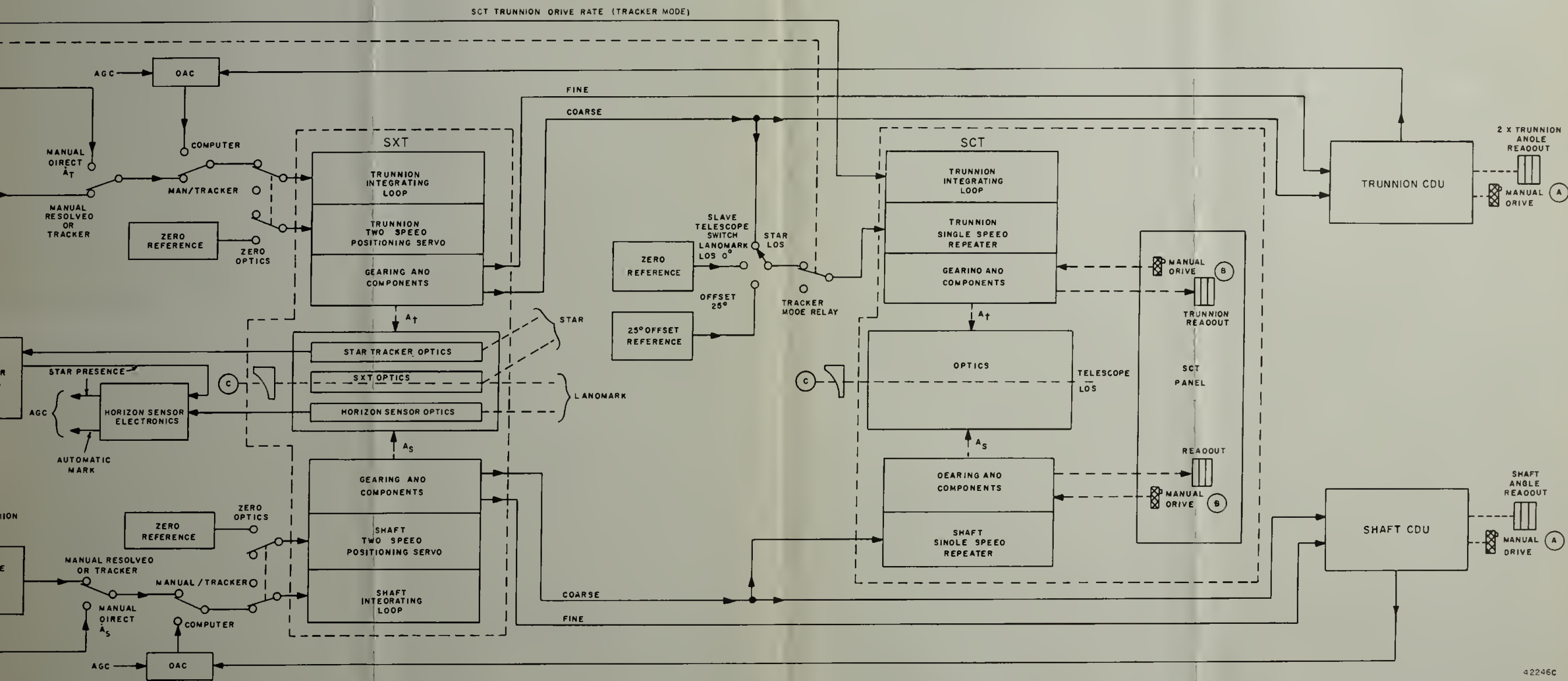
The OSS consists of an optical unit mounted on the nav base, two CDU's, portions of the G and N indicator control panel, portions of the PSA, portions of D and C electronics, portions of control electronics, and the tracker X and Y assembly. In the OSS, the CDU's are mechanized as precision repeaters and indicators. The G and N indicator control panel contains the controls and indicators that are used to establish OSS operating modes.

Figure 2-18 is a functional block diagram of the OSS. The diagram shows the flow of data for the various modes of operation selected by mode switching and the functional relationship among the various blocks. Each functional block is described in subsequent paragraphs.

2-5.1 SEXTANT. The SXT is a highly accurate, dual LOS, electro-optical instrument with 28 power magnification and 1.8 degrees field of view. It is capable of sighting two celestial targets simultaneously and measuring the angle between them with 10 arc seconds accuracy. One LOS, called landmark LOS (LLOS) is fixed along the shaft axis normal to the local conical surface of the spacecraft. The LLOS is positioned by changes in spacecraft attitude. The other LOS, called star LOS (S<sub>t</sub>LOS), has two degrees of rotational freedom about the shaft and trunnion axis. Variation about the trunnion axis is represented by movement of an indexing mirror, as shown in figure 2-19. S<sub>t</sub>LOS positioning is controlled by electro-mechanical integration loops consisting of servos, tachometers, and associated electronics. Control of the servos is determined by operating modes which are selected using G and N indicator control panel switches. The S<sub>t</sub>LOS movement is independent of the fixed LLOS. Measurements are made by first sighting into the SXT eyepiece and adjusting spacecraft attitude until the LLOS image is centered on the SXT reticle. Subsequent positioning of the S<sub>t</sub>LOS to locate the star image coincident with the LLOS is done to satisfy requirements necessary for measurements to be taken between the two images. (Coincidence must be as near the reticle center as possible.) Positioning accuracies of the SXT trunnion and shaft axes are within 10 and 40 arc seconds, respectively.

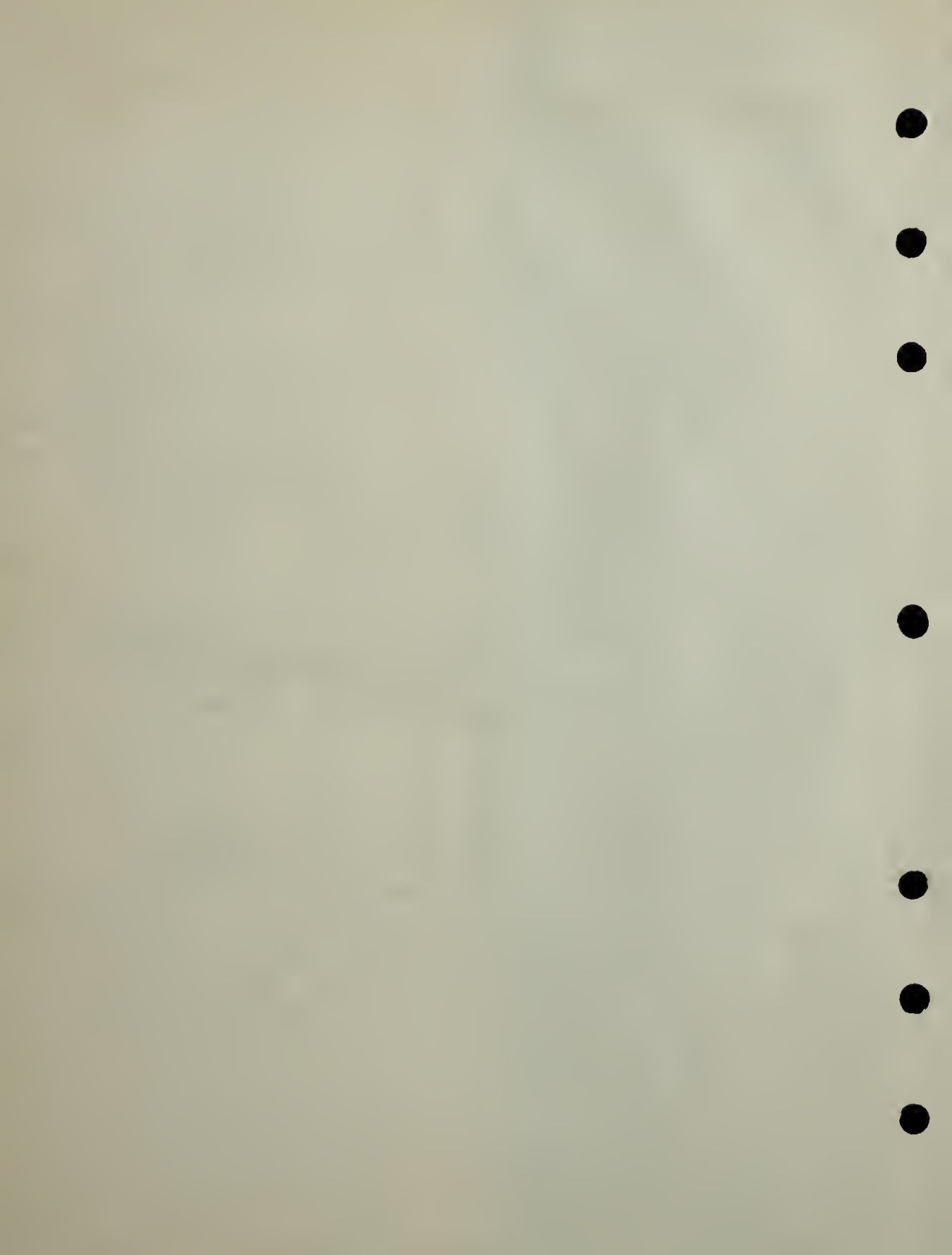
The SXT head assembly also incorporates the electro-optical star tracker and horizon sensor. The star tracker LOS is parallel to the S<sub>t</sub>LOS and is directed into the optics by a tab on the SXT indexing mirror. The horizon sensor consists of an independent optical system with an LOS parallel to that of the LLOS.

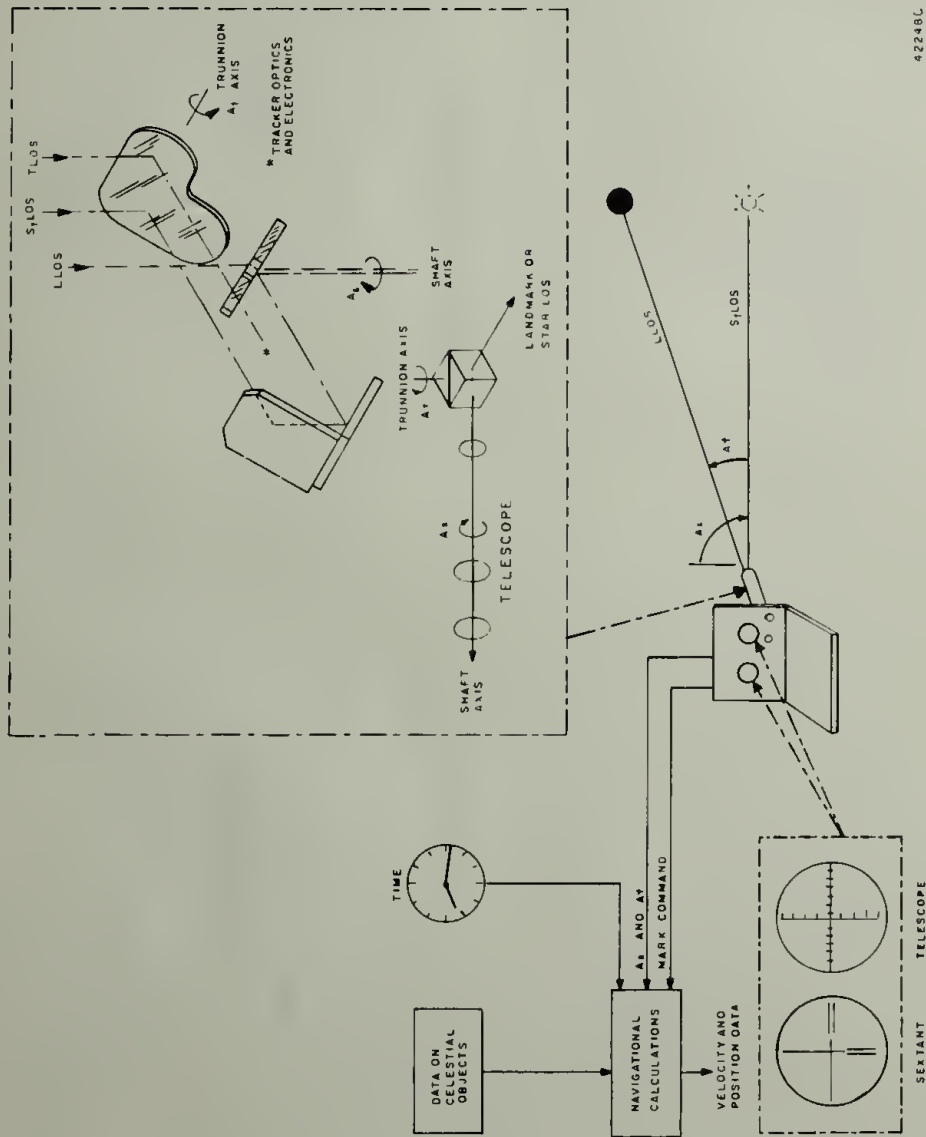




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Figure 2-18. OSS, Functional Block Diagram



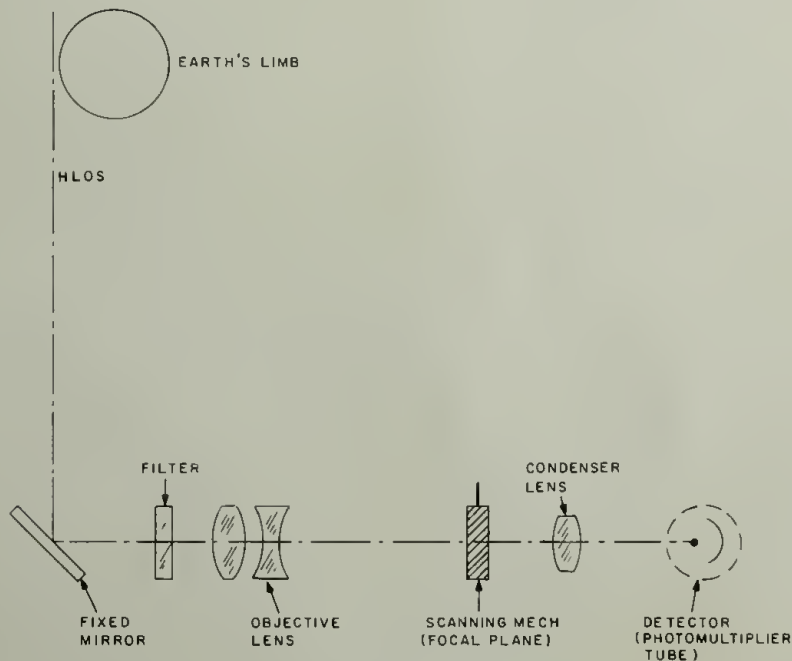


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Figure 2-19. Optical Unit Assembly, Simplified Schematic Diagram

2-5.2 HORIZON SENSOR. The horizon sensor is an electro-optical device which locates the earth's horizon by detecting 50 percent peak atmospheric illumination. The horizon sensor LOS (HLOS), like that of the SXT LLOS, is fixed parallel to the shaft axis and is positioned by reorientation of the spacecraft.

The horizon sensor optics are shown in the simplified schematic, figure 2-20. Light from the earth's limb is reflected by the mirror, collected by the objective lens, and focused at the scanning mechanism, which modulates the incoming light. The modulated light passes through the collector lens to the photomultiplier tube, which amplifies and converts the light pulses to electrical signals. After the HLOS has cycled through the earth's limb, 50 percent peak is sensed by the electronics and automatically a mark signal is provided to the AGC.



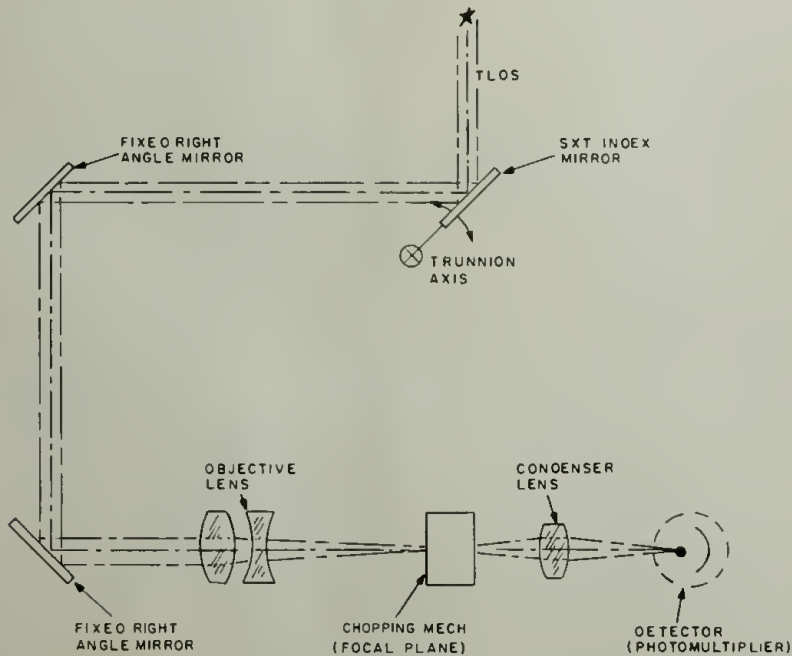
42252A

Figure 2-20. Horizon Sensor, Simplified Schematic Diagram

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2-5.3 STAR TRACKER. The star tracker (tracker) is an electro-optical device which maintains automatic star lock-on after manual acquisition of a celestial target. Since the tracker maintains star lock-on automatically, the astronaut is required only to direct and control the LLOS.

The tracker optics are shown in the simplified schematic figure 2-21. A portion of the light from the star is introduced into the tracker optical path by the SXT indexing mirror side tab. The star light is reflected by the tab and directed into the fixed right angle mirrors. The objective lens receives the reflected light and serves to focus it into the scanning mechanism. The condenser lens collects the modulated scanning mechanism output and introduces it into the detector photomultiplier tube.



42253B

Figure 2-21. Star Tracker, Simplified Schematic Diagram



The dual tuning fork scanning mechanism brackets the focal plane created by the objective lens. Two aperture plates mounted to the tuning fork tines modulate the light as the tines vibrate across its path. The electronics section utilizes the modulated signal received from the detector tube for star presence and position data. X and Y axis error signals are generated and fed into the SXT mechanization loops. This nulls the servos which serve to maintain target lock-on.

2-5.4 SCANNING TELESCOPE. The SCT is a single LOS, refracting type, low power instrument with 60 degrees instantaneous field of view. The SCT wide field of view is used for general celestial viewing and recognition of target bodies for sighting setups and measurements. In addition, it is used to track landmark points during earth and lunar orbits.

The SCT has two axes of rotational freedom (see figure 2-19), defined as the shaft and trunnion axes. Rotation about the shaft axis defines increments of shaft angle movement ( $A_s$ ). Rotation about the trunnion axis defines increments of trunnion angle movement ( $A_t$ ).

The prime element of the SCT is a double dove prism, (prism), mounted in the head assembly. The prism introduces the target image into the SCT optical system. The prism is positioned about the two axes interpreted in  $A_s$  and  $A_t$ . Mechanically, this is accomplished by rotation, through a differential, of the complete head assembly and driving of the prism on its mount. A differential gearing system enables independent positioning of  $A_s$  and  $A_t$ . The independent positioning enables the LOS established through the prism to traverse within the following limits: zero degrees (parallel to shaft axis) to  $\pm 60$  degrees in  $A_t$  elevation, unlimited 360 degrees in  $A_s$ . When the SCT is slaved to the SXT, rotation is limited to 270 degrees due to limit stops along the SXT shaft axis. Due to obstructions created by aperture limitation in the spacecraft frame, the LOS along the trunnion axis has a useful range of approximately 58 degrees. Therefore, the aggregate maximum field that can be viewed by rotating the trunnion and shaft within their respective limits is 116 degrees.

The optics hand controller controls the shaft and trunnion drive rates. The drive rates are integrated by SXT servos which position the SCT LOS. The shaft and trunnion angles can be read directly from the SCT by counters mounted in the face of the optical panel.

2-5.5 SEXTANT TRUNNION INTEGRATING LOOP. The SXT trunnion servos control rotation of the SXT indexing mirror. These servos function as an integrating loop in all modes of operation except zero optics and star tracker modes. The loop is a resolver system with a 1/64 revolution electrical null point accuracy. The loop integrates the drive rate input and causes the SXT indexing mirror to rotate at a corresponding angular velocity.

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2-5.6 SEXTANT TRUNNION POSITIONING SERVO. In zero optics mode, the SXT trunnion integrating loop is converted to a two-speed, shaft positioning servo. This is accomplished by the zero optics relays which connect the 1X and 64X resolvers into the loop as position sensing devices. The error voltage outputs from these resolvers are fed to motor drive amplifiers through a two-speed switch. The zero optics relays reconnect the tachometer generator feedback from direct to compensated feedback. The servo continues to drive until the mechanical shaft is aligned to the electrical zero reference. In zero position, the LLOS is parallel to the SLOS.

2-5.7 SEXTANT SHAFT INTEGRATING LOOP. The SXT shaft servos control rotation of the complete head assembly. These servos function as an integrating loop in all modes of operation except zero optics and star tracker modes. The loop is a resolver system with a 1/16 revolution electrical null point accuracy. The loop integrates the drive rate input and causes the SXT optics to rotate at a corresponding angular velocity.

2-5.8 SEXTANT SHAFT POSITIONING SERVO. In zero optics mode, the SXT shaft integrating loop is converted to a two-speed, shaft positioning servo. This is accomplished by the zero optics relays which connect the 1/2X resolvers into the loop as position sensing devices. The error voltage outputs from these resolvers are fed to motor drive amplifiers through a two-speed switch. The zero optics relays reconnect the tachometer-generator from direct to compensated feedback. The servo drives until the mechanical shaft is aligned to the electrical zero reference. In zero shaft position, the split reticle crosshairs are positioned at 90 and 180 degrees.

2-5.9 DRIVE RATE RESOLUTION CIRCUIT. The purpose of this circuit is to resolve the optics hand controller drive rates so that the image motion in the eyepiece (up-down and left-right) is independent of the shaft angle. Without this resolution, the direction in which the image would move in response to the optics hand controller would vary and depend upon the shaft angle. The drive rates are routed through the resolution circuit by resolved manual mode switching which is controlled from the G and N indicator control panel. The resolution is accomplished by a resolver contained in the shaft CDU.

2-5.10 VARIABLE SHAFT GAIN CIRCUIT. To assist in taking optical sightings, the image motion rate, (up-down or left-right), produced in the eyepiece must be constant for a given rate input from the optics hand controller. Since the trunnion angle affects this rate, a computing resolver in the trunnion CDU and a cosecant function generator are used to modify the image motion rate so that it is independent of the trunnion angle. The shaft gain circuit affects shaft drive rate only and is connected to the optics hand controller output by switching optics into the resolved manual or tracker mode.

2-5.11 TELESCOPE SHAFT REPEATER. The SCT shaft servo is a single-speed, repeater servo which continuously senses the SXT shaft position and movement. The SCT shaft servo input signal is the coarse resolver output signal from the SXT shaft servo. The SCT shaft angle, therefore, is always slaved to the SXT shaft servo. The gear train also drives a mechanical angle counter which may be read out from the optical panel to the left of the SCT eyepiece. Direct manual drive to the gear train is provided by a manual input adapter.

2-5.12 TELESCOPE TRUNNION INTEGRATING LOOP CIRCUIT AND REPEATER. The SCT trunnion servo may function as an integrating loop or a single-speed repeater depending on mode switching. In the tracker mode, the servo operates as a rate or integrating device for the trunnion rate input ( $A_t$ ) from the optics hand controller.

When the SLAVE TELESCOPE selector is set to either  $0^\circ$  OFFSET or  $25^\circ$  OFFSET positions, the SCT repeater is disconnected from the master system. The SCT repeater input is connected to a transformer which provides, as a zero reference, a fixed  $25^\circ$  electrical offset signal. The positioning of the SCT, therefore, during  $0^\circ$  or  $25^\circ$  offset is independent of the position of the SXT master servos.

2-5.13 CDU LOOP CIRCUIT. The optics CDU's are functionally the same as the IMU CDU's except that the SXT trunnion and shaft servos operate as masters for the trunnion and shaft CDU's respectively. The slaving of the CDU's to the SXT servos takes place during all modes of operation.

2-5.14 MODES OF OPERATION. The OSS incorporates multiple modes of operation to facilitate the taking of precise measurements within short time increments. The specific mode selected effectively adapts the system to fit the needs of the astronaut under varying situations prior to sightings. The OSS operates in one of four prime modes and can be controlled in either of two control modes. Each is selected by switching in the G and N indicator control panel. The principal modes are:

- (1) Zero Optics /  $25^\circ$  Offset
- (2) Manual
- (3) Tracker
- (4) Computer.

To aid in understanding OSS operation and resultant effects while viewing through the SCT and SXT eyepieces, the following paragraphs discuss each of the modes relative to hypothetical situations depicted in illustrations of image movement versus reticle position.

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2-5.14.1 Zero Optics / 25° Offset Mode. In zero optics, mode relays convert the SXT trunnion and shaft loops into each of the two speed null sensing servos. The positioning servos then drive the SXT optics into alignment with zero reference inputs. This mode of operation is normally established as a part of a preliminary procedure for taking optical sightings.

Entering the zero optics mode causes the bank of SXT input relays to disconnect the SXT loops from all data source drive rate inputs. This switches in zero alignment reference inputs, and serves to mechanize each loop as a positioning servo. (See figure 2-22.)

In the SXT trunnion loop, the 1X and 64X resolver transmitter outputs are switched back to the loop MDA by a two-speed switch. These resolver output signals terminate at zero optics relay contacts whenever the loop functions as an integrating device with rate inputs. In zero optics mode, the relay contacts close and apply the output signals to a two-speed, coarse-fine switch. The resolvers are mechanized as control transformer error detectors for the trunnion integrating loop circuit and generate error signals proportionate to the displacement of the mechanical shaft from the electrical zero reference. These error signals are used to drive the mechanical shaft until it is precisely aligned to the zero reference. The zero optics relay also reconnects the tachometer generator from direct to compensated feedback so that the servo characteristics assume those of a positioning servo.

The SXT shaft integrating loop is mechanized identically to that of the trunnion loop. In the SXT loop the 1/2X and 16X resolvers serve as error detectors for the two-speed, shaft positioning servo.

When the landmark target is centered on the SCT reticle the maximum range for locating a star target is limited to approximately 25°. To afford a viewing area compatible to the SXT included  $A_t$  capability (50°), an SCT  $A_t$  25° offset has been provided. In effect the SCT trunnion angle is displaced 25 degrees, placing the landmark target at the edge of the field of view. Proportionately, the viewing range for locating a star is increased to approximately 50 degrees.

2-5.14.2 Manual Modes. In manual modes of operation the direction and rate of image motion viewed on the SCT and SXT eyepieces are manually controlled. There are two manual modes: the direct mode and the resolved mode. The direct manual mode permits image movement in a coordinate system, while the resolved manual mode permits independent movement of the image coordinates relative to a rectangular system.

The optics hand controller and speed selector on the G and N indicator control panel are used for manually acquiring the landmark and star targets. Displacement of the optics hand controller generates SXT trunnion and shaft angular drives ( $A_t$  and  $A_s$ ).

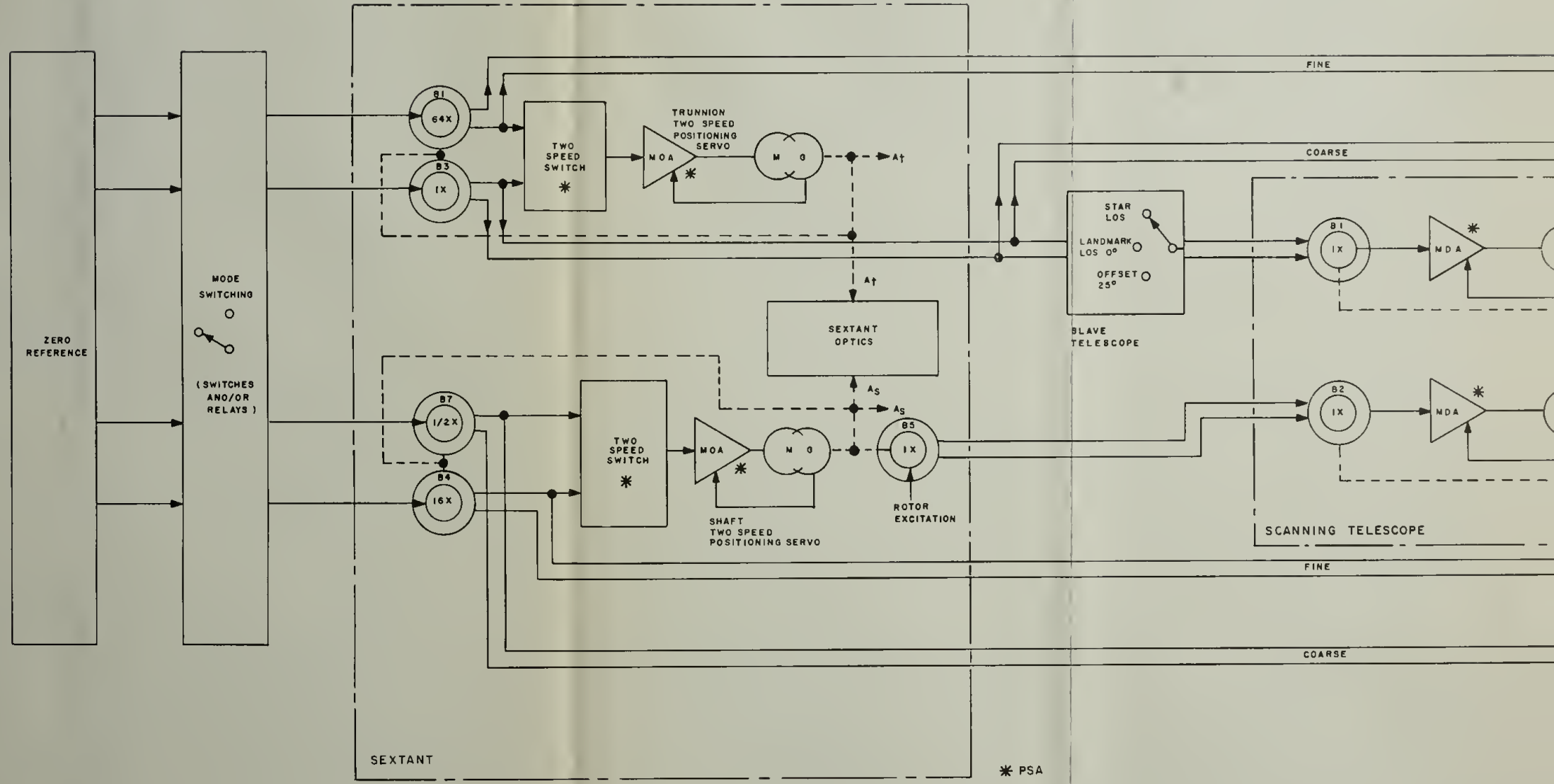
The manual input directly controls the SXT trunnion and shaft servos. Resolver transmitters driven by these servos transmit positional information to each of the two-speed CDU trunnion and shaft servos, as well as to the single-speed trunnion and shaft servos in the SCT. By this means, the CDU and SCT are both slaved to the SXT. The image motion may also be observed through the SCT eyepiece. The trunnion and shaft angles can be read out at the counters on the CDU panel.

In manual modes, the SXT trunnion and shaft servo loops function as rate servos which rotate the SXT optics in a direction and rate proportional to the manual displacement of the optics hand controller and speed selector. Rotation continues until the command signals are manually discontinued. The optics hand controller is spring loaded and, when released, removes the command error signals and causes the servos to stop. The optics remain in the new position until new drive rate error signals are introduced.

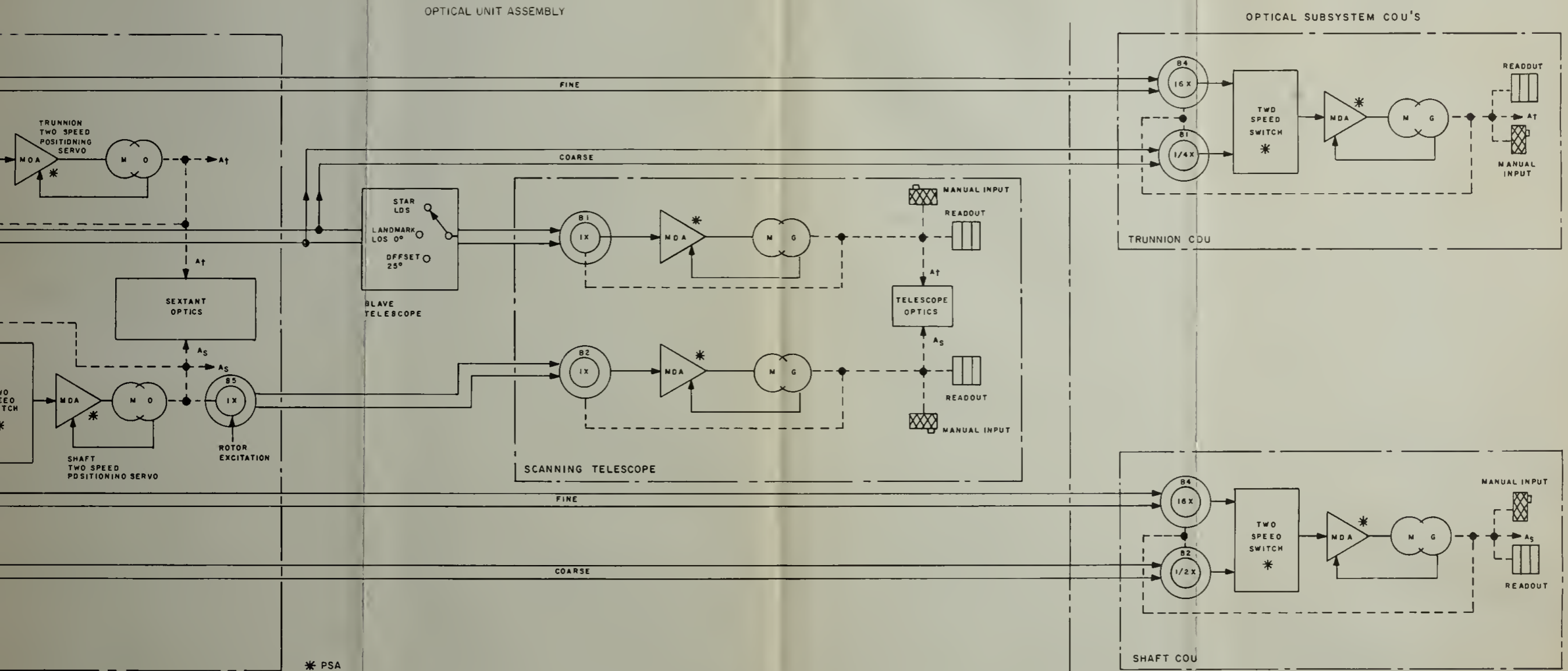
2-5.14.2.1 Direct Manual Mode. Figure 2-23 illustrates the direction of image movement as viewed in the SCT and SXT eyepieces using the optics hand controller in the direct manual mode. For purposes of description, the typical image presentations of figure 2-23 are discussed by position numbers as follows:

- (1) Position 1. A landmark target is selected by manipulation of spacecraft attitude controls and centered on the reticle. The star target at this point is not in the SCT field of view.
- (2) Position 2. By setting in the  $A_t 25^\circ$  offset, as previously mentioned, the landmark target is displaced to the edge of the SCT field of view. The selected star target is now positioned in the field of view.
- (3) Position 3. The SCT reticle is displaced in  $A_s$  to align the star image on the reticle reference line. The included angle between landmark and star image, as measured on the reticle reference line, must be less than  $50^\circ$  in order to maintain images in the SXT reticle.
- (4) Position 4. When viewing in the SXT eyepiece, both landmark and star images now appear in the field of view. The star image may appear to be misaligned with respect to the shaft axis reticle reference.
- (5) Position 5. Fine alignment of the star image with the  $A_s$  reticle reference is accomplished by positioning the optics hand controller.
- (6) Position 6. The star image is displaced in  $A_t$  toward the center of the landmark target aligned on the center of the reticle.
- (7) Position 7. Super-imposition of the star target on the landmark target is accomplished and the MARK button depressed.

OPTICAL UNIT ASSEMBLY

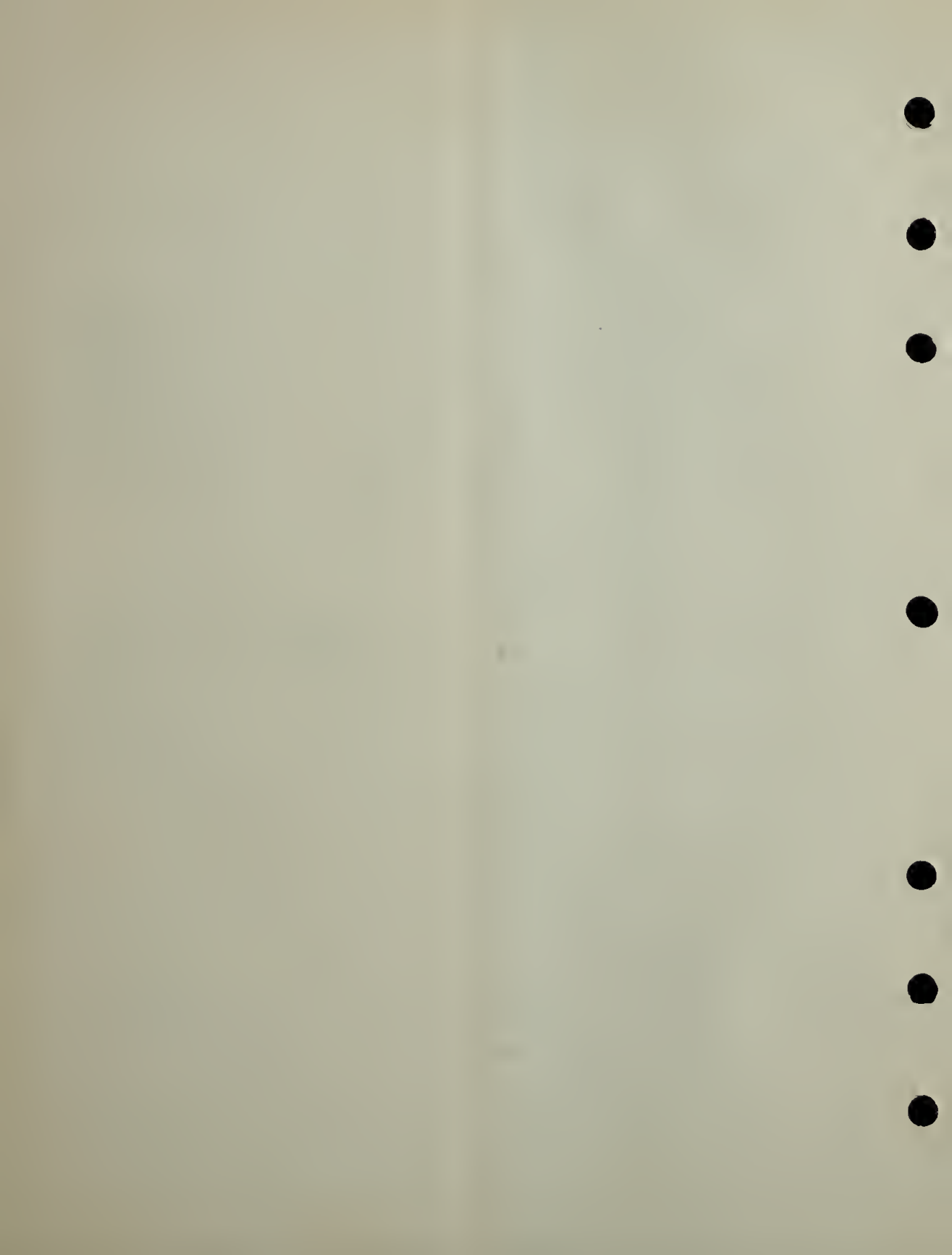


APOLLO GUIDANCE AND NAVIGATION SYSTEM

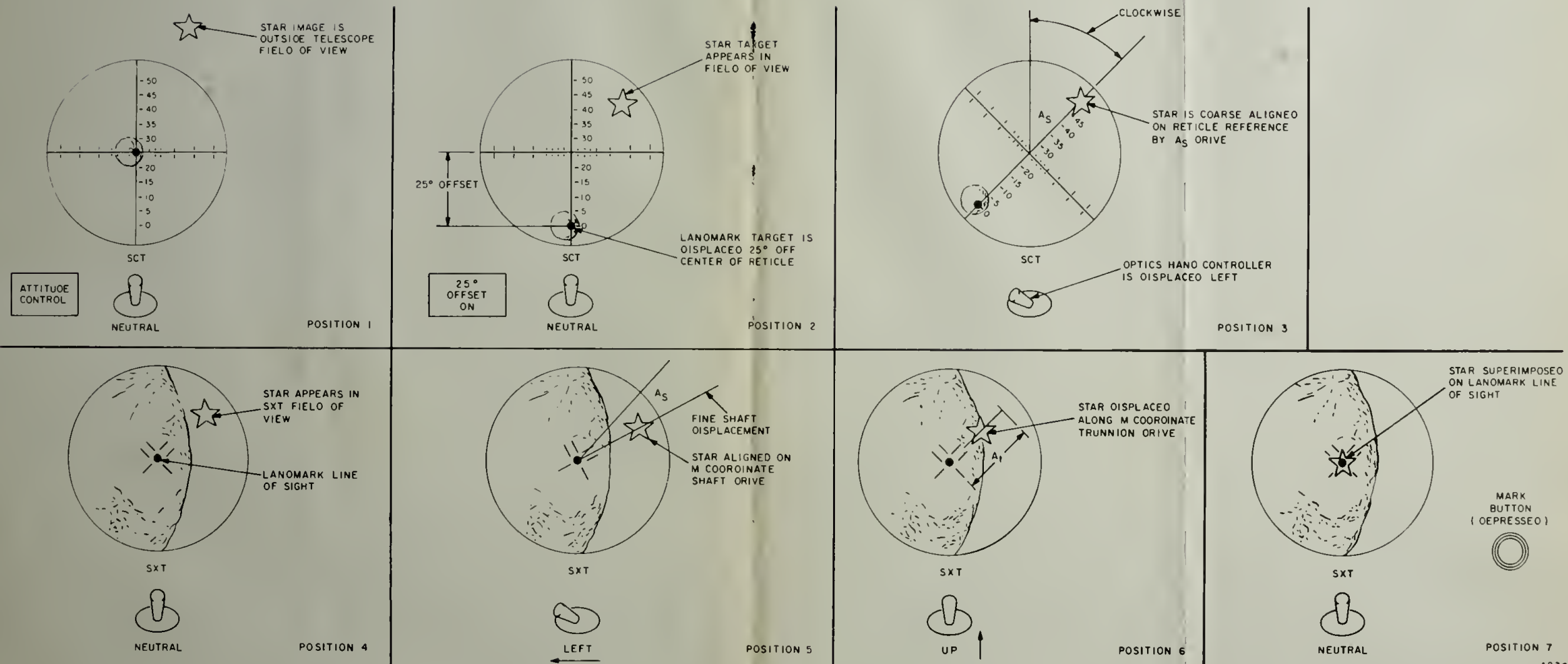


422508

Figure 2-22. Optics Positioning Loops, Zero Optics Mode

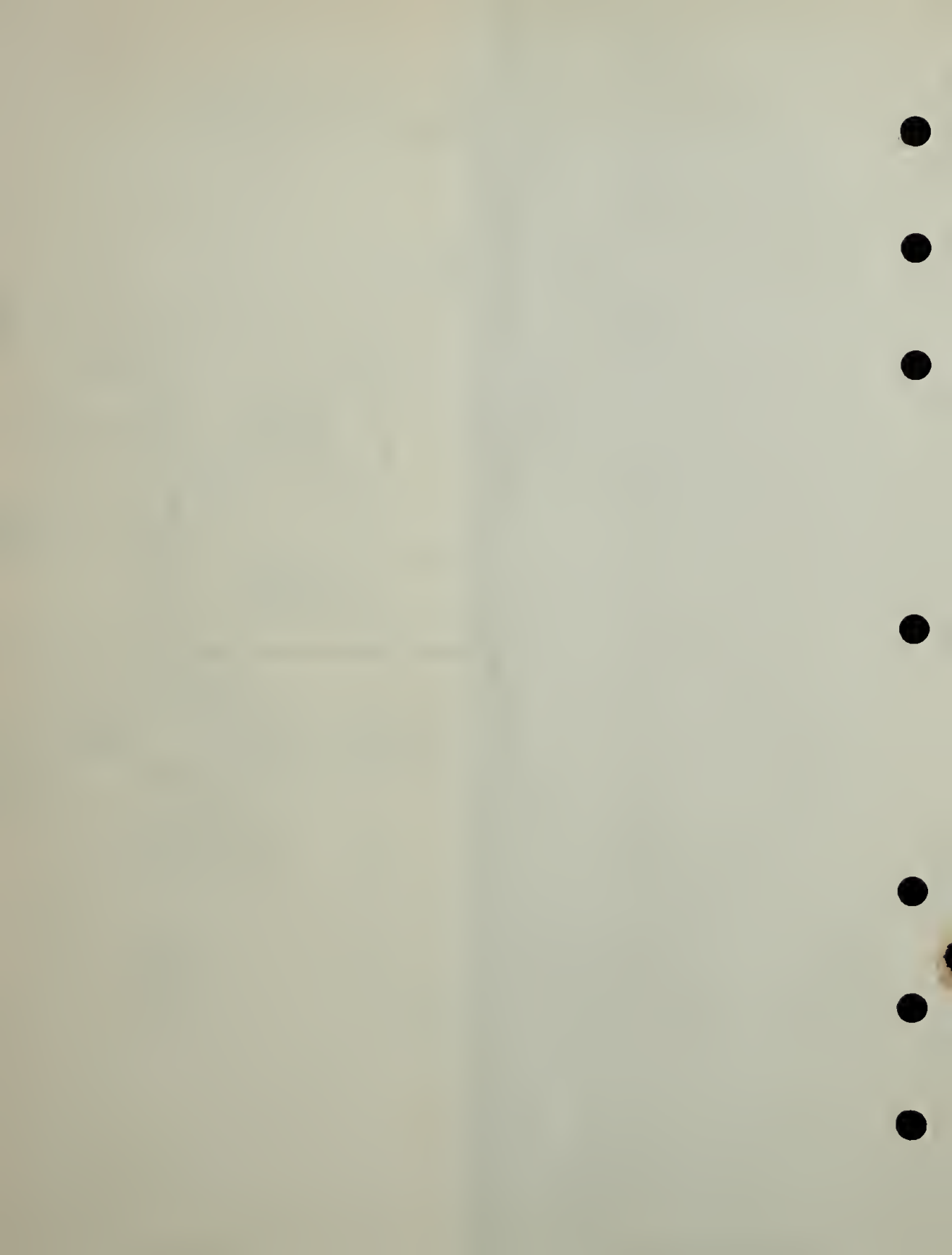






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Figure 2-23. Image Presentations, Direct Manual Mode



APOLLO GUIDANCE AND NAVIGATION SYSTEM

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In direct manual mode, the SXT trunnion and shaft servos are mechanized as rate integrating servo loops. (See figure 2-24.) The trunnion and shaft angular drive rate signals ( $A_t$  and  $A_s$ ) are fed through switching relays directly into the MDA's of their respective servos.

The trunnion drive rate signal ( $\dot{A}_t$ ) causes the trunnion servo, located in the SXT optics, to drive the SXT indexing mirror around the trunnion axis in a direction and at a rate proportional to the direction and displacement of the optics hand controller. Similarly, the shaft drive rate signal ( $\dot{A}_s$ ) causes the shaft to rotate the entire SXT optics around the shaft axis.

2-5.14.2.2 Resolved Manual Mode. Figure 2-25 illustrates the direction of image movement in the SXT eyepiece using the optics hand controller while in resolved manual mode. For purposes of description, the typical SXT image presentations of figure 2-25 are discussed by position numbers, as follows:

(1) Position 1. With the landmark and star images coarse aligned by the SCT, both targets are presented in the SXT reticle. At this point, the image is not aligned with the SXT reticle.

(2) Position 2. When the optics hand controller is positioned up-down or left-right, the image movement appears to follow or is coordinated with controller motion. In this particular operation the controller is positioned downward and the image is displaced in that direction.

(3) Position 3. With the star target to the right of the landmark the hand controller is displaced left and the image movement follows.

(4) Position 4. This presentation depicts the star target superimposed on the landmark target. At this time the MARK button is depressed and the sighting completed.

In resolved manual mode, the SXT trunnion and shaft servos are mechanized as rate or integrating loops. Drive rate resolution and variable gain is added to the shaft servo loops to make the rate and direction of the image motion independent of the shaft axis and trunnion angle. (See figure 2-26.)

Switching relays direct the drive rate signals (up-down and left-right) from the optics hand controller to two resolver drive amplifiers (RDA). The up-down signal is amplified by one RDA and applied to one rotor winding of the 1X resolver in the CDU shaft servo. The left-right signal is amplified on the second RDA and applied to the other rotor winding. The rotor of the 1X resolver is positioned to the shaft angle ( $A_s$ ). The voltages induced in the stator windings are a function of the two rotor input voltages and the shaft angle. The R and M coordinates drive rate signals are resolved by the 1X

resolver into shaft and trunnion signals which are then fed to the respective motor drive amplifiers. This servo causes the SXT indexing mirror to rotate around the trunnion axis at a rate and direction proportional to the drive rate signal causing the image to move up or down. In the SXT trunnion gear train, a coarse/fine (1X/64X), resolver transmitter pair feeds the 1/4X and 16X resolver control transformers in the CDU trunnion servo. This action slaves the CDU trunnion servo to the SXT trunnion servo.

The left or right drive rate signal from the 1X resolver in the CDU shaft servo is fed to the SXT shaft servo through a cosecant amplifier which is positioned in the input circuit by switching relays. This amplifier functions as a variable gain device between trunnion angles of 10 to 60 degrees. The amplifier employs a 1/2X computing resolver in the CDU trunnion servo as a minor loop. The effect of this cosecant generator is to make the rate of image motion (angular velocity) independent of changes in trunnion angle, by decreasing the shaft speed as trunnion angle increases. The reduction in shaft speed enables a constant rate of trunnion peripheral velocity to be achieved regardless of trunnion angle. This insures that the optics LOS does not sweep past the target before recognition.

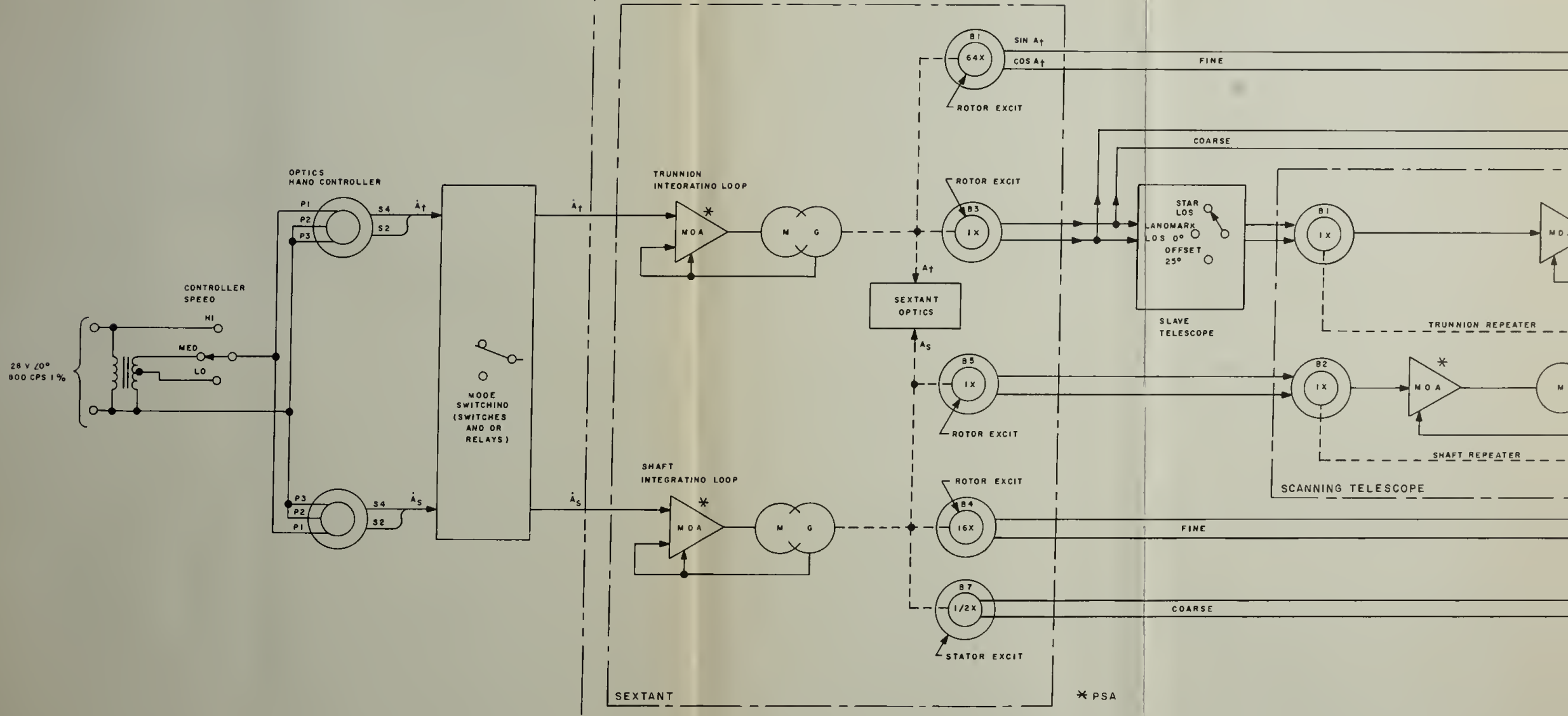
One input to the summing network of the cosecant function generator is the drive rate along the Y axis, which is obtained after resolution by resolver B3 in the CDU shaft servo. The motion along this axis increases at a rate proportional to the sine of the trunnion angle ( $A_t$ ). To compensate for this effect, an inverse sine factor (the cosecant) is introduced. A computing resolver in the CDU trunnion gear train is employed to yield the function  $0.5C \sin A_t$  to compensate for the gear train ratio. The controlled electrical variable (C) drives the SXT shaft integrating loop so that its angular velocity is independent of the trunnion angle. In this way, a uniform sweep rate along the Y axis is achieved throughout the range of trunnion angles. The resolution of the drive rates onto the Y axis is used as a direct input to the shaft integrating servo loop.

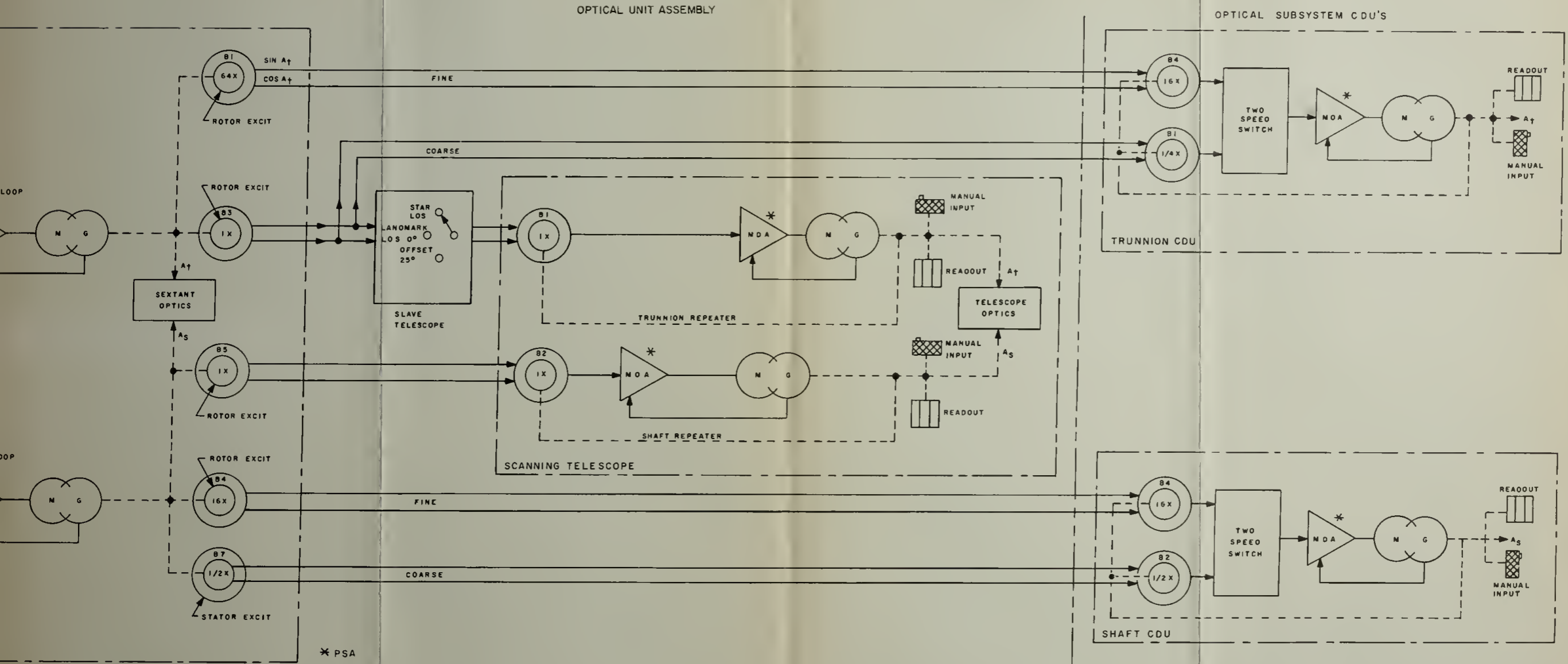
2-5.14.3 Tracker Mode. In the tracker mode, the star tracker (tracker) controls the SXT optics positioning loops after the initial star acquisition has been achieved. The outputs of the tracker are two position error signals, one along the X axis and the other along the Y axis. (See figure 2-27.) These outputs are similar to the manual resolved drive rate outputs from the optics hand controller in resolved manual mode. The tracker senses the direction of star image drift from star tracker null and generates drive position signals in the SXT integrating loops. The drive rate error signals reposition the star image onto the star tracker null.

2-5.14.3.1 Star Tracker. The tracker includes an optical system and scanner, a photomultiplier tube, and associated electronics. The star light is collected and focused by the optics onto the scanning mechanism, which consists essentially of two vibrating tuning forks with rectangular slit type apertures. The apertures of the tuning forks are mutually perpendicular and their null center defines the coordinate system of the star tracker. Each tuning fork resonator is driven by a precisely controlled oscillator. An electromagnetic pickup for each fork assures precision control of oscillator frequencies and maintains constant amplitude of vibration.

G AND N INDICATOR CONTROL PANEL (CONTROLS)

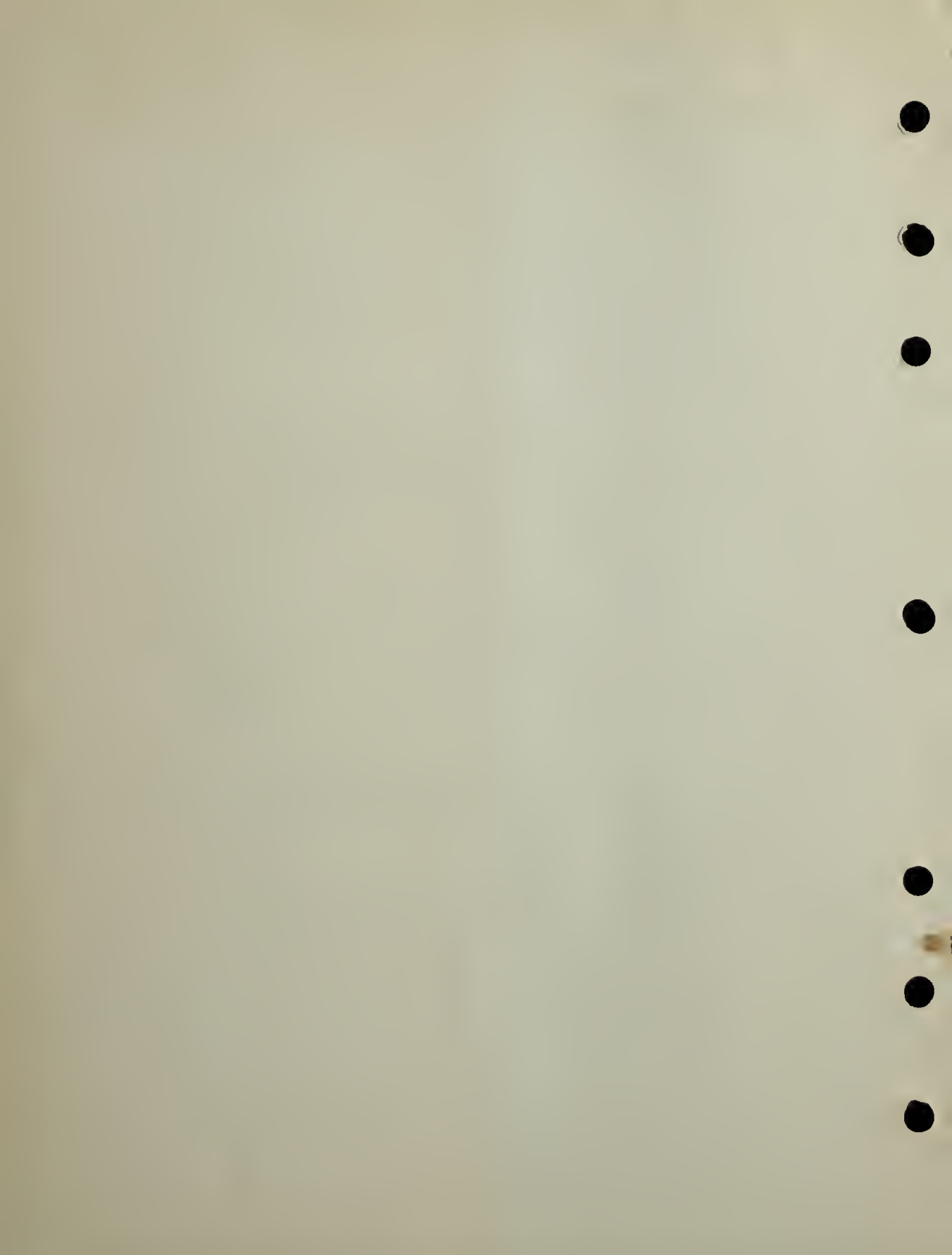
OPTICAL UNIT ASSEMBLY





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Figure 2-24. Optics Positioning Loops, Direct Manual Mode



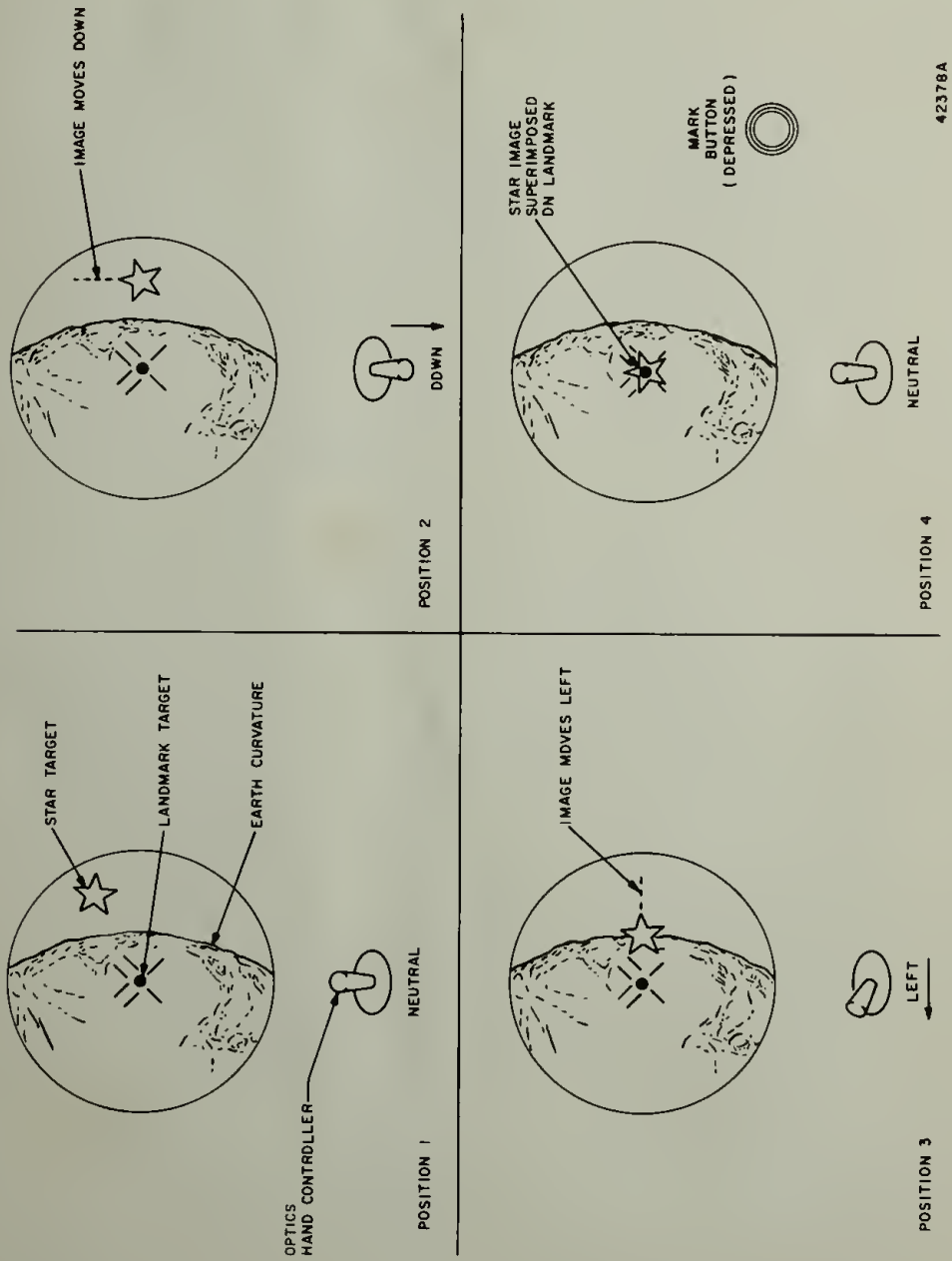


Figure 2-25. Image Presentations, Resolved Manual Mode



One tuning fork vibrates at a slightly different frequency from the other. The star flux, entering the tracker optics, is scanned by a 7 by 9 Lissajous pattern. This aids accuracy as well as precision error detection. The photomultiplier tube is a transducer which converts the modulated light from the scanner into corresponding electrical pulses. The tracker electronics, which contains narrow band amplifiers, demodulators, modulators and comparator networks, receives the photomultiplier output. The signals received are filtered to extract noise and unwanted harmonics; amplified and demodulated. The signal is then modulated for interpretation of its positioning intelligence in a form consistent with the excitation frequency of the servo loops. The resultant is fed to the excitation frequency of the tuning forks. If the image is not at star tracker null, an output is generated in proportion to the error displacement with directional intelligence (phase). This is fed to the servo loops through MDA's as X and Y drive position error signals. This serves to position the SXT in  $A_S$  and  $A_t$  as necessary for tracker null, thereby sustaining target lock-on.

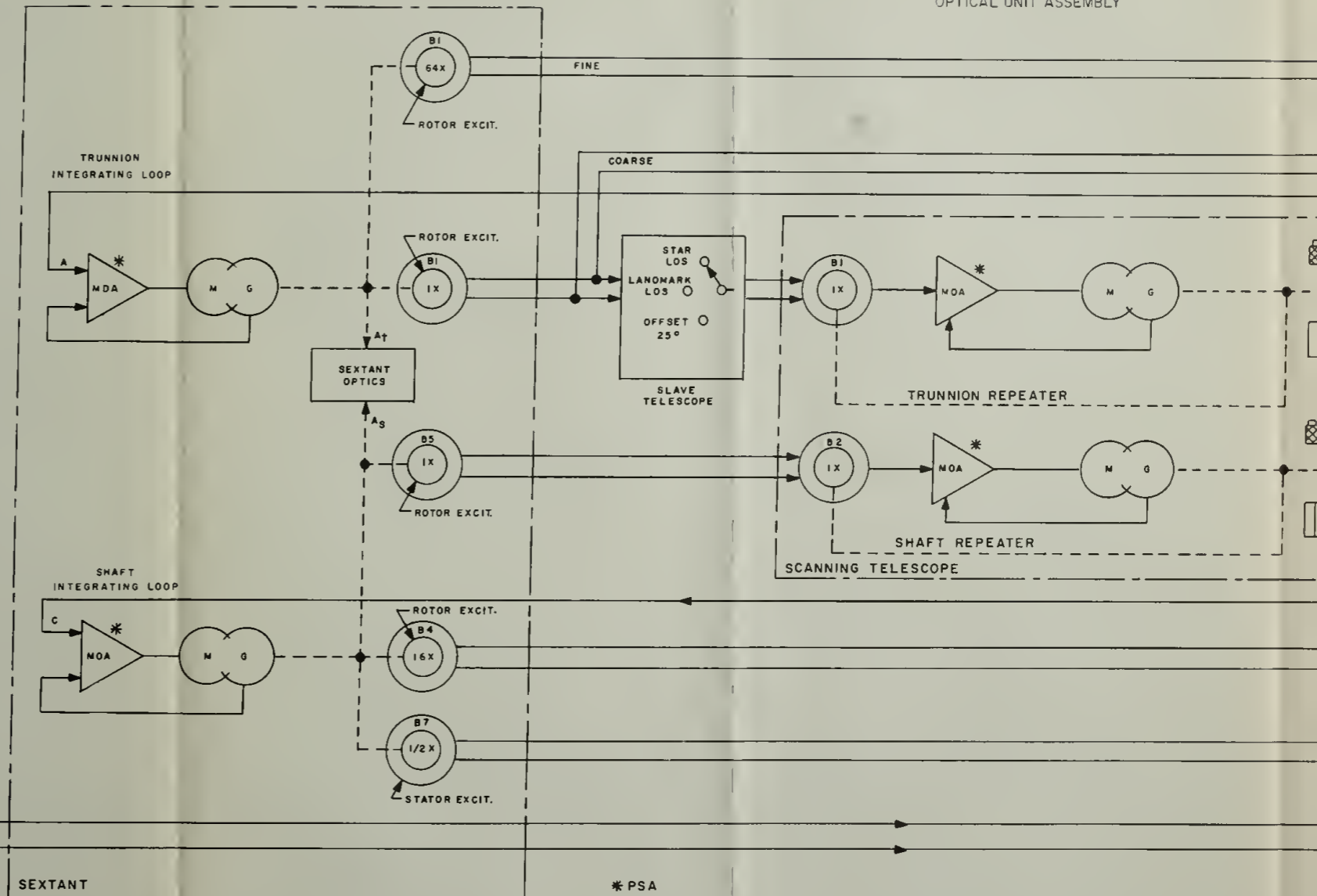
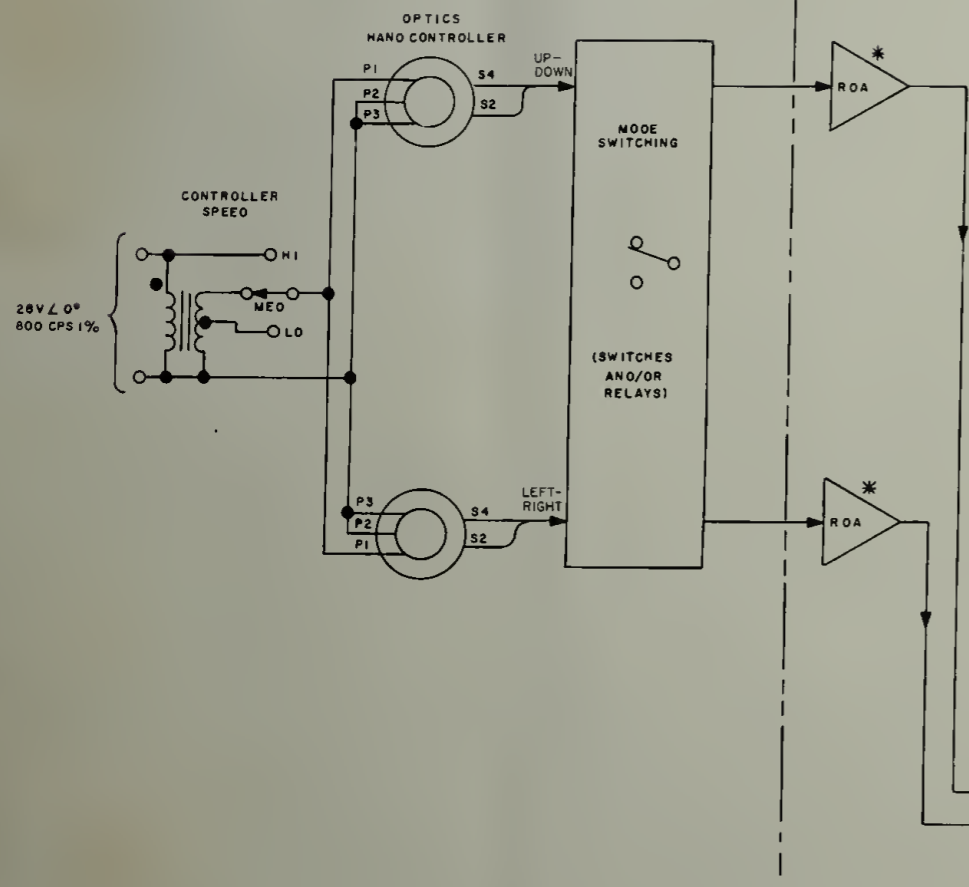
The tracker also incorporates circuits which control the photomultiplier sensitivity in proportion to light magnitudes sensed through SXT optics. This circuit generates an automatic gain control signal which regulates the power supply input. This in effect varies the sensitivity of the photomultiplier and assures uniform output when sighting stars of various magnitudes. This circuit also notifies the AGC by supplying a signal indicating star presence in the star tracker field of view.

2-5.14.3.2 Sextant Shaft and Trunnion Servo Loop. The X and Y outputs from the star tracker drive the SXT shaft and trunnion servo loops. The Y output drives the SXT shaft servo loop through the cosecant function generator. The outputs of the star tracker are referenced to the rectangular X and Y coordinate system. Cosecant attenuation to the SXT shaft servo loop is accomplished by mode switching. Mode switching interposes the cosecant function generator in the input line from the star tracker Y output to the SXT shaft servo loop. (See figure 2-27.)

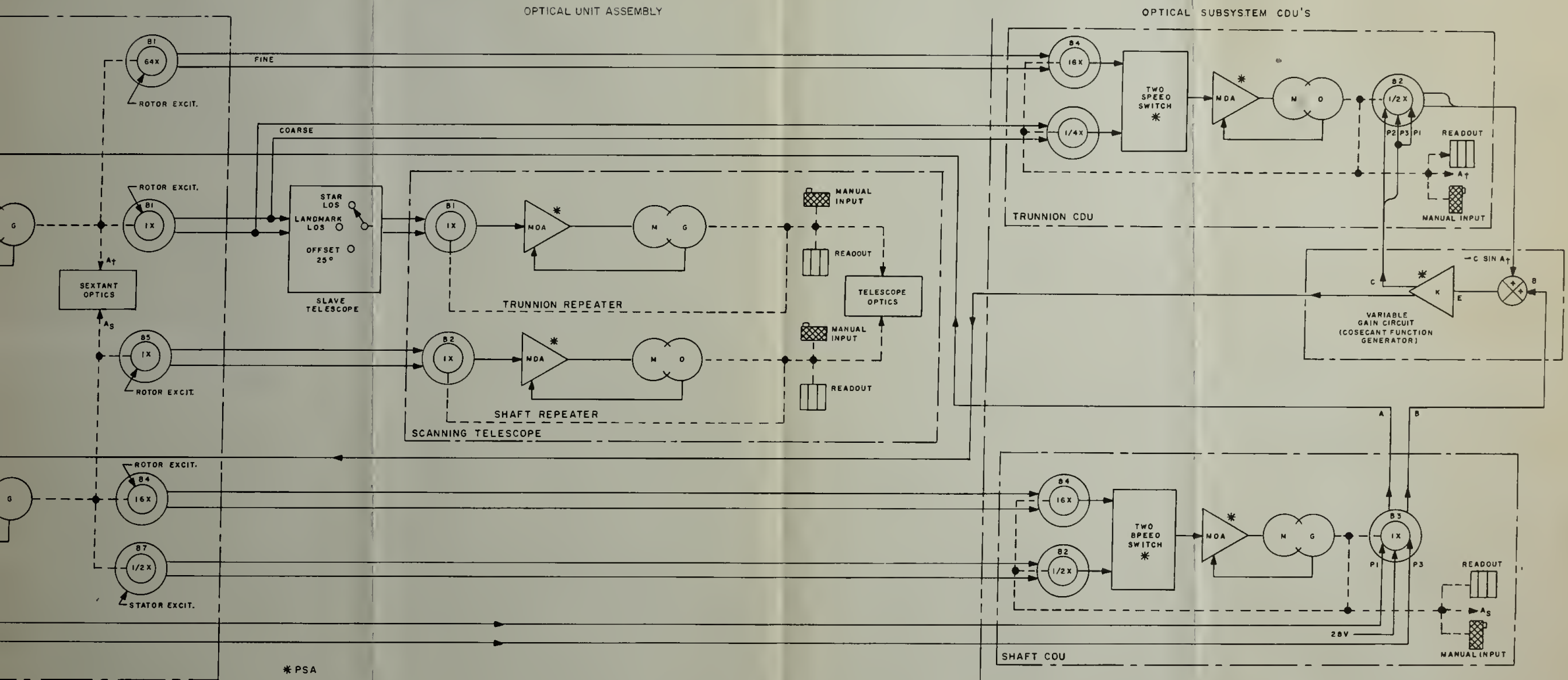
2-5.14.3.3 Scanning Telescope Servo Circuits. In tracker mode, the shaft servo loops function as a single speed repeater in the same manner as in manual resolved mode. The SCT trunnion servo, however, is mechanized as an integrating loop. Tracker mode switching permits the optics hand controller trunnion output ( $A_t$ ) to drive the SCT trunnion integrating loop directly. While the star tracker causes the SXT loops to maintain optical lock-on to the target star, and the CDU's to repeat and provide readouts for this positioning, the SCT is not slaved to the SXT except in shaft positioning. The SCT may be manually scanned without interfering with the SXT or CDU's. This independent manual control frees the SCT for performance of other visual functions over the wide  $60^\circ$  field of view.

G AND N INDICATOR CONTROL PANEL (CONTROLS)

OPTICAL UNIT ASSEMBLY

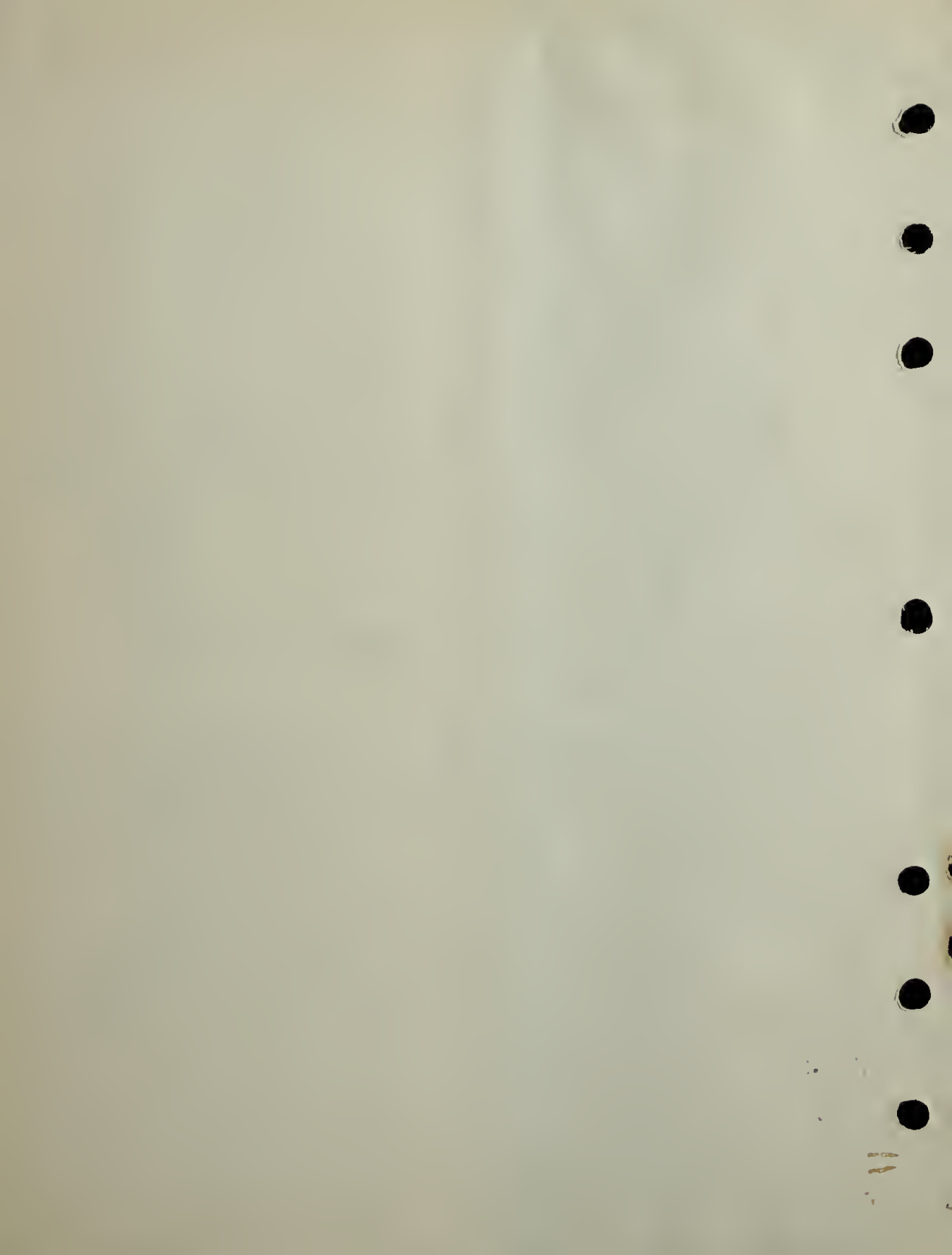


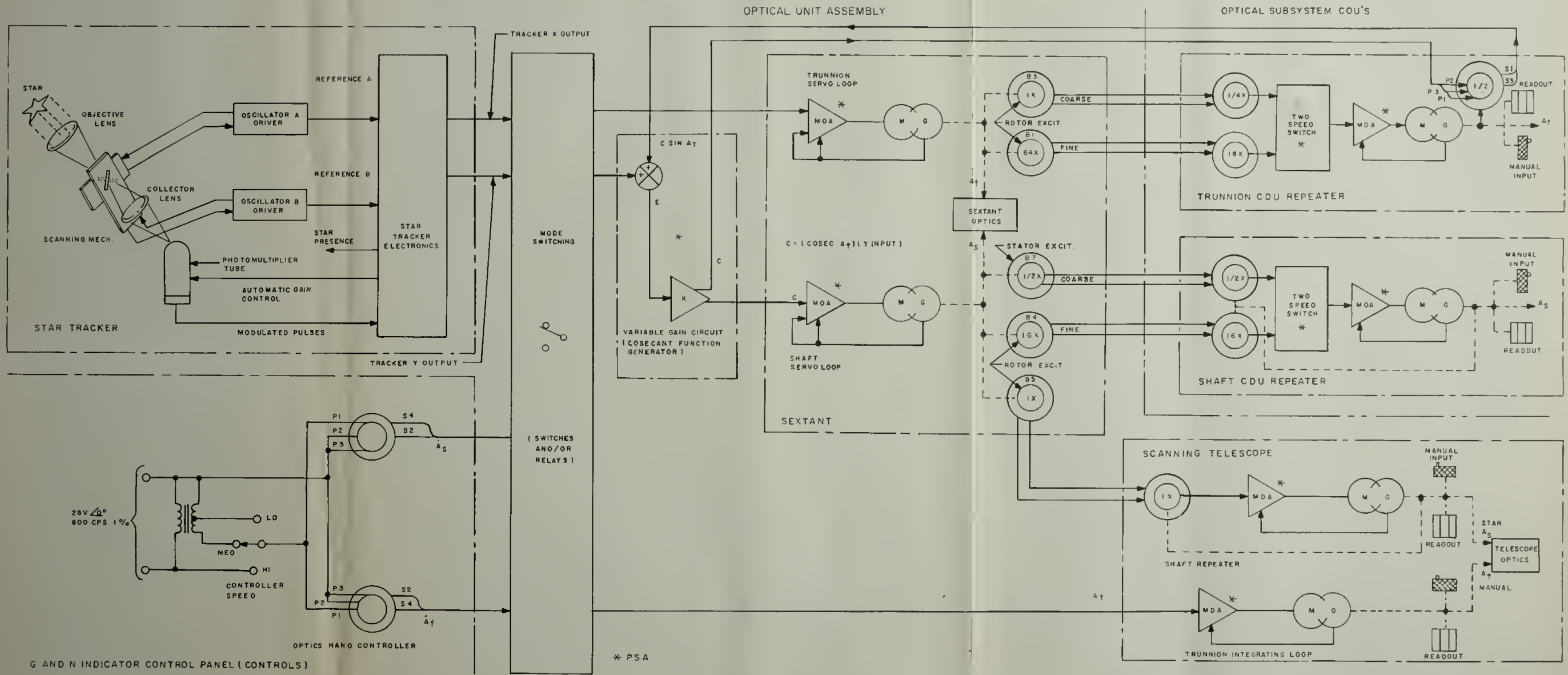
APOLLO GUIDANCE AND NAVIGATION SYSTEM



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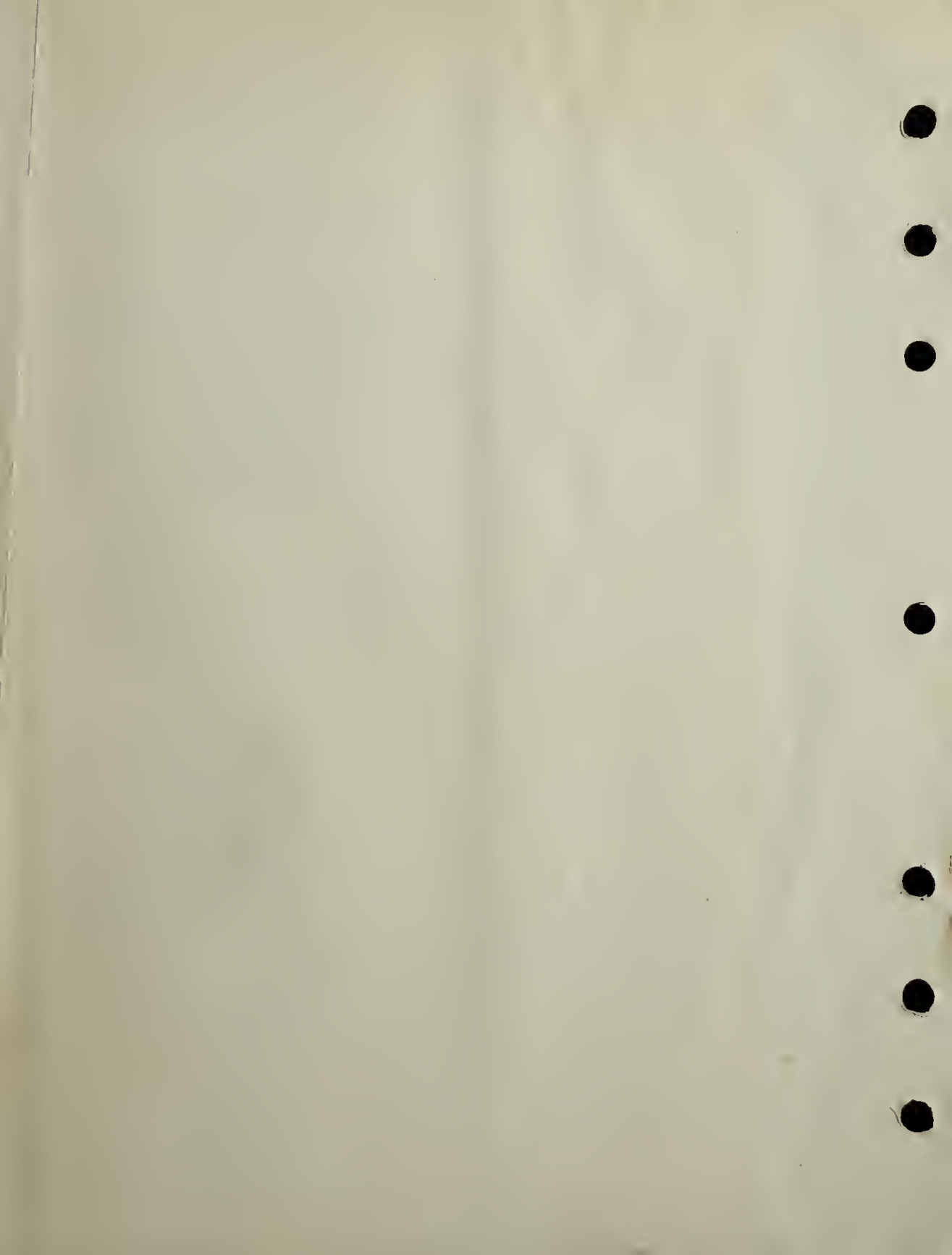
Figure 2-26. Optics Positioning Loops, Resolved Manual Mode





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Figure 2-27. Optics Positioning Loops, Star Tracker Mode



## APOLLO GUIDANCE AND NAVIGATION SYSTEM

2-5.14.4 Computer Mode. The computer mode is initiated from the G and N indicator control panel by the astronaut. The computer then controls and drives the OSS loops. The computer can initiate zero optics, tracker operate, and computer torquing. During the computer mode the AGC routes torquing pulsetrains to a digital to analog converter (DAC), which converts the digital pulses into analog signals that drive the sextant. As the sextant is driven, the CDU's and telescope follow as in the manual direct mode. As the CDU's follow, the CDU encoders convert shaft rotation into digital pulses which are sent to the DAC and the AGC. The encoder pulses to the DAC reduce the DAC output until it is zero. The encoder pulses to the AGC are accumulated in the optical registers and indicate optical angles.

## 2-6 COMPUTER SUBSYSTEM

The CSS is the control and processing center of the G and N system. It consists of the AGC, a main panel DSKY, and a navigation panel DSKY. The CSS processes data and issues discrete and control pulses to the G and N system and to the other Apollo spacecraft systems. The AGC is a parallel digital control computer with many features of a general purpose computer. As a control computer the AGC aligns the IMU, positions the optics (sextant), and issues control commands to subsystems to the spacecraft. As a general purpose computer the AGC solves the guidance and navigation equations required for the round trip to the moon. In addition, the AGC monitors the operation of the spacecraft, including the CSS.

The main function of the AGC (see figure 2-28) is to execute the programs stored in memory. Programs are written in a machine language called basic instructions. A basic instruction contains an operation (order) code and a relevant address. The order code defines the data flow within the AGC and the relevant address selects the data that is to be used for computations. The sequence generator controls data flow. The order code of each instruction is entered into the sequence generator, and the sequence generator produces a different sequence of control pulses for each instruction. It is the responsibility of each instruction sequence to make sure that it will be followed by another instruction. In order to specify the sequence in which instructions are to be executed, the instructions are normally stored in successive memory locations. By adding the quantity one to the address of an instruction being executed, the location of the instruction to be executed next is derived. Execution of an instruction is complete when the order code of the next instruction is transferred to the sequence generator and the relevant address is in the central processor.

The central processor consists of several flip-flop registers. It performs arithmetic operations and data manipulations on information accepted from memory, the input registers, and priority control. Arithmetic operations are performed using the ONE's complement number system. Values up to 14 bits (excluding sign) can be processed with an additional bit produced for overflow or underflow. All operations within the central processor are performed under control of pulses generated by the sequence generator (indicated by dashed lines in figure 2-28). In addition, all words read out of memory are

checked for correct parity, and a parity bit is generated for all words written into memory within the central processor. Odd parity is used; therefore, all words stored in memory including the parity bit contain an odd number of ONE's. The central processor also supplies data and control signals through the output registers and interface to the various spacecraft subsystems.

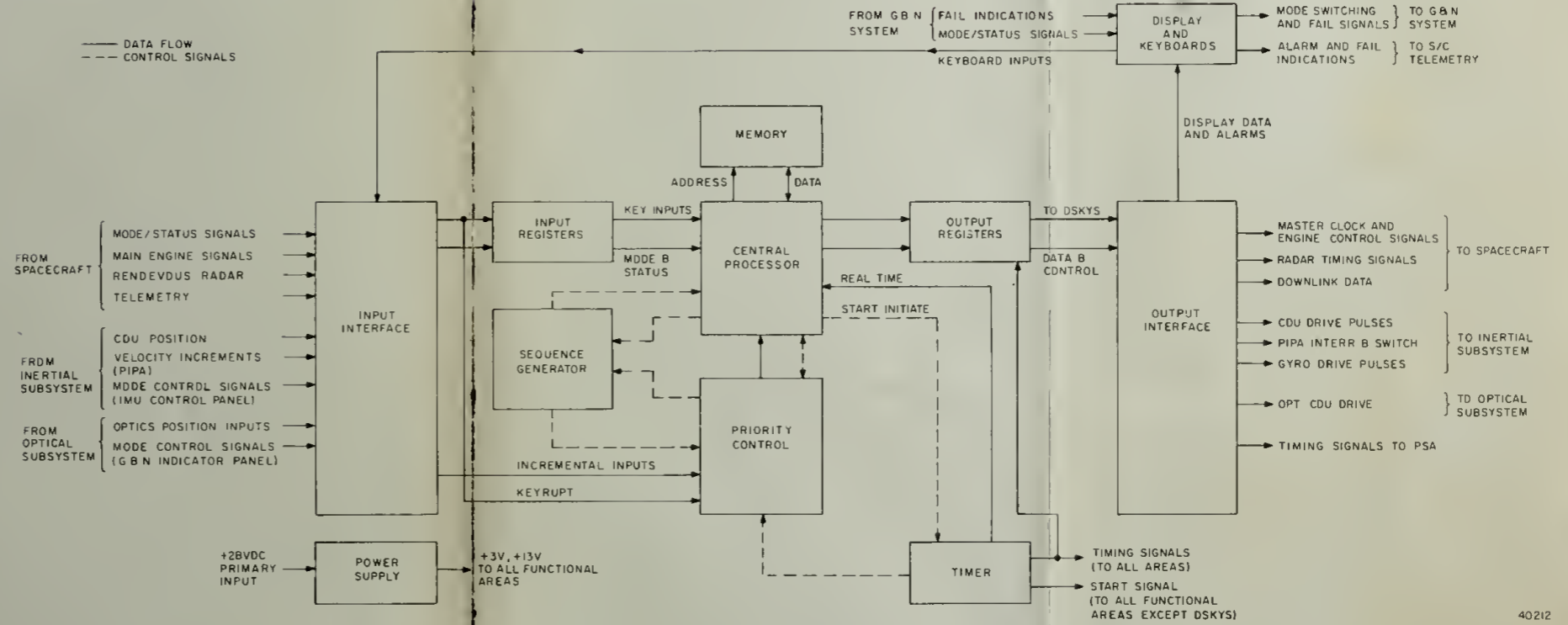
The AGC has provision for six program/interrupts. These six programs, with their order of priority, are: T3RUPT, RPT2, T4RUPT, KEYRUPT, UPRUPT, and DOWNRUPT. The T3RUPT and T4RUPT programs are controlled by the AGC. The DOWNRUPT program is initiated at the completion of every parallel-to-serial conversion for downlink operation. The remaining priority programs are initiated by external inputs to the AGC. The RPT2 program is initiated by acceleration information from the spacecraft, or by failures of the radar or optics. The KEYRUPT program is initiated when a DSKY push-button is depressed or when priority control receives a mark signal (discrete bit) from the OSS to indicate a sighting. The UPRUPT program is initiated when a complete UP-LINK word is received from the spacecraft telemetry section.

Before a priority program can be executed, the current program must be interrupted; however, certain information about the current program must be preserved. This includes the program counter and any intermediate results contained in the central processor. Priority control produces an interrupt request signal, which is sent to the sequence generator. This signal, acting as an order code, causes the execution of an instruction that transfers the current contents of the program counter and any intermediate results to memory. In addition, the control pulses transfer the priority program address in the priority control to the central processor, and then to memory via the write lines. As a result, the first basic instruction word of the priority program is entered into the central processor from memory, and execution of the priority program is begun. The last instruction of each priority program restores the AGC to normal operation, provided no other interrupt request is present. This instruction transfers the previous program counter and intermediate results from their storage locations in memory back to the central processor.

Certain data pertaining to the flight of the spacecraft is used to solve the guidance and navigation problems required for the round trip to the moon. This data, which includes real time, acceleration, and IMU gimbal angles, is stored in memory locations, called counters. The counters are continuously updated as new data becomes available. An incrementing process implemented by priority control changes the contents of the counters. Data inputs to priority control are called incremental pulses. Each incremental pulse produces a counter address and a priority request. The priority request signal is sent to the sequence generator, where it functions as an order code. The control pulses produced by the sequence generator transfer the counter address to memory through the write lines of the central processor. In addition, the control pulses enter the contents of the addressed counter into the central processor for incrementing.



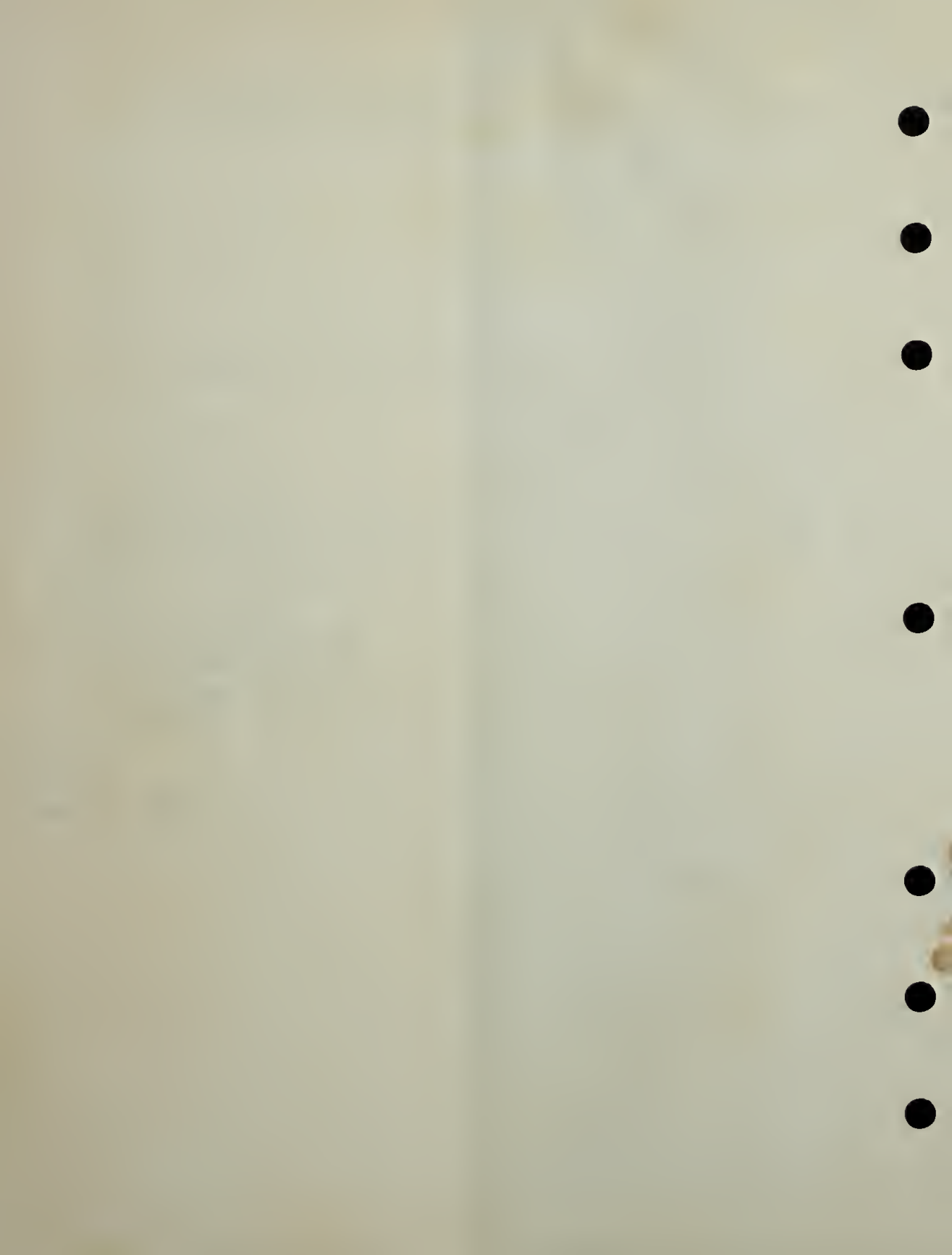
APOLLO GUIDANCE AND NAVIGATION SYSTEM



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*memory system 2M*

Figure 2-28. CSS, Block Diagram



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Real time plays a major role in solving guidance and navigation problems. Real time is maintained within the AGC in the main time counter of memory. The main time counter provides a 745.65 hour (approximately 31 days) clock. Incremental pulses are produced in the timer and sent to priority control for incrementing the main time counter. The Apollo mission requires that the AGC clock be synchronized with the Atlantic Missile Range (AMR) clock. The AGC time is compared with AMR time once every second by downlink operation.

Continuous drive pulses originate in the timer as fixed-frequency timing and strobe signals. The timing signals strobe the outputs from the output registers and the resulting continuous drive pulses are sent to the spacecraft. Rate signals, which are bursts of drive pulses, originate in the output section and are sent to the IMU CDU's or gyros, and to the optics CDU's (sextant and star tracker). Rate signals are also used for controlling the attitude of the spacecraft. The number of pulses in each burst and occurrence of each burst are controlled by a program. The program is dependent on incremental pulse feedback to priority control from the IMU and optics CDU's. The destination of the various rate signals, as well as the type of rate signals (incrementing or decrementing), are also selected by this program.

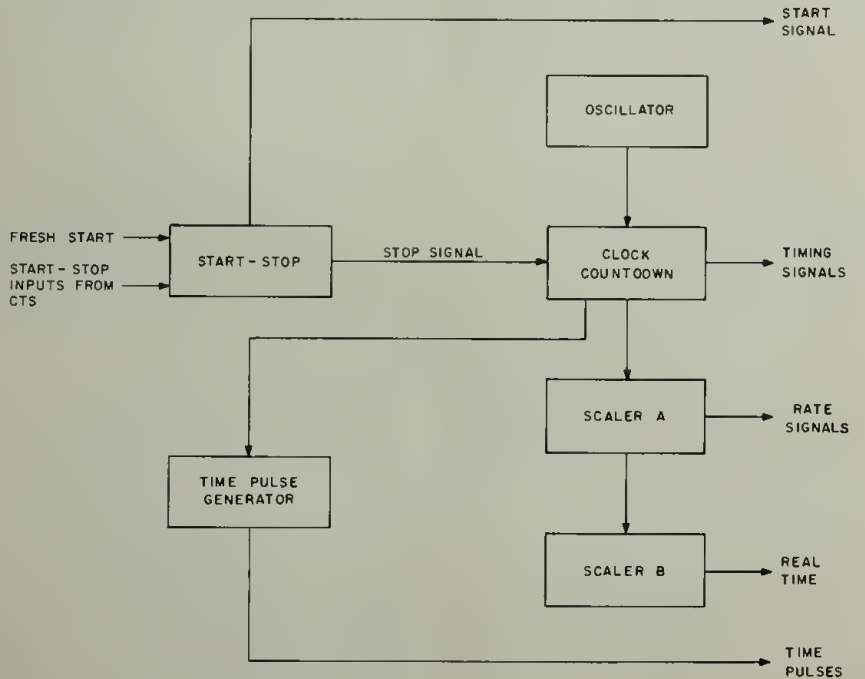
The uplink word from the spacecraft telemetry system and the word from the radar are supplied as incremental pulse inputs to priority control. As these words are received, priority control produces the address of the uplink or radar counter in memory and requests the sequence generator to execute the instructions which perform the serial-to-parallel conversion of the input word. When the serial-to-parallel conversion is completed, the parallel word is transferred to a storage location in memory by the uplink priority program. The uplink program also retains the parallel word for subsequent downlink transmission. Another program converts the parallel word to a coded display format and transfers the display information to the DSKY's.

The downlink operation of the AGC is asynchronous to the spacecraft telemetry system. The telemetry system supplies all the timing signals necessary for the downlink operation. These signals include start, end, and bit sync pulses. The end pulse is sent also to priority control.

The CSS contains two DSKY's. With the keyboard, the astronaut can load information into the AGC, retrieve and display information contained in the AGC, and initiate any program stored in memory. A keycode is assigned to each keyboard pushbutton. When a keyboard pushbutton on either DSKY is depressed, the keycode is produced and sent to an input register. The same keycode is sent also to priority control, where it produces both the address of a priority program stored in memory and a priority request signal, which is sent to the sequence generator. An interrupt request functions as an order code and initiates an instruction for interrupting the program in progress and executing the priority program stored in memory. A function of this program is to transfer the keycode, temporarily stored in the input register, to the central processor, where it is decoded and processed. A number of keycodes are required to specify an address, or a

data word. The program initiated by a keycode also converts the information from the DSKY keyboard to a coded display format. The coded display information is transferred by another program to an output register, and sent to the display portion of each DSKY. The display notifies the astronaut that the keycode was received, decoded, and processed properly by the AGC.

2-6.1 TIMER. The timer generates all of the timing functions required for operation of the AGC and also supplies timing signals to the other spacecraft systems. The timer (figure 2-29) consists of a clock oscillator, clock countdown circuit, scalars A and B, time pulse generator, and the start-stop logic.



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Figure 2-29. Timer, Block Diagram

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The oscillator generates a source frequency, which is divided into the basic clock rate of the system by the clock countdown circuit. Scaler A further divides the countdown circuit output to produce rate signals and gating outputs. The output of scaler A is applied to scaler B, and is then further divided to produce real time indications of 23.3 hours. The time pulse generator, also fed by the clock countdown circuit, generates a recurring series of sequential timing pulse outputs, which define one memory cycle time within the AGC.

The start-stop logic inhibits the clock countdown circuit (thus preventing word flow) when input conditions to this logic indicate a fresh start for the AGC. The start-stop logic can also be controlled from the CTS so that individual memory cycle times can be observed.

2-6.2 SEQUENCE GENERATOR. The sequence generator (figure 2-30) consists of the following: (1) the interrupt service, (2) SQ service, register, and decoder, (3) state counter, (4) instruction decoder, (5) control pulse generator, (6) and branching control. This functional area of the AGC executes the various machine instructions which control the flow of data in the AGC. A machine instruction is defined by an order code entered into the SQ register from the central processor. This input is decoded and, in conjunction with the subinstruction code from the state counter, is applied to the instruction decoder. A machine instruction consists of one or more subinstructions. The state counter essentially indicates the subinstruction to be executed. Consequently, the output of the state counter is applied to the instruction decoder as a subinstruction command along with the instruction defined by the SQ register output. The output of the instruction decoder is applied to the control pulse generator, which generates a sequence of control pulses for the particular instruction involved. This sequence of control pulses, generated for use throughout the AGC, defines a 12 action cycle, which is referred to as a memory cycle time (MCT) within the AGC. Thus, each subinstruction occupies a time interval of one memory cycle time.

A control pulse is fed back from the control pulse generator to step the state counter to the condition necessary for generating the next subinstruction. After the control pulses are generated for the last subinstruction, the order code of the next instruction in the program is entered into the SQ register.

A program interrupt request from priority control interrupts the program currently in progress, clears the SQ register of the previous order code, and forces an interrupt order code into the SQ register and state counter. This causes the sequence generator to execute an interrupt instruction. At the completion of the interrupt request, the interrupted program is resumed unless another interrupt request is present. An interrupt program has priority over the normal program being executed and cannot be inhibited or interrupted except by the start signal from the timer or by a transfer control request from the CTS.

A counter increment request does not interrupt the program in progress in the same manner as an interrupt request, but places a hold on the instruction being executed. This is accomplished by applying a hold signal to the SQ register and state counter to temporarily hold the order code of the instruction being executed. Simultaneously, a counter instruction command applied to the control pulse generator causes associated control pulses to be generated for the particular counter command. Upon completion of the counter command, the sequence generator executes the instruction which had been temporarily inhibited.

During certain instructions, tests for overflow, underflow, sign, and for the quantity minus zero are accomplished by the branching commands, which are applied to the control pulse generator to produce specific control pulses. These control pulses modify the execution of certain subinstructions as dictated by the branching control test.

2-6.3 CENTRAL PROCESSOR. The central processor, figure 2-31, consists of the flip-flop registers, write, read, and clear control logic, write amplifiers, memory buffer register, and the parity logic. All data and arithmetic manipulations within the AGC take place in the central processor.

Primarily, the central processor performs operations indicated by the programs written into memory. Communication within the central processor is accomplished through the write amplifiers. Data flows from memory to the flip-flop registers or vice-versa, between individual flip-flop registers, or into the central processor from external sources. In all instances, data is placed on the write lines and routed to a specific destination under control of the write, clear, and read logic. This logic section accepts control pulses from the sequence generator and generates signals to read from one location in the central processor onto the write lines, and write into another location. As stated previously, this read-write operation can occur between memory and the flip-flop registers, between registers, or from sources external to the central processor.

The memory buffer register buffers all information read out or written into memory. During readout, parity is checked by the parity logic and an alarm is generated in case of incorrect parity. During write-in, the parity logic generates a parity bit for information being written into memory.

The flip-flop registers are used to accomplish the data manipulations and arithmetic operations. Each register is 16 bits or one computer word in length. Data flows into and out of each register as dictated by control pulses associated with each register. The control pulses are generated by the write, clear, and read control logic.

External inputs through the write amplifiers include the bank address when fixed memory is being addressed, control pulses which are associated with specific instructions, the start address for an initial start condition, and all interrupt addresses from priority control. Information from the input registers and the output registers is placed on the write lines and routed to specific destinations either within or external to the central processor. Inputs from the CTS allow a word to be placed on the write lines during system test.

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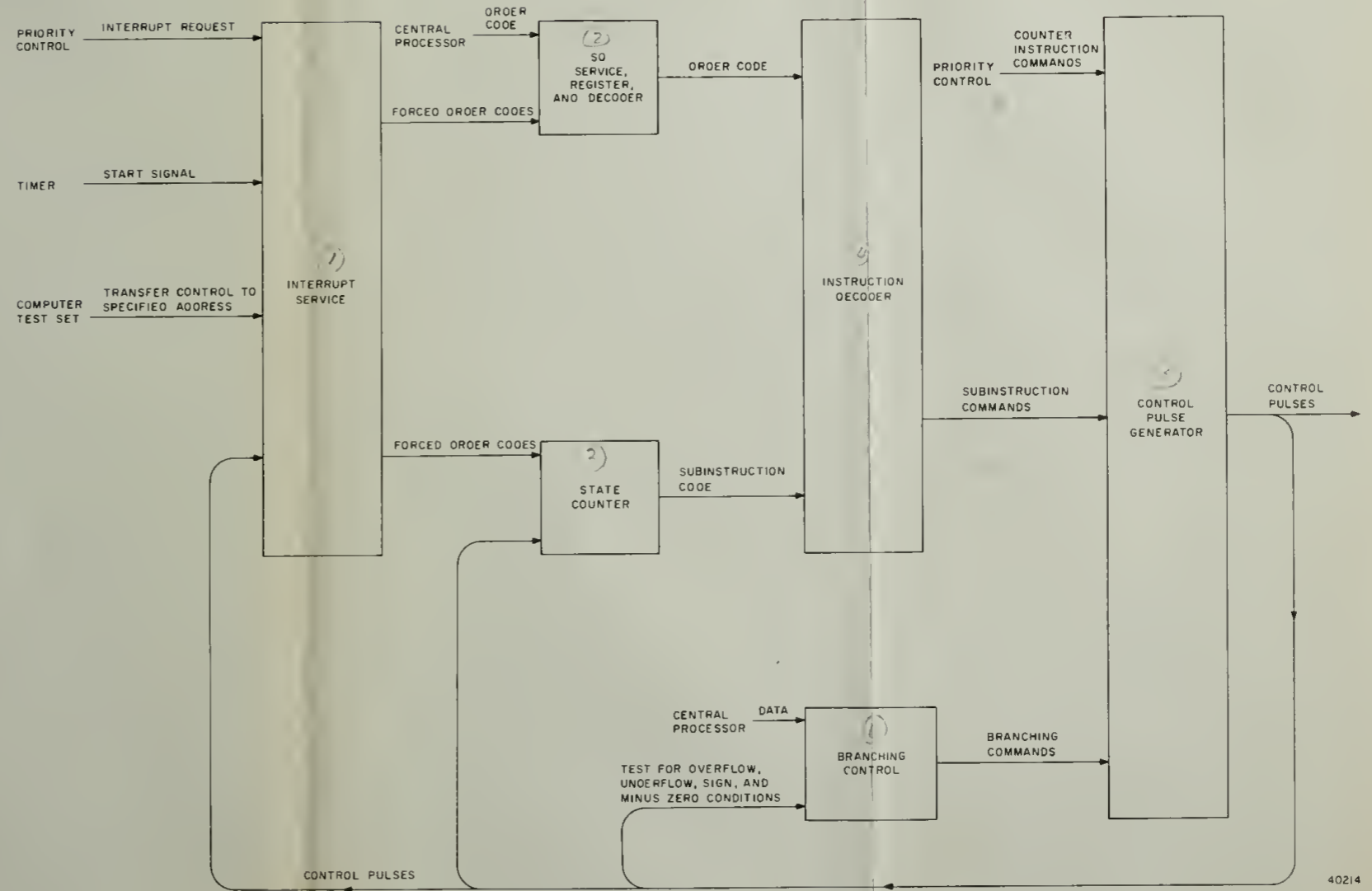
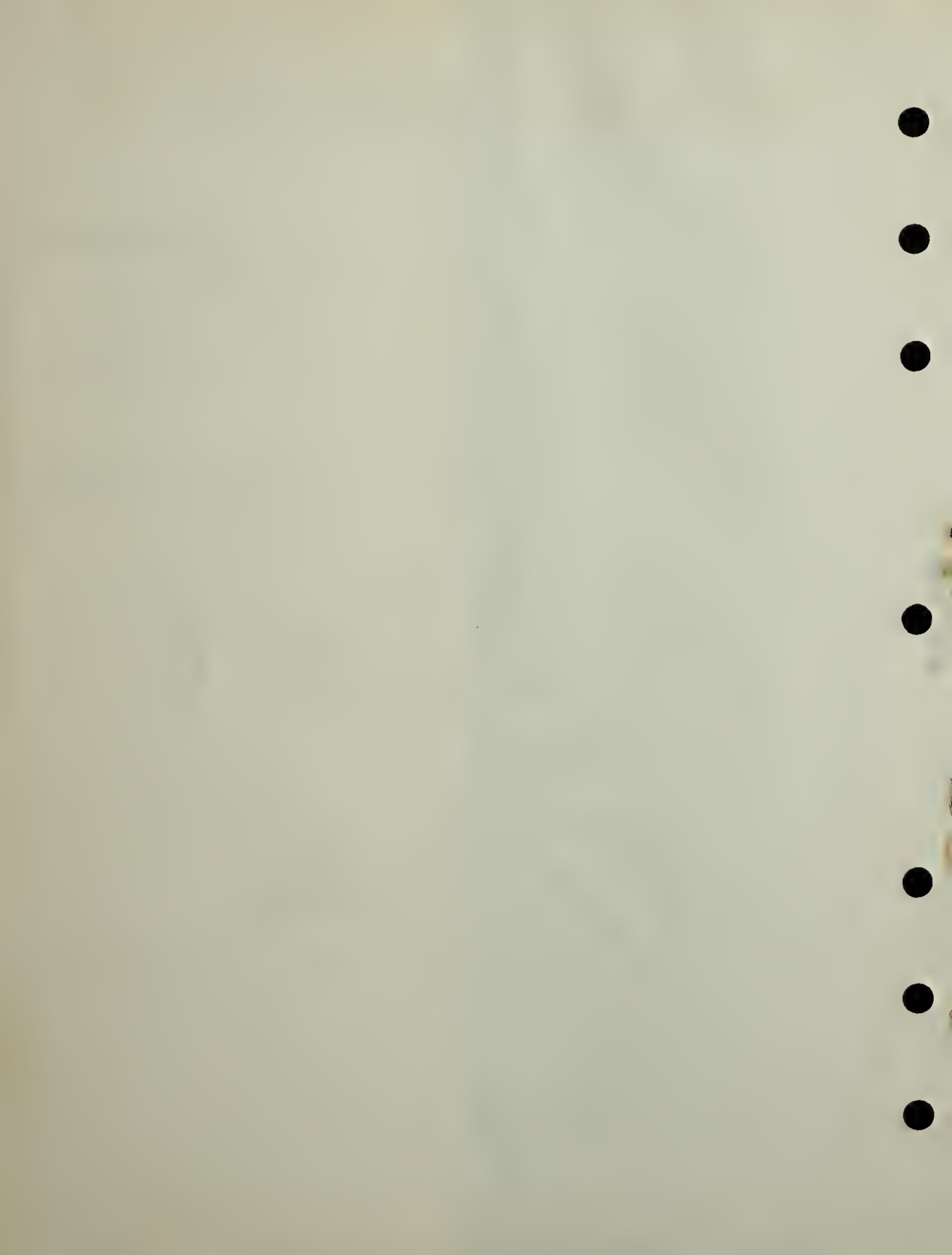


Figure 2-30. Sequence Generator, Block Diagram





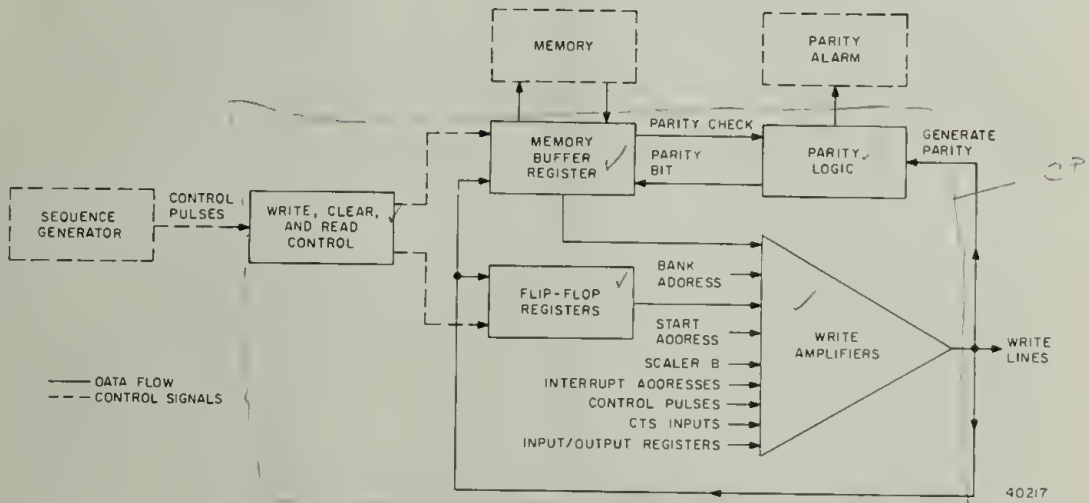


Figure 2-31. Central Processor, Block Diagram

2-6.4 INPUT-OUTPUT SECTION. The input-output system, figure 2-32, consists of the input registers, output registers, downlink converter, rate control logic, and alarm control logic.

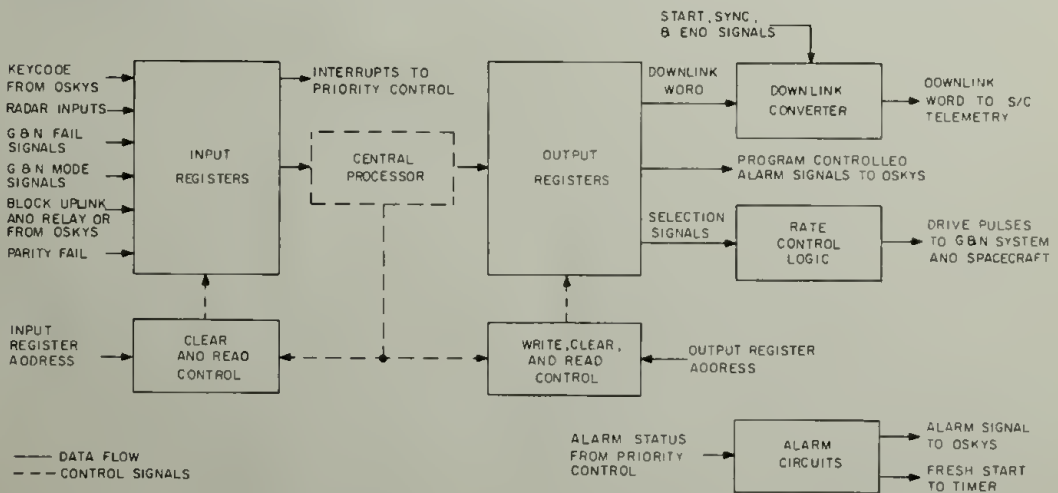


Figure 2-32. Input-Output, Block Diagram

The input registers, which are flip-flop registers, are identical in operation to the flip-flop registers of the central processor, with the exception of the write-in operation. Data inputs from the DSKY's, G and N system, and the spacecraft are applied directly to the bit positions of the input registers. The registers are interrogated under program control, and data is read onto the write lines in the central processor when the input register addresses are generated. The input register applied certain inputs to the priority control logic. When they occur, these inputs cause specific interrupt conditions within the AGC.

The output registers are also identical to the flip-flop registers of the central processor. Data from the write lines is written into these registers, and is read out to the downlink converter or rate control logic when the output register addresses are generated. Program-controlled alarms, the telemetry alarm, and AGC activity indication to the DSKY's are also read out through the output registers. The downlink converter converts the downlink word from the AGC into a form suitable for the telemetry system. The rate control logic provides drive pulses and rate signals to the G and N system and the spacecraft.

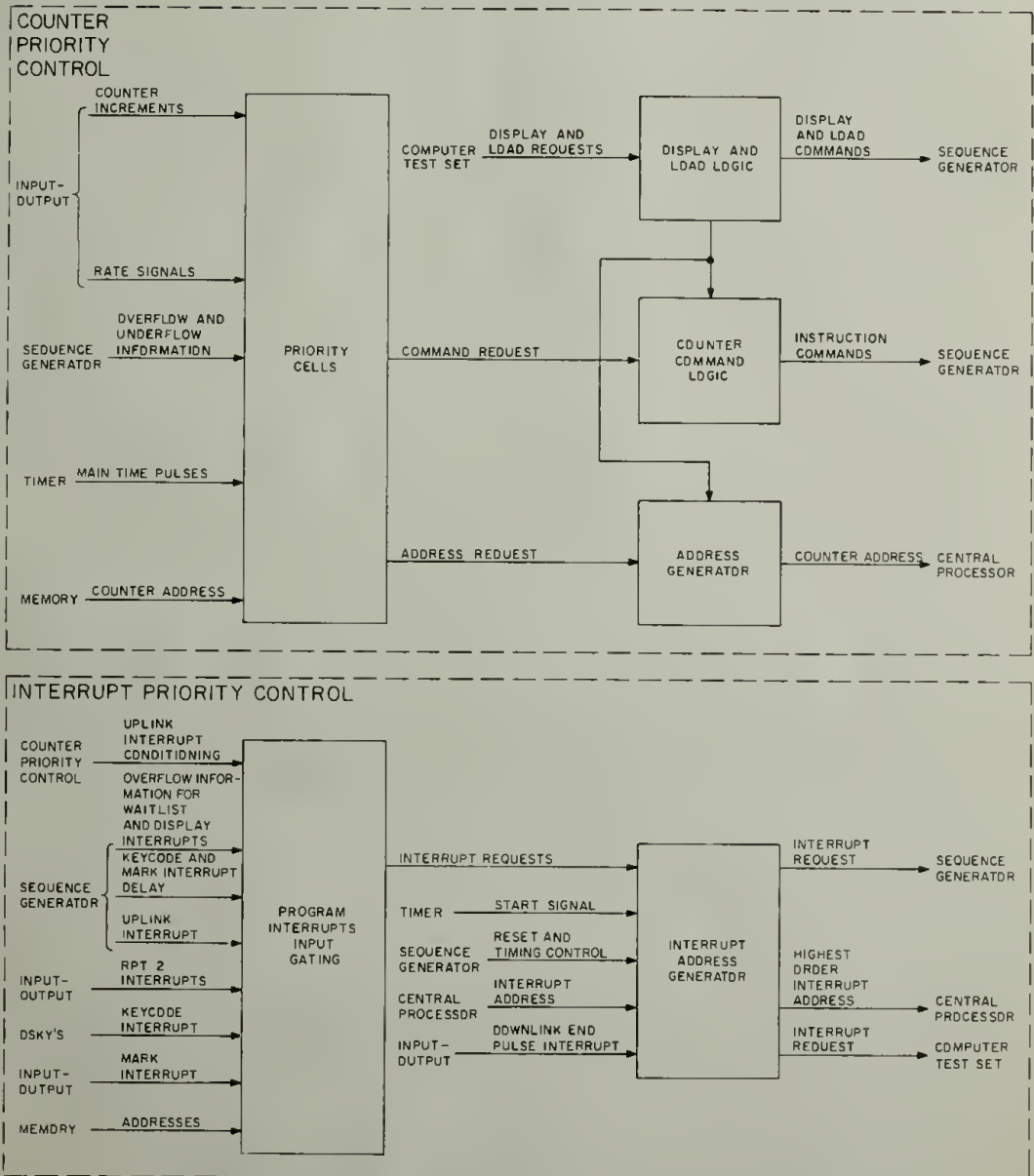
The alarm circuits monitor the status of specific sequences in the AGC including parity check, and generate an alarm indication which is applied to the DSKY's. Coincident with an alarm indication, a fresh start signal is applied to the timer from the alarm circuits.

2-6.5 PRIORITY CONTROL. Priority control, figure 2-33, consists of counter priority control and interrupt priority control. Counter priority control updates the counters in erasable memory associated with elements such as the PIPA and CDU. During test functions, counter priority control implements display and load requests from the CTS. Interrupt priority control transfers AGC control to one of six interrupt (RUPT) transfer sub-routines that initiate programs which deal with conditions such as alarms or keycode inputs from the DSKY's.

Counter priority control updates specific counters when counter increment requests and rate signals are received from the output registers, when main time pulses are received from the timer, and when overflow and underflow signals are received from the sequence generator. Only one counter is updated at a time. However, pulses for several counters may be received simultaneously. When this occurs, the counters are updated in order of preassigned priority. Counter priority control determines the type of counter instruction command inputs and produces the address of the counter to be updated. The sequence generator receives these commands and implements increment, decrement, shift, or shift and add one operations within the central processor.

When a display or load request is received from the CTS, counter priority control commands the sequence generator to execute a display or load instruction. The display instruction causes the contents of a CTS-addressed memory location to be displayed on the CTS. The load instruction allows the CTS to load data into a CTS-addressed location in memory.

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Figure 2-33. Priority Control, Block Diagram

Interrupt priority control receives program interrupt requests, and initiates transfer to one of the following interrupt (RUPT) transfer subroutines: T3RUPT, RPT2, T4RUPT, KEYRUPT, UPRUPT, and DOWNRUPT. (These subroutines are listed in their order of priority.) Interrupt inputs are applied to the program interrupt input gating circuit. This circuit supplies all available interrupt requests, except the downlink-end-pulse, to the interrupt address generation circuit. The interrupt address generation circuit supplies an interrupt request signal to the sequence generator and supplies the address of the highest priority interrupt request present to the central processor. An interrupt request signal is also generated and applied to the CTS. A timing control signal from the sequence generator enables the highest priority interrupt address which is then sent to the central processor. This interrupt address is the address of the first instruction of a RUPT transfer subroutine. Timing pulses are applied to enable the interrupt address generation circuit operations at the proper times. The timer start signal (GOJAM) clears all interrupt requests that are present.

Waitlist, display, and uplink interrupt requests are controlled by operations within counter priority control. Counters associated with the task execution and display interrupt programs are incremented until overflows are detected by the sequence generator. The counter operation command generation circuit within counter priority control produces an uplink interrupt conditioning signal when a complete uplink word has been received and stored in the uplink counter. The sequence generator delays the keycode and mark interrupt requests. This action prevents the keycode and mark interrupt requests from interfering with lower order interrupt requests in progress.

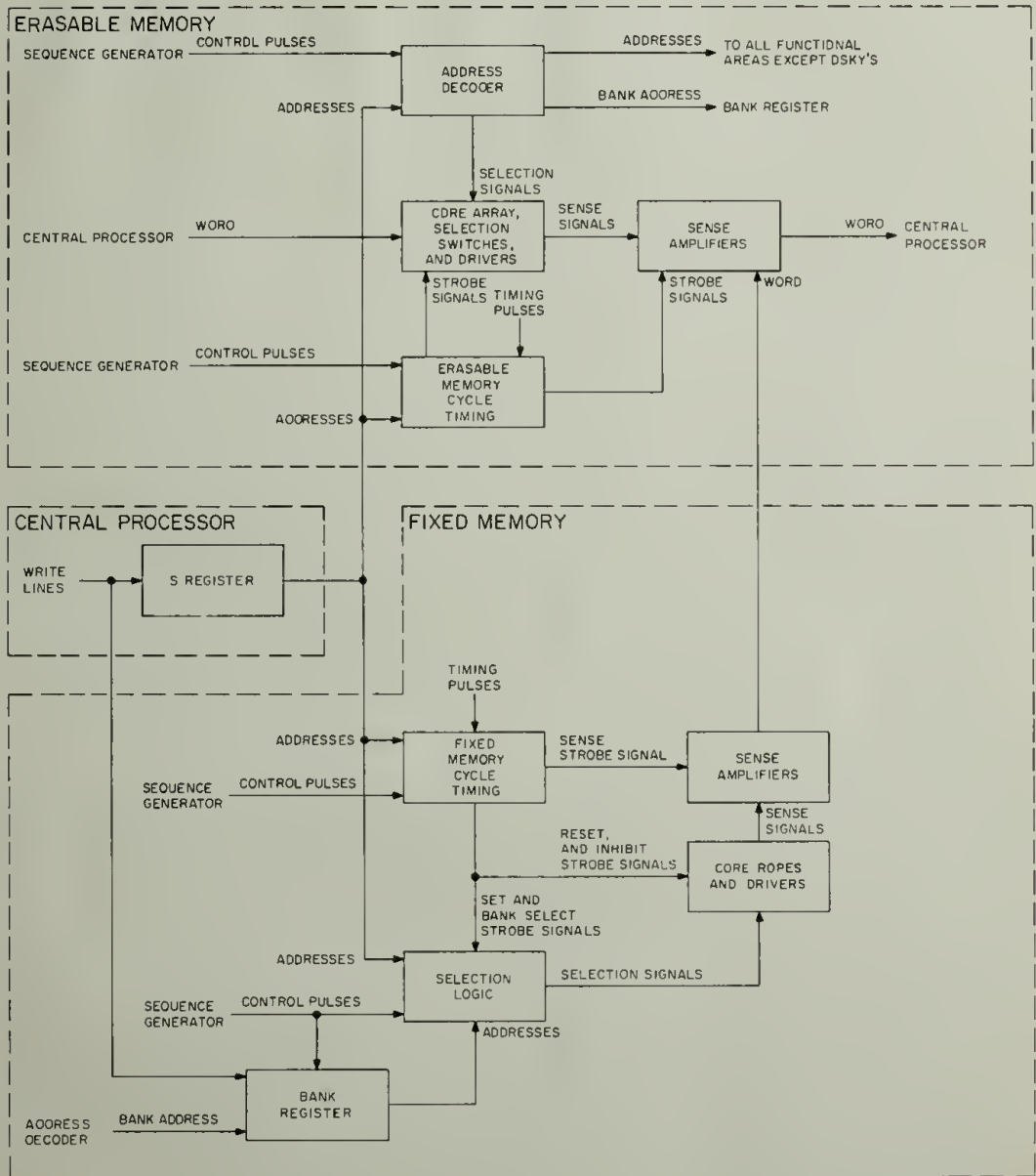
2-6.6 MEMORY. Memory (figure 2-34) consists of an erasable memory with a storage capacity of 1024 words and a fixed core rope memory. Erasable memory is a random-access, destructive-readout storage device. Data stored in erasable memory can be altered or updated. Fixed memory is a non-destructive storage device. Data stored in fixed memory is unalterable since the data is wired in and readout is non-destructive.

Both memories contain magnetic-core storage elements. In erasable memory the storage elements form a core array; in fixed memory the storage elements form three core ropes. Erasable memory has a density of one word per 16 cores; fixed memory has a density of eight words per core. Each word is located by an address.

Addresses are assigned to instructions to specify the sequence in which they are to be executed, and blocks of addresses are reserved for data, such as constants and tables. The information is then put into assigned locations in erasable memory with the CTS, the DSKY's, uplink, or program operation. Information is placed into fixed memory permanently by weaving patterns through the magnetic cores.

Both memories use a common address register (register S) in the central processor. When register S contains an address pertaining to erasable memory, the erasable memory cycle timing is energized. Timing pulses sent to the erasable memory cycle timing then produce strobe signals for the read, write, and sense functions. The address decoder receives addresses from register S and produces selection signals for the core array. The address decoder also sends addresses to the bank register and to all functional areas except the DSKY's. The selection switches perform a decoding function

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Figure 2-34. Memory, Block Diagram

which permits data to be written into or read out of the selected storage location. When a word is read out of a storage location in erasable memory, the location is cleared. It must be put back into its storage location via the write process. When a word is written into a storage location, the word enters memory from the buffer register in the central processor and is strobed into the selection storage location by write driver outputs. When a word is read from a storage location, the word is strobed by read driver outputs and applied to the sense amplifiers. The sense amplifiers are strobed also and the information is entered into the central processor. The memory buffer register receives information from both memories. Word flow is from fixed memory to the erasable memory sense amplifiers and then into register G.

Fixed memory contains an additional address register (bank register), which is necessary because of the increased number of locations. The address in register S energizes the fixed memory cycle timing when a location in fixed memory is addressed. The timing pulses sent to the fixed memory cycle timing produce the strobe signals for the read and sense functions. The selection logic receives addresses from registers S and the bank register (BNK) and produces selection signals for the core ropes. Register BNK receives addresses from the central processor write lines when the register is addressed and when the proper control pulses from the sequence generator are present. The content of a storage location in fixed memory is strobed from the fixed memory sense amplifiers to the erasable memory sense amplifiers and then entered into the memory buffer register in the central processor.

2-6.7 DISPLAY AND KEYBOARDS. There are two DSKY's associated with the AGC: one on the main display and control panel designated the main DSKY, and second on the lower control panel of the G and N system designated the navigation DSKY. The DSKY's are almost identical; a few differences exist between the two in the number of controls and alarm indicators.

Each DSKY (figure 2-35) consists of a keyboard, relay matrix with associated decoding circuits, displays, alarm circuits, and power supply. The keyboard, which contains several numerical, sign, and other control keys, allows the astronaut to exercise control of the AGC. The inputs from the keyboard are entered into an input register and are processed by the AGC.

The inputs entered from the keyboard, as well as other information, appear on the displays after extensive processing by the program. The display of information is accomplished through the relay matrix. A unique code for the characters to be displayed is formed by fifteen bits from an output register in the AGC. This code is then decoded by the decoding circuits. The decoded word energizes specific relays in the matrix which causes the appropriate characters to illuminate. The information displayed is the result of a keycode punched-in by the astronaut, or is computer-controlled information. The display characters are formed by electro-luminescent segments which are energized by a voltage from the power supply routed through relay contacts. Specific inputs from the G and N system are also applied to certain relays in the matrix. These inputs are simultaneously entered into the AGC to produce the desired code and energize the appropriate relays. The resulting relay-controlled outputs are mode and fail signals to the G and N system.

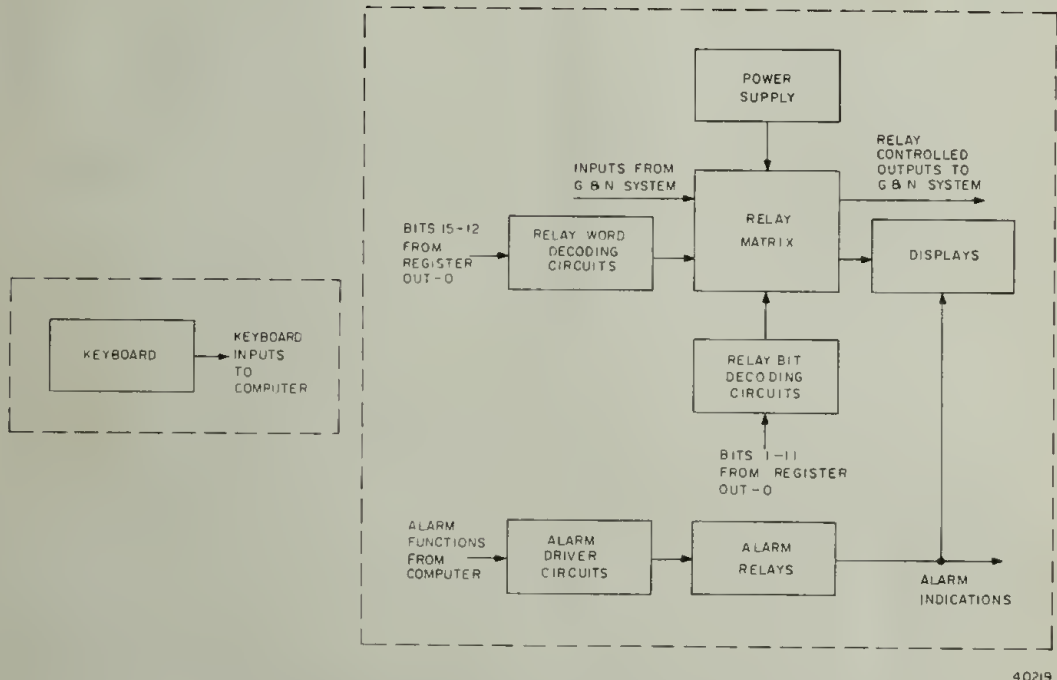


Figure 2-35. Display and Keyboard, Block Diagram

The alarm circuits accept the alarm functions from the AGC. In the navigation panel DSKY, the alarm indications are applied to associated alarm display lamps. In the main panel DSKY, the alarms are applied to the spacecraft telemetry system.

2-6.8 POWER SUPPLY. The power supply (figure 2-36) furnishes operating voltages to the AGC and the DSKY's. Primary power of 28 volts dc from the spacecraft is applied to three power switches. Two of these switches furnish +3 volts, and one switch the +13 volt output. The circuits of all three switches are identical. The dc output voltage is determined by the regulator circuits which also maintain a constant output from both voltage sources. The regulator circuits are driven by a sync signal input from the timer. During subsystem test, inputs from the CTS can be used to simulate power supply failures.

One of the +3 volt outputs and the 13 volt output are applied to the filter circuits. The filter outputs are used primarily for operation of the memory circuits. Additional filter circuits for the voltage outputs are contained on most of the modules to which these voltages are applied.

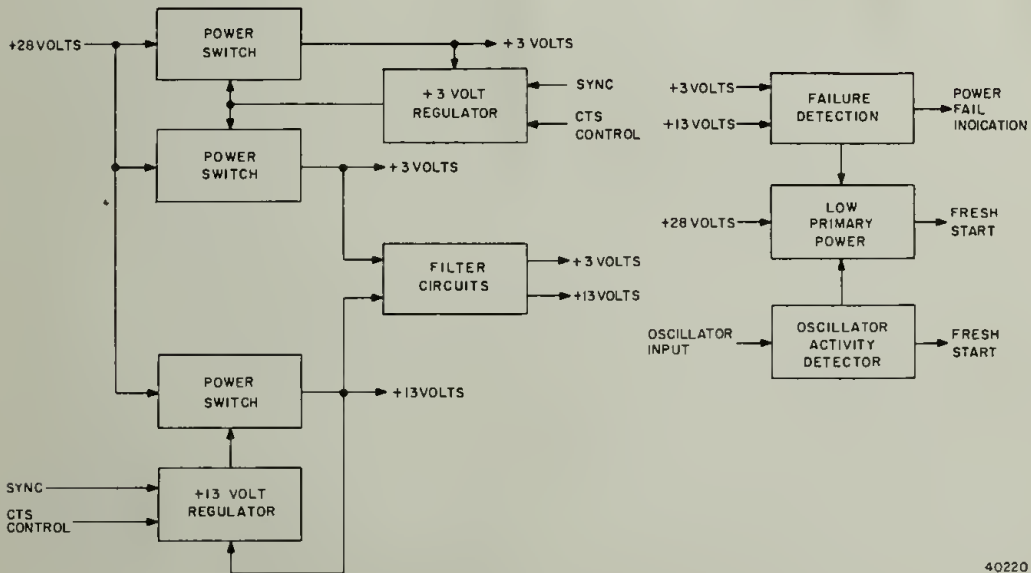


Figure 2-36. Power Supply, Block Diagram

The failure detection circuits monitor the +3 and +13 volt outputs, and produce a power fail indication to the spacecraft in the event either supply fails. The primary power input of 28 volts dc is also monitored by a circuit which generates an AGC re-start signal should the primary power fall below a predetermined level. The oscillator activity detector assures a start condition in the AGC during a power up sequence until the oscillator starts running.

2-6.9 MACHINE INSTRUCTIONS. Each machine instruction is a distinct operation such as add, increment the addressed counter, or multiply. The machine instructions are defined by order codes or command signals in the sequence generator. Order codes are supplied from the central processor or generated within the sequence generator. Each machine instruction consists of one or more subinstructions. The subinstructions are defined by subinstruction codes or by command signals within the sequence generator. Each subinstruction requires one memory cycle time for execution. One memory cycle time is defined by timing pulses T01 through T12. There are three functional divisions of machine instructions: regular, involuntary, and miscellaneous.



2-6.9.1 Regular Machine Instructions. Regular machine instructions identify distinct operations during program executions and consist of basic instructions and extra code instructions. Each basic instruction word in memory contains a three bit order code which identifies a basic instruction. This three bit order code is converted to a four bit order code within the central processor and then is supplied to the sequence generator. The three bit order code identifies eight basic instructions. Three additional regular machine instructions, the extra code instructions, are identified by order codes obtained within the central processor by indexing. Indexing adds selected quantities to quantities specified by the three bit order code. Therefore, the four bit order code sent to the sequence generator is not limited to identifying eight instructions. Eleven regular machine instructions, consisting of eight basic instructions and three extra code instructions, are identified. The eight basic instructions are as follows:

- |                               |                          |
|-------------------------------|--------------------------|
| (1) Transfer control.         | (5) Clear and subtract.  |
| (2) Count, compare, and skip. | (6) Transfer to storage. |
| (3) Index.                    | (7) Add.                 |
| (4) Exchange.                 | (8) Mask.                |

The extra code instructions consist of the multiply, divide, and subtract instructions.

The transfer control instruction transfers AGC control to an instruction word in a given location. The address of the instruction word that was to be executed next is stored, and a transfer control instruction can later be used to return AGC control to this stored instruction word.

The count, compare, and skip instruction selects one of four new instruction words, depending on the magnitude and sign of a quantity at a given location. This branching control allows program options depending on the results of selected computations.

The index instruction modifies basic instruction words to obtain order codes of extra code instructions and to obtain other basic instruction words. If a basic instruction word result is desired, either the order code, the relevant address, or the order code and relevant address can be changed. The relevant address cannot be changed when an order code of an extra code instruction is obtained.

The exchange instruction exchanges the contents of the central processor accumulator with the contents of a given erasable memory location or central processor register. If a location in fixed memory is given, its contents are copied into the accumulator after the former accumulator contents are cleared.

The clear and subtract instruction enters the complement of the contents at a given location into the accumulator. If the given location is the accumulator, the accumulator contents are complemented.

The transfer to storage instruction copies the accumulator quantity into an erasable memory location or into another flip-flop register. If one memory location is not sufficient to store the quantity, other instructions which copy part of the quantity into a second location may be initiated.

The add instruction copies the contents of a given location into the accumulator if the accumulator was initially cleared. If the accumulator contained a number, the add instruction adds the contents of the given location to the number in the accumulator. If the given location is the accumulator, the accumulator contents are doubled.

The mask instruction detects individual-bit conditions of the binary word contained in the accumulator. The results are used to determine program execution options.

The multiply instruction multiplies the accumulator contents by the contents of a given location. The result, because of its length, is stored in the accumulator and another register. The contents of the accumulator are squared if the given location is the accumulator.

The divide instruction divides the contents of a given location into the accumulator contents. The quotient is stored in the accumulator; any remainder is stored separately.

The subtract instruction subtracts the contents of a given location from the accumulator contents. The result is stored in the accumulator. If the accumulator was initially cleared, the subtract instruction copies the complement of the contents of a given location into the accumulator. If the given location is the accumulator, the result is a minus zero.

2-6.9.2 Involuntary Machine Instructions. Involuntary machine instructions, which do not obtain order codes from the central processor, consist of interrupt and counter instructions. These instructions are initiated by program interrupt and resume condition signals and by counter instruction commands. The program interrupt request and counter instruction commands are generated by priority control. Resume conditions are detected by the sequence generator when an interrupting program is finished. Order and subinstruction codes for the two involuntary interrupt instructions are generated within the sequence generator. These are the interrupt and resume instructions that allow an interrupting program to be executed. The counter instruction commands from priority control inhibit program execution and initiate the counter instructions. There are four counter instructions: increment, decrement, shift, and shift and add one. The counter instruction commands control the sequence generator outputs and also prevent the stored order and subinstruction codes from affecting sequence generator outputs. Therefore, the counter instructions do not require order and subinstruction codes.

The interrupt instruction accomplishes transfer operations necessary to initiate an interrupt program. Instruction information and computation results of the current program are stored so that later the current program can be resumed at the point of interruption. Also, the address of the first instruction word of the interrupt program is brought into the central processor.

The resume instruction occurs at the end of an interrupting program. This instruction restores the instruction information and computation results. Execution of the interrupted program is then resumed.

The counter instructions are initiated in the counter priority control circuits which also supply the address of the applicable counter to the central processor. A counter word is then brought into the central processor, and the counter operation is performed. The increment instruction adds one to the counter word; the decrement instruction subtracts one from the counter word; the shift instruction shifts the contents one place to the left; and the shift and add one instruction shifts the contents one place to the left and adds one. The shift instructions accomplish serial-to-parallel conversions of inputs to the AGC.

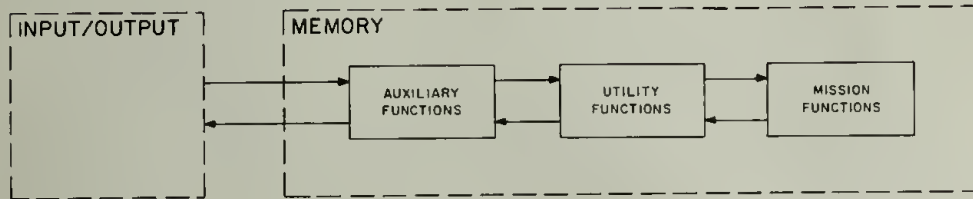
2-6.9.3 Miscellaneous Machine Instructions. The miscellaneous instructions consist of the go, start at specified address, display, and load instructions. The sequence generator generates order and subinstruction codes for the go and start at specified address instructions. The timer supplies the start signal which initiates the start instruction. The CTS supplies the start at specified address signal. The display and load initiation signals are instruction commands received from priority control circuits and are initiated by the CTS. As with the counter instructions, the display and load instructions have no order or subinstruction code.

The go instruction occurs in conjunction with the start signal. This instruction transfers AGC control to an instruction word that begins a program operation which places the AGC in an idle condition. Through DSKY operation, the AGC can be returned to the program operating when the start signal occurs, or any other selected program. Other programs might be selected to perform tests if the start signal was generated as a result of an alarm. (The start signal can also be generated by the CTS.)

The start at specified address instruction enables the CTS to transfer AGC control to selected instruction words. An address is received from the CTS and copied into the central processor when the instruction is performed.

The display and load instructions are initiated by the CTS. The display instruction obtains a word from memory that is addressed by the CTS and provides this word to the CTS for display and other uses. The load instruction loads data from the CTS into memory locations that are addressed by the CTS.

2-6.10 PROGRAMS. An AGC program performs such functions as solving guidance and navigation problems, testing the operation of the G and N system, and monitoring the operation of the spacecraft. Such a program consists of a group of program sections that are classified according to the functions they perform. These functions are defined as mission functions, auxiliary functions, and utility functions. (See figure 2-37.)



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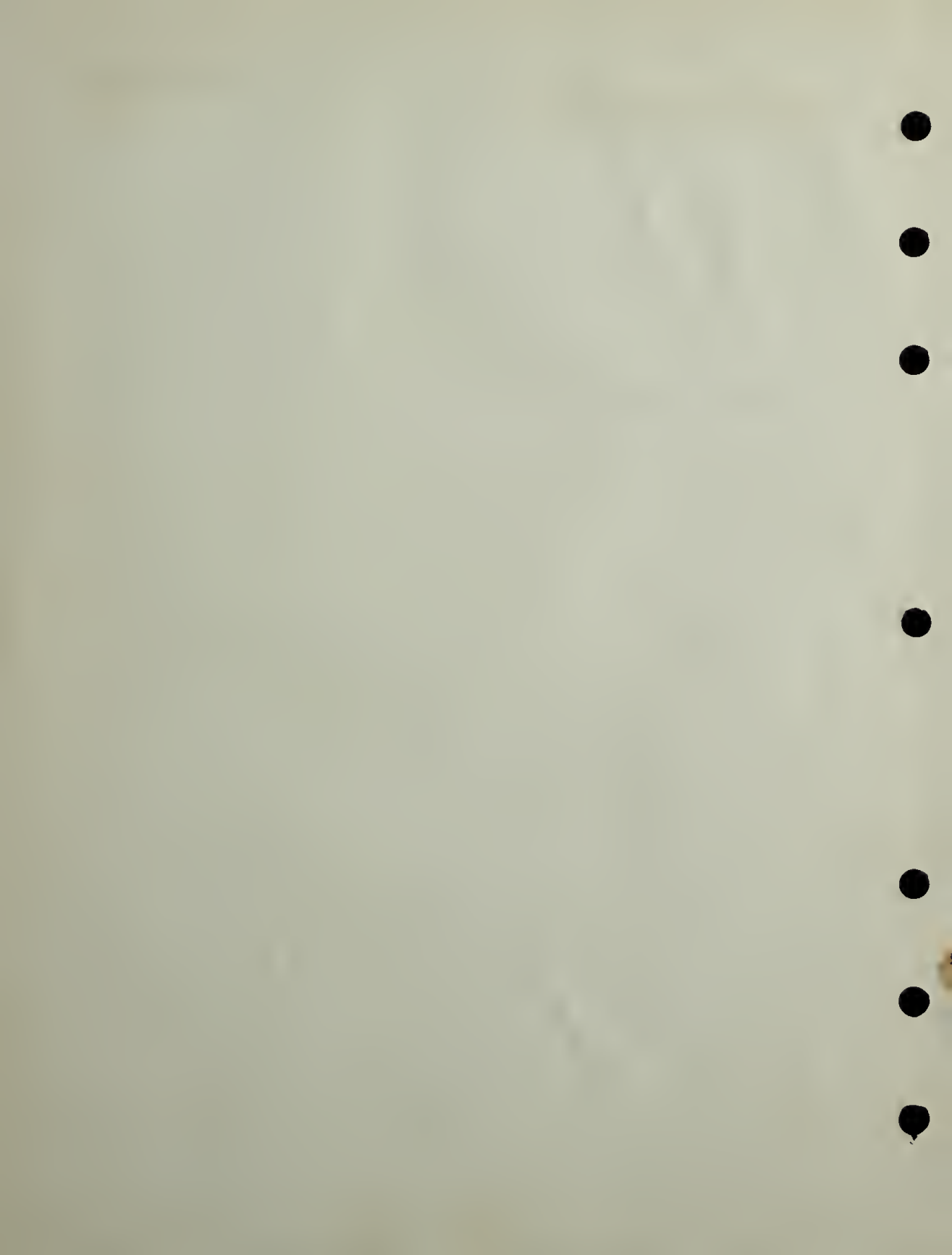
Figure 2-37. Program Organization

2-6.10.1 Mission Functions. Mission functions are performed by program sections that implement operations concerned with the major objectives of the Apollo mission. These operations include erecting the IMU stable member and aligning it to a desired heading while the spacecraft is located on the ground. The stable member is also aligned each time the ISS is re-energized during a flight. In addition, the mission functions include computation of spacecraft position and velocity during coasting periods of the flight by solution of second-order differential equations which describe the motions of a body subject to the forces of gravity.

2-6.10.2 Auxiliary Functions. Auxiliary functions are executed at the occurrence of certain events, requests, or commands. Auxiliary functions are performed by program sections that implement many and varied operations in support of the mission functions. These operations include:

- (1) Starting and restarting most program sections in response to a keyboard entry via the DSKY's or as the result of a hardware failure.
- (2) Accepting and processing keyboard and uplink information.
- (3) Supplying data to the telemetry system.
- (4) Servicing devices outside the CSS which require high frequency attention.
- (5) Selecting the various modes of the IMU and optics and controlling the use of these units.
- (6) Providing the means for aligning the IMU in flight.
- (7) Testing the CSS and other elements of G and N system.
- (8) Displaying alarm messages on the DSKY's to notify the operator of failure conditions within the G and N system.

2-6.10.3 Utility Functions. Utility functions are performed by program sections that coordinate and synchronize AGC activity to guarantee orderly and timely execution of required operations. These functions control the operation of the mission functions and schedule AGC operations on either a priority or a real-time basis. The utility functions also translate interpretive language to basic machine language which allows complex mathematical operations such as matrix multiplication, vector addition, and dot product computations to be performed within the framework of compact routines. In addition, the utility functions save the contents of registers A and Q during an interrupt condition and enable data retrieval and control transfer between isolated banks in the fixed-switchable portion of fixed memory.



## Chapter 3

## PHYSICAL DESCRIPTION

## 3-1 SCOPE

This chapter describes G and N system components. The purposes and capabilities of each component are discussed. Module location and identification, and location and functions of controls and indicators are presented where applicable. Basic components of the system are shown in figure 3-1. Nomenclature and location of each component are listed in table 3-I.

Table 3-I: G and N System Components

Nomenclature	Short Form Nomenclature	Part Number	Location
G and N indicator control panel	G and N indicator control panel	1014664-011	Center of navigator's panel
Navigation base frame assembly	nav base	1899982	Behind G and N indicator control panel
Inertial measuring unit	IMU	1001500	Lower section of nav base
Optical unit assembly	OUA	2011000	Upper section of nav base
Optics shroud assembly	optics shroud	1014502-011	OUA
Optics cover assembly	optics cover	1014532	Attaches to optics shroud
Condition annunciator	condition annunciator	1023040	Above OUA
Power and servo assembly	PSA	1007570	Below G and N indicator control panel

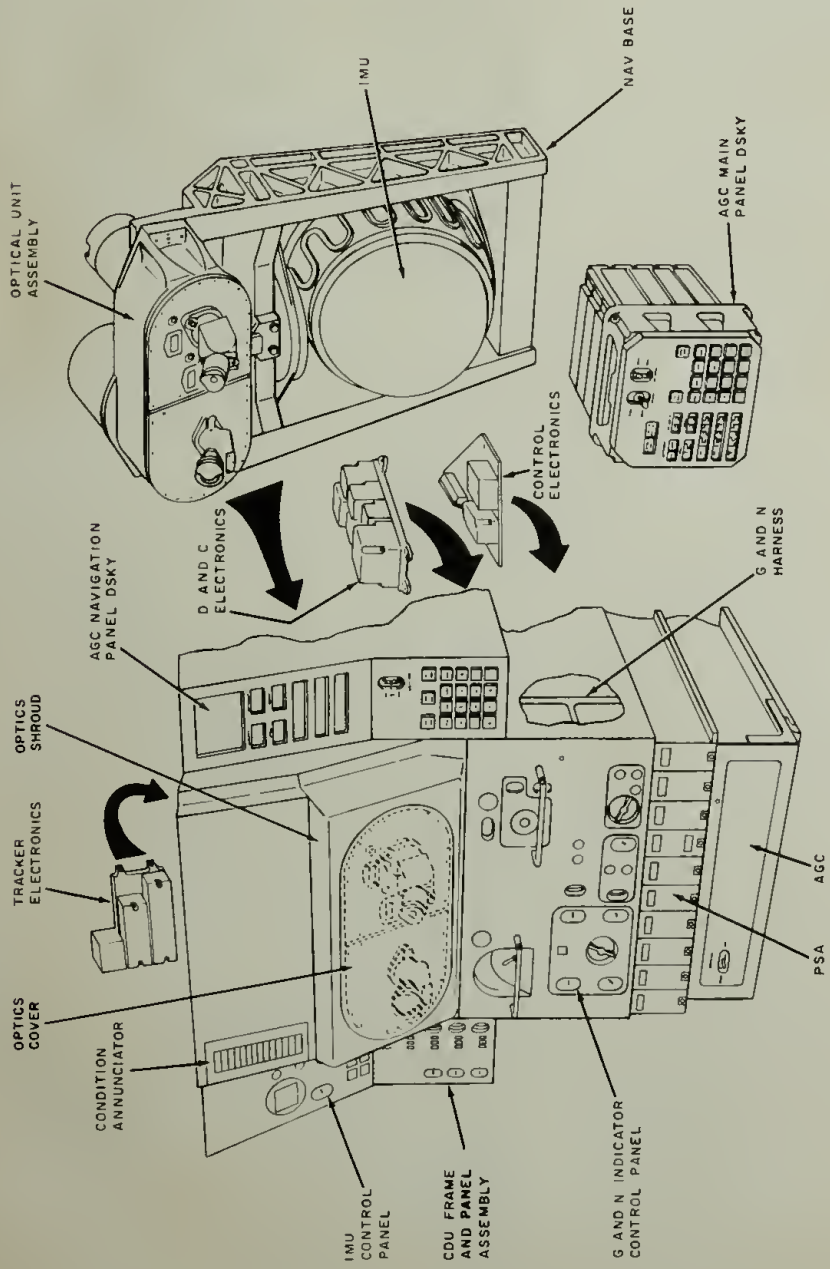
(Sheet 1 of 2)

Table 3-I. G and N System Components (cont)

Nomenclature	Short Form Nomenclature	Part Number	Location
Apollo guidance computer	AGC	1003700	Below PSA
IMU control panel assembly	IMU control panel	1014628	To left of condition annunciator
Coupling display unit frame and panel assembly	CDU frame and panel assembly	1016903	Below IMU control panel
Coupling display unit	CDU (ISS)	1015500-021	In CDU frame and panel assembly below IMU control panel
	CDU (OSS)	1015500-031	
Apollo guidance computer navigation panel display and keyboard	AGC navigation panel DSKY	1003706	To right of condition annunciator and OUA
Apollo guidance computer main panel display and keyboard	AGC main panel DSKY	1003707	On main control panel of command module
Guidance and navigation harness and PSA end connector assembly	G and N harness	1015086	Behind G and N indicator control panel
Display and control electronics assembly	D and C electronics	1015065	Behind G and N indicator control panel
Control electronics assembly	control electronics	1015064	Behind G and N indicator control panel
Signal conditioner assembly	signal conditioner	1007121	Behind G and N indicator control panel
Tracker X and Y electronics assembly	tracker electronics	1007585	On spacecraft secondary structure

(Sheet 2 of 2)





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Figure 3-1. G and N System

### 3-2 NAVIGATION BASE AND OPTICAL UNIT ASSEMBLY

The nav base and optical unit assembly (figure 3-2) consists of the nav base, optical unit assembly, bellows, seals, and vibration isolators.

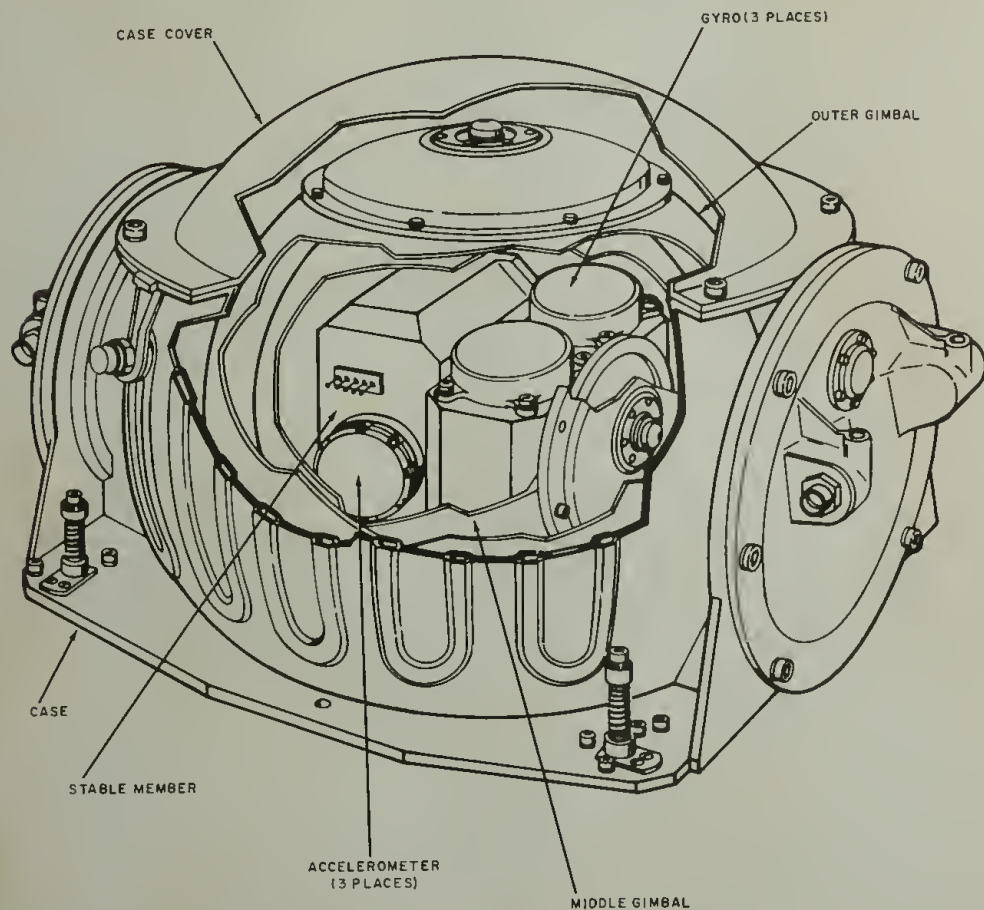
**3-2.1 NAVIGATION BASE FRAME ASSEMBLY.** The nav base provides mounting facilities for the optical unit and the IMU. It is machined from a single block of beryllium to achieve optimum strength-to-weight ratio and to insure accurate alignment of the OUA and IMU. The nav base is shock-mounted behind the G and N indicator control panel, along the inner conical surface of the command module.

**3-2.2 OPTICAL UNIT ASSEMBLY.** The OUA consists of two optical instruments, a sextant (SXT) and a scanning telescope (SCT), mounted on a common optical base. (See figure 3-3.) The base is rigidly mounted to the nav base in position over the IMU. Three precision ball mounts on the optical base provide for mounting the OUA to the nav base. Two bellows function as flexible seals between the inner shell of the spacecraft and the housings of the SXT and SCT.

**3-2.2.1 Optical Base.** The optical base is a precisely machined beryllium casting which provides for mounting and supporting the shaft axis drive and control components of the SXT and SCT. Internal components of the base are sealed by SXT and SCT panels (figure 3-3) which provide mountings for the SXT and SCT eyepiece assemblies. Two windows in the SCT panel assembly provide for viewing the indications of the SCT shaft and trunnion mechanical angle counters. To allow manual positioning of the SCT trunnion and shaft axes in the event of servo positioning loop failure, the SCT panel is equipped with conventional adapters to accept positioning tools.

**3-2.2.2 Sextant.** The SXT assemblies are contained within a cylindrical housing which protrudes outward from the optical base. (See figure 3-4.) The housing contains optical components, trunnion drive assemblies and SXT head tracker, and horizon photometer electronic components. The SXT head assembly is protected by an aluminum alloy head cover. Two apertures are cut into the head cover assembly. An elongated aperture extending to the periphery of the cover permits unobstructed lines-of-sight for both the SXT and tracker assemblies through their entire operating ranges. A small circular aperture located at the upper left of the cover affords a full line of sight for the horizon photometer.

**3-2.2.3 Scanning Telescope.** The SCT assemblies are contained within a cylindrical housing which protrudes outward from the optical base. (See figure 3-4.) The housing contains optical and trunnion drive assemblies. The SCT head assembly is protected by a counterweight and cover assembly. This assembly has an elongated aperture which allows an unobstructed line-of-sight through the entire SCT operating range.



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Figure 3-5. IMU

3-3.2 MIDDLE GIMBAL. The middle gimbal (MG) is a mechanical link between the stable member and the outer gimbal (OG). The middle and outer gimbal ADA's and their pre-amplifiers are mounted on the middle gimbal. Two 40 contact slip ring assemblies carry electrical signals between the middle gimbal and outer gimbal. A dc torque motor and a 1X resolver are mounted in tandem at one end of the gimbal, and a 16X resolver and dc torque motor at the other end.

3-3.3 OUTER GIMBAL. The outer gimbal supports the middle gimbal and revolves within the IMU case. Two 50 contact slip rings route electrical signals to and from the case. Two axial blowers, mounted on the outer gimbal, circulate air between the middle gimbal and the inner wall of the case.

3-3.4 IMU CASE. A liquid cooled case contains the three gimbal system. Attachment of the outer gimbal to the case is similar to the inter-gimbal mountings described in paragraphs 3-3.1 through 3-3.3. Two electrical connectors at each end of the case connect the IMU to the G and N harness. A water-glycol coolant solution from G and N coolant circuit number one is circulated through passages in the case to maintain a constant temperature range. Coolant supply and return lines are attached at quick-disconnect fittings on the IMU case.

#### 3-4 POWER AND SERVO ASSEMBLY

The PSA (see figure 3-6) contains encapsulated electronic circuitry for the inertial and optical subsystems. Ninety modules are mounted on ten nickel-plated, magnesium alloy trays. Each tray has a locating tongue which fits into a groove in the PSA end connector assembly to assure proper alignment of electrical connectors. The tapered tongue also helps maintain physical contact between the base of the tray and the thermal interface material which transmits heat to the coldplate. Each tray has a captive fastening screw and an electrical connector at the front end for interface with GSE. Table 3-II shows the location of all modules and briefly describes their functions.

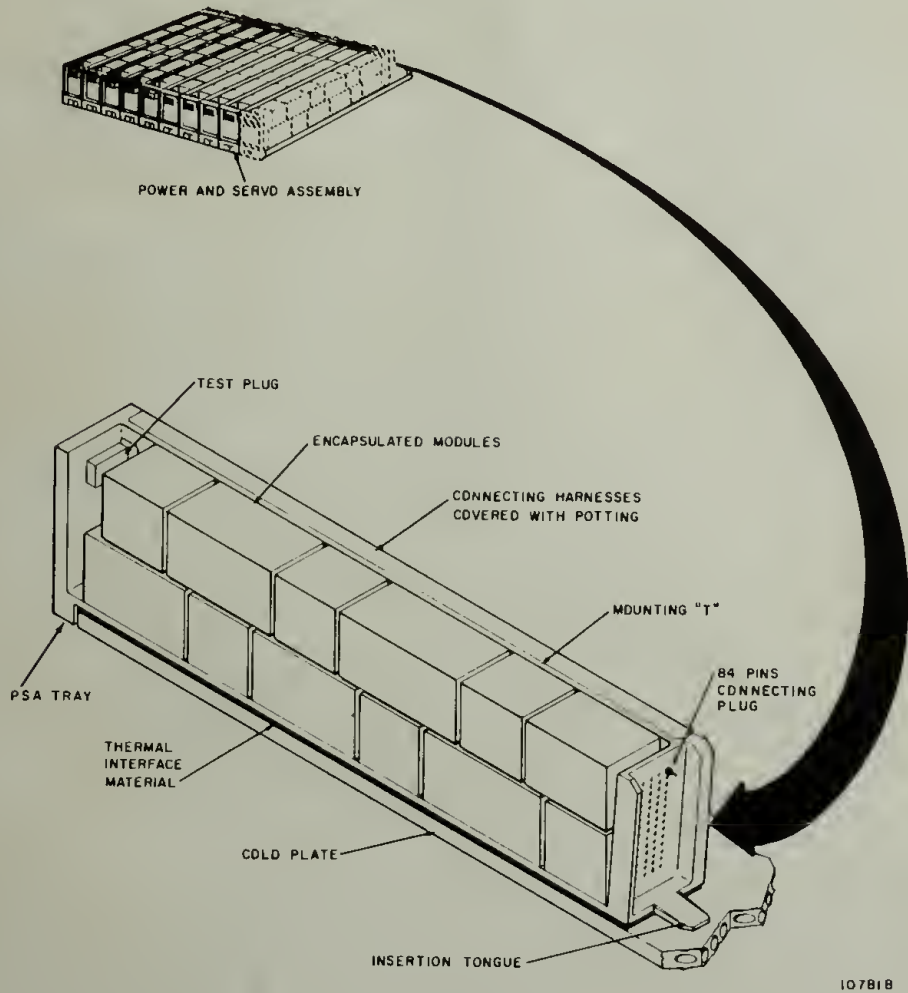
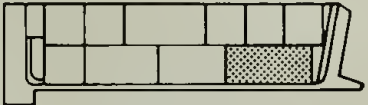
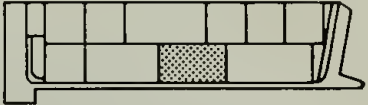
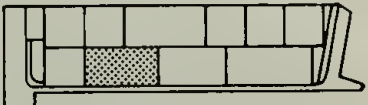
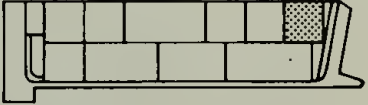

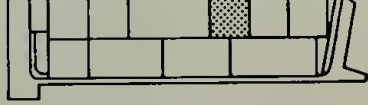


Figure 3-6. PSA

Table 3-II. Location and Functions of PSA Modules

Module Part Number	Module Assembly Name and Function	Location
1007540-021	Gimbal Servo Amplifier - Demodulates and amplifies inner gimbal error signals and supplies correction signals to inner gimbal torque motor.	Tray 1, Part Number 1007571, Gimbal Servo Electronics Assembly  14481-1
1007540-021	Gimbal Servo Amplifier - Amplifies middle gimbal error signals and supplies correction signals to middle gimbal torque motor.	
1007540-021	Gimbal Servo Amplifier - Amplifies outer gimbal error signals and supplies correction signals to outer gimbal torque motor.	
1007541-021	Gimbal Coarse Alignment Amplifier - Demodulates and amplifies IG CDU resolver output signal and supplies signal to inner gimbal servo amplifier during coarse align mode.	
1007541-021	Gimbal Coarse Alignment Amplifier - Amplifies MG CDU resolver output signals and supplies signals to middle gimbal servo amplifier during coarse align mode.	
1007541-021	Gimbal Coarse Alignment Amplifier - Amplifies OG CDU resolver output signals and supplies signal to outer gimbal servo amplifier during coarse align mode.	






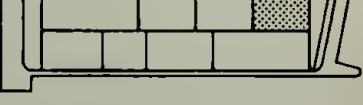
(Sheet 1 of 15)

Table 3-II. Location and Functions of PSA Modules (cont)

Module Part Number	Module Assembly Name and Function	Location
Tray 1 (cont)		
1007542-011	-28 VDC Power Supply - Supplies -27.5 vdc bias voltage for various PSA modules.	
1007543-021	3200 CPS AAC, Filter and Multivibrator - Supplies and regulates 3200 cps voltage to 3200 cps 1% power amplifier and to temperature controller power supply.	
1007544-011	3200 CPS 1% Power Amplifier - Supplies 3200 cps ducosyn excitation voltage.	
1007545-021	Temperature Controller Power Supply - Supplies 20 volt rms square wave to IMU temperature control circuits.	
Tray 2, Part Number 1007572, Power Supply Electronics Assembly		
1007546-011	800 CPS AAC, Filter and Multivibrator - Supplies and regulates 800 cps voltage to 1% power amplifier.	
1007547-011	800 CPS 1% Power Amplifier - Supplies 28 volt, 800 cps power for the 5% power amplifier, for excitation of resolvers and CDU tachometers, for input to motor drive amplifier during slewing, for autopilot reference, and for coarse align demodulator.	

14481-2

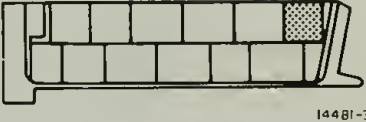





Table 3-II. Location and Functions of PSA Modules (cont)

Module Part Number	Module Assembly Name and Function	Location
Tray 2 (cont)		
1007548-011	800 CPS 5% Power Amplifier - Supplies 28 volt, 800 cps power for gyro wheel excitation through the IMU load compensation module.	
1007549-021	25.6 KC Encoder Excitation Power Supply - Supplies 25.6 kc excitation for optics CDU encoders.	
1007549-021	25.6 KC Power Supply - Supplies 25.6 kc excitation for IMU CDU encoders.	
1007551-011	Failure Indicator - Detects failure and supplies operating power for IMU, CDU, AGC, or accelerometer failure lamps. Supplies 102.4 kc failure indication pulses to AGC.	
1007552-011	Pulse Torquing Power Supply - Supplies +120 and +32 vdc and regulated +12 (±0.25) vdc for gyro pulse torquing.	
1007550	IMU - CDU Load Compensation - Corrects power factor of power supply load and converts 800 cps 5% power to two phase power for gyro wheel excitation.	

(Sheet 3 of 15)


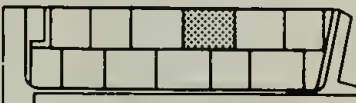

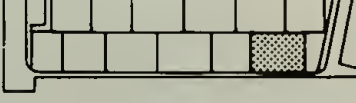




Table 3-II. Location and Functions of PSA Modules (cont)

Module Part Number	Module Assembly Name and Function	Location
1007507-021	DC Differential Amplifier and Precision Voltage Reference - Supplies a precision reference voltage for X IRIG pulse torquing current control.	Tray 3, Part Number 1007573, Gyro and Accelerometer Electronics Assembly 
1007507-021	DC Differential Amplifier and Precision Voltage Reference - Supplies a precision reference voltage for Y PIPA pulse torquing current control.	
1007507-021	DC Differential Amplifier and Precision Voltage Reference - Supplies a precision reference for X PIPA pulse torquing current control.	
1007509-021	X PIPA Calibration - Contains torque compensation and scale factor networks for the X PIPA. Matched with X PIPA in IMU.	
1007509-021	Y PIPA Calibration - Contains torque compensation and scale factor networks for the Y PIPA. Matched with Y PIPA in IMU.	
1007517-011	AC Differential Amplifier - Amplifies the X PIPA signal.	







(Sheet 4 of 15)

Table 3-II. Location and Functions of PSA Modules (cont)

Module Part Number	Module Assembly Name and Function	Location
Tray 3 (cont)		
1007517-011	AC Differential Amplifier - Amplifies the Y PIPA signal.	
1007519-011	Interrogator - Converts amplified X PIPA signal generator output to digital torque commands.	
1007519-011	Interrogator - Converts amplified Y PIPA signal generator output to digital torque commands.	
1007521-021	Pulse Torque Gyro Calibration - Contains torque compensation and scale factor networks for the X IRIG. Matched with X IRIG in IMU.	
1007527-021	Binary Current Switch - Switches constant current pulses between X PIPA torque generators to null the X PIPA loop. Supplies pulses to the forward - backward counter to indicate velocity changes.	
1007527-021	Binary Current Switch - Switches constant current pulses between Y PIPA torque generators to null the Y PIPA loop. Supplies pulses to the forward - backward counter to indicate velocity changes.	



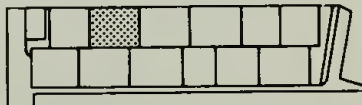

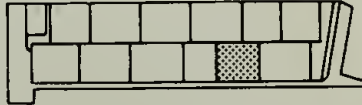

(Sheet 5 of 15)

Table 3-II. Location and Functions of PSA Modules (cont)

Module Part Number	Module Assembly Name and Function	Location
1007507-021	DC Differential Amplifier and Precision Voltage Reference - Supplies a precision reference voltage for Y IRIG pulse torquing current control.	Tray 4, Part Number 1007574, Gyro and Accelerometer Electronics Assembly  14481-4
1007507-021	DC Differential Amplifier and Precision Voltage Reference - Supplies a precision reference voltage for Z IRIG pulse torquing current control.	
1007507-021	DC Differential Amplifier and Precision Voltage Reference - Supplies a precision reference voltage for Z PIPA pulse torquing current control.	
1007509-021	Z PIPA Calibration - Contains torque compensation and scale factor networks for the Z PIPA. Matched with Z PIPA in the IMU.	
1007516-011	Ternary Current Switch - Switches current pulses to the X IRIG torque generator to control gimbal position.	
1007516-011	Ternary Current Switch - Switches current pulses to the Y IRIG torque generator to control gimbal position.	


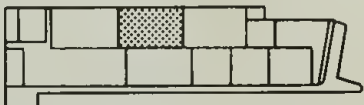
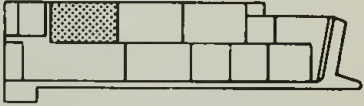


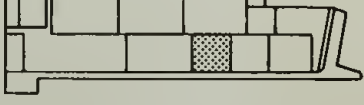
(Sheet 6 of 15)

Table 3-II. Location and Functions of PSA Modules (cont)

Module Part Number	Module Assembly Name and Function	Location
Tray 4 (cont)		
1007516-011	Ternary Current Switch - Switches current pulses to the Z IRIG torque generator to control gimbal position.	
1007517-011	AC Differential Amplifier - Amplifies the Z PIPA signal.	
1007519-011	Interrogator - Converts amplified Z PIPA signal generator output to digital torque commands.	
1007521-021	Pulse Torque Gyro Calibration - Contains torque generator compensation and scale factor networks for Y IRIG. Matched with Y IRIG in IMU.	
1007521-021	Pulse Torque Gyro Calibration - Contains torque generator compensation and scale factor networks for Z IRIG. Matched with Z IRIG in IMU.	
1007527-011	Binary Current Switch - Switches constant current torque pulses between the Z PIPA torque generator windings to null the Z PIPA loop. Supplies pulses to the forward - backward counter to indicate velocity changes.	

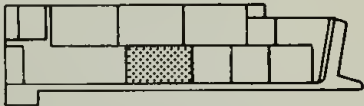


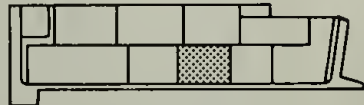
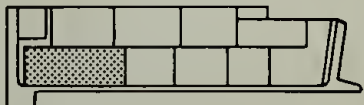
(Sheet 7 of 15)

Table 3-II. Location and Functions of PSA Modules (cont)

Module Part Number	Module Assembly Name and Function	Location
		<p>Tray 5, Part Number 1007575, CDU and Gyro Accelerometer Electronics Assembly</p>
1007554-011	Encoder - Converts IG CDU signals to digital information.	 <p style="text-align: right;">14481 5</p>
1007554-011	Encoder - Converts MG CDU signals to digital information.	
1007554-011	Encoder - Converts OG CDU signals to digital information.	
1007555-011	CDU Digital to Analog Converter - Converts AGC digital outputs to analog signals for use in IG CDU.	
1007555-011	CDU Digital to Analog Converter - Converts AGC digital outputs to analog signals for use in MG CDU.	
1007555-011	CDU Digital to Analog Converter - Converts AGC digital outputs to analog signals for use in OG CDU.	

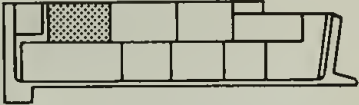



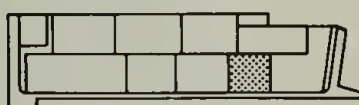


(Sheet 8 of 15)

Table 3-II. Location and Functions of PSA Modules (cont)

Module Part Number	Module Assembly Name and Function	Location
1007558	Forward - Backward Counter and Computer Output - Removes redundant velocity information from PIPA pulses and supplies the resultant incremental velocity pulses to the AGC.	Tray 5 (cont) 
1007561	CDU Zeroing and Lock Relays - Shorts out the sine windings of the IG and MG CDU 1X resolvers. Removes 28 vdc from CDU motor drive amplifier in CDU manual mode. Informs AGC of CDU manual mode operation.	
1007546-011	800 CPS AAC, Filter and Multivibrator - Supplies and regulates 800 cps voltage to 800 cps 1% power amplifiers.	Tray 6, Part Number 1007576, CDU and Power Supply Electronics Assembly 
1007547-011	800 CPS 1% Power Amplifier - Supplies 28 volt, 800 cps power for optics CDU tachometer and resolver excitation. Supplies power to the 800 cps 5% power amplifier.	14481-6 
1007548-011	800 CPS 5% Power Amplifier - Supplies 28 volt, 800 cps power for optics CDU servomotor excitation and for sextant power.	


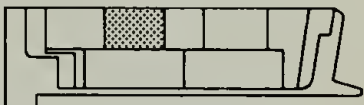

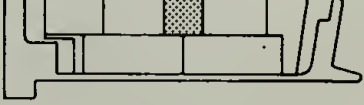


(Sheet 9 of 15)

Table 3-II. Location and Functions of PSA Modules (cont)

Module Part Number	Module Assembly Name and Function	Location
Tray 6 (cont)		
1007557-011	Motor Drive Amplifier and Selector Circuit - Supplies polarized 800 cps power to drive the OG CDU motor.	
1007557-011	Motor Drive Amplifier and Selector Circuit - Supplies polarized 800 cps power to drive the IG CDU motor.	
1007557-011	Motor Drive Amplifier and Selector Circuit - Supplies polarized 800 cps power to drive the MG CDU motor.	
1007510-011	CDU Resolver Loads - Provides load compensation for CDU resolvers.	
1007564-011	CDU Zeroing Transformer, Relays, and Entry Relays - Provides circuitry and relay switching to zero the CDU's.	
Tray 7, Part Number 1007577, Miscellaneous Electronics Assembly		
1007552-011	Pulse Torquing Power Supply - Supplies +32 and +120 vdc for accelerometer pulse torquing.	
1007218-011	Precision Voltage Regulator Delay Module - Allows 6 second time delay in 32 volt pulse torque supply.	

14481-7

Table 3-II. Location and Functions of PSA Modules (cont)

Module Part Number	Module Assembly Name and Function	Location
Tray 7 (cont)		
1007554-011	Encoder - Converts shaft CDU signals to digital information.	
1007554-011	Encoder - Converts trunnion CDU signals to digital information.	
1007556-011	IMU Temperature Controller - Contains circuitry for automatic control of IMU temperature.	
1007563-011	CDU Fixed Resolution Transformation and Entry Mode Assembly - Provides fixed resolution transformation to compensate for the displacement of spacecraft axes and step-down transformer for roll body offset error signal during entry.	
1007518-011	IMU Temperature Indicating Alarm and Backup Controller - Supplies signals which indicate an out of tolerance temperature in the IMU. Contains a backup temperature control circuit.	
Tray 8, Part Number 1007578, Optical Electronics Assembly		
1007555-011	CDU Digital to Analog Converter - Converts AGC digital outputs to analog form for use in the shaft CDU.	

14481-8



Table 3-II. Location and Functions of PSA Modules (cont)




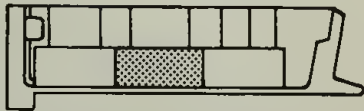

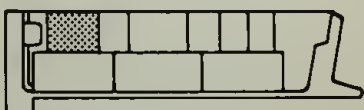





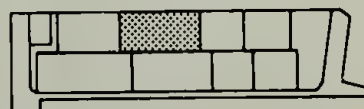
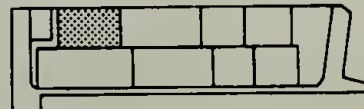

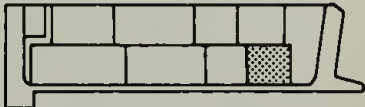


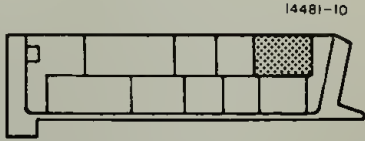

Module Part Number	Module Assembly Name and Function	Location
Tray 8 (cont)		
1007555-011	CDU Digital to Analog Converter - Converts AGC digital outputs to analog form for use in the trunnion CDU.	
1007522-011	Two Speed Switch - Provides signal selection for switching null-seeking servo loops from coarse to fine synchro error detection.	
1007581-011	Motor Drive Amplifier - Drives the SCT shaft motor.	
1007581-011	Motor Drive Amplifier - Drives the SXT shaft motor.	
1007581-011	Motor Drive Amplifier - Drives the SXT trunnion motor.	
1007526	Buffer Circuit - Isolates optics test points.	
1007567	Relay - Provides relay switching of optics control.	

Table 3-II. Location and Functions of PSA Modules (cont)

Module Part Number	Module Assembly Name and Function	Location
1007528	SCT Moding - Provides a fixed input to the SCT 1X resolver corresponding to a 25 degree offset in the SCT and provides optics moding capability.	Tray 8 (cont) 
1007522	Two Speed Switch - Provides signal selection for switching null-seeking servo loops from coarse to fine synchro error detection.	Tray 9, Part Number 1007579, Optical Electronics Assembly 
1007581	Motor Drive Amplifier - Drives the trunnion CDU motor.	 14481-9
1007581	Motor Drive Amplifier - Drives the shaft CDU motor.	
1007581	Motor Drive Amplifier - Drives the SCT trunnion motor.	
1007526	Buffer Circuit - Isolates optics test points.	

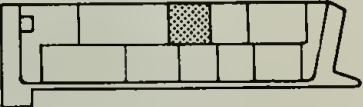

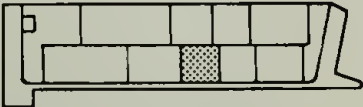
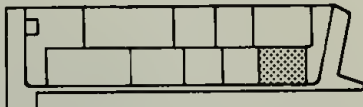
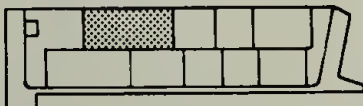
(Sheet 13 of 15)

Table 3-II. Location and Functions of PSA Modules (cont)

Module Part Number	Module Assembly Name and Function	Location
1007567	Relay - Provides relay switching of optics control.	Tray 9 (cont) 
1007524	Cosecant Generator - Maintains the image trace of the optics at a constant rate regardless of trunnion angle in the resolved mode.	
1007651	Resolver Drive Amplifier - Provides buffering and phase shift between the optics hand controller and the 1X resolver.	
1007548-011	800 CPS 5% Power Amplifier - Supplies 28 volt, 800 cps power for IMU blowers and CDU drive motors.	Tray 10, Part Number 1007580, Power Diodes and Signal Conditioning Electronics Assembly 
1007590-011	G and N Subsystem Supply Filter - Filters 28 vdc IMU operating voltage and supplies 27 vdc to condition lamps on the condition annunciator.	
1007590-011	G and N Subsystem Supply Filter - Filters 28 vdc IMU standby voltage and supplies 27 vdc to condition lamps on the condition annunciator.	

(Sheet 14 of 15)

Table 3-II. Location and Functions of PSA Modules (cont)

Module Part Number	Module Assembly Name and Function	Location
Tray 10 (cont)		
1007590-011	G and N Subsystem Supply Filter - Filters 28 vdc optics operating voltage and supplies 27 vdc to condition lamps on the condition annunciator.	
1007591-011	800 CPS Compensation - Provides capacity compensation to counteract inductive loading on the 800 cps 1% and 5% power supplies.	
1007511-011	Modulator and Loop Compensation - Converts star tracker dc output signals to suppressed carrier ac signals and provides servo loop frequency compensation.	
1007525-011	Signal Conditioner Power Supply - Provides 20 and 2.5 vdc power for the signal conditioner assembly and 28 vdc excitation voltage for IMU pressure transducer.	
1007559-011	Photometer Electronics - Sends a star presence signal to the AGC when a star is in the star tracker field of view and when the horizon photometer has reached 1/2 peak intensity of the earth's limb (blue line).	

(Sheet 15 of 15)

APOLLO GUIDANCE AND NAVIGATION SYSTEM

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## 3-5 APOLLO GUIDANCE COMPUTER

The AGC (figure 3-7) consists of two flat tray assemblies bolted back to back. The tray assemblies, as a unit, measure approximately 22 by 15 by 5.5 inches. The unit is mounted on a base coldplate which is a part of the spacecraft. The base coldplate is an aluminum alloy, liquid cooled, honeycombed structure which dissipates heat generated by the AGC.

3-5.1 LOGIC TRAY A. The logic tray A assembly (figure 3-8) contains 40 modules: 36 logic modules and four interface modules. All modules are mounted on the tray and then potted with a silastic compound. The side of the tray that faces the other tray is also potted.

Tray A has three connectors: two on the front and one on the rear. A 360 pin front connector connects the AGC to the DSKY's, to other parts of the G and N system, and to other spacecraft systems. A 126 pin front connector provides interface with ground support equipment. The 172 pin rear connector provides interface between tray A and tray B.

3-5.2 MEMORY TRAY B. The memory tray B assembly (figure 3-9) contains 25 modules. All modules are potted into the tray except the rope modules. The four rope modules are protected by a cover which bolts to the tray. A STBY/ON (standby) switch mounted on the front of tray B provides a standby mode of operation for conservation of power.

Tray B has two connectors: one front and one rear. The 19 pin front connector connects the AGC to the main power source of 28 volts dc. The 172 pin rear connector provides interface between trays A and B.

## 3-6 COUPLING DISPLAY UNIT

Five CDU's are used in the G and N system. Two, part number 1015500-031, provide angle readouts for the trunnion and shaft of the sextant. Three, part number 1015500-021, control the positions of and provide angle readouts for the inner, middle, and outer gimbals of the IMU.

The CDU contains a motor-tachometer, four resolvers, a digital encoder, a two pole three position switch, (in part number 1015500-021 only) display dials, gearing, and electronic circuitry. Figure 3-10 shows major parts.

## 3-7 DISPLAY AND CONTROL ELECTRONICS

The display and control electronics (D and C electronics) (figure 3-11) is an auxiliary chassis which holds six encapsulated modules. The modules and their functions are listed in table 3-III.

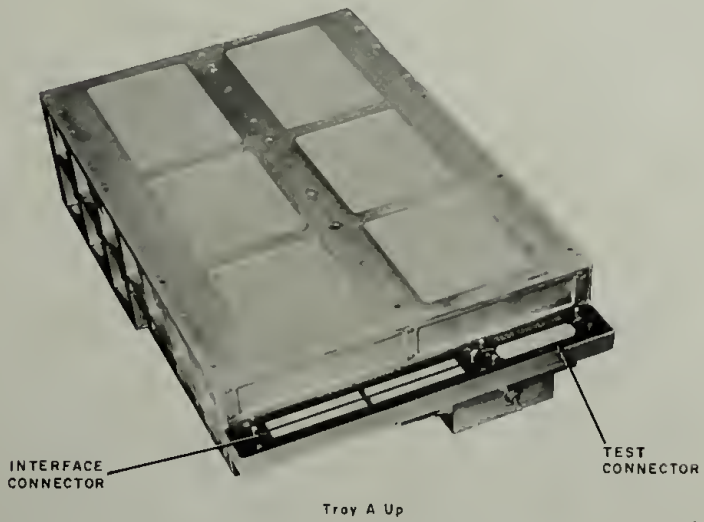


Figure 3-7. AGC



Figure 3-8. Logic Tray A

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Figure 3-9. Memory Tray B

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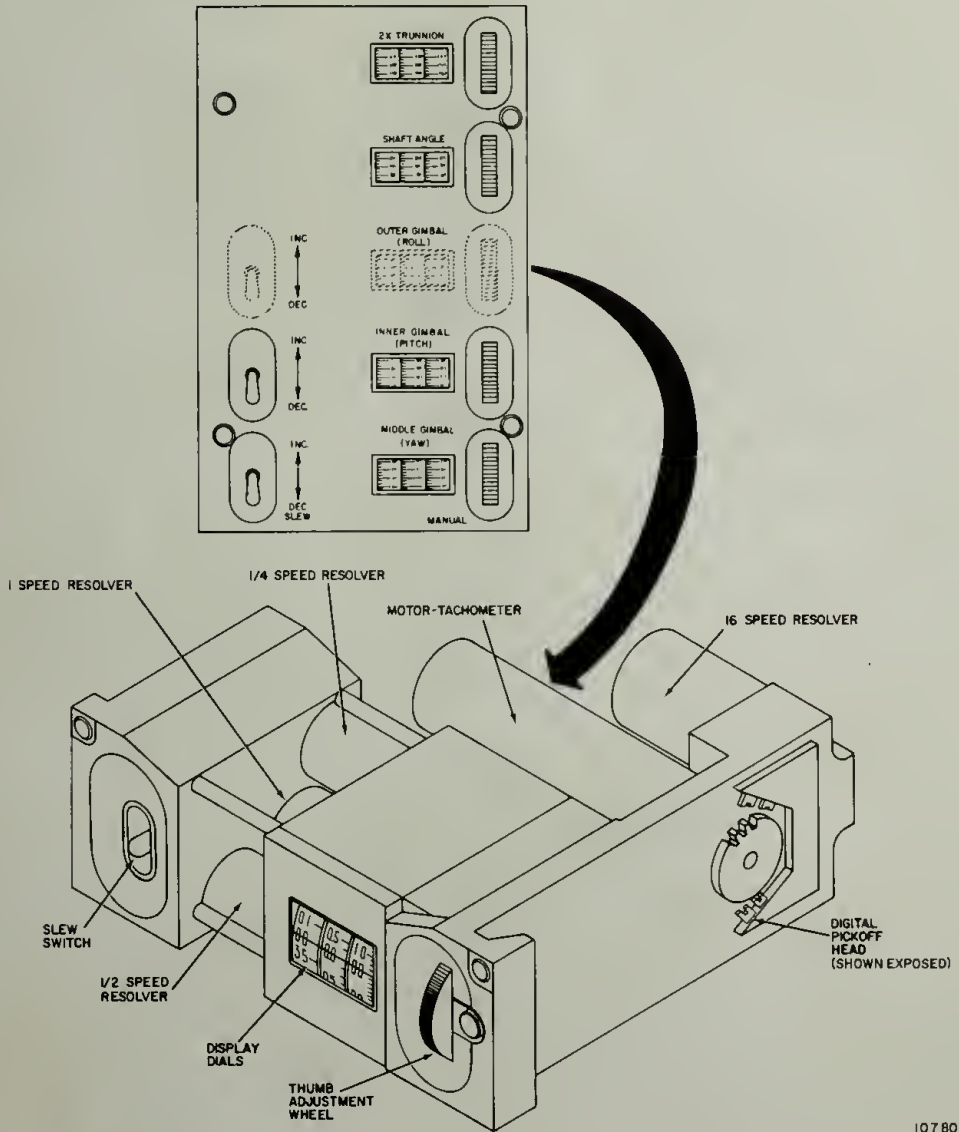
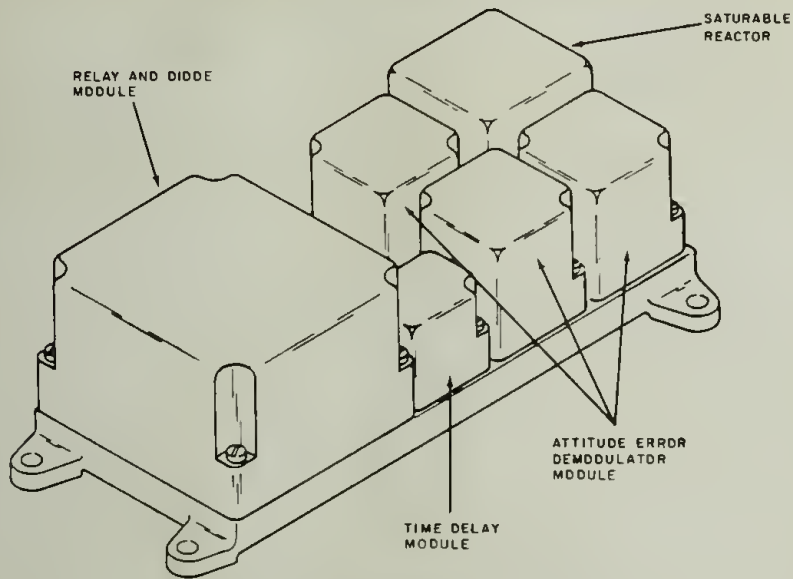


Figure 3-10. CDU





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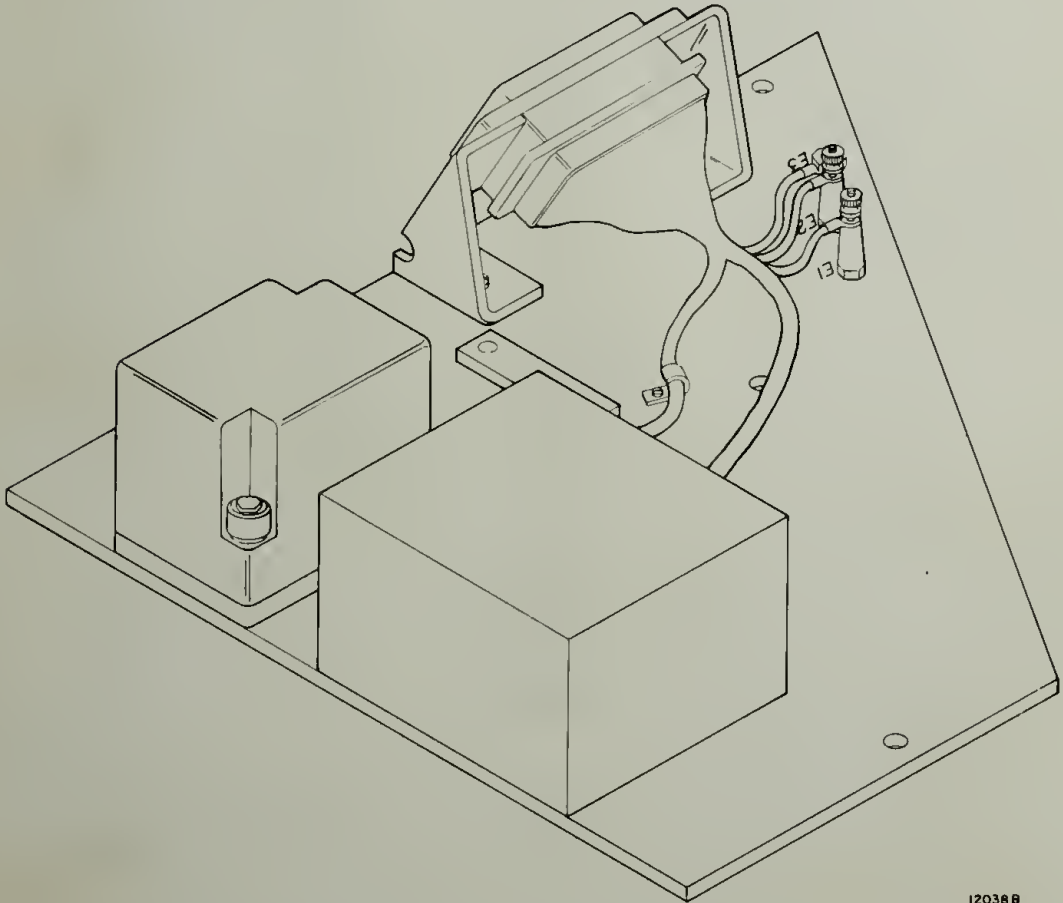
Figure 3-11. D and C Electronics

Table 3-III. Functions of D and C Electronics Modules

Module Number	Function
1015038-021	Time Delay - Prevents power from being applied to IMU torque generators until power has been applied to gyro wheels for 100 seconds.
1014638 (3 required)	Attitude Error Demodulator - Supplies signal to IMU control panel IMU-CDU DIFFERENCE meter.
1015036-011	Relay and Diode Module - Contains circuitry used in conjunction with the IMU control panel for manual control of IMU and with AGC for computer control of IMU.
1010455	Saturable Reactor - Supplies 0 to 6.3 volts, 400 cps power to D and C panel lamps. (The DC control winding is controlled by the BRIGHTNESS control on the G and N indicator control panel.)

3-8 CONTROL ELECTRONICS

The control electronics (figure 3-12) is an auxiliary chassis which provides a relay and diode module for switching of gimbal lock lamps. It also provides a transformer which supplies power for testing and operating lamps in the lower display and control group.

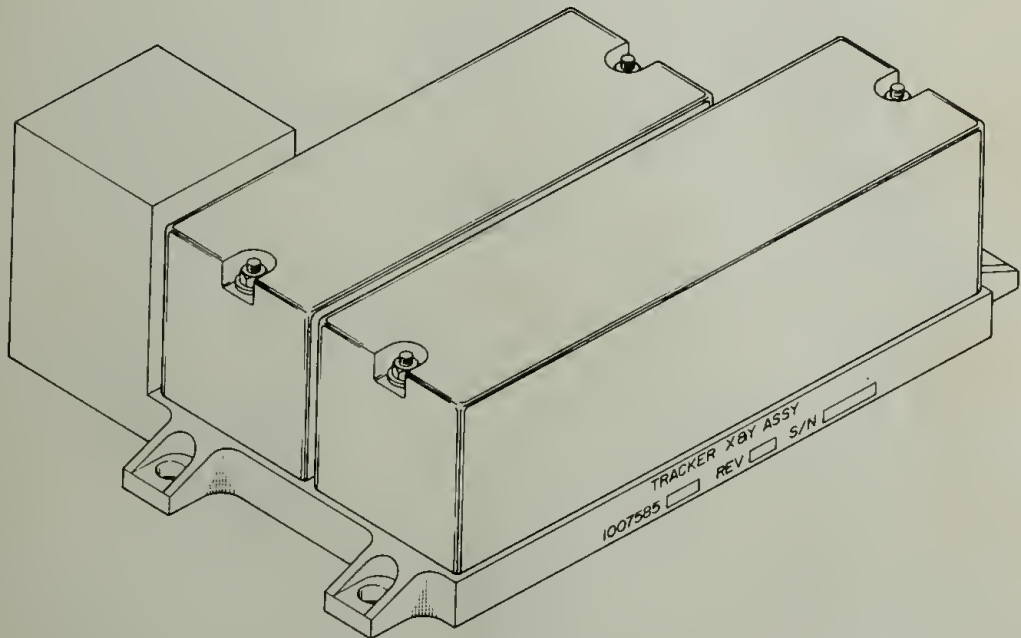


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Figure 3-12. Control Electronics

## 3-9 TRACKER ELECTRONICS

The tracker electronics (figure 3-13) is mounted on the secondary structure of the command module above the OUA. This unit receives star tracker outputs from the sextant and generates servo drive signals to position the SXT S<sub>t</sub>LOS in terms of shaft and trunnion angles.



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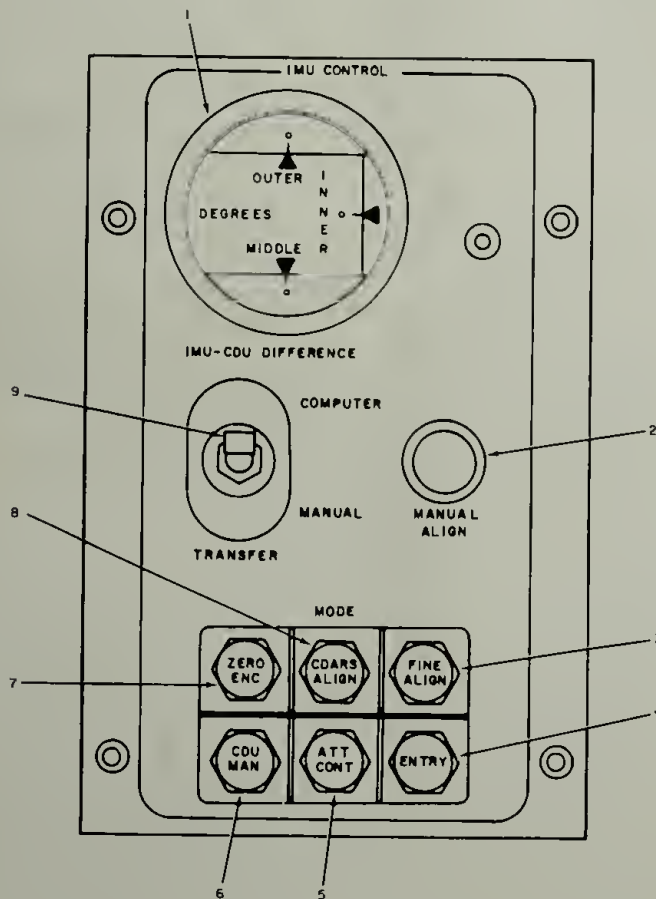
Figure 3-13. Tracker Electronics

## 3-10 DISPLAYS AND CONTROLS

Through the use of lamp brightness controls on the G and N panels, the displays are readable under all light conditions. Indicator lamps are incorporated within the pushbuttons to indicate switch positions. The toggle switches are recessed to prevent accidental operations.

3-10.1 IMU CONTROL PANEL. The IMU control panel (figure 3-14) provides a means for controlling and monitoring IMU modes and for selecting either manual or AGC control of the IMU. Figure 3-14 illustrates and describes the displays and controls.

3-10.2 CONDITION ANNUNCIATOR. The condition annunciator (figure 3-15) is a panel of warning, caution, and status lamps. The panel is located above the upper left corner of the optical unit. Figure 3-15 illustrates and describes the condition lamps which are mounted on the panel.



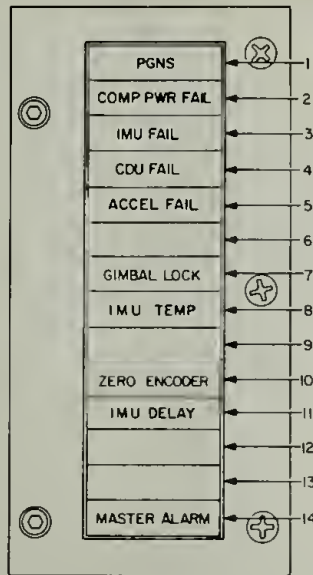
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Figure 3-14. IMU Control Panel (Sheet 1 of 2)

## APOLLO GUIDANCE AND NAVIGATION SYSTEM

Index Number	Control or Indicator	Function
1	IMU-CDU DIFFERENCE meter	Indicates differences between outer, inner, and middle gimbal axis angles and their respective CDU angle indications.
2	MANUAL ALIGN pushbutton	Energizes coarse align relay when TRANSFER switch is in MANUAL position.
3	FINE ALIGN pushbutton	Energizes fine align relay to allow fine alignment of IMU.
4	ENTRY pushbutton	Energizes entry relay to permit automatic positioning of spacecraft for entry.
5	ATT CONT pushbutton	Deenergizes all relays to permit AGC control of spacecraft attitude.
6	CDU MAN pushbutton	Energizes CDU manual relay to allow manual positioning of CDU's.
7	ZERO ENC pushbutton	Energizes zero encoder relay and fine align relay to allow CDU zeroing.
8	COARS ALIGN pushbutton	Energizes coarse align relay to allow IMU coarse alignment.
9	TRANSFER switch	Determines method of IMU control: manual or AGC.

Figure 3-14. IMU Control Panel (Sheet 2 of 2)



14711A

Index Number	Control or Indicator	Function
1	PGNS lamp	Indicates malfunctions in primary G and N system equipment.
2	COMP PWR FAIL lamp	Indicates loss of -10 volt, -3 volt, or +28 volt power within the AGC.
3	IMU FAIL lamp	Indicates IMU gimbal servo error failure or loss of 3,200 cps power, gyro wheel power, or -28 volt dc power within the IMU.
4	CDU FAIL lamp	Indicates a loss of 25.6 kilocycle power, loss of CDU motor excitation, or a CDU gimbal error.
5	ACCEL FAIL lamp	Indicates an accelerometer error failure.

Figure 3-15. Condition Annunciator (Sheet 1 of 2)

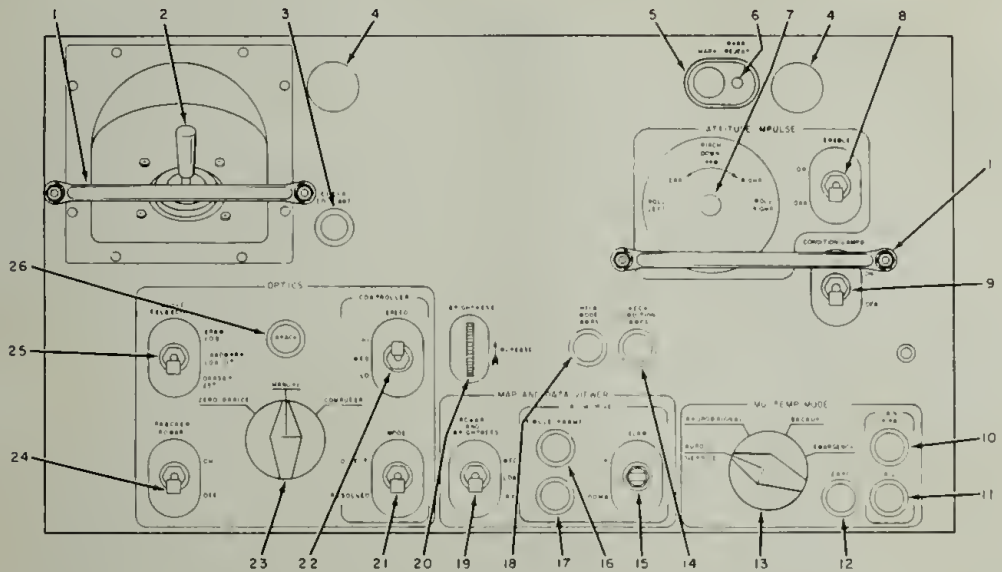
Index Number	Control or Indicator	Function
6	Spare	
7	GIMBAL LOCK lamp	Indicates when the angle between the outer and middle gimbal exceeds $\pm 60$ degrees, thus indicating a potential gimbal lock.
8	IMU TEMP lamp	Indicates that IMU temperature is deviating more than 4 degrees from normal in proportional control.
9	Spare	
10	ZERO ENCODER lamp	Indicates when the CDU's are being zeroed. Lamp goes out after a time delay.
11	IMU DELAY lamp	Indicates the 100 second IMU time delay following IMU turn-on
12	Spare	
13	Spare	
14	MASTER ALARM lamp	Indicates failure in G and N system.

Figure 3-15. Condition Annunciator (Sheet 2 of 2)

3-10.3 G AND N INDICATOR CONTROL PANEL. The G and N indicator control panel (figure 3-16) provides displays and controls for the following functions:

- (1) IMU temperature control.
- (2) Manual spacecraft maneuvering.
- (3) Manual optics positioning.
- (4) Optics mode control.

Figure 3-16 illustrates and describes the displays and controls.



14714

Index Number	Control or Indicator	Function
1	Assist grip	Enables navigator to stabilize himself while operating panel in a zero gravity environment.
2	Optics hand controller	Supplies a signal to drive the optics about the shaft axis and/or trunnion axis in manual mode.
3	CHECK COOLANT pushbutton	Supplies power to lamps in back of panel to enable navigator to check for coolant leaks.
4	Observation window	Enables navigator to observe IMU coolant connections.
5	MARK pushbutton	When pressed, sends a signal to the AGC to record time and the optics and gimbal angles.

Figure 3-16. G and N Indicator Control Panel (Sheet 1 of 4)



## APOLLO GUIDANCE AND NAVIGATION SYSTEM

Index Number	Control or Indicator	Function
6	MARK REJECT pushbutton	Cancels inputs initiated by MARK pushbutton.
7	ATTITUDE IMPULSE hand control	Supplies signals to the stabilization and control system to position the spacecraft in attitude.
8	ATTITUDE IMPULSE ENABLE switch	Enables ATTITUDE IMPULSE hand control operation of spacecraft when ATTITUDE IMPULSE ENABLE switch is placed in ON position and when energized by stabilization and control system attitude control or G and N system attitude control signals.
9	CONDITION LAMPS switch	Disables all lamps on the condition annunciator except the MASTER ALARM lamp.
10	IMU TEMP MODE GAIN PIPA pushbutton	When pressed, connects a resistor to the PIPA temperature indicating bridge which produces an error signal (equivalent to +5 degrees temperature deviation) to light alarm indication lamps.
11	IMU TEMP MODE GAIN IRIG pushbutton	When pressed, connects a resistor to the IRIG temperature indicating bridge which produces an error signal (equivalent to -5 degrees temperature deviation) to light alarm indication lamps.
12	IMU TEMP MODE ZERO pushbutton	When pressed, connects two resistors equivalent to the bridge set point to the temperature indicating bridges so an error signal can not be produced.
13	IMU TEMP MODE selector	Provides selection of proportional, backup, or emergency heater control and provides, when in the auto override position, automatic switching from proportional to emergency control.

Figure 3-16. G and N Indicator Control Panel (Sheet 2 of 4)

Index Number	Control or Indicator	Function
14	CHECK CONDITION LAMPS pushbutton	Lights GIMBAL LOCK condition and IMU TEMP FAIL condition lamps when CONDITION LAMPS switch is in ON position.
15	MAP AND DATA VIEWER FILM DRIVE SLEW switch	Not used.
16	MAP AND DATA VIEWER FILM DRIVE SINGLE FRAME UP pushbutton	Not used.
17	MAP AND DATA VIEWER FILM DRIVE SINGLE FRAME DOWN pushbutton	Not used.
18	CHECK MODE LAMPS pushbutton	Supplies power to check mode lamps on IMU control panel and TRACK lamp on panel.
19	MAP AND DATA VIEWER POWER AND BRIGHTNESS switch	Not used.
20	Panel BRIGHTNESS control	Varies the dc power to the control winding of the D and C electronics saturable reactor to change lamp brightness.
21	OPTICS MODE CONTROLLER	Selects either direct or resolved positioning of the optics.
22	OPTICS SPEED CONTROLLER	Varies power for optics hand controller use.
23	OPTICS mode selector	Selects circuitry for either zeroing the optics, manual control of optics, or AGC control of optics.

Figure 3-16. G and N Indicator Control Panel (Sheet 3 of 4)

Index Number	Control or Indicator	Function
24	TRACKER POWER switch	Supplies power to sextant, controls trunnion CDU encoder granularity, and supplies discrete to AGC.
25	SLAVE TELESCOPE switch	Slaves the SCT to the SXT S <sub>t</sub> LLOS or the SXT LLOS, or offsets the SCT 25° in trunnion angle from the SXT LLOS.
26	TRACK pushbutton	Initiates automatic optics tracking when a star presence signal is present.

Figure 3-16. G and N Indicator Control Panel (Sheet 4 of 4)

3-10.4 AGC NAVIGATION PANEL DISPLAY AND KEYBOARD. The AGC navigation panel DSKY (figure 3-17) measures approximately 22 by 6 by 14 inches. It is divided into two sections: one section for displays and one section for the keyboard. The display section contains 12 failure indication lights, eight operation display lights, and 18 data display lights. Functions of the controls and indicators are given in Table 3-IV. Three interchangeable decoding modules are mounted at the rear of the display section. The keyboard section contains 19 keys and a brightness control. A case containing four interchangeable relay trays and a power supply module is mounted on the rear of the keyboard. Each of the relay trays consists of seven modules, each module containing six relays. The power supply module supplies the voltage required to light the display indicators.

3-10.5 AGC MAIN PANEL DISPLAY AND KEYBOARD. The AGC main panel DSKY (figure 3-17) measures approximately 10 by 9 by 7 inches and is mounted in the left hand side of the main instrument panel of the command module. The front panel contains 18 keys, two failure indication lights, a brightness control, and a toggle switch.

### 3-11 G AND N HARNESS

The G and N harness (figure 3-18) connects the G and N system to the spacecraft power supplies and electrically interconnects the G and N system components. These connections are made through a six branch wiring harness and PSA end connector assembly. Component connections are shown in table 3-IV.

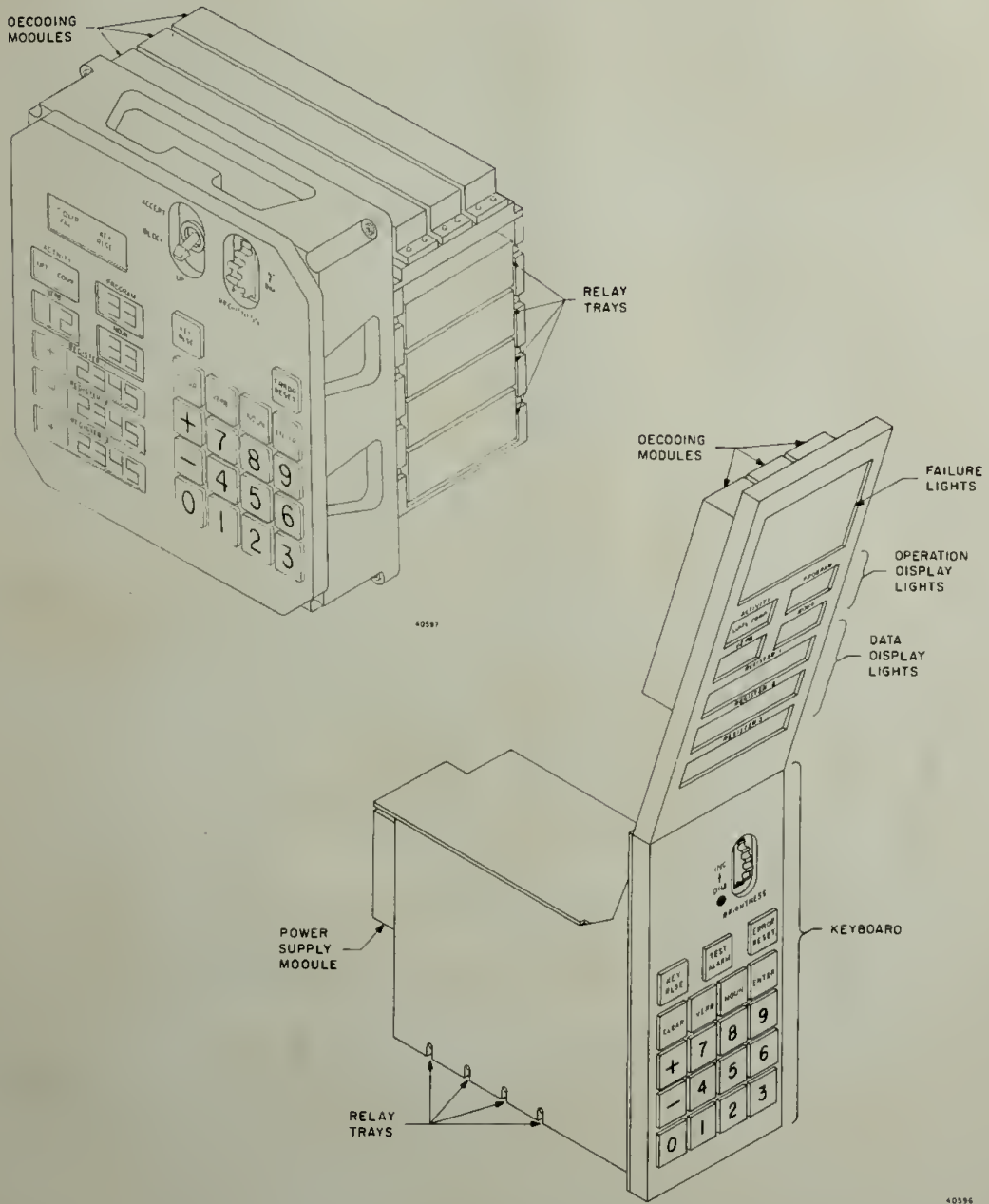


Figure 3-17. AGC Main and Navigation Panel Displays and Keyboards  
(Sheet 1 of 3)

## APOLLO GUIDANCE AND NAVIGATION SYSTEM

Control or Indicator	DSKY	Function
Failure lights	Navigation panel	Indicate which of eight possible alarms has occurred.
ACTIVITY lights	Navigation panel Main panel	Indicate information is being received via UPLINK and/or that a test condition is in progress.
PROGRAM lights	Navigation panel Main panel	Indicate which program the AGC is processing.
VERB lights	Navigation panel Main panel	Indicate verb code entered at keyboard.
NOUN lights	Navigation panel Main panel	Indicate noun code entered at keyboard.
Data display lights	Navigation panel Main panel	Displays pertinent data to astronaut. A plus or minus sign signifies data is decimal.
COMP FAIL light	Main panel	Indicates failure has occurred in the AGC.
CHECK FAIL light	Navigation panel	Indicates invalid keyboard operation.
TEST ALARM key	Navigation panel	Tests several failure lights to insure operation.
KEY RLSE key	Navigation panel Main panel	Releases displays initiated by the keyboard so that information supplied by program action may be displayed.
UP TL switch	Main panel	Controls reception of information via UPLINK.
BRIGHTNESS control	Navigation panel Main panel	Controls brightness of operation and data display lights.

Figure 3-17. AGC Main and Navigation Panel Displays and Keyboards  
(Sheet 2 of 3)

Control or Indicator	DSKY	Function
ERROR RESET key	Navigation panel Main panel	Clears failure lights tested when TEST ALARM key is used and tests for real alarm rather than transient alarm.
CLEAR key	Navigation panel Main panel	Clears data contained in data registers. Clears whichever display register is currently in use.
VERB key	Navigation panel Main panel	Conditions the AGC to interpret the next two numerical characters as an action request.
NOUN key	Navigation panel Main panel	Conditions the AGC to interpret the next two numerical characters as an address code.
ENTER key	Navigation panel Main panel	Informs the AGC that assembled data is complete; execute the requested function.
+ key	Navigation panel Main panel	Enters positive sign for decimal data.
- key	Navigation panel Main panel	Enters negative sign for decimal data.
0 through 9 keys	Navigation panel Main panel	Enters data, address code, and action request code into the AGC.

Figure 3-17. AGC Main and Navigation Panel Displays and Keyboards  
(Sheet 3 of 3)

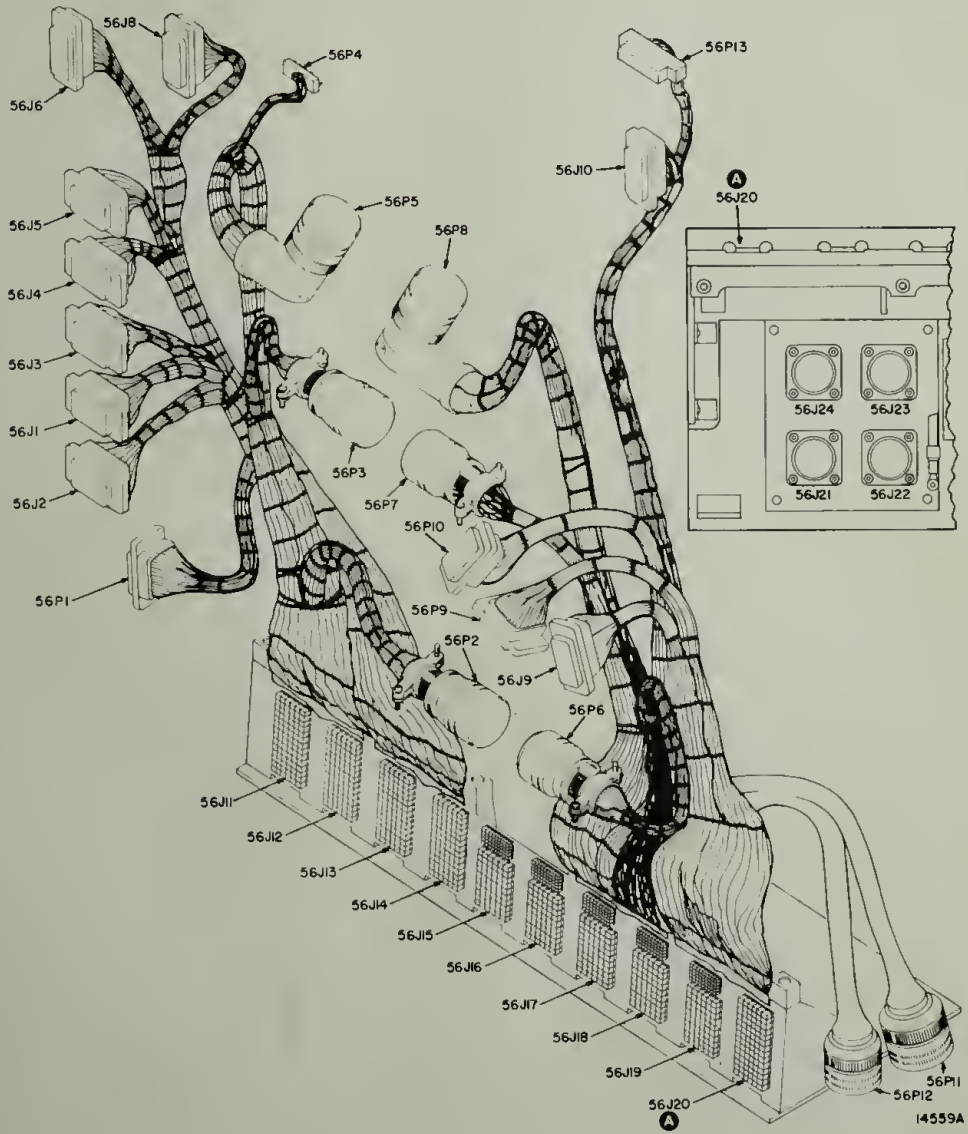


Figure 3-18. G and N Harness

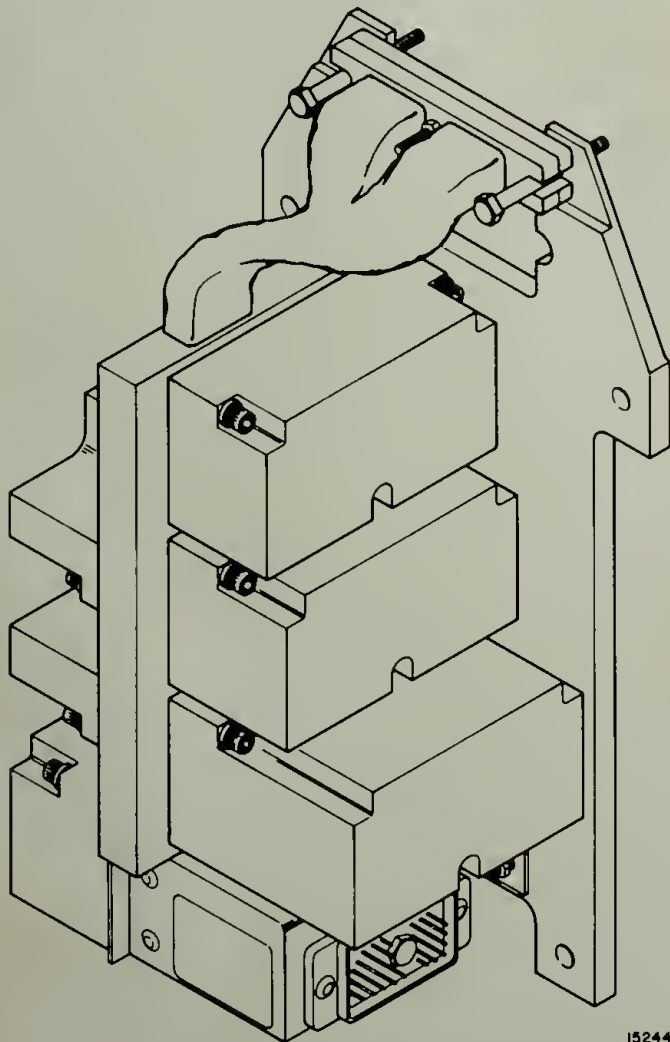
Table 3-IV. G and N Harness Connections

G and N Harness Connector	Component	Component Connector
56P1	D and C electronics	50A3J1
56P2	IMU	35J1
56P3	IMU	35J3
56P4	SXT	65A1J2
56P5	SXT	65A1J1
56P6	IMU	35J2
56P7	IMU	35J4
56P8	SCT	65A2J1
56P9	Signal conditioning module	30J1
56P10	Control electronics	50A4J1
56P11	Spacecraft (SC) power connector	A16J190
56P12	SC power connector	A16J191
56P13	Tracker electronics	45A12J1
56J1	Inner gimbal CDU	40A4P1
56J2	Middle gimbal CDU	40A5P1
56J3	Outer gimbal CDU	40A3P1
56J4	Shaft angle CDU	40A2P1
56J5	Trunnion CDU	40A1P1
56J6	IMU control panel	50A2P1
56J8	Condition annunciator	15P1
56J9	G and N indicator control panel	50A1P1
56J10	AGC navigation panel DSKY	05A6P1
56J11	PSA tray 1	45A1P1
56J12	PSA tray 2	45A2P1
56J13	PSA tray 3	45A3P1
56J14	PSA tray 4	45A4P1
56J15	PSA tray 5	45A5P1
56J16	PSA tray 6	45A6P1
56J17	PSA tray 7	45A7P1
56J18	PSA tray 8	45A8P1
56J19	PSA tray 9	45A9P1
56J20	PSA tray 10	45A10P1
56J21	AGC interconnect harness	05A5P1
56J22	AGC interconnect harness	05A5P2
56J23	AGC interconnect harness	05A5P6
56J24	AGC interconnect harness	05A5P7



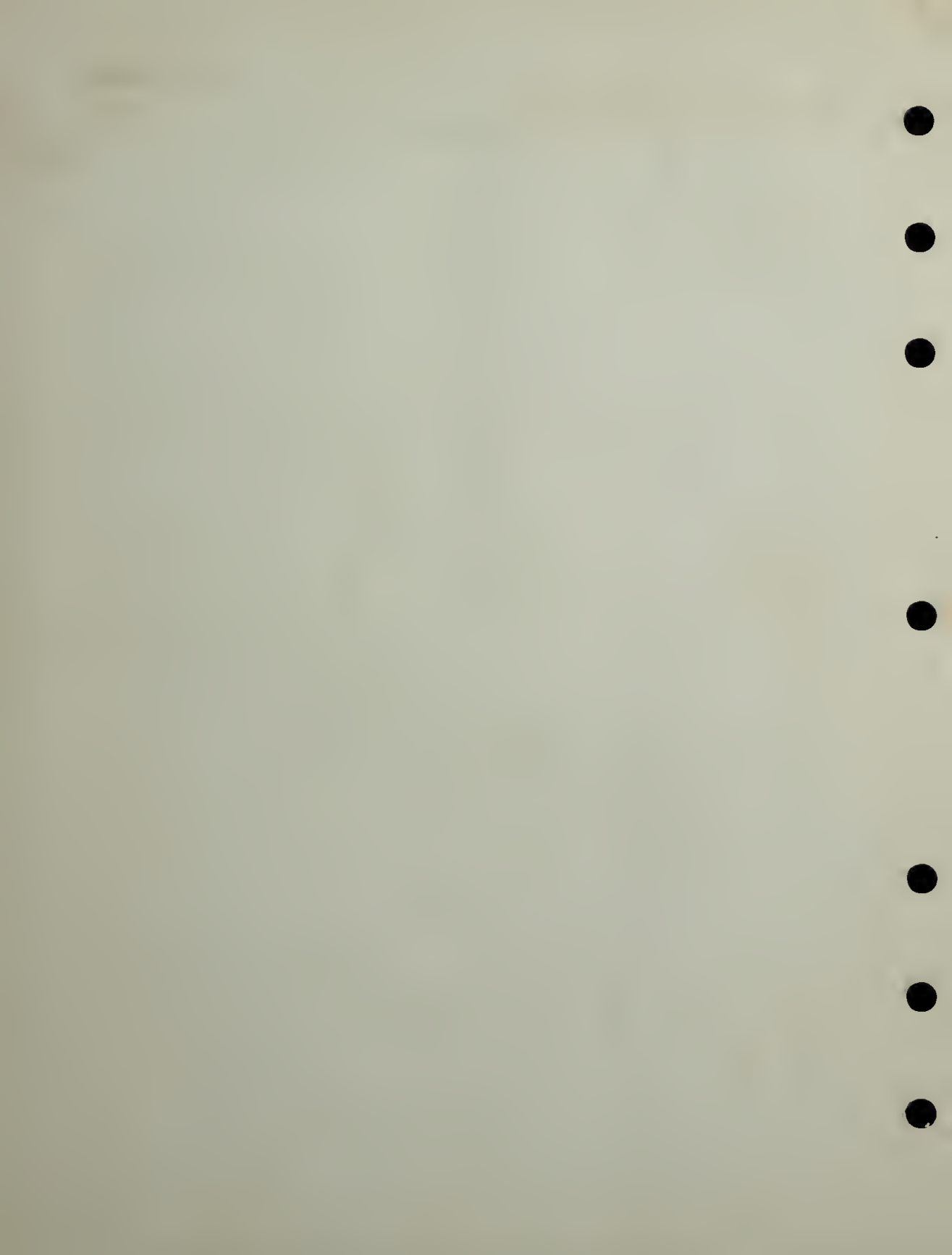
## 3-12 SIGNAL CONDITIONER ASSEMBLY

The signal conditioner assembly (figure 3-19) is mounted to the rear of the G and N station in the spacecraft. This unit conditions G and N system signals so that they are acceptable to the airborne telemetry system.



15244

Figure 3-19. Signal Conditioner Assembly



## Chapter 4

## COMPONENT THEORY OF OPERATION

## 4-1 SCOPE

This chapter discusses the operation of individual assemblies by explaining, in detail, the operation of components or circuits in the assemblies. The detailed discussions are generally limited to those components or circuits whose operation is not apparent in the functional descriptions presented in chapter 2.

## 4-2 INERTIAL MEASURING UNIT

The inertial measuring unit (IMU) is a three-degree-of-freedom, stabilized platform assembly consisting of a stable member on which accelerometers and stabilization gyros are mounted, three gimbals, gimbal mounted electronics, and six inter-gimbal assemblies which house torque motors and resolvers.

4-2.1 GIMBALS. The IMU gimbals consist of a supporting gimbal or case, an outer gimbal mounted to the case, a middle gimbal mounted to the outer gimbal, and an inner gimbal or stable member mounted to the middle gimbal. The IMU gimbal mechanization is illustrated in figure 4-1.

4-2.1.1 Stable Member. The stable member (figure 4-2) is machined from a solid block of cold pressed and sintered beryllium. Holes are bored in the block for mounting three 25 inertial reference integrating gyros (25 IRIG's) and three 16 pulsed integrating pendulums (16 PIP's). Three separate IRIG preamplifiers in a single module, three PIP preamplifier modules, one ADA preamplifier module, one angular differentiating accelerometer (ADA), and an emergency heater control module are also mounted on the stable member. The stable member or inner gimbal is supported by the middle gimbal and is free to rotate 360 degrees about the inner gimbal axis.

An inter-gimbal assembly is attached to each end of the stable member to connect the stable member to the middle gimbal and to define the inner gimbal axis. Figure 4-3 illustrates the inner axis inter-gimbal assembly. The inter-gimbal assemblies contain a pair of low preloaded ball bearings, torque motors, resolvers, and slip ring assemblies. The dc torque motors, located in each inter-gimbal assembly, operate in parallel in the stabilization loop to drive the stable member about the inner gimbal axis. The dc torque motors are approximately six inches in diameter and have permanent magnet stators.

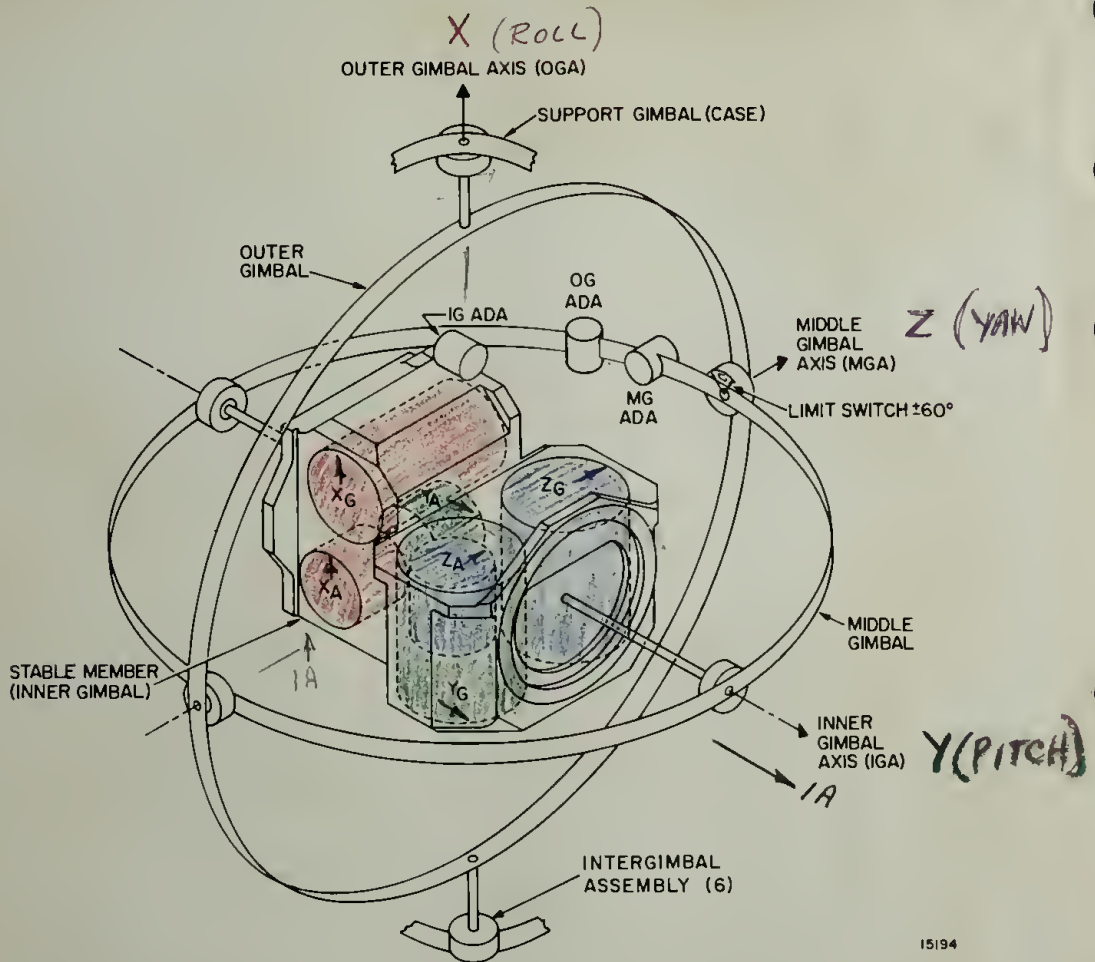


Figure 4-1. IMU Gimbals, Mechanization Diagram

A single speed (1X) coarse resolver transmitter is located in the inter-gimbal assembly at the positive end of the inner gimbal axis, and a 16 speed (16X) fine resolver transmitter is located in the inter-gimbal assembly at the opposite end. The inter-gimbal assemblies are referred to as the 1X inner axis inter-gimbal assembly and the 16X inner axis inter-gimbal assembly. The resolvers are used to transmit the angular displacement of the stable member about the inner gimbal axis to the coupling display units (CDU's). The output of the resolvers is an 800 cps signal proportional to the sine and cosine of the inner gimbal angle. A gyro error resolver, also located in the 1X inner axis inter-gimbal assembly, is used in the stabilization loop to transform gyro errors into gimbal axis errors. The slip ring assemblies contain 40 contacts that route the stable member power and signal inputs and outputs.

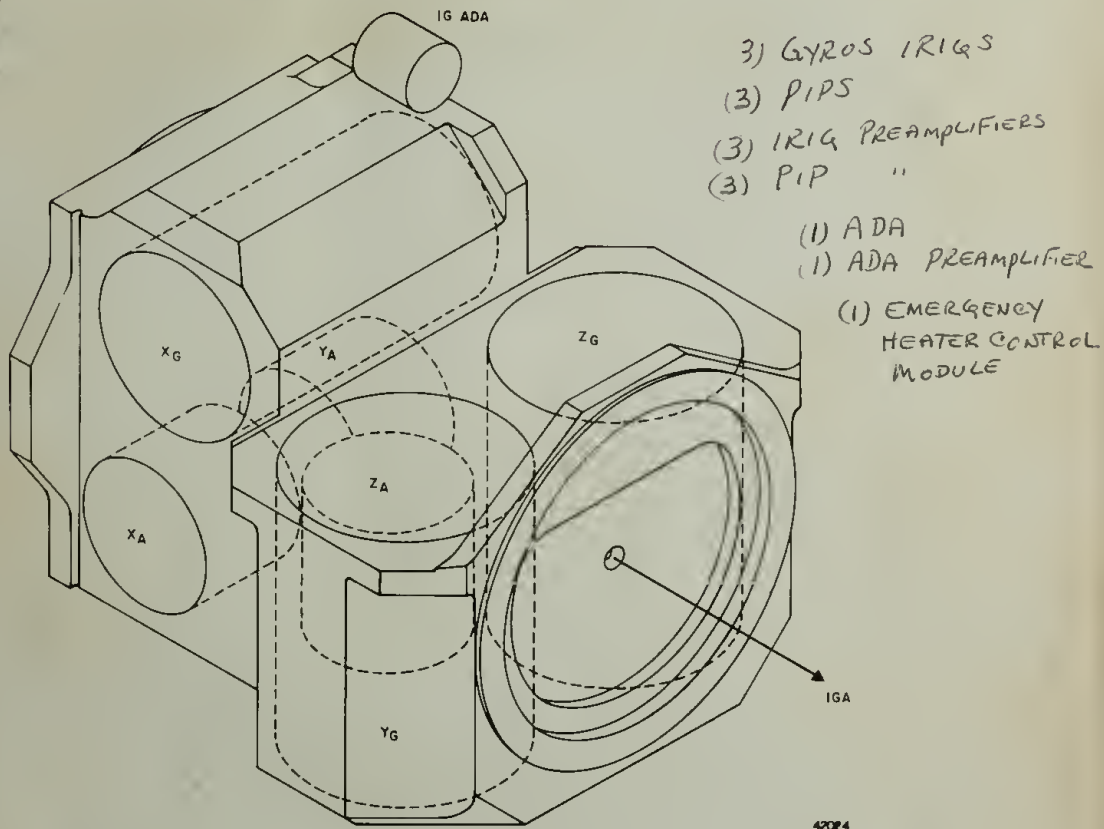


Figure 4-2. Stable Member ROTATES 360° ABOUT IGA.

**4-2.1.2 Middle Gimbal.** The middle gimbal is spherical and is assembled from two hemispherically shaped sections of aluminum alloy. An inter-gimbal assembly is attached to each end of the middle gimbal to connect the middle gimbal to the outer gimbal and to define the middle gimbal axis. The inter-gimbal assembly provides 360 degrees of freedom for the middle gimbal. Each inter-gimbal assembly contains ball bearings, a dc torque motor, a 40 contact slip ring, and a gimbal angle resolver transmitter. A 1X coarse resolver is located at the positive end of the middle gimbal axis and a 16X fine resolver is located at the opposite end. Other components mounted on the middle gimbal include two ADA's and two ADA preamplifiers in separate modules. One ADA is positioned to sense rotational motion of the middle gimbal and the other ADA is positioned to sense rotational motion of the outer gimbal. A limit switch is also included on the middle gimbal axis in the 1X inter-gimbal assembly to signal the astronauts when the middle gimbal angle exceeds plus or minus 60 degrees and the possibility of a gimbal lock condition exists.

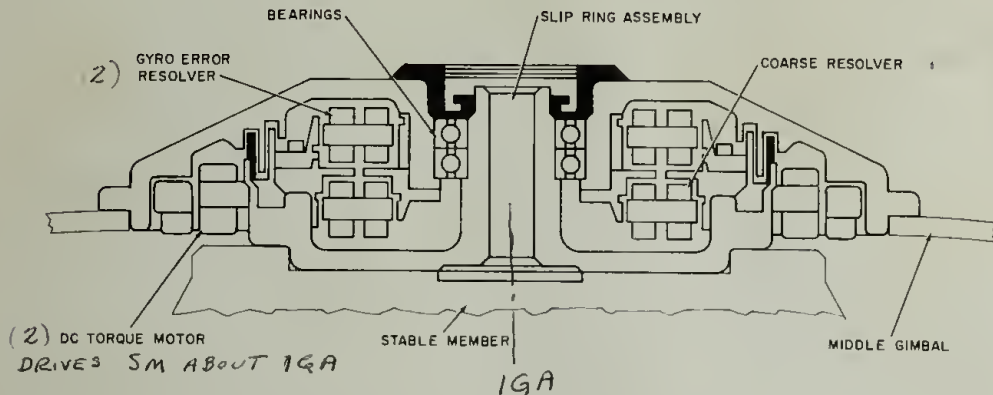


Figure 4-3. Inter-Gimbal Assembly ONE ON EACH END

4-2.1.3 Outer Gimbal. The outer gimbal is similar in general configuration, fabrication, and assembly to the middle gimbal. An inter-gimbal assembly is attached to each end of the outer gimbal to connect the outer gimbal to the support gimbal or case, and to define the outer gimbal axis. The inter-gimbal assembly provides 360 degrees of freedom for the outer gimbal. Each inter-gimbal assembly contains ball bearings, a dc torque motor, a gimbal angle resolver, and a 50 contact slip ring assembly. A 1X coarse resolver is located at the positive end of the outer gimbal axis, and a 16X fine resolver is located at the opposite end. A third resolver, the pitch-yaw resolver, is located in the 1X outer axis inter-gimbal assembly. A pressure transducer is located on the 16X outer axis inter-gimbal assembly and provides a signal representative of IMU internal pressure. The pitch-yaw resolver transfers steering error signals from the gimbal axes to the nav base axes. A precision resolver alignment module is also mounted to the 16X outer axis inter-gimbal assembly and provides compensation for physical errors in each axis. Other components on the outer gimbal include two variable-speed axial flow blowers, which circulate air over the middle and support gimbals; two blower speed control modules; and a 28 volt dc regulator module for the temperature control system.

4-2.1.4 Support Gimbal. The support gimbal or case is spherical and fabricated of aluminum alloy. The support gimbal consists of a center section containing integral coolant passages which circulate water-glycol from the spacecraft coolant system. Connection to the spacecraft coolant system is through quick disconnect couplings located at each end of the coolant passages. The mounting flanges and hardware of the center section are used to attach the IMU to the nav base. A connector mount assembly is bolted to each end of the center section and covers the outer axis inter-gimbal assemblies. One connector mount assembly provides access to the precision resolver alignment module mounted on the 16X outer axis inter-gimbal assembly. A pressure valve assembly is on the connector mount assembly located at the 1X outer axis end. Two electrical connectors are on each of the connector mount assemblies. The support gimbal is completed by the addition of a spherical cover to the top and bottom of the center section to hermetically seal the IMU.

## APOLLO GUIDANCE AND NAVIGATION SYSTEM

4-2.2 25 INERTIAL REFERENCE INTEGRATING GYRO. The 25 IRIG stabilization gyro (figure 4-4) is a fluid and magnetically suspended, single-degree-of-freedom, integrating gyro. The designation in the name denotes the case diameter in tenths of inches. The stabilization gyros are the sensing elements of the stabilization subsystem. Three 25 IRIG's are mounted on the stable member so that their input axes are mutually perpendicular. Any change in the attitude of the stable member is sensed by one or more of the gyros. The gyros convert this displacement into an error signal which is amplified and fed into the gimbal torque motors. The gimbal torque motors reposition the stable member until the error signals are nulled and the original orientation of the stable member is re-established.

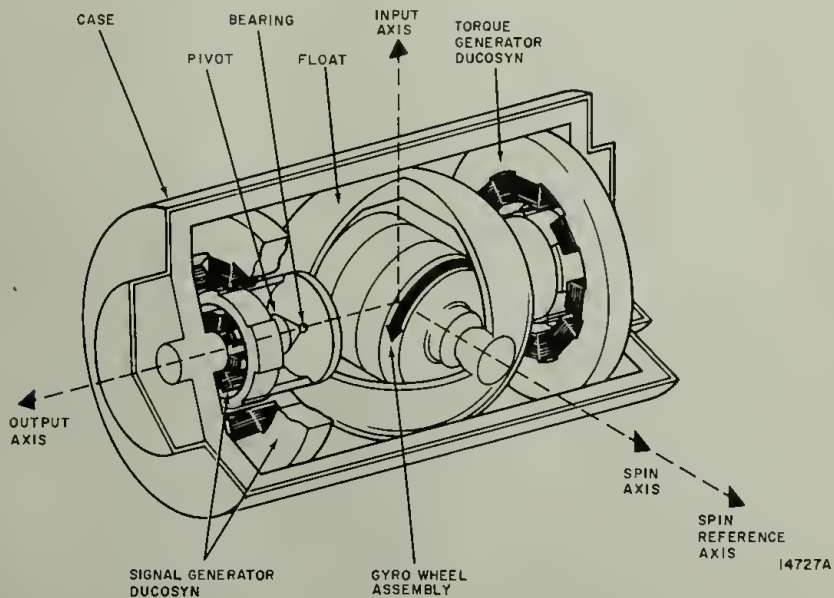


Figure 4-4. 25 IRIG, Simplified Cutaway View

The 25 IRIG consists of a wheel assembly, a spherical float, a cylindrical case, a signal generator ducosyn, and a torque generator ducosyn. The wheel is mounted within the sealed float on a shaft perpendicular to the float axis and spins on preloaded ball bearings. The wheel is driven as a hysteresis synchronous motor in an atmosphere of helium. The float is mounted within the case on a shaft axially coincident with the longitudinal axes of both float and case. Precision hard-alloy pivots and bearings are located at each end of the float shaft, with the bearing being part of the float assembly. The torque generator ducosyn is mounted on one end of the float shaft, while the signal generator ducosyn is mounted on the opposite end. The volume between the float and case is filled with a suspension and damping fluid.

There are four axes associated with the 25 IRIG: the input axis, the spin axis, the spin reference axis, and the output axis. While the wheel is spinning, the gyro tends to maintain its attitude with respect to space. If the gyro is forced to rotate about an axis (the input axis) perpendicular to the axis about which the wheel spins (spin axis), it will respond with a torque about an axis perpendicular to both spin and input axis (the output axis). The spin axis becomes misaligned from its normal or null position (spin reference axis) by an amount equal to the angle through which the output axis has rotated. The spin reference, input, and output axes are always mutually perpendicular. The rotation produced about the output axis in response to a rotation about the input axis in a single-degree-of-freedom gyro is called gyroscopic precession. The output axis is along the float shaft. Rotation of the gyro about its input axis results in a precession of the float.

The signal generator ducosyn is mounted on the positive output axis end of the float to provide magnetic suspension of the float with respect to the case, and to serve as a transducer to provide an electrical analog signal which indicates the amount and direction of the angular rotation of the float about the output axis. The torque generator ducosyn is mounted on the negative output axis end of the float to provide magnetic suspension, and to serve as a transducer to convert electrical error signals to a torque about the output axis when desired.

Since float movement is a measure of angular displacement of the gyro, friction on the float shaft (output axis) is a critical factor of gyro sensitivity. Several measures are taken to reduce this friction to a negligible level. One means of doing this is fill the space between the float and case with a fluid which has the same density (specific gravity) as that of the float itself. This fluid causes the float to be suspended with respect to the case. The means by which the fluid density is kept equal to the density of the float is by the controlled application of heat. Heating coils are attached to the 25 IRIG end mounts to maintain the density of the fluid. Two sensors are submerged in the fluid to indicate the temperature of the fluid. The particular suspension fluid used in the IRIG is polychromotrifluoroethylene. The fluid also provides proper damping of float movement. The fluid suspension is supplemented by magnetic suspension. Magnetic suspension is achieved by generating magnetic forces which keep the pivot centered in the bearing. The magnetic suspension forces are created by the magnetic suspension portion of both the signal generator and torque generator ducosyns. Under normal environmental conditions the pivot in the 25 IRIG will never touch the bearing. Under extreme environments, even with both fluid and magnetic suspension, the pivot may periodically touch the bearing. To minimize the resulting friction, polished precision hard-alloy bearings and pivots are used.



## APOLLO GUIDANCE AND NAVIGATION SYSTEM

Since there are ferrous parts in the wheel assembly, any oxygen present would cause them to rust. Helium is used in the float, rather than a vacuum, since the helium acts as a good conductor of heat away from the wheel motor. Helium, being a light gas, generates little windage, resulting in the additional advantage of low windage losses in the wheel motor. The helium is placed in the float at a reduced pressure of one-half atmosphere to further reduce these windage losses.

**4-2.2.1 Gyro Wheel Assembly.** The gyro wheel assembly consists of a wheel, a shaft, hysteresis ring, ball bearings, and bearing retainers. The wheel is a composite wheel consisting of a beryllium hub with a rim of heavy metallurgical steel called gyro metal fitted onto the hub. The purpose of the composite wheel is to concentrate as much weight as possible in the outside rim, providing the wheel with a high moment of inertia. The shaft is made of steel and is machined to serve as the inner race for the ball bearings. The shaft is hollow and has female threads on each end. Preloading of the wheel is achieved and controlled by bolting the bearing retainers to the hub. The bearing retainers press on the outer bearing race exerting a wedging action on the balls. As a result a deliberate load (preload) is imposed on the wheel bearing which will constrain the axial movement of the wheel to a rotational plane at right angles to the shaft. The amount of preload is carefully determined since excessive preload will introduce excessive bearing friction that would limit bearing life. The hysteresis ring is constructed of laminated, specially hardened steel. The hysteresis ring is fitted on the wheel hub and serves as a rotor for the hysteresis synchronous motor which drives the wheel.

**4-2.2.2 Float Assembly.** The float assembly consists essentially of the float gimbal, two hemispheres, hysteresis motor stator, and bearings. The wheel assembly is bolted to the float by threaded rings. The rings also hold together the float gimbal and the float hemispheres, both of which are made of beryllium. The hysteresis motor stator is placed inside the float gimbal with the power leads brought out through each end of the float gimbal. The float shaft is an integral part of float gimbal and extends outward from the float to mount the float bearings and ducosyn rotors. The tungsten carbide bearings, when placed on each end of the float gimbal, define the output axis. The signal and torque generator rotors are salient four-pole types made of high permeability nickel. The magnetic suspension rotors are cylindrical and made of ferrite. The float gimbal also has a hole fitted with a ball and screw seal through which the float is evacuated and filled with helium. Preliminary balance weights are placed on the float gimbal for rotational balancing prior to the float being inserted into the case. Balance weights along the spin axis and the input axis are accessible from outside the case and are used for rotational balancing after final assembly.

**4-2.2.3 Case.** The case consists essentially of main housing and damping block assemblies, end housing assembly, and main cover assembly. The float assembly is encased by the main housing assembly and is supported with respect to the end housing by the pivot assemblies. Beryllium damping blocks fill the space around the float. These blocks provide the necessary control of the damping gap (the width of the gap between the float assembly and case), thereby controlling the damping coefficient. The end housings are held to the main housing by clamping caps. The end housings contain the tungsten carbide

pivot assemblies, ducosyn stators, bellows to take up the expansion and contraction of the suspension fluid, and a setscrew and ball seal to allow filling with the suspension fluid. Four balance adjusters, provided in the main housing assembly, allow access to the adjustable balance weights along the spin axes and the input axes. After hermetically sealing and balancing of the unit, the 25 IRIG is covered by a main cover assembly which provides a magnetic shield plus a second hermetic sealing.

4-2.2.4 Pre-alignment Package. The pre-alignment package contains the magnetic suspension capacitors, padding resistors, temperature control sensors, main heater, and auxiliary heater. The pre-alignment package is added to the signal generator end of the 25 IRIG case during final assembly, making the gyro a pre-aligned gyro. When the pre-aligned gyro is placed in the IMU stable member, an additional heater is placed on the torque generator end.

4-2.3 16 PULSED INTEGRATING PENDULUM. The accelerometers in the IMU are the 16 PIP's. The 16 PIP in itself is not an accelerometer, but an acceleration sensitive device. When fixed in its associated accelerometer loop, the 16 PIP becomes an integrating accelerometer (16 PIPA).

The 16 PIP is basically a cylinder with a pendulous mass unbalance (pendulous float) and is pivoted with respect to a case. The pendulous float has no electrical power requirements as it is completely mechanical in operation. The volume between the pendulous float and case is filled with a fluid. A signal generator ducosyn, located at one end of the float, provides magnetic suspension of the float with respect to the case and acts as a transducer to convert mechanical rotation of the float with respect to the case into electrical analog signals. A torque generator ducosyn, located at the other end of the float, provides magnetic suspension of the float with respect to the case and acts as a transducer to convert error signals, in the form of electrical pulses, into mechanical torque about the float shaft. A 2 volt rms, 3,200 cps, single phase excitation is required for the magnetic suspension portion of each ducosyn and for the transducer portion of the signal generator ducosyn.

The output axis of the 16 PIP is defined by the axis of the pivots which support the float with respect to the case. (See figure 4-5.) The pendulum axis is defined by a line which passes through the mass unbalance and intersects the output axis at a right angle. The input axis is the axis along which the 16 PIP is sensitive to acceleration. The input axis and pendulum axis form a plane that is perpendicular to the output axis. When the float rotates about the output axis, the pendulum axis becomes displaced from its normal or null position (pendulum reference axis) by an amount equal to the angle through which the float has rotated. The pendulum reference, input, and output axes are always mutually perpendicular.

The mass unbalance hangs below the output axis and swings like a pendulum when accelerated. Figure 4-6 illustrates the result of acceleration along the input axis as viewed from the positive end of the output axis or signal generator end of the 16 PIP.

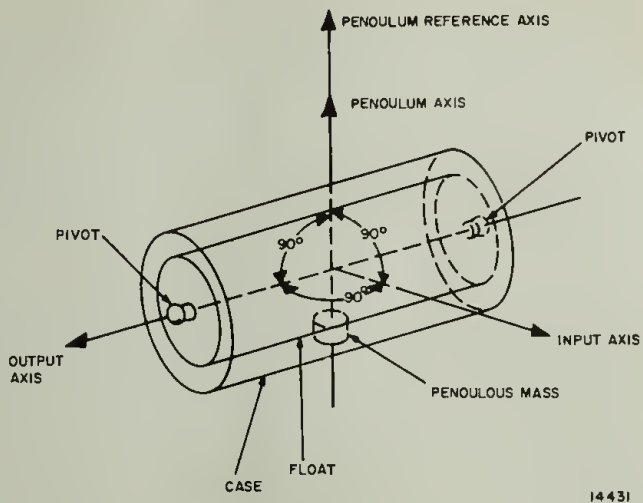


Figure 4-5. Definition of 16 PIP Axes

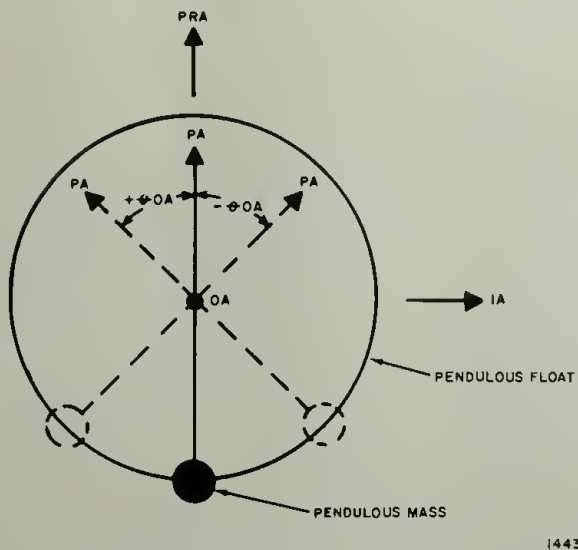


Figure 4-6. Result of Acceleration Along Input Axis

Acceleration along the input axis (IA) results in the pendulous mass producing a torque that rotates the float. Acceleration in the direction of the positive input axis (the direction in which the arrowhead points) results in the float being torqued about the output axis (OA) by a pendulous torque resulting in a negative angular displacement ( $-\theta_{OA}$ ) about the output axis. Conversely, acceleration in the direction of the negative input axis produces pendulous torque resulting in a positive displacement ( $+\theta_{OA}$ ) about the output axis. When no acceleration is present along the input axis, the pendulum axis (PA) is coincident with the pendulum reference axis (PRA), and the angular displacement about the output axis is zero. By definition, the 16 PIP is at null when the angular displacement about the output axis equals zero.

Since the 16 PIP is a pendulum, the relationship of acceleration versus angular displacement about the output axis varies as a tangent function. The amount of acceleration the pendulous mass senses varies as the tangent of the angle of displacement. In other words, the pendulum senses the full amount of applied acceleration only when the pendulum axis is at right angles to the input axis. As the pendulum axis becomes displaced, increasingly larger amounts of applied acceleration result in increasingly smaller amounts of angular displacement. In other words, the pendulum becomes less sensitive to acceleration as the angle of displacement increases. Therefore, maximum sensitivity and linearity of the 16 PIP occur near null. To assure maximum sensitivity and linearity of operation, the accelerometer loop in which the 16 PIP is used restricts the angular displacement about the output axis to very small excursions in either direction from null. The accelerometer loop is designed so that the torque developed by the torque generator is equal to and opposite the pendulous torque resulting from applied acceleration. Therefore, the acceleration to which the 16 PIP is being subjected is represented by the magnitude and direction of the average torque pulse current flowing in the torque generator. The signal generator, located at the positive end of the output axis, senses an angular displacement of the float about the output axis. The phase and magnitude of the output signals from the signal generator secondary winding are determined by the direction and amount of float displacement. The error signals are processed by the accelerometer loop into incremental velocity pulses to the AGC and into torquing pulses to the torque generator to torque the float back to its null position.

**4-2.3.1 Float Assembly.** The float is a hollow beryllium cylinder fitted with a shaft on which the float pivots are located. On both ends of the float are four salient pole transducer rotors and cylindrical magnetic suspension rotors with tapered inside diameters. The pendulous mass screws into and protrudes slightly from the float. Adjustable balance weights for rotational balancing of the float are located along the pendulum axis and the input axis. The completed float assembly is placed in a main housing assembly and the main housing assembly is filled with a suspension fluid. The suspension fluid provides fluid suspension of the float with respect to the case and viscous damping of the float.

**4-2.3.2 Main Housing Assembly.** The main housing assembly consists of a main housing and two end housings. The main housing contains a bellows assembly to take up the expansion and contraction of the suspension fluid that result from variations in the temperature of the fluid. Each end housing contains a pivot bearing, an eight pole magnetic suspension stator, and either an eight pole signal generator stator or torque generator

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stator. The two end housings are called the signal generator end housing (on the +OA end) and the torque generator end housing (on the -OA end). The magnetic suspension units have tapered stator poles and a tapered rotor, developing magnetic suspension forces in both radial and axial directions.

4-2.3.3 Outer Case Assembly. The main housing assembly is completely covered by an outer case which provides magnetic shielding and a hermetic seal for the unit. Heating coils are placed between the main housing and outer case to heat the suspension fluid to the proper temperature for fluid suspension of the float. All electrical connections for signal and torque generators, magnetic suspension units, and heaters are brought out through the torque generator end of the case.

4-2.4 DUCOSYN. Ducosyns are used in both the 16 PIP and the 25 IRIG for magnetic suspension of the floats, signal generator action, and torque generator action. This discussion will be primarily concerned with the ducosyns used in the 25 IRIG, but the basic principles presented are also applicable to the 16 PIP ducosyns.

The ducosyn is a separate magnetic suspension microsyn and separate transducer microsyn in a single unit. This design eliminates the cross-coupling effects that are present in a single microsyn designed to perform both the magnetic suspension and the transducer function. A cross section of a typical ducosyn is shown in figure 4-7. The unit contains two separate stators mounted in the end housing and two separate rotors mounted on a common mounting ring of the float assembly. The inside stator consists of eight outwardly projecting poles which are wound to provide magnetic suspension forces. The outside stator consists of eight inwardly projecting poles which are wound to provide either signal generator or torque generator action. The outer rotor is the transducer rotor and consists of four unwound poles projecting outward. The inner rotor, which is the magnetic suspension rotor, is cylindrical and unwound.

4-2.4.1 Ducosyn Signal Generator. The ducosyn signal generator converts angular rotations of the float about the output axis into an electrical analog signal. The signal generator stator has eight poles with both a primary winding and a secondary winding per pole. The poles are wound as shown in figure 4-8, so that four alternate poles (2, 4, 6, and 8) have both primary and secondary windings wound in the same direction. The other four poles (1, 3, 5, and 7) have secondary windings wound opposite to primary windings. When the primary excitation goes positive with respect to ground, flux travel, (assuming conventional current flow and using the right-hand rule) is toward the rotor in poles 1, 2, 5, and 6, making them north poles. Flux travel is away from the rotor in poles 3, 4, 7, and 8, making them south poles. On the negative half cycle of primary excitation, the pole polarities are reversed.

The number of primary turns on each pole is equal, so the magnitude of primary flux developed is equal in all eight poles. Since the primary flux is alternating, it induces a voltage in the secondary windings. The amount of voltage induced in the secondary winding depends on flux density, that is, the amount of flux flowing through the stator pole. Maximum voltage is induced when flux density is maximum. Flux density is maximum when the magnetic reluctance is a minimum. Magnetic reluctance is minimum when a rotor pole is directly opposite a stator pole.

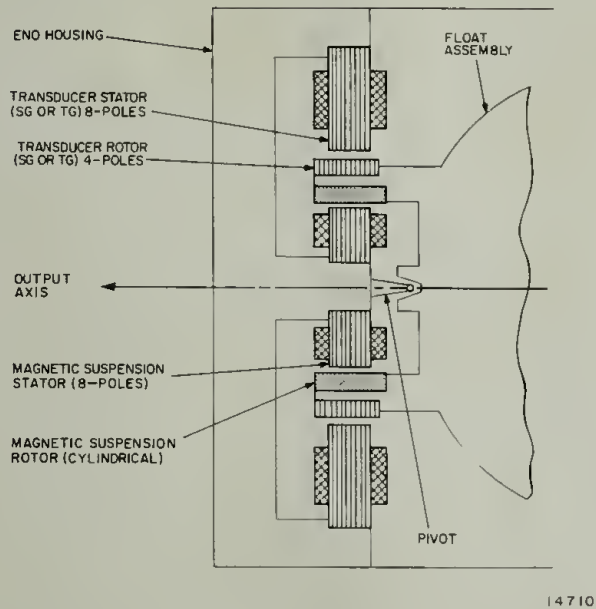
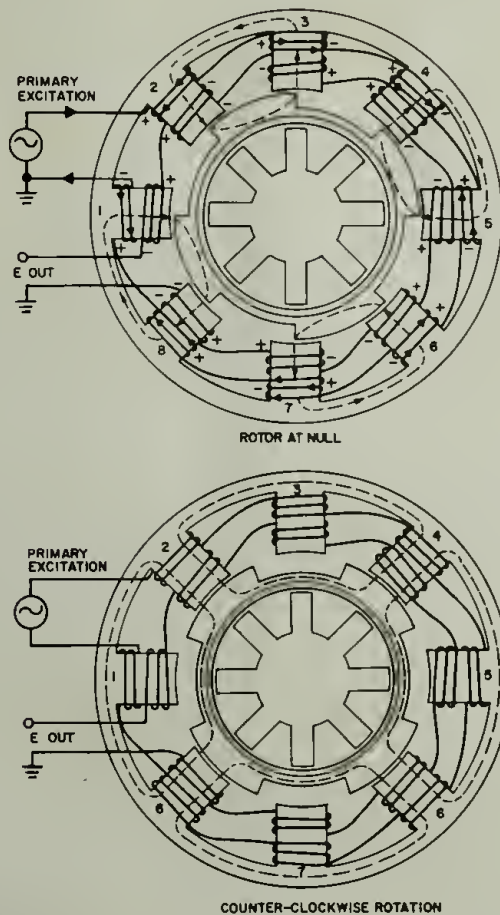


Figure 4-7. Generalized Ducosyn Construction

When the rotor is in the null position as shown in figure 4-8, an equal portion of a rotor pole is lined up with each stator pole; therefore, the flux density of each pole is equal. On the positive half cycle of primary excitation, secondary windings 2, 4, 6, and 8 produce outputs which are positive with respect to ground; and secondary windings 1, 3, 5, and 7 produce outputs which are negative with respect to ground. Since the secondary windings all have an equal number of turns, the secondary voltages add to zero. On the negative half cycle of primary excitation, the polarities are reversed, but the net output still adds to zero. Secondary windings 2, 4, 6, and 8 produce voltages that are in-phase with the primary excitation, while secondary windings 1, 3, 5, and 7 produce voltages 180 degrees out-of-phase with the primary excitation.

When the rotor is rotated counterclockwise as a result of float displacement as shown in figure 4-8, the equality of the air gap reluctance is destroyed. Therefore, the reluctance of the air gap at pole faces 2, 4, 6, and 8 is decreased and the reluctance of the air gap at pole faces 1, 3, 5, and 7 is increased. The change in air gap reluctance results in greater flux density in poles 2, 4, 6, and 8 than in poles 1, 3, 5, and 7. The voltages induced in secondaries 2, 4, 6, and 8 are greater than the output induced in secondaries 1, 3, 5, and 7. Therefore, the net output voltage is in phase with the primary excitation. The magnitude of the net output voltage depends on the degree of air gap reluctance unbalance.



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Figure 4-8. Ducusyn Signal Generator Operation

The greater the rotor displacement from null, the greater the output voltage. In the same manner a clockwise rotation from null decreases the voltages induced in the in-phase secondary windings and increases the voltages induced in the 180 degree out-of-phase secondary windings. The net output, therefore, is a voltage 180 degrees out-of-phase with the primary excitation. The magnitude of this voltage is again determined by the amount of clockwise angular displacement of the float.

The signal generator is insensitive to a translational movement; that is, the voltages induced due to rotor translation cancel each other because of the symmetry of the signal generator. For example, if the rotor translation is toward stator poles 1 and 8 and away from poles 4 and 5, then the flux path between 1 and 8 is strengthened, and the flux path between 5 and 4 is weakened. The secondaries of pole pairs 1 and 8 and 5 and 4 are wound in opposition, and the voltages induced due to translation cancel in each pair of windings. A similar situation exists for all other flux paths and for translation in any direction.

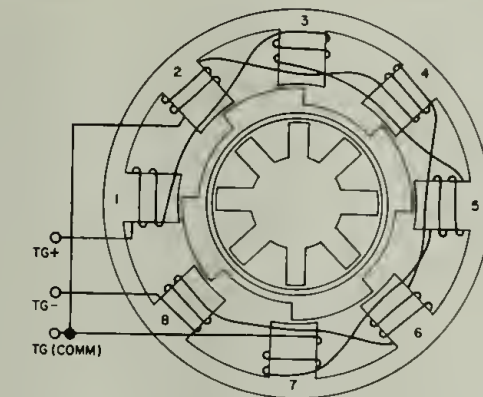
4-2.4.2 Ducosyn Torque Generator. The ducosyn torque generator converts electrical pulses into torque that rotates the float assembly about the output axis. The torque generator stator has eight poles with a single winding per pole. The windings are connected as shown in figure 4-9 and the center tap is brought out as a ground or common lead. When clockwise torque is desired, positive pulses (with respect to TG COMM) are applied to TG+, and nothing is applied to TG-. When counterclockwise torque is desired, positive pulses are applied to TG-, and nothing is applied to TG+. When no torque is desired, neither winding is excited.

When positive pulses are applied to TG+, stator poles 1 and 5 become north poles, and poles 3 and 7 become south poles. (See figure 4-9.) Since the rotor was originally centered between adjacent poles, clockwise torquing action results as the rotor tends to align itself symmetrically with respect to the north-south pole pairs. In other words, the magnetic lines of force following the path of least reluctance through the initially misaligned rotor create a nonuniform magnetic field. The field has a higher flux density on one side of each pole than on the other side. Therefore, the portion of the rotor lying in this field experiences a force in a direction away from the higher density to the lower density. If unrestrained, the rotor rotates until the rotor poles are centered under the stator poles. At this point maximum flux density is uniformly concentrated in each air gap creating a symmetrical magnetic field. The rotor becomes motionless. When positive pulses are applied to TG-, poles 4 and 8 become north poles, poles 2 and 6 become south poles, and the rotor is torqued counterclockwise.

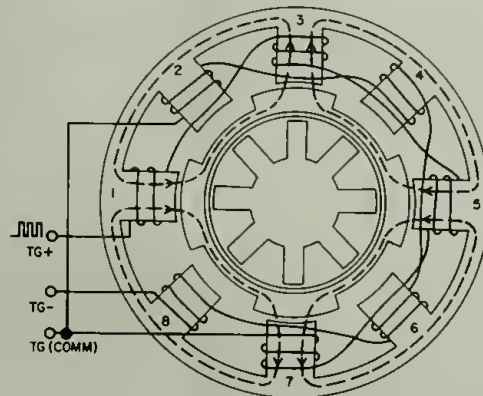
The direction of the desired torque is controlled by applying torquing pulses to the appropriate TG lead. The magnitude of the developed torque is dependent upon the strength of the north-south pole pairs, which is in turn dependent upon the amount of current flowing through the windings as a result of applied torquing pulses. Torque on the torque generator rotor produces torque on the float. The float torque creates an error signal from the ducosyn signal generator. The position of the IMU stable member can thus be changed by utilizing the compensating reaction from the stabilization subsystem.

4-2.4.3 Ducosyn Magnetic Suspension. The magnetic suspension unit (figure 4-10) of the ducosyn is unique in that the rotor and stator relationship is inverted. The cylindrical rotor eliminates the reaction torques that exist with salient pole rotors under high magnetic suspension. The wound stator is mounted in the 25 IRIG or 16 PIP end housing and the unwound cylindrical rotor is mounted on the float. The 16 PIP magnetic suspension unit has tapered stator poles and rotor that develop both radial and axial magnetic suspension. The suspension capacitors are mounted on the outside of the 25 IRIG or 16 PIP.





ROTOR AT NULL



POSITIVE TORQUING SIGNALS APPLIED

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Figure 4-9. Ducusyn Torque Generator Operation

Each stator winding is part of a series RLC circuit. (See figure 4-11.) Although the equivalent circuit illustrated shows only two poles, it is representative of any of the four pairs of diametrically opposed stator poles.  $L_1$  and  $L_2$  represent the inductances of the stator windings.  $R_1$  and  $R_2$  represent the total resistance of each stator circuit.  $C_1$  and  $C_2$  are the external fixed capacitors in series with the resistance and inductance. The values of  $L_1$  and  $L_2$  vary inversely with the size of air gaps A and B respectively.

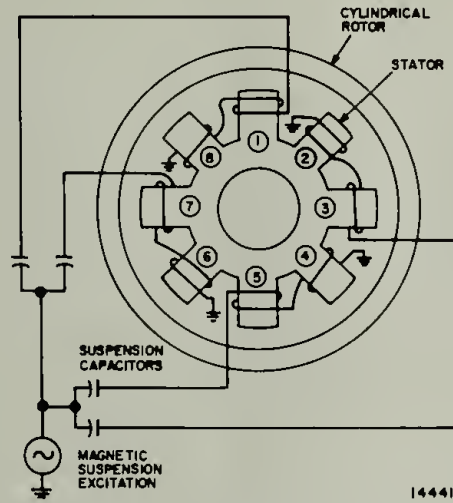


Figure 4-10. Ducosyn Magnetic Suspension Unit

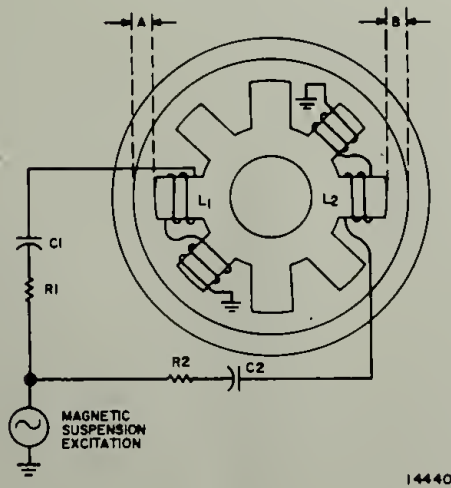


Figure 4-11. Ducosyn RLC Equivalent Circuit

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The excitation to the magnetic suspension unit is maintained at a specific frequency, leaving the inductance the only circuit variable. When the inductance is varied until the inductive reactance equals and cancels the capacitive reactance, circuit resonance is achieved. At resonance the total circuit impedance is at a minimum, consisting only of resistance, and the current is thus at a maximum. During construction and testing a fixed suspension capacitor is selected that develops a value of capacitive reactance that is less than the value of inductive reactance present when the rotor is at null, allowing a current flow at null that is less than the maximum or resonant current. In operation, translational movement of the rotor from its null point alters the inductance to bring the circuit closer to or further from resonance.

It can be seen that the current flow through the  $R_1$ ,  $L_1$ ,  $C_1$  circuit of figure 4-11 varies when the inductance is varied by varying the air gap  $A$ . There will be some position of the rotor (or value of  $A$ ) at which the value of  $L$  will produce resonance and maximum current. As the rotor moves in either direction ( $A$  gets larger or smaller) from the resonant point, the current falls off sharply, since the value of  $L$  (and inductive reactance) changes to make the circuit impedance greater. The current in the stator winding determines the amount of magnetic energy in the stator pole. The attractive force on the rotor is equal to the change in magnetic energy divided by the change in air gap. This relationship of force versus air gap is such that as the rotor moves away from the stator (increasing  $A$ ), the attractive force rises to a maximum, then decreases sharply as the rotor passes through the resonant point. A negative or repelling force is developed as the rotor is moved beyond the resonant point. In operation, the movement of the rotor is limited by the float pivots to a very short distance so that only a rising attractive force results as the rotor is moved away from the stator to its maximum allowable displacement. Conversely, as the rotor moves closer to the stator, decreasing the air gap, the attractive force decreases.

When both circuits of figure 4-11 are considered, it can be seen that as the rotor moves left, air gap  $A$  increases and air gap  $B$  decreases, and vice-versa. The attractive force at one stator pole changes inversely to the change in attractive force at the other stator pole. When the rotor is displaced from its null point (where the forces on the rotor from both poles are equal), the force from the pole the rotor is approaching decreases, and that of the opposite pole increases. The resultant force is then in a direction to move the rotor back to the null position. This action magnetically clamps the rotor between its operating limits. Since the four pairs of stator poles are arranged in a circle within the rotor, their simultaneous action effectively suspends the rotor. The air gap in the 16 PIP magnetic suspension unit is varied by both radial and axial movements of the rotor since the rotor and the stator poles are tapered. The float therefore is suspended both radially and axially.

4-2.5 ANGULAR DIFFERENTIATING ACCELEROMETER. The ADA (figure 4-12) is a fluid damped, torsional pendulum with a rotor winding that generates a voltage as a result of relative motion in a permanent magnet field fixed to the case. The pendulum consists of a rotor floated in fluid and suspended by two torsion wires along the input axis. Eight pairs of permanent magnets, located around the rotor, are mounted to the case. The rotor is suspended so that the rotation of the outer case about the axis of the torsion wire causes pick-off coils in the rotor to move through the eight flux paths from the permanent magnets.

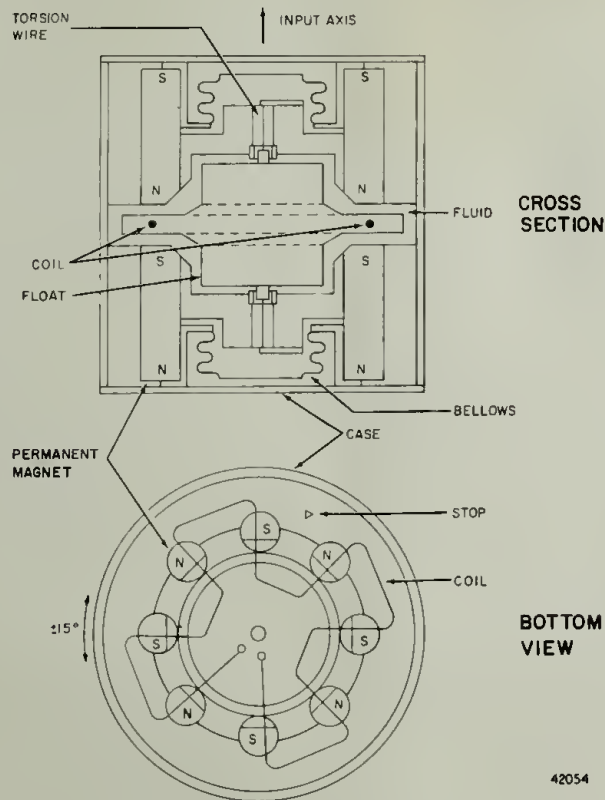


Figure 4-12. ADA

The movement of the pick-off coils cutting the magnetic flux paths generates a voltage in the coils. The magnitude of the generated voltage is directly proportional to the rate at which the pick-off coils cut the magnetic lines of force, and therefore, directly proportional to the angular velocity of the rotor relative to the case. The polarity of generated voltage is determined by the direction of rotor motion relative to the case. When there is no relative motion between the pick-off coils and magnets, there is no output from the ADA.

If the motion of the case is below the natural frequency of the pendulum, the rotor attempts to follow the case. As the rate of case acceleration increases, the rotor falls farther and farther behind the case, causing relative motion between the pick-off coils and the magnetic field. As soon as the angular acceleration of the case becomes constant, the rotor maintains a new fixed position with respect to the case because of the torque resulting from the twisting of the torsionwires. There is no longer an output signal since the relative motion has ceased. Therefore, for case motion below the natural pendulum frequency, the suspension wire exerts primary control over the rotor motion, providing an output signal proportional to the rate of change of acceleration.

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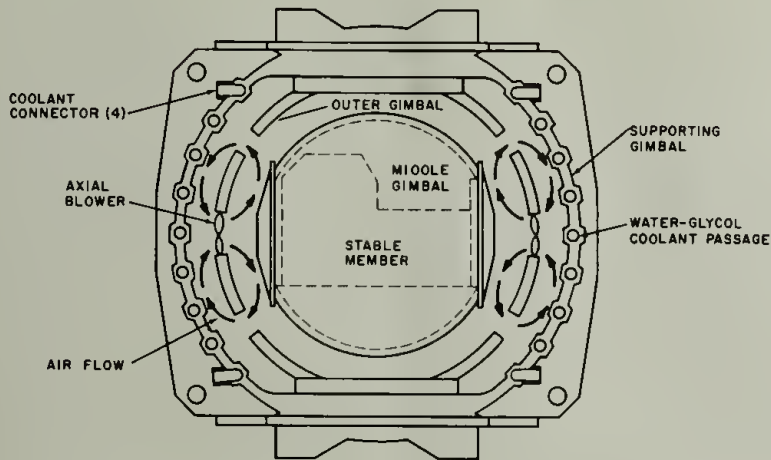
If input signals are above the natural frequency of the rotor, the inertia of the rotor causes the rotor to remain stationary while the case rotates about it. The relative motion between the case and the rotor results entirely from the movement of the case. Therefore, for case motion above the natural pendulum frequency, the output signal is proportional to the angular velocity of the case about the input axis.

A stop on the rotor limits the pick-off coils to plus or minus 15 degrees of angular freedom. The output signal is carried from the rotor to the external terminals by a fine wire, friction free, suspension system. To provide damping and resistance to high gravity loading, the rotor floats in a high density flotation fluid. The rotor is balanced to insure that the centers of mass, rotation, and buoyancy coincide so that the ADA is insensitive to linear accelerations. The flotation fluid requires an operating temperature of 90 to 137 degrees Fahrenheit to keep the ADA characteristics within tolerances. Since variations in temperature cause the fluid to expand or contract, bellows at each end of the case allow the fluid to expand so ADA parts will not be strained.

4-2.6 IMU TEMPERATURE CONTROL SYSTEM. The IMU temperature control system maintains the temperature of the stabilization gyros and accelerometers within the required temperature limits during both standby and operating modes of the IMU. The system supplies and removes heat to maintain IMU heat balance with minimum power consumption. Heat is removed by convection, conduction, and radiation. The natural convection used during the IMU standby mode changes to blower controlled, forced convection during IMU operating modes. (See figure 4-13.) The IMU internal pressure is between 3.5 and 15 psia to provide the required forced convection. To aid in removing heat, a water-glycol solution passes through the coolant passages in the IMU supporting gimbal. The temperature control system contains circuits designed to supply normal proportional temperature control with the capability of either backup or emergency control if the proportional control would malfunction. The IMU temperature control system contains indicating circuitry which provides controls, critical parameter monitoring capability, alarm condition indications, and provisions for isolating malfunctions.

4-2.6.1 Indicating Circuitry. The indicating circuitry (figure 4-14) provides the following:

- (1) Astronaut displays and controls.
  - (a) IMU temperature condition lamps.
  - (b) Manual selection of proportional, backup, or emergency control, as well as auto-override control which automatically switches from proportional to emergency control when an alarm condition prevails.
  - (c) Zero and gain pushbuttons to check the operation and calibration of the indicating bridges and the alarm circuits.
- (2) Telemetry signals.
  - (a) Gyro and accelerometer average temperature indications.



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Figure 4-13. Forced Convection In IMU

- (b) Controlled heater current and blower current indications.
  - (c) IMU temperature control failure indication.
- (3) Power and servo assembly (PSA) tray 7 test points.
- (a) Gyro and accelerometer average temperature indications.
  - (b) Controlled heater current and blower current indications.
  - (c) Proportional control bridge excitation and control current.

The primary function of the indicating circuitry is to monitor the gyro and accelerometer temperatures and provide alarm indications if the gyro or accelerometer temperature exceeds allowable limits. The gyro and accelerometer temperature indicating bridges, the gyro and accelerometer indicating bridge amplifiers, and the temperature alarm amplifier perform this function. The gyro and accelerometer indicating bridges are dc resistance bridges, one leg of which contains, respectively, the gyro temperature indicating sensors and the accelerometer temperature indicating sensors. Each bridge is excited by a dc voltage. When the average temperature of the inertial instruments is the nominal value (133.5 degrees Fahrenheit for gyros and 130.0 degrees Fahrenheit for accelerometers), there is equal current flow through the legs of each bridge. When the gyro or accelerometer temperature deviates from the nominal value, the

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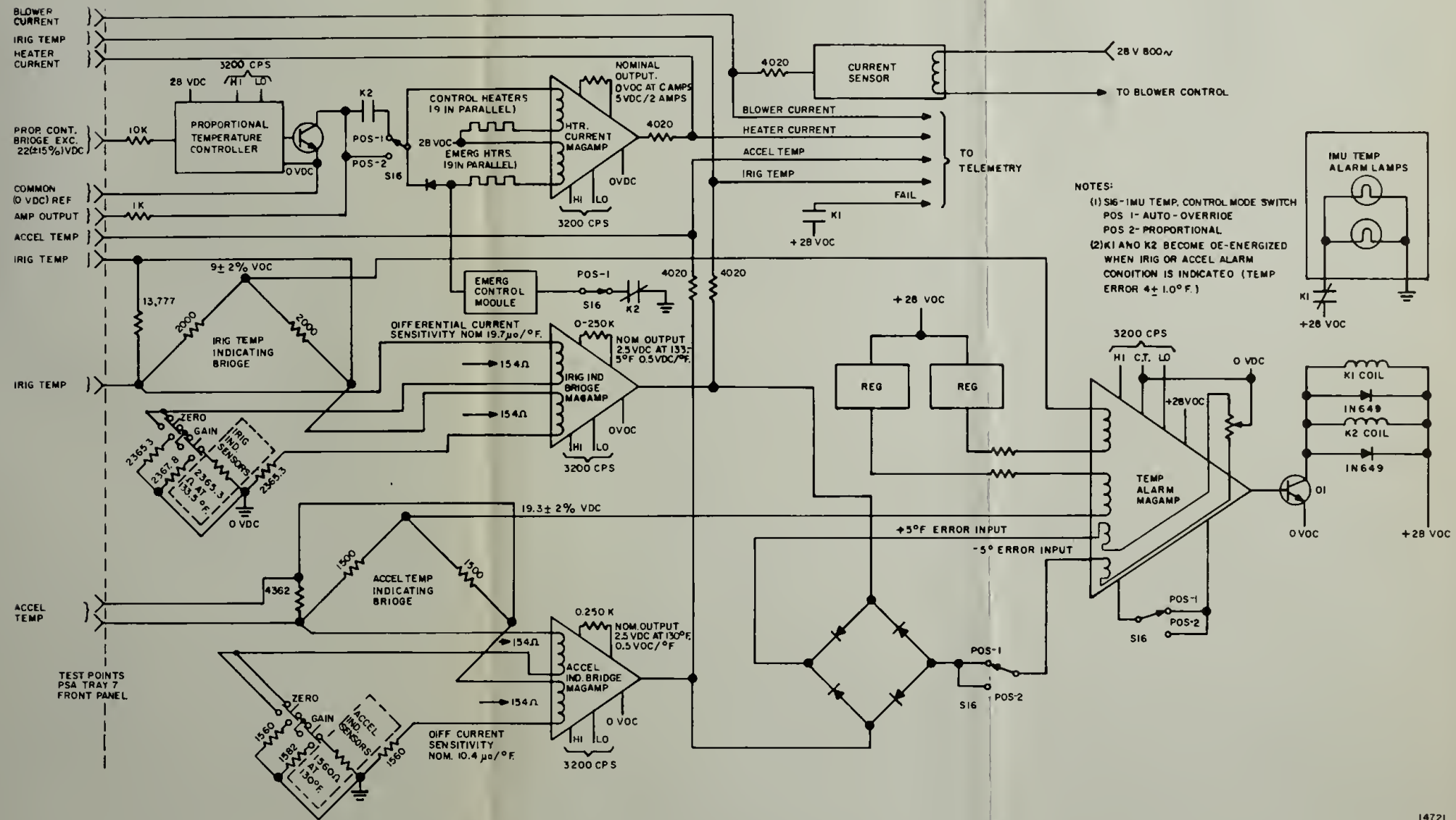
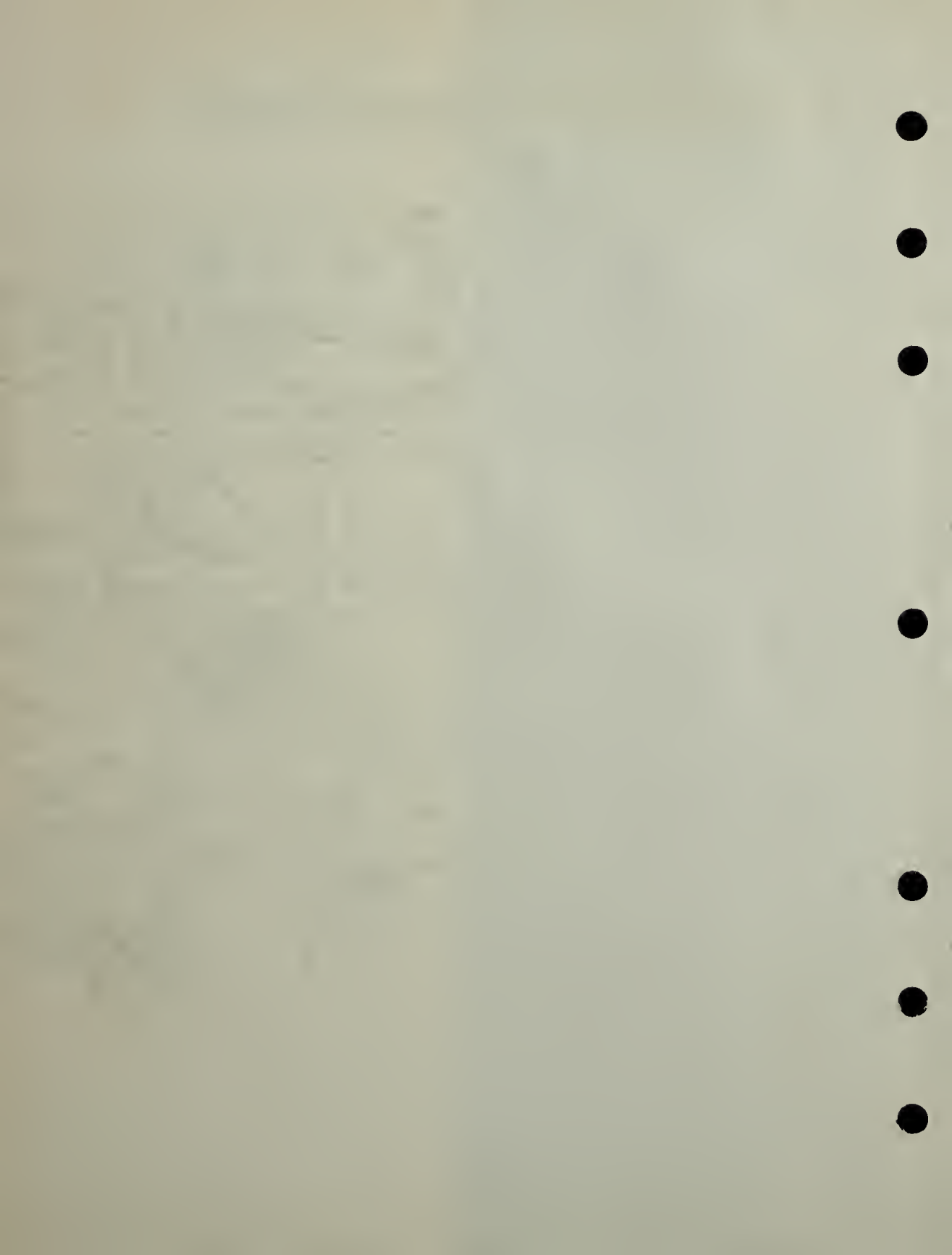


Figure 4-14. Indicating Circuitry, Simplified Diagram





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resistance of its indicating sensors changes. The changed resistance results in unequal current flow through the legs of the bridge in which the sensors are connected. Each bridge is connected so that the current flow through the legs also flows through the control windings of a temperature indicating bridge amplifier. Therefore, the input to the amplifiers is the difference in current flow in the legs of the bridges. The temperature indicating bridges also produce a differential voltage across a resistor connected across the bridges. This differential voltage is routed directly to test points in PSA tray 7 for monitoring purposes. The temperature indicating bridge amplifiers are magnetic amplifiers containing two saturable reactor stages. These amplifiers linearly amplify the differential current in the legs of the indicating bridges. The gyro and accelerometer amplifiers are identical except for the external feedback resistors which adjust the gain according to the application. Each amplifier provides a 0 to 5 volt dc output that is linearly proportional to a temperature deviation of -5 to +5 degrees Fahrenheit (0.5 volt dc/degree). At zero temperature deviation, the nominal output is 2.5 volts dc. The outputs of the indicating bridge amplifiers are applied through a diode bridge logic network to the control windings of the temperature alarm amplifier. The outputs of the indicating bridge amplifiers are also routed directly to telemetry and PSA tray 7 test points as average gyro and accelerometer temperature indications. The temperature alarm amplifier, a magnetic amplifier containing two saturable reactor stages, controls the conduction of output transistor Q1. The output of the temperature alarm amplifier normally maintains transistor Q1 in the on configuration, energizing alarm relays K1 and K2. When the total gyro or total accelerometer temperature deviation is between 3 and 5 degrees Fahrenheit, the temperature alarm amplifier switches transistor Q1 off, deenergizing alarm relays K1 and K2. Deenergized relay K1 routes 28 volts dc to the IMU TEMP lamp on the condition annunciator, indicating an alarm condition, and 28 volts dc to telemetry as an IMU temperature control failure indication. Deenergized relay K2 supplies a ground to the emergency heater control module, enabling the emergency control circuit to provide temperature control if the IMU TEMP MODE selector switch is in position 1 (auto-override).

The indicating circuitry also contains a heater current amplifier and a blower current sensor. The heater current amplifier is a magnetic amplifier which provides a 0 to 5 volt dc output signal that is proportional to the total heater current (0 to 2 amperes) flowing through its control windings. The heater current amplifier output is routed to telemetry and PSA tray 7 test points. The blower current sensor is a transformer circuit module that provides a 0 to 5 volt dc output signal linearly proportional to the 0 to 1.0 ampere, 800 cps blower current flowing through the input winding. The blower current sensor output is routed to telemetry and PSA tray 7 test points.

The calibration and operation of the indicating circuitry can be checked by using the ZERO and GAIN pushbuttons on the G and N indicator control panel. When the ZERO pushbutton is pressed, the gyro and accelerometer indicating sensors are disconnected from their respective temperature indicating bridges and a fixed resistor is connected into each temperature indicating bridge. The fixed resistance is equal to the sensor resistance at the nominal temperature (zero temperature deviation). The output of the indicating bridge is routed to the PSA tray 7 test points where a check can be made on the calibration of the indicating circuitry. With the ZERO pushbutton pressed, the IMU TEMP lamp

on the condition annunciator will not be lighted. When the IRIG GAIN pushbutton is pressed, the gyro indicating sensor is disconnected and a fixed resistor is connected to the gyro temperature indicating bridge. The fixed resistance is equal to the gyro indicating sensor resistance at a -5 degree Fahrenheit temperature deviation. When the PIPA GAIN pushbutton is pressed, the accelerometer indicating sensor is disconnected and a fixed resistor is connected to the accelerometer temperature indicating bridge. The fixed resistance is equal to the accelerometer indicating sensor resistance at a +5 degree Fahrenheit temperature deviation. The output of each bridge is monitored at the test points on PSA tray 7. When either the IRIG GAIN pushbutton or the PIPA GAIN pushbutton is pressed, the IMU TEMP lamp on the condition annunciator lights, providing a visual check on the indicating circuitry. With the IMU TEMP MODE selector switch in position 1 (auto-override) and with either GAIN pushbutton pressed, temperature control automatically switches from proportional control to emergency temperature control, which may be monitored on the PSA tray 7 test points.

4-2.6.2 Proportional Temperature Control Circuit. The proportional temperature control circuit is the primary means of maintaining the gyro and accelerometer temperature and provides the most accurate control. Proportional control is available in two temperature control system modes of operation, auto-override and proportional. The auto-override mode automatically switches from proportional control to emergency control if the proportional control circuit malfunctions. If a malfunction occurs in the proportional mode, the switching to emergency control is performed manually. Figure 4-15 shows the proportional control circuit in the auto-override mode.

The proportional temperature control circuit consists essentially of a temperature control bridge, a temperature control magnetic amplifier, an output power transistor, and the gyro and accelerometer heaters. The bridge output, which is proportional to the gyro temperature deviation, is the input to the temperature control magnetic amplifier. The output of the temperature control magnetic amplifier drives a power transistor, whose switching action provides a ground to energize the gyro and accelerometer heaters.

When the gyro temperature is stabilized at its nominal temperature of 133.5 degrees Fahrenheit, the bridge is balanced and the output error voltage is minimum. A deviation in gyro temperature from the nominal changes the resistance of the temperature control sensors. The changed resistance causes the bridge circuit to produce an output error voltage proportional to the deviation in temperature. The bridge error voltage causes a corresponding current to flow through the control windings of the temperature control magnetic amplifier. The bridge has an adjustable control which adjusts the balance or set point of the bridge to maintain the gyro temperature variation to within plus or minus 0.1 degree of the nominal temperature. The temperature control magnetic amplifier consists of three saturable reactor stages. In conjunction with the output power transistor, the amplifier provides an overall gain of 46 watts of output per microampere of input. The magnetic amplifier supplies a square wave of 6,400 pulses per second to the base of the output transistor. The amplifier output pulses switch on the transistor and maintain the transistor in the on configuration for the duration of the pulse. While the transistor is on, a ground is applied to the gyro and accelerometer control heaters (nine connected in parallel) and the emergency heaters (nine connected in parallel), completing the 28 volt dc circuit that energizes the heaters. The amplifier modulates the width of the output pulses proportional to the temperature control bridge output. The width of the pulses controls the amount of time the transistor is turned on and therefore controls the amount of current drawn by the heaters.

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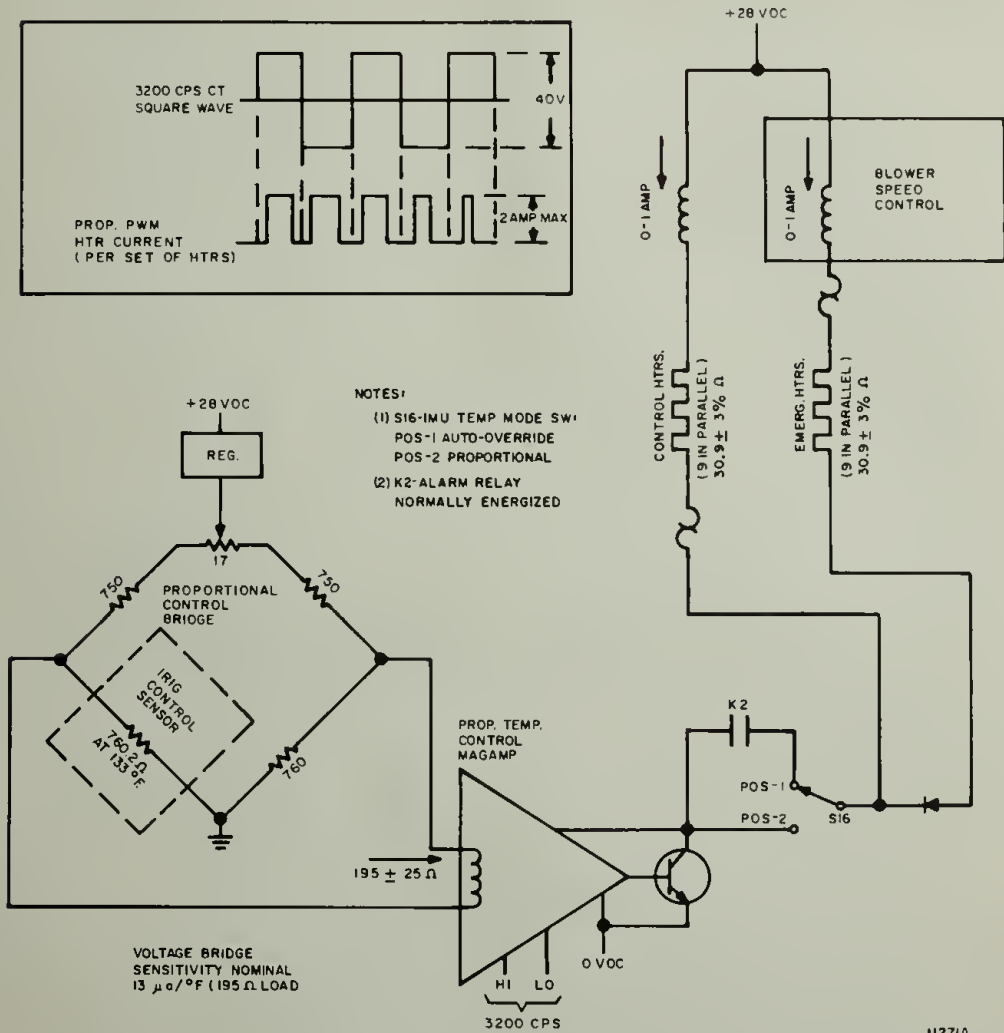


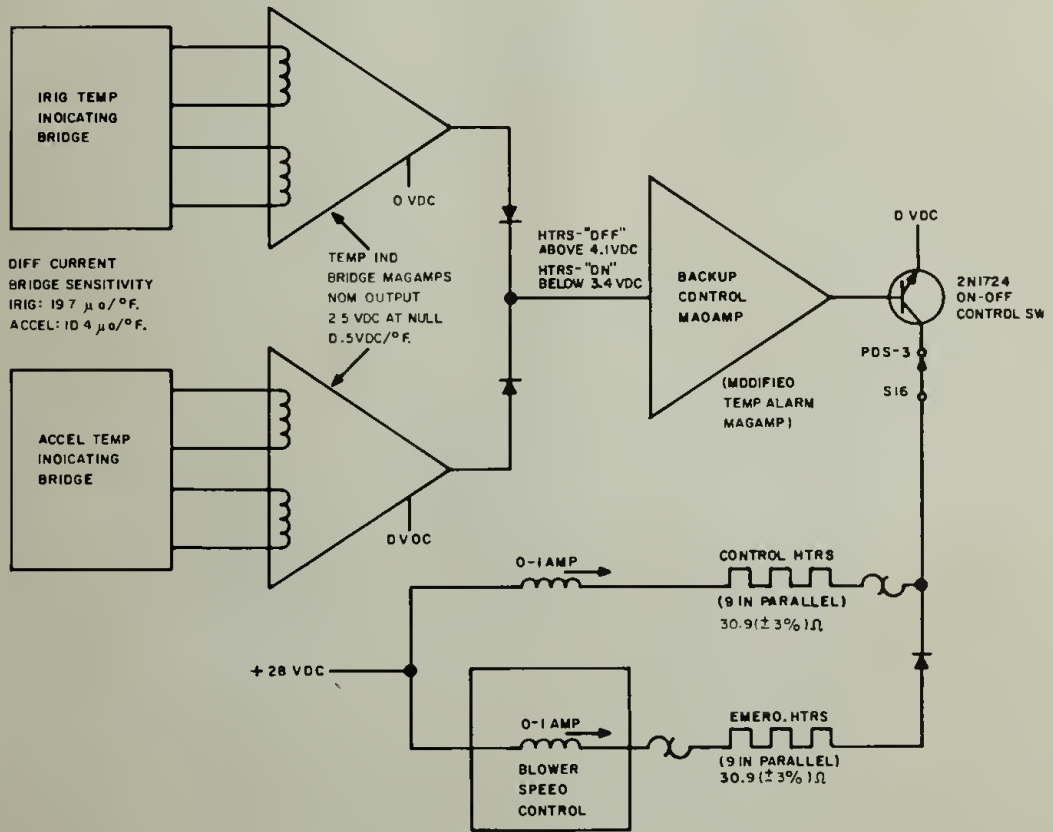
Figure 4-15. Proportional Temperature Control, Simplified Diagram

Since the heater current is proportional only to the temperature deviation sensed by the gyro temperature control sensors, the accelerometers are forced to track the gyros. During IMU operation power may be supplied to the fixed accelerometer heaters to compensate for the heat supplied to the gyro temperature control sensors by gyro wheel motor heat dissipation. The fixed accelerometer heaters are energized by the 28 volt dc regulator module located on the outer gimbal.

During IMU operation the IMU blowers, located on the outer gimbal, are operating. To minimize the controlled heater power required, blower speed control is provided that is inversely proportional to heater current. To accomplish this the emergency heaters are connected in series with the control windings of two saturable reactors (one per blower), which function as blower speed controllers. The saturable reactor 800 cps output to the blowers is at a minimum when the heater current flowing through the control windings is at the 1.0 ampere maximum, and at a maximum when the heater current is zero. Blower speed control is used for all temperature control modes.

4-2.6.3 Backup Temperature Control Circuit. The backup temperature control circuit (figure 4-16) is less accurate than the proportional control circuit. It is used only if the proportional control circuit fails. Setting the IMU TEMP MODE selector to position 3 (backup) activates the backup temperature control circuit. In backup control, portions of the temperature control system indicating circuit are utilized as control circuitry. Modifying the temperature alarm magnetic amplifier circuit connections enables it to operate as a backup control amplifier, providing on-off control to the gyro and accelerometer heaters. The input to the control windings of the temperature alarm amplifier remains the outputs from the IRIG and PIP indicating bridge magnetic amplifier circuits. The IRIG and PIP indicating sensors function as temperature control sensors. The output of each indicating bridge magnetic amplifier is 0 to 5 volts dc, linearly proportional to a temperature deviation of -5 to +5 degrees Fahrenheit (0.5 volt dc/degree). The nominal output of the amplifier is 2.5 volt dc with a zero bridge error input (133.5 degree Fahrenheit for IRIG and 130 degrees Fahrenheit for PIP's).

The modification of the temperature alarm magnetic amplifier consists of connecting output power transistor Q1 to the control and emergency heaters, and removing the excitation from the amplifier bias winding, thereby changing the limits at which output power transistor Q1 is switched on and off. As a result of the operating limit changes, the temperature alarm amplifier switches on the output power transistor, energizing the heaters, when the total output error from either indicating bridge amplifier is above approximately +3.2 degrees Fahrenheit (4.1 volts dc) and switches off the transistor when the error is below approximately +1.8 degrees Fahrenheit (3.4 volts dc). Transistor Q1 therefore, energizes the control and emergency heaters when the gyro temperature becomes lower than 135.3 degrees Fahrenheit as sensed by the gyro indicating sensors, or when the accelerometer temperature becomes lower than 131.8 degrees Fahrenheit as sensed by the accelerometer indicating sensors. Transistor Q1 switches off, deenergizing the heaters, when the gyro temperature becomes 136.7 degrees Fahrenheit as sensed by the gyro indicating sensors, or when the accelerometer temperature becomes 133.2 degrees Fahrenheit as sensed by the accelerometer indicating sensors.



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Figure 4-16. Backup Temperature Control, Simplified Diagram

As a result of the modification within the temperature control circuit during backup control, the IMU TEMP lamp on the condition annunciator does not function meaningfully as a temperature alarm indicator. Since alarm relay K1, which lights the lamp, remains connected to the temperature alarm amplifier output transistor, it is energized when the transistor is on and deenergized when the transistor is off. The IMU TEMP lamp lights when the heaters are off and goes out when the heaters are on. The remaining functions of the temperature control system remain unimpaired.

4-2.6.4 **Emergency Control Circuit.** The emergency control circuit shown in figure 4-17 is used during alarm conditions until the malfunction can be determined. The emergency control is manually activated by setting the IMU TEMP MODE selector to position 4 (emergency), or automatically activated when alarm relay K2 deenergizes while the IMU TEMP MODE selector is in position 1 (auto-override).

The emergency control circuit consists of a heater control module, a mercury thermostat, and the nine emergency IRIG and PIP heaters. The heater control module, located on the stable member, is activated when it receives a 28 volt dc low through the contacts of K2 and/or the IMU TEMP MODE selector. The emergency heaters are energized by a 28 volt dc high through the control windings of the blower speed control magnetic amplifier and through the contacts of a safety thermostat, and a 28 volt dc low through the switching action of power transistor Q2. The mercury thermostat, located on the stable member near the emergency heaters, acts as a control sensing element. When the mercury thermostat is closed (above 130 degrees Fahrenheit), the base of transistor Q1 is shorted to ground and the heater control module is inoperative. When the mercury thermostat opens (below 128 degrees Fahrenheit), the short is removed allowing transistor Q1 to conduct. Transistor Q1 drives transistor Q2 to conduction, applying a ground to the emergency heaters. A mercury thermostat heater, connected in parallel with the emergency heaters, improves the mercury thermostat response to gyro and accelerometer temperature changes. The IMU TEMP lamp on the condition annunciator lights and remains lighted during the emergency control operation.

### 4-3 POWER AND SERVO ASSEMBLY

The PSA provides a central mounting point for the guidance and navigation (G and N) system power supplies and a majority of the G and N system electronics. The operation of those G and N system electronics located in the PSA is discussed fully in the functional descriptions contained in Chapter 2. The power supplies located in the PSA are the inertial subsystem (ISS) power supplies, the optical subsystem (OSS) power supplies, and the signal conditioner power supplies.

4-3.1 **INERTIAL SUBSYSTEM POWER SUPPLIES.** Inputs to the ISS power supplies are 7 volt signal pulses from the AGC and +28 volts from the spacecraft dc primary power.

4-3.1.1 **-28 Volt DC Supply.** The -28 volt dc power supply module is in tray 1 of the PSA. It supplies excitation to three gimbal servo amplifier modules and three gimbal coarse align amplifier modules in tray 1 of the PSA. It also supplies excitation to three ac differential amplifier modules located in trays 3 and 4. The -28 volts dc is also supplied to the

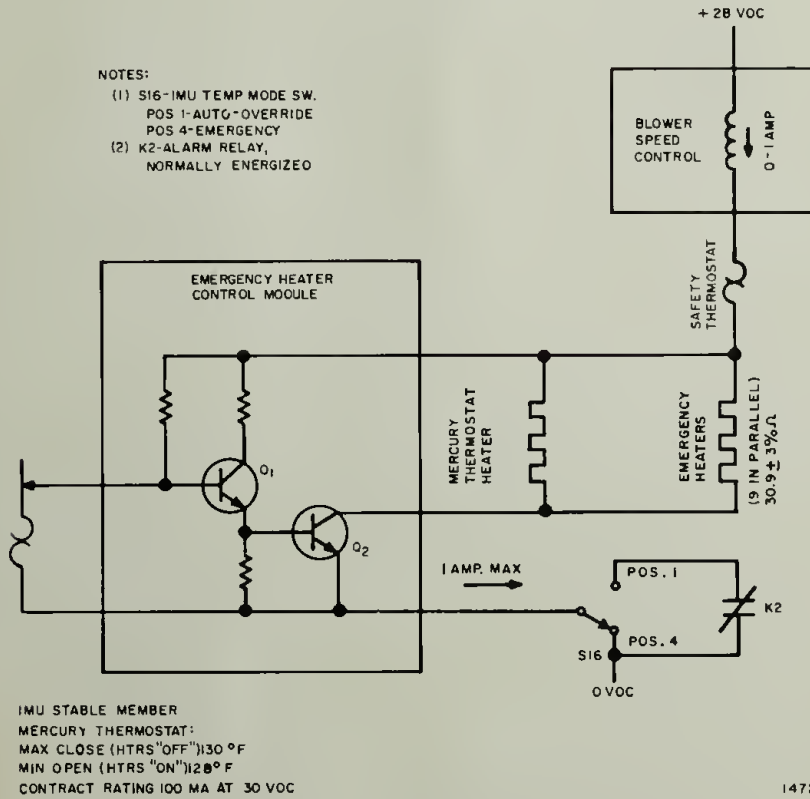
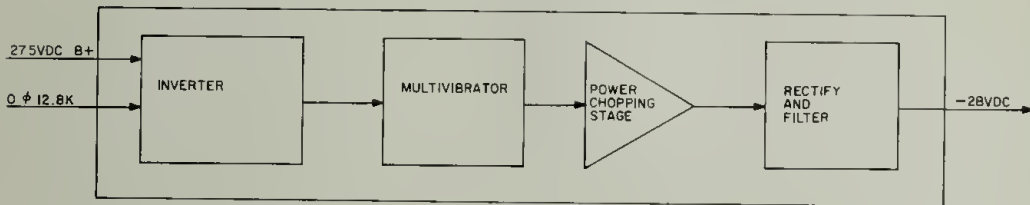


Figure 4-17. Emergency Temperature Control, Simplified Diagram

ADA preamplifiers in the IMU. (See figure 4-18.) Inputs to the -28 volt dc power supply are +27.5 volt dc primary power for B+ application and 12,800 pps continuous power from the AGC scaler as a 7 volt, 3 microsecond square pulse. The 12,800 pps input is inverted and supplied to a multivibrator with a triggered frequency of 6.4 kc. If no input is supplied to the multivibrator, it free-runs at 6.0 to 6.2 kc. The multivibrator output drives a high-power chopping stage. The output of this chopping stage is applied to a full-wave rectifier through transformer coupling. The full-wave rectifier circuit provides a filtered negative voltage output.



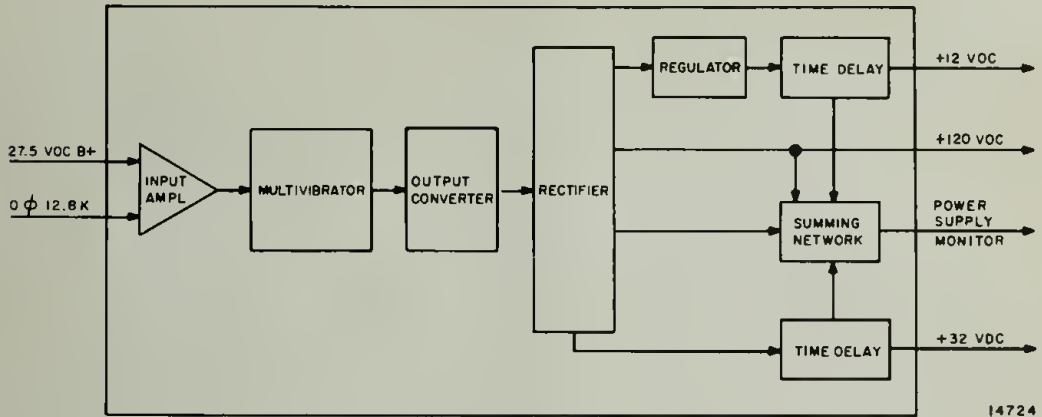
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Figure 4-18. -28 Volt DC Power Supply, Block Diagram

4-3.1.2 Pulse Torquing DC Power Supply. The pulse torquing dc power supply module is in trays 2 and 7 of the PSA. This power supply provides one of the 16 PIPA current switch excitations, one of the 25 IRIG current switch excitations, precision voltage regulator power, and a monitoring signal for the pulse torquing dc power supply outputs. The pulse torquing dc power supply modules can be used interchangeably as a 25 IRIG power supply or 16 PIPA power supply. When they supply the three PIP accelerometer loops, the +12 volt dc output is not used. (See figure 4-19.) A 27.5 volt dc B+ signal from spacecraft primary power and a 5 volt, 3 microsecond, square pulse at 12,800 pps from the AGC scaler are the inputs to the pulse torquing dc supply. The pulse train input is inverted and supplied to a multivibrator which is triggered, and runs at 6.4 kc. If an input is not supplied, the multivibrator free-runs at 6.0 to 6.2 kc. The output of the multivibrator is supplied to a high-power chopping stage which amplifies, chops, and transformer-couples the signal to a full-wave rectifier. The +12 volt dc output is regulated using a three stage transistor circuit with a zener reference.

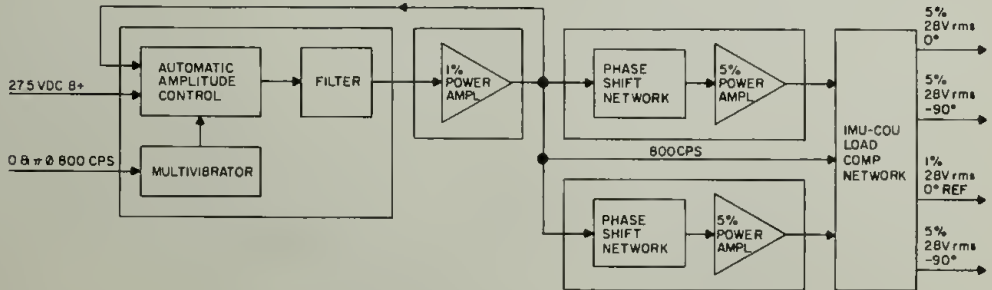
4-3.1.3 IMU-CDU 800 CPS Power Supply. The IMU-CDU 800 cps power supply consists of three types of modules; automatic amplitude control, filter and multivibrator; 1 percent amplifier; and 5 percent amplifier. The IMU-CDU 800 cps power supply contains two 5 percent amplifiers, one of which is in tray 10 of the PSA. The remaining modules of the IMU-CDU 800 cps power supply are in tray 2 of the PSA. (See figure 4-20.) The





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Figure 4-19. Pulse Torquing DC Power Supply, Block Diagram



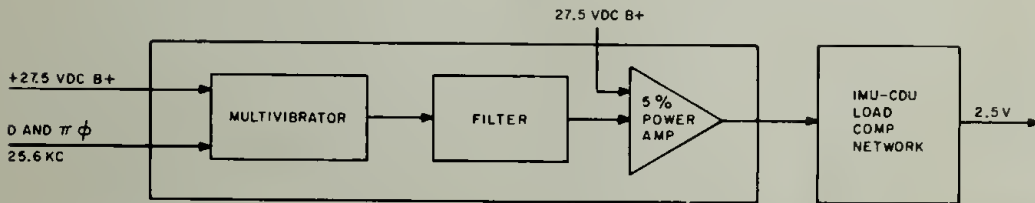
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Figure 4-20. IMU-CDU 800 CPS Power Supply, Block Diagram

output of the 800 cps, 1 percent amplifier provides coupling display unit (CDU) resolver excitation, CDU tachometer excitation, autopilot reference, IMU resolver excitation, and coarse align demodulation. The output of one 5 percent amplifier is used for 25 IRIG wheel excitation and the other 5 percent amplifier provides IMU blower and CDU motor excitation. A dual phase (zero and pi), 800 cps, 5 volt, 3 microsecond pulse from the AGC scaler is the input to a multivibrator that is part of the automatic amplitude control, filter and multivibrator module. The automatic amplitude control output is filtered before it is supplied as an input to the 1 percent power amplifier module. The output of the 1 percent power amplifier is a 28 volt rms signal which, in addition to its direct uses, is a feedback signal to the automatic amplitude control and an input to the 5 percent power

amplifiers. The input signal to the 5 percent power amplifiers is applied to a phase shift network and then amplified to obtain the 28 volt rms, -90 degree out-of-phase output. The outputs of both the 5 percent and the 1 percent power amplifiers are applied to an IMU-CDU load compensation network to provide a power factor correction. In addition, a portion of the 5 percent power amplifier output is phase shifted +90 degrees back to 0 degree by the IMU-CDU load compensation network. The other portion remains at -90 degrees. Both 5 percent outputs of the IMU-CDU load compensation network supply the 25 IRIG wheel with two phase excitation. The -90 degree output is also the excitation for the IMU blowers and the CDU motors.

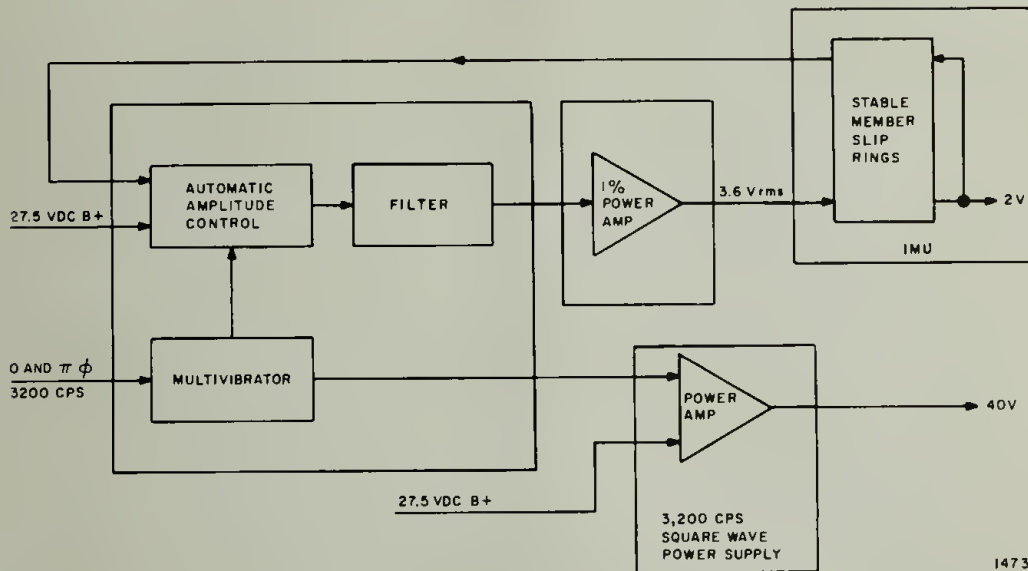
4-3.1.4 IMU-CDU 25.6 KC Power Supply. The IMU-CDU 25.6 kc power supply module is in tray 2 of the PSA. The outputs of this power supply provides IMU-CDU encoder excitation. (See figure 4-21.) The zero and pi phase, 25.6 kc, 3 microsecond pulse continuous AGC input is sent to a multivibrator in conjunction with a 27.5 volt dc, B+ voltage. The output of the multivibrator is filtered and amplified. The amplifier output is 2.5 volts, 25.6 kc. The IMU-CDU load compensation network provides a power factor correction for the 2.5 volt signal.



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Figure 4-21. IMU-CDU 25.6 KC Power Supply, Block Diagram

4-3.1.5 3,200 CPS Power Supply. The 3,200 cps power supply consists of three modules in tray 1 of the PSA: an automatic amplitude control, a 1 percent power amplifier, and a square wave temperature control power supply. (See figure 4-22.) The outputs of the 3,200 cps power supply provide 16 P1P and 25 IRIG ducosyn magnetic suspension and signal generator primary excitation. The 3,200 cps, square wave power supply is used for IMU heater control. In addition to the 27.5 volt dc, B+ voltage, a zero and pi phase, 5 volt input pulse is applied to a multivibrator in the automatic amplitude control circuitry. The multivibrator, supplies a signal to the automatic amplitude control and the 5 percent power amplifier of the temperature control module. The signal from the automatic amplitude control is chopped and filtered and used as an input to the 1 percent power amplifier. The amplifier output provides the excitation for ducosyn signal generator and magnetic suspension units. The amplifier output is exactly 2.0 volts when sensed at the stable member. This 2.0 volt level is used as a feedback signal to the automatic amplitude control module.



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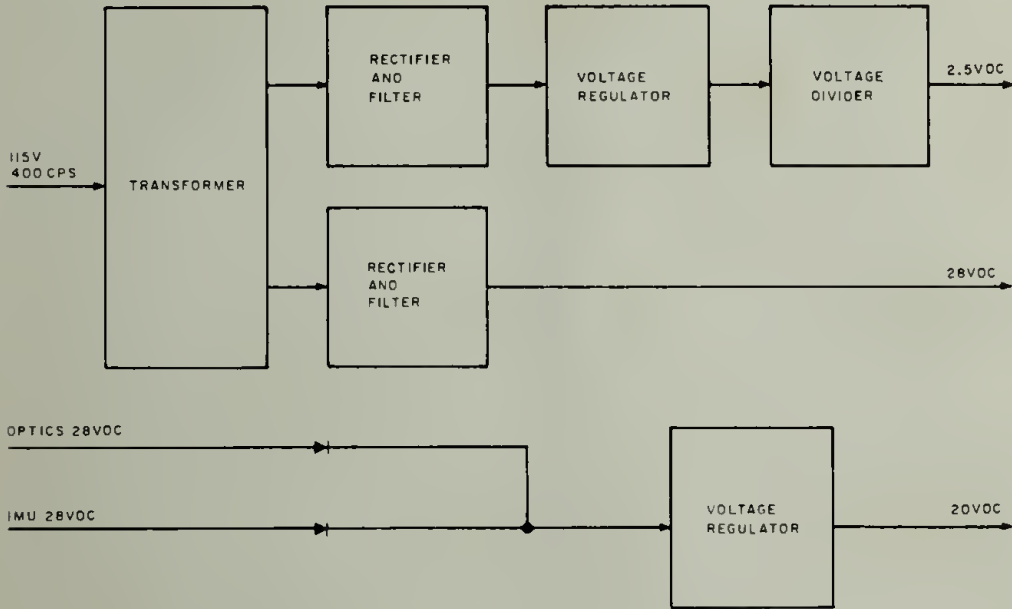
Figure 4-22. 3,200 CPS Power Supply, Block Diagram

4-3.2 OPTICAL SUBSYSTEM POWER SUPPLIES. The inputs to the OSS power supplies are 5 volt signal pulses from the AGC and the +28 volt dc primary spacecraft power.

4-3.2.1 Optics 800 CPS Power Supply. The optics 800 cps power supply is in tray 6 of the PSA. The optics 800 cps power supply is identical to the IMU-CDU 800 cps power supply except that it does not have two 5 percent amplifiers. The output from the 1 percent amplifier is used for optics CDU tachometer and resolver excitation. The output from the 5 percent amplifier provides optics CDU servomotor excitation and sextant power.

4-3.2.2 Optics 25.6 KC Power Supply. The optics 25.6 kc power supply is in tray 2 of the PSA. It is identical to the IMU-CDU 25.6 kc power supply. The output of the optics 25.6 kc power supply provides optics CDU encoder excitation.

4-3.3 SIGNAL CONDITIONER POWER SUPPLIES. The signal conditioner power supply module consists of three separate power supplies which provide 2.5 volt dc conditioning bias voltage and 20 volt dc B+ supply voltage to the signal conditioner assembly. The module also provides 28 volts dc for IMU pressure transducer excitation. The signal conditioner power supply module is in tray 10 of the PSA. (See figure 4-23.)



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Figure 4-23. Signal Conditioner Power Supplies, Block Diagram

Inputs to the signal conditioner power supplies are optics 28 volts dc, IMU 28 volts dc, and 115 volts, 400 cps. The 115 volt, 400 cps input is applied to a transformer that has two output windings. One output of the transformer is rectified and filtered to provide the 28 volt dc pressure transducer supply. The second transformer output is rectified, filtered, and applied to a series regulator circuit. The output of the regulator is attenuated by a voltage divider to provide the 2.5 volt dc conditioning bias voltage. The optics 28 volts dc and the IMU 28 volts dc are applied to the 20 volt dc signal conditioner B+ power supply circuit through isolation diodes so that the power supply circuit will continue to function as long as either 28 volt dc input is present. The 28 volt dc input is applied across a zener diode and resistor to provide a reference to a regulator circuit whose output provides the signal conditioner assembly B+ supply.

#### 4-4 DISPLAY AND CONTROL GROUP

The display and control group includes the G and N indicator control panel, the IMU control panel, the optics shroud and cover assembly, the control electronics, and the D and C electronics. The operation of the IMU control panel and the optics shroud and cover assembly are apparent in the functional descriptions given in Chapter 2 and require no further discussion. The same is true of the G and N indicator control panel with the exception of the optics hand controller and the attitude impulse switch, both of which are mounted on the G and N indicator control panel. The operation of these two components and the operation of the control electronics and the D and C electronics are discussed in subsequent paragraphs.

**4-4.1 DISPLAY AND CONTROL ELECTRONICS.** The D and C electronics are welded, encapsulated, plug-in modules mounted on a base assembly which is attached to the spacecraft structure above the left PSA tray. The electronics consists of portions of the panel brightness control circuit, a time delay module, a relay and diode module, and three attitude error demodulators. The relay and diode module contains circuitry associated with mode control of the ISS. The operation of the relay and diode module is discussed fully in Chapter 2.

**4-4.1.1 Panel Brightness Control Circuit.** The panel brightness control circuit allows the navigator to control the brightness of various lamps and indicators in the spacecraft. The panel brightness control circuit consists of a saturable reactor, a potentiometer, and a sensitive switch. The 6 volt, 400 cps lamp power is applied to the lamps through the ac winding of the saturable reactor. A change in current flow in the dc control winding affects the impedance of the ac winding. The varying impedance results in a change in the voltage across the lamps. The panel brightness control potentiometer, located on the G and N indicator control panel, is shunted directly across the dc control winding and diverts all or part of the dc current through the potentiometer. When the potentiometer resistance is adjusted to its maximum value, most of the dc current flows through the control winding. The dc current in the control winding causes the reactor core to saturate, effectively decreasing the impedance of the ac winding to a minimum. The decreased impedance then allows nearly all of the applied 6 volts to be dropped across the lamps (at least 5.5 volts). When the resistance of the potentiometer is at a minimum, all of the dc current is diverted through the potentiometer. With no dc current in the control winding, the impedance of the ac winding is at its maximum value. Nearly all of the applied 6 volts is then dropped across the ac winding, leaving a very low voltage across the lamps (no more than 0.3 volt). When the potentiometer is adjusted to its minimum resistance position, a cam on the potentiometer shaft actuates the switch which deenergizes the dc control circuitry.

**4-4.1.2 Time Delay Circuit.** The time delay circuit is used during IMU turn-on to provide time for the stabilization gyro wheels to come up to speed before power is applied to the stabilization loop. When the ISS is switched into the operate mode, 28 volt dc, B+ voltage is applied to the time delay module to initiate the timing cycle. The 28 volts dc is applied across a dropping resistor and an 18 volt zener diode. The 18 volts at the zener diode is applied to a resistor-capacitor network that has a time constant of 100 seconds. The resistor-capacitor network controls the conduction of a transistor. The transistor conducts to saturation during the initial heavy surge of charging

current and then starts cutting off as the voltage across the capacitor builds up and the charging current decreases. The function of the transistor is to hold the base of a second transistor near ground potential and prevent it from conducting. The second transistor is a Darlington circuit device which, because of its very high input impedance, provides an isolation stage between the timing circuitry and the output or relay driver stage. As the first transistor starts cutting off, it allows the voltage at the base of the second transistor to rise. The resulting rising emitter current in the second transistor produces a rising voltage across its emitter resistor. The emitter resistor voltage is applied to a 12 volt zener diode. When the voltage across the zener diode reaches 12 volts, conduction occurs through a resistor to ground, establishing a voltage across the resistor. This voltage provides a positive potential at the base of a third transistor, the output switching transistor. The positive potential applied by the conducting zener diode overcomes the small amount of emitter reverse bias that is applied at the start of the timing cycle to keep the output transistor turned off. When the output transistor is switched on, it applies a 0 volt dc ground return which energizes relay K6, located in the relay and diode module. Energized relay K6 closes the 0 volt dc mode relay common line, thereby enabling power application to the stabilization loop.

A second feature of the time delay module is that a subsequent ISS power turn-on occurring within a certain time limit after power turn-off does not create a full 100 second time delay. This feature is added because a 100 second time delay is not necessary if the gyro wheels are still spinning, which they will continue to do after the power has been removed. The less than 100 second time delay is accomplished by forcing the capacitor to discharge through a resistance that is much higher than the resistance that controlled the charging current, giving the resistor-capacitor network a long discharge time. If an ISS power turn-on occurs before the resistor-capacitor network has completely discharged, the ensuing time delay will be shortened since fewer than 100 seconds will be required to recharge the capacitor.

4-4.1.3 Attitude Error Demodulator. The three attitude error demodulators receive and demodulate the 800 cps error signal ( $E_{ig}$ ,  $E_{mg}$ , and  $E_{og}$ ) resulting from the difference between the angular position of the IMU and CDU 1X resolvers. The error signal input to each demodulator is applied through an input transformer to two transistors connected in a Darlington type circuit to provide a high input impedance. The error signal is then transformer-coupled to a phase sensitive demodulator circuit consisting of two dual emitter chopper/switch transistors. The switching action of the transistors is controlled by a switch drive circuit consisting of an 800 cps reference signal applied through a transformer to the base-collector junction of each transistor. The switch drive circuit alternately turns on one transistor while the other one is turned off. The output is a dc signal whose magnitude and polarity are dependent on the magnitude and phase of the input error signal, respectively. The dc output is filtered by a capacitor and applied to the IMU-CDU difference meter. The demodulator provides a unity output-to-input voltage ratio. To keep the output within the range afforded by the 0 to 2 volt full scale meter movement, the input is clipped above 2.2 volts.

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4-4.2 CONTROL ELECTRONICS. The control electronics, in conjunction with the G and N indicator control panel, provides switching for the gimbal lock lamps, and supplies excitation for testing and operating lamps in the lower display and control group and the condition annunciator. The control electronics consists of a power transformer and a relay and diode module. Both are mounted on a base assembly which is attached to the spacecraft structure behind the G and N indicator control panel.

A 115 volt, 400 cps input from the spacecraft electrical power system energizes the power transformer primary winding. The transformer secondary windings provide 6 volt lamp excitation, a 1.5 volt output of zero and pi phase, and a 26 volt output. The 1.5 volt output and the 26 volt output are not used in the G and N system configuration covered by this document.

The relay and diode module contains two relays. One relay is energized by the 28 volt dc gimbal lock signal from the limit switch on the middle gimbal axis. The signal is present when the middle gimbal angle exceeds plus or minus 60 degrees with respect to the outer gimbal. One set of energized relay contacts applies 28 volts dc to light the gimbal lock lamp on the condition annunciator. A second set of energized relay contacts applies spacecraft 0 volt dc to light the gimbal lock lamp on the spacecraft main display and control panel. The second relay is energized by a MARK command from the G and N indicator control panel or by an automatic MARK command from the horizon sensor. A set of energized contacts routes the MARK command to the AGC.

4-4.3 OPTICS HAND CONTROLLER. The optics hand controller drives the sextant to a desired trunnion and shaft position during either the direct manual optics mode or the resolved manual optics mode. The optics hand controller output is applied through relays to the sextant drive amplifiers. The telescope follows the sextant during manual optics mode; however, during the track mode, when the sextant is driven automatically by the star tracker, the telescope trunnion may be driven directly by the optics hand controller.

The optics hand controller consists of a handle which drives a gear train to position either of two synchro resolvers. Up and down movements of the handle position the resolver that drives the sextant to a trunnion position during the direct mode. Left and right movements position the resolver that drives the sextant to a shaft position during the direct mode. The resolver rotor windings are excited by the output of a speed controller switch which selects 28 volts, 800 cps, when the switch is set to HI, or lower values from taps of a stepdown transformer when the switch is set to MED or LOW. The voltage induced in the resolver stator windings depends upon the rotor winding excitation and the angular position of the rotor. When the optics hand controller is at its neutral position, both resolvers are at null, with outputs of less than 200 millivolts. The maximum output obtainable from either resolver, with the speed controller switch set to HI and the optics hand controller moved to its physical limit in the proper direction, is 10.5 volts rms. Left and down movements produce outputs of zero phase. Right and up movements produce outputs of pi phase. The maximum output obtainable from both the trunnion resolver and the shaft resolver is 1.29 volts rms with the speed controller switch set at the MED position, and 0.129 volt rms with the speed controller set to the LOW position.

4-4.4 ATTITUDE IMPULSE SWITCH. The attitude impulse switch commands small precise spacecraft attitude changes in all three axes, individually or simultaneously, when aligning the sextant for navigation sightings. The attitude impulse switch is connected to the stabilization and control system (SCS). The normal rate and attitude signals are disconnected from the SCS channels when the ATTITUDE IMPULSE ENABLE switch is placed in the ON position during SCS attitude control mode or G and N attitude control mode.

The attitude impulse switch consists of six single pole-single throw momentary contact switches (two per axis) and an actuating shaft. The switches are positioned about the shaft and adjusted so that deflections of the shaft will actuate the switches. A pair of switches is associated with each direction of shaft deflection: up and down deflections actuate the pitch switches, right and left deflections actuate the roll switches, and a twisting or turning motion actuates the yaw switches. Any combination of roll, yaw, and pitch switches may be actuated by moving the shaft diagonally and twisting the shaft. The attitude impulse control signal generation is internal to the SCS, but is commanded or activated by deflection of the attitude impulse switch. When a momentary contact switch in the attitude impulse switch is actuated, it completes the connection from the SCS signal source to the proper control channels of the SCS and causes a switching amplifier in the SCS to generate a single pulse, the polarity of which will move the spacecraft in the desired direction. The pulse is applied through the jet selection logic circuit to the jet control solenoids setting up a reset sequence that opens (fires) a jet, then closes it immediately to generate a minimum impulse. The duration of the minimum impulse is approximately 12 milliseconds and will initiate a spacecraft rotation drift rate of less than 0.24 arc minutes/second.

#### 4-5 SIGNAL CONDITIONER ASSEMBLY

The signal conditioner assembly (signal conditioner) receives 34 G and N system signals and converts each of them to a common voltage and impedance range (0 to 5 volts) acceptable to the spacecraft pulse code modulated (PCM) multiplexer or encoder. Four additional signals, which do not require conditioning, are routed through the signal conditioner to the multiplexer. The multiplexer then transforms the conditioned signals into a form suitable for telemetry transmitter modulation. The signal conditioner also provides isolation between the component or circuit being monitored and the telemetry system. The signal conditioner consists of six different modules and a mounting frame assembly on which the modules are mounted. The complete signal conditioner is mounted to the rear of the G and N system station in the spacecraft.

Each type of module is designed to condition a particular type of G and N system signal. The six conditioning modules are:

- (1) Torque motor signal conditioner.
- (2) CDU resolver signal conditioner.
- (3) Scaling signal conditioner.



- (4) IRIG and PIPA signal conditioner.
- (5) Gimbal signal conditioner.
- (6) Optics signal conditioner.

The signal conditioner receives 20 volt dc, B+ supply voltage and 2.5 volt dc conditioning bias voltage from the signal conditioner power supply in tray 10 of the PSA. The 20 volt dc B+ is applied to each module except the optics signal conditioner. The 2.5 volt dc bias voltage is connected in series with the outputs of all modules except the scaling signal conditioner so that the 2.5 volt dc bias low becomes the common low to the telemetry system. (See figure 4-24.) The 2.5 volt dc bias high is connected to the signal low of each module and becomes the reference point for the 0 to 5 volt signal outputs of the signal conditioner modules. In this manner a zero phase ac signal, after conditioning, may be represented as a dc voltage value above the 2.5 volt reference. A pi phase signal, after conditioning, may be represented as a dc voltage value below the 2.5 volt reference. Bipolar dc signals from the G and N system which may be positive or negative and have a zero volt reference may, after conditioning, be represented in a similar manner. Positive voltages may be represented as a voltage value above the 2.5 volt reference and negative voltages may be represented as a voltage value below the 2.5 volt reference.

**4-5.1 TORQUE MOTOR SIGNAL CONDITIONER.** The torque motor signal conditioner module conditions the inner, middle, and outer gimbal torque motor signals to a representative 0 to 5 volt dc voltage. The module contains three identical signal conditioning circuits. Each circuit contains a chopper, an ac amplifier, and a phase sensitive demodulator. The input signals, which may vary from approximately +7 to -7 volts dc, are received from the torque drive amplifiers.

The incoming dc signal is first applied to a chopper circuit consisting of two dual emitter chopper/switch transistors. The chopper modulates an 800 cps square wave reference with the dc input. The modulated square wave, which is representative of the magnitude and polarity of the dc input, is transformer-coupled to the ac amplifier. The amplified signal is transformer-coupled to a phase sensitive demodulator circuit consisting of two dual emitter chopper/switch transistors. The switching action of the transistor pairs in both the chopper circuit and the demodulator circuit is controlled by a switch drive circuit consisting of an 800 cps reference signal applied through a transformer to the base-collector junction of each transistor. The switch drive circuit alternately turns on one transistor while the other one is turned off. The output of the demodulator is a pulsating dc signal whose magnitude and polarity are dependent on the magnitude and polarity of the input signal. The output of the demodulator is filtered and then biased at 2.5 volts dc. The output of the torque motor signal conditioner, which could vary from +2.5 volts to -2.5 volts at a zero reference will, as a result of the 2.5 volt reference, remain in a 0 to 5 volt range.

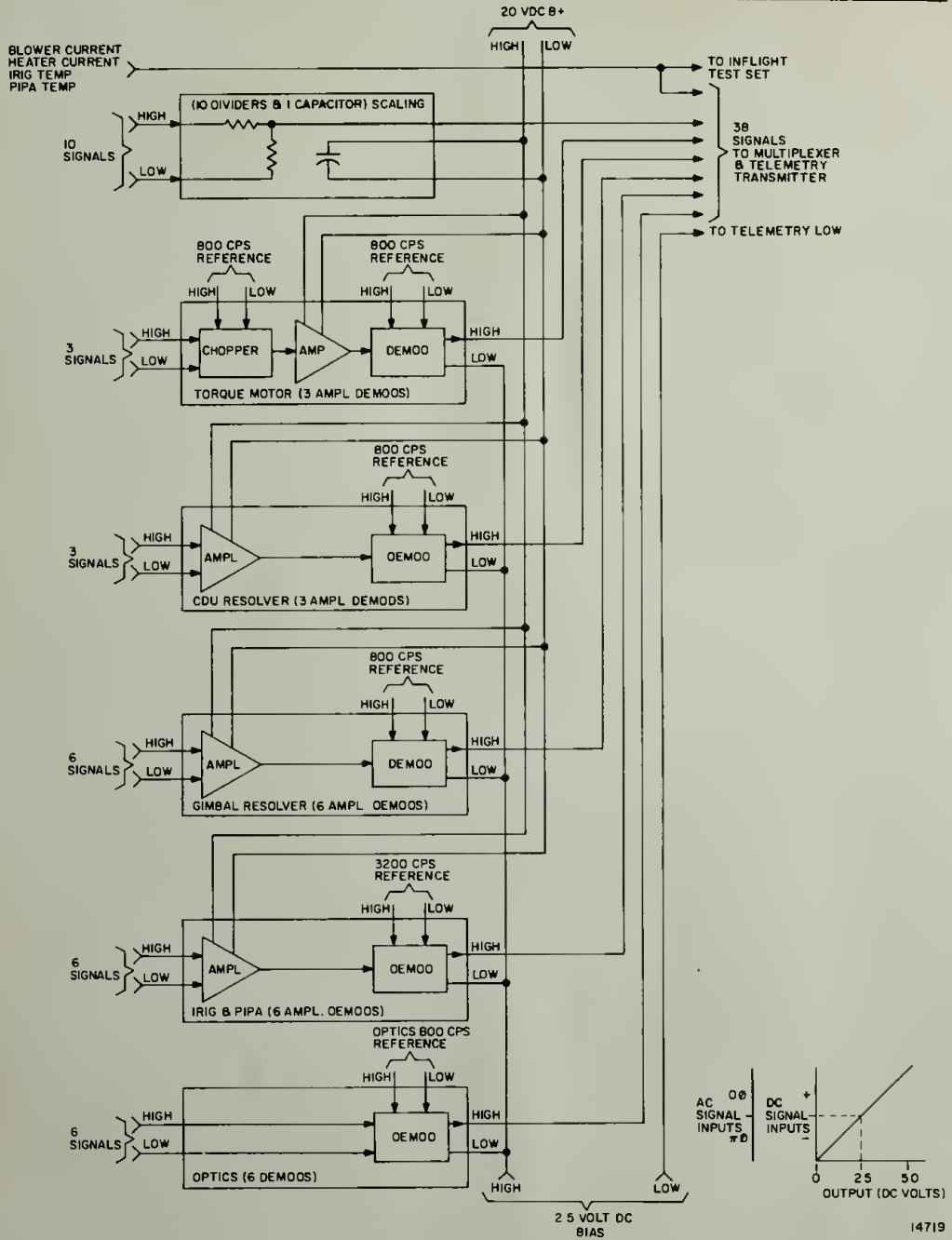


Figure 4-24. Signal Conditioner, Block Diagram

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4-5.2 CDU RESOLVER SIGNAL CONDITIONER. The CDU resolver signal conditioner module conditions the inner, middle, and outer gimbal CDU 1X resolver error signals into a representative 0 to 5 volts dc. The module contains three identical signal conditioning circuits, each of which contains an amplifier and a phase sensitive demodulator. The inputs to the amplifier and demodulator are transformer-coupled. The operation of the demodulators is similar to that in the torque motor signal conditioner module. The magnitude and polarity of the CDU resolver demodulator, however, are dependent on the magnitude and phase of the input signal, respectively.

4-5.3 SCALING SIGNAL CONDITIONER. The scaling signal conditioner module conditions ten discrete dc signals which require only voltage division. The voltage divider circuits drop the input signals to the proper 0 to 5 volt level. The scaling signal conditioner module also contains a capacitor which filters the 20 volt dc, B+ supply voltage.

4-5.4 IRIG AND PIPA SIGNAL CONDITIONER. The IRIG and PIPA signal conditioner module conditions six signals. Three signals are the three 16 PIP ducosyn signal generator outputs. The other three signals originate at the 25 IRIG signal generators. As a result of the resolution of the X and Z gyro signals, the three signals represent the Y gyro and inner gimbal error, the middle gimbal error, and the outer gimbal error. The module contains six identical signal conditioning circuits, each containing an amplifier and a phase sensitive demodulator. The demodulator is similar in operation to the demodulators previously discussed. The IRIG and PIP demodulators, however, require a 3,200 cps reference. The 3,200 cps reference is applied to six modulator circuits through a buffer transformer and amplifier circuit which provides isolation between the signal conditioner module and the 2 volt, 3,200 cps source.

4-5.5 GIMBAL RESOLVER SIGNAL CONDITIONER. The gimbal resolver signal conditioner module conditions the signals from the sine and cosine windings of the inner, middle, and outer gimbal 1X resolvers. The module contains six signal conditioning circuits, each containing an amplifier and a phase sensitive demodulator. The operation of the circuits is similar to the CDU resolver signal conditioning circuits.

4-5.6 OPTICS SIGNAL CONDITIONER. The optics signal conditioner module conditions signals from the shaft and trunnion CDU MDA's, the sextant trunnion and sextant shaft MDA's and the direct shaft and trunnion controllers. The module contains six signal conditioning circuits, each of which is a phase sensitive demodulator. The reference for the demodulators is from the optics 800 cps, 1 percent power supply.

#### 4-6 COUPLING DISPLAY UNIT

The coupling display units (CDU) provide a coupling between the AGC or the astronaut and the IMU and the optics. Either the AGC or the astronaut may transmit angular data to the IMU. The CDU also provides the astronaut a visual readout of the IMU and optics angular data during the coarse align, fine align, and manual CDU modes of operation. Desired angles are transmitted by the CDU loop to the IMU in analog form during the coarse align and manual CDU modes. The CDU loop is also capable of repeating the IMU gimbal angles and the optics angles, and transmitting this angular data to the AGC in

digital form in fine align mode. The CDU's in the ISS may also be used to provide a coupling between the astronaut or AGC and the SCS. Five CDU's are required by the G and N system, three in the ISS, and two in the OSS. Each CDU contains a servo motor-tachometer, four resolvers, a digital encoder, three display dials, and a thumbwheel; all are interconnected by a stainless steel gear train. Each CDU also contains a slew switch, which is not utilized in the OSS CDU loop application. The gear train is driven by either the thumbwheel or the servo motor-tachometer. The servo motor-tachometer is an 800 cps ac unit which drives the CDU gear train and produces a feedback signal proportional to the output shaft rate. The motor is driven by the MDA in the PSA. Input signals to the MDA are received from the CDU resolvers, the digital to analog converter in the PSA, and the slew switch; all of which represent CDU loop errors. The motor converts the various CDU loop error signals into the appropriate output shaft angle and velocity. The tachometer provides a negative feedback signal, proportional to the motor shaft speed, to the MDA. The slew switch provides a 6.25 volt, 800 cps signal of zero or pi phase to the MDA to position the ISS CDU's during the manual CDU mode of operation. The four resolvers can be utilized either for angular data transmission or angular error resolution. The specific resolvers utilized and their functions depend on the CDU application. The digital encoder (figure 4-25) converts the angular motion of the CDU output shaft into a digital signal which can be used by the AGC.

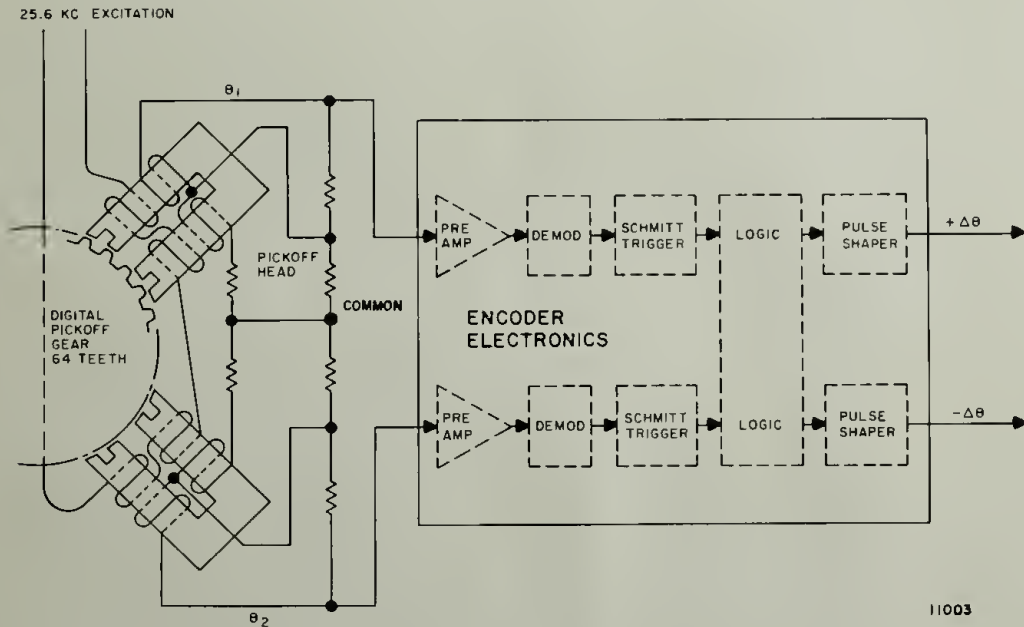


Figure 4-25. Digital Encoder, Functional Diagram

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The digital encoder consists of a digital pickoff gear, two U-shaped digital pickoff heads, and the encoder electronics. Primary and secondary coils are wound on each of the two legs of each pickoff head. The primary coil is excited with 25.6 kilocycles. The secondary coils are connected in opposition. When the movable armature (pickoff gear) is symmetrically located between each of the two legs, the mutual inductance between the two legs is the same. Since the secondaries are wound in opposition, no output voltage results. This position of the gear is referred to as the null position. If the armature is displaced from the null position, a greater voltage is induced in one of the coils. Motion of the gear tooth in the opposite direction similarly produces a greater output voltage in the other coil. The output voltage varies sinusoidally with the displacement of the gear teeth. Thus, this device modulates the excitation at a frequency proportional to the velocity of the armature. The second pickoff head is located so that its output voltage will be displaced from the first output voltage by 90 degrees. The relative phasing between the two outputs indicates the direction of shaft movement.

The first portion of the digital encoder electronics is a preamplifier which is followed by a synchronous demodulator. The output of the demodulator is converted into square waves by the Schmitt trigger. The square wave outputs are then fed into a logic network which identifies the direction of rotation and produces voltage spikes on one output line ( $+\Delta\Phi$ ) for clockwise rotation of shaft and on the other line ( $-\Delta\Phi$ ) for counterclockwise rotation. These spikes are then converted to the proper logic level for the AGC by pulse shaping networks. Each pulse presented to the AGC represents a finite number of arc-seconds of shaft travel. The number depends on the subsystem in which the CDU is being used. The logic of the encoder electronics provides two distinct encoder modes of operation; either one pulse per gear tooth or two pulses per gear tooth. Again, the modes of operation depend on subsystem mechanization.

While the digital encoder is providing the AGC with information about the position of the CDU, the AGC must also be provided with a means of controlling the movement of the CDU. This is accomplished by the DAC. The DAC receives commands from the AGC and converts these commands to an electrical output usable in the MDA. The inputs from the AGC are pulses of approximately 3 microseconds duration with a repetition rate of 3,200 pps. These pulses are not applied continuously but are supplied in bursts from the AGC. The feedback signal from the encoder also consists of pulses, but the repetition rate varies according to the speed of encoder pickoff gear rotation. The AGC inputs cause a capacitor in the DAC to be charged. The charge on this capacitor is reflected into the DAC output stage by two integrated choppers operating at 800 cps. The output of the DAC is an 800 cps square wave with a maximum amplitude of approximately 10 volts peak-to-peak. This output is utilized by the motor drive amplifier to position the CDU. The negative feedback from the encoder is required to insure that only a defined amount of CDU movement will occur per pulse from the AGC. The encoder input discharges the capacitor that has previously been charged by the AGC input thereby shutting off the DAC.

#### 4-7 OPTICAL UNIT ASSEMBLY

The optical unit assembly (OUA) consists of two electro-optical instruments, a sextant (SXT), and a scanning telescope (SCT), mounted on a common base. The SXT head assembly also houses the horizon sensor and star tracker.

4-7.1 SCANNING TELESCOPE. The structure of the SCT is shown in figure 4-26. The head assembly is rotated about the shaft axis by the shaft drive servo in response to shaft position or rate commands. The trunnion servo drive rotates only the double dove prism in response to trunnion position or drive rate commands.

The SCT optical base section houses most of the electro-mechanical components of the shaft and trunnion servos (including motor-generators, gear trains, resolvers, and mechanical counters) and the housing and lamp assembly. The SCT panel assembly is fastened to the optical base section and contains windows for viewing the shaft and trunnion mechanical counters, input adapters for providing manual control of the gear trains (using the universal tool as a handcrank), the eyepiece prism housing assembly, and the eyepiece assembly. The shaft axis section contains the outer and inner telescope tube assemblies. The outer tube assembly contains the objective lens system and reticle assembly. The inner tube assembly contains the pechan prism and half of the relay lens system. The trunnion axis section contains the double dove prism and mount assembly, mount support, cam-follower and spring assembly, and trunnion worm shaft.

Detailed theory of operation for the SCT is divided into four general areas of discussion: optical complex, shaft servo loop, trunnion servo loop, and drive assemblies.

4-7.1.1 SCT Optical Complex. The SCT optical complex (see figure 4-27) consists of a double dove prism and mount assembly, a one power telescope, and an eyepiece assembly.

4-7.1.1.1 Double Dove Prism and Mount Assembly. The double dove prism and mount assembly (see figure 4-28) contains two dove prisms. The prisms are matched optically, cemented together at the hypotenuse, and accurately positioned and clamped to a mount. The double dove prism is the first optical element in the SCT optics to pick up the target image. The double dove prism inverts and transmits the image to the objective lens assembly.

The rotational drive of the double dove prism and its mount is achieved through the use of a worm gear and worm shaft. The worm shaft is driven by a motor generator in the SCT trunnion drive gearbox. An angle counter for displaying the trunnion angle through the telescope panel is mounted in the trunnion drive gearbox. The angle counter is set for a zero reading when a resolver, a component of the trunnion drive gearbox, is at the null setting.

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Positional accuracy is made possible using an anti-backlash device. This device consists of a cam on the double dove prism worm shaft, a cam follower, and a spring assembly. The cam follower is held against the cam by the spring, thereby minimizing the backlash of the worm drive. Preloaded bearings in the double dove prism mount and in the worm drive also assist in precise operation of the trunnion drive.

4-7.1.1.2 One Power Telescope. The SCT one power telescope consists of an objective lens assembly, reticle assembly, pechan prism, relay lens assembly, eyepiece prism assembly, and an eyepiece assembly.

The objective lens assembly consists of three cemented doublets fitted into the upper end of the outer telescope tube. This objective cluster transmits light which passes through the double dove prism and produces an image at the reticle plane. Each lens assembly is made up of a positive and negative lens bonded by cement. A 60 degree field of view is obtained with an aperture of approximately 5 millimeters.

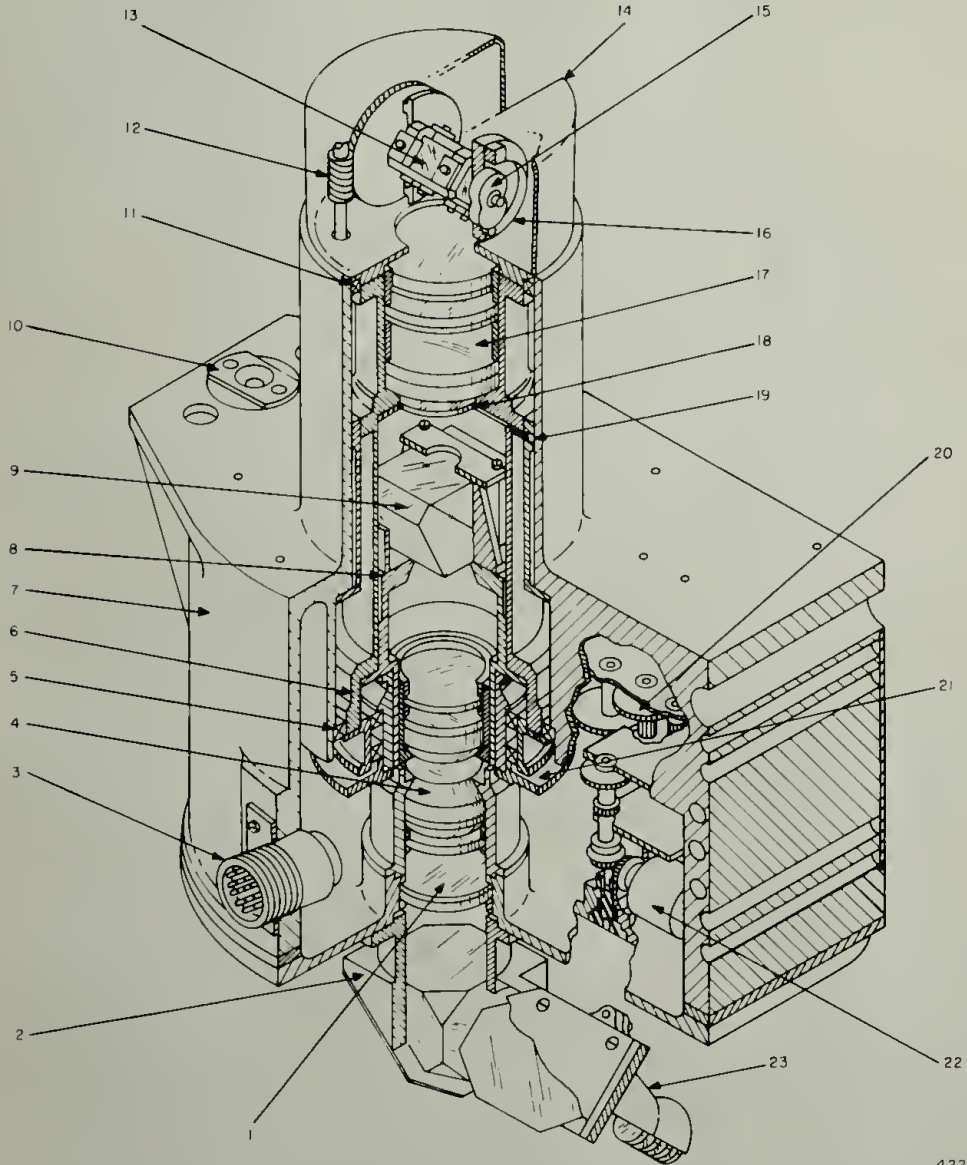
The reticle assembly is located in the outer telescope tube assembly (the second assembly in the optical path) and is adjacent to the objective lens assembly. The inverted image transmitted by the objective lens assembly is focused onto the reticle assembly. The reticle is accurately positioned in the focal plane of the objective lens assembly. The reticle crosshair intersection is the reference target for the image transmitted from the double dove prism and objective lens assembly.

The reticle is illuminated from the edge by four incandescent lamps located in the housing and lamp assembly. This assembly is secured to the optical base and envelops the outer telescope tube assembly. Three light-transmitting rods, assembled 120 degrees apart in the reticle plane, direct the light from the incandescent lamps to the reticle. The rods are fastened to the outer telescope tube and provide uniform illumination at any shaft angle position.

The pechan prism (figure 4-29) (located in the inner telescope tube assembly at the end facing the reticle assembly) erects the inverted image. The prism is in the optical path between the reticle and the first relay lens assembly.

The pechan prism consists of two sections separated by an air space. This design achieves the erecting of the image and increases the axial length of the optical path and decreases the physical length of the SCT.

The relay lens assembly consists of two groups of lenses. One is a housing and lens assembly fastened to the end of the inner telescope tube assembly opposite that holding the pechan prism. The second is a telescope relay lens assembly secured to the inside face of the telescope panel assembly. The relay lens assembly transfers the erected image from the pechan prism to the eyepiece window at unity magnification.



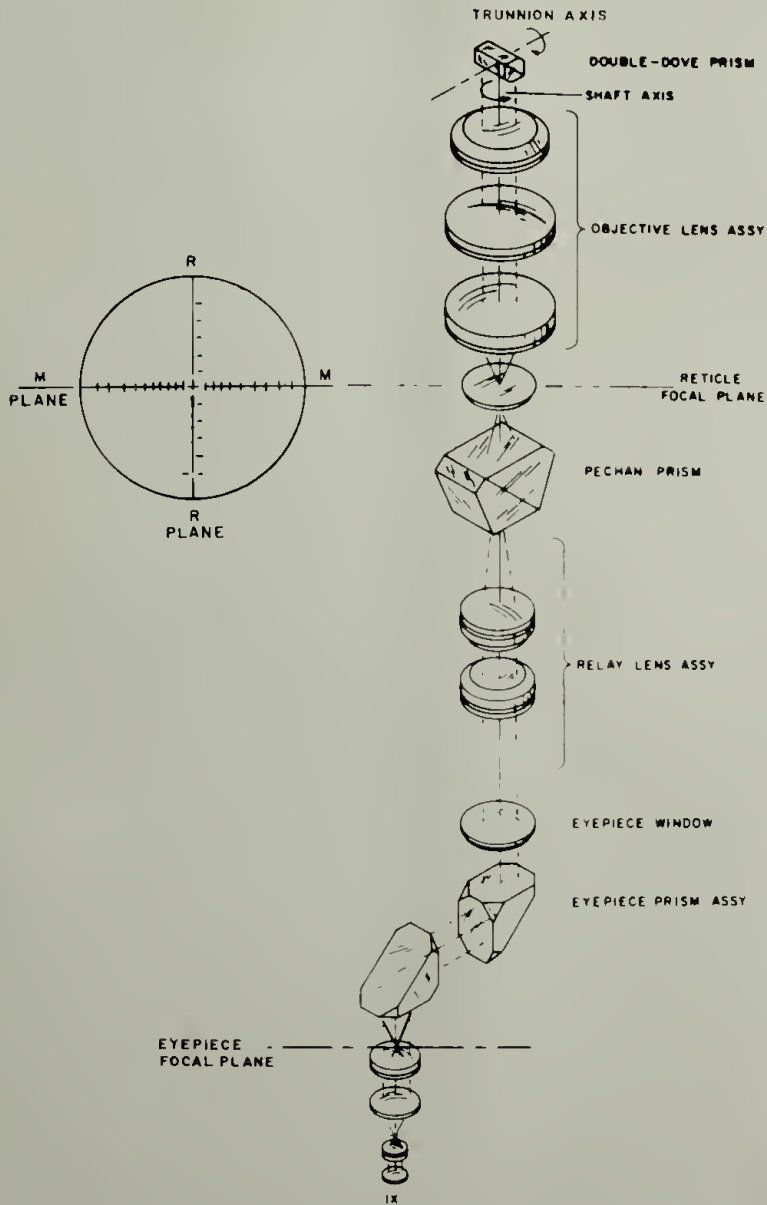
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Figure 4-26. SCT (Sheet 1 of 2)



1. Eyepiece window
2. Eyepiece prism housing assembly
3. Electrical connector
4. Relay lens assembly
5. Ball bearing (outer telescope tube assembly)
6. Outer telescope tube assembly
7. Optical base
8. Inner telescope tube assembly
9. Pechan prism
10. Ball mount (3)
11. Ball bearing (outer telescope tube assembly)
12. Trunnion drive worm shaft
13. Dove prism and mount assembly
14. SCT head cover
15. Anti-backlash cam
16. Anti-backlash spring and cam follower
17. Objective lens assembly
18. Reticule assembly
19. Housing and lamp assembly
20. Shaft drive gear box
21. Cluster gear assembly
22. Shaft angle counter
23. Eyepiece assembly

Figure 4-26. SCT (Sheet 2 of 2)



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Figure 4-27. SCT Optics

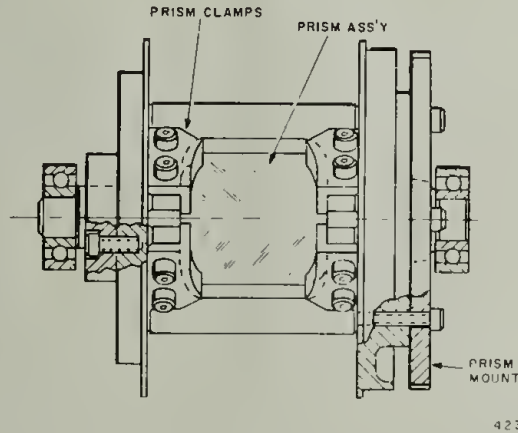


Figure 4-28. Double Dove Prism

The eyepiece window is assembled to the SCT panel assembly. The panel assembly acts as a seal between the SCT eyepiece prism housing assembly and SCT components exposed to environmental conditions outside the command module. The eyepiece window has no optical effect and transmits the image directly from the relay lens assembly to the SCT eyepiece prism housing assembly.

The SCT eyepiece prism housing assembly is fastened to the telescope panel assembly. Its two prisms transfer the image from the relay lens assembly to the lens system of the eyepiece assembly.

4-7.1.1.3 SCT Eyepiece Assembly. The SCT eyepiece assembly is secured to the SCT eyepiece prism housing assembly. It receives the image from the SCT eyepiece prism housing assembly prisms and transfers it, without magnification, to the eye of the observer. The eyepiece assembly consists of three lens assemblies (telescope objective lenses) secured into the SCT eyepiece housing.

The SCT eyeguard assembly is fastened to the end of the SCT eyepiece housing. It is made of non-toxic, synthetic rubber and is adjustable in an axial direction. The adjustment allows for differences in facial contours of the astronauts.

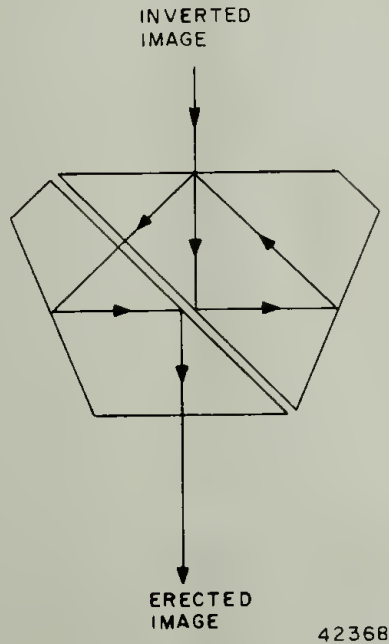


Figure 4-29. Pechan Prism

The SCT long relief eyepiece assembly is provided as optional equipment as a replacement for the SCT eyepiece assembly. It contains a lens assembly and a positive lens mounted into an SCT eyepiece housing. Unlike the contoured eyeguard assembly of the SCT eyepiece assembly, a rubber guard is cemented flat against the end of the SCT eyepiece housing.

4-7.1.2 SCT Optics Light Transmission. The optical efficiency of the SCT allows approximately 40 percent of the light impinging on the double dove prism to be transmitted to the eyepiece. Light losses in the SCT are held to a minimum by the use of multiple anti-reflection coatings which increase the efficiency of all transmitting surfaces.

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4-7.1.3 SCT Shaft Servo Loop. A single speed, positioning servo loop (see figure 4-30) is used to rotate the SCT optics about the shaft axis. The 1X resolver B2 generates an error signal proportional to the mechanical shaft displacement from the electrical reference input. The reference input is the sine-cosine output pair from 1X resolver transmitter B5 in the SXT shaft master servo. The error signal input is applied to pin 9 of the MDA summing network. In this application, only one error input is applied to the summing network. (The remaining inputs are routed to common ground.) The feedback input to pin 7 is fed from pin 2 of the feedback compensation network when the MDA is used in a position servo. In position servo configuration, the feedback input to pin 7 is fed directly into a feedback compensation network. The amplifier circuit then generates the motor drive signals in the phase and magnitude required to drive resolver control transformer B2 to null. When nulled, the SCT servo mechanically aligns the rotor with the electrical input. The SCT shaft angle is thus slaved to the SXT shaft angle.

4-7.1.4 SCT Trunnion Servo Loop. Articulation of the double dove prism and mount assembly about the trunnion axis is controlled by the SCT trunnion servo loop (see figure 4-31). This servo may function either as a single speed, positioning servo or as an integrating (or rate) servo. The servo functions as a positioning servo in all modes except tracker mode. When functioning as a positioning servo, the SCT trunnion MDA input and tachometer feedback relay K2 is deenergized. The source of the MDA input error is 1X resolver B1 driven by the SCT trunnion gear train. This resolver functions in exactly the same way as 1X resolver B2 driven by the SCT trunnion gear train. The error signal (high) input is applied to input pin 5 of the MDA summing network via pins 23 and 7 of relay K2. The feedback compensation output from pin 2 is applied to pin 7 of the MDA summing network via relay contacts 6 and 9. Thus, when input relay K2 is deenergized, the servo configuration is identical to the single speed SCT shaft positioning servo.

When the OSS is set up for tracker mode, the SCT trunnion servo assumes the configuration of an integrating or rate servo. In tracker mode, input relay K2 is energized. This removes from the MDA summing network both resolver B1 error and the feedback compensation inputs. At the same time, the command signal from the trunnion output of the SXT hand controller is switched as an input to pin 5 of the MDA summing network via relay contacts 10 and 7. The input to pin 7 of the MDA summing network is fed from the tachometer rate feedback via relay contacts 20 and 9. These two inputs at pins 5 and 7 set up the SCT trunnion servo as an integrating loop whereby the hand controller input drive rate  $A_t$  is integrated and causes the gear train to rotate at the corresponding angular velocity.

When the OSS is set up in any mode except tracker mode, the source of the input signal is the output of single speed resolver control transformer B1 or  $0^\circ$  and  $25^\circ$  offset reference voltage. The electrical reference input originates from one of three sources through the operation of three relays in the SCT switching module. The relay configurations depend on the setting of the three position SLAVE TELESCOPE switch.

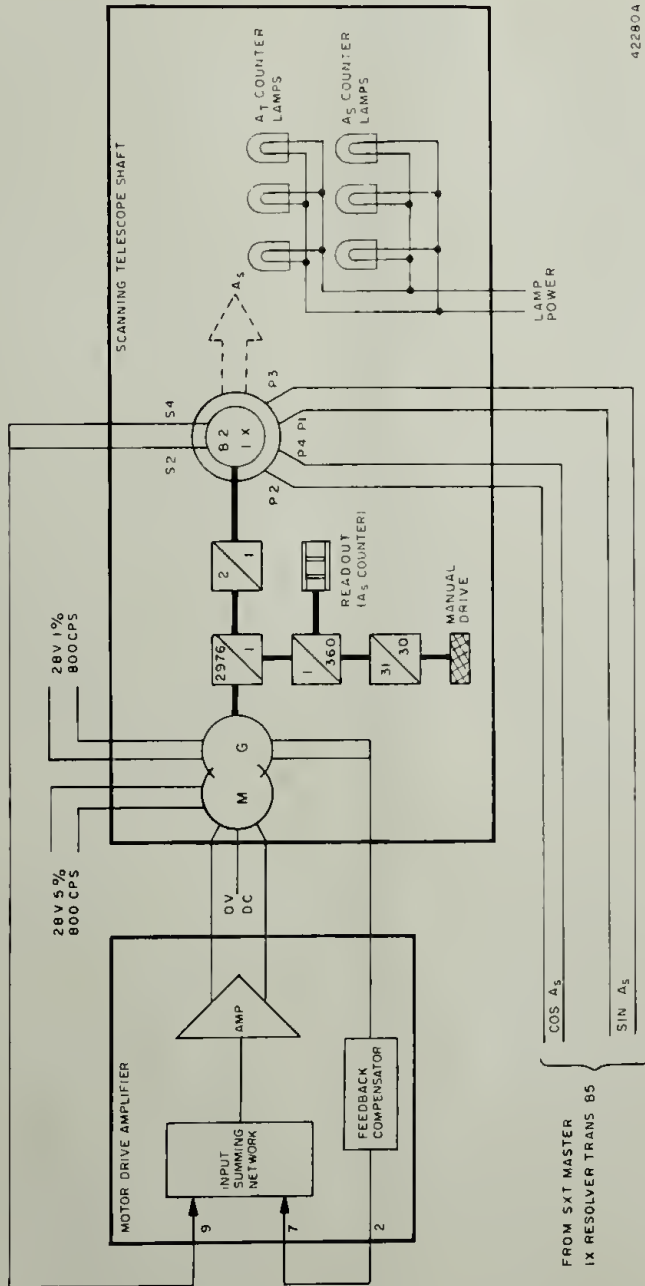
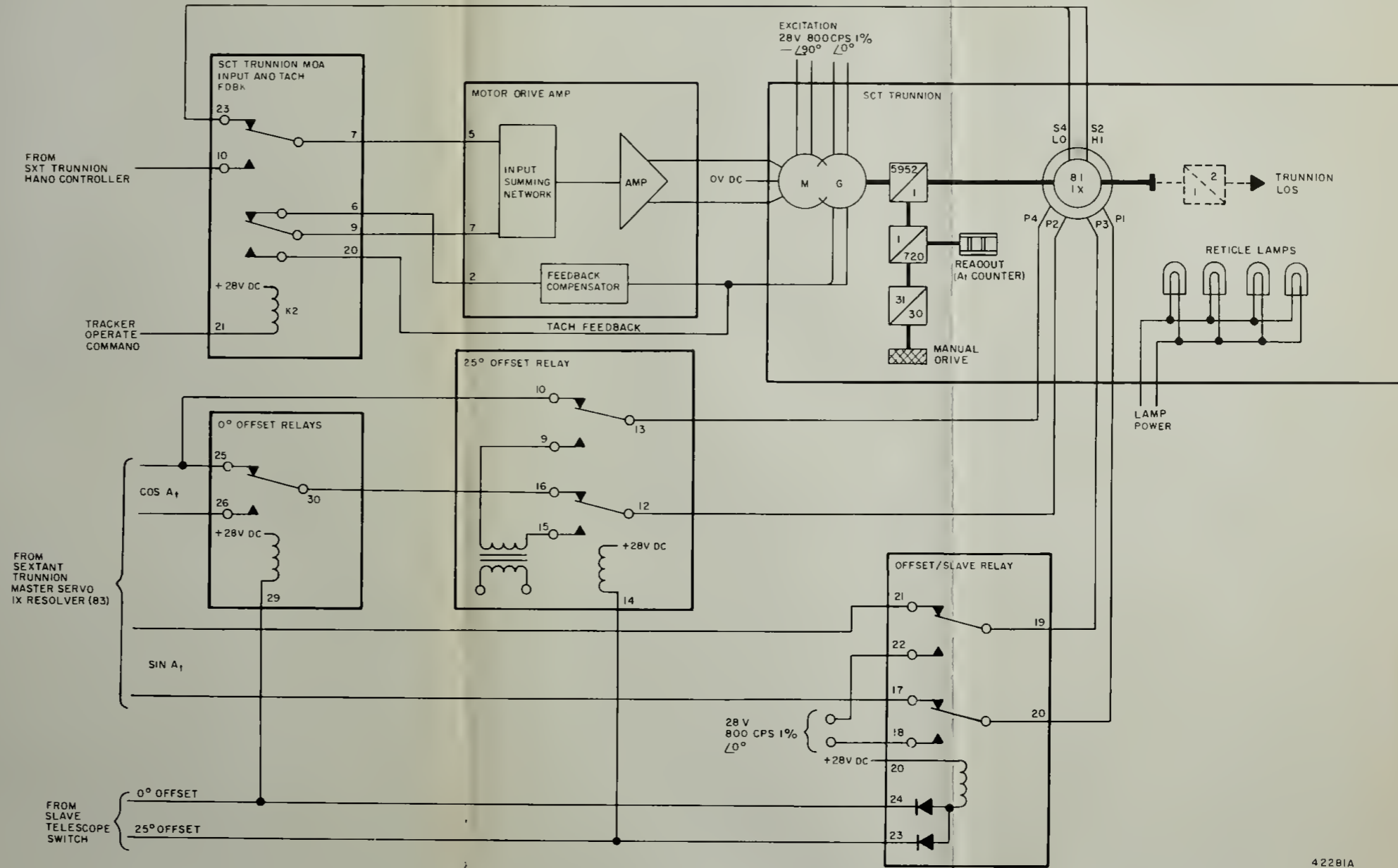


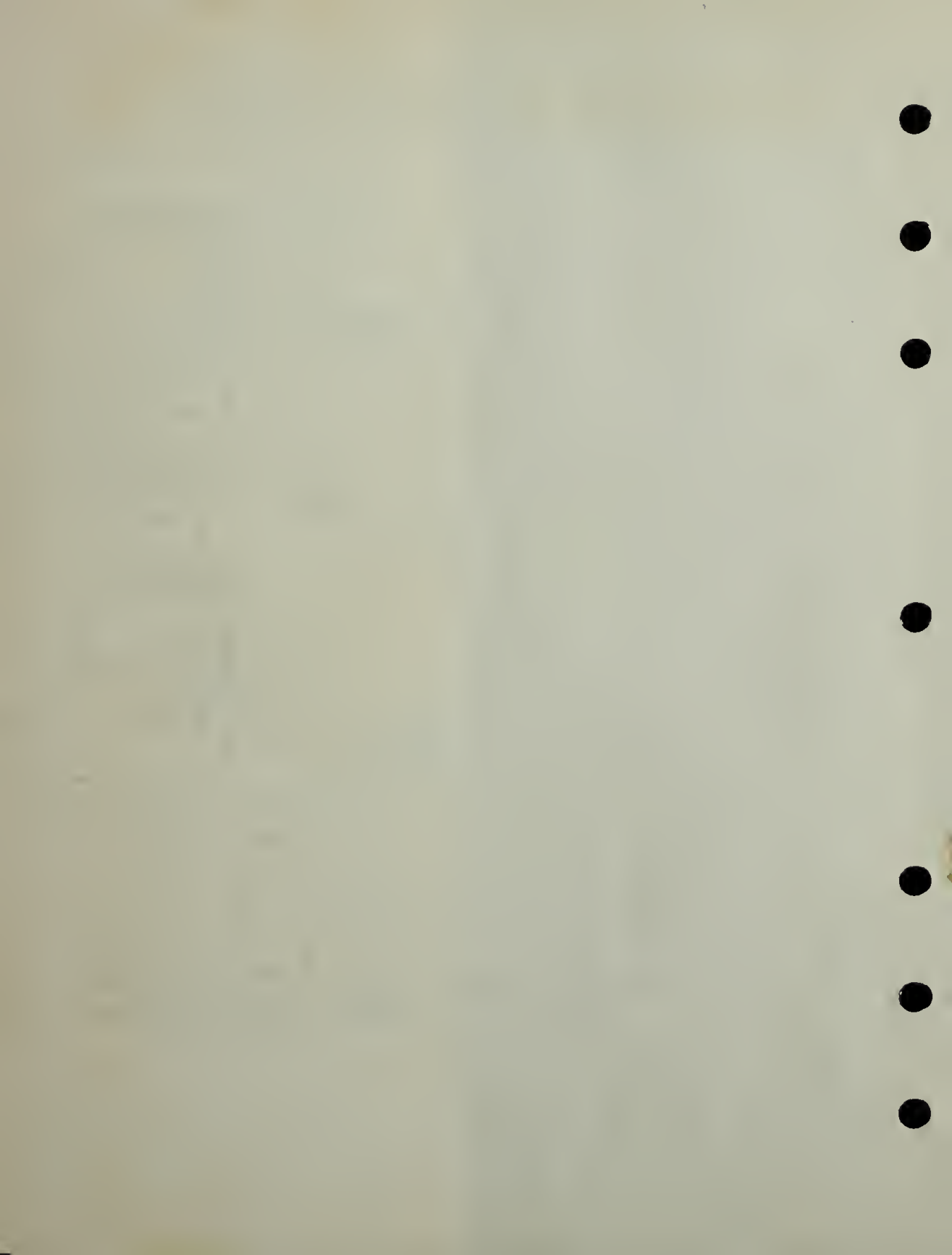
Figure 4-30. SCT Shaft Servo Loop, Block Diagram

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Figure 4-31. SCT Trunnion Servo Loop, Block Diagram





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When the SLAVE TELESCOPE switch is in STAR LOS position, all relays are deenergized. This applies the sine-cosine output windings from 1X SCT trunnion servo resolver transmitter B3 to the primary (stator) of SCT trunnion controller transformer B1 forming a precision data transmission system from the SXT to the SCT. The SCT trunnion positioning loop is slaved to the SXT master.

When the SLAVE TELESCOPE switch is placed in 0° OFFSET position, the 0 degree offset relay and the offset/slave relay are energized. This disconnects the SXT resolver transmitter inputs, applies a fixed 28 volt, 800 cps, zero phase reference signal to the sine winding (P1-P3) of resolver B1 and shorts out the cosine winding (P2-P4). This establishes a zero electrical reference with which the positioning servo aligns.

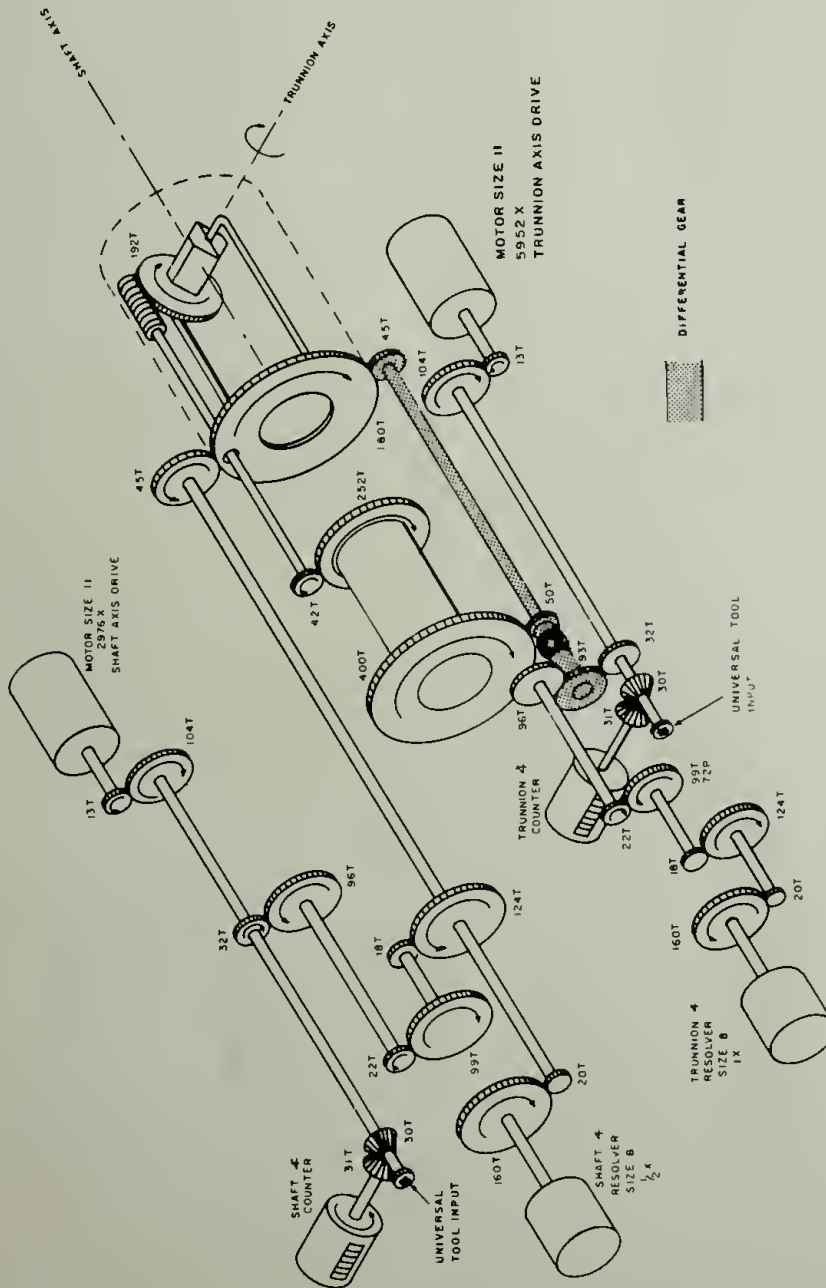
When the SLAVE TELESCOPE switch is placed in 25° OFFSET position, the 25 degree offset relay and the offset/slave relay are energized. This substitutes a fixed reference voltage from the secondary of a transformer to the cosine winding of transformer B1 (P2-P4) and causes the electrical reference to rotate precisely 25 degrees. The servo loop aligns itself with this reference and causes the SCT optics to move to a fixed 25 degree trunnion angle offset.

**4-7.1.5 SCT Drive Assemblies.** The single speed SCT obtains rotational drive about shaft and trunnion axes through two motor generators, one for each axis. Reduction gearing, motor generators, resolvers, and angle counters for shaft and trunnion axes are assembled in two separate gearboxes located in the optical base. The following paragraphs contain details of SCT gearbox components and their operation.

**4-7.1.5.1 Gear Reduction Ratios.** Figure 4-32 contains an operational diagram of the SCT reduction gearing. In trunnion axis, the gear reduction ratio between motor generator shaft and double dove prism is 5952:1. Worm mesh lead accuracy is maintained within 30 arc seconds. In shaft axis, the gear reduction ratio between motor generator shaft and double dove prism is 2976:1.

**4-7.1.5.2 SCT Differential.** SCT shaft and trunnion axis drives are linked by a differential gear assembly. The differential gear assembly permits trunnion axis positioning independent of shaft axis, and shaft axis rotation without introducing errors in the trunnion axis. The differential gear layout is shown in detail in figure 4-33. The shaft drive gear is pinned to the differential shaft. The trunnion gears are mounted on ball bearings and rotate freely about the differential shaft. The trunnion drive and positioning gears are connected by a planetary gearing system which is pinned to the differential shaft. This allows rotation of the shaft drive gear without introduction of errors into trunnion positioning, and trunnion drive gear rotation without affecting the shaft drive gear.

**4-7.1.5.3 SCT Angle Counter.** Two identical counters (see figure 4-34) displaying SCT shaft and trunnion axis angles are located in the optical base. The counters are viewed through lighted bezel windows in the SCT panel. Each counter contains three drums interconnected through geneva gearing. A flip-up counter shade is geared to the drums to permit continuous numerical display. The counter is calibrated to display readouts from 0 to 359.98 degrees with graduations in 0.02 degree increments. Counter rotation is continuous in either direction. One revolution of the counter input shaft results in a one degree change in counter indication.



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Figure 4-32. SCT Gearing Diagram

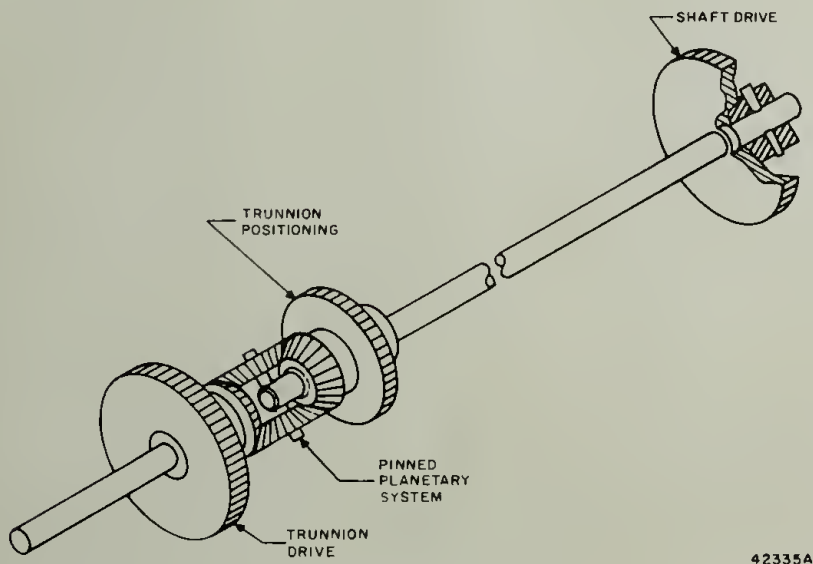


Figure 4-33. SCT Differential Gear Assembly

4-7.2 SEXTANT. The SXT structure is shown in figure 4-35. The complete index head assembly is rotated by the shaft servo in response to shaft position or shaft rate commands. The trunnion servo rotates the indexing mirror and mount assembly about the trunnion axis in response to trunnion positioning or drive rate commands. The shaft and trunnion drive mechanisms affect the star line of sight (S<sub>t</sub>LOS) only, while the landmark line of sight (LLOS) is fixed along the shaft axis. The horizon sensor optics are rigidly mounted and use a line of sight, parallel to the LLOS, called the horizon line of sight (HLOS). The star tracker optics are also fixed, but use the tracker line of sight (TLOS) which is introduced by an extension of the SXT indexing mirror. For purposes of description, the SXT is divided into the index head assembly and the base section.

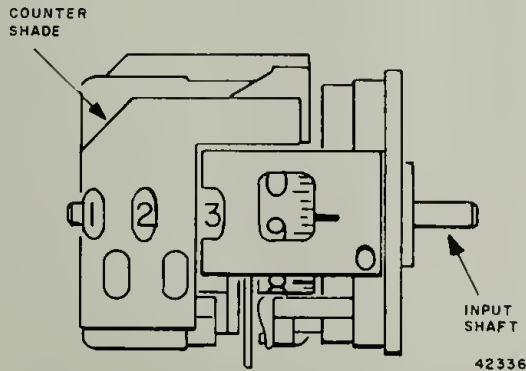


Figure 4-34. SCT Angle Counter

The SXT index head assembly contains the indexing mirror and mount assembly, SXT right angle mirrors, beam splitter, trunnion drive electromechanical components, and horizon sensor and star tracker optics with head electronics and power supplies.

The SXT base section houses the shaft axis assembly, shaft drive electromechanical components (for example, motor-generator, shaft drive gearbox, and resolver rotors), and SXT eyepiece. Rotating components, mounted on the shaft axis assembly, include the SXT telescope tube assembly (with objective and intermediate lens), the SXT reticle assembly, and the shaft resolver rotors. The SXT panel assembly covers the underside (face) of the optical base. This assembly contains the eyepiece window and has provision for mounting the SXT eyepiece assembly. The detailed theory of operation for the SXT is divided into four general areas of discussion: optical complex, shaft servo loop, trunnion servo loop, and eyepiece assembly.

4-7.2.1 SXT Optical Complex. The SXT optical complex (see figure 4-36) consists of SXT indexing mirror and mount assembly, right angle mirrors, beam splitter, SXT telescope lenses, and eyepiece assembly.

4-7.2.1.1 SXT Indexing Mirror Mount Assembly. The SXT indexing mirror is constructed of heat-treated beryllium and its reflecting surface is overcoated with silicon monoxide. The underside of the mirror is undercut in several places for weight reduction and balance. The indexing mirror is mounted in the mirror mount assembly of the sextant head. The assembly rotates on precision ball bearings in the trunnion axis and is provided with counterweights to maintain balance in any position. A side tab, or extension, at the upper half of the indexing mirror picks off light and directs it to the star tracker optics.

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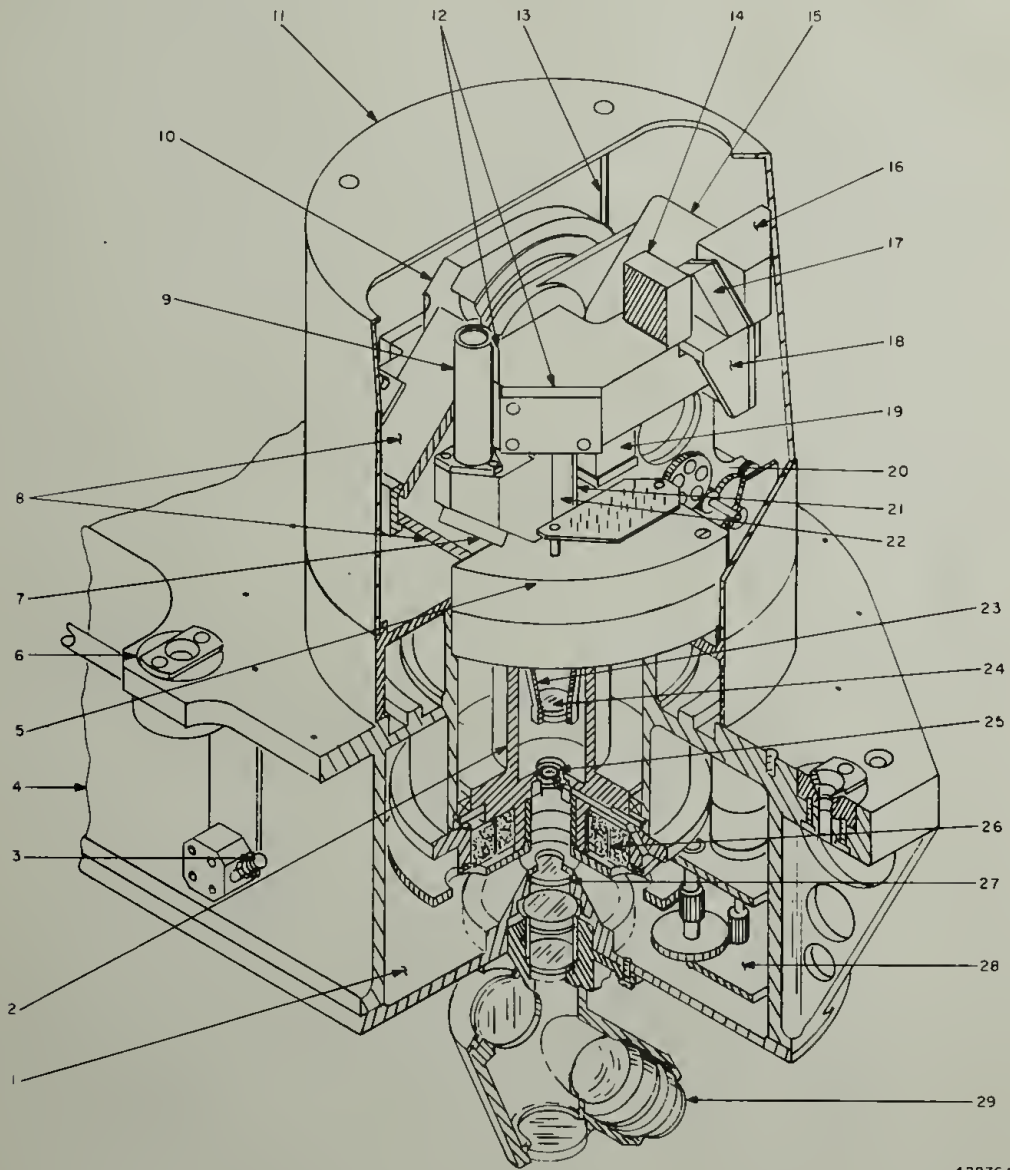
4-7.2.1.2 SXT Head Right Angle Mirrors. Two mirrors are fixed at right angles to each other and reflect the star image onto the reflecting surface on the underside of the beam splitter. Both mirrors are made of heat-treated, nickel coated beryllium. The reflecting surfaces are aluminized and overcoated with silicon monoxide.

4-7.2.1.3 Beam Splitter. The SXT optics provide two distinct lines of sight and different degrees of light transmission for two simultaneously viewed images. These capabilities are derived by incorporation of the beam splitter. The dual line of sight capability is established by beam splitter construction: one image is transmitted directly by total internal reflection of one surface; the second image transmitted is displaced slightly due to refraction.

The beam splitter is manufactured from grade B optical glass which is fine-annealed. (See figure 4-37.) The annealing process prevents formation of internal stresses within the glass during the cooling process. This is accomplished by preventing the outer surface from solidifying while the inner portion is still hot. The beam splitter dimensions are approximately 2.9 x 2.2 x 0.47 inches. The top and bottom surfaces are polished flat within 1/4 wave length at 5461 angstroms. These two surfaces are parallel to within 30 seconds of arc and display a resolving power of 3 seconds of arc or better at 45 degree incidents for transmission and reflection.

The S<sub>t</sub>LOS is much brighter than the LLOS when viewed through the eyepiece. To make these images easily discernible, their intensities are transmitted at different levels. The beam splitter provides the required variations in transmission due to its surface reflectivity characteristics. Both surfaces are coated with a high efficiency reflection-transmission reducing film resulting in 75 percent reflection and 25 percent transmission. (See figure 4-38.) When light is introduced into the SXT optics at a 45 degree angle to the optical-mechanical axis, these multiple film layers cause a beam splitting effect. Composite light losses in the SXT are such that approximately 4 percent of impinging light is transmitted for the fixed path LLOS versus 25 percent for the S<sub>t</sub>LOS.

4-7.2.1.4 SXT Telescope Optical Complex. The SXT telescope optical complex, mounted in the SXT shaft axis assembly, consists of the objective lens, the intermediate lens, and reticle assemblies. A triplet and a single lens form part of the telescope objective lens assembly at the upper end of the lens holder which tapers due to the smaller diameter of the intermediate lenses. A set of these intermediate lenses is mounted at the lower end of the lens holder assembly. The objective and intermediate lens assemblies form a telephoto type lens system. The reticle is positioned in the focal plane of the objective lens. The edge illumination of the SXT reticle is provided by four lamps which light three transmitting rods spaced evenly around the reticle. The eyepiece window serves as a seal in the SXT panel. The SXT eyepiece window is similar in function to the SCT eyepiece window.

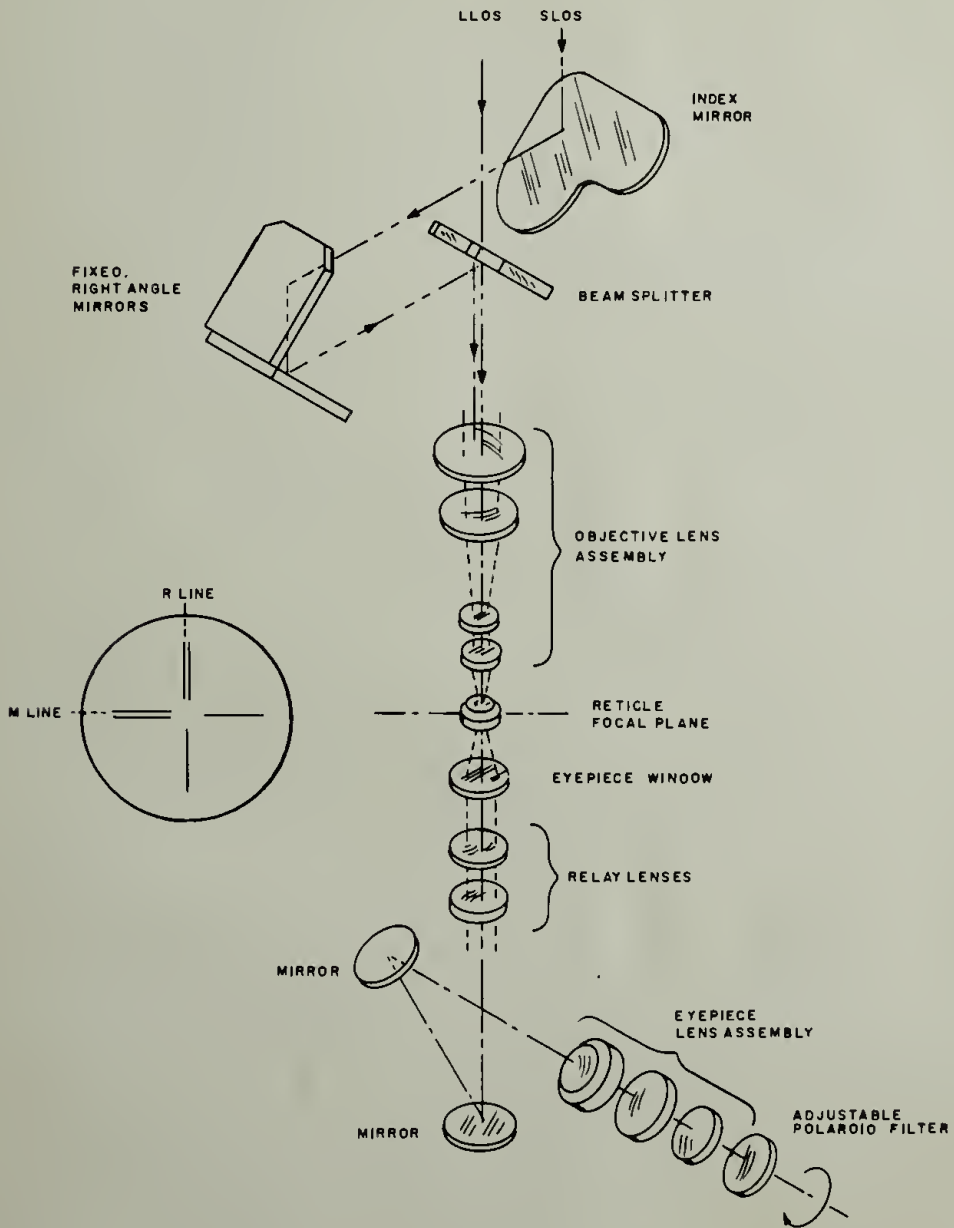


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Figure 4-35. SXT (Sheet 1 of 2)

1. SXT panel assembly
2. Shaft axis assembly
3. Coolant passages (Not used)
4. Optical base
5. Tracker and horizon sensor power supplies
6. Ball mount (3)
7. Horizon sensor mirror
8. SXT right-angle mirrors
9. Horizon sensor objective lens and filter housing
10. Trunnion resolver
11. SXT head cover
12. Star tracker right-angle mirrors
13. Threaded rod (cover support) (2)
14. Tuning fork drive amplifiers
15. Indexing mirror and mount assembly
16. Tracker head electronics
17. Tracker tuning fork resonator
18. Star tracker photomultiplier and lens housing
19. Horizon sensor head electronics
20. Trunnion drive gear box
21. Horizon sensor photomultiplier and lens housing
22. Horizon sensor tuning fork resonator
23. SXT objective lens holder assembly
24. SXT telescope intermediate lens assembly
25. Reticle assembly
26. Shaft resolvers
27. Eyepiece window
28. Shaft drive gearbox
29. SXT eyepiece assembly

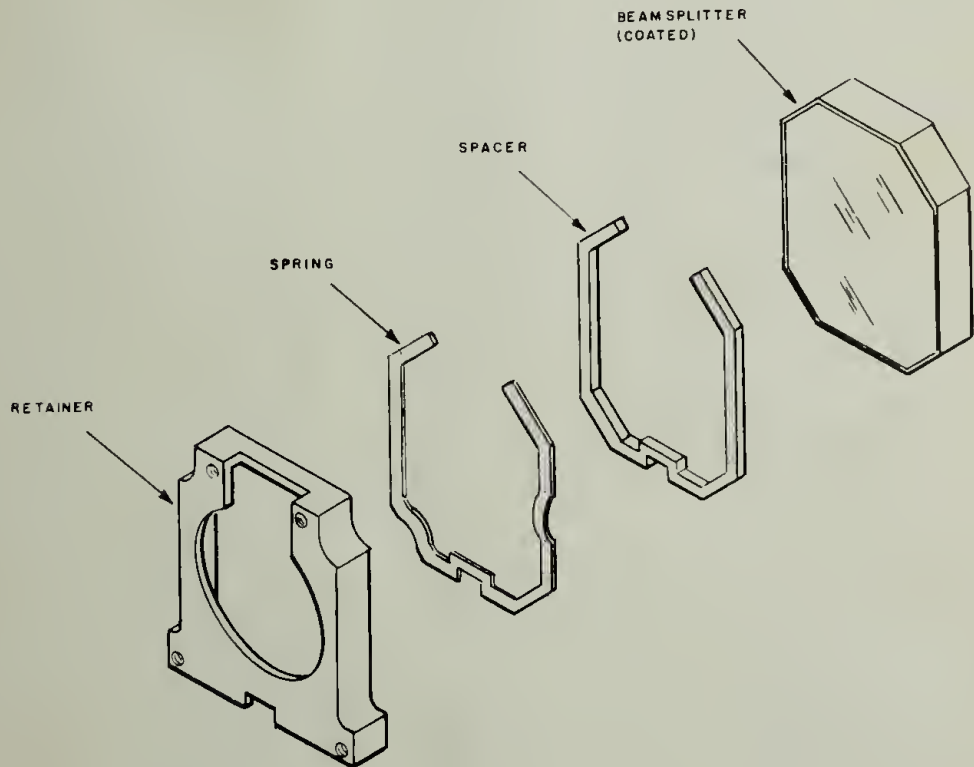
Figure 4-35. SXT (Sheet 2 of 2)



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Figure 4-36. SXT Optics

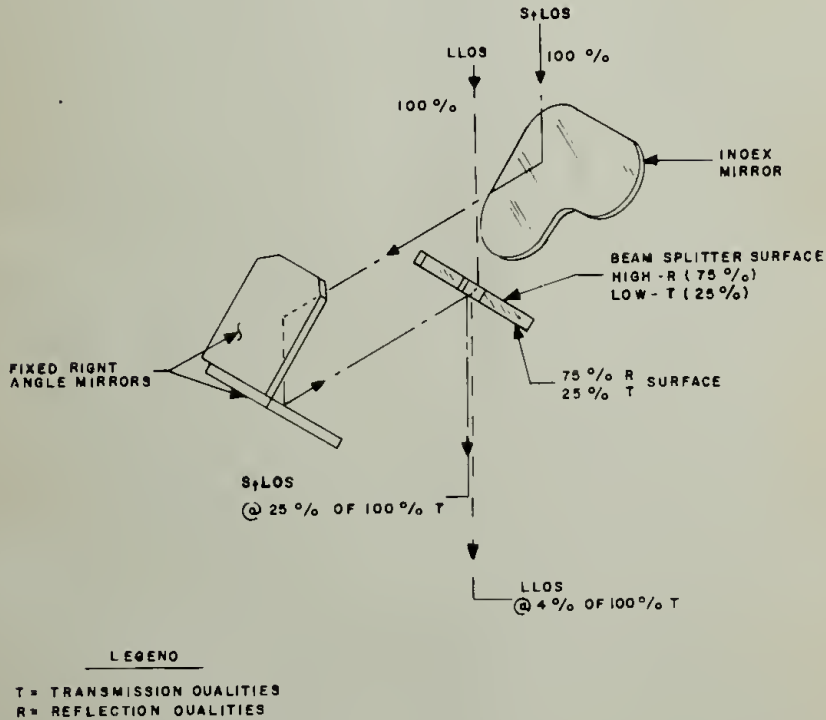




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Figure 4-37. Beam Splitter Construction

4-7.2.1.5 SXT Eyepiece Assembly. The SXT eyepiece assembly consists of the relay lens assembly, two mirrors, and the ocular eyepiece assembly. The relay assembly contains two doublets which relay the image to the primary of two mirrors. The mirrors reduce the length of the system and transfer the image into the eyepiece ocular assembly. The eyepiece ocular assembly contains two doublets, a single lens, and a polaroid filter. The adjustable filter provides landmark (LLOS) image brightness adjustment without affecting star image (StLOS).



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Figure 4-38. Beam Splitter Characteristics

In effect, the SXT eyepiece assembly represents a telemicroscope of 0.34 inch focal length and contributes to the SXT 28 power magnification by providing 3.4 power magnification from the relay assembly. Focal length of the eyepiece assembly equals one inch, which results in a total magnification of 28 power.

## APOLLO GUIDANCE AND NAVIGATION SYSTEM

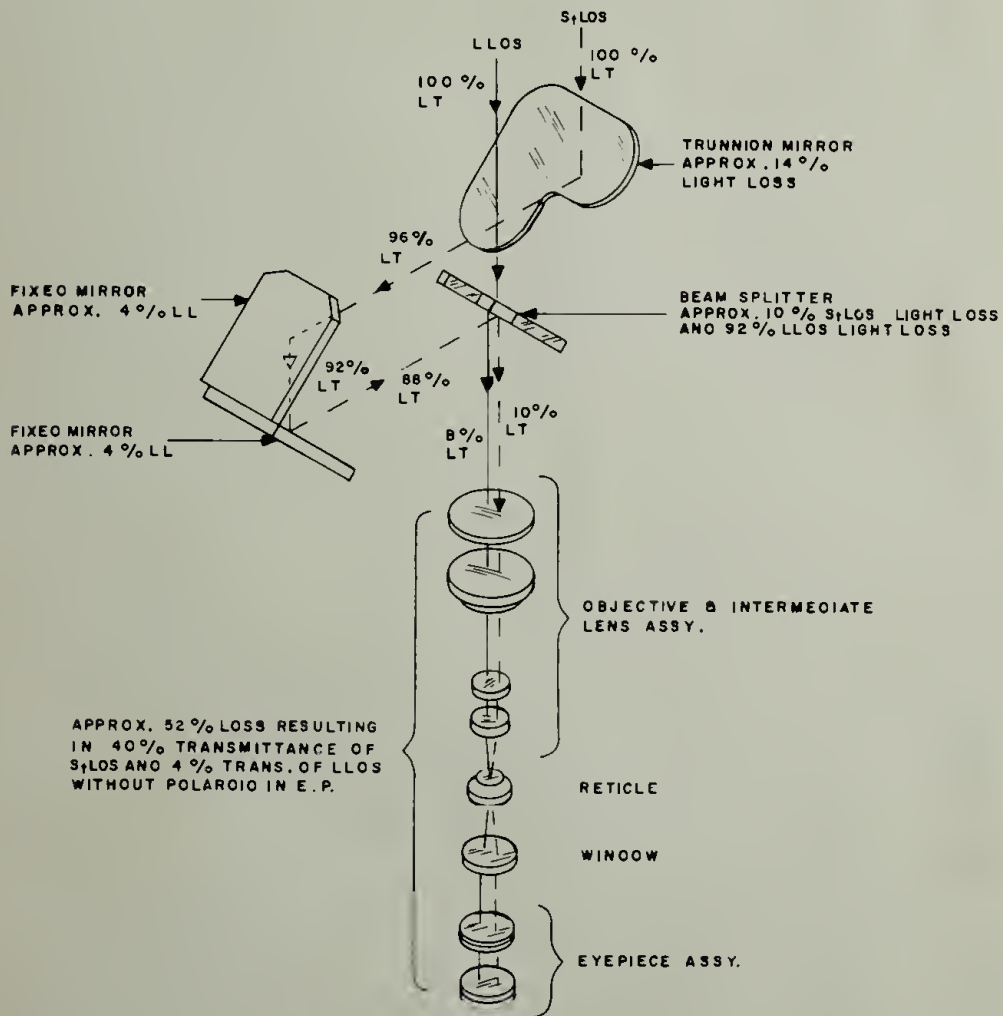
4-7.2.1.6 SXT Optics Light Transmittance. When a beam of light passes through a different medium, the intensity will decrease. This loss of intensity is mainly due to absorption. With respect to the SXT S<sub>t</sub>LOS (see figure 4-39), incident light impinging on and emerging from the trunnion mirror is reduced by a factor of approximately 4 percent. The resulting 96 percent is passed on to the first fixed mirror, which causes a further reduction of 4 percent passing on 92 percent of the light to the second fixed mirror. The second fixed mirror further reduces transmitted light by 4 percent, leaving approximately 88 percent to be reflected by the beam splitter. The beam splitter will reflect approximately 90 percent of the light principally in the shorter wavelength of the visible spectrum. Light loss in the objective lens assembly and through the eyepiece amounts to approximately 52 percent, resulting in total light transmission of approximately 40 percent for the S<sub>t</sub>LOS.

The total light losses in the LLOS (see figure 4-39) amount to approximately 96 percent, with 92 percent occurring at the beam splitter. The remaining 8 percent emerging from the beam splitter is further attenuated by a factor of 48 percent, through the objective and eyepiece assemblies, as discussed in the preceding paragraph. This results in an overall transmittance of 4 percent.

4-7.2.2 SXT Shaft Servo Loop. Rotation of the SXT index head about the shaft axis is controlled by the SXT shaft servo loop (see figure 4-40). This loop may function as either a precision two speed positioning servo loop or as an integrating servo loop. The servo is used as an integrating loop in hand controller and computer modes; in all other modes the servo loop is set as a two speed, positioning servo.

When the OPTICS MODE switch is placed in ZERO OPTICS position, the SXT shaft two speed switch input relay, the SXT shaft feedback relay, and the SXT MDA input shorting relay are energized. The two speed switch relay applies the output of secondary winding S2 of the 16X resolver (fine) and the output of secondary winding S3 of the SXT 1/2X resolver (coarse) to the two speed switch. The SXT shaft feedback relay disconnects the tachometer feedback from the MDA input summing network and switches the feedback through the compensation network as required for the positioning servo configuration.

The zero optics shorting relay places the rate input to pin 9 of the MDA at zero. Consequently, the error input to the servo is taken from the two speed switch and is proportional to the SXT shaft displacement from the zero electrical reference. The zero reference for 1/2X coarse resolver B7 is obtained from the 28 volt, 800 cps stator excitation supply. The zero reference for the 16X fine resolver B4 is more precise and is established by the 28 volt, 800 cps rotor excitation across P1-P3 and the excitation across P2-P4, adjusted by the resolver trimming module. The two speed servo loop drives the SXT gear train into accurate alignment with the zero reference.

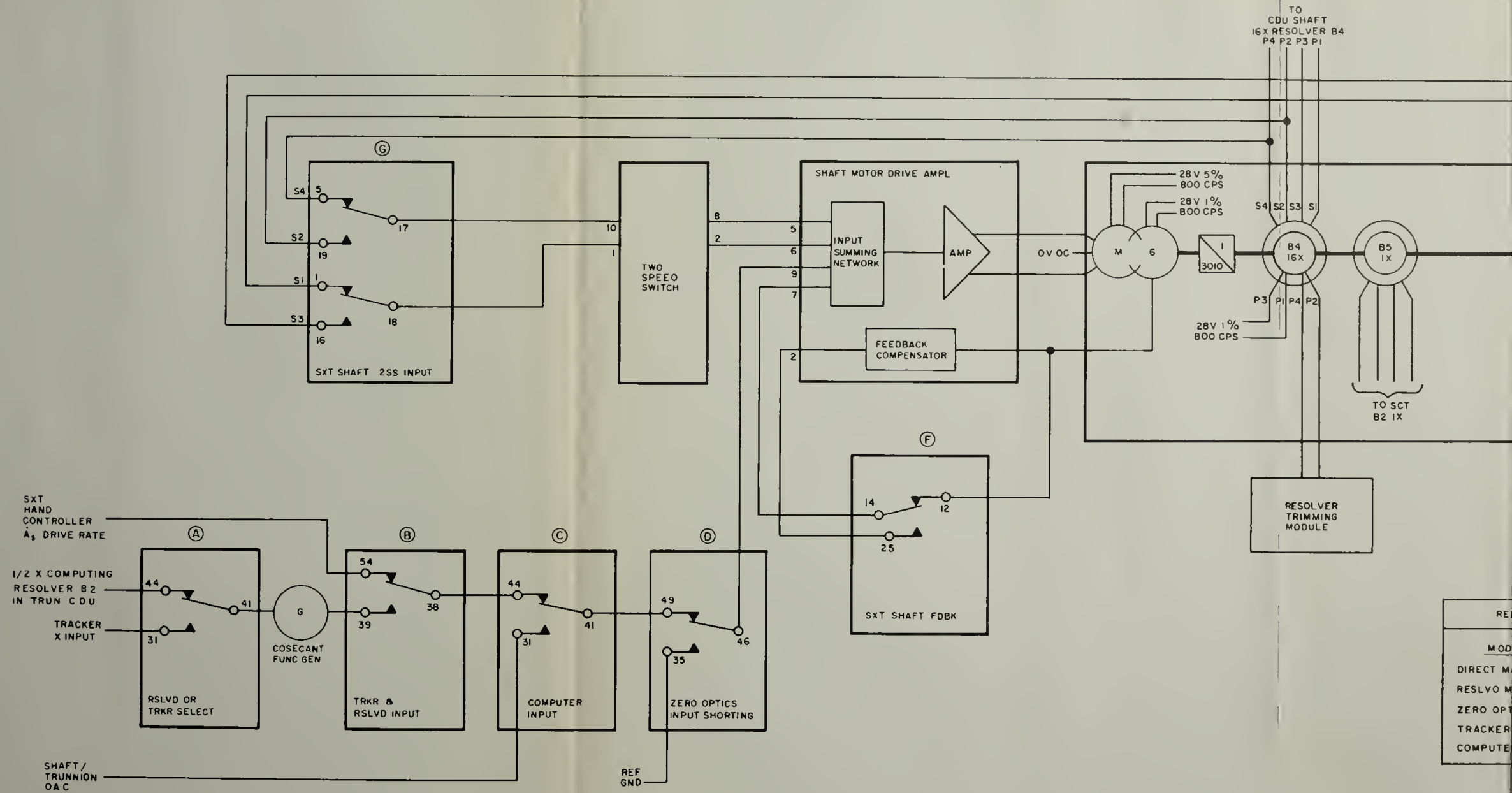


LEGEND

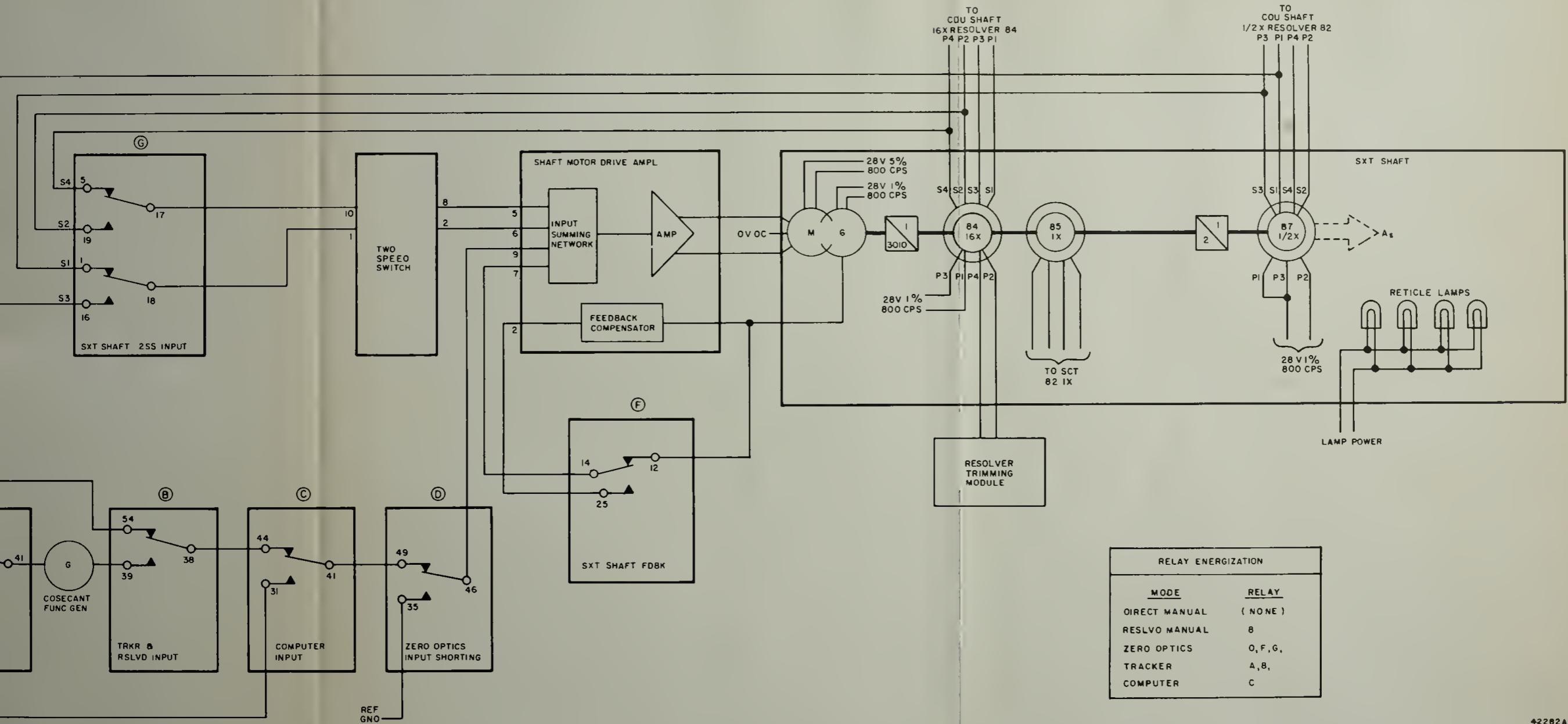
LT = LIGHT TRANSMITTANCE  
LL = LIGHT LOSS

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Figure 4-39. SXT Optics Light Transmittance



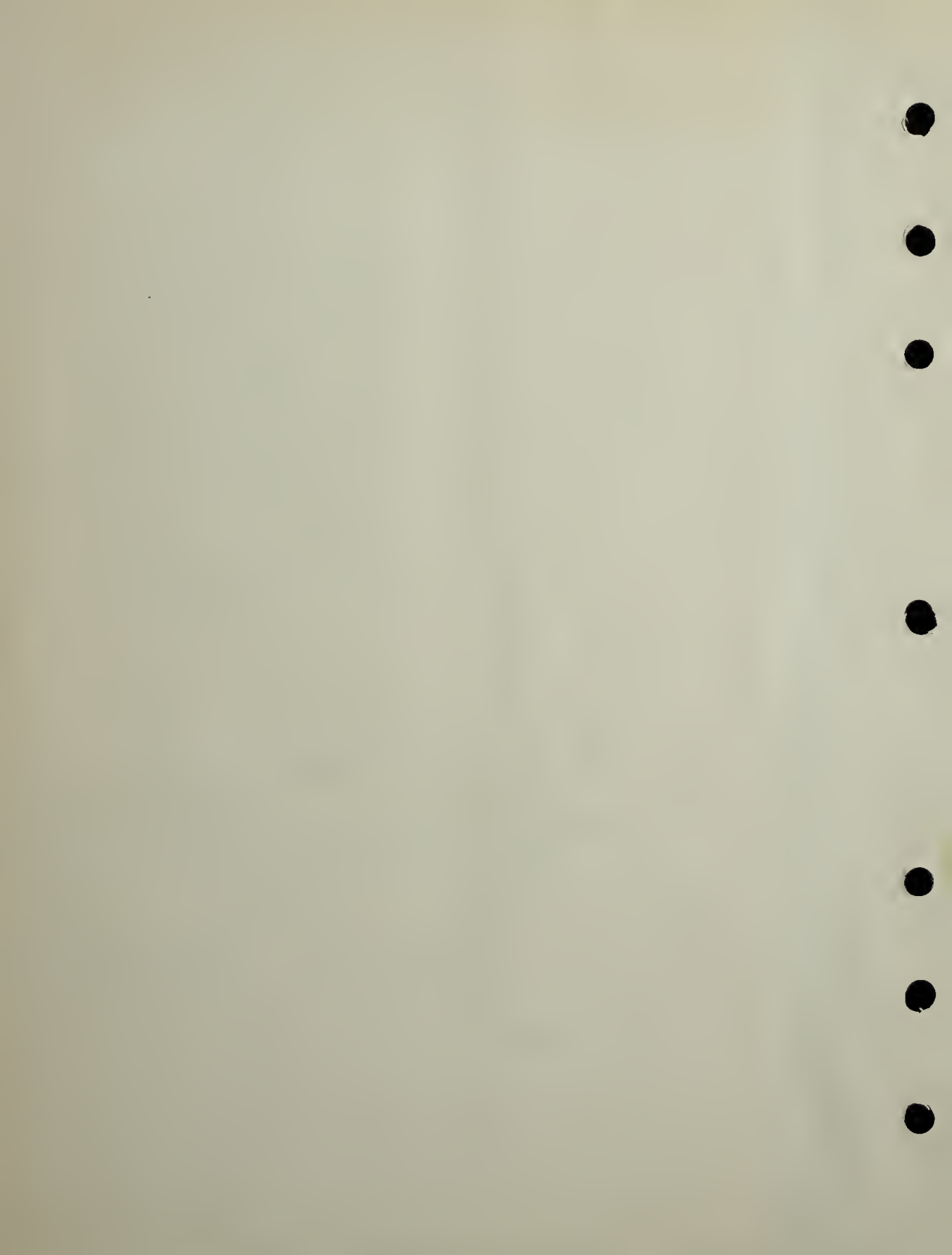
RES
MOD
DIRECT M
RESLVO M
ZERO OPT
TRACKER
COMPUTE



RELAY ENERGIZATION	
MODE	RELAY
DIRECT MANUAL	( NONE )
RESLVO MANUAL	B
ZERO OPTICS	O, F, G,
TRACKER	A, B,
COMPUTER	C

Figure 4-40. SXT Shaft Servo Loop, Block Diagram

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In system modes of operation other than zero optics, the SXT shaft two speed switch input relay, the SXT shaft feedback relay and the input shorting relay are deenergized. Deenergizing of the first two relays sets up the servo as an integrating loop. This places the two inputs to pins 5 and 6 of the MDA from the two speed switch at zero, and restores the tachometer feedback input to pin 7. Deenergizing of the third relay (the input shorting relay) removes the zero input to pin 9 of the MDA summing network and switches in the rate error. This rate error is obtained from one of three drive rate sources, depending on mode switching. When in tracker mode, the resolved or tracker mode select relay and the tracker and resolved input relay are energized, applying the X output from the star tracker assembly to the servo loop. The signal is then applied through contacts 31 and 41 of the resolved or tracker mode select relay through the cosecant function generator to contacts 39 and 38 of the tracker and resolved input relay. The signal is then fed through contacts 44 and 41 of the deenergized computer input relay, and finally through contacts 49 and 46 of the deenergized input shorting relay to pin 9 of the MDA summing network.

When the system is in resolved manual mode, the same relay configuration prevails, except that the resolved or tracker mode select relay is deenergized. The tracker and resolved input relay is then disconnected from the star tracker source and switched to resolved hand controller rate input from 1/2X computing resolver B2, driven by the trunnion gear train of the CDU.

When operating in direct manual mode, all the relays are deenergized. The source of the drive rate error signal then is the sextant hand controller. The signal is then fed through contacts 54 and 38 of the tracker and resolved input relay, through contacts 44 and 41 of the computer input relay, through contacts 49 and 46 of the input shorting relay to pin 9 of the MDA summing network.

When operating in computer mode (OPTICS MODE switch in COMPUTER position), the computer input relay is energized. This connects the input to pin 9 of the MDA to the AGC via the digital analog converter (DAC). This signal is applied via contacts 31 and 41 of the energized computer input relay and contacts 49 and 46 of the deenergized input shorting relay.

**4-7.2.3 SXT Trunnion Servo Loop.** Rotation of the SXT indexing mirror about the trunnion axis is controlled by the SXT trunnion servo loop (figure 4-41). This servo is similar to the SXT shaft servo in that mode relays select a precise two speed positioning servo loop in the zero optics mode and an integrating servo loop in the remaining modes. The same series of input relays switch the input to pin 9 of the MDA from one of three sources: (1) the SXT trunnion hand controller during direct manual mode; (2) the resolved drive rate from trunnion CDU 1/2X resolver B2 during resolved manual mode; (3) the Y axis output from the star tracker assembly during tracker mode. All relays are energized as explained previously.

SXT trunnion and shaft angles are obtained by interpreting displacement of the SXT indexing mirror about both axes. Two pancake resolvers, mechanically linked with the SXT indexing mirror and SXT head assembly, sense and transmit analog equivalents of SXT mirror displacements about trunnion and shaft axes.



4-7.2.4 SXT Drive Assemblies. The SXT obtains rotational movement about shaft and trunnion axes through two motor generators. Reduction gearing, motor generators, and resolvers are contained in two separate gearboxes. One is located in the optical base; the other is located in the index head setup assembly. (See figure 4-42.)

In trunnion axis, positioning of the indexing mirror is restricted mechanically to a range of -5 to +50 degrees through the use of a limit stop. A command torsion spring assembly is provided in the drive assembly to minimize positioning error.

In trunnion axis, the gear reduction ratio between motor generator shaft and indexing mirror is 11780:1. The gear reduction ratio in shaft axis drive between motor generator shaft and indexing mirror is 3010:1.

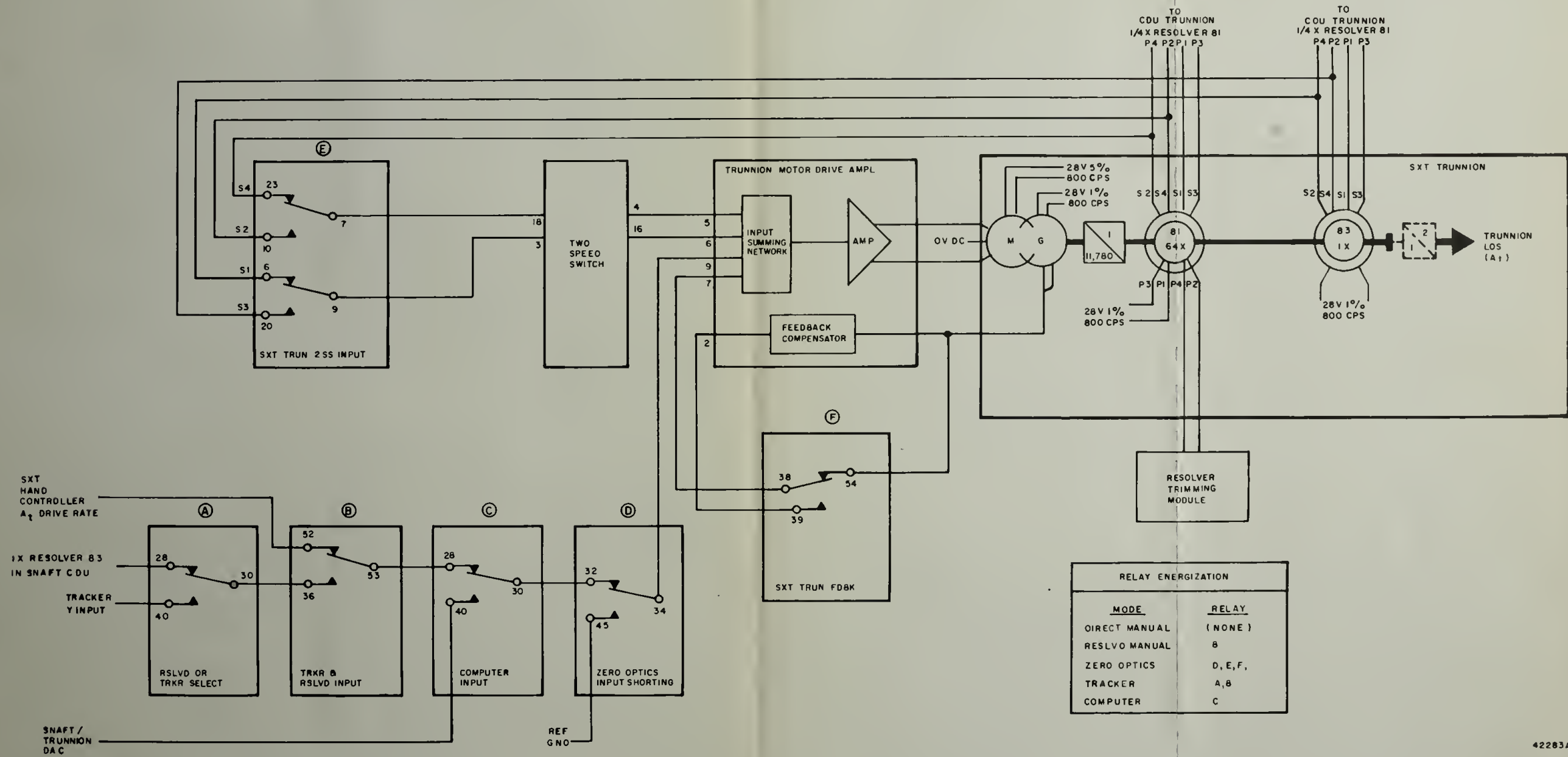
4-7.3 HORIZON SENSOR. The horizon sensor includes optical elements, a light resonator, and electronics which determine the earth's horizon by detection of 1/2 peak atmospheric illumination. This enables use of the earth's limb as a space navigational reference. Figure 4-43 is a detailed block diagram of the horizon sensor circuits.

4-7.3.1 Horizon Sensor Optics. The optical elements of the horizon sensor (figure 4-44) include an optical filter, an objective assembly and a collector lens, a single tuning fork light resonator assembly, and electronics. Reflected light from the earth's limb passes through an optical and ultraviolet filter and is viewed by an objective lens which focuses the light onto the resonator assembly via a reflecting mirror. The assembly modulates the light as it vibrates across the light path. The pulses of light are then directed to a photomultiplier tube via a collector lens. The photomultiplier tube acts as a transducer which converts time-based light pulses into electrical pulses with corresponding timing.

The objective lens is an air-spaced, positive-negative doublet with an 18 mm clear aperture, an effective focal length (EFL) of 65 mm, and a focal ratio (f number) of approximately 3.7. The lens is corrected for wavelengths corresponding to the S4 response of the photomultiplier (0.4 microns), that is, the objective lens and phototube are matched for spectral sensitivity. The collector is a single lens with a clear aperture of 5 mm and an EFL of 5.5 mm.

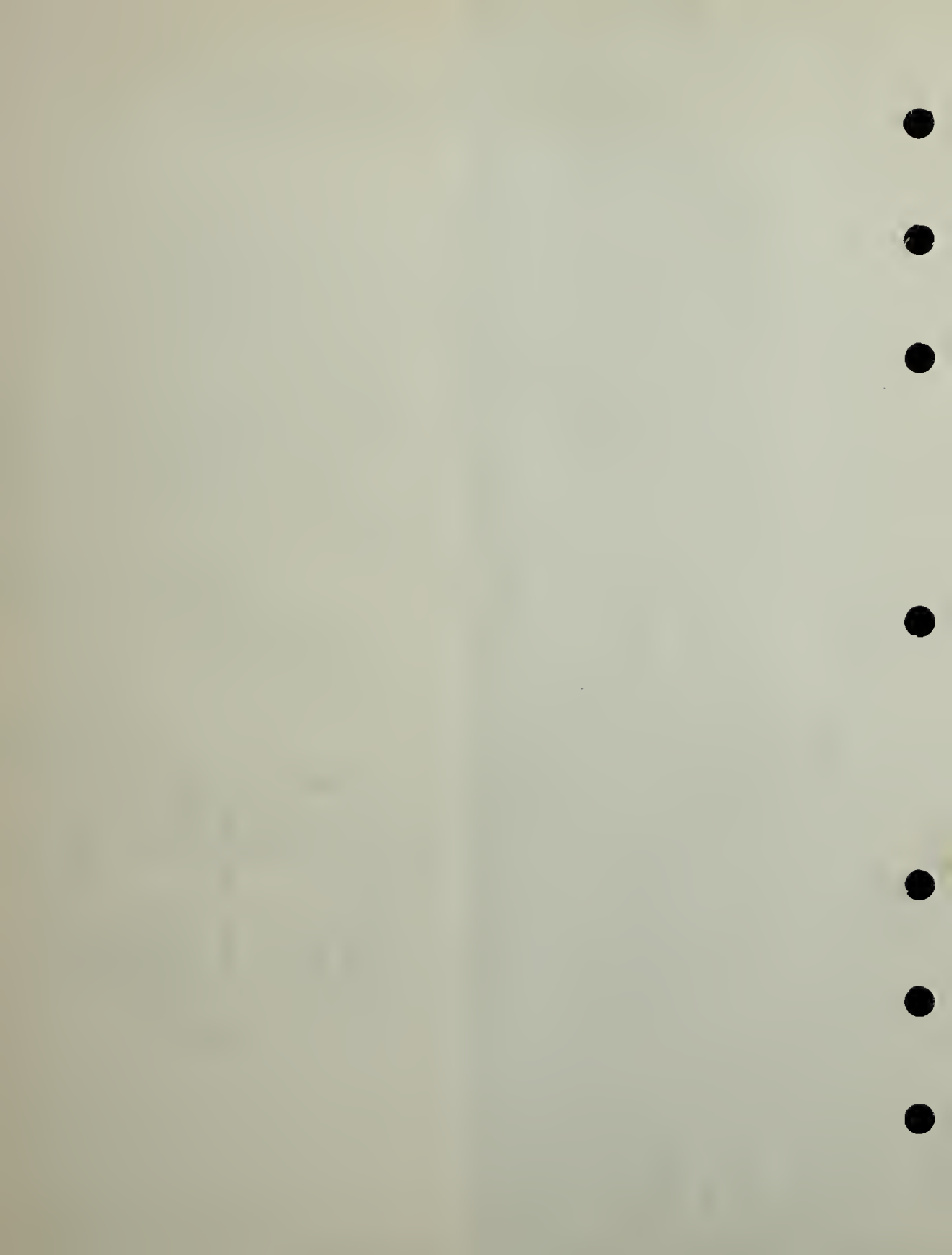
4-7.3.2 Light Resonator Assembly. The light resonator assembly used in the horizon sensor is a single vibrating tuning fork with single drive and pickup coils. A drive coil and pickup coil are adjacent to the fork tine. The drive and pickup coil are used in conjunction with the drive amplifier to form a precision oscillator. The fork tine resonates at a natural frequency of 550 cps. In the horizon sensor, light is modulated by the fork tine as it vibrates across the slit. Vibration frequency and amplitude are held constant. The tuning fork and drive amplifier form a precision oscillator where the frequency of oscillation is controlled by the resonant frequency of the tuning fork. The intensity of the modulated light is a function of the location of the HLOS with respect to peak illumination in the earth's atmosphere.

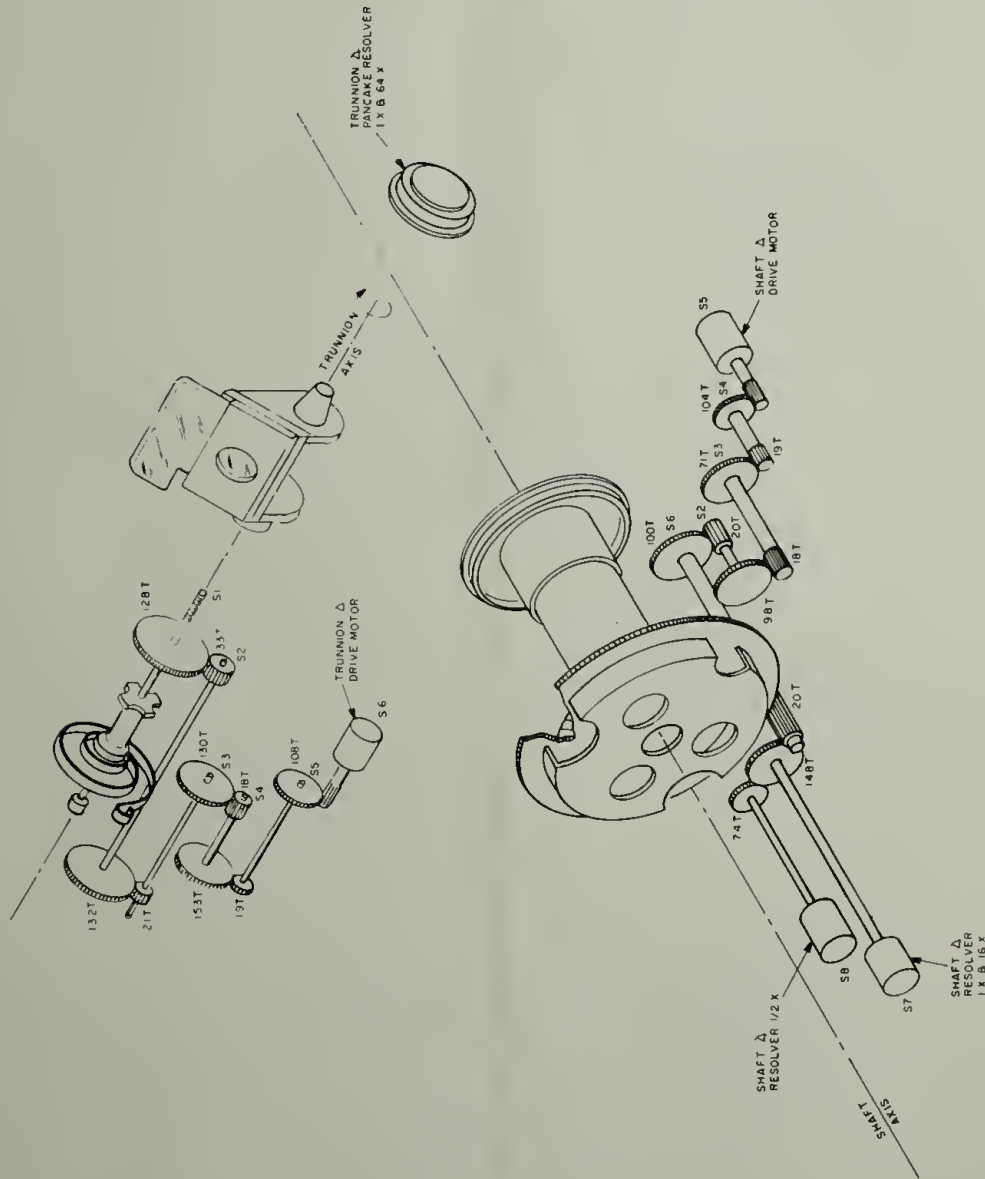
APOLLO GUIDANCE AND NAVIGATION SYSTEM



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Figure 4-41. SXT Trunnion Servo Loop, Block Diagram





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Figure 4-42. SXT Gearing Diagram

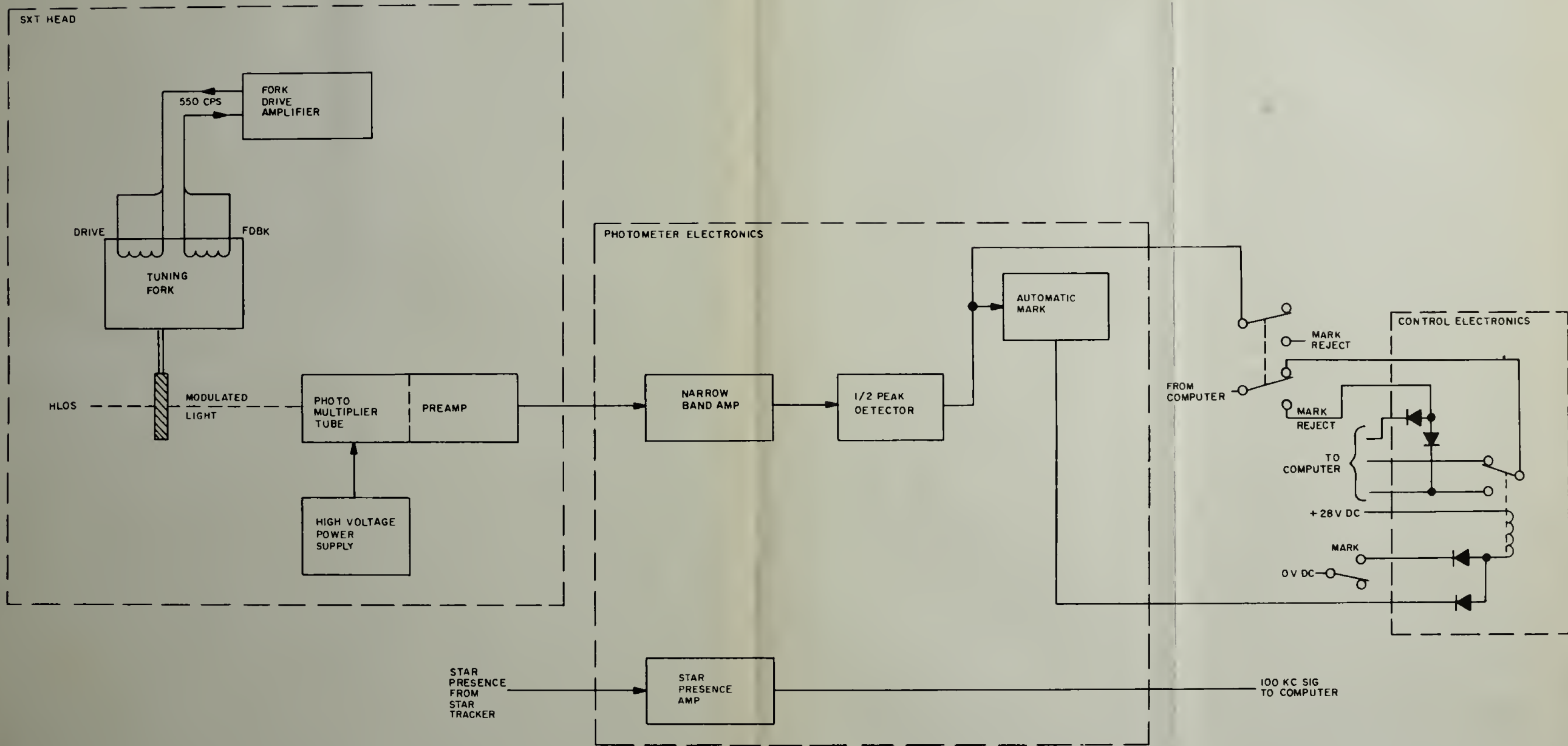
4-7.3.3 Horizon Sensor Electronics. The horizon sensor electronics include the photomultiplier tube and its fixed high voltage supply, preamplifier, and fork drive amplifier, all of which are mounted inside the SXT head; a narrow band amplifier; 1/2 peak detector; automatic mark; and star presence gate. The horizon sensor high voltage power supply is similar to that of the star tracker, except that it is fixed and supplies an output of -900 volts dc.

4-7.3.3.1 Photomultiplier Tube. The photomultiplier tube (figure 4-45) is a light-sensitive device using photo emission and secondary emission to develop a measurable output current for very low levels of incident illumination. Primary photo current for low light levels is so small that special amplification techniques are required in most applications.

In a photomultiplier tube, the photoelectrons emitted by the cathode are, in general, electrostatically directed to a secondary emitting surface called a dynode which emits 3 to 7 secondary electrons for each primary electron. These secondary electrons are focused to a second dynode which repeats the process. In each successive stage, an ever-increasing stream of electrons is emitted until those emitted from the last dynode are collected by the anode and constitute the output current. In addition to 6 to 14 dynodes, the photomultiplier tube contains other electrodes for focusing the electron stream to reduce space-charge effects, or to accelerate the electrons to reduce transit-time effects. The last dynode is followed by an anode which collects the electrons and serves as the signal output electrode.

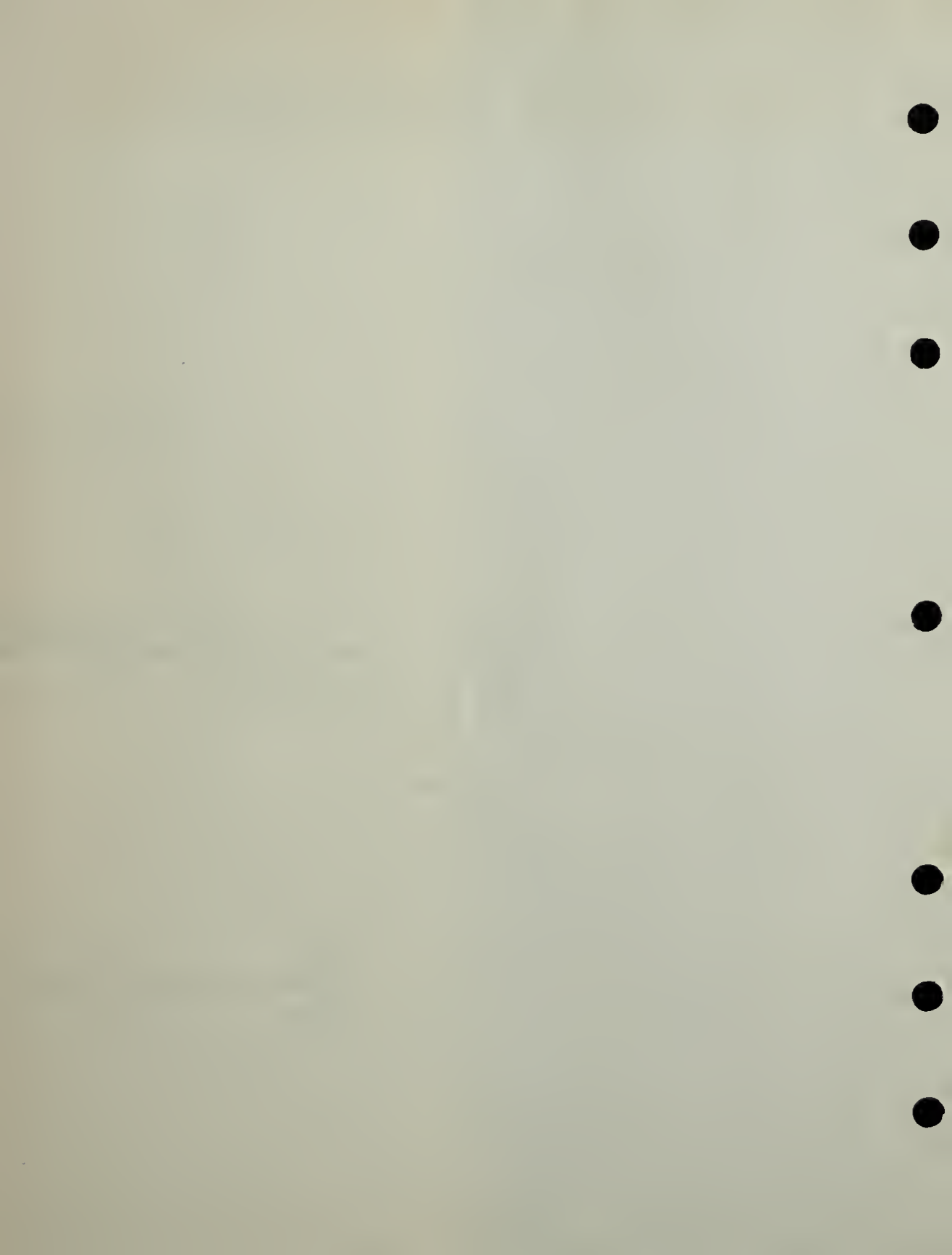
Both the star tracker and horizon sensor use a miniature photomultiplier tube: RCA Model 8571, a nine-stage, side-on type having S4 response. Every photomultiplier tube has a spectral S4 response curve (see figure 4-46). This characteristic is obtained by plotting the output of the tube at intervals of the incident light. The vertical axis in figure 4-46 is the percentage of the maximum photomultiplier tube response; the horizontal axis is divided into angstroms. This tube peaks at 0.4 microns (4000A) in the blue portion of the spectrum. This type of tube uses cesium-antimony dynodes and a cesium-antimony opaque photocathode. Window material is Corning No. 0080 lime glass, or equivalent. The tube is intended for specialized applications involving extremely low light levels. It features a combination of high photo sensitivity, high secondary emission amplification, and low dc dark current.

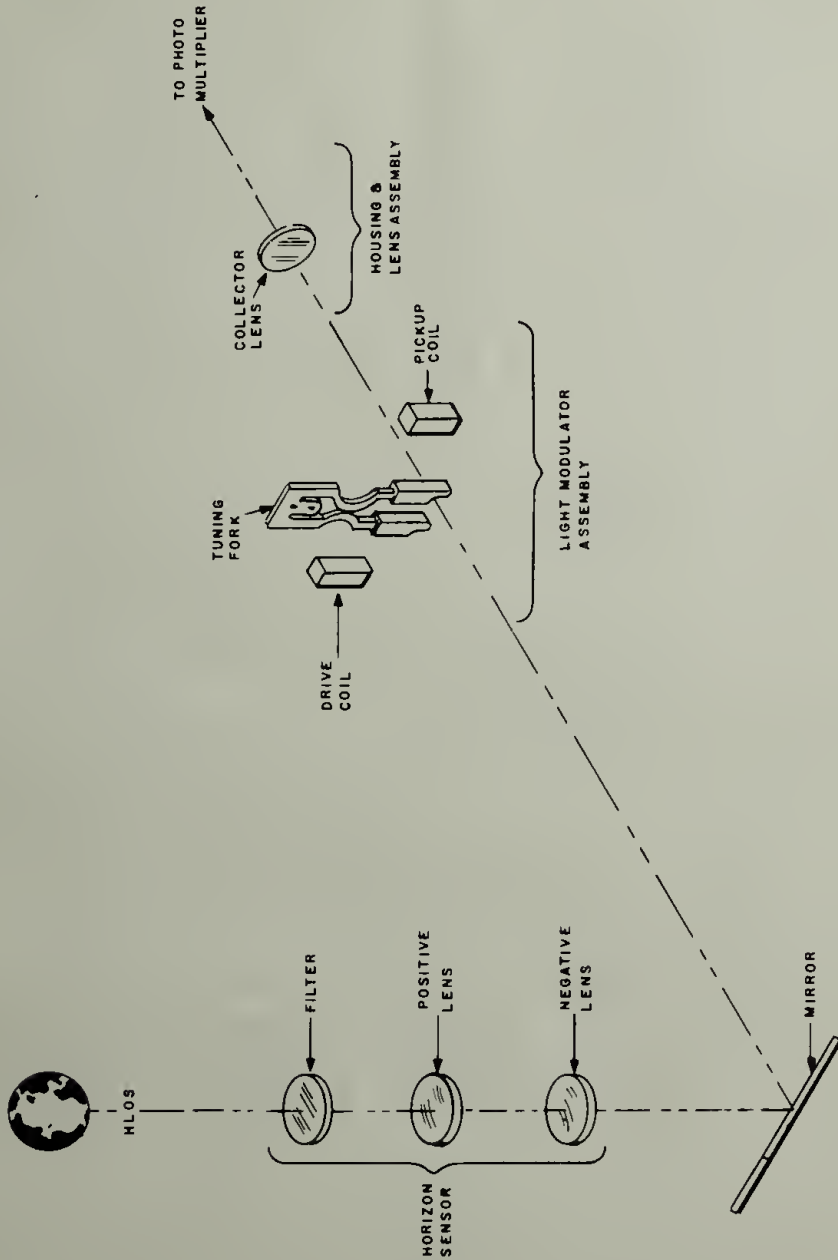
The frequency response of the tube is flat up to a frequency of about 100 megacycles, above which the variation in electron transit time becomes the limiting factor. The size, shape, and position of the dynodes are critical; in the tube the last dynode (number 9, figure 4-45) is so shaped as to partially enclose the anode and to serve as a shield to prevent the fluctuating potential of the anode from interfering with electrons focusing in the interdynode region.



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Figure 4-43. Horizon Sensor Circuit, Block Diagram

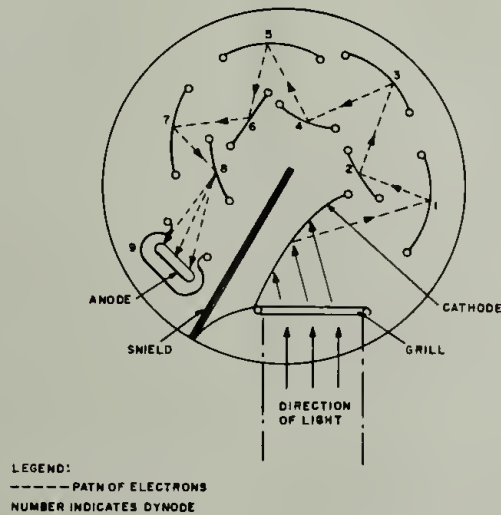




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Figure 4-44. Horizon Sensor Optics



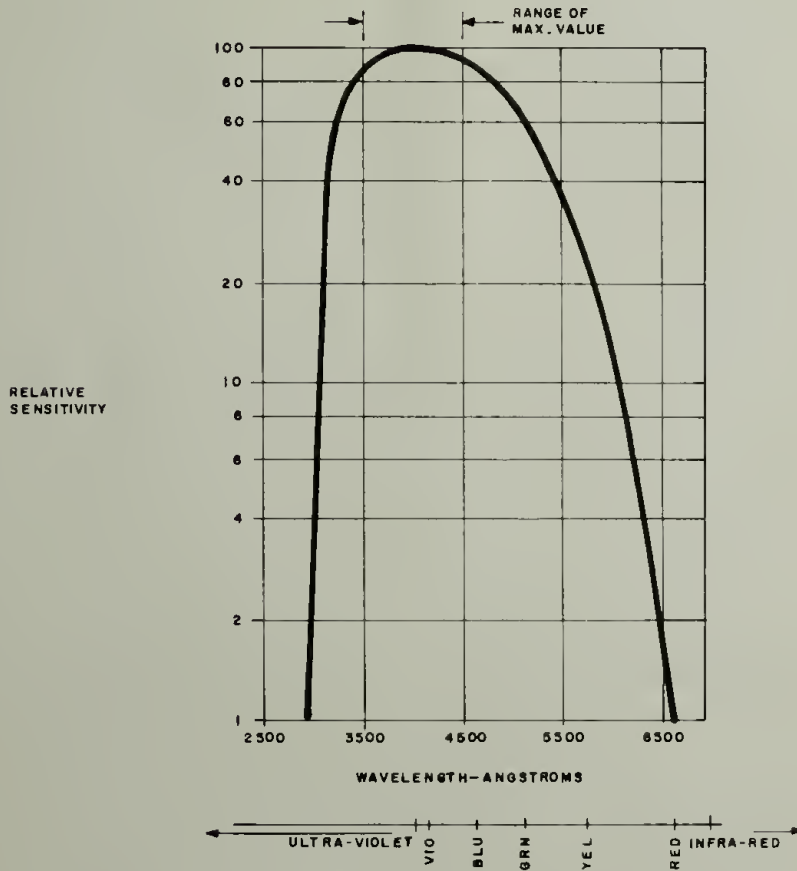


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Figure 4-45. Photomultiplier Tube Diagram

The anode consists of a grating which allows the electrons from dynode number 8 to pass through to dynode number 9. Spacing between dynode number 9 and the anode creates a collecting field so that all the electrons emitted by dynode number 9 are collected by the anode. Therefore, the output current is substantially independent of the instantaneous positive anode potential over a wide range. The shield, which extends between the cathode and the anode, shields the cathode from the anode and prevents ion feedback. The grill through which the incident radiation reaches the cathode is connected to the cathode and is an electrostatic shield for the open side of the electrode structure.

The photomultiplier tube output must be amplified since it is a dc output proportional to illumination. Because difficulties of dc amplification would be incurred in effecting more than one stage of amplification, the horizon sensor and tracker use a light-chopping device. By interrupting at regular intervals the light striking the photomultiplier, an ac output can be obtained and amplified. Narrow band amplifier responses at the mechanical frequency of the light-chopping device permit higher gains per stage and reduce the noise problem.



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Figure 4-46. Photomultiplier S4 Response Curve

4-7.3.3.2 Preamplifier. A preamplifier amplifies the pulses from the photomultiplier tube and acts as a buffer to present a high input impedance to the photomultiplier tube and low output impedance to the narrow band amplifiers. Basically, the preamplifier is a four stage amplifier providing a gain of 10, with a field effect transistor as the input stage for high input impedance (about 50 megohms) and low noise. Both the photomultiplier tube and preamplifier are combined in one housing to minimize any pickup in their critical area where the signal is small and the preamplifier input is very high.

4-7.3.3.3 550 cps Narrow Band Amplifier. The 550 cps narrow band amplifier filters the fundamental and second harmonic signals from the total phototube output. This filtering greatly improves the signal-to-noise ratio of the system by rejecting much of the phototube noise, thereby providing increased sensitivity. In addition, the narrow band amplifier provides a signal gain of 10.

4-7.3.3.4 Peak Detector. The peak detector rectifies the narrow band amplifier output and provides a positive dc charge to a capacitor. The positive dc charge is fed to the capacitor through a field effect transistor which provides the high impedance necessary to prevent the capacitor from discharging. The capacitor will remain charged at the peak signal level. One half of the peak signal is fed to the comparator.

4-7.3.3.5 Comparator. The input section of the comparator is a resistor summing junction which combines two incoming signals; half the positive rectified maximum value of the horizon signal, and the negative rectified value of the horizon signal. The resulting voltage will be positive or negative depending on whether or not the horizon signal has reached the half peak value. (See figure 4-47 for waveforms.) This dc sum voltage is then chopped, using the forkdrive signal as a chopping voltage. The resulting ac signal will be zero phase or 180 degree phase, depending on whether the dc sum voltage is positive or negative. This crossover point is the half intensity point of horizon light. The ac signal is amplified to increase the accuracy of detection of the crossover point. The ac signal is then demodulated and the resulting dc signal fed to the horizon gate.

The input section of the horizon gate consists of a Schmitt trigger which provides a step signal when the input from the comparator crosses from positive to negative. This step signal controls a switch which turns on a 100 kc signal to the AGC as the indication that HLOS has been attained.

4-7.4 STAR TRACKER. The star tracker includes optical elements, a special light modulator, and electronics to form a functional unit. The unit provides precise star position error information for the sextant trunnion and shaft servo integrating loops when the optical subsystem is operating in tracker mode. Figure 4-48 is a detailed block diagram of the star tracker.

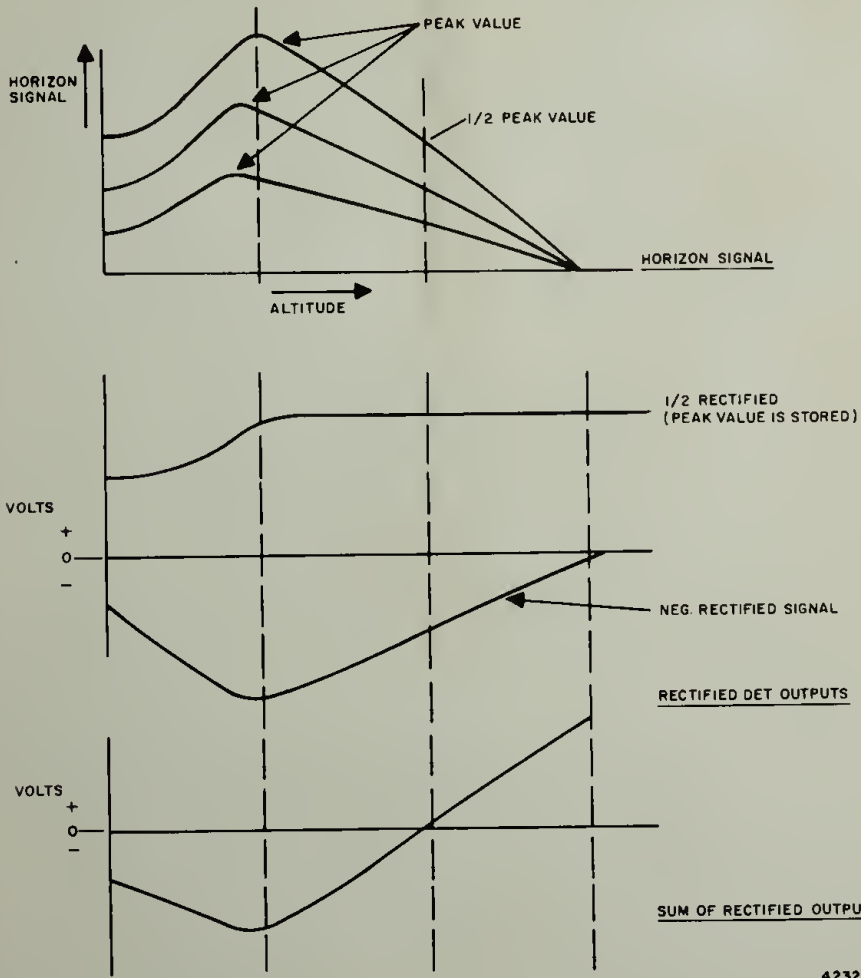


Figure 4-47. Horizon Sensor Waveforms

4-7.4.1 Star Tracker Optics. The star tracker optics are shown in figure 4-49. The star tracker line of sight is nearly parallel to the sextant star line of sight. Star light flux is introduced in the tracker optics via the side tab of the SXT indexing mirror. Light from a selected star is reflected by the SXT indexing mirror onto two fixed right angle mirrors which deflect the light back through an objective lens which gathers and focuses the light. A tuning fork type of resonator assembly, situated at the focal plane, modulates the star light flux. Two tuning forks modulate the light in the field of view with respect to a null and generate light pulses which are condensed and directed to a tracker photomultiplier tube. Modulated light is converted to electrical signals and amplified by the photomultiplier tube. In this process, light is modulated and converted to generate error signals along the tracker X and Y axes. The error signals are used by the shaft and trunnion servo loops to maintain  $S_tLOS$  at the null position. In this way the star tracker retains automatic lock-on of the star.

Radiated star light is viewed by the objective lens. This lens is an air-spaced doublet having 20 mm clear aperture, an E.F. of 75 mm, and an f number of approximately 3.7. The lens is corrected for wavelengths corresponding to the S4 response of the photomultiplier tube (0.4 microns), that is, the objective lens and phototube are matched for spectral sensitivity. The objective lens focuses a cone of radiated star light at its focal plane so that the total field is approximately 0.5 degree. The angular field is equivalent to a 0.84 mm (0.033 inch) diameter circle at the focal plane. In effect, this dimension corresponds to the minimum total excursion of the tracker without vignetting.

4-7.4.2 Light Resonator Assembly. The resonator assembly (figure 4-50), which modulates the star light flux, consists of two identical tuning forks with slotted aperture plates attached to their tines. The tuning forks are mounted end to end (tine against tine) so that the aperture plates overlap one another. The slots of one tuning fork are aligned to the sextant and the slots of the second are aligned to and define their own detection axes.

A drive coil and pickup coil are adjacent to the fork tines of each tuning fork. The drive coil and pickup coil are used in conjunction with their respective drive amplifier to form a precision oscillator. The X axis fork resonates at a natural frequency of 455 cps, the Y axis fork resonates at 356 cps. The slits attached to the tines therefore sweep across the optical axis at these rates. Light can pass only through the open square formed by the intersection of the mutually perpendicular slits. The scanning pattern formed by this square is a spiral-like motion with the square aperture periodically sweeping toward the optical center and then sweeping away from it along the spiral path. Because of the precision control of the vibrating frequencies and amplitudes, the pencil of continuous light from the star is converted to bursts of light with a unique phase and time relationship for each star position. Therefore, the light which passes through the resonator assembly onto the photomultiplier is modulated light containing star position information. This information is utilized by the tracker electronics for the generation of X axis and Y axis error signals.

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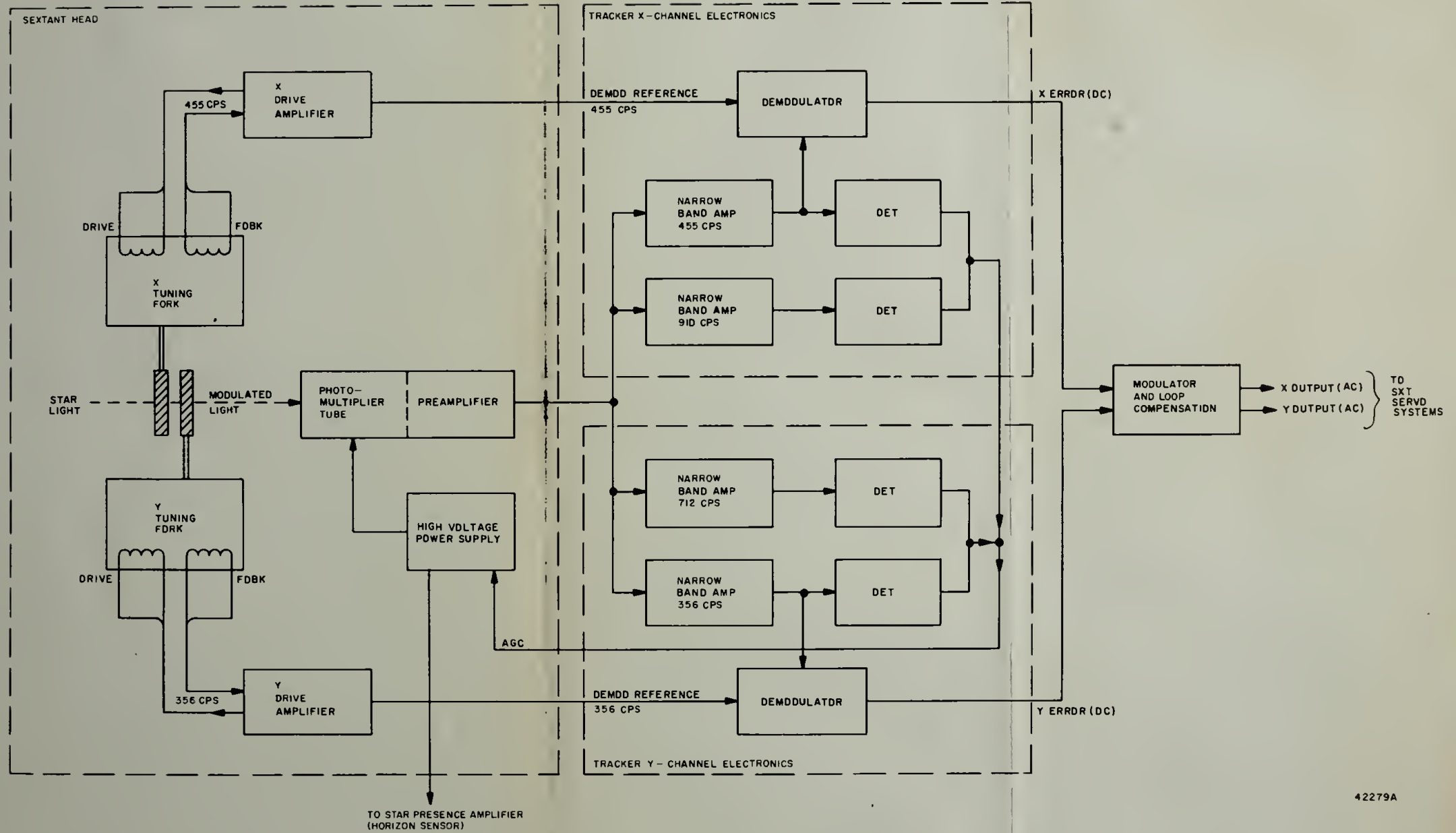
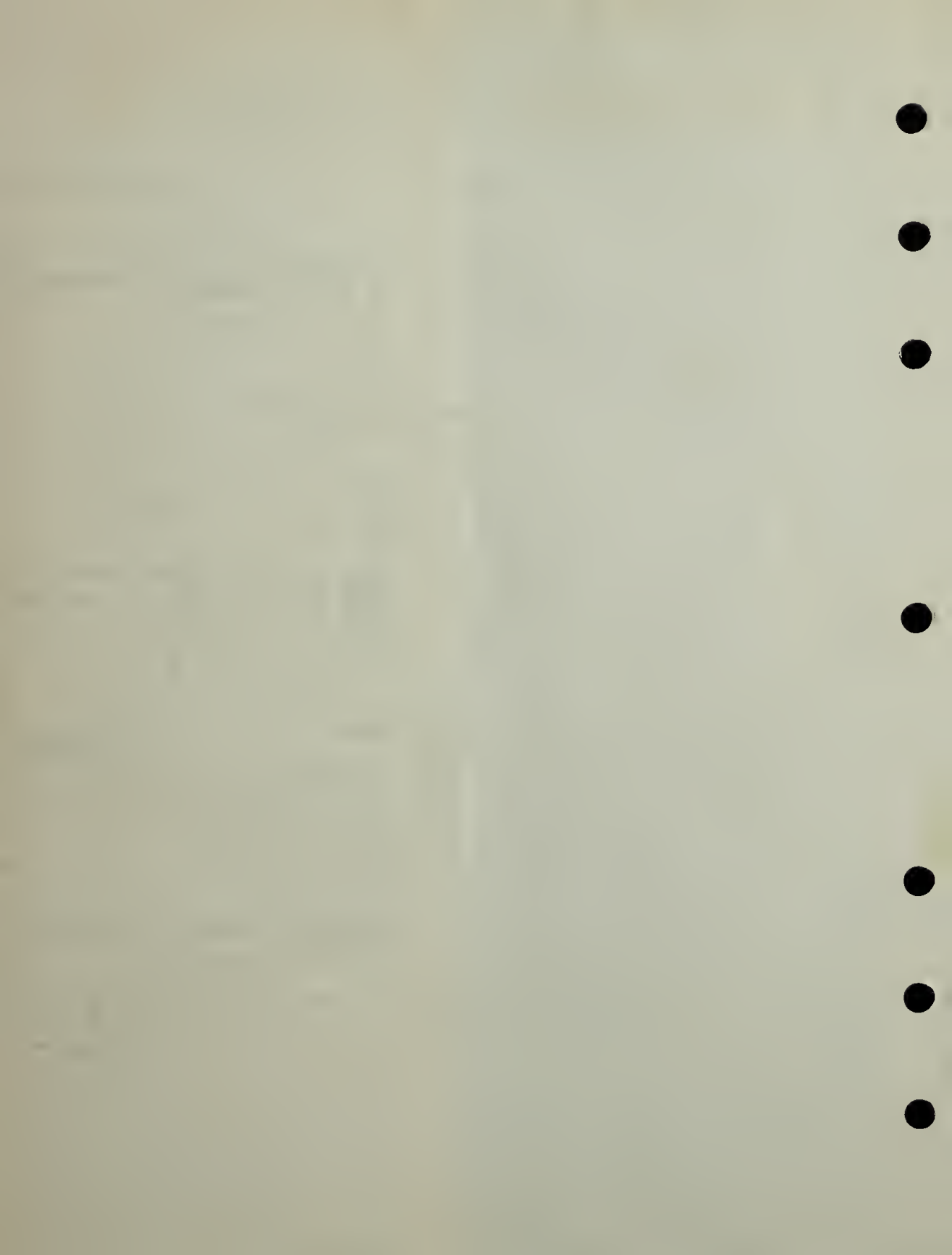
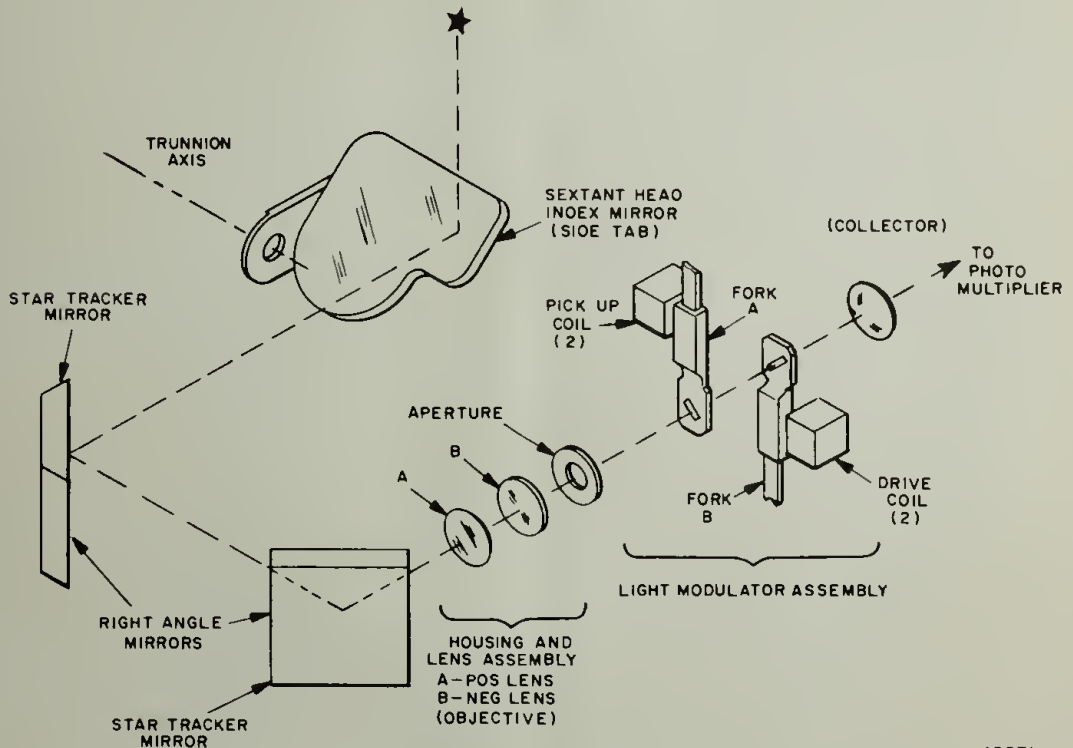


Figure 4-48. Star Tracker Circuit, Block Diagram

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Figure 4-49. Star Tracker Optics

The actual aperture is 0.0092 inch wide and the half-amplitude swing is 0.01 inch. The field of view, therefore, is 0.0092 plus two times 0.01 or 0.0292 inch.

When the star image is focused at the center of oscillation, the image is cut twice for each cycle of fork motion. The resulting signal contains a maximum of the double frequency component (712 and 910 cps due to the double chopping in this case) and there is no fundamental frequency component. This null waveform is on and off for equal periods of time and is referred to as a symmetrical waveform.



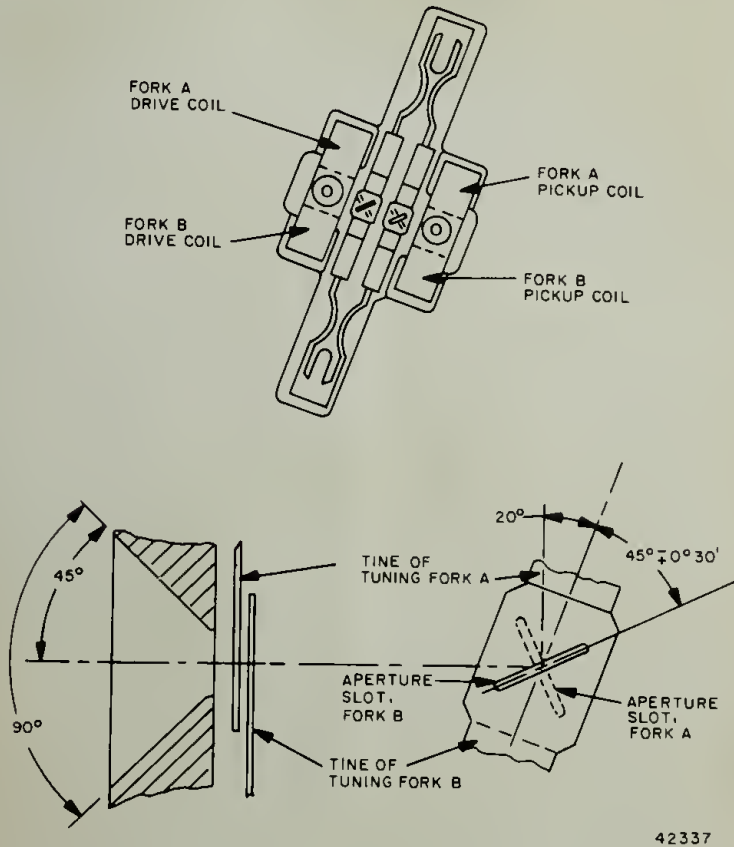


Figure 4-50. Star Tracker Light Modulator Assembly

When the star image is not at the center of aperture oscillation, the duty cycle (the on-off intervals and phase change) changes. The resulting waveforms contain varying amounts of fundamental and second harmonic components.

The fundamental frequency signal is used to drive the SXT servomotors for tracking purposes. The sum of the fundamental and second harmonic is used as the indication of star presence because this sum remains relatively constant over the range of star positions.

4-7.4.3 Star Tracker Electronics. The star tracker electronics include the photomultiplier tube and its variable high-voltage power supply, preamplifier, and X and Y fork drive amplifiers, all mounted inside the SXT head; two narrow band amplifiers; two detectors; a demodulator; and a common modulator and loop compensation circuit. The preamplifier and narrow band amplifiers operate in the same manner as those used in the horizon sensor, paragraph 4-7.3.3.

4-7.4.3.1 Photomultiplier. A single photomultiplier tube is used to convert the modulated light to electrical signals. Operation characteristics of this tube are described in paragraph 4-7.3.3.1. The applied anode to cathode voltage is nominally set to 1000 volts. To minimize the effects of magnetic fields, the phototube is enclosed in a magnetic shield. The output of the phototube is fed to the X and Y channel electronics via a preamplifier.

4-7.4.3.2 X and Y Axis Fork Drive Amplifiers. Each tuning fork and associated fork drive amplifier form a precision frequency oscillator, where the frequency of oscillation is controlled by the resonant frequency of the fork. The feedback coil measures the amplitude of the fork vibration. This signal is fed back to the amplifier to maintain a constant vibration amplitude. An output from each amplifier is fed to its respective demodulator, where it serves as a reference input. This assures synchronization of the electronics with the physical vibration of the tuning fork.

4-7.4.3.3 Detectors. The detector circuitry is a part of the narrow band amplifier assemblies. The diode detector rectifies and sums the four tracker signals (fundamental and second harmonic from the X axis and fundamental and second harmonic from the Y axis) to provide a star presence indication and automatic gain control signals for the tracker high voltage power supply.

4-7.4.3.4 High Voltage Power Supply. A variable high voltage power supply provides a driving voltage for the tracker photomultiplier tube. This voltage varies from 800 to 1200 volts and is controlled by the automatic gain control voltage, a function of star intensity. The automatic gain control assures that drive signals derived from the star will be a function of star position error only and will not vary with star intensity. The tracker high voltage power supply assembly also contains part of the star presence detection circuitry, which amplifies output of the detectors and provides a signal to the star presence amplifier located in the tracker electronics.

4-7.4.3.5 Star Presence Amplifier. The star presence amplifier increases the dc signal from the star presence section of the high voltage power supply and uses the signal to switch a 100 kc signal to the AGC when satisfactory acquisition is achieved.

4-7.4.3.6 Demodulator. The X and Y channel fundamental narrow band amplifiers provide input signals to their respective demodulators which convert the output to a dc error. A second input to each demodulator is the reference input from its associated tuning fork drive amplifier to provide synchronization with the vibrating fork. If the target star

is centered in the tracker field of view, the output from the demodulator is zero, due to cancelling effects of the two inputs. As soon as the star drifts off the null position, the light bundles passing through the scanner occur at different intervals and the photo-multiplier tube preamplifier generates corresponding inputs for its narrow band amplifier. The relationship between the narrow band amplifier output and the demodulator reference from the tuning fork oscillator now contains error information proportional to the shift in star flux from the center of the tracker field of view. The X axis demodulator generates a dc signal proportional to the drift of the star along the light modulator X axis, and the Y axis demodulator generates a dc signal proportional to the drift of the star along the light modulator Y axis. These dc outputs are fed to modulator and loop compensation networks.

4-7.4.3.7 Modulator and Loop Compensation Circuit. This module (located in the PSA) contains two identical circuits: one for light modulator X error dc input and the other for light modulator Y error dc input. A common 28 volt, 800 cps reference input is applied to a transformer, one secondary of which is used in the X channel and the other in the Y channel. The +28 volt dc supply as well as the reference are applied by the TRACKER POWER switch on the G and N indicator control panel. The ac reference voltages are applied to the base circuits of phase sensitive type modulators which convert the X and Y dc error signals into ac error signals of the corresponding phases and amplitudes. These signals are then applied through lead-lag compensating networks, two-stage amplifiers, and output transformers to the SXT shaft and trunnion servo systems. The servos drive the optics in response to the error signals so that the star is maintained in the center of aperture oscillation, thereby removing the error signals. This automatically completes the servo loops for tracker mode.

#### 4-8 APOLLO GUIDANCE COMPUTER

This paragraph contains a discussion of the theory of operation of the Apollo Guidance Computer (AGC). Two levels of theory discussion, functional and detailed, are presented for each element of the AGC. Machine instructions and programs are also described in sufficient detail for support of maintenance activities.

4-8.1 TIMER. The timer generates all of the timing functions required for operation of the computer subsystem (CSS); it also supplies signals to the other spacecraft systems. The timer (figure 4-51) consists of the clock oscillator, clock countdown, scalers A and B, time pulse generator, and start-stop logic. The clock oscillator generates the input for the clock countdown circuit which divides the clock oscillator signal and produces inputs for the scalers and the time pulse generator. The start-stop logic supplies stop signals to the clock countdown circuit when the start signal GOJAM is applied throughout the AGC.

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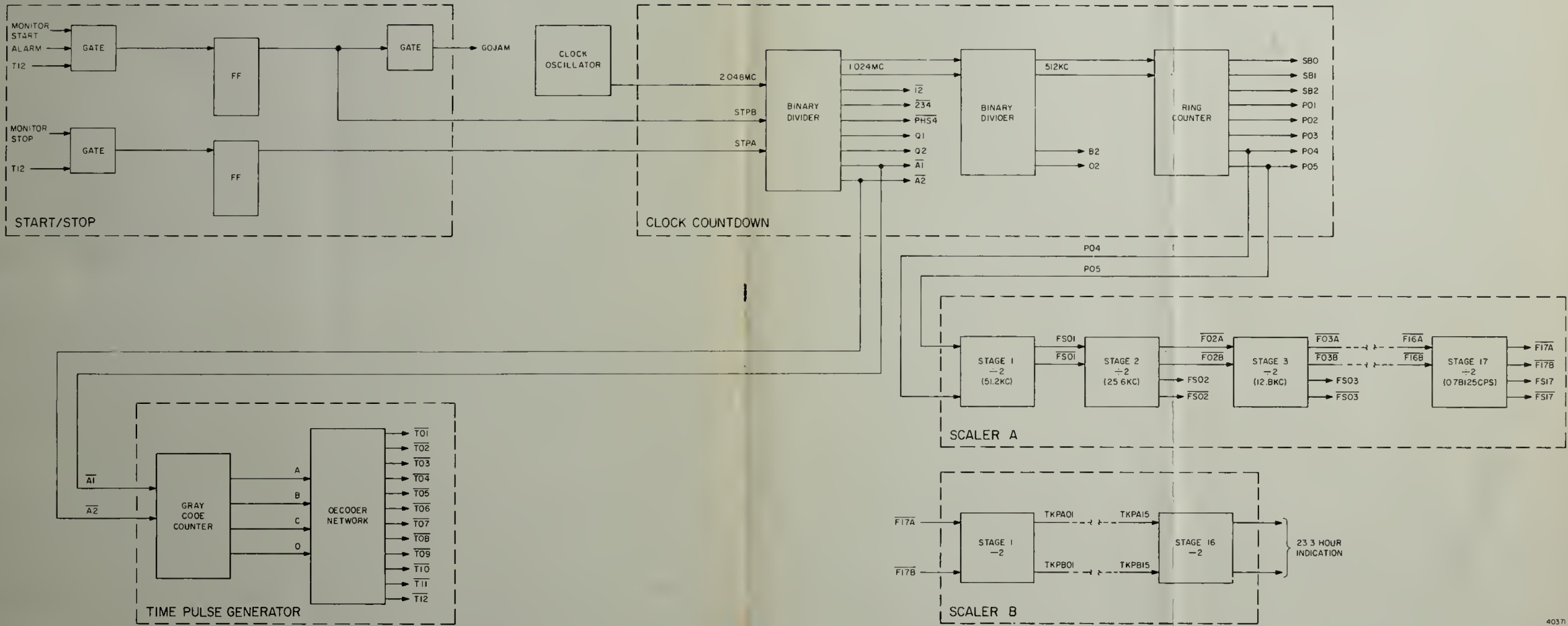


Figure 4-51. Timer, Functional Diagram



## APOLLO GUIDANCE AND NAVIGATION SYSTEM

The input to scaler A is divided to produce rate signals and an output to scaler B. Scaler B divides the output of scaler A to produce real time indications of 23.3 hours. The input to the time pulse generator from the clock countdown circuit produces control signals for use throughout the AGC. The start-stop logic produces stop signals and signal GOJAM in the event that an AGC alarm is sent to the start-stop logic. The stop signals are applied to the clock countdown circuit and inhibit the signal feed to the time pulse generator. This inhibits timing signal outputs from the time pulse generator; at the same time, signal GOJAM is produced by the start-stop logic and fed throughout the AGC.

4-8.1.1 Clock Oscillator Functional Description. The clock oscillator is a crystal-controlled modified Pierce oscillator that generates the source frequency of 2.048 mc for the timer. The clock oscillator consists of five stages: an input amplifier, buffer circuit, shaper, output circuit, and power regulator. The 2.048 mc signal from the output circuit drives the first binary divider in the clock countdown circuit.

4-8.1.2 Clock Countdown Functional Description. The clock countdown circuit contains two binary dividers and a ring counter. The first binary divider circuit divides the input frequency of 2.048 mc by two and generates output signals  $\overline{A1}$ ,  $\overline{A2}$ ,  $Q1$ ,  $Q2$ ,  $\overline{PHS4}$ ,  $\overline{12}$ , and  $\overline{234}$  at a 1.024 mc rate. Signals  $\overline{A1}$ ,  $\overline{A2}$ , and  $\overline{PHS4}$  are 0.25 microsecond pulses, and signals  $Q1$  and  $Q2$  are 0.5 microsecond square waves. The read, write, and clear control signals  $\overline{12}$  and  $\overline{234}$  are 0.25 microsecond and 0.75 microsecond pulses, respectively, and are produced by gating signal  $Q1$  with  $Q2$  and  $Q1$  with  $Q2$ . Signals STPA and STPB, generated by the start-stop logic, inhibit the  $\overline{A1}$  output, which prevents any word flow in the AGC. Timing signals cannot be produced by the time pulse generator without signal  $\overline{A1}$ . The second binary divider circuit divides the 1.024 mc input from the first divider by two and generates signals B2 and D2, which are 512 kc square waves. Two separate 512 kc outputs drive the ring counter, which generates signals P01 through P05. Signals P01 through P05 are 5 microsecond pulses at a 102.4 kc rate. The ring counter outputs are used to generate signals SB0, SB1, and SB2, which are 3 microsecond pulses, also at a rate of 102.4 kc.

4-8.1.3 Scaler A Functional Description. Scaler A contains 17 identical divider stages and generates signals at various rates from 51.2 kc to 0.78125 cps. The first stage of the scaler is driven by ring counter output signals P03 and P05. Thereafter, each successive stage divides the output of the previous stage by two.

4-8.1.4 Scaler B Functional Description. Scaler B contains 16 identical divider stages and is similar to scaler A with the exception that information can be read out. The outputs of the last stage of scaler A drive the first stage of scaler B. Each successive stage performs a division by two up to the last stage (TKPA16). An output from the last stage indicates time intervals of 23.3 hours.

4-8.1.5 Time Pulse Generator Functional Description. The time pulse generator produces timing pulse outputs  $\overline{T01}$  through  $\overline{T12}$ , which are used in various sections of the AGC. The timing pulses are generated by decoding the output of the gray code counter,

which is driven by input signals  $\overline{A1}$  and  $\overline{A2}$  from the clock countdown circuit. The time pulse generator is inhibited by monitor start and monitor stop commands or by an alarm.

4-8.1.6 Start-Stop Logic Functional Description. The start-stop logic generates signals STPA, STPB, and GOJAM. Signals STPA and STPB are applied to the first binary divider circuit and inhibit the  $\overline{A1}$  output. This action subsequently inhibits timing pulse outputs T01 through T12 and prevents any word flow within the AGC. A monitor stop command from the computer test set (CTS) coincident with T12 (timing pulse 12) causes signal STPA to be generated, which stops the time pulse generator. The time pulse generator resumes its normal sequence when the monitor stop command is removed. A monitor start command from the CTS or an alarm condition each coincident with T12 causes signal STPB to be generated. Signal STPB causes GOJAM to be generated.

4-8.1.7 AGC Clock Oscillator Detailed Description. The AGC clock oscillator (figure 4-52) generates the source frequency of 2.048 mc and consists of five stages: an input amplifier (Q1), buffer circuit (Q2), shaper (Q3), output circuit (Q5), and power regulator (Q4). Transistor Q1 operates as a class A amplifier that drives the Q2 buffer circuit. The sinusoidal output of Q2 is applied to pulse shaper Q3. The resultant square wave is applied to transistor Q5, the output circuit. Transistor stage Q4 forms a power regulator for the oscillator.

Variable inductor L1 compensates for frequency drift due to component aging. The output of Q2 feeds a dc feedback loop, made up of CR5, CR6, C4, C7, R17 and R26, which controls the peak-to-peak output level of transistor Q1.

The power regulator stage consists of Q4, zener diodes CR1 and CR2 rated at 6.2 volts each, filter capacitors C10 and C11, dropping resistors R29 and R30, and diodes CR7 and CR8 that form an OR circuit. During normal operation CR7 is forward biased and CR8 is reverse biased. An AGC requirement is that the oscillator must be the last unit to sense the failure if a power failure should occur. To satisfy this requirement, CR8 becomes forward biased upon a power failure and sustains operation of the oscillator for a short period of time.

The temperature compensation circuit, consisting of resistors R1 through R9 and R31, thermistors RT1 and RT2, and varicap CR3 improves oscillation stability. The varicap is a reverse-biased diode that introduces capacitance into the circuit. When the reverse bias is varied by temperature change, the effective capacitance in series with the crystal changes. This change stabilizes the frequency of the oscillator. Resistor R27 and capacitor C12 are the internal temperature sensor and provide a resistive indication of the clock oscillator temperature.

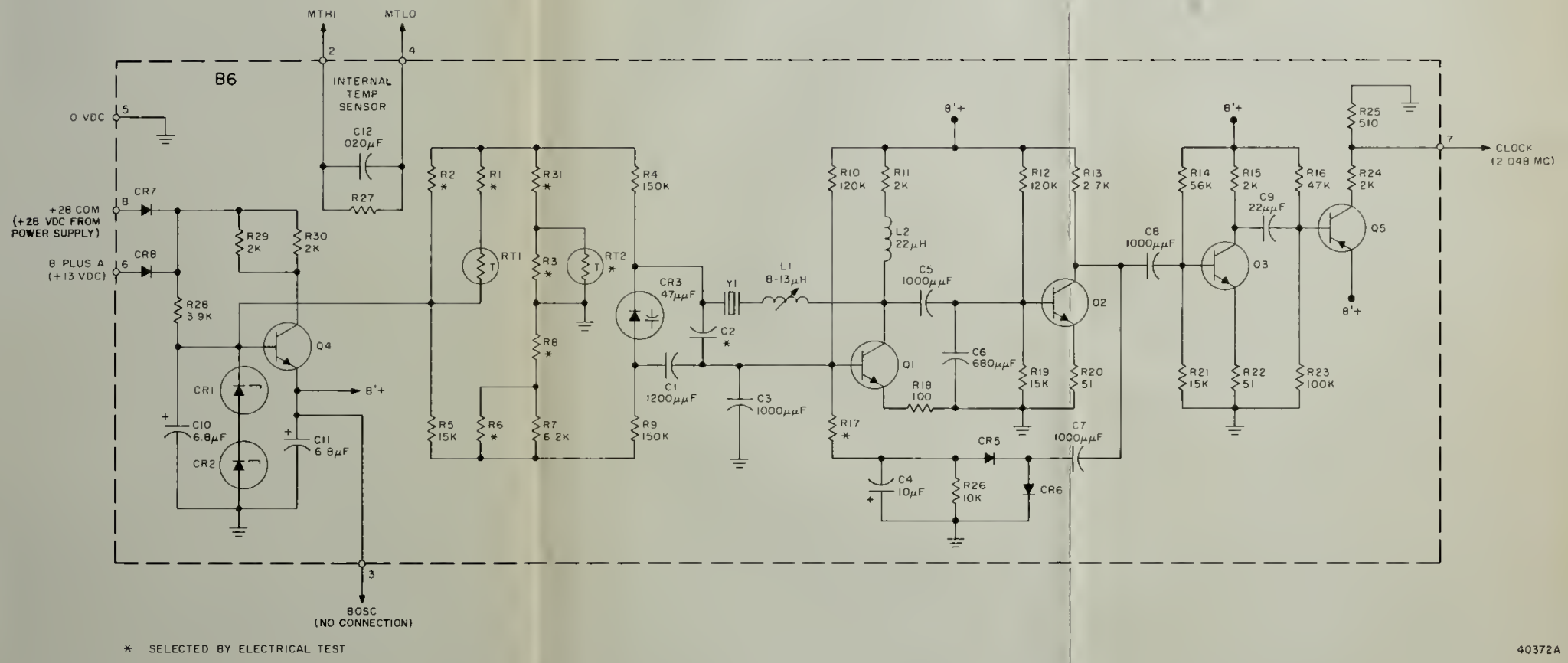


Figure 4-52. AGC Clock Oscillator Circuit





NOTE: Refer to Appendix C for an explanation of logic diagram symbology.

4-8.1.8 Clock Countdown Detailed Description. Each binary divider (figure 4-53) consists of two flip-flops and associated gating circuits. The clock input (2.048 mc) from the oscillator is applied to input gates 50004 and 50005 of the first flip-flop through gates 50001 and 50003. The clock input also is inverted by gate 50002 and is applied to input gates 50008 and 50009 of the second flip-flop. This inversion allows an enabling clock pulse to the second flip-flop during the interval that the clock input goes positive. The outputs of gates 50004 and 50005 are fed forward to the input gates of the second flip-flop. This feed-forward technique is incorporated in the first divider because of the high frequency of the clock input and prevents the possibility of sneak pulses which would result in undesired states of the flip-flop. This action also assures that the two flip-flops maintain a 90-degree phase relationship.

Certain initial conditions are assumed in order to present a detailed discussion of the first binary divider (frequency divider). Assume that FF50010-50011 is in the reset state, as indicated in the waveforms of figure 4-54. The output of the set side (gate 50011) is a logic ZERO, which enables one leg of gate 50004. When the clock input is at the negative portion of its cycle, the second leg of gate 50004 is enabled. Gate 50009 inverts the input from gate 50002 to a logic ZERO and enables the third leg of gate 50004. Gate 50004 will now produce a logic ONE output and set FF50006-50007. The output of gate 50004 is fed forward to gate 50008. This prevents any output from gate 50008, which would set FF50010-50011. On the positive portion of the clock input, the output from gate 50004 becomes a logic ZERO and enables one leg of gate 50008. Gate 50002 also becomes a logic ZERO at this time and enables one leg of gate 50008. The remaining leg of gate 50008 is enabled by the logic ZERO output (reset side) from FF50006-50007. The output from gate 50008 is a logic ONE and sets FF50010-50011. During the next negative transition of the clock input, FF50006-50007 is reset by the output from gate 50005. Likewise, on the next positive portion of the clock input, FF50010-50011 is reset by the output from gate 50009. Thus, FF50006-50007 is alternately set and reset during negative transitions of the input clock pulse, and FF50010-50011 is alternately set and reset on positive transitions of the clock input. This results in the two flip-flop outputs being 90 degrees out of phase. The outputs from the first frequency divider, A1 through A4, are pulses of approximately 0.25 microsecond duration occurring at a rate of 1.024 mc. Outputs A1 - A3, and A2 - A4 occur in coincidence. The A1 output is inhibited by applying signal STPA or STPB to gate 50017. Both of these inputs are from the start-stop logic, and, when either is generated, the A1 output is blocked, which subsequently inhibits the time pulse generator. Signals A2 and A3 drive the second binary divider circuit of the clock countdown section.

Outputs Q1 and Q2 are generated from the two flip-flop outputs of the first binary divider circuit. Each of these outputs is a 1.024 mc train with a pulse width of 0.5 microsecond. Primarily, the Q1 and Q2 outputs are used to derive the 12 and 234 timing signals (figure 4-55) for read, write, and clear operations in the flip-flop registers of the central processor.

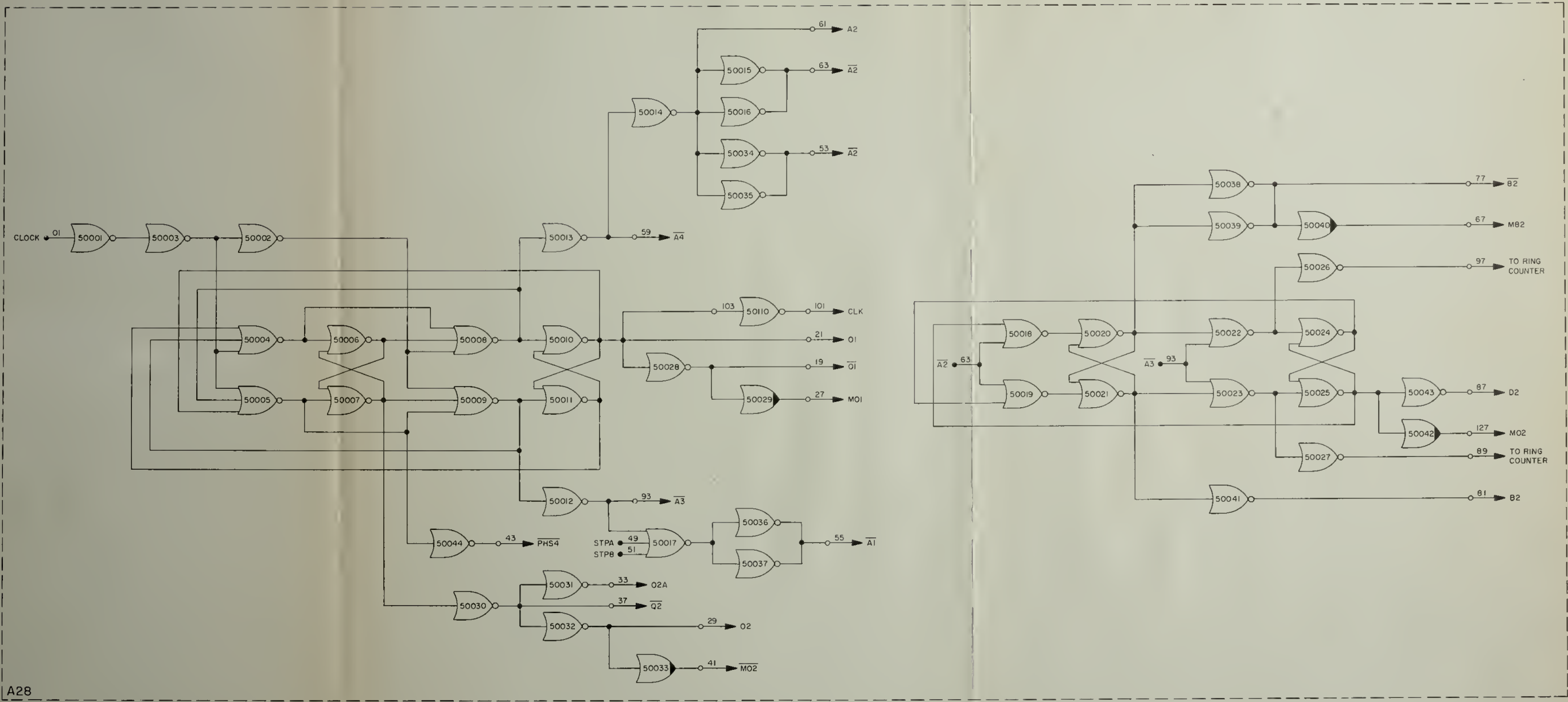
The second binary divider circuit (frequency divider) of the clock countdown section consists of FF50020-50021, FF50024-50025, and associated gates. This section accepts the two 1.024 mc outputs ( $A_2$  and  $A_3$ ) from the first divider and generates square wave outputs B2,  $\overline{B_2}$ , and D2 at a rate of 512 kc. Operation of the second divider circuit is identical to that of the first divider. The waveforms for the second divider are illustrated on figure 4-56.

The ring counter (figure 4-57) consists of five flip-flop circuits with outputs P01 through P05. The ring counter is driven by the 512 kc output from the second frequency divider. Outputs P01 through P05 are 5 microsecond pulses at a rate of 102.4 kc. Outputs occur 1 microsecond apart as shown in the waveforms of figure 4-58. The correct count sequence from the ring counter is established by forcing the counter into a particular mode. This is accomplished by allowing output P02 to be a logic ONE only if P01 and P05 are both logic ZERO's. Output P02 is a logic ZERO only if both P01 and P05 are logic ONE's. Strobe signals SB0, SB1, and SB2 (50204, 50203, and 50201) are 3 microsecond pulses at a rate of 102.4 kc as shown on figure 4-58. During the presence of strobe stop signal MSBSTP, these outputs are not produced.

4-8.1.9 Scaler A Detailed Description. Scaler A (figure 4-59) consists of 17 divider stages that generate output signals at rates from 51.2 kc to 0.78125 cps. The output rates from each stage are indicated in table 4-I. The input to stage 1 (P03, P05) is a 102.4 kc signal from the ring counter. Output FS01, which is applied to the second stage, is at a rate of 51.2 kc. The remaining stages are cascaded in a similar manner, which results in a division by two of the input from the previous stage. The output from stage 1 of scaler A is from the flip-flop only (FS01). The remaining stages have outputs in addition to the flip-flop outputs, which are designated, for example, F02A and F02B. The period and polarity of these outputs are indicated on table 4-I.

4-8.1.10 Scaler B Detailed Description. Scaler B (figure 4-60) consists of 16 identical divider stages, located on logic modules A1 through A16. The outputs from the last stage of scaler A (F17A, F17B) are applied to the first stage of scaler B. The stages are cascaded in a manner similar to those of scaler A so that each stage divides the input of the previous stage by two.

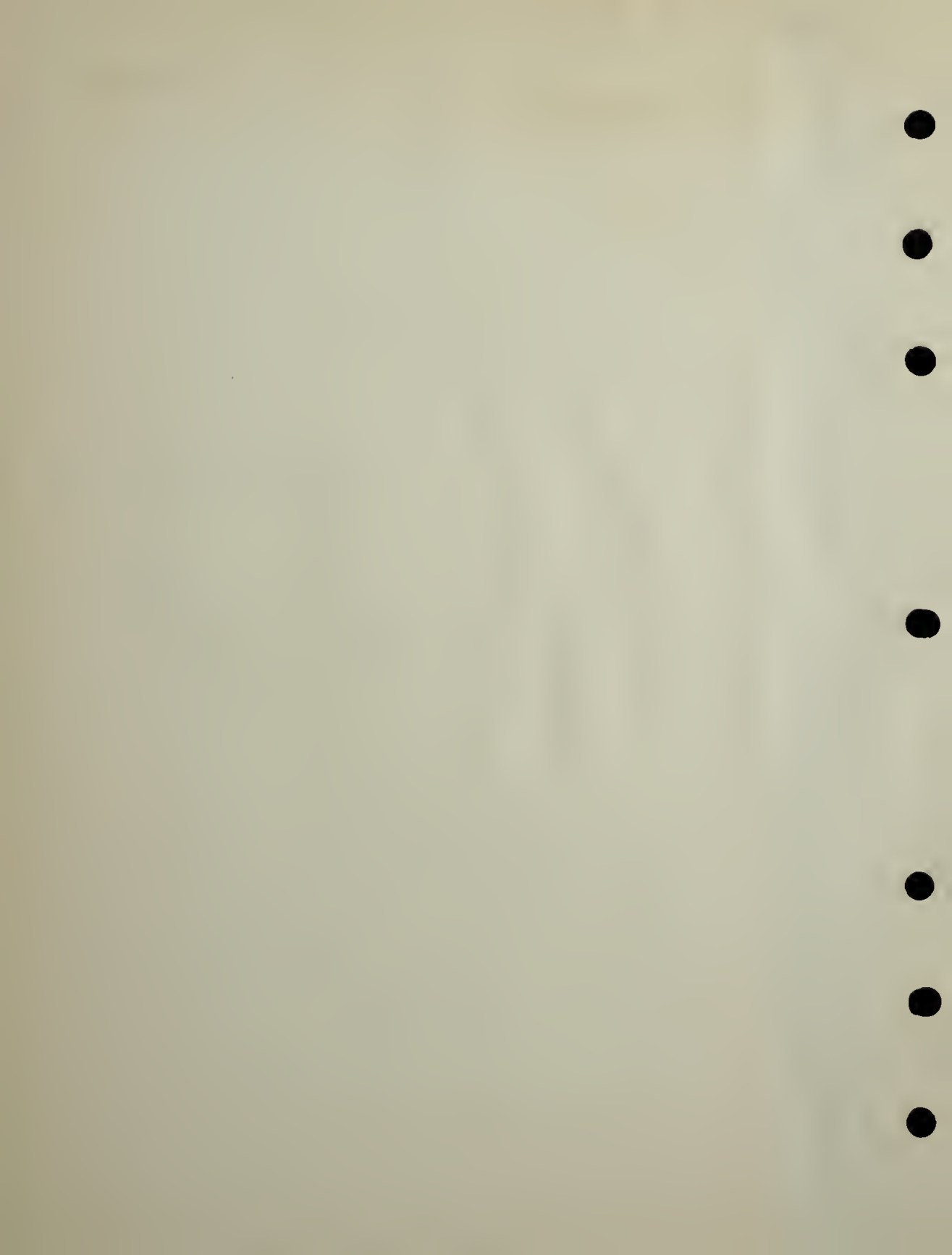
Scaler B is used to provide real time indication up to a maximum interval of 23.3 hours. Actually, all 16 stages comprise a 16 bit word which is applied to the TIME 1 and TIME 2 counters in erasable memory. This is accomplished by read signal RV1G. This signal is generated, under program control, and places the content of all 16 stages of scaler B on the write lines (WL01 - WL16) in the central processor. From the write lines the information updates the TIME counters in erasable memory.



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Figure 4-53. Binary Dividers



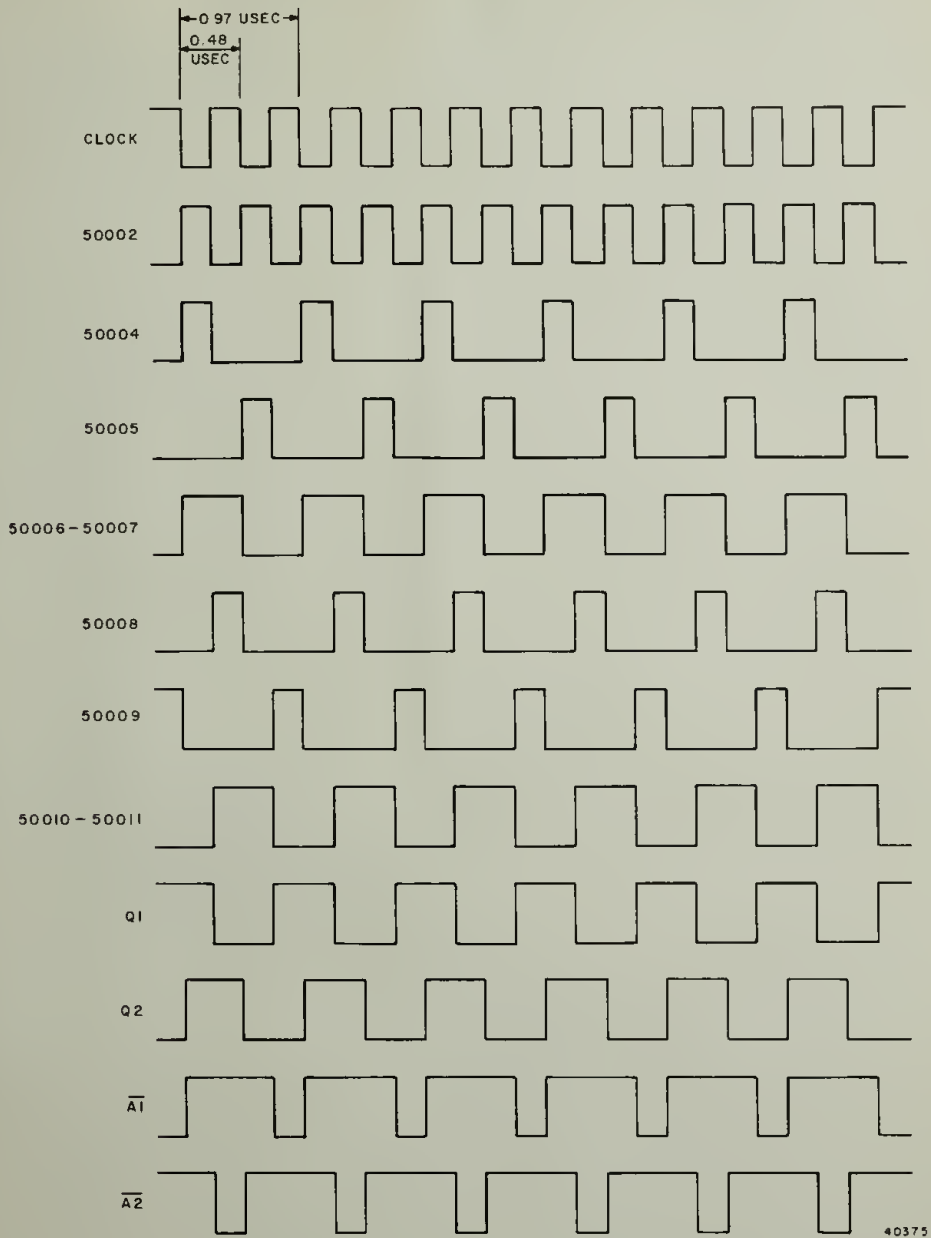


Figure 4-54. First Binary Divider Waveforms

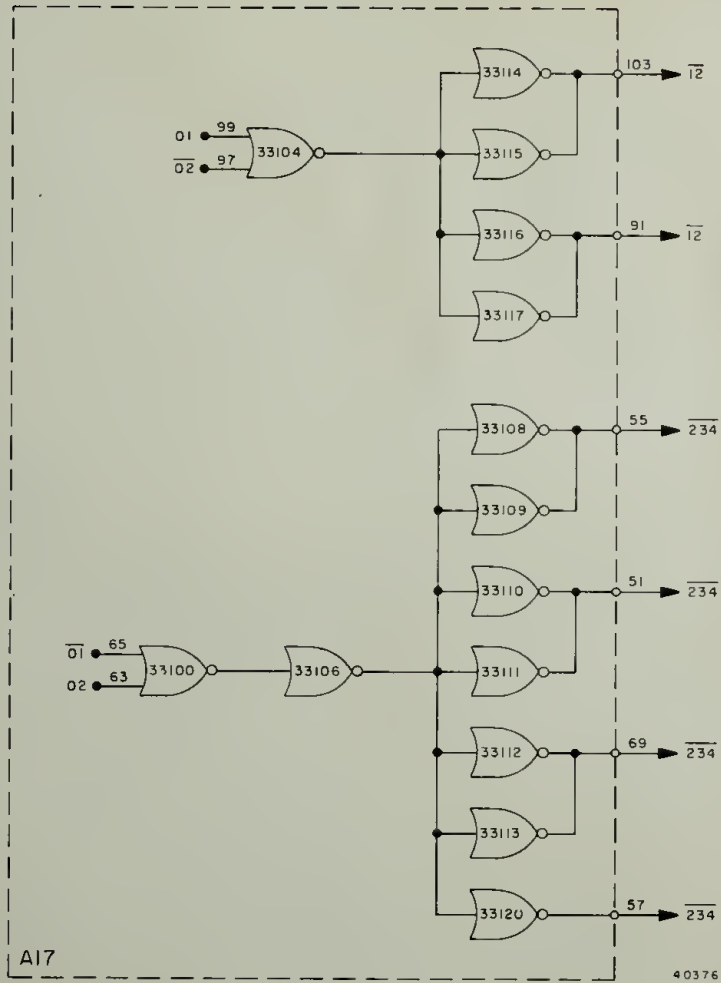
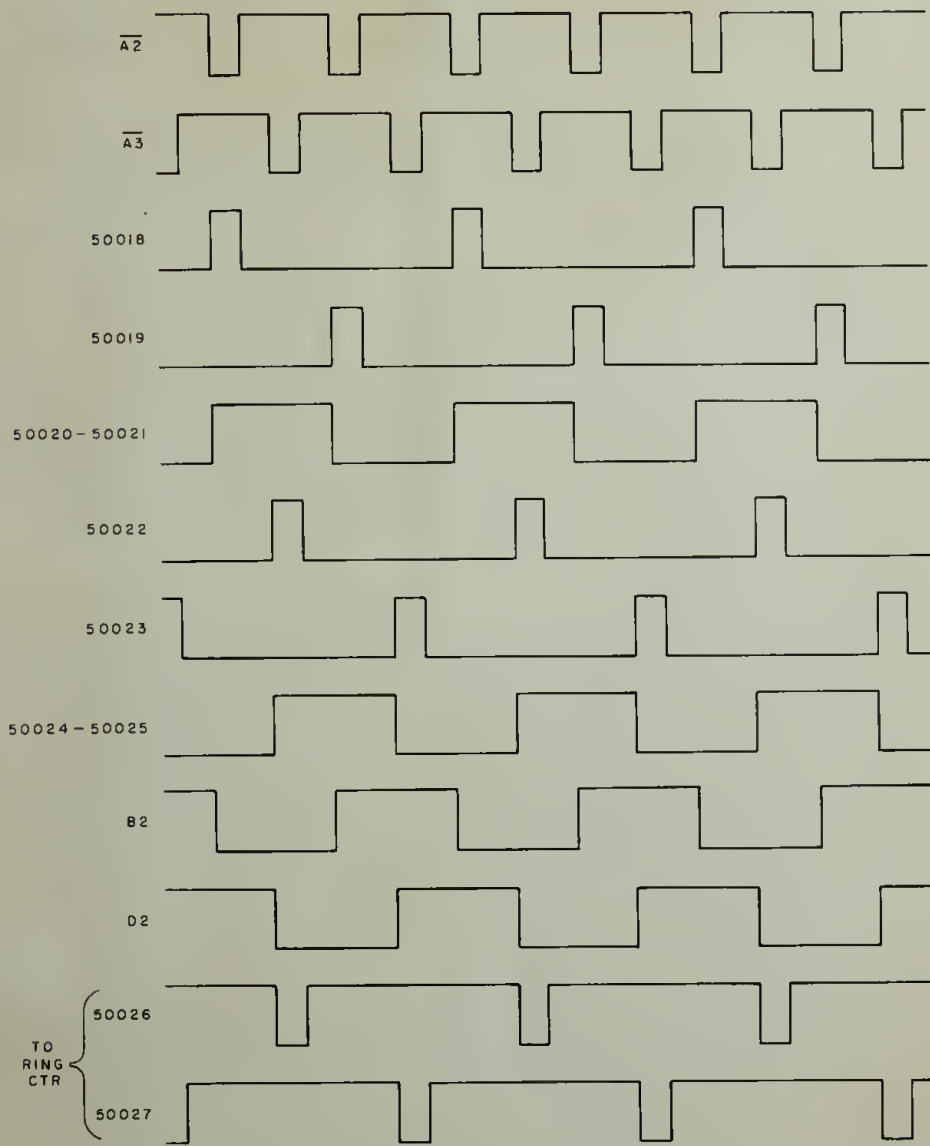


Figure 4-55. Read, Write, and Clear Timing Signals



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Figure 4-56. Second Binary Divider Waveforms



4-8.1.11 Time Pulse Generator Detailed Description. The time pulse generator (figure 4-61) produces timing pulse outputs  $\overline{T01}$  through  $\overline{T12}$ . This section contains a 2 phase, 4 bit gray code counter and decoder. The gray code counter contains primary and secondary level flip-flop storage and generates signals A through D and their complements. The primary level flip-flops generate the gray code of the next count in the timing sequence. The secondary level flip-flops store the gray code. Timing signals  $\overline{T01}$  through  $\overline{T12}$ , produced by the decoder, are used to generate the gray code of the next count in the timing sequence. Since the generation of each bit is identical, the explanation of only one bit and its complement is discussed.

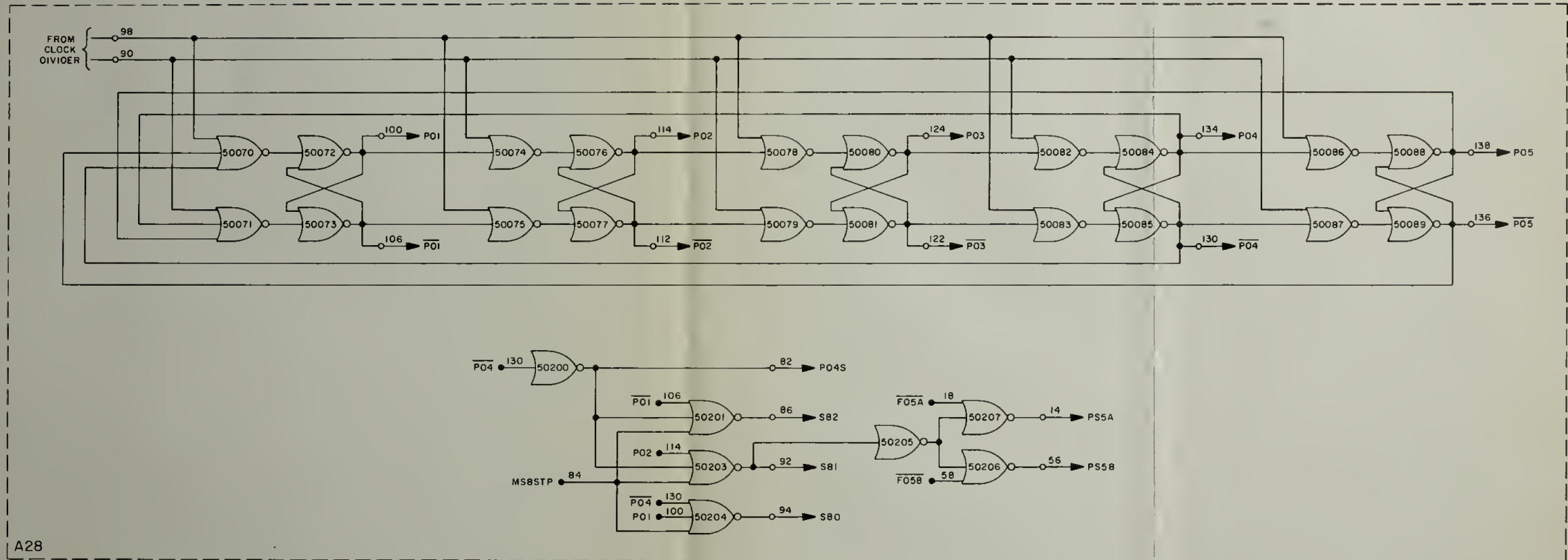
Primary level storage is formed by FF62003-62004 and its associated gates, 62001 and 62002. Secondary level storage is formed by FF62007-62008 and associated gates 62005 and 62006. Timing signals  $\overline{T01}$  through  $\overline{T12}$ , produced by the decoder, are applied to the control gates of the primary level flip-flops to generate the gray code of the next count in the timing sequence. The primary level flip-flops are conditioned by these signals such that the state of one and only one flip-flop responds to gating signal  $\overline{A2}$ . For example: FF62003-62004 can be set only if timing pulse  $\overline{T06}$  and gating signal  $\overline{A2}$  are simultaneously applied to gate 62001. The flip-flop is reset only if signals  $\overline{T10}$  and  $\overline{A2}$  are simultaneously applied to gate 62002. The gray code output from the primary level flip-flops is applied to the control gates of the secondary level flip-flops and entered into storage by gating signal  $\overline{A1}$ .

The output of the secondary level flip-flops is applied to the decoder, which generates outputs  $\overline{T01}$  through  $\overline{T12}$ . Each time the decoder generates a timing pulse, the gray code count advances by one. This operation continues with the counter advancing one state at a time through the count sequence shown in figure 4-61 until it returns to the initial state 0000.

As long as gating signals  $\overline{A1}$  and  $\overline{A2}$  are present and neither level of flip-flops is inhibited, the counter will continue to advance and maintain itself within the permissible states. However, when power is first applied to the counter, the counter may not be in a state which is part of the count sequence. The illegal states of the count sequence are ABCD, ABC $\overline{D}$ , A $\overline{B}$ CD, A $\overline{B}$ C $\overline{D}$  (states 0111, 1110, 1011, and 1010). These four states are reduced to the logic condition AC. Gate 62021 produces an output only when the logic condition AC exists. The purpose of gate 62021 is to reset FF62022-62023, which changes signal C to a logic ZERO and forces the counter into a legal state.

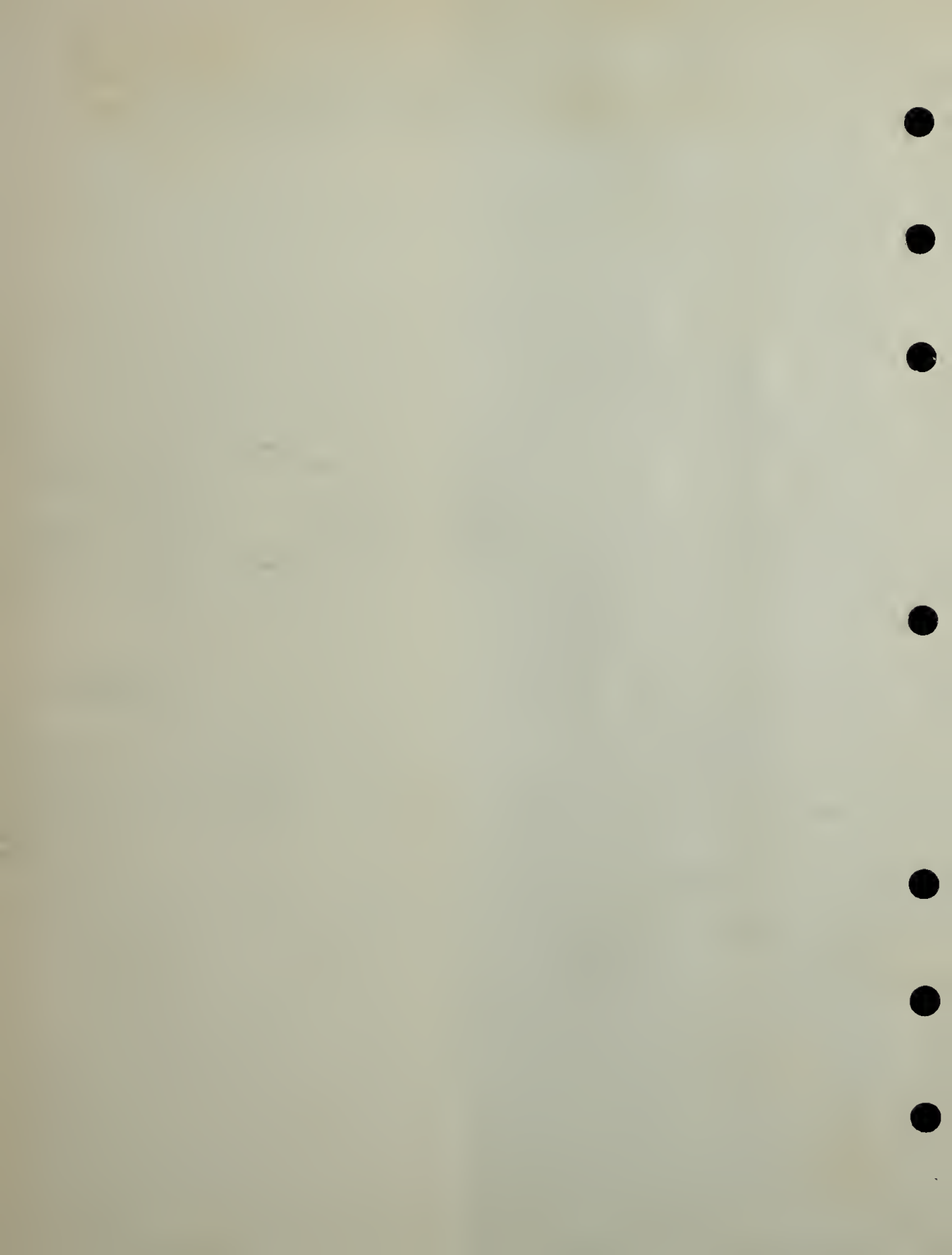
The count sequence may be interrupted by inhibiting either level of flip-flops. In the AGC the secondary level is inhibited by blocking the  $\overline{A1}$  input from the first binary divider. This prevents the primary level flip-flops from changing state and therefore halts the advance of the counter. The counter may be stopped at any time; however, the AGC demands that the counter not be stopped except at time 12.

4-8.1.12 Start-Stop Logic Detailed Description. The start-stop logic (figure 4-62) generates signals STPA, STPB, and GOJAM. Signal STPA, generated by FF50313-50314, and signal STPB, generated by FF51307-51308, are applied to the first binary divider of the clock countdown circuit (figure 4-53) and inhibit the  $\overline{A1}$  output, which subsequently inhibits timing pulse outputs  $\overline{T01}$  through  $\overline{T12}$ . This action prevents any



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Figure 4-57. Ring Counter Logic



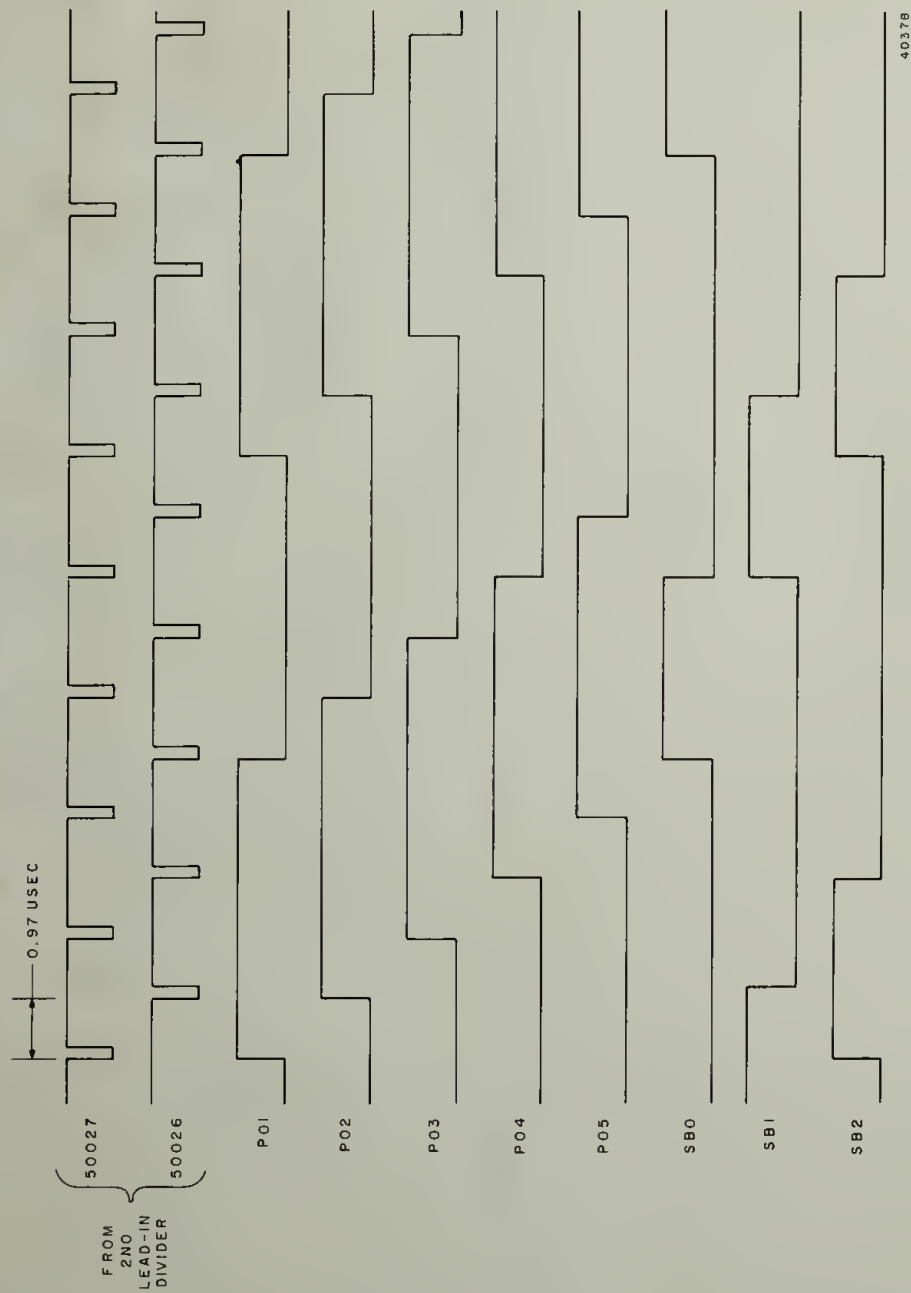


Figure 4-58. Ring Counter Waveforms

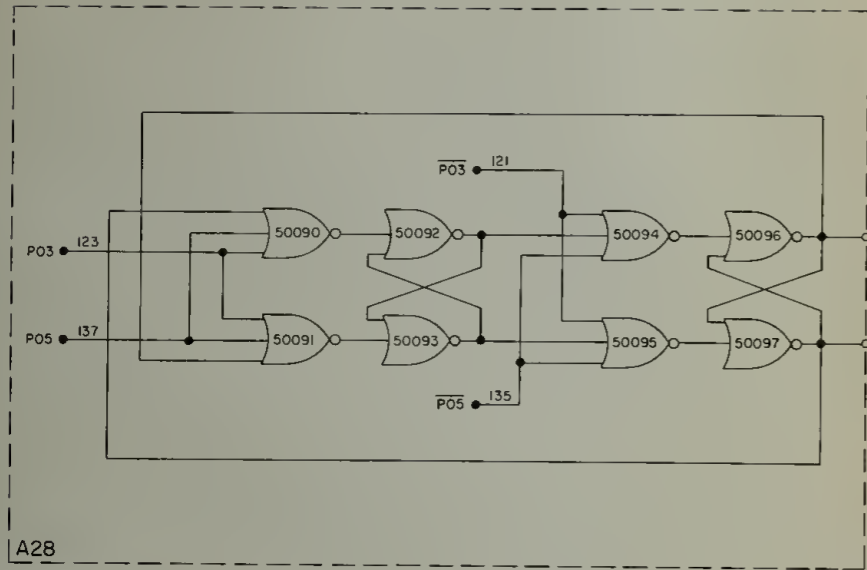
word flow within the AGC. A monitor stop command (MSTP) from the CTS coincident with  $\overline{T12}$  causes signal STPA to be generated and stops the time pulse generator. The time pulse generator resumes its normal sequence when the monitor stop command is removed. A monitor start command (MSTRT) from the CTS or an alarm condition (ALGA) coincident with  $\overline{T12}$  causes signal STPB to be generated by FF51307-51308. Signal STPB in turn causes signal GOJAM. This is essentially a clear signal within the AGC which inhibits access to memory, clears the output registers, clears the RUPT priority flip-flops, and generates a GO condition in the sequence generator. Input STRT2 indicates a power failure and has the same effect as the alarm input.

4-8.2 SEQUENCE GENERATOR. The sequence generator (figure 4-63) executes machine instructions and is divided into six sections: interrupt service, SQ register and decoder, state counter and decoder, instruction decoder, control pulse generator, and branching control. Each machine instruction is defined by an order code. When executing a program, the instruction is transferred into the central processor, usually register B. At the request of the sequence generator, the order code is entered into register SQ. The input is decoded, and, in conjunction with the subinstruction code from the state counter, it is applied to the instruction decoder, producing subinstruction commands. The subinstruction commands in turn produce control pulses from the control pulse generator which cause the execution of an instruction.

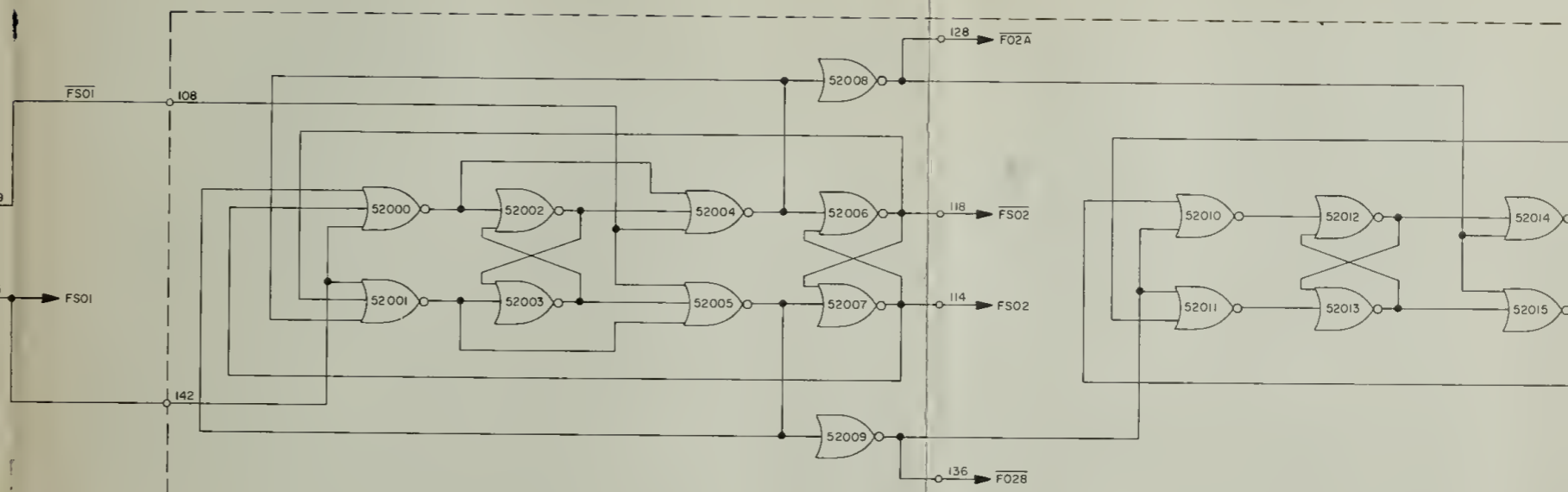
4-8.2.1 Interrupt Service Functional Description. The interrupt service (figure 4-63) controls the order code in register SQ and decoder and the subinstruction code in the state counter and decoder. The order code is either the prior contents of central processor register B or a forced order code generated by sequence generator operation. The subinstruction code designates particular subinstructions.

Each subinstruction is defined by a 4 bit order code and a 2 bit subinstruction code. The order codes and subinstruction codes for the subinstructions are listed in table 4-II. The condition of signal INKL, the SQ decoder outputs, and the state decoder outputs for the subinstructions are listed also. The SQ decoder and state decoder outputs are functions of the order and subinstruction codes. The subinstruction ST code, listed in table 4-II, is a binary-coded octal representation of the order code and subinstruction code. The subinstruction CCS code describes the SQ decoder outputs and state decoder outputs. Derivation of the subinstruction ST and CCS codes is shown on figure 4-64.

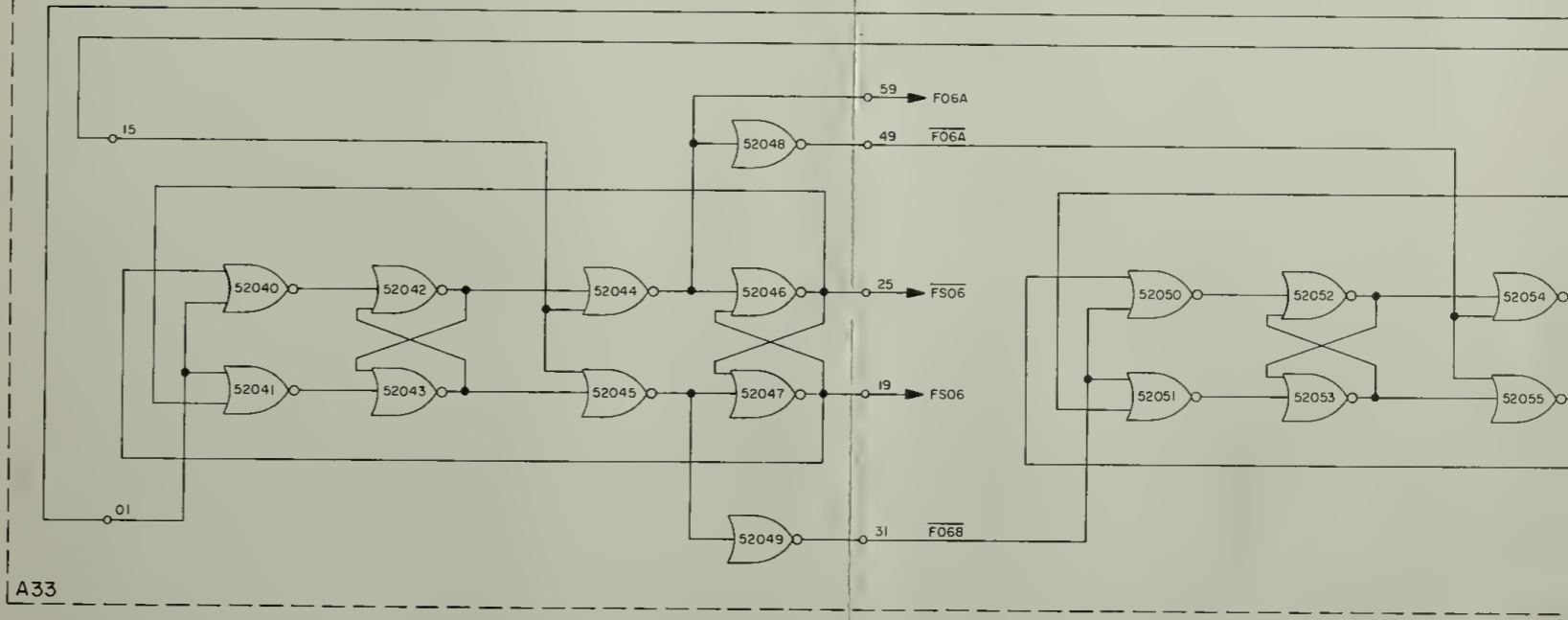
A subinstruction code is generated by signals applied to the primary level state flip-flops. Outputs from these flip-flops are supplied to the secondary level flip-flops through the state transfer gate in the state counter and decoder. The state transfer gate is controlled by the subinstruction code transfer inhibit flip-flop and the increment inhibit gate. If priority control signals a counter increment operation with signal INKL, the subinstruction code transfer inhibit flip-flop is set at time 8. This flip-flop inhibits the subinstruction code transfer through the state transfer gate at time 12. The inhibiting action is prevented if interrupt signal MTCSAI or GOJAM is present at the increment inhibit gate. The subinstruction code for RUPT1, MTCSAI, or GOJAM is then supplied to the secondary level state flip-flops and processed after the counter increment action.



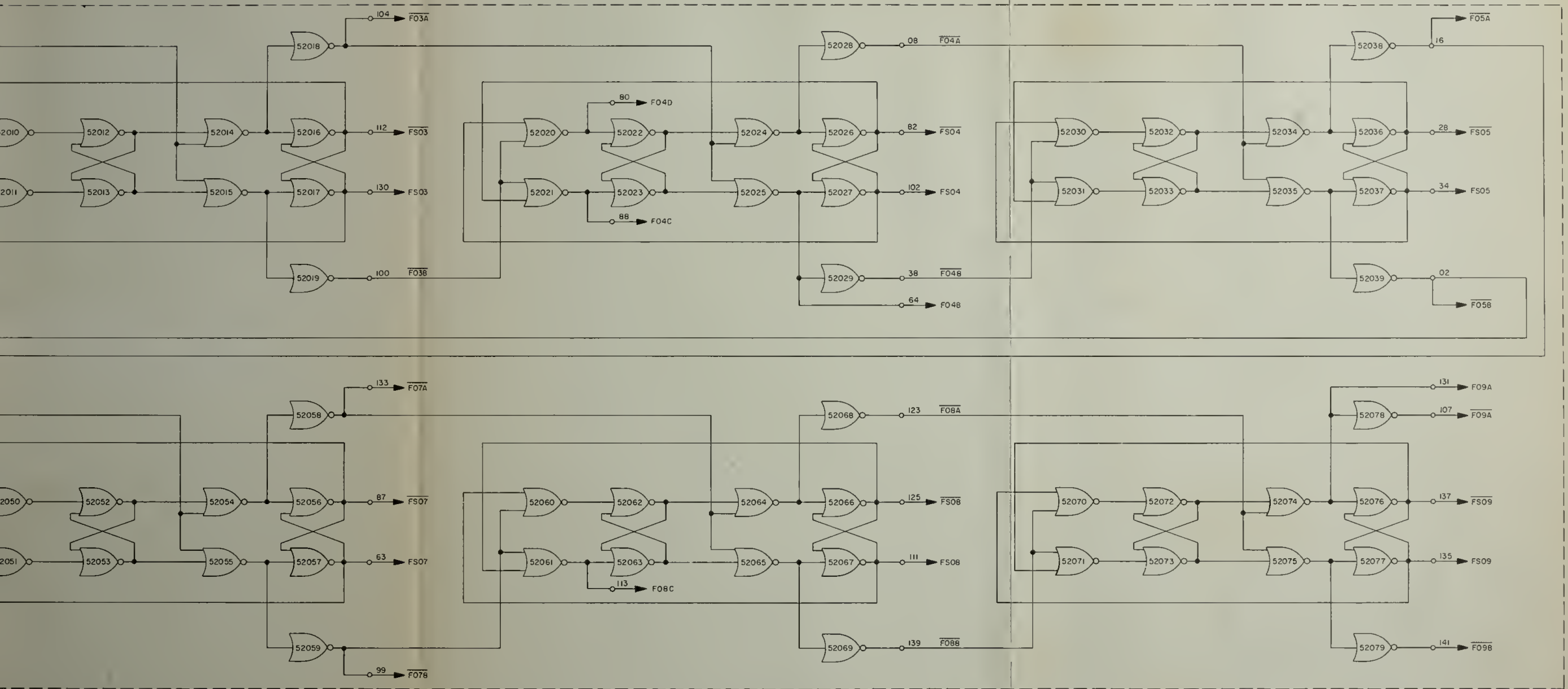
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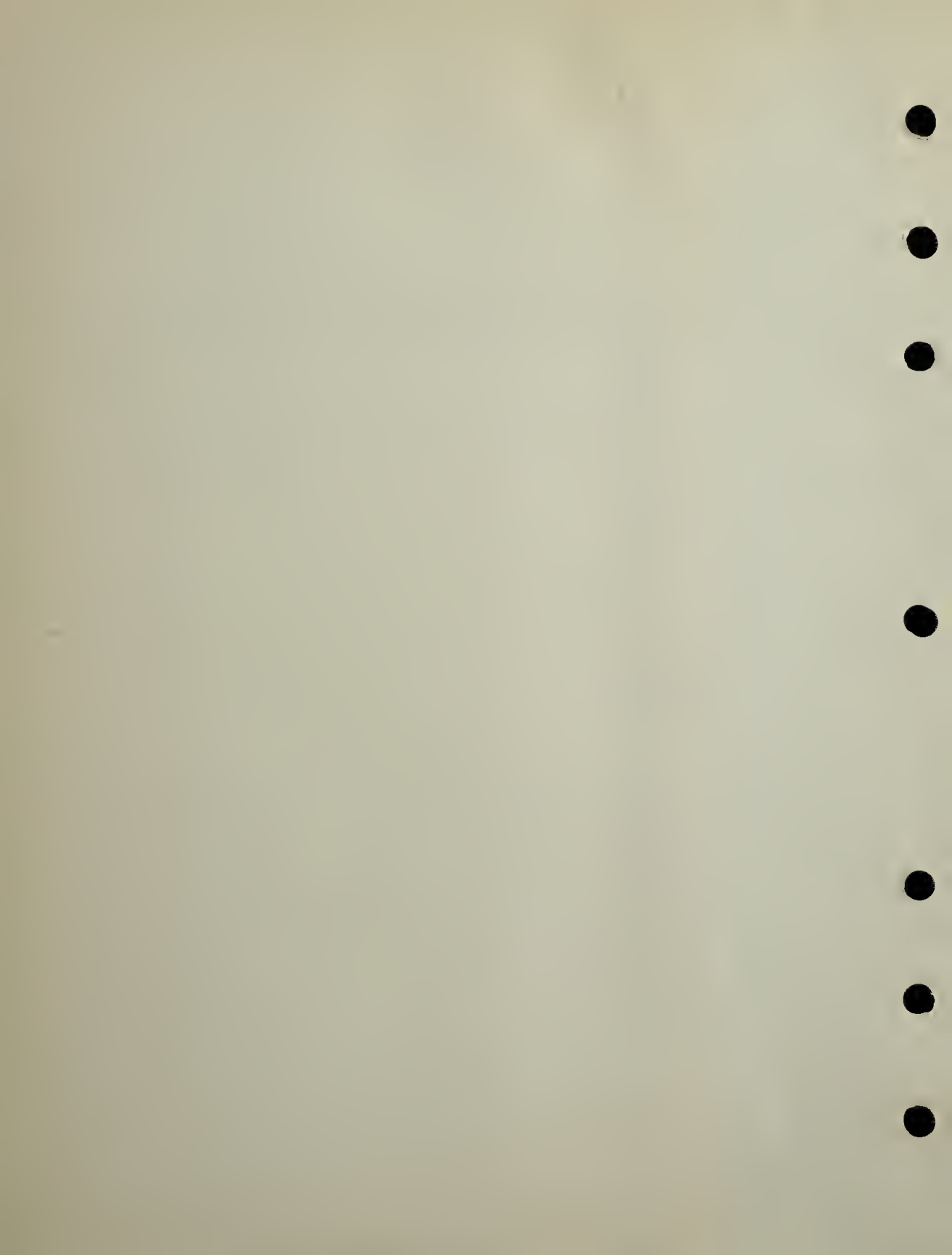


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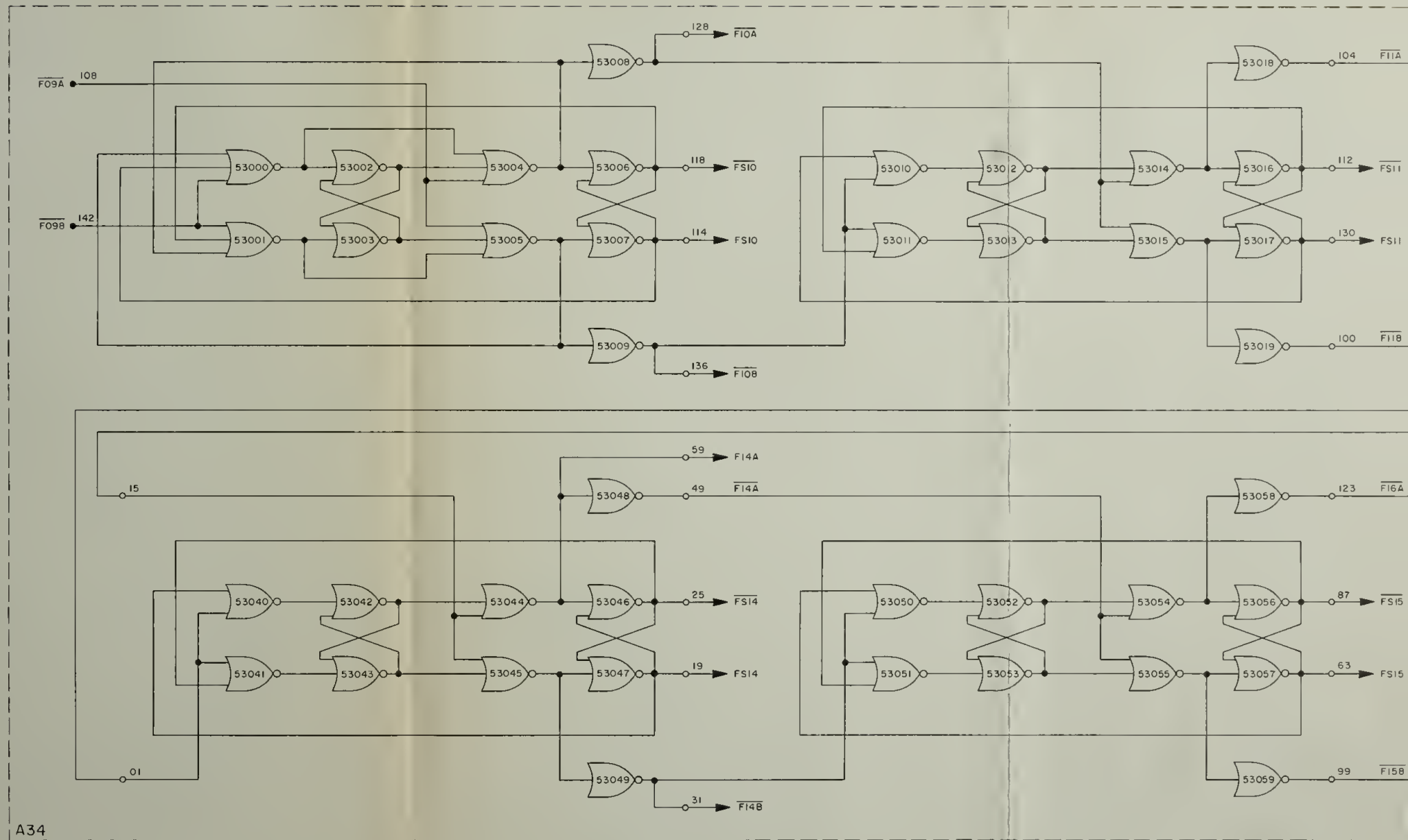


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Figure 4-59. Scaler A (Sheet 1 of 2)

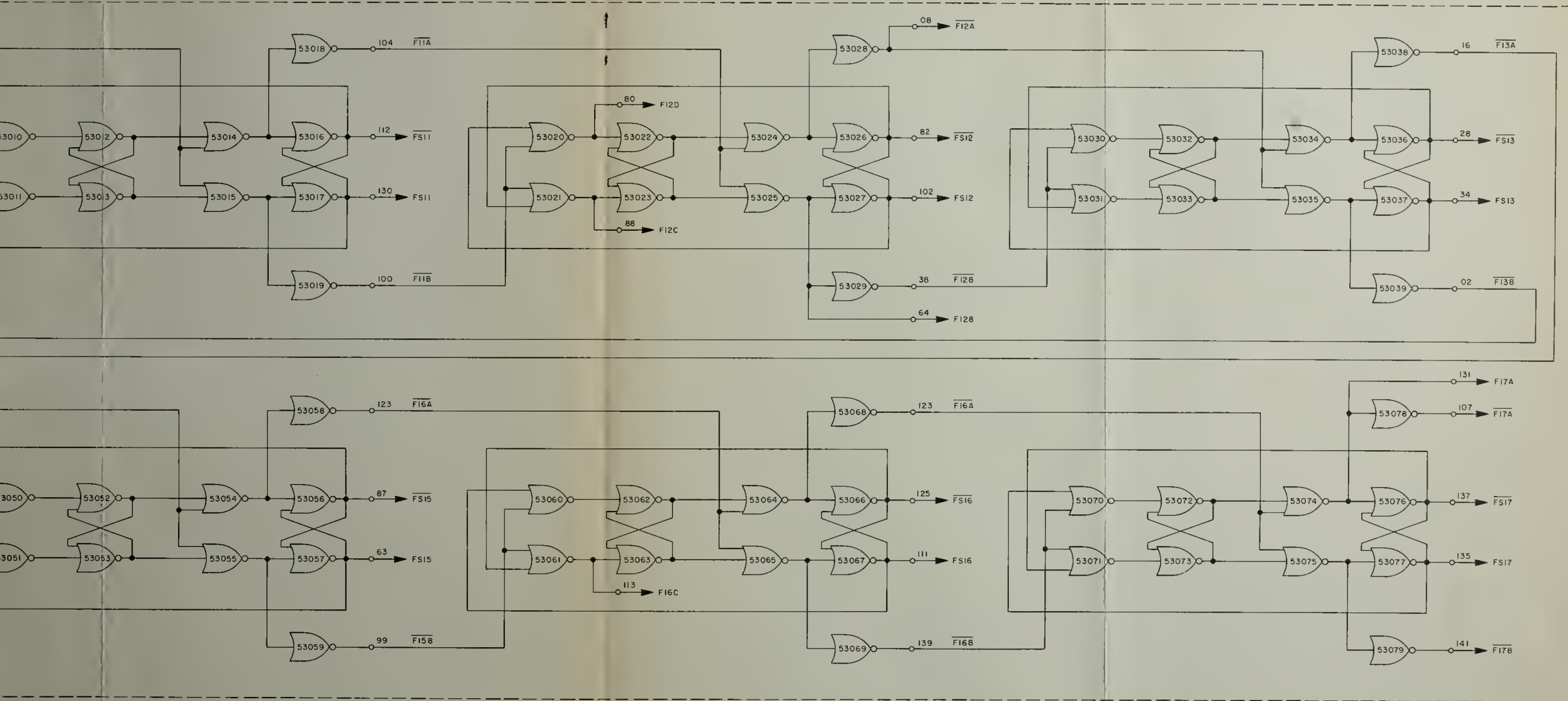






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Figure 4-59. Scaler A (Sheet 2 of 2)

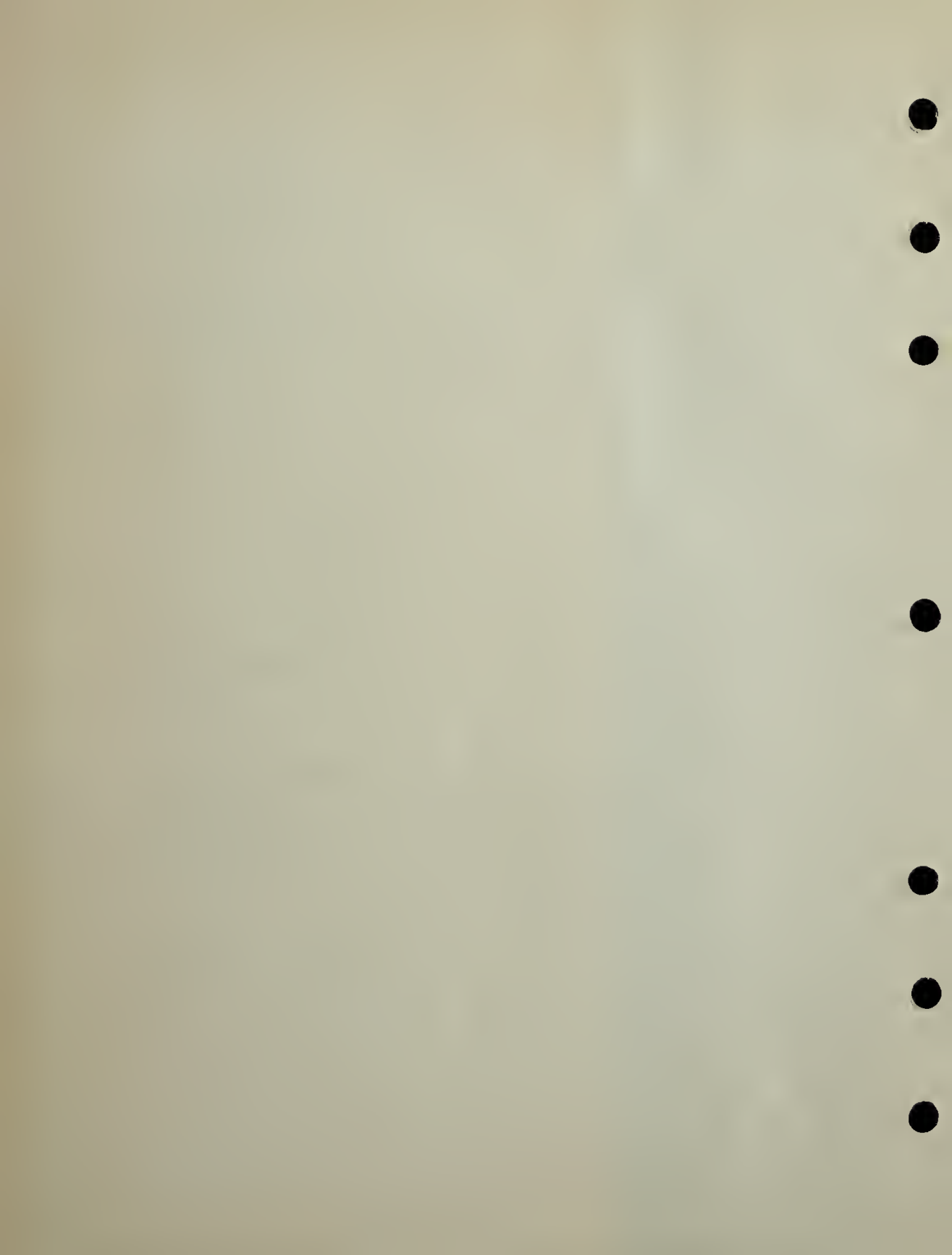


Table 4-I. Scaler A Outputs

Output	Frequency	Period	Polarity
FS01, FS01	51.2 kpps	19.5 μsec	
FS02, FS02 *F02A, F02B	25.6 kpps	39.1 μsec	Negative
FS03, FS03 *F03A, F03B	12.8 kpps	78.0 μsec	Negative
FS04, FS04 *F04A, F04B F04B *F04C, F04D	6.4 kpps	156.0 μsec	Negative Positive
FS05, FS05 *F05A, F05B	3.2 kpps	312.0 μsec	Negative
FS06, FS06 F06A *F06A, F06B	1.6 kpps	624.0 μsec	Positive Negative
FS07, FS07 *F07A, F07B	800.0 pps	1.25 msec	Negative
FS08, FS08 F08A, F08C F08C	400.0 pps	2.5 msec	Negative Positive
FS09, FS09 *F09A *F09A, F09B	200.0 pps	5.0 msec	Positive Negative
FS10, FS10 *F10A, F10B	100.0 pps	10.0 msec	Negative
FS11, FS11 *F11A, F11B	50.0 pps	20.0 msec	Negative
FS12, FS12 *F12A, F12B *F12B, F12C, F12D	25.0 pps	40.0 msec	Negative Positive
FS13, FS13 *F13A, F13B	12.5 pps	80.0 msec	Negative
FS14, FS14 *F14A F14A, F14B	6.25 pps	160.0 msec	Positive Negative
FS15, FS15 F15A, F15B	3.125 pps	320.0 msec	Negative
FS16, FS16 *F16A, F16B	1.5625 pps	640.0 msec	Negative
FS17, FS17 *F17A *F17A, F17B	0.78125 pps	1.3 sec	Positive Negative

\*Pulse outputs are 10-μsec wide.

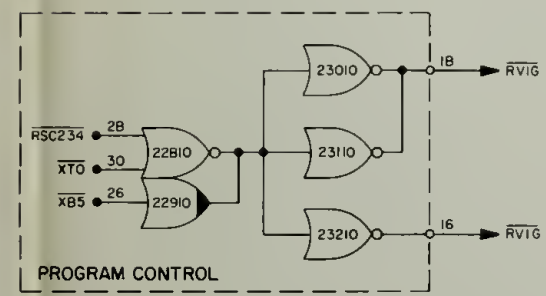
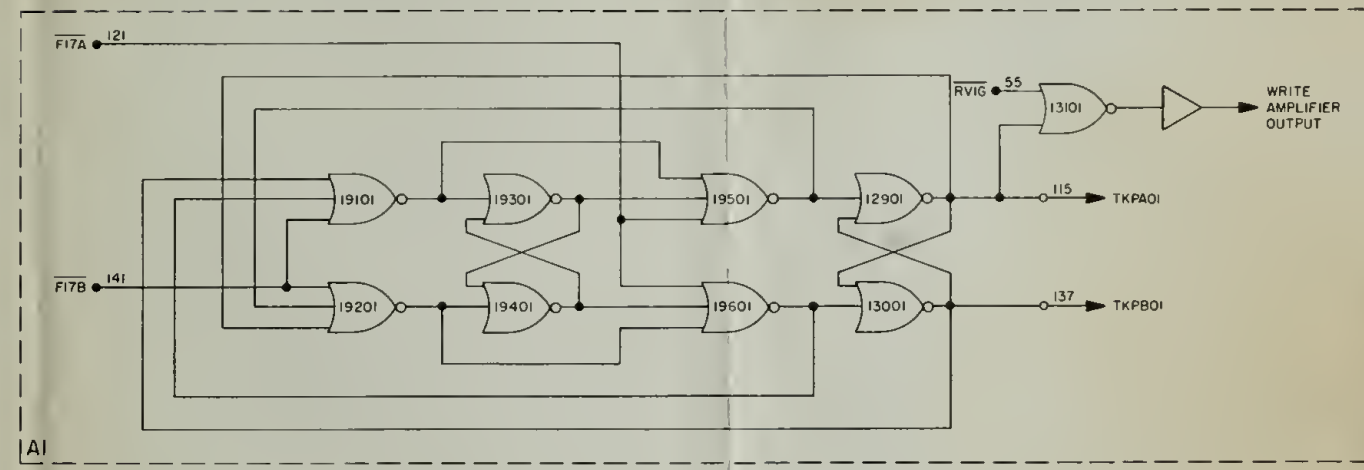
A request for a new order code is initiated by control pulse NISQ. Pulse NISQ is generated by the control pulse generator at time 11 of the last subinstruction of a machine instruction. NISQ sets the new instruction flip-flop, which resets at the following time 4. The new instruction request output is supplied to the OVF/UNF interrupt inhibit flip-flop, the interrupt inhibit gate, the SQ clear gate, and the SQ read/write gates. This input to the OVF/UNF inhibit flip-flop and the interrupt inhibit gate is applicable to interrupt operations. The SQ clear gate produces a clear signal (CSQG) for register SQ at time 12. Also, at time 12 the SQ read/write gate produces two write signals and a read register B signal (RBQ). The order code is read out of register B, and write amplifier outputs WL13 through WL16 are supplied to register SQ: WL13 and WL14 through the order code transfer gate and WL15 and WL16 directly. The SQ clear gate and the SQ read/write gates are also controlled by start signals GOJAM and MTCSAI and by the interrupt signal. GOJAM controls the clear and write signals so that order code 0000 is set in register SQ. Signal MTCSAI also sets the order code to 0000 and causes a subinstruction code of 11; GOJAM causes a subinstruction code of 01.

The interrupt signal is the output of the interrupt inhibit gate and signals instruction RUPT. The interrupt signal controls the SQ clear gate, SQ read/write gates, and order code transfer gates to obtain the order code for subinstruction RUPT1 (the first subinstruction of instruction RUPT). The interrupt signal also obtains subinstruction code 01 for subinstruction RUPT1. To obtain 01, the interrupt signal sets the least significant digit (LSD) primary level state flip-flop. The ST1 and ST2 signals from the control pulse generator adjust the subinstruction code as required during changes of subinstructions within a machine instruction. Subinstructions RSM and MP3 both require a subinstruction code of 11, and both have detection gates to set the most significant digit (MSD) primary level state flip-flop. The detection gates are the RSM gate and the multiply CTR gate. The LSD primary level state flip-flop is set by control pulse ST1 for subinstructions RSM and MP3. The subinstruction code output from the primary level state flip-flops and signal INKL are inputs to the state decoder.

Signal GOJAM, the request for instruction GO, sets the order code to 0000 and the subinstruction code to 01. Signal GOJAM is applied to the SQ clear gate and the SQ read/write gates. Signal CSQG is generated and register SQ is cleared at time 12. Simultaneously, write signals WSQF and WSGQ are inhibited. Clearing register SQ and the inhibiting and write inputs set the order code to 0000. Again, signal GOJAM is sent to the first state of the LSD primary level state flip-flop to set the subinstruction code to 01. The AGC then accomplishes instruction GO.

Signal GOJAM inhibits signals MTCSAI and  $\overline{\text{RUPTOR}}$ , resets the interrupt-in-progress flip-flop and the inhint/relint flip-flop, and then inhibits the memory control signal (MC) command in the instruction decoder. These actions are necessary to obtain a new start within the AGC. Effectively, all requests and priorities are removed and the sequence generator is cleared. Signal MTCSAI sets the order code to 0000 and the subinstruction code to 11. This order code and subinstruction code are for instruction TCSA, which is then executed. Signal MTCSAI inhibits generation of  $\overline{\text{RUPTOR}}$  and overrides the INKL action of inhibiting the subinstruction code transfer. Therefore, MTCSAI has priority over program interruptions, and TCSA is performed after any counter increment operation.

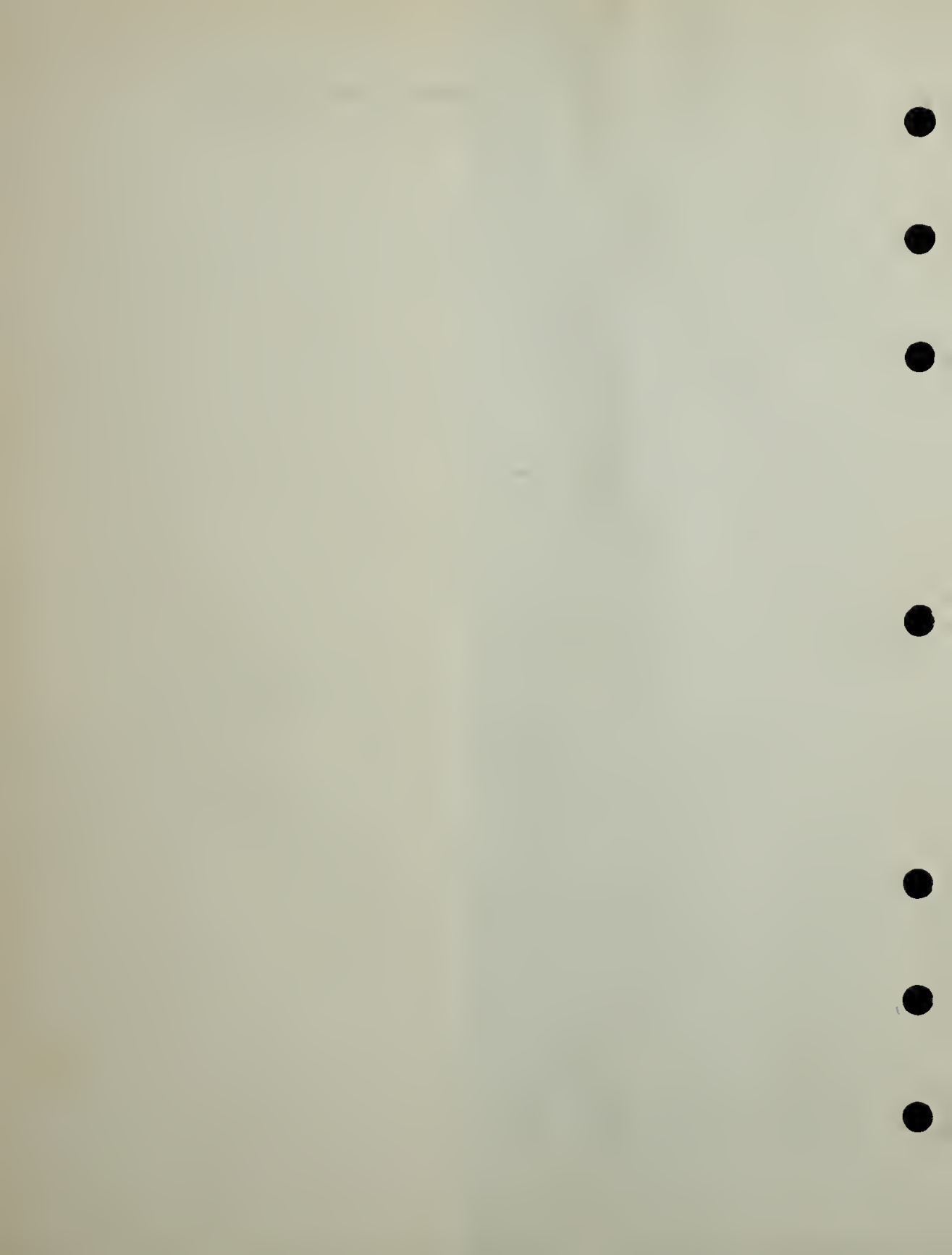
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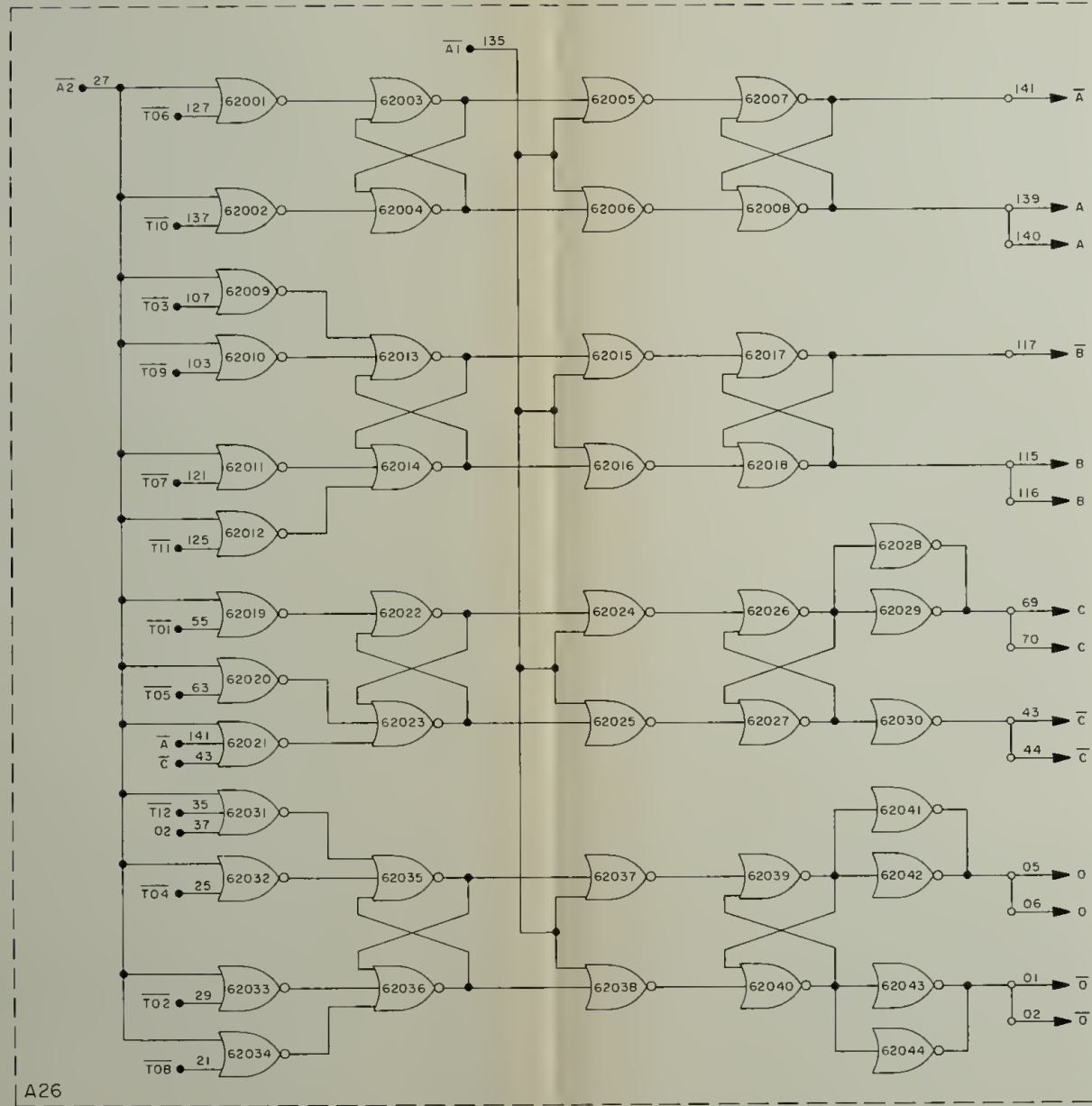


PIN NO MODULE	INPUT		OUTPUT		REAO
	I21	I41	I115	I137	55
A 1	F17A	F17B	TKPA01	TKPB01	RVIG
A 2	TKPA01	TKPB01	TKPA02	TKPB02	RVIG
A 3	TKPA02	TKPB02	TKPA03	TKPB03	RVIG
A 4	TKPA03	TKPB03	TKPA04	TKPB04	RVIG
A 5	TKPA04	TKPB04	TKPA05	TKPB05	RVIG
A 6	TKPA05	TKPB05	TKPA06	TKPB06	RVIG
A 7	TKPA06	TKPB06	TKPA07	TKPB07	RVIG
A 8	TKPA07	TKPB07	TKPA08	TKPB08	RVIG
A 9	TKPA08	TKPB08	TKPA09	TKPB09	RVIG
A10	TKPA09	TKPB09	TKPA10	TKPB10	RVIG
A11	TKPA10	TKPB10	TKPA11	TKPB11	RVIG
A12	TKPA11	TKPB11	TKPA12	TKPB12	RVIG
A13	TKPA12	TKPB12	TKPA13	TKPB13	RVIG
A14	TKPA13	TKPB13	TKPA14	TKPB14	RVIG
A15	TKPA14	TKPB14	TKPA15	TKPB15	RVIG
A16	TKPA15	TKPB15	TKPA16	TKPB16	RVIG

40380A

Figure 4-60. Scaler B

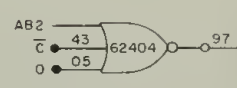
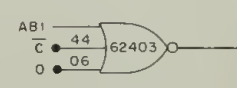
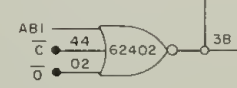
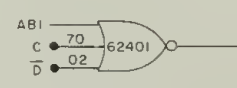
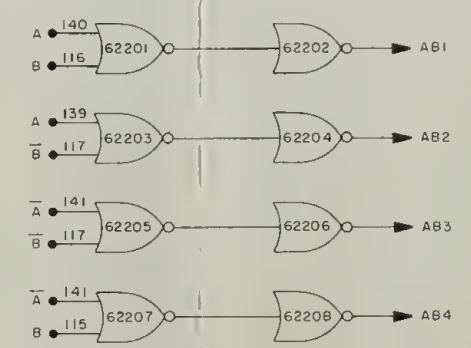




A26

AB	00	01	11	10
00	12	1	10	9
01	1	6	7	8
11	2	5		
10	3	4		

COUNT SEQUENCE



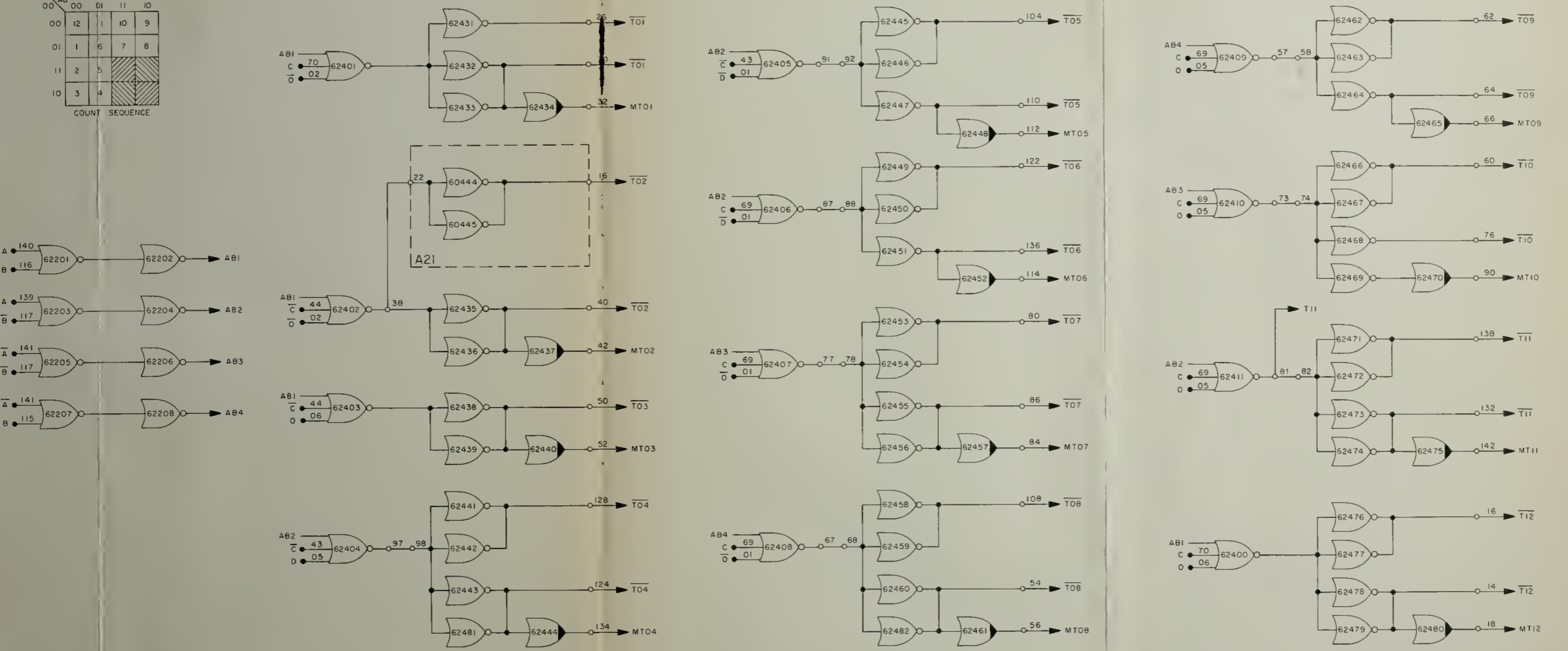
3B

97



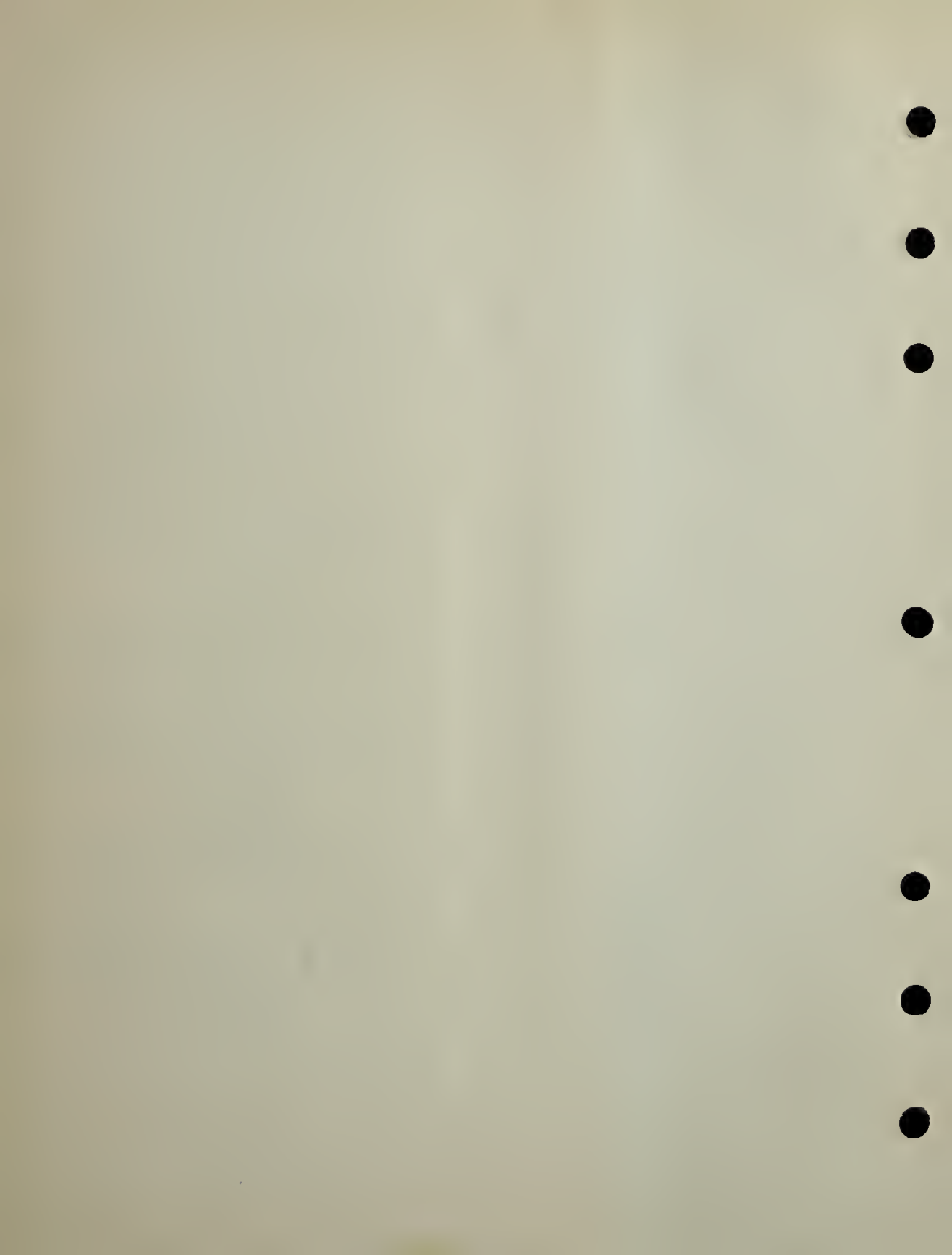
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AB	00	01	11	10
00	12	1	10	9
01	1	6	7	8
11	2	5		
10	3	4		
	COUNT		SEQUENCE	



40381

Figure 4-61. Time Pulse Generator



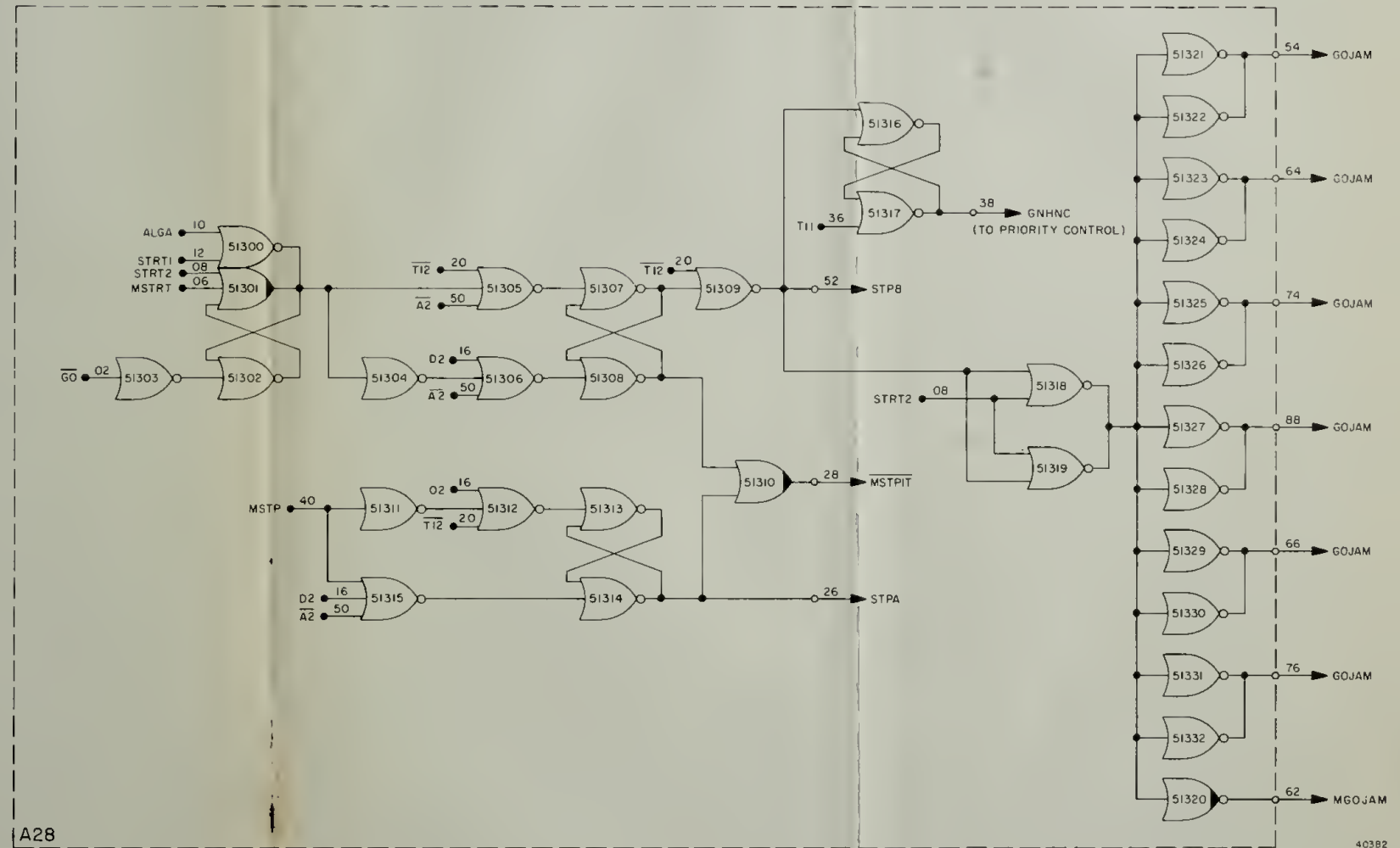
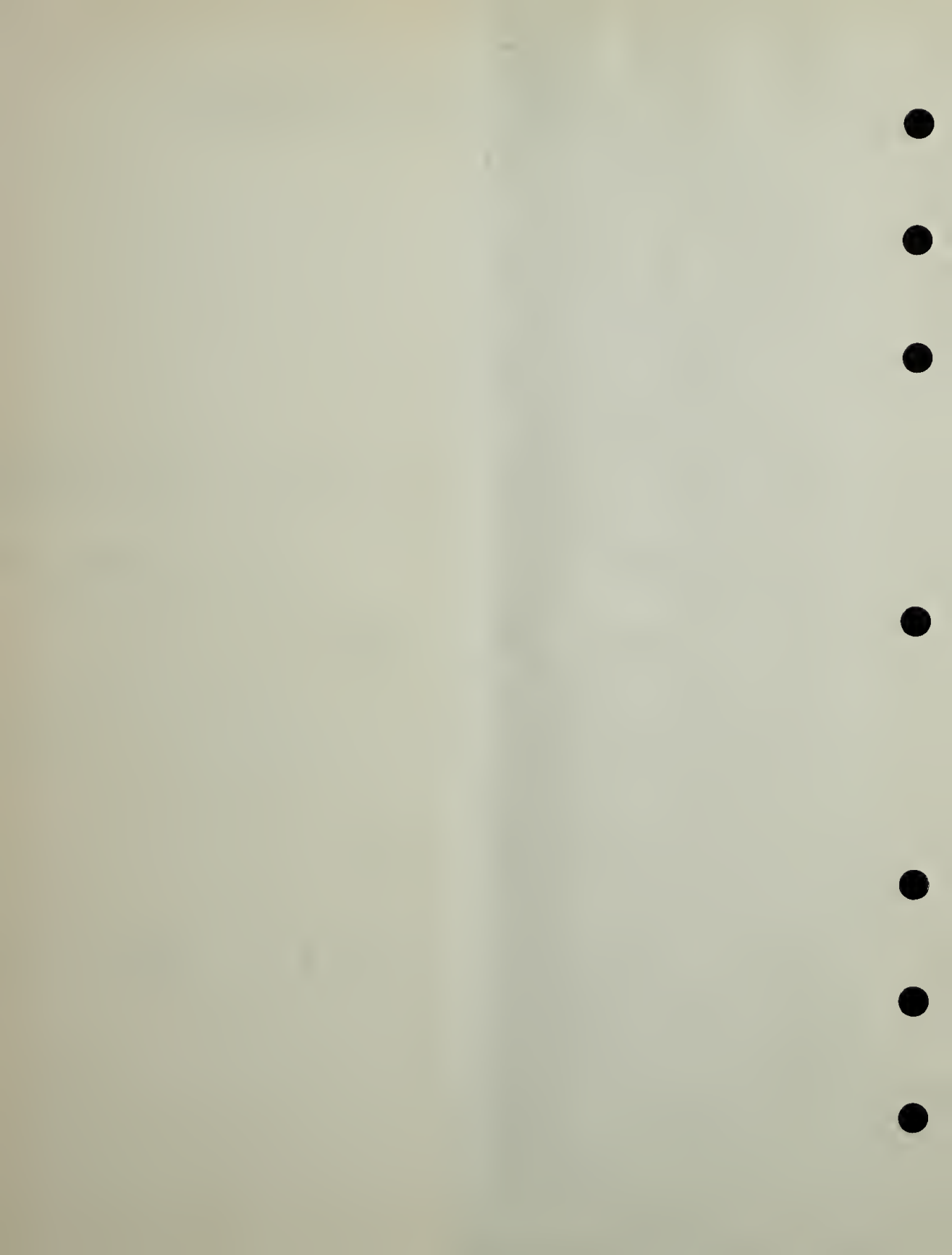
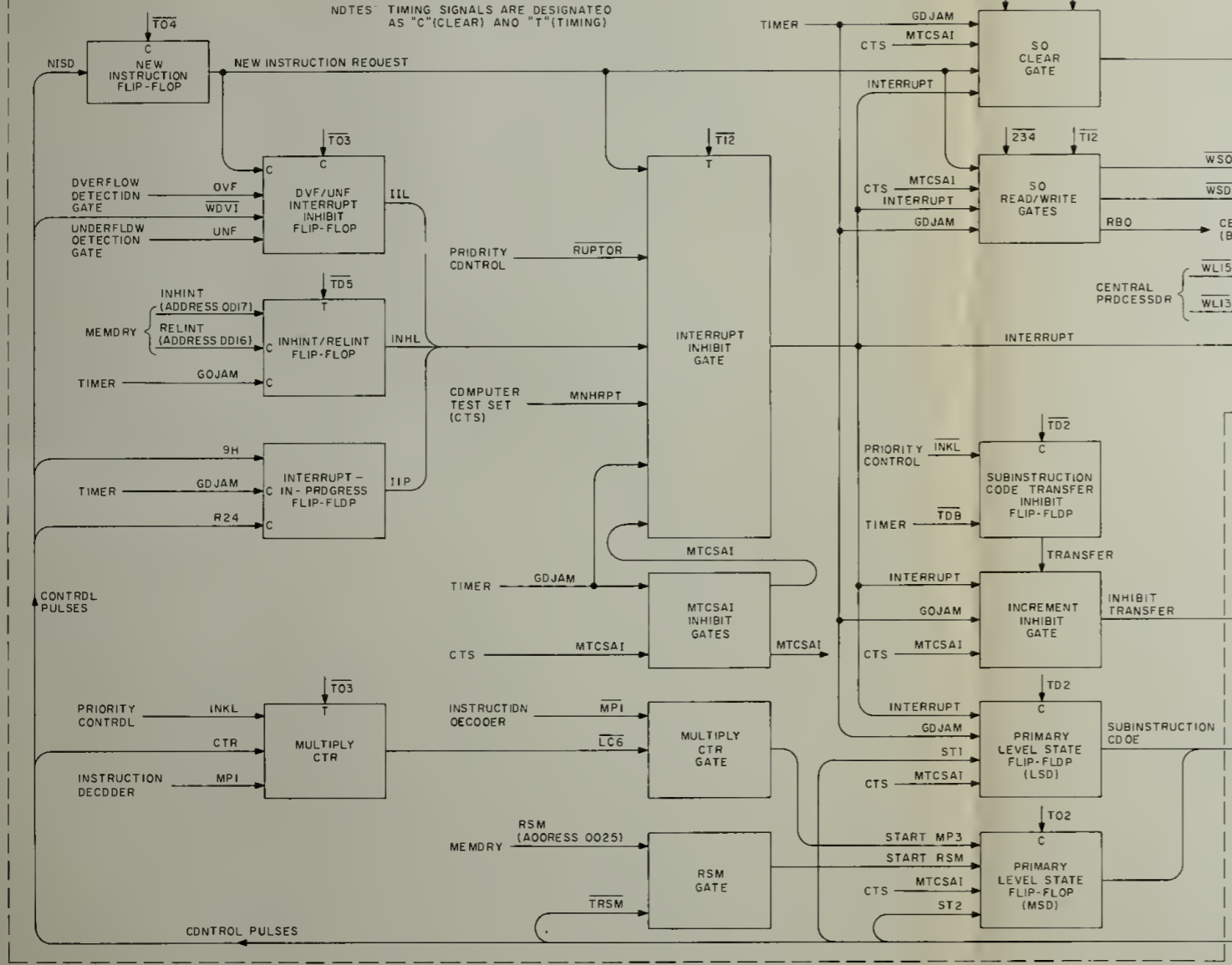


Figure 4-62. Start-Stop Logic



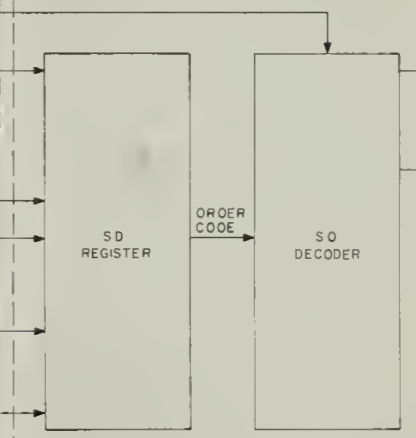
# INTERRUPT SERVICE

NOTES: TIMING SIGNALS ARE DESIGNATED AS "C"(CLEAR) AND "T"(TIMING)

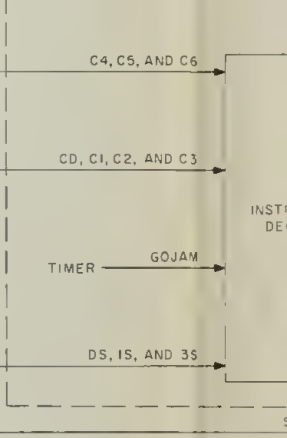


PRIORITY CONTRL INKL

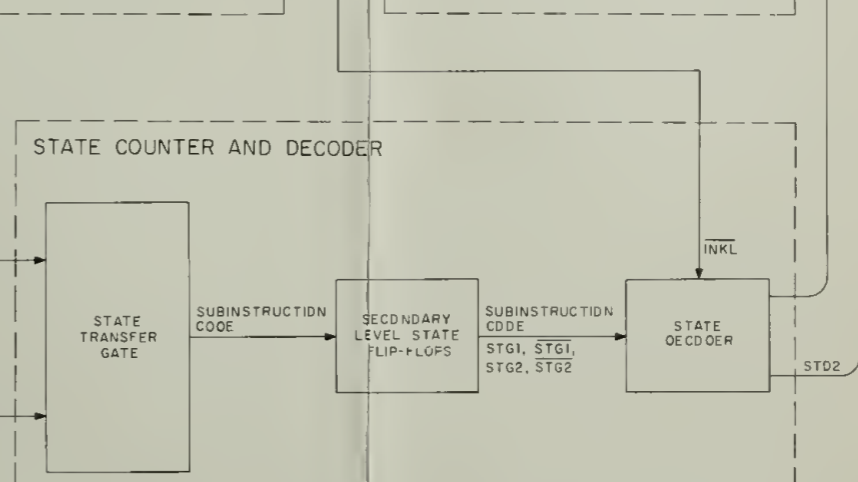
# SQ REGISTER AND DECODER



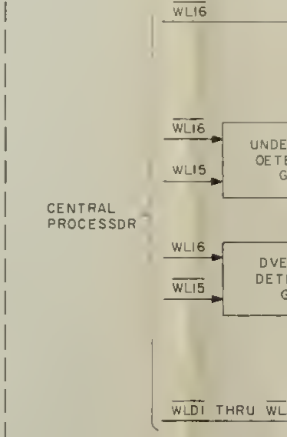
# INSTRUCTION DECODER



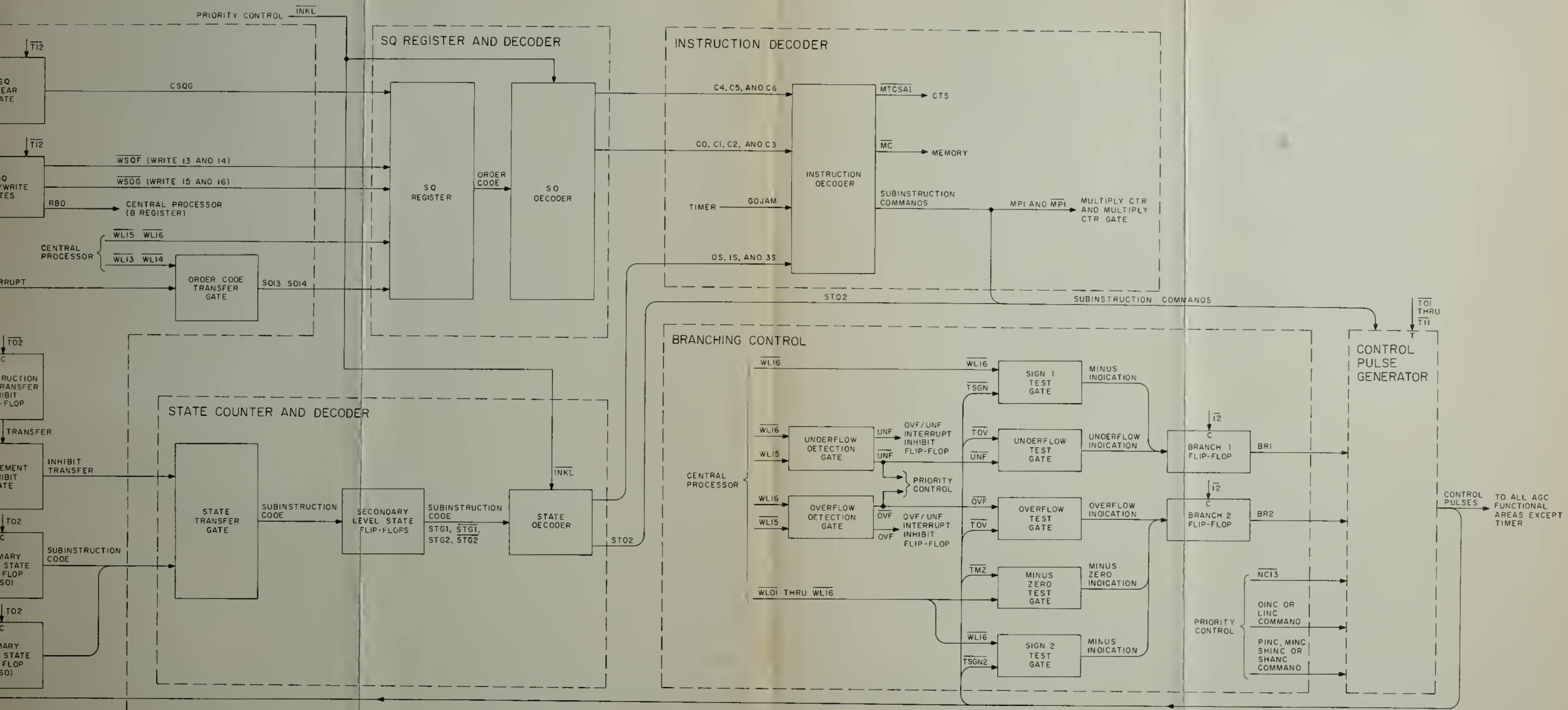
# STATE COUNTER AND DECODER



# BRANCHING CONTROL



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Figure 4-63. Sequence Generator, Functional Diagram

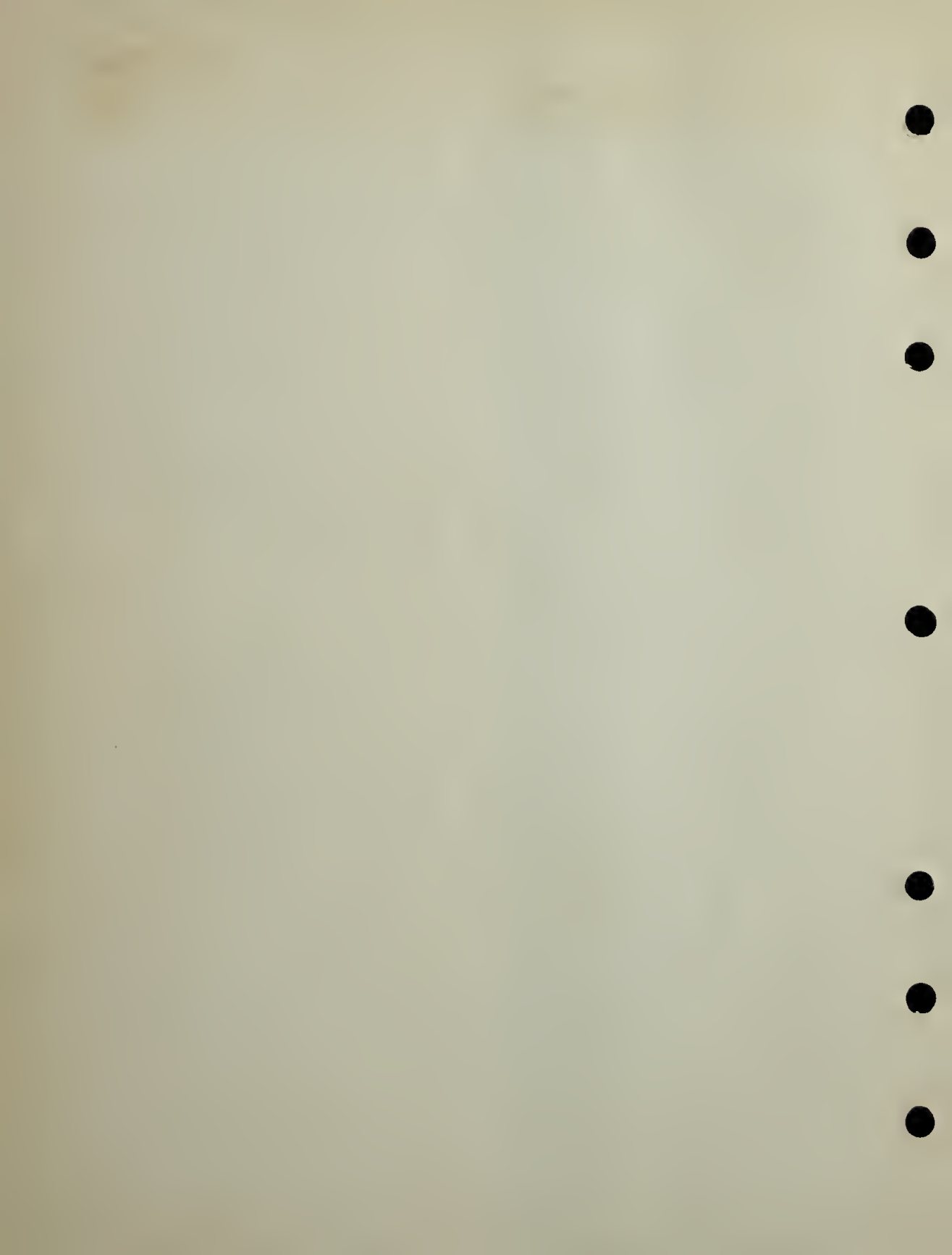


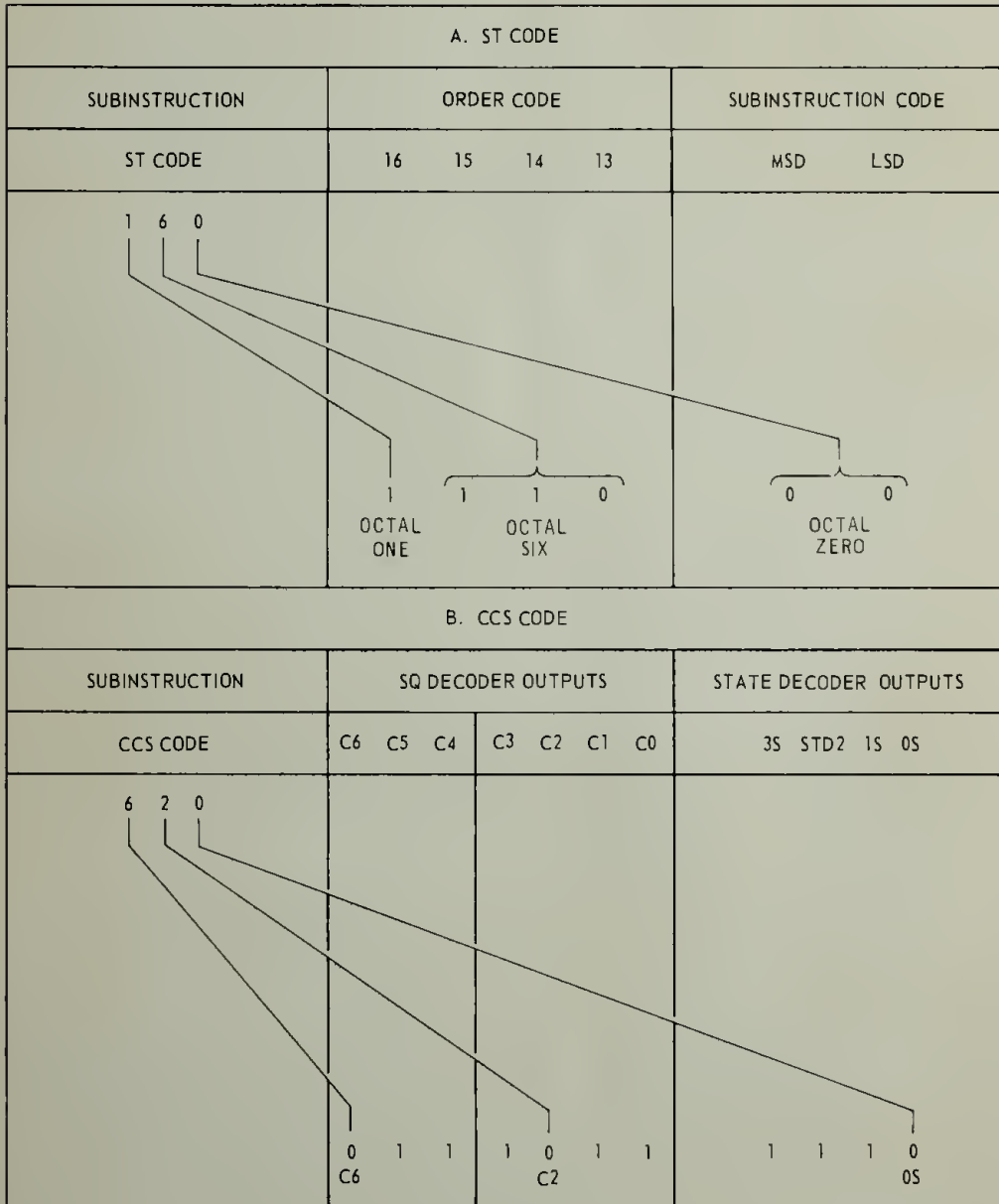
Table 4-II. Sequence Generator Codes

Subinstruction		Order Code			Subinstruction Code		INKL	SQ Decoder Outputs						State Decoder Outputs					
Initials	ST Code	16	15	14	13	MSD		LSD	C6	C5	C4	C3	C2	C1	C0	3S	STD2	1S	0S
STD2	XX2	X	X	X	X	1	0	0	X	X	X	X	X	X	1	1	1	1	1
TC0	000	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	0	0
XCH0	030	0	0	1	1	0	0	0	1	0	0	1	1	1	1	0	1	0	0
CS0	140	1	1	0	0	0	0	0	1	1	1	1	1	0	1	0	1	0	0
TS0	150	1	1	0	1	0	0	0	1	1	1	1	0	1	1	0	1	0	0
MSK0	170	1	1	1	1	0	0	0	1	1	0	1	1	1	1	0	1	0	0
AD0	160	1	1	1	0	0	0	0	1	1	1	0	1	1	1	0	1	0	0
NDX0	020	0	0	1	0	0	0	0	1	1	0	1	0	1	1	0	1	0	0
NDX1	021	0	0	1	0	0	1	0	1	0	1	0	1	1	1	0	0	1	0
CCS0	010	0	0	0	1	0	0	0	1	1	0	1	0	1	1	0	1	0	0
CCS1	011	0	0	0	1	0	1	0	1	1	0	1	0	1	1	0	0	1	0
SU0	130	1	0	1	1	0	0	0	1	0	1	0	1	1	1	0	1	0	0
MP0	110	1	0	0	1	0	0	0	1	0	1	1	1	1	1	0	1	0	0
MP1	111	1	0	0	1	0	1	0	1	0	1	1	1	0	1	0	0	1	0
MP3	113	1	0	0	1	1	1	0	1	0	1	1	0	1	0	0	1	1	0
DV0	120	1	0	1	0	0	0	0	1	0	1	1	0	1	1	0	1	0	0
DV1	121	1	0	1	0	0	1	0	1	0	1	1	0	1	1	0	0	1	0
RUPT1	031	0	0	1	1	0	1	0	1	1	0	1	1	1	1	0	0	1	0
RUPT3	033	0	0	1	1	1	1	0	1	1	0	1	1	1	0	0	1	1	1
RSM	023	0	0	1	0	1	1	0	1	1	0	0	1	1	0	0	1	1	1
PINC		X	X	X	X	X	X	1	1	1	1	X	X	X	X	0	X	0	X
MINC		X	X	X	X	X	X	1	1	1	1	X	X	X	X	0	X	0	X
SHINC		X	X	X	X	X	X	1	1	1	1	X	X	X	X	0	X	0	X
SHANC		X	X	X	X	X	X	1	1	1	1	X	X	X	X	0	X	0	X
GO	001	0	0	0	0	0	1	0	1	1	0	1	1	1	0	1	0	0	1
TCSA	003	0	0	0	0	1	1	0	1	1	0	1	1	1	0	0	1	1	1
OINC		X	X	X	X	X	X	1	1	1	1	X	X	X	X	0	X	0	X
LINC		X	X	X	X	X	X	1	1	1	1	X	X	X	X	0	X	0	X

MSD - Most Significant Digit, LSD - Least Significant Digit, X Indicates 0 or 1

0690





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Figure 4-64. ST and CCS Code Instruction

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Signal RUPTOR interrupts a current program in favor of a program of higher priority. Signal RUPTOR initiates instruction RUPT, which causes the contents of registers Z and B to be transferred to locations 0024 and 0025.

At the completion of instruction RUPT, program control is transferred to one of six RUPT subtransfer routines. During the execution of these subroutines, control is transferred to the interrupting program. If RUPTOR is not inhibited by the other inputs to the interrupt inhibit gate, the following operations occur at time 12:

- (1) The interrupt signal enables the SQ clear gate, and signal CSQG clears register SQ of the previous order code.
- (2) The interrupt signal inhibits the SQ read/write gates from generating read signal RBQ and write signal WSQG. However, write signal WSQF is generated. Inhibiting write signal WSQG results in bits 15 and 16 of the order code becoming logic ZERO's.
- (3) The interrupt inhibit gate output inhibits the order code transfer gate. This results in bits 13 and 14 of the order code becoming logic ONE's.
- (4) The interrupt sets the LSD primary level state flip-flop. The resultant order code is 0011, and the resultant subinstruction code is 01. Subinstruction RUPT1 is now executed.

The interrupt inhibit gate is enabled by RUPTOR, which indicates an interrupting program. Signal RUPTOR is inhibited by the start instruction requests (signals GCJAM and MTCSAI), by a monitor inhibit interrupt request (signal MNHRPT), and by an output of the new instruction flip-flop when it is reset. In addition, there are three program-controlled inhibits: Interrupt-in-progress, inhibit-interrupt/release-interrupt, and overflow/underflow. These three program-controlled inhibits are indicated by signals IIP, INHL, and IIL, respectively.

Signal IIP is the output of the interrupt-in-progress flip-flop. The flip-flop is set by signal 9H at time 9 of subinstruction RUPT1. Signal R24 or GOJAM resets the flip-flop. Signal R24 is generated at action 1 of subinstructions RUPT1 and RSM. Therefore, signal IIP is a logic ONE from action 9 of subinstruction RUPT1 until action 1 of subinstruction RSM. Subinstruction RSM recalls the interrupted program. This timing for signal IIP prevents an interrupting program from being interrupted.

Signal INHL is the output of the inhint/relint flip-flop. This signal is produced at time 5 whenever INHINT address 0017 is present. Signal INHL is released either at time 5 whenever relint address 0016 is present or when signal GOJAM is present. Addresses 0016 and 0017 are used in programs that require operation without interruption.

Signal IIL is generated by the OVF/UNF interrupt inhibit flip-flop. This flip-flop is set when either the overflow signal (OVF) or the underflow signal (UNF) is in coincidence with control pulse WOVI. The OVF/UNF interrupt inhibit flip-flop is reset at time 3 after the new instruction flip-flop is set by control pulse NISQ. Signal NISQ occurs at action 11 during the last subinstruction of a machine instruction.

4-8.2.2 Register SQ and State Counter Functional Description. The SQ decoder and state decoder (figure 4-63) receive the order code, subinstruction code, and request-for-increment signal INKL. Outputs from the SQ decoder and state decoder, with one exception, are supplied to the instruction decoder to initiate subinstruction commands. The outputs of the SQ decoder and state decoder are listed in table 4-II. The exception is subinstruction command STD2. The state decoder produces STD2 whenever subinstruction code 10 is present; STD2 requires no order code.

Signal  $\overline{\text{INKL}}$  forces the SQ decoder and state decoder outputs to all logic ONE's with the exception of STD2, which is forced to a logic ZERO level. The instruction decoder interprets the SQ decoder and state decoder outputs as a hold state, and the increment operation is performed after the next time 12. After the increment operation is performed, the order code in register SQ and the subinstruction code in the primary level state flip-flops designate the subinstruction to be performed. This order code and subinstruction code can be changed during the increment operation by an interrupt, GOJAM, or MTCSAI signal.

4-8.2.3 Instruction Decoder Functional Description. The instruction decoder (figure 4-63) produces subinstruction commands, memory control signal  $\overline{\text{MC}}$ , and monitor signal  $\overline{\text{MTCSAI}}$  according to the SQ decoder and state decoder outputs and signal GOJAM. There are separate outputs for each subinstruction command, and only one is specified at a time. Signal  $\overline{\text{MC}}$  inhibits memory during subinstruction DV1, subinstruction MP1, and GOJAM.

4-8.2.4 Control Pulse Generator Functional Description. The control pulse generator (figure 4-63) receives timing pulses from the timer, subinstruction commands from the instruction decoder and state decoder, signals from branching control, and instruction commands from priority control. The control pulse generator combines timing pulses, commands, and branching signals to produce the proper control pulses during the proper action time for specific subinstructions.

The control pulse generator receives the commands for all counter instructions and signal  $\overline{\text{NC13}}$  from priority control. These commands produce the control pulses for instructions PINC, MINC, SHINC, and SHANC. Signal  $\overline{\text{NC13}}$  produces control pulse RSCT at action 1 of the counter instructions.

The command for instruction OINC or LINC is sent directly to the control pulse generator from priority control. These CTS display and load requests are like subinstruction commands and cause the control pulse generator to produce the proper control pulses. Signal OINC or LINC is always accompanied by the request for increment signal  $\overline{\text{INKL}}$ . This is necessary because the present instruction must be postponed.

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4-8.2.5 Branching Control Functional Description. Branching control (figure 4-63) requirements during machine instructions are detected and then indicated by signals BR1 and BR2. These signals, with their complements, are supplied to the control pulse generator. Five test gates, enabled by control pulses and condition signals during applicable machine instructions, control the branch flip-flops, which produce the BR signals. The condition signals include overflow and underflow indications and a 16 bit word from the central processor.

The underflow or overflow conditions are tested by control pulse  $\overline{TOV}$  in the underflow and overflow test gates during subinstruction TS. Control pulse BR1 is produced if there is an underflow; BR2 if there is an overflow. The BR1 and BR2 signals condition control pulse generator gates so that control pulses are generated during actions 4, 5, and 7 of subinstruction TS. These control pulses are generated only if overflow or underflow exists.

A quantity present on the write amplifier outputs is tested for branching operations by control pulses  $\overline{TSGN}$ ,  $\overline{TMZ}$ , and  $\overline{TSGN2}$ . Control pulses  $\overline{TSGN}$  and  $\overline{TSGN2}$  enable tests for sign during machine instructions to branch according to a positive or a negative quantity. The difference in the two is that control pulse  $\overline{TSGN}$  causes signal BR1 to be produced and control pulse  $\overline{TSGN2}$  causes signal BR2.

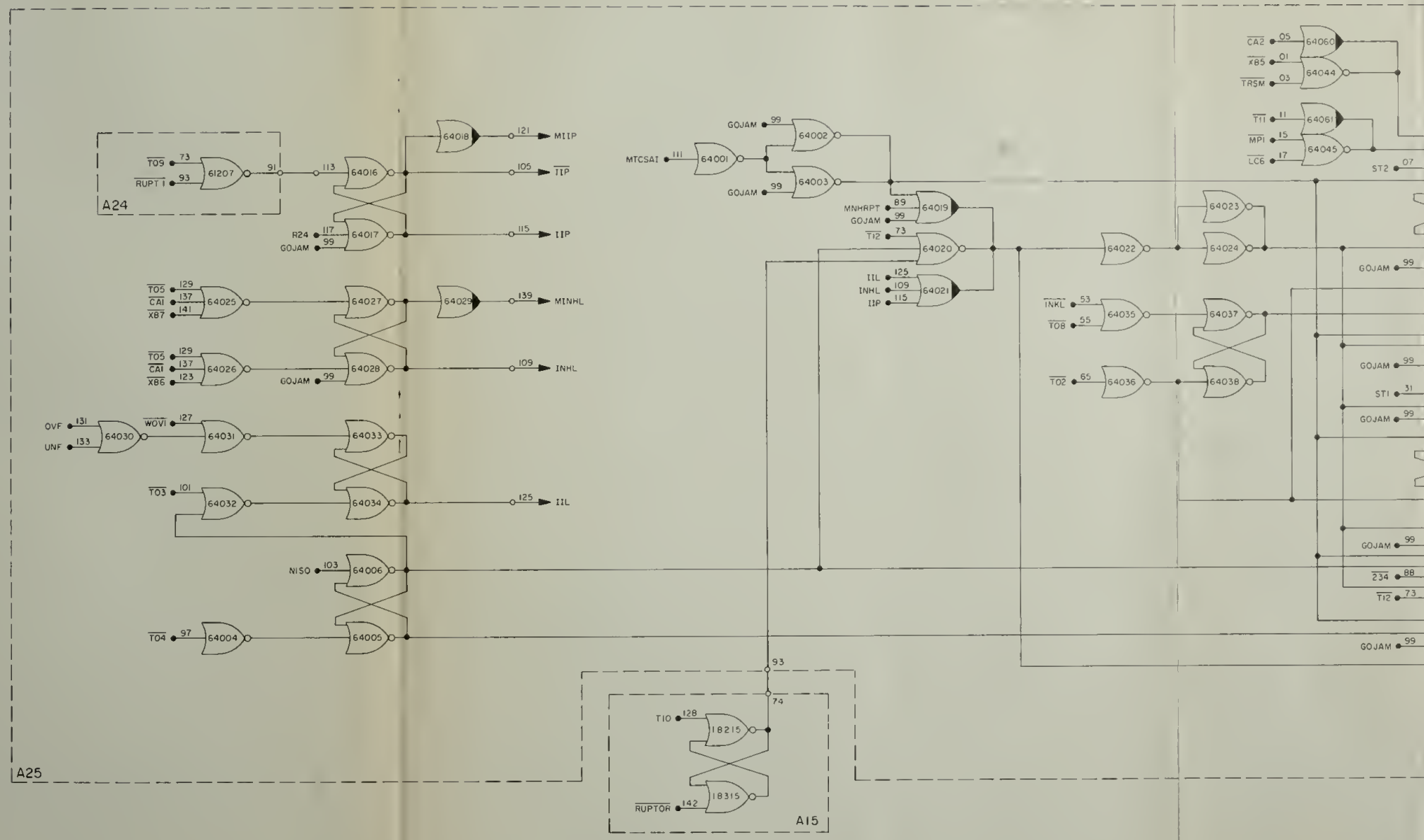
Control pulses  $\overline{TSGN}$  and  $\overline{TMZ}$  select one of four alternatives during subinstruction CCS0. Control pulse  $\overline{TSGN}$  tests the sign. If negative, the minus indication sets the branch 1 flip-flop, which produces signal BR1. Control pulse  $\overline{TMZ}$  then tests for the quantity minus zero. If present, the minus zero indication sets the branch 2 flip-flop, which produces signal BR2. If the test for sign initiated by control pulse  $\overline{TSGN}$  found a positive sign, BR1 is not produced and the 16 bit word is complemented before  $\overline{TMZ}$  occurs. The quantity minus zero, all logic ONE's, is produced if the prior word was the quantity plus zero, all logic ZERO's. A minus indication then sets the branch 2 flip-flop and BR2 is produced when control pulse  $\overline{TMZ}$  occurs. Signal BR2 is not produced if the prior word was greater than plus zero. The detected quantity minus zero (BR1 and BR2), less than minus zero (BR1 and not BR2), plus zero (BR2 and not BR1), or greater than plus zero (not BR1 and not BR2) selects different control pulses during subinstruction CCS0.

Control pulses  $\overline{TSGN2}$  and  $\overline{TSGN}$  select one of four alternatives during subinstruction MP0. They test the sign of two different quantities.

4-8.2.6 Interrupt Service Detailed Description. The interrupt service (figure 4-65) consists of the new instruction flip-flop, interrupt flip-flops, and transfer gates. The interrupt service controls the order code in register SQ and the subinstruction code. The sequence generator generates the order code internally or requests that it be transferred from the central processor. The subinstruction code produced by the primary level flip-flops designates particular subinstructions.

The operation to obtain an order code is initiated by signal NISQ. Signal NISQ is produced by the control pulse generator during the previous instruction. The new instruction flip-flop, FF64005-64006, (figure 4-65) is set by signal NISQ and remains set until the following time 4. The new instruction flip-flop output is applied to the SQ clear gate (64009) and SQ read/write gates (64007 and 64008). At time 12, clear signal CSQG is produced by gate 64009 and supplied to register SQ, and two write signals and one read signal are produced by gates 64007 and 64008. Read signal RBQ reads the order code of the next instruction from register B into the write amplifiers. Outputs WL13 and WL14 are transferred from the write amplifiers to order code transfer gates 64013 and 64014, and are loaded in register SQ by write signal WSQF. Outputs WL15 and WL16 are also transferred from the write amplifiers but loaded directly into register SQ by write signal WSQG. The OVF/UNF interrupt inhibit flip-flop (FF64033-64034) and the interrupt inhibit gate (64020) also receive an input from the new instruction flip-flop. This input is applicable to interrupt operations only.

A subinstruction code is generated by signals applied to the primary level state flip-flops (FF64042-64043 and FF64047-64048). Outputs from these flip-flops are supplied to the secondary level flip-flops (FF64052-64053 and FF64057-64058) through the state transfer gates 64050, 64051 and 64055, 64056. The state transfer gates are controlled by the subinstruction code transfer inhibit flip-flop (FF64037-64038) and the increment inhibit gate (64039). If priority control signals a counter increment operation with signal INKL, the subinstruction code transfer inhibit flip-flop is set at time 8. The output from this flip-flop inhibits the state transfer gate, which prevents the subinstruction code from being supplied to the secondary level flip-flops at time 12. This inhibiting action is prevented if the interrupt signals (MTCSAI or GOJAM) are present at the increment inhibit gates (64001, 64002, and 64003). The subinstruction code for RUPT1, MTCSAI, or GOJAM is then supplied to the secondary level state flip-flops (FF64052-64053 and FF64057-64058) via the primary level flip-flops (FF64042-64043 and FF64047-64049) and processed after the counter increment action.



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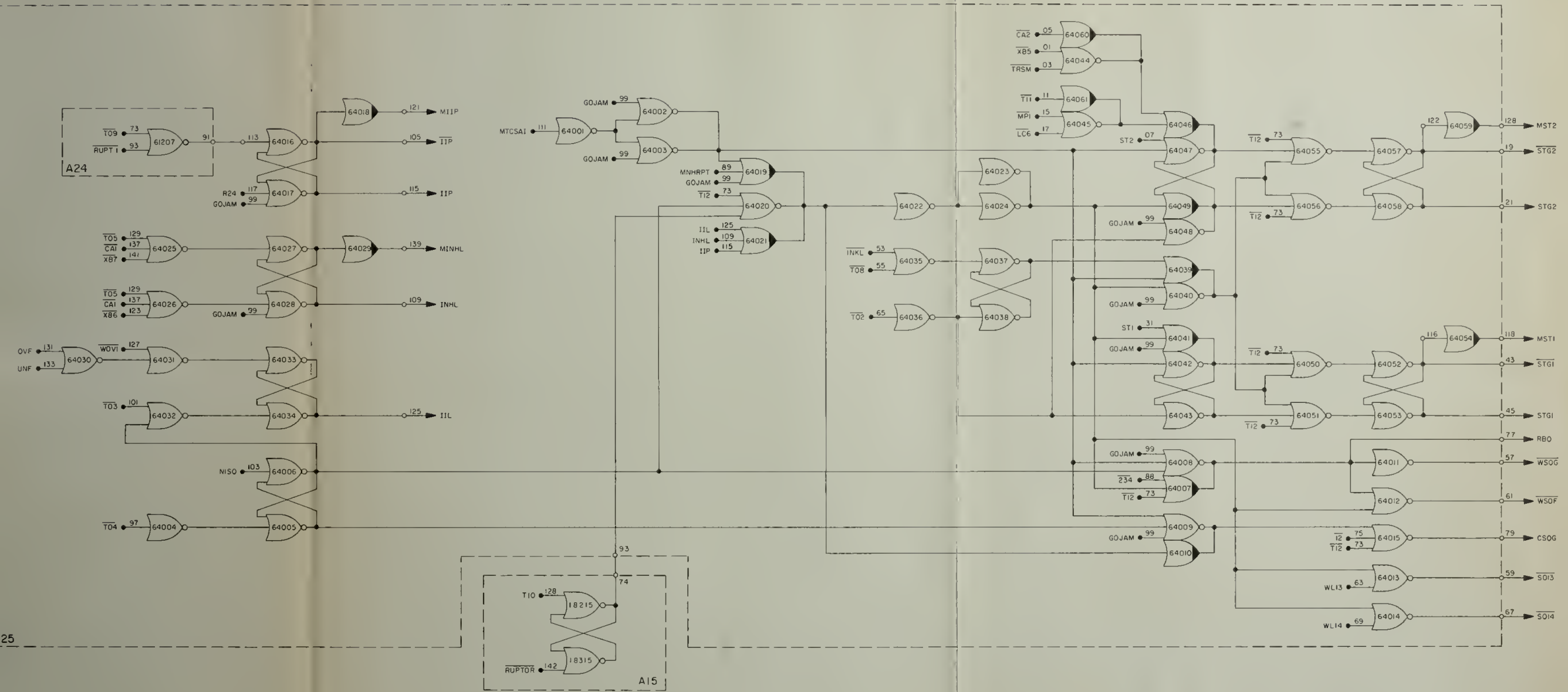


Figure 4-65. Sequence Generator Interrupt Service





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Start signals (GOJAM and MTCSAI) and interrupt signals control the SQ clear gate and the SQ read/write gates. GOJAM produces clear signal CSQG at time 12 and clears register SQ. Simultaneously, write signals  $\overline{WSQF}$  and  $\overline{WSQG}$  are inhibited. This action produces the order code of 0000. Signal GOJAM is applied also to the LSD primary level state flip-flop (FF64042-64043), which forces the subinstruction code to 01. This combination of order code and subinstruction code initiates instruction GO. Signal GOJAM inhibits signals MTCSAI and  $\overline{RUPTOR}$ , resets the interrupt-in-progress flip-flop (FF64016-64017) and the inhint/relint flip-flop (FF64027-64028), and inhibits an  $\overline{MC}$  command in the instruction decoder. These actions are necessary to obtain a new start within the AGC. Effectively, all requests and priorities are removed, and the sequence generator is cleared.

Signal MTCSAI (request for instruction TCSA) from the CTS forces the order code to 0000 in the same manner as signal GOJAM. Subinstruction code 11, required for the initiation of instruction TCSA, is produced by setting both primary level state flip-flops. Signal MTCSAI inhibits the generation of signal  $\overline{RUPTOR}$  and overrides the inhibiting action of the subinstruction code transfer by signal  $\overline{INKL}$ . Therefore, MTCSAI has priority over program interruptions, and instruction TCSA is performed after any counter increment operation.

Signal  $\overline{RUPTOR}$  interrupts a current program in favor of a program of higher priority. Signal  $\overline{RUPTOR}$  is supplied to the interrupt inhibit gate (64020) and produces the interrupt signal that initiates the execution instruction (RUPT). At the completion of instruction RUPT, program control is transferred to one of six RUPT transfer routines. If  $\overline{RUPTOR}$  is not inhibited by the other inputs to the interrupt inhibit gate, the following operations occur at time 12:

- (1) The interrupt signal enables the SQ clear gate (64010), and signal CSQG clears register SQ of the previous order code.
- (2) The interrupt signal inhibits the SQ read/write gates (64007, 64011) from generating read signal RBQ and write signal  $\overline{WSQG}$ . However, write signal  $\overline{WSQF}$  is generated. Inhibiting write signal  $\overline{WSQG}$  causes bits 15 and 16 of the order code to become logic ZERO's.
- (3) The interrupt inhibit gate output inhibits the order code transfer gates (64013, 64014). This causes bits 13 and 14 of the order code to become logic ONE's.
- (4) Finally, the interrupt signal sets the LSD primary level state flip-flop (FF64042-64043). The resultant order code is 0011, and the resultant subinstruction code is 01. Subinstruction RUPT1 is now executed.

A program interruption is initiated when the interrupt inhibit gate is enabled by signal RUPTOR. Signal RUPTOR becomes a logic ZERO and can effect a program interruption only if there are no other inhibiting signals. A program interruption will not be initiated if any of the following signals is present: start instruction request GOJAM or MTCSA1, monitor inhibit interrupt request MNHRPT, and the output of the new instruction flip-flop, when reset. In addition to these inhibits there are three program-controlled inhibits: interrupt-in-progress, inhibit-interrupt/release-interrupt (inhint/relint), and overflow/underflow. These three program-controlled inhibits are indicated by signals IIP, INHL, and IIL, respectively.

Signal IIP is the output from the interrupt-in-progress flip-flop (FF64016-64017). The flip-flop is set by the output signal of gate 61207 at time 9 of subinstruction RUPT1. Signal R24 or GOJAM resets the flip-flop. Signal R24 is generated at action 1 of subinstructions RUPT1 and RSM. Therefore, signal IIP is a logic ONE from action 9 of subinstruction RUPT1 until action 1 of subinstruction RSM. Subinstruction RSM recalls the interrupted program. This timing for signal IIP prevents an interrupting program from being interrupted.

Signal INHL is the output from the inhint/relint flip-flop (FF64027-64028). This signal is produced at time 5 whenever INHINT address 0017 is present. Signal INHL is released either at time 5 when relint address 0016 is present or when signal GOJAM is present. Addresses 0016 and 0017 are used in programs that require operation without interruption.

Signal IIL is generated by the overflow/underflow interrupt inhibit flip-flop (FF64033-64034). This flip-flop is set when either overflow (OVF) or underflow (UNF) occurs coincident with control pulse WOVI. The overflow/underflow interrupt inhibit flip-flop is reset at time 3 after the new instruction flip-flop is set by control pulse NISQ. Control pulse NISQ occurs at action 11 during the last subinstruction of a machine instruction.

When a program is interrupted in favor of a program of higher priority, the interrupted program is transferred to memory and retained until the program of higher priority is processed. At the completion of the higher-priority program the interrupted program will be recalled by subinstruction RSM and completed. Subinstruction RSM is initiated at the end of each interrupting program. (RSM returns the contents of locations 0024 and 0025 to registers Z and B and causes the interrupted program to be resumed.) Subinstruction NDX0 generates a TRSM control pulse and enables the RSM gate (64044, 64060) when address 0025 is available. The RSM gate sets the MSD primary level state flip-flop (FF64047-64049) to produce the subinstruction code. Subinstructions NDX0 and RSM have the same order code (0010); however, control pulse ST1 is produced by the control pulse generator and sets the LSD primary level state flip-flop to adjust the subinstruction code to execute subinstruction RSM instead of NDX0.

4-8.2.7 Register SQ and State Counter Detailed Description. The SQ decoder and state decoder (figure 4-66) convert the order code and subinstruction codes into signals that can be combined in the instruction decoder to produce subinstruction commands. All output signals except subinstruction STD2 are applied to the instruction decoder.

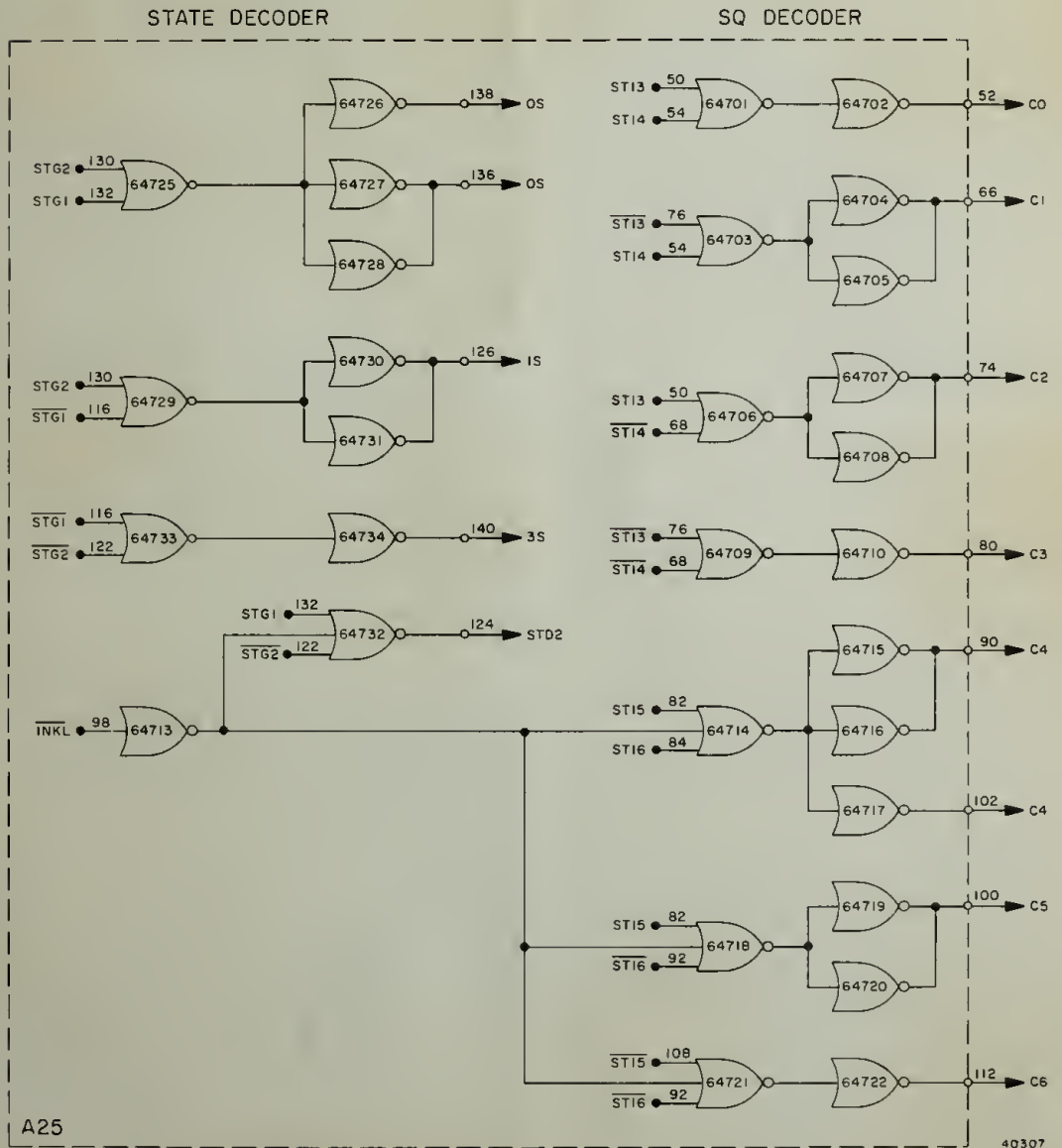


Figure 4-66. SQ Decoder and State Decoder

The state decoder produces signal STD2 whenever subinstruction code 10 from the secondary level flip-flop is present. Signal STD2 requires no order code.

Signal  $\overline{\text{INKL}}$  is supplied to both the SQ decoder and state decoder from priority control and forces the SQ and state decoder outputs to a condition of all ONE's with the exception of signal STD2, which is forced to a logic ZERO level. The instruction decoder then interprets the SQ and state decoder outputs as a hold state, and the increment operation is performed after the next time 12. After the increment operation is performed, the order code in register SQ and the subinstruction code in the primary level state flip-flops designate the subinstruction to be performed. This order code and subinstruction code can be changed during the increment operation by an interrupt, GOJAM, or MTCsAI signal.

4-8.2.8 Instruction Decoder Detailed Description. The instruction decoder (figure 4-67) combines the output from the SQ and state decoders to produce subinstruction commands. Signal GOJAM is supplied also to the instruction decoder and inhibits the generation of the memory cycle ( $\overline{\text{MC}}$ ) command. Only one subinstruction is specified at a time and is supplied as a separate output to the control pulse generator.

4-8.2.9 Control Pulse Generator Detailed Description. The control pulse generator produces the control pulses required for completion of subinstructions throughout the AGC. The generation of control pulses is determined by the input signals from the state decoder, instruction decoder, branch flip-flops, and priority control. Each control pulse produced performs a specific function. The combination of the different pulses generated completes a particular subinstruction. For example: figure 4-68 illustrates signal  $\overline{\text{WA}}$ ,  $\overline{\text{RA}}$ , and  $\overline{\text{WALP}}$ . Signals  $\overline{\text{WA}}$  and  $\overline{\text{RA}}$  are necessary for writing information into and reading information out of register A.

Signal  $\overline{\text{WALP}}$  is generated only during a multiply instruction and causes register A in conjunction with register LP to form a double-length shifting accumulator. Signal  $\overline{\text{WALP}}$ , generated at the time of signal  $\overline{\text{T11}}$  of an MP0 instruction by gates 61276 and 61522, transfers bit 1 from the write lines to bit position 14 of register LP. This manipulation of data accomplishes the required shifting during a multiply instruction.

When the AGC executes a transfer control instruction or a divide instruction, the address of the next instruction is stored in register Q before the transfer control is processed. This is done to enable the AGC to return to the original instruction after completion of the transfer control. At the time of signal  $\overline{\text{T08}}$ , during a transfer control instruction (figure 4-69), gates 60630 and 60715 generate signal  $\overline{\text{WQ}}$ . Generated also at time of signal  $\overline{\text{T08}}$  is control pulse  $\overline{\text{RZ}}$ . This combined action transfers the information from register Z to register Q. When a divide instruction is being executed, register Q holds the dividend during computation and the remainder at completion of the instruction.

Register Z normally stores the address of the next instruction. This is accomplished by incrementing the present instruction being executed by one in the adder and transferring the result to register Z. Figure 4-70 illustrates the condition under which control pulses  $\overline{\text{WZ}}$  and  $\overline{\text{RZ}}$  are generated. In the case of instruction STD2 read

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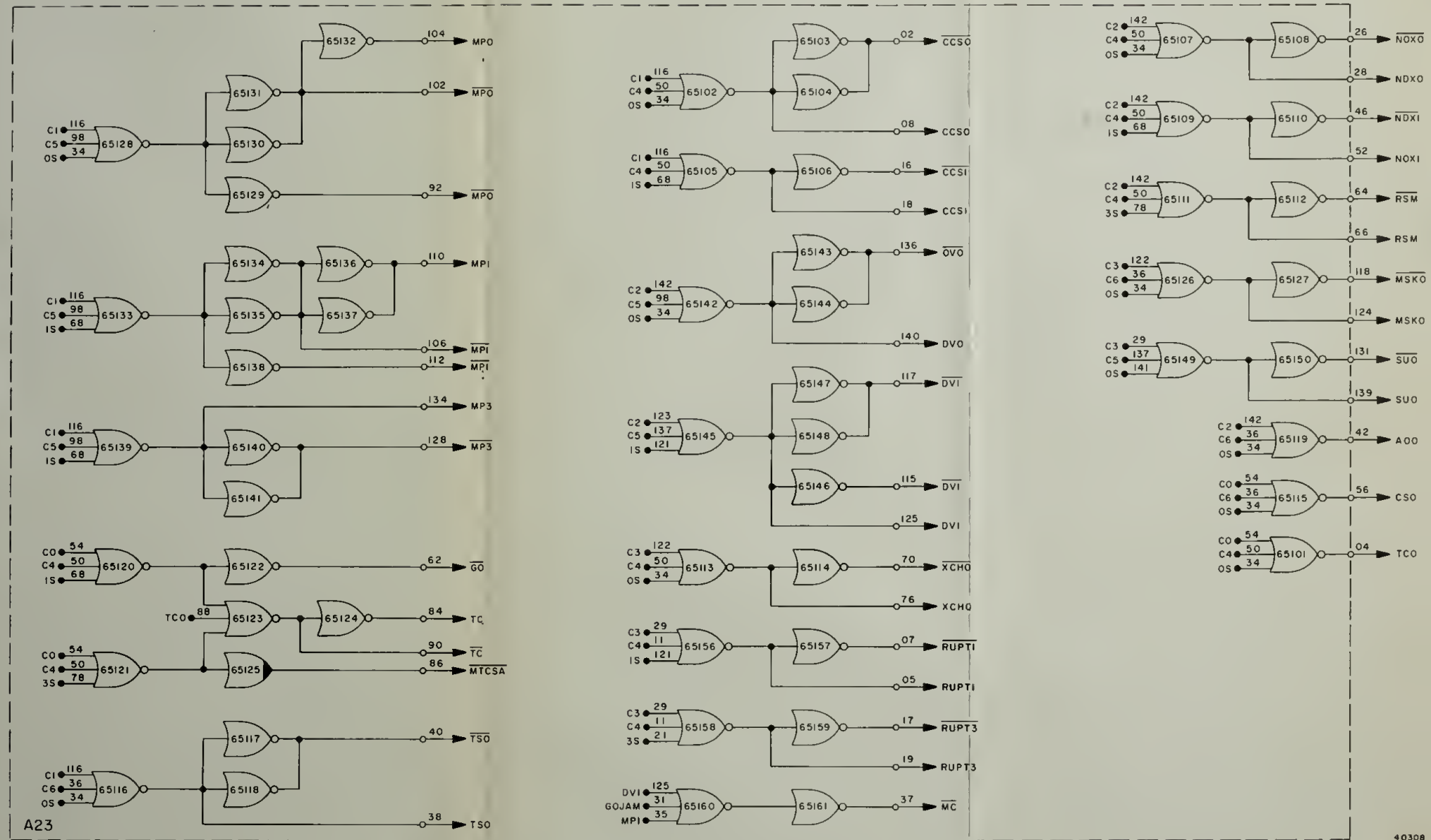
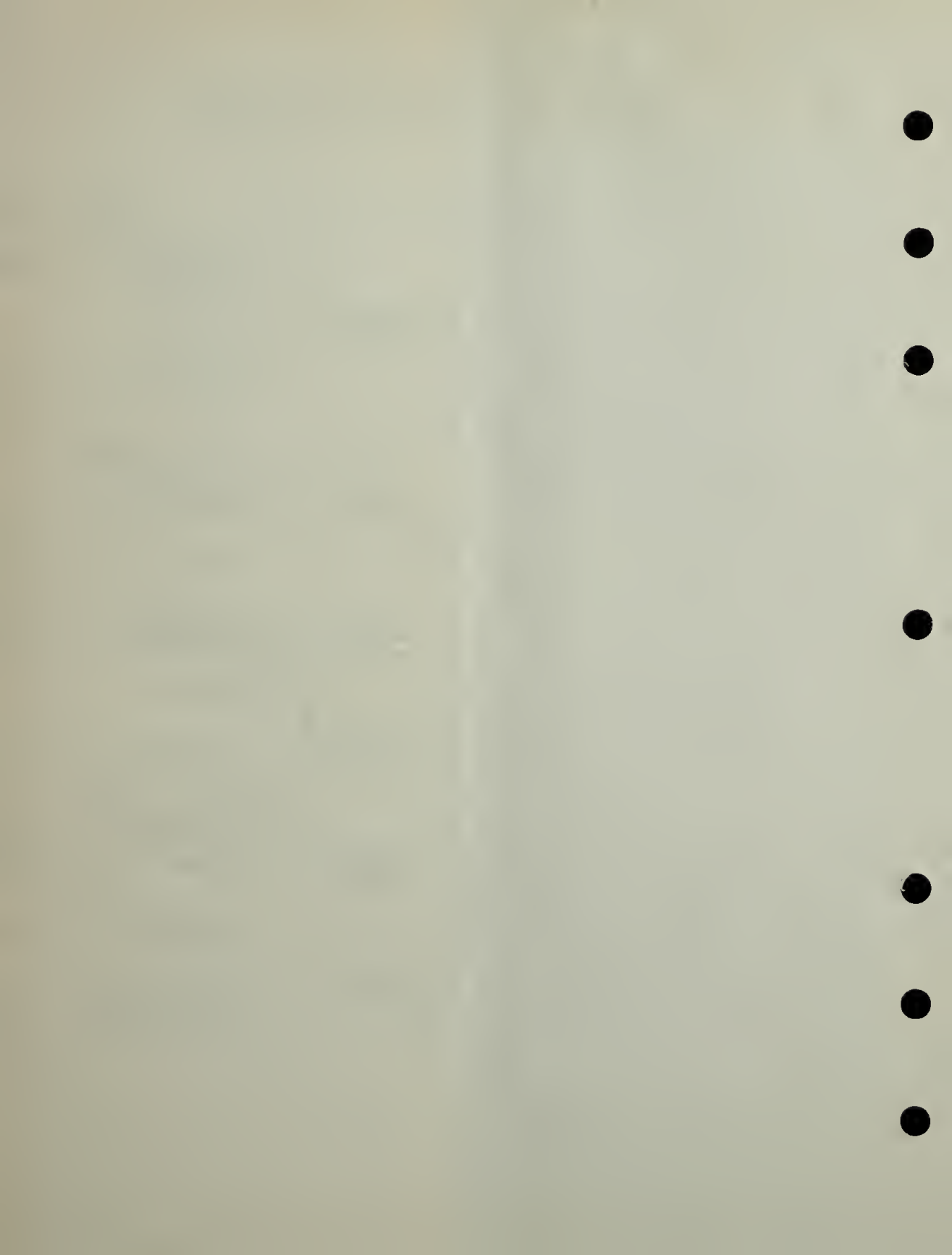
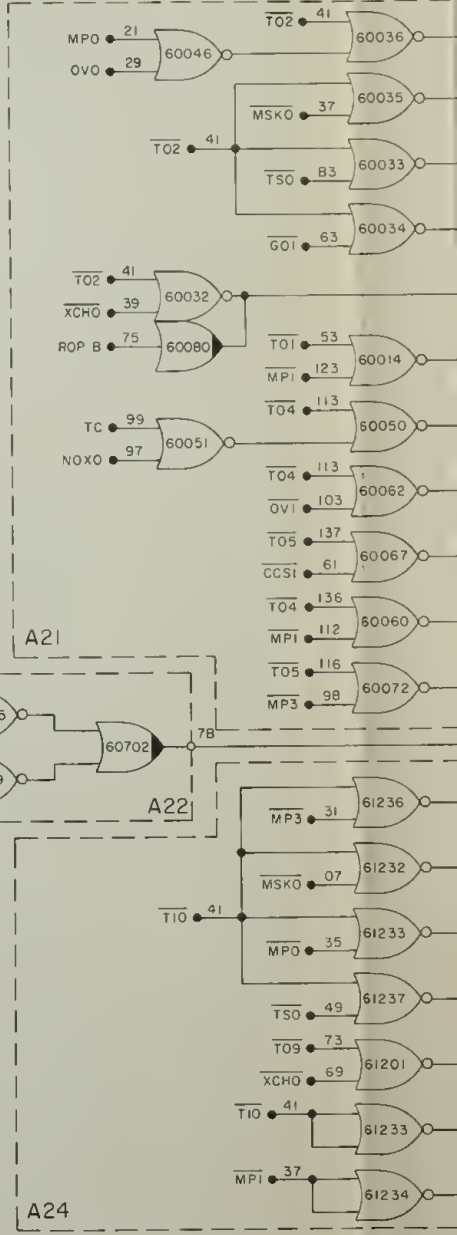
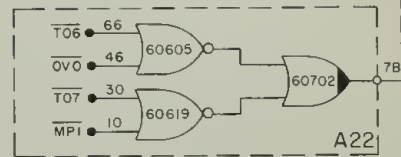
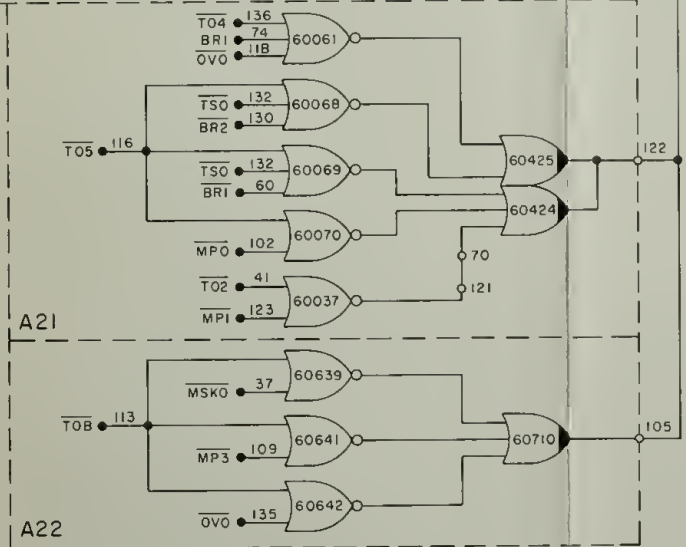
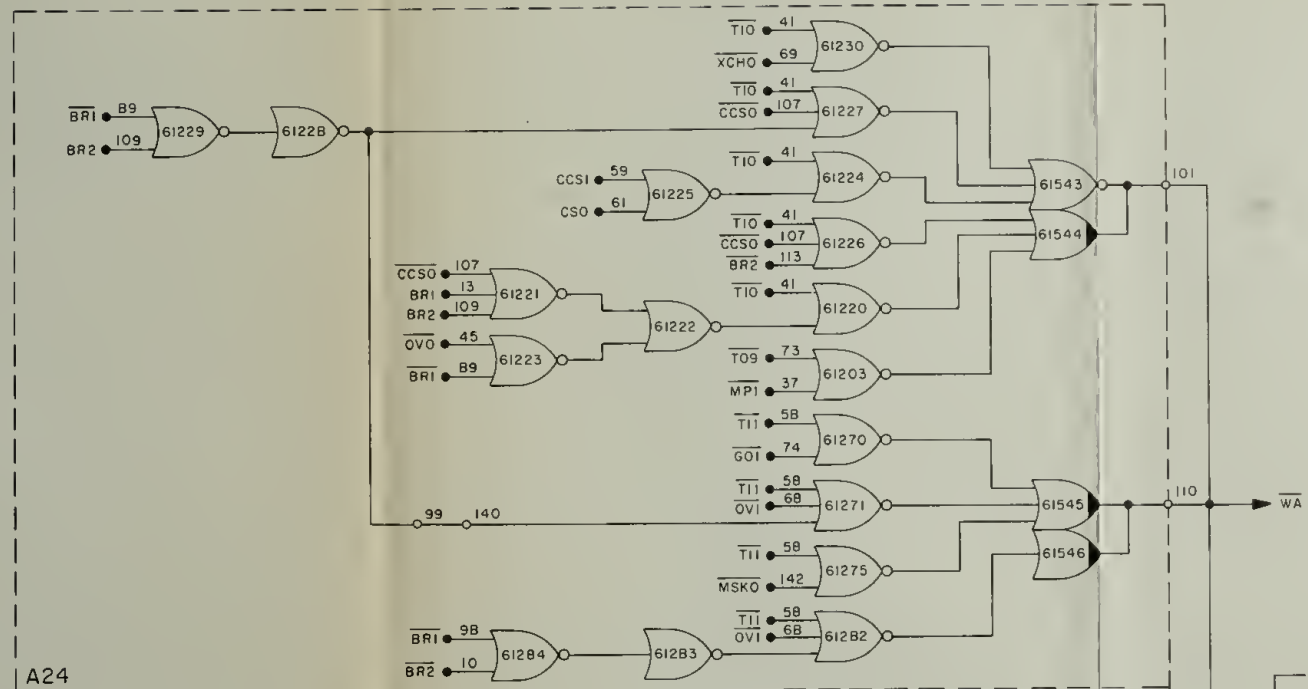


Figure 4-67. Instruction Decoder





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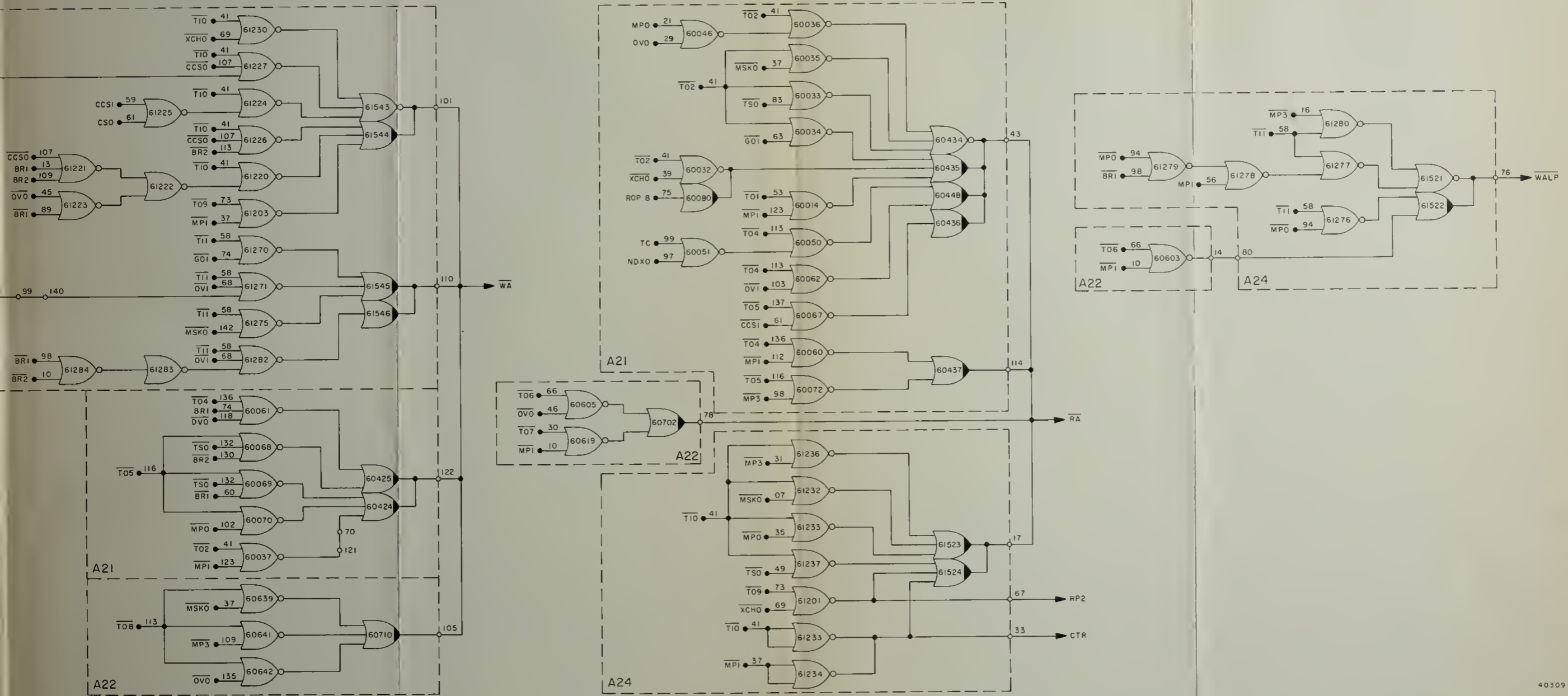
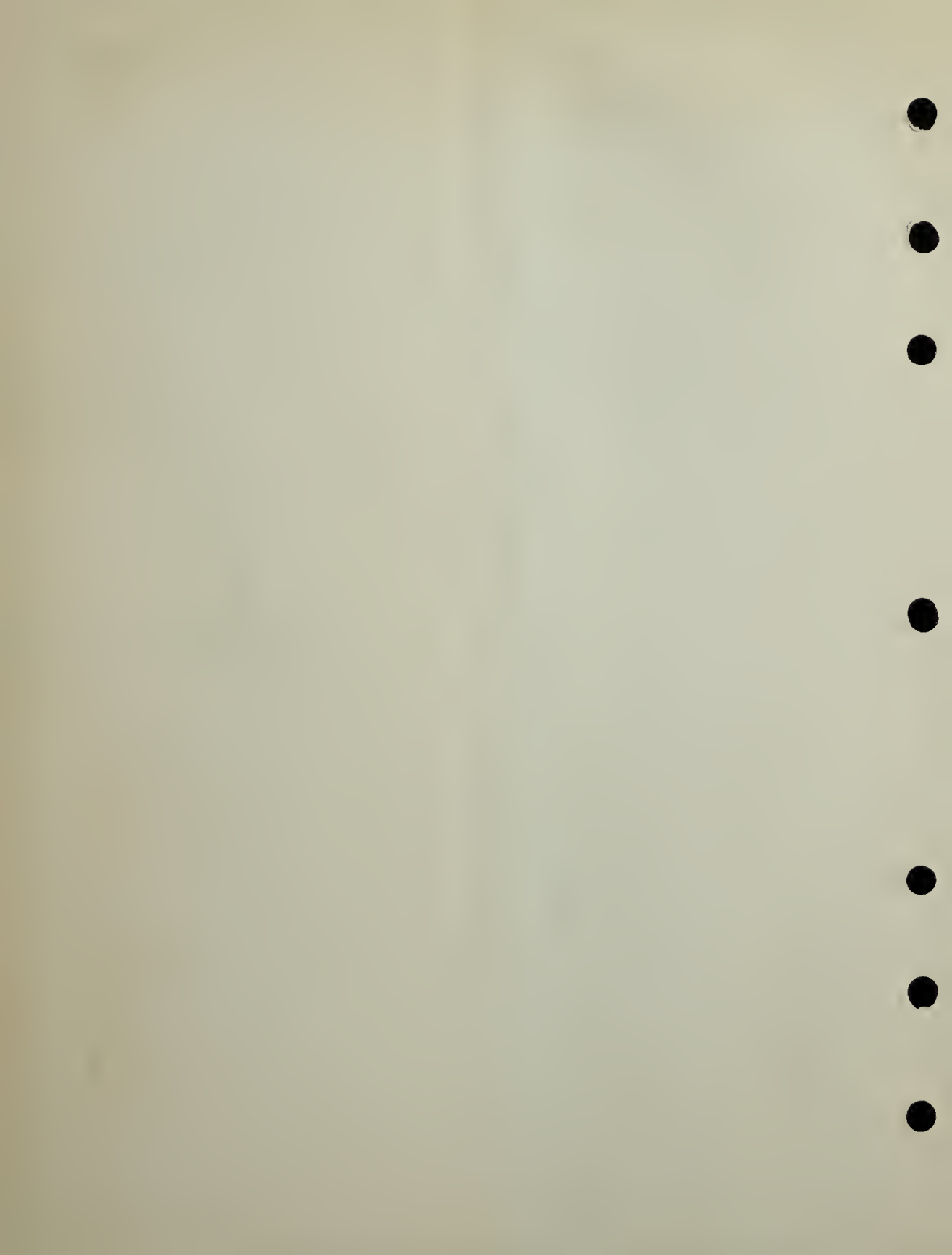


Figure 4-68. Register A Control Pulses





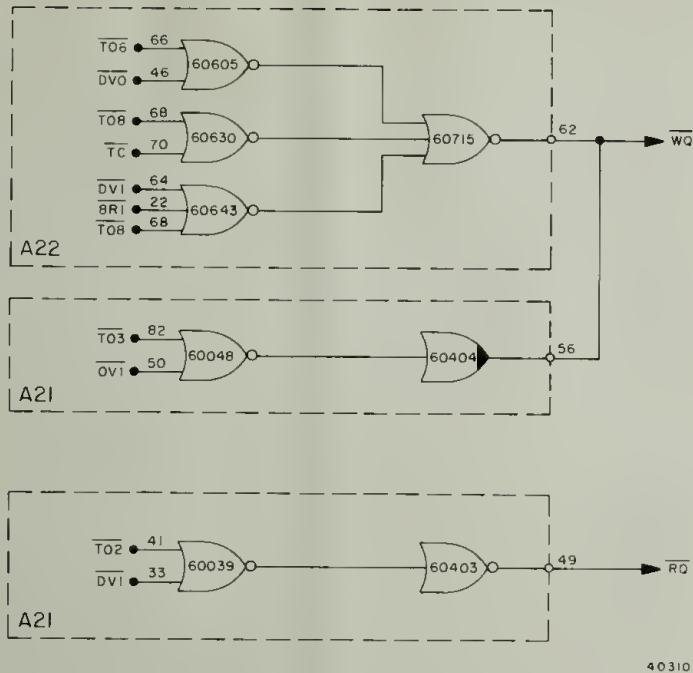
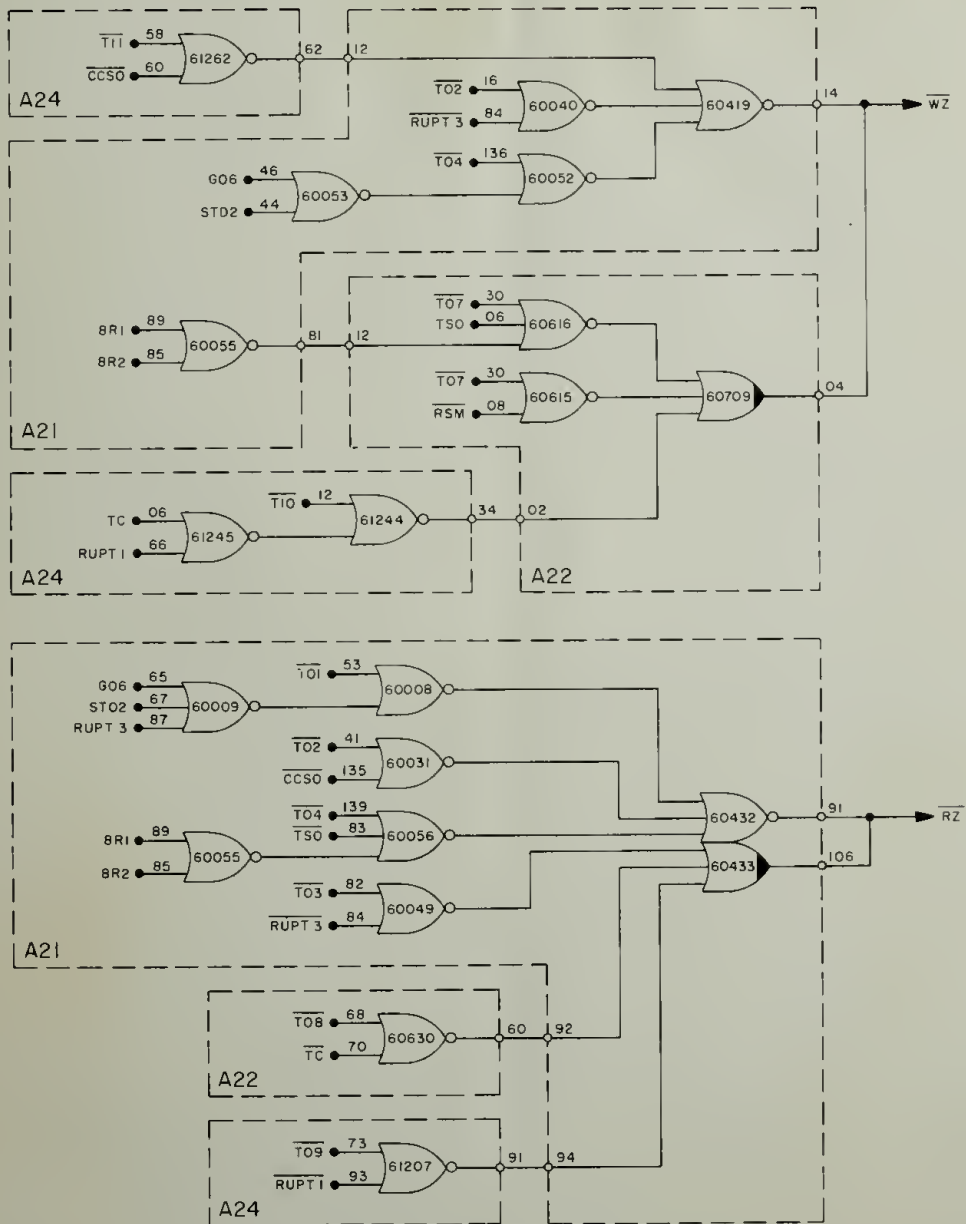


Figure 4-69. Register Q Control Pulses

pulse  $\overline{RZ}$  is generated at action 1 by gates 60009, 60008, and 60432. Control pulse  $\overline{WS}$  is also generated during action 1. These two pulses enable the read gates of register Z and write gates of register S simultaneously. This transfers the next instruction into register S. At action 4 of the same instruction control pulses  $\overline{RU}$  and  $\overline{WZ}$  are generated by gates 60053, 60052, and 60419. These control pulses read the incremented information from register U into register Z. The information in register Z now represents the next instruction.

Control pulse  $\overline{RLP}$  and  $\overline{WLP}$  (figure 4-71) enable the read and write gates of register LP during a multiply or divide instruction. The AGC multiplies by addition and divides by subtraction. Since the AGC can add or subtract only two numbers at any one time, subtotals must be computed continually until the final result is achieved. These subtotals are retained in register LP during multiplication and in register Q during division. Register A is brought into use by special control pulse WALP (figure 4-68), thus forming with register LP a double-length shifting accumulator. As the quantities are added, the contents of registers A and LP are shifted to the right until the final product is established, at which time the next instruction is processed. In division, register Q retains the dividend and upon completion of the instruction contains the remainder. The contents of register LP indicate if the quotient is positive or negative.



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Figure 4-70. Register Z Control Pulses

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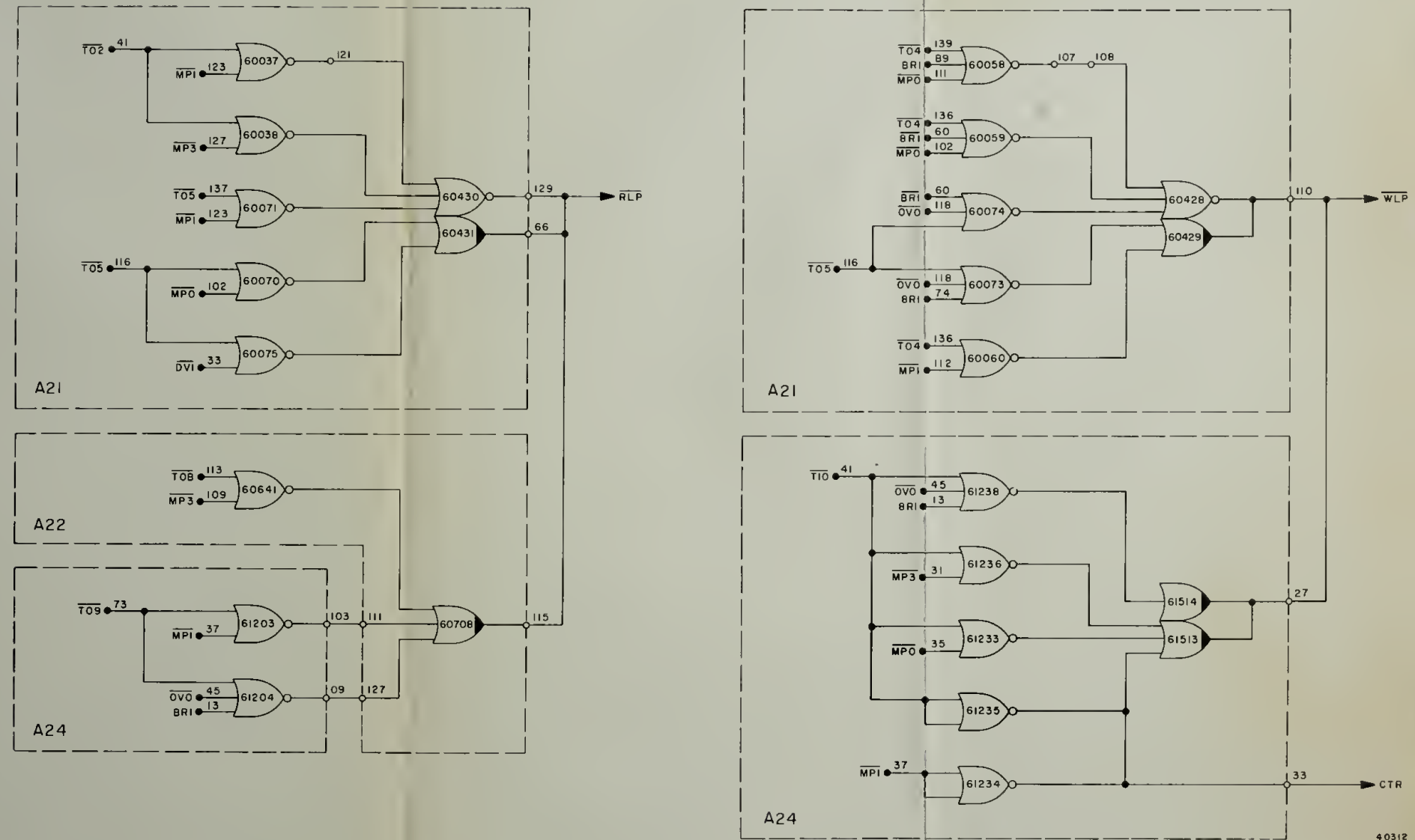
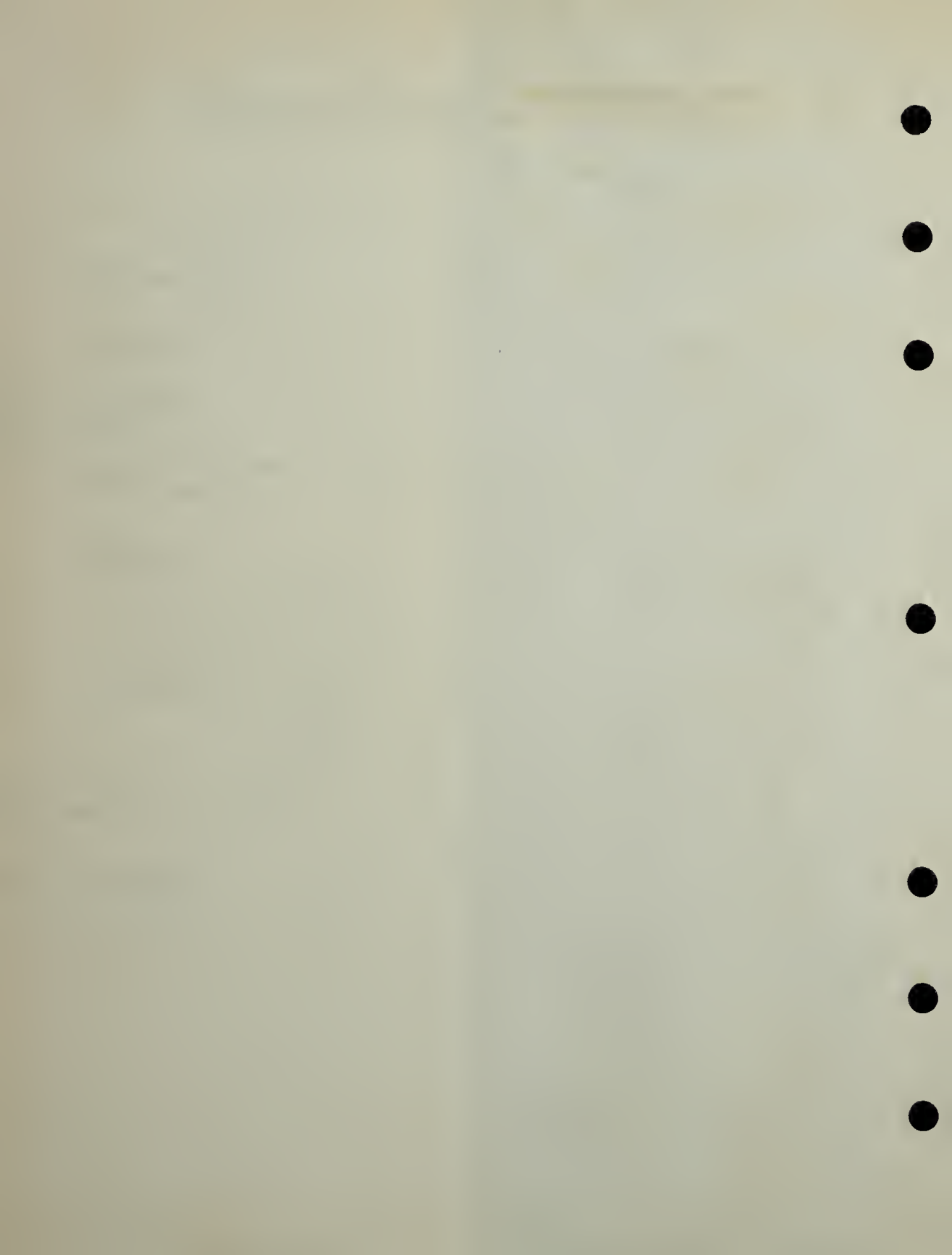


Figure 4-71. Register LP Control Pulses



Information to be processed is normally sent first to register B of the central processor. The register serves primarily as a storage element until the information is requested. The register stores the order code and relevant address of the instruction to be executed next.

Registers S and SQ function in a manner similar to other registers of the central processor. Information is written into these registers from the write lines by signal  $\overline{WS}$ . No read signal is generated to read out information. The outputs and their complements (ST01 - ST16) are available directly from the output gates. Write signal  $\overline{WS}$  is generated at all times by gates 60015 and 60401 (figure 4-72) except during instruction MP1. Thus, an address is written into register S at action 1 of each memory cycle for every instruction except MP1.

The control pulses associated with the transfer of information to and from register B are generated by the circuitry on figure 4-73. For example, during action 1 of a transfer control instruction signal G05 (produced by signal TC) enables gates 60646, 60644, and 60724, producing read signal  $\overline{RB}$ . Simultaneously, the write gates of register S are enabled by signal WS, and the order code is transferred from register B to register S. At action 7 signal G05 is coincident with time pulse  $\overline{T07}$ , and gates 60610, 60612, and 60718 produce signal  $\overline{WB}$ , writing the order code of the next instruction into register B. The complement of  $\overline{RB}$  is produced for certain programs; to place this information on the write lines, control pulse  $\overline{RC}$  is required. As in the case of the divide instruction, gates 60061 and 60418 are enabled at the time of signal  $\overline{T04}$ , producing signal  $\overline{RC}$  and transferring the complement of register B to register A.

Register G functions as a buffer for information coming from and going to erasable memory and fixed memory. The outputs from the sense amplifiers are connected directly to register G. Data written into register G from memory is a function of memory cycle timing and is considered to be written into register G at action 6. At action 7 of a transfer control instruction, control pulse  $\overline{RG}$  (figure 4-74) is produced by signals G05 and time pulse  $\overline{T07}$  and causes the contents of register G to be placed onto the write lines. This information is gated into register B by write pulse  $\overline{WB}$ . Register G is normally cleared at action 3 in preparation for information from the sense amplifiers. However, during an MP0 or DV0 instruction it is necessary to

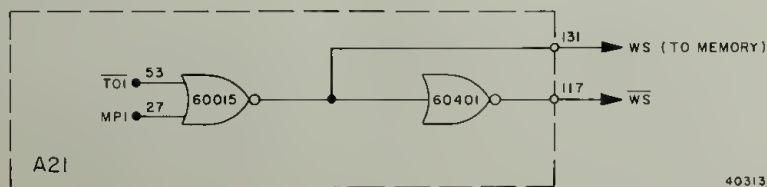


Figure 4-72. Register S Control Pulses

clear register G at action 2 because an address for information stored in a flip-flop register may be present at action 3. Control pulse CLGS is produced by gates 60046, 60036, 60442, and 60443 for this purpose.

The adder portion of the AGC contains two input registers (X and Y) and one output register (U). Information written into registers X and Y are added, and the sum is written into register U. However, when information is contained in only one input register, it may be incremented by one on command. For example, at action 1 of subinstruction STD2 gates 60007, 60005, 60438, and 60414 and 60415 (figure 4-75) generate control pulses  $\overline{WY}$  and CI. These control pulses, in conjunction with control pulses  $\overline{RZ}$  and  $\overline{WS}$ , transfer information contained in register Z to registers S and Y. Control pulse CI increments the contents of register Y by one.

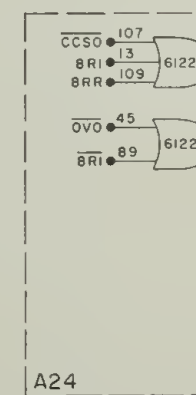
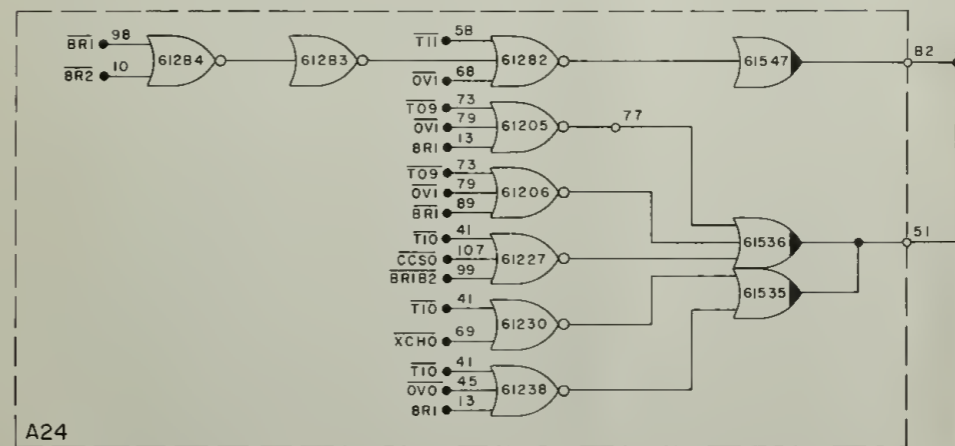
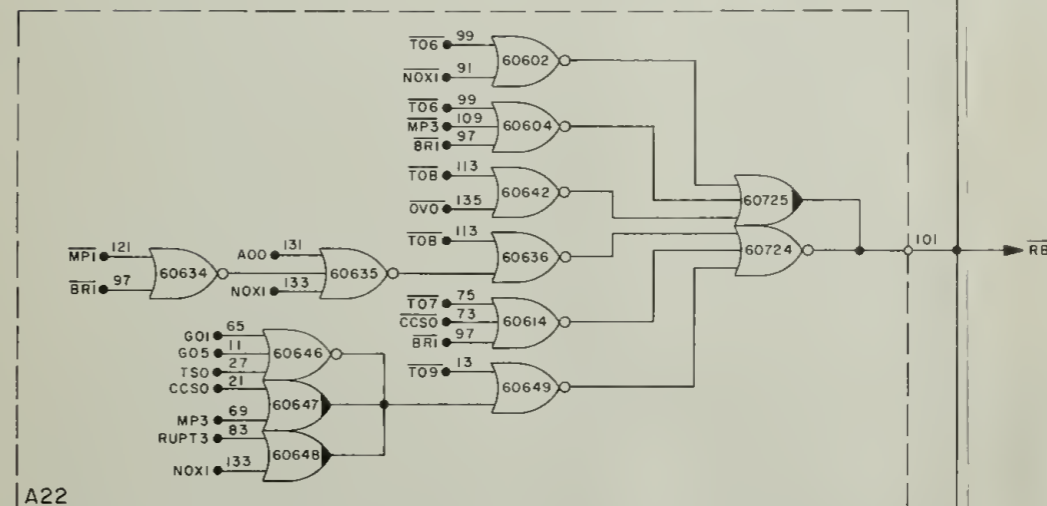
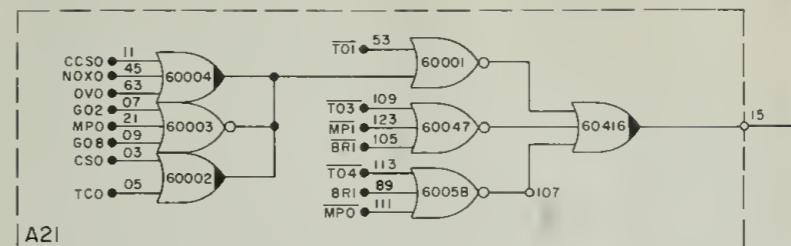
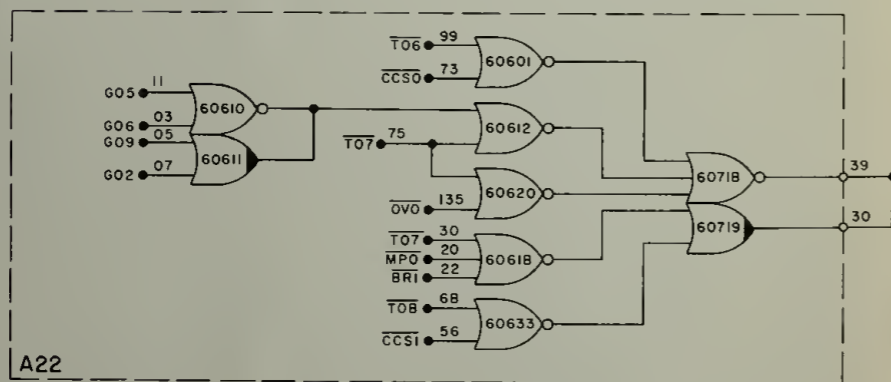
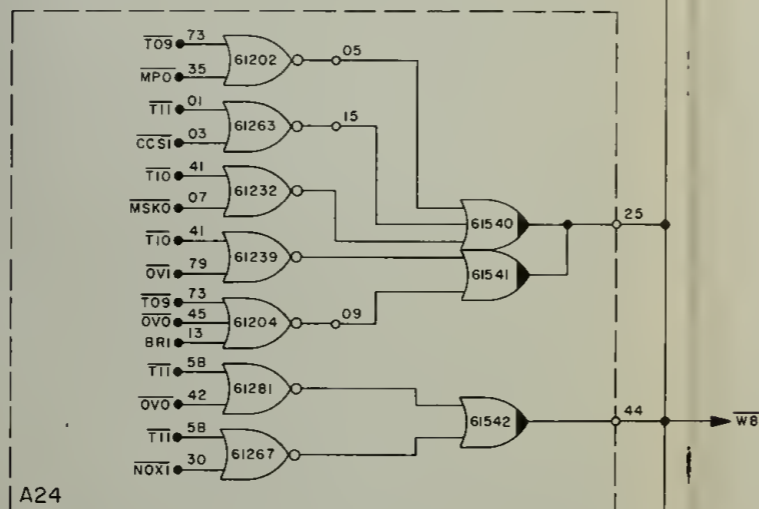
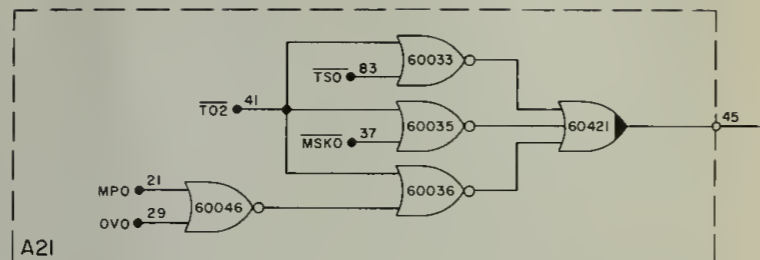
At action 4 the read gates of register A are enabled by control pulse  $\overline{RU}$ . This incremented information is written into register Z and represents the next instruction.

Information being read out of memory is checked for possible error by the parity logic. Information coming from memory is tested for proper parity by writing the information into the parity register. For example, at action 7 of a transfer control instruction signals G05 and  $\overline{T07}$  enable gates 60610, 60612, and 60732 (figure 4-76) to produce control pulse  $\overline{WP}$ . Control pulse  $\overline{RG}$  is also produced and the contents of register G are transferred to the parity logic. The command test parity is given by control pulse  $\overline{TP}$  at the output of gate 60705. If the parity is correct, no alarm registers. When information is written into memory, the information is checked and the proper parity bit is generated ( $\overline{GP}$ ) by gate 60701 during action 8.

During an exchange instruction a flip-flop in the parity circuits stores the parity bit of one word while the parity logic checks another word for correct parity. This flip-flop can be considered a single-bit-position register (P2) and is enabled for write-in and read-out by control pulses  $\overline{WP2}$  and  $\overline{RP2}$  which are generated only during an exchange instruction.

During the execution of various subinstructions it is necessary to store information temporarily in addressable registers A, Q, Z, and LP. This is accomplished by writing the address of the desired register into register S. For example, during a transfer control instruction the address of the flip-flop register is entered into register S at action 1. At action 7 signal G05 and time pulse  $\overline{T07}$  enable gates 60612 and 60720 (figure 4-77), which produces control pulse  $\overline{RSC}$  and thus reads the information from the flip-flop register directly into register B.

Register G also is enabled but contains no information at this time. During action 8 the information of the original program, prior to the initiation of the transfer control instruction, is transferred from register Z to register Q. At action 9 control pulse  $\overline{WSC}$  is generated by gates 60649 and 60706, which transfers the information in register B to the addressed flip-flop. At action 10 the incremented information in register U and is transferred to register Z. Register Z now contains the next instruction.





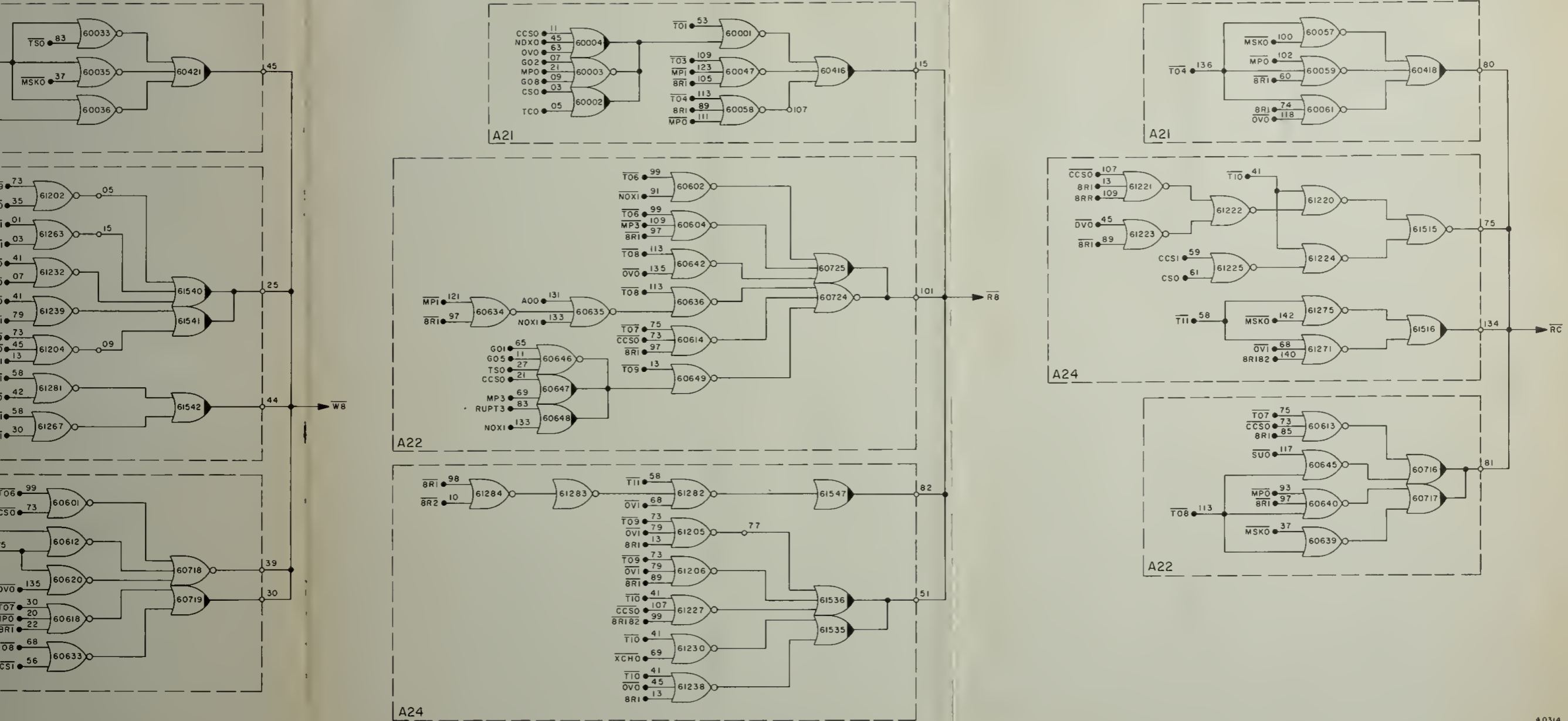


Figure 4-73. Register B Control Pulses



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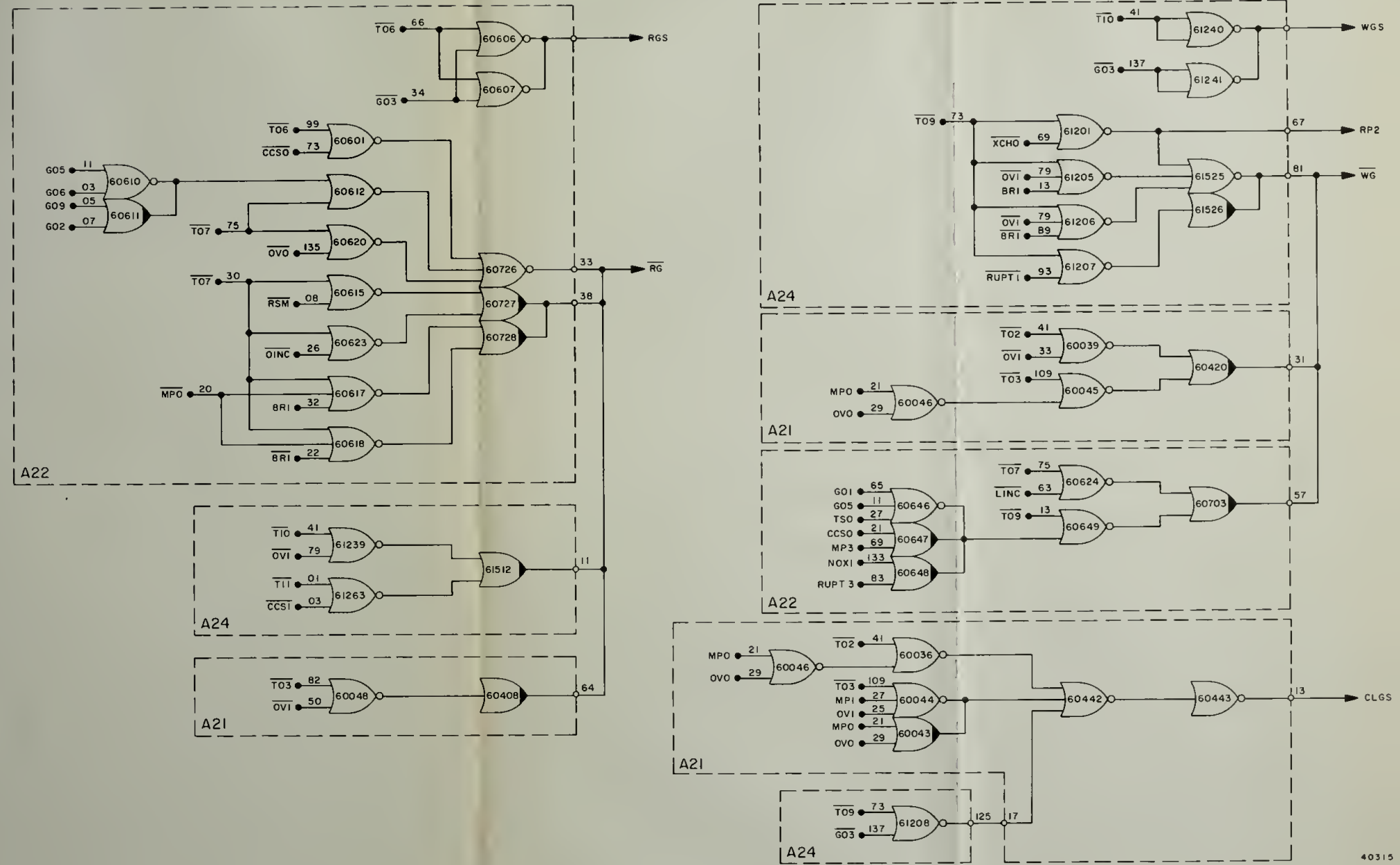
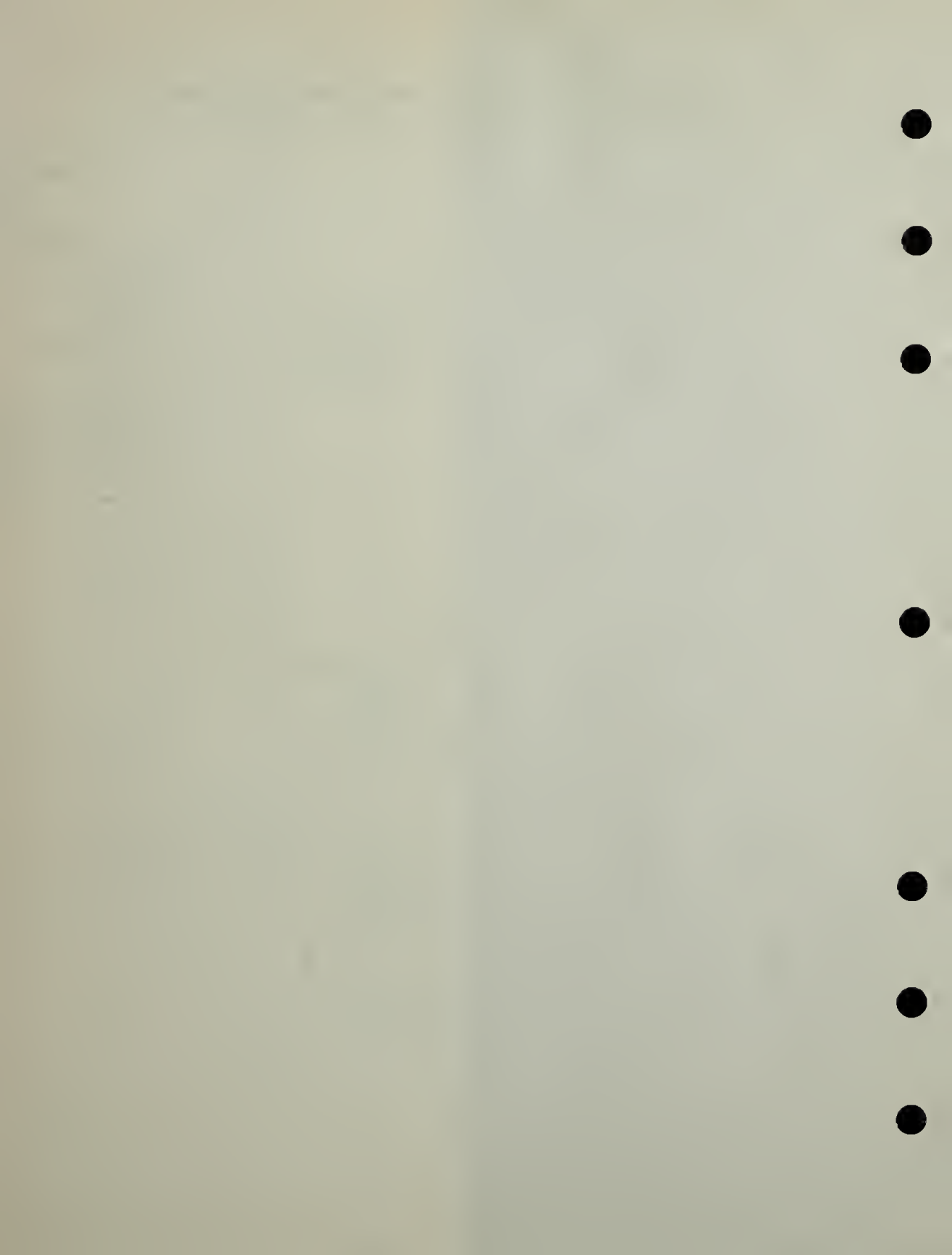
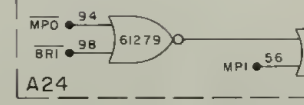
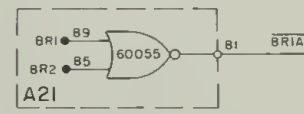
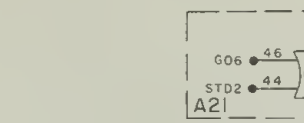
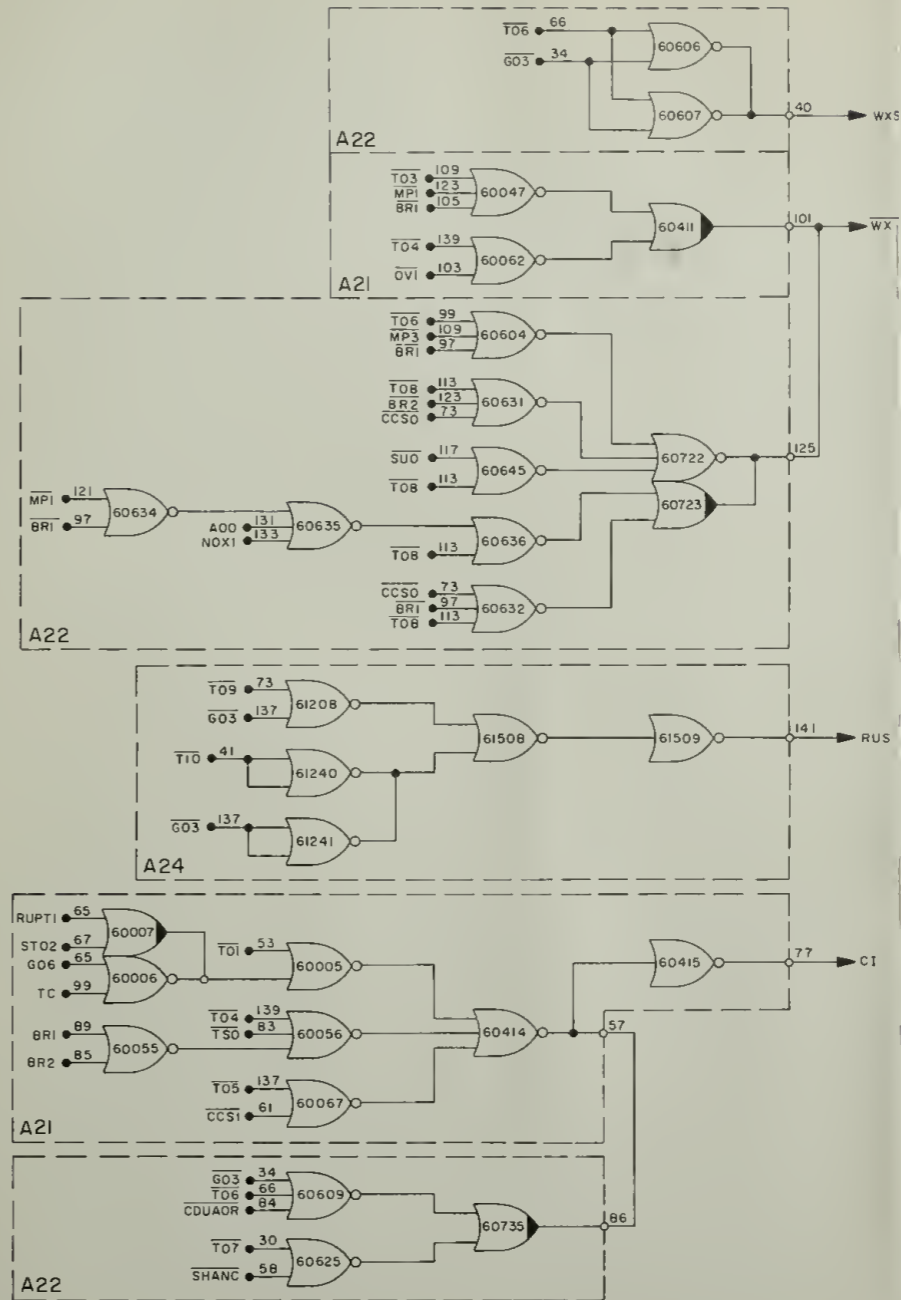
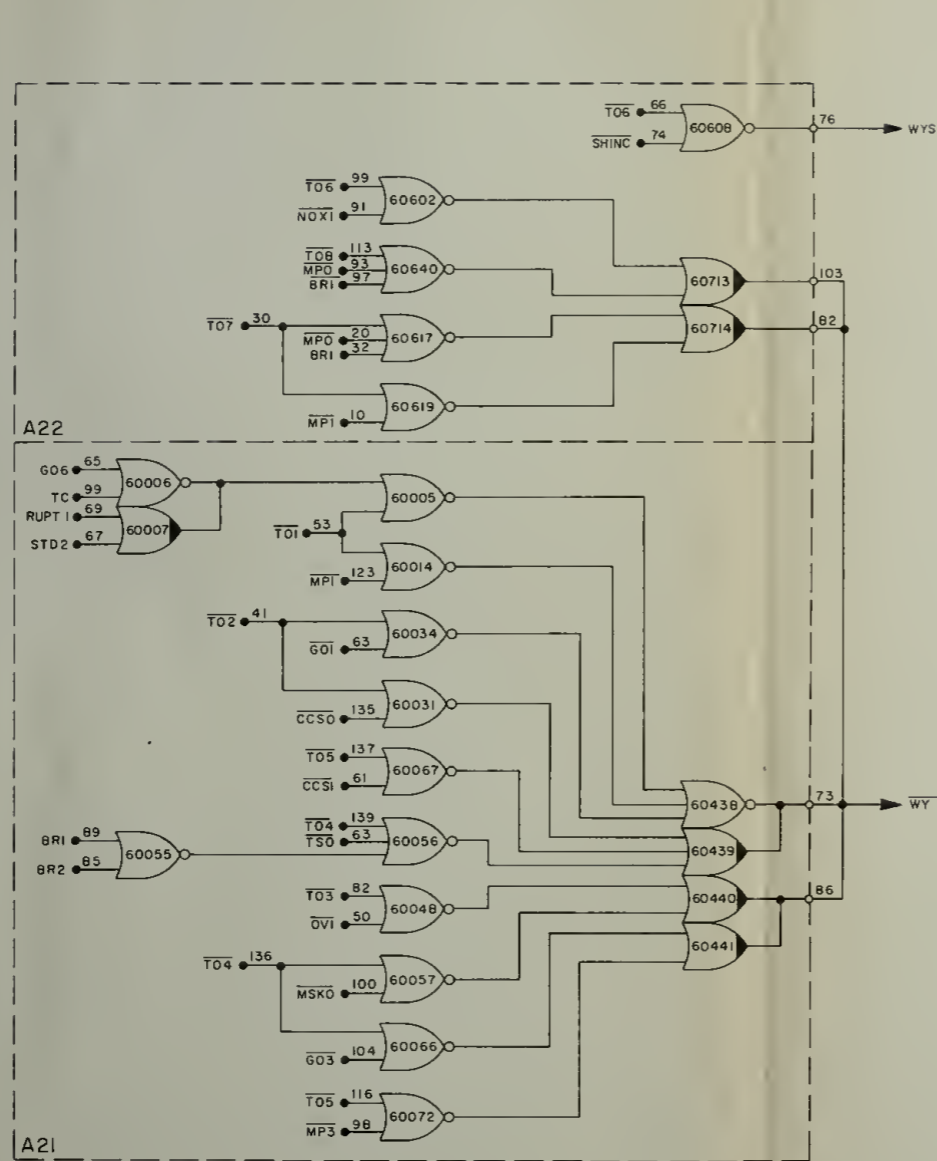


Figure 4-74. Register G Control Pulses





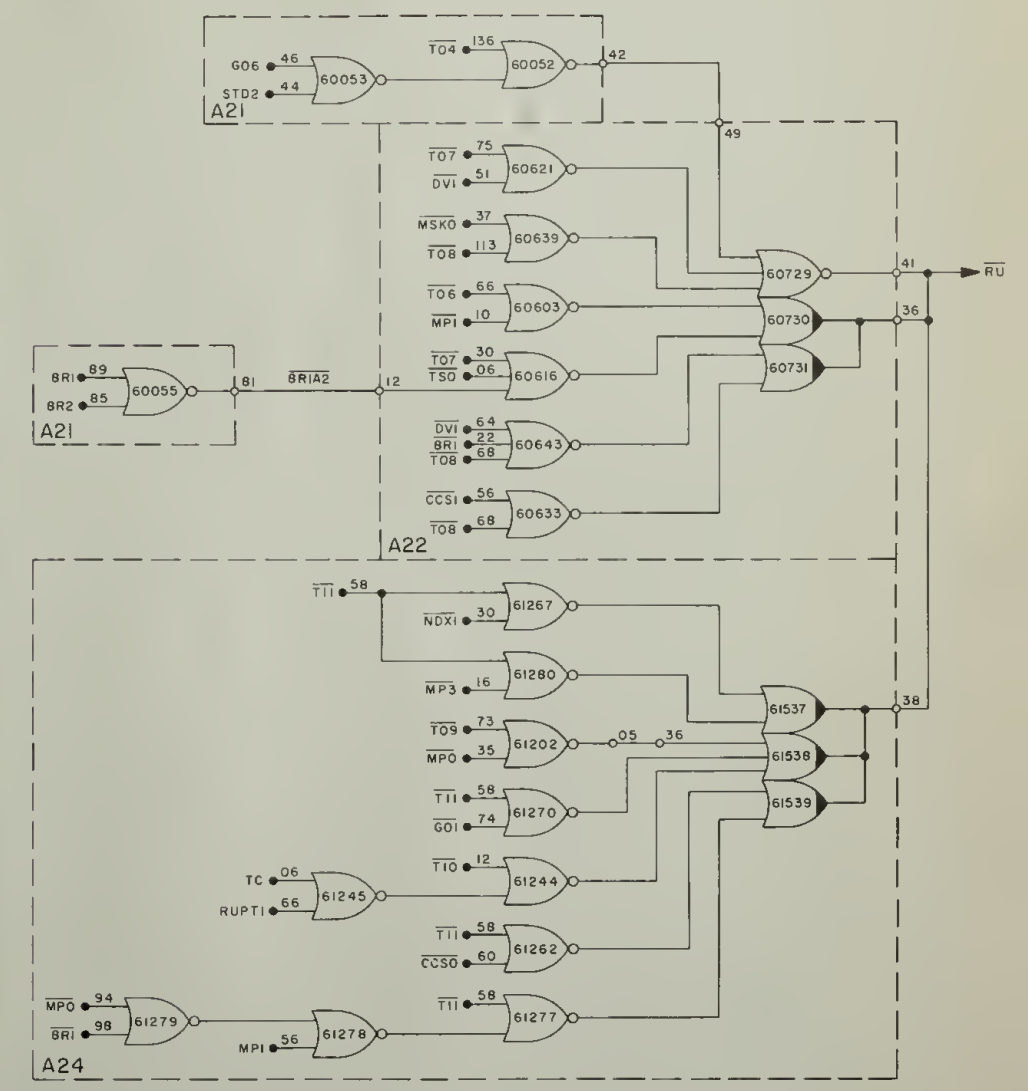
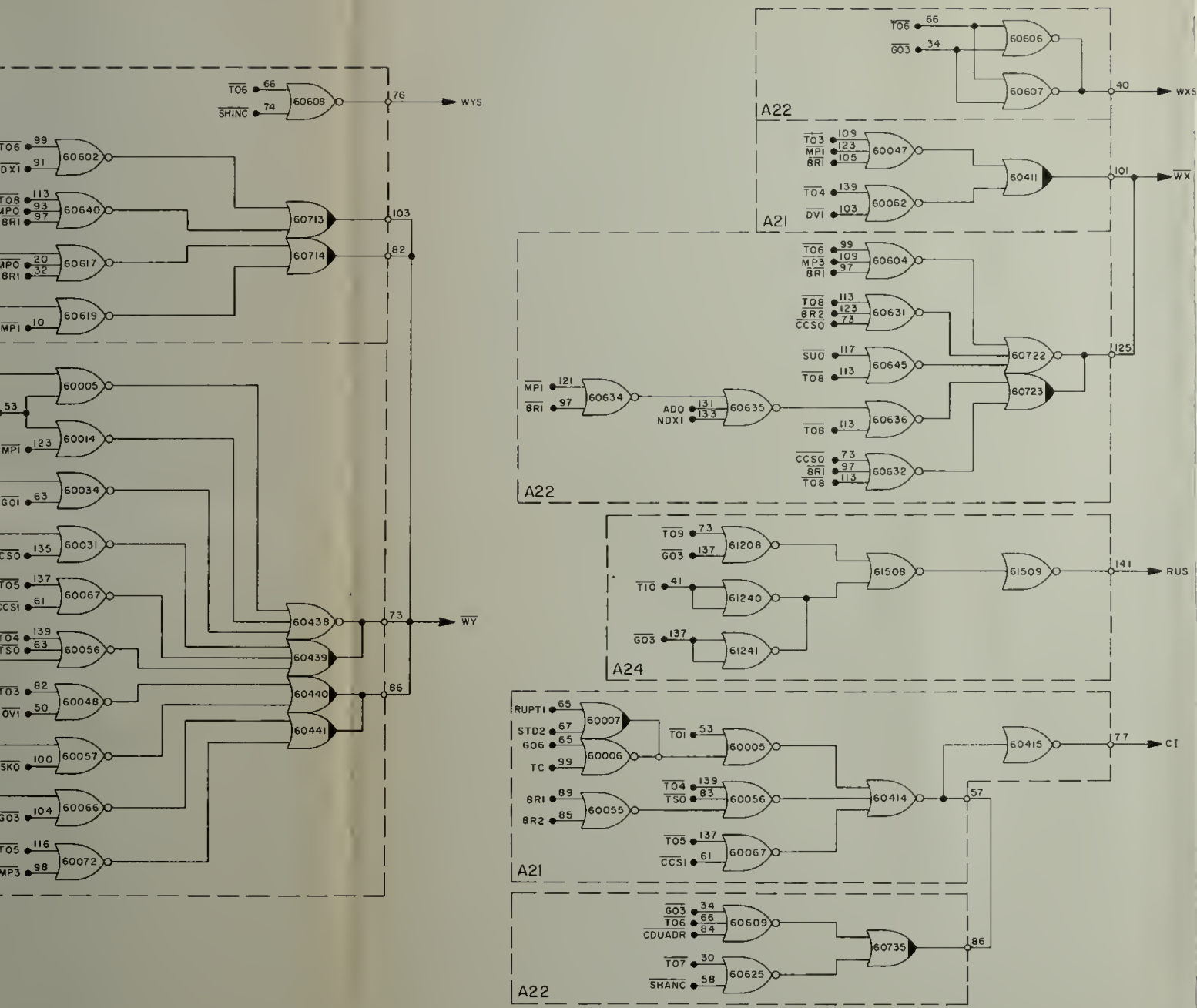
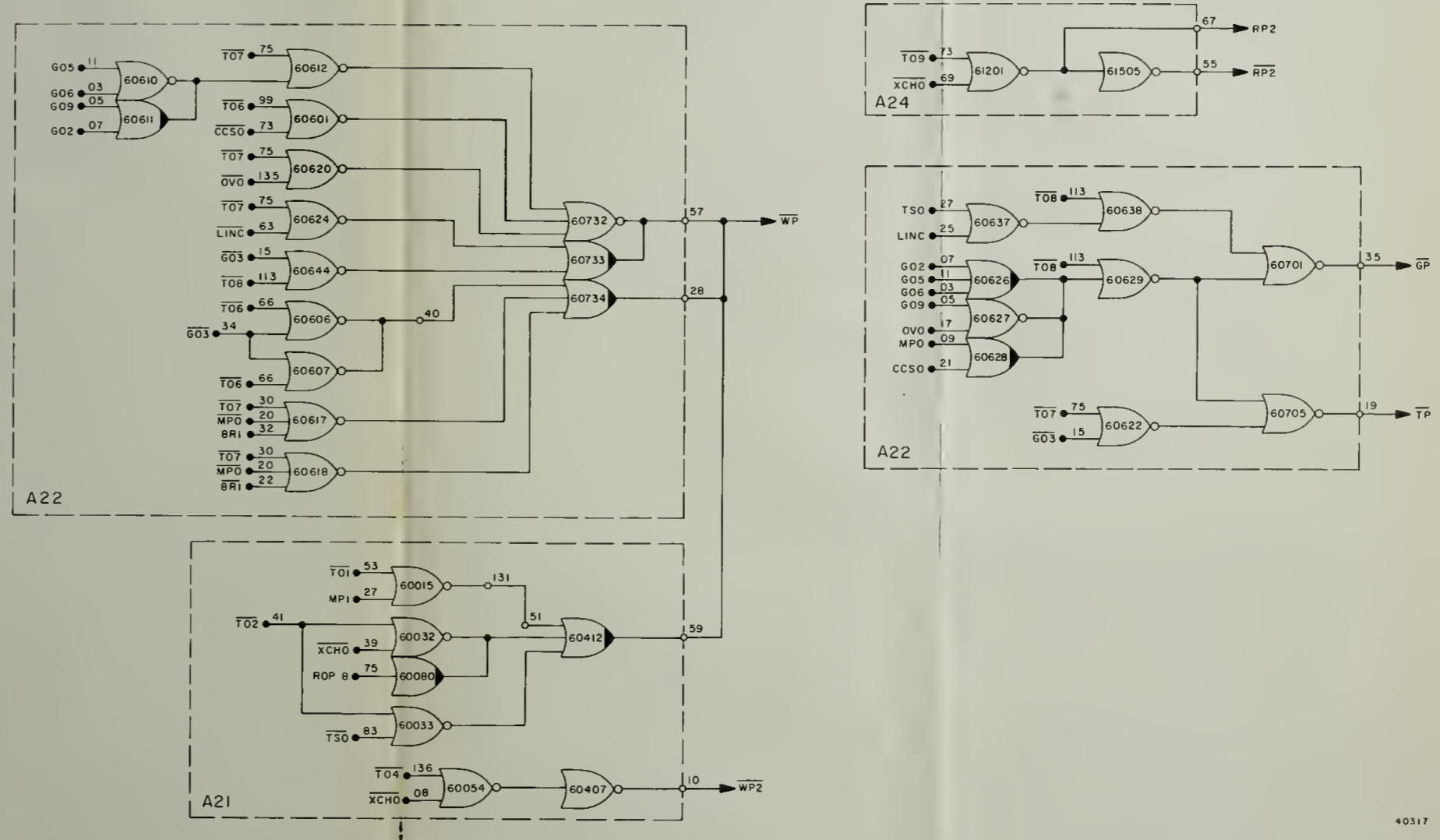


Figure 4-75. Adder (Registers X and Y) Control Pulses

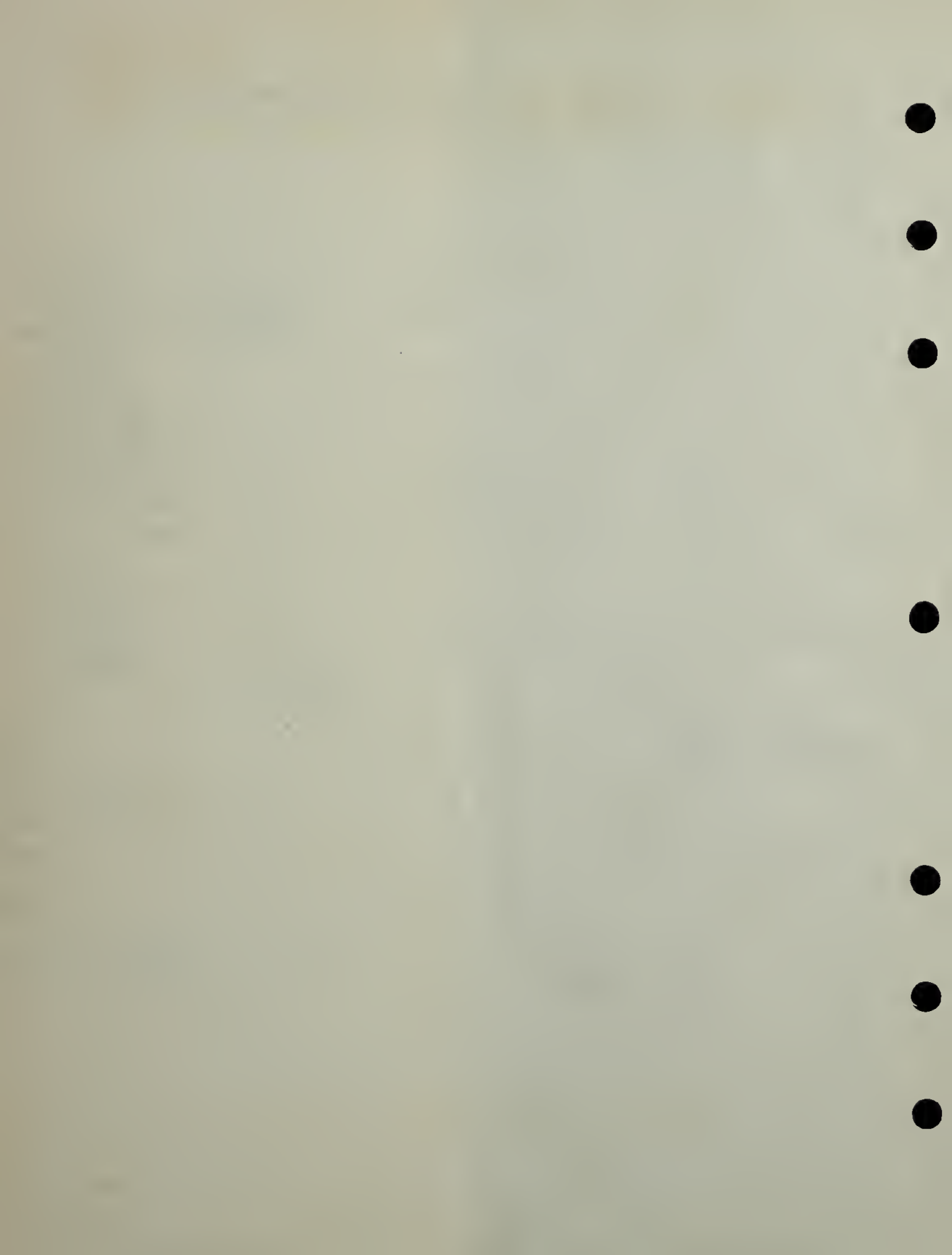


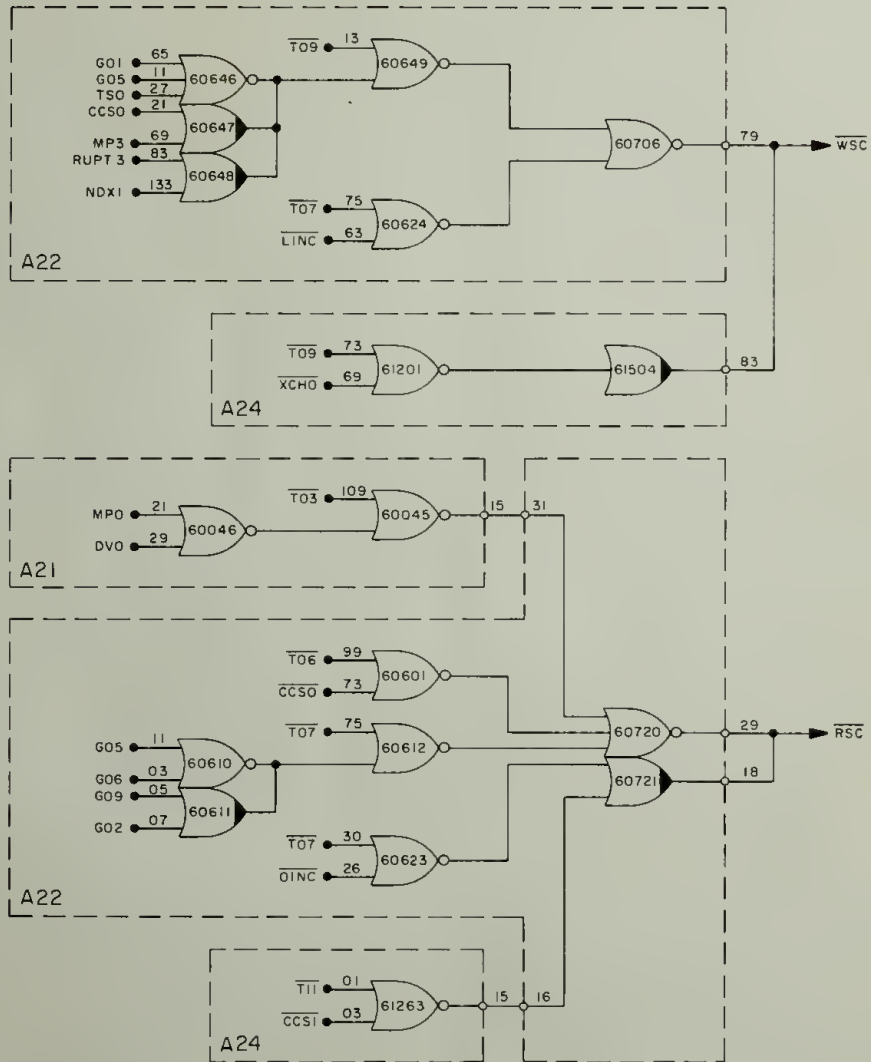


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Figure 4-76. Parity Logic Control Pulses







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Figure 4-77. Addressable Registers Control Pulses

Instruction GO, generated by signal GOJAM, initiates the execution of the AGC program at address location 2030 in fixed memory, which is determined by control pulse RSTRT. Instruction GO and timing pulses T01 and 234 enable gates 60016 and 60017 (figure 4-78), which produces control pulse RSTRT.

At the completion of a subinstruction the AGC is alerted for the next subinstruction by control pulse NISQ. For example, at action 11 of subinstruction STD2 control pulse NISQ is generated by gates 61260, 61261, 61517, and 61518 (figure 4-79). This control pulse is sent to the new instruction flip-flop (FF64005-64006) to initiate the next instruction.

During the execution of an add or subtract subinstruction, gates 61270 and 61501 are enabled and produce control pulse WOVC (figure 4-80). Control pulse WOVC is sent to the overflow and underflow detection gate. Should overflow or underflow occur, incremental pulses will be produced by the appropriate detection gate and a PINC or MINC command will be generated to increment or decrement the overflow counter. The execution of a PINC, MINC, or SHINC command causes gates 61240,

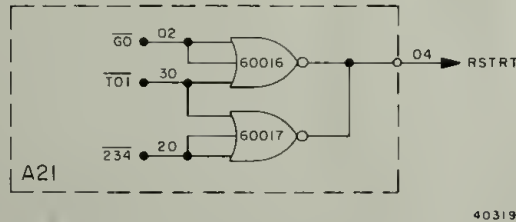


Figure 4-78. Control Pulse RSTRT

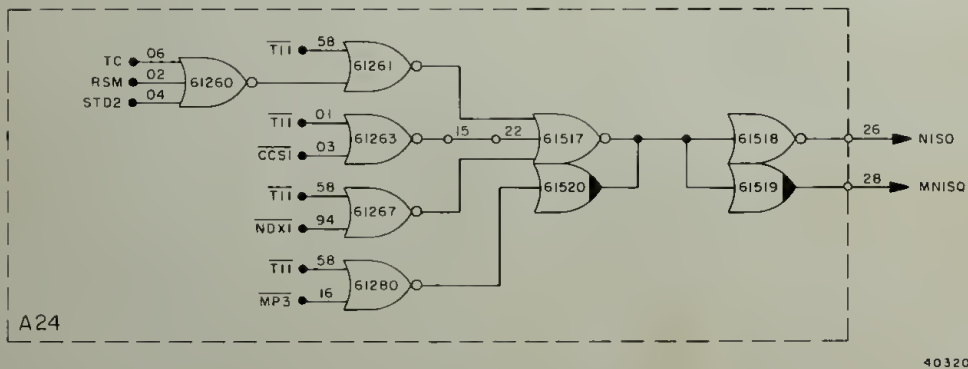
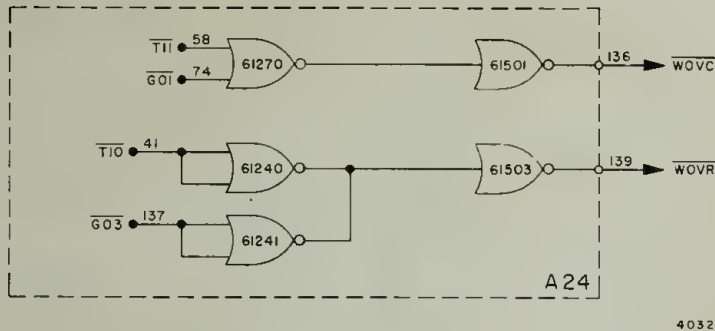


Figure 4-79. Control Pulse NISQ



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Figure 4-80. Control Pulses  $\overline{WOVc}$  and  $\overline{WOVr}$

61241, and 61503 to generate control pulse  $\overline{WOVr}$ . This control pulse enables the overflow counter test gate in counter priority control, allowing the proper counter to be incremented.

Control pulse  $\overline{WOVl}$  is generated when overflow or underflow occurs during the instructions specified by the inputs to the gates on figure 4-81. Control pulse  $\overline{WOVl}$

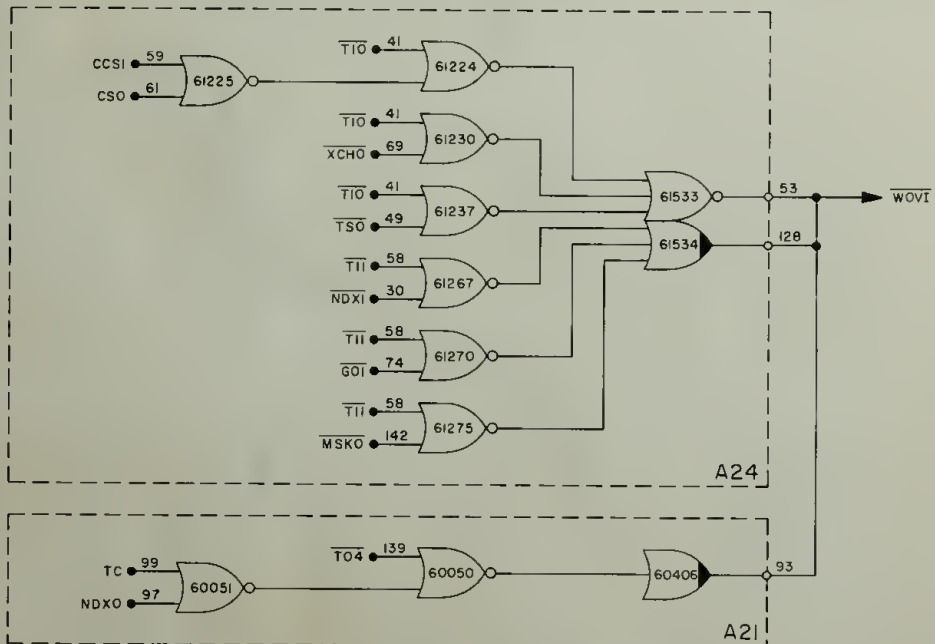


Figure 4-81. Control Pulse  $\overline{WOVl}$

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sets the OVF/UNF interrupt/inhibit flip-flop in the sequence generator. The output of this flip-flop prevents a program interruption until the overflow counters have been incremented or decremented.

The address transfer gates in counter priority control transfer the address of the counter to be incremented or decremented to register S. To accomplish this, the address transfer gates must receive control pulse RSCT. This control pulse is produced when gate 60013 (figure 4-82) receives timing pulses T01, 234 and signal NC13.

An AGC program can be interrupted in favor of a program of higher priority. Signal  $\overline{\text{RUPTOR}}$  is produced by the priority chain and sent to the sequence generator to execute instruction RPT. Execution of instruction RPT1 prepares the AGC for the interrupt program and initiates the execution of subinstruction RUPT3. At action 2

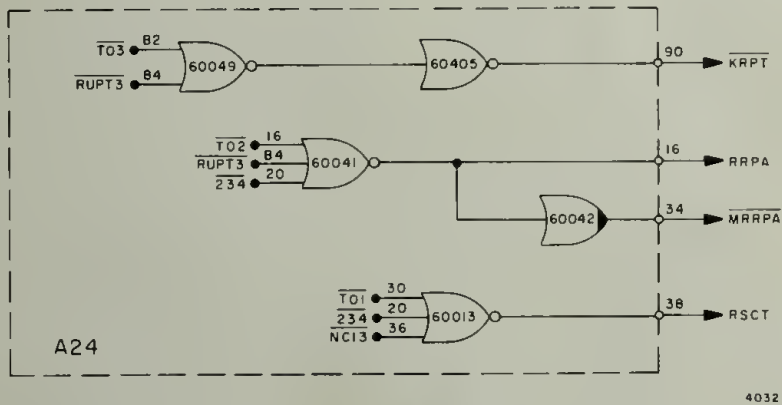


Figure 4-82. Control Pulses  $\overline{\text{KRPT}}$ , RRPA, and RSCT

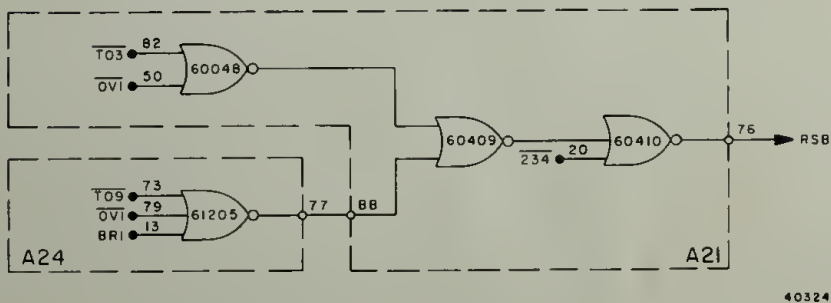


Figure 4-83. Control Pulse RSB

of subinstruction RUPT3, control pulse RRPA is produced by gate 60041 (figure 4-82) and, in conjunction with write pulse WZ, transfers the address of the interrupt program to register Z. At action 3 of the same subinstruction control pulse KRPT is produced by gates 60049 and 60405. This control pulse clears the request flip-flop that initiated the program interrupt.

Control pulse RSB is generated by gates 60048, 60049, and 60410 (figure 4-83) during action 3 of subinstruction DV1 and causes the octal quantity 100000 to be placed on the write lines. This action accomplishes one of the required manipulations for the completion of a divide instruction.

During the execution of subinstruction CCS0 it is necessary to test for the quantity minus zero. Control pulse  $\overline{\text{TMZ}}$  is produced at the time of signal  $\overline{\text{T07}}$  during a CCS0 subinstruction by gates 60613, 60614, 60704 (figure 4-84) and sent to the minus zero test gate. This test is necessary to select the proper set of control pulses for the execution of subinstruction CCS0.

Control pulses RB1 and RB2 (figure 4-85) are special control pulses generated for use during subinstructions MP0, DV0 and CCS0. Both control pulses are used to accomplish specific manipulations during the appropriate subinstruction. During the execution of counter increment instruction PINC, control pulse RB1 causes the quantity plus one (00001) to be placed on the write lines (gate 60063). This output is inhibited when angular data is being processed as indicated by signal  $\overline{\text{CDUADR}}$ .

Control pulses ST1 and ST2 (figure 4-86) adjust the order code prior to the execution of a desired subinstruction. For example, prior to the execution of subinstruction DV1, signals  $\overline{\text{T11}}$  and DV0 enable gates 61281, 61530, and 61532, which produces control pulse ST1. This control pulse is sent to the primary level state flip-flops to adjust the order code so the proper control pulses will be generated for the completion of subinstruction DV1.

During an MP0 and DV0 subinstruction, control pulses  $\overline{\text{TSGN}}$  and  $\overline{\text{TSGN2}}$  are generated to test the sign of the quantities used in multiplying and dividing. For

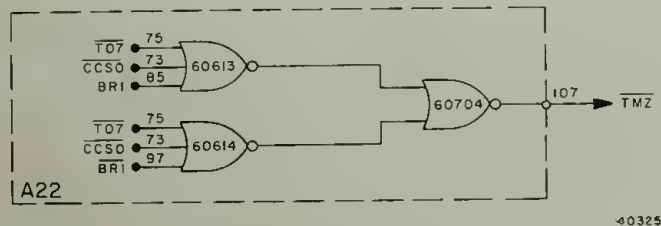
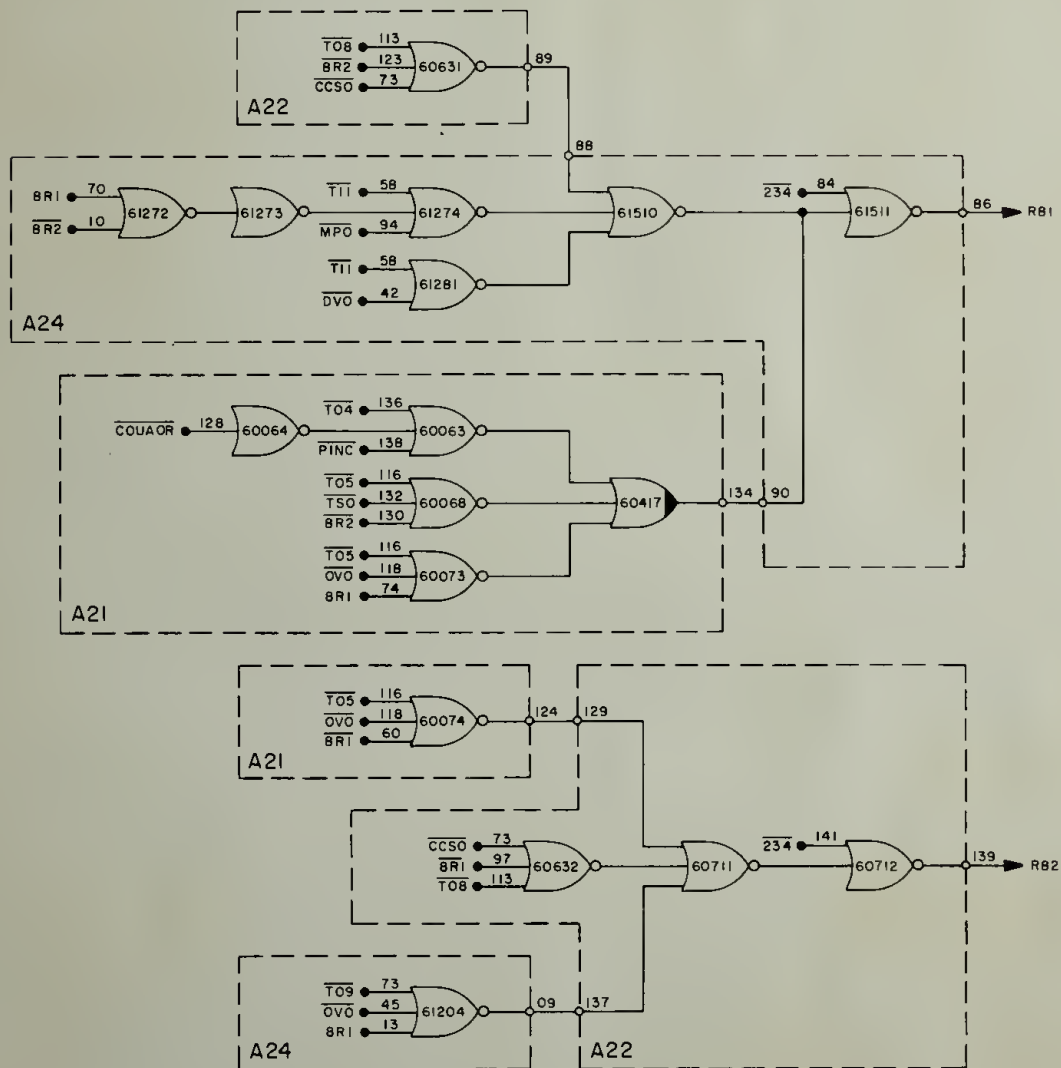


Figure 4-84. Control Pulse  $\overline{\text{TMZ}}$



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Figure 4-85. Control Pulses RB1 and RB2

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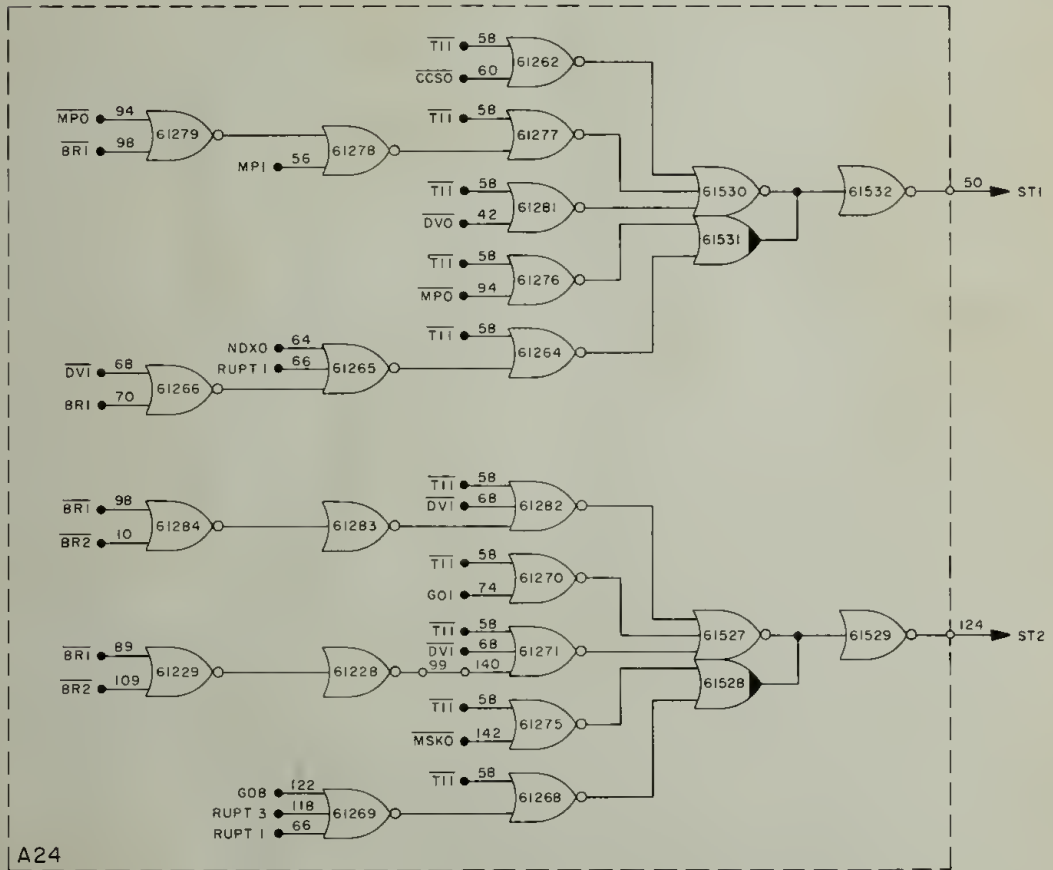
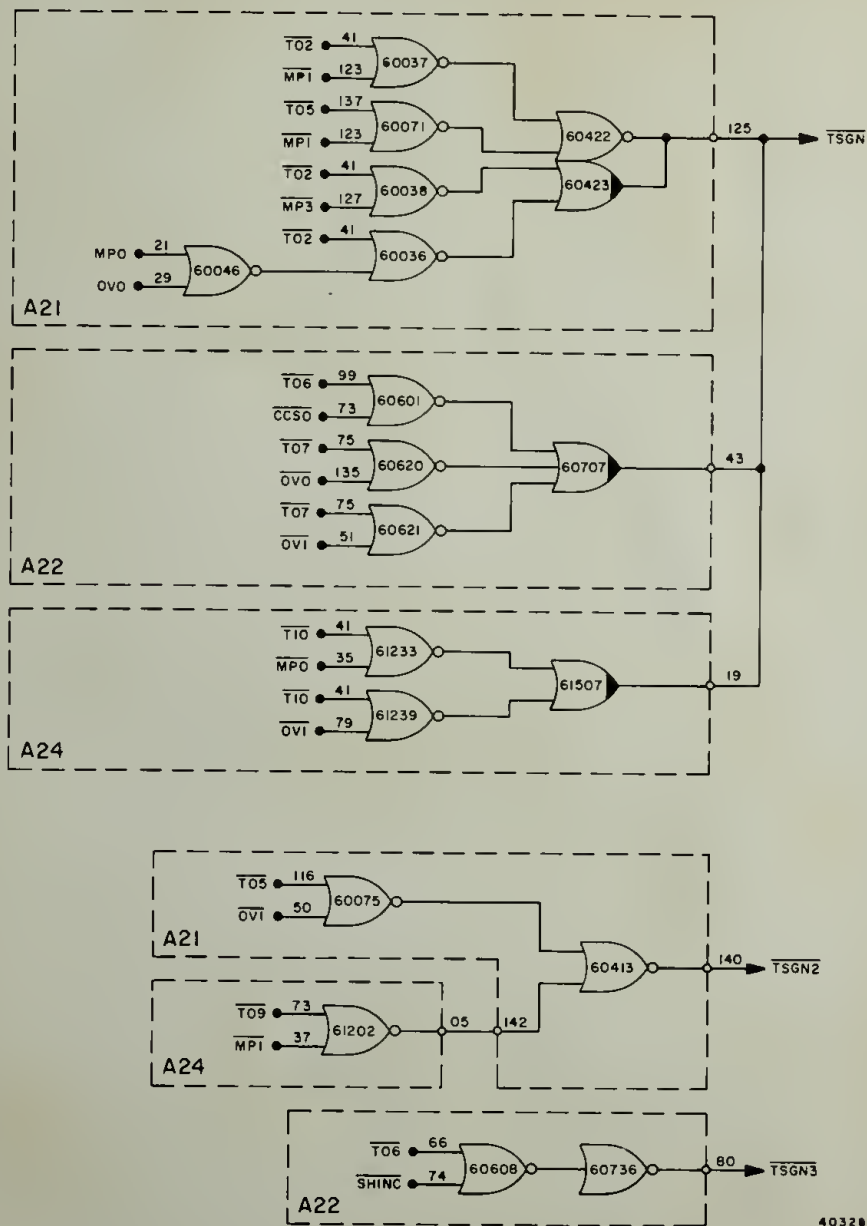


Figure 4-86. Control Pulses ST1 and ST2

example, during an MP0 subinstruction the signs of the multiplier and multiplicand are tested with control pulses  $\overline{TSGN}$  and  $\overline{TSGN2}$  produced at appropriate times by gates on figure 4-87 to insure both quantities have the same sign. If the signs are incorrect, one quantity is shifted to correct the sign. Subinstruction MP0 then proceeds to completion of the step. The same process is employed during a DV0 subinstruction with one exception, an octal quantity is added to the quantity with the incorrect sign. The subinstruction can then proceed toward the completion of that required step. A CCS0 subinstruction also employs control pulse  $\overline{TSGN}$  to test the sign of the accumulator and determines the proper set of control pulses required to complete subinstruction CCS0.





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Figure 4-87. Control Pulses TSGN, TSGN2, and TSGN3

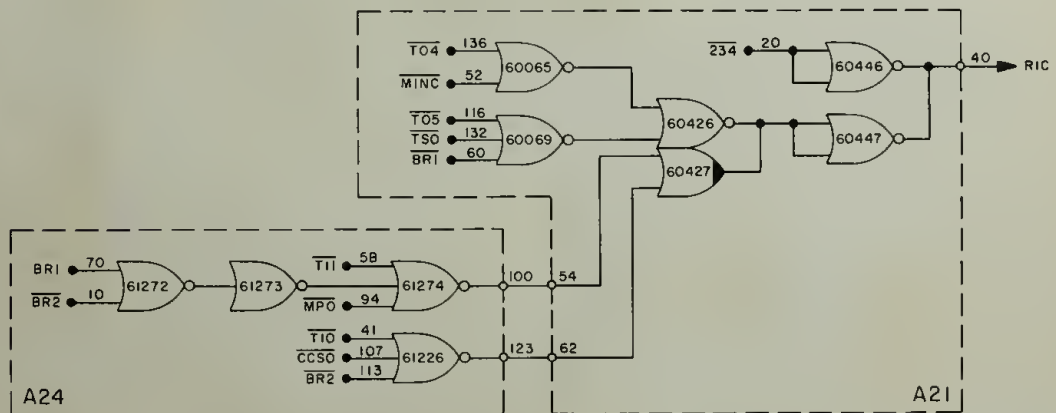
Control pulse  $\overline{\text{TSGN3}}$  is generated during a SHINC command to test for the flag bit (bit position 16 of a parallel word) of the uplink gate. When this flag is present signal  $\overline{\text{RP5}}$  is produced by the uplink gate and commands the priority chain to produce signal  $\overline{\text{RUPTOR}}$ .

Control pulse RIC (figure 4-88) transfers the quantity minus one (octal 177776) to the write lines at the request of the appropriate subinstruction to correct the contents of the accumulator prior to completion of the subinstruction.

A multiplication operation requires the execution of subinstruction MP1 six times. At the end of each execution the contents of the multiply counter are decremented by one by means of control pulse CTR. Control pulse CTR is generated at the time of signal  $\overline{\text{T10}}$  during subinstruction MP1 by gates 61233 and 61239 (figure 4-89). Decrementing continues until the multiply counter contains zero, at which time subinstruction MP3 is executed.

Control pulse  $\overline{\text{TRSM}}$ , which is generated at action 10 of an NDX0 subinstruction by gates 61231 and 61502 (figure 4-90), is applied to the RSM gate. This control pulse, coincident with address 0025, produces an output from the RSM gate which allows the AGC to return to the original program.

Control pulse R22 is generated by gate 60012 (figure 4-91) at the time of signal  $\overline{\text{T01}}$  during subinstruction DV1, and causes address 0022 to be placed on the write lines. This address is entered in register S and results in a cycle-left operation of any data entered into register G.



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Figure 4-88. Control Pulse RIC

Control pulse R24 is generated at the time of signal  $\overline{T01}$  during instructions RUPT and RSM by gates 60011 and 60010. During instruction RUPT the address of the subinstruction (the interrupted program) to be executed next is transferred from register Z to memory location 0024. At the completion of the interrupt program subinstruction RSM (address 0024) is written into register S. The information contained at address 0024 is now returned to the central processor.

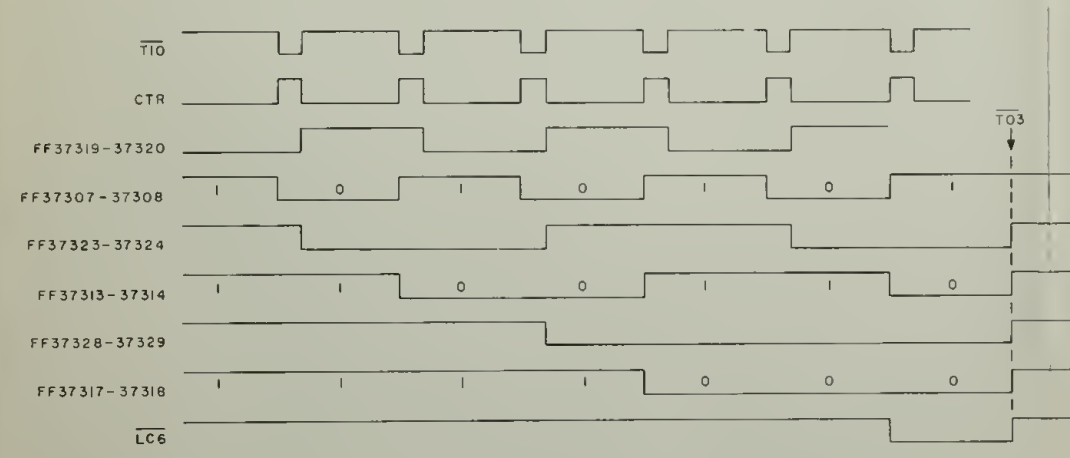
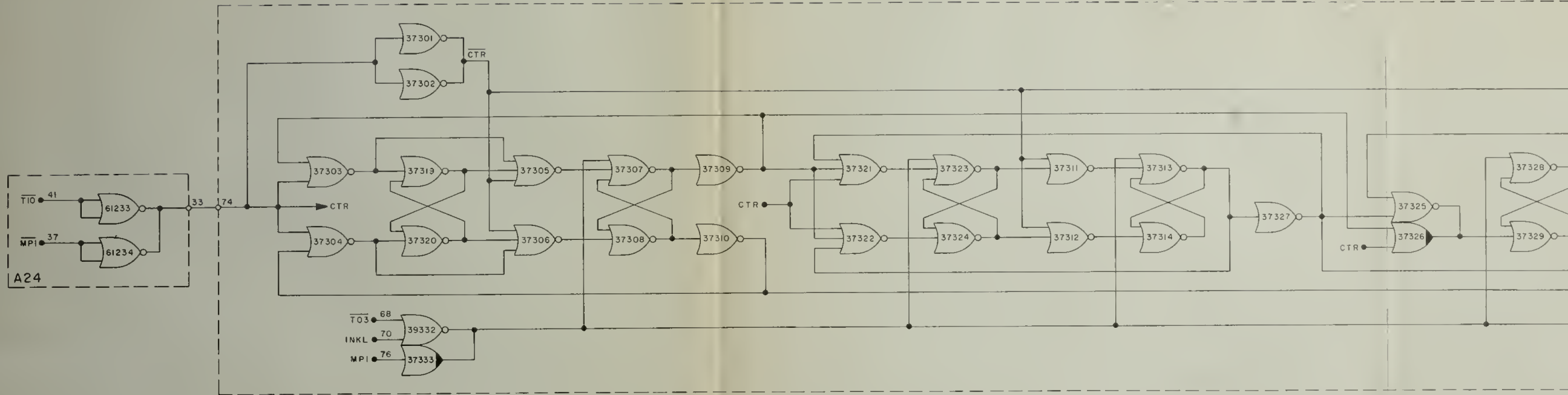
The G generator (figure 4-92) provides the AGC with control pulses G01 through G09, which represent the logic combinations of various instructions. For example, signal G01 is a logic ONE when an add instruction (AD0) or subtract instruction (SU0) is being executed. Likewise, signal G02 is a logic ONE during instruction MSK0 or AD0 or SU0. The remaining outputs can be determined from figure 4-92. Signal G03 is used as an enabling signal (logic ZERO) during counter instructions PINC, MINC, or SHINC.

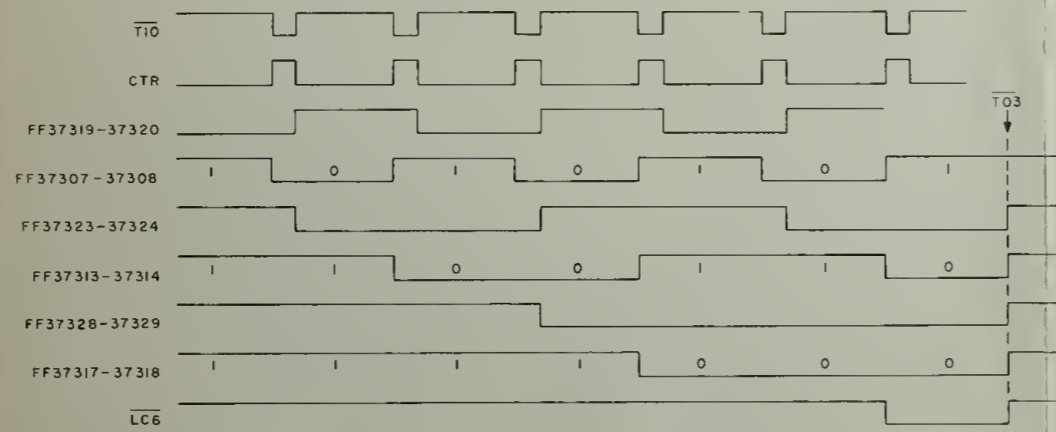
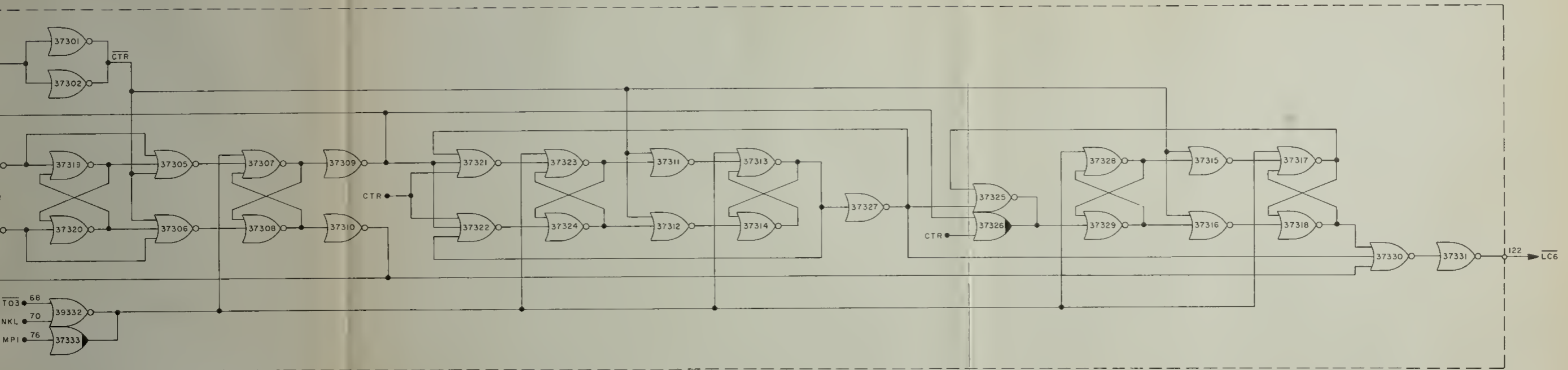
Control pulse  $\overline{T0V}$  is generated at the time of signal  $\overline{T02}$  of a TS0 subinstruction by gates 60033 and 60402 (figure 4-93). This control pulse tests the accumulator for overflow or underflow and transfers the contents of write amplifiers 16 and 15 to the sequence generator and executes the appropriate branching function.

Signal RB14, generated by gate 61243 (figure 4-94), is a special control pulse that enters the octal quantity 020000 in the accumulator at action 10 of subinstruction MP0. This quantity corrects the contents of the accumulator prior to completion of subinstruction MP0.

4-8.2.10 Branching Control. It is necessary to test the sign bit of the accumulator during the execution of subinstruction CCS0. It is necessary also to test for the quantity minus zero. The results of these two tests are used to select the proper set of control pulses for the execution of subinstruction CCS0.

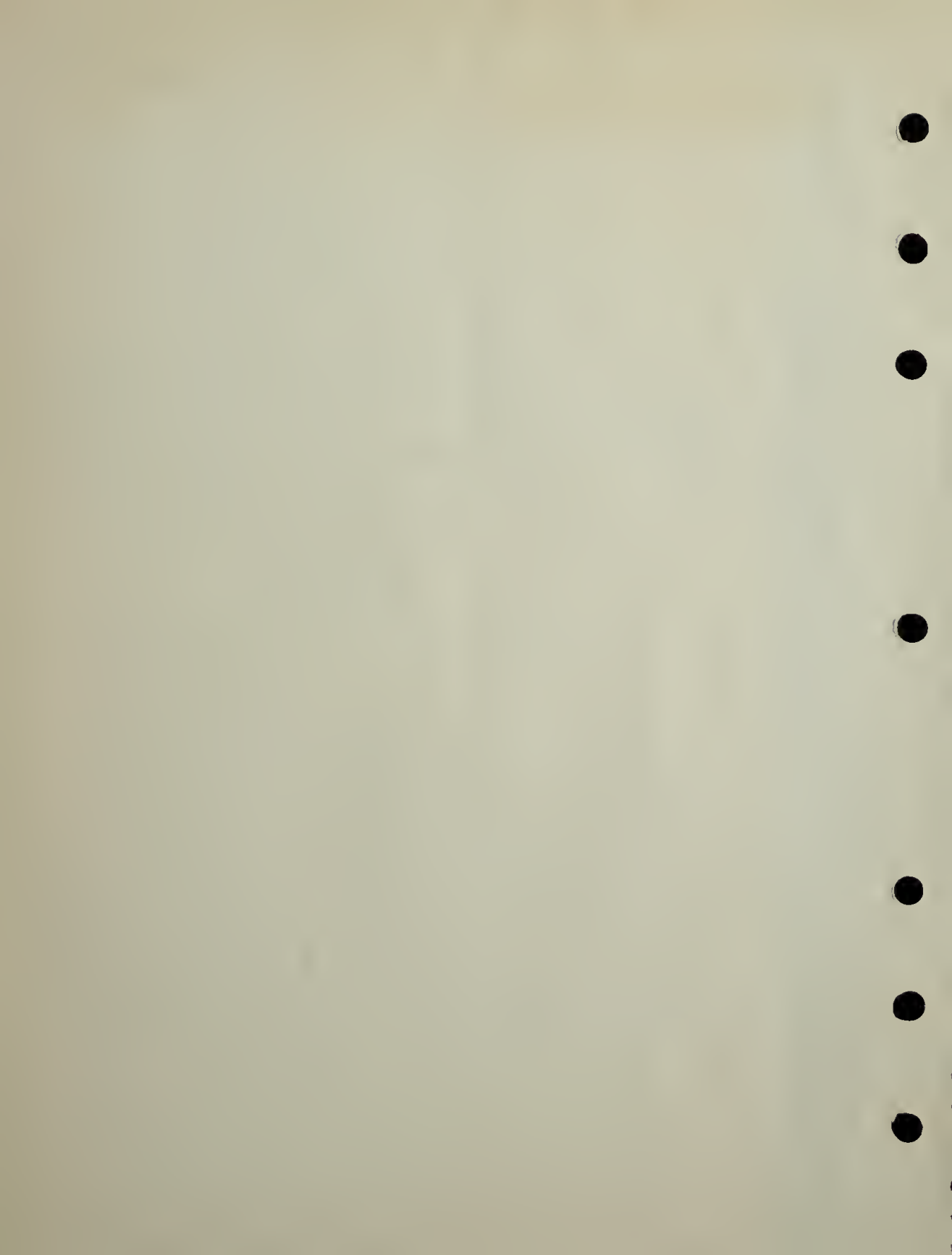
The test for sign is accomplished with control pulse  $\overline{TSGN}$ , which is generated at action 6 of subinstruction CCS0. Signal  $\overline{TSGN}$  is sent to sign 1 test gate 65163 (figure 4-95), which also receives signal  $\overline{WL16}$ . Signal BR1 (a logic ONE) is produced by the branch flip-flops if signal  $\overline{WL16}$  is a logic ZERO. Signal BR1 is supplied to the control pulse generator, where it is used in conjunction with subinstruction command CCS0 to produce control pulses  $\overline{RB}$  and  $\overline{TMZ}$  at action 7. Signal BR1 is not generated and control pulses  $\overline{RC}$  and  $\overline{TMZ}$  are produced at action 7 if signal  $\overline{WL16}$  is a logic ONE.





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Figure 4-89. Control Pulse CTR



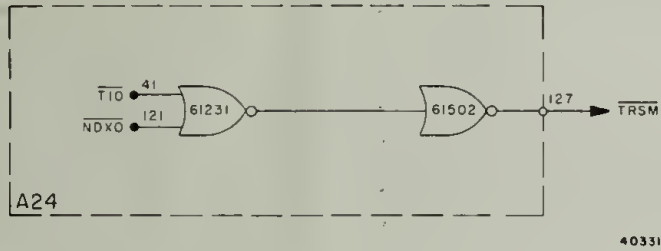


Figure 4-90. Control Pulse  $\overline{\text{TRSM}}$

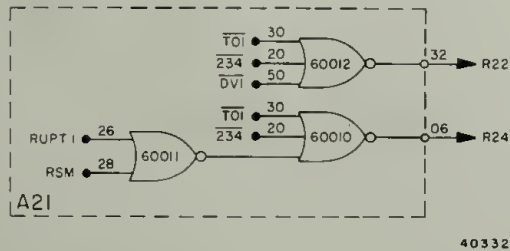


Figure 4-91. Control Pulses R22 and R24

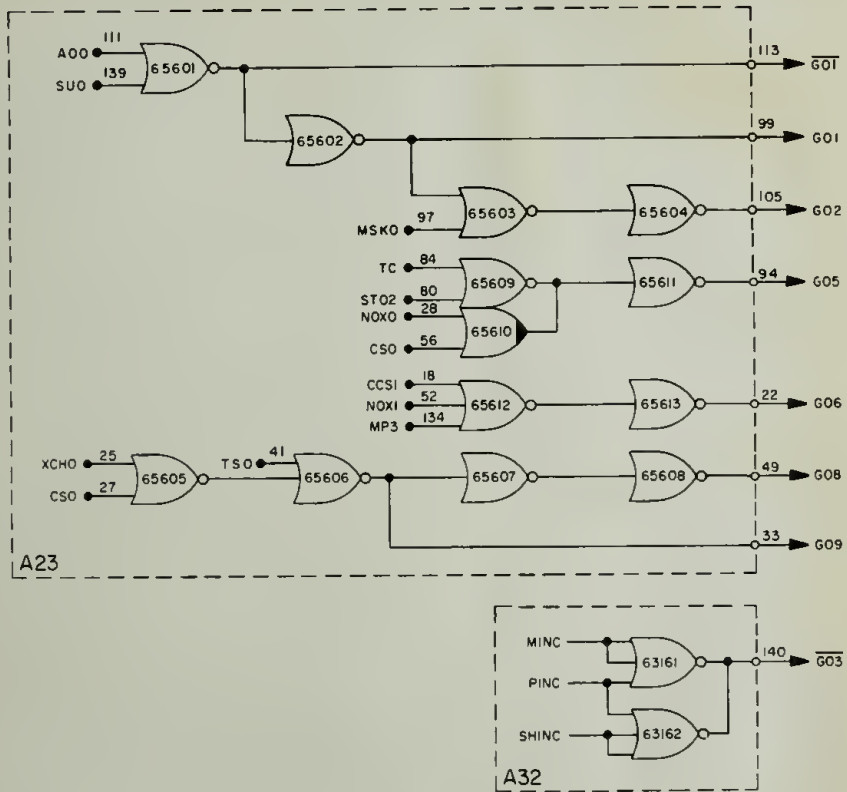


Figure 4-92. G Generator

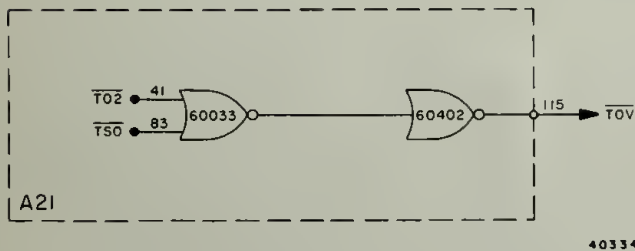


Figure 4-93. Control Pulse  $\overline{TOV}$

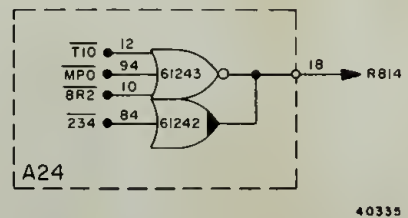
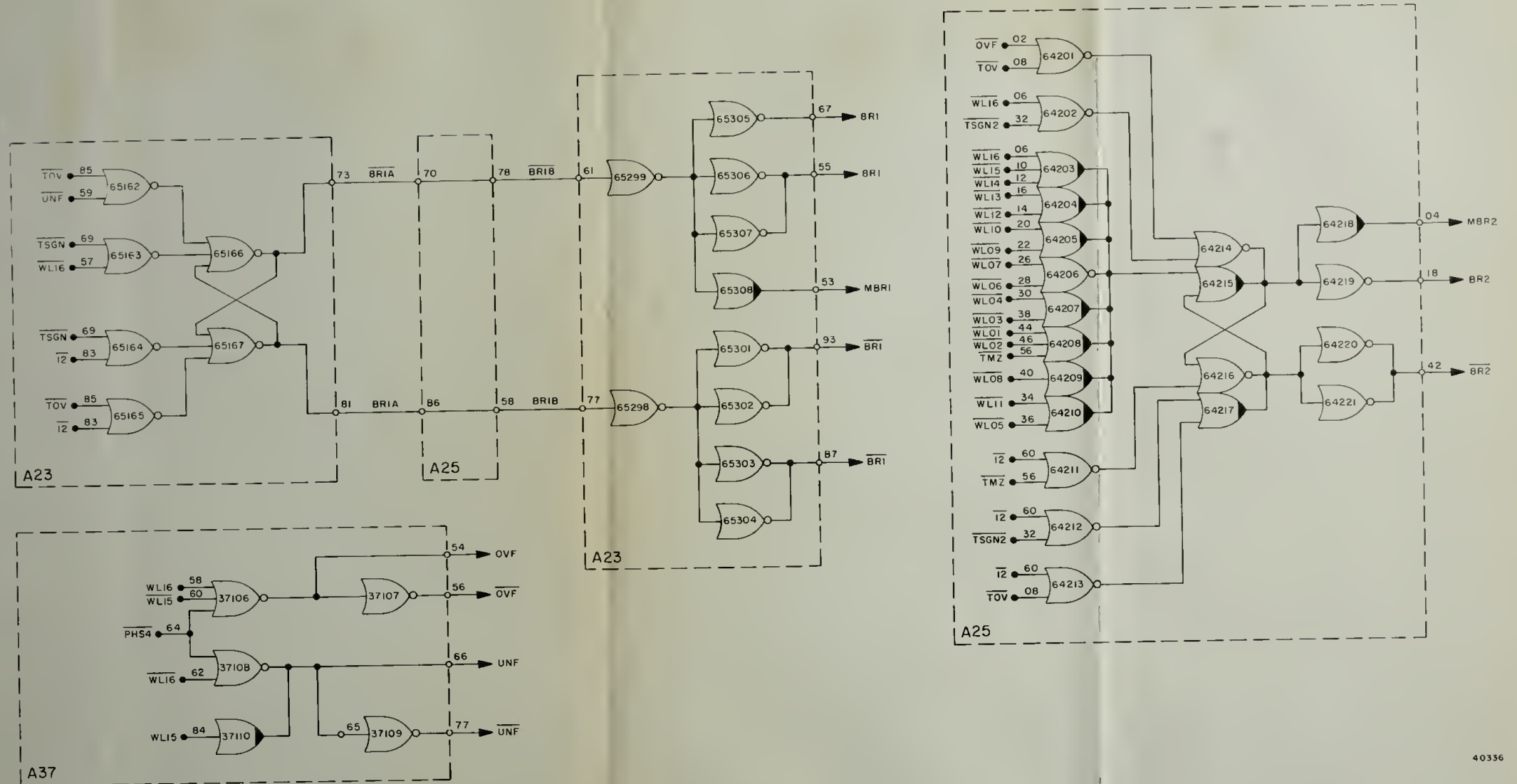


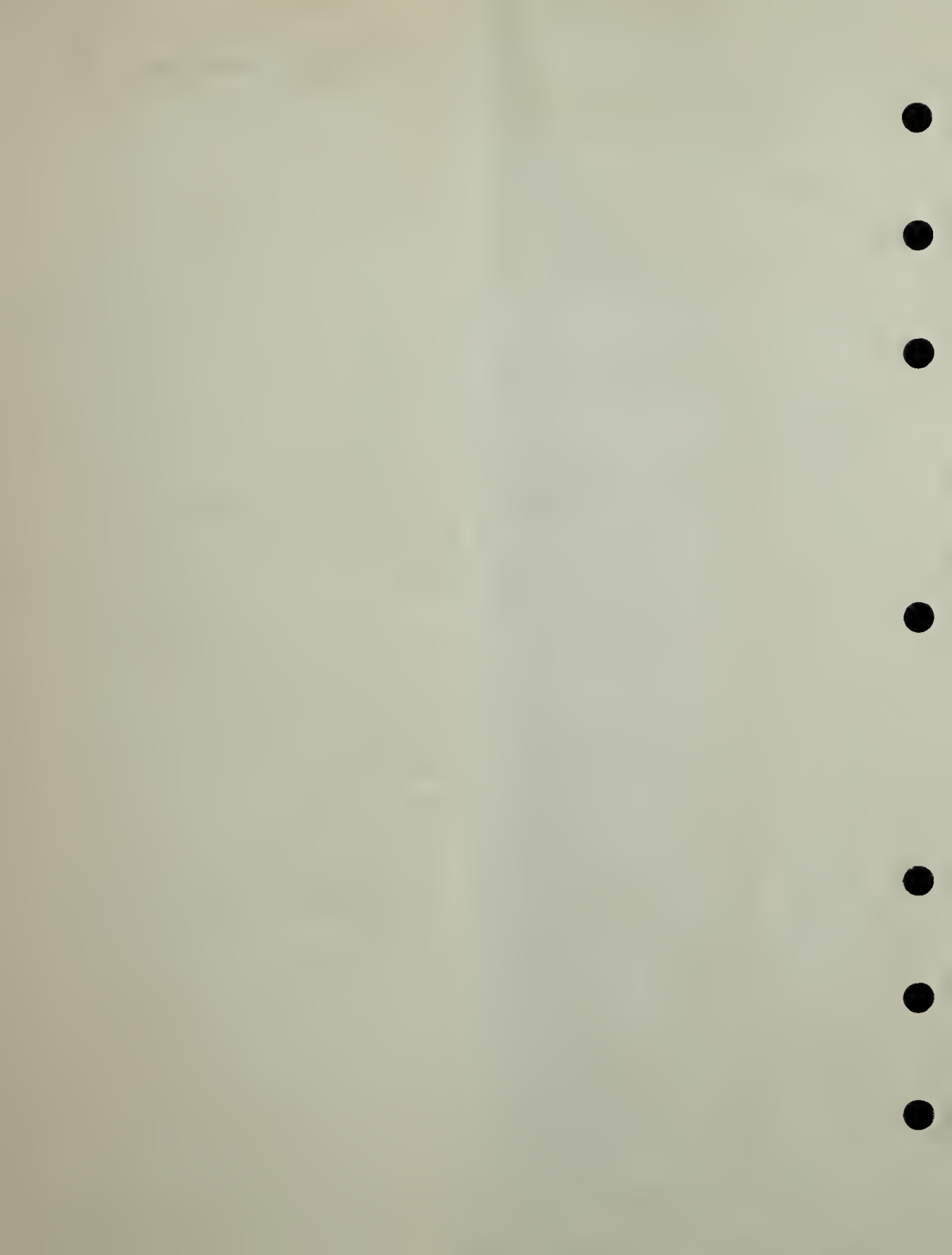
Figure 4-94. Control Pulse RB14





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Figure 4-95. Branch Flip-Flops



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Signal  $\overline{\text{TMZ}}$  is sent to the minus zero test gate 64211, which also receives signals  $\overline{\text{WL01}}$  through  $\overline{\text{WL16}}$ . Signals  $\overline{\text{BR1}}$  and  $\overline{\text{BR2}}$  (logic ONE's) are produced by the branch flip-flops if signals  $\overline{\text{WL01}}$  through  $\overline{\text{WL16}}$  are all logic ZERO's. Signals  $\overline{\text{CCS0}}$ ,  $\overline{\text{BR1}}$ , and  $\overline{\text{BR2}}$  control the control pulse generator to produce control pulses  $\overline{\text{RB1}}$ ,  $\overline{\text{RB2}}$ ,  $\overline{\text{WX}}$ ,  $\overline{\text{GP}}$ , and  $\overline{\text{TP}}$  at action 8. If  $\overline{\text{BR1}}$  is generated and  $\overline{\text{BR2}}$  is not generated, control pulses  $\overline{\text{RB2}}$ ,  $\overline{\text{WX}}$ ,  $\overline{\text{GP}}$ , and  $\overline{\text{TP}}$  are produced. If  $\overline{\text{BR1}}$  and  $\overline{\text{BR2}}$  are not produced, control pulses  $\overline{\text{GP}}$  and  $\overline{\text{TP}}$  are generated. If  $\overline{\text{BR2}}$  is present and  $\overline{\text{BR1}}$  is not, control pulses  $\overline{\text{RB1}}$ ,  $\overline{\text{WX}}$ ,  $\overline{\text{GP}}$ , and  $\overline{\text{TP}}$  are generated.

Branching functions are utilized also during subinstruction TS. Tests for overflow or underflow are conducted at action 2 with the overflow and underflow test gate by control pulse  $\overline{\text{TOV}}$  and signals  $\overline{\text{UNF}}$  and  $\overline{\text{OVF}}$ .

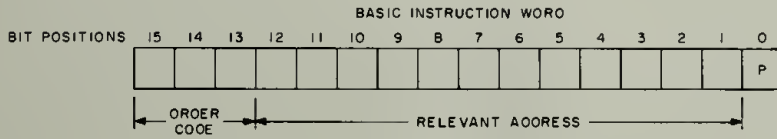
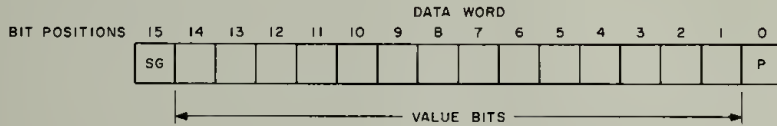
4-8.3 CENTRAL PROCESSOR. The central processor consists of nine 16 bit flip-flop registers the write amplifiers and parity logic. The flip-flop registers to be discussed are the four addressable registers (A, Q, Z, and LP), register B, the address register (S and SQ), memory buffer register G, and registers X and Y which comprise the adder. Functionally, the central processor performs all arithmetic operations required of the AGC, buffers all information coming from and going to memory, checks for correct parity on all words coming from memory, and generates parity for all words written into memory.

Each flip-flop register consists of 16 bit positions. The service gates associated with each register generate write, clear, and read control signals, which allow information to flow from memory to the central processor, between registers of the central processor, from the central processor to other portions of the AGC, or from the central processor to memory.

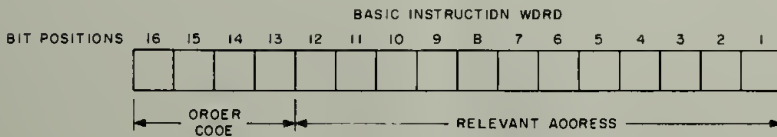
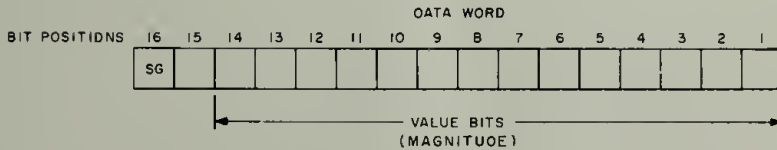
Registers A, Q, and LP and registers X and Y, which comprise the adder, are primarily involved in arithmetic operations. Registers B and Z are essentially storage elements in that they store the operation or step to be performed next in the program. Registers S and SQ contain the address (location in memory) of the data to be worked with the order code of the instruction to be executed.

Data is transferred between registers of the central processor or from the central processor to other portions of the system through the write amplifiers. The write amplifiers also function to place inputs from other sections of the AGC (e.g., memory and priority control) or from the CTS on the write lines.

Data words and basic instruction words consist of 16 bits when stored in fixed or erasable memory. The bits are numbered 0 through 15, reading from right to left. As indicated on figure 4-96, bit position 0 is always reserved for the parity bit, P. Data words stored in fixed or erasable memory consist normally of a sign bit (SG) in position 15, 14 value bits, and the parity bit. A ZERO in position 15 represents a plus sign, a ONE a minus sign. A basic instruction word is composed of a 3-bit order code in bit positions 15 through 13, a 12 bit address code (relevant address) in bit positions 12 through 1, and the parity bit. Data words and basic instruction words in other registers of the central processor contain 16 bits, which are numbered 1 through 16,



*a. word format for Memory*



*b. word format for Control Processor registers*

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**Figure 4-96. Word Formats**

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reading from right to left. Data words contain a sign bit and 14 value bits. Bit 15 is used for overflow and underflow. Basic instruction words contain 4 order code bits and 12 relevant address bits.

The parity bit provides a simple means of detecting single errors (or any odd number of errors) during readout from fixed or erasable memory. If the number of ONE's contained in bit positions 1 through 15 is an even number, bit position 0 contains a ONE. This brings the total number of ONE's contained in a word to an odd number. If the number of ONE's contained in bit positions 1 through 15 is an odd number, bit position 0 contains a ZERO. This leaves the total number of ONE's contained in a word at an uneven number. Bit position 1 contains the lowest order digit and position 15 the highest.

A word transferred from memory to the memory buffer register in the central processor is tested for parity. A parity alarm is generated in case of incorrect parity, sent to the input-output section, and transferred to the display portion of the Display and Keyboards. In the event that the word is to be returned to memory, a parity bit is generated, entered into the memory buffer register, and, with the word, returned to memory. A parity bit is produced in the same manner for words from other registers in the central processor being transferred to memory.

The memory buffer register (register G) buffers all information read out of memory into the central processor and likewise buffers all information written into memory from the central processor.

4-8.3.1 Flip-Flop Registers Functional Description. The register service gates (figure 4-97) control the write-in, clear, and readout functions of the flip-flop registers. Write control signals are normally generated as a function of a write control pulse, such as signal  $\overline{WA}$ , from the sequence generator and timing pulse  $\overline{234}$  from the timer. Write control signals are produced also for registers A, Q, Z, and LP when, under program control, a memory address ( $XT0$ - $XB0$  through  $XT0$ - $XB3$ ) and write control signal  $\overline{WSC234}$  are present. Read signals are generated as a function of a read control pulse, such as  $\overline{RA}$ , and timing pulse  $\overline{234}$ . Read control signals are produced for the addressable registers when a memory address and read control signal  $\overline{RSC234}$  are present. Clear signals are generated usually by a write control signal and timing pulse  $\overline{12}$ . Clear signals occur coincident with the second 0.25 microsecond interval of the write signal (the write signal is approximately 0.75 microsecond wide). Thus, each register is cleared and then immediately written into. Registers Q, Z, and LP clear signals are produced by gating a write control signal and timing pulse  $\overline{12}$  or by gating write control signal  $\overline{WSC234}$  with a particular memory address. Registers S and SQ have no associated read gates. Information contained in registers S and SQ is available directly through output amplifiers. Register B has two read gates: one for direct and one for complemented readout.

Registers S and SQ service gates receive control signals from the timer, sequence generator, priority control, and the CTS. Timing pulses  $\overline{12}$  and  $\overline{234}$  and write control pulse  $\overline{WS}$  are gating functions for clear and write pulses  $\overline{WSG}$  and  $\overline{CSG}$ . All signals applied to register S and SQ service, with the exception of  $\overline{WS}$ , are gating functions for signals  $\overline{WSQG}$ ,  $\overline{WSQF}$ ,  $\overline{CSQG}$ ,  $\overline{SQ13}$ , and  $\overline{SQ14}$ , which control register SQ

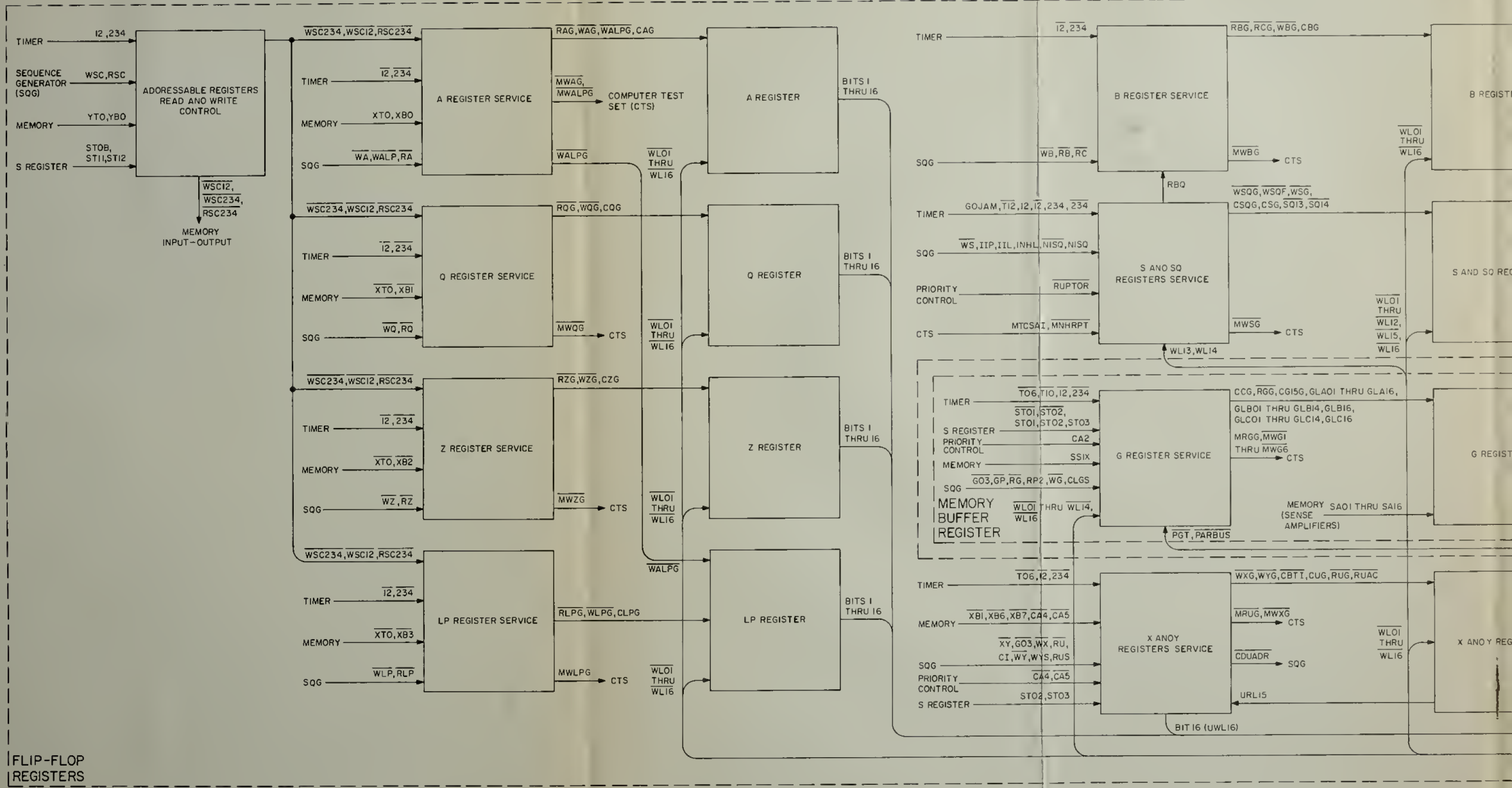
operation. The timing of the signals applied to the register S and SQ service which affect register SQ operation was discussed in the functional description of the sequence generator.

The register X and Y service gates generate the write, clear, and read signals supplied to registers X and Y (adder). In addition to these control signals, the register X and Y service generates signal  $\overline{CDUADR}$ , which is generated during the addition of angular data. Special considerations as to sign reversal and carry must be made during the addition of angular data. The input signals from the sequence generator are gating functions for the write, clear, and read signals. Input signal CI indicates that a +1 increment must be added to the content of the adder. Signals ST02 and ST03 from register S are combined with the addresses from memory to provide the necessary address indications used in the adder operation during the addition of angular data.

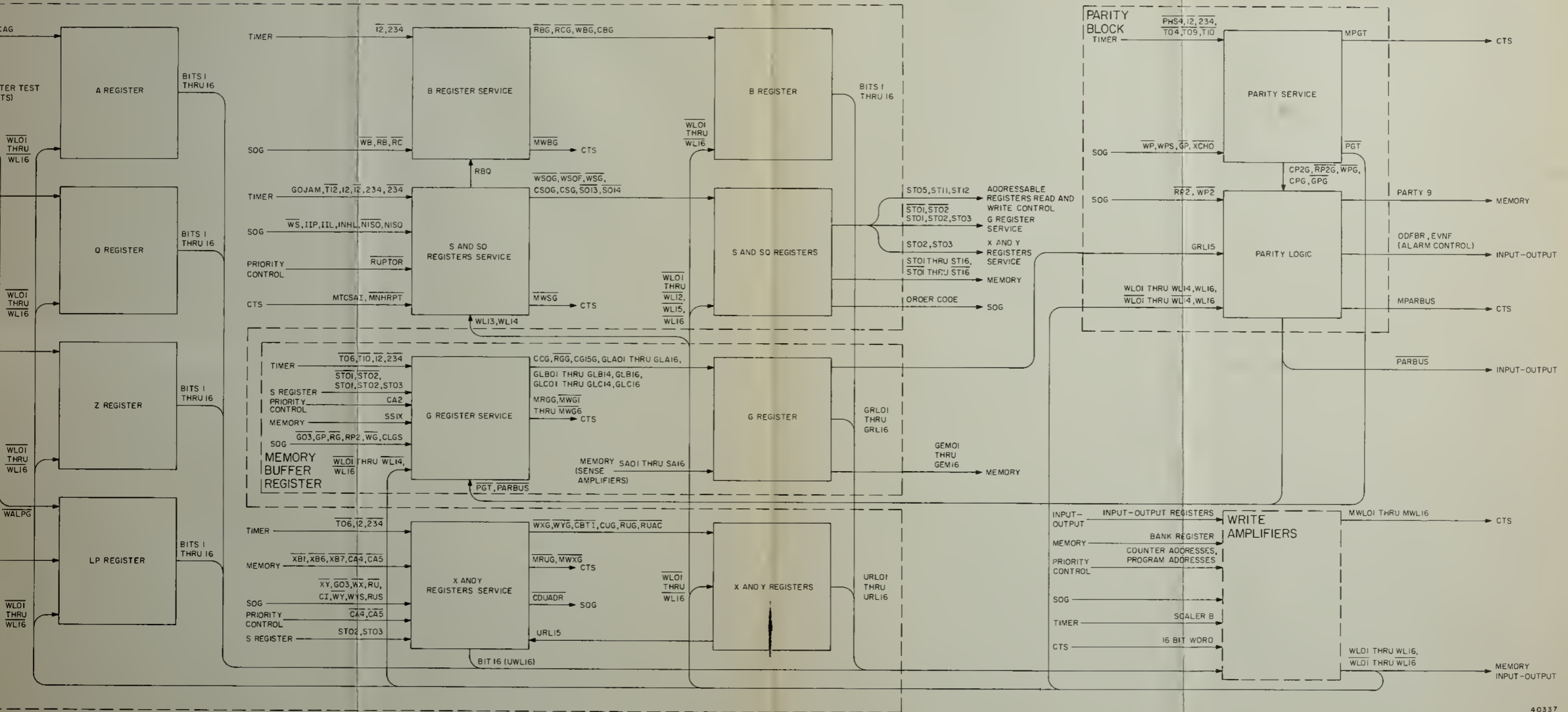
The register A service gates produce two write signals ( $\overline{WAG}$  and  $\overline{WALPG}$ ), which control writing into register A. If signal  $\overline{WAG}$  is produced, write line inputs WL01 through WL16 are written directly into register A. If signal  $\overline{WALPG}$  is produced, input WL16 is written into bit positions 15 and 16 of register A (see table 4-III). With signal  $\overline{WALPG}$  present, input WL01 is stored in bit position 14 of register LP (see table 4-III). The present content of register LP, the lowest order bit of the word in register A, is then manipulated as necessary for various arithmetic operations. Inputs WL01 through WL16 to addressable registers Q and Z are written directly into the corresponding bit positions. When register LP write signal  $\overline{WLPG}$  is produced,

Table 4-III. Write Line Inputs to Registers A and LP

Write Control Signal	Bit Position															
	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01
	$\overline{WL}$ Input															
Register A																
$\overline{WAG}$	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01
$\overline{WALPG}$	16	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02
Register LP																
$\overline{WLPG}$	01	01	X	14	13	12	11	10	09	08	07	06	05	04	03	02
$\overline{WALPG}$	X	X	01	X	X	X	X	X	X	X	X	X	X	X	X	X



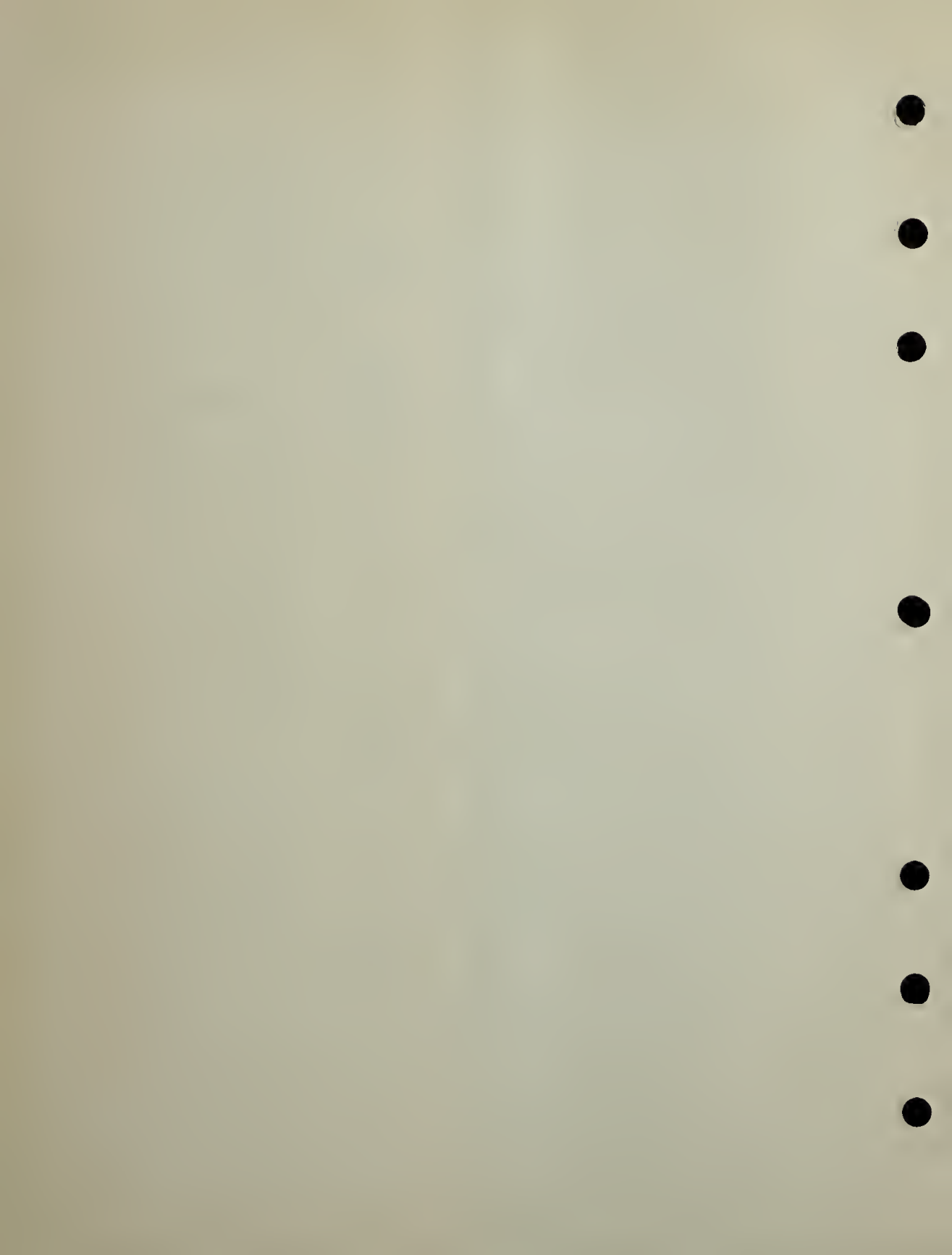
FLIP-FLOP  
REGISTERS



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Figure 4-97. Central Processor, Functional Diagram





the write line inputs to register LP are not written directly into the corresponding bit positions. Inputs WL15 and WL16 and bit position 14 are not used, and input WL01 is written into bit positions 15 and 16. Register B is written into with write signal WBG, cleared with clear signal CBG, and receives one of two read signals, RBG (read B) or RCG (read C). Signal RBG causes the content of register B to be supplied to the write amplifiers, and signal RCG causes the complement of register B to be supplied to the write amplifiers. Register S receives write signal WSG and clear signal CSG. Register S provides outputs ST01 through ST12 and their complements, which are applied through amplifiers to the memory selection circuits and to other portions of the central processor. Register SQ receives write signals WSQG and WSQF and clear signal CSQG from the register SQ service. The input information for register SQ is SQ13, SQ14, WL15, and WL16. Register SQ provides the order code to the sequence generator. The adder (registers X and Y) provides outputs URL01 through URL15 and UWL16, which are applied to the write amplifiers.

4-8.3.2 Write Amplifiers Functional Description. There are sixteen write amplifiers, each of which is associated with one bit position of each of the registers. Inputs are provided to the write amplifiers from the central processor registers, from circuits within the AGC, and from the CTS. The inputs from the central processor registers were described previously. The input-output registers supply 16 bit input words to the write amplifiers, and memory supplies 5 bit bank register addresses to the write amplifiers. Counter and program addresses are supplied to the write amplifiers from priority control during counter increment and program interrupt operations, and the sequence generator supplies binary-coded octal quantities and the start address to the write amplifiers. These quantities are required by the central processor during the execution of machine instructions. The start address initiates instruction GO when GOJAM is generated. The timer supplies a 16 bit real time word from scaler B to the write amplifiers. The CTS supplies 16 bit address or data words to the write amplifiers. In addition to supplying the inputs to the central processor registers, the write amplifiers supply inputs to the bank register in memory and to the output registers in the input-output. Signals MWL01 through MWL16 are the data signals supplied to the CTS. The CTS writes the data into registers according to write signals, such as MWAG (monitor write A).

4-8.3.3 Memory Buffer Register Functional Description. Register G is the memory buffer register and buffers between the central processor and memory. Register G provides data words to memory and is written into either from the write lines through register G service or directly from the memory sense amplifiers.

Register G service gates control shift and cycle operations within the G register. These editing operations are specified by addresses 0020 through 0023 in register S. If one of the addresses is present, the register S signals are gated with signals WG, 234, and CA2 to control write signals within the register G service. The 15 bit word present on the write lines is then controlled by the write signals to produce signals GLA, GLB, and GLC, which are supplied to register G. The word is written into register G by the GLA, GLB, and GLC signals either directly or it is shifted or cycled as specified by the address in register S. The PGT and PARBUS signals from the parity circuits control the parity that is written into bit position 15 in register G.

4-8.3.4 Parity Block Functional Description. The parity block produces parity error information (if any), generates parity bits for words being written into memory, generates a parity bit for the telemetry word, and produces an inhibiting signal for memory. All words received by the central processor from memory are processed by the parity circuits.

Fifteen bits of a word for parity tests are supplied from register G through the write amplifiers to the parity logic. The parity bit (signal GRL15) is supplied directly to the parity logic from register G. The word being tested for parity is applied to storage flip-flops in the parity logic which are connected to a parity tree (summing circuit). The parity tree is controlled by the  $\overline{WPG}$ , CPG, and  $\overline{GPG}$  signals (write, clear, and generate parity, respectively) from the parity service. Register P2 stores a generated parity bit during an exchange instruction when the write P2 signal,  $\overline{WP2}$ , is received from the sequence generator. Otherwise, the parity bit is written into bit position 15 of register G when signal PGT from the parity service and signal PARBUS from the parity logic are coincident. Signal  $\overline{PARBUS}$  is used also in the input-output to write the parity bit for the telemetry word. Signal PARTY 9 is an inhibiting signal supplied to memory. Signals ODFBR and EVNF are supplied to the parity alarm circuit, and signals MPGT and MPARBUS are monitor signals for the CTS.

4-8.3.5 Flip-Flop Register Operation Detailed Description. A single bit position of flip-flop register A is illustrated on figure 4-98. The description in the following paragraphs details operation of this flip-flop, which is identical to all flip-flops in the register. Further, the concepts presented in this discussion are basic to all flip-flop registers in the central processor. Functional differences between the registers are described under the specific register headings.

Each of the flip-flop registers has a capacity of 16 bits. One bit position of each register is contained on each of 16 identical logic modules. This is illustrated on figure 4-98 by enclosing bit position 1 of register A and indicating logic module A1.

Each bit position of the registers consists of a write gate (register A has two write gates) and a read gate. The register is cleared by a clear or reset pulse applied directly to the reset input. Information is written into the register from the write line

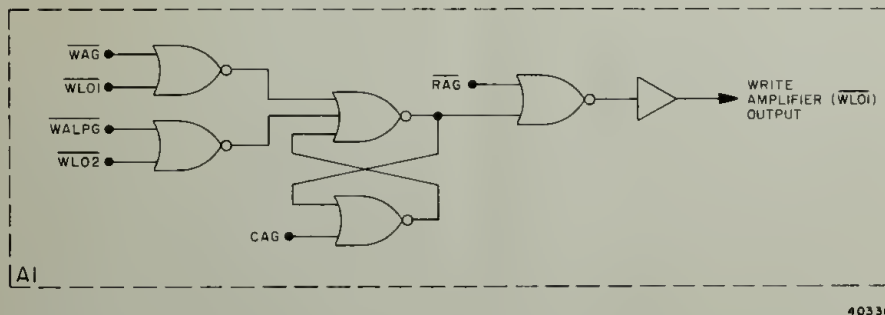


Figure 4-98. Register A Single Bit Position

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( $\overline{WL01}$ ) when the write signal  $\overline{WAG}$  enables the gate. Thus, the flip-flop is cleared and immediately written into. The read signal enables the read gate and causes the information stored in the flip-flop to be placed on the write lines. The write line outputs are labeled  $\overline{WL01}$  through  $\overline{WL16}$ , corresponding to the bit positions of the register. By enabling the read gates of one register and the write gates of another register simultaneously, information is transferred between registers of the central processor.

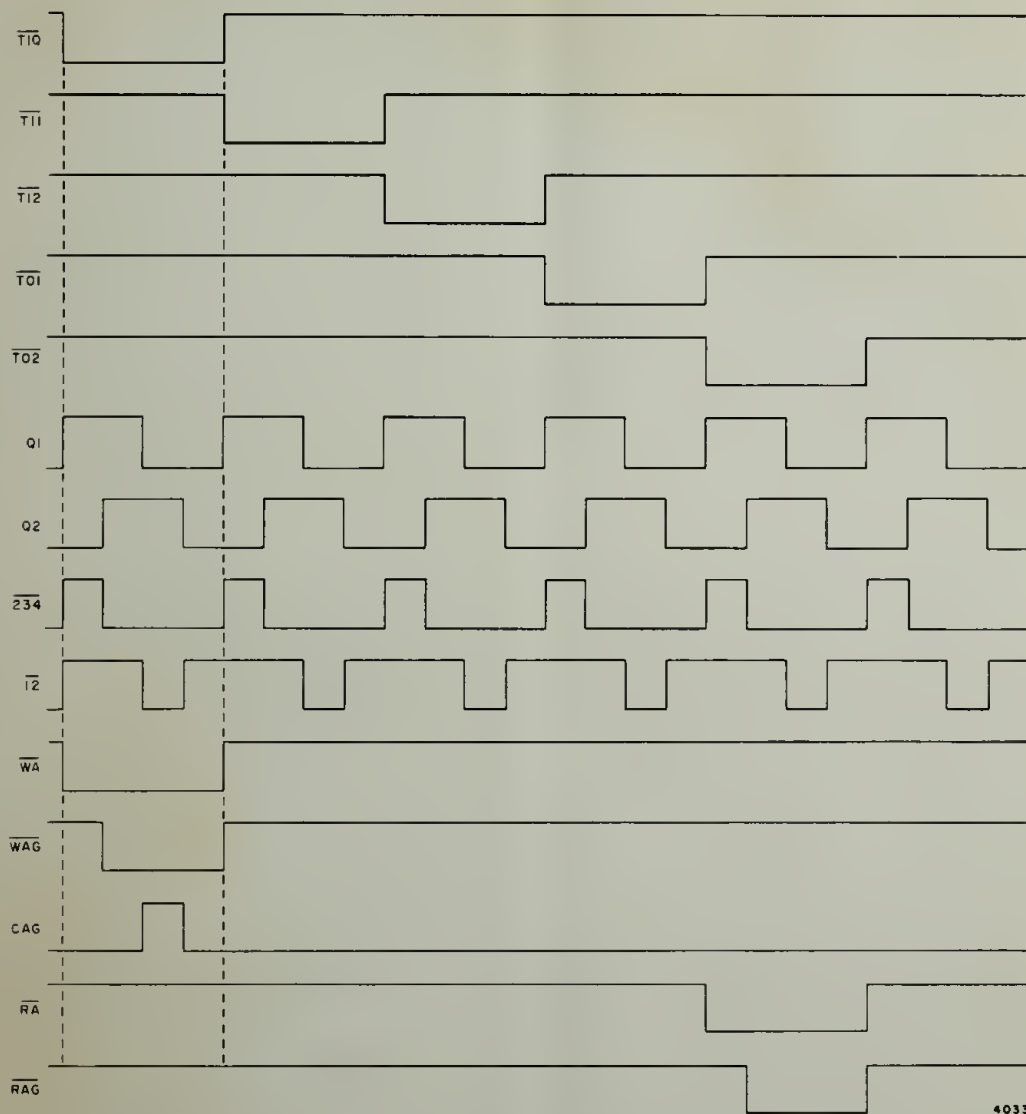
4-8.3.6 Register Service Gates. Information is transferred into and out of the flip-flop registers of the central processor under control of write, clear, and read signals, which are generated by associated write, clear, and read gates for each register. Inputs to the register service gates consist of read and write control pulses from the crosspoint matrix of the sequence generator and timing signals  $\overline{12}$  and  $\overline{234}$  from the timer.

Timing signal  $\overline{234}$ , in conjunction with the write and read control pulses, is used to derive the write and read signals, and signal  $\overline{12}$ , in conjunction with the write control pulse, is used to derive the clear signal. As an example, the write, clear, and read signals for register A are illustrated on figure 4-99 and discussed in the following paragraphs.

Write control pulse  $\overline{WA}$  from the crosspoint matrix occurs for one action (0.97 microsecond). On figure 4-99  $\overline{WA}$  occurs during action 10 of the memory cycle. This control pulse, coincident with timing signal  $\overline{234}$ , results in 0.75 microsecond write signal  $\overline{WAG}$  from the write service gate of register A. The clear or reset pulse,  $\overline{CAG}$ , is generated by gating the write control pulse and timing signal  $\overline{12}$ . This is a 0.25 microsecond positive transition and occurs during the third quarter of an action coincident with the write signal. Thus, the flip-flop is first cleared and then immediately written into. Figure 4-99 illustrates that the write signal is active for approximately 1/4 microsecond before the clear pulse occurs. However, there is sufficient delay so that the flip-flop is not written into until the clear pulse terminates. The clear pulse occurs only when a write signal is generated. Therefore, information written into the register is retained until the next write signal occurs.

The read control pulse, similar to the write control pulse, is 0.97 microsecond wide and is gated with timing signal  $\overline{234}$  to produce a 0.75 microsecond read signal,  $\overline{RAG}$ , from the read service gate. The read signal enables the read gates and causes information in the registers to be placed on the write lines. The read signal does not destroy the content of the register. Information is retained in each flip-flop and can actually be read out several times until the next write signal occurs.

4-8.3.7 Addressable Register Service. Under program control, write, clear, and read signals for registers A, Q, Z, and LP are generated for write-in and readout. This is accomplished with memory addresses 0000 through 0003 and timing signals  $\overline{WSC234}$ ,  $\overline{WSC12}$ , and  $\overline{RSC234}$ . The timing signals, in conjunction with address 0000, enable register A service, address 0001 the Q service gates, address 0002 the Z service gates, and address 0003 the LP service gates. These addresses occur during the execution of various routines (manipulations which are common to different programs).



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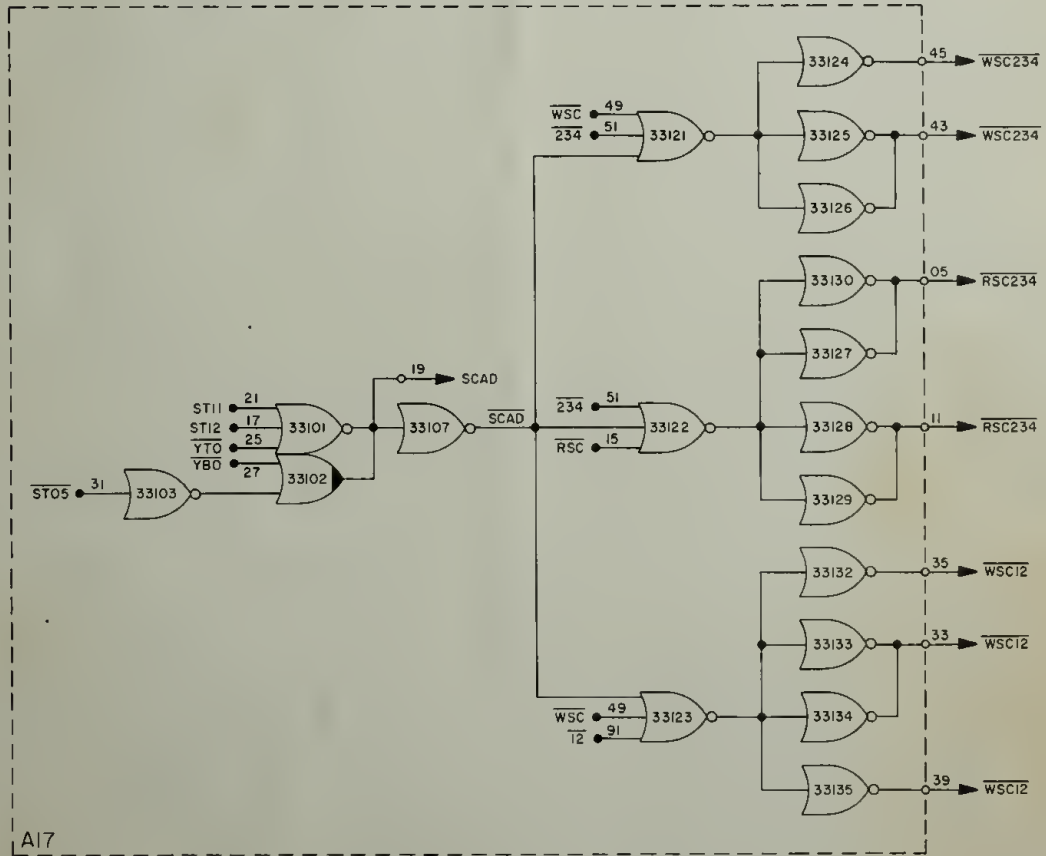
Figure 4-99. Register A - Write, Clear, and Read Signals

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The timing signals are generated as shown on figure 4-100. Inputs  $\overline{WSC}$  and  $\overline{RSC}$  are control pulses generated in the crosspoint matrix and gate with timing signal  $\overline{234}$  to produce write signal  $\overline{WSC234}$  and read signal  $\overline{RSC234}$ . Control pulse  $\overline{WSC}$  gates with timing signal  $\overline{12}$  to produce the clear signal  $\overline{WSC12}$ .

Signal  $\overline{SCAD}$  enables the addressable register service gates if any one of octal addresses 0000 through 0017 is present. There is no access to memory at this time since signal SCAD is a logic ONE and inhibits erasable memory cycle timing.

For octal addresses above 0017 through 0037, signal  $\overline{ST05}$  is a logic ZERO. This signal is inverted and becomes a logic ONE at the input to gate 33102. Output SCAD is now a logic ZERO and enables memory cycle timing;  $\overline{SCAD}$  is a logic ONE and inhibits the addressable register service gates described previously.



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Figure 4-100. Addressable Registers, Read and Write Control

4-8.3.8 Register A. Register A (figure 4-101), or accumulator, normally retains information between the execution of individual instructions. This is accomplished by write signal  $\overline{WAG}$ , which gates information on the write lines ( $\overline{WL01}$  through  $\overline{WL16}$ ) into register A. This information is read out when read signal  $\overline{RAG}$  enables the read gates.

Write signal  $\overline{WALPG}$  enables the second write gate input to register A when the accumulator is used in conjunction with register LP during multiply operations. Bit 2 from the write lines is written into bit position 1, bit 3 into bit position 2, et cetera. Bit 1 on the write lines is written into bit position 14 of register LP by write signal  $\overline{WALPG}$ . The sign bit ( $\overline{WL16}$ ) is written into bit positions 15 and 16. This manipulation of data accomplishes the required shifting during a multiply instruction.

4-8.3.9 Register Q. Register Q (figure 4-102) is used during the execution of a transfer control instruction (TC) or a divide instruction (DV). Information on the write lines is gated into the corresponding bit positions of the register by write signal  $\overline{WQG}$ . During a transfer control instruction a specific address is transferred into register Q and stored in the event that a transfer to the original sequence of instructions takes place. During a divide instruction register Q holds the dividend and, upon the completion of the instruction, contains the remainder.

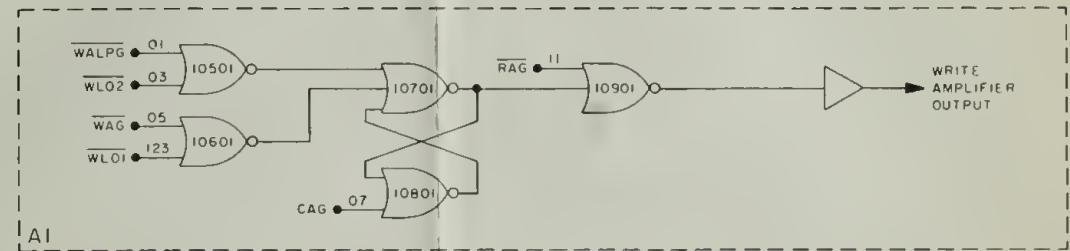
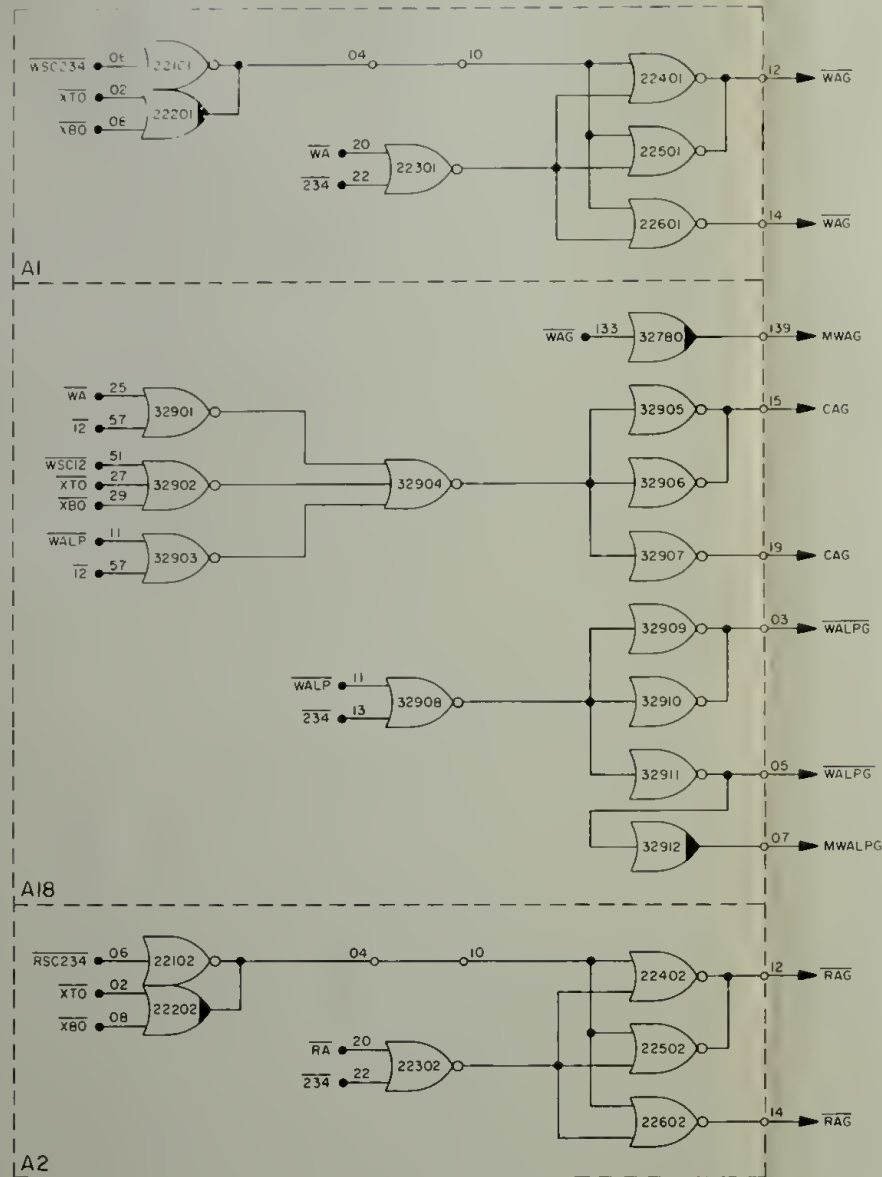
4-8.3.10 Register Z. Register Z (figure 4-103), also referred to as the program counter, stores the address of the instruction to be executed next. During the execution of a basic instruction, the content of register Z is incremented by one in the address. The result (next address) is again stored in register Z.

4-8.3.11 Register LP. Register LP (figure 4-104) functions only during instructions MP (multiply) and DV (divide). This register, in conjunction with register A during these instructions, forms a double-length shifting accumulator. Information from the write lines is cycled right into register LP by write signal  $\overline{WALPG}$ . Write signal  $\overline{WALPG}$  is generated during specific portions of the multiply and divide instructions and writes bit 1 from the write lines into bit position 14 of register LP when subtotals are computed during a multiply instruction, and the remainder during a divide instruction.

4-8.3.12 Register B. Register B (figure 4-105) is primarily a storage element. This register stores the order code and relevant address of the instruction to be executed next. This is not in conflict with the description given for register, Z which stores the next address. The next address may be that of an instruction or a subinstruction.

The write, clear, and read signals for register B are generated by associated control pulses and timing signals, as described previously. This register is not addressable through program control as are registers A, Q, Z, and LP. Two read signals ( $\overline{RBG}$  and  $\overline{RCG}$ ) are generated to gate information from register B onto the write lines. This is functionally similar to readout of the other registers. Read signal  $\overline{RBG}$  is generated by gating read control signal  $\overline{RB}$  and timing signal 234 or by signal  $\overline{RBQ}$ . This latter signal reads the content of register B and causes an address to be placed on the write lines and the order code to be written into registers S and SQ. Read signal  $\overline{RCG}$  gates the complement of register B when required for certain programs.

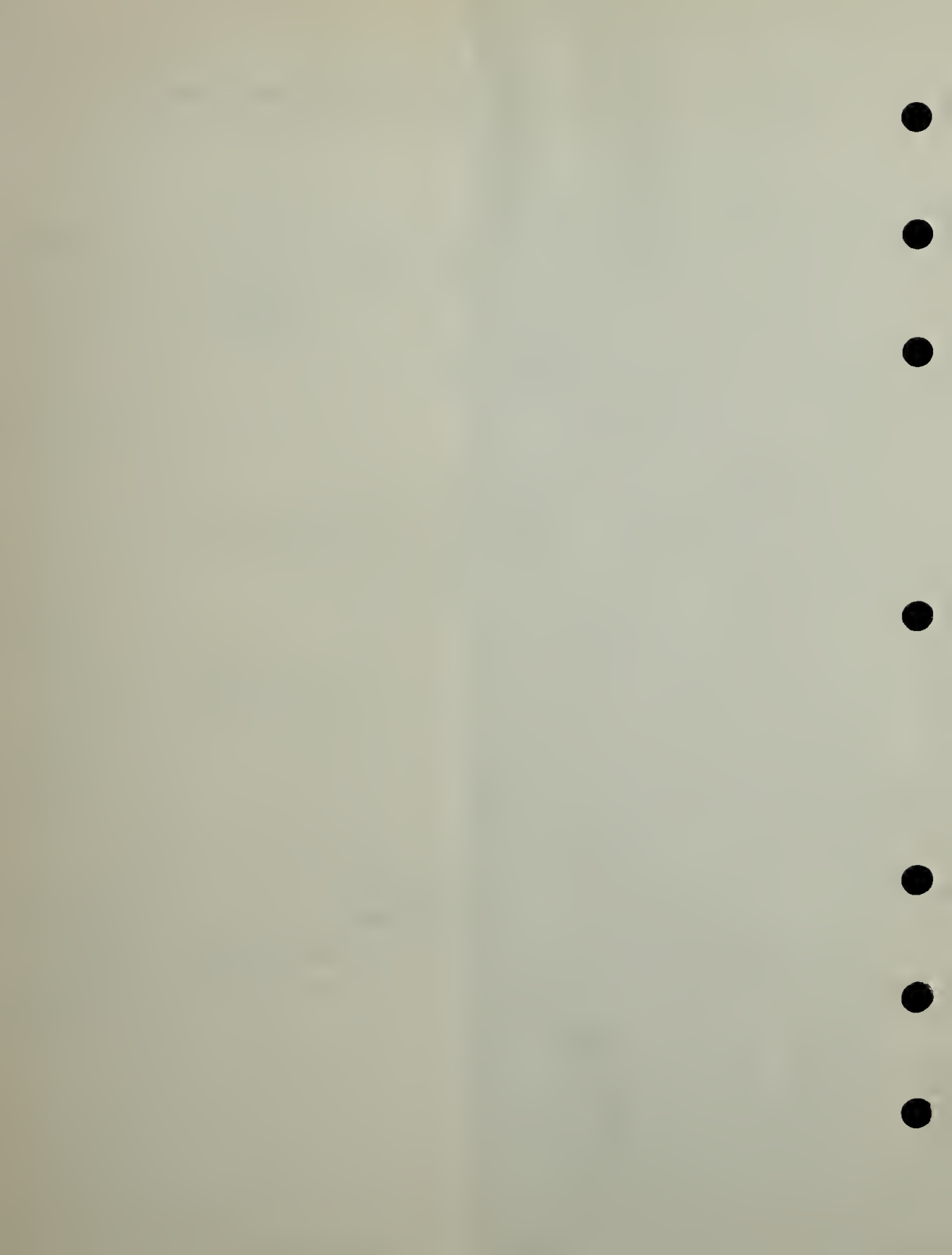
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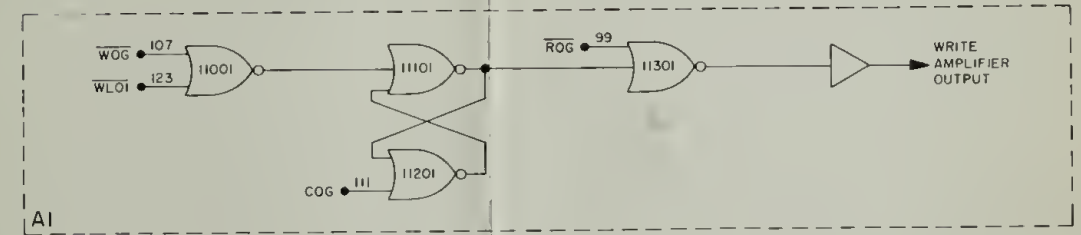
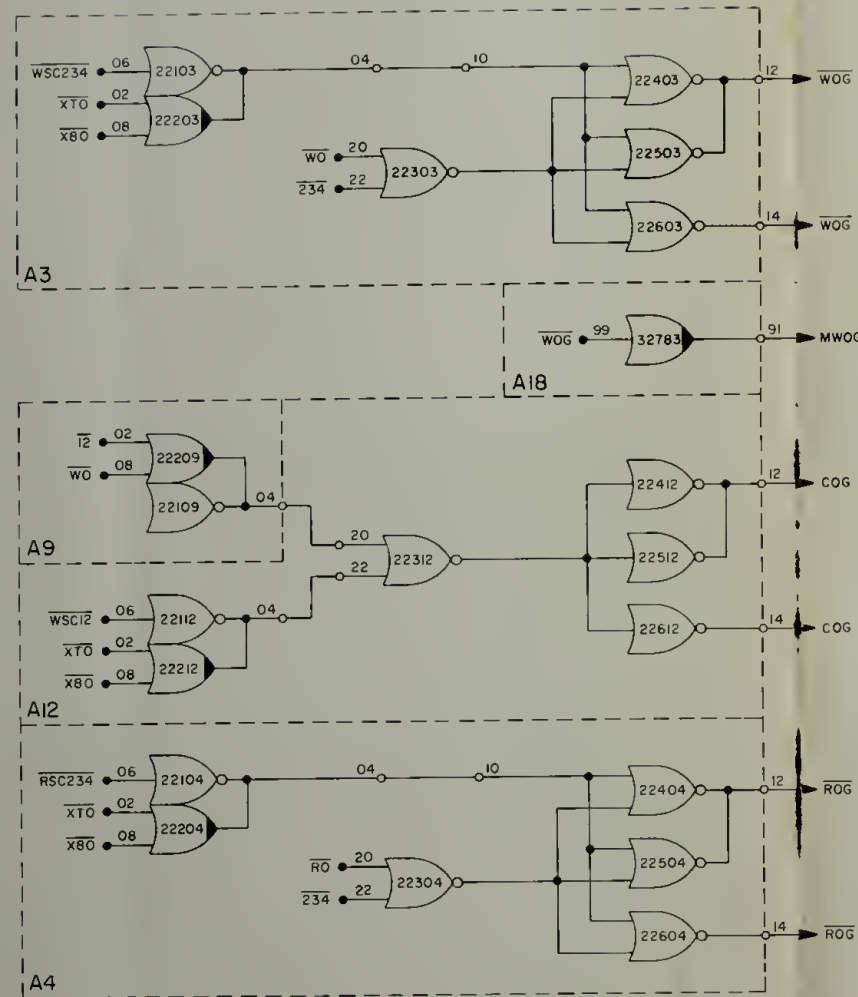
PIN NO MODULE	WRITE		WRITE		CLEAR	READ
	01	03	05	123	07	11
A1	WALPG	WLO2	WAG	WLO1	CAG	RAG
A2	WALPG	WLO3	WAG	WLO2	CAG	RAG
A3	WALPG	WLO4	WAG	WLO3	CAG	RAG
A4	WALPG	WLO5	WAG	WLO4	CAG	RAG
A5	WALPG	WLO6	WAG	WLO5	CAG	RAG
A6	WALPG	WLO7	WAG	WLO6	CAG	RAG
A7	WALPG	WLO8	WAG	WLO7	CAG	RAG
A8	WALPG	WLO9	WAG	WLO8	CAG	RAG
A9	WALPG	WLO10	WAG	WLO9	CAG	RAG
A10	WALPG	WLO11	WAG	WLO10	CAG	RAG
A11	WALPG	WLO12	WAG	WLO11	CAG	RAG
A12	WALPG	WLO13	WAG	WLO12	CAG	RAG
A13	WALPG	WLO14	WAG	WLO13	CAG	RAG
A14	WALPG	WLO15	WAG	WLO14	CAG	RAG
A15	WALPG	WLO16	WAG	WLO15	CAG	RAG
A16	WALPG	WLO16	WAG	WLO16	CAG	RAG

Figure 4-101. Register A





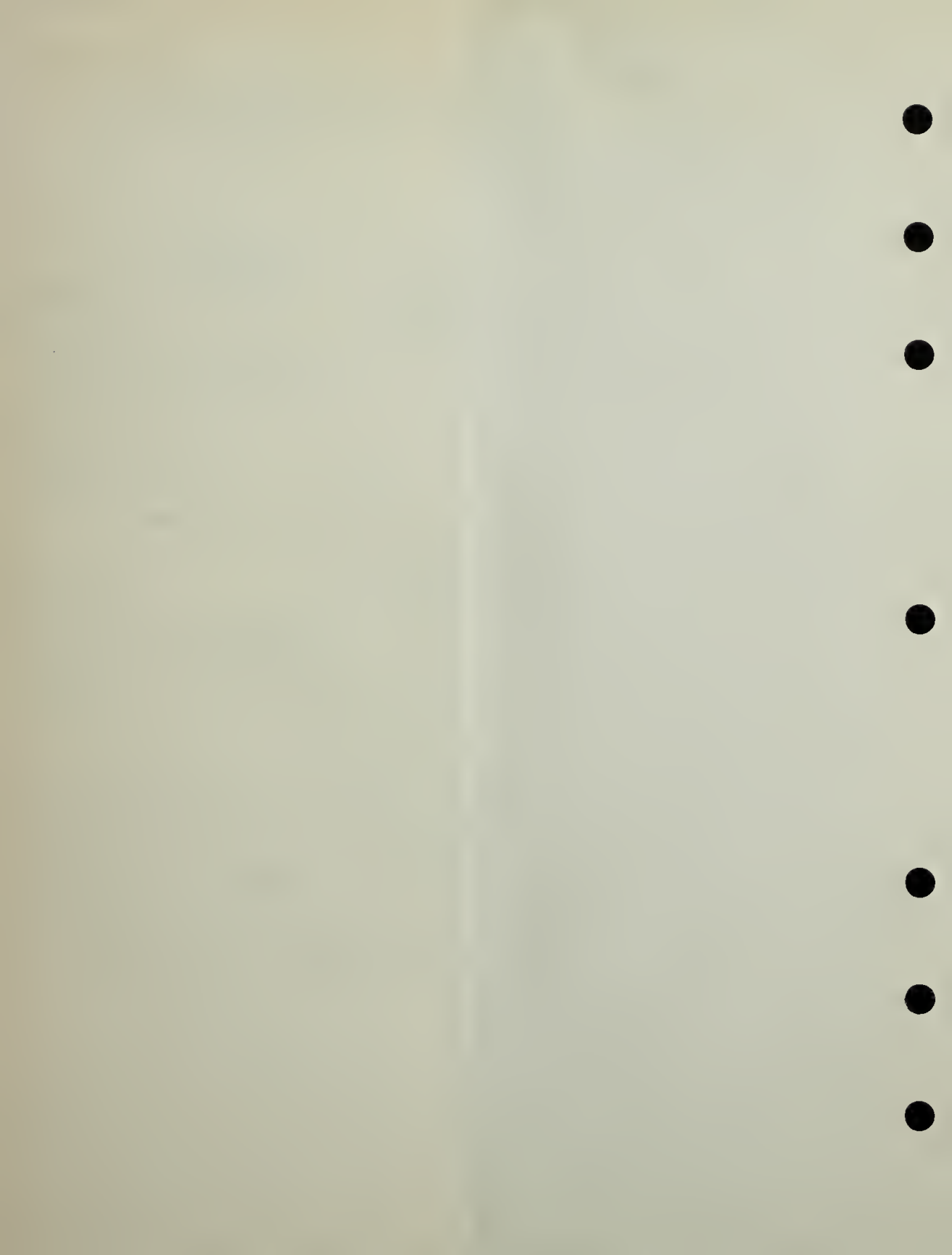
APOLLO GUIDANCE AND NAVIGATION SYSTEM



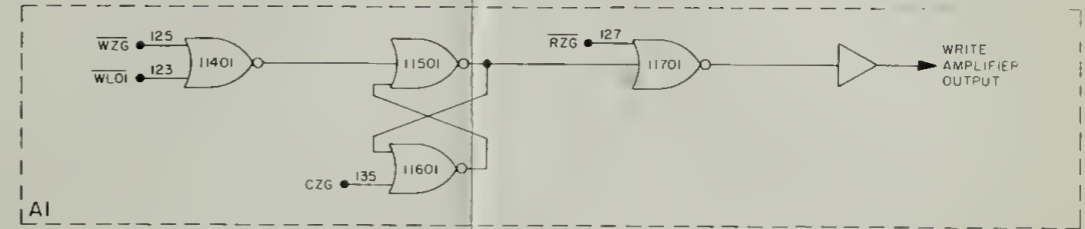
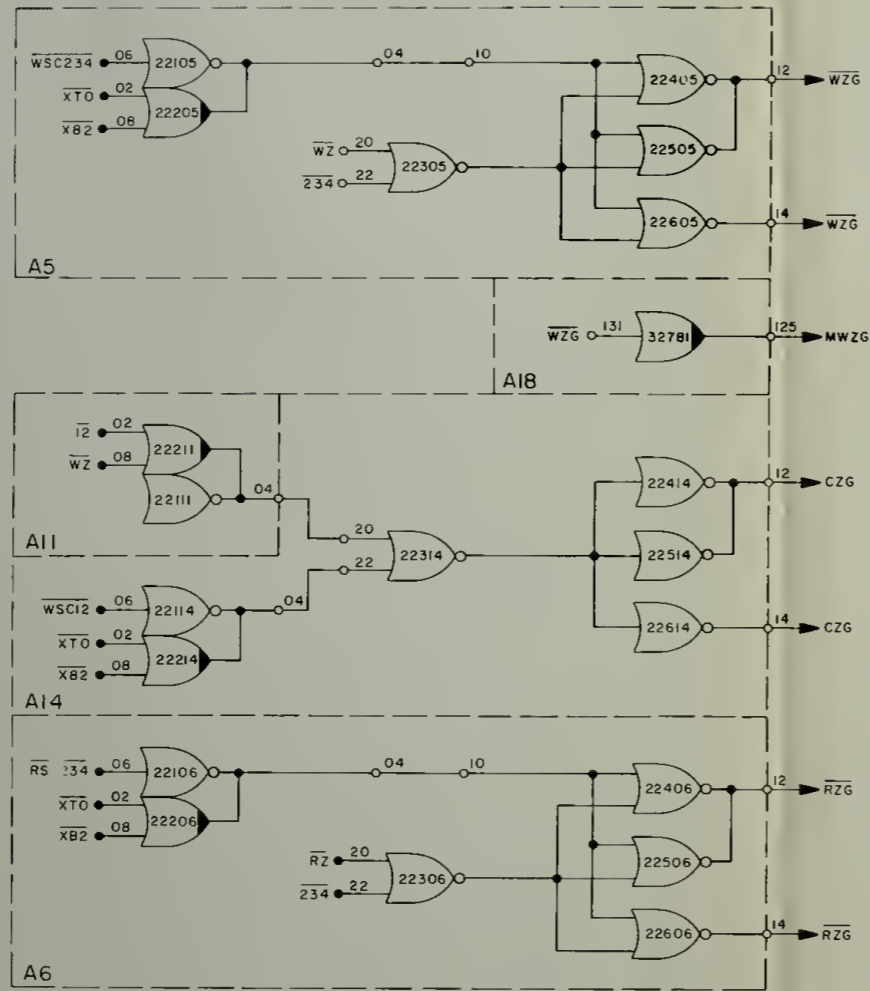
MODULE	WRITE		CLEAR	READ
	107	123	111	99
A 1	WOG	WLO1	COG	ROG
A 2	WOG	WLO2	COG	ROG
A 3	WOG	WLO3	COG	ROG
A 4	WOG	WLO4	COG	ROG
A 5	WOG	WLO5	COG	ROG
A 6	WOG	WLO6	COG	ROG
A 7	WOG	WLO7	COG	ROG
A 8	WOG	WLO8	COG	ROG
A 9	WOG	WLO9	COG	ROG
A10	WOG	WLO10	COG	ROG
A11	WOG	WLO11	COG	ROG
A12	WOG	WLO12	COG	ROG
A13	WOG	WLO13	COG	ROG
A14	WOG	WLO14	COG	ROG
A15	WOG	WLO15	COG	ROG
A16	WOG	WLO16	COG	ROG

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Figure 4-102. Register Q



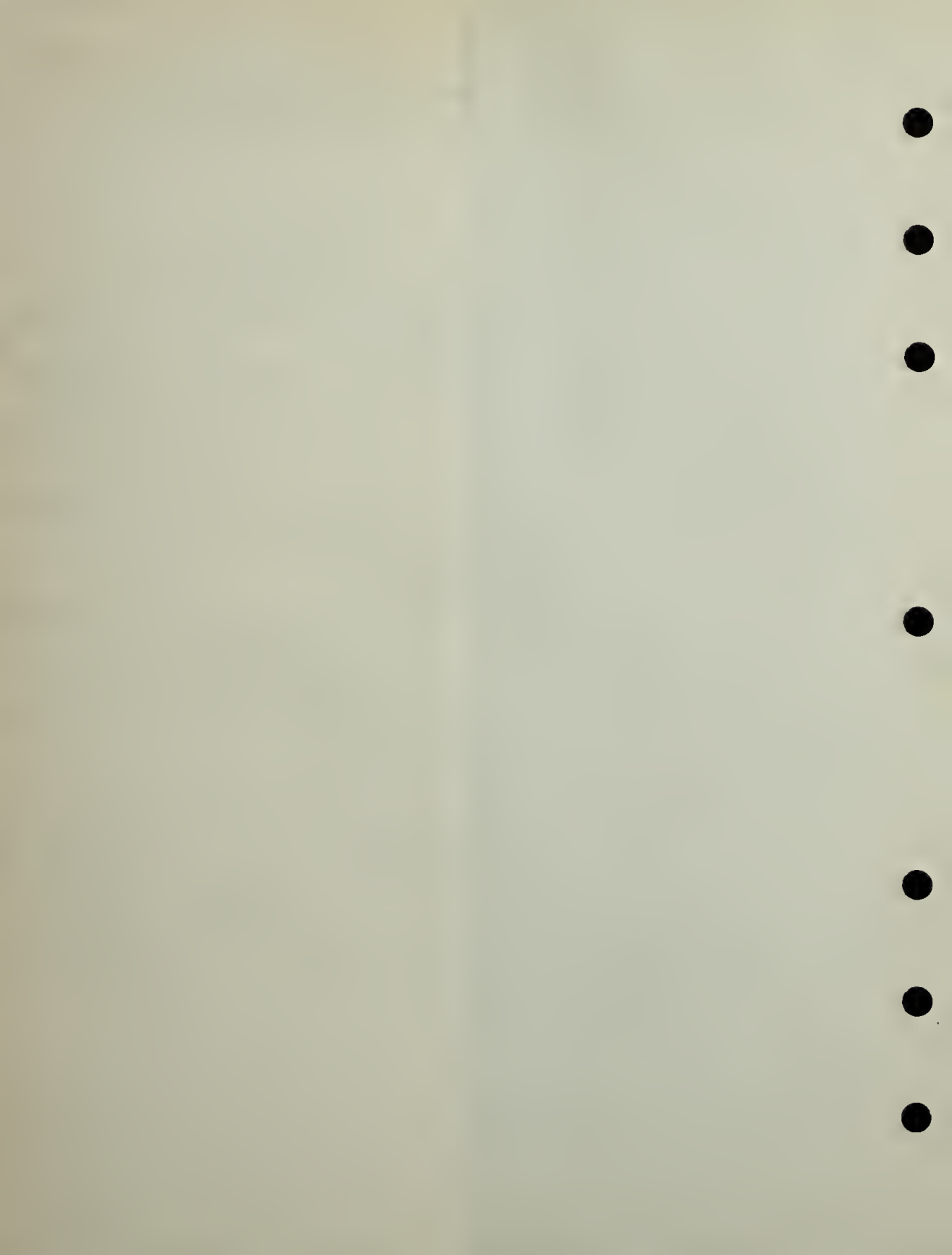
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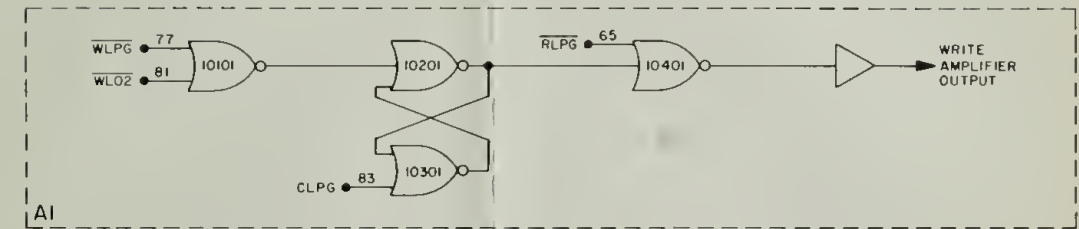
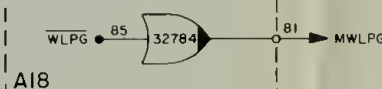
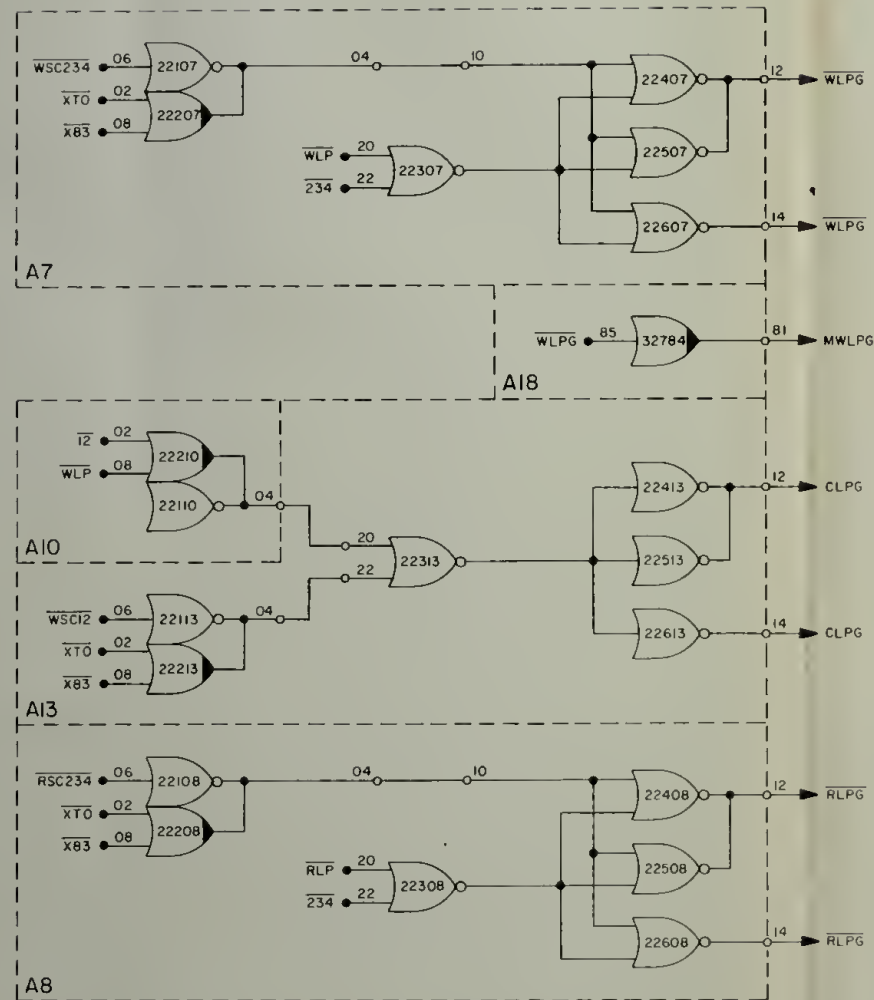


MODULE	PIN NO	WRITE		CLEAR	READ
		125	123	135	127
A 1		WZG	WLO1	CZG	RZG
A 2		WZG	WLO2	CZG	RZG
A 3		WZG	WLO3	CZG	RZG
A 4		WZG	WLO4	CZG	RZG
A 5		WZG	WLO5	CZG	RZG
A 6		WZG	WLO6	CZG	RZG
A 7		WZG	WLO7	CZG	RZG
A 8		WZG	WLO8	CZG	RZG
A 9		WZG	WLO9	CZG	RZG
A10		WZG	WLO10	CZG	RZG
A11		WZG	WLO11	CZG	RZG
A12		WZG	WLO12	CZG	RZG
A13		WZG	WLO13	CZG	RZG
A14		WZG	WLO14	CZG	RZG
A15		WZG	WLO15	CZG	RZG
A16		WZG	WLO16	CZG	RZG

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Figure 4-103. Register Z



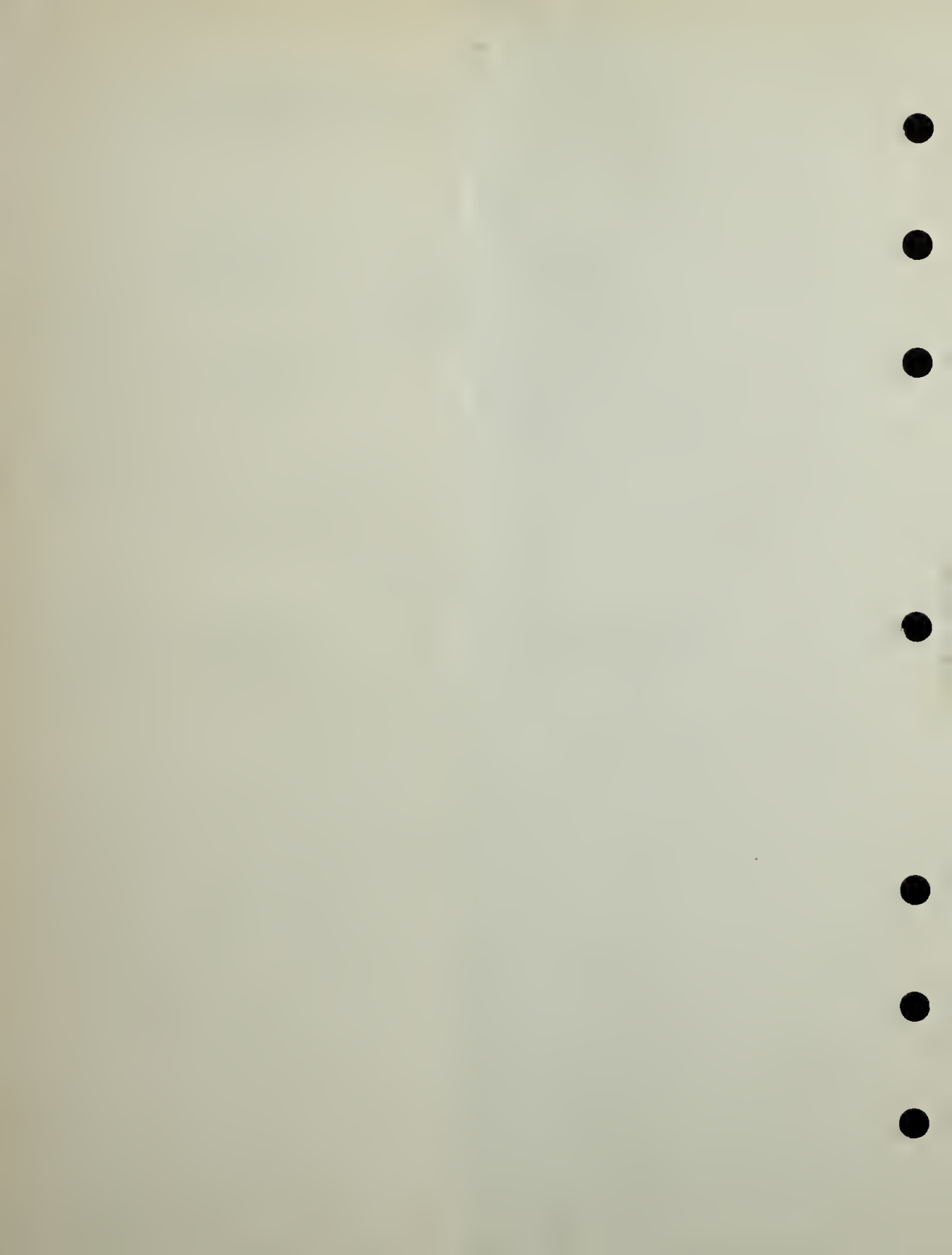


MODULE	WRITE		CLEAR	READ
	77	81	83	65
A 1	WLPG	WLO2	CPLG	RLPG
A 2	WLPG	WLO3	CLPG	RLPG
A 3	WLPG	WLO4	CLPG	RLPG
A 4	WLPG	WLO5	CLPG	RLPG
A 5	WLPG	WLO6	CLPG	RLPG
A 6	WLPG	WLO7	CLPG	RLPG
A 7	WLPG	WLO8	CLPG	RLPG
A 8	WLPG	WLO9	CLPG	RLPG
A 9	WLPG	WL10	CLPG	RLPG
A10	WLPG	WL11	CLPG	RLPG
A11	WLPG	WL12	CLPG	RLPG
A12	WLPG	WL13	CLPG	RLPG
A13	WLPG	WL14	CLPG	RLPG
A14	WALPG *	WLO1	CLPG	RLPG
A15	WLPG	WLO1	CLPG	RLPG
A16	WLPG	WLO1	CLPG	RLPG

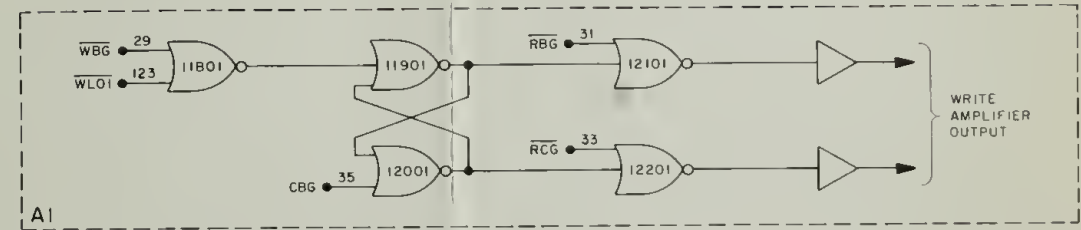
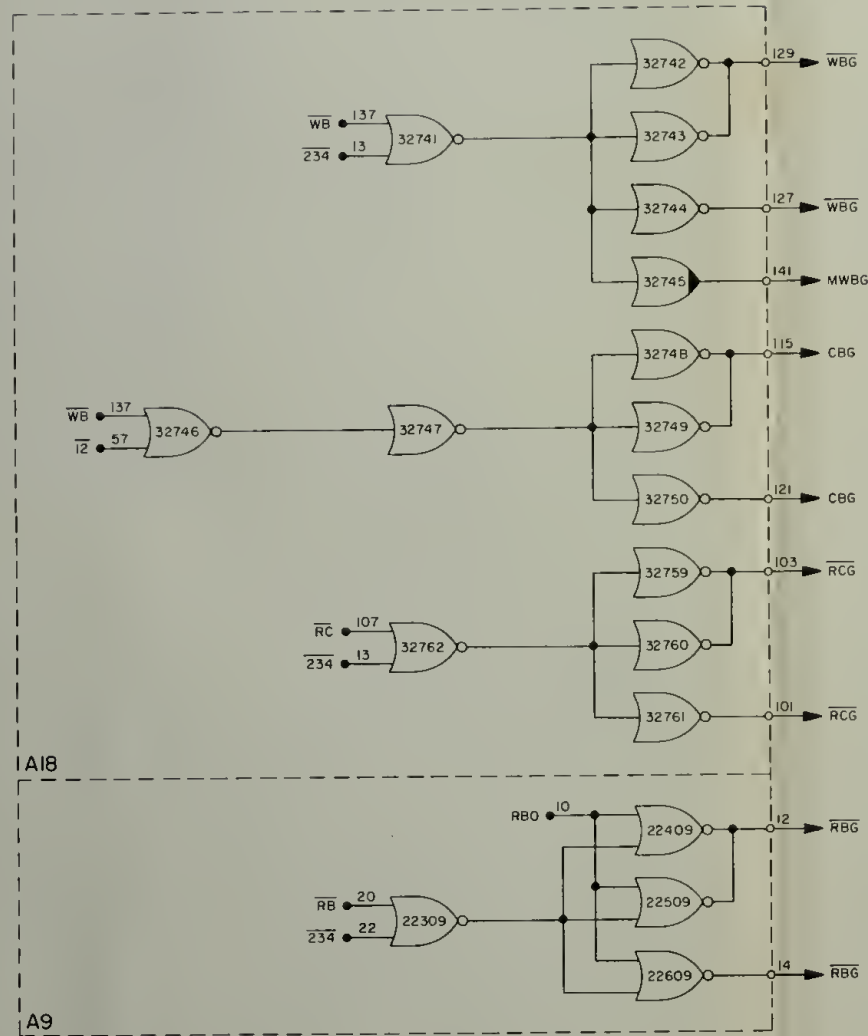
\* WRITE CONTROL SIGNAL WALPG GENERATED BY (A) REGISTER SERVICE.

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Figure 4-104. Register LP



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PIN NO MODULE	WRITE		CLEAR	READ	READ COMPLEMENT
	29	123	35	31	33
A 1	WBG	WLO1	CBG	RBG	RCG
A 2	WBG	WLO2	CBG	RBG	RCG
A 3	WBG	WLO3	CBG	RBG	RCG
A 4	WBG	WLO4	CBG	RBG	RCG
A 5	WBG	WLO5	CBG	RBG	RCG
A 6	WBG	WLO6	CBG	RBG	RCG
A 7	WBG	WLO7	CBG	RBG	RCG
A 8	WBG	WLO8	CBG	RBG	RCG
A 9	WBG	WLO9	CBG	RBG	RCG
A10	WBG	WLO10	CBG	RBG	RCG
A11	WBG	WLO11	CBG	RBG	RCG
A12	WBG	WLO12	CBG	RBG	RCG
A13	WBG	WLO13	CBG	RBG	RCG
A14	WBG	WLO14	CBG	RBG	RCG
A15	WBG	WLO15	CBG	RBG	RCG
A16	WBG	WLO16	CBG	RBG	RCG

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Figure 4-105. Register B





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4-8.3.13 Registers S and SQ. Registers S and SQ (figure 4-106) make up a total of 16 bits and function in a manner similar to the other registers of the central processor. Information is written into these registers from the write lines, but no read signal is generated to read out information. The outputs and their complements (ST01 through ST16) are available directly from the output gates.

Register S (memory address register) contains 12 bit positions for selecting the contents of memory. Ten bit positions are used to select from the 1024 address locations of erasable memory. All 12 bit positions are used in conjunction with the bank register to select from the content of fixed memory.

Write signal  $\overline{WSG}$  gates write lines  $\overline{WL01}$  through  $\overline{WL12}$  into register S. The write control signal, WS, is generated at all times except during instruction MP1. Thus, an address is written into register S at action 1 of each memory cycle for every instruction except MP1. A logic ZERO closer to the emitter potential of ground is realized by connecting the write control pulse and timing signal  $\overline{12}$  into separate gates with a common output, as shown for clear signal CSG. Connecting both inputs to a single gate would result in a logic ZERO out which is actually more positive with respect to ground. Since the required transition for the clear signal is positive, the configuration shown on figure 4-106 ensures that the register will not be cleared by any extraneous condition appearing on the write control and timing signal inputs when these inputs do not enable the gate.

The 4 bit (ST13 through ST16) register SQ contains the order code of the instruction to be executed. Bits 13 and 14 are entered into register SQ from the sequence generator; bits 15 and 16 are entered directly from the write lines.

The write and clear signals from the SQ service gates are generated as a function of conditions in the sequence generator. At time 11 in a memory cycle a new instruction request signal (NISQ) is produced by the crosspoint matrix and is applied to the SQ clear gate (through gate 64009) and write gates (through gate 64008). At time 12 ( $\overline{12}$ ), CSQG is generated and clears the register SQ. Coincident with this action, signal RBQ (read B) is generated and causes the order code from register B to be placed on the write lines. Bits 15 and 16 from register B are written into register SQ by write signal  $\overline{WSQG}$ . Bits 13 and 14 are applied through gates 64013 and 64014 and written into register SQ as SQ13 and SQ14 by write signal  $\overline{WSQF}$ .

The output from the interrupt inhibit gates (64019, 64020, and 64021) is normally logic ZERO and has no effect on the SQ clear and write service gates. When an interrupt request occurs, signal RUPTOR, coincident with a new instruction request (NISQ) at time 12, enables the SQ clear gate, and signal CSQG clears register SQ of the previous order code. The inhibit interrupt gate output inhibits gate 64007 and prevents read signal RBQ and write signal  $\overline{WSQG}$  from being generated. Consequently, bits 15 and 16 of the order code become logic ZERO's. Write signal  $\overline{WSQF}$  is enabled, however, and outputs SQ13 and SQ14 become logic ONE's into the register SQ. Therefore, the order code during interrupt is forced to a condition of 0011. Other inputs to the interrupt inhibit gate prevent the current interrupt program from being interrupted except by start instruction requests GOJAM or MTCSAI or a monitor inhibit request (MHRPT).

Signal GOJAM, the request for instruction GO, inhibits SQ write signals  $\overline{WSQG}$  and  $\overline{WSQF}$ . Register SQ is cleared by CSQG, and the order code is forced to a condition of 0000, which causes the sequence generator to execute instruction GO. Signal GOJAM also inhibits the start instruction request signal (MTCSAI) from the CTS.

Signal MTCSAI inhibits the SQ write signals and forces the order code to 0000. The effect of MTCSAI, however, is to cause the sequence generator to execute a transfer control instruction (TCSA).

4-8.3.14 Register G Detailed Description. Register G (figure 4-107) buffers all information coming from and going to erasable memory and fixed memory. This register also functions during certain programs to shift or cycle information as required.

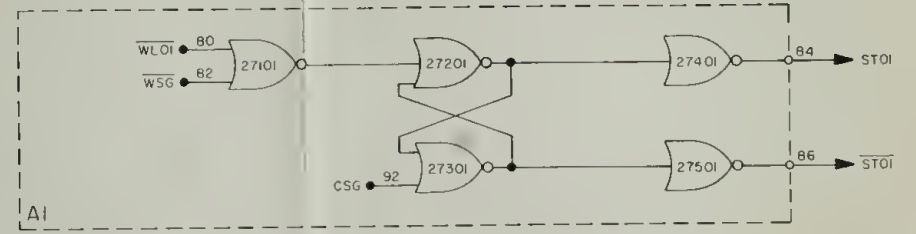
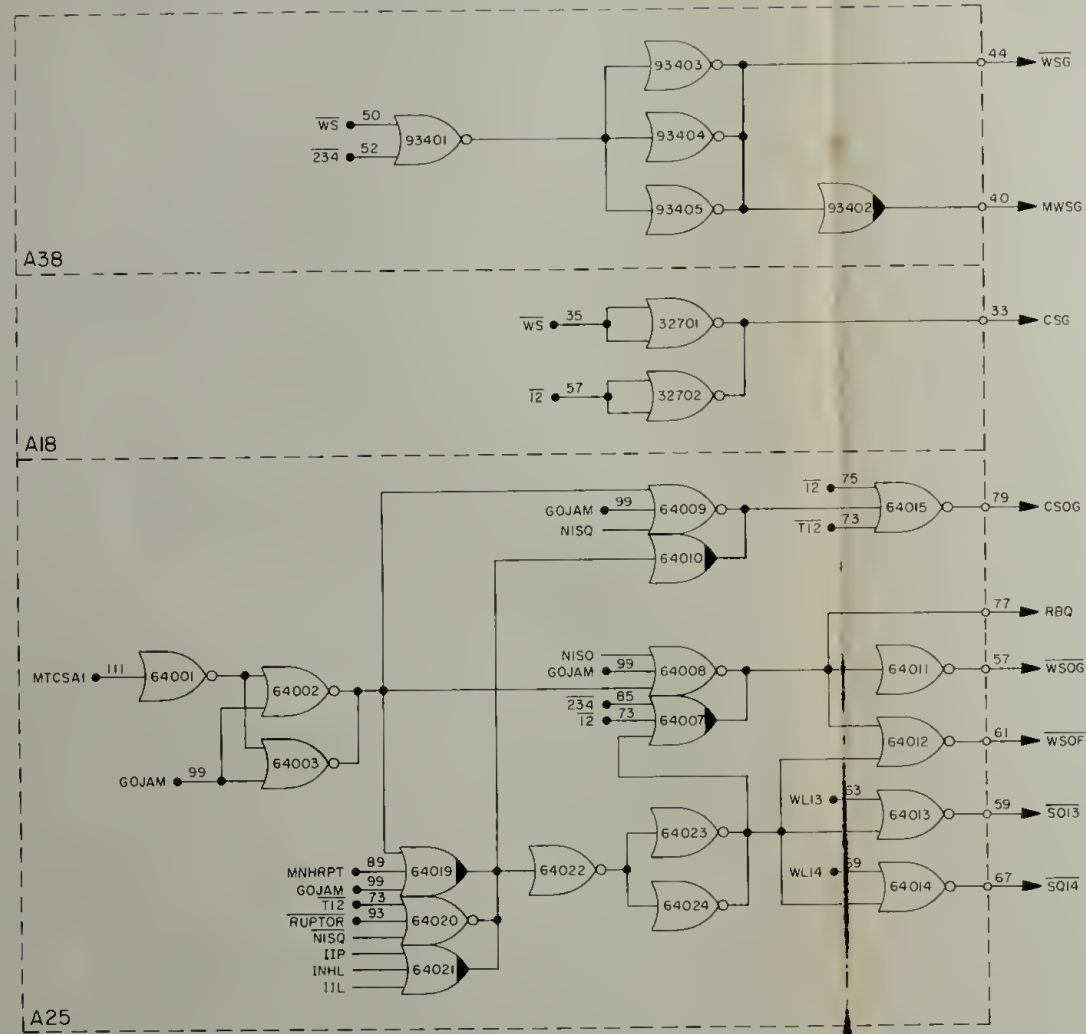
Data from fixed or erasable memory is written into register G from sense amplifier outputs SA01 through SA16, which are wired directly into the corresponding bit positions of register G. The data is written in as a function of memory cycle timing and is considered to be read out of memory into register G by action 6 of a memory cycle (one MCT = 11.97  $\mu$ sec). Bit position 15 of register G contains the parity bit. No other data is written into this bit position. When data is to be written into erasable memory, a parity bit (GLA15) is generated and entered into bit position 15 to be deposited into memory with the rest of the word. The inputs to memory are applied through the extended NOR gates with outputs labeled GEM01 through GEM16.

Inputs GLA01 through GLA16, GLB01 through GLB16, and GLC01 through GLC16 to the write gates are generated when register G is the recipient of data at times other than a readout from memory. Normally, write signals GLA01 through GLA16 (except GLA15) are generated to write into register G from the write lines. Write signals GLB01 through GLB16 and GLC01 through GLC16 involve cycle and shift functions. These write signals are described in detail in the following paragraphs.

Write service consists of six write control signals,  $\overline{WG1G}$  through  $\overline{WG6G}$ , which are shown on figure 4-108. These signals are generated in pairs as a function of the address contained in register S. For all address except octal 0020 through 0023 write control signals  $\overline{WG1G}$  and  $\overline{WG5G}$  are generated and gate information from the write lines into register G. These signals are generated by write control pulse  $\overline{WG}$  from the sequence generator coincident with timing signal 234, and an enabling input from gate 32210 (for all addresses except 0020 through 0023) applied to gate 32211.

Octal addresses 0020 through 0023 are produced under program control to perform shift and cycle operations. Signal CA2, which is applied to gate 32210, is a logic ONE for addresses 0020 through 0027. This input is inverted and gates with signal ST03, which is a logic ZERO for addresses 0020 through 0023, as indicated in table 4-IV. Gate 32211 is enabled by these two inputs; the output inhibits write signals  $\overline{WG1G}$  and  $\overline{WG5G}$  and enables the gating complex which produces the other four combinations of write control signals as a function of addresses 0020 through 0023. Write control pulse  $\overline{WG}$  enables gate 32233 for write-in to register G during the shift and cycle functions. All cycling and shifting is done around parity bit position 15 of register G.

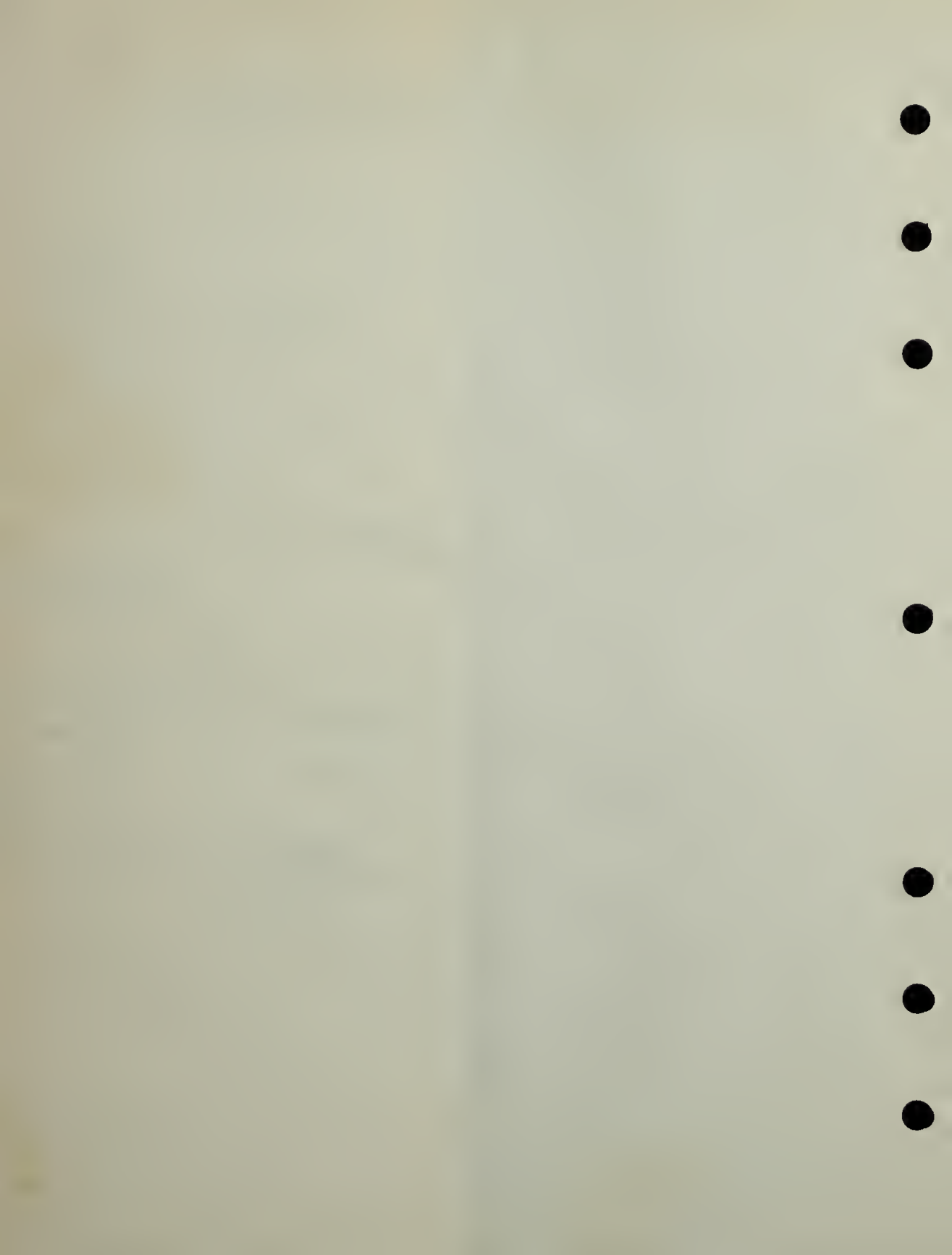
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MODULE	PIN NO	WRITE		CLEAR	OUTPUT	
		80	82	92	84	86
A 1		WLO1	WSG	CSG	ST01	ST01
A 2		WLO2	WSG	CSG	ST02	ST02
A 3		WLO3	WSG	CSG	ST03	ST03
A 4		WLO4	WSG	CSG	ST04	ST04
A 5		WLO5	WSG	CSG	ST05	ST05
A 6		WLO6	WSG	CSG	ST06	ST06
A 7		WLO7	WSG	CSG	ST07	ST07
A 8		WLO8	WSG	CSG	ST08	ST08
A 9		WLO9	WSG	CSG	ST09	ST09
A10		WLO10	WSG	CSG	ST10	ST10
A11		WLO11	WSG	CSG	ST11	ST11
A12		WLO12	WSG	CSG	ST12	ST12
A13		SQI3	WSOF	CSOG	ST13	ST13
A14		SQI4	WSOF	CSOG	ST14	ST14
A15		WLO15	WSOG	CSOG	ST15	ST15
A16		WLO16	WSOG	CSOG	ST16	ST16

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Figure 4-106. Registers S and SQ (Sheet 1 of 2)



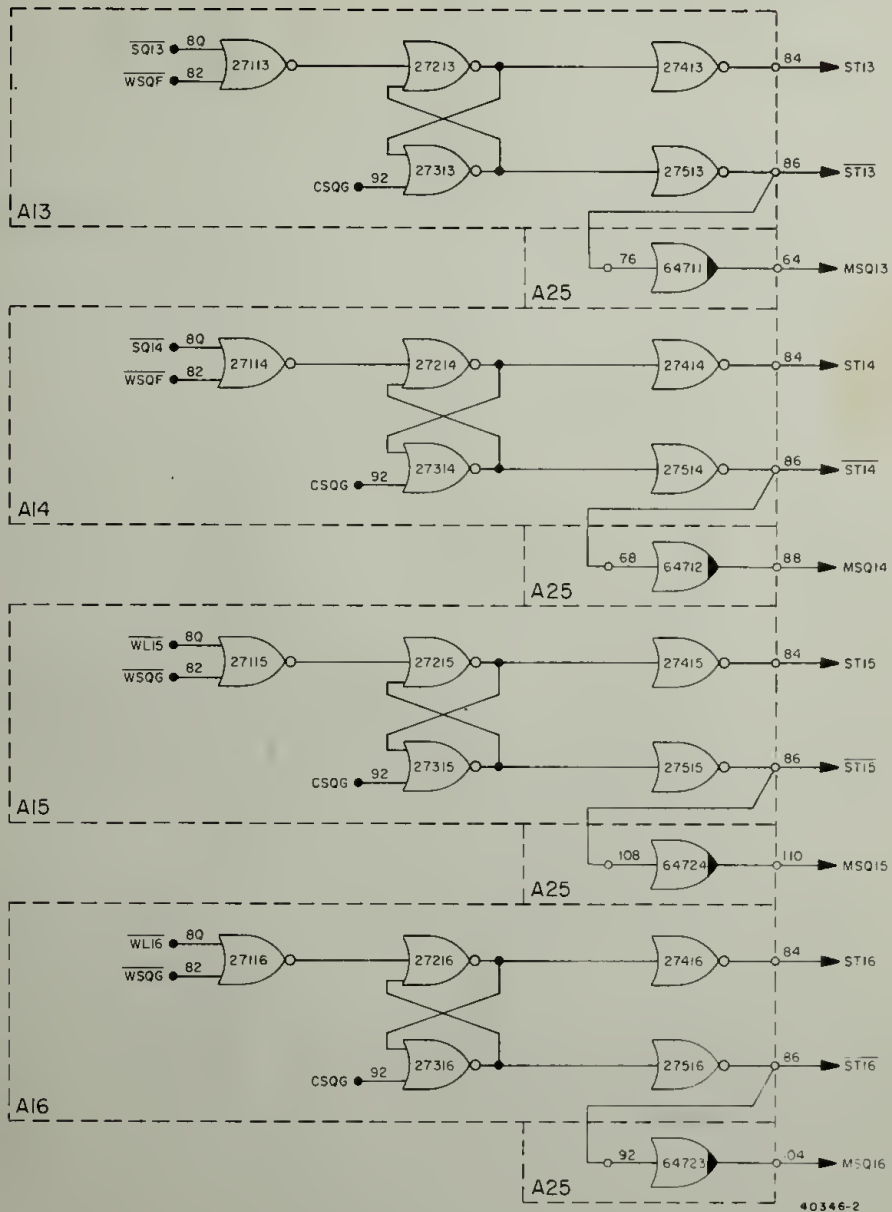
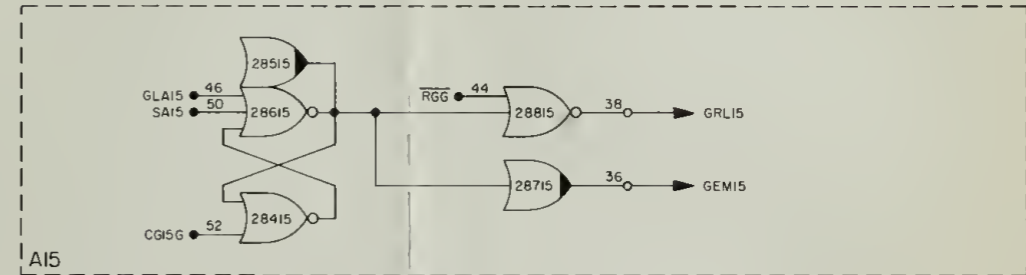
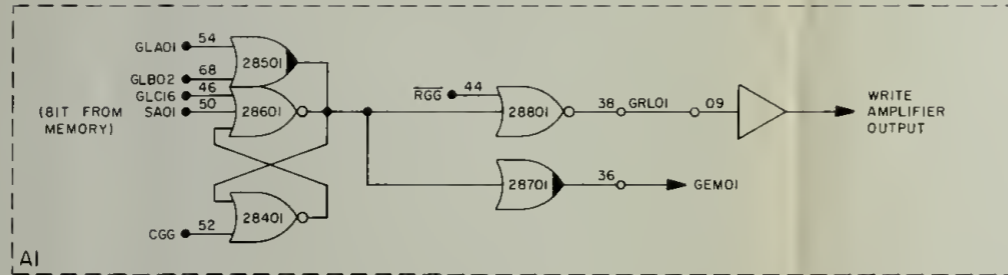


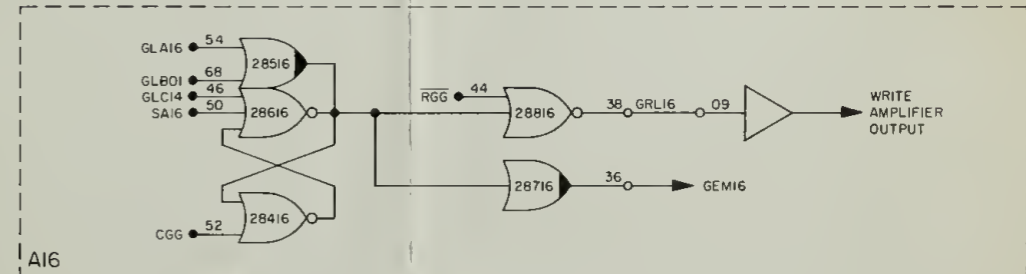
Figure 4-106. Registers S and SQ (Sheet 2 of 2)

Table 4-IV. Address and Control Signals for Shift and Cycle Operations

Signal	Address	Register S Content						Register G Write Control
		ST06	ST05	ST04	ST03	ST02	ST01	
CA1	10	0	0	1	0	0	0	$\overline{\text{WG1G}}, \overline{\text{WG5G}}$
	11	0	0	1	0	0	1	$\overline{\text{WG1G}}, \overline{\text{WG5G}}$
	12	0	0	1	0	1	0	$\overline{\text{WG1G}}, \overline{\text{WG5G}}$
	13	0	0	1	0	1	1	$\overline{\text{WG1G}}, \overline{\text{WG5G}}$
	14	0	0	1	1	0	0	$\overline{\text{WG1G}}, \overline{\text{WG5G}}$
	15	0	0	1	1	0	1	$\overline{\text{WG1G}}, \overline{\text{WG5G}}$
	16	0	0	1	1	1	0	$\overline{\text{WG1G}}, \overline{\text{WG5G}}$
	17	0	0	1	1	1	1	$\overline{\text{WG1G}}, \overline{\text{WG5G}}$
CA2	20	0	1	0	0	0	0	$\overline{\text{WG2G}}, \overline{\text{WG4G}}$ (cycle right)
	21	0	1	0	0	0	1	$\overline{\text{WG2G}}, \overline{\text{WG5G}}$ (shift right)
	22	0	1	0	0	1	0	$\overline{\text{WG3G}}, \overline{\text{WG6G}}$ (cycle left)
	23	0	1	0	0	1	1	$\overline{\text{WG3G}}, \overline{\text{WG5G}}$ (shift left)
	24	0	1	0	1	0	0	$\overline{\text{WG1G}}, \overline{\text{WG5G}}$
	25	0	1	0	1	0	1	$\overline{\text{WG1G}}, \overline{\text{WG5G}}$
	26	0	1	0	1	1	0	$\overline{\text{WG1G}}, \overline{\text{WG5G}}$
	27	0	1	0	1	1	1	$\overline{\text{WG1G}}, \overline{\text{WG5G}}$



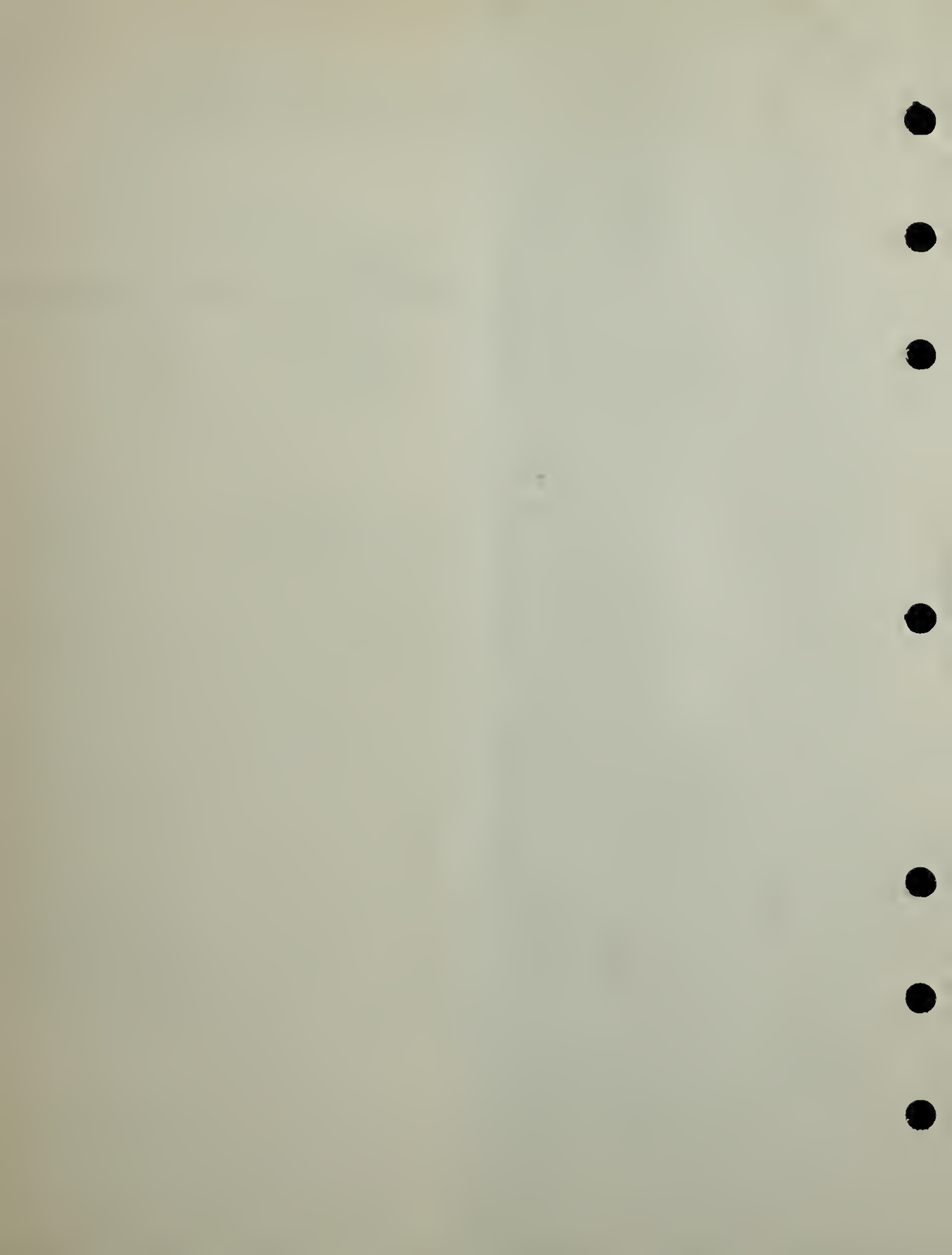
MODULE	PIN NO	WRITE				CLEAR	READ	OUTPUT	TO MEMORY
		54	68	46	50	52	44	38	36
A 1	GLA01	GL802	GLC16	SA01	CGG	$\overline{RGG}$	GRL01	GEM01	
A 2	GLA02	GL803	GLC01	SA02	CGG	$\overline{RGG}$	GRL02	GEM02	
A 3	GLA03	GL804	GLC02	SA03	CGG	$\overline{RGG}$	GRL03	GEM03	
A 4	GLA04	GL805	GLC03	SA04	CGG	$\overline{RGG}$	GRL04	GEM04	
A 5	GLA05	GL806	GLC04	SA05	CGG	$\overline{RGG}$	GRL05	GEM05	
A 6	GLA06	GL807	GLC05	SA06	CGG	$\overline{RGG}$	GRL06	GEM06	
A 7	GLA07	GL808	GLC06	SA07	CGG	$\overline{RGG}$	GRL07	GEM07	
A 8	GLA08	GL809	GLC07	SA08	CGG	$\overline{RGG}$	GRL08	GEM08	
A 9	GLA09	GL810	GLC08	SA09	CGG	$\overline{RGG}$	GRL09	GEM09	
A 10	GLA10	GL811	GLC09	SA10	CGG	$\overline{RGG}$	GRL10	GEM10	
A 11	GLA11	GL812	GLC10	SA11	CGG	$\overline{RGG}$	GRL11	GEM11	
A 12	GLA12	GL813	GLC11	SA12	CGG	$\overline{RGG}$	GRL12	GEM12	
A 13	GLA13	GL814	GLC12	SA13	CGG	$\overline{RGG}$	GRL13	GEM13	
A 14	GLA14	GL816	GLC13	SA14	CGG	$\overline{RGG}$	GRL14	GEM14	
A 15			GLA15	SA15	CG15G	$\overline{RGG}$	GRL15	GEM15	
A 16	GLA16	GL801	GLC14	SA16	CGG	$\overline{RGG}$	GRL18	GEM16	

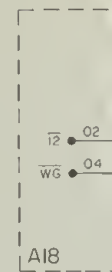
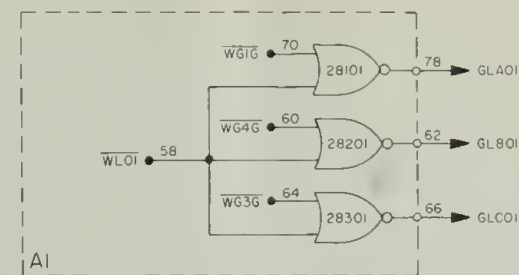
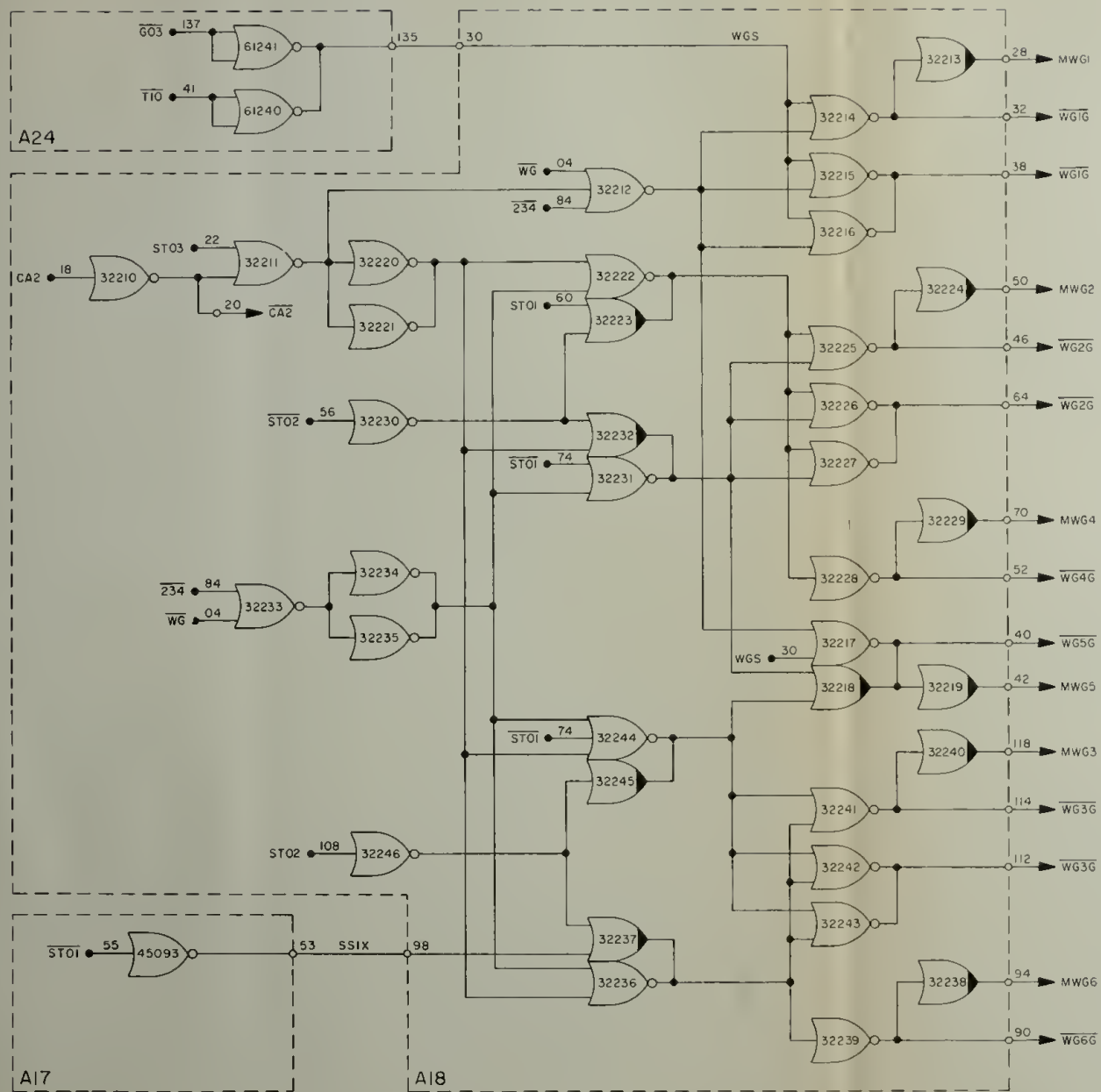


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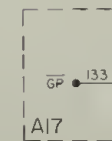
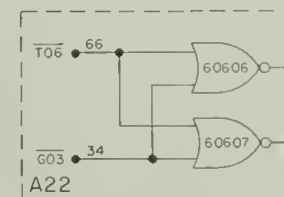
Figure 4-107. Register G

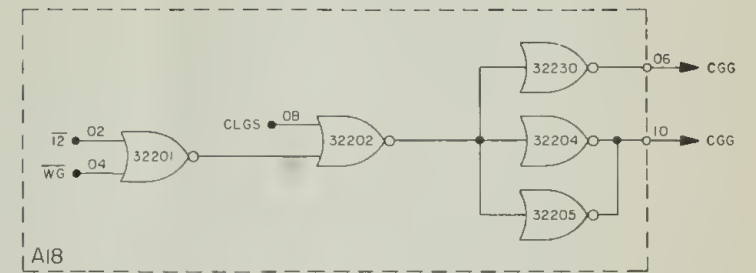
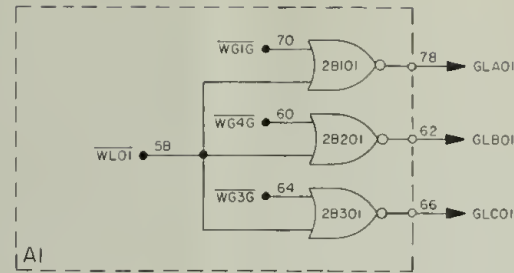
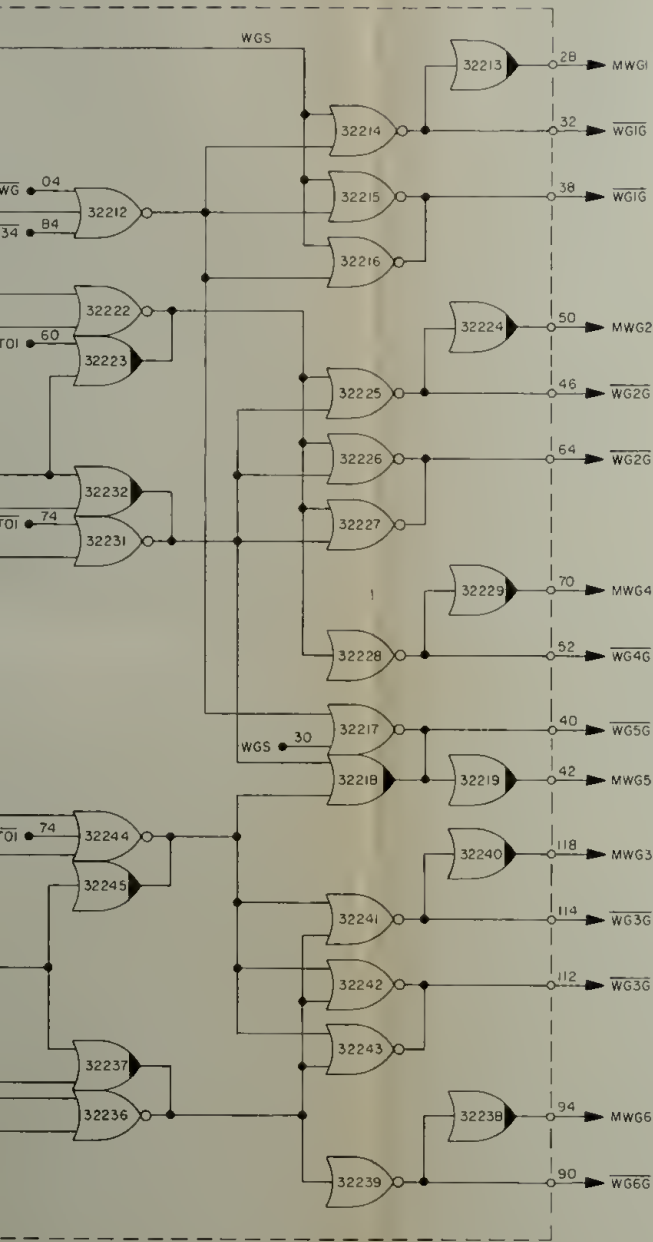




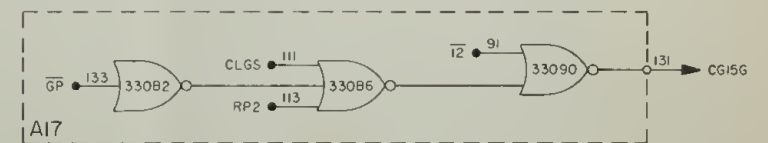
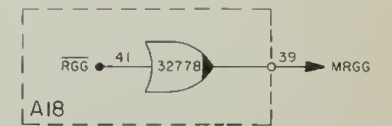
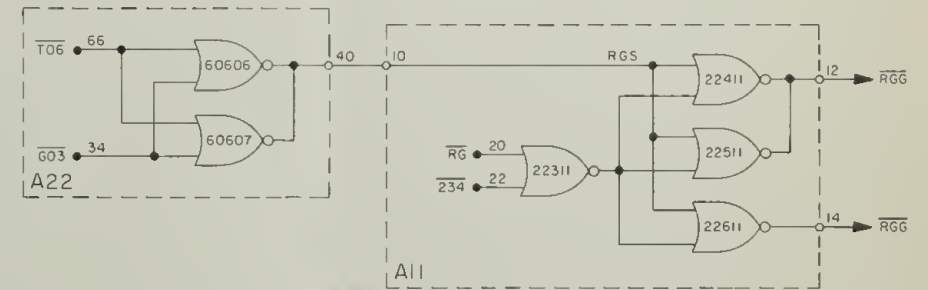


MODULE	PIN NO	WRITE CONTROL				OUTPUT		
		58	70	60	64	78	62	68
A 1	$\overline{WLO1}$	$\overline{WG1G}$	$\overline{WG4G}$	$\overline{WG3G}$	GLA01	GL801	GLC01	
A 2	$\overline{WLO2}$	$\overline{WG1G}$	$\overline{WG2G}$	$\overline{WG3G}$	GLA02	GL802	GLC02	
A 3	$\overline{WLO3}$	$\overline{WG1G}$	$\overline{WG2G}$	$\overline{WG3G}$	GLA03	GL803	GLC03	
A 4	$\overline{WLO4}$	$\overline{WG1G}$	$\overline{WG2G}$	$\overline{WG3G}$	GLA04	GL804	GLC04	
A 5	$\overline{WLO5}$	$\overline{WG1G}$	$\overline{WG2G}$	$\overline{WG3G}$	GLA05	GL805	GLC05	
A 6	$\overline{WLO6}$	$\overline{WG1G}$	$\overline{WG2G}$	$\overline{WG3G}$	GLA06	GL806	GLC06	
A 7	$\overline{WLO7}$	$\overline{WG1G}$	$\overline{WG2G}$	$\overline{WG3G}$	GLA07	GL807	GLC07	
A 8	$\overline{WLO8}$	$\overline{WG1G}$	$\overline{WG2G}$	$\overline{WG3G}$	GLA08	GL808	GLC08	
A 9	$\overline{WLO9}$	$\overline{WG1G}$	$\overline{WG2G}$	$\overline{WG3G}$	GLA09	GL809	GLC09	
A 10	$\overline{WLO10}$	$\overline{WG1G}$	$\overline{WG2G}$	$\overline{WG3G}$	GLA10	GL810	GLC10	
A 11	$\overline{WLO11}$	$\overline{WG1G}$	$\overline{WG2G}$	$\overline{WG3G}$	GLA11	GL811	GLC11	
A 12	$\overline{WLO12}$	$\overline{WG1G}$	$\overline{WG2G}$	$\overline{WG3G}$	GLA12	GL812	GLC12	
A 13	$\overline{WLO13}$	$\overline{WG1G}$	$\overline{WG2G}$	$\overline{WG3G}$	GLA13	GL813	GLC13	
A 14	$\overline{WLO14}$	$\overline{WG1G}$	$\overline{WG2G}$	$\overline{WG6G}$	GLA14	GL814	GLC14	
A 15	PGT	PARBUS	---	---	GLA15	---	---	
A 16	$\overline{WLO16}$	$\overline{WG5G}$	$\overline{WG2G}$	$\overline{WG3G}$	GLA16	GL816	GLC16	



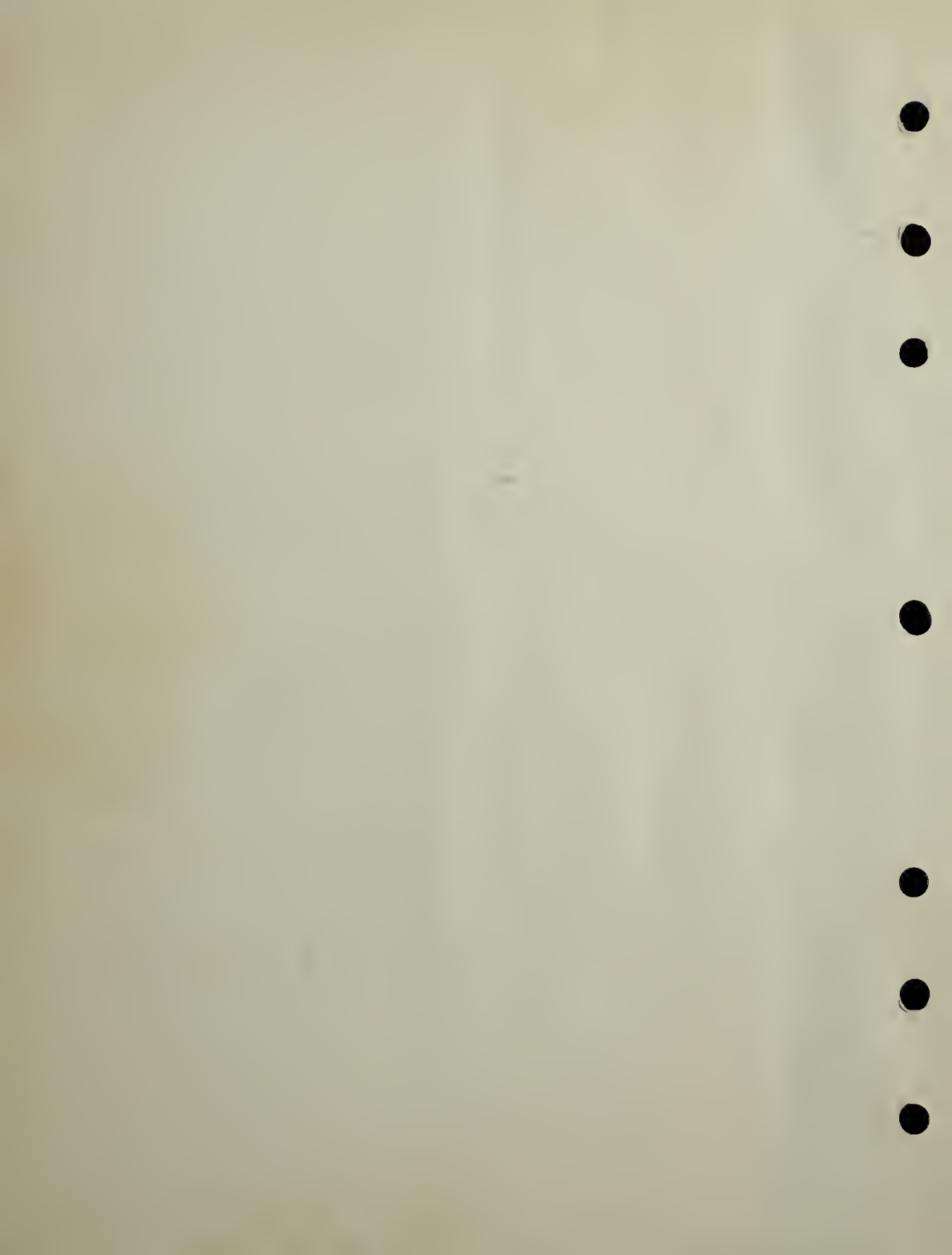


PIN NO MODULE	WRITE CONTROL				OUTPUT		
	5B	70	60	64	78	62	6B
A 1	WL01	WG1G	WG4G	WG3G	GLA01	GLB01	GLC01
A 2	WL02	WG1G	WG2G	WG3G	GLA02	GLB02	GLC02
A 3	WL03	WG1G	WG2G	WG3G	GLA03	GLB03	GLC03
A 4	WL04	WG1G	WG2G	WG3G	GLA04	GLB04	GLC04
A 5	WL05	WG1G	WG2G	WG3G	GLA05	GLB05	GLC05
A 6	WL06	WG1G	WG2G	WG3G	GLA06	GLB06	GLC06
A 7	WL07	WG1G	WG2G	WG3G	GLA07	GLB07	GLC07
A 8	WL08	WG1G	WG2G	WG3G	GLA08	GLB08	GLC08
A 9	WL09	WG1G	WG2G	WG3G	GLA09	GLB09	GLC09
A10	WL10	WG1G	WG2G	WG3G	GLA10	GLB10	GLC10
A11	WL11	WG1G	WG2G	WG3G	GLA11	GLB11	GLC11
A12	WL12	WG1G	WG2G	WG3G	GLA12	GLB12	GLC12
A13	WL13	WG1G	WG2G	WG3G	GLA13	GLB13	GLC13
A14	WL14	WG1G	WG2G	WG6G	GLA14	GLB14	GLC14
A15	PGT	PARBUS	---	---	GLA15	---	---
A16	WL16	WG5G	WG2G	WG3G	GLA16	GLB16	GLC16

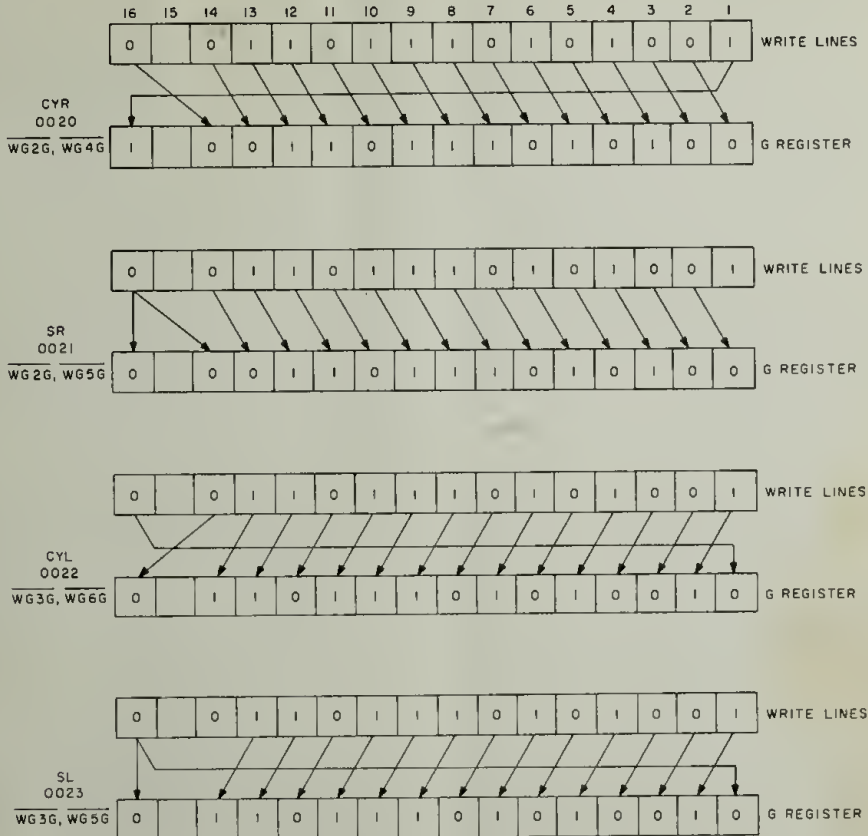


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Figure 4-108. Register G Service



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Figure 4-109. Register G Shift and Cycle

Octal address 0020 causes a word to be cycled right when entered into register G. This address, coincident with write control pulse  $\overline{WG}$ , enables gates 32222 and 32223 and causes write control signals  $\overline{WG2G}$  and  $\overline{WG4G}$  to be generated. Data is cycled right as shown on figure 4-109.

Address 0021 enables gates 32231 and 32232 and causes write signals  $\overline{WG2G}$  and  $\overline{WG5G}$  to be generated for a shift-right operation. Bit 16 from the write lines is entered into bit positions 16 and 14 of register G, and all the other bits are shifted one position to the right. No action occurs with bit 1 from the write lines; this bit is effectively shifted off the end.

Address 0022 enables gates 32236 and 32237 and causes write signals  $\overline{WG3G}$  and  $\overline{WG6G}$  to be generated for a cycle-left operation. As shown on figure 4-109, bit 16 from the write lines is written into bit position 1 of register G. Bit position 2 of register G contains bit 1 from the write lines up to bit position 16, which contains bit 14 from the write lines.

Address 0023 enables gates 32244 and 32245 and causes write signals  $\overline{WG3G}$  and  $\overline{WG5G}$  to be generated for a shift left. Bit 16 from the write lines is entered into bit positions 16 and 1 of register G, and all other bits are entered into register G one position to the left. No action occurs with bit 14 from the write lines; this bit is effectively shifted off the end.

The write control signals described previously are applied to 16 groups of gates (3 gates in each group). Logic modules A1 through A16 each contain one identical group of gates. The group located on logic module A1 is illustrated on figure 4-108. The table beneath this gating configuration indicates the connections to the gates for the corresponding logic module. In module A1 write line input  $\overline{WL01}$  gates with write signals  $\overline{WG1G}$ ,  $\overline{WG4G}$ , and  $\overline{WG3G}$  and causes output GLA01, GLB01, or GLC01 to be generated, depending on the operation involved. Normally, GLA01 (through GLA16) is generated. This output, which is actually bit 1 from the write lines, is applied to bit position 1 of register G (figure 4-107). Control signal GLB01 is generated by gating signals  $\overline{WL01}$  and  $\overline{WG4G}$ . The latter signal is produced during a cycle-right operation. Note in the table on figure 4-107 that signal GLB01 feeds bit position 16 of register G, GLB02 bit position 1, et cetera. Control signal GLC01 is generated by gating signals  $\overline{WL01}$  and  $\overline{WG3G}$ . The latter signal is produced during both cycle-left and shift-left operations and causes bit 1 from the write lines to be deposited in bit position 2 of register G.

The clear signal for register G (CGG) is generated by write control pulse  $\overline{WG}$  from the sequence generator and timing signal  $\overline{12}$  or by control pulse CLGS, also generated in the sequence generator.

The read signal ( $\overline{RGG}$ ) is also generated as a function of two separate inputs. Normally, control pulse  $\overline{RG}$  gates with timing signal  $\overline{234}$  to produce  $\overline{RGG}$ . The second input is the result of gating  $\overline{T06}$  and  $\overline{G03}$ . Signal  $\overline{G03}$  indicates an increment, decrement, or shift command (PINC, MINC, SHINC, respectively) for the counters in erasable memory. Thus, at time 6, during PINC, MINC, or SHINC, read signal  $\overline{RGG}$  is generated.

A separate clear signal, CG15G, is generated for bit position 15 (parity bit position) of register G. When a parity bit is to be generated, control pulse GP enables gate 33082 and, coincident with timing signal 12, generates signal CG15G. Signal CLGS also causes signal CG15G to be generated. The third condition involves read signal RP2. This latter input is generated during an exchange instruction and indicates a readout of register P2 in the parity section. The output from this single bit register is the parity bit of a word to be written into register G. Clear signal CG15G is generated prior to this bit being written into register G.

4-8.3.15 Adder (Registers X and Y) Detailed Description. The adder (figure 4-110) is a 16 bit parallel adder with end-around carry and is the basic arithmetic unit of the AGC. The adder processes two numbers at a time, one number each is contained in registers X and Y. The output gating complex senses for the carry, and in addition, provides outputs from each bit position to the write lines.

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PIN NO MODULE	WRITE			CLEAR	READ	CARRY		OUTPUT
	31	32	34	33	37	35	36	38
A 1	WLO1	WXG	WYG	CUG	RUG	CBT1	CRY01	URL01
A 2	WLO2	WXG	WYG	CUG	RUG	CRY01	CRY02	URL02
A 3	WLO3	WXG	WYG	CUG	RUG	CRY02	CRY03	URL03
A 4	WLO4	WXG	WYG	CUG	RUG	CRY03	CRY04	URL04
A 5	WLO5	WXG	WYG	CUG	RUG	CRY04	CRY05	URL05
A 6	WLO6	WXG	WYG	CUG	RUG	CRY05	CRY06	URL06
A 7	WLO7	WXG	WYG	CUG	RUG	CRY06	CRY07	URL07
A 8	WLO8	WXG	WYG	CUG	RUG	CRY07	CRY08	URL08
A 9	WLO9	WXG	WYG	CUG	RUG	CRY08	CRY09	URL09
A10	WLO10	WXG	WYG	CUG	RUG	CRY09	CRY10	URL10
A11	WLO11	WXG	WYG	CUG	RUG	CRY10	CRY11	URL11
A12	WLO12	WXG	WYG	CUG	RUG	CRY11	CRY12	URL12
A13	WLO13	WXG	WYG	CUG	RUG	CRY12	CRY13	URL13
A14	WLO14	WXG	WYG	CUG	RUG	CRY13	CRY14	URL14
A15	WLO15	WXG	WYG	CUG	RUG	CRY14	CRY15	URL15
A16	WLO16	WXG	WYG	CUG	RUAC	CRY15	CRY16	URL16

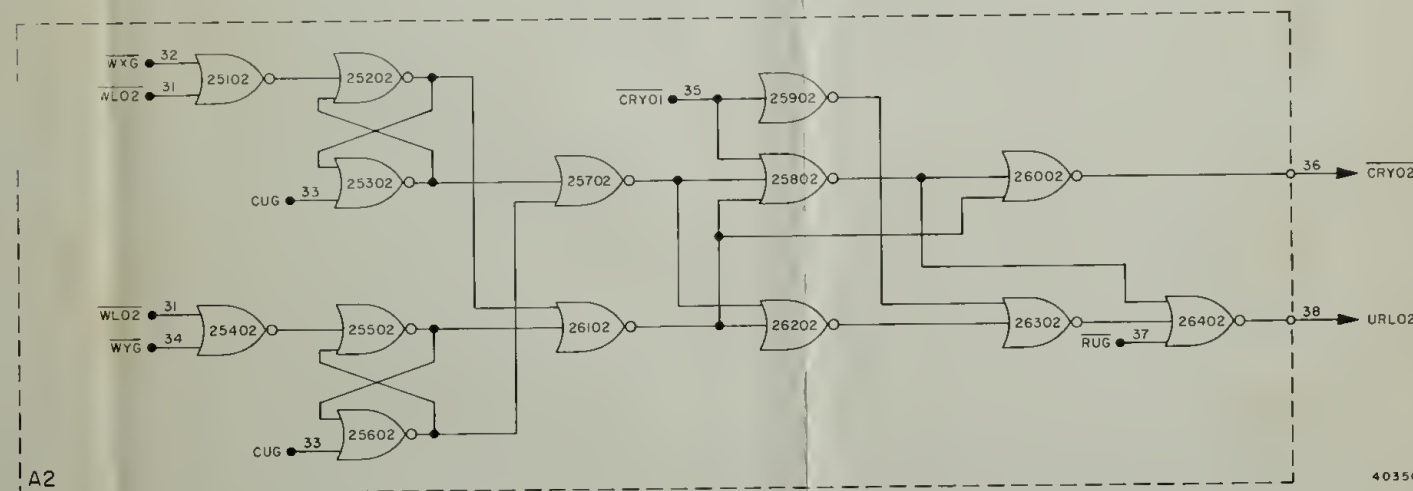
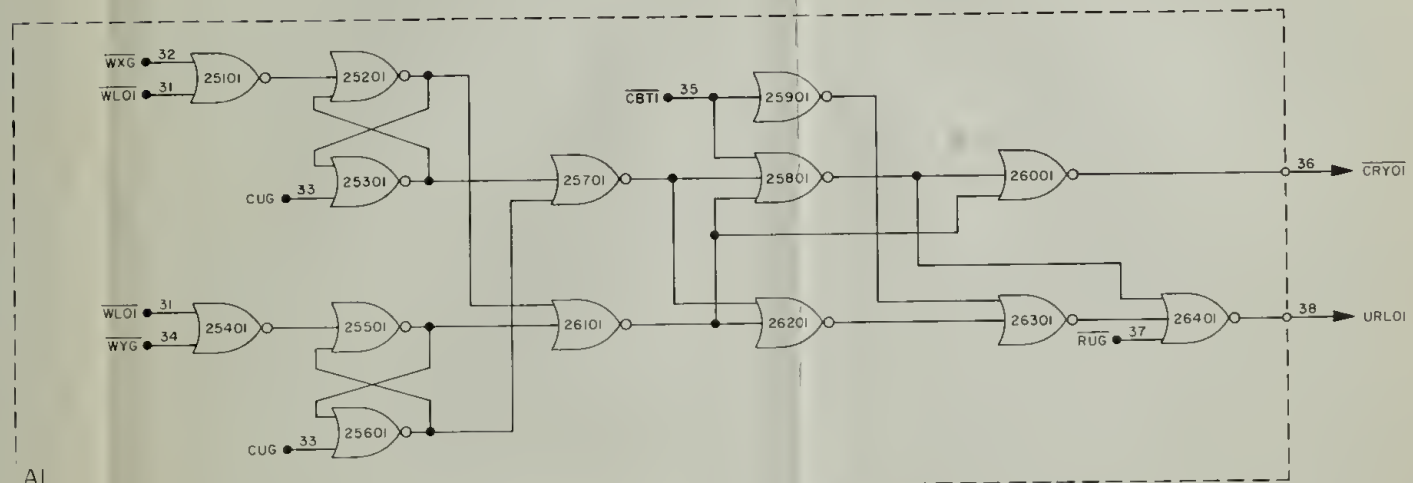
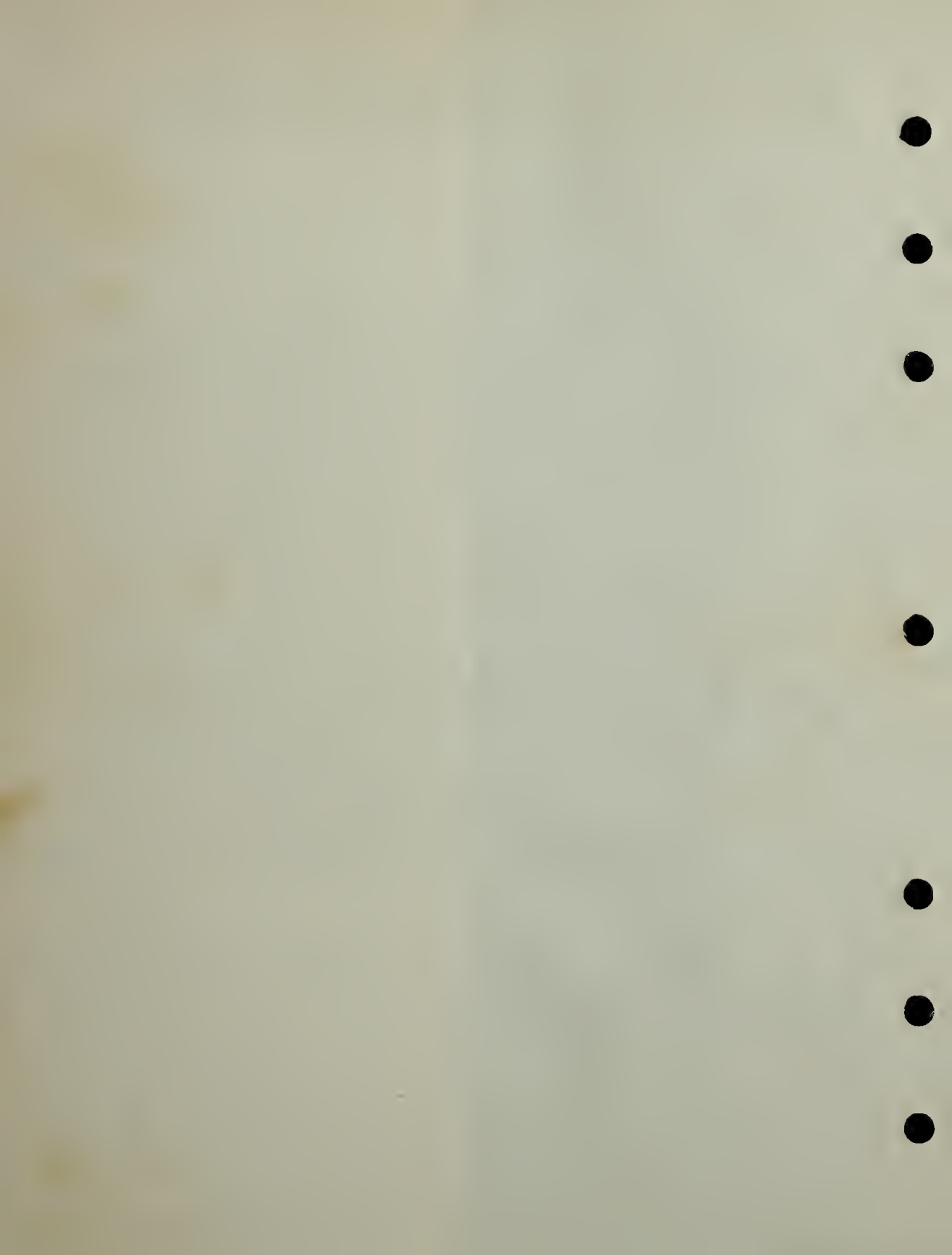


Figure 4-110. Adder (X and Y Registers - Bit Position 1, 2)





## APOLLO GUIDANCE AND NAVIGATION SYSTEM

Registers X and Y are functionally identical to the other flip-flop registers of the central processor. Write signals  $\overline{WXG}$  and  $\overline{WYG}$  are generated to gate information from the write lines into each register. As shown in the service section for the adder (figure 4-111) the write signals are produced as a function of control pulses  $\overline{WX}$  and  $\overline{WY}$  or signals WXS and WYS.

Control pulses  $\overline{WX}$  and  $\overline{WY}$  are generated in the sequence generator and gate with timing signal 234 to produce write signals  $\overline{WXG}$  and  $\overline{WYG}$ . This method is identical to that described previously for generating write signals for the flip-flop registers.

Signals WXS and WYS are a function of counter instructions PINC, MINC, and SHINC. Signal WXS is generated at time 6 coincident with a PINC, MINC, or SHINC instruction ( $\overline{GO3}$  is the logic OR of these three counter instructions). Signal WYS is generated at time 6 coincident with a SHINC instruction only. During instructions PINC and MINC the quantity of the addressed counter from erasable memory is entered into register X at time 6 by control pulse WXS. The quantity plus one during PINC or minus one during MINC is entered into register Y at time 4 by control pulse  $\overline{WY}$ .

Instruction SHINC is a shift instruction, and the shifting is accomplished by entering the quantity of the addressed counter into both registers X and Y at time 6. During instruction SHINC, write control pulse  $\overline{WY}$  is generated at time 4 and the registers are cleared. There is no information on the write lines at this time, however. At time 6 the quantity of the addressed counter from erasable memory is simultaneously entered into registers X and Y by control pulses WXS and WYS.

The clear signal, CUG, is generated as a function of write control pulse  $\overline{WY}$  and clears both registers X and Y simultaneously. Register Y is written into first for all instructions except SHINC.

The read signal,  $\overline{RUG}$ , is generated as a function of read control pulse  $\overline{RU}$  or signal RUS. Signal RUS is generated during instructions PINC, MINC, and SHINC to read out the content of the adder. The read signal is applied to the read gate of each bit position (1 through 15). Actually, the read gate contains the summation of the bits in registers X and Y. For example, gate 26401 in figure 4-110 is the summation of the two bits entered into bit position 1 of registers X and Y. The read gate outputs URL01 through URL15 are applied directly to the write amplifiers.

Output URL16 is applied to the write amplifiers as UWL16 through gates 35156 and 35157 (figure 4-111) in the service section. This allows read-out of bit 16 to be inhibited and prevent end-around carry when angular data is processed. The overflow bit position (URL15) is placed on the write lines in place of bit 16 when angular data is processed. Bit position 16 of the adder is read out by signal  $\overline{RUAC}$ , which is read and carry (if any). The read signal,  $\overline{RUG}$ , enables gate 35153 and causes  $\overline{RUAC}$  to be produced except when memory locations 0041, 0047, and 0050 through 0056 are addressed (UPLINK, CDU, OPT, and TRKR). The carry gate output from each bit position (CRY01 through CRY16) is applied to the next-higher-order bit position ( $\overline{CRY01}$  to bit position 2 et cetera). The end-around carry from bit position 16 ( $\overline{CRY16}$ ) is applied to bit position 1 through the service section (gate 35135) as  $\overline{CBT1}$ .

End-around carry is inhibited during a SHINC instruction when the UPLINK counter (address 0041 into gate 35145) or the RADAR IN counter (address 0056 into gate 35143) is being incremented and when angular data (OPT and TRKR counters) is processed. A logic ONE is forced into bit position 1 during certain instructions by the carry-in flip-flop (FF35136-35137). Control pulse CI is generated by the sequence generator and sets the flip-flop. The set output is inverted by gate 35135 and applied as an enabling level to the carry-in gate of bit position 1. Clear signal CUG resets the flip-flop.

Figure 4-112 shows several examples of quantities that could be entered into the adder during normal computations and when angular data is being processed. Negative numbers processed during normal computations are in ONE's complement notation. There are no negative quantities except minus ONE (MINC) during the addition of angular data. All numbers representing angles are positive. For convenience, three bit quantities with sign and overflow/underflow bit positions have been chosen. These quantities can be both positive, both negative, or of opposite sign. A positive number has a ZERO in the sign bit position, a negative number a ONE.

The quantities entered into the adder during normal computations contain the sign bit in both positions 15 and 16. If overflow or underflow occurs, bit positions 15 will contain a value bit which is opposite to the correct sign bit. A ONE in bit position 15 indicates overflow when both operands are positive; a ZERO in bit position 15 indicates underflow when both operands are negative. The correct sign of the sum is always contained in bit position 16. The addition of two negative quantities almost always results in end-around carry since negative binary numbers are the complements of positive numbers, though not the corresponding positive numbers. This can be ascertained from the scale in figure 4-112.

When angular data is processed, bit position 15 is used as an additional value bit position. A ONE or a ZERO in this bit position has no significance as overflow/underflow bit since during the addition of angular data, all numbers are positive.

When dealing with angular data, the incremental inputs represent rotations up to 360°. Angles between 0° and 180° are represented by the octal quantities 00000 and 40000 respectively. The quantity representing one increment less than 180° contains ONE's in the first 14 bit positions of the word as indicated in figure 4-112. In order to accommodate the angles between 180° and 360° the capacity of the register must be increased. This is accomplished by using the overflow/underflow bit (bit 15). Incremental inputs can now step the register to a maximum quantity of 77777 octal, which represents one increment less than 360°.

Bit 16 (URL16) is applied to the write lines as UWL16 through gates 35156 and 35157 during general computations (as shown in the examples of figure 4-112). Output URL15 applied to gate 35152 is inhibited at this time by the output of gate 35149. This gate output, in conjunction with signal URL15, is used to prevent end-around carry when angular data is being added. This process is described in the following paragraphs.

Read-out of bit 16 and consequently end-around-carry is inhibited when the UPLINK, CDU, OPT, and TRKR counters of erasable memory are incremented or

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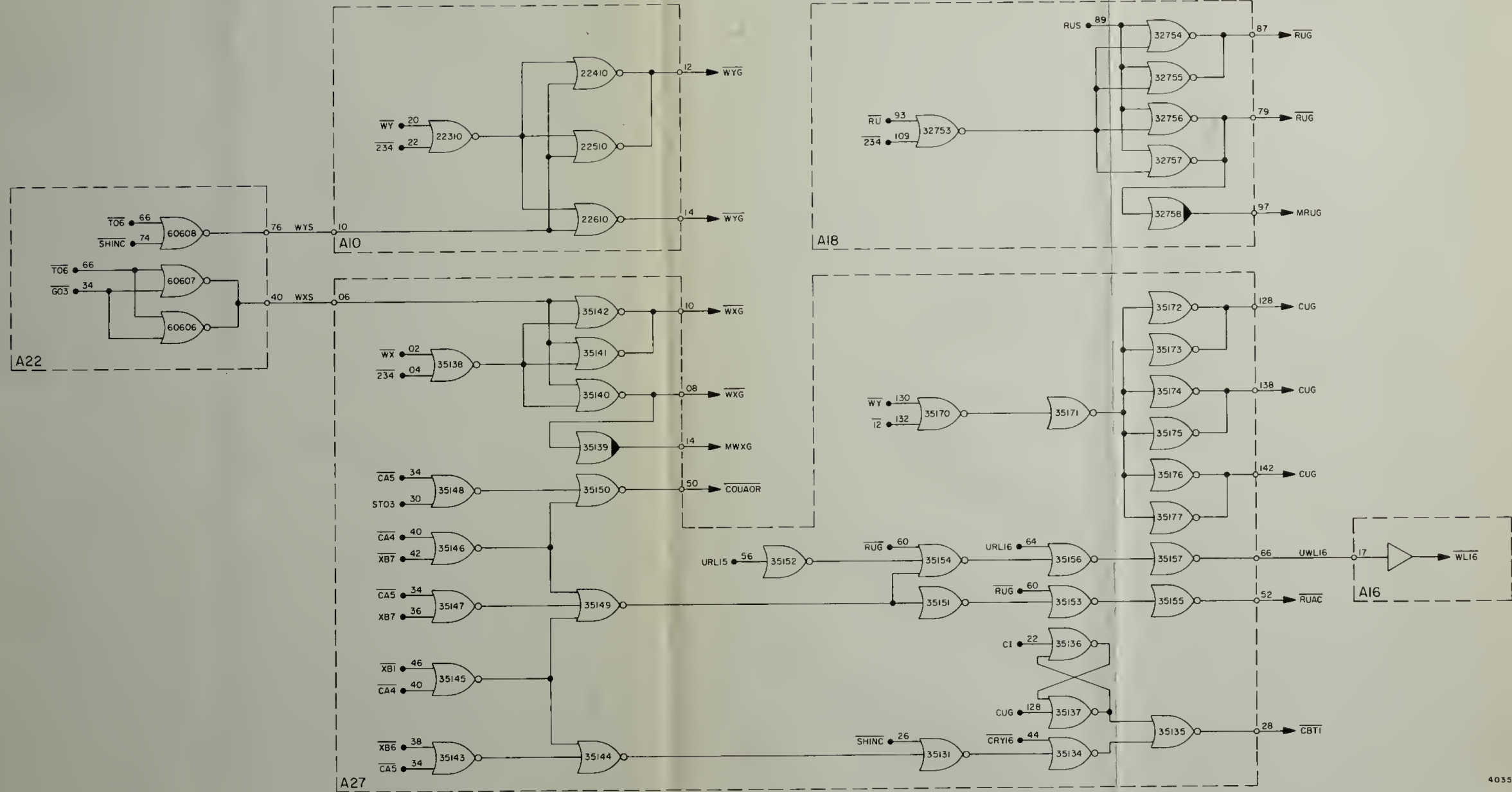
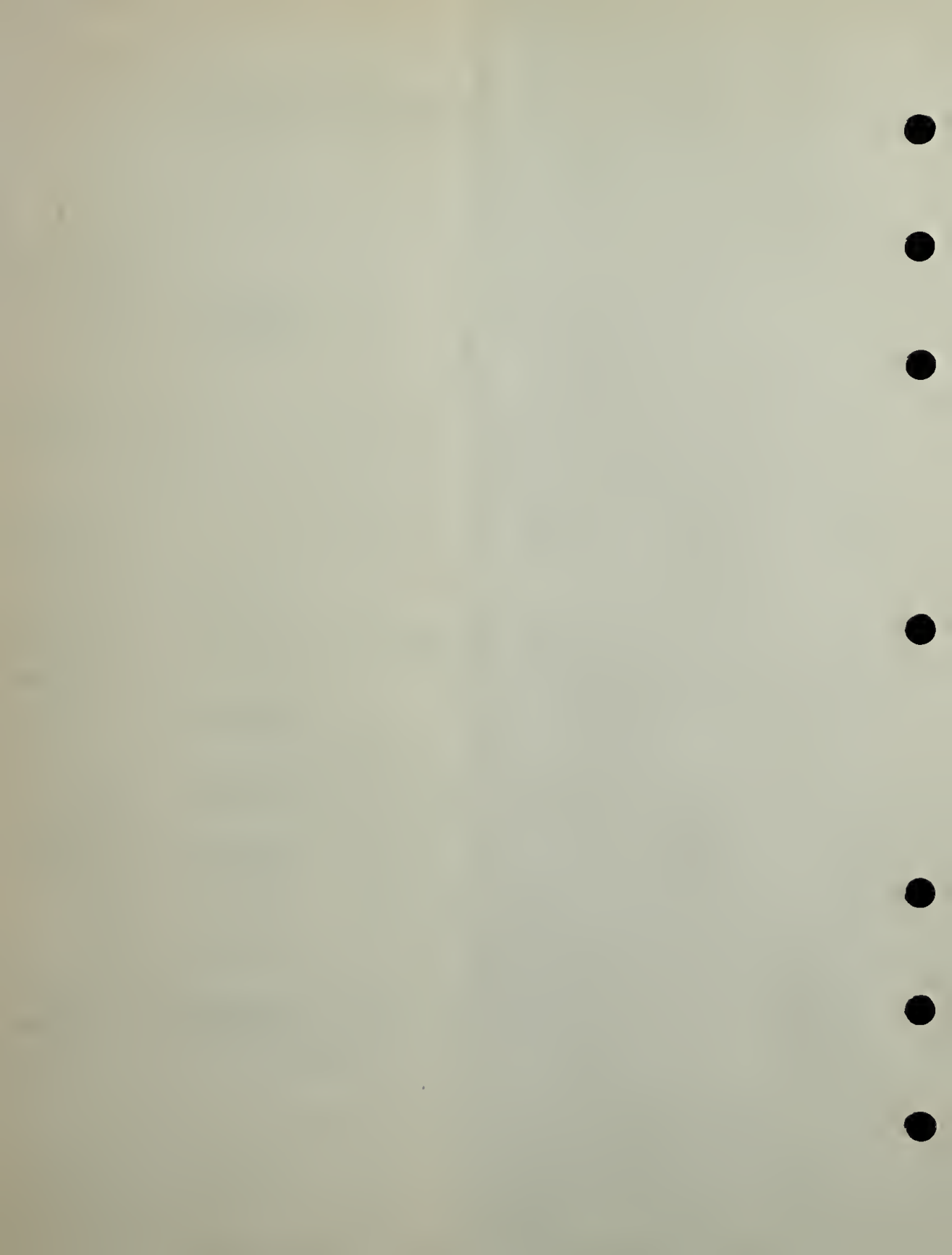


Figure 4-111. Adder (X and Y) Service



X (+4)	00100	Two Positive Quantities No Overflow
Y (+1)	00001	
U (+5)	00101	
X (-4)	11011	Two Negative Quantities No Underflow
Y (-1)	11110	
U (+5)	00101	
U (-5)	11010	Two Positive Quantities With Overflow
X (+6)	00110	
Y (+3)	00011	
U (+9)	01001	Two Negative Quantities With Underflow
X (-6)	11001	
Y (-3)	11100	
U (-9)	10110	Two Quantities of Opposite Sign
X (+1)	00001	
Y (-7)	11000	
U (-6)	11001	

NORMAL COMPUTATION

+7	0	0111
+6	0	0110
+5	0	0101
+4	0	0100
+3	0	0011
+2	0	0010
+1	0	0001
+0	0	0000
-0	1	1111
-1	1	1110
-2	1	1101
-3	1	1100
-4	1	1011
-5	1	1010
-6	1	1001
-7	1	1000

SCALE  
Negative Numbers  
in ONES  
Complement  
Notation

0	0	0000	0°
1	0	0001	
2	0	0010	
3	0	0011	
4	0	0100	
5	0	0101	
6	0	0110	
7	0	0111	
*8	1	1000	180°
9	1	1001	
10	1	1010	
11	1	1011	
12	1	1100	
13	1	1101	
14	1	1110	
15	1	1111	
0	0	0000	360°

\*Quantities representing angles of 180° and beyond carry a ONE in the sign bit position and are not negative numbers. Read-out of the sign bit positions is inhibited during the addition of angular data - what appears in bit position 15 (OVF/UNF hit) is placed on the write-lines in the sign bit position. A ONE in bit position 16 indicates angles of 180° and beyond.

PLUS INCREMENT (PINC)

X	0	0111	(Represents one increment less than 180°)
Y			(No quantity entered into Y during PINC)
CDUADR (CI) (+1)	0	0001	(Control pulse CDUADR causes forced carry)
U	1	1000	(Carry into OVF/UNF bit to represent 180°)

This represents bit position 15 which now becomes part of the magnitude for angles between 180° and 360° if any more positive increments occur.

Sign bit position now contains same quantity as bit position 15. Read-out of this position is inhibited and is replaced by bit 15.

X	1	1111	(Represents one increments less than 360°)
Y			(No quantity entered into Y during PINC)
CDUADR (CI) (+1)	0	0001	
U	1	0000	

This ONE would normally carry into bit position 16 and change the sign, but since read-out is inhibited, it is replaced by bit 15.

MINUS INCREMENT (MINC)

X (0)	0	0000	
Y (-1)	1	1110	(Quantity [-1] entered into Y by MINC command)
CDUADR (CI) (+1)	0	0001	(Control pulse CDUADR causes forced carry)
U	1	1111	(Represents one increment less than 360°)

X (1)	0	0001	(Represents one increment more than 0°)
Y (-1)	1	1110	(Quantity [-1] entered into Y by MINC command)
CDUADR (CI) (+1)	0	0001	
U (0)	0	0000	

Inhibit Carry  
(Carry is inhibited and correct sum with sign appears at output gates)

ADDITION OF ANGULAR DATA

Figure 4-112. Addition of Two Binary Numbers



decremented. Addresses 41 (UPLINK), 47, 50, 51 (CDU X, Y, Z), 52, 53, (OPT X, Y) or 54, 55, 56 (TRKR) result in an enabling output from gate 35149 to gates 35151 and 35154. This inhibits the read and carry signal ( $\overline{RUAC}$ ) for bit position 16 and allows URL15 to be read out to write lines 15 and 16. Since readout of bit position 16 is now inhibited, the output line URL16 is a logic ZERO and enables gate 35156. When read signal  $\overline{RUG}$  enables gate 35154, bit position 15 (URL15) is placed on the write line as signal UWL16.

Any one of the CDU counter addresses (47, 50, or 51) or OPT counter addresses (52, 53) causes control pulse  $\overline{CDUADR}$  to be generated. This control pulse in turn produces a forced carry (C1), which sets the carry-in flip-flop and forces a logic ONE (CBT1) into bit position 1 of the adder. This operation occurs only when the CDU or OPT counters are being incremented or decremented. Address 47 enables gate 35146; the combination of inputs to gate 35148 enables this gate for addresses 50 and 51, 52 and 53. The output from either one of these gates is inverted by gate 35150 and results in  $\overline{CDUADR}$  as an enabling level. This output is a logic ONE for all other addresses. This forced carry occurs in place of value 00001, which is normally entered into Y during a PINC instruction by control pulse RB1. Output  $\overline{CDUADR}$  inhibits RB1 when the CDU counters are incremented during a PINC instruction.

**4-8.3.16 Write Amplifiers Detailed Description.** The write amplifier (figure 4-113) is an extended NOR gate with a capacity of 24 inputs. One write amplifier is contained in each of the 16 logic modules (A1 through A16). Outputs WL01 through WL16 and their complements are available and are designated as the write lines.

The write amplifiers function logically as an OR gate. If any one input is a logic ONE, output WL-- is a logic ONE, and the complement output  $\overline{WL--}$  is a logic ZERO. The latter output is used extensively to transfer information from one register to another.

The majority of inputs to the write amplifiers are from the flip-flop registers. The output from each bit position of the registers is wired directly to an associated write amplifier input (bit 1 to write amplifier 1 et cetera). The 16 bit output of any one register involves the write amplifiers on all 16 logic modules (A1 through A16). The flip-flop register inputs can be ascertained on figure 4-94 from the table and simplified logic drawings of the write amplifiers on modules A1 and A16.

The inputs to the write amplifiers, excluding the flip-flop register inputs, are described in the following paragraphs.

Inputs GRL01 through GRL16 are from register G. Bit position 16 of register G is wired to both write amplifiers 15 and 16. This places the sign bit of a word in these two adjacent positions when a transfer of data occurs from memory to the central processor.

The adder outputs are applied to the write lines as URL01 through URL15 and UWL16. Bit 16 is the corrected sign bit of the word.

Inputs CAD01 through CAD06 are from the counter priority control logic and determine the address of the counter in erasable memory which is to be updated. Since these inputs are applied to the six low-order bit positions, counters at locations up to 0077 could be addressed. However, the arrangement of counters in erasable memory at present involves addresses 0034 through 0057. A specific counter address is determined by the correct combination of inputs CAD01 through CAD06. This is illustrated as follows for the address of the UPLINK counter: as an example, address 41. For this particular address, CAD06 and CAD01 are logic ONE's; the remaining are logic ZERO's. Inputs to write amplifiers 7 through 15 are not enabled at this time. Therefore, the full address is 00041 (octal).

Write Line	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1
	0			0			0			4			1		

Outputs RWL11 through RWL14 from register BNK are placed on the write lines through pin 13 of gates 14211 through 14214. Output RWL16 from the same register is placed on the write line through pin 21 of gate 14216. These outputs are identical to R0 through R4 from register BNK, which are used to select among the five banks of fixed memory.

Control pulse RSB (pin 13, gate 14216) is generated during subinstruction DV1 and causes the quantity 1 000 000 000 000 000 (minus zero, 100000 octal) to be placed on the write lines. This action accomplishes one of the required manipulations during this subinstruction.

Control pulse RB2 (pin 21, gate 14202) is generated during subinstruction DV0 and is applied as an input to write amplifier 2. This causes the quantity 0 000 000 000 000 010 (plus two, 000002 octal) to be placed on the write lines to accomplish a specific manipulation during subinstruction DV0.

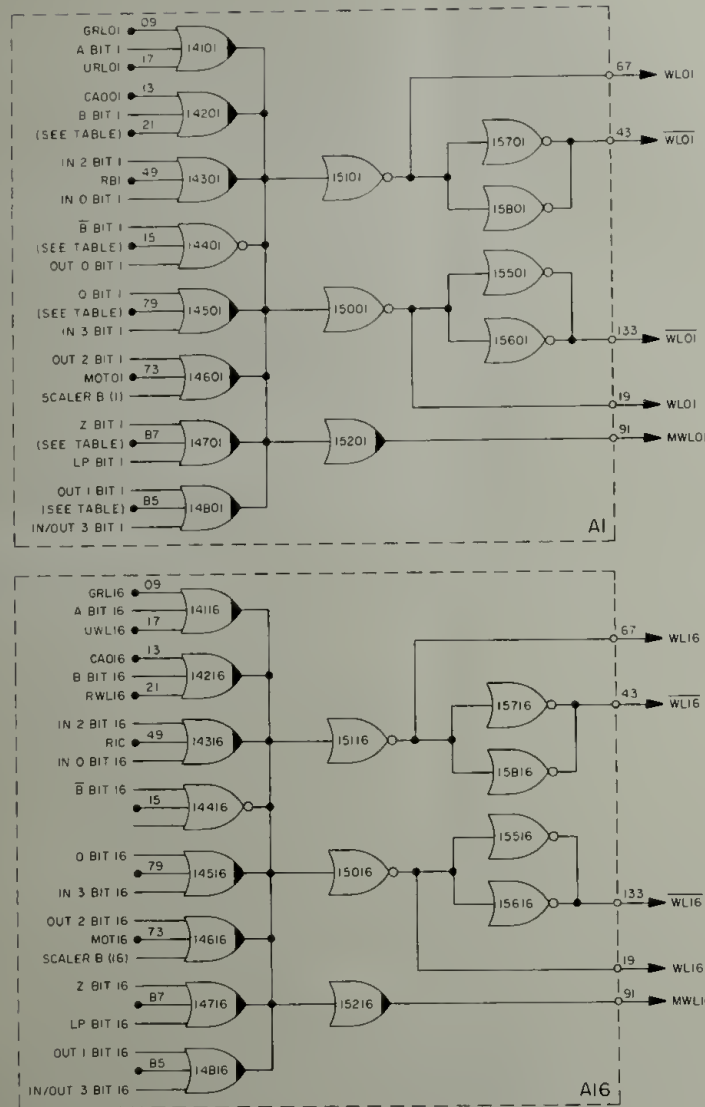
Inputs RAD03 through RAD05 and RAD11 are placed on the write lines from the interrupt priority control logic. These inputs are used to determine one of addresses 2000, 2004, 2010, 2014, 2020, and 2024, which are, respectively, the locations in fixed memory for the first instruction of the T3RUPT, RPT2, T4RUPT, KEYRUPT, UPRUPT, and DOWNRUPT transfer routines. These locations are addressed, as indicated in table 4-V, when interrupt priority control receives interrupt requests.

Control pulse RB14 applied to WL14 is generated during subinstruction MP0. This causes the quantity 0 010 000 000 000 000 (020000 octal) to appear on the write lines. The logic ONE on WL14 is written into bit position 13 of register LP.

Control pulse RB1 is generated during certain subinstructions and causes the quantity plus one (000001 octal) to be placed on the write lines.



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MODULE INPUT	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
PIN 09	GRL16	GRL16	GRL14	GRL13	GRL12	GRL11	GRL10	GRLO9	GRLOB	GRLO7	GRLO6	GRLO5	GRLO4	GRLO3	GRLO2	GRLO1
A BIT	BIT 16	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1
PIN 17	UWL16	URL15	URL14	URL13	URL12	URL11	URL10	URL09	URL08	URL07	URL06	URL05	URL04	URL03	URL02	URL01
PIN 13	RSB		RWL14	RWL13	RWL12	RWL11					CA006	CA005	CA004	CA003	CA002	CA001
B BIT	BIT 16	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1
PIN 21	RWL16		RB14			RAD11					RA005	RAD04	RAD03	RB2		
IN 2 BIT	BIT 16	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1
PIN 49	RIC	RIC	RIC	RIC	RIC	RIC	RIC	RIC	RIC	RIC	RIC	RIC	RIC	RIC	RIC	RBI
IN 0 BIT	BIT 16	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1
B BIT	BIT 16	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1
PIN 15												R22			R22	
OUT 0 BIT	BIT 16	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1
O BIT	BIT 16	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1
PIN 79												R24		R24		
IN 3 BIT	BIT 16	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1
OUT 2 BIT	BIT 16	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1
PIN 73	MOT16	MOT15	MOT14	MOT13	MOT12	MOT11	MOT10	MOT09	MOT08	MOT07	MOT06	MOT05	MOT04	MOT03	MOT02	MOT01
SCALER B	STAGE 16	STAGE 15	STAGE 14	STAGE 13	STAGE 12	STAGE 11	STAGE 10	STAGE 9	STAGE 8	STAGE 7	STAGE 6	STAGE 5	STAGE 4	STAGE 3	STAGE 2	STAGE 1
Z BIT	BIT 16	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1
PIN 87						RSTR1						RSTR1	RSTR1			
LP BIT	BIT 16	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1
OUT 1 BIT	BIT 16	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1
PIN 85																
IN/OUT 3	BIT 16	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1
WRITE LINE	WL16	WL15	WL14	WL13	WL12	WL11	WL10	WLO9	WLOB	WLO7	WLO6	WLO5	WLO4	WLO3	WLO2	WLO1

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Figure 4-113. Write Amplifier



Table 4-V. Program Interrupt Addresses

RAD11	RAD05	RAD04	RAD03	Address	RUPT Transfer Routine
1	0	0	0	2000	T3RUPT
1	0	0	1	2004	RPT2
1	0	1	0	2010	T4RUPT
1	0	1	1	2014	KEYRUPT
1	1	0	0	2020	UPRUPT
1	1	0	1	2024	DOWNRUPT

The quantity minus one is placed on the write lines by control pulse R1C, which is applied to write amplifiers 2 through 16. There is no connection to write amplifier 1. This action results in the quantity 1 111 111 111 111 110 (177776 octal) when R1C is generated.

Control pulse R22, generated during subinstruction DV1, causes address 0022 to be placed on the write lines. This address is entered into register S and results in a cycle-left operation of any data entered into the register G.

Control pulse R24 is generated during instructions RUPT (interrupt) and RSM (resume) and causes address 0024 to be placed on the write lines. During an interrupt program (RUPT), the address of the instruction to be executed next, which is stored in register Z, is transferred to location 0024 in memory. When the interrupt program is completed, the resume instruction (RSM) generates control pulse R24. Address 0024 is written into register S and the information entered into this location in memory during instruction RUPT is returned to the central processor.

A 16 bit word can be loaded into the AGC from the CTS through inputs MDT01 through MDT16.

Control pulse RSTRT produces the start address when instruction GO is generated by signal GOJAM. The start address is in fixed memory at location 5364, which is determined by RSTRT as follows:

Write Line	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0	0
				0			2			0			3			0

4-8.3.17 Parity Circuits Detailed Descriptions. The parity circuits consist of parity service and parity logic. This logic area functions in the AGC as follows:

- (1) It ensures that all words transferred from memory to the central processor are read out correctly.
- (2) It generates a parity bit for all words that are written into memory.
- (3) It stores the generated parity bit of a word while another word is checked for correct parity. This latter function occurs during an exchange instruction (XCH).

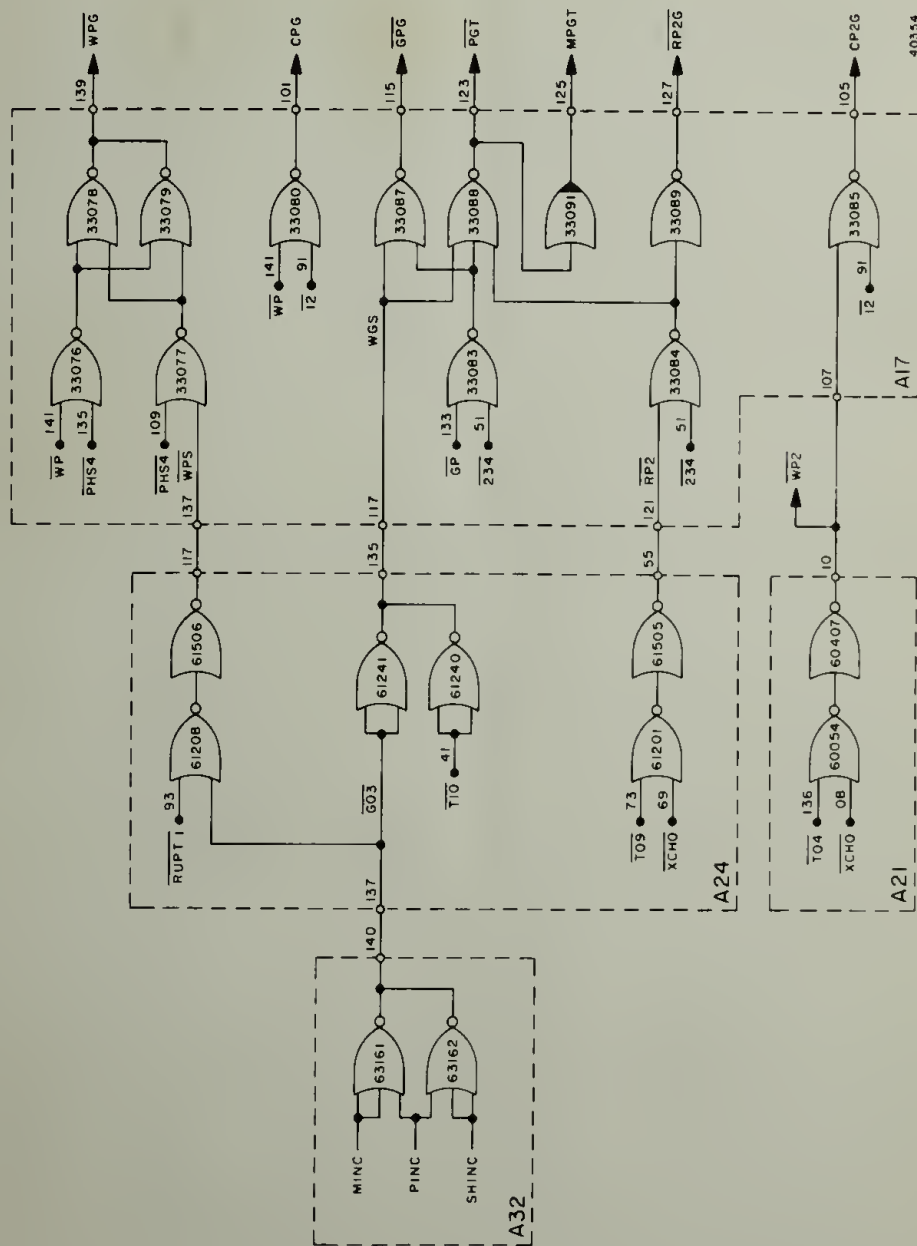
Parity check in the AGC is that of odd parity; that is, the total number of logic ONE's in the word including the parity bit is odd.

A word read out of memory is transferred to the parity logic from register G. Bits 1 through 16, excluding bit 15 (the parity bit which is never placed on the write line), are applied to the input section of the parity logic. This gating complex combines the 15 bit input from the write lines into a 5 bit word, which is stored in the five flip-flops (A through E). This 5 bit word is written into the flip-flops by write signal  $\overline{WPG}$ . If the incoming word has an even number of logic ONE's (excluding the parity bit), flip-flop outputs A through E will contain an even number of logic ONE's; if the incoming word has an odd number of logic ONE's, flip-flop outputs A through E will contain an odd number of logic ONE's.

Write signal  $\overline{WPG}$  is generated as shown in the parity service section, figure 4-114, by gating write control pulse  $\overline{WP}$  and timing signal  $\overline{PHS4}$ . This is similar to the method for generating write signals for the flip-flop registers except that signal  $\overline{PHS4}$  is used instead of signal  $\overline{234}$ . Signal  $\overline{PHS4}$  occurs during the last 0.25 microsecond of a 1 microsecond interval. The clear pulse,  $\overline{CPG}$ , is generated to clear flip-flops A through E prior to the write signal  $\overline{WPG}$ . This is identical to the method described for the flip-flop registers. Signal  $\overline{WPG}$  occurs coincidentally with the read signal for register G ( $\overline{RG}$ ). Thus, the data from register G is read out and placed on the write lines and coincidentally is written into flip-flops A through E. Write signal  $\overline{WPG}$  is also produced during an interrupt program ( $\overline{RUPT1}$ ) coincident with a  $\overline{PINC}$ ,  $\overline{MINC}$ , or  $\overline{SHINC}$  instruction. In this case, the content of a counter in erasable memory is read out and checked for correct parity by the parity logic.

The parity bit from bit position 15 of register G is applied to gate 33172 (figure 4-115) ( $\overline{PARBUS}$ ) and is written into flip-flop F by  $\overline{WPG}$ . If the parity bit is a logic ONE, flip-flop F is set when the write signal occurs ( $\overline{WPG} \cdot \overline{PARBUS}$ ). If the parity bit is a logic ZERO, flip-flop F remains reset. The set and reset outputs from the parity bit flip-flop are used to generate an output which is indicative of an even (EVNF) or odd (ODFBR) number of logic ONE's in the word (excluding parity).

Flip-flop outputs A through E are applied to a second series of gates which comprise the parity tree. The parity tree combines this 5 bit input into a 2 bit output and produces an output from gate 33057 which is indicative of the total number of logic ONE's in the word excluding the parity bit. Inputs A, B, and C are combined to



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Figure 4-114. Parity Service

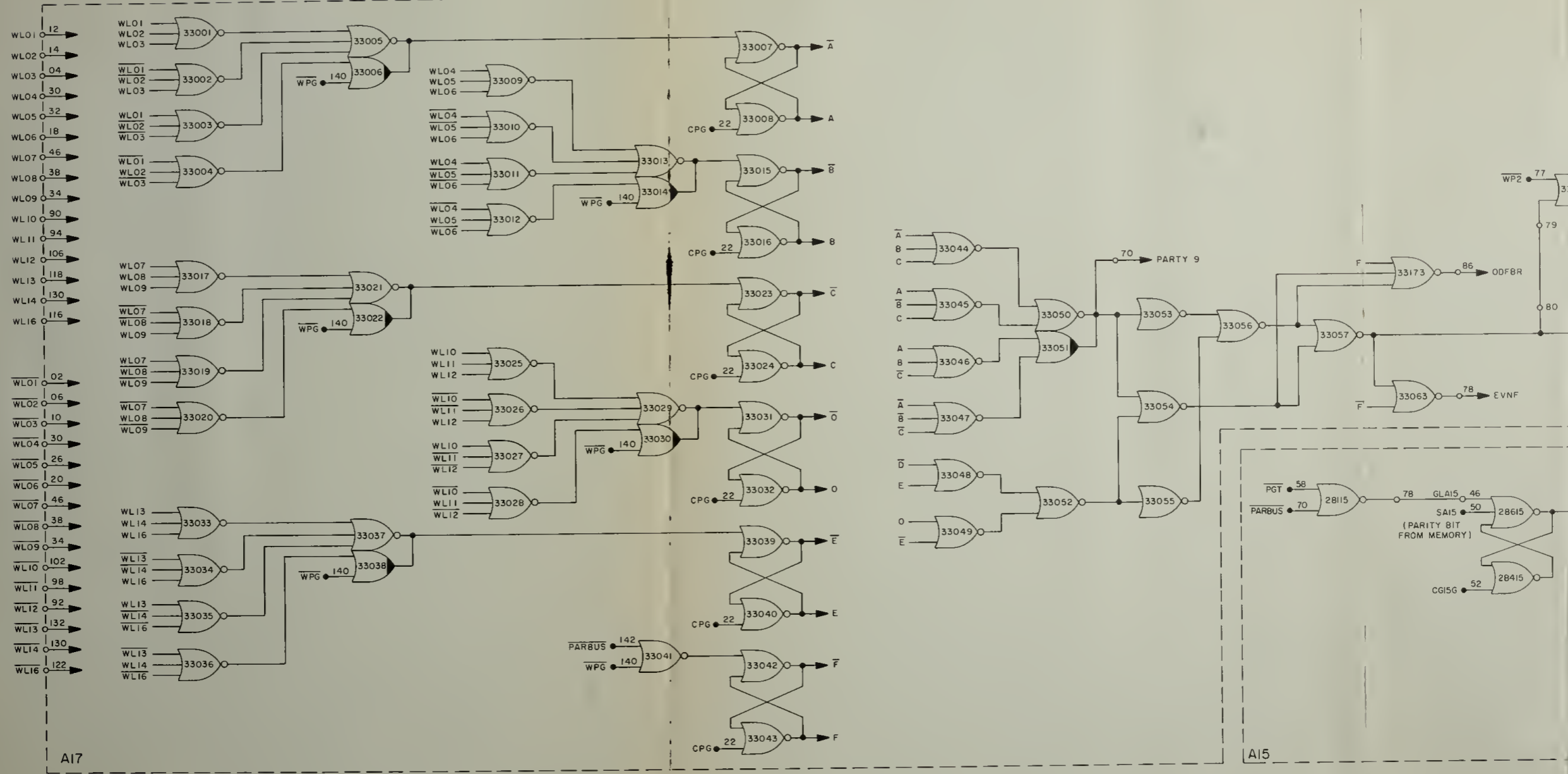
produce an output from gates 33050 and 33051 which is indicative of the number of logic ONE's in bits 1 through 9 of the word. A logic ONE output from gates 33050 and 33051 indicates an even number of logic ONE's in bits 1 through 9, a logic ZERO output indicates an odd number of logic ONE's in bits 1 through 9. In a similar manner, flip-flop outputs D and E are combined to produce an output from gate 33052 which is indicative of the number of logic ONE's in bits 10 through 16 (excluding 15, the parity bit). The parity tree output from gate 33057, as stated previously, is indicative of the total number of logic ONE's, excluding parity, in the word. This output is a logic ONE if the total number of logic ONE's is even, and a logic ZERO if the total number of logic ONE's is odd.

Gates 33173 and 33063 compare the output (F) of parity flip-flop with the output of the parity tree. If the total number of logic ONE's in the word is odd, signal ODFBR is a logic ONE, indicating this condition. If the total number of logic ONE's is even, signal EVNF is a logic ONE. Signal EVNF or ODFBR is a logic ONE if there is no parity error. Both of these signals are logic ZERO's if a parity error occurs. This condition sets the parity alarm flip-flop, generates a parity alarm from the alarm circuits, and causes signal GOJAM to be produced.

When a word is to be written into erasable memory, the parity logic generates a parity bit and writes this parity bit into position 15 of register G. This is accomplished by reading the word from the appropriate register (and placing it on the write lines) into the parity logic. The word is checked for an even or odd logic ONE condition in a manner identical to that described previously, and a parity alarm occurs in case of incorrect parity. The parity tree output (gate 33057) is applied to gate 33062. This output is the correct parity bit of the word. Signal  $\overline{\text{GPG}}$  (generate parity) is generated by the parity service gates and causes the generated parity bit to be placed on the parity bus (PARBUS). The parity bit is written into bit position 15 of register G by signal  $\overline{\text{PGT}}$ , which is generated coincidentally with  $\overline{\text{GPG}}$ . From bit position 15 of register G the parity bit is written into memory through the gate with output labeled GEM15.

Signals  $\overline{\text{GPG}}$  and  $\overline{\text{PGT}}$  are generated normally by control pulse  $\overline{\text{GP}}$  from the sequence generator coincidentally with timing pulse 234. During counter increment/decrement instruction PINC, MINC, or SHINC, and signals  $\overline{\text{GPG}}$  and  $\overline{\text{PGT}}$  are produced to write into erasable memory the generated parity bit of the appropriate counter that is being updated.

During an exchange subinstruction (XCH0), FF33059-33060 stores the parity bit of one word while the parity logic checks another word for correct parity. This flip-flop can be considered as a single bit position register (P2). It is used only during the execution of subinstruction XCH0. This is indicated by the inputs to the gates of the parity service section (figure 4-106) which generate the write, clear, and read signals for this flip-flop. Write, clear, and read signals  $\overline{\text{WP2}}$ ,  $\overline{\text{CP2G}}$ , and  $\overline{\text{RP2G}}$  are generated as a function of control pulse  $\overline{\text{XCH0}}$  from the sequence generator. The clear and write signals are generated during time 4 of this subinstruction ( $\overline{\text{T04}} \cdot \overline{\text{XCH0}}$ ). At time 9 the read signal  $\overline{\text{RP2G}}$  causes the parity bit to be placed on the parity bus and subsequently to be written into memory through bit position 15 of register G. The manipulation of data is more apparent if all the control pulses generated during



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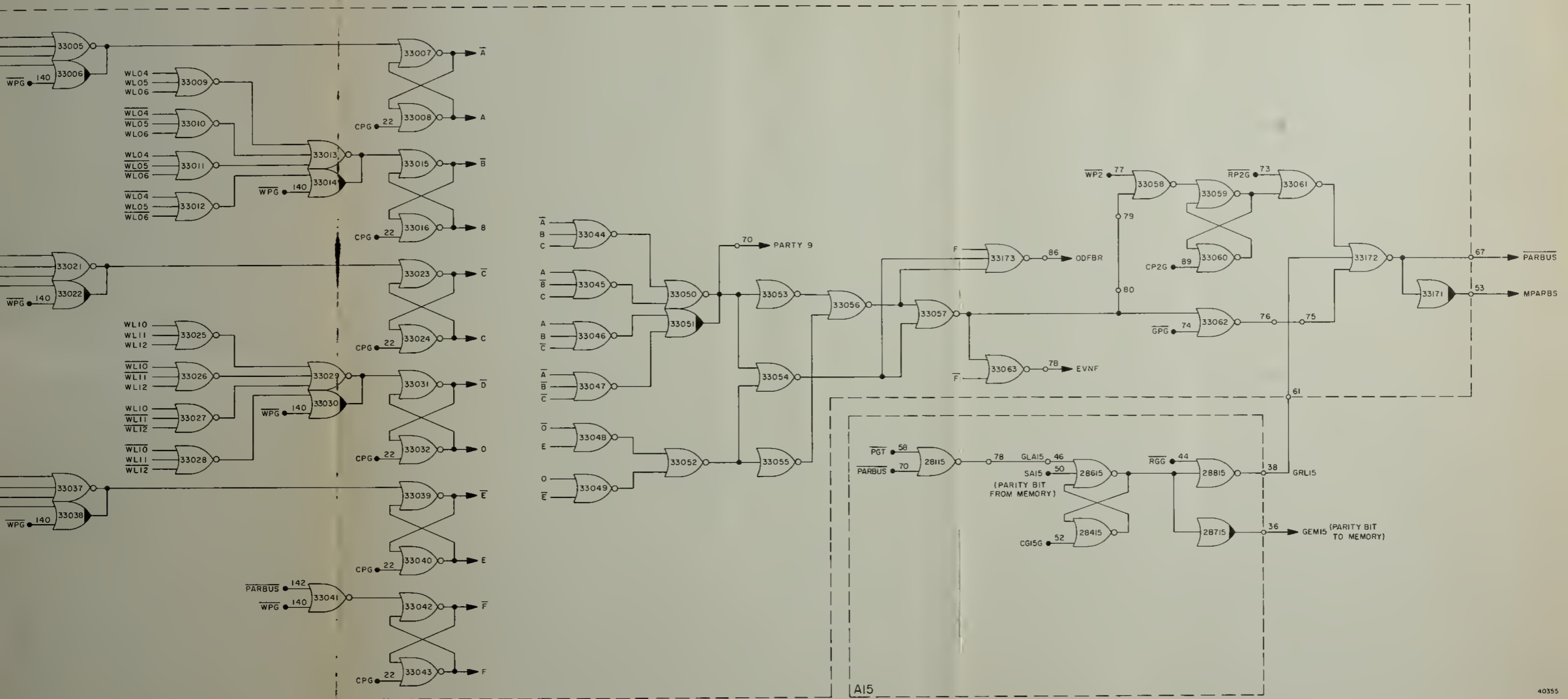
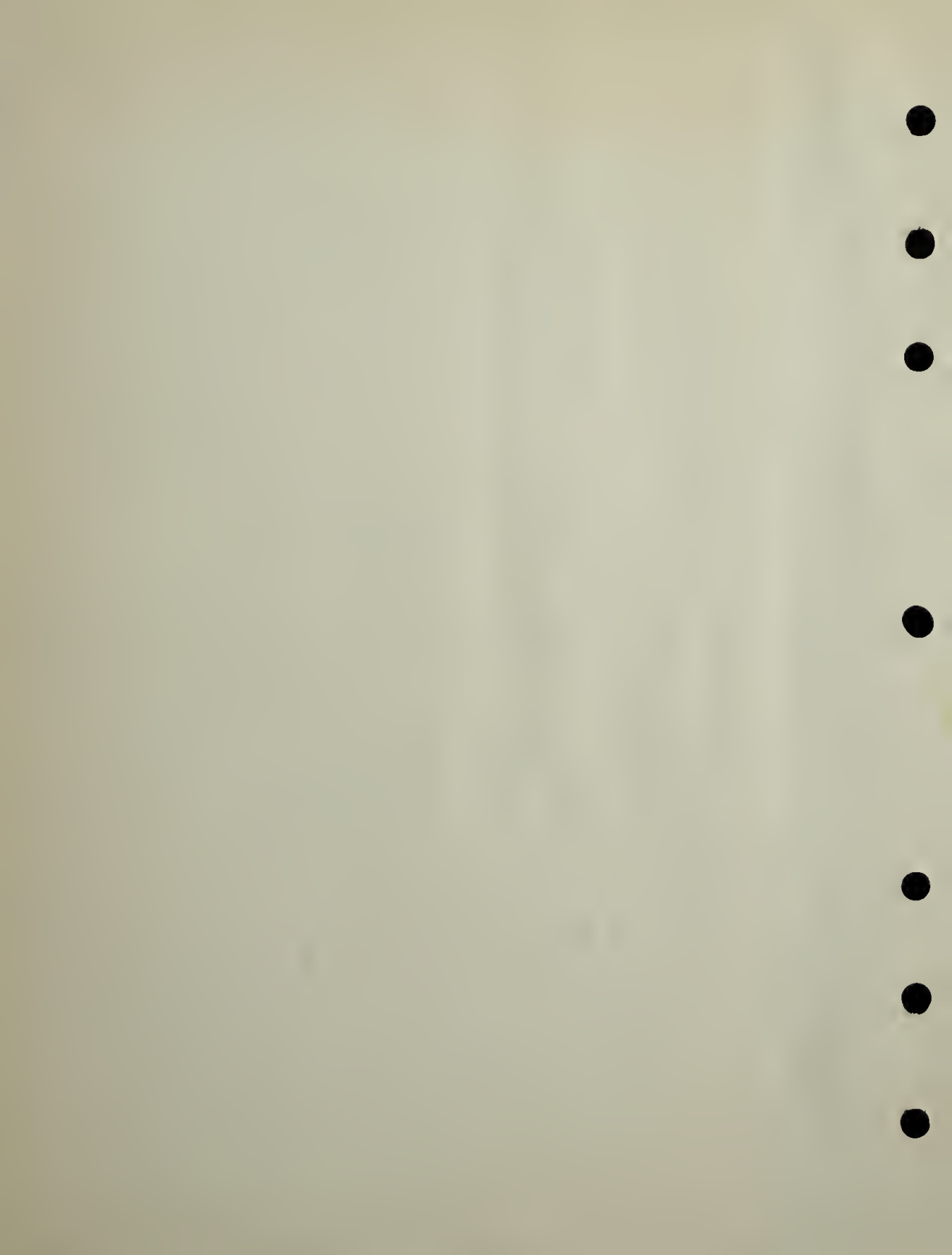


Figure 4-115. Parity Logic





subinstruction XCH0 are examined. A step-by-step discussion of the execution of instruction XCH0 and all the control pulses generated during each action is contained in paragraph 4-8.8, Machine Instructions.

4-8.4 INPUT-OUTPUT. The input-output section consists of the input registers, output registers, the downlink converter, alarm control circuit, rate control circuits, and interface circuits. The input-output section provides the means by which information is transferred between the AGC and the other spacecraft systems.

This functional area provides drive pulses, rate signals, and discrete bit outputs to the spacecraft systems; display and alarm information to the display and keyboards (DSKY's); and serial data to the spacecraft (downlink) telemetry system. Inputs to the AGC, such as keycodes from the display and keyboards, discrete bits from the spacecraft, and telemetry timing pulses, are provided through the input-output section.

The interface circuits are discussed as an integral part of the input-output section. However, since interfacing is not restricted to this functional area alone, but to the entire AGC, the interface circuits do not appear on the input-output functional diagrams. A discussion of the interface circuits follows the discussion of the input-output section.

4-8.4.1 Input-Output Registers Functional Description. The input-output registers (figure 4-116) consists of registers IN 0, IN 2, IN 3, OUT 0, OUT 1, and OUT 3 and associated service circuits. The input registers receive inputs directly from AGC circuits and from subsystems external to the AGC. These inputs do not require write control pulses to be written into the input registers; they are entered directly into the bit positions of the registers. The input and output registers provide inputs to the write amplifiers in the central processor. The central processor provides inputs from the write amplifiers to the output registers. The quantities present on the write lines are written into the output registers with write control pulses.

The register service circuits produce the clear and read signals for the input registers, and the write, clear, and read signals for the output registers. The clear signals are generated as a function of memory addresses and the clear control signal from the central processor. Register IN 0 clear signal is produced also when signal MKTRP or TRP4 is received from priority control. Trap circuits in the interrupt priority control produce the MKTRP signal when the MARK pushbutton is depressed, and the TRP 4 signal when a DSKY key is depressed. The read signals are generated as a function of memory addresses and the read control signal from the central processor. The output register write signals are a function of memory addresses and the write control signal from the central processor. The output register service circuits also generate clear signals when signal GOJAM is received from the timer.

4-8.4.2 Input Registers Detailed Description. The input registers (IN 0, IN 2 and IN 3) are flip-flop registers similar to the flip-flop registers in the central processor. Each register consists of 16 bit positions. The effective capacity of each register is 15 bits since the same data is entered simultaneously into bit positions 15 and 16. The bit outputs are placed on the write lines and are entered into the central processor.

The input registers are termed addressable registers. Each register has an associated address, which is generated under program control, and allows clear and read control pulses for each register to be generated. For example, address 0004 generated by the program enables the clear and read control signals for register IN 0. Likewise, address 0006 enables the control signals for register IN 2 and address 0007 enables the control signals for register IN 3.

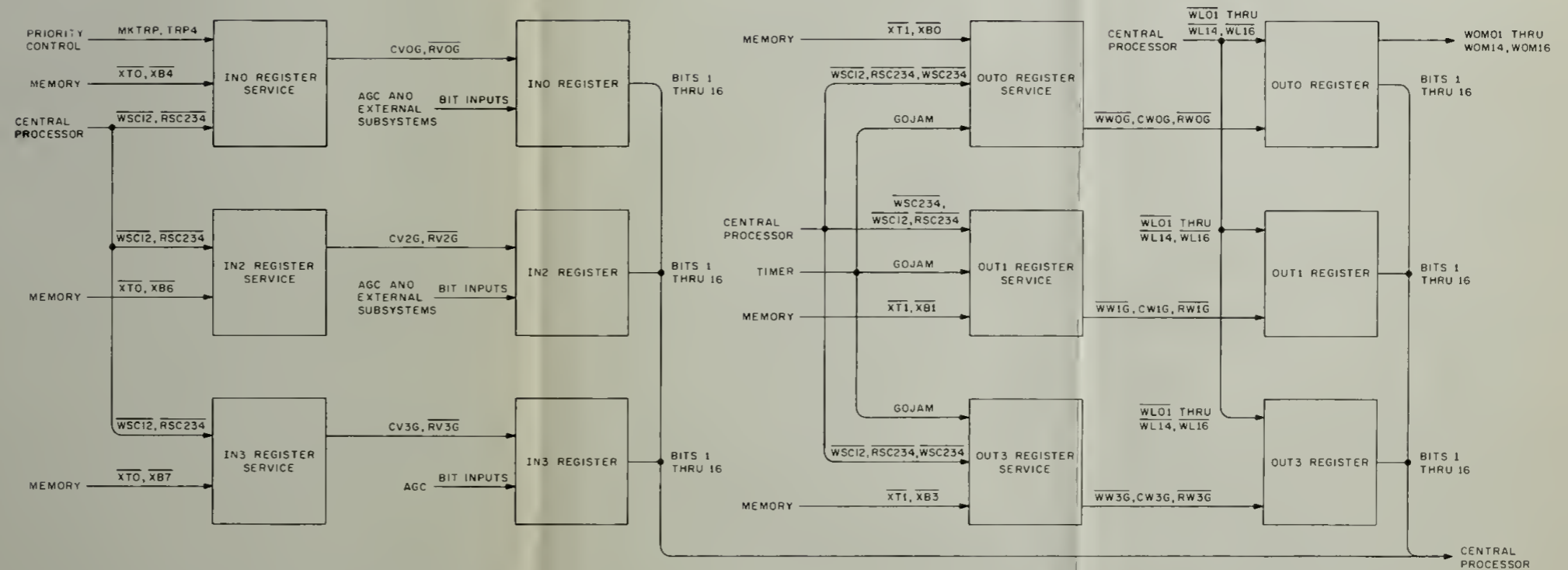
There is no write service for the input registers. The input data from the interface circuits is applied directly to each flip-flop. The registers are interrogated by program and data is read out and placed on the write lines in the central processor.

4-8.4.2.1 Register IN 0. Register IN 0 (figure 4-117) accepts inputs from the DSKY's, priority control, the spacecraft and the G and N indicator control panel. These inputs appear in table 4-VI. The clear and read signals for register IN 0 are generated as a function of address 0004 (indicated by inputs  $\overline{XT0}$  and  $\overline{XB4}$  to the service gates), write control signal  $\overline{WSC12}$  for the clear pulse, and read control signal  $\overline{RSC234}$  for the read signal. These two control signals are generated in the central processor. Clear signal CVOG is also generated as a function of inputs TRP4 and MKTRP. These inputs are described in the following paragraphs.

The keycode (KEY 1-KEY 5) from either DSKY is entered into bit positions 1 through 5 of register IN 0. It is simultaneously entered into the Interrupt Priority Control circuits (KEYRUPT) and causes signal TRP4 to be generated. This signal, applied to the clear service gates (37770), generates CVOG to clear the entire register prior to the entry of the keycode. A similar condition results when signal MARK from the G & N indicator control panel is entered into bit positions 15 and 16. Signal MARK is simultaneously entered into the Interrupt Priority Control circuits and causes signal MKTRP to be generated, which in turn causes CVOG to clear the entire register prior to the entry of the MARK signal.

The block uplink signal (BLKUPL) entered into bit position 6 of IN 0 originates in the AGC main panel DSKY. This is a switch-controlled input initiated by the astronaut to prevent uplink information from entering the AGC. A related signal input is entered into bit position 7 of IN 0. The inhibit upsync signal (NHSYNC), generated in Priority Control, also prevents uplink bits from entering the AGC and indicates that the uplink bits are entered into the AGC faster than a predetermined rate.

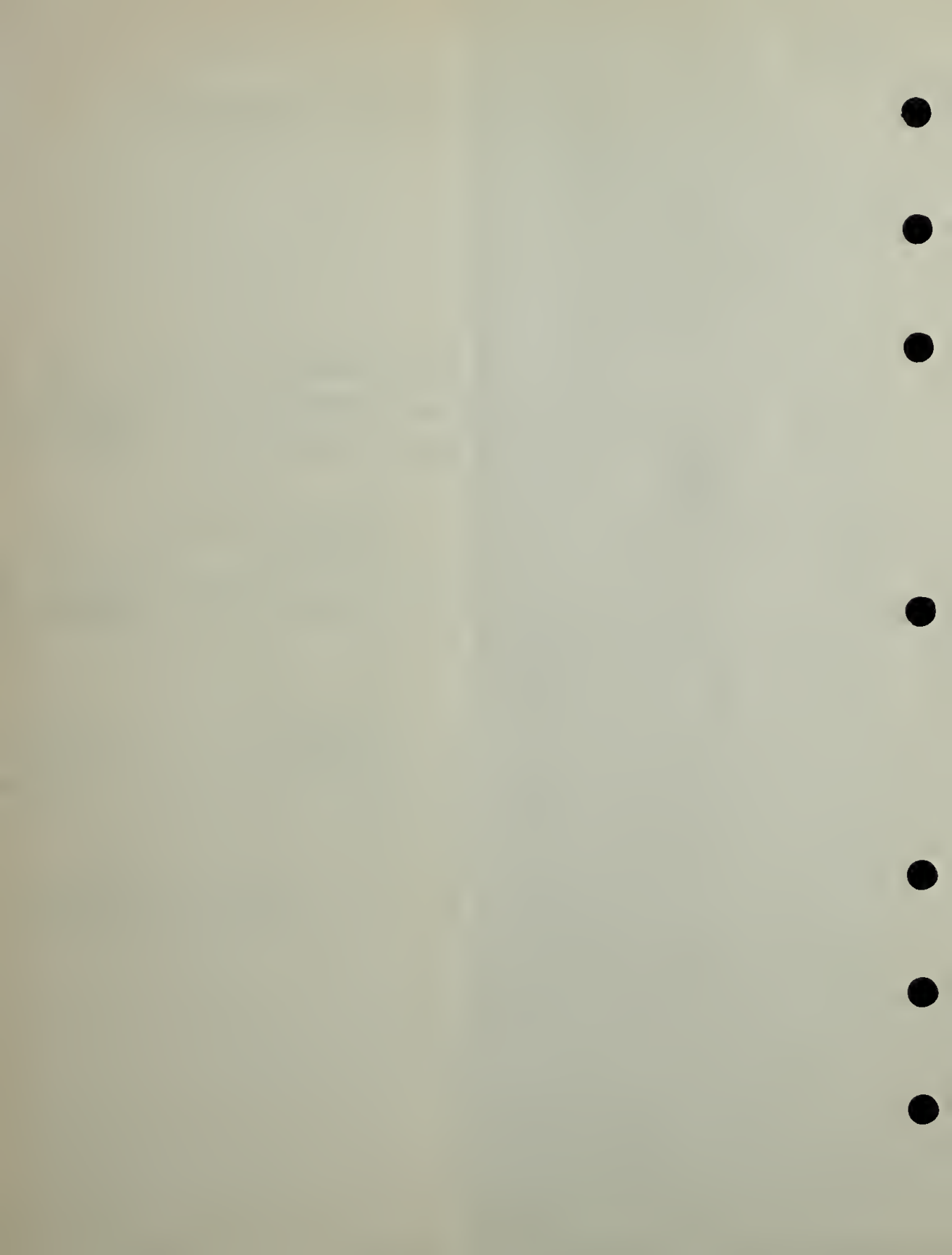
The data entered into bit positions 11 through 13 of register IN 0 (indicated in table 4-VI) originates in the spacecraft. These inputs are three of a number of inputs termed the unmanned flight signals. These inputs are used to energize relays in the AGC main panel DSKY. Outputs from the relays provide contact closures to the spacecraft.

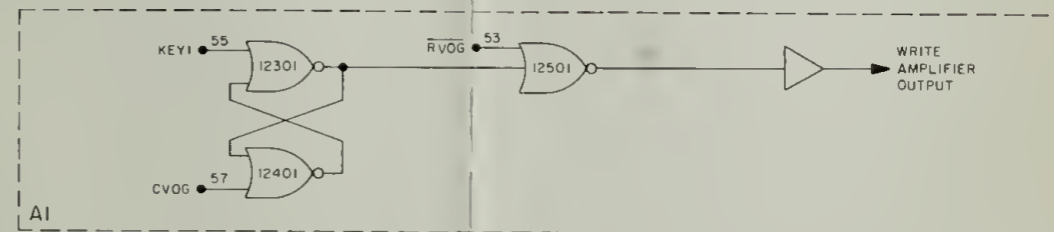
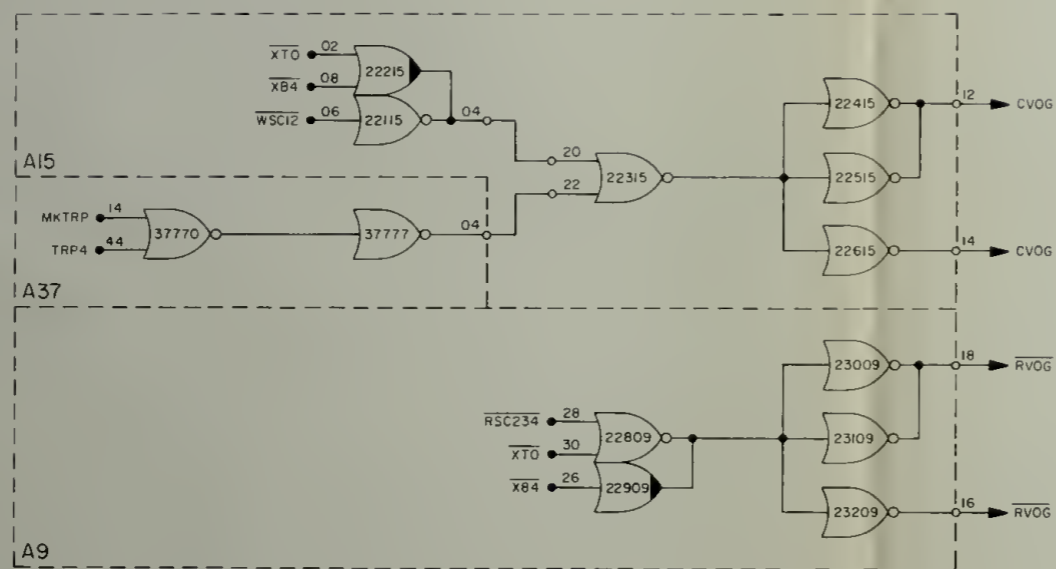


- NOTES
- 1 OUT2 REGISTER IS PART OF RATE CIRCUITS
  - 2 OUT4 REGISTER IS PART OF DOWNLINK CONVERTER
  - 3 IN1 REGISTER, WITH CONNECTIONS, IS SCALAR B

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Figure 4-116. Input-Output Registers, Functional Diagram





MOOULE	PIN NO	INPUT	CLEAR	READ
A 1	55	KEY 1	57	$\overline{RVOG}$
A 2		KEY 2	CVOG	$\overline{RVOG}$
A 3		KEY 3	CVOG	$\overline{RVOG}$
A 4		KEY 4	CVOG	$\overline{RVOG}$
A 5		KEY 5	CVOG	$\overline{RVOG}$
A 6		BLKUPL	CVOG	$\overline{RVOG}$
A 7		NHSYNC	CVOG	$\overline{RVOG}$
A 8		SPARE	CVOG	$\overline{RVOG}$
A 9		SPARE	CVOG	$\overline{RVOG}$
A10		SPARE	CVOG	$\overline{RVOG}$
A11		G/N ATT CONTROL	CVOG	$\overline{RVOG}$
A12		G/N DV MODE	CVOG	$\overline{RVOG}$
A13		G/N ENTRY MODE	CVOG	$\overline{RVOG}$
A14		SPARE	CVOG	$\overline{RVOG}$
A15		MARK	CVOG	$\overline{RVOG}$
A16		MARK	CVOG	$\overline{RVOG}$

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Figure 4-117. Register IN 0



Table 4-VI. Inputs to IN Registers

Register	Bit Position	Description	
IN 0	1 through 5	Keycode entered from the DSKY. Causes KEYRUPT	
	6	Block uplink. Prevents uplink data from being entered into the AGC (from main DSKY)	
	7	Inhibit uplink sync (NHSYNC from priority control)	
	8 through 10	Spare	
	11	G/N Attitude Control	
	12	G/N Δ V Mode	
	13	G/N Entry Mode	
	14	Spare	
	15, 16	Mark from G & N control panel. (Order to read angular data. Causes KEYRUPT)	
	IN 2	1 through 4	Timer outputs for finer time quantization.
		5	Lift OFF
6		Guidance Release	
7		Ullage	
8		SIVB Separate	
9		SM/CM Separate	
10		CDU fail	
11		PIPA fail	
12		IMU fail	
13		SCS Δ V	
14		G/N Monitor	
15, 16		Parity alarm	
IN 3		1	Zero encoder
		2	Coarse align
	3	Lock CDU	
	4	Fine align	
	5	Attitude control mode (switch input)	
	6	Transfer control to computer (switch input)	
	7	Roll re-entry	
	8	Spare	
	9	Spare	
	10	Optics mode S3. Star tracker on	
	11	Star present	
	12	Zero optics	
	13	Optics mode S1. Command moudle sextant on	
	14	Optics mode S2. Computer control	
	15, 16	Or of C1-C33 (DSKY Relays)	



4-8.4.2.2 Register IN 2. Register IN 2 (figure 4-118) accepts inputs from the timer, spacecraft, G & N system, and the central processor. The clear and read signals are generated in a manner identical to that described for register IN 0, except that memory address 0006 (indicated by  $\overline{XT0}$  and  $\overline{XB6}$  to the service gates) is used as dictated by the program.

Inputs  $\overline{FS07}$  through  $\overline{FS10}$  to bit positions 1 through 4 from the timer are used for time quantization. The rates of these inputs are respectively 800 pps, 400 pps, 200 pps, and 100 pps.

The inputs to bit positions 5 through 9 inclusive, and 13 and 14 (indicated in table 4-VI) are control mode and status signals from the spacecraft. The CDU, PIPA, and IMU fail signal inputs to bit positions 10, 11, and 12 are used to energize relays in the DSKY's and provide fail indications of these elements to the G and N system.

A parity alarm, indicating incorrect parity of a word read-out of memory into the central processor, is entered into bit positions 15 and 16.

4-8.4.2.3 Register IN 3. Register IN 3 (figure 4-119) accepts inputs from the ISS, the G and N indicator control panel, and the two DSKY's. The clear and read signals are generated in a manner identical to that described for register IN 0, except that memory address 0007 (indicated by  $\overline{XT0}$  and  $\overline{XB7}$  to the service gates) is used as dictated by the program.

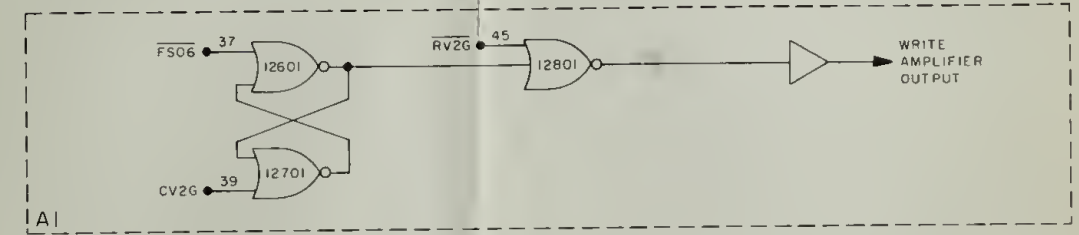
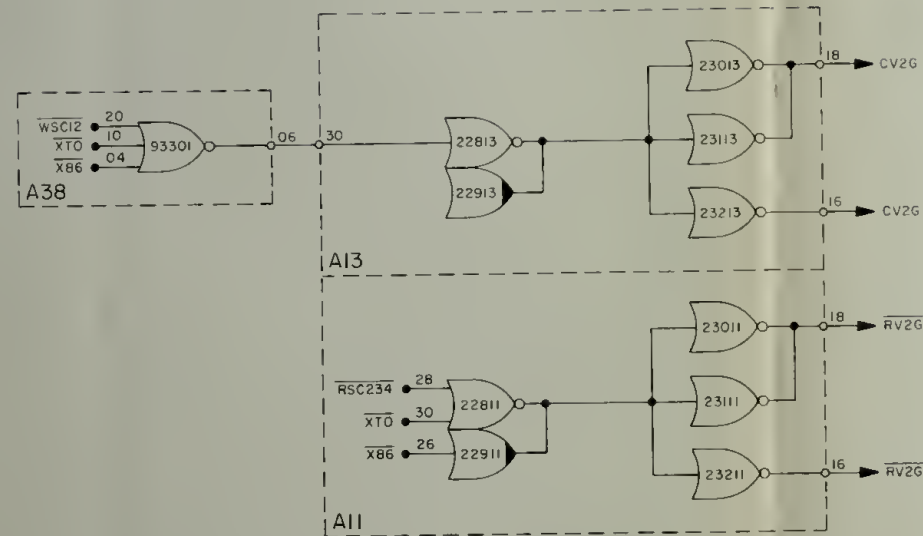
The inputs to bit positions 1 through 5, and 7, (see table 4-VI) are IMU mode signals indicating one of the six modes listed and are also used to energize relays in the AGC navigation panel DSKY which confirms the completion of these IMU mode requests. Bit 6 is the input from the TRANSFER switch which allows AGC control of the IMU.

The inputs to bit positions 10 through 14 are switch inputs from the G and N indicator control panel and indicate the conditions listed in table 4-VI. Inputs OPTMS3 (Star Tracker On) to bit position 10 and ZEROPT to bit position 12 are also routed to the AGC navigation panel DSKY to provide contact closure indications of these inputs to the OSS.

4-8.4.3 Output Registers Detailed Description. The output registers (OUT 0 through OUT 4 inclusive) are flip-flop registers similar to the flip-flop registers in the central processor. Each register consists of 16 bit positions; however, the effective capacity is 15 bits since the information read-out of bit positions 15 and 16 of each register is the same. The output registers, similar to the input registers, are also addressable. The associated addresses generated by the program are as follows:

OUT 0-0010  
OUT 1-0011  
OUT 2-0012  
OUT 3-0013  
OUT 4-0014

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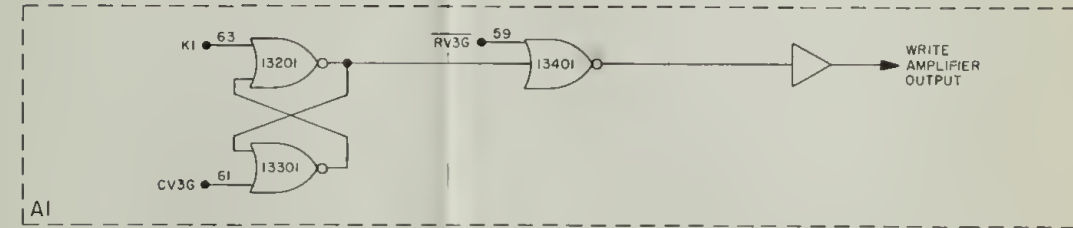
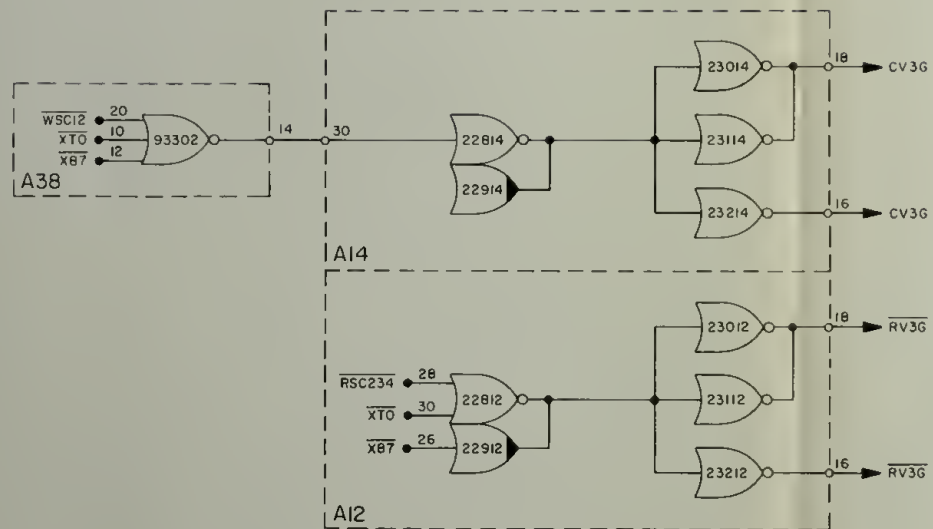


MODULE	PIN NO	INPUT	CLEAR	READ
		37	39	45
A 1		FS07	CV2G	RV2G
A 2		FS08	CV2G	RV2G
A 3		FS09	CV2G	RV2G
A 4		FS10	CV2G	RV2G
A 5		LIFT OFF	CV2G	RV2G
A 6		GUID REL	CV2G	RV2G
A 7		ULLAGE	CV2G	RV2G
A 8		S1VB SEP	CV2G	RV2G
A 9		SM/CM SEP	CV2G	RV2G
A10		CDU FAIL	CV2G	RV2G
A11		PIPA FAIL	CV2G	RV2G
A12		IMU FAIL	CV2G	RV2G
A13		SCS ΔV	CV2G	RV2G
A14		G/N MONITOR	CV2G	RV2G
A15		PARITY ALARM	CV2G	RV2G
A16		PARITY ALARM	CV2G	RV2G

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Figure 4-118. Register IN 2

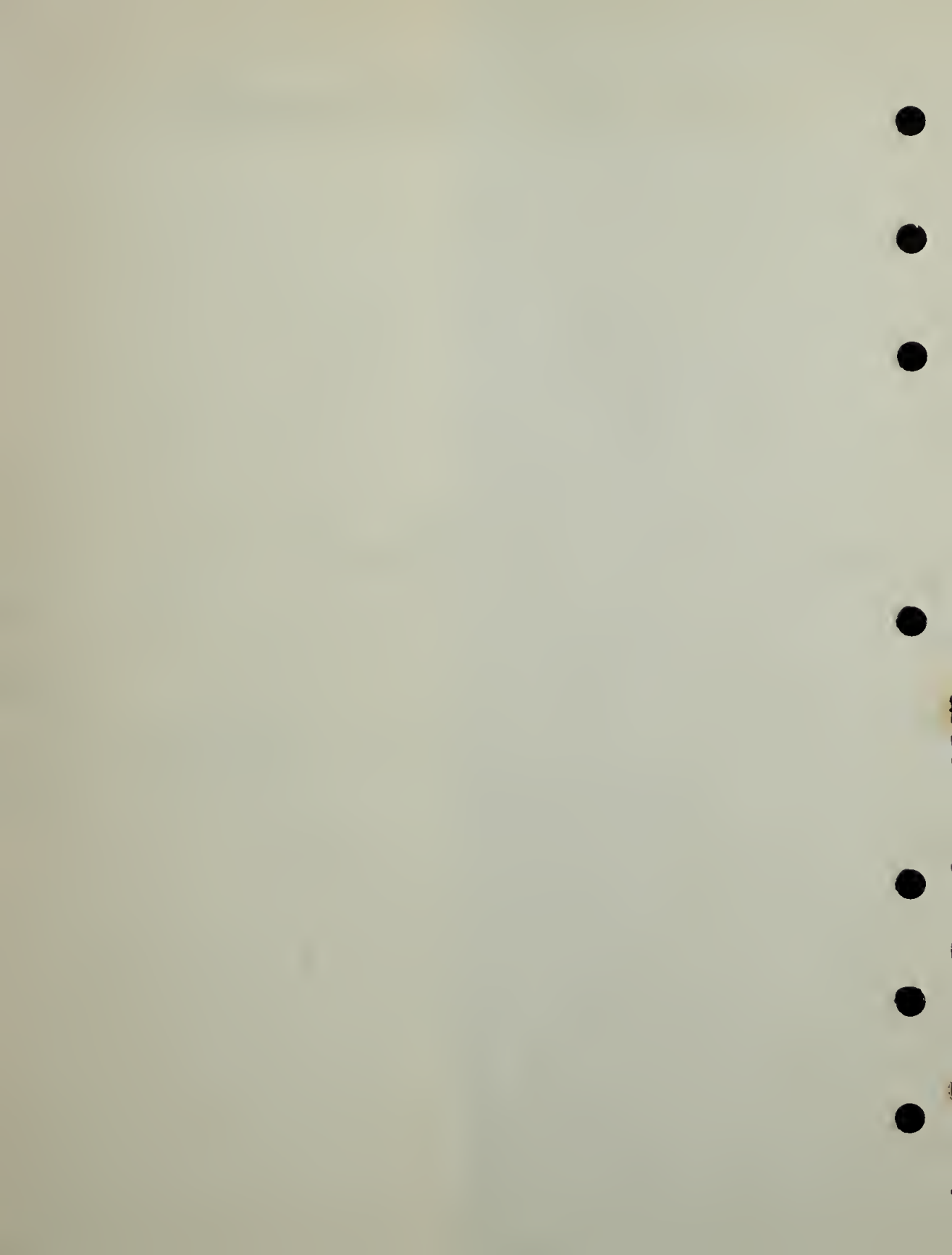




MODULE	PIN NO	INPUT	CLEAR	READ
		63	61	59
A1		K1	CV3G	$\overline{RV3G}$
A2		K2	CV3G	$\overline{RV3G}$
A3		K3	CV3G	$\overline{RV3G}$
A4		K4	CV3G	$\overline{RV3G}$
A5		K12	CV3G	$\overline{RV3G}$
A6		TRNSW	CV3G	$\overline{RV3G}$
A7		K5	CV3G	$\overline{RV3G}$
A8		SPARE	CV3G	$\overline{RV3G}$
A9		SPARE	CV3G	$\overline{RV3G}$
A10		OPTMS3	CV3G	$\overline{RV3G}$
A11		STAR PRESENT	CV3G	$\overline{RV3G}$
A12		ZEROPT	CV3G	$\overline{RV3G}$
A13		SEXT ON	CV3G	$\overline{RV3G}$
A14		OPTMS2	CV3G	$\overline{RV3G}$
A15		C1-C33	CV3G	$\overline{RV3G}$
A16		C1-C33	CV3G	$\overline{RV3G}$

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Figure 4-119. Register DN 3



These addresses enable the clear, write, and read service gates for the output registers in conjunction with control signals  $\overline{WSC}$  and  $\overline{RSC}$  from the central processor. Data is written into the output registers from the write lines in the central processor. This data is read out and placed on the write lines by associated read signals with the exception of register OUT 4. This register contains downlink information. The outputs are strobed by the output of a counter. Of the five output registers, only four are used (see table 4-VII). Connections are made to register OUT 3, but no data is applied to this register. The following discussions outline operation of registers OUT 0 and OUT 1 under separate headings. Register OUT 2 is discussed as part of the rate control circuits, and register OUT 4 as part of the downlink converter.

4-8.4.3.1 Register OUT 0. Register OUT 0 (figure 4-120) supplies the relay bit (RLYBIT) and relay word (RLYWD) outputs to the DSKY's. The data is furnished by the program and written into the register from the write lines in the central processor. Clear and write signals are generated as a function of address 0010 (indicated by  $\overline{XT1}$  and  $\overline{XB0}$  to the service gates) and write control pulse  $\overline{WSC12}$ . (The clear signal for register OUT 0 and all output registers except OUT 4 is also generated by signal  $\overline{GOJAM}$ .) The read signal is generated as a function of address and read control signal  $\overline{RSC234}$ . The data in bit position 16 is wired to the read gate of bit position 15. When the read signal is generated, the same data appears on write lines 15 and 16. These outputs are labeled WOMO1 through WOM14 and WOM16.

4-8.4.3.2 Register OUT 1. Register OUT 1 (figure 4-121) supplies programmed controlled alarms to the DSKY's, a reset signal to Interrupt Priority Control, an identification word and block pulse to the downlink converter, and a control bit for generating engine on pulses to the spacecraft. The programmed controlled alarms are supplied to the DSKY's from bit positions 1 through 5 of register OUT 1. These alarms are indicated in table 4-VII. The RUPT trap reset signal from bit position 7 is applied to Interrupt Priority Control as  $\overline{WITD07}$  to clear this circuit of an interrupt condition. The ID word from bit position 9 and the block end pulse from bit position 10 are described in table 4-VII. The output from bit position 13 (ENON) is applied to the continuous pulse control logic, which supplies a train of pulses to the spacecraft.

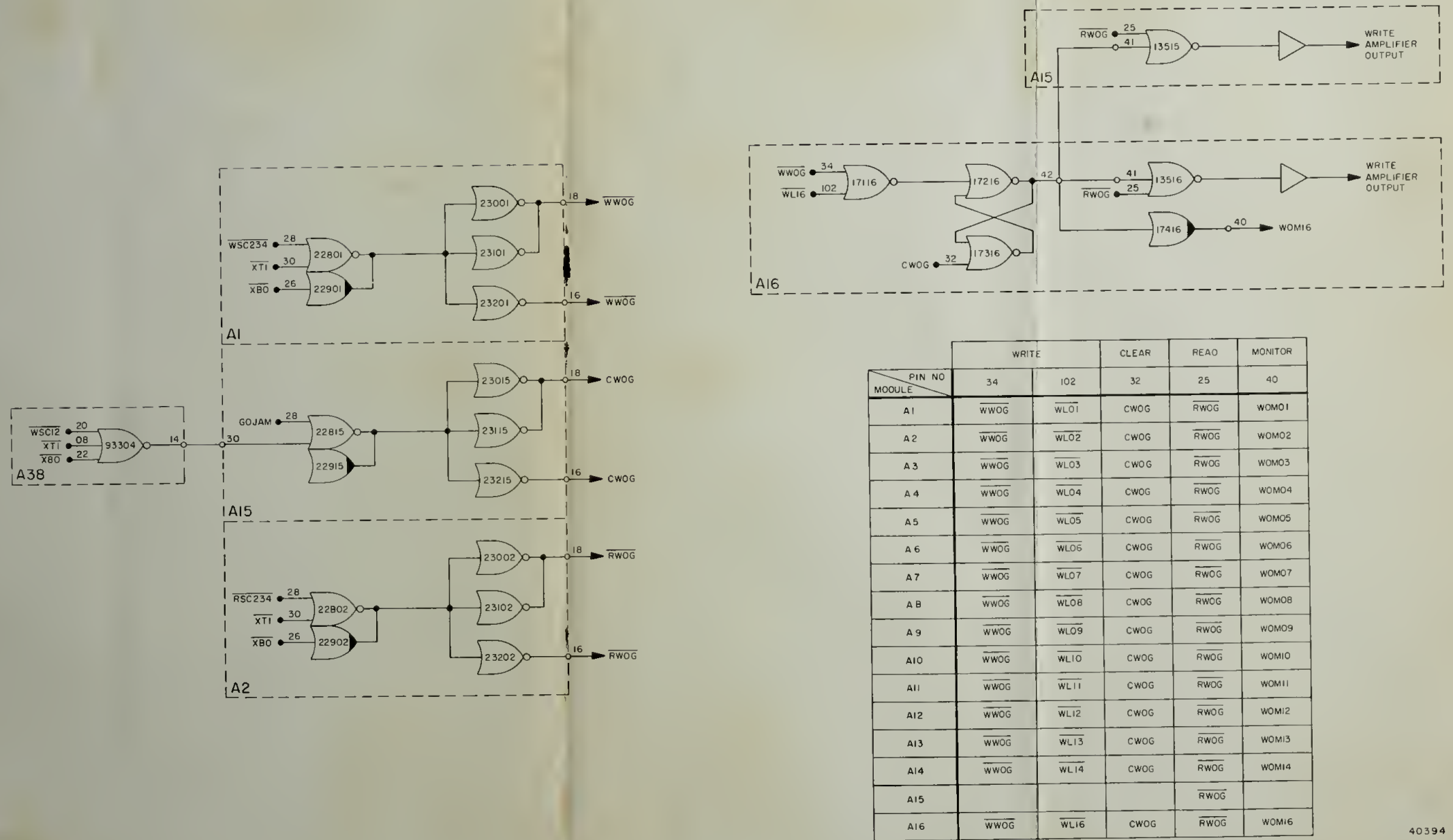
The clear signal is generated as a function of address 0011 (indicated by  $\overline{XT1}$  and  $\overline{SB1}$  to the service gates) and write control signal  $\overline{WSC12}$  and the write signal is generated by the address and write control signal  $\overline{WSC234}$ . The read signal is generated as a function of the address and read control signal  $\overline{RSC234}$ .

4-8.4.3.3 Register OUT 3. Register OUT 3 (figure 4-122) is presently not used. Connections are made to this register; however, no data is written in.

4-8.4.4 Downlink Converter Functional Description. The downlink converter (figure 4-123) consists of the bit sync converter, parallel-to-serial converter, and register OUT 4. The downlink converter converts parallel data words in register OUT 4 to serial words for the spacecraft telemetry system. The spacecraft telemetry system synchronizes the downlink converter by supplying start, bit sync, and end pulses.

Table 4-VII. OUT Registers Bit Outputs to Interface

Register	Bit Position	Description
OUT 0	1 through 11 12 through 16	Relay bits to the DSKY's Relay word to the DSKY's
OUT 1	1 2 3 4 5 6 7 8 9  10  11 12 13 14 15, 16	Program alarm (to displays) Computer activity (to displays) Key release (to displays) Telemetry alarm (to displays) Program check failure alarm (to displays) Spare RUPT trap reset (RUPT2) Spare ID word. For downlink data identification. A ONE in this bit position causes ONE's in the last 8 bits of the 40-bit telemetry word Block end pulse. Blocks downlink data transmission Spare Spare Engine-on Spare Spare
OUT 2	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15, 16	RADAR C RADAR B                   OUTCR3 RADAR A THRUST OPT Y OPT X                   OUTCR2 + (increment) - (increment) Z (middle gimbal) Y (inner gimbal) X (outer gimbal) Gyro CDU + (increment) - (decrement)
OUT 3	1 through 16	Not used
OUT 4	1 through 16	Downlink telemetry



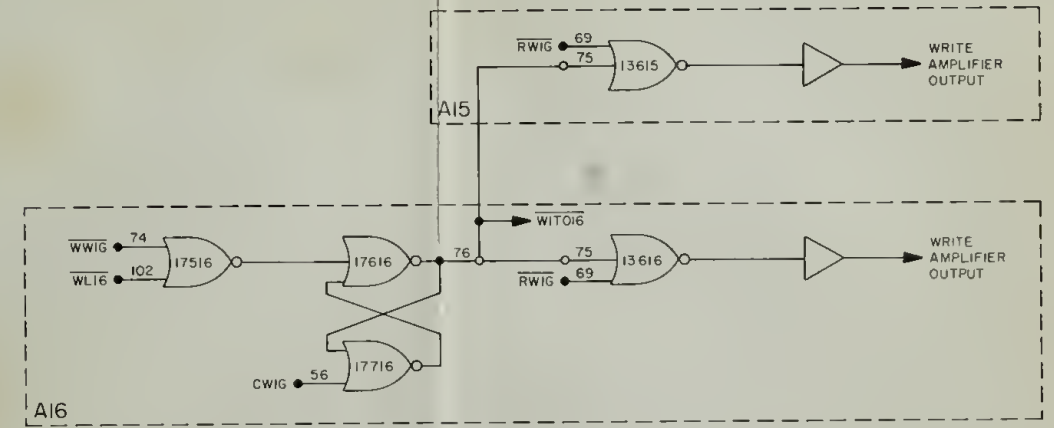
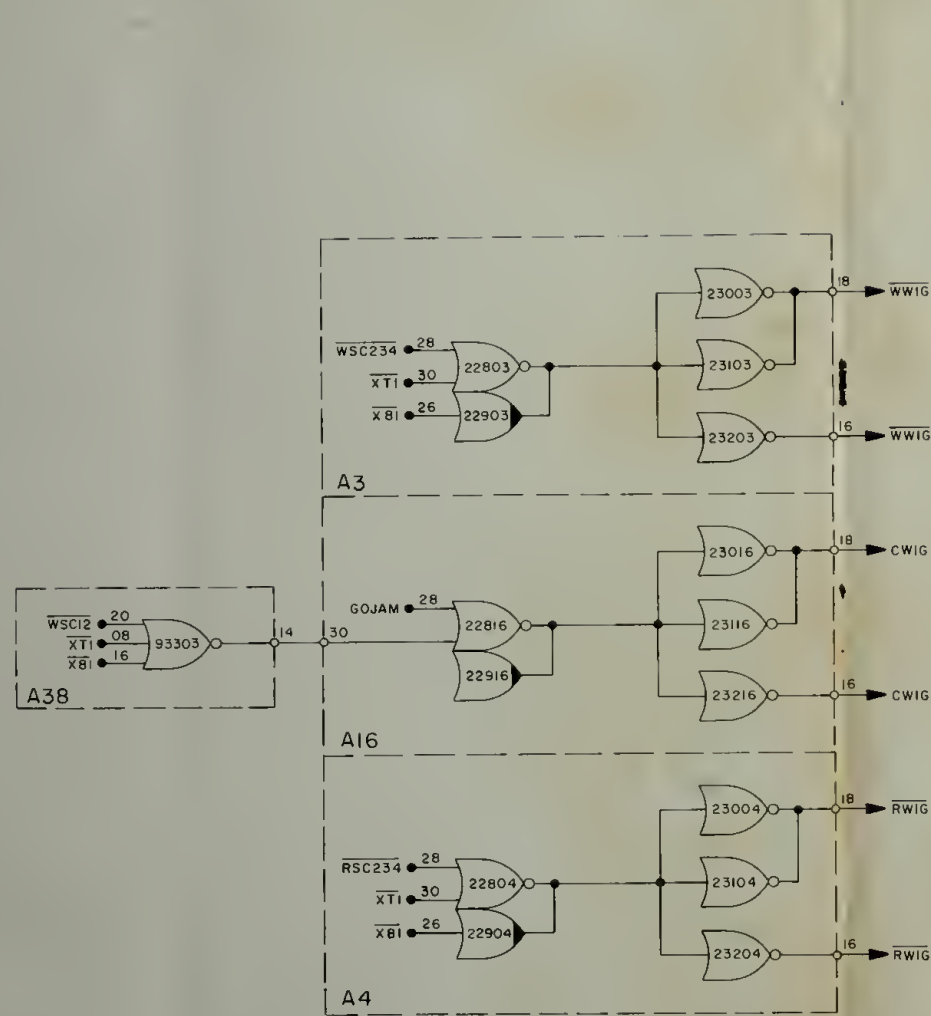
MODULE	PIN NO	WRITE		CLEAR	READ	MONITOR
		34	102	32	25	40
A 1		WWOG	WL01	CWOG	RWOG	WOM01
A 2		WWOG	WL02	CWOG	RWOG	WOM02
A 3		WWOG	WL03	CWOG	RWOG	WOM03
A 4		WWOG	WL04	CWOG	RWOG	WOM04
A 5		WWOG	WL05	CWOG	RWOG	WOM05
A 6		WWOG	WL06	CWOG	RWOG	WOM06
A 7		WWOG	WL07	CWOG	RWOG	WOM07
A 8		WWOG	WL08	CWOG	RWOG	WOM08
A 9		WWOG	WL09	CWOG	RWOG	WOM09
A 10		WWOG	WL10	CWOG	RWOG	WOM10
A 11		WWOG	WL11	CWOG	RWOG	WOM11
A 12		WWOG	WL12	CWOG	RWOG	WOM12
A 13		WWOG	WL13	CWOG	RWOG	WOM13
A 14		WWOG	WL14	CWOG	RWOG	WOM14
A 15					RWOG	
A 16		WWOG	WL16	CWOG	RWOG	WOM16

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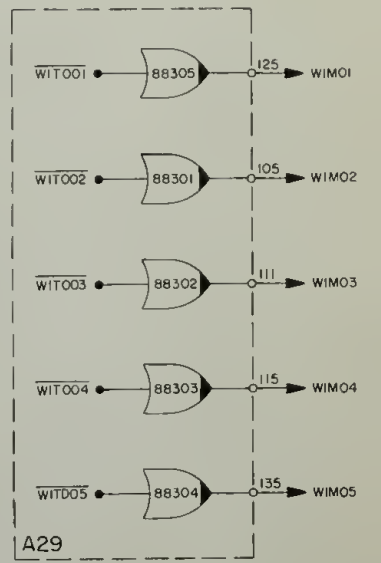
Figure 4-120. Register OUT 0







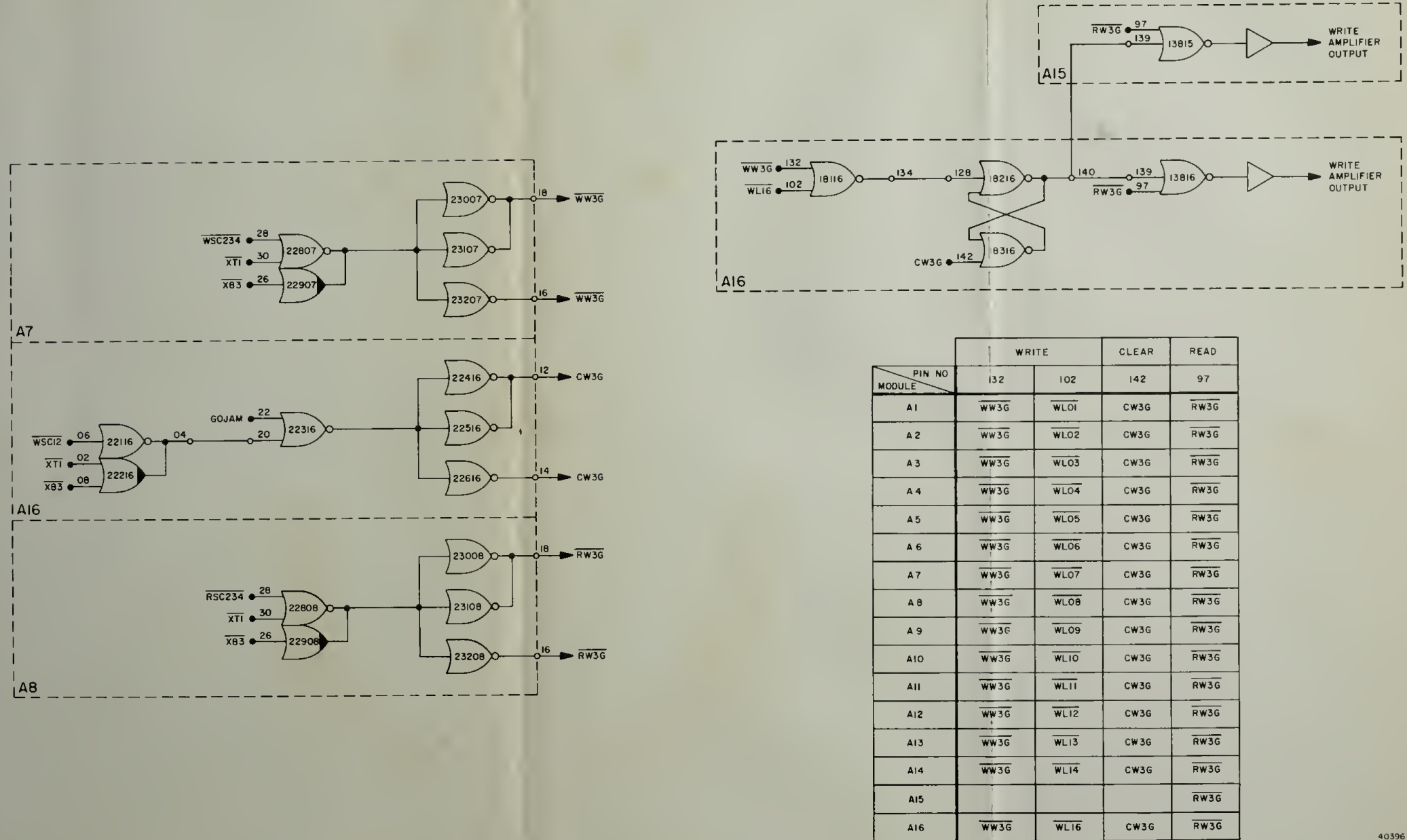
MODULE	PIN NO	WRITE		CLEAR	READ	FF OUT
		74	102	56	69	76
A 1		WWIG	WLO1	CWIG	RWIG	WIT001
A 2		WWIG	WLO2	CWIG	RWIG	WIT002
A 3		WWIG	WLO3	CWIG	RWIG	WIT003
A 4		WWIG	WLO4	CWIG	RWIG	WIT004
A 5		WWIG	WLO5	CWIG	RWIG	WIT005
A 6		WWIG	WLO6	CWIG	RWIG	WIT006
A 7		WWIG	WLO7	CWIG	RWIG	WIT007
A 8		WWIG	WLO8	CWIG	RWIG	WIT008
A 9		WWIG	WLO9	CWIG	RWIG	WIT009
A10		WWIG	WLO10	CWIG	RWIG	WIT010
A11		WWIG	WLO11	CWIG	RWIG	WIT011
A12		WWIG	WLO12	CWIG	RWIG	WIT012
A13		WWIG	WLO13	CWIG	RWIG	WIT013
A14		WWIG	WLO14	CWIG	RWIG	WIT014
A15					RWIG	
A16		WWIG	WLO16	CWIG	RWIG	WIT016



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Figure 4-121. Register OUT 1





MODULE \ PIN NO	WRITE		CLEAR	READ
	132	102	142	97
A 1	WW3G	WLO1	CW3G	RW3G
A 2	WW3G	WLO2	CW3G	RW3G
A 3	WW3G	WLO3	CW3G	RW3G
A 4	WW3G	WLO4	CW3G	RW3G
A 5	WW3G	WLO5	CW3G	RW3G
A 6	WW3G	WLO6	CW3G	RW3G
A 7	WW3G	WLO7	CW3G	RW3G
A 8	WW3G	WLO8	CW3G	RW3G
A 9	WW3G	WLO9	CW3G	RW3G
A 10	WW3G	WLO10	CW3G	RW3G
A 11	WW3G	WLO11	CW3G	RW3G
A 12	WW3G	WLO12	CW3G	RW3G
A 13	WW3G	WLO13	CW3G	RW3G
A 14	WW3G	WLO14	CW3G	RW3G
A 15				RW3G
A 16	WW3G	WL16	CW3G	RW3G

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Figure 4-122. Register OUT 3



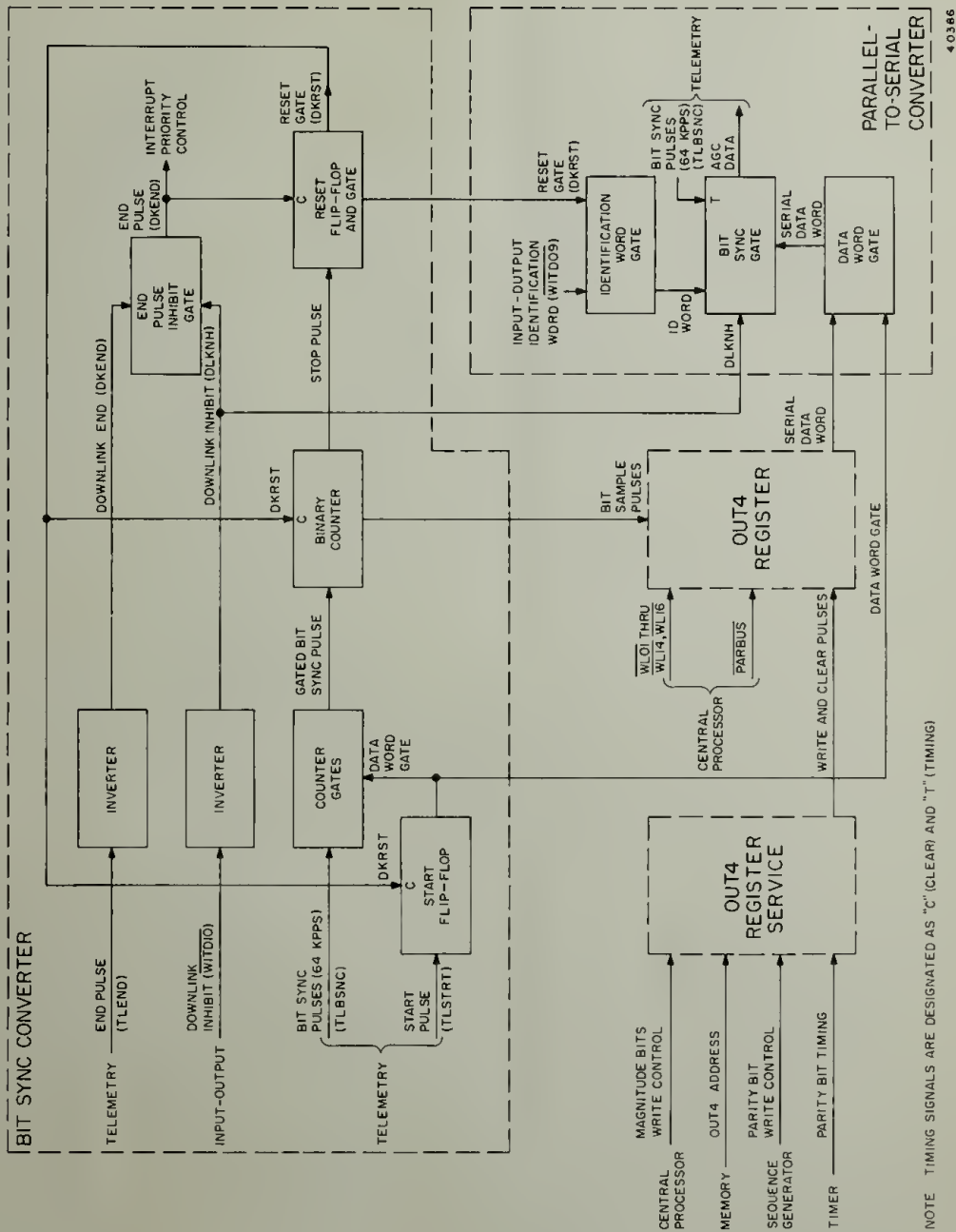


Figure 4-123. Downlink Converter, Functional Diagram

In the spacecraft telemetry system, the AGC is allotted the first five 8 bit telemetry words in each frame. The first and second telemetry words contain the 16 bit AGC word, the third and fourth words repeat the 16 bit AGC word, and the fifth telemetry word contains an 8 bit identification code. Therefore, the AGC message comprises a total of 40 bits in each telemetry frame.

The start pulse (TLSTRT) sets initial counter and gate conditions in the downlink converter prior to the first bit sync pulse (TLBSNC). Each bit sync pulse steps the binary counter and causes a 1 bit output from the downlink converter. After the required 40 bit sync pulses have been supplied to the spacecraft telemetry system, the end pulse (TLEND) occurs and resets the downlink converter to its initial condition. The end pulse also inhibits the downlink converter output. A downlink inhibit signal (DLKHN), produced by AGC program operation, inhibits downlink converter operation and generates signal DKEND, which is required to initiate the telemetry-message display program.

Operation begins when the start pulse sets the start flip-flop to condition the counter gates and the data word gate. The bit sync pulses are then applied through the counter gates to step the binary counter. The binary counter is initially set to zero by the start pulse control through the counter gates. The binary counter controls bit pulses, which gate individual bit positions in register OUT 4.

Register OUT 4 receives 15 bits and the parity bit from the central processor and receives write and clear pulses from register OUT 4 service. The write control inputs from the central processor and the address of register OUT 4 from memory (0014) initiates the write and clear pulses for register OUT 4. The OUT 4 address, the parity generate signal from the sequence generator, and timing signals control the write and clear pulses for the parity bit input to register OUT 4. The data bits and the parity bit are written into register OUT 4 at different times during a memory cycle and prior to the receipt of the start pulse. Bit position 15 contains the parity bit; positions 16 and 14 through 1 contain the data bits.

The count specified by the binary counter when the first bit pulse is received is 0000. Bit position 16 is gated out first by bit pulses from the binary counter. The data word gate is enabled if bit position 16 contains a logic ONE. The output from the data word gate and the bit sync pulse enable the bit sync gate, and a logic ONE is sent to the spacecraft telemetry system. When the first bit sync pulse is removed, the binary counter steps to 0001 and the bit pulses enable bit position 14. The next bit sync pulse strobes bit position 14 and conditions the binary counter so that it will step to 0010 when the second bit sync pulse is removed. This strobing action continues (bit position 16, then 14 through 1) until the sixteenth bit sync pulse strobes the parity bit position (15) which is the last bit position transmitted. The binary counter now resets to 0000 and the seventeenth bit sync pulse strobes bit position 16 to begin sending the AGC word for the second time. Bit sync pulse 32 completes the second transmission of the AGC word and initiates action within the binary counter to produce the stop pulse.

The stop pulse sets the reset flip-flop and is supplied through the reset gate as signal DKRST. Signal DKRST conditions the identification word gate, resets the start flip-flop, and sets the binary counter to 0001. The start flip-flop inhibits the data word gate and the counter gates. The bit sync gate is now controlled by the identification word gate and the next 8 bit sync pulses. Eight logic ONE's or eight logic ZERO's, according to the identification word input, are then sent to the spacecraft telemetry system.

The end pulse occurs after the 40 bit sync pulses required to send the AGC word and the 8 bit code. The end pulse inhibit gate clears the reset flip-flop and signals DKRST is removed and the identification word gate is inhibited. The identification word gate output, in conjunction with the data word gate output, inhibits the bit sync gate. This inhibit remains until the next start pulse occurs and the transmission of another word is initiated.

The downlink inhibit signal inhibits the end pulse and inhibits the bit sync gate. Downlink converter outputs are inhibited until after this output is removed and an end pulse is received. The next start pulse then sets the binary counter to 0000, and operation is resumed.

**4-8.4.5 Downlink Converter Detailed Description.** The downlink circuits transform AGC parallel data selected by program control into serial data for transmission by the telemetry section. Register OUT 4 is used to perform the parallel-to-serial conversion. A telemetry word consists of 8 bits of information. Thus, one computer word comprises two telemetry words. Data to be transmitted downlink is placed on the write lines and written into register OUT 4 (figure 4-124). The register bit positions are then strobed by the output (F1 through F4) of a binary counter applied to the read gates of each bit position. This action causes one bit of the word at a time (in serial fashion) to be read out to the telemetry section through the interface.

The downlink circuits (figure 4-125) are synchronized by input sync pulses from the spacecraft. The start pulse (TLSTRT) sets the start flip-flop (FF93006-93007). The flip-flop output enables the data word gate (93018) and the binary counter input gates (93008 and 93009 on figure 4-126). The telemetry bit sync pulses are then gated into the binary counter through the input gates. Outputs F1 through F4 and their complements are supplied to the various bit positions of register OUT 4 to gate out the information serially to the data word gate. The information in the register is strobed or sampled twice, causing four telemetry words from the AGC to be generated. The counter overflows on the thirty-secondth input sync pulse. This sets the stop flip-flop (FF93225-93226) and causes reset signal DKRST to be generated, which resets the start flip-flop and inhibits additional sync pulses from stepping the counter. Reset signal DKRST also conditions the counter to a state of 0001 and enables the identification word gate (93020, figure 4-125). Bit 9 from register OUT 1 also is applied to this gate. An 8-bit output results, indicating that two identical words were transmitted. At the completion of the 8-bit identification train, the telemetry end signal (TLEND) resets the stop flip-flop and inhibits DKRST. If register OUT 4 is not to be reloaded at this time, bit 10 from register OUT 1 (block end pulse) is a ONE and inhibits the end signal. The next start pulse (TLSTRT) causes the same word to be transmitted again.



The binary counter outputs are applied to the read gates of register OUT 4 such that bit 16 is strobed first; bit 14 is strobed next and the remaining bits in descending order to bit 1. Bit 15, the parity bit of the word, is the last bit transmitted.

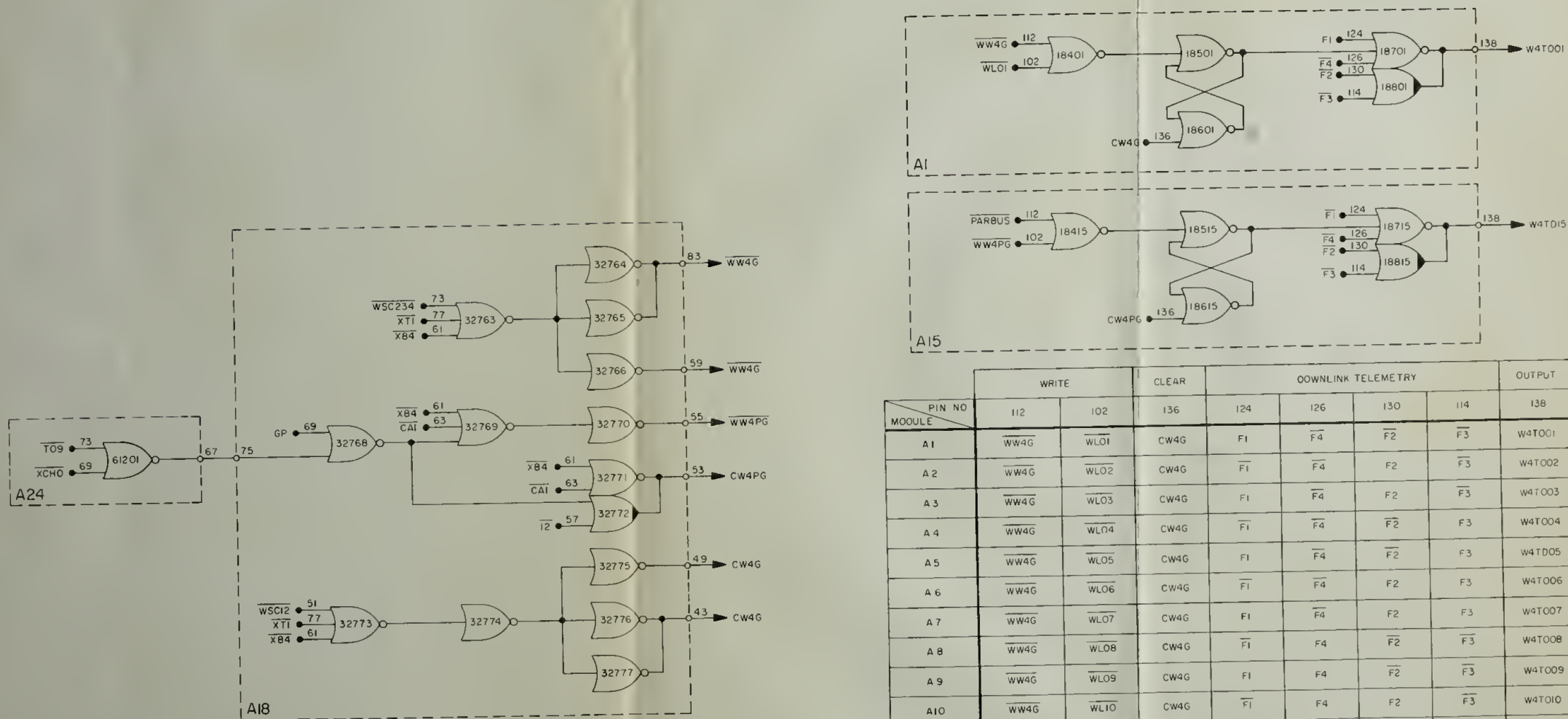
4-8.4.6 Alarm Control Circuits. The alarm circuits provide outputs to the DSKY's which are indicative of specific conditions in the AGC. These alarms are RUPT lock alarm (RPTAL), TC trap alarm (TCAL), counter fail alarm (CTRAL), parity fail alarm (PAL), and scaler fail alarm (SCAFAL). Four additional alarms are generated but not as part of the alarm circuits as discussed in this paragraph. Three of these are generated under program control and are available from bits 1, 4, and 5 of register OUT 1. The alarms are, respectively, program alarm, telemetry alarm, and program check fail alarm. A power supply fail alarm indication is also provided to the main and navigation control panels from the computer power supply.

4-8.4.6.1 RUPT Lock Alarm. The RUPT lock alarm output (figure 4-127) is enabled if an interruption has been in progress longer than 10 msec (RPTLDS) or if an interruption has not occurred during an 80 msec period (NRPTAL). Assume that an interrupt is in progress (IIP). Input IIP holds FF88120-88121 reset. Signal ALSET is inverted and sets FF88114-88115. If an interrupt is still in progress when HNDPPS occurs, input IIP is still a logic ZERO and consequently will not have reset FF88114-88115. The reset output from this flip-flop enables gate 88116 when HNDPPS occurs and causes RPTLDS to be generated. The interval between ALSET and HNDPPS is 10 msec. Consequently an interrupt condition has only 10 msec maximum time to be completed; otherwise an alarm will be generated. If no interruption is in progress when signal F14A occurs, FF88120-88121 is set. If no interruption occurs when F14B enables gate 88122, the output from this gate sets FF88123-88124 and enables the RUPT lock alarm output. The interval between F14A and F14B is 80 msec. Outputs RPTAL (10 msec interval) and NRPTAL (80 msec interval) are applied to gate 88751, and either one causes signal ALGA to initiate a GOJAM condition. Thus, if an interruption is too long or does not occur as described above, signal GOJAM restarts the AGC.

4-8.4.6.2 TC Trap Alarm. The TC trap alarm generation circuit (figure 4-127) is similar to that of the RUPT lock alarm circuit. An alarm is generated if a TC (transfer control) instruction has been in progress for an interval greater than 10 msec or if no TC instruction is executed during the 10 msec period of ALSET and HNDPPS. When ALSET occurs FF88128-88129 is set. If the execution of the instruction is completed when HNDPPS occurs, the flip-flop is reset (by the output from gate 88127) and no alarm indication occurs. If the TC instruction is still in progress during HNDPPS, FF88131-88132 is set and the alarm registers. A TC alarm registers in conjunction with a counter alarm for this 10 msec test interval. Signal INKL to gate 88127 indicates a counter increment request. Therefore, if either TC0 or INKL is present during HNDPPS, the alarm occurs.

If a TC instruction is not executed (which would reset FF88134-88135 in the interval between ALSET and HNDPPS [10 msec]), gate 88136 is enabled and sets FF88137-88138. This in turn causes TCLDS to register an alarm. Outputs TCAL and NTCAL, similar to the interrupt alarm conditions, cause signal ALGA to generate GOJAM and restarts the AGC.

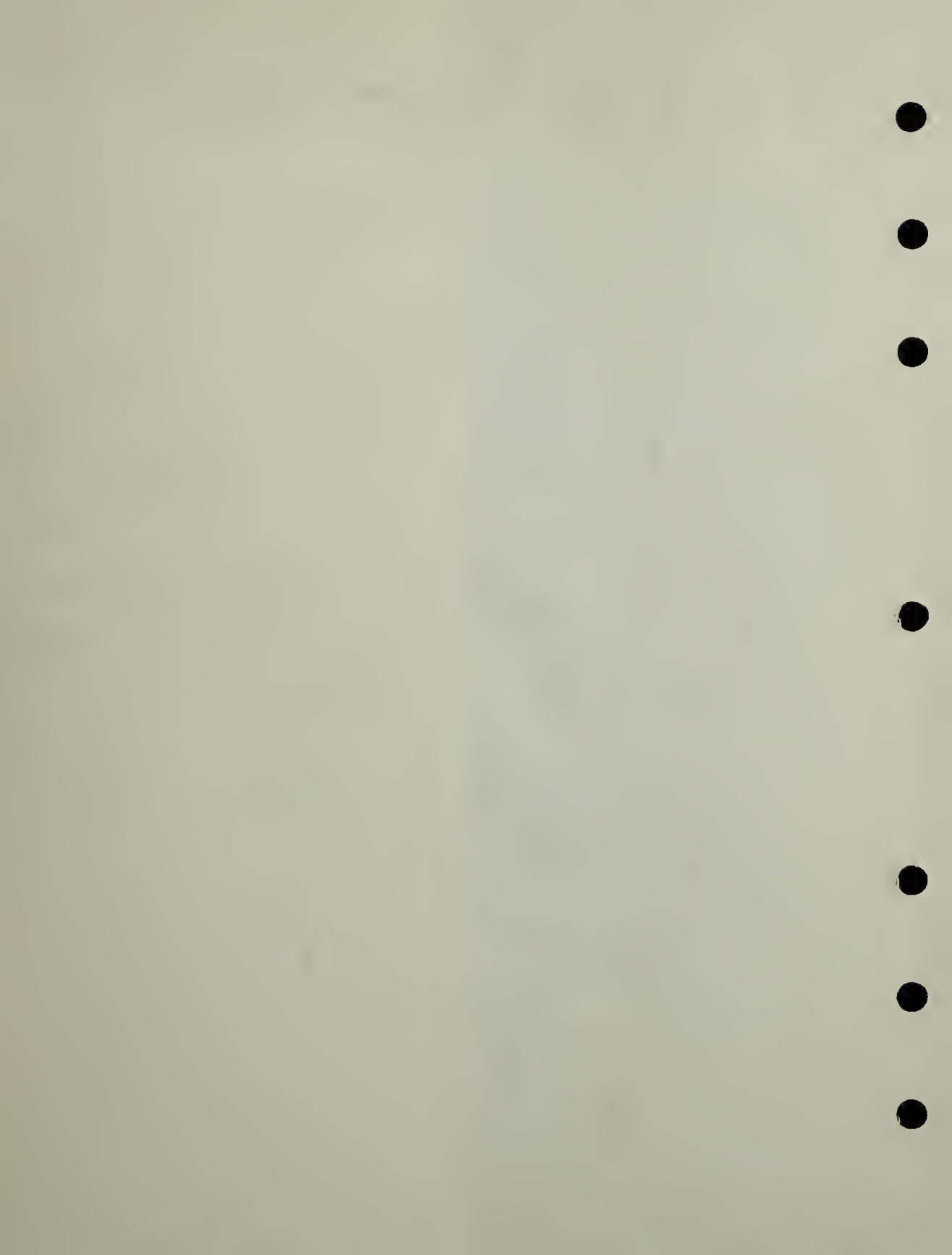
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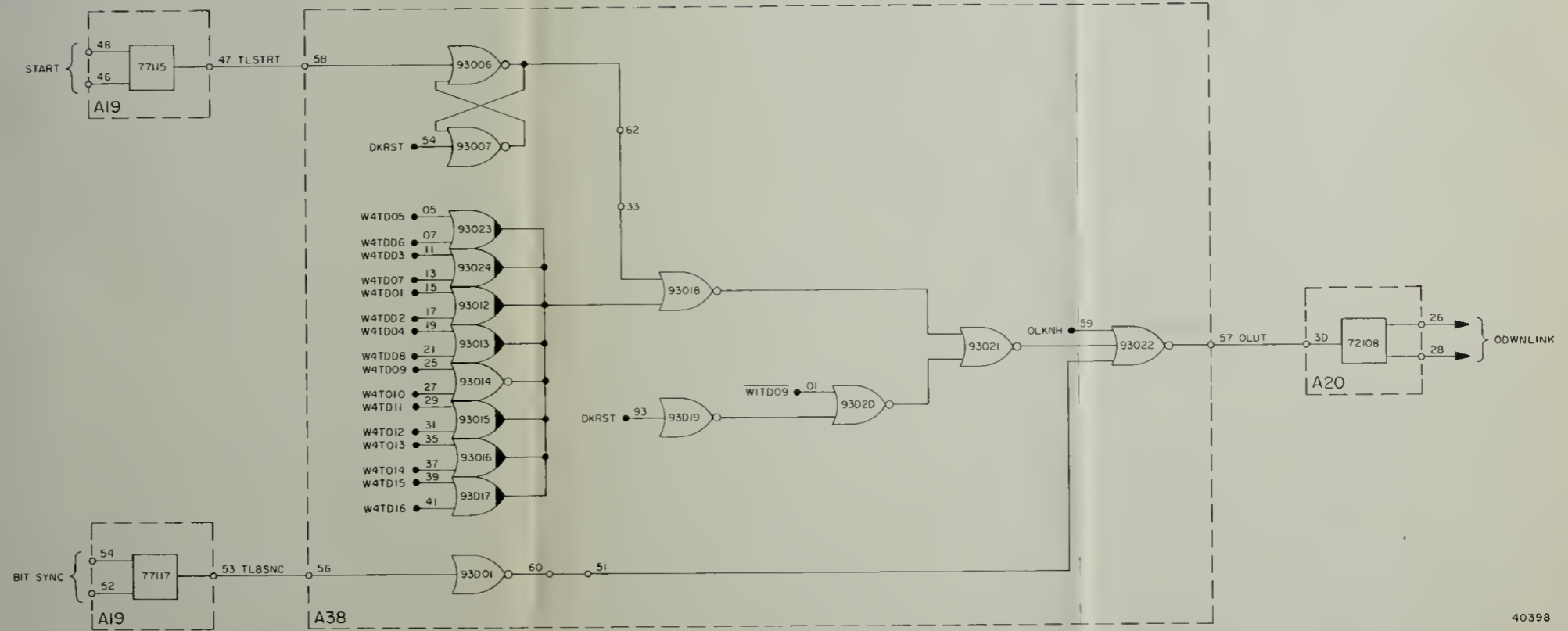


MODULE	WRITE		CLEAR	DOWNLINK TELEMETRY				OUTPUT
	112	102	136	124	126	130	114	138
A 1	WW4G	WLO1	CW4G	F1	F4	F2	F3	W4T001
A 2	WW4G	WLO2	CW4G	F1	F4	F2	F3	W4T002
A 3	WW4G	WLO3	CW4G	F1	F4	F2	F3	W4T003
A 4	WW4G	WLO4	CW4G	F1	F4	F2	F3	W4T004
A 5	WW4G	WLO5	CW4G	F1	F4	F2	F3	W4T005
A 6	WW4G	WLO6	CW4G	F1	F4	F2	F3	W4T006
A 7	WW4G	WLO7	CW4G	F1	F4	F2	F3	W4T007
A 8	WW4G	WLO8	CW4G	F1	F4	F2	F3	W4T008
A 9	WW4G	WLO9	CW4G	F1	F4	F2	F3	W4T009
A 10	WW4G	WLO10	CW4G	F1	F4	F2	F3	W4T010
A 11	WW4G	WLO11	CW4G	F1	F4	F2	F3	W4T011
A 12	WW4G	WLO12	CW4G	F1	F4	F2	F3	W4T012
A 13	WW4G	WLO13	CW4G	F1	F4	F2	F3	W4T013
A 14	WW4G	WLO14	CW4G	F1	F4	F2	F3	W4T014
A 15	PARBUS	WW4PG	CW4PG	F1	F4	F2	F3	W4T015
A 16	WW4G	WLO16	CW4G	F1	F4	F2	F3	W4T016

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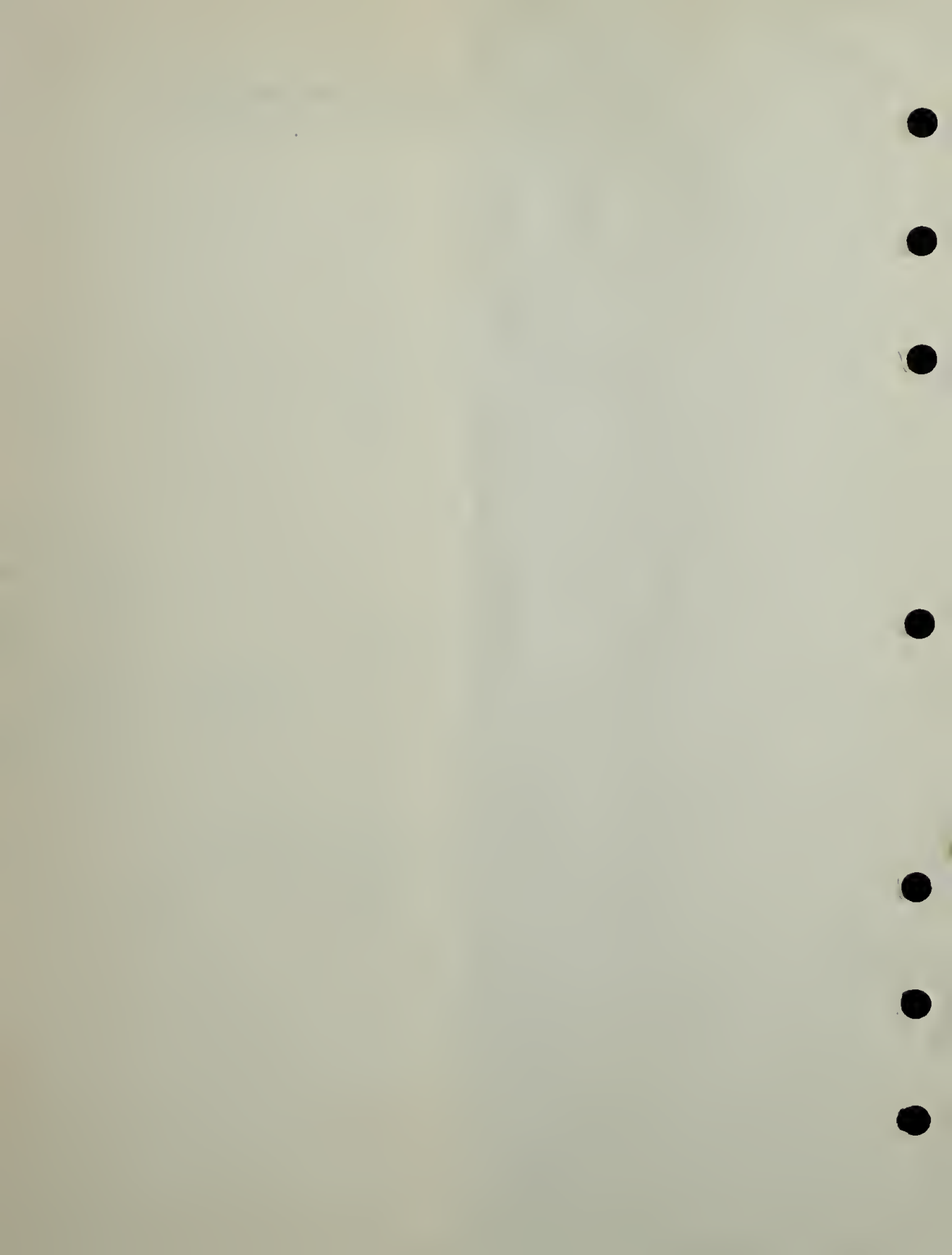
Figure 4-124. Register OUT 4

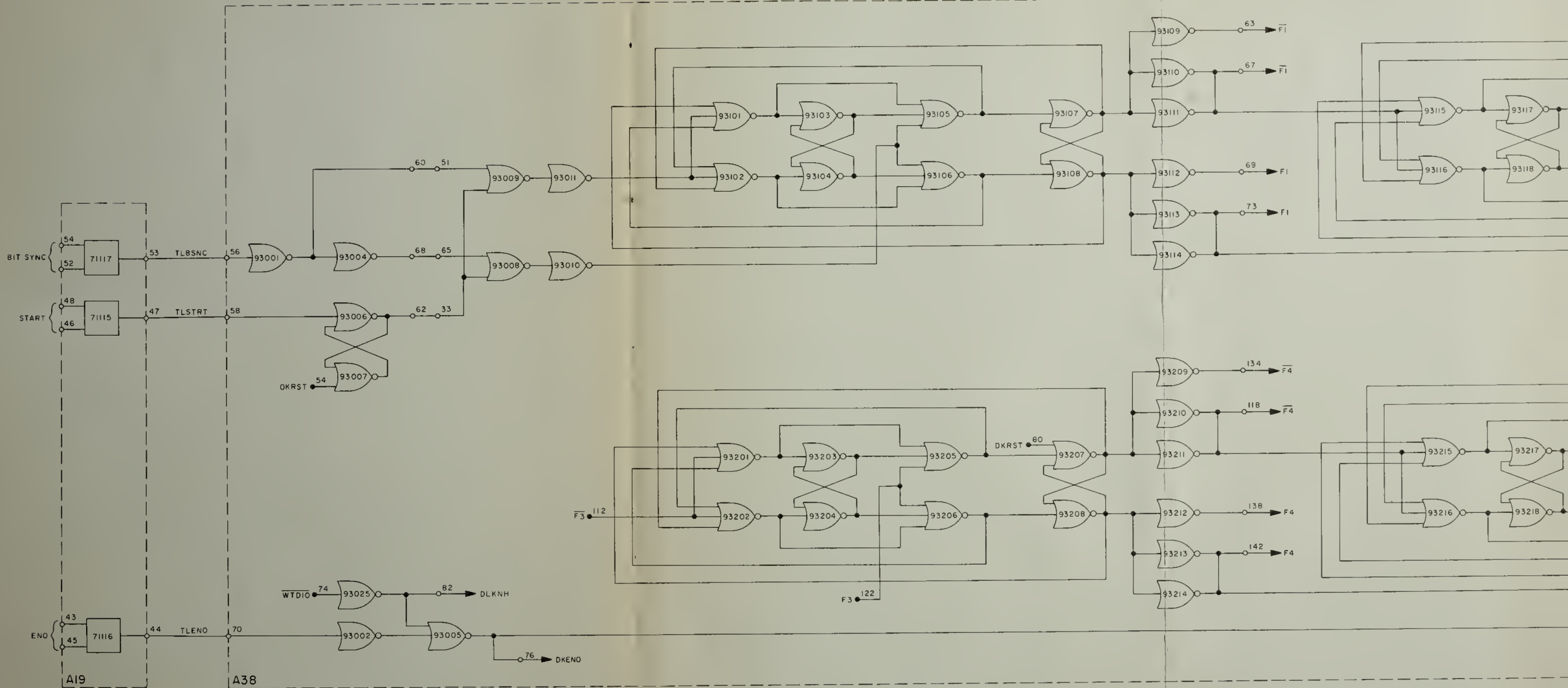




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Figure 4-125. Downlink Telemetry Parallel To Serial Converter





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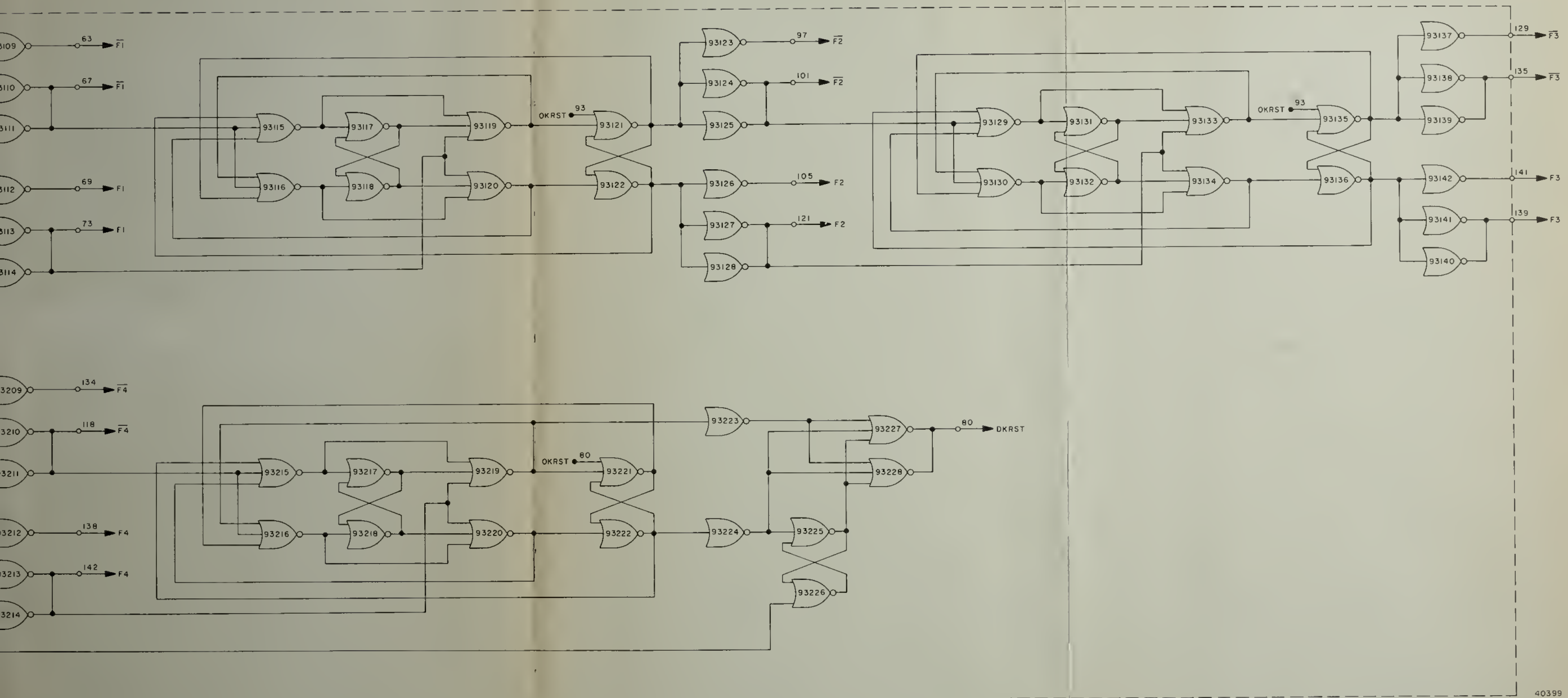
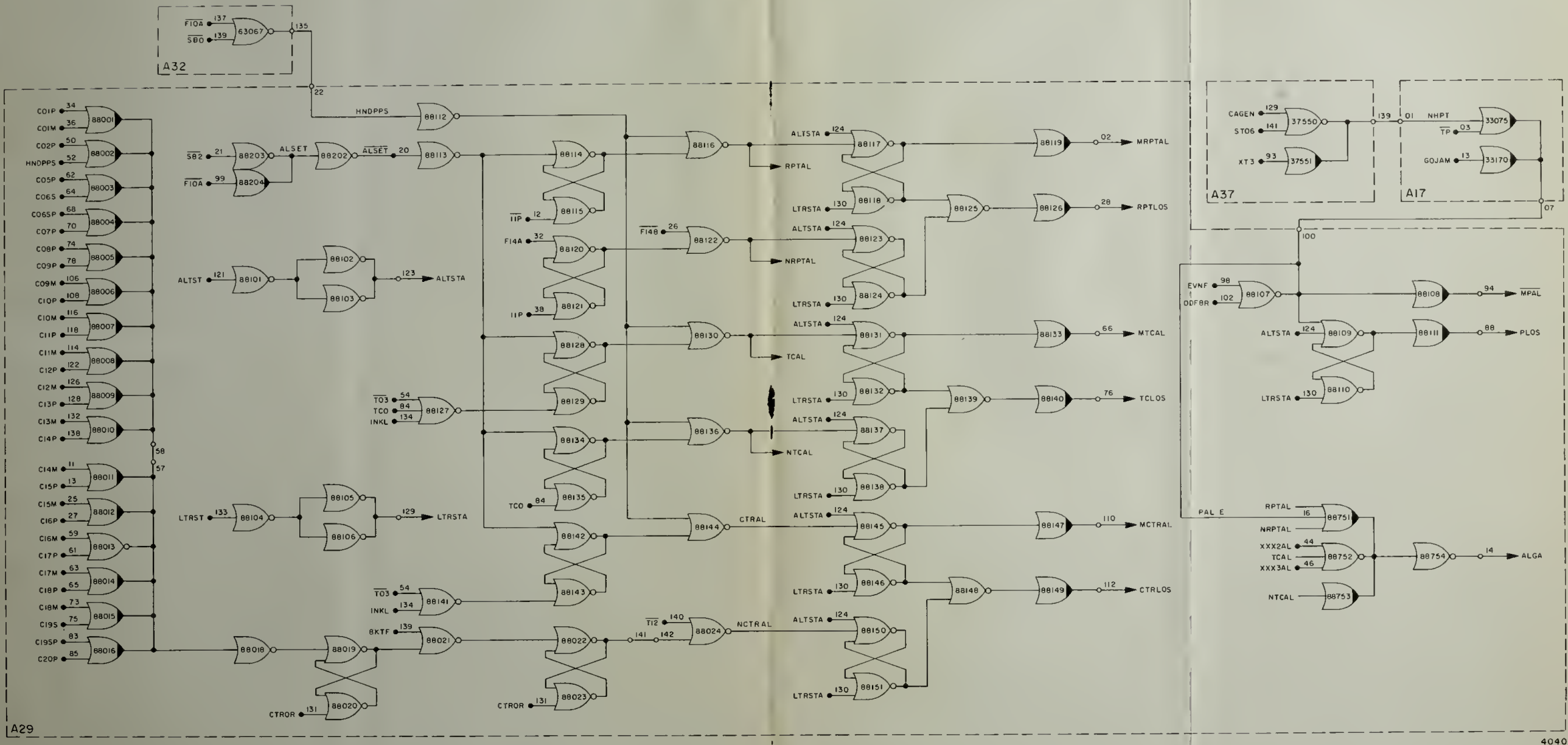


Figure 4-126. Downlink Telemetry Bit Sync Counter





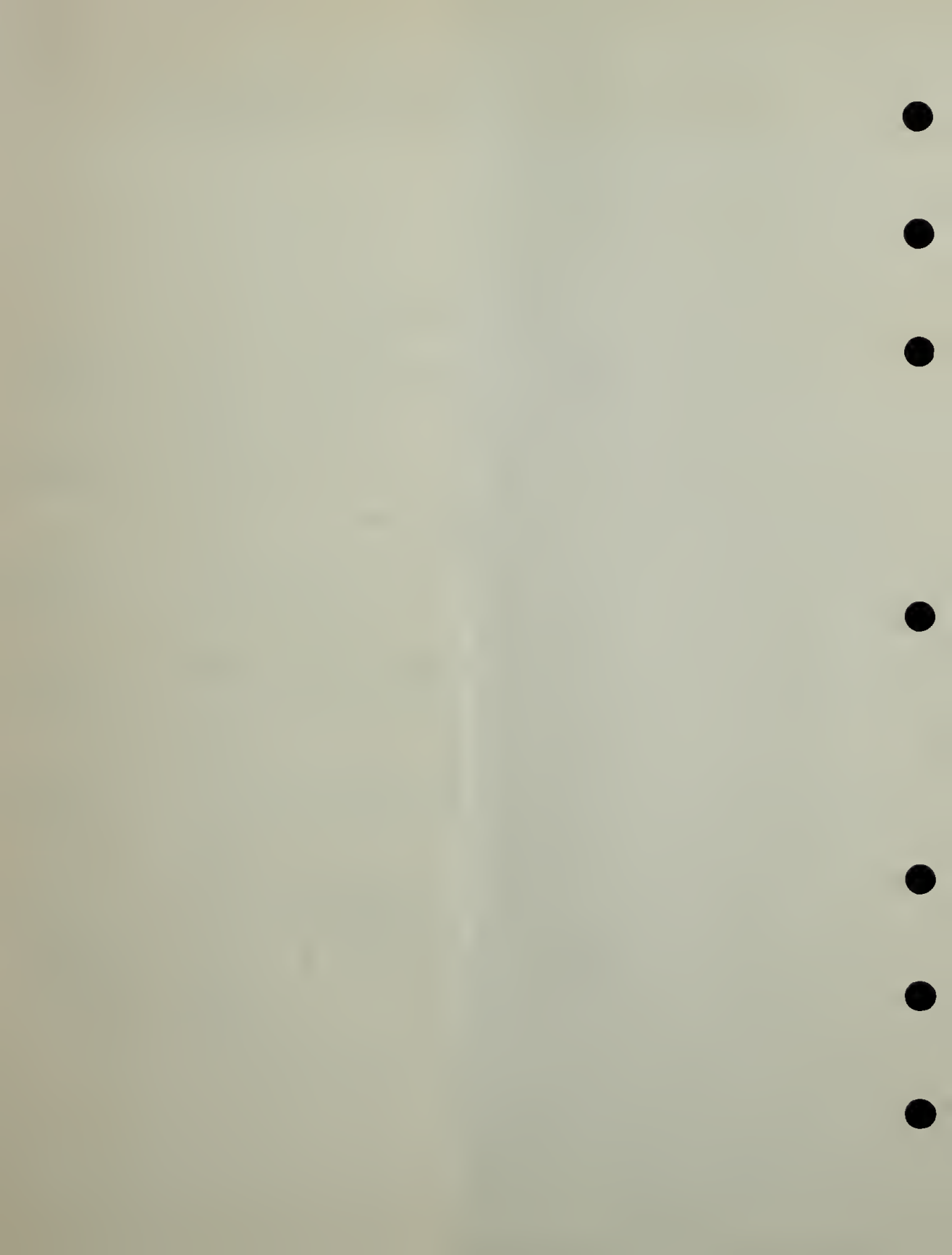
APOLLO GUIDANCE AND NAVIGATION SYSTEM



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Figure 4-127. Alarm Circuits



4-8.4.6.3 Counter Fail Alarm. The counter fail alarm registers if a counter increment is in progress for more than 10 msec or if a counter increment operation is requested and does not take place. When a counter is being incremented, signal INKL is ONE and inhibits gate 88141. Signal ALSET (inverted) sets FF88142-88143. If the counter increment is completed when HNDPPS occurs, the flip-flop is reset (INKL becomes ZERO). If the counter increment is not completed, an alarm registers. This occurs coincidentally with the TC alarm described previously, since INKL is one of the gating conditions in the TC trap alarm circuits (gate 88127).

The incremental inputs to the counters of erasable memory are also applied from priority control to the extended NOR gate configuration (88013, et cetera) of figure 4-127. Any incremental input sets FF88019-88020. The output from this flip-flop conditions gate 88021 to set FF88022-88023. If the request to increment occurs by time 9 of the memory cycle, signal CTROR (request to increment) resets both flip-flops and no alarm registers. If no request to increment occurs, signal BKTF, which is coincident with time 9, enables gate 88021 and sets FF88022-88023. At time 12 the alarm flip-flop (88150-88151) is set and indicates the failure of counter priority control to process a counter increment request. This indication is sent to the CTR FAIL indicator on the AGC navigation panel DSKY.

4-8.4.6.4 Parity Fail Alarm. A parity fail alarm occurs if a word has been incorrectly read out of memory as a result of a core or flip-flop malfunction. Parity check is that of odd parity since the total number of ONE's in the word, including the parity bit, is odd. A test for correct parity (TP) is performed on all words read out of memory above address 0030. This address is specified by the inputs to gates 37550 and 37551. Below this address, or if signal GOJAM occurs, no parity test occurs.

For a correct parity check, either signal EVNF or ODFBR is a logic ONE and inhibits an output from gate 88107 in figure 4-127. If both of these signals are logic ZERO's, incorrect parity is indicated and FF88109-88110 is set. This results in a PARITY FAIL indication on the AGC navigation panel DSKY. A parity alarm causes signal GOJAM to be generated (ALGA applied to the timer).

4-8.4.6.5 Scaler Fail Alarm. The scaler fail alarm circuit (figure 4-128), monitors output FS10 from scaler A in the timer. This is a 100 pps signal applied to the monitor circuit on module B31. The absence of this signal results in a SCALER FAIL indication on the AGC navigation panel DSKY and does not initiate signal GOJAM.

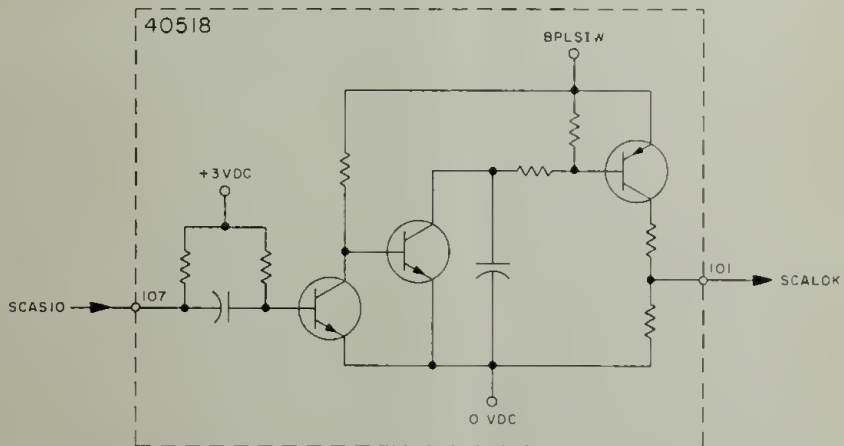
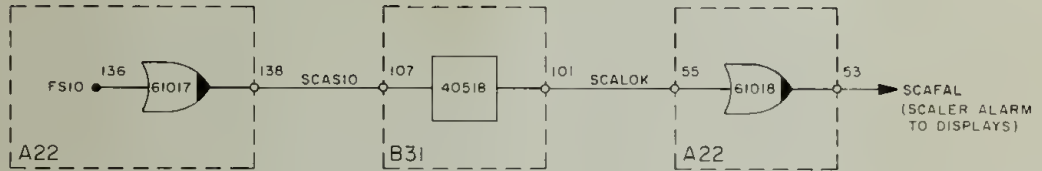
4-8.4.7 Rate Control Circuits Detailed Description. The rate control circuits provide drive pulses to the spacecraft, the G and N system, the PSA, the radars, and counter priority control. The drive pulses can be divided into two basic categories: those which are generated by the content of specific bit positions of register OUT 2 under program control and those which are generated continuously as a function of outputs from the timer. The specific bit positions of register OUT 2 associated with the rate counters are indicated in table 4-VII. A rate counter is preset to some value by a program and is then incremented. The drive pulses are gated out until overflow occurs. The bit positions associated with that particular counter are then cleared, and the drive pulses cease.

There are three clear lines for register OUT 2 (figure 4-129) each of which is enabled to clear all bit positions simultaneously either when memory address 0012 is present during normal program operations or when GOJAM is generated. A third condition for each clear line involves the memory location of associated rate counters in erasable memory (OUT CTR1, OUT CTR2, OUT CTR3). Address 0042 (OUT CTR1) causes clear signal CW2AG to be generated and clear only bit positions 9 through 14 and 16 when overflow occurs. In a similar manner address 0043 (OUT CTR2), coincident with overflow, causes clear signal CW2BG to be generated and clear only bit position 4 through 8. Address 0057, coincident with overflow, causes CW2CG to be generated and clear only bit positions 1 through 3. The indicated counter outputs are used to generate specific pulse rates to other spacecraft systems.

4-8.4.7.1 Rate Control Gating Signals. Gating signals for the rate control logic (figure 4-130) are generated by inputs from the timer. Strobe signals SB0, SB1, and SB2 are 3 microsecond pulses at a rate of 102.4 kpps which are inverted to produce negative-going enabling signals. Signal  $\overline{\text{RATE}}$  is a 3.2 kpps negative pulse train. The width is determined by the narrowest signal input to gate 77020. This signal is SB2, which is 3 microsecond wide.

4-8.4.7.2 Rate 1 Control. The rate 1 control logic (figure 4-131) generates drive pulses for the gyros (IRIG) and the CDU of the IMU. Two additional outputs (CAP and CAM) are provided to the counter priority control logic to increment the associated rate counter OUTCR1. Bits 12 and 13 of register OUT 2 differentiate to which unit the drive pulses are to be sent (see table 4-VIII). A ONE in bit position 12 indicates that drive pulses are to be sent to the gyros; a ONE in bit position 13 indicates that drive pulses are to be sent to the CDU. When either bit position contains a ONE, the rate 1 control flip-flop is set. This enables the transfer gates (77006 and 77009). The flip-flop is not reset until bit positions 12 and 13 both contain logic ZERO's, which occurs on overflow of the rate 1 counter. Bits 14 and 16 are used to differentiate between incremental and decremental pulses to either unit. A ONE in bit position 14 indicates plus increments; a ONE in 16 indicates negative increments. The designated incremental pulses are gated through the transfer gates by signal  $\overline{\text{RATE}}$ . The output from the transfer gate is applied also to the counter priority control logic (CAP if positive, CAM if minus). This action increments the rate 1 counter (OUTCR1) in erasable memory. Initially, this counter is preset to some value by the program, depending on the number of drive pulses to be sent. When overflow occurs, the specified number of pulses will have been gated out, bit positions 9 through 14 and 16 are cleared by signal CW2AG, and the drive pulses cease.

Drive pulses X, Y, and Z (+ and -) are applied through the interface to the gyros or the CDU as a function of bits 9, 10, and 11 of register OUT 2. The specific conditions of bit positions 9 through 16 necessary to send drive pulses to each unit are listed in table 4-VIII.



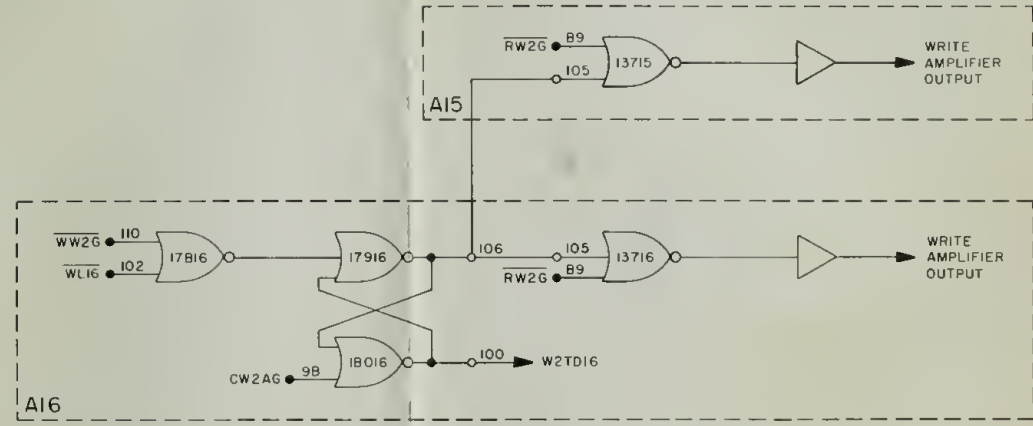
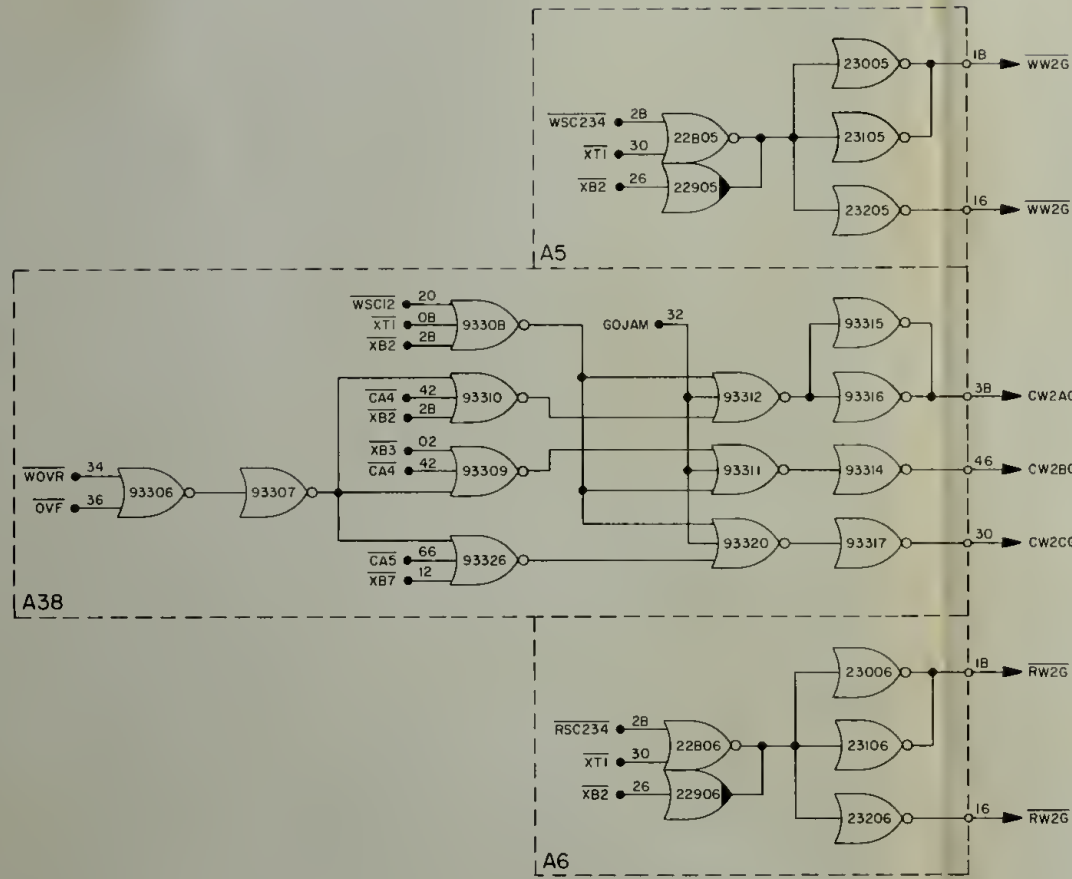
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Figure 4-128. Scaler Fail Alarm Circuits

Table 4-VIII. Rate 1 Control Signals

Signal	Bit Positions						
	16, 15	14	13	12	11	10	9
	-	+	CDU	Gyro	X	Y	Z
+CDU Z	0	1	1	0	0	0	1
-CDU Z	1	0	1	0	0	0	1
+CDU Y	0	1	1	0	0	1	0
-CDU Y	1	0	1	0	0	1	0
+CDU X	0	1	1	0	1	0	0
-CDU X	1	0	1	0	1	0	0
+IRIG Z	0	1	0	1	0	0	1
-IRIG Z	1	0	0	1	0	0	1
+IRIG Y	0	1	0	1	0	1	0
-IRIG Y	1	0	0	1	0	1	0
+IRIG X	0	1	0	1	1	0	0
-IRIG X	1	0	0	1	1	0	0

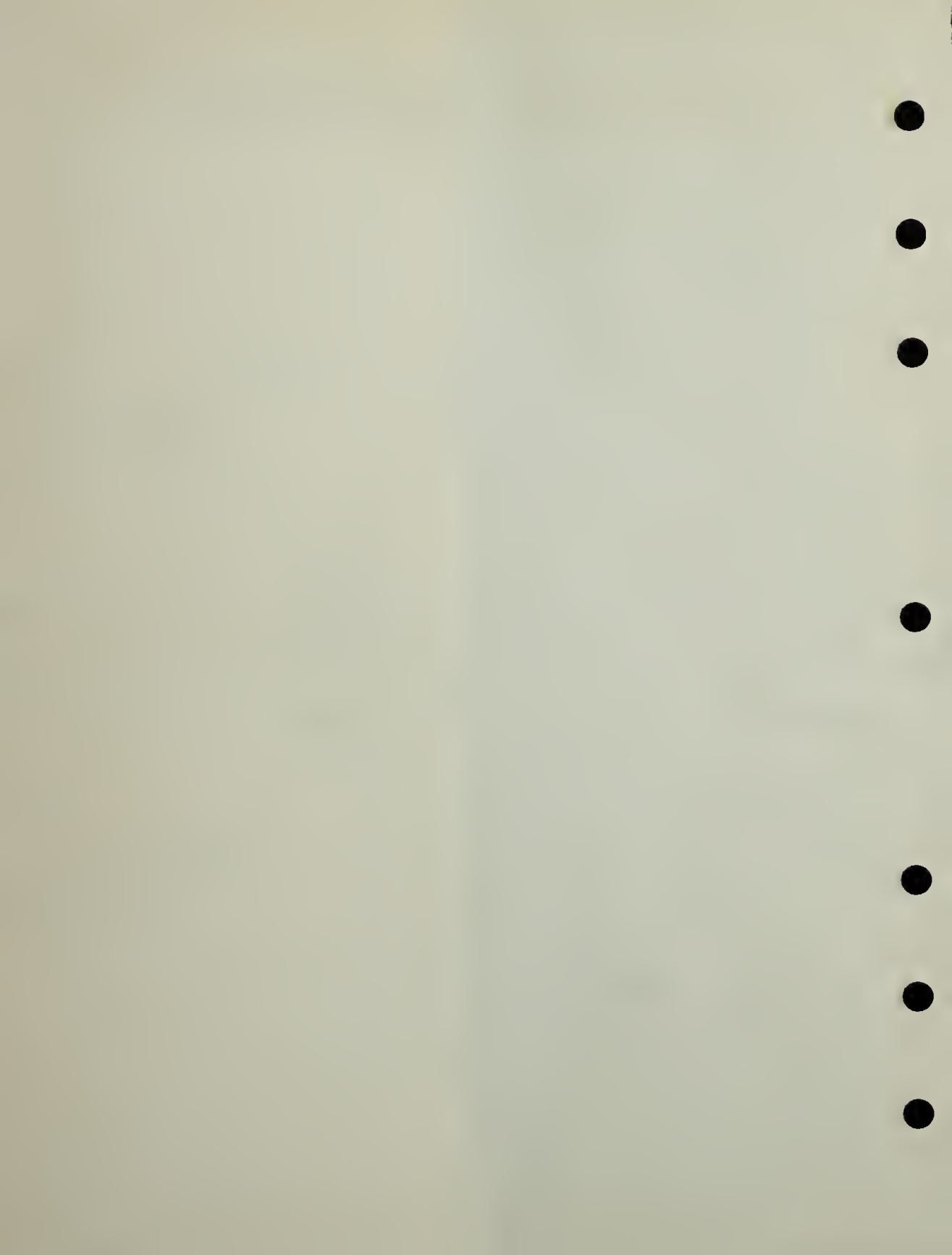
4-8.4.7.3 Rate 2 Control. The rate 2 control logic (figure 4-132) generates drive pulses to the spacecraft engines (+ and - thrust), to the optics, and incremental pulses to counter priority control, which increment the associated rate counter (OUTCR2). The method of providing drive pulses to these units is similar to that for the gyros and CDU. Bits 4 through 8 of register OUT 2 are used to produce the drive pulses. Bit 4 is a ONE for pulses to the spacecraft; bit 5 or 6 is a ONE for pulses to the optics and X axes, respectively. The type of pulse, incremental or decremental, is determined by bit 7 or 8. An incremental or decremental pulse, indicated by a ONE in either bit position 7 or 8, sets the rate 2 flip-flop. The output is gated through the transfer gate by signal RATE. Output C08P is applied to counter priority control to increment the rate 2 counter. When overflow occurs, clear signal CW2BG is generated and clears bit position 4 through 8 and the drive pulses cease. The conditions necessary for bits 4 through 8 to generate drive pulses to the spacecraft and optics are listed in table 4-IX.



MODULE	WRITE				OUTPUT
	110	102	9B	B9	
A 1	WW2G	WL01	CW2CG	RW2G	W2TD01
A 2	WW2G	WL02	CW2CG	RW2G	W2TD02
A 3	WW2G	WL03	CW2CG	RW2G	W2TD03
A 4	WW2G	WL04	CW2BG	RW2G	W2TD04
A 5	WW2G	WL05	CW2BG	RW2G	W2TD05
A 6	WW2G	WL06	CW2BG	RW2G	W2TD06
A 7	WW2G	WL07	CW2BG	RW2G	W2TD07
A 8	WW2G	WL08	CW2BG	RW2G	W2TD08
A 9	WW2G	WL09	CW2AG	RW2G	W2TD09
A10	WW2G	WL10	CW2AG	RW2G	W2TD10
A11	WW2G	WL11	CW2AG	RW2G	W2TD11
A12	WW2G	WL12	CW2AG	RW2G	W2TD12
A13	WW2G	WL13	CW2AG	RW2G	W2TD13
A14	WW2G	WL14	CW2AG	RW2G	W2TD14
A15				RW2G	
A16	WW2G	WL16	CW2AG	RW2G	W2TD16

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Figure 4-129. Register OUT 2





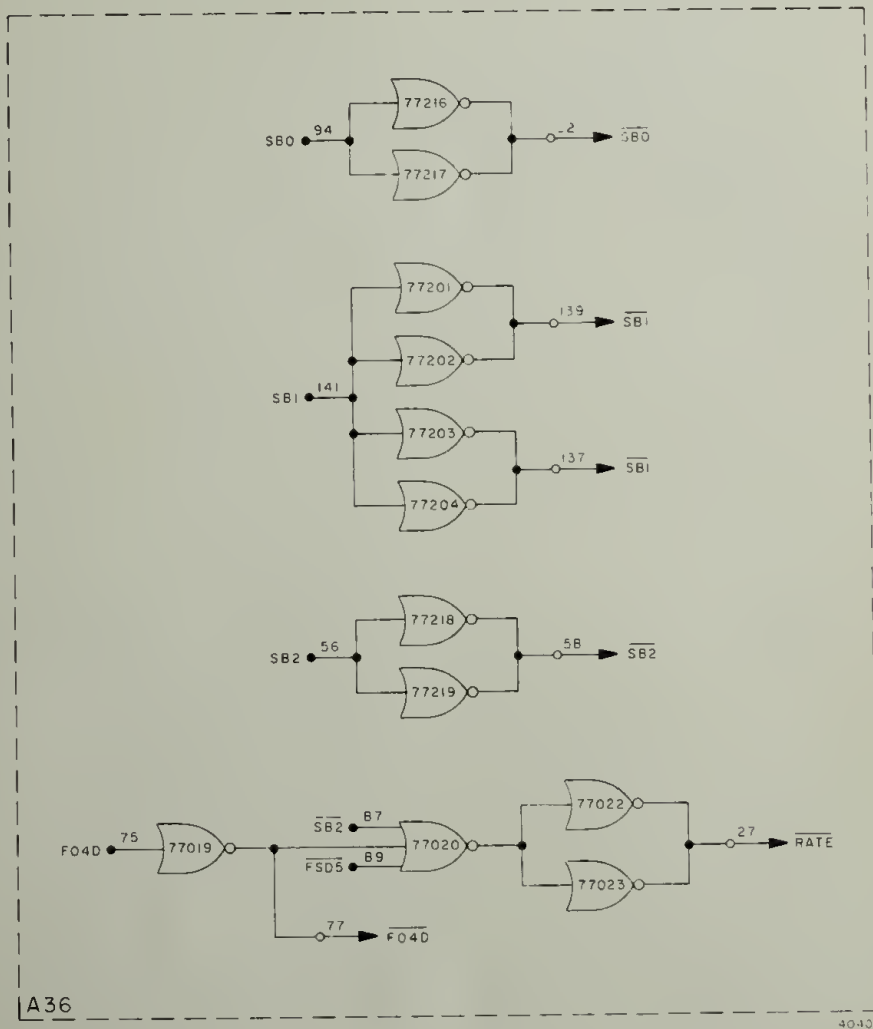


Figure 4-130. Rate Control Logic

Table 4-IX. Rate 2 Control Signals

Signal	Bit Position				
	8	7	6	5	4
	-	+	OPT X	OPT Y	S/C
+Thrust (S/C)	0	1	0	0	1
-Thrust	1	0	0	0	1
+Y optics	0	1	0	1	0
-Y optics	1	0	0	1	0
+X optics	0	1	1	0	0
-X optics	1	0	1	0	0

4-8.4.7.4 Rate 3 Control. (Rate 3 control logic is incorporated in the AGC for Block I Series 100, but is not used.) The rate 3 control logic (figure 4-133) generates drive pulses for the rendezvous and LEM radars and incremental pulses for the rate 3 counter (OUTCR3) applied through the counter priority control logic. A ONE in bit position 1, 2, or 3 of register OUT 2 sets the rate 3 control flip-flop. The output from the flip-flop is applied to the transfer gates along with signal  $\overline{\text{RATE}}$  and bit 1 of the register. If bit 1 is a ONE, gate 77107 is enabled, which indicates a plus increment. If bit 1 is a ZERO, gate 77108 is enabled, which indicates a minus increment. The outputs from these two gates, CCP or CCM (plus or minus), are sent to counter priority control to increment the rate 3 counter. The drive pulses to the radars are then generated as a function of bits 1 and 2 of the register, as indicated in table 4-X.

4-8.4.7.5 Continuous Drive Pulses. The continuous drive pulses, supplied from the AGC to the other subsystems are indicated in the logic drawing of figure 4-134. Bits 13, 14, and 16 of register OUT 1 control the pulses supplied to the spacecraft. These are engine control signals and, although they are generated under program control (a ONE in bit 13, 14, or 16), they are continuous in that once enabled no specific number is generated, as is the case with the rate counters. A ONE in bit position 13, 14, or 16 of register OUT 1 sets the engine control flip-flop coincidentally with timing signal SB0. The flip-flop output enables the engine sequence gates. A ONE in bit position 13 enables the engine-on (ENON) output; a ONE in bit position 14 enables the thrust command output (THRCOM); a ONE in bit position 16 enables the engine-off output (ENOFF). All three outputs occur at a rate of 102.4 kpps. The engine control flip-flop is reset at the termination of the thrust sequence when bits 13, 14, and 16 are all logic ZERO's.

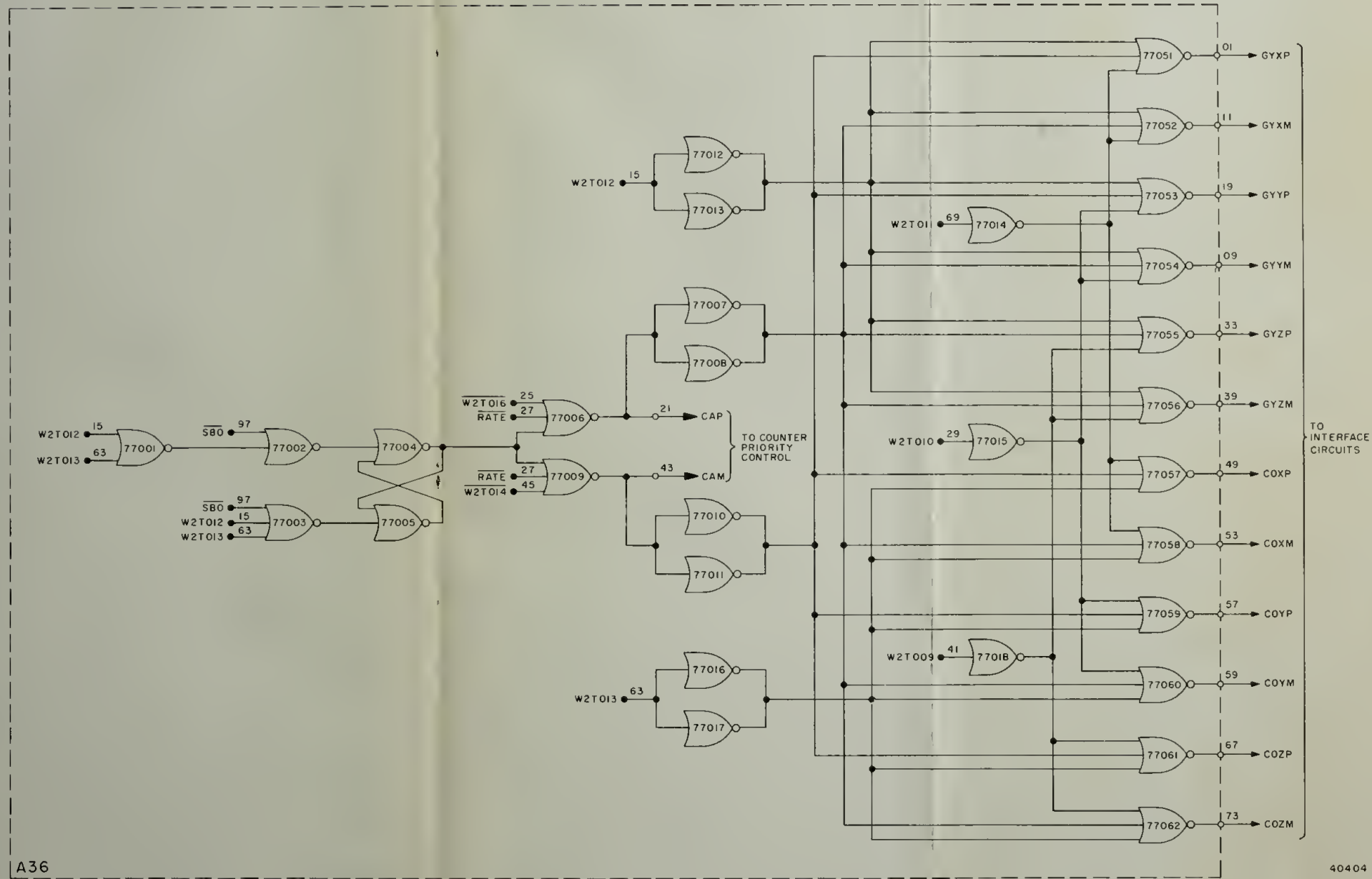
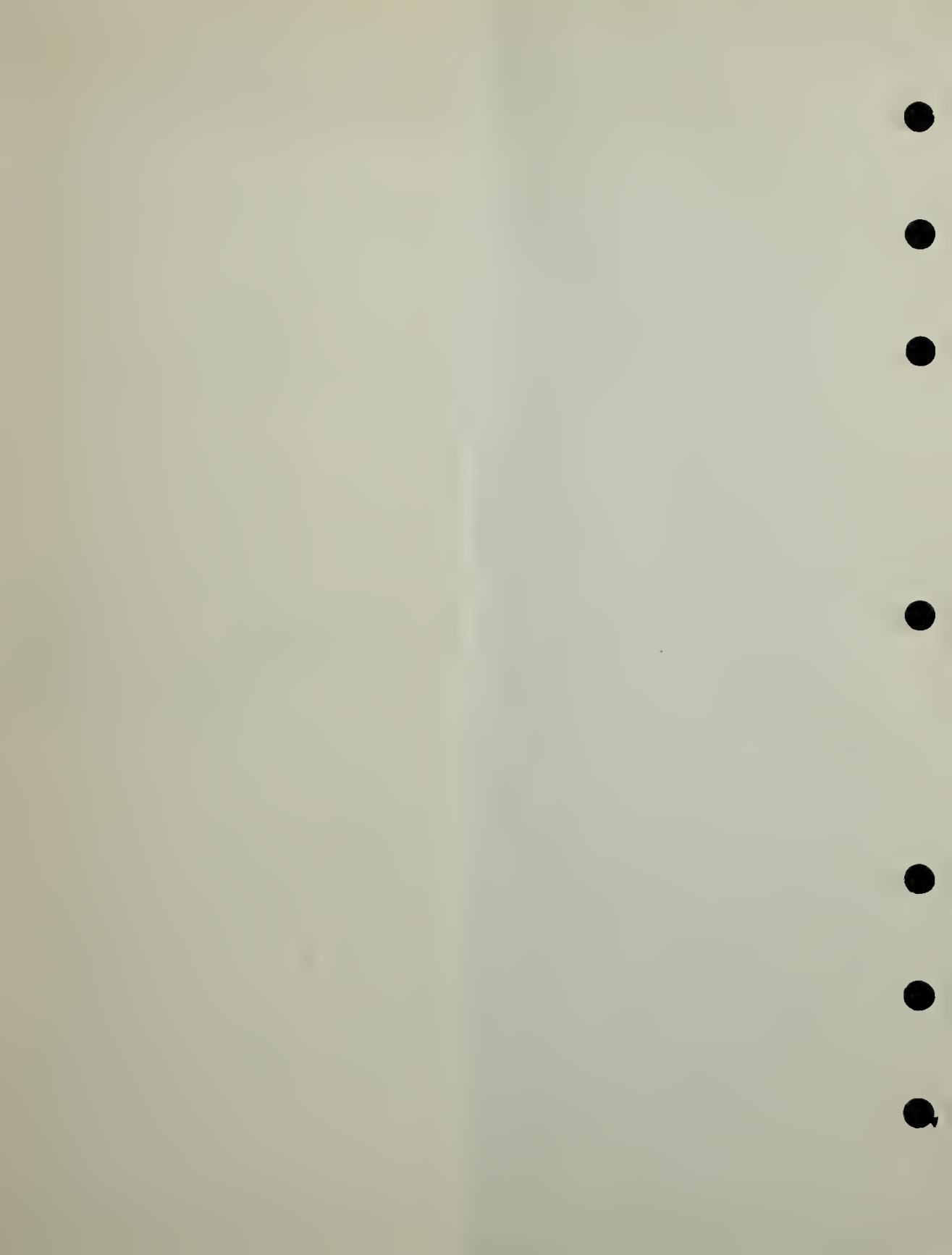


Figure 4-131. Rate 1 Control



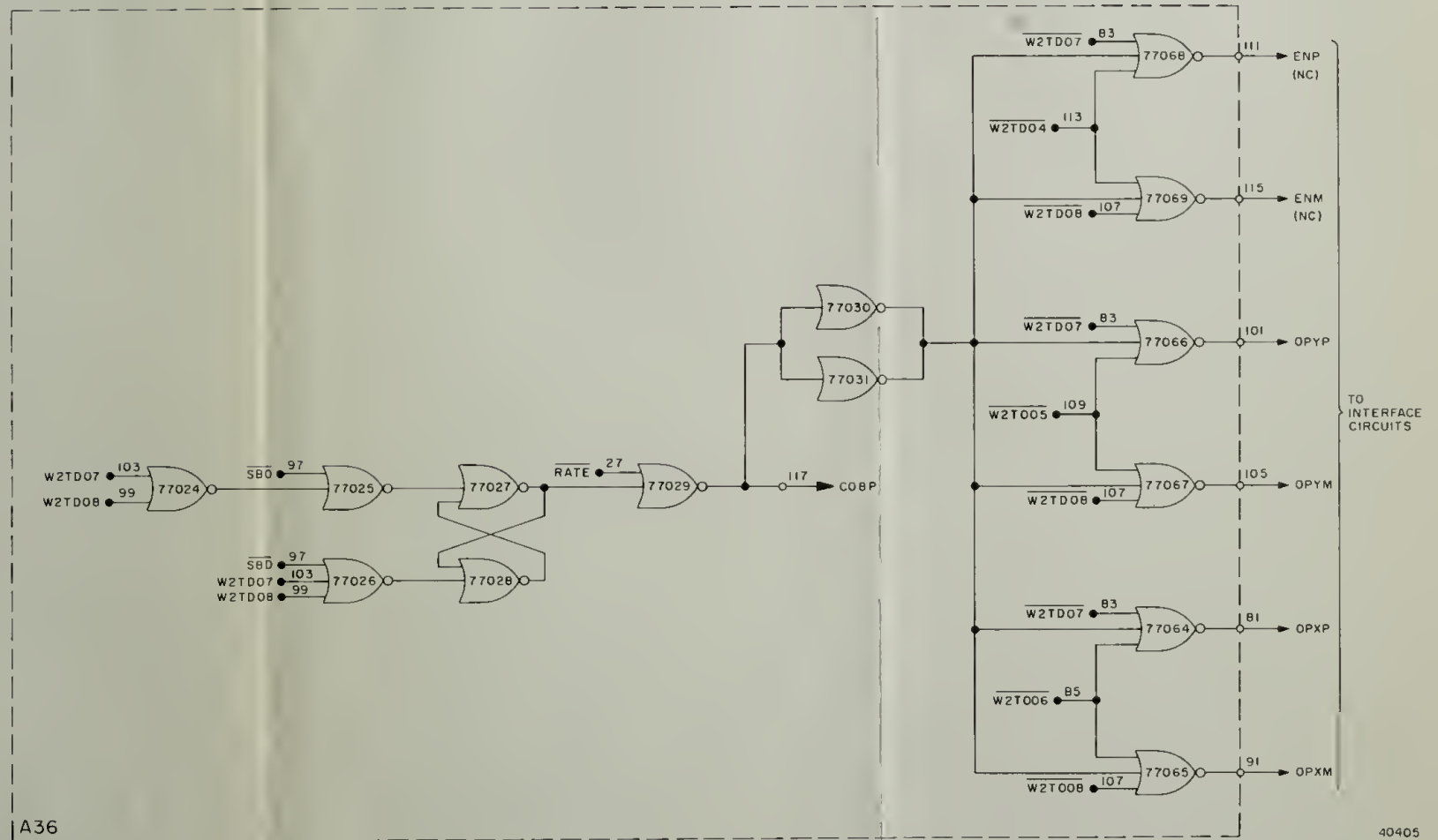


Figure 4-132. Rate 2 Control



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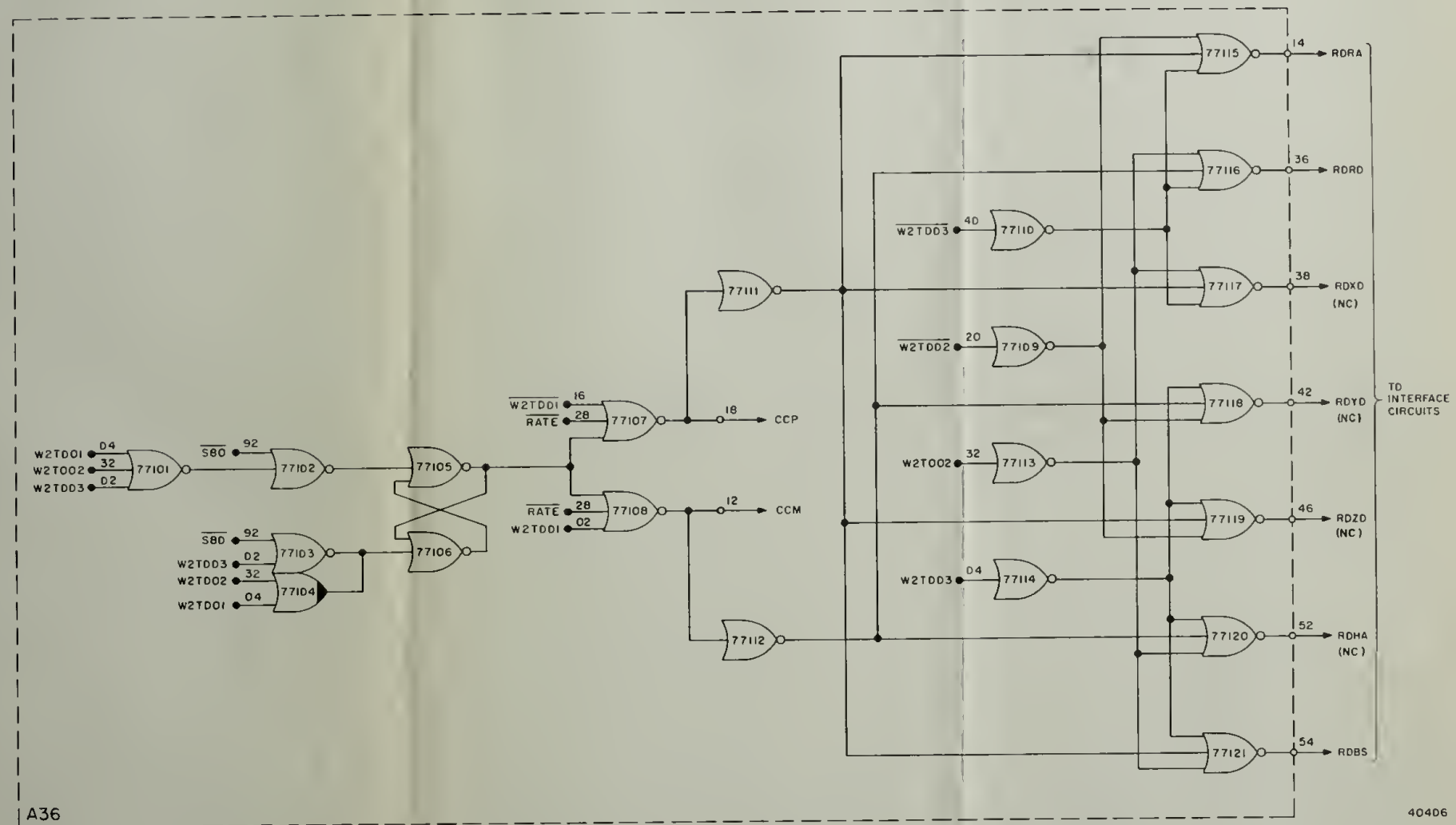
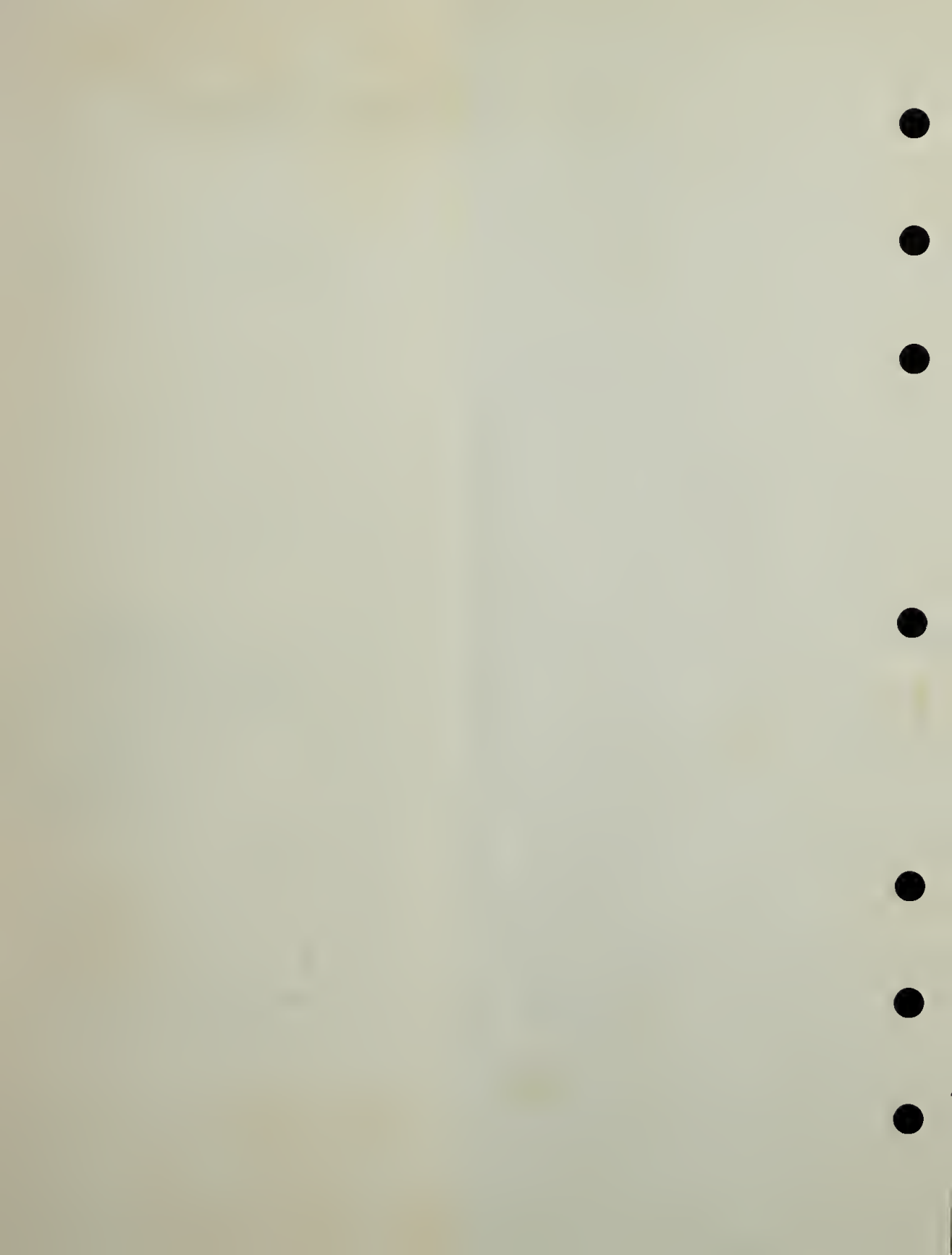


Figure 4-133. Rate 3 Control





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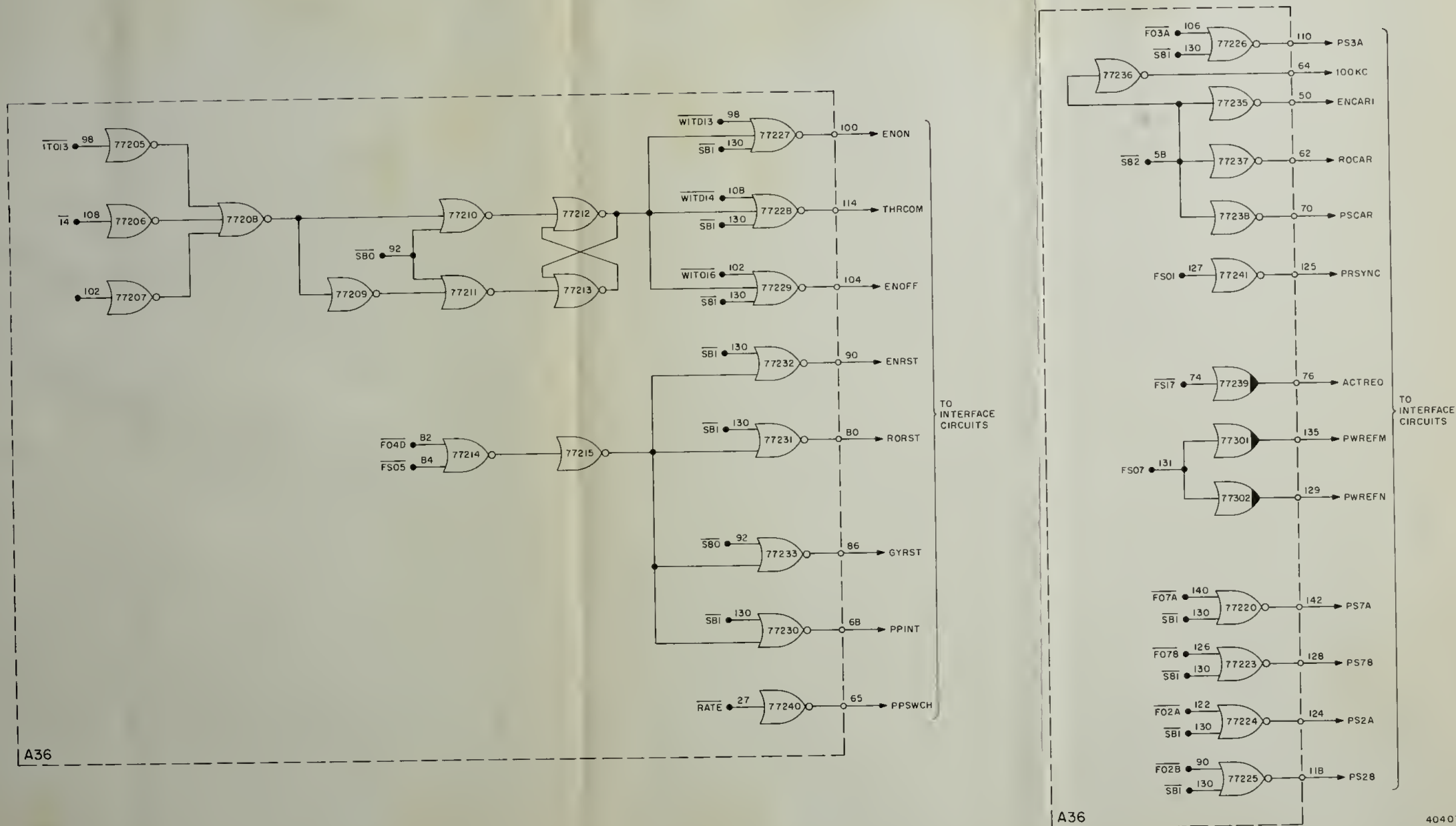


Figure 4-134. Continuous Pulse Control

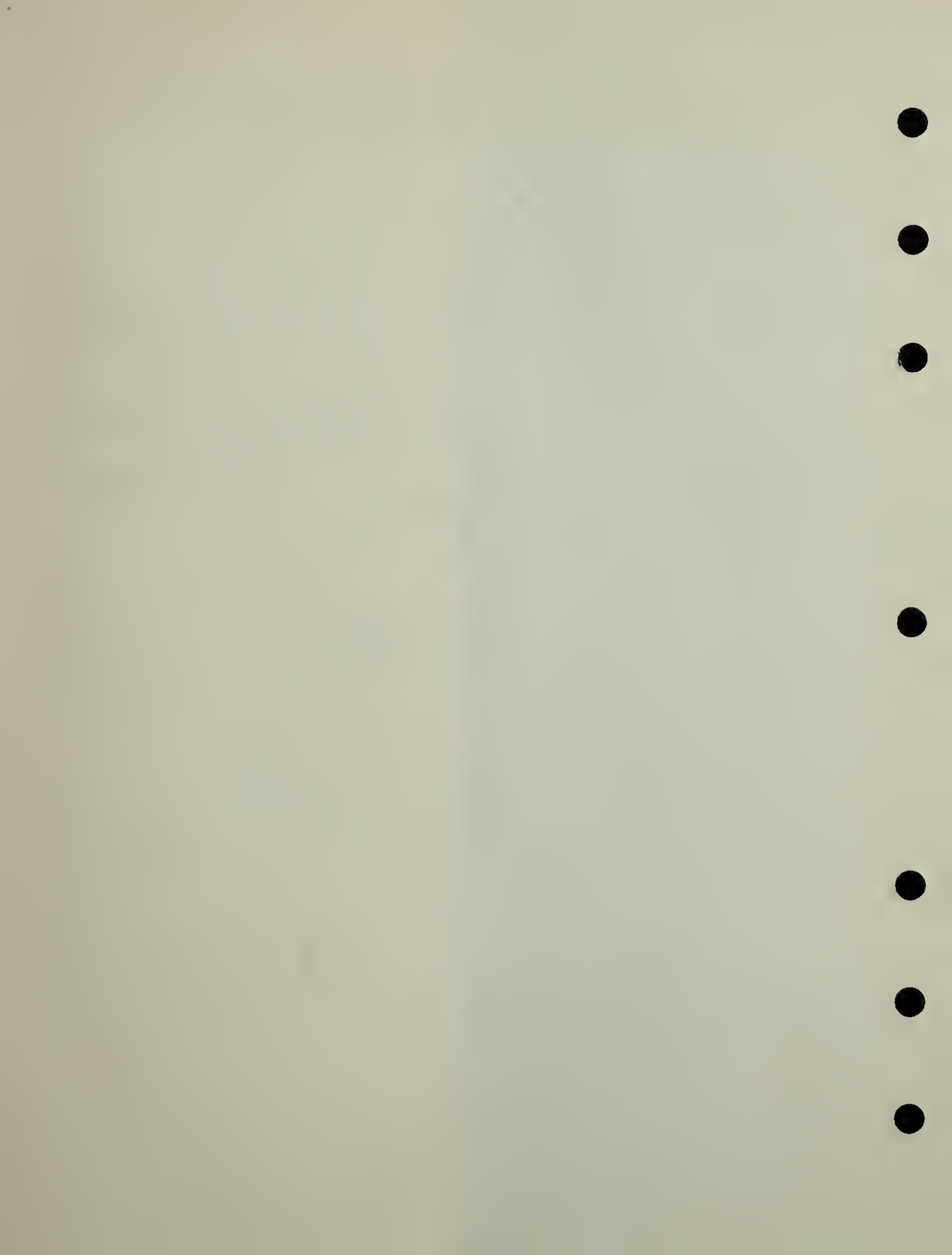


Table 4-X. Rate 3 Control Signals

Signal	Bit Position		
	3	2	1
RDRA	0	0	1
RDRD	0	1	0
RDXD	0	1	1
RDYD	1	0	0
RDZD	1	0	1
RDHA	1	1	0
RDBS	1	1	1

The reset signals to the spacecraft (ENRST), radar (RDRST), and gyros (GYRST), as well as the PIPA interrogate and PIPA switching signals, are 3-2-kpps outputs. This is the same repetition rate as gating signal RATE. The remaining continuous pulse outputs can be ascertained from figure 4-134.

4-8.4.8 Interface Modules (A19 and A39) and (A20 and A40). The interface modules are located at the front of AGC Tray A (logic tray) and provide interfacing between the AGC and the DSKY's, the spacecraft, and the remainder of the G & N system. All inputs to and outputs of the logic modules in the AGC are routed through the interface modules. Interface modules A19 and A39 are identical as are A20 and A40. Figure 4-135 through 4-138 illustrate the signal flow of all signals in and out of the AGC through the interface modules.

4-8.4.8.1 Interface Circuits. There are a total of five basic interface circuits that provide the proper input and output voltage levels and impedance matching between the AGC and other spacecraft systems. These five circuits are contained in the interface modules. There are three additional interface signal designations which are not interface circuits as such but do interface specific inputs and outputs between the AGC and the other subsystems of the G & N system. These three designations are a series resistor input/output configuration (R), switch closure (S) which involves the closing of relay

contacts in the power supply (tray B) to indicate power failure, and wire input/output lines (W) for routing primary power. All of the signals interfaced with the AGC have an alphanumeric code rather than the functional name when routed outside any particular subsystem. This code is used in the interface drawings and designates the interface circuit type, signal type, and number (for example, YE035).

The first letter designates the interface circuit type:

- D Discrete type input circuit
- K Discrete type input circuit
- R Resistor in series with signal
- S Switch Closure
- T Discrete type output circuit
- W Connecting Wire
- X Transformer coupled output circuit
- Y Transformer coupled input circuit

The second letter designates the type of signal:

- A Indicates the signal is under counter control; each output pulse is counted (for example, XA142)
- B Indicates the signal is under program control (for example, XB011)
- C Indicates the signal is continuous (for example, XC148)
- D Indicates the signal is a dc level (for example, RD086)
- E Indicates the signal goes to an IN bit or comes from an OUT bit (for example, DE158)
- G Indicates the signal goes to a counter (for example, YG132)

The digits indicate interface signals between specific systems:

- 001 - 100 AGC/Spacecraft Interface
- 100 - 200 AGC/G & N Interface
- 200 - 300 AGC/DSKY Interface
- 300 - 400 Navigation DSKY/G & N Interface
- 400 - 500 Main DSKY/Spacecraft Interface
- 500 - 600 AGC/CTS Interface
- 700 - 800 AGC/CTS Interface
- 800 - 900 AGC/Spacecraft Interface
- 900 - 1000 AGC/G & N Interface

The transformer input interface circuit (Y) consists of a pulse transformer and associated components which provide impedance matching and the voltage level necessary to operate the micrologic contained in the AGC. The transformer output interface circuit (X) consists of a pulse transformer driven by an input transistor circuit. It provides the required output impedance to match the circuits of the spacecraft and other subsystems of the G and N system. The filters (P) connected to the various output circuits filter the +13 volt input to these circuits. The K network and the D network consist of an RC filter, the output of which is applied directly to micrologic circuits in the AGC. The T network is simply a transistor driver circuit which buffers outputs from the AGC to the DSKY's.

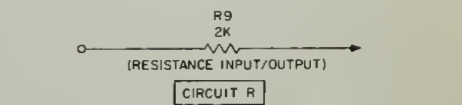
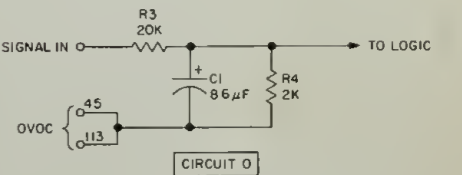
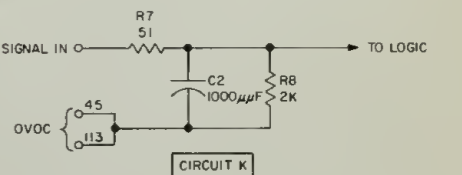
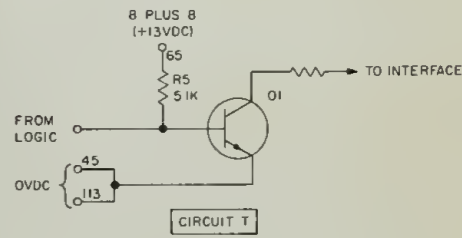
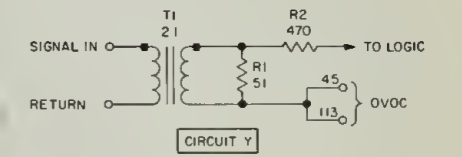
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Figure 4-135. Interface Module A19

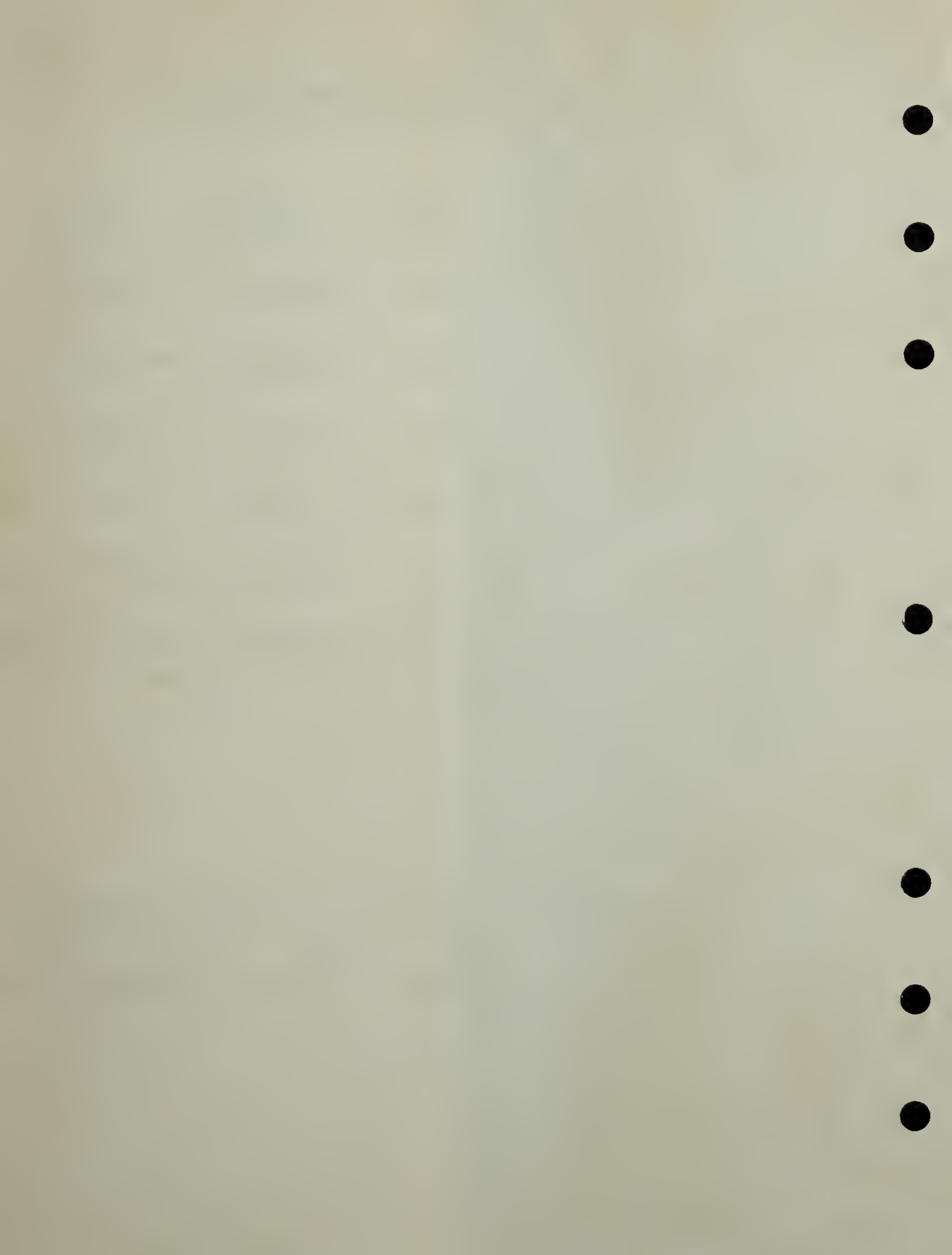


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Figure 4-136. Interface Module A39





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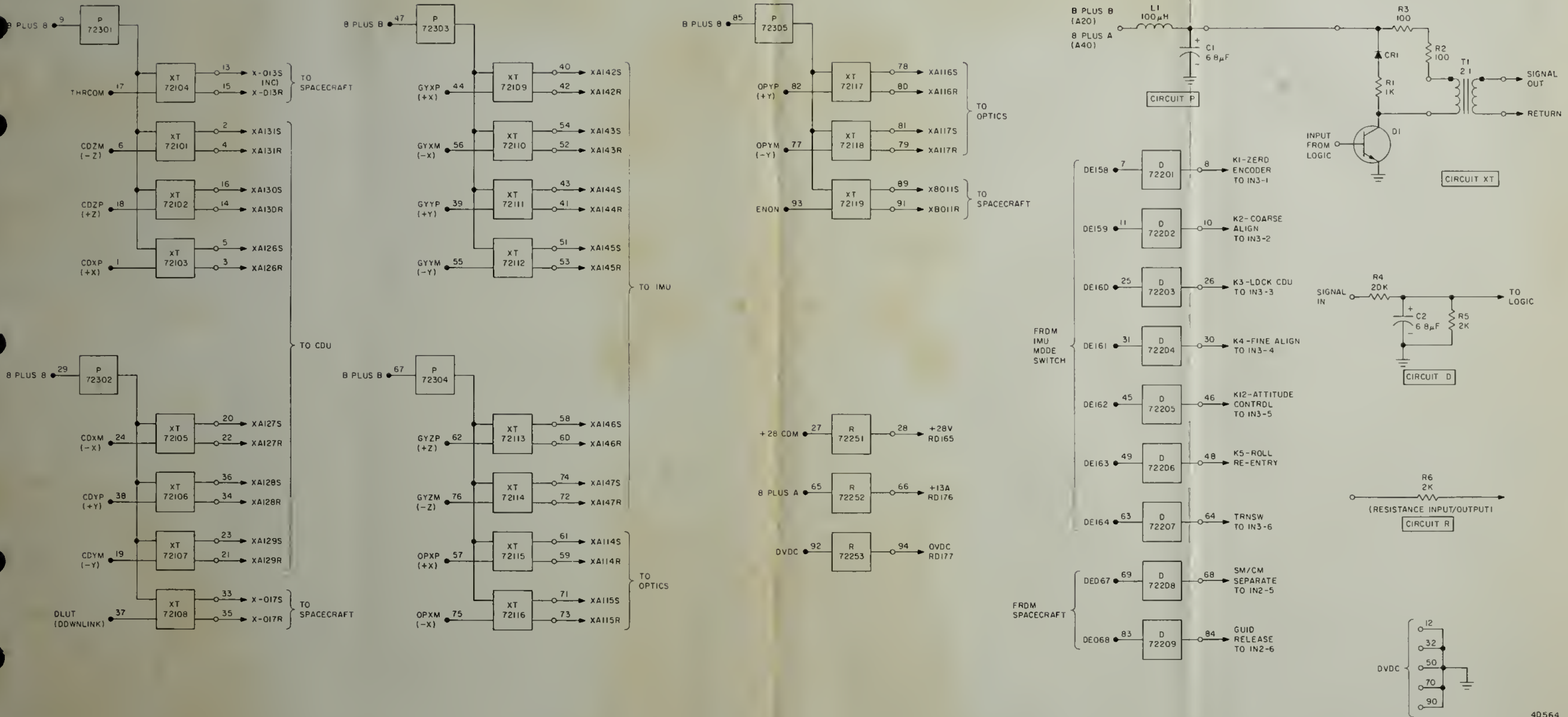
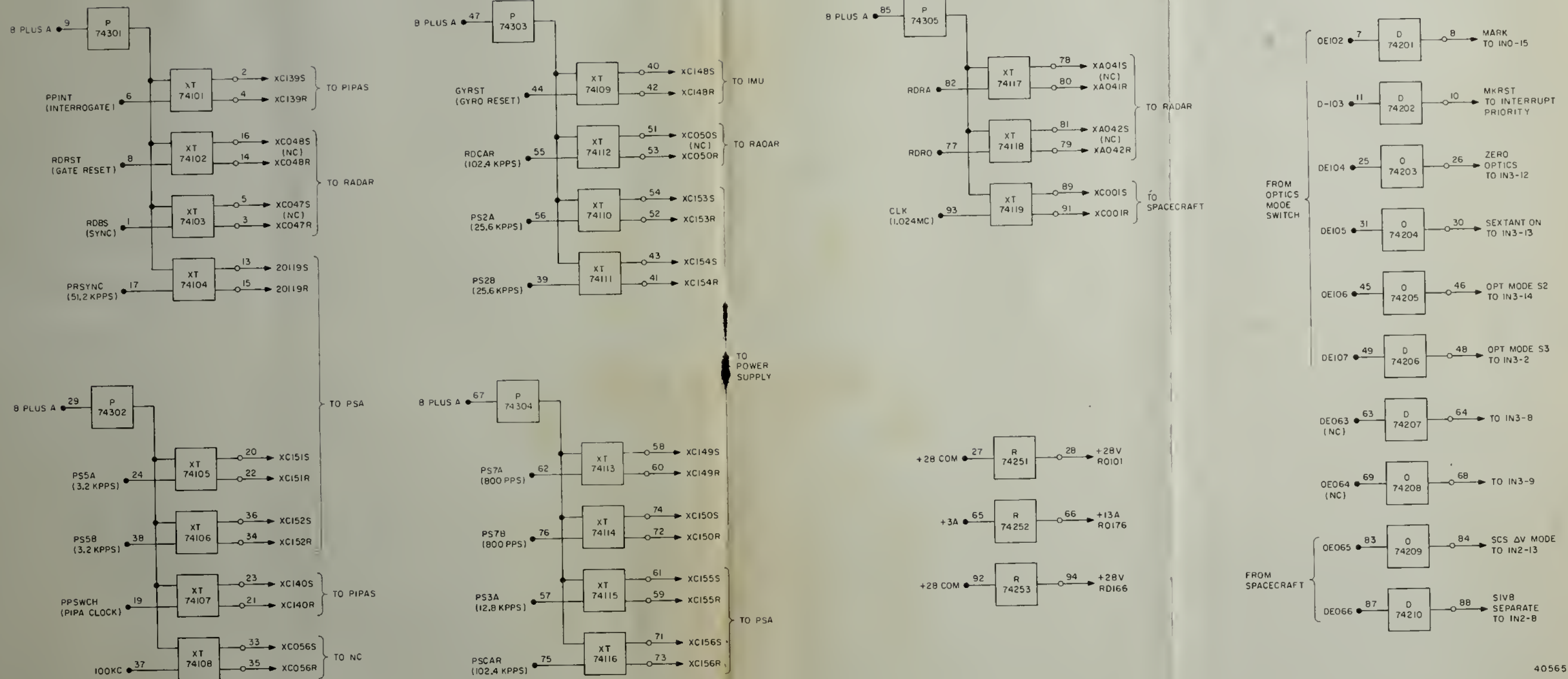


Figure 4-137. Interface Module A20

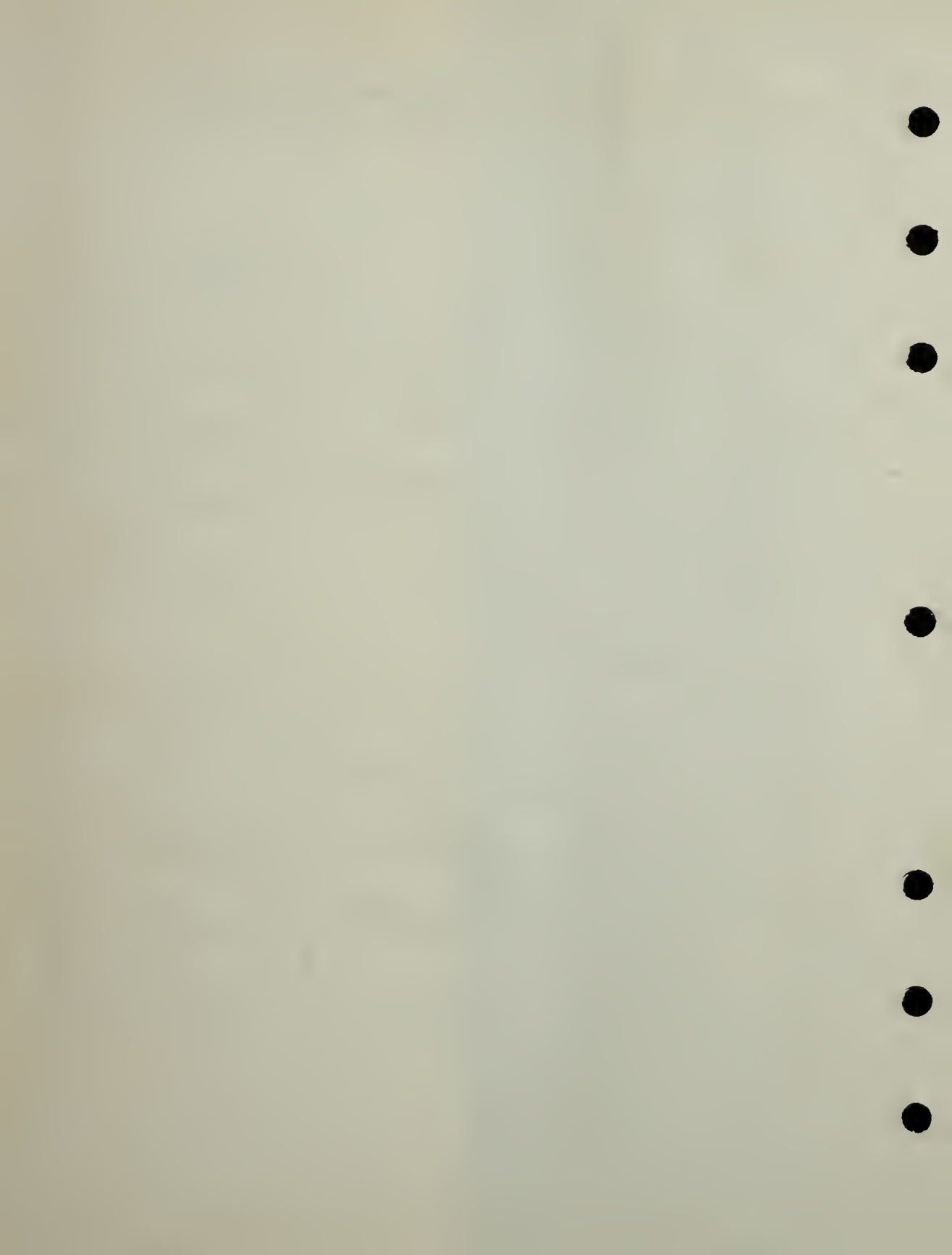


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Figure 4-138. Interface Module A40



The series resistor configuration (R) is used to common-switch inputs from the IMU and OSS and to provide short circuit protection for temperature monitoring signals and some outputs from the power supply. There are only two switch closure lines and these control the AGC power fail indication from the power supply to the condition annunciator and main panel fail lights (SF157 and SF26 respectively). The wire input/output lines (W) provide primary power connections, B+ voltages, and ground and shielding connections.

4-8.5 PRIORITY CONTROL. Priority control consists of counter priority control and interrupt priority control. Counter priority control initiates action to update counters. The counters are (in the order of priority in which they are updated) in erasable memory locations 0034 through 0057. Interrupt priority control transfers AGC control to one of six interrupt (RUPT) transfer subroutines that initiate programs which deal with conditions such as keycode inputs from the DSKY's. These subroutines are, in order of priority, T3RUPT, RPT2, T4RUPT, KEYRUPT, UPRUPT, and DOWNRUPT.

4-8.5.1 Counter Priority Control Functional Description. Counter priority control (figure 4-139) receives incremental pulses for 20 counters. Seven counters require only an increment operation, eleven require either an increment or a decrement operation, and two require either a shift or a shift-and-add-one operation. Counter instruction PINC accomplishes increment operations, MINC accomplishes decrement operations, SHINC accomplishes shift operations, and SHANC accomplishes shift-and-add-one operations. Counter priority control commands the sequence generator to execute instruction OINC or LINC when read or load requests are received from the CTS. Instruction OINC allows the content of an addressed location to be displayed on a CTS panel. Instruction LINC allows data to be entered into an addressed location. The CTS provides addresses to the write amplifiers in the central processor in conjunction with these two instructions.

Twenty priority cells, C01 through C20, are located in counter priority control. Each consists of one or more input flip-flops, request transfer gates, and a request flip-flop, all connected in a priority chain. The input flip-flops are grouped according to the types of inputs received for the various counters. The input flip-flops in group A receive pulses which initiate incrementing (PINC) operations only. The input flip-flops in group B receive pulses which initiate incrementing (PINC) or decrementing (MINC) operations. There are two input flip-flops in each cell of group B for each of the counters that can be incremented or decremented. The input flip-flops in group C receive pulses which initiate shift (SHINC) or shift-and-add-one (SHANC) operations. The counters associated with the group C input flip-flops store the results of serial-to-parallel conversions.

4-8.5.1.1 PINC Command Generation. Only PINC commands are generated when incremental pulses are supplied to the group A input flip-flops. Inputs to this group of flip-flops initiate incrementing operations for the time and output rate counters.

The main time counter consists of the TIME 1 and TIME 2 counters (cells CO2 and CO3). The main time counter keeps track of real time and is incremented by the 100 pps output of the TIME 1 and 3 counter gate. The 16 bit TIME 1 counter has a capacity of 163.83 seconds and, at overflow, initiates signal  $\overline{OVF}$  in the sequence generator. This signal, coincident with  $\overline{WOVR}$  from the sequence generator, enables the overflow test gate. The output of this gate, coincident with the TIME 1 counter address that is still present, enables the TIME 2 counter gate which sets the TIME 2 input flip-flop.

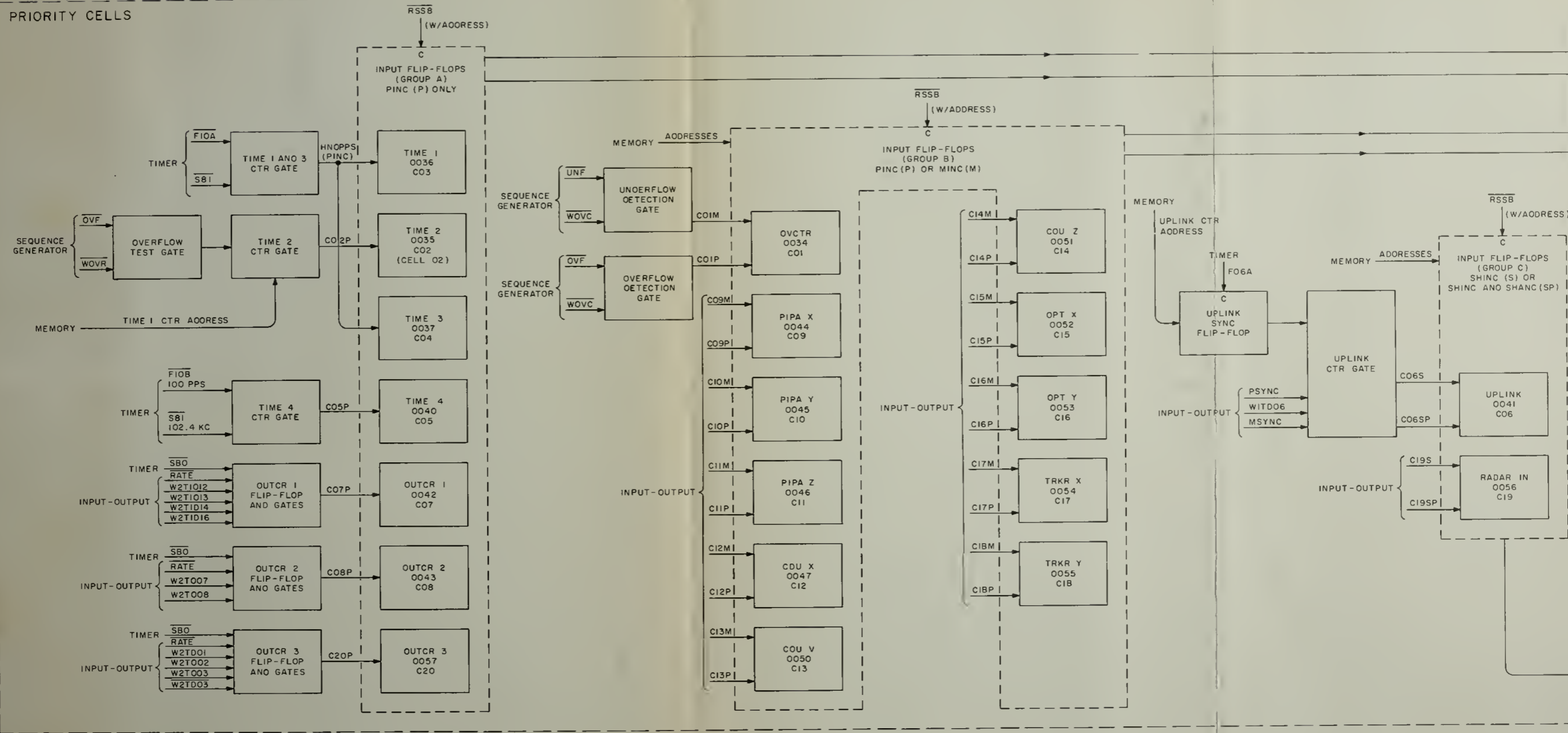
The TIME 3 and TIME 4 counters initiate waitlist and display interrupt requests used in the interrupt priority control. Program operations initially set these counters to a predetermined value. The counters are then incremented at 100 pps until overflow occurs, at which time control is transferred by interrupt priority control to the proper RUPT transfer subroutine.

An output from each group A input flip-flop controls a corresponding request transfer gate in a cell. When enabled by an input flip-flop that is set, each request transfer gate supplies a set input to the request flip-flop in the cell at time 9. A priority chain interconnects all request flip-flop outputs. Within the priority chain, a request flip-flop that is set inhibits the outputs of all lower-priority request flip-flops. Therefore, the highest-priority cell that contains information controls the address generator. The resultant counter address is transferred to register S in memory at action 1 of a counter instruction. Control pulse RSCT from the sequence generator transfers the address (RSCT is produced when signal  $\overline{NC13}$  is generated). Signal  $\overline{NC13}$ , the output from the increment control flip-flop, occurs when signal  $\overline{CTROR}$  enables the CTROR inhibit gate.

The priority chain produces CTROR from the priority blocking gates whenever any request flip-flop is set. Signal  $\overline{CTROR}$  and inhibit signals MNHNC, OINC, and LINC control the CTROR inhibit gate. If none of the inhibiting signals is present,  $\overline{CTROR}$  sets the increment and decrement control flip-flops at time 12. Signals INKL and  $\overline{INKL}$  from the incrementing flip-flop inhibit execution of the next subinstruction by the sequence generator. Signal  $\overline{INKL}$  also conditions the reset strobe generator so that the reset signal  $\overline{RSSB}$  is produced at the following time 9. Signal  $\overline{RSSB}$ , in conjunction with the address of the counter being controlled, resets the input and request flip-flops.

A PINC counter command is produced by the priority chain whenever a request to increment the TIME or OUTCTR counters is being processed. The address request signal is supplied to the address generator, and a command request signal is supplied to the command transfer gates. The applicable command transfer gate is enabled at time 2, and sets the PINC command flip-flop. The sequence generator receives PINC at time 2, and this signal remains during execution of the PINC counter instruction. At time 12 of the PINC counter instruction, the clear gate is enabled, clear signal CLCS is produced, and the PINC command flip-flop is reset.

PRIORITY CELLS



APOLLO GUIDANCE AND NAVIGATION SYSTEM

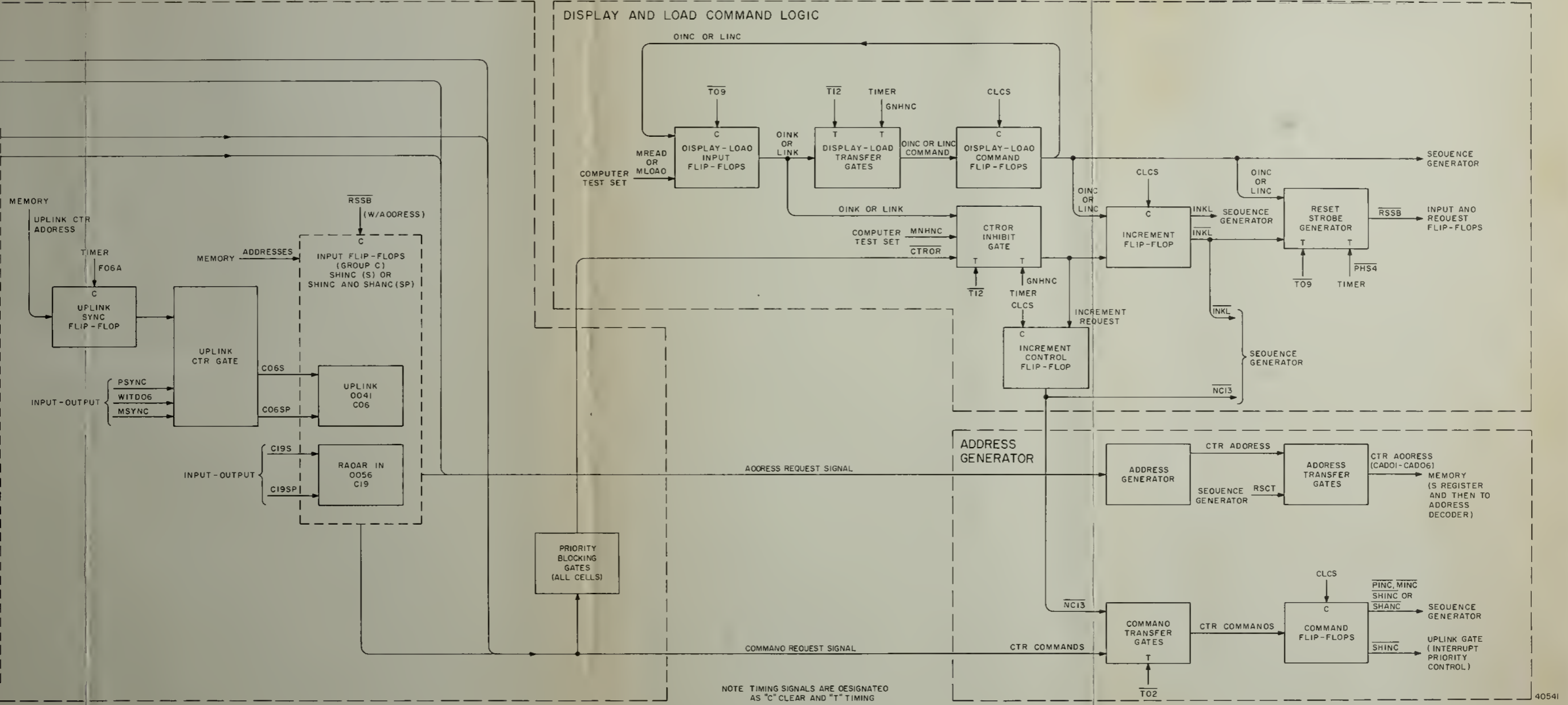
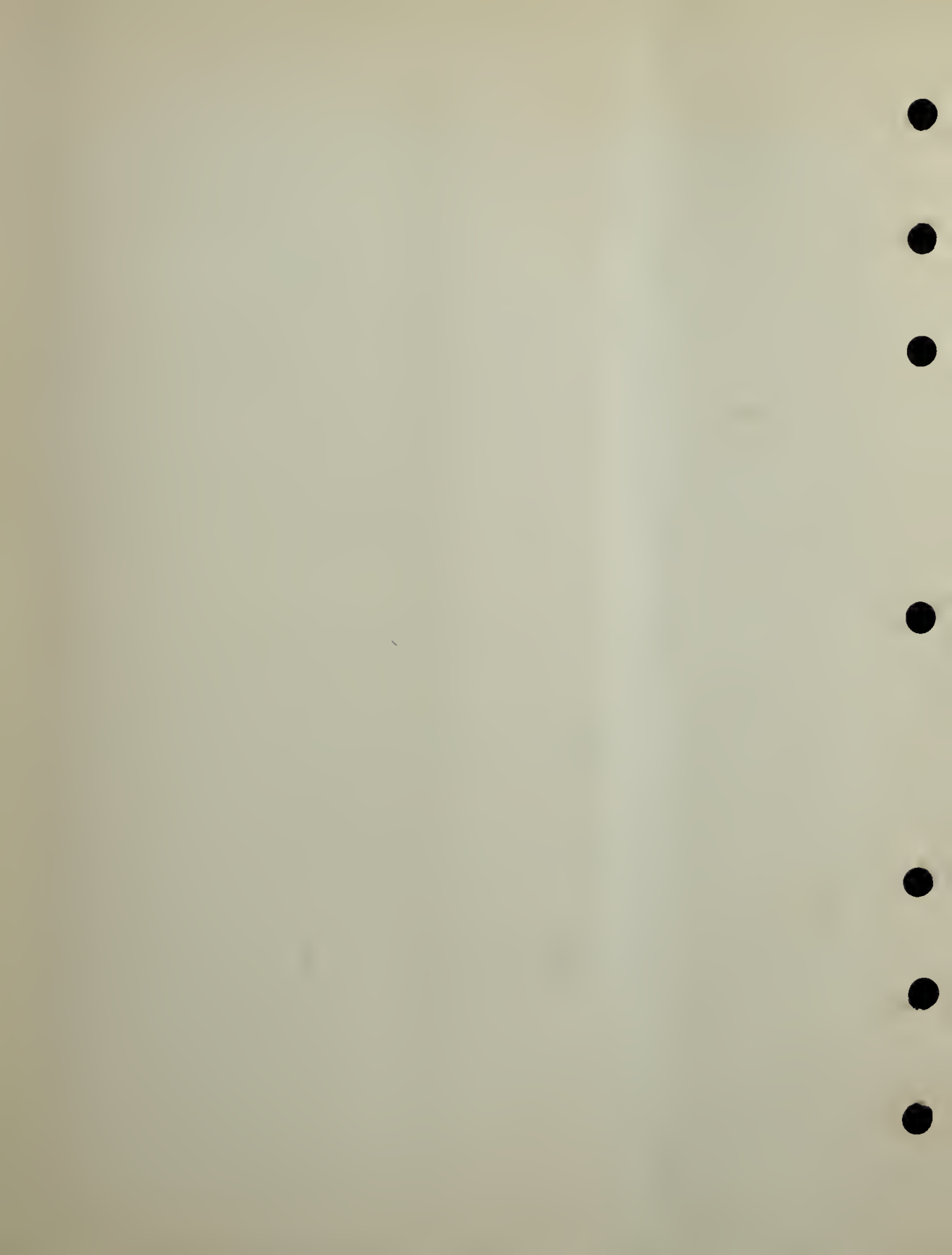


Figure 4-139. Counter Priority Control, Functional Diagram





4-8.5.1.2 PINC and MINC Command Generation. PINC and MINC commands are generated when incremental pulses are supplied to the group B input flip-flops. Inputs to the group B input flip-flops initiate incrementing and decrementing operations for the overflow counter and the input counters.

The overflow counter is incremented or decremented after the execution of machine instruction AD K or SU K if overflow or underflow occurred during the instruction. The input counters keep track of the incremental pulses supplied by the PIPA, CDU, OPT, and TRKR. Control pulses  $\overline{UNF}$ ,  $\overline{OVF}$ , and  $\overline{WOVC}$  from the sequence generator control the underflow and overflow detection gates. These gates provide incremental pulses which initiate MINC (pulse C01M) and PINC (pulse C01P) counter instructions for the overflow counter. Incremental pulses from the input-output control the remaining group B input flip-flops.

The PINC or MINC counter commands require an address from memory. This address occurs after the address of the overflow or input counter is supplied to memory through the address transfer gates. The address from memory and an output from the applicable input flip-flop then enable a gate to produce a PINC or MINC counter command input to the command transfer gates. This counter command then sets a command flip-flop, and either a  $\overline{PINC}$  or a  $\overline{MINC}$  signal is supplied to the sequence generator. This signal, along with  $\overline{INKL}$  and  $\overline{NC13}$ , causes the execution of the applicable counter instruction.

4-8.5.1.3 SHINC and SHANC Command Generation. The SHINC and SHANC commands are generated when incremental pulses are supplied to the group C input flip-flops. Inputs to the group C input flip-flops initiate shift (SHINC) or shift-and-add-one (SHANC) counter instructions for the UPLINK and RADAR IN counters.

The UPLINK counter gate receives incremental pulses PSYNC and MSYNC from the input-output control. The gate also receives inhibiting signals from the uplink sync flip-flop and input-output control. The inhibiting signal from the input-output control is WTD06, the block uplink bit of register OUT 1. The uplink sync flip-flop is set by the uplink counter address supplied from memory and reset by timing signal F06A.

The SHINC and SHANC counter commands from the group C input flip-flops are produced when a flip-flop is set and the proper address is present from memory. These counter commands are supplied also to the command transfer gates. Counter command SHANC sets the SHANC command flip-flops; counter command SHINC sets the SHINC command flip-flop.  $\overline{SHINC}$  or  $\overline{SHANC}$  signals from the command flip-flops are supplied to the sequence generator at time 2, when the command transfer gates are enabled.

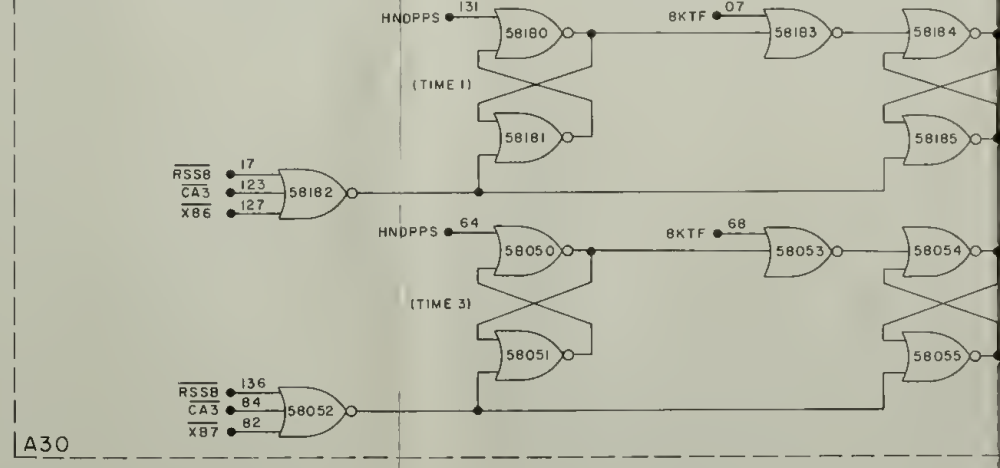
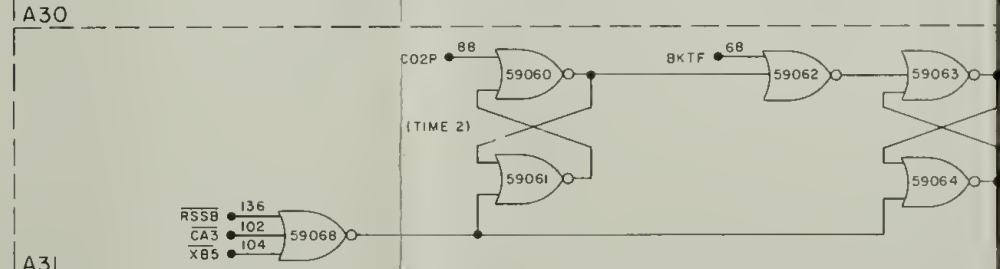
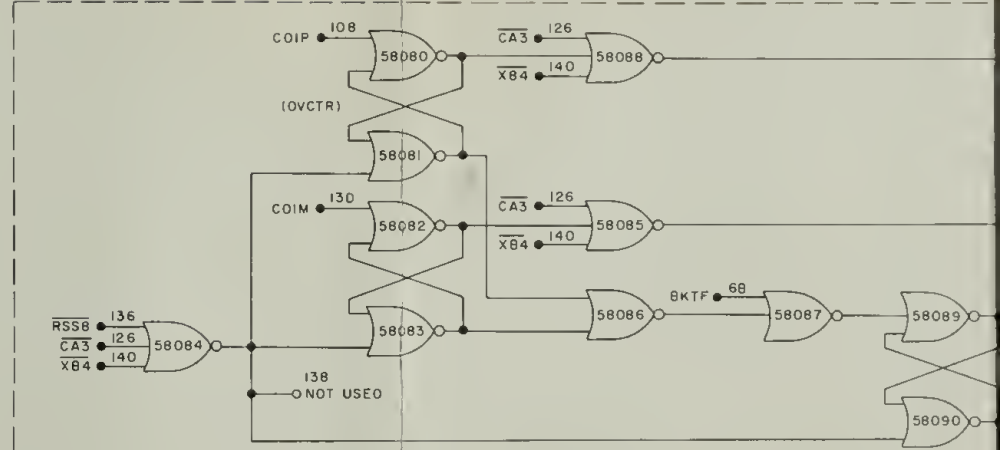
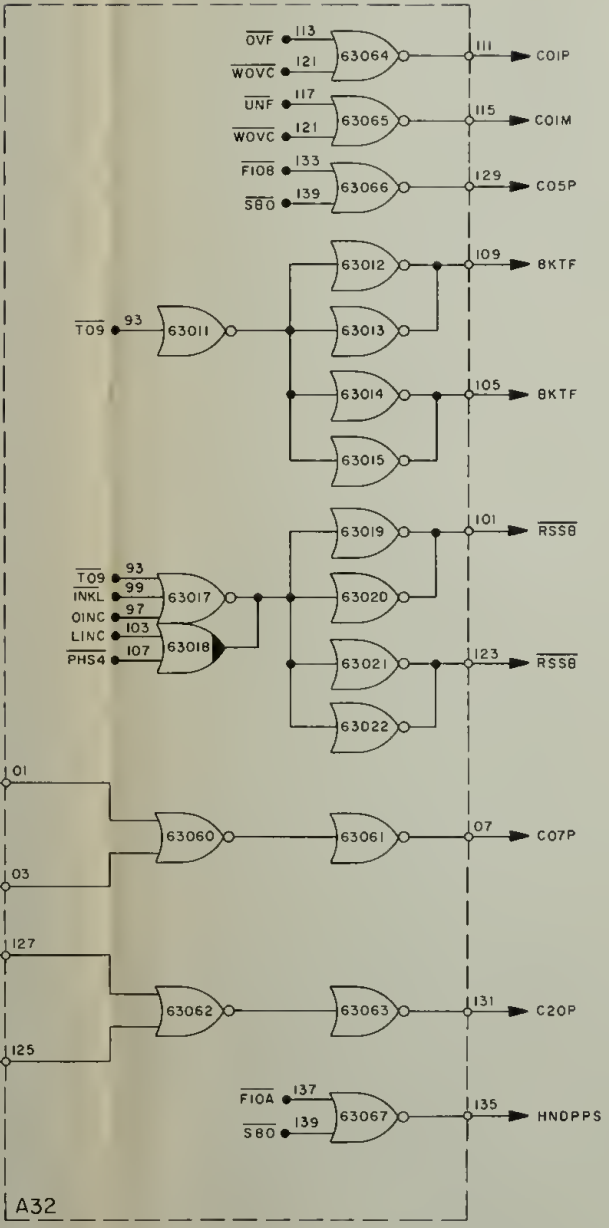
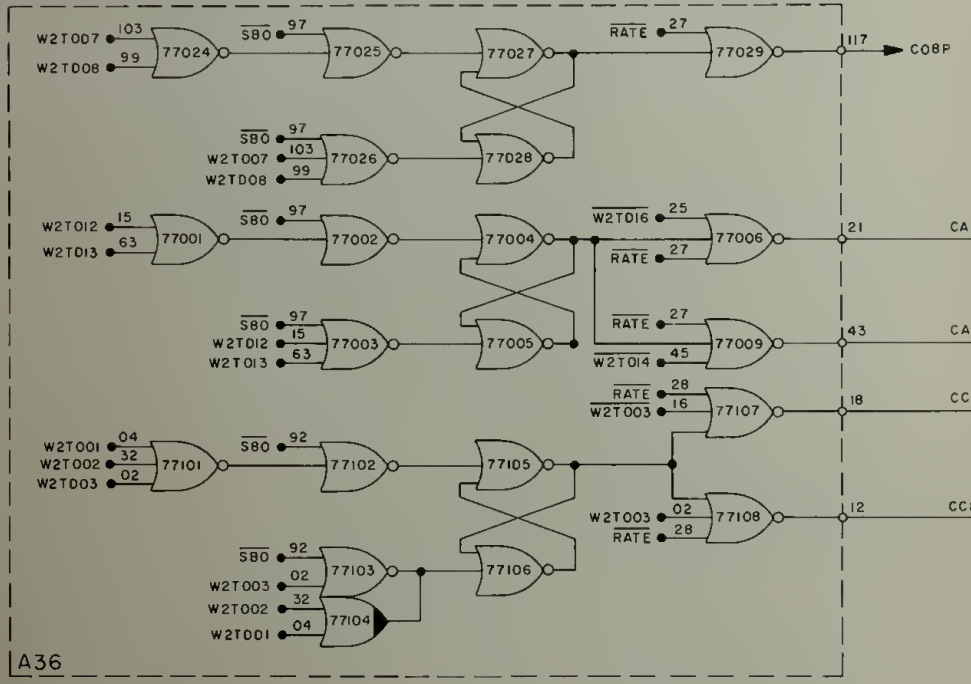
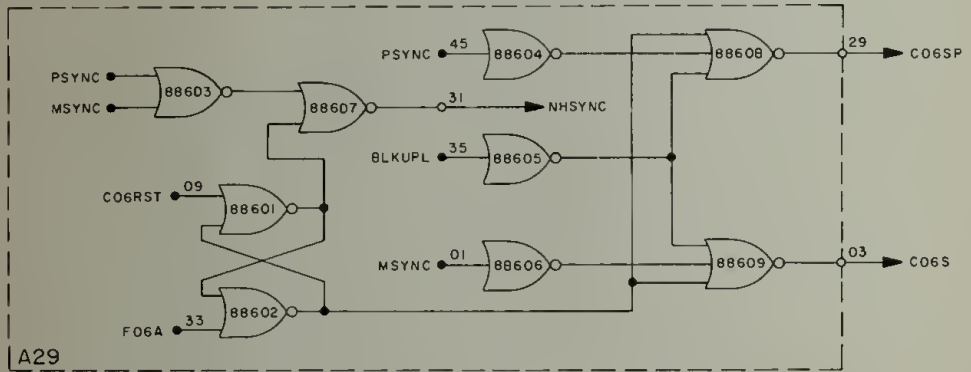
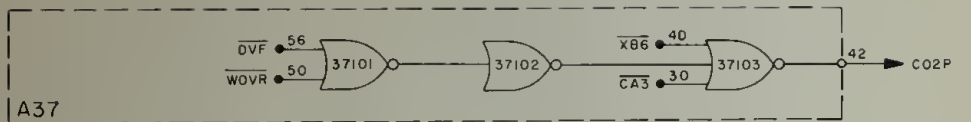
4-8.5.2 Counter Priority Control Detailed Description. Counter priority control (figure 4-140) contains 20 priority cells which comprise the priority chain. Each cell is associated with 1 of the 20 counters in memory; each counter being an addressable 16-bit register. The cells (C01-C20) consist of one or more input flip-flops for receiving incremental inputs, request transfer gates, and request flip-flops for transferring the incremental pulses to the associated counter.

The input flip-flops of counter priority control are divided into three groups. Group A contains 7 input flip-flops and receives incremental pulses that initiate plus increment (PINC) operations. Group B contains 22 input flip-flops that initiate either PINC or decrementing (MINC) operations. Group C contains 7 input flip-flops that initiate shift (SHINC) or shift-and-add-one (SHANC) operations. The priority chain determines which incremental input has highest priority and initiates a PINC, MINC, SHINC, or SHANC operation.

Counter priority control updates counters in locations 0034 through 0057 of erasable memory. The purpose of each counter is outlined in table 4-XI. Only the time counters at locations 0035, 0036, 0037, and 0040 and output counters at 0042, 0043, and 0057 are incremented by the outputs from group A flip-flops. Input counters (0044 through 0047 and 0050 through 0055) are incremented or decremented by the outputs from the group B flip-flops. The UPLINK counter (0041) and the RADAR IN counter (0056) receive SHINC and SHANC pulses from the outputs of the group C flip-flops. Since the input flip-flops of each group receive signals that perform essentially the same operation in each priority cell, the signal flow for only one of each group of input flip-flops will be discussed.

4-8.5.2.1 Incrementing. The pulses supplied to the group A input flip-flops result in a PINC command. This command increments by one the counter specified by the address generator (figure 4-141). As an example, the execution of a PINC counter command is discussed for the TIME 2 counter at location 0035 in erasable memory.

When the TIME 1 counter overflows, signals  $\overline{\text{OVF}}$  and  $\overline{\text{WOVR}}$  from the sequence generator enable the overflow test gate (37101). The output from this gate is inverted and enables the TIME 2 CTR gate coincident with the address of the counter of higher priority previously updated (TIME 1 counter, address 0036). Signal C02P, produced by gate 37103, sets the input flip-flop (FF59060-59061). The output from the flip-flop conditions the request transfer gate (59062). The second input to this gate, BKTF (block transfer), enables at time 9 and sets the request transfer flip-flop (FF59063-59064). The set and reset outputs from this flip-flop are applied to gates 59066 and 59065, respectively. Gate 59065 produces output C02A, which is applied to the address generator and the counter command logic (figure 4-142).



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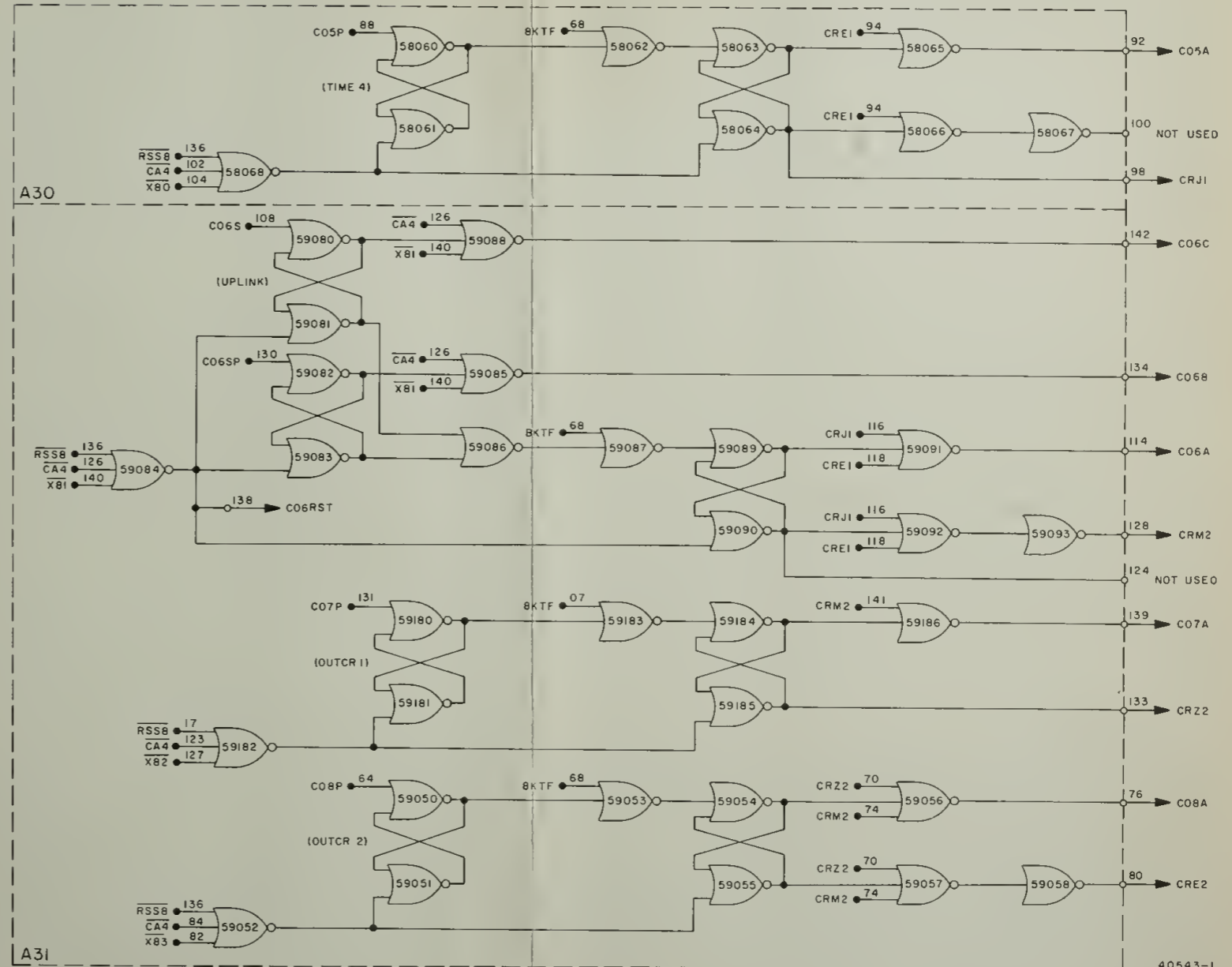
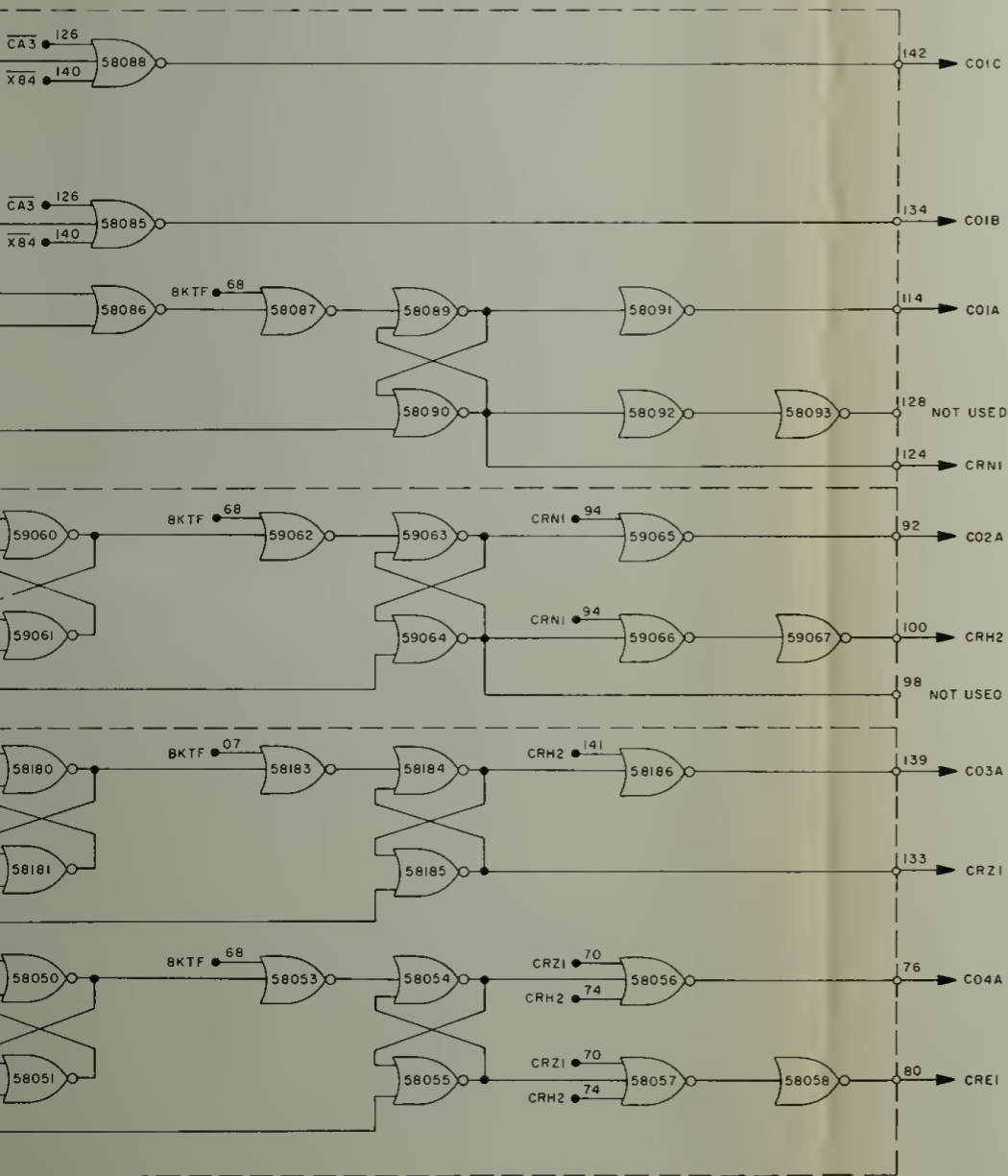
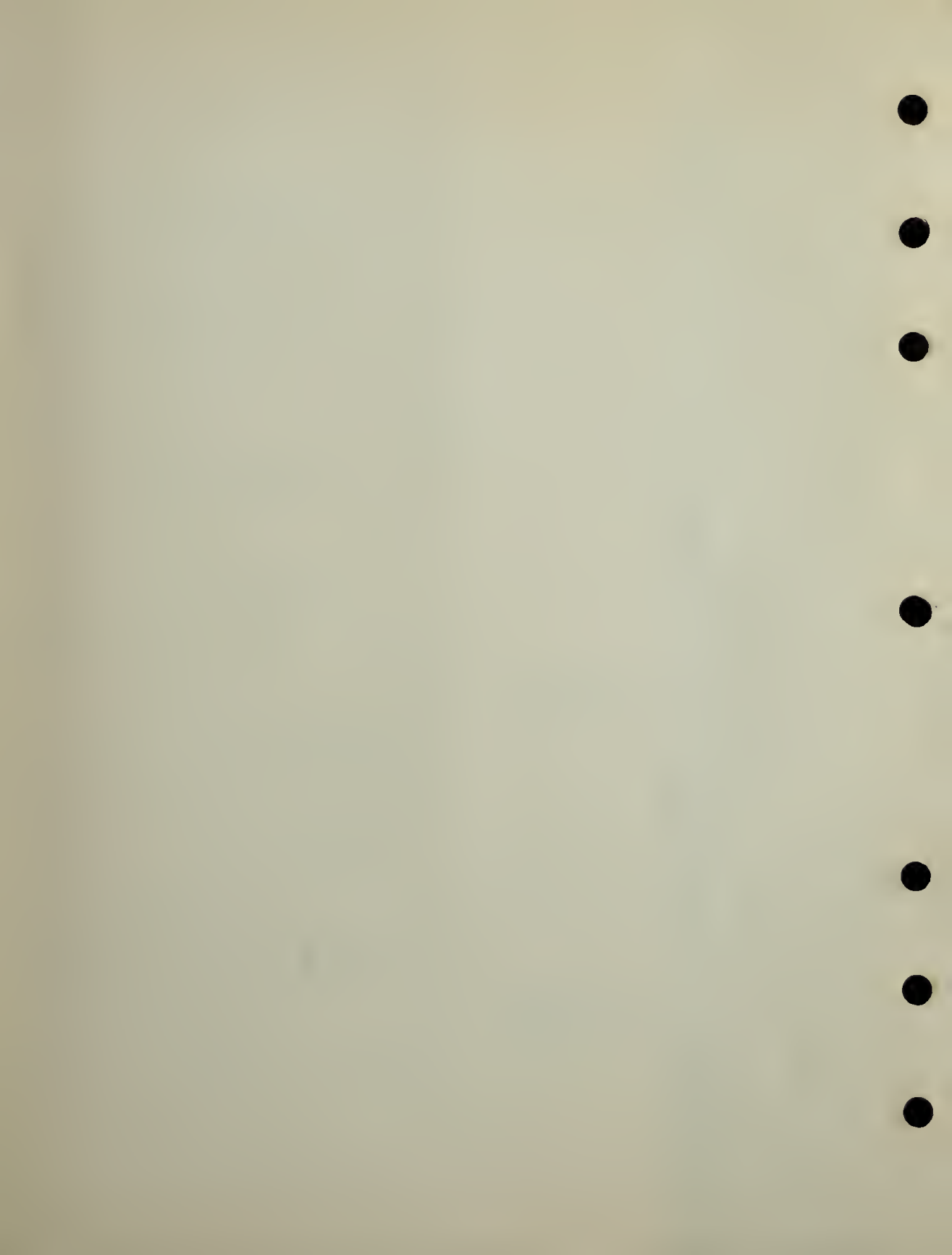
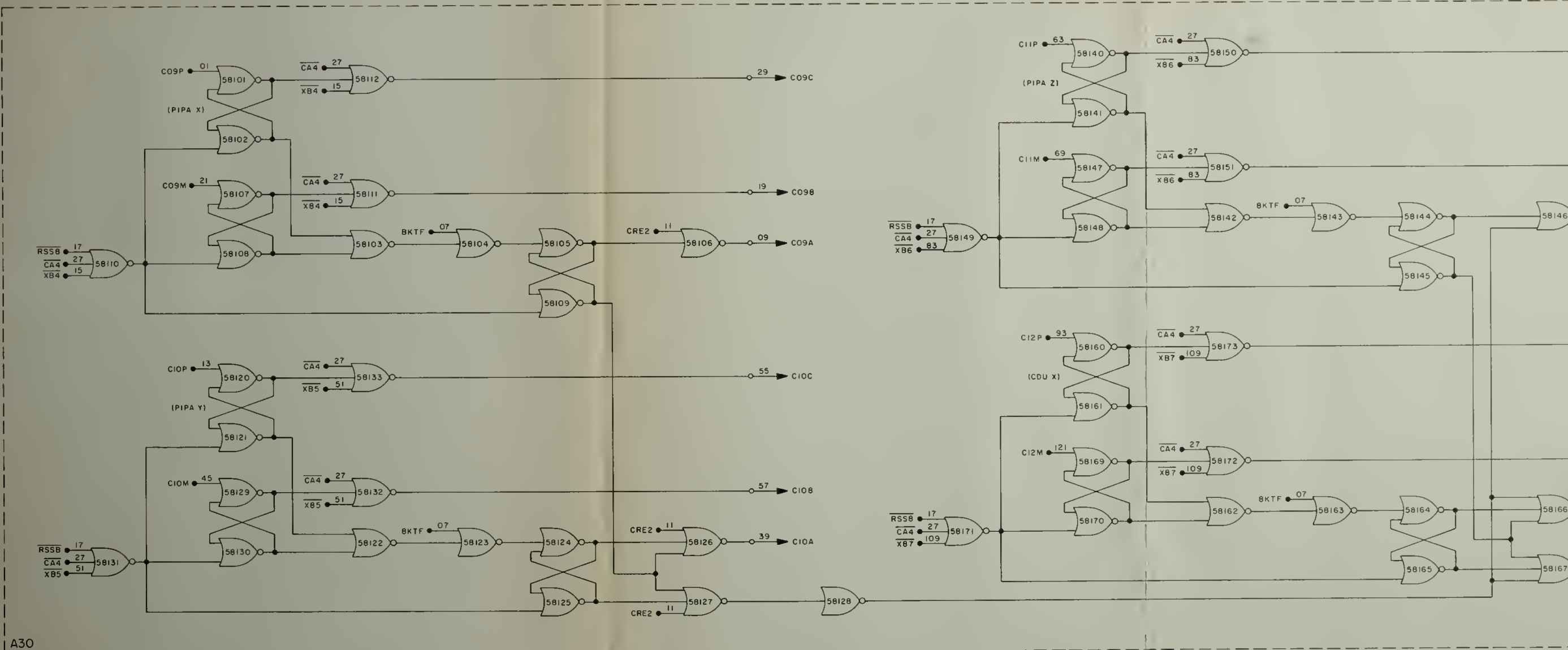


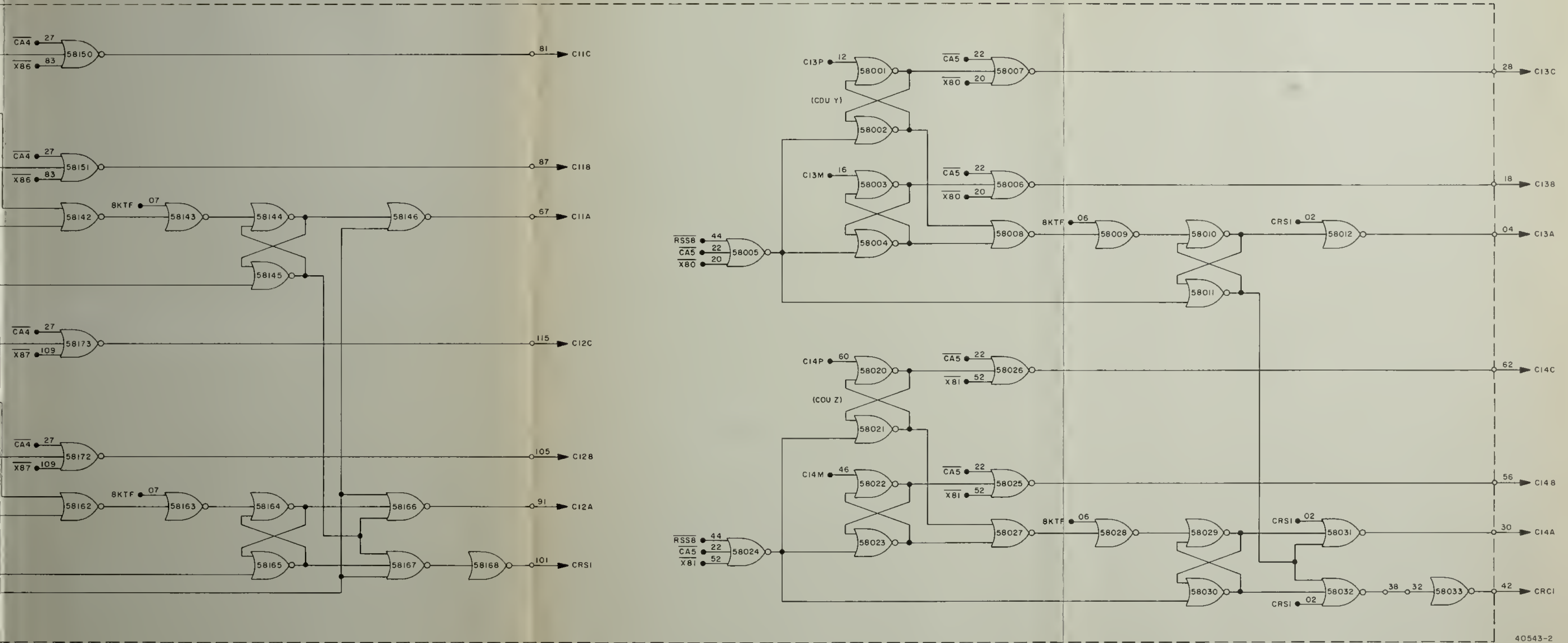
Figure 4-140. Counter Priority Control  
(Sheet 1 of 3)





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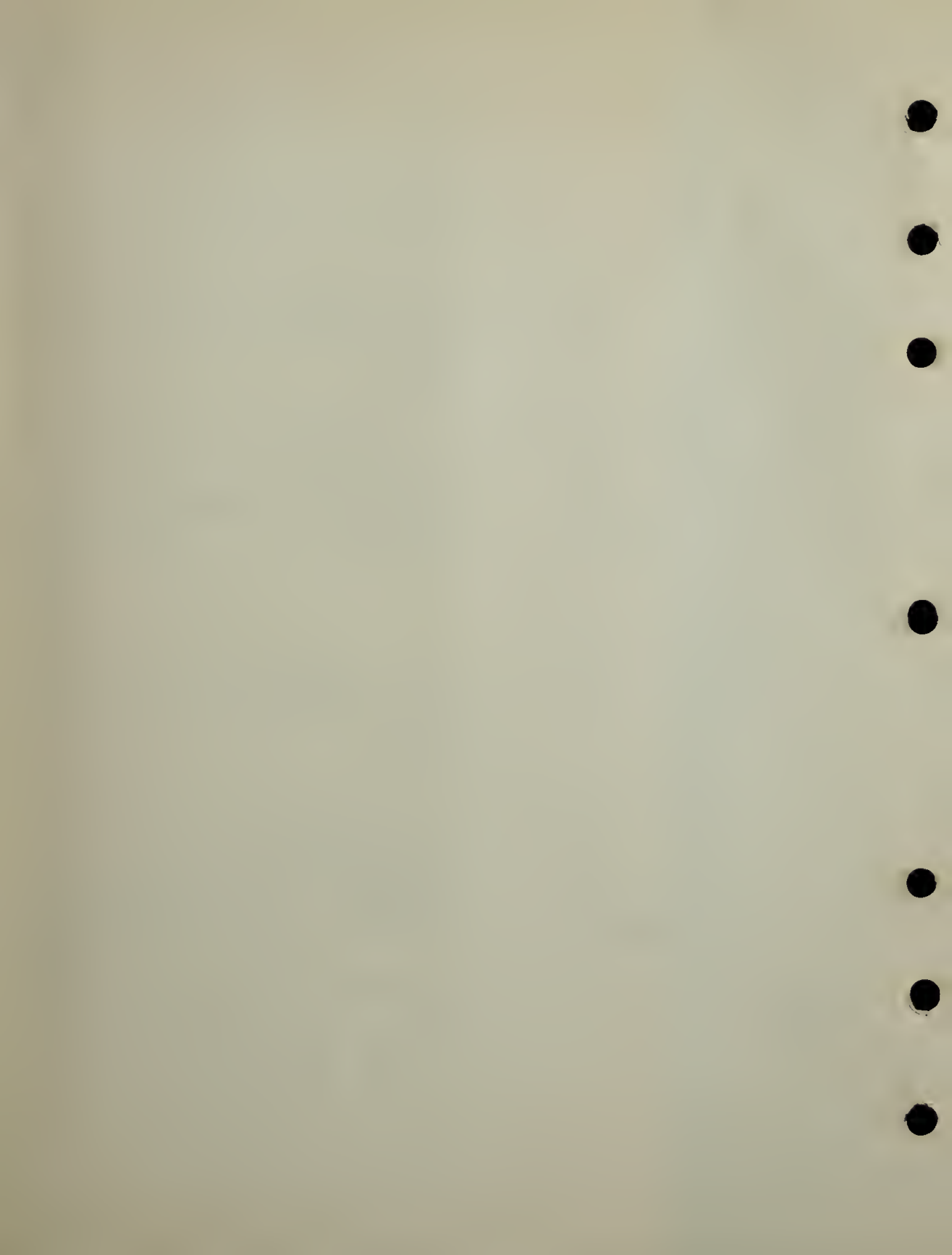
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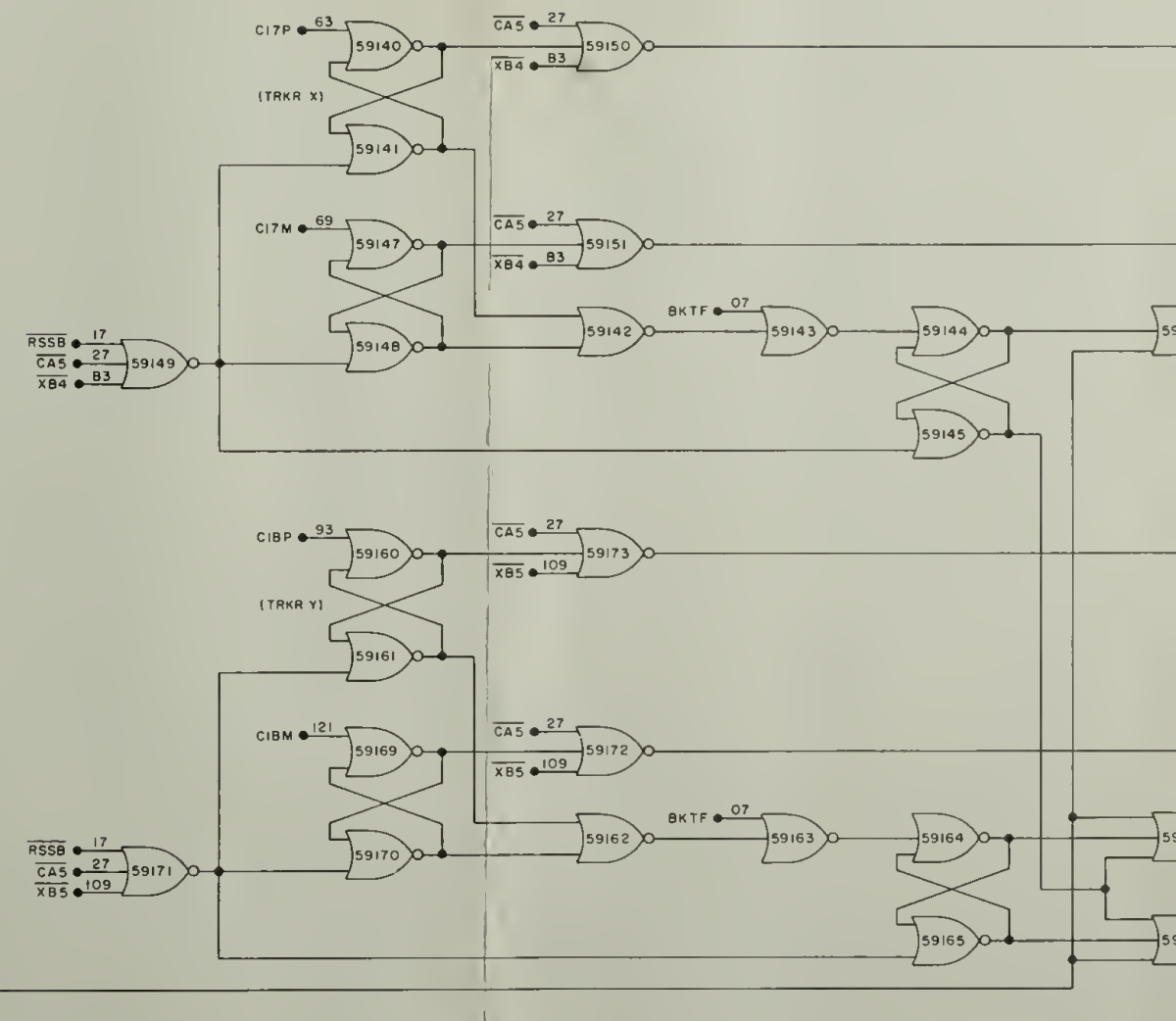
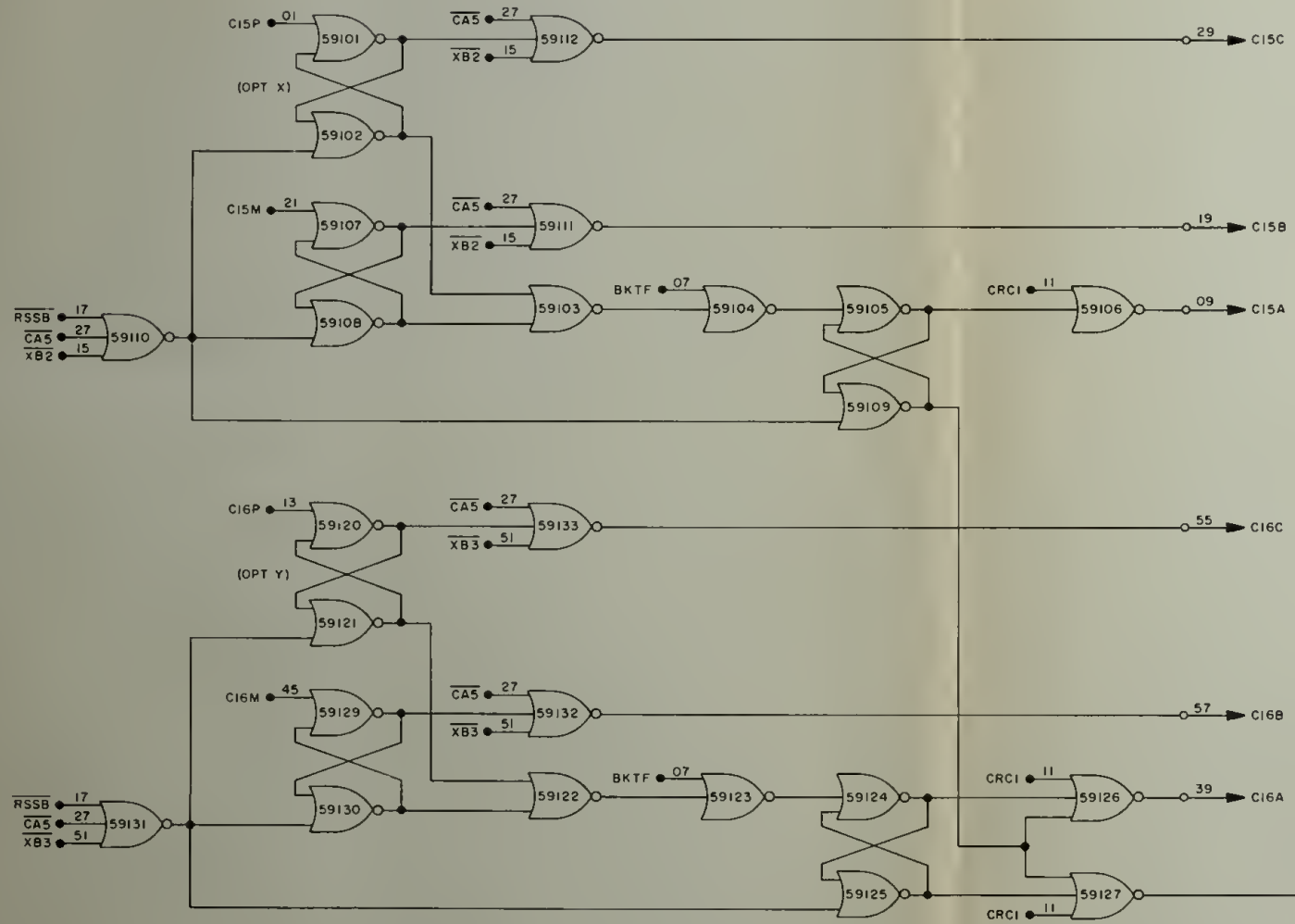


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Figure 4-140. Counter Priority Control  
(Sheet 2 of 3)







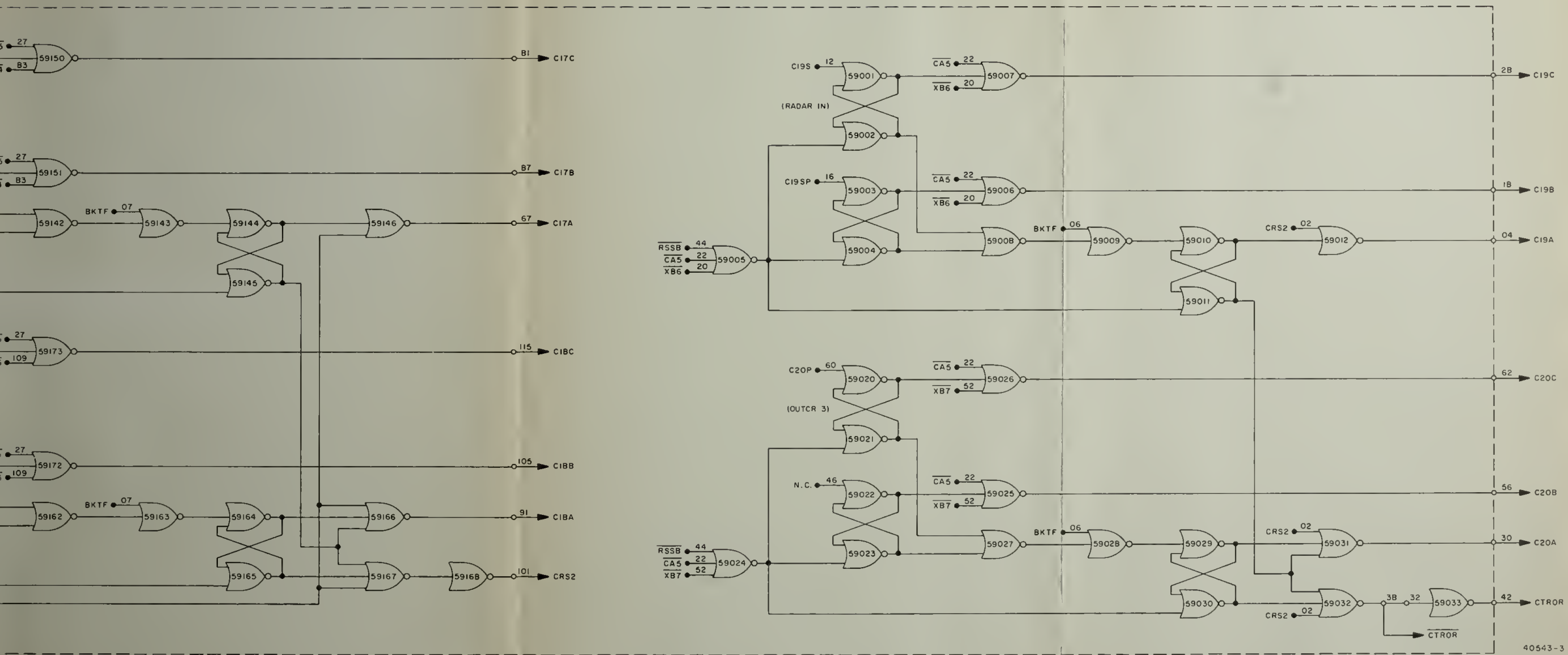


Figure 4-140. Counter Priority Control  
(Sheet 3 of 3)

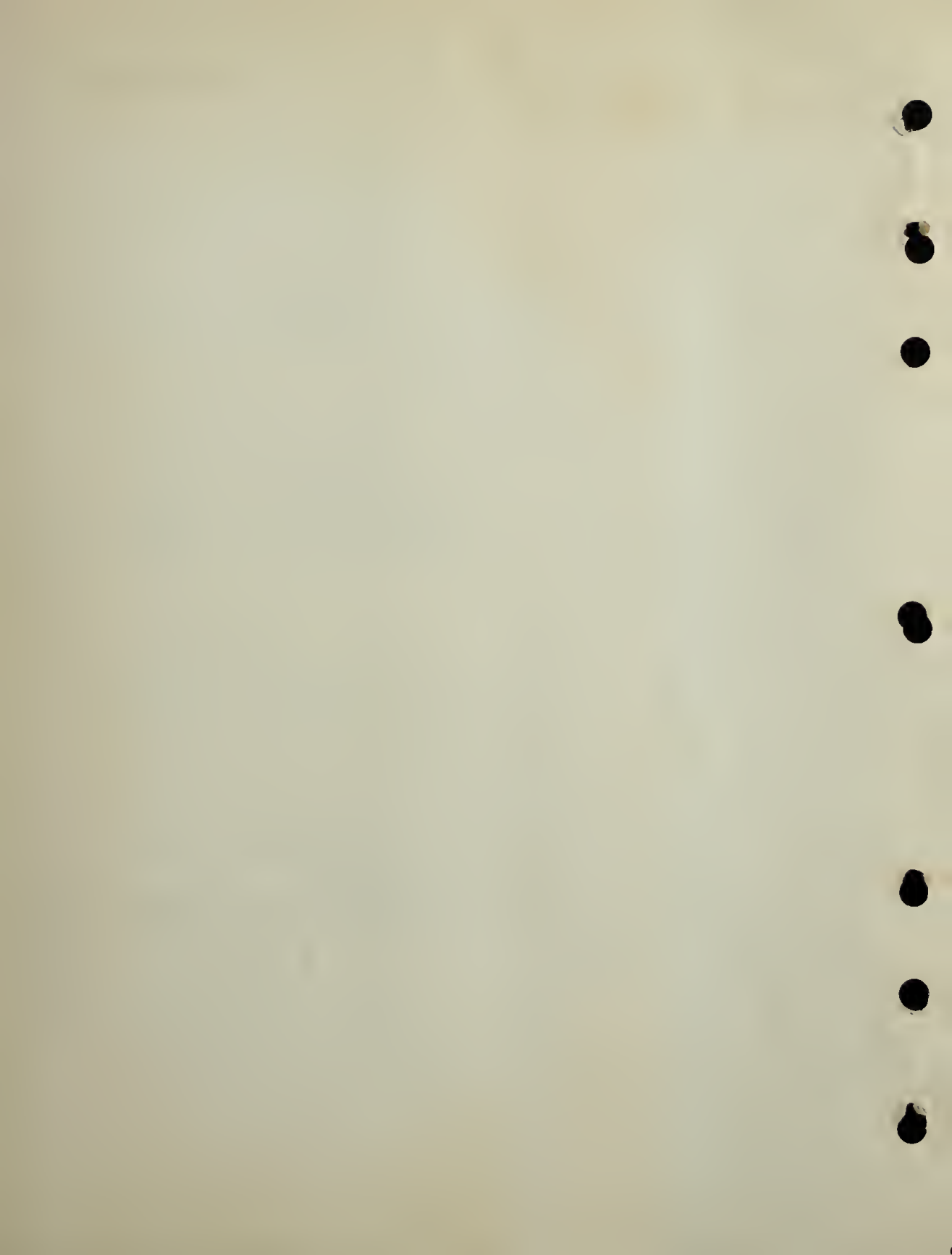


Table 4-XI. Register Assignments (Erasable Memory)

Octal Address	Initials	Name and Purpose	Incremental Inputs	Location
0034	OVCTR *	Overflow counter **	+ or -	In erasable memory
0035	TIME 1 †	Main time counters **	+	
0036	TIME 2 †			
0037	TIME 3 ††	Time counter for T3 RUPT program **	+	
0040	TIME 4 †	Time counter for display programs **	+	
0041	UPLINK ††	Used as serial-to-parallel converter for uplink **	Shift or shift and add one	
0042	OUTCR1 ϕ	Rate counter for CDU's and IRIG's **	+	
0043	OUTCR2 ϕ	Rate counter for optics and thrust control **	+	
0044	PIPA X	Input counters **	+ or -	
0045	PIPA Y		+ or -	
0046	PIPA Z		+ or -	
0047	CDU X		+ or -	
0050	CDU Y		+ or -	
0051	CDU Z		+ or -	
0052	OPT X		+ or -	
0053	OPT Y		+ or -	
0054	TRKR X		+ or -	
0055	TRKR Y		+ or -	

(Sheet 1 of 2)

Table 4-XI. Register Assignments (Erasable Memory) (cont)

Octal Address	Initials	Name and Purpose	Incremental Inputs	Location
0056	RADAR IN	Input counters ** (cont)	Shift or shift and add one	In erasable memory (cont)
0057	OUTCR3 $\Phi$	Rate counter for Radar **	+	
0100 thru 0615		Reserved for Interpreter and executive programs.		

\* In case of overflow or underflow (as caused by instructions AD K and SUK)OVCTR is incremented or decremented. Interrupting programs with AD K instructions must prevent overflow and underflow or preserve the content of OVCTR.

\*\* For operations performed by the adder.

† TIME 1 counts time increments of 10 msec received from the clock and scaler. Overflows generated by incrementing TIME 1 increment TIME 2 (TIME 2 counts time increments of 163.84 sec).

†† TIME 3 is used as a general-purpose timer. Counting time increments of 10 msec to a preset number. It causes program interrupts (WAIT RPT) at the time of overflow. The WAITLIST program initiates the proper actions.

‡ TIME 4 counts 10 msec time increments to a preset number. It causes program interrupts (DISRUPT) at the time of overflow and is concerned with display programs.

‡‡ UPLINK is used as a serial-to-parallel converter. When signals are received from the uplink, the content of UPLINK is shifted by adding a ZERO or a ONE as a new lowest-order bit. The first bit of a word is always a ONE, so that the ONE when present in position 15 at the time of the next shift indicates that the complete word will be received after that shift. This initiates the UPRUPT program.

$\Phi$  OUTCR1, OUTCR2, and OUTCR3 count quantitative increments to a preset number. At the time of overflow, the output of that part of register OUT 2 is stopped.

(Sheet 2 of 2)

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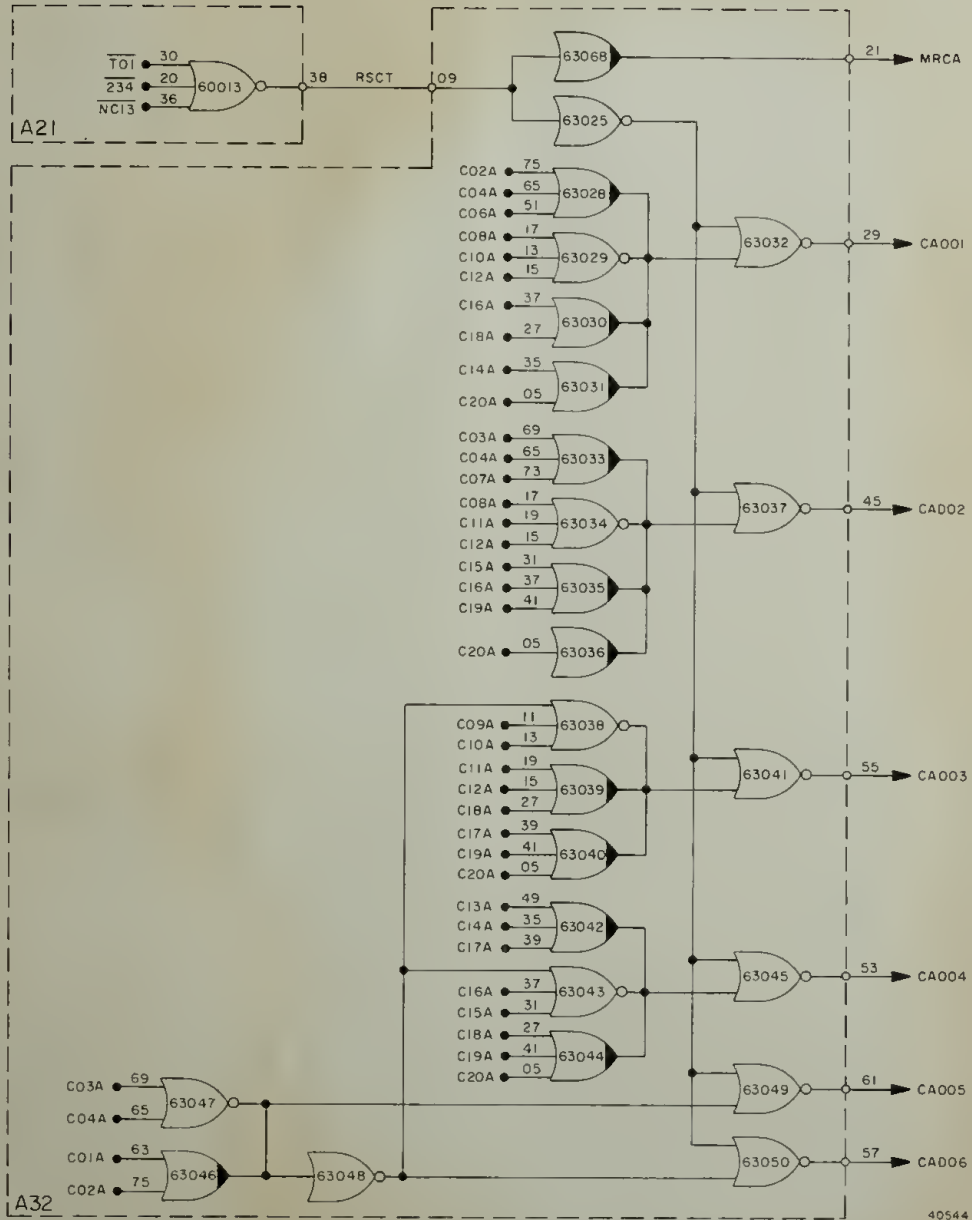
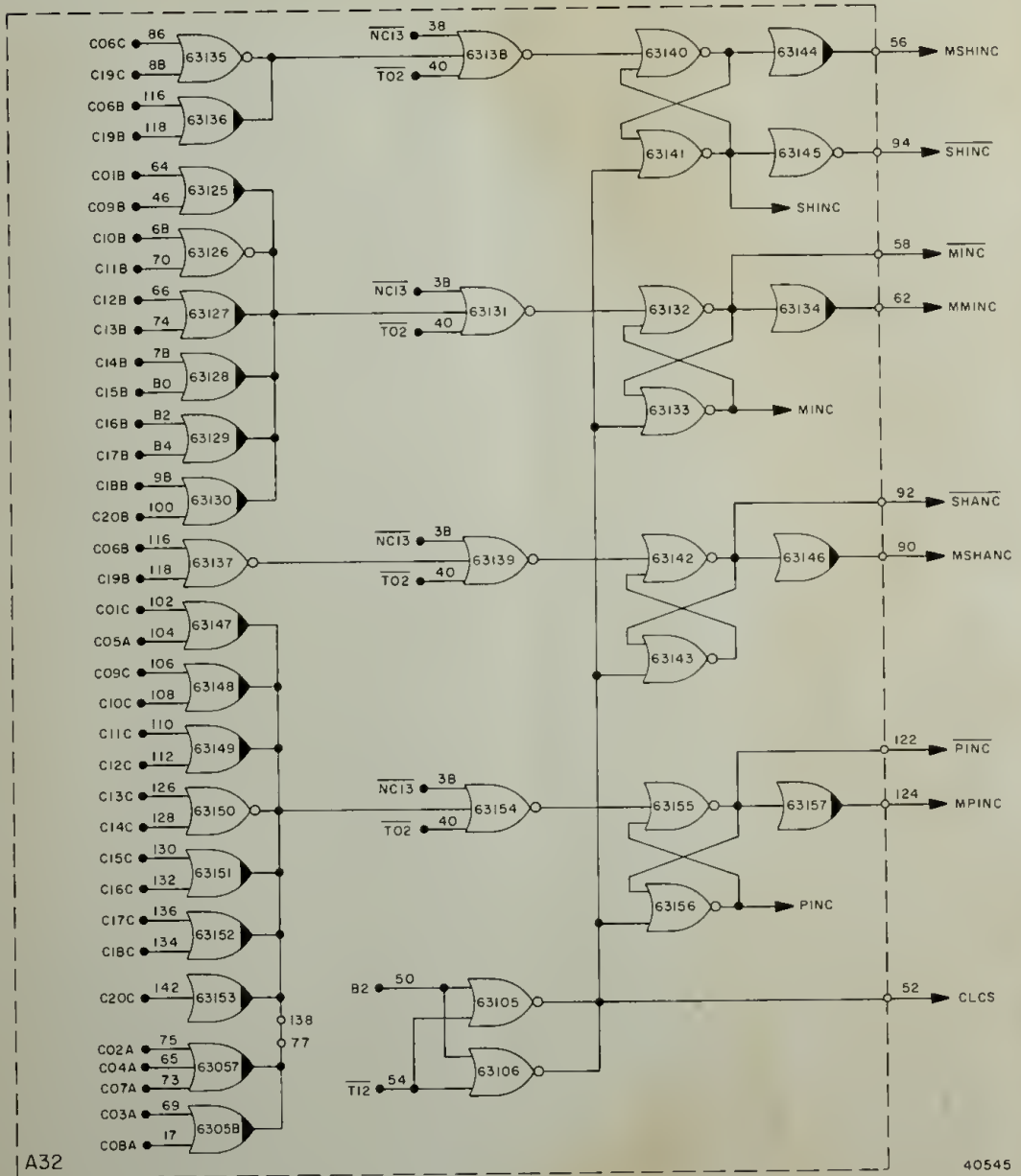


Figure 4-141. Address Generator (Counter Priority)



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Figure 4-142. Counter Command Logic



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In the address generator, C02A is used to generate the address of the TIME 2 counter. Outputs CAD01-CAD06 are applied to the write lines and will represent the correct combination for the address of this counter. In the command logic, C02A sets the PINC command flip-flop coincidentally with T02 and NC13. Signal NC13 enables the input gate.

Gate 59066 produces output CRH2, which temporarily inhibits any output from all lower-priority request flip-flops. The inhibit is removed at the next time 9 (RSSB) so that inputs to the next-lower-priority cell can be processed in the next memory cycle.

4-8.5.2.2 Incrementing or Decrementing. The group B input flip-flops function similarly to the group A flip-flops with the exception that outputs from group B initiate increment or decrement operations. Input pulses supplied to the input flip-flops from the sequence generator and subsystems of the G & N system initiate the generation of PINC or MINC commands.

As an example of operation of the group B flip-flops, incrementing and decrementing of the overflow counter at location 0034 will be discussed. A plus increment operation to the overflow counter is identical to that of the TIME 2 counter described previously. The minus increment operation is described in detail.

A MINC command is generated by supplying a set signal to the input flip-flop of the overflow counter priority cell (FF58082-58083) from the underflow detection gate (CO1M from gate 63065). The reset output from FF58082-58083 conditions gate 58085, which is unable to produce signal C01B until the address for the overflow counter is generated. The set output from FF58082-58083 is inverted by gate 58086, and enables one leg of the request transfer gate (58087). At time 9 (BKTF) the request transfer gate output sets the request transfer flip-flop (FF58089-58090). The request transfer flip-flop supplies the priority chain with inhibiting signal CRN1, and supplies the address generator with signal C01A.

Signal C01A, coincident with control pulse  $\overline{RSCT}$ , produces the address (0034) of the overflow counter. This address enables gate 58085. Signal C01B is now produced and enables the command transfer gate (63125), which sets the MINC command flip-flop coincident with signal NC13 and time pulse T02.

4-8.5.2.3 Shift or Shift-And-Add-One. The group C flip-flops receive incremental pulses that are used to generate shift (SHINC) or shift-and-add-one (SHANC) commands. SHINC or SHANC initiate operations within counter priority control which accomplish serial-to-parallel conversion for the UPLINK and RADAR IN counters. Input pulses supplied to the input flip-flops from the UPLINK CTR gate and input-output initiate the generation of SHINC or SHANC commands. A SHINC command is generated for a ZERO of the serial input word, and SHINC and SHANC are generated simultaneously for a ONE of the serial input word.

For a SHINC command, the UPLINK CTR gate (88609) supplies set signal C06S to input flip-flop FF59080-59081. The reset output from this flip-flop conditions gate 59088; the set output is inverted by gate 59086. This action subsequently produces the address of the UPLINK counter through a transfer of pulses via the request transfer gate (59087) at time 9, and the request transfer flip-flop (FF59089-59090). This address is transferred to the memory address generator by the address transfer gate and simultaneously enables gate 59088. Signal C06C is now produced by the output from gate 59088 and conditions the command transfer gate (63135). The output from gate 63135 enables gate 63138, which is conditioned by signal  $\overline{NC13}$  and time pulse T02. This gate sets the command flip-flop (FF63140-63141) and produces the SHINC command, which is applied to the sequence generator.

When an input signal is supplied to counter priority control, signal  $\overline{CTROR}$  is produced by the last cell of the priority chain and is applied to the CTROR inhibit gates (63102 and 63104) in the display and load logic (figure 4-143). If inhibiting signals MNHNC, OINK, and LINK are not present, the output from the CTROR inhibit gate sets the increment flip-flop (FF63113-63114), which produces signal INKL, and also sets the increment control flip-flop (FF63107-63108), which produces signal INKL, and also sets the increment control flip-flop (FF63107-63108), which produces signal  $\overline{NC13}$ . Signal INKL and INKL are sent to the sequence generator to inhibit the execution of the next subinstruction.

Signal  $\overline{INKL}$  also conditions the reset strobe generator (RSSB) input gates (63017 and 63018, figure 4-140). At time T09, the reset strobe generator output gates produce signal  $\overline{RSSB}$ , which resets the input and request flip-flops in the priority cells. Signal  $\overline{NC13}$  enables the input gates of the command flip-flops and the RSCT control pulse gate of the sequence generator. This allows both the address and the specified command to be generated.

4-8.5.3 Address Generator. The address generator (figure 4-141) supplies outputs CAD06 through CAD01 (high order to low order) to the write amplifiers in the central processor. The various combinations of these outputs represent the address of the specific counters to be updated.

All inputs to the address generator from the priority cells bear the suffix A (C02A, C06A, etc.). By examining the address generator logic, the correct combination of outputs CAD06-CAD01 can be determined, which represents a particular address. For example, input C06A is from the UPLINK priority cell. This input is applied to several gates in the address generator causing outputs CAD06-CAD01 respectively to assume a condition of (100) (001). When placed on the write lines address 0041 is generated as the address of the UPLINK counter.

The address is gated onto the write lines at time 1 ( $\overline{T01}$ ) of the memory cycle time following the memory cycle time in which the request to update occurred. This is accomplished by gate 60013 which generates transfer signal RSCT at time 1, as indicated by signal  $\overline{NC13}$ .

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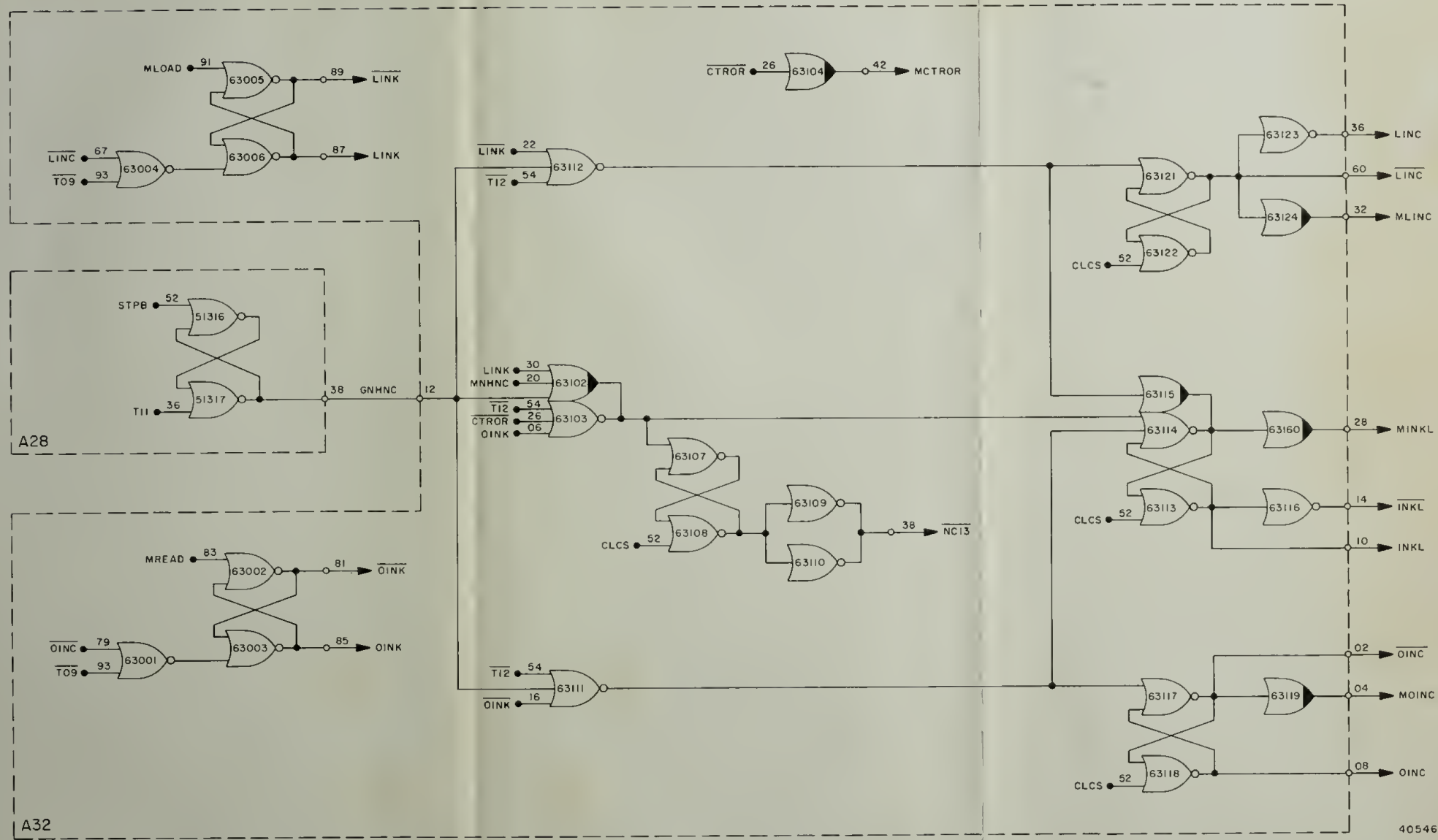
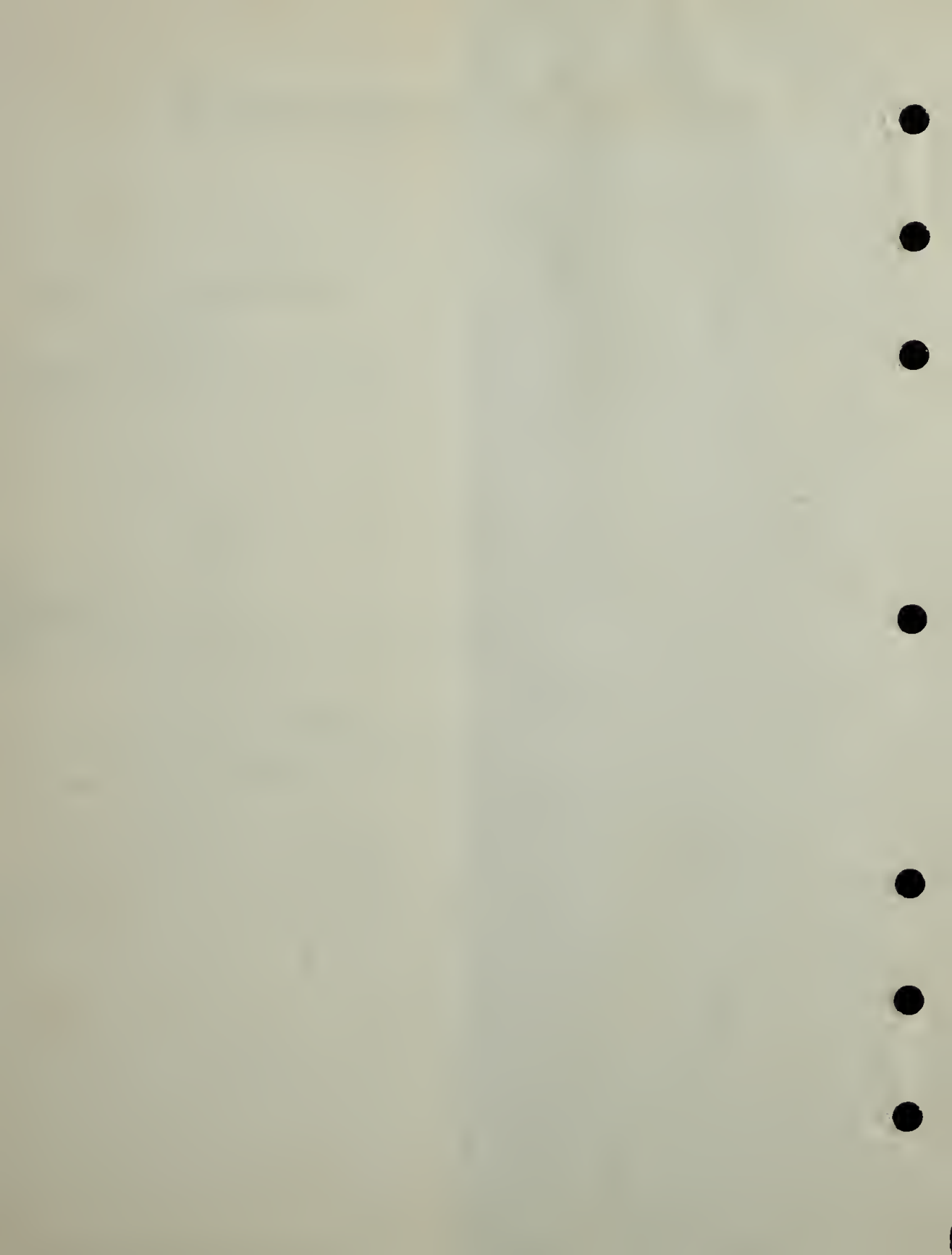


Figure 4-143. Display and Load Logic



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4-8.5.4 Counter Command Generation. The counter command logic (figure 4-142) generates the commands to increment (PINC), decrement (MINC), shift (SHINC) or shift-and-add-one (SHANC). These command signals are applied to the sequence generator, which generates the proper control pulses. Counters for which an increment operation occurs set the PINC command flip-flop. These are inputs with suffixes A and C (C02A, C01C) to extended NOR gate 63150. All inputs with suffix B (C01B) set the MINC command flip-flop. A SHINC command is generated by inputs C06C (UPLINK) and C19C (TRKR R). A SHANC command is always generated simultaneously with SHINC. This is indicated by inputs C06B and C19B to both the SHANC and SHINC command flip-flops.

The counter commands are gated out at time 2 immediately following the address. The command flip-flops are reset at time 12 (T12) coincident with B2 from the timer.

NOTE: Although the CTS is outside the scope of this document, one of its functions is described in the following paragraph in the interest of clarity.

4-8.5.5 Display and Load Instruction Control. The Display and Load Logic (figure 4-143) supplies Counter Priority Control with display and load requests MREAD and MLOAD from the CTS. These requests allow the contents of an addressed location to be displayed on the CTS, or allow data to be entered into an addressed location from the CTS.

Either signal MREAD or MLOAD sets a respective input flip-flop. The operation of both circuits is identical. Therefore, only the display instruction (MREAD) will be detailed. Signal MREAD is a set signal for the display input flip-flop (FF63002-63003). The output of the display input flip-flop, OINK, is supplied as an inhibiting signal to the counter increment inhibit gate (63103). This prevents the increment control flip-flop (FF63107-63108) from being set. The counter increment control signal, NC13, is now inhibited, and prevents the execution of counter instructions. The display transfer gate (63111) is conditioned by signal  $\overline{\text{OINC}}$ , and at time 12 (T12) sets the display command flip-flop (FF63117-63118). Signal GNHNC is generated as a function of STPB which sets FF51316-51317. Signal STPB in turn is generated by a monitor start command (MSTRT) from the CTS. A monitor start command causes signal GOJAM and inhibits any display or load routines from the CTS until FF51316-51317 is reset at time 11 and enables the display transfer gate, the load instruction transfer gate (63112), and the counter increment inhibit gate 63103).

The display transfer gate output sets the display command flip-flop causing signal OINC to be generated and sets the increment flip-flop (FF63113-63114) generating signal INKL. Signal OINC is applied to the sequence generator for execution of the display instruction. Signal INKL is fed back to the CTS indicating that a display command is being executed.

4-8.5.6 Counter Service Gates. The counter service gates (figure 4-144), generate enabling signals for various portions of the logic when the counters in erasable memory are to be updated. The counter address generate signal (CAGEN) is a logic ONE for memory addresses 0000 through 0077. This is determined by the inputs to gate 45611. Signal ST07 is a logic ZERO up to address 0077; therefore the output of 45611 is a ONE up to this address as a function of this input. The signal is not generated for addresses beyond 0077. This is accomplished by inputs ST08, ST11, and ST12 (these inputs become logic ONE and inhibit the gate).

The output of gate 45611 is inverted to produce signal CAGEN, and enables the gates which generate outputs CA1 through CA5. An output occurs from one of these gates when specified locations in memory are addressed. These are as follows:

- CA1 - Locations 0010 through 0017
- CA2 - Locations 0020 through 0027
- CA3 - Locations 0030 through 0037
- CA4 - Locations 0040 through 0047
- CA5 - Locations 0050 through 0057

These outputs are inverted and become enabling signals ( $\overline{CA1}$  through  $\overline{CA5}$ ) when the specific locations in memory are addressed. Signal CA1 is generated when CAGEN,  $\overline{XT1}$ , and ST06 are coincident. The two latter signals are from the memory addressing section and are both logic ZERO to enable gate 45616 when locations 0010 through 0017 are addressed. Similarly,  $\overline{XT2}$  and ST06 are logic ZERO when locations 0020 through 0027 are addressed and, coincident with CAGEN, cause CA2 to be generated. Signals CA4 and CA5 are generated not only as a function of the associated memory address, but also as a function of a counter increment condition; that is, a counter increment request (INKL) must be taking place in order to generate CA4 and CA5.

4-8.5.7 Interrupt Priority Control Functional Description. Interrupt priority control (figure 4-145) addresses locations 2000, 2004, 2010, 2014, 2020, and 2024 of fixed memory. These locations store the first instruction of the interrupt (RUPT) transfer subroutines. Interrupt requests, supplied to the input logic, initiate action in the address generator to produce a fixed memory address and signal RUPTOR. Signal RUPTOR initiates interrupt operation in the sequence generator.

4-8.5.7.1 Input Logic. The input logic receives interrupt request signals and produces interrupt signals RP1, TRP2, RP3, TRP4, MKTRP, and RP5 for the address generator. (TRP4 and MKTRP are both fourth priority interrupt request signals.) The TIME 3 and 4 counter addresses from memory indicate if the waitlist counter or display counter is being incremented when overflow occurs. The waitlist address in conjunction with overflow initiates signal RP1. The display address in conjunction with overflow initiates signal RP3. The RPT2 interrupt request signals are not connected at present. The keycode and mark interrupt inputs initiate signals TRP4 and MKTRP, respectively. The keycode interrupt inputs occur when any keys on the navigation control DSKY's are operated. The mark interrupt input occurs when the

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mark signal is received from the ISS. The address of the uplink counter is required in conjunction with the uplink interrupt conditioning signal RP5. The downlink end pulse occurs after a complete downlink word has been sent to the spacecraft telemetry system. The downlink end pulse is applied directly to the address generator circuits; not through the input logic.

Signal RP1 initiates the first priority T3RUPT transfer subroutine. Signal TRP2, if used, would initiate the second priority RPT2 transfer subroutine. Signals TRP4 and MKTRP initiate the fourth priority KEYRUPT transfer subroutine. Signal RP5 initiates the fifth priority UPRUPT transfer subroutine. The downlink end pulse, DKEND, initiates the sixth and lowest priority DOWNRUPT transfer subroutine.

The signals that enable the keycode trap and mark trap circuits are supplied from mechanical switches. A trap circuit produces only one pulse output when an input signal is gated with timing signals that produce a train of pulses. A trap circuit consists of two interconnected flip-flops. The first flip-flop receives a train of pulses whenever the applicable switch is pressed and the second flip-flop receives a reset signal when the same switch is released. The first input pulse produces an output from the first flip-flop which, besides being the trap output, sets the second flip-flop. The second flip-flop then inhibits further outputs from the first flip-flop until the switch is released and the second flip-flop is reset.

Any DSKY pushbutton, when pressed, produces keycode signals that enable the keycode trap. The mark signal from the ISS enables the mark trap. The sequence generator inhibits these traps with the RUPT3 signal. Otherwise, the KEYRUPT request generated would interfere with a lower priority DOWNRUPT or UPRUPT request being processed. This exception is made because the keycode and mark interrupt requests, unlike all other requests, can occur while an interrupt request is being processed. Signal KYRST resets the keyboard trap and signal MKRST resets the mark trap. These reset signals rise to logic ONE levels when the pushbuttons are released. When enabled, either trap generates signal ZZZZ. Signal ZZZZ clears register IN O in the central processor of previous information.

Uplink signal RP5 is produced when a complete uplink word is received. During the execution of instruction SHINC or SHANC, signal SHINC conditions the uplink gate. When the flag bit of the parallel word is shifted into bit position 16, signal WL16 is produced and sent to the uplink gate. The sequence generator produces signal TSGN2 at time 6 of instruction SHINC and SHANC. Signal TSGN3, supplied to the uplink gate, tests for the flag bit. The uplink gate produces signal RP5 if the flag bit is present.

4-8.5.7.2 Address Generator. The address generator produces the interrupt-transfer-subroutine address, signal RUPTOR, and signal MRPTR. Interrupt requests set request flip-flops in the address generator. Address detection gate outputs reset the request flip-flops after the address is sent to the central processor and after the last subinstruction of RUPT (RUPT3) is begun. All request flip-flop outputs are connected in a priority chain that supplies inputs to the address transfer gates. The priority chain supplies the address of the highest-priority interrupt that has been requested.

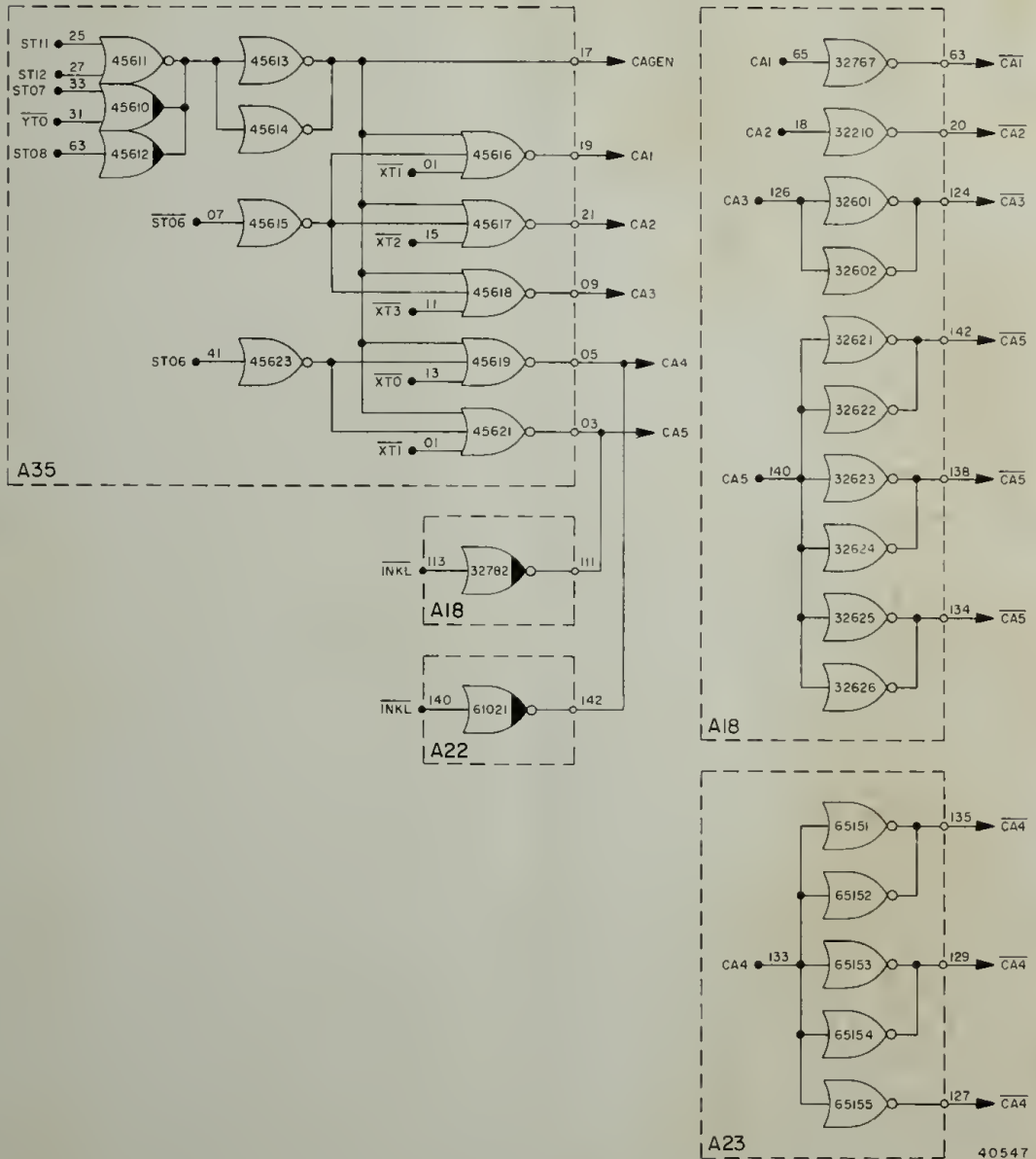
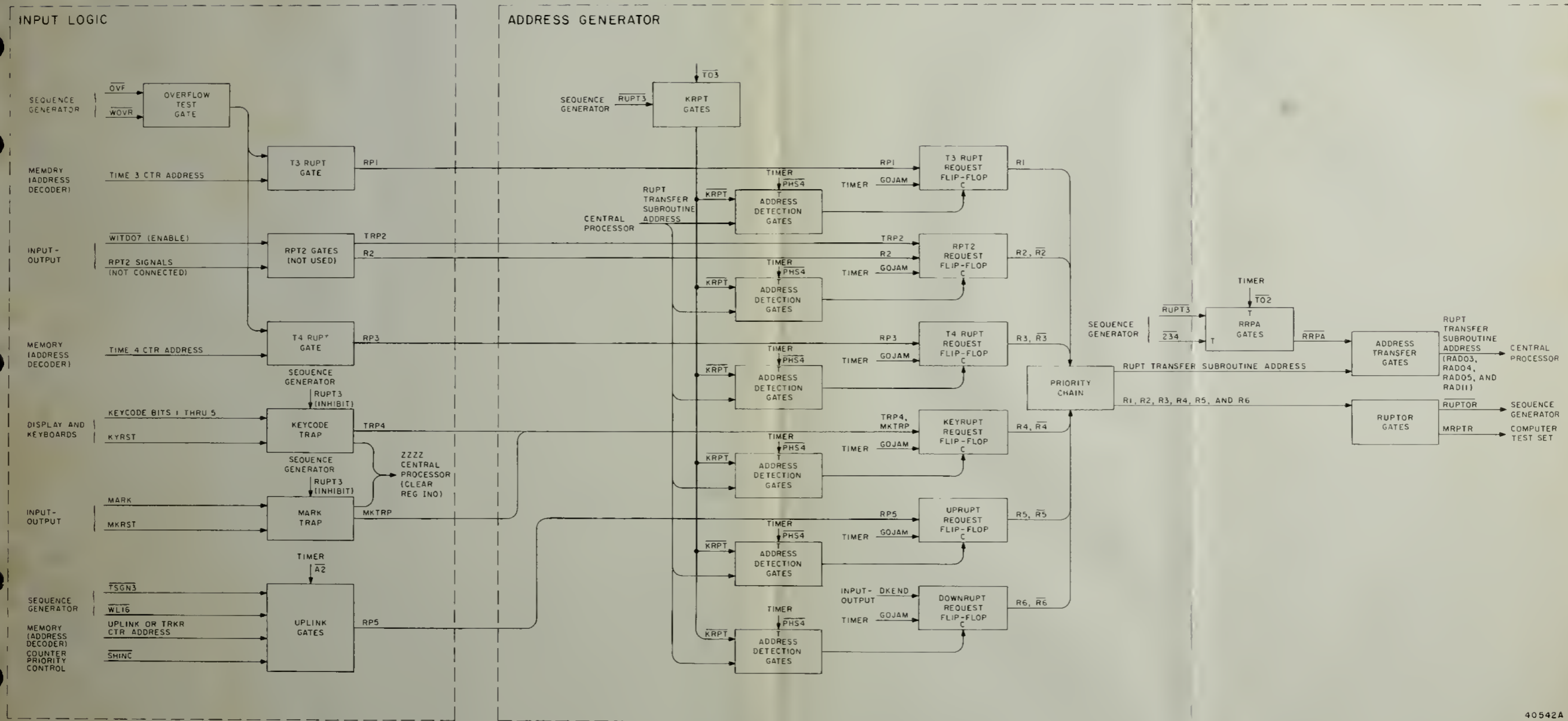


Figure 4-144. Counter Service Gates

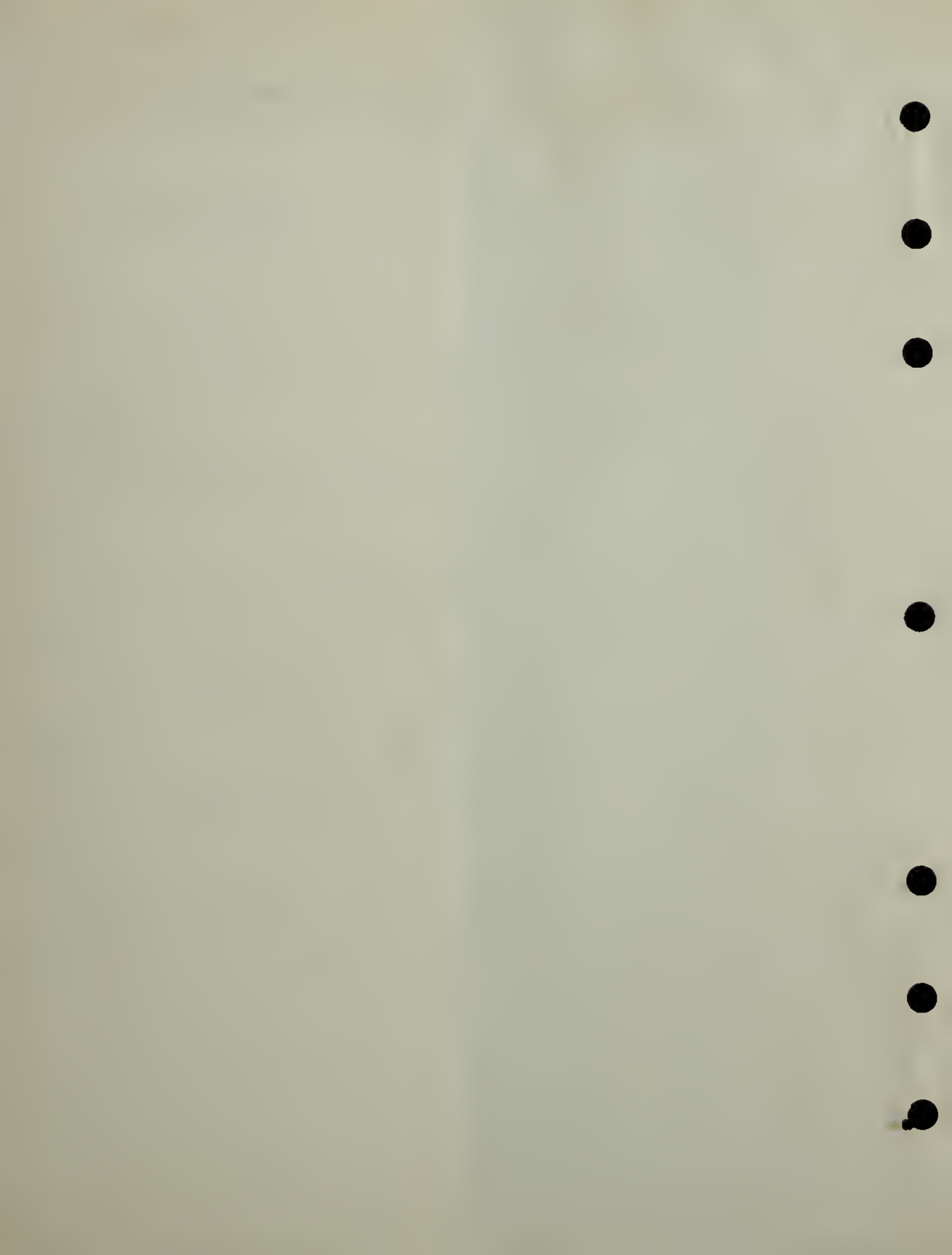


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Figure 4-145. Interrupt Priority Control



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The priority chain also enables the RUPTOR gates to produce signals  $\overline{\text{RUPTOR}}$  and  $\overline{\text{MRPTR}}$ . Signal  $\overline{\text{RUPTOR}}$  initiates machine instruction RUPT in the sequence generator. Signal  $\overline{\text{MRPTR}}$  is used in the CTS circuits.

The priority chain supplies address 2000, 2004, 2010, 2014, 2020, or 2024 to the address transfer gates. At time 2 of subinstruction RUPT3, the sequence generator enables the RRP A gates. Signal RRP A then transfers the RUPT transfer subroutine address through the address transfer gates to the central processor where it is written into register Z. At time 3 of subinstruction RUPT3, the sequence generator enables the KRPT gates that supply  $\overline{\text{KRPT}}$  to the address detection gates. One set of address detection gates are now enabled by coincidence of  $\overline{\text{KRPT}}$ , timing signal  $\overline{\text{PHS4}}$ , and the RUPT transfer subroutine address that is now being processed by the central processor. The enabled address detection gates reset the request flip-flop that stored the request. If another request flip-flop is set, that request is now applied to the address transfer gates and another interrupt operation is begun.

4-8.5.8 Interrupt Priority Control Detailed Description. The input logic of interrupt priority control (figure 4-146) receives interrupt request signals and produces interrupt signals RP1, TRP2, RP3, TRP4, MKTRP, and RP5. The TIME 3 and TIME 4 counter addresses from memory (0037 and 0040 respectively) indicate if these counters are being incremented when overflow occurs. The TIME 3 address coincident with overflow ( $\overline{\text{OVF}}$ ) initiates signal RP1 from gate 37104. The TIME 4 counter address coincident with overflow initiates signal RP3 from gate 37105. The keycode from the DSKY's and the MARK input from the G & N indicator control panel initiate signals TRP4 and MKTRP, respectively. These two inputs both have the same level priority. Information received via UPLINK and from the RADAR IN counter, as indicated by addresses 0041 and 0056 respectively to gates 35145 and 35143, initiates signal RP5 when the flag bit in the incoming word is detected. The flag is present as sensed by a ONE in bit position 16 of the write lines ( $\overline{\text{WL16}}$ ) during the test for flag ( $\overline{\text{TSGN3}}$ ) coincident with SHINC from the sequence generator and  $\overline{\text{A2}}$  from the timer.

The signals that enable the keycode trap (TRP4) and the mark trap (MKTRP) circuits are supplied from mechanical switches. The trap circuit consists of two flip-flops interconnected in such a manner that only one pulse output occurs for each input. The first flip-flop receives a set signal when the applicable switch is pressed; the second flip-flop receives a reset signal when the same switch is released. The input produces an output from the first flip-flop which, in addition to being the trap output, sets the second flip-flop. The second flip-flop then inhibits further outputs from the first flip-flop until the switch is released and the second flip-flop is reset.

Any one of the keycode inputs (KEY 1 - KEY 5) from the DSKY's enables the keycode trap input gate (37404). The MARK signal enables the mark trap input gate (37502). The input gates are temporarily inhibited by the RUPT 3 signal input from the sequence generator; otherwise, the KEYRUPT request generated would interfere with a lower priority UPRUPT or DOWNRUPT routine being processed. This exception

to interrupt requests exists because the keycode and mark requests, unlike all other requests, can occur while an interrupt request is already in process. Signal KYRST resets the keyboard trap, and MKRST resets the mark trap circuit. Both of these signals are generated when the associated pushbuttons are released.

The interrupt signals from the input logic are applied to the address generator (figure 4-147) to produce the address for the particular interrupt condition. Each of the interrupt signals is applied to an associated input flip-flop generating one of signals R1 through R6. These signals are applied to a decoder network which generates outputs RAD01 through RAD06 in proper combination to represent the address of the interrupt condition. The decoder network also establishes the priority of the interrupt inputs. Signal RP1 (R1) has the highest priority, TRP2 (R2) the second highest priority, RP3 (R3) the third highest priority, TRP4 and MKTRP (R4) the fourth highest priority, RP5 (R5) the fifth highest priority, and DKEND (R6) the lowest priority. Signal DKEND is not applied through the input logic. It is supplied directly to the address generator from the down-link telemetry section (figure 4-125). The various combinations of outputs RAD01 through RAD06 which are supplied to the write lines in the central processor in order to generate the interrupt addresses are listed below in order of priority:

RAD11	RAD05	RAD04	RAD03	Generates Address	Interrupt Routine
1	0	0	0	2000	T3RUPT
1	0	0	1	2004	RPT2
1	0	1	0	2010	T4RUPT
1	0	1	1	2014	KEYRUPT
1	1	0	0	2020	UPRUPT
1	1	0	1	2024	DOWNRUPT

Outputs RAD01 through RAD06 are placed on the write lines at time 2 of sub-instruction RUPT 3 by signal RRP A (generated by gate 60041). At time 3 of the same subinstruction, the input flip-flops are reset by reset signal  $\overline{KRPT}$  coincident with the address of the interrupt routine from the write lines. For example, if T3RUPT is initiated, outputs RAD01 through RAD06 cause address 2000 to appear on the write lines. Write lines WL03 and WL05 are logic ZERO enabling gates 37004 and 37005 respectively in the address generator. These inputs coincident with reset signal  $\overline{KRPT}$  reset FF37015-37016.

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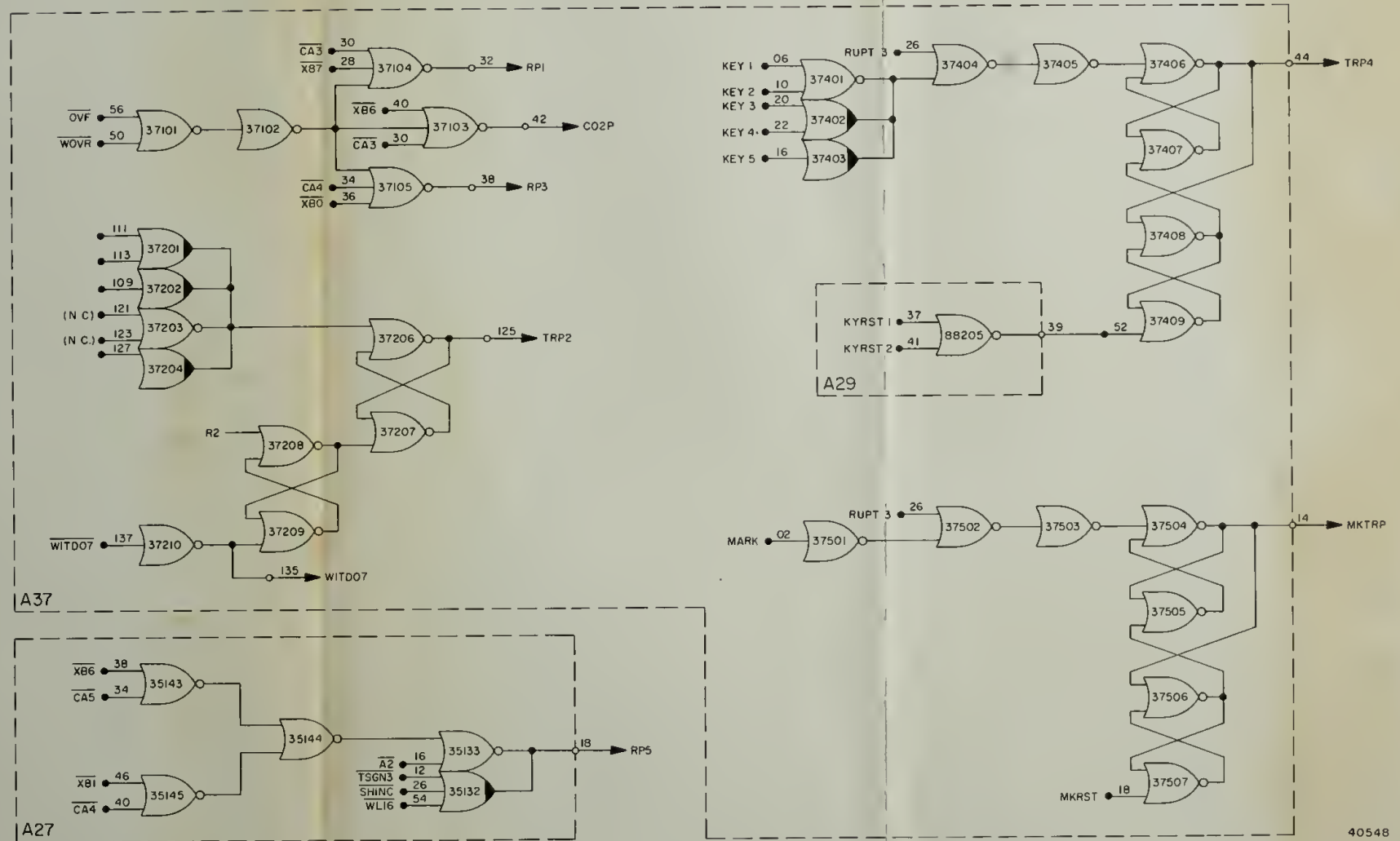
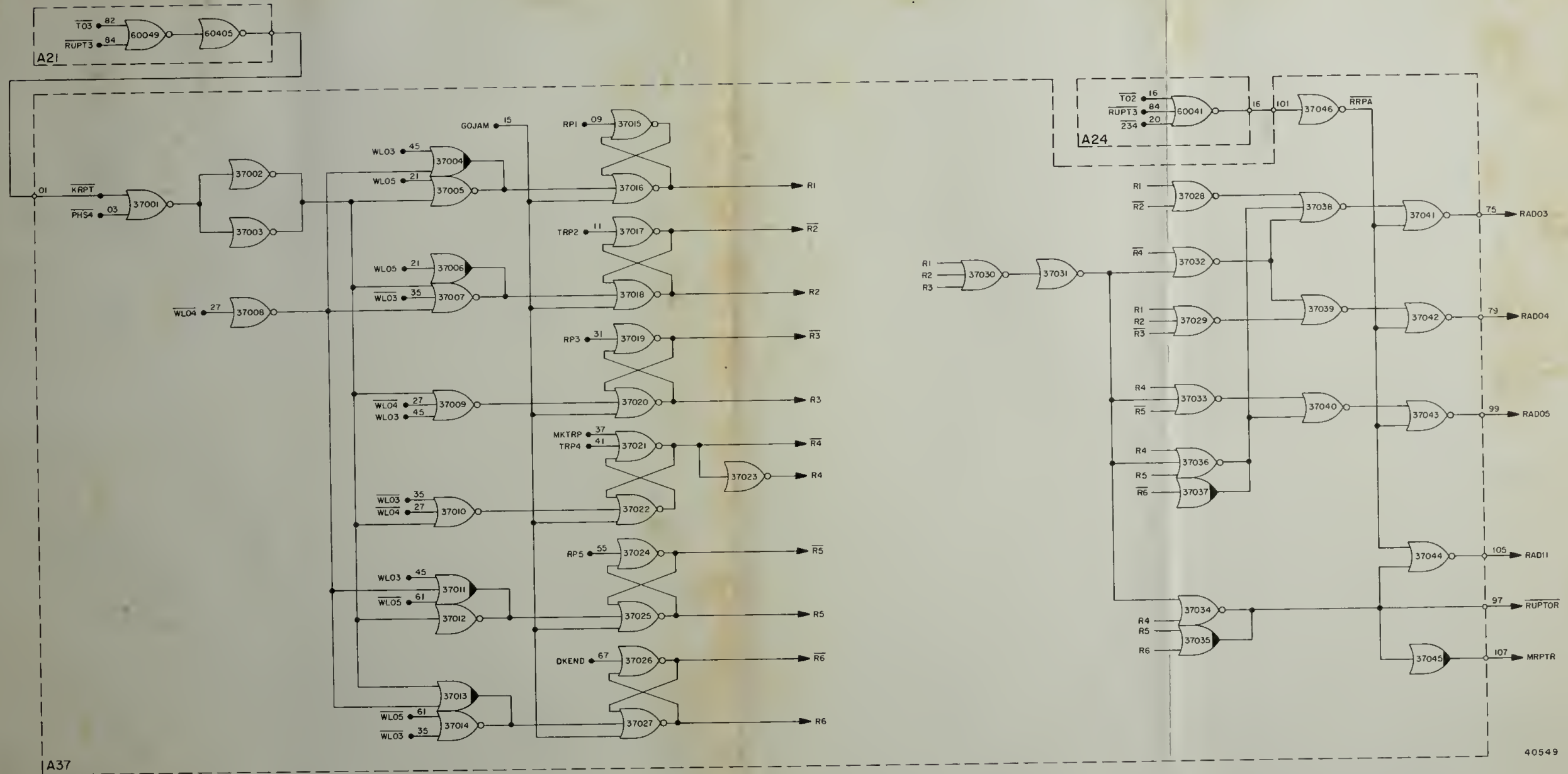


Figure 4-146. Interrupt Priority Control, Input Logic





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Figure 4-147. Address Generator (Interrupt Priority)

