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Digital Dev. Memo #376

To: Eldon Hall
From: Allen Harano
Date: 27 July 1967
Subj: Absence of Clear Rope Signals In Block II AGC's

c: Lee?

In an attempt to further investigate the failure of AGC C2 with flight ropes (Sunburst 116) at KSC (21 July 1967), tests were conducted on AGC C200 (P/N 2003200-011X, S/N RAY 21) using Sundial D ropes.

The logic signal CLROPE, which enables the Clear Rope drivers, was grounded and the AGC was powered up. The computer was "hung up" with continuous parity failures in fixed memory. The 14 volt supply was raised to 15.9 volts and the computer successfully ran Self-Check. The 14 volt supply was then lowered in 0.1 volt increments. At 14.9 volts a program Alarm occurred when attempting to perform a V36E (quite repeatable) and the computer would not start Self-Check.

The hardware configuration was as follows: Computer Sub-System setup, Sundial D in modules B1, B2 and B3; jumper module in B4; nothing in B5 and B6.

The Clear Rope Drivers are used to reset all of the cores only on an "aborted" cycle (a fixed memory cycle that is started and then "aborted" when it is found that the OP code is a quarter code and that the address is really an erasable address). Any programs written to check the performance of the clear rope drivers should perform an "aborted" cycle with an appropriate "address" just prior to reading out fixed memory.

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