

## SPACE AND INFORMATION SYSTEMS DIVISION

## SYSTEMS SUPPORT TRAINING

## CONTROL PULSES

Pulse	Purpose		
A2X	Copies bits 16 through 1 of register A directly (not through WA's) into bit positions 16 through 1 of register X.		
B15X	Enters a ONE into bit position 15 of re-	Enters a ONE into bit position 15 of register X.	
CI	Inserts carry bit into bit position 1 of the Adder. This adds the quantity one to the content of the Adder if no bit is carried around (from bit positions 16 to bit position 1).		
CLXC	Clears register X if flip-flop BR1 contains a ZERO. (Used in instruction DV E.)		
DVST	Modifies the content of the stage counter (ST) by complementing the content of the next higher bit position as shown below:		
	Binary Oct	al	
	000 0		
	001 1		
	011 3		
	111 7		
	110 6		
	100 4		
EXT	Enters a ONE into bit position EXT of	register SQ.	
G2LS	Copies bits 16, 15 through 4, and 1 of register G directly (not through WA's) into bit positions 16, 12 through 1, and 15 of register $X$ .		
KRPT	Resets interrupt priority cell.		
L16	Enters a ONE into bit position 16 of register L.		
L2GD	Copies bits 16 and 14 through 1 of register L directly (not through WA's) into bit positions 16 and 15 through 2 of register G; enters a ONE into bit position 1 of register G if pulse MCRO is generated.		
MONEX	Clears register X and enters ONE's into bit positions 16 through 2.		
MOUT	Causes the generation of one minus dri	ve pulse.	

Pulse	Purpose
WALS	Clears register A and writes the content of WA's 16 through 3 into bit positions 14 through 1. If bit position 1 of register G contains a ZERO, the content of bit position 16 of register G is entered into bit positions 16 and 15 of register A; if bit posi- tion 1 of register G contains a ONE, the content of output gate U 16 of the Adder is entered into bit positions 16 and 15 of register A. WALS also clears bit positions 14 and 13 of reg- ister L, and writes the content of WA's 2 and 1 into these bit positions.
WB	Clears register B and writes the content of WA's 16 through 1 into bit positions 16 through 1.
WCH	Clears the output channel specified by the content of register S and writes the content of WA's 16 and 14 through 1 into bit positions 15 through 1.
WG	Clears register G and writes the content of WA's 16 through 1 into bit positions 16 through 1, except if register S contains addresses 0020 through 0023 in which case the WA content is cycled or shifted (paragraph 30-41).
WL	Clears register L and writes the content of WA's 16 through 1 into bit positions 16 through 1.
WOVR	Tests the content of WA's 16 and 15 for positive overflow: if register S contains 0025, counter 0024 is incremented; if register S contains 0026, 0027, or 0030, instruction RUPT is executed.
WQ	Clears register Q and writes the content of WA's 16 through 1 into bit positions 16 through 1.
WS	Clears register S and writes the content of WA's 12 through 1 into bit positions 12 through 1.
wsc	Clear the CP register specified by the content of register S and writes the content of WA's 16 through 1 into bit positions 16 through 1.
WSQ	Clears register SQ and writes the content of WA's 16 and 14 through 10 into bit positions 16 and 14 through 10.

## Purpose

Pulse

WY

- Clears registers X and Y and carry flip-flop CI; writes the content of WA's 16 through 1 into bit positions 16 through 1 of register Y. WY12 Clears registers X and Y and carry flip-flop CI; writes the content of WA's 12 through 1 into bit positions 12 through 1 of register Y. WYD Clears registers X and Y and carry flip-flop CI, writes the content of WA's 16 and 14 through 1 into bit positions 16 and 15 through 2 of register Y; writes the content of WA 16 into bit position 1 of register Y except in SHINC sequence, or unless bit position 15 of reg-
- by control pulse NEACON. Clears register Z and writes the content of WA's 16 through 1 into WZ bit positions 16 through 1.

ister L contains a ONE at PIFL, or if end around carry is inhibited

- Z.15 Enters a ONE into bit position 15 of register Z.
- Z16 Enters a ONE into bit position 16 of register Z.
- ZAP Causes the generation of control pulses RU, G2LS, and WALS (used in instruction MP K).
- ZIP Causes generation of control pulses A2X and L2GD (used in instruction MP K); performs read/write operations depending on the content of bit positions 15, 2, and 1 of register L as shown:

	L15	L2	Ll	Read	Write	Carry	Remember
	0	0	0	-	WY		S
	0	0	1	RB	WY	-	
	0	1	0	RB	WYD	-	-
	0	1	1	RC	WY	- CI	MCRO
	1	0	0	RB	WY	-	-
	1	0	1	RB	WYD		-
	1	1	0	RC	WY	CI	MCRO
	1	1	1	-	WY	-	MCRO
	If MCI	RO occi	urs, a (	ONE is ent	ered into I	15	
ZOUT	Stops	the gen	eration	of drive p	ulses.		

Pulse	Purpose
NEACOF	Permits end around carry upon completion of subinstruction MP3.
NEACON	Inhibits end around carry (also during WYD) until NEACOF.
NISQ	Causes loading of next instruction into register SQ (implies RB and WSQ at time 12). Also resets the stage counter (ST) to 0; frees certain restrictions; permits execution of instruction RUPT and of all Counter Instructions.
PIFL	Prevents writing into bit position 1 of register Y on control pulse WYD if bit position 15 of register L contains a ONE. (Used in instruction DV.)
PONEX	Clears register X and enters a ONE into bit position 1.
POUT	Causes the generation of one plus drive pulse.
PTWOX	Clears register X and enters a ONE into bit position 2.
R15	Enters 000015 into WA's,
RIC	Enters 177776 (minus one) into WA's.
R6 -	Enters 000006 into WA's.
RA	Reads bits 16 through 1 of register A into WA's 16 through 1.
RAD	Reads address of next instruction. RAD appears at last time 8 of an instruction and is normally interpreted as RG. If the next instruction is INHINT, RELINT, or EXTEND, RAD is interpreted as RZ and ST2 instead.
RB	Reads bits 16 through 1 of register B into WA's 16 through 1.
RB1	Enters 000001 into WA's.
RBIF	Enters 000001 into WA's if flip-flop BR1 contains a ONE.
RB2	Enters 000002 into WA's.
RBBK	Reads the BB (both bank) configuration into the WA's, i.e., copies the content of bit position 16 of register FBANK into WA's 16 and 15, the content of bit positions 14 through 11 of register FBANK into WA's 14 through 11, and the content of bit positions 11 through 9 of register EBANK into WA's 3 through 1.

Pulse	Purpose
RC	Reads the complemented content of register B (bits 16 through 1 of C) into WA's 16 through 1.
RCH	Reads the content of the input-output channel specified by the contents of register S; bit 15 is read into WA's 16 and 15, and bits 14 through 1 are read into WA's 14 through 1.
RG	Reads bits 16 through 1 of register G into WA's 16 through 1.
RL	Reads bit 16 of register L into WA's 16 and 15, and bits 14 through 1 into WA's 14 through 1.
RL10BB	Reads low 10 bits, i.e., bits 10 through 1 of register B into WA's 10 through 1; replaces $c(S)$ , which includes a quarter code, by a 10 bit address.
RQ	Reads bits 16 through 1 of register Q into WA's 16 through 1.
RRPA	Enters into the WA's the address of a RUPT Transfer Routine supplied by the Interrupt Priority Control.
RSC	Reads the content of the CP register specified by the content of register S; bits 16 through 1 are read into WA's 16 through 1.
RSCT	Enters into the WA's the address of a counter address supplied by the Counter Priority Control (paragraph 30-94).
RSTRT	Enters 004000 (Block II start address) into WA's.
RSTSTG	Resets the stage counter to 0 (refer to DVST).
RU	Reads bits 16 through 1 of Adder output gates (U) into WA's 16 through 1.
RUS	Reads bit 15 of Adder output gates (U) into WA's 16 and 15, and bits 14 through 1 into WA's 14 through 1.
RZ	Reads bits 16 through 1 of register Z into WA's 16 through 1.
ST1	Sets stage 1 flip-flop to ONE at next time 12.
ST2	Sets stage 2 flip-flop to ONE at next time 12.
STAGE	Causes the execution of next subinstruction as defined by the content of the stage counter (ST).

Pulse	Purpose
TL15	Copies bit 15 of register L into flip-flop BR1,
TMZ	Tests the content of the WA's for minus zero: if bits 16 through 1 are all ONE's, flip-flop BR2 is set to ONE; otherwise BR2 is set to ZERO.
TOV	Tests the content of WA's 16 and 15 for overflow: set flip-flops BR1 and BR2 to 01 in case of positive overflow, or to 10 in case of negative overflow.
TPZG	Tests the content of register G for plus zero: if bits 16 through 1 are all ZERO's, flip-flop BR2 is set to ONE; otherwise the content of BR2 is not changed.
TRSM	Tests signals XT1/ and XB7 of selection logic for the resume address (0017) during the execution of subinstruction NDX0: if 0017 is present, subinstruction RSM3 is executed next by setting c(ST) = 3; otherwise subinstruction NDX1 by setting $c(ST) = 1$ .
TSGN	Tests content of WA 16 for sign: if a ZERO, flip-flop BR1 is set to ZERO; if a ONE, flip-flop BR1 is set to ONE without changing the content of flip-flop BR2.
TSGN2	Tests content of WA 16 for sign: if a ZERO, flip-flop BR2 is set to ZERO; if a ONE, flip-flop BR2 is set to ONE without changing the content of flip-flop BR1.
TSGU	Tests content of output gate Ul6 of Adder for sign: if a ZERO, flip-flop BRl is set to ZERO; if a ONE, flip-flop BRl is set to ONE.
U2BBK	Copies bits 16 and 14 through 11 of the Adder output gates (U) into bit positions 16 and 14 through 11 of register FBANK, and bits 3 through 1 (of U) into bit positions 3 through 1 of register EBANK. U2BBK may be inhibited by signal MONWBK, which is generated if register BBANK is addressed.
WA	Clears register A and writes the content of WA's 16 through 1 into bit positions 16 through 1.