



TELEMETRY SYSTEM
FOR
PROJECT APOLLO

R1-3047A-31-1

technical proposal



RADIATION
Melbourne

A Division of Radiation Incorporated

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TELEMETRY SYSTEM
FOR
PROJECT APOLLO

for

COLLINS RADIO COMPANY
CEDAR RAPIDS, IOWA

Attention: Mr. J. W. Stewart, Buyer

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1.0 DESIGN APPROACH

Based on a sincere desire to participate in the Apollo Program, Radiation Incorporated has assigned its most proficient and experienced aerospace PCM engineers to review the Collins Specification with emphasis on providing the optimum system to meet specification requirements, as well as sufficient flexibility to meet any future requirements which may arise as the Apollo Program develops.

Throughout, the approach has been to use design concepts which stem from previously flight proven and qualified systems, Radiation's circuit design experience is sufficiently broad so that it will not be necessary to use circuit techniques not previously studied or in use in operating Radiation PCM telemetry systems. This approach has yielded a system which complies with or exceeds all of the CRC specification requirements.

It would be most difficult to meet the reliability requirement of 0.997 for 340 hours for this type of system were it not for the human capability of in-flight maintenance. The Radiation design has been based upon the utilization of a combination of circuits which have been proven reliable through extensive qualification testing and actual operational use, interwoven with unique self-checking circuitry. High reliability is achieved through integrating an optimum arrangement of a minimum combination of operational circuits, together with self-checking circuitry, that allows quick fault detection, location, and replacement in the event of a failure, into each module.

Only 54 modules of 12 different types are used, each of which is replaceable "in-flight". These modules are not intended for in-flight repair, but are repairable in the normal sense. As an aid to more rapid location of the failure, Radiation can provide IFTS output signals from each module rather than from each SEP as required by the specification. Through this approach, a reliability figure of 0.9988 is achieved for a system weighing 65.4 pounds with spares.

The packaging concept has closely followed the SEP approach outlined by CRC. Using this approach, the optimum configuration was found to be three double SEP's in lengths of 14", 10", and 15".

The connectors were found to be the limiting factor of reliability. Radiation has prepared an alternate connector approach which eliminates the connectors within the SEP and considerably increases reliability while decreasing size and weight. However, this approach violates the limitation of 500 connector pins per double SEP imposed by the specification. This alternate approach is discussed in detail in Appendix "G".

The system electrical design approach closely follows that used on the existing Radiation OAO, Telstar and Nimbus satelliteborne PCM telemetry systems which contain extremely low power circuitry. With the use of low power circuitry the system power consumption is 5.25 watts at the normal rate of 64 kc.

The system accuracy requirement of $\pm 0.5\%$ was not difficult to meet for the 5.0 volt channels, but offers a real challenge for low-level signals in the presence of common mode voltages of ± 32 volts. This accuracy requirement will be met by a unique application of an existing Radiation differential amplifier. This approach consists of bootstrapping the common mode voltage by a capacitive charge transfer method at the amplifier output.

Another Radiation design goal was to provide a system with a great deal of inherent flexibility. All functions are compatible with a doubling of the 64 kc bit rate. The number of channels can be changed simply by re-arrangement of the multiplexer modules. Other functional circuitry and self-checking circuitry is similarly flexible.

Since the techniques used in the construction of this system are presently being used in the production of the OAO, Telstar and Nimbus satelliteborne PCM telemetry systems, the productability of the system is assured. This ensures that prompt delivery of equipment may be made with no chance of unforeseen assembly problems, or difficulties during qualification testing.

The PERT networks contained in Section 6.0 of Volume II, combined with the various other sections of the management proposal, delineate the Work Statement Radiation will follow in accomplishing the requirements of the APOLLO PCM Program under subcontract to CRC.

A summary of the specifications to which the Radiation Incorporated proposed PCM telemetry system for Apollo will conform is shown in Table 1.0.

1.1 Design Philosophy

1.1.1 System Description

A block diagram of the proposed Apollo telemetry is shown in Figure 1.1.1. It consists of a group of commutators and sub-commutators, an analog-to-digital converter, a digital multiplexer, an output register, a programmer and a power supply

TABLE 1.0

SPECIFICATION SUMMARY TABLE

I. INPUTS

A. Analog

Level	0-5 v	0-250 mv
Rate	1-500 sps	1 sps
No. Channels	375	100
Accuracy	0.392%	0.470%
Source Z (min)	0	0
(max)	5000 Ω	5000 Ω
Load Z (sample)	50 meg nom	50 meg nom.
(nonsample)	>100 meg	>100 meg
I back (sample)	<80 na	<15 na
(nonsample)	<5 na	<5 na
Com. mode reject.		>4 x 10 ⁶ to 1
Max. com. mode		± 32 v
Fault Voltage	30 v	32 v
Source Loading (OFF)	>100 meg	>100 meg

B. Digital

Level (1)	min. 3.5	max. 10.0
(0)	min. -0.5v	max. 0.5v
No. Channels	43 sets of 8	
Rate	1 sps to 10 sps	
Source Z	0-5000 Ω	
Load Z	>50 K	
Source Loading (OFF)	>2 meg	

C. Commands

	<u>Freq</u> <u>Std</u>	<u>Minimum</u> <u>Data</u>
Rate	512 kc	(Switch)
Level	0.0 & 10.0 ± 0.5 v	
Load Z	10 K min.	

II. OUTPUTS

Bit Rate	64 kc and	1 to 2 kc
Amplitude	0 = ± 0.5 v	1 = 6 ± 0.5 v
Source Z	600 ± 120 Ω	
NRZ Form	Change	

III. POWER

Voltage	115 v	+2.0 v	-2.0 v
Freq.	400 cps,		3 ϕ
P Max =	Nominal 5.25 w		

IV. WEIGHT

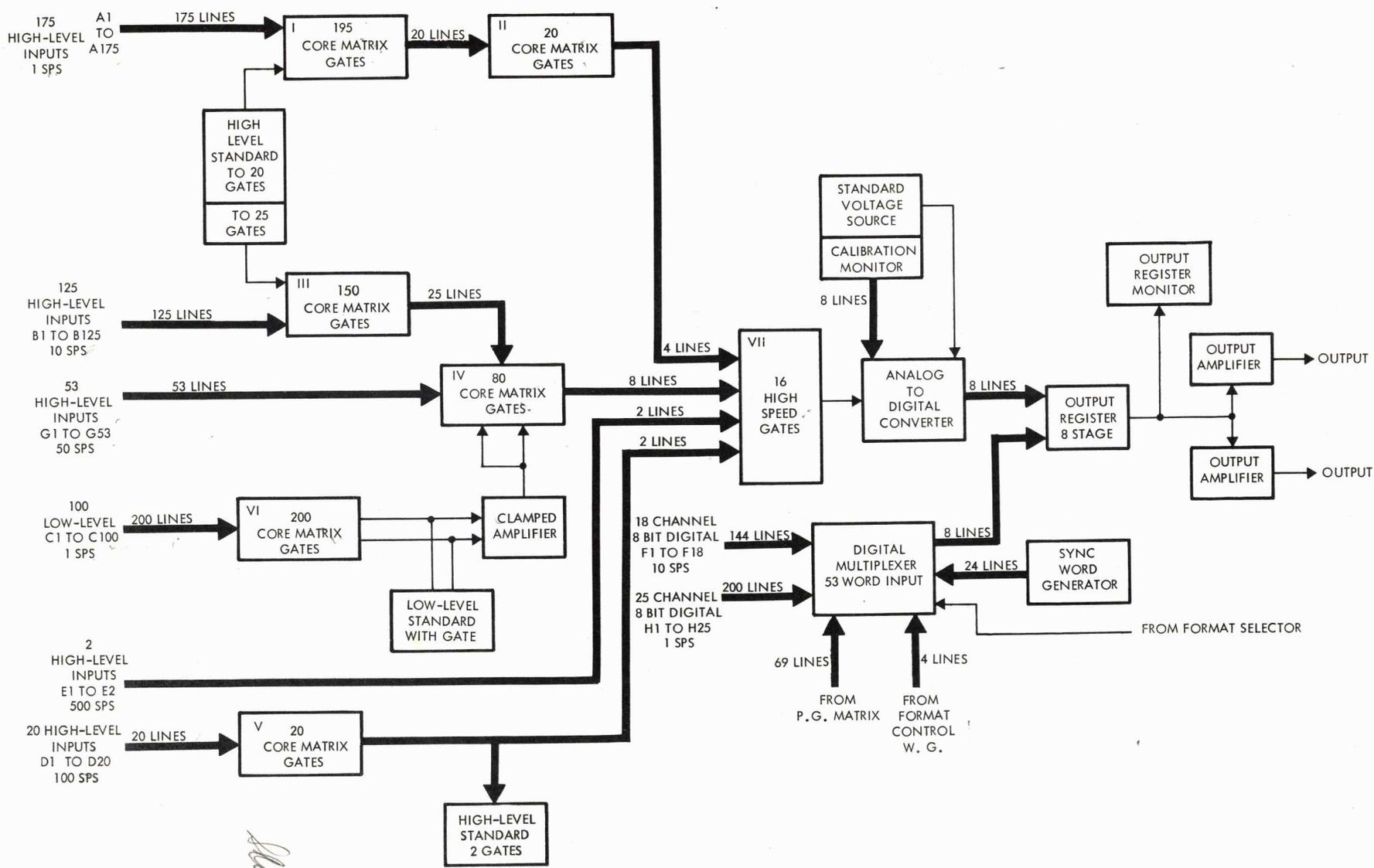
56.97 pounds	(Basic System)
8.40 pounds	(Spares)

V. SIZE

Three Double SEP's

322
500 to 128 kc

Slide 1



Sheet 2

Figure 1.1.1 System Block Diagram

The purpose of the commutators and sub-commutators is to time-division multiplex the various analog data channels into the analog-to-digital converter in a manner which will provide sampling rates in accordance with the specifications. The analog-to-digital converter converts the PAM signals from the commutators into 8-bit binary words, which are fed into the output register. Shifting the output register at the system bit rate then provides a serial PCM output.

The digital multiplexer alternates with the commutator - A/D converter system during a portion of each frame to provide samples of the digital signals which constitute a portion of the input data. Outputs from the digital multiplexer are fed directly into the output register during digital samples.

The programmer contains the system clock, counters, and other timing circuits required for synchronizing the operations of the remainder of the system.

The system timing is based upon the use of 64,000 bits per second, 8 bits per word, 160 words per sub-frame and 50 sub-frames per frame. This provides one frame and 50 sub-frames per second. The 500 sps channels are sampled at equal intervals ten times per sub-frame, and the 100 sps channels are sampled at equal intervals twice per sub-frame. The 50 sps channels are sampled each sub-frame, the 10 sps channels every fifth sub-frame, and the 1 sps channel once each frame. The resulting format provides 149 data words per sub-frame. Three words are reserved for synchronizing and one for sub-frame identification, leaving seven unused words in each sub-frame for calibration and fault detection.

The output bit rate is lowered by simply reducing the read-in and read-out rate of the output register. Thus, even though the commutators and analog-to-digital converter continue to operate at a faster rate in order to continue to accommodate self-checking features, only a fraction of the words generated will be transferred to the output register. Power conservation may be accomplished by removing power to the unused commutators and by applying power only intermittently to the analog-to-digital converter.

1.1.1.1 Data Format

Figure 1.1.1.1 represents a format which is used for the purpose of discussing the proposed design. A variety of formats can be derived with relatively minor changes to the system. A patch panel will be provided to make a variety of minimum rate formats normally available.

The format consists of a sub-frame, shown in Figure 1.1.1.1, which is both super-commutated and sub-commutated. The sub-frame contains 160 words and repeats 50 times per second. The "E" channels which are to be sampled 500 times per second appear ten times per sub-frame. The "C" channels which are sampled once per second each occur only once per frame. The "A" channels occupy four words (18, 58, 98, and 138) in the sub-frame. All of the 200 channel spaces available in the major frame for these words are not utilized. Forty-four "A" channels have been assigned of the 50 spaces available in each of these four words. For purposes of this proposal, a minimum data format has been selected which reduces the bit rate to 1.6 kilobits per second. In this mode, four words of the frame are stepped through the output register at 1/40th of the normal speed. The four words arbitrarily selected are numbers 18, 58, 98, and 138 which include all of the "A" channels. The unassigned spaces in these channels will be used to provide the following: (1) three sync words which will be the first three words in the new frame; (2) mode identification which will be the fourth word; (3) twenty channels of test data for the "in flight testing". This utilizes 199 of the 200 words in the minimum data rate frame. Sync words, Frame ID, and test words appear elsewhere in the frame, as shown in Figure 1.1.1.1. At normal speed, three sync words occur once per a 160 word frame. At minimum data rate three sync words occur once per frame of 200 words.

The minimum data format described is utilized because of its simplicity, small number of additional components, and resulting reliability. Radiation Incorporated does not intend this to be construed as the only method of providing this function. The design of the proposed telemetry system is flexible with almost an infinite variety of formats available. However, commensurate increases in the complexity of programming and the output register functions must be expected as a trade off for greater flexibility.

1.1.1.2 Programming

An over-all view of the programmer system function is presented in Figure 1.1.1.3-2. The basic clock rate of 512 kc is either an internal crystal controlled oscillator or an external input. The 512 kc is counted down to one per sec. Normally the count is derived from the external 512 kc source and the counter is reset by the external "once per second" pulse to achieve phase lock with vehicle time. In the absence of a satisfactory external clock the internal 512 kc is used and the external 1/sec reset is inhibited. The counter is divided into four sections which yield basic word rates, frame rates and the two sub-commutation rates down to 1/sec. Outputs from the counters drive a diode matrix which provides programming for commutation, encoding and serialization of the data. Commutation of analog data is accomplished by three types of transistor gates. Digital data are commutated by a diode gate digital multiplexer. Internal digital inputs such as sync words, test words and frame identification words are also gated through the digital multiplexer. Analog data, after commutation, are presented to the coder which includes a "sample and hold" function, "analog-to-digital" conversion, and buffered output. Digital words from the coder and from the digital multiplexer are presented in proper sequence to the output register which makes the parallel-to-serial conversion.

NORMAL FORMAT

1 SYNC	21 G 5	41 G 12	61 G 19	81 TEST	101 G 32	121 G 39	141 G 46
2 SYNC	22 E 1	42	62 E 2	82 B (5)	102 E 1	122 FORMAT ID	142 E 2
3 SYNC	23 B (5)	43 G 13	63 B(5)	83 G 27	103 B (5)	123 G 40	143 B (5)
4 D 1	24 D 6	44 D 11	64 D 16	84 D 1	104 D 6	124 D 11	144 D 16
5 C 1	25 G 6	45 G 14	65 G 20	85 C 28	105 G 33	125 G 41	145 G 47
6 E 1	26 B (5)	46 E 2	66 B (5)	86 E 1	106 B (5)	126 E 2	146 B (5)
7 B (5)	27 G 7	47 B (5)	67 G 21	87 B (5)	107 G 34	127 B (5)	147 G 48
8 D 2	28 D 7	48 D 12	68 D 17	88 D 2	108 D 7	128 D 12	148 D 17
9 TEST	29 G 8	49 C (50)	69 G 22	89 TEST	109 G 35	129 C (50)	149 G 49
10 F (4/5)	30 E 2	50 F (5)	70 E 1	90 F (4/5)	110 E 1	130 F (5)	150 E 2
11 G 2	31 B (5)	51 G 15	71 B (5)	91 G 29	111 B (5)	131 G 42	151 B (5)
12 D 3	32 D 8	52 D 13	72 D 18	92 D 3	112 D 8	132 D 13	152 D 18
13 G 3	33 FRAME ID	53 G 16	73 G 23	93 C 30	113 H (25/50)	133 G 43	153 G 50
14 E 2	34 G 9	54 E 1	74 G 24	94 E 1	114 G 36	134 E 2	154 G 51
15 B (5)	35 G 10	55 B (5)	75 G 25	95 B (5)	115 G 37	135 B (5)	155 G 52
16 D 4	36 D 9	56 D 14	76 D 19	96 D 4	116 D 9	136 D 14	156 D 19
17	37 G 11	57 G 17	77 G 26	97 TEST	117 G 38	137 G 44	157 G 53
18 A (44/50)	38 E 1	58 A (43/50)	78 E 2	98 A (44/50)	118 E 1	138 A (44/50)	158 E 2
19 G 4	39 B (5)	59 G 18	79 B (5)	99 G 31	119 B (5)	139 G 45	159 B (5)
20 D 5	40 D 10	60 D 15	80 D 20	100 D 5	120 D 10	140 D 15	160 D 20

Figure 1.1.1.1 Normal Format

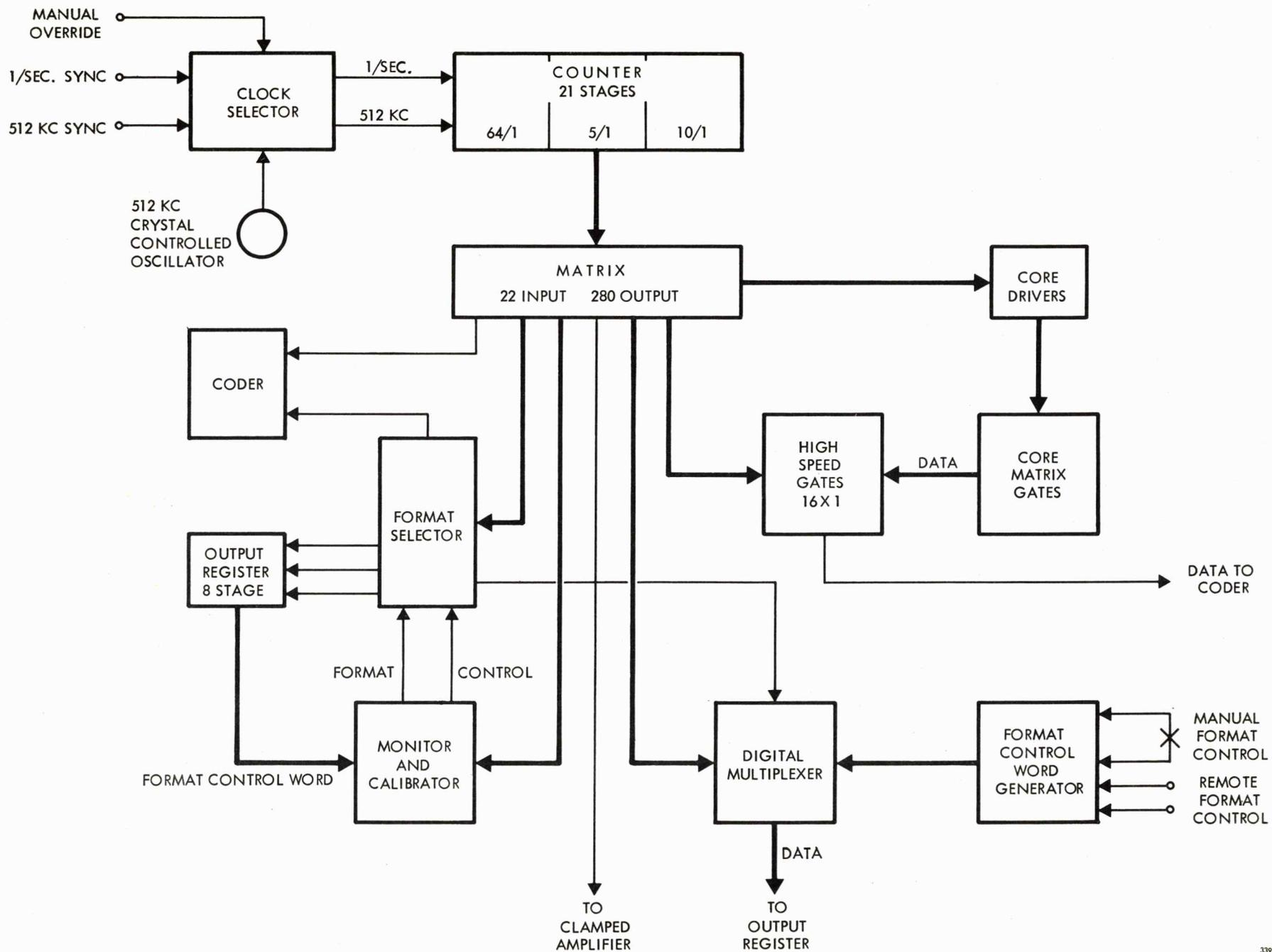


Figure 1.1.1.3-2 Program Generator Block Diagram

The change from Normal Speed to Minimum Data Speed is initiated by a specific word in the format. This word is generated by the "Format Control Word Generator", and it is controlled either remotely from the ground or manually from within the vehicle. One of two unique words will be generated. The first programs normal bit rate and the second, minimum bit rate. The selected word is inserted into the format and is detected by a monitor at the output register. This word will also be detected by the ground station to indicate that bit rate will change in the following frame. The monitor senses the format control word and sends a control signal to the Format Selector. The Format Selector gates the programming to the coder, digital multiplexer and output register, providing for either Normal Speed Output or Minimum Data Output. The change from one format to the other is effected only at the end of a complete sub-commutation cycle so that no break in synchronization occurs. It should be possible to effect similar logic in the ground station. The time of changeover decision is accomplished in the monitor.

1.1.1.3 Flow of Data

Data flow may be seen by referring to Figure 1.1.1. A cascade system is used to limit the number of gates connected to a single output line. The gates of blocks I, II, III, IV and V are of the same type. These are "Bright Switch" transistor gates in which the transistors are made to conduct by a pulse from a winding on a saturating core transformer. (See Appendix A). The gates of block IV are similar, except that a single transformer drives two duo-transistor gates and the gates are designed to be opened for a longer period.

Block VII is made up of high-speed gates, since these individual gates must be opened and closed at the 8 kc word rate to prevent inter-channel crosstalk. The high-speed multiplexer gate obtains its high performance through the use of a matched transistor pair used in conjunction with a square loop core transformer. (Figure 1.1.1.3-1.) The gate is activated when the driver transistor is turned ON by a logical input from the programmer. This action allows current to flow from the V2 supply to ground, inducing a voltage in the primary of the transformer. The collector-base junctions of the gate transistors are forward biased, and clamp the secondary voltage to approximately 0.9 volts. This voltage is reflected through the turns ratio of the transformer to the primary winding. The V2 supply voltage minus the primary voltage establishes a current through R2, which is sufficient to supply drive for the gate transistors and excitation current for the ferromagnetic core. Before core saturation can occur the logic input turns OFF the driver transistor, reversing the current flow in the transformer. This action turns OFF the gate transistors and resets the core of the transformer for the next gate pulse. Since core material with a relatively square hysteresis loop and high maximum permeability is used, the bulk of the excitation current is used to arrive at the knee of the loop, traversing the region of low permeability. Very little current is required to sustain voltage for the bulk of the gating period. This helps maintain drive current regulation for the switch pair. The transistors used for the switch pair have sufficiently uniform drive characteristics to eliminate the need for balancing resistors in series with the bases.

From block VII, the output of the Analog Data Commutator is routed to the Analog-to-Digital Converter, then to the Output Register. The Output Register produces a serial NRZ code which is conditioned by two independent output amplifiers.

An important feature of the system is its self test and calibration facility. Unused channels from each block of gates are selected to provide checking and calibration functions. A high reference voltage goes to one-half of the channels and a low reference voltage to the other half so that both offset and gain may be checked. Portions of this function are shown in Figure 1.1.1.3-2 -- note that block I has an input to 20 gates, block III has an input to 25 gates, and block V has an input to two gates from a high-level standard. At the output of block VI, a low-level standard is gated as an input to the clamped amplifier. A high reference voltage during word 89 and a low reference voltage during word 9 of the 160 word frame are presented once per second to the amplifier input. Once per second during another sub-frame, words 9 and 89, a low reference voltage and a high reference voltage are presented to the coder. These reference voltages provide a check on the offset and gain accuracy of the coder, clamped amplifier and selected gates. To monitor these channels, the digital words are examined either at the coder output (block designated "Calibration Monitor") or at the Output Register (block designated "Output Register Monitor"). Errors in these words exceeding a predetermined weight and number per unit time will cause outputs indicating faults in the system which are related to specific modules.

1.1.1.4 Coding of Analog Data

Analog data is converted into a representative digital code by using the familiar half-split approximation method. Analog signals from the high-level or low-level channels are fed to a sample-and-hold amplifier so that the time that a data sample is taken is precisely known. The output of the sample-and-hold circuit is a current which is proportional to the input sample. This current has weighted constant currents summed to it as described in Appendix B. Current sums other than zero cause different trial currents to be summed with the input until a balance is reached. The currents used to balance the input represent the binary equivalent of the analog input voltage.

1.1.1.5 Synchronization

Two aspects of synchronization are considered here (1) bit rate sync and (2) frame sync. In the case of bit sync, stability can be assured only if frequent transitions occur in every frame. If, by chance, successive words containing full code (i.e., all ONE's) or zero code (all ZERO's) occur, bit errors beyond the specification tolerances may be encountered by the ground station when eight or more channels are at full or zero code. This possibility could be eliminated by limiting full code

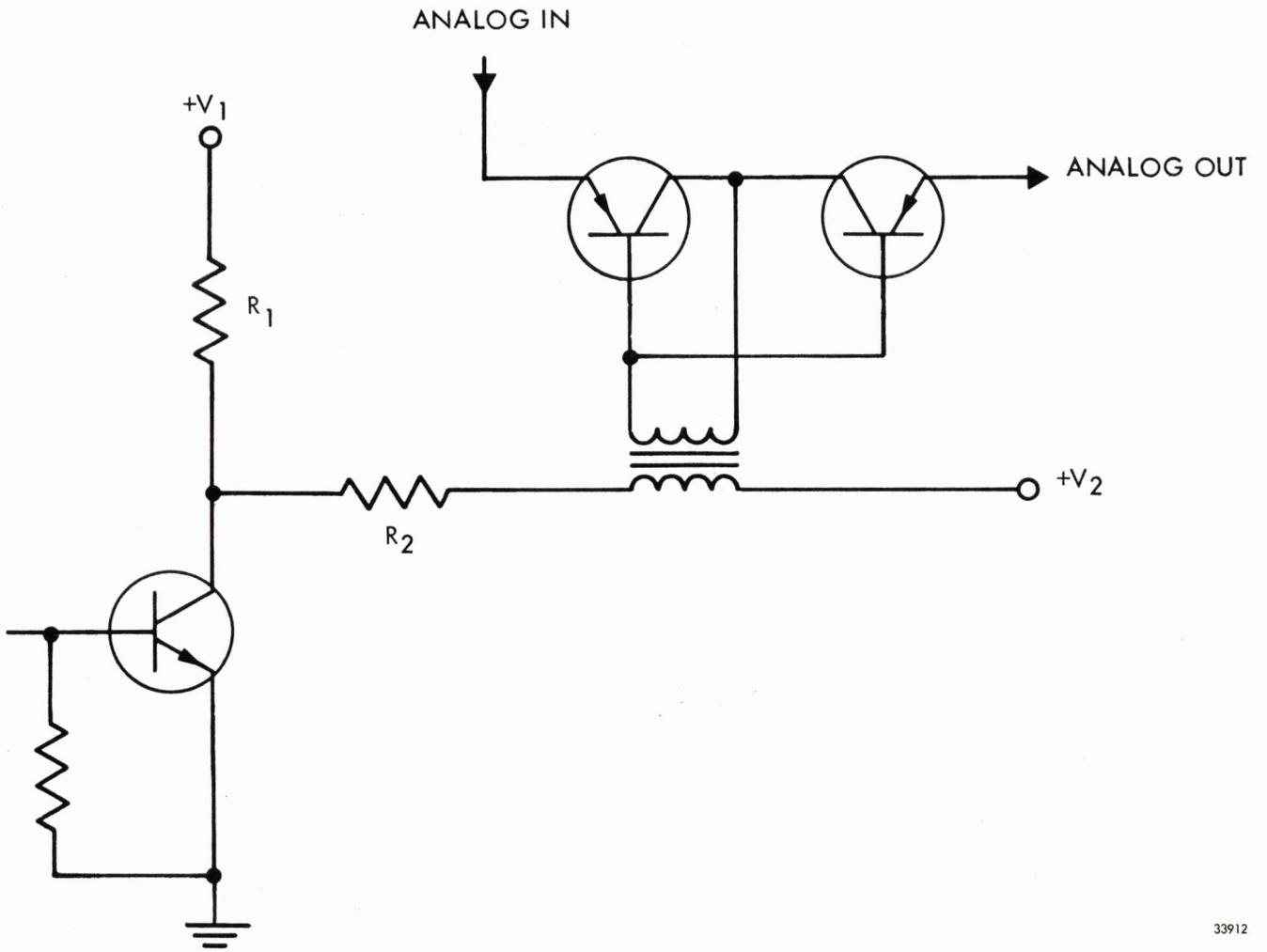


Figure 1.1.1.3-1 High-Speed Multiplexer Gate

to 254 bits and stopping zero code at one bit. This would insure at least one transition in every analog data word with a negligible increase in quantization error (from 0.1961 to 0.1976 per cent). The digital data channels represent a negligible part of the frame and therefore present no problems to bit sync.

Appendix C shows that frame sync should be achieved in three frames or less with a probability of less than one failure in 10^6 . This is accomplished with a pseudo-random type code made up of 23 of the 24 bits available in the three sync words. The relation of the Sync Word Generator to the over-all system block diagram is shown in Figure 1.1.1.3-2. The proposed system incorporates a slight optional addition to this method, which should result in a marked decrease in the failure probability. Alternate sub-frames use complementary sync words. This improves the capability of maintaining synchronization under conditions of severe noise and reduces the possibility of a false sync condition. It is within the scope of the programmer to provide almost any means of achieving frame sync in accordance with the requirements of the ground station equipment. The method proposed is recommended and exceeds the specifications. Sync words can be altered by a simple change of wiring on a small patch panel.

In the minimum data format, one frame has a duration of one second, and sync words occur only once per frame. If frame sync is lost it cannot be regained before a sync word occurs, thus sync may not be regained within the 1/10th second specified. However, the system as proposed is capable of changeover from the normal to minimum data speed, or back to normal, without losing internal sync. Losing and regaining sync at the normal transmission speeds can be accomplished in less than 0.06 second with a failure probability of 10^{-6} . In the slow speed mode, sync could be regained in less than three seconds with a failure probability of 10^{-6} .

Assuming a random occurrence of ONE's and ZERO's in either mode, bit errors should have a probability of much less than 10^{-6} .

1.1.1.6 Power Conservation

Conservation of power utilizing the minimum data format can be achieved by disabling circuitry associated with unused channels. However, the power involved is not significant except in the case of the clamped amplifier. If none of the "C" channels are to be used in the Minimum Data Format (which is the format being discussed), a significant power saving is achieved by removing power from this amplifier during the slow bit rate operation. Power for the clamped amplifier is routed through the Format Selector and switched OFF in the proposed system. Power to other unused circuitry can be controlled in a like manner.

1.1.1.7 Error Analysis

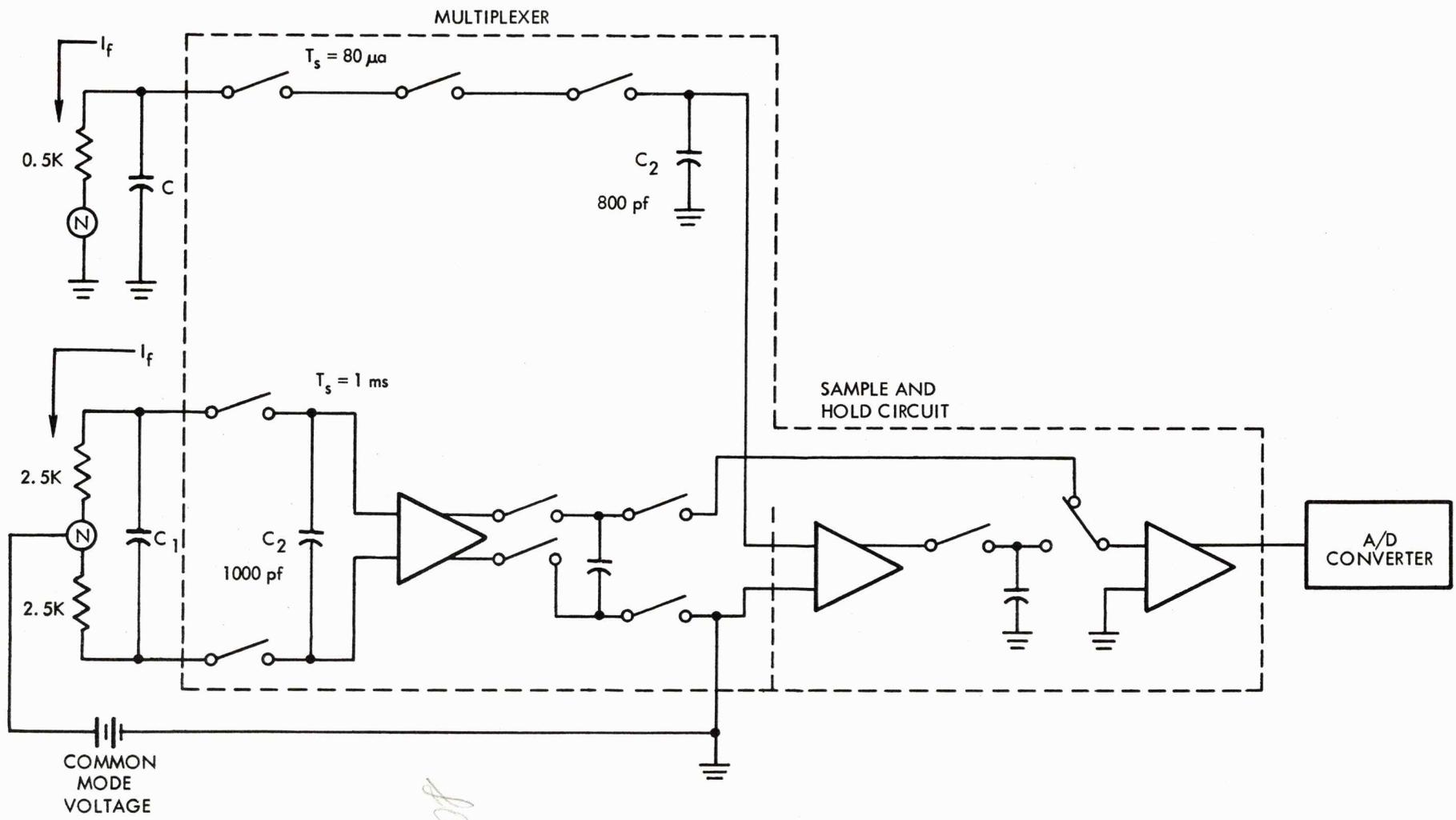
The transfer error of the proposed PCM multiplexer - A/D converter combination is within the specified ± 0.5 per cent analog accuracy specification while the digital circuitry will exceed 10^7 operations without error. All requirements of the specification and subsequent official clarifications have been considered.

1.1.1.7.1 Sources of Error

The signal path followed by the high- and low-level analog inputs is diagramed in Figure 1.1.1.7.1. The worst case conditions of high source resistance, maximum common mode voltage and worst fault conditions are assumed. The high-level multiplexer errors are due to feedback current and gate offset. Crosstalk errors are negligible. Feedback current is a maximum of ± 80 na or ± 0.008 percent. Since three gates are in series, an error budget assignment of ± 200 uv for offset permits a maximum error of ± 0.012 percent. Because of the high input impedance of the sample-and-hold amplifier, errors due to gate ON resistance are negligible. Resistive loading error is ± 0.005 percent. The sample-and-hold circuit has a gain error of ± 0.001 percent, an offset of ± 0.02 percent and nonlinearity of ± 0.001 percent. Pedestal error (caused by switching transients) is limited to ± 0.02 percent. The only significant source of dynamic error is the time uncertainty (aperture time) in the sample-and-hold gate. A maximum of one-half microsecond uncertainty with a 100 cps input results in a ± 0.008 percent error.

The A/D converter error due to combined gain and linearity inaccuracy will be ± 0.1 percent and the peak quantizing error is ± 0.196 percent.

For the low-level path, gate offset will be held to ± 50 uv which corresponds to ± 0.02 percent error. Differential feedback current will be ± 15 na maximum or ± 0.03 percent for the balanced 5K ohm source. The differential amplifier input impedance is greater than 50 megohms so gate resistance errors are negligible. For 0 - 5 K sources, the resistive loading error is ± 0.005 percent maximum. Because of the low bandwidth required for the amplifier, noise may be held to 0.1 mv 3 sigma (± 0.04 percent). Gain will be adjusted to within ± 0.03 percent and the amplifier offset will be within 0.02 percent. Linearity will be better than ± 0.001 percent. The combination of the differential amplifier and the "flying capacitor" will provide a common mode rejection of considerably better than four million to one, or ± 0.0032 percent for a 32 volt common mode input. Because of the "flying capacitor" differential-to-single-ended conversion, only the output amplifier of the sample-and-hold circuit is used in the low-level path. The droop is reduced to ± 0.001 percent as is the pedestal due to the larger capacitor used for holding. The aperture time is increased, but since the input frequency is 500 times less than for the high-level case, the dynamic error is negligible.



Handwritten note: Bus 8

Figure 1.1.1.7.1-1 Input Signal Path

1.1.1.7.2 Error Summation

The prediction of system accuracy depends upon the method chosen for error summation. For both the high- and low-level channels, the error budget assignments listed above are realistic as proven in similar systems. It is predicted that the specified accuracy will be met even with a straight linear summation of worst case errors as shown in Table 1.1.1.7.2. A commonly used alternative to straight summation is to determine the standard deviation of error by assigning each error contributing factor a rectangular probability distribution and taking the square root of the sum of the variances. This method has the restrictions of the central limit theorem and requires random inputs and statistically independent error sources. In examining the error contributors listed in Table 1.1.1.7.2, it is seen that only the low-level noise and crosstalk terms can be said to be random. For the test case, a very non-random input is used, so peak quantizing error must be included, since it is not equally likely that for a given measurement the input signal will be anywhere within the quantizing aperture. Offsets will generally be uncorrelated, but gain and non-linearity terms cannot be said to be independent without conclusive test data on a specific configuration. It is therefore recognized that the most probably correct error summation will lie between a statistical summation and the straight summation, but the straight summation of Table 1.1.1.7.2 gives a pessimistic result and therefore complete confidence that the specified accuracy will be achieved.

TABLE 1.1.1.7.2

HIGH-LEVEL ERRORS		LOW-LEVEL ERRORS	
<u>Multiplexer</u>		<u>Multiplexer</u>	
Feedback current	± 0.008 %	Feedback current	± 0.030 %
Resistive loading	0.005	Resistive loading	0.005
Gate offset	0.012	Gate offset	0.020
<u>Sample and Hold</u>		<u>Amplifier</u>	
Gain	0.001	Noise	0.040
Offset	0.020	Gain	0.030
Non-linearity	0.001	Offset	0.020
Pedestal	0.020	Non-linearity	0.001
Crosstalk	0.001	Common mode error	0.0032
Droop	0.020		
Aperture time	0.008	<u>Sample and Hold</u>	
<u>A/D Converter</u>		Gain	0.001
Non-linearity and gain	0.100	Offset	0.020
Quantizing error	0.196	Non-linearity	0.001
		Pedestal	0.001
		Crosstalk	0.001
		Droop	0.001
TOTAL	± 0.392 %	<u>A/D Converter</u>	
		Non-linearity and Gain	0.100
		Quantizing error	0.196
		TOTAL	± 0.470 %

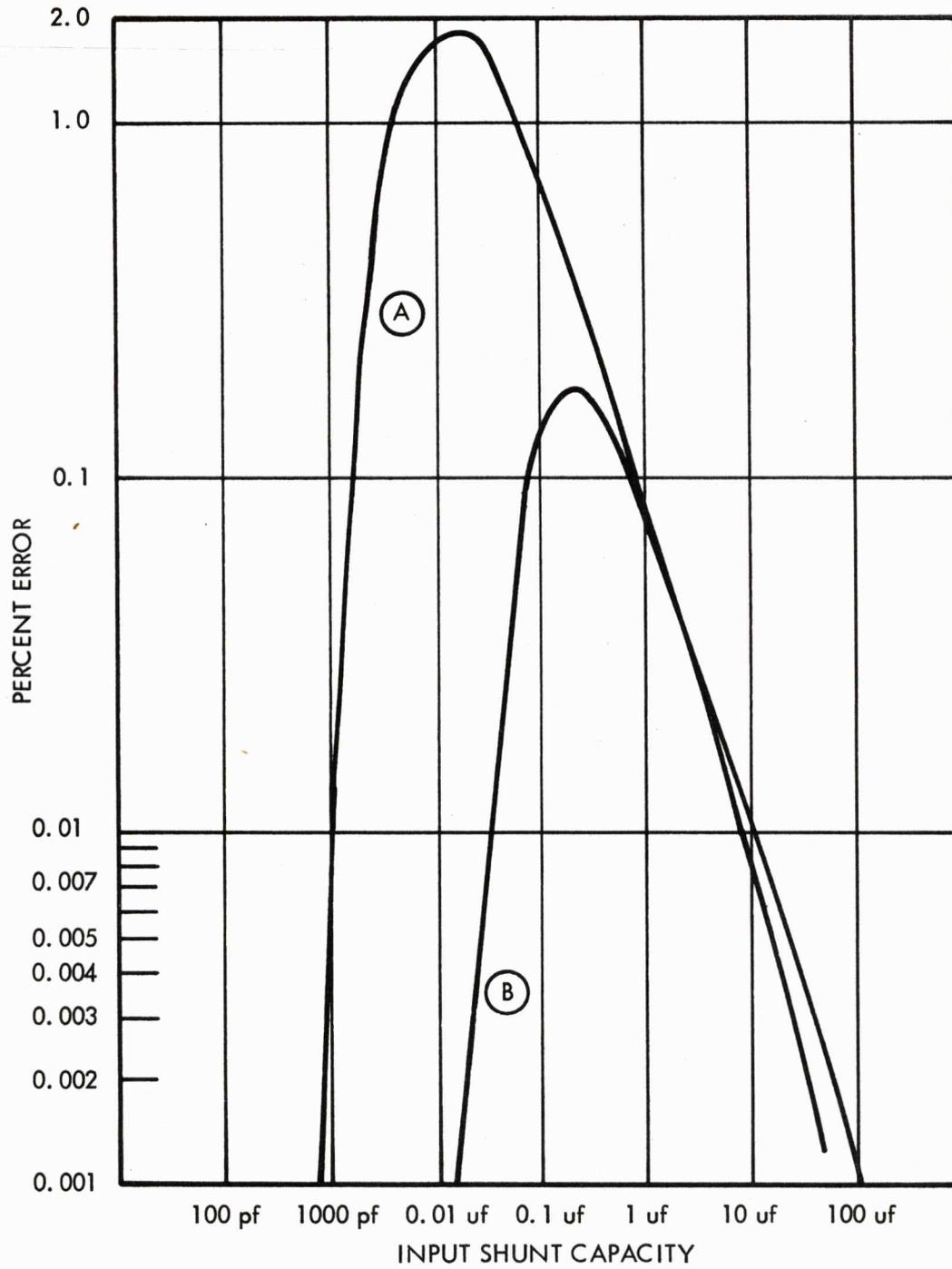
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1.1.1.7.3 Source Capacitance Error

The answer to Question #28 at the bidder's conference requires that the input shunt capacitance limitations of the proposed system be detailed. Finite input shunt capacitances will cause charge transfer errors and low pass filtering errors. Figure 1.1.1.7.1 shows the capacitance values beyond the input gates (C2) as being 800 pf for the high-level circuit and 1000 pf for the low-level circuit. Charge transfer error is given by:

$$\text{Percent error} = \frac{100 C_2}{C_1 + C_2} e^{-\frac{T_s}{R_s (C_1 + C_2)}} \quad (\text{See Figure 1.1.1.7.3})$$

where R_s = source resistance
 T_s = sample time



NOTE:

CURVE A IS FOR HIGH LEVEL WITH $R_s = 5K$

CURVE B IS FOR LOW LEVEL WITH $R_s = 5K$

Figure 1.1.1.7.3 Charge Transfer Error

Low pass filtering amplitude error will be given by:

$$\text{Percent error} = 100 \left(1 - \frac{1}{2\pi f R_s C_1} \right)$$

The equivalent time delay error for any input function may be computed by considering that the response of an RC filter is to delay a ramp function by one time constant ($R_s C_1$).

1.1.2 Reliability

The reliability requirements for the Apollo Telemetry sub-system form the hinge point of the entire design approach. For this reason, a detailed assessment has been made of the sub-system reliability. (See Appendix E, Reliability Assessment).

The results of this analysis are presented in Figure 1.1.2. It is seen that with one spare provided for each module type, a probability of successful performance for 340 hours of 0.9988 is achieved for the telemetry sub-system.

The equipment was sub-divided into the replaceable modules and each of these modules were then carefully analyzed. The total telemetry sub-system reliability requirement (a probability of successful performance for 340 hours of 0.997) was then apportioned among the various modules -- based on their relative complexity and/or relative importance to the successful operation of the telemetry. This apportioned reliability was used as the design goal in the evaluation of each module.

The packaging design considered similar plug-in modules (54 modules - twelve types) so that the high reliability can be achieved without undue sacrifice in weight and size and with a minimum amount of spares.

The spare item concept considered that each of the different module types would have at least one spare associated with it -- even though the reliability requirement can be achieved with some modules without spares. Modules (types A, B, and G) wherein some failures are permitted within 1% of the number of channels, were separated (for analysis purposes) into that circuitry that would cause more than 1% failures (-1 type) and that causing less than 1% failures (-2 type). Effective failure rates were calculated for each to arrive at the module failure rate.

The spare concept also permits analysis based on non-operating stand-by item redundancy. If "s" spares are standing by to support "n" identical modules in a system, we have "(n + s)" modules of this type, and we can withstand up to "s" failures of this module without loss of the system. The spare items will be inserted into the functional scheme by human action. Failure sensing circuitry is used to locate the failed item. Failures in the failure-sensing circuitry were also considered as part of the module failure rate.

The assessment of the number of spares required to meet the reliability specification depends upon two assumptions:

1. Failure rates used for piece part (See Appendix E).
2. The probability distribution associated with stand-by item redundancy from which the reliability will be calculated. The three distributions considered and the conditions under which they are applicable are:
 - Binominal Distribution (worst case for non-operating standby): For the initial reliability estimates presented herein, the binominal expansion theory was used for the calculations. The mathematical model is:

$$R = p^{(n+s)} + (n+s)qp^{(n+s-1)} + \dots + \left[(n+s)C_s \right] q^s p^n$$

where

- R = reliability of module sub-system (including its spares)
- p = reliability of one module
- q = unreliability of one module
- C = algebraic symbol for number of combinations

The failure rate of the non-operating spare item while in standby was considered to be same as in the operating mode (worst case).

- Time-Dependent probability distribution -- different failure rates: When the reliability studies to be performed indicate that a different failure rate exists for the module in the standby and operational mode, the reliability function will be expressed as a time dependent probability by integrating over the time domain the joint frequency distribution, e.g., when one module and one spare have failure rates of λ and λ^1 , then

$$R = p \left(1 + \frac{1}{K} - \frac{1}{K} p^K \right)$$

where

- p = reliability of operating module
- K = λ^1 / λ

MODULE	FAILURE RATE PER MODULE $\lambda \times 10^{-6}$	EFFECTIVE MODULE FAILURE RATE - ALLOWING UP TO 1% LOSS OF CHANNELS -	NUMBER OF MODULES PER SYSTEM (N)	PROBABILITY OF SUCCESS FOR ONE MODULE AND 340 HOURS	INITIAL RELIABILITY APPORTIONMENT (FOR N MODULES)	NUMBER OF SPARES REQUIRED (S)	PROBABILITY OF SUCCESS PERMITTING NO MORE THAN "S" FAILURES
HIGH-LEVEL ANALOG GATE MODULE TYPE A (GATES USED FOR SUPER COMMUTATION ON FAILURE CHECKING)	7.109	—	5	0.99758	0.99976	1	0.99991
HIGH-LEVEL ANALOG GATE MODULE TYPE A-1 (FAILURE CAUSES LOSS OF MULTIPLE CHANNELS)	2.984	—	15	0.99899	0.99946	1	0.99986
HIGH-LEVEL ANALOG GATE MODULE TYPE A-2 (FAILURE CAUSES LOSS OF A SINGLE CHANNEL)	4.125	1.960×10^{-10}					
LOW-LEVEL ANALOG GATE MODULE TYPE B-1 (FAILURE CAUSES LOSS OF MULTIPLE CHANNELS)	3.673	—	5	0.99870	0.99982	1	0.999949
LOW-LEVEL ANALOG GATE MODULE TYPE B-2 (FAILURE CAUSES LOSS OF A SINGLE CHANNEL)	6.100	1.471×10^{-10}					
CLAMPED AMPLIFIER MODULE - TYPE C	16.500	—	1	0.99439	0.99982	1	0.999968
8-BIT CODER MODULE - TYPE D	17.955	—	1	0.99390	0.99981	1	0.999963
OUTPUT REGISTER, OUTPUT REGISTER MONITOR, & OUTPUT DRIVERS - MODULE TYPE E	6.505	—	1	0.99779	0.99996	1	0.999995
DIGITAL MULTIPLEXER GATE MODULE TYPE G-1 (FAILURE CAUSES LOSS OF MULTIPLE CHANNELS)	2.649	—	8	0.9991	0.99994	1	0.999958
DIGITAL MULTIPLEXER GATE MODULE TYPE G-2 (FAILURE CAUSES LOSS OF A SINGLE CHANNEL)	1.781	$.525 \times 10^{-10}$					
16 HIGH-SPEED GATE MODULE - TYPE H	7.410	—	1	0.99748	0.99991	1	0.999994
PROGRAMMER MODULE - TYPE P	9.608	—	5	0.99673	0.99980	1	0.999839
PROGRAMMER MODULE - TYPE I	9.608	—	5	0.99673	0.99980	1	0.999839
PROGRAMMER MODULE - TYPE J	9.983	—	1	0.99661	0.99997	1	0.999988
ROW AND COLUMN DRIVERS - ANALOG MULTIPLEXER. MODULE TYPE M	4.273	—	5	0.99855	0.99982	1	0.999968
CONNECTORS - THAT PORTION AFFIXED TO THE S. E. P. AND NOT REPLACED WITH THE SPARE MODULE	1.144	—	—	—	0.99961	—	0.99961
POWER SUPPLY MODULE - TYPE K	4.686	—	1	0.99841	0.99994	1	0.999998

RESULTS

- (1) INITIAL SYSTEM RELIABILITY APPORTIONMENT (PRODUCT OF ALL MODULE RELIABILITIES) = 0.997
- (2) ACHIEVED SYSTEM RELIABILITY (PROBABILITY OF SUCCESS FOR 340 HOUR MISSION) = 0.9988

Figure 1.1.2 Reliability Analysis

- Poisson Distribution (optimistic case): If the non-operating standby item is considered to have zero failure rate while in standby, the Poisson is applicable. However, this is optimistic because it is generally true that the non-operating units will exhibit a failure rate due to storage, vibration and shock environments.

$$R = p \left[1 + \lambda t + \frac{(\lambda t)^2}{2!} + \dots + \frac{(\lambda t)^s}{s!} \right]$$

p = reliability of one module

The Standby Redundancy is an acceptable approach provided the time to restore the system is considered to be practically inconsequential. The requirement is 0.25 hours.

A preliminary prediction of 0.23 hours mean-time-to-repair for the Apollo equipment has been made using the RCA-RADC questionnaire prediction technique. It is expected that this figure can be improved somewhat in the final design; however, the amount of improvement possible is definitely limited by the requirement to use a special wrench to remove or loosen seven bolts in order to gain access to the replaceable modules.

To insure meeting the reliability and maintainability requirements, Radiation Incorporated will define, implement, and monitor a reliability program based upon that presented in Paragraph 3.3.

1.1.3 Calibration and Self-Checking System

1.1.3.1 Purpose

The purpose of the calibration and self-checking system is to satisfy the requirements of AR-131-3 Para. 3.1.5 and AR-104-3 Para. 3.6. The in-flight test requirements will be accomplished by supplying one output from each telemetry SEP to the NAA IFTS. The output will indicate GO or NO-GO for that specific SEP. The in-flight maintenance requirements will be implemented by having one pin for each module brought out to the front panel connector to indicate GO or NO-GO for each module in that SEP. All of the module condition signals can be compatible with the IFTS equipment so that the IFTS would display failures at the module level. The stimuli for testing will be automatically provided by the telemetry programmer so as to perform the tests when they will not interfere with system operation.

1.1.3.2 Features

The testing scheme proposed has the following features which make it attractive for this application.

1.1.3.2.1 Simplicity

The monitoring circuits contain very few parts and the majority of the components are inactive elements. The complexity of the calibration and maintenance circuitry will be about ten percent of the system or less.

1.1.3.2.2 Sensitivity

The present concept is to monitor each internal circuit which could cause the loss of five or more input channels -- five channels being nearly 1% of the total. The failure would cause one SEP IFTS NO-GO signal to be generated and the in-flight maintenance pin for the specific module would read in the NO-GO state.

1.1.3.2.3 Human Engineering

The test sequence will be performed automatically, continuously, and require the operator's attention only if a failure is induced. The specific module that failed will be located by the internal circuitry and pointed out to the operator via the test plug or, at option, through the IFTS. The module number can correspond to the connector pin numbers in order such that pin R will always be module 1, pin P always module 2, etc. The external stimuli may be used to reset the error indicator if required.

1.1.3.2.4 Fail-Safe

The absence of a voltage indicates a failure. Also, the input standard circuitry, the circuitry being tested, and the comparison circuitry will either be tested through other tests or all three be included in the same module. This checks against a false GO condition because two highly selective failures in two of the three circuits would be necessary to provide this false condition. The input standard and the circuitry tested will normally be in the same module. By comparing the two standards one to the other during the test the accuracy of the standards is checked.

1.1.3.2.5 Adaptability

The system can easily be adapted for more or less checking and also to perform more sophisticated tests, if required.

The circuit can be given a decision making capability such that it would indicate a NO-GO condition only if a specified number of errors occur within a specified length of time.

1.1.3.3 State-of-the-Art

No components or circuit techniques are envisioned that have not been previously studied or used in now operating Radiation telemetry systems. Improved transistors are used which may not be on the Minuteman parts list at this time, but which can undoubtedly qualify.

1.1.3.4 Design Trade-Offs

This system is proposed because of its simplicity and reliability. No improvement in performance, or other features, would be anticipated by the addition of complexity. In the same manner it facilitates flexibility and maintainability.

1.1.3.5 Block Diagram

Figures 1.1.3.5,1 through 1.1.3.5,3 will be used to describe the types of testing that can be incorporated into the telemetry system. The types of tests fall into the following different categories.

- | | |
|--|--|
| (1) <u>Calibration Tests</u> | (2) <u>Signal Flow Test</u> |
| <ul style="list-style-type: none">● Analog-to-Digital Converter● Low-Level Amplifier● Single Analog Gates that have inputs from five or more channels. | <ul style="list-style-type: none">● Drivers● Inverters● Flip-Flops● Counters● Diode Matrix |
| (3) <u>Continuity Test</u> | |
| <ul style="list-style-type: none">● Core Matrix Rows● Core Matrix Columns | |

1.1.3.5.1 Calibration Tests

Figure 1.1.3.5.1 shows the test scheme to check the calibration of the Analog-to-Digital Converter. Two tests are made. The first test will use a voltage 0.5% of full-scale above zero to measure the offset voltage. The second test will use a voltage 0.5% less than full-scale to measure full-scale accuracy. The acceptable limits for both tests can be made adaptable to the contractor's requirements. Calibration limits that are integral powers of two would be preferred. Figure 1.1.3.5.1-1 also indicates the fail safe feature on the block level. If one block in the module fails, a second block out of the two would have to fail in an exactly opposite manner to within 0.5% to cancel the first failure. Whether the failure be due to standard input, circuits under test, monitor or output standard, it will be corrected by changing modules. The digital outputs of the coder can also be transmitted to the ground for verification via the spare output words.

The low-level amplifier and the analog gates that have inputs from more than one channel are tested in a similar manner -- except in these two cases the calibrated input plus the circuit under test and the gates between it and the coder are located physically in the same module. The coder module, which is checked first, is then used as the output standard and monitor. The failure signals can be interlocked so that an amplifier and/or gate will not indicate failure when the coder fails and the coder will not indicate failure when the other modules are at fault. Figure 1.1.3.5.1-2 is a block diagram of the low-level amplifier testing circuitry.

1.1.3.5.2 Signal Flow Test

Signal flow tests are made on the active digital circuits. In this type of test the output of the circuit is compared with the input to see that the circuit reacts properly when the input is present and does not react when the input is not present. Figure 1.1.3.5.2 is a block diagram of this type of test. The test does not interfere with the operation of the circuit but actually tests the circuit while in use. Again, the complete test circuit is included in the same module with the circuitry being tested or the test circuitry is common to other test functions.

1.1.3.5.3 Continuity Test

In the first level analog gates, only one channel goes through each gate. The loss of one gate would cause the loss of only one channel. However, the loss of a row or column in the matrix would cause the loss of five or more channels. The row and column lines on the first level gates are checked for continuity. The second and third level gates are calibrated individually because they involve five or more channels each. Figure 1.1.3.5.3 is a block diagram of the continuity checking test. This test is performed continuously and does not interfere with circuit operation.

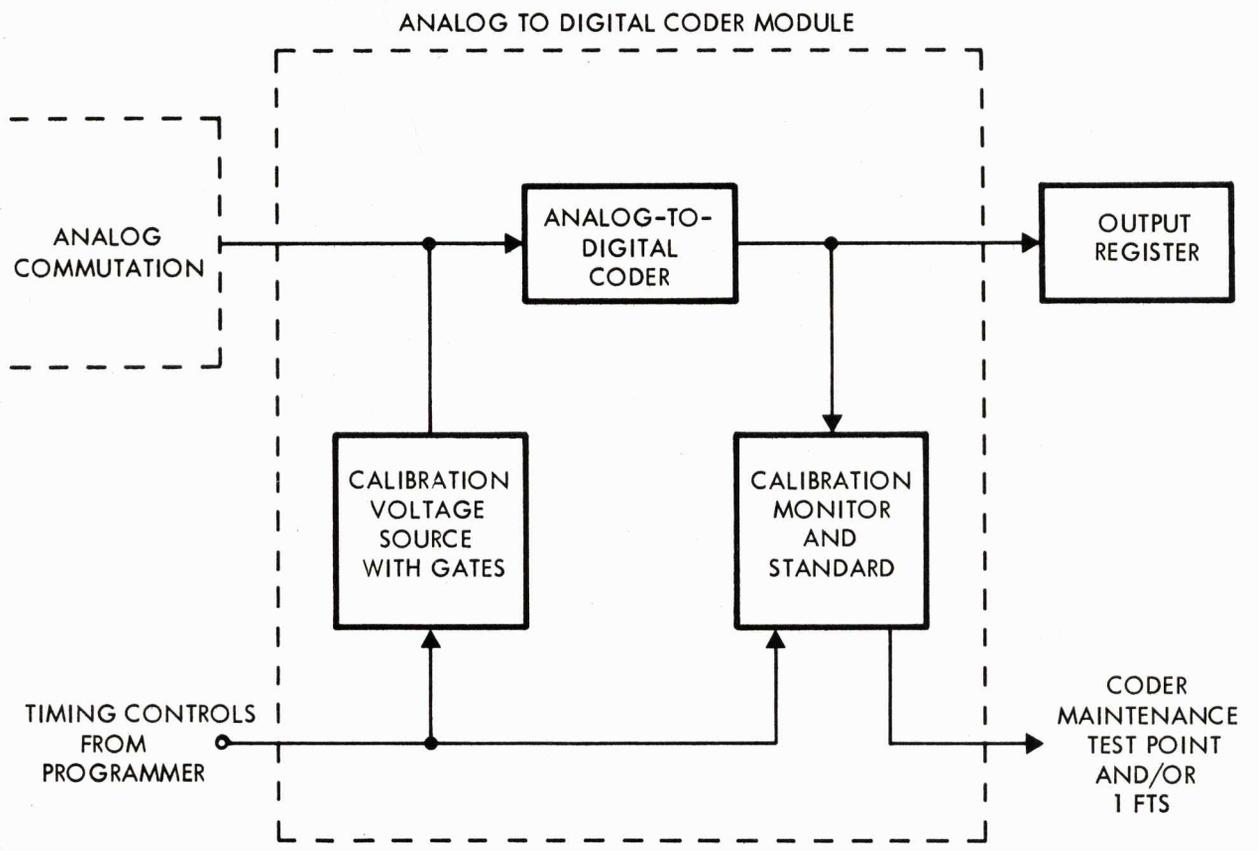
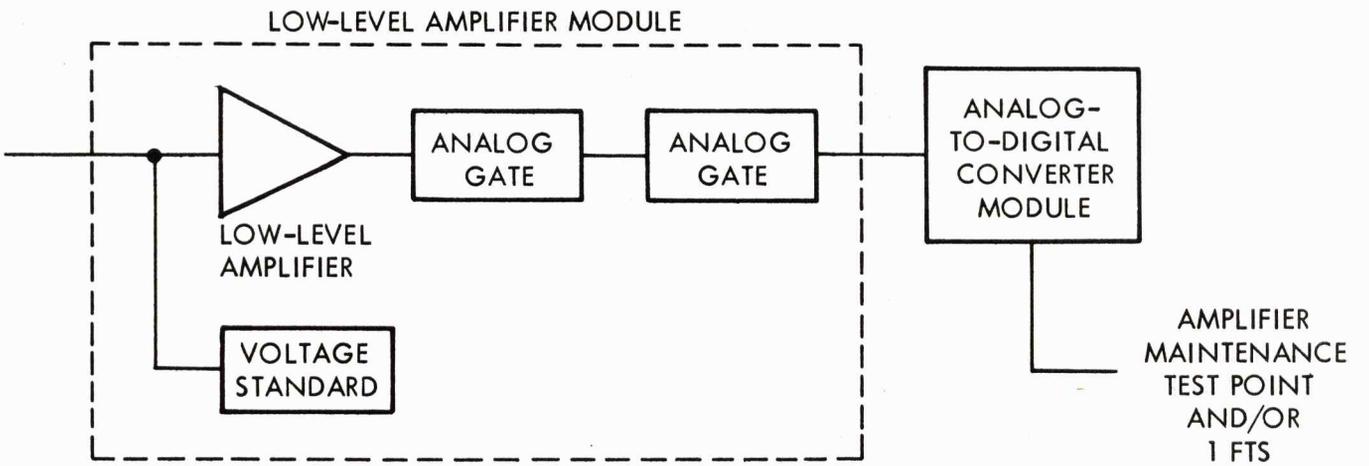


Figure 1.1.3.5.1-1 ADC - Block Diagram

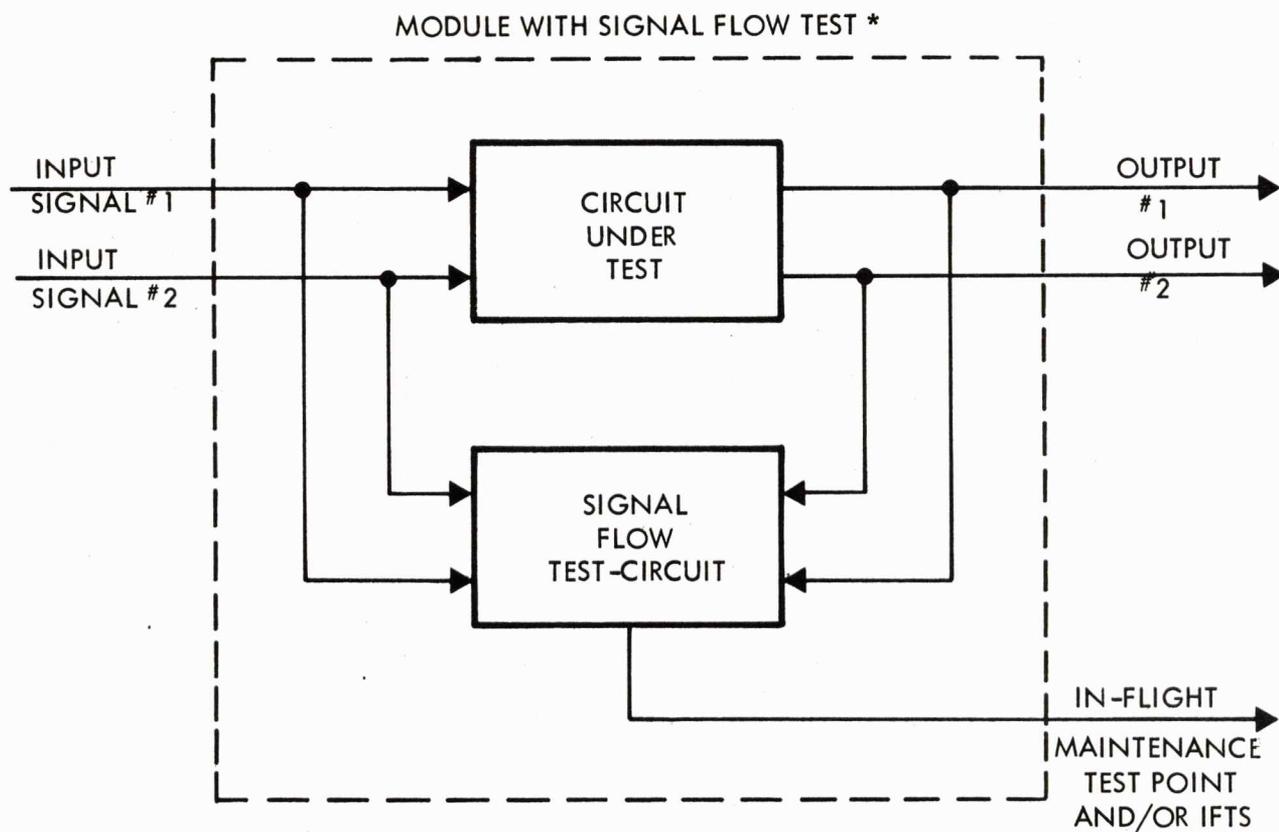
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Figure 1.1.3.5.1-2 Amplifier - Block Diagram

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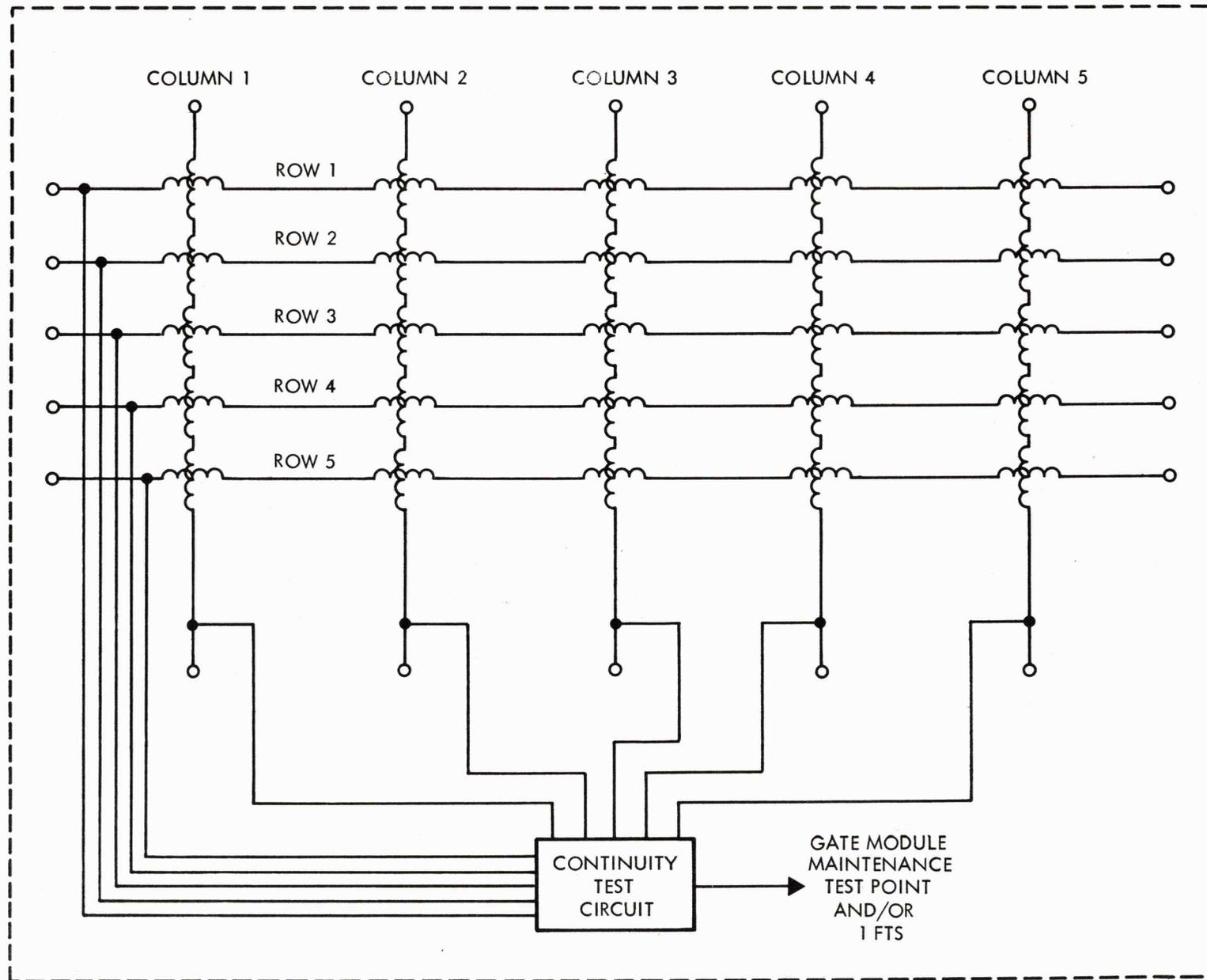


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Figure 1.1.3.5.2 Signal Flow, In-Flight Test

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ANALOG GATE MODULE



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Figure 1.1.3.5.3 Continuity Test Diagram

1.1.4 Packaging

Radiation Incorporated proposes full compliance with the CRC Specification in all areas relating to mechanical design and packaging. Arrival at this position has been attained with considerable study and debate of packaging approaches, many requiring deviations from the specification, but which hold potential advantages in the areas of weight, reliability and maintainability. We feel obligated to offer the results of this study and analysis to the Apollo Program and so include an alternate packaging concept in Appendix G of this proposal.

1.1.4.1 Interpretations

The following interpretations of AR104-3 are presented as a basis for the packaging details to follow:

1. A maximum of 500 pins is allowed for double SEP connectors; these connectors must be located as shown in Figure 3-10 of AR104-3; and, the 500 pins may be contained in more than one connector.
2. Maintainability of the system must include replaceable plug-in units, but the level of replaceable unit is dependent on reliability, weight, replacement time and cost.

1.1.4.2 Package Description

The telemetry system is completely housed in three double SEP units of the following lengths:

<u>Unit No.</u>		<u>Length</u>	<u>Module Quantity</u>
1	High-Level Multiplexer	14 inches	20
2	Coder/Low-Level Multiplexer	10 inches	12
3	Programmer/Digital Multiplexer	15 inches	22

Each SEP contains two rows of single width modules of the prescribed dimensions, and one inch in thickness. Modules contain either one or two Cannon 37 pin D series connectors depending on quantity of pins required. There are 54 total modules in the system of the following types and quantities:

MODULE SUMMARY

<u>Type</u>	<u>Function</u>	<u>Quantity</u>	<u>Type</u>	<u>Function</u>	<u>Quantity</u>
A	High-Level Gate	20	H	High-Level, High-Speed Gate	1
B	Low-Level Gate	5	I	Programmer	5
C	Low-Level Amplifier	1	J	Programmer	1
D	Coder	1	K	Power Supply	1
E	Output Register	1	M	Gate Driver	5
G	Digital Multiplexer	8	P	Programmer	5
TOTAL					54

The required reliability figure is achieved with one spare module of each discreet type. Further improvement in reliability predictions is readily obtained by increasing the spares quantity. A weight versus reliability trade-off curve is shown in Figure 1.4.4.

The module design and construction follow the details specified in AR104-3. Each module consists of a one inch thick cast aluminum frame which supports a G-10 fiberglass printed circuit card, and the 37 pin Cannon connectors. Right-angle pins were considered for connecting the printed circuit to the connectors, but these have been discarded in favor of insulated hook-up wire which provides the required stress relief.

The electronic components are assembled in welded sub-modules of cordwood configuration, potted in polyurethane foam and mounted directly to the printed circuit card of the module. The polyurethane foam is a veteran of three satellite programs --- Nimbus, Telstar, and OAO. Either Freon or carbon dioxide blowing agent is available without effect on cost or delivery. Specific approval for the use of this foam will be requested upon award of contract, per 3.4.4.8 of AR104-3. The repairability of the sub-module is not significantly hampered by the foam encapsulant, since it may be readily removed -- and since the assembly drawing of the sub-module is a photographic enlargement of the actual configuration, location of the faulty area or component is simple.

1.1.4.3 Weight

The weight of the basic system without spares is 56.97 pounds. The weight of spare modules required to achieve

the 0.9988 reliability figure is 8.4 pounds. For maximum reliability within the 80 pound maximum limit, the addition of 10 more spares provides a probability of operation after 340 hours of 0.99961, which is the connector limited figure. Further possibilities of weight reduction are described in the alternate packaging concept in Appendix G. That alternate approach is, in fact, a concentrated attempt to reduce weight while maintaining reliability and performance levels.

1.1.4.4 Thermal

In this discussion, only the effects of conduction to the thermal interface material are considered. The neglect of both radiation and convection lends conservatism to our values, particularly under sea level conditions. The near vacuum conditions of outer space and the low temperature differences encountered with this packaging technique are further evidence of the validity of these assumptions.

The multi-module packaging approach in accordance with the Design Criteria Specification simplifies the thermal analysis in many respects. Our thermal dissipation per unit conducting area is of such low value that we may further neglect the beneficial effect of adjacent (cooler) modules in determining our worst case. Specifically, we may treat our worst case module as an entity without regard for surrounding influences which, by definition of "worst case" must necessarily reduce the temperature differential we would experience by isolating that module from other packaged circuitry.

In contrast to the use of metal component boards, the conventional printed circuit for intersub-module wiring is proposed. Inter-component wiring is effected by nickel ribbon welding, subsequently encapsulated with urethane foam to complete the sub-module. A sub-module here refers to a welded assembly of resistors, capacitors, transistors and other electrical lumped constant devices. This is to avoid confusion with the "Collins Module", a field replaceable element in each equipment.

A maximum of two component boards are placed within each module with the circuit sides of these cards placed face-to-face within the module and separated by an insulator. The foamed components are thereby pressed into intimate contact with the module conducting faces. Each module is comprised of two halves, identical investment castings, which, when joined, form the completed module in accordance with Collins Design Criteria Specification. Each module half is an open-faced enclosure such that all heat given up to the relatively large face is conducted without seams or joints to one 2.25 square inch face which bears directly against the thermal interface material. Thus, the proposed technique, through printed circuit cards, achieves the effect of metal component cards by virtue of detail construction. See Figure 1.1.4.4-1 for a view of module construction.

As a result of using identical halves to "build" a module, we may further reduce our worst case thermal model to a single casting and a single printed circuit card. The full compliance of our packaging to the Design Criteria Specification is assurance that we may conduct thermal tests in the exact manner specified.

There is a problem in obtaining the large temperature rise in the fluid with the small thermal dissipation of our equipment. Flow rates will be almost infinitesimal depending upon the source and return pressures. The greater the pressure drop across our cold plate, the greater the temperature rise due to adiabatic expansion through the throttling device.

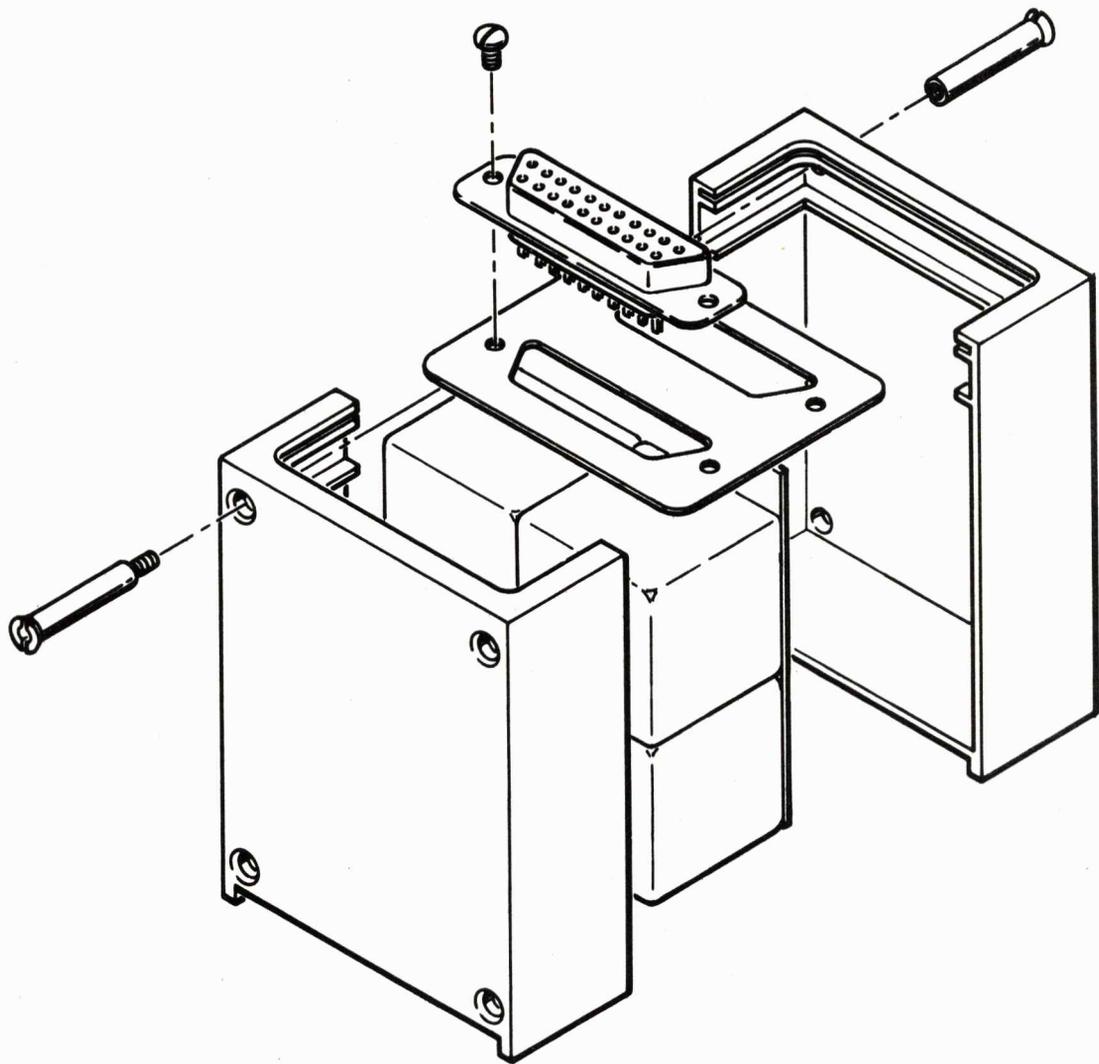
The majority of heat removed by the cold plate will be due to the chamber environment and the throttling mentioned previously, with only a small percentage contributed by component thermal dissipation. A variable orifice at the inlet will be used to obtain the flow rate needed to achieve the specified temperature rise across the cold plate. Our facilities are fully equipped to simulate the cold plate, pigeon-hole thermal installation outlined by the specification.

Figure 1.1.4.4-2 is a worst case study report based upon combining our highest heat density module with our greatest component dissipation. The interface material temperature gradient is an assumed value based upon typical RFI gasketing such as silicone impregnated woven stainless steel mesh. Certainly, sound detail design of conventional finger stock assemblies could effect substantially less thermal drop than the material we have used in this example.

The temperature gradient from the 1/4 watt resistor to the sub-module surface is based upon actual measurement as determined from our Telstar, OAO, and Nimbus PCM systems.

1.1.4.5 Vibration Effects

It is expected that the initial mechanical design will result in sub-module resonances which will coincide with input frequency in the 200 to 500 cps range. Since the structure of the SEP package is complex for accurate analytical solution, a mechanical model of the SEP package will be built for vibration test and analysis. This model will simulate actual weights, size, configuration and construction techniques and will be monitored at critical internal locations to determine G-levels that the electronic components and connectors would realize. From these results the mechanical design will be altered as necessary to bring the acceleration forces down to acceptable levels. The final design will be established by modifying the mechanical model to conform to that design and re-running the qualification level vibration tests. Although not a specification requirement, the mechanical model is considered to be one of the most valuable aids to achieving qualification of the system without mechanical redesign. Radiation's experience on previous satellite programs has provided invaluable data on limits that components, solder joints and weld joints can withstand. This data will serve as the principal criteria for internal acceptance of the mechanical design.



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Figure 1.1.4.4-1 Replaceable Module Exploded View

1. EQUIPMENT
2. MODULE NO. OR NAME
3. BOARD NO. (WHERE APPLICABLE)
4. MODULE DISSIPATION (WATTS)
5. BOARD DISSIPATION (WATTS)
6. BOARD THICKNESS (INCHES)
7. INTERFACE MATERIAL R_T - ($^{\circ}\text{C IN.}^2/\text{WATT}$)

CODER NO. 1

2

2

.06

8. INTERFACE MATERIAL BASE AREA - IN.^2
9. $\Delta T_1 = R_T Q/A_{IM}$
10. $\Delta T_2 =$ (FROM FIGURE 3-16) AR-104-3
11. $\Delta T_1 + \Delta T_2 = K$
12. DATE
13. PREPARED BY

2.0

$4(2)/2 = 4^{\circ}\text{C}$

6.2 $^{\circ}\text{C}$

10.2 $^{\circ}\text{C}$

8-15-62

W. CORRY

1	2	3	4	5	6	7	8
COMPONENT DESIGNATION	TYPE OF COMPONENT	COMPONENT DISSIPATION (WATTS)	MANUFACTURER'S MAX TEMP LIMIT ($^{\circ}\text{C}$) (SEE NOTE 1)	MAXIMUM ALLOWABLE OPERATING TEMP ($^{\circ}\text{C}$) (SEE NOTE 2)	ΔT_3 ($^{\circ}\text{C}$) (SEE NOTE 3)	$\Delta T_3 + K$	DESIGN MARGIN (SEE NOTE 4)
	RESISTOR (CARBON COMPOSITION)	.25	100	25	8	18.2	6.8

NOTES:

1. MAX JUNCTION OR BODY TEMPERATURE
2. FROM PARAGRAPH 3.3.2.1.
3. $\Delta T_3 =$ CALCULATED JUNCTION OR BODY TEMPERATURE RISE ABOVE MOUNTING SURFACE TEMPERATURE.
4. COLUMN 5 MINUS COLUMN 7.

Figure 1.1.4.4-2 Module Thermal Analysis

1.1.4.6 Other Environmental Effects

Ability of the mechanical model, and the subsequent E-model and D-model to safely pass the sine/random vibration tests provides a high degree of confidence that the system will safely pass the specified shock and steady state acceleration tests. The "solid mass" configuration of the SEP yields an assembly which is highly resistant to effects of shock and acceleration.

No degradation of performance or reliability is expected to result from the high altitude test. Previous Radiation Incorporated designs of similar equipment have safely undergone up to 13 days at 10^{-6} mm Hg while being cycled between -5°C and $+55^{\circ}\text{C}$. By using materials and components in the Apollo design which have previously passed such tests we achieve maximum confidence that the Apollo telemetry will safely pass the specified 10^{-4} mm Hg, four-day period.

Acoustic noise tests are not expected to produce any degradation of performance or reliability. The conclusion results from: (a) the natural component frequency being several hundred cps and (b) the foam encapsulant providing excellent acoustical attenuation at those frequencies. The sound pressure level at the expected box resonance and the low coupling efficiency of the package is expected to result in an induced vibration level on the components of 3 to 4 g's, which is an extremely safe margin.

Humidity tests at 120°F and 95% RH for 360 hours yields some cause for concern. Humidity testing to date on the foam sub-modules has consisted of the same RH and temperature as above, but for shorter periods of time. One of the first pre-qualification tests that will be run, then, is long term effects of 95% RH on the foam encapsulant. No trouble is expected since none has occurred in the past. However, should moisture seepage occur there are at least two ready solutions -- (a) apply a conformal epoxy coating to the entire module before potting or (b) apply a flexible sealer over the sub-module after foam potting.

Fungus non-nutrients are used throughout. All non-metallics will be carefully re-evaluated for fungus growth support properties.

The rain test can be passed satisfactorily by two methods -- (a) adequately sealing the SEP such that water cannot enter or (b) potting all exposed circuitry, contacts and wiring internally to resist the moisture. Radiation's approach will be the former if a study of the problem reveals it to be practicable; if not, approach (b) will be employed.

Explosive atmosphere tests are not expected to present any problem since the telemetry system contains no switches or spark producing contacts.

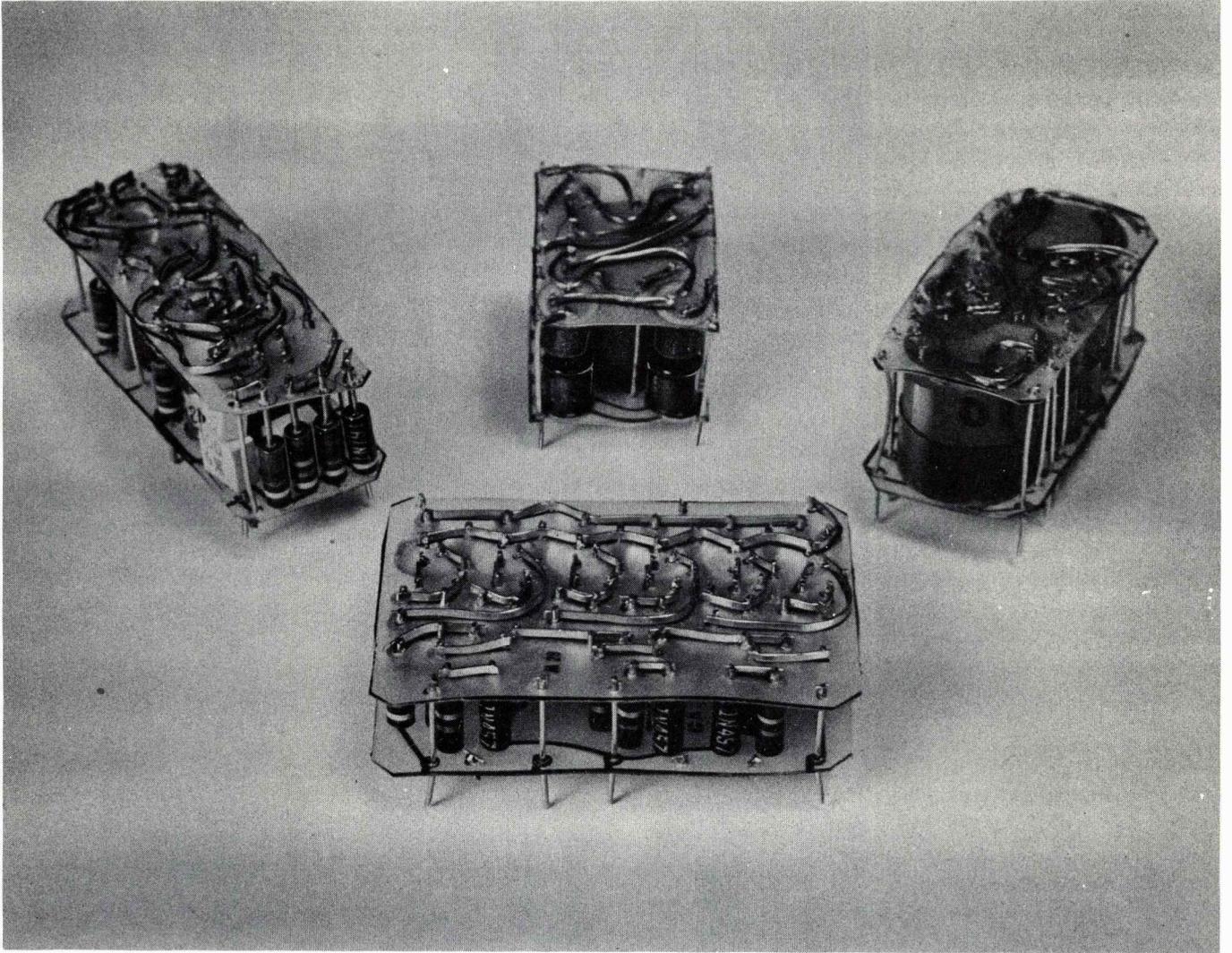
Sand, dust and salt spray requirements are easily met by the efforts in complying with rain and humidity specifications.

Ozone, a particularly active form of oxygen, will simply speed up any reaction that would occur between oxygen and some other element. By choosing materials which do not readily combine with oxygen, the effects of ozone atmosphere will be reduced to a safe level.

The specified nuclear radiation levels are not of such severity to cause degradation of the semiconductors or other materials. Although silicon devices are more susceptible to radiation than germanium, the energy level is not high enough to consider using the lower performance germaniums.

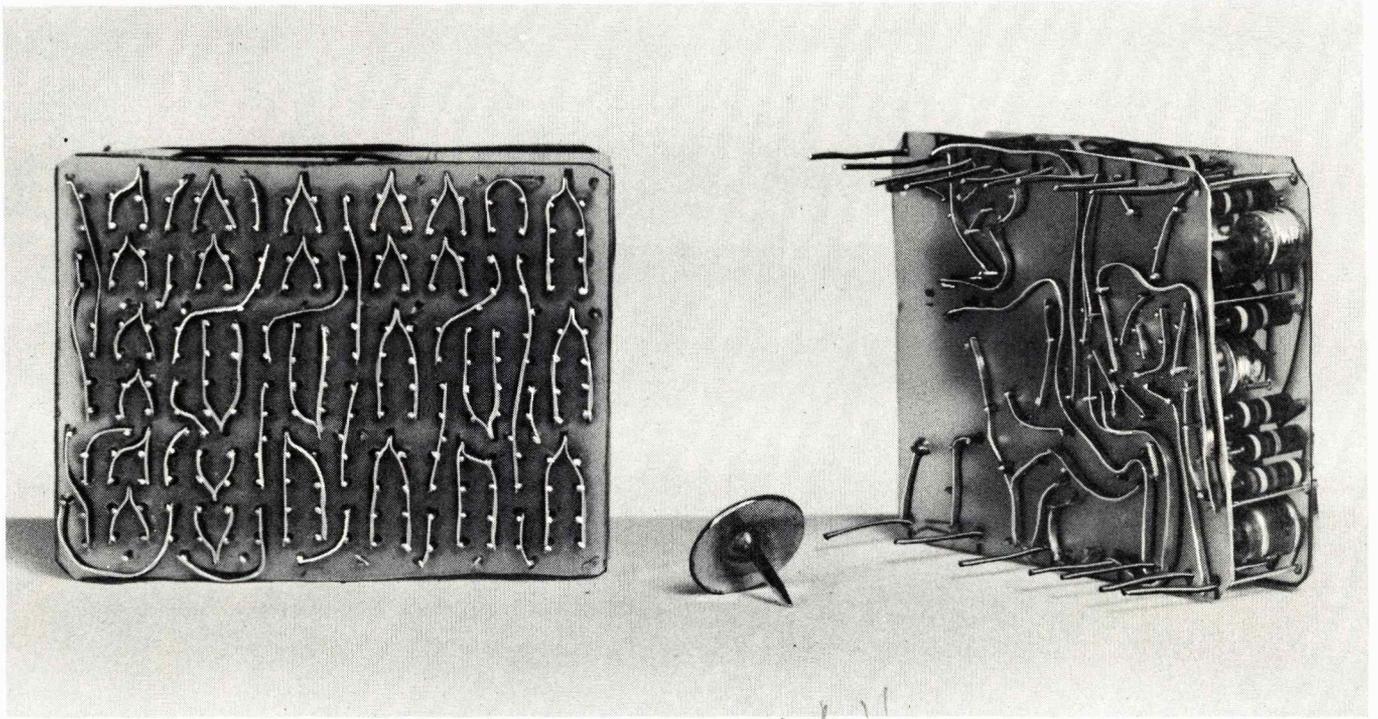
1.1.4.7 Welded Sub-Module Design and Fabrication

The welded sub-module design proposed for Apollo is the same design that has proved successful for Radiation on the Nimbus, Telstar and OAO satellite programs. Figures 1.1.4.7-1 and -2 show several examples of the welded cordwood construction prior to foam potting. The welded joints are provided supplementary support by a conformal coating of epoxy over the inter-connecting ribbon surface. After potting, the sub-module is mounted flush to a printed circuit card via leads protruding out the bottom of the sub-module. The height of all sub-modules mounted to a common card is held constant through the use of accurate potting molds. These sub-modules, then, all being of the same height, provide a regular top surface which can accept a distributed compressive load from an adjacent card assembly or from a flat plate. This is exactly what is proposed for supporting the card assembly against the severe shock and vibration forces. See Figures 1.1.4.7-3, -4, and -5 for photographs of sub-module card assemblies. The replaceable module assembly design includes provisions for holding the card assemblies in that module under compression, thus extending to the sub-module level CRC's "solid mass" approach to the SEP design. The distributed forces on the foam sub-module are on the order of 20 psi. This technique has been employed on the satellite programs previously mentioned with excellent results. Whereas amplifications of input vibration levels often reach 10 and 15 to 1 (yielding 100 to 150 g's with a 10 g input) for conventional printed circuit assemblies supported at the edges only, Radiation has been able by the compression technique to reduce amplifications to a maximum of 3-5 to 1 for various systems. With the maximum vibration input specified in AR104-3 of 13.5 g rms, a 3 to 1 amplification would yield maximum internal G-levels of 40.5 and a 5 to 1 amplification, a maximum of 67.5 -- both well within the limits that components and interconnections can withstand in the 200-500 cps range. Frequencies above 500 cps are effectively damped out by the foam sub-module, and frequencies below 200 are below the natural frequency of the SEP. In addition to the low amplification provided by foam sub-modules, the damping effect of the thermal

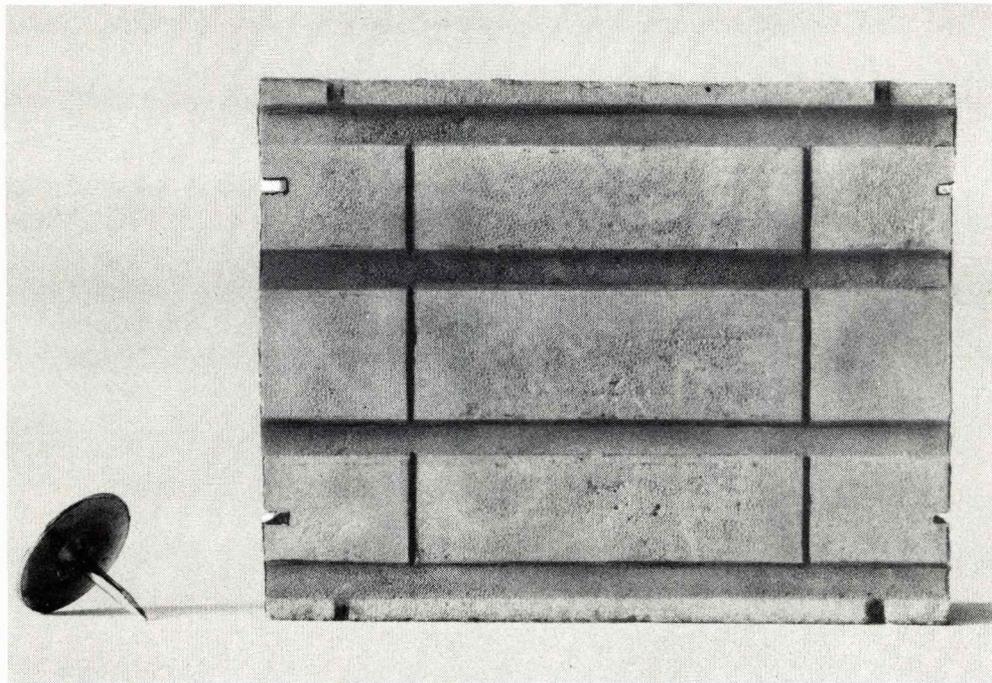


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Figure 1.1.4.7-1 Welded Cordwood Construction

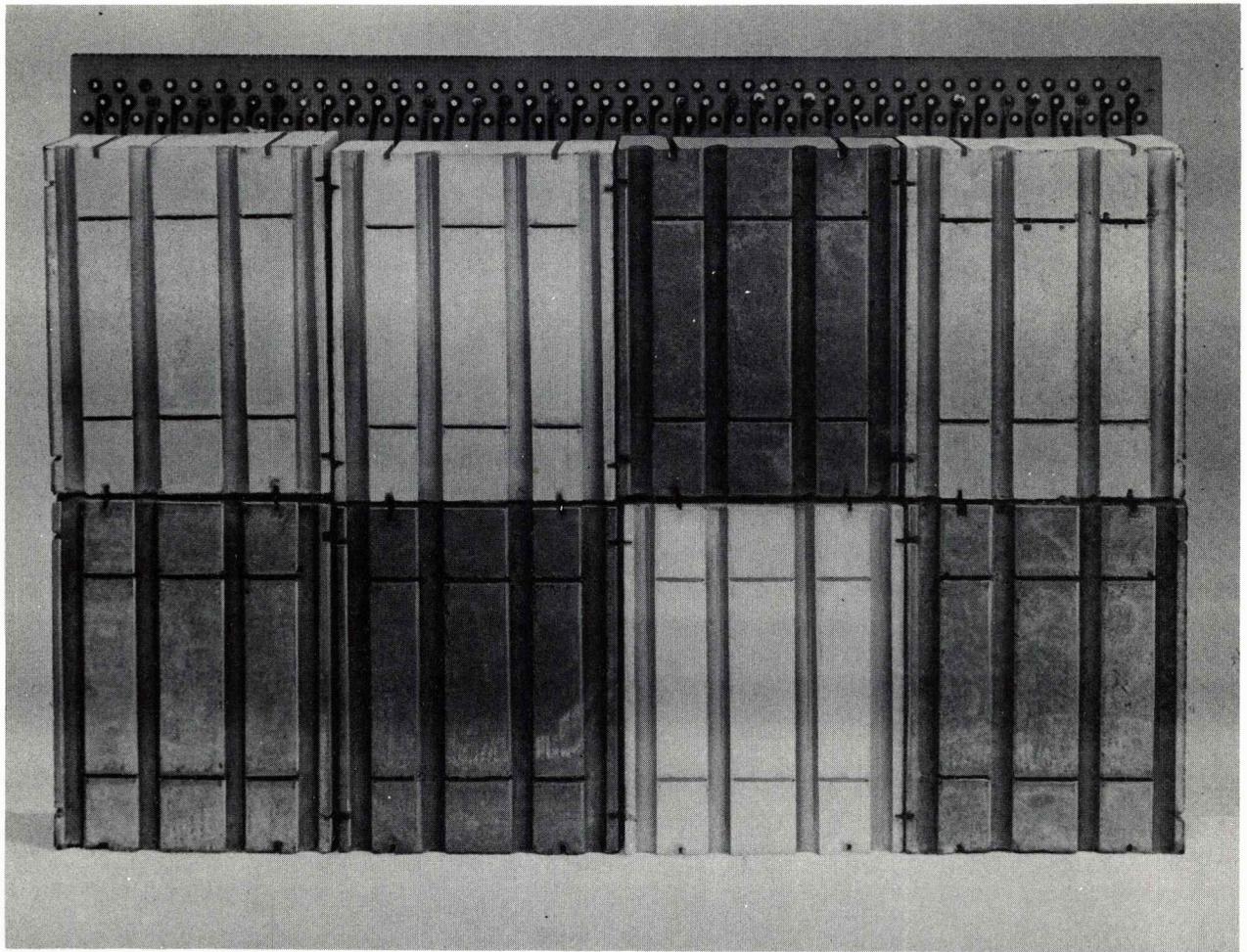


Slide 11



Slide 12

Figure 1.1.4.7-2 Welded Cordwood Construction



35141

Figure 1.1.4.7-3 Sub Module-Card Assemblies



35091

Figure 1.1.4.7-4 Sub Module-Card Assemblies



32721

Figure 1.1.4.7-5 Sub Module-Card Assemblies

interface material between the SEP and the mounting plate is expected to provide additional damping, thus lowering the G-level seen by the SEP. Further, the weight of telemetry system should serve to lower the natural frequency of the spacecraft rack to a level below that of the individual SEP's, thus preventing overlap of resonances.

1.1.4.8 Elapsed Time Meter

An elapsed time meter is provided as required in Section 6.4 of AR131-3. Details on location and mounting arrangement will be coordinated with CRC.

1.2 THEORY

1.2.1 Data System

1.2.1.1 Low-Level Multiplexer

To handle the low-level data, a 100 channel multiplexer and clamped amplifier are used. The multiplexer is of the core matrix type described in Appendix A. The output of all channel gates are paralleled, and presented at the input of the amplifier. The low-level amplifier is a unique design, using a system of clamping to compensate for feedback current and voltage offset. This process is described in Appendix D. Because of the high common mode voltage presented to the amplifier, the entire amplifier is floated above ground, and then "boot-strapped" to the common mode voltage. This configuration reduces the effective common mode, as seen by the amplifier, to less than one volt. The output of the amplifier is a high-level differential voltage riding at the common mode voltage above ground. To convert from a differential to single ended voltage and eliminate the common mode voltage, a "flying capacitor" is used. A diagram of the scheme is shown in Figure 1.2.1.1-1. During the operational period of the amplifier, the charge gate G1 is closed allowing the transfer capacitor C1 to charge to the differential output voltage of the amplifier. When C1 is fully charged, G1 is opened and the transfer gate G2 is closed. The voltage across C1 now appears as a single ended input to the coder. The common mode rejection of this transfer scheme is the ratio of the distributed capacity on the high side of the signal line, C2, to the transfer capacity C1. This ratio can easily be made 1000 to 1. The over-all common mode rejection is the product of the amplifiers rejection of its one volt common mode (20,000 to 1 easily attainable) and the transfer scheme's rejection ratio; hence 20,000,000 to 1 is attainable.

1.2.1.2 Analog-to-Digital Converter (Coder)

The coder proposed for Apollo is of the half-split type described in Appendix B. Several unique features are incorporated which improve its accuracy and stability over the usual airborne type coder. The weighted currents are generated by constant current sources as shown in Figure 1.2.1.2-1. Zener diode Z, transistors Q1 and Q2, and R3 form a normal constant current source. Z is used as a reference for all current sources. Resistors R1 and R2 divide the voltage drop of D1 and D2. The ratio of R1 and R2 is chosen to exactly compensate the temperature characteristics of the V_{be} of Q1 and of Z. The magnitude of the current from the source is determined by R3. To provide high-speed operation of the circuit, the current is not switched on and off as dictated by the input signal, but is diverted from the current summing bus, when not used by the current control flip-flop operating through D3 and D4.

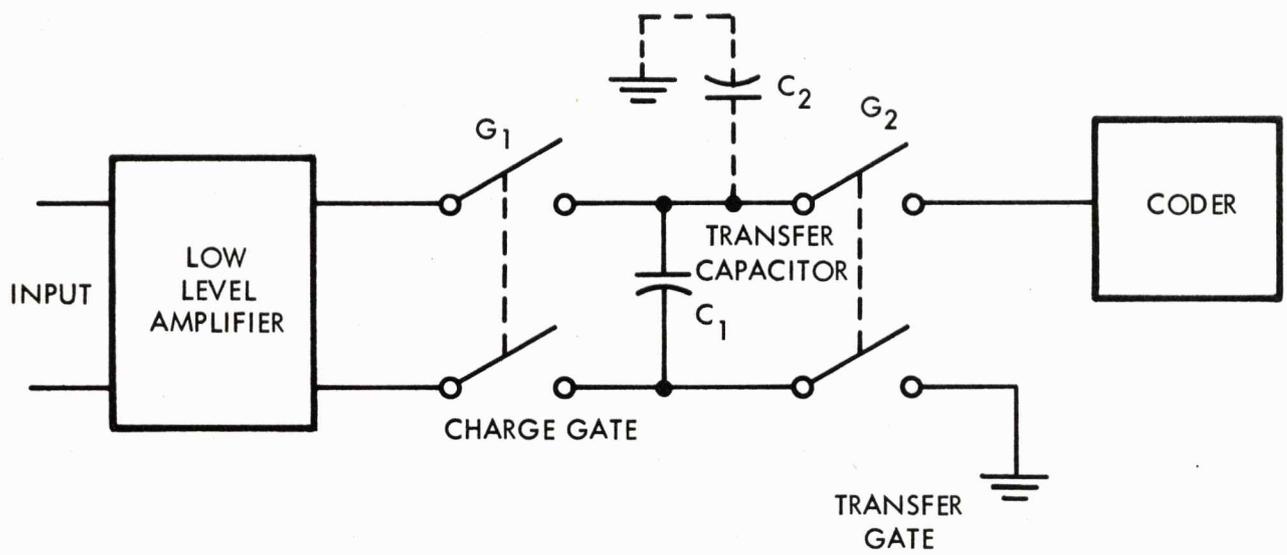
In the past, the speed of the half-split coder has been limited by the response time of the current generating resistors, and a practical bit rate limit has been 350 kc. Using the above technique, bit rates in excess of 5 mc have been realized with very low power consumption. The proposed coder will operate at a bit rate of approximately 1 mc. This rate is in excess of the system word rate requirement, but reduces the hold time of the sample-and-hold amplifier, thus reducing its error contribution to the system. This scheme is commensurate with an increase in bit rate to 128 kc.

The sample-and-hold amplifier is shown in block form in Figure 1.2.1.2-2. It is of the conventional type. When a data channel gate is closed, the sample gate is also closed. Just prior to encoding of the analog signal, the sample gate is opened, and the analog input is retained on the hold capacitor. This prevents changes of the input analog from affecting the code output.

1.2.1.3 Program Generator

The designs are well proven -- used by Radiation in Minuteman, Telstar, Nimbus, OAO and many other telemetry systems. The clock oscillator is a quartz crystal controlled, transistor type, and includes shaping amplifiers, gates and a band pass amplifier.

The counters used are the two transistor flip-flop type with diode steering. The matrix consists of an array of diode gates driven by the flip-flops. Two extra counter stages will be used to reduce the logical connections in the matrix. The addition of four transistors with associated diodes, resistors, and capacitors will be offset in the saving of a few hundred diodes in the matrix.



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Figure 1.2.1.1-1 Flying Capacitor Diagram

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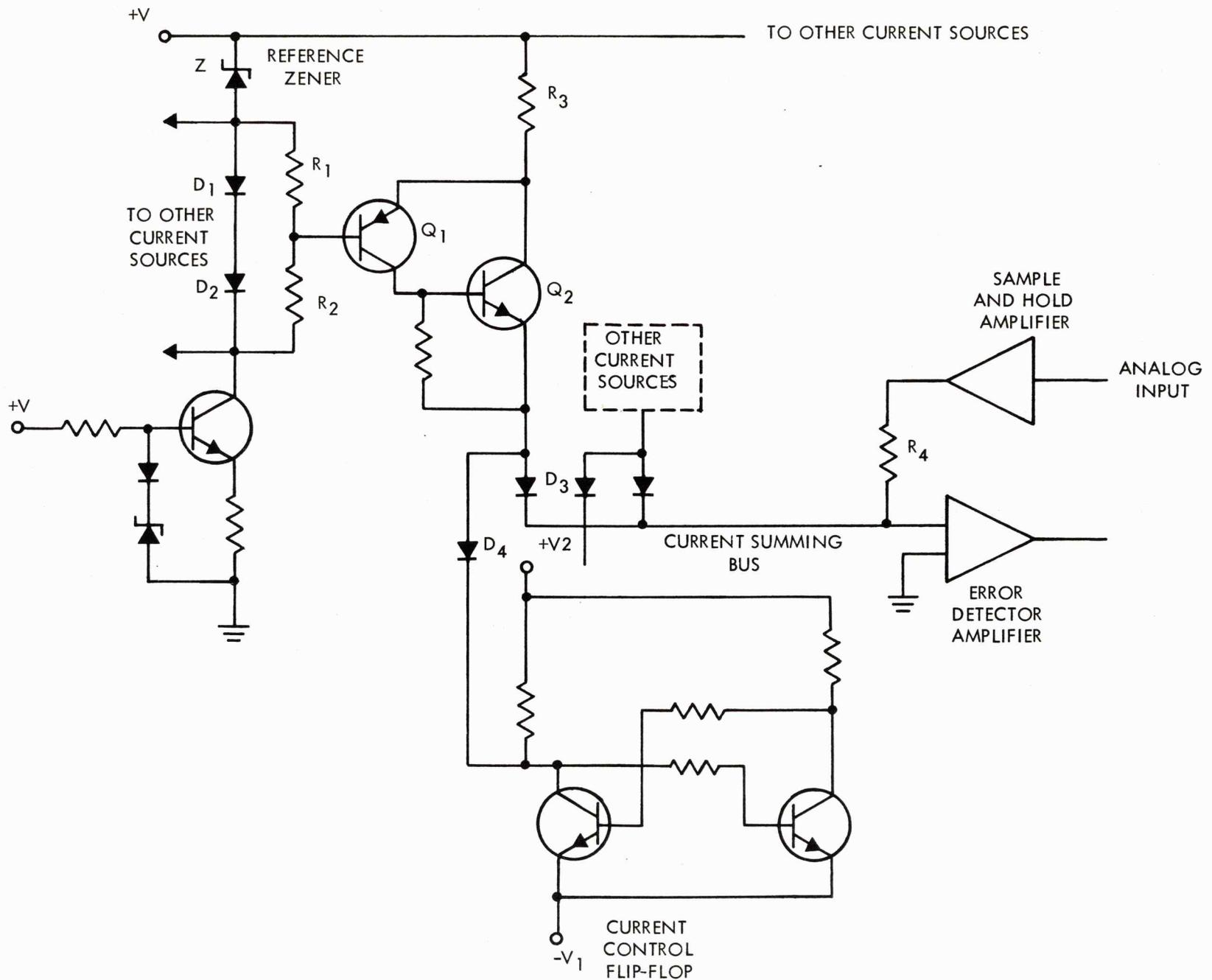
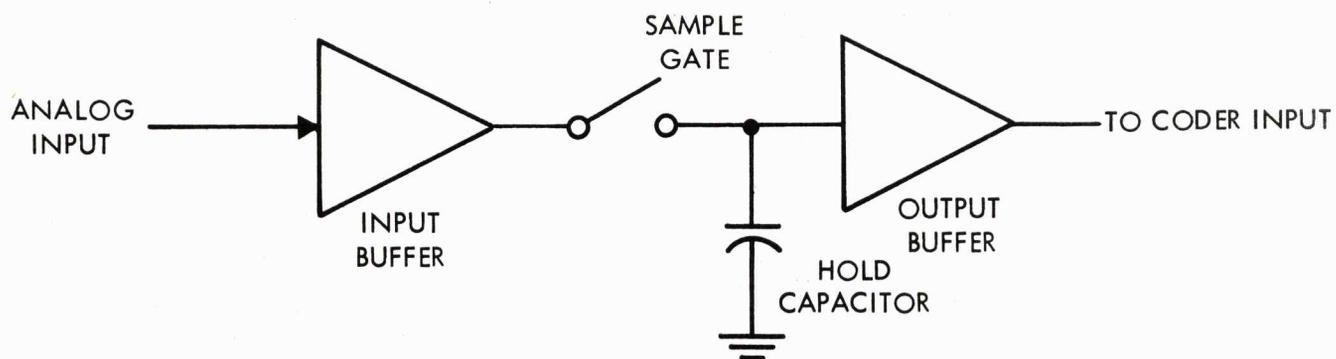


Figure 1.2.1.2-1 Coder Current Generator and Control Circuits



33920

Figure 1.2.1.2-2 Sample and Hold

1.2.1.4 Digital Multiplexer

The Digital Multiplexer serves to gate the digital channels and the identification word into the output register section of the telemetry equipment. The Digital Multiplexer receives the necessary commands from the telemetry programmer so as to gate the digital information into the output register according to the required frame format. The Digital Multiplexer is required to read into the output register in a minimum length of time so that the number of output register stages can be the minimum of eight. This rapid read-in feature requires that the read-in time be as shown in Figure 1.2.1.4-1. The read-in pulse-width can be one-fourth of a bit time and will have to occur between the time that the eighth bit of the n^{th} word is read into the code flip-flop and the first bit of the $(N + 1)$ word is required to read out.

This scheme requires only that the Digital Multiplexer be operated $1/4$ of one bit per word which means it has a $1/8 \times 1/4 = 1/32 = 0.0312$ duty cycle. This duty cycle allows a 97% power savings in the multiplexer by only applying power during the shortest interval required. Figure 1.2.1.4-2 shows the block diagram of how Radiation implements the low power Digital Multiplexer. The power switch is turned ON only for one-fourth of one bit per word. The power switch output is then applied to each digital word driver. Only the one digital word driver called out by the frame format is turned ON at one time. The controls from the programmer enable the correct digital word driver. The digital word driver then enables the eight individual bit gates such that the digital word can be immediately read into the output register. The drivers and power switches will be monitored for in-flight maintenance and the IFTS. The bit gates only effect one bit of a digital word and present plans do not require individual channel monitors.

1.2.1.5 Output Register

The output register receives digital inputs in parallel by bit and series by word on eight lines from both the digital multiplexer and the analog-to-digital coder. The block diagram of the output register is shown in Figure 1.2.1.5-1. The blocks shown can all be in the same module to facilitate the self checking feature. The shift registers will be similar to those used in the OAO system except the OAO output register was redundant. It should be noted that no reset circuitry is included. The reset function is accomplished by shifting ZERO's in as the word is shifted out. The serial output of the shift register is used to drive the NRZ code flip-flop which generates the PCM waveform at the command of the programmer. The NRZ code flip-flop also serves as a storage element for the last bit of each word while the following word is being read into the shift register. The NRZ code flip-flop drives the two output amplifiers of the system. The in-flight monitor serves to test the output register and other fixed words such as the frame synchronization words and the format code word. The output register is tested by first reading in one test word and monitoring the output and then reading in that word's complement and checking it. If the frame synchronization words set all of the registers in each of the two conditions the output register test could be performed using these and the output register test words omitted. The output register test words are transmitted for ground station verification.

The output register timing of the read-in, read-out and shifting pulses is given in Figure 1.2.1.5-2. The read-in pulses gate the broadside information into the register. The read-out pulses gate the shift register output into the code flip-flop and the shift pulse actuates the serialization function of the shift register.

The changes required for the reduced bit rate occur primarily in the programmer. The read-in pulses for the omitted words are inhibited from gating the digital multiplexer and the analog-to-digital converter into the output register. This allows only the words in the reduced frame to enter the output register. Shift pulses and read-out pulses are inhibited such that only those required at the reduced bit rate reach the output register controls. If the shift and read-out pulses are changed from 64 kc to 1.6 kc, then output bit rate will also change from 64 kc to 1.6 kc.

1.2.1.6 Power Supply

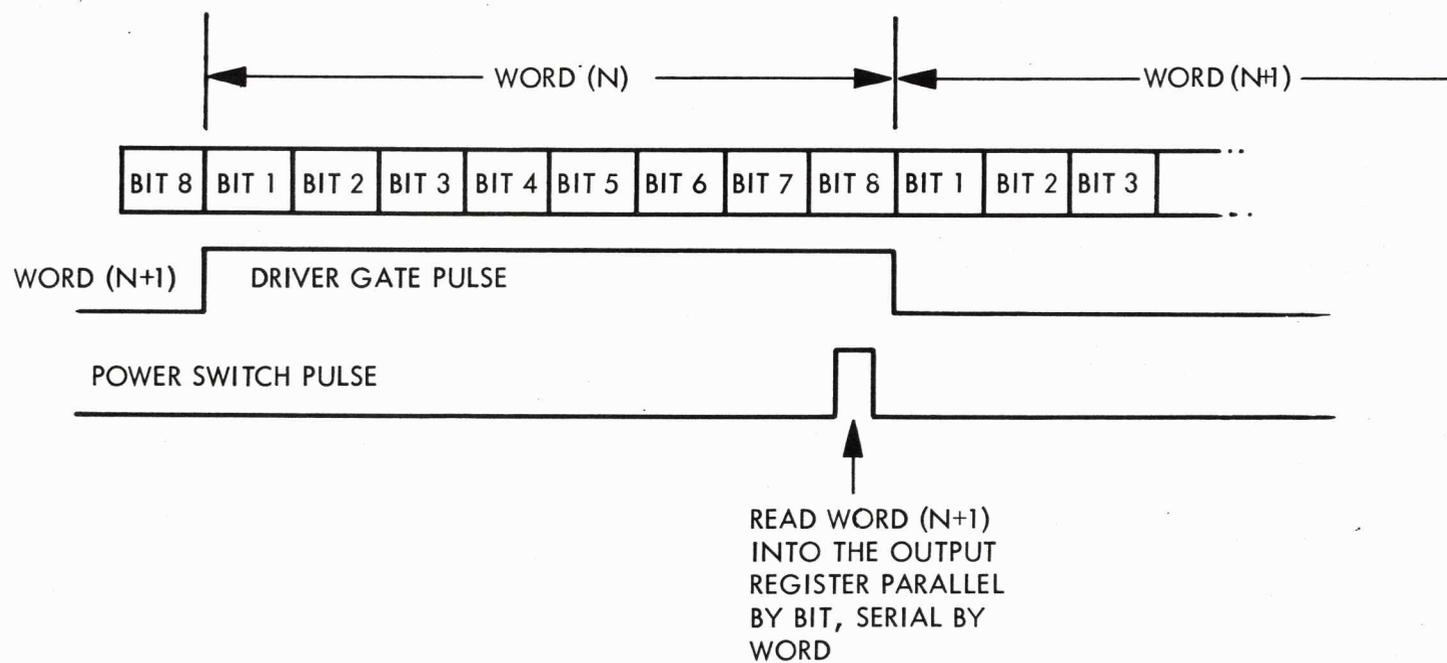
The power supply which derives the various dc voltages for use in the system will be of the three phase full-wave type. While only single phase excitation will be required, all three phases are used to provide a phase balanced load, and prevent loss of the telemetry equipment during loss of one phase of the primary supply. Ripple filters on the output dc will be designed to give adequate filtering on single phase operation. The above approach is somewhat heavier than the use of a single phase supply, but the increase in reliability more than offsets this penalty. The power required during normal rate is estimated at 5.25 watts and during minimum rate 3.4 watts.

While the system specification calls for the use of ac as the primary source of power, dc could be used if required for reasons of power available from the vehicle's prime supply.

1.2.2 Calibration and Self-Checking System

1.2.2.1 General Theory

The prime purpose of the calibration and self-checking system is to detect any failure which could cause the loss of 1% or more of the channels and locate the fault to one specific SEP and one specific module. The IFTS equipment is notified of the faulty SEP location and the module location is represented on the front panel test connector. The module locating signals can be compatible with and may be used by the IFTS if required.



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Figure 1.2.1.4-1 Digital Multiplexer Timing

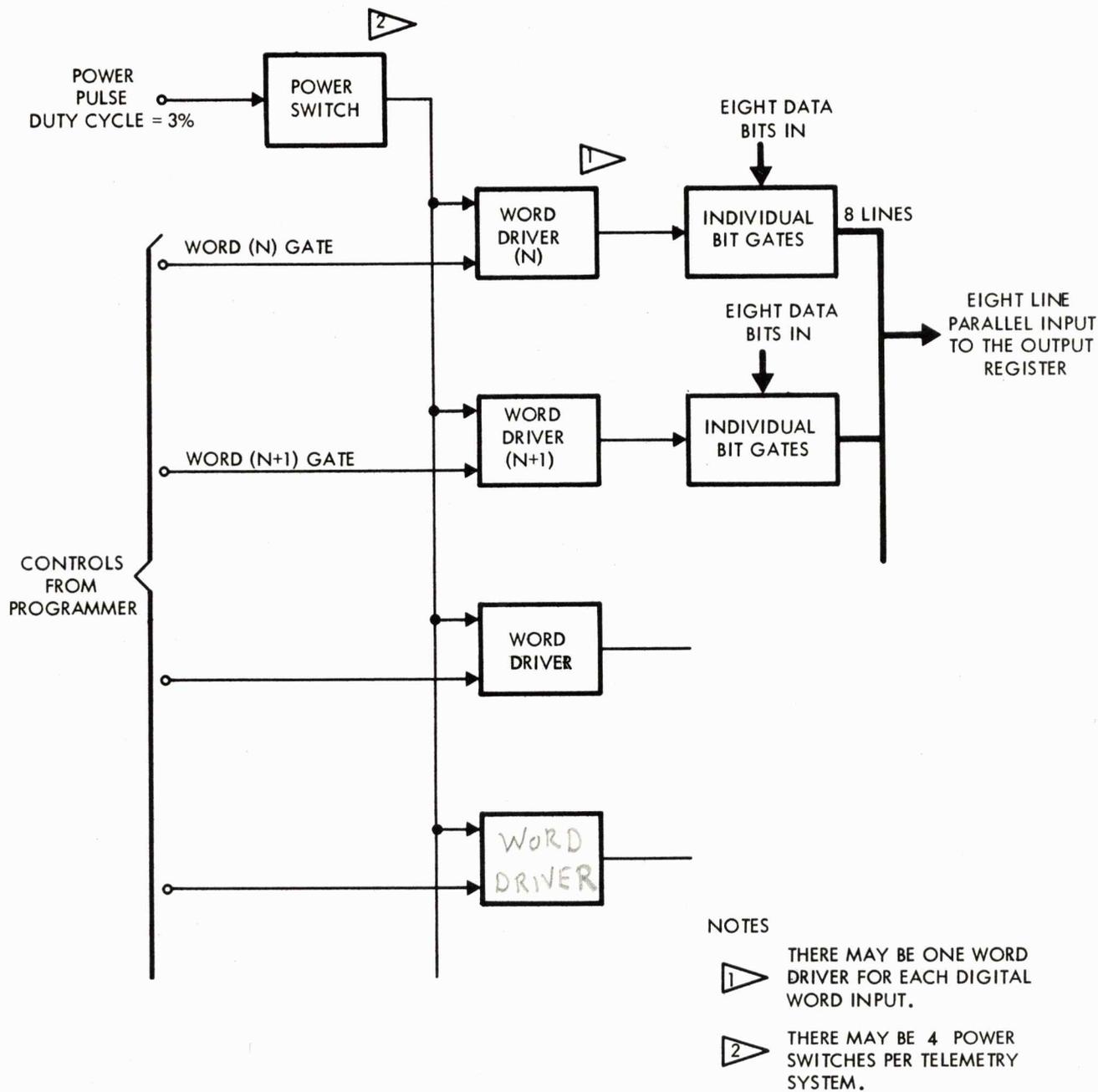
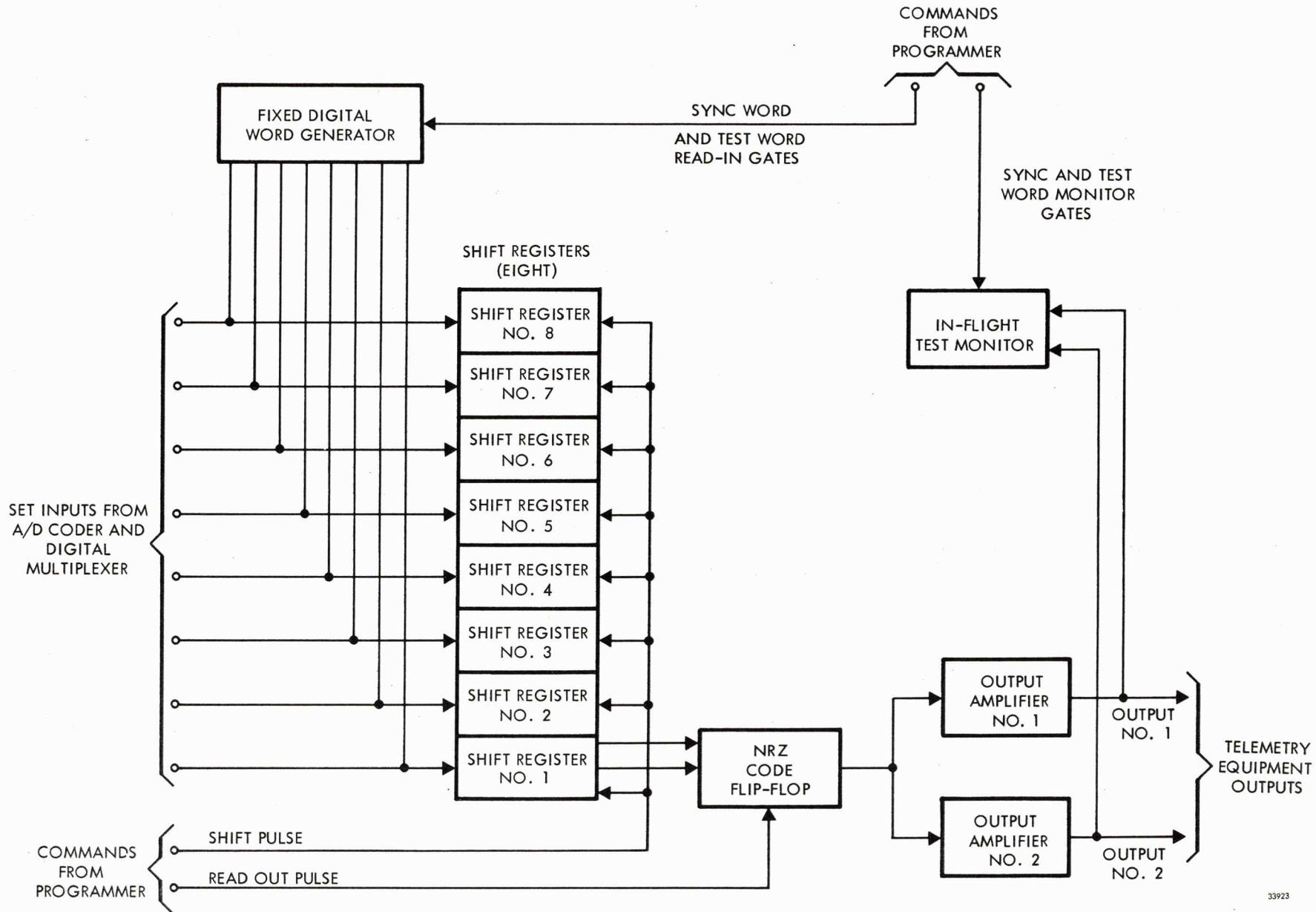


Figure 1.2.1.4-2 Digital Multiplexer Block Diagram



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Figure 1.2.1.5-1 Output Register Block Diagram

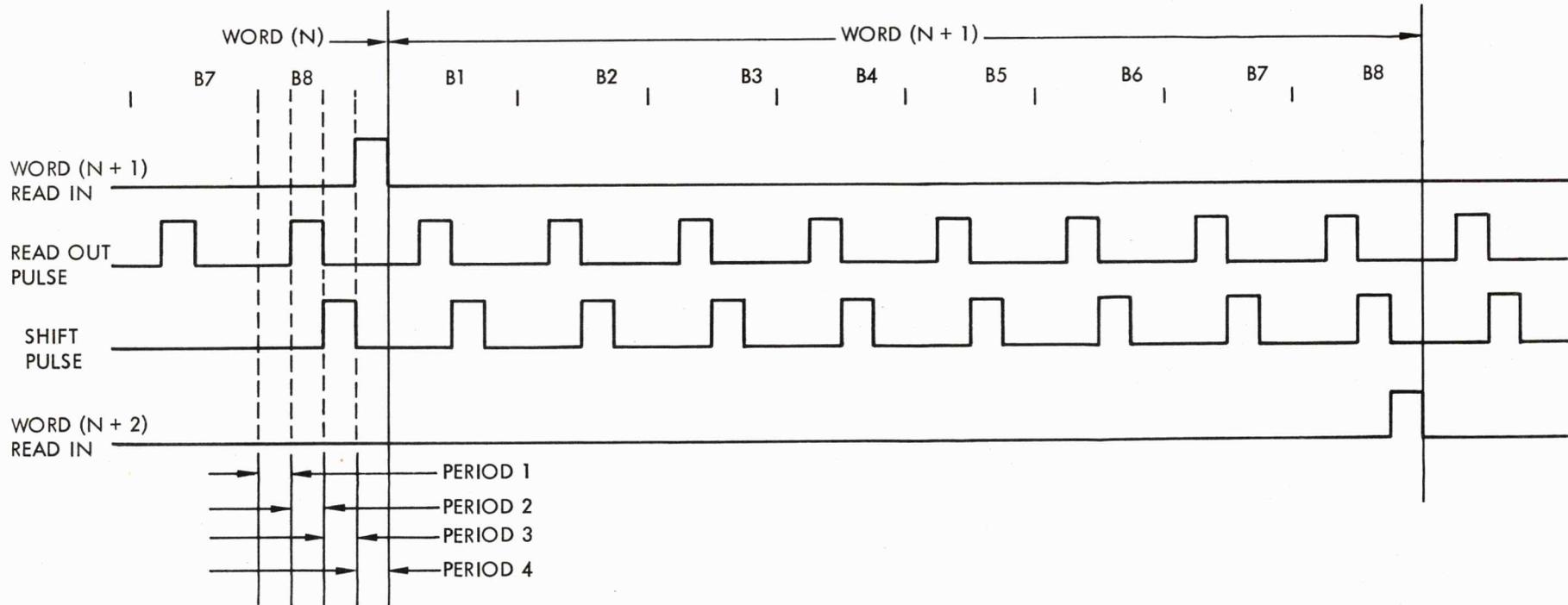


Figure 1.2.1.5-2 Output Register Timing

A critical circuit for the purpose of this discussion is defined as a circuit which will cause the loss of five or more channels.

The block diagram of how the over-all calibration and self-checking system is shown in Figure 1.2.2.1. The block diagram shown is the functional block for simplification because the complete block diagram would have to show each critical circuit in the entire telemetry equipment, since each critical circuit has its self-checking circuit included in the module with it.

The critical circuits shown in Figure 1.2.2.1 each have a self-checking circuit. If only one critical circuit is in a module its output goes directly to the in-flight maintenance monitor connector and to the SEP combining logic. When one or more independent critical circuits appear in the same module, the indications are combined by the module combining logic to provide only one indicating wire per module. The individual indications from each module are combined in the SEP combining logic to furnish one indicating signal per SEP to the IFTS. The individual module indicating wires could also be supplied to the IFTS if desired.

1.2.2.2 Test Theory

The actual test circuits will be designed specifically for each critical circuit to best meet the spacecraft requirements. Design effort and circuit standardization become important only after all other requirements are satisfied.

In general all of the tests divide into three different types. These are:

- Calibration Test
- Signal Flow Test
- Continuity Test

1.2.2.2.1 Calibration Test

Calibration tests are used to check analog circuits such as the individual analog gates (in some cases), the low-level amplifier, and the analog-to-digital converter. The amplifier and coder are checked at two points, near zero and near full-scale, to determine the calibration of two important characteristics, "offset" and "gain". The analog gates need only be checked for "offset" because any variation in gate impedance or balance will effect both "offset" and "gain".

The block diagram in Figure 1.2.2.2.1 shows the scheme involved in making the calibration tests. The input to the circuit is a highly stable, constant voltage standard. This standard is similar to those used in Radiation satelliteborne telemetry equipment. The accuracy of the standard will be as high as practical so it contributes as little as possible to the total error output of the circuit. The standard voltage, circuit under test, and the monitor will be electrically isolated. The output of the circuit will be transferred to digital information (if it is analog) and compared to a fixed digital standard, which is the input analog voltage times the transfer function of the circuit. The circuitry will be able to measure the calibration accuracy to the design limit of the circuit, plus the accuracy of the input standard and the analog-to-digital converter. The Digital Standard will be accurate, since it is hard wired into the monitor. The circuit under test is used to compare two standards, analog and digital. If any of the three should fail an error would be indicated. In order for two failures to occur and compensate for one another it would require that the failures be algebraically opposite and still within the accuracy required.

This scheme inherently includes a feature whereby the accuracy error limits can be easily changed in binary powers of the incremental voltage. Also, this design facilitates the addition of an error counting circuit which could be used to allow a certain number of errors per unit of time before a failure indication is given. The errors per unit time feature would prevent unforeseen non-recurring induced errors from indicating a failure in the system when there is none. The extent of the application of these available variations in failure mode criteria will be based upon CRC's requirements.

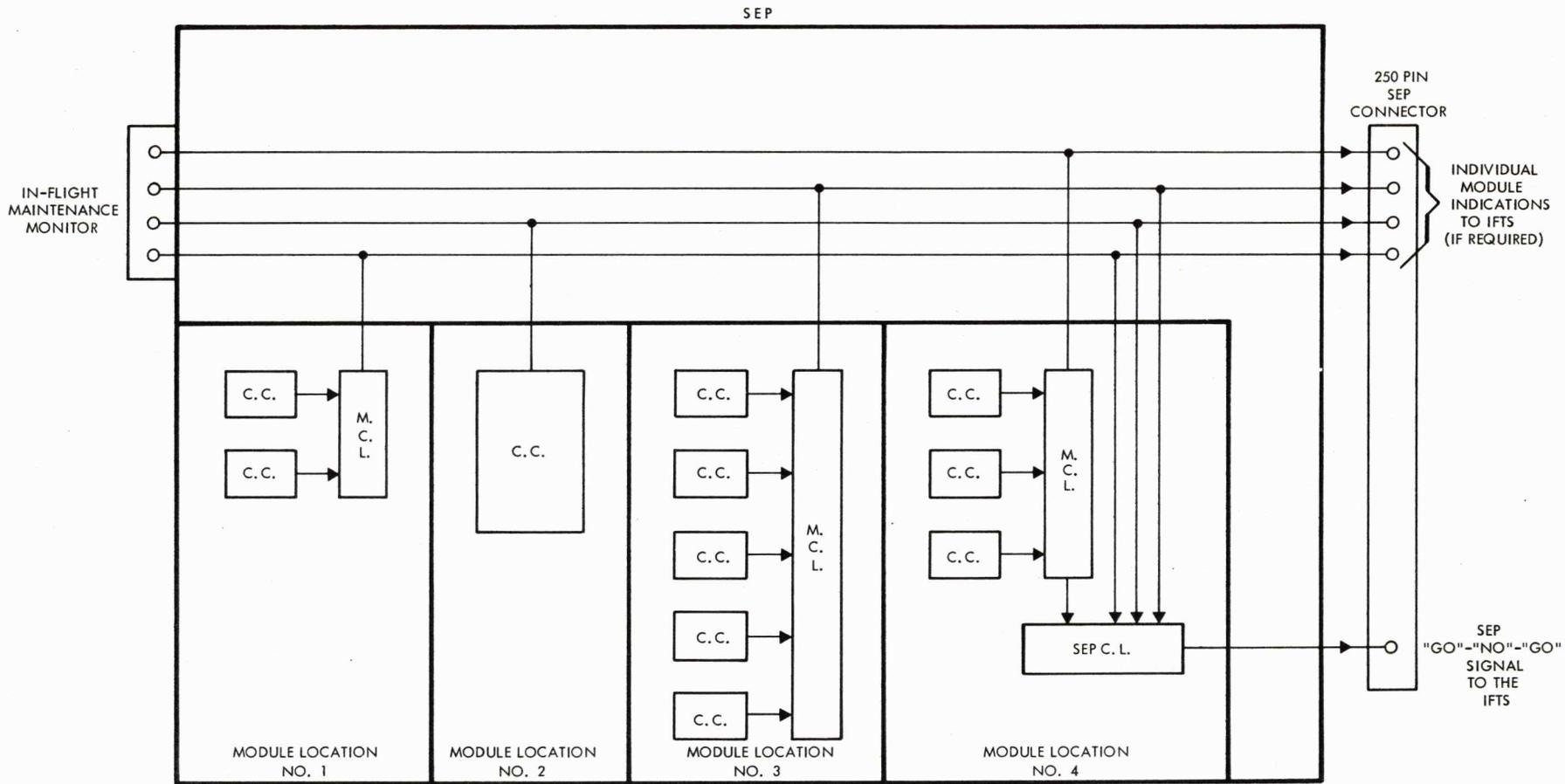
1.2.2.2.2 Signal Flow Test

The signal flow test is a simple Go No-Go test to determine that the input signal causes an output signal to be generated and that no output signal is generated without the presence of an input signal. The signal flow test can be used to test the power switches, drivers, inverters, flip-flops, counters, diode matrices and other circuits.

This test is automatically and continuously performed on the circuit during operation. It also serves to insure that the circuit is not working when it has not been commanded to work. Figure 1.1.3.5.2 is a block diagram which shows the interconnection between the circuit being tested and the signal flow test circuits.

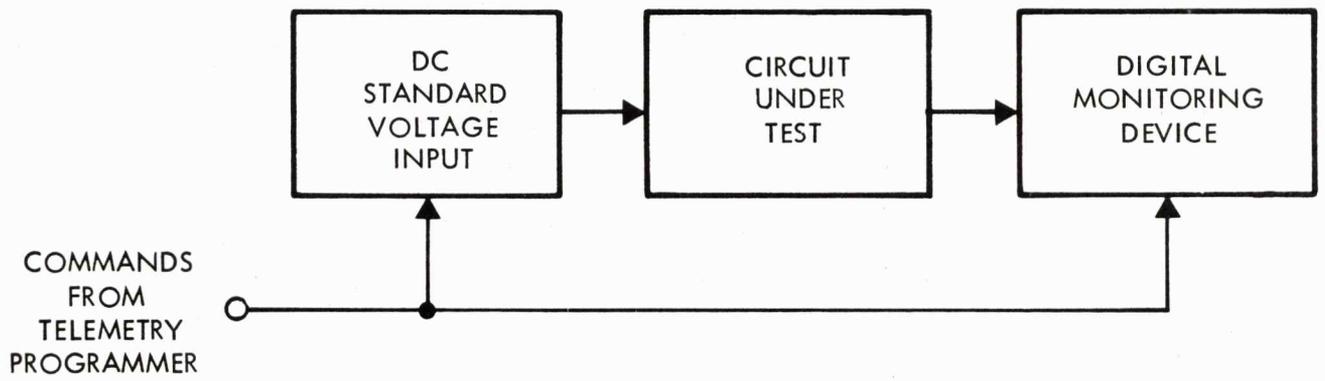
1.2.2.2.3 Continuity Test

The continuity test is made to determine if the signal or power path is complete. This test will be used on the core matrix modules to detect an open row or column circuit through the transformers. Shorted core windings are not considered because only one channel would be lost on the modules checked thusly. The power supply will be monitored with similar circuitry to detect correct voltages and proper operation.



ABBREVIATIONS:
 C.C. = CRITICAL CIRCUIT
 M.C.L. = MODULE COMBINING LOGIC
 SEP C.L. = SEP COMBINING LOGIC

Figure 1.2.2.1 Calibration Self-Checking System



33947

Figure 1.2.2.2.1 Calibration Tests of Analog Circuitry

1.2.2.2.3 Other Tests

The foregoing tests and combinations of the three are envisioned to handle all of the necessary in-flight testing of critical circuits. Other types of tests may be used if they are proven superior for the required application.

1.2.2.3 Combining Logic

The combining logic will consist primarily of simple diode resistor type OR circuitry with a flip-flop included to add the dc level output feature when the output is not ordinarily a dc level.

Combining logic can be used in modules containing more than one critical circuit to combine the signals and furnish one Go No-Go signal from each module. The signals from all of the modules in an SEP will also be combined to give one Go No-Go indication to the IFTS from each SEP.

1.3 STATE-OF-THE-ART

The proposed PCM telemetry equipment for Project Apollo has been formulated from combinations of proven missile and spacecraft hardware with only minor variations. These designs are derived directly from hardware developed and proven reliable on Minuteman, Titan I, Titan II, Telstar, OAO and Nimbus. Emphasis throughout the design of the proposed equipment has been heavily placed upon the use of proven, reliable, circuitry. Since the proposed combinations of these equipments wholly meet the requirements of the Apollo PCM telemetry equipment, the application of untried and unproven approaches has been excluded in the interest of reliability commensurate with the shortest possible delivery time.

Experience has taught Radiation Incorporated that unproven designs, short delivery requirements and reliability are completely incompatible.

1.4 DESIGN TRADE-OFFS

During the preparation of this proposal Radiation Incorporated Engineers have given careful thought to the trade-offs in the design of the telemetry equipment in terms of Reliability, Weight, Size, Power, Accuracy, Flexibility, Maintainability, Producibility, Delivery Time, and Cost. In no case has Reliability been compromised in favor of any parameter . . . , although redundant circuitry similar to that in Radiation's design for the OAO satelliteborne PCM telemetry equipment was carefully considered. Had the In-Flight Maintenance concept not been a requirement, redundant circuits would have been necessary. But in the presence of this human ability to make repairs while in flight, the redundant circuits afford no significant improvement in reliability and considerably increase the size, weight and power required by the equipment.

1.4.1 Elimination of Module Connectors

Only one trade-off has been considered as a worthwhile alternate -- this is in the area of packaging. As shown in Paragraph 1.4.2, in the trade-off of reliability versus weight, the connectors are the limiting factor of reliability. A significant improvement in reliability, size and weight is offered by the alternate described in Appendix G which describes the trade-off advantages of a significant number of connectors. Unfortunately, this alternate approach violates the specification requirements regarding the number of pins per SEP. Radiation realizes that this approach may be incompatible with the spacecraft requirements. In any event, any spare pins on SEP and module connectors will be used to duplicate the most important functions and add some connector redundancy to increase the reliability.

1.4.2 Reliability Versus Weight Study

1.4.2.1 General

A study was made considering trade-offs between reliability and weight. The results are graphically presented in Figure 1.4.2-1. It should be pointed out that this is a discrete point relationship because of the use of spares to achieve the high reliability required, i.e., fractional spares have no meaning. However, the plot is shown as a continuous function to facilitate the presentation of the relative reliability versus weight trade-offs possible.

Studies were also made of alternative system packaging configurations before settling on the approach presented here in the proposal. An approach considering the use of six SEP's with internal hard wiring, and one replaceable (spare) SEP for each of these was evaluated. The total weight of this configuration was approximately the same as the system described in the proposal, but the reliability was considerably lower (though still meeting the specified 0.997 probability of success).

Another approach investigated was the use of two double SEP's (again with hard wiring) to contain the complete telemetry sub-system. This approach required the use of three spares (two for the more complex SEP and one for the other). Again,

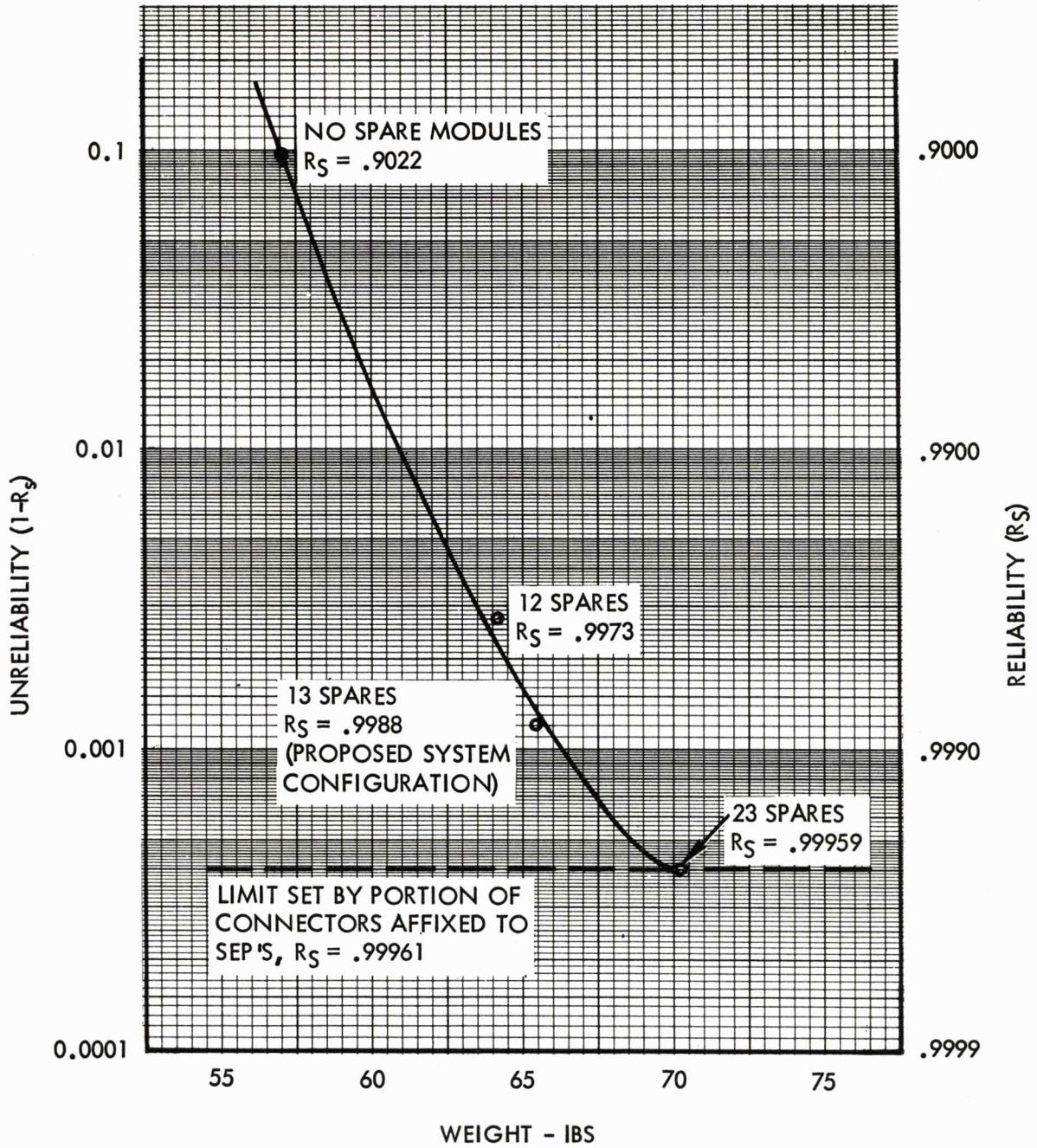


Figure 1.4.2.1 Reliability vs Weight

the total weight was approximately the same and the reliability within specification limits, but still lower than for the proposal approach. This was because duplication of programmer functions was necessary in order to stay within the connector limitations. Another approach that avoided this problem was taking exception to these connector limitations is discussed in Appendix G.

1.4.2.2 Graphical Presentation

Further trade-offs have been considered within the proposed sub-system packaging approach, and several significant points were chosen for graphical presentation.

A straight forward system with no spares was evaluated. Next, enough spares were added to bring the reliability up to the value specified for the telemetry sub-system.

The optimum configuration was then evaluated, where one spare was provided for each different type of module. This resulted in a probability of success for 340 hours of 0.9988, with an attendant weight of 65.4 pounds.

The last configuration evaluated considered the use of double spares for the least reliable modules, resulting in a probability of success of 0.99959. Further improvements in the telemetry sub-system reliability are limited to an upper value of 0.99961 which is the reliability of the connectors affixed to the SEP's. That portion of the module connector which is replaceable with the module is considered as such. However, the other portion which is part of the SEP hardware is not repairable in-flight and must be considered accordingly.

1.5 Component Count

The following table lists the component count for the Apollo PCM Telemetry Equipment.

PROJECT APOLLO

Unit Description Telemetry (PCM-System)

Module Description _____

Module Size (See Memorandum) _____

Part Description	Number of Parts Used	
	C & M	Tele & P/S
Transistors	- Germanium	
	- Silicon	101 2430
Diodes, Silicon	- Power	30
	- Signal	358 5568
	- Zener	20
Tubes	- Power	
	- Special (magnatron, amplifron)	
Resistors	- Composition, fixed	679 2101
	- Composition, variable	
	- Film, fixed	21
	- Wirewound, fixed	32
	- Wirewound, variable	
Capacitors	- Ceramic, fixed	536 276
	- Ceramic, Variable	
	- Mica, fixed	
	- Mica, variable	
	- Tantalum Electrolytic, fixed	14
	- Paper, fixed	
Chokes/Coils	- RF	2
	- Power	2
	- Variable	
Connectors	-	74
Crystals	-	1
Filters	- Crystal	
	- Mechanical	4
Meters	-	1
Relays	- Coax	
	- Open	
	- Sealed	
Socket	- Tube	
	- Relay	
	- Crystal	
	- Transistor	
Switches	- Toggle	
	- Wafer	
Transformer	- RF	
	- IF/Audio	
	- Power	3
	- Saturated Core Transformer	425

2.0 SPECIFICATION COMPLIANCE

The equipment proposed in the body of this proposal fully complies with the requirements of AR131-3 and the referenced documents. This is made possible by Radiation Incorporated's experience in the design, development, and production of similar equipment.

Only one area requires possible clarification: Paragraph 3.4.3.6 of AR131-3 states that synchronization should be ensured in 0.1 second under normal conditions. It is assumed that "normal conditions" include the normal bit rate of 64 kc. Since three frames are required to attain synchronization at the minimum data rate, three seconds would be required to attain the required confidence level that synchronization had been achieved.

3.0 DESIGN CRITERIA COMPLIANCE

Radiation Incorporated proposes to meet the intent of all requirements of AR104-3. The following paragraphs are added to clarify these requirements.

3.1 Environmental Test

Radiation will subject the telemetry equipment to the environmental qualification and acceptance tests in essential conformity with Collins Radio Specification AR104-3. A qualification test procedure will be submitted to Collins 30 days prior to the scheduled commencement of tests. It is assumed that Collins will approve this procedure within 21 days after submission. The final qualification test report will be submitted within 45 days after completion of the tests.

The following modifications to the Collins specification AR104-3 are proposed:

<u>Paragraph</u>	<u>Modification</u>
3.2.2.1	Add "Vibration system equalization shall be within ± 3 db."
3.2.2.7	Radiation will comply with the Cobalt-60 radiation test which is to be established later, subject to the availability of a suitable test facility. Since the test is not now defined, no prices are included for the radiation test. Prices will be negotiated when the test is defined.
3.2.2.8	Radiation proposes to insure that fungus growth cannot be supported by certification of component parts and materials rather than by test.
3.2.2.9	Radiation proposes to subject the telemetry equipment to an accelerated ozone test of one part per million for 10 days. This test will insure meeting the requirements of Paragraph 3.2.2.9.

It has been assumed that

- (a) System operation on a cold plate is required only in the test of Paragraph 3.2.2.4;
- (b) Collins' Test Report Format is not significantly different from Radiation's format or MIL-T-9107;
- (c) Radiation must fabricate a cold plate heat exchanger for the test of Paragraph 3.2.2.4 and Radiation will not supply a heat exchanger to Collins.

3.2 Interference Control

Generated interference levels resulting from the 512 kc clock signals, various bit rates, and digital waveforms within the system will exceed the limits imposed by Document AR104-3. The system package and interconnecting cable shields will constitute an effective system interference shield. Application of the shielding and grounding concepts delineated in the specification have been proven successful with similar systems in achieving lowest practical interference and susceptibility levels consistent with minimum weight design. Specific interference control philosophy is detailed in Appendix F.

3.3 Reliability Program Plan

3.3.1 Introduction

To assure that the reliability goals of the Apollo spacecraft telemetry system are met Radiation Incorporated will conduct a time-phased reliability program based on the requirements of MIL-R-27542 (Amend. 1), and specific contractual requirements. This program will emphasize frequent monitoring of reliability levels and the rapid feedback of information to design and fabrication groups.

Responsibility for implementing and maintaining this program will be placed with the Reliability Section. A Reliability representative will be assigned to work on the program management team to coordinate with the various Task groups at a sufficiently high level of management to assure that reliability aspects receive timely consideration and that contractual reliability requirements are met.

3.3.2 Time-Phased Reliability Program

The reliability program for the proposed equipment will consist of four phases as follows:

- Design Requirements Study
- Engineering Models, Manufacturing and Testing Phase
- Detailed Design Phase
- Prototype Models, Manufacturing and Testing Phase

The task assignments will span one or more phases of the program as depicted in Figure 3.3.2-1. The time phasing will provide the prime contractor with frequent reports and checkpoints for monitoring the reliability efforts and the over-all status of the design. The specific tasks to be accomplished during each of the phases are as follows:

Phase I - Design Requirements Study

A. Reliability Program Plan - A detailed reliability program plan will be prepared early in the program describing the efforts required in the various reporting areas. This plan will provide adequate control of all key operations during the design, development, manufacturing, and testing stages. It will be an amplification and expansion of the proposal program plan and will provide the detail necessary to implement and control the necessary efforts in support areas. The plan will be submitted to the customer within 30 days of contract award and thereafter will be considered as directive in nature upon all organizations involved in the reliability program.

B. Specific and General Derating Philosophy - The general derating philosophies laid down in AR 104-3 Para. 3.3.3 will be followed in the design of the equipment. In addition to these a specific derating philosophy will be developed expressing the additional derating requirements necessary to assure that the highest inherent mean-time-to-failure possible will be achieved consistent with the limitations imposed by other design considerations such as size, shape, weight, power consumption, etc.

C. Reliability Requirements and Formulation Study - During the reliability requirement and formulation studies, reliability engineers will work with design engineers as an integrated team to develop the optimum design concept. Configuration analysis studies will be made considering trade-offs among such factors as performance, reliability, power consumption, weight and size.

Redundancy techniques on a part, block and system level as well as multimode analysis will be used as necessary for achieving the required reliability and operating life. Consideration will also be given to the use of design techniques which allow malfunctions to occur with only minor degradations in over-all system performance.

Radiation Incorporated has available a computer program for its IBM 1620 computer that makes possible very rapid evaluation of alternative system configurations. It is expected that this program or its equivalent will be used during this phase of system design. (See Appendix E-2 "Reliability Analysis and Prediction through Application of Digital Computer")

D. Preliminary Reliability Analysis and Prediction - The optimum design concept will be converted into a reliability mathematical model. The reliability requirement will be sub-divided to system blocks and finally allocated to component parts. Progressive reliability goals will be established for each major phase of the program.

The preliminary estimate will be based on a parts count technique using the number of parts in each functional group, the average thermal and electrical stress levels seen by these parts, the other environmental stresses anticipated, and the typical failure rates for each part type.

The reliability assessments will cover the prelaunch, launch, flight and re-entry periods.

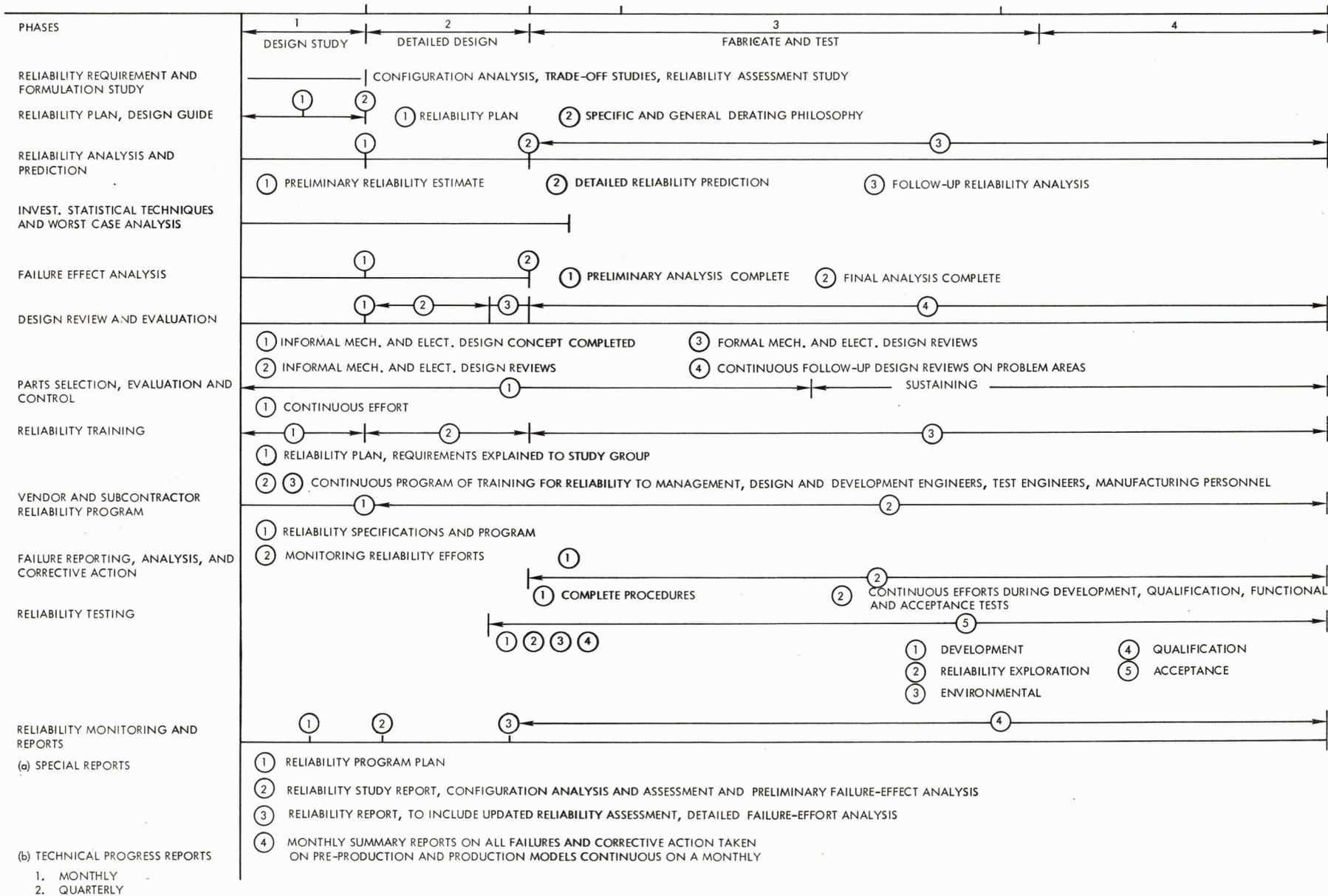


Figure 3.3.2-1 Time Phases Reliability Program

A mathematical model will be prepared using probability theory techniques which consider the success and/or failure frequency distributions of the various system blocks in the particular time domains involved for each successful mode of operation.

It is expected that the computer program mentioned above could also be used during this phase to perform the actual calculations involved.

Failure rate data will be obtained from various sources including Boeing Document D-590, Section 500, "Highly Reliable Parts"; RCA Technical Report TR-59-416-1, Revision Volume 14, "Reliability Stress Analysis for Electronic Equipment;" Radiation in-plant and field data; and manufacturer's data.

E. Failure Mode Analysis - A reliability block diagram will be prepared from the functional system schematic indicating the functional arrangements of the "black boxes" and the design output requirements. A preliminary failure mode analysis will be performed on the higher levels of the assembly for the purpose of studying the following:

- Possible failures and failure modes.
- The compensating provisions inherent in the design or possible alternate operating modes.
- The result of each failure mode on system performance.
- The probability of a particular failure occurring.

Failures will be classified into categories according to their effect on over-all system performance. The failure mode analysis will provide information on specific areas where re-design would improve reliability or reduce the consequences of a given failure.

F. Statistical Design Studies - Radiation will perform statistical design studies to evaluate the adequacy of the design of the Apollo telemetry equipment. A MANDEX Worst-Case tolerance analysis is proposed.

Starting during the design requirements study phase of the program both reliability and computer programming personnel will be made available to assist engineers in setting up the analysis on their circuits. It is expected that time will have to be leased on an IBM 7090 computer for the actual analysis; however, there are two such machines available in the immediate area.

This analysis is expected to continue through the detailed design phase or until all circuits of interest have been evaluated.

In this type of study the transfer function (output as a function of input) is derived for each circuit. This function is expanded into a Taylor series and the partial derivative of each output parameter with respect to each input parameter taken. Using the resulting equation the effect on output of changing an input can be examined and the critical values of inputs learned.

In addition to the MANDEX analysis proposed above, it is further proposed to conduct a statistical analysis of the effects of component aging on circuit performance. Methods to be investigated include the Parameter Variation, VINIL and Monte Carlo techniques. Pricing of implementing any additional methods is contingent on the performance of the MANDEX study and on being able to obtain computer programs for the IBM 7090 from North American Aviation.

G. Parts Selection, Evaluation and Control - A parts selection, evaluation, and control plan will be prepared. The purpose of this document will be to present a plan that will ensure that design engineers specify and use only parts which perform reliably as demonstrated by previous history from other aerospace programs.

Radiation expects to utilize parts already proven on the Minuteman program to maximum extent possible. Where there are not Minuteman parts available, parts that have proved their adequacy on programs such as the Titan, Nimbus and Telstar PCM's as well as parts from other missile programs will be recommended.

Evaluation of parts will include, but not be limited to the following:

- Investigation of the justification for and the application of each part.
- Preparing specifications for the procurement and control of parts.
- Providing evidence that the part can meet or exceed the performance and reliability requirements of the specification. (IDEP Data, etc.)
- Determining the degradation parameters as a function of time so that adequate safety factors can be designed into circuits to allow for parameter shifts.
- Establishing the necessary restrictions on acceptable range of values and the applications.
- Determining the component cycling, aging and derating factors necessary to provide increased reliability.

Parts which must be used in specific applications and which have not been qualified on the Minuteman program will be submitted to Collins for testing and approval. Reliability Engineers working with personnel from the Engineering Standards and Components group will prepare submissions with proper supporting evidence and forward them to Collins.

Product Assurance will subject all incoming parts to a thorough receiving inspection and will maintain records on quality levels achieved and individual vendor quality histories.

H. Design Review and Evaluation - A design review program will be established on the Apollo telemetry equipment similar to that used on other major projects. The program will involve planned and continuous monitoring of the design concepts and efforts to assure a final design that will meet the performance and reliability specifications. Intra and inter-departmental efforts will be combined for analysis of the design, thus providing a well integrated and coordinated final design. Design review activity will span the following program phases:

- Conceptual Design Phase
- Detailed Design Phase
- Production and Testing of Engineering Models
- Production and Testing of Prototype Models.

Informal mechanical and electrical design reviews will be held between cognizant design and reliability engineers on a continual basis. Formal design review meetings will take place throughout the conceptual and detailed design phases. These will involve design, support, and reliability engineers as well as Product Assurance and Manufacturing personnel. These reviews will be held by project management.

I. Reliability Training - A reliability training program will be established for all assigned personnel; both engineering and manufacturing. The training program in the engineering areas will principally consist of explaining the reliability plan and requirements to the various personnel and then keeping them aware of these requirements by presentations at design reviews, memos, etc.

The cognizant section heads in the engineering groups are charged with the responsibility to assure that the skills and knowledge of their personnel keeps pace with the advancing technology.

In the Manufacturing Division the training of the production and testing personnel will be accomplished through a continuous formal training effort. Instruction will be given in the fabrication techniques necessary to assure the reliability of the equipment produced. In addition lectures and poster campaigns will emphasize the over-all importance of reliability in a system such as the Apollo PCM.

Product Assurance personnel will contribute to the training effort by continuously criticizing the workmanship and techniques used by Manufacturing personnel.

J. Vendor and Subcontractor Reliability - The reliability efforts of vendors and subcontractors will be controlled through the following activities:

- Writing specifications for parts and equipment which contain definite reliability requirements as well as positive control of those production characteristics which are known to influence the reliability.
- Imposing reliability system requirements on vendors to assure that parts are produced by a manufacturing system capable of producing consistently reliable parts.
- Requiring vendors to submit objective evidence of attaining reliability goals for their components.
- Subjecting parts to tests after receipt to verify that reliability requirements have been met.
- Maintaining liaison with vendor personnel to become aware of the problems associated with their particular product.

K. Reliability Program Review - During this phase a plan for a periodic reliability program review will be developed and included in the formal reliability program plan. The reliability program will be reviewed against predicted growth curves; and weak points in the system will be reviewed and eliminated.

L. Reliability Reports - In order to keep the customer abreast of the progress of the reliability program specific information feedbacks are planned. These will take the form of special and monthly reports. The reports to be submitted during this phase are:

1. Special Reliability Reports

These reports will present the results of studies conducted and predictions made during Phase I as follows:

- a. Reliability Program Plan
- b. Specific Derating Philosophies
- c. Preliminary Analysis and Prediction
- d. Failure Mode Analysis - Block Level
- e. Parts Selection Evaluation and Control Plan
- f. Reliability Program Review Plan

2. Statistical Design Investigation Report describing in detail the statistical design methods investigated and recommended.

3. Monthly and Quarterly Progress Reports

A special section of the monthly and quarterly technical progress report will be devoted to the reliability program efforts.

4. Quarterly Reliability Status Report

Phase II - Detailed Design

A. Detailed Reliability Analysis and Prediction - All circuits will be evaluated to determine that proper derating factors have been applied in accordance with the derating philosophies in AR 104-3 and those developed during Phase I of the Radiation reliability program. Data from thermal mockup studies will provide accurate information on temperature stresses and hot spots. A prediction of the mean-time-to-failure and probability of survival without exhausting stocks of spares will be completed and reported. The prediction will be based on electrical, thermal and environmental stresses utilizing typical failure rates from the Minuteman program and from other appropriate sources such as RCA TR-59-41601, Reliability Stress Analysis for Electronic Equipment, Radiation Incorporated and vendor data.

The 1620 computer will be used for this prediction and all subsequent predictions on system design changes as cost factors dictate.

B. Failure Mode Analysis, Detailed - The failure mode analysis will become more detailed as the design progresses toward the hardware stage. The analysis will be taken to the circuit level. The results of the analysis will be prepared so that it may be used as a basic trouble-shooting guide useful in the design of test and checkout equipment.

C. Statistical Design Studies - The MANDEX and other statistical analyses begun during the design requirements study phase will be continued during this phase until all circuits of interest have been analyzed. It is expected that most of the actual computer analysis will be completed during this phase.

D. Parts Selection Evaluation and Control - During this phase the parts control program planned during Phase I will be implemented. It is expected that design engineering groups will request approval for all non-Minuteman parts through the channels established by the Reliability Section. Suitable mechanisms will be established to assure that all parts used will receive such approval.

The Reliability Section will maintain logs giving the status of all non-standard parts approvals requested.

E. Design Review and Evaluation - Informal mechanical and electrical design reviews will continue between the cognizant design and reliability engineers. As the design approaches finalization, formal (critical) mechanical and electrical design reviews will be scheduled with design specialists who are not part of the participating design effort attending. Any problem areas revealed in the design reviews will be resolved prior to finalizing the design. The program manager will take the action necessary to resolve the problem areas by:

- Making written assignments on all open items established by the design review to the respective individuals or organizations, stating responsibility for taking appropriate action.
- Assigning to individuals or organizations the specific recommendations or technical solutions made by the design review committee for improving design adequacy, or improving the designated degradation factors of procurement, producibility and usage.
- In the case of marginal design parameters, potential problem areas, questionable test data, etc. arrange for additional design analysis or testing effort to eliminate these conditions or to prove that the design is completely adequate.
- Delegate the reliability engineer the responsibility to monitor the status and effectiveness of corrective action being taken by the designated persons or organizations.

Figure 3.2.2-2 illustrates the Reliability design Approval Data Flow implemented at Radiation Incorporated.

F. Reliability Training - The training program for engineering personnel discussed under Phase I will continue. Implementation of a training program for fabrication employees will begin and the first training sessions specifically applicable to the Apollo program will be held.

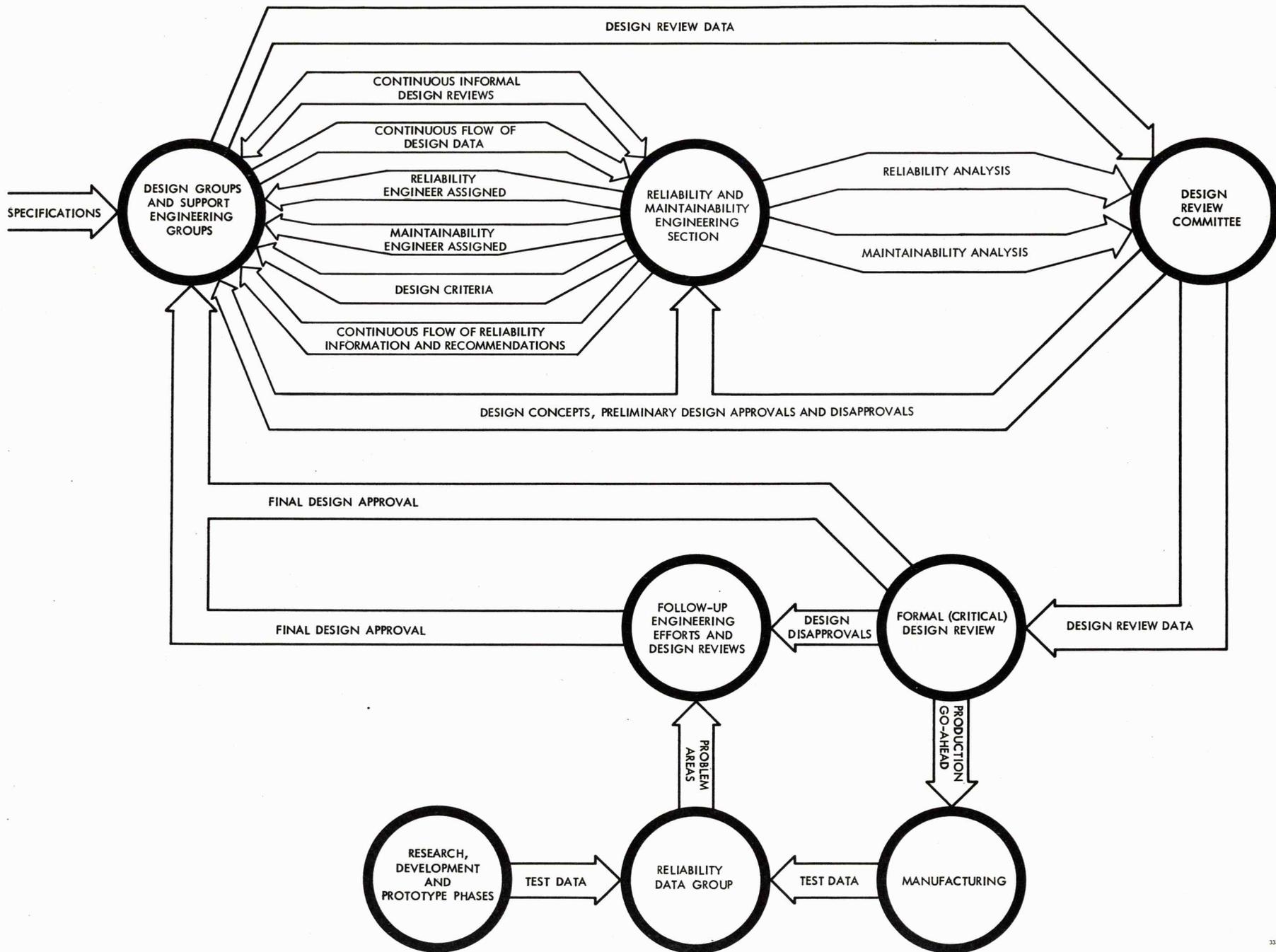


Figure 3.3.2-2 Reliability Data Flow

G. Vendor and Subcontractor Reliability - The efforts outlined under Phase I will continue; however, the activity in this area will be increased as the procurement for the program begins.

H. Failure Reporting, Analysis and Corrective Action - A failure reporting, analysis and corrective action system will be implemented during this phase. The basic policies and procedures for the functioning of this system will be described in the program plan. Specific procedures will be implemented to assure that all failures of parts or equipment on the program are reported to the reliability section. Each failure will be analyzed to determine the cause and classified accordingly. Wherever corrective action is required to remove the cause for or prevent the recurrence of a failure, written requests for corrective action will be forwarded by the Reliability Section to the cognizant group, and followed up to assure that appropriate action is taken.

Failure recurrence control will be obtained by checking each failure report for previous occurrences. Where failure occur repetitively additional study will be made and additional corrective action requested.

Figure 3.3.2-3 depicts the reliability information flow.

The Reliability Section will originate a failure analysis report on each failure describing in detail the events surrounding it and the exact nature of the failure. Photographs will be used wherever possible to clarify the failure analysis report. These reports will be disseminated to the various interested organizations within Radiation.

The Reliability Section has facilities (See Table 3.3.2-4) for the disassembly and study of failed components to determine or verify the cause of failure. To support these facilities there are personnel trained in various fields of engineering and science available to serve as consultants in the failure analyses.

Suitable forms will be designed to permit effective and efficient reporting of each failure. These forms will meet the requirements of MIL-R-27542 except where needless duplication of records would result.

Failure reports will be filed in a manner so that access may be readily obtained to any particular report and so that monthly and quarterly failure experience histories may be obtained. After the program moves into the manufacturing stages the volume of data collection will make it necessary to store data on punched cards. This technique is presently used on other major programs and can be readily adapted to the Apollo program.

Failure Data will be forward to CRC five (5) days after occurrence. Failure analysis reports will be forwarded to CRC fifteen (15) days after failure and recaps of monthly failure history will be submitted as a part of the monthly and quarterly technical reports.

I. Reliability Program Review - Reliability Program reviews will take place during this phase as scheduled in the Reliability Program Plan.

J. Reliability Testing - The Reliability Section will follow the progress of the Apollo equipment through the various stages of reliability and qualification testing. All failures of the equipment occurring during reliability exploration, qualification, environmental, system integration and other testing at Radiation Incorporated will be reported through the failure reporting system. Exhaustive failure analyses will be conducted to determine the cause of each failure and action will be taken wherever indicated to prevent recurrence. Similar data will be forwarded to the Reliability Section by personnel accompanying the equipment to Collins for final testing. In addition operating time records will be maintained on all items of equipment. This data will be used by Reliability to confirm that the equipment meets the requirements of the contract.

K. Reliability Reports -

1. Statistical Study Reports
2. Monthly and Quarterly Technical Reports
3. Failure Data and Analysis
4. Quarterly Reliability Status

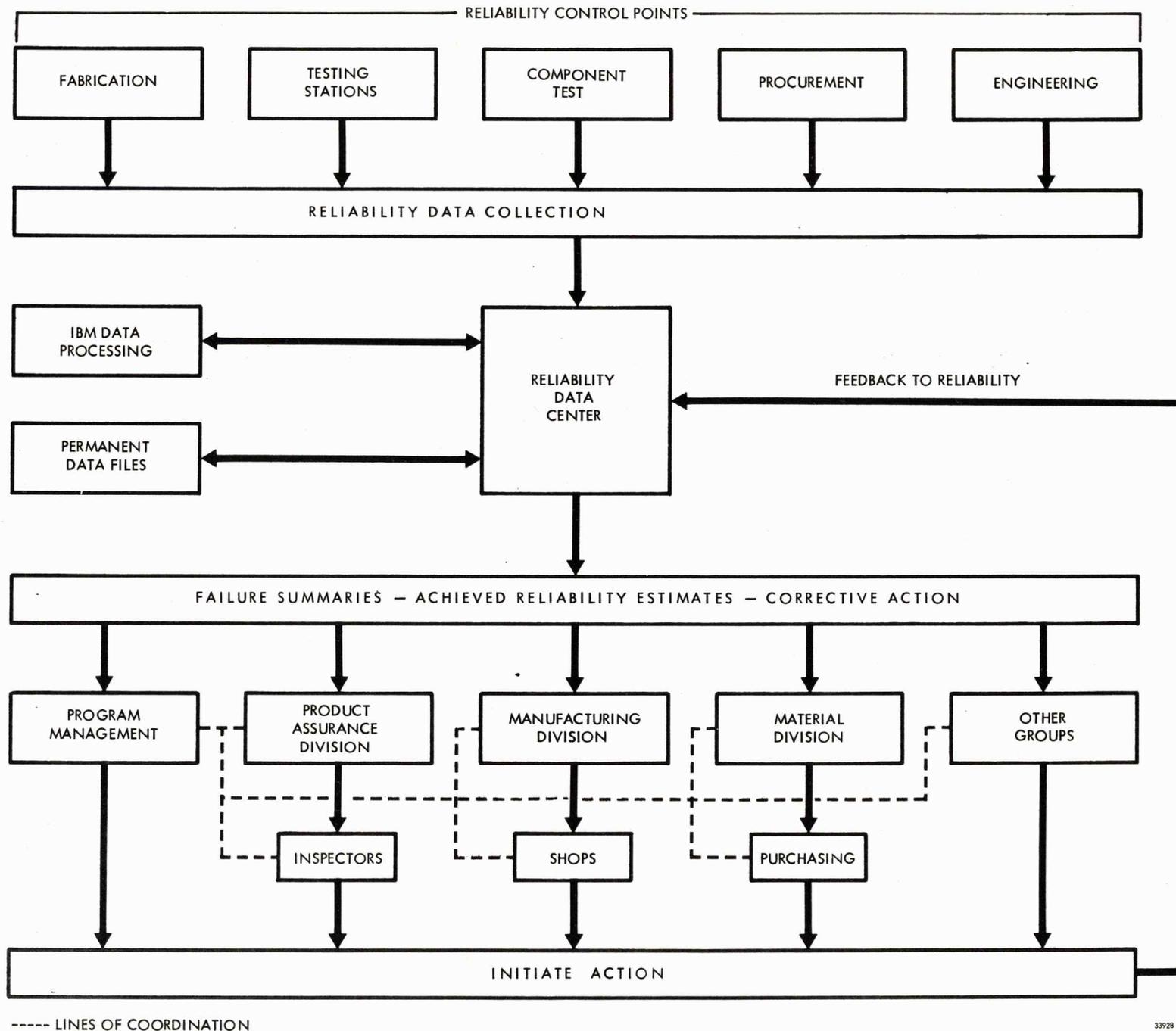


Figure 3.3.2-3 Reliability Channels of Communication

TABLE 3.3.2-4
FAILURE ANALYSIS FACILITIES

Reliability - Data Group - J. F. House

- Complete range of electronics test and measuring equipment.
- AO Spencer Cycloptic Stereomicroscope
- Hand Tools for disassembly of components

Product Assurance - J. B. Rivera

- 14" Nikon Optical Comparator - 100 x mag.
- Complete range of mechanical measuring equipment accuracy 0 - .001 inch;
1 sec. angular
- Rockwell Hardness Tester
- Dye penetrants
- Magnaflex Magnatest ED-500-Lead composition analyzer
- Tensile Tester - 10,000 pound capacity
- Stereo and metallurgical measuring microscopes
- Dermitron film thickness measuring machine
- Hi-pot Tester

Special Processes Laboratory - N. K. Hopp, Chemist

- Equipment to perform full range of inorganic qualitative and quantitative chemical analysis

Manufacturing Research Laboratory - W. A. Collar

- Metallographic examinations
- Micro-sections and examination
- Strength and deflection measuring equipment

The Standards and Components and Engineering Testing Services at Radiation are able to perform any special information or reliability confirmation tests such as life, electrical, environmental, stress and corrosion resistance tests to confirm failure modes or verify the suitability of component applications. Such tests would also be conducted under the cognizance of a Reliability Engineer.

Standards and Components Laboratory - E. Coates

- Full range of electronic test and measuring equipment for resistance, capacitance, inductance, voltage, current and frequencies.

Environmental Test Group - O. G. Hancock

Shock	- 0 - 120 g's	Humidity	- 20% to 100%
Vibration	- 2 - 3000 cps, 6000 force pounds random, 7500 force pounds sinusoidal	Pressure	- 10 ⁻⁷ to psig.
Temperature	- -73°C to +150°C	Acceleration	- Rotary 0 - 120 g's
		Salt Spray	-

Phases III and IV - Manufacturing and Testing of Engineering and Prototype Models

A. Failure Reporting, Analysis and Corrective Action - The failure reporting system implemented during the previous phase will continue to operate and during this phase will continue to be an important tool in isolating final design, producibility problems and fabrication problems. Reporting to all interested groups will continue as outlined under Phase II.

B. Parts, Material, and Assembly Traceability - A parts, materials and assembly traceability program will be implemented during this phase. The program will be conducted by Product Assurance and Production Control personnel with surveillance by the reliability group. The program will ensure that adequate documentation exists to trace out the assembly and part serial numbers of all components installed in each system. The controlling documents will be the Product Assurance system log books and the Production Control flow sheets.

C. Design Review and Evaluation - Follow-up design reviews will be held on problem areas revealed in the formal design reviews and on problems revealed in the testing program. To provide corrective action on problems subsequent to final design approval, the reliability data group will be charged with the responsibility to take the necessary corrective actions.

D. Training - Training efforts will continue during this phase with particular emphasis on fabrication personnel.

E. Follow-Up Reliability Analysis Program - Continuous up-grading of the mathematical model, prediction, and measured reliability growth from design changes and data from various testing programs will be undertaken. Reliability characteristics will be evaluated for any design changes or problem areas. A final prediction will be reported at the end of the program.

F. Reliability Program Review - Reliability Program reviews will continue during this phase; however, the frequency of such reviews will decrease during the latter portions of Phase IV.

G. Reliability Testing - The Reliability Section will monitor the results of testing programs on all Apollo equipment through the failure reporting system. All departures from equipment specifications will be reported to Reliability, failure analyses will be conducted and appropriate action to prevent recurrence will be obtained. Follow-up will be made on all failures to assure that corrective actions are adequate.

H. Reliability Reports -

1. Follow-Up Reliability Analysis Report
2. Failure Data and Analysis
3. Monthly and Quarterly Reports
4. Quarterly Reliability Status

3.3.3 Maintainability Program Plan

3.3.3.1 Introduction

Radiation Incorporated has an established maintainability program capable of performing to the requirements of MIL-M-26512, Maintainability Requirements for Weapons, Support, and Command and Control Systems, and Equipment. The aim of this program is to provide the customer with equipment of maximum possible maintainability within the limitations imposed by the contract, design constraints, equipment applications and reliability requirements. The program also aims to provide the customer with predicted and observed values of the mean-time-to-repair (MTTR = average troubleshooting time plus average repair times) and thus enable him to make objective evaluations of system performance.

3.3.3.2 Program Plan

In order that equipment maintainability be optimized against other characteristics and for system requirements of 0.25 hour mean-time-to-repair be met, it is necessary for maintainability to be considered continuously from earliest design concept through physical design and fabrication and testing of equipment. To this end, Radiation will establish an integrated maintainability program on the Apollo spacecraft telemetry. The major phases of the program and the specific tasks to be accomplished during each are presented below:

3.3.3.2.1 Design Concept Phase

During this phase maintainability engineers will work closely with those responsible for basic design concepts to assure that maintainability aspects are given proper attention. Predictions of the MTTR for various system blocks will be made using the RCA-RADC questionnaire prediction technique. These predictions will be used as a basis for evaluating and recommending design changes.

3.3.3.2.2 Physical Design Phase

During this phase the maintainability engineers will continue to work with design engineers to assure that basis maintainability concepts placed in the design are carried out as the design becomes formalized. The evaluation of the effect of design changes on MTTR will be continued. Each equipment block will be independently evaluated for maintainability characteristics using the Maintainability Check list, sample pages attached. The results of these evaluations will be used as a basis for recommendations for design changes to improve maintainability characteristics.

During this phase a maintainability engineer will attend all equipment design reviews to assure that maintainability principles are incorporated in all designs.

3.3.3.2.3 Fabrication and Testing Phase

A data collection system will be established as an integral portion of the Reliability Failure System for the purpose of collecting actual repair and trouble shooting time data. This data will be used to confirm, statistically, the validity of the MTTR's previously collected. The confidence levels associated with the observed MTTR's will be stated.

3.3.3.2.4 Subcontractor Maintainability

Maintainability engineers will assure that all subcontracts issued for procurement of equipment used in the system contain requirements for consideration of maintainability. It is expected that the requirements will be scaled to the relative contribution to over-all maintainability of the procured item. Liaison will be maintained with subcontractor maintainability personnel to monitor the progress of the maintainability program in his plant. Maintainability evaluations and predictions will be obtained as required.

3.3.3.2.5 Information Feedback

In order to keep the customer abreast of the progress of the maintainability program at Radiation, definite information feedbacks are planned as follows:

- Maintainability program plan in accordance with the requirements of MIL-M-26512 including the names and organizational positions of the personnel assigned to the task.
- Prediction of equipment MTTR based on design concepts as outlined in 3.3.2.1.2.1 above.
- Input to monthly technical reports outlining significant actions, problems areas, corrective actions, equipment reviews and changes in the predicted MTTR. It is expected that these reports will be used as the vehicle for updating the MTTR predictions.
- Final report on the maintainability program including the observed MTTR's and their associated confidence levels.
- Special reports on maintainability aspects of the system as requested by the customer or as the need is recognized.
- Listings of maintenance tasks and special tools as required by MIL-M-26512.

3.3.3.3 Performance and Qualifications

Radiation Incorporated has demonstrated a capability to design highly maintainable equipment on several past programs such as the Minuteman and AC Spark Plug/Titan PCM Telemetry Systems. The maintainability of this equipment has been demonstrated in the field in dozens of firings. High levels of maintainability have been achieved in-plant by the close cooperation between design and maintainability personnel and the application of maintainability design principles such as use of plug-in modules and chassis, built-in automatic testers and failure indicators, liberal use of test points, minimization of special tools and widespread use of quick release hardware. Based on past performance Radiation is confident that the contractual figure of .25 hours or better MTTR can be met.

3.3.4 Reliability Organization

Responsibility for defining, implementing, and monitoring the reliability and maintainability programs is assigned to the Reliability Engineering Section. This section functions under Engineering reporting administratively to the Data Systems Division Director. It provides reliability and maintainability engineering services to the Programs and Projects at Radiation - Melbourne. The section assigns reliability engineers to work directly with the various design groups during the design, development, pre-production and qualification test, production and testing phases.

A reliability coordinator will be assigned to the Program Management team to program and control the reliability and maintainability functions with Engineering Design, Product Assurance, Engineering Components and Standards, Manufacturing Procurement, Environmental Test and other departments concerned with the programs. This coordination provides for the implementation and dissemination of these programs within the departments.

The Reliability Section is divided into system reliability design, data collection and maintainability groups. The system reliability group assignments include mathematical model analysis, reliability study requirements and continuous critique of the electrical and mechanical designs. The reliability data group provides a history of component parts, non-standard part approval and evaluation, failure analysis and reporting, corrective action requirements and statistical services. The maintainability group provides maintainability predictions, design guides, design consultation, tooling and spares recommendations and data collection.

Reliability Section facilities include a library of reliability reference material and data storage as well as facilities for analysis of failures.

The present staff of the Reliability Section can absorb the activities required during Phase I of the Apollo contract.

4.0 PRODUCT ASSURANCE

4.1 The Product Assurance Organization

Product Assurance has the responsibility, independently, to assure that our products comply with applicable drawings and specifications and to advise and assist other organizations in carrying out the functions which affect product quality and reliability. A Product Assurance organization chart is shown in Figure 4.1.

Quality Control monitors and controls the fabrication, processing, assembly, and test of all products manufactured by Radiation Incorporated.

Purchased Materials Quality Control monitors and controls all purchased materials and vendor quality control practices and capabilities.

The Standardization Laboratories maintain standards traceable to NBS and periodically calibrate all electrical and physical measuring and process control equipment within the Company as well as critical manual and automatic tools.

Administrative, professional and quality control engineering support to the Product Assurance organization and other affected Radiation organizations is supplied by the Quality Assurance Services function. This function also periodically audits the Product Assurance functions, Radiation's compliance with contractual requirements, and the requirements of our quality control system.

A single quality assurance system is used throughout all operations and is applied uniformly to R & D work, and limited quantity fabrication by either Engineering or Manufacturing, including assembly, test and shipment. A Product Assurance Manual is available, upon request, which describes in considerable detail the quality assurance program that will be followed for the proposed hardware.

4.2 Compliance

As required by Terms and Conditions Clause 37 and elsewhere in the quotation request, our quality assurance system will comply with NASA Quality Publication NPC 200-2 dated April 1962, and, of course, with 200-3 without significant revisions or additions to present quality operations.

Prior programs at Radiation have shown the concepts of 200-2 to be desirable and necessary for development, manufacture, qualification, and test of satelliteborne, highly reliable equipment. The Radiation Quality Control System complies with MIL-Q-9858 and Air Force Specification Bulletins 515 (Control of Non-Conforming Supplies) and 520 (Calibration of Measuring and Testing Equipment). An Air Force Quality Control Representative and staff have been resident at Radiation for a number of years.

Our quality assurance practices comply with North American Aviation, Incorporated, General Requirements for Supplier's Quality Control System MQ 0802-001 (4 April 1962). Also, we have complied with the Boeing Quality Control Spec. D1-8000, on the Minuteman program (among many others) under the surveillance of a resident Boeing Quality Control Team for the past three years. A NASA resident is currently assigned to our facility in connection with the Nimbus program.

4.3 General Description of Quality Controls by Area

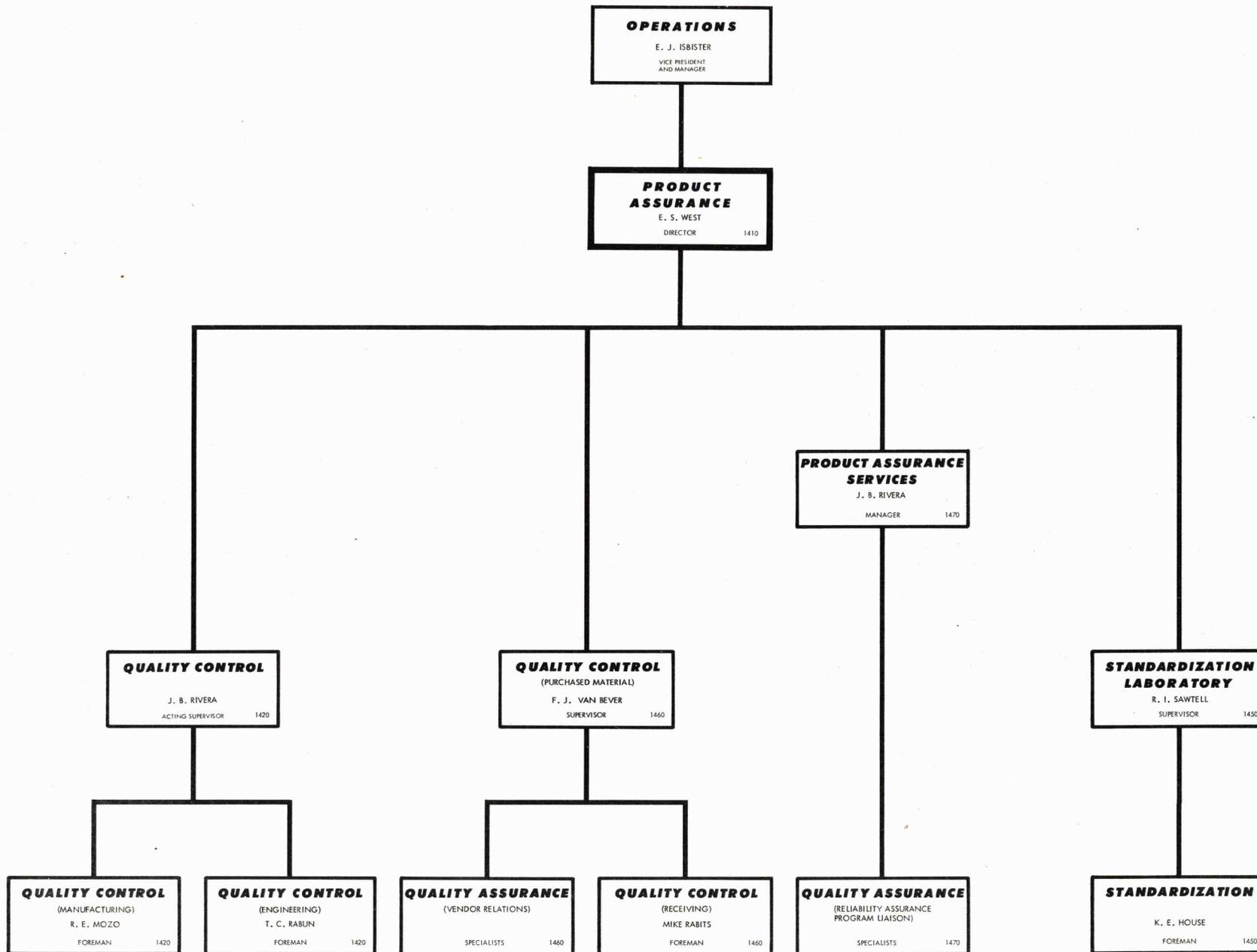
4.3.1 Design and Development

At Radiation, Product Assurance is an integral part of the Design Review Program. A Product Assurance representative participates in conceptual, major, and final design reviews. His function is to assure that internally invoked, as well as contractually invoked quality standards and requirements, are considered in the design at the outset. These standards and requirements must be reflected in the Engineering Drawings for internal use and in Procurement Specifications for purchased parts.

In addition, during this phase the Product Assurance Design Review Representative maintains close liaison with the Q. C. Inspectors on the project. He alerts them of possible quality problems and uses their feedback as a valuable input at subsequent Design Reviews.

4.3.2 Procured Material

Continuous vendor analysis assures that only vendors having adequate capability are utilized as sources for items purchased for Radiation Incorporated equipment. Vendor ratings influence ordering. Purchased Material Quality Control may approve, disapprove, or invoke additional controls on vendors as required. Additional assurance is derived through sophisticated receiving inspection practices.



RELATIVE LOCATION OF POSITIONS INDICATED
ON THIS CHART DOES NOT NECESSARILY DESIGNATE
COMMENSURATE EQUALITY IN AUTHORITY OR TITLES

Figure 4.1 Product Assurance Organization Chart

Special surveys of vendor's quality control systems and capabilities are made covering significant procurements.

Receiving Inspection involves the acceptance of only those parts whose quality conforms to the contract requirements. Methods used in Receiving Inspection include:

1. Purchase order review
2. Use of detailed inspection instructions
3. Supplier quality history records with periodic summary reports based on records of each item inspected
4. Procedure for use and control of necessary measuring equipment, gages and standards
5. Statistically and technically valid sampling
6. Discrepant material disposition review
7. Corrective action to prevent recurrence of discrepancies
8. Vendor counseling
9. Surveillance and inspection at source
10. Invocation of Radiation's "Supplier Quality Control System Requirements" on vendors (ES 155-900217) when desirable. For the Apollo Project NCP 200-3 and appropriate sections of NCP 200-2 would be invoked.

4.3.3 Inspection and Test

Each phase of fabrication is subjected to rigid tests and inspections. Criteria for acceptance of these inspections and tests are provided by Radiation Drawings, Specifications, Inspection Procedures, Test Procedures, and Standards. These Standards are widely distributed to using activities in four volumes. They are a useful tool to facilitate the specification of parts and assemblies and to specify the workmanship standards which are applicable. They also detail standard processes and inspection criteria. The Standard Process Manual contains a step-by-step breakdown of the process, analysis of applicable solutions, and a list of materials used.

Detailed Standard Workmanship Practices are distributed to operators and all inspectors. These standards are illustrative and indicate not only optimum practices with acceptance criteria, but also specifically warn against practices which are unacceptable. This type of workmanship standardization is one of the key reasons why all Radiation practices consistently represent the best current industry practices known. They are based on Radiation's extensive experience with missileborne telemetry systems. Over four-hundred standards appear in our Standards Manual and are utilized by Design, Manufacturing, and Product Assurance personnel.

The last phase of the inspection and test program is a thorough Final Acceptance Test to independently validated procedures, insuring operational performance of the equipment before delivery.

4.3.4 Non-Conforming Material

Non-conforming material is discovered, identified, and segregated at the various inspection stations of fabrication and assembly. The method of identification describes the cause of the defect and its disposition (standard repair, rework, MRB). Radiation has an operating Material Review Board with a resident AFQCR as chairman. This MRB in conjunction with established methods of controlling non-conforming material, complies with MIL-Q-9858, Paragraph 3.11, and USAF Specification Bulletin NR 515. It also complies with NCP 200-2, Paragraph 8.

4.3.5 Inspection and Test Equipment

Radiation has a sophisticated program for the calibration control of inspection and test equipment performed by the Product Assurance Standardization Laboratory. Inspection and test equipment is calibrated periodically against certified standards, traceable to the National Bureau of Standards. Indication of calibration status is shown on each piece of inspection and test equipment. Out-of-calibration equipment is tagged and its use is prohibited. Calibration records are maintained for each piece of equipment, and recalibration cycles are adjusted to compensate for wear and deterioration.

Our inspection and test equipment calibration program is in complete compliance with MIL-Q-9858, Paragraph 3.4, and USAF Spec. Bulletin NR 520. It also complies with NCP 200-2, Paragraph 9.

4.3.6 Failure Reporting and Corrective Action

A data collection program will be maintained during the production and testing phases. In brief, the task is divided into three major areas of work which are:

1. Collection, processing, summarizing, and organization of equipment operating time and discrepancies.
2. Analysis and investigation of discrepancies. Distribution of summary reports of discrepancies and status of follow-up action.
3. Testing adequacy of corrective action.

To minimize the manual handling and to expedite the analysis, the data is coded into IBM cards for processing on accounting machines. Data is continuously collected on the corrective actions and compared with the previous data to determine effect.

Forms will be prepared to facilitate the collection and dissemination of information. Summaries of all failures and corrective action taken will be prepared monthly.

Reliability studies will be maintained on the data.

4.3.7 Drawing Change Control

Radiation has a system of drawing change control which complies with MIL-Q-9858, Paragraph 3.3, and which will comply with NCP 200-2, Paragraph 2.3.

The Print Control Center distributes approved drawing changes to all holders of affected drawings, simultaneously. Obsolete drawings are picked up at the time of delivery of revised drawings.

Quality Control is one of the prime users of drawings under change control. As such, it is in a good position to monitor the timeliness and effectiveness of drawing change control on a continuous basis.

5.0 TECHNICAL DOCUMENTATION

5.1 General

The technical documentation requirement for Project Apollo follows closely the internal requirements established by Radiation-Melbourne, for pursuit of similar contracts. We have, as permanent support facilities, groups organized to implement engineering reports, specifications, sketches, drawings, general report writing, photographs, movies, support manuals, and requirement documents such as QC, reliability, purchasing, etc. The major group responsible is the Technical Services Division for the physical publication of technical documents. This division has drafting, technical writing, reproduction, photography, printing, provisioning, art, and typing departments. Rough drafts for specification items are obtained from the Engineering Division, Quality Assurance Division, Reliability Group, and associated corporate departments. The departments of the Technical Services Division then prepares the formal documents for issuance to the customer.

5.2 Requirements

The requirements for technical documentation of Project Apollo are summarized in Table 5.2. This table lists the document type, submission frequency, department in which prepared, and division furnishing preparation information. The documents will be transmitted via the Program Management Office.

5.3 Procedures

The formal documents will be initiated by the division performing a task, published by the Technical Services Division, correlated and submitted to Collins by the Technical Document Center of the program office. For example, the final drawings would be done by the drafting department of the Engineering Services Division utilizing the technical inputs from the Manufacturing and Engineering Divisions. The final prints and reproducible will then be transmitted by the documentation control center of the Program Office.

Drawings are prepared on drawing formats which meet, or exceed all requirements of MIL-STD-2B. Drawing practices used are defined by Company Drafting Manual which is based on MIL-D-70327.

Detail drawings are prepared for individually fabricated piece parts and are tabulated to depict similar parts where possible. Subassembly and assembly drawings contain a List of Material as an integral part of the drawing.

Schematic diagrams utilize MIL-STD-15 and MIL-STD-16 for graphic symbols and reference designations, respectively. Drawing quality is constantly reviewed for reproducibility, this quality permits reproducing to MIL-D-5480 and assures suitable copy for microfilming to MIL-M-9868 requirements. Technical correctness is maintained by a very thorough drawing check made prior to release.

Radiation prepares specification control drawings of all items supplied by vendors with their applicable part numbers.

Material and Process Specifications are documented in the form of "Company Standards" and are referenced directly on the applicable drawings. These specifications indicate the minimum requirements with procedural steps defined for uniform results.

Printed Wiring art work masters are prepared with the aid of a Haag-Streit Coordinatograph which maintains an accuracy of 0.001 inches over a thirty-six (36) inch length. Art work is usually made four (4) times size; consequently, when reduced, any inaccuracies are further reduced.

TABLE 5.2

TECHNICAL DOCUMENTATION REQUIREMENTS

DOCUMENT	SUBMITTED	SUBSEQUENT ISSUES	RESPONSIBLE GROUP	INFORMATION SOURCE
Equipment Specification	1 month, ARO	As Required	Data Systems Engineering	Project Engineer
Material Parts, Process Specifications	20 days/USE	As Required	Data Systems Engineering	Project Engineer
Preliminary Design	1 month ARO	As Completed on Major Changes	Data Systems Engineering	Project Engineer
Final Design	When design is Completed	As Required	Data Systems Engineering	Project Engineer
Program Plan	1 month	As Required	Program Management	Program Manager Staff
Facilities Plan	1 month	As Required	Program Management	Program Manager Staff
Test Plan	1 month	As Required	Data Systems Engineering	Project Engineer
Manufacturing Plan	1 month	As Required	Manufacturing Division	Production Engineering
Reliability Plan	1 month	As Required	Engineering Division	Reliability Design
Quality Control Plan	1 month	As Required	Product Assurance Division	Quality Control
Monthly Progress Report	1st day of First Month	18th day of each month for first two months of calendar quarter	Program Manager	Project Engineer
Quarterly Progress Report	5th day of third month of each calendar quarter	5th day of third month of each calendar quarter	Program Manager	Project Engineer
Final Report	3 months after completion of all other technical contractual requirements		Program Manager	Project Engineer
Monthly Weight and Balance Reports	20th day of first month	20th day each month	Program Manager	Project Engineer
Test Equipment List	1 month ARO	As Required	Data Systems Engineering	Program Manager
Emergency Action Reports	As Required	--	Data Systems Engineering	Project Engineer
Quarterly Reliability Status Report	Last day of calendar quarter	Last day of each calendar quarter	Data Systems Engineering	Program Manager
Equipment Status Report	1 December 1962	As Required	Data Systems Engineering	Project Engineer
Technical Data, Reports and Analyses	2 weeks after completion of each block of effort or logical subdivisions thereof	--	Data Systems Engineering	Project Engineer
Design Information	As Required	--	Data Systems Engineering	Project Engineer
Notice of Proposed Vendor Survey	15 days prior to intended survey	--	Subcontract Coordinator	Program Manager
Notice of Vendor Selection	15 days prior to selection	--	Subcontract Coordinator	Program Manager
Still Photographs	17 days after exposure submitted weekly	--	Technical Services	Publications
Motion Picture Photography Documentation	10 days after shooting	--	Technical Services	Publications
Film Clips	6 days after completion of shooting	--	Technical Services	Publications
Basic Materials Reports	Last day of second calendar quarter	Subsequent report last day of every other calendar quarter. Final report 1 month after completion of the work for the final period of the contract.	Product Assurance	Quality Control

TABLE 5.2 (Continued)

TECHNICAL DOCUMENTATION REQUIREMENTS

DOCUMENT	SUBMITTED	SUBSEQUENT ISSUES	RESPONSIBLE GROUP	INFORMATION SOURCE
Qualification Status List Qualification Procedures, Reports and Data	3 months ARO Procedures: 1 month prior to intended use. Reports: 15 days after each test series	5th day of each month As Required	Data Systems Engineering Data Systems Engineering	Project Engineer Project Engineer
Failure Data	5 days after Failure	As Required	Engineering	Reliability Design
Monthly Failure Summary	3 months after start of contract	Last day of each month	Engineering	Reliability Design
Acceptance Test Data Sheet	15 days after each test	--	Data Systems Engineering	Project Engineer
Data and Reports on other tests	20 days after each test or test series		Data Systems Engineering	Project Engineer
Part Application Reports, Procedures and data	Procedures: 15 days prior to intended use Reports: 1 month after completion of test	As Required	Engineering and Product Assurance	Reliability Design and Quality Control
Part Screening Procedures	15 days prior to Intended use	As Required	Product Assurance	Quality Control
Failure Analysis and Corrective Action Reports	15 days after failure	As Required	Engineering	Reliability Design
Development Tests	--	--	Data Systems Engineering	Project Engineer
Explanatory Tests	Procedures: 30 days prior to use. Reports: 1 month after completion of test	As Required	Data Systems Engineering	Project Engineer
Hardware List	60 days after Contract Award	As Required	Program Manager	Project Engineer/Manu- facturing Engineer
Special Sampling Plans	45 days prior to intended use	As Required	Product Assurance	Quality Control
Inspection Measuring and Test Equipment Procedures	1 month ARO	As Required	Product Assurance	Quality Control
Monthly Quality Report	31 December 1962	End of Each month	Product Assurance	Quality Control
Quarterly Summary of Quality Control Performance Audit	31 December 1962	End of each calendar quarter	Product Assurance	Quality Control
Inspection and Test Procedures	45 days prior to intended use	As Required	Product Assurance	Quality Control
Process Control Procedures	1 month prior to intended use	As Required	Product Assurance	Quality Control
Storage Procedures for end items	1 month prior to intended use	As Required	Product Assurance	Quality Control
Application of Sampling Plans	1 month prior to intended use	As Required	Product Assurance	Quality Control
Assembly Standards	1 month prior to intended use	As Required	Product Assurance	Quality Control
Approval Drawings	5 days after release	5 days after release	Technical Services	Drafting
Maintenance Drawings	As Released	As Released	Technical Services	Drafting
Final Drawing	3 months after completion of all other technical require- ments	--	Technical Services	Drafting

TABLE 5.2 (Continued)

TECHNICAL DOCUMENTATION REQUIREMENTS

DOCUMENT	SUBMITTED	SUBSEQUENT ISSUES	RESPONSIBLE GROUP	INFORMATION SOURCE
Data List	With final drawings required per final drawings above	--	Technical Services	Drafting
Drawing List	2 months after contract award	Every 2 weeks	Technical Services	Drafting
Provisioning Parts Breakdown	30 days after 100% drawing release	Monthly	Technical Services	Project Engineer
Checkout Manuals	30 days prior to equipment delivery	As Required by changes and equipment deliveries	Technical Services	Publications
Maintenance and Repair Manuals	30 days prior to equipment delivery	As Required by changes and equipment deliveries	Technical Services	Publications

6.0 GROUND SUPPORT EQUIPMENT

This section of the proposal describes the Ground Support Equipment recommended by Radiation for the Apollo Telemetry System. This section also includes the design philosophy of the GSE and its intended usage.

6.1 Statement of Problem

During the design, development, manufacturing, test and integration of complex equipment such as required for the Apollo program, GSE is required that is capable of accurately and reliably determining the performance of the system. The GSE as described herein is, in general, required at several levels of usage in the program and at several geographical locations.

Two basic types of equipment are recommended. The first type may be called Simulation and Test Equipment and the second Telemetry Checkout Equipment. The requirements placed upon each of these two types are generally described in the following paragraphs.

6.1.1 Simulation and Test Equipment

Simulation and Test Equipment as described herein provides three functions, consisting of:

- o Simulation and/or simulation of system inputs,
- o Acquisition of measured system responses and
- o Evaluation of test results.

In order for the results and conclusions of a test to be valid, the test equipment must be reliable and must not cause a malfunction or introduce errors in the system under test. Semi-automatic test equipment is also desirable for this application due to the large number of input channels and number of parameters that must be measured and interpreted.

Simulation and test equipment is required at the seller's facility to determine the over all system performance, particularly in final proof testing prior to shipment. Additional equipment is also required at the customer's facility as the telemetry system is integrated with other system components. Simulation and test equipment is also required by the customer and the military agency to assure that the system is performing its intended functions within the limits specified. The equipment required at the seller's facility will be included as part of the proposed system and will be similar to the simulation and test equipment described herein. Additional systems are recommended at the customer's facility for acceptance testing and for system integration.

Simulation and test equipment is required at the launch complex to provide a rapid means of functionally testing the system during the pre-flight phases of the mission. Although the requirements placed upon this system are not as stringent as those for final proof testing, all simulation and test systems will be identical. This alleviates the requirement for two different designs. In the case of the functional test equipment, a modified program can be used to reduce the number of measurements and therefore the time required to perform each test.

The simulation and test equipment must not only check the operational portion of the telemeter, but also the built-in calibration and self-checking equipment. For the test results to be considered reliably, the test equipment, both built-in and GSE, must perform accurately and within the limits specified. Each function must be checked to determine that the system is performing as required. This requires an understanding of the system under test, the parameters to be measured and their inter-relations, and how the various error contributing factors must be combined in predicting the overall system performance. This, almost of necessity, requires that the supplier of the telemetry system design and build the simulation and test equipment.

Since the system will be used by relatively inexperienced personnel, it must be simple and reliable to operate. Each mode of operation will, therefore, be switch selectable and the channels to be processed will be programmed into the test equipment through punched paper tape. The test system must also include self-checking features so that its accuracy and operational performance is known prior to each test.

6.1.2 Telemetry Checkout Equipment

During the pre-launch phase GSE will be required at the launch complex to receive data from the spacecraft for display and permanent storage. This equipment, of necessity, must be designed to meet different functional requirements than the simulation and test equipment, since it will be used after the telemetry system has been installed in the spacecraft. The telemetry system will not be as accessible as if it were placed on the bench. It is therefore desirable, if not necessary, to check out the telemetry system over an R. F. or hardwire link. The same checkout system can also be used to meet the needs of collecting and monitoring data over the telemetry system as the other parts of the spacecraft are stimulated during a pre-launch checkout. In this way, proper operation of the system can be determined by comparing the stimulation forces to the telemetered output. The

checkout equipment can also be used to provide data acquisition, display and permanent data storage during the pre-flight phase of the mission, either during the boost into orbit or during passage of the spacecraft over the receiving site.

6.1.3 General Requirements

General purpose test equipment is not available to meet all of the requirements stated in the preceding paragraphs. Special purpose simulation and test equipment, as well as telemetry checkout equipment, must therefore be provided. The design of this equipment requires a detailed knowledge of the telemetry system, both as to its operation and detailed design. The general requirements that this equipment must meet can be described as follows.

GSE, if it is to perform its intended function, must provide operator simplicity such that it can be rapidly and accurately programmed. It must perform its task rapidly since many parameters must be measured if the over-all performance of the system is to be determined in a reasonable time. When one considers the fact that most systems employ hundreds of input channels whose accuracy must be determined, in some cases statistically, it becomes obvious that the GSE must operate at high speed.

With the advent of high-accuracy systems, the performance requirements for the GSE have been increased proportionally. This requires the careful selection and design of precision input simulators, encoders, multiplexers, etc.

GSE is required in many cases to operate reliably and accurately over extended and severe environments. This must be considered in the selection and design of the equipment.

Standardization is also desirable since the equipment may be used not only for one program but for several programs. Standardization and modular construction help to improve the logistics of supply, since fewer numbers and types of spare parts need to be stocked for all systems.

GSE should always include self-checking features to assure the operator that the equipment is operating within design limits before it is used. Self-checking should rapidly and accurately measure the performance of the test equipment.

6.2 Levels of Usage

The two types of test equipment as described in the preceding sections will be required at several levels within the program. The following paragraphs list the quantity and location of the recommended GSE and the level of usage.

6.2.1 Simulation and Test Equipment

Simulation and special purpose test equipment is recommended as follows:

- 1 set - System integrater's facility or customer facility
- 1 set - Located at the launch site or near the launch site

6.2.2 Telemetry Checkout Equipment

Telemetry checkout equipment as proposed herein is recommended at the following locations and in the quantities indicated.

- 1 set - System integrater's or customer facility
- 2 sets - Located at or near the launch site.

6.3 Technical Description

Equipment meeting all of the requirements described in Section 4.0 of the specification have been designed and developed by Radiation for other similar programs. Typical examples are the Airborne Telemetry System Input Simulator for the Titan I and Titan II programs; Checkout Rack Test Fixture for Titan I and Titan II; Simulation and Test Equipment for the Minuteman Airborne System and Telemetry Data Acquisition Systems; Telemetry System Test Sets for NASA for the Nimbus Program, as well as Simulation and Test Equipment for NASA on the OAO Telemetry System.

The discussion that follows describes typical test and checkout equipment recommended to Collins Radio Company for use with the Apollo Telemetry System. In nearly all cases, the proposed equipment can be implemented with components developed on previous programs. In all cases the equipment will utilize standard building block techniques and all solid state construction.

6.3.1 Simulation and Test Equipment

The functions that will be performed by the recommended simulation and test equipment are as follows:

- o Measure the individual channel accuracy including offset, gain, quantizing error, common mode, and source loading error.
- o Determine proper channel sequencing.
- o Measure inter-channel crosstalk.
- o Provide external commands and sync signals to control the telemetry system in all modes of operation.
- o Measure the linearity on selected channels.
- o Measure the primary voltage, current and frequency.
- o Determine correct operation of the built-in calibration and self test equipment, including the accuracy of all standard voltage levels.

The block diagram of the proposed simulation and test equipment is illustrated in Figure 6.3.1. The proposed system provides continuous monitoring of the primary voltage, current and frequency. Visual monitoring is provided by a meter display for voltage and current. Voltages representing the magnitude of the primary voltage and current are also fed to a sequencer that sequentially samples the input for digitizing and recording on the printer. The primary frequency is converted to an analog voltage, digitized and printed out. Thus, as the results of the test are tabulated, the input primary power is also tabulated for reference purposes. This feature of the system is also useful for tests that require that the input voltage and frequency be varied.

The simulated data inputs to the telemetry system are derived from a programmable precision voltage source controlled by a programmer. The low impedance outputs from the precision voltage source are fed through pre-selected series resistors to simulate input source impedances. Thus, errors due to loading of the source impedance by the system input will be measured as part of the overall system accuracy, as well as the offsets due to leakage currents through the source impedance.

In the case of the low-level inputs, a common mode voltage will be applied of pre-determined magnitude. The effect of this signal is also measured as part of the overall system error.

Outputs from the precision voltage source are fed to the sequencer and to a digital volt meter. The digital volt meter is required only for maintenance and repair of the simulation and test equipment. The digital values representing the analog data inputs to the system are fed to a comparator where they are compared to the digital output from the telemetry system. The digital comparator is controlled by the programmer such that the data outputs out of tolerance are detected and printed out. A go/no-go indicator light is also provided to indicate channels out of tolerance.

The simulated analog data inputs are fed to the telemetry system where they are sequentially sampled, digitized, combined with digital data, and fed out serially. The serial output from the telemetry system is fed to a serial-to-parallel converter in the test set. At this point the outputs from the converter are fed to a visual display for read-out of any selected data channel, to a sync pattern detector and to the digital comparator previously described.

The sync pattern detector functions to check each parallel data word to determine if it contains a sync pattern. If recognition occurs at the proper place within the frame a symbol is printed out by the printer. If correct sync recognition does not occur, an error symbol is printed. The sync pattern detector will be similar to that developed on the Minuteman program. This detector can be programmed to recognize any combination of ONE's or ZERO's in a word through the use of toggle switches. The detector is so designed that an output occurs whenever a sync pattern is detected.

The visual display consists of three Nixie lights which are used to indicate the decimal value of any selected data word. The word for display is selected by the programmer.

The programmer is the heart of the simulation and test system and is used to control the entire system, including the telemetry system. In the latter case, the programmer supplies the required format control signals as well as sync signals to the telemetry system. Through the programmer the telemetry system can be checked in each of its modes of operation.

The programmer includes a punched paper tape reader, which is used to read-in each new set of test conditions. These instructions may include such items as the magnitude of the input voltages to the system, the tolerance limits for the digital comparator, the channel sequence, etc. New programs can be readily and rapidly inserted through the read-in of the punched paper tape. This essentially eliminates the necessity for multitudes of switches and controls for each test configuration and greatly reduces the time required to set up each new test condition.

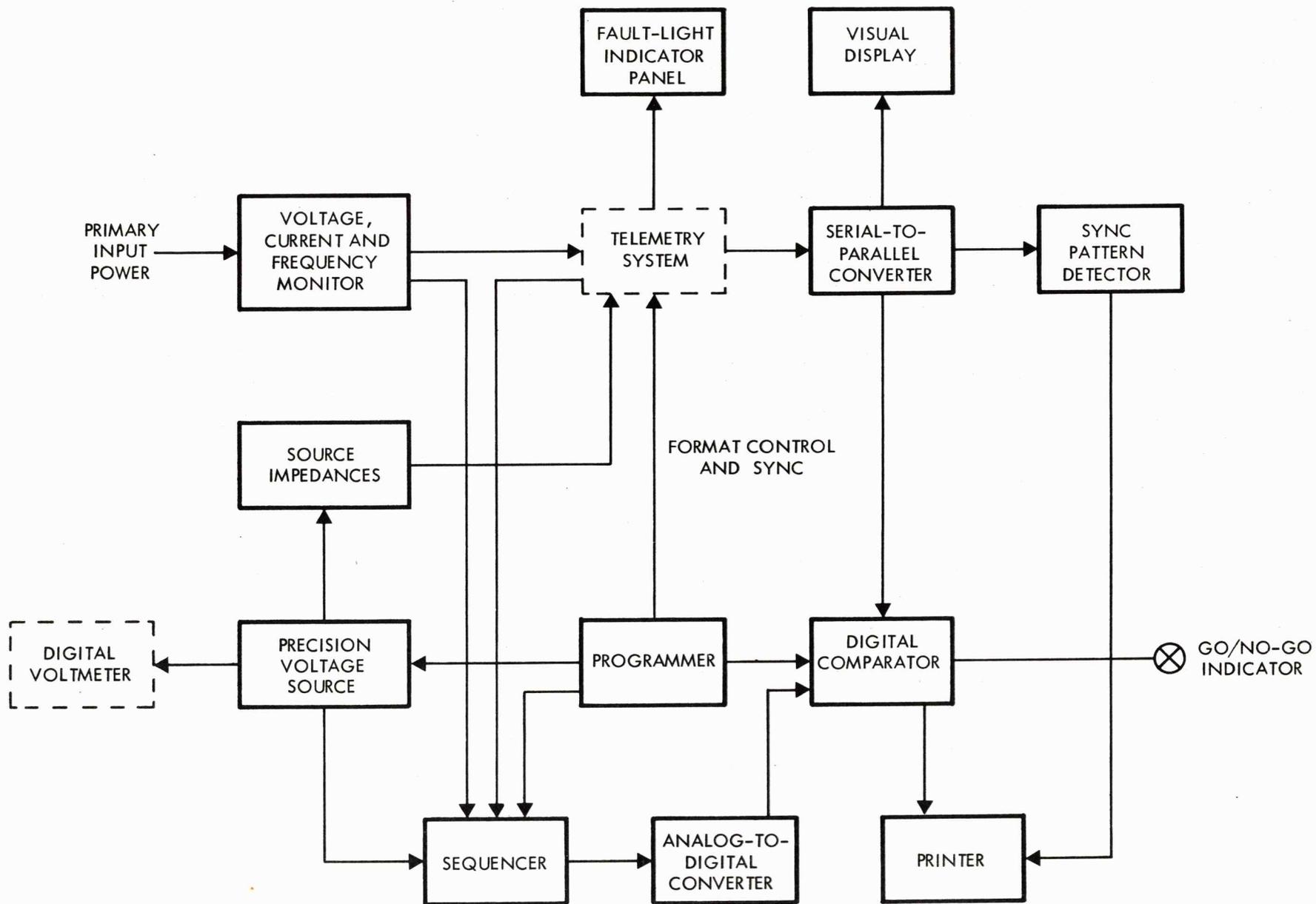


Figure 6.3.1 GSE Simulation Checkout Equipment

A printer is proposed to tabulate the data from the telemetry system in the sequence that the data channels occur. Channels out of tolerance will be indicated in red. The occurrence of the unique sync pattern will be indicated by a special symbol. Since known inputs will be fed to the system input, proper sequencing of the telemeter can be checked by referring to the tabulated print-out and their relationship to the special sync symbol. Out of tolerance channels can be readily detected by noting the print-outs in red.

Since the telemetry system does not include indicators for calibration and self-checking system, an indicator panel will be supplied as part of the simulation and test equipment. As simulated inputs are applied to the system the calibration system will be checked. Since data channels are tabulated in their proper sequence, when the system is operating correctly, the results of the tests of the system can be compared to the indicated fault conditions. In this test of the calibration system the standard voltage levels applied to the system as calibration inputs are fed to the sequencer and the digitized data is tabulated by the output printer. Thus, the operator has a continuous check of the calibration voltages as the system tests are performed.

Since the test equipment may not indicate correct operation of the calibration system when the system is not in fault, faults must be introduced into the system. This is accomplished by bringing out part of the calibrator voltage divider to test points on the telemetry system. The test equipment can be connected to these test points and the calibration voltages can be varied by predetermined amounts. Since the comparator in the calibration system has a fixed program, varying the calibration voltages has the effect of introducing a fault in the system. Since faults can be introduced at several places in the system using this method, the operation of the calibration system can be completely checked.

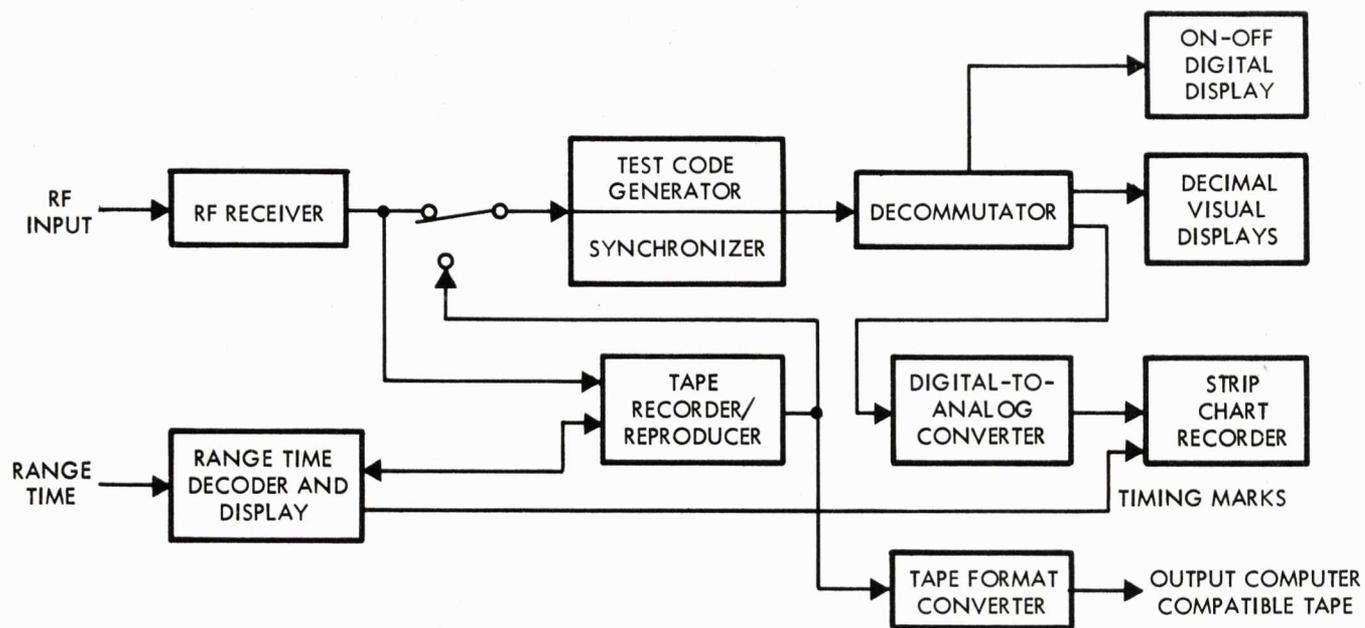
Since the simulation and test equipment will be used primarily in bench testing, it will be hard-wired to the telemetry system through connectors and through test points. All test points will be buffered so that shorts to the test point will not affect the operational accuracy of the system. The operational system is here defined such that it does not include the calibration and self-checking system.

The telemetry calibration system also includes a counter and matrix for checking the sequencing of the telemeter. These elements will be checked by the simulation and test system by introducing an error into the calibration system counter. The introduction of this error will not affect the operational accuracy and performance of the telemetry system, but at the same time provides a check of the correct operation of the built-in calibration system.

6.3.2 Telemetry Checkout Equipment

A block diagram of a typical Telemetry Checkout Equipment is illustrated in Figure 6.3.2. A similar system was built by Radiation for the Minuteman program. The system recommended performs the following functions:

- o Receiving data over RF or hardwire link
- o Recording received data on magnetic tape
- o Real time data display
- o Formatting for data entry into digital computers.



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Figure 6.3.2 Block Diagram, Typical Telemetry Checkout Equipment

APPENDIX A

MAGNETIC COMMUTATOR

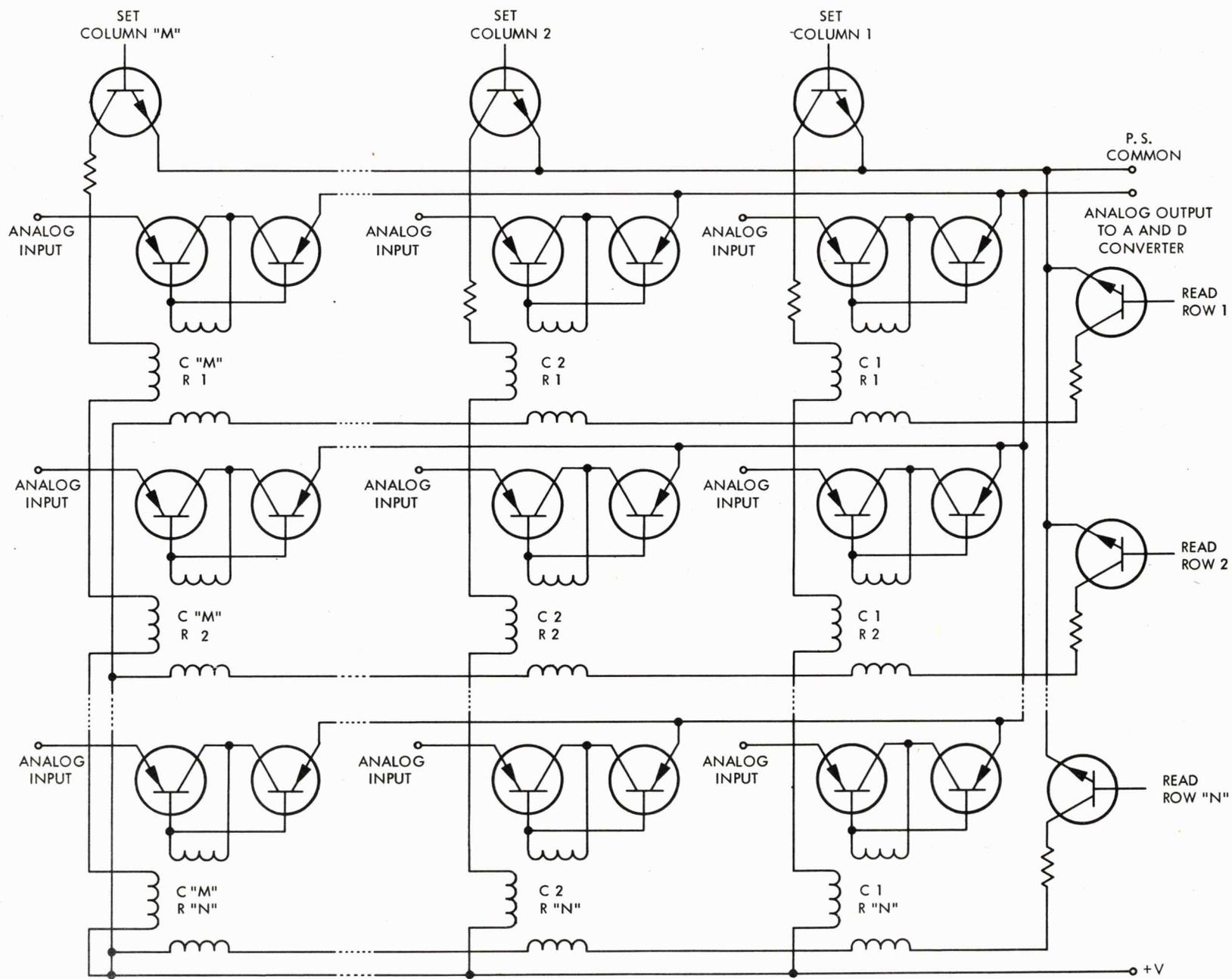
Shown in Figure A1 is a magnetic commutator with the transformers and gates connected in an "M" column, "N" row matrix array. The transistor gates generally used for switching high-level analog signals, are driven by the transformers which also act as magnetic logic elements to aid the sequencing of channels.

The switching element consists of two transistors, operating in the inverse configuration, with the collectors connected. This configuration results in very low emitter-to-emitter impedance and offset voltage when the switch is energized. The switch is non-conducting during the absence of a drive signal from the transformer. Driving the gates with a transformer not only facilitates sequencing logic but also effectively isolates the drive circuit from the signal circuit permitting greater accuracies.

The gate transformers have cores made of square-loop magnetic material which are driven into a state of negative saturation by current through a SET winding and into a state of positive saturation by current through a READ winding. The windings are polarized so that the gate is energized only when the core is changing from a state of negative saturation to positive saturation. This means that, if the hysteresis loop of the core material is sufficiently square and the core is completely saturated, the gate will be activated only by the first READ signal after the core has been SET. Additional READ signals to the transformer will not activate the gate until the core has again been set. This permits their use in the matrix array.

As shown in Figure A1, the SET windings of all transformers in a column are connected in series, and the READ winding of all transformers in a row are connected in series. With this array, a single set signal will set all the cores in a column. A single READ signal will be sent to all transformers in a row, however, the only gate in that row which will be activated will lie in that column of transformers which had been SET. Thus, all channels may be gated in sequence by sequentially setting each column and reading all rows.

The Timing Diagram, Figure A2, shows the time relationship of events necessary to sequentially sample all channels. The diagram is symmetrical because of an assumption that the sampling rate of each channel was one sample per frame. If



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Figure A-1 High-Level Magnetic Commutator

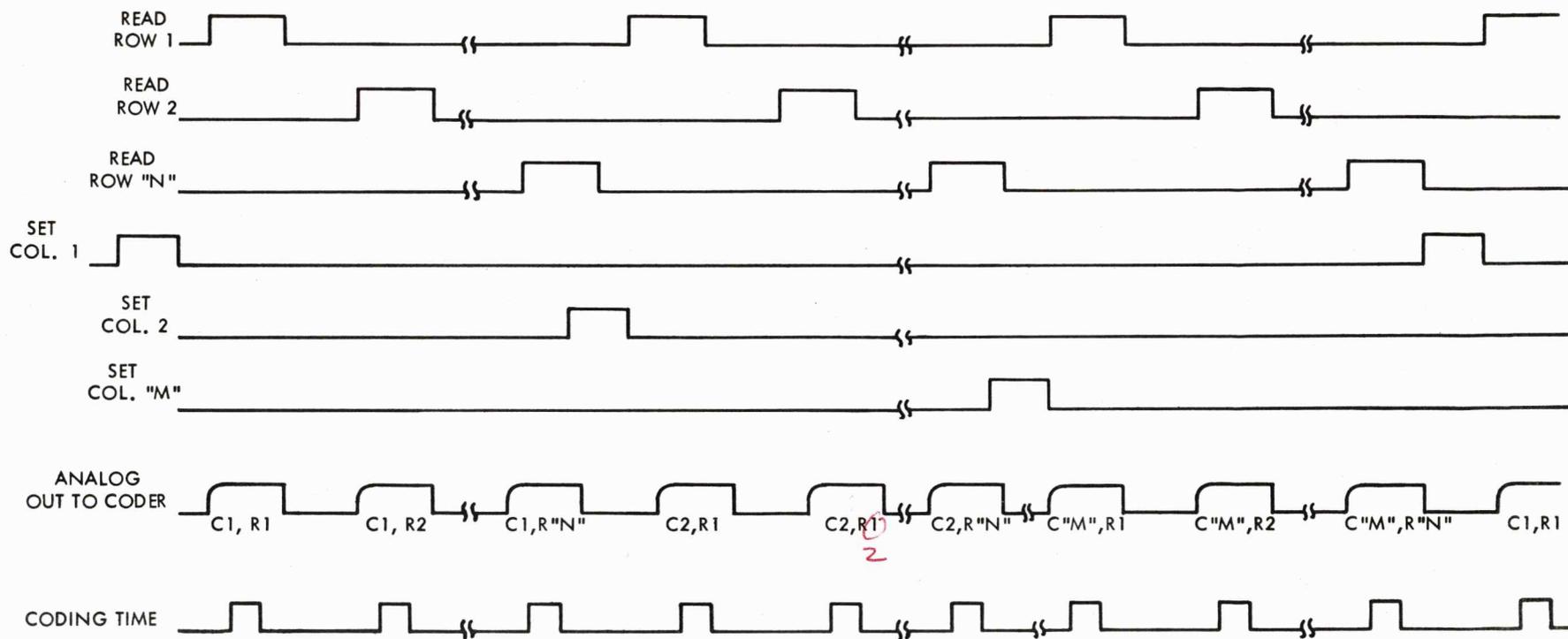


Figure A-2 Magnetic Commutator Timing

super-commutation is desired one or more columns may be set more than once per frame. In fact any timing may be achieved as long as the following requirements are met:

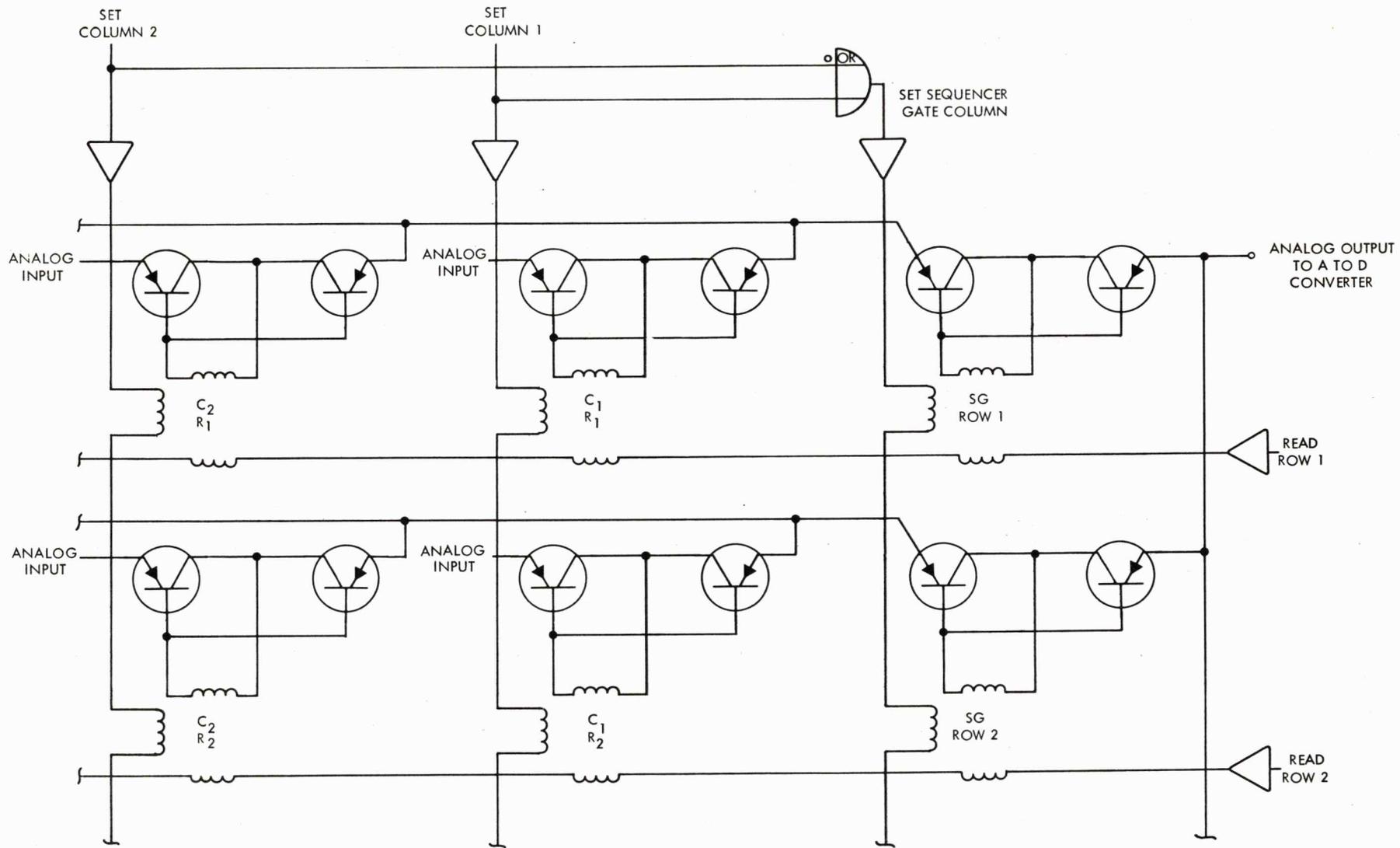
1. Pulse widths of SET and READ signals must be sufficient to saturate cores.
2. There must be sufficient time between READ signals to SET a column.
3. All gates in a column must be READ before another column is SET.

The matrix configuration shows the output of all channel gates tied to a common analog output. Theoretically, it would be possible to have any number of rows and columns connected as shown; however, practically, there is a limit to the number of gates which may be tied together.

It was assumed earlier that a gate was completely non-conducting when not activated. Since the gates are transistors, there will be leakage currents through each closed gate in the order of two to three nanoamps. The currents from each gate will add, Flow-Back through the open gate and appear as feedback current to the source impedance, causing an error in the analog voltage being sampled. The error is proportional to the magnitude of the source impedance and the feedback current. The feedback current is in turn proportional to the number of gates tied to a single point. It may be necessary to limit the number of gates tied to a single output in order to achieve stringent accuracy specifications. Also, each gate has some capacity, on the order of ten picofarads, which, collectively, could seriously degrade the rise time of the analog signal. This is another reason to limit the number of gates tied to a single output.

A method of achieving a reduction in the number of gates to a single output point and still maintain the same logic is to use Sequencer Gates as shown in Figure A3. The outputs of all channel gates in one row are connected to a sequencer gate which is opened each time a READ signal is applied to that row. Thus, the sequencer gate is open each time any channel gate in its row is open. To function in this manner, it is only necessary to SET the sequencer gate column each time any other column is SET.

The outputs of all sequencer gates are tied to a common line to the A to D Converter. By using sequencer gates, the number of gates tied to a single output is reduced to one row plus the column of sequencer gates. The feedback currents and



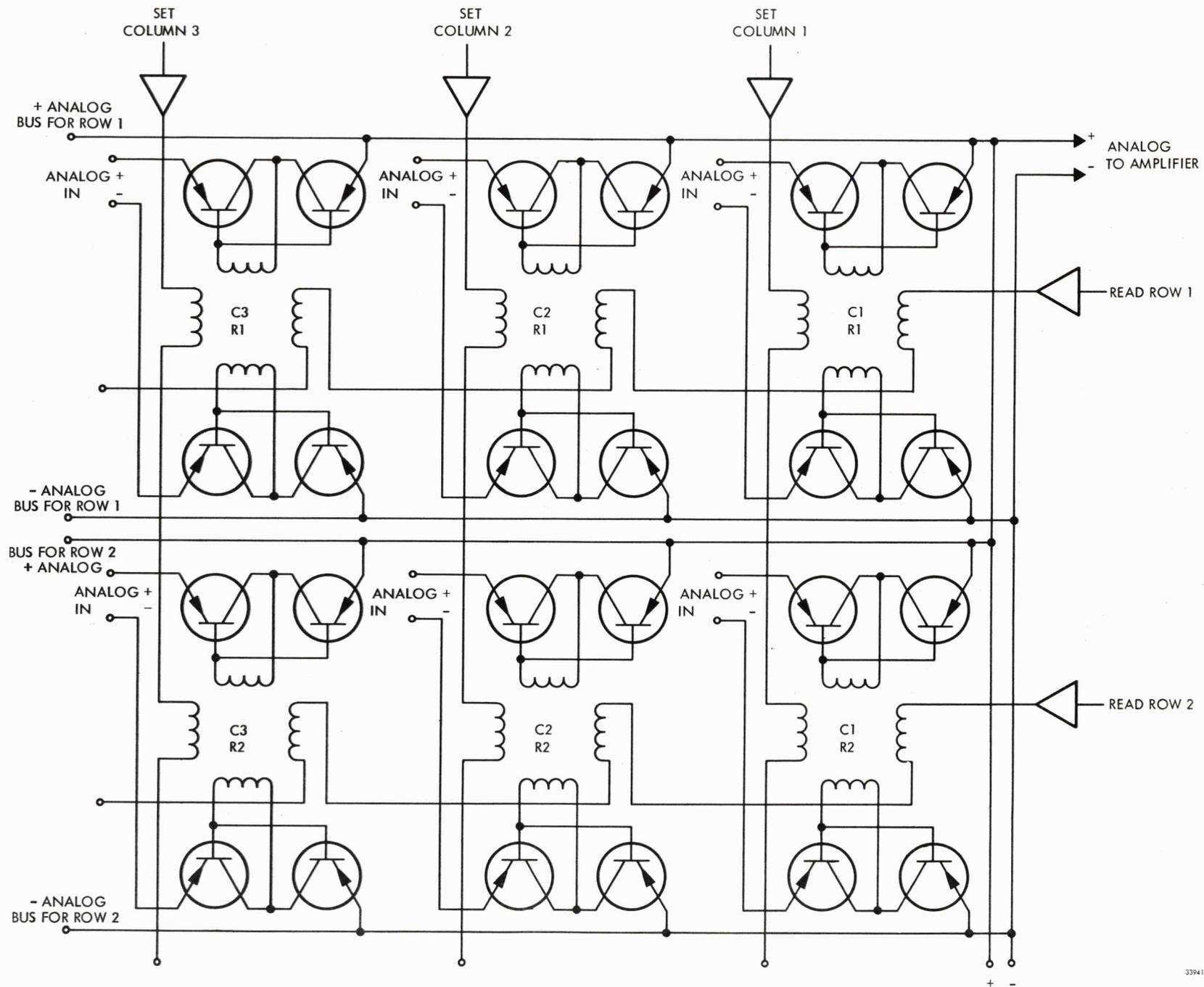
33940

Figure A-3 Magnetic Commutator With Sequencer Gates

total gate capacitance presented to the analog sources are therefore reduced by the same amount, resulting in greater accuracies in analog signals presented to the A to D Converter.

The commutation of the low-level analog signals is usually accomplished in such a manner that the signals are presented differentially to an amplifier. A method of achieving this is shown in Figure A4. Each gate has two switches which are activated simultaneously by the same transformer. The plus and minus analog inputs, representing a differential signal from one analog source, are presented simultaneously to the amplifier. Sequential sampling of each low-level channel is achieved by the same SET and READ considerations required by the high-level commutator.

The use of Sequencer Gates are more necessary for low-level commutating than high-level except when a Clamped Amplifier is used. Sequencer gates for low-level signals would be the same as shown in Figure A3 except that each gate would have the two switches for plus or minus analog signals.



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Figure A-4 Low-Level Magnetic Commutator

APPENDIX B

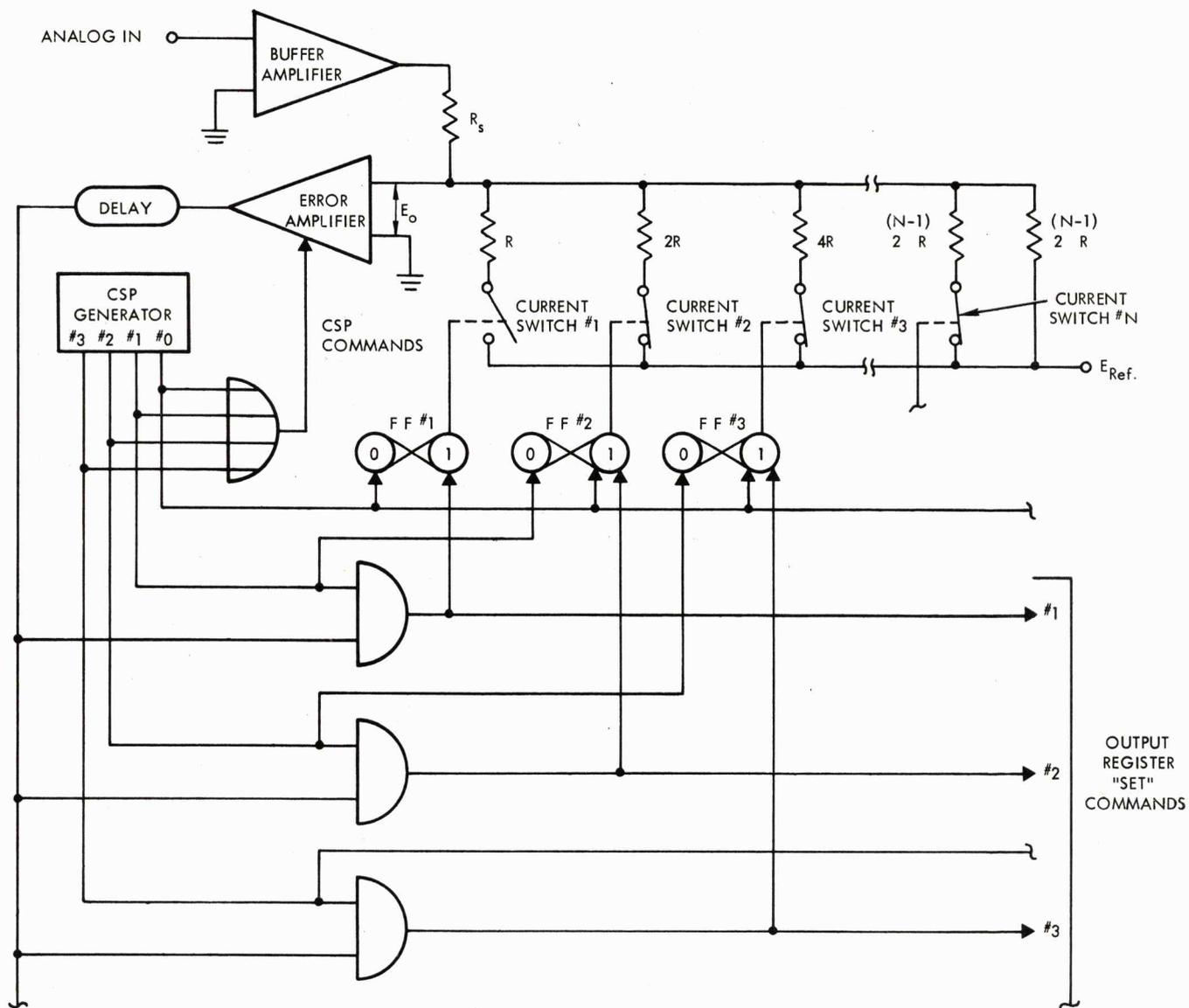
ANALOG-TO-DIGITAL CONVERTER

High-speed analog-to-digital conversion may be achieved by use of the half-split sampling technique shown in Figure B1. The single-ended analog signal is presented to the summing resistor R_s through the Buffer Amplifier which has unity gain. The current summing network is such that, with full scale analog in, and all current switches closed, the input to the Error Amplifier, E_o , is zero. There is no output from the Error Amplifier unless E_o is positive. Also necessary for an Error Amplifier output is a Code Sequential Pulse command from the CSP Generator.

A Current Switch is closed only when its respective Current Switch Flip-Flop is in the ONE state. Current Switches "1" through "n" represent "most significant" to "least significant" bit, respectively, in the Output Register. That is, with only Switch No. 1 closed, E_o would approach zero as Analog approached 50% Full Scale. Similarly, with only Switch No. 2 closed, E_o would approach zero as the analog input approached 25% of Full Scale, etc.

Assume that full scale analog is applied to the Buffer Amplifier and a coding sequence has just begun. Refer to the timing diagram in Figure B2. All Error Amplifier outputs are delayed so that they "overlap" the following CSP pulse, indicated by the shaded area in the waveforms.

CSP No. 0 resets the Current Switch Flip-Flops so that all current switches are closed except Switch No. 1. Since the Analog is assumed full scale, E_o will be positive and a delayed output from the Error Amplifier will AND with CSP No. 1. This Set Command No. 1 sets the most significant bit into the output register and closes Current Switch No. 1 by setting Current Flip-Flop No. 1 to the ONE state. CSP No. 1 also opens Current Switch No. 2 by setting Current Flip-Flop No. 2 to the ZERO state. With full scale Analog in, E_o will still be positive, and the delayed output from the Error Amplifier will AND with CSP No. 2. This Set Command No. 2 sets the second most significant bit in the output register and closes Current Switch No. 2 by setting Current Flip-Flop No. 2 to the ONE state. CSP No. 2 also opens Current Switch No. 3 and this sequence of events continues until all bits are set into the Output Register.



slide 7

Figure B-1 A to D Converter

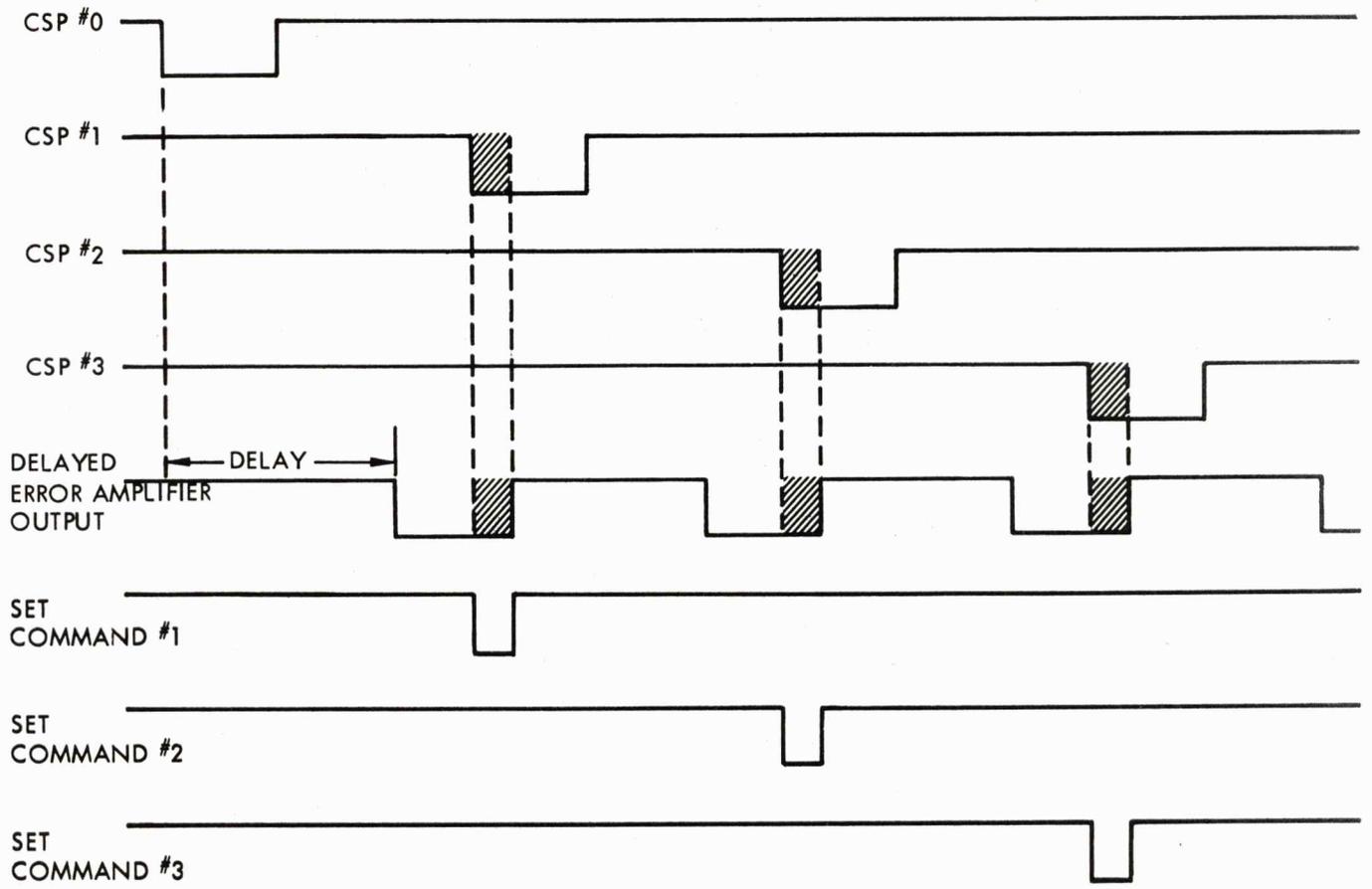


Figure B-2 A to D Converter Timing

Similarly, if the Analog In had been zero, E_o would never have been positive, and no output would have been available from the Error Amplifier. Therefore, no bits would have been set in the Output Register. In this manner, a digital code word may be generated for any analog signal between zero and full scale with a resolution equal to the "weight" of the least significant bit. The "weight" of the least significant bit is: $\frac{\text{Full Scale Analog (in volts)}}{2^N - 1}$

where $N =$ number of bits in full scale digital word.

Example: Full Scale Analog = 5 V

Number of Bits in
Full Code Digital
Word = 8

$$\begin{aligned} \text{Weight of Least Significant Bit} &= \frac{5 \text{ V}}{2^8 - 1} = \frac{5 \text{ V}}{255} \\ &= 19.6 \text{ m V} \end{aligned}$$

APPENDIX C

SYNCHRONIZATION ASPECTS

Bit Synchronization:

In comprehensive airborne data handling systems, consideration should be given to providing a capability of using any of three NRZ transmission types interchangeably. These types are:

NRZ - Type C - In this type a ONE is represented by one state and a ZERO by the second state.

NRZ - Type M - In this type a ONE is represented by a change of state while a ZERO is represented by no change in state.

NRZ - Type S - In this type a ONE is represented by no change of state and a ZERO by a change of state.

The first of these three types is the most commonly used, and if the data is of a random nature, the probability of extended intervals without a transition becomes remote. Consequently, no difficulty is usually encountered by the ground station due to lack of transitions.

While it is relatively simple to construct a bit synchronizer which will not drift in the absence of transitions, it is impossible to build one that will not attempt to lock on to noise of about the same frequency as the oscillator of the phase-lock loop. Furthermore, it has not been demonstrated that clamping on the last error signal is the most desirable mode of operation for a bit rate synchronizer.

If there is a good probability that long strings of ONE's or ZERO's will occur due to test procedures or normal operation, the provision should be made in the data handling equipment for all three types of NRZ signals.

The decision to do this, however, should be weighted by the effect which such a change will have on the mean-time-between-failure of the airborne telemetry equipment.

Frame Synchronization:

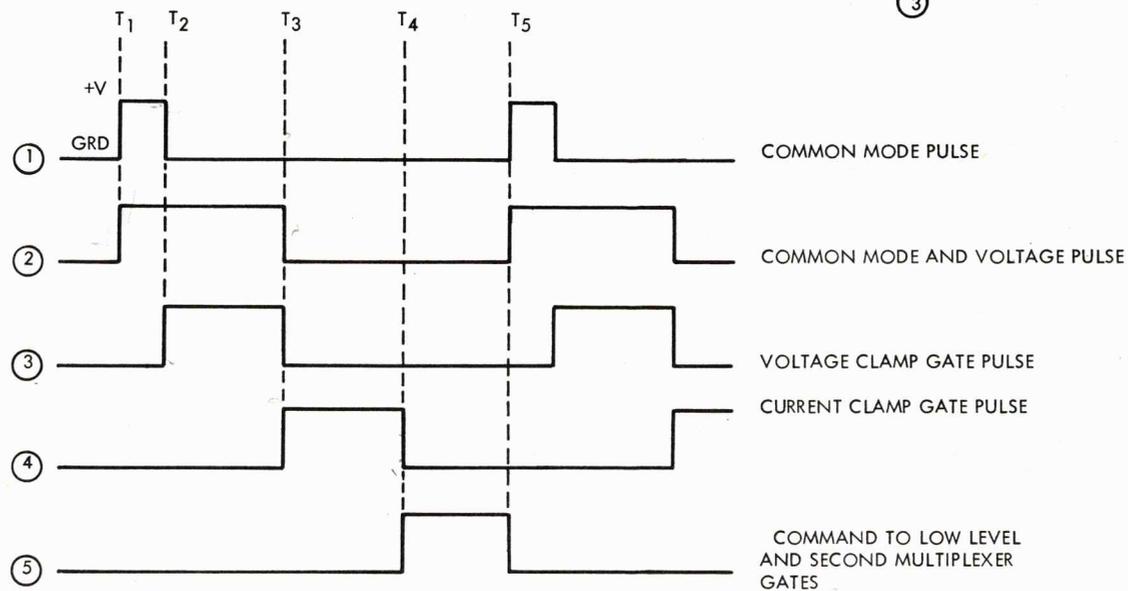
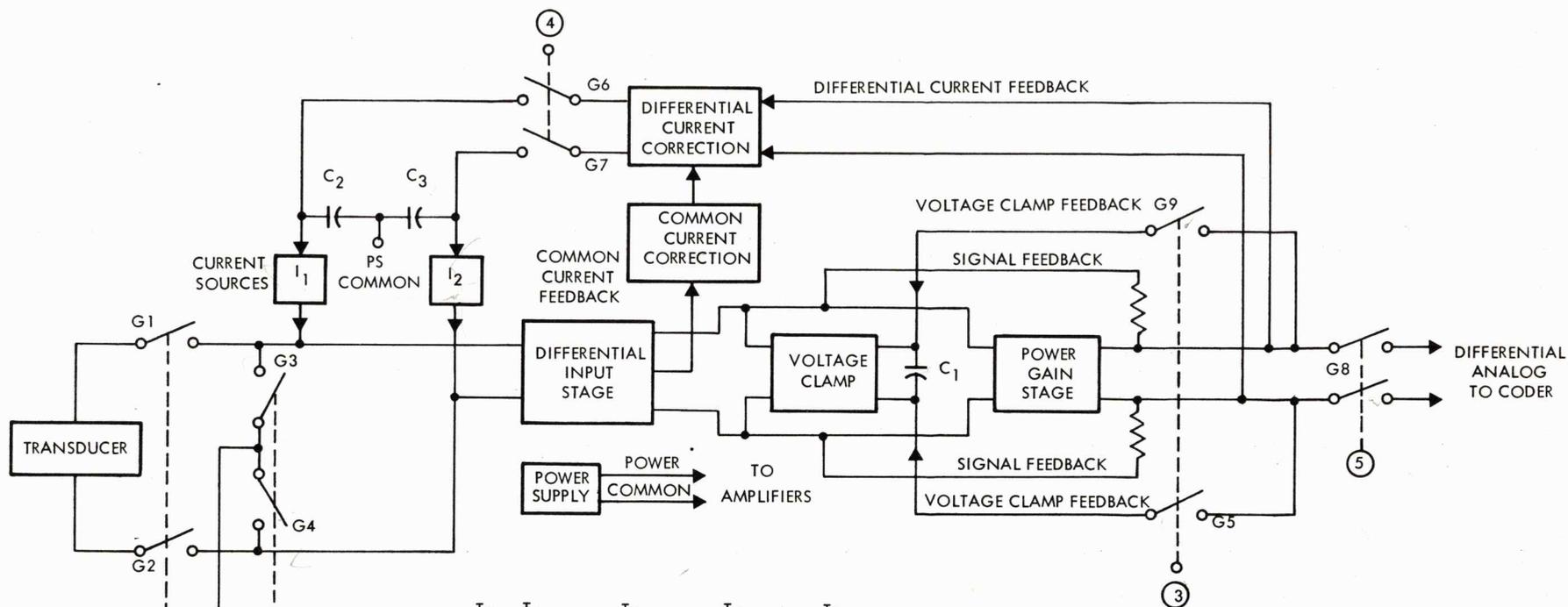
It is proposed to allocate a twenty-four bit interval for the frame sync configuration, and eight bits for the subframe identification word.

This frame and subframe sync information can be handled easily by ground stations, and provides assurance of locking on to the correct sync within three frames.

With a 24-bit word and a bit error probability of 10^{-6} , the probability of an error is approximately 24×10^{-6} if we ignore the higher order terms in the binomial expansion; the probability of even one error occurring in each of five consecutive frames is approximately 10^{-23} .

While the probability of finding false sync in the data is in the order of 10^{-4} for any one frame, the use of the complementary twenty-four bit in alternate frames renders the probability of occurrence in the data almost vanishingly small. The nature of data is such that normally only the less significant bits change from frame to frame. Consequently, the more significant bits could be changed only by erroneous transmission. If we assume that the most significant of the 24 bits could change only in the case of an error, its probability of reversing in the second frame is 10^{-6} . With the remaining twenty-three bits random, the probability of their being complements of their state in the preceding frame is 2^{-23} or approximately 10^{-7} . Consequently, the probability of complementary data occurring in successive frames is about 10^{-13} .

At higher bit error rates, the advantages of complementary frame syncs are less, but as long as there is at least one bit in a false sync which cannot change due to the nature of the data, the complementary syncs are preferable.



Slide 10

Figure D-1 Clamped Differential D.C. Amplifier

APPENDIX E-1

RELIABILITY ASSESSMENT

Details relating to the reliability assessment study are contained in this section of the Appendix to clarify the approach taken in arriving at the reliability figures.

Failure Rates

The failure rates used for these assessments are those found in Boeing Document D-590 for Minuteman high reliability components, type "B". Chart I gives a listing of the "B" level failure rates used here, (extracted from above document) and the corresponding "M" level.

The following statements were taken from this Boeing document: "B" level parts are electrically and mechanically identical to "M" level parts, but are not board mounted or serialized and are not subjected to parameter drift screening. Failure rates on the referenced "M" level standard pages apply to the "M" level part only. Since no failure rate curve for "B" level parts are presently available, the values listed below shall be used."

The "M" level failure rates are actually the Minuteman high reliability "goals". The "B" level failure rates used here are in many cases several orders of magnitude higher than that of the corresponding "M" level part.

If "M" level failure rates are realizable in a "B" level part, there will of course be either a significant increase in reliability or decrease in weight due to a reduction in spares -- or both. It should be pointed out that the use of "M" level failure rates for this assessment would be extremely optimistic, since "M" level parts are for use on Minuteman only, and therefore represent goals which it is expected the components can obtain through extensive component improvement programs.

<u>COMPONENT TYPE</u>	<u>"B" LEVEL FAILURE RATE</u>	<u>"M" LEVEL FAILURE RATE</u>
Transistor, Silicon	0.1×10^{-6}	0.01×10^{-6}
Diode, Silicon Computer	0.02×10^{-6}	0.0002×10^{-6}
Diode, Silicon Gen. Purpose	0.1×10^{-6}	0.02×10^{-6}
Diode, Silicon Reference	0.25×10^{-6}	0.02×10^{-6}
Resistor, Fixed Composition	0.005×10^{-6}	0.0009×10^{-6}
Resistor, Precision Wire Wound	0.25×10^{-6}	0.007×10^{-6}
Capacitor, Glass	0.005×10^{-6}	0.0008×10^{-6}
Capacitor, Tantalum	0.5×10^{-6}	0.05×10^{-6}
Transformer, Magnetic Logic	0.05×10^{-6}	0.01×10^{-6}

CHART I

FAILURE RATES

Module Analysis

Pertinent details related to the evaluation of each different module type are given below.

1. High-Level and Low-Level Analog Gate Modules (Type A and B)

These modules contain the analog gates and their failure sensing circuitry. For purposes of this reliability analysis, the modules have been divided into that circuitry where a failure would cause loss of more than one percent of the input channels, and that circuitry where a failure would cause loss of only a single channel. Figure 1 is a detailed failure effects analysis of the gate and its magnetic core driver. This analysis was required in order to make the division a valid one.

The failure rate of that portion of the module where failures are not allowed was then combined with the "effective" failure rate of the other portion, calculated assuming that up to one percent of the channels are allowed to fail.

2. Digital Multiplexer Gate Module (Type G)

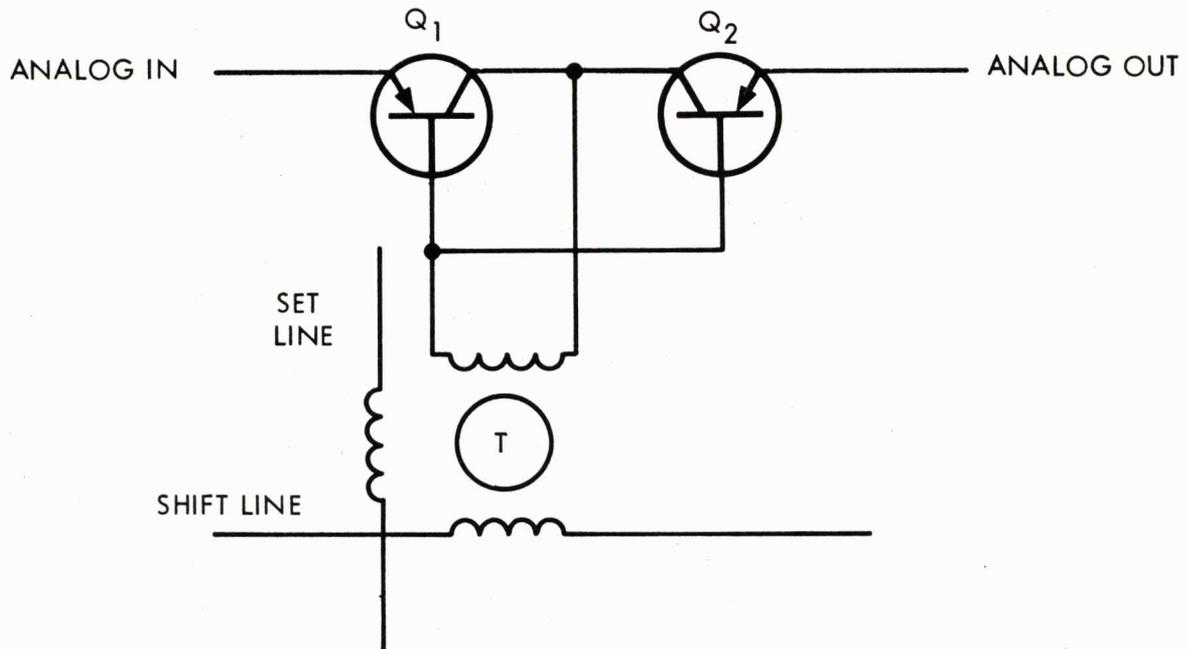
These modules contain the digital gates used to sequence the various digital groups. Again, the module was divided as explained in 1 above. Figure 2 gives the detailed failure effects analysis for this type of gate. The failure rates were calculated assuming that up to one percent of the input signals are allowed to fail.

3. Remaining Modules

The remaining modules are handled in a straight-forward manner in that any failure would cause losses in excess of the one percent allowed.

4. Connectors

The failure rate for that portion of the connector affixed to the individual module has been included with the total module failure rate. These failure rates were calculated as per Collin's instructions, i.e., 0.0007%/1000 hours for each connector with an additional 0.0001%/1000 hours assigned to each pin. This portion of the connector is of course replaced with the spare module.

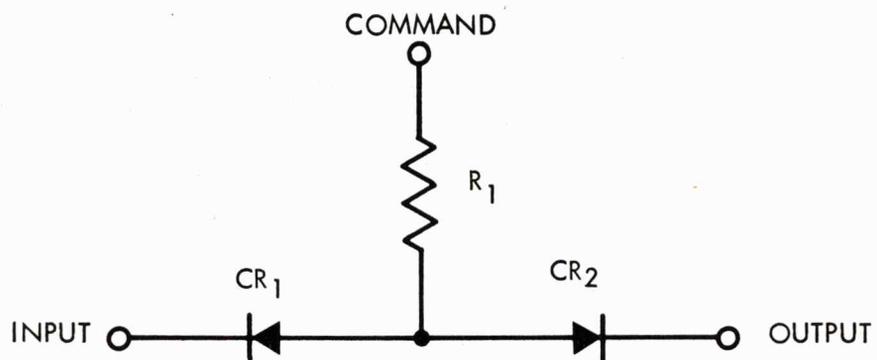


<u>FAILURE MODE</u>	<u>RESULT</u>
OPEN E, Q ₁	1 OPEN CHANNEL
Q ₂	1 OPEN CHANNEL
OPEN C, Q ₁	1 OPEN CHANNEL
Q ₂	1 OPEN CHANNEL
OPEN B, Q ₁	1 OPEN CHANNEL
Q ₂	1 OPEN CHANNEL
SHORT C-E, Q ₁	1 CHANNEL OF ANALOG INFO DEGRADED
Q ₂	SHORTED CHANNEL (MULTIPLE CHANNELS DEGRADED)
SHORT B-E, Q ₁	1 CHANNEL OF ANALOG INFO DEGRADED
Q ₂	SHORTED CHANNEL (MULTIPLE CHANNELS DEGRADED)
SHORT C-B, Q ₁	1 OPEN CHANNEL
Q ₂	1 OPEN CHANNEL
DEGRADED T	1 OPEN CHANNEL

AN OPEN IN THE "SET LINE" CAUSES LOSS OF ONE ENTIRE (VERTICAL) ROW.

AN OPEN IN THE "SHIFT LINE" CAUSES LOSS OF ONE ENTIRE (HORIZONTAL) COLUMN.

Figure E-1 Analog Gate Failure Analysis



FAILURE MODE

OPEN R₁
 OPEN CR₁
 OPEN CR₂
 SHORT CR₁
 SHORT CR₂

RESULT

LOSE ONE CHANNEL
 LOSE ONE CHANNEL
 LOSE ONE CHANNEL
 LOSE MULTIPLE CHANNELS
 LOSE MULTIPLE CHANNELS

Figure E-2 Digital Multiplexer Failure Effects Analysis

However, the other part of the connector that is a portion of the S.E.P. hardware is not replaceable. For that reason, a failure rate has been assigned to them and included in the over-all system probability of success.

APPENDIX E-2

SYS SYM NO	UNIT DWG NO	UNIT SYM NO	EXACT NO OF FAIL- URES	UPPER LIMIT OF SUMMA- TION	NO. CHAN/ PATHS/ UNITS	ST'BY REDUND FACTOR	FUNCTION SYMBOL	PROBABILITY OF SUCCESS	MISSION OPER TIME
HL	60468	OH	00	00	001	00	A	.97372851	8760.00
HL	00468	OM	00	00	012	00	B	.88561267	8760.00
HL	00068	ON	00	04	048	00	C	.99999972	8760.00
HL	00468	QM	01	00	012	00	D	.10758035	8760.00
HL	00068	ON	00	00	048	00	E	.90135279	8760.00
HL	60408	OY	00	00	001	00	F	.99332465	8760.00
HL	60408	OY	00	00	001	00	G	.99332465	8760.00
HL	01227	OP	00	00	001	00	H	.99863476	8760.00
HL	41227	OO	00	00	001	50	I	.98973525	8760.00
HL	41407	OB	00	00	001	00	J	.99949295	8760.00
HL	41406	OR	00	00	001	00	K	.99954560	8760.00
HL	51527	OC	00	00	001	00	L	.99424698	8760.00
HL	30754	OF	00	00	001	00	M	.99975385	8760.00
HL	61029	OD	00	00	001	00	N	.99214420	8760.00
HL	00009	OS	00	00	001	00	O	.99836716	8760.00
HL	60995	OG	00	00	001	00	P	.99838301	8760.00

OUTPUT
OF
PASS #3

P_{HL} MODE RELIABILITY = .92766915 8760.00

OUTPUT
OF
PASS #4

Figure 5. Computer Output Format For Passes No. 3 and No. 4

4. Control - Once the system aspects are loaded into the computer, it can be used to insure that the reliability design goals are being met by rerunning a complete prediction with each circuit release. The effects of design changes, relative to reliability, can also be measured in this manner.

5. As a Design Tool - The Design Goal Program can be used to optimize the system design configuration by "backing into" a contractual reliability figure. This assures that a minimum degree of redundancy is employed to achieve the goal.

APPENDIX F

INTERFERENCE CONTROL

Purpose

This appendix describes the interference control program which will be implemented. The probable degree of specification compliance is predicted and supporting data taken on similar systems is presented.

Clarification

Paragraphs 3.7.5.1 (2) and 3.7.5.4 (1) of document AR-104-3 define the multiple point grounding requirements for the shields of cables which conduct frequencies of 50 kc or higher. This is interpreted to include all cables intentionally conducting signals whose composition necessarily require the presence of this frequency range in amounts which might prevent interference control specification compliance.

Interference Control Program

The interference control program will consist of:

- (a) Application of proven effective circuit and cable grounding and shielding techniques.
- (b) Provide a system package, including interconnecting cable shields, which will ensure adequate system shielding.
- (c) Isolation of interference sources from the input and output circuits to the maximum practical extent consistent with the equipment detailed specification and minimum weight design.
- (d) Design and application of suitable filter and suppression components.
- (e) Evaluation testing of system components to verify or improve interference control techniques throughout development.
- (f) Provide support to the manufacturing activity to ensure the most effective attainable application of interference control on flight systems.

Grounding and Shielding Techniques

Radiation Incorporated has participated in the development and fabrication of several airborne PCM telemetry systems for missile and satellite applications. The cable and circuit grounding and shielding concept defined in Paragraphs 3.7.5 and 3.7.6 of AR-104-3 has been found to yield the maximum practical degree of interference and susceptibility control when properly applied in conjunction with the program previously outlined. Figures F-1 and F-2 demonstrate the effectiveness of these techniques in actual hardware items. Airborne telemetry system radiated interference levels are typically determined almost entirely by the input and output cable shield grounding configuration. System susceptibility to external fields will be reduced by minimizing of the induced interference levels on input, output, and interconnecting cables. In some instances, both single end and multiple point grounded cable shields may be necessary to provide susceptibility protection and adequate containment of system generated interference levels.

System Packaging

An over-all-system interference shield will be established by:

- (a) Designing RF tight module covers and connector pan assemblies.
- (b) Maintaining an adequate RF seal between module case and connector pan assembly.
- (c) Specifying an over-all multiple point grounded shield for each system interconnecting cable.
- (d) Ensuring that at least one pin of each System SEP Unit connector is maintained at chassis RF ground through minimum impedance. Only multiple point grounded interconnecting cable shields will be connected to chassis ground on this pin. Single point grounded cable shields will require a separate ground pin.

Internal Interference Source Isolation

System interference sources will be grouped together and separated physically from input and output cables as much as the flexibility of the system design allows. An effort will be made to insert relatively low interference level circuitry in the input and output cable connection areas in order to take maximum advantage of conducted noise decrement within the system.

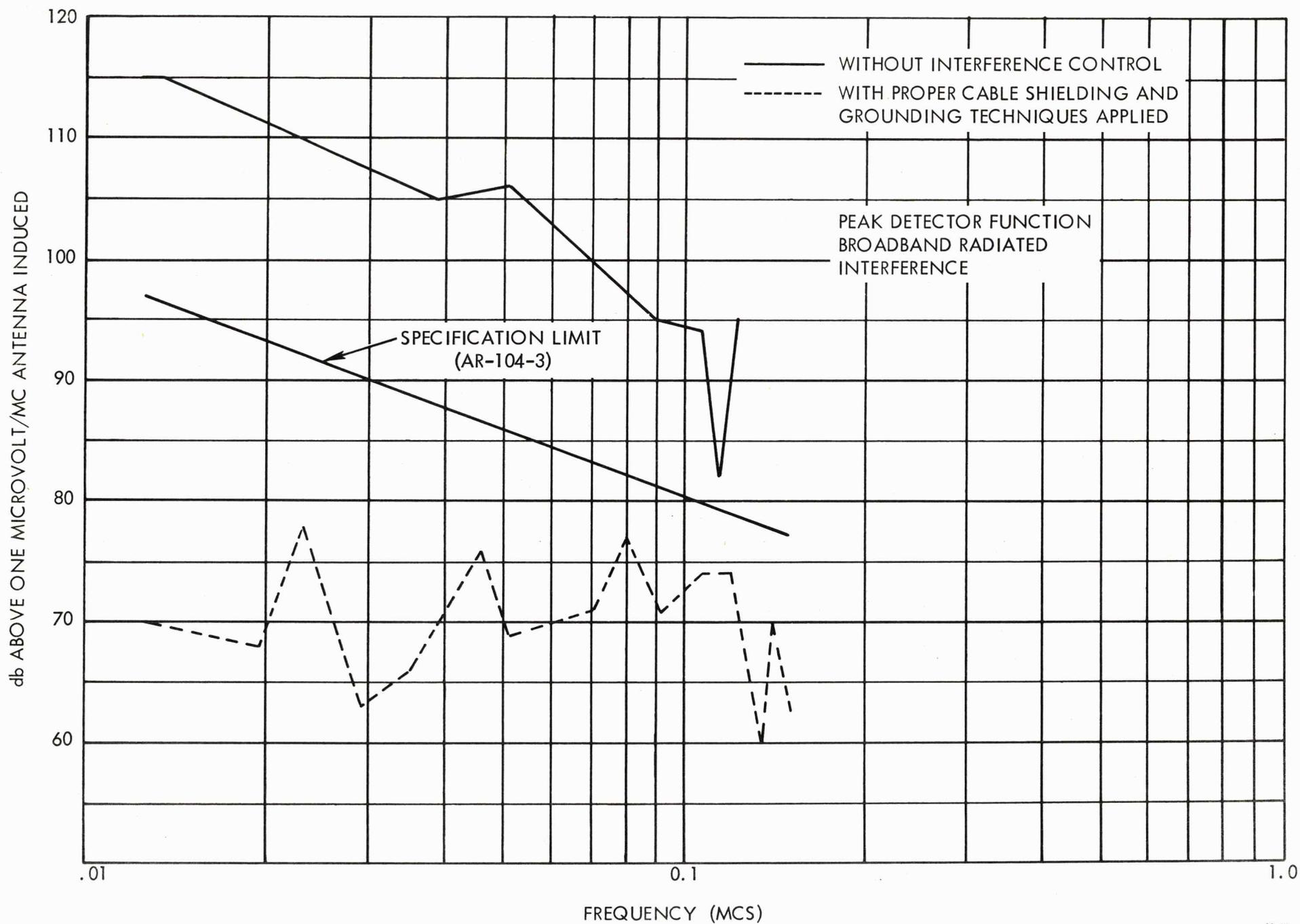


Figure F-1 Broadband Radiated Interference

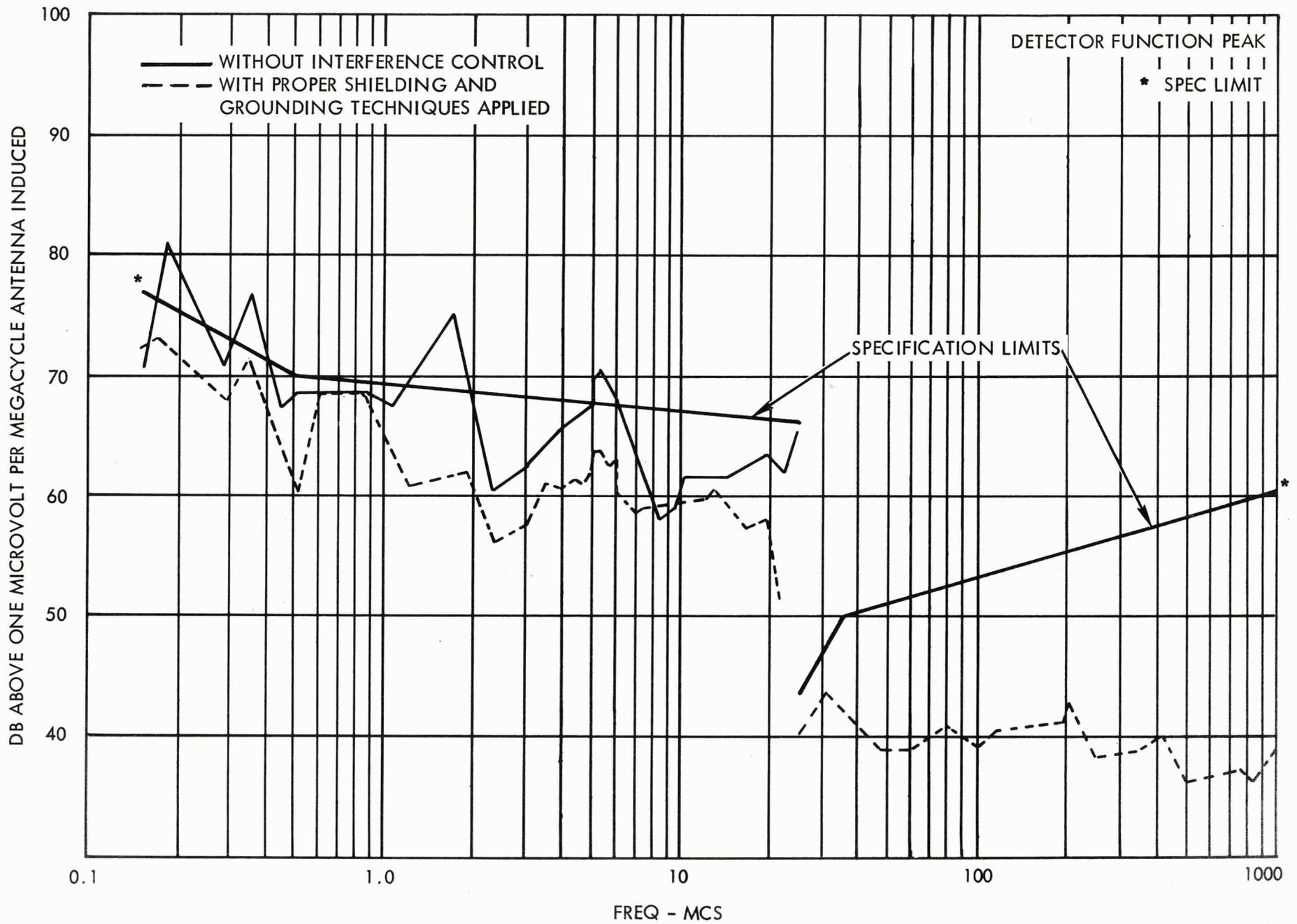


Figure F-2 Broadband Radiated Interference

Filters and Suppression Components

Primary power line filters will be used. Filtering within the system will be considered only after all other techniques have been determined to be inadequate.

Evaluation Testing

Interference control design will be evaluated during the system development program through component level measurements. Figure F-1 and F-2 illustrate the effectiveness of this technique.

Interference Tests

Applicable Tests

The following tests will be performed on one pre-production system in accordance with Table 3-4 of AR-104-3:

- (a) Interference conducted on primary power input lines (Test A.1).
- (b) Interference conducted on signal and command interface lines (Test A.2). A representative sampling of the system inputs will be measured.
- (c) Interference generated within and radiated from the system will be measured (Test B.1).
- (d) System susceptibility to RF energy conducted on the primary power input lines will be measured (Test D.1).
- (e) System susceptibility to radiated RF fields will be determined (Test D.4).
- (f) System susceptibility to 400 cps fields will be measured (Tests D.7 and D.8).

Non-Applicable Tests

The following tests described in Table 3-4 of AR-104-3 will not be performed:

- (a) Antenna conducted RF interference (Tests C.1, C.2, and C.3) apply only to receiving and transmitting systems.

- (b) System susceptibility to audio-frequency energy conducted on primary power lines (Test D.2) applies only to systems having dc primary power input.
- (c) System susceptibility to transients (Test D.3) applies only to systems employing dc primary power input.
- (d) Intermodulation and front-end rejection measurements (Tests D.5 and D.6) apply only to receiving equipment.

Specification Compliance

Analysis of data recorded during measurements of similar airborne PCM telemetry systems indicates that compliance with the interference control requirements specified in document AR-104-3 can be achieved. Restricting the use of multiple point cable shield grounding to circuits conducting frequencies of 50 kc and higher may result in excessive radiated interference levels in the 15-20 kc frequency range. Should these levels exceed the appropriate allowable limits, and also constitute a flight operation problem, a deviation in cable shield grounding may be necessary.

Apparent interference levels resulting from measurement of the requisite RF content of the intentional digital waveform conducted on system interface leads will not be considered as failure to meet interference control requirements.

Representative interference levels are illustrated in Figures F-1, F-2 and F-3.

SYSTEM RELIABILITY ANALYSIS AND PREDICTION THROUGH THE APPLICATION OF A DIGITAL COMPUTER

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Summary

This paper describes how the reliability prediction processes used to estimate the survival life of equipment designs was automated on a digital computer. The method employed and the advantages and results of its application to a satellite telemetry system are discussed.

Introduction

The satellite era has compressed development and delivery schedules, generally reduced the number of total production units required, and increased the stringency of reliability specifications. The program development cycle generally allows a minimum amount of time and number of equipments for operational, environmental, and reliability testing. The testing and ensuing small production run is often completed prior to accumulating a sufficient amount of equipment operating experience to insure complete "debugging" of the design.

To compensate for the lack of equipment operating experience the reliability engineer must rely more heavily on mathematical reliability predictions. Starting with the conceptual design phase and continuing throughout the design cycle, frequent reliability assessments of the design must be made. These assessments are instrumental in:

1. Optimizing the system design relative to reliability trade-offs.
2. Guiding initial system design to insure that the contract reliability specification can be met.
3. Monitoring the circuit designs to be sure the reliability budget is being adhered to.
4. Gaining confidence that the reliability demonstration tests and/or the operational reliability performance will be met.
5. Minimizing the equipment "debugging" time because of part misapplication.

Because of the long-life expectancy of satellite equipments, redundancy, at the component part, circuit, and unit levels, is commonly employed. This, and other methods of increasing the equipment reliability, greatly increases the mathematical complexity of a reliability estimate. The repetitive nature and quantity of part level calculations, as well as the complexity of the circuit and unit formulas, lend themselves to digital computer application.

Scope of the Computer Program

When a customer invokes a reliability program, there are normally two (2) major contractual milestones associated with the mathematical reliability prediction process.* These milestones are:

1. Establishment of Reliability Design Goals
2. Equipment Reliability Predictions (Preliminary Interim, and Final)

The mathematical techniques used to accomplish the two tasks are identical. However, the inputs and outputs are different because of the point in the design schedule in which they occur. Consequently the program established, on the computer, was developed to satisfy the requirements of both tasks. The following paragraphs give a brief explanation of the inputs and outputs of the computer program when applied to the Design Goal and Reliability Prediction tasks.

Establishment of Equipment Design Goals

Early in the conceptual system-design phase or, in some instances, during the contract proposal phase, the computer program is employed to guide the system designers to insure that the contractual reliability specifications will be achieved. The inputs to the computer are:

1. Various possible system design configurations.
2. Various reliability trade-offs to test, such as part, circuit, or unit-level redundancy, allowable losses, etc.
3. A tentative listing of component parts employed in each design configuration.
4. A range of component thermal stresses.
5. A range of mission or operating time periods to be assessed.
6. A range of the component electrical stress ratios (Derating).

* To limit the length of this paper, no attempt is made to present the underlying philosophies or the processes involved with reliability predictions. For detailed information refer to ASTIA Document AD-148556

The computer estimates and prints out a reliability figure of merit for each system configuration under the various conditions of stress (electrical and thermal), failure conditions, and operating time periods. An analysis of the program results will establish which system design configuration yields the greatest reliability and what type and level of reliability trade-offs are necessary to attain the reliability specifications. When the system configuration is established, the computer outputs provide a firm basis for the component part derating philosophy that must be imposed on the circuit designers and automatically establishes the circuit, unit, and system-level reliability goals.

Reliability Predictions

Concurrent with circuit design, the program is used to construct frequent reliability predictions to determine if the reliability goals are being met. Because of the speed and low cost of running a prediction, it is feasible to make a complete system prediction as each new circuit is released, or an engineering change is made. The effects of component part changes and circuit complexity are quickly assessed relative to their effects on the system reliability goals.

The computer program used to establish the design goals is employed for reliability predictions. The difference rests with the input data. Whereas the inputs to the Design Goal were a range of parameters to assess, the Reliability Prediction has only one set of parameters to contend with. The inputs to the Reliability Prediction Program are:

1. Specific component part application data.
2. Component part ambient operating temperatures.
3. System and unit configuration data.
4. Mission or operating time period.

The output of this program is a reliability prediction documented by the computer on pre-established forms, ready for reproduction and distribution.

Generalized Computer Process

The program was developed to be as flexible as possible. This was accomplished by treating the various formulas and procedures used to estimate component part, unit, and system probabilities as basic sub-routines. In addition, the over-all prediction was programmed such that four (4) progressive steps, or passes are required on the computer. This flexibility permits using small portions of the program individually. Figure 1 shows a generalized block flow-diagram of the Design Goal and Reliability Prediction Program.

Following is a brief description of the functions performed by each pass of the computer:

1. Pass Number 1 - A basic failure rate is selected from the stored empirical failure-rate data for each component part, based upon the component electrical stress and environmental stress. The selected component part failure rate is then modified, if required, for circuit application.

2. Pass Number 2 - The failure-rate for the next higher assembly (unit) is arrived at by summing the component part failure rates. The probability of successful operation for any specified operating time period, under the condition of no allowable failures, is computed based on the exponential probability distribution.

3. Pass Number 3 - The unit probability is computed under any specified definition of success.

4. Pass Number 4 - The unit probabilities are combined which yields the system, or modal reliability in terms of the probability of successful operation.

Application of the Program

An example is given to present the over-all computer program capabilities and the processes associated with its application. The example is a satellite PCM telemetry system. However, only the computer inputs-outputs required to display the programs capability are given.

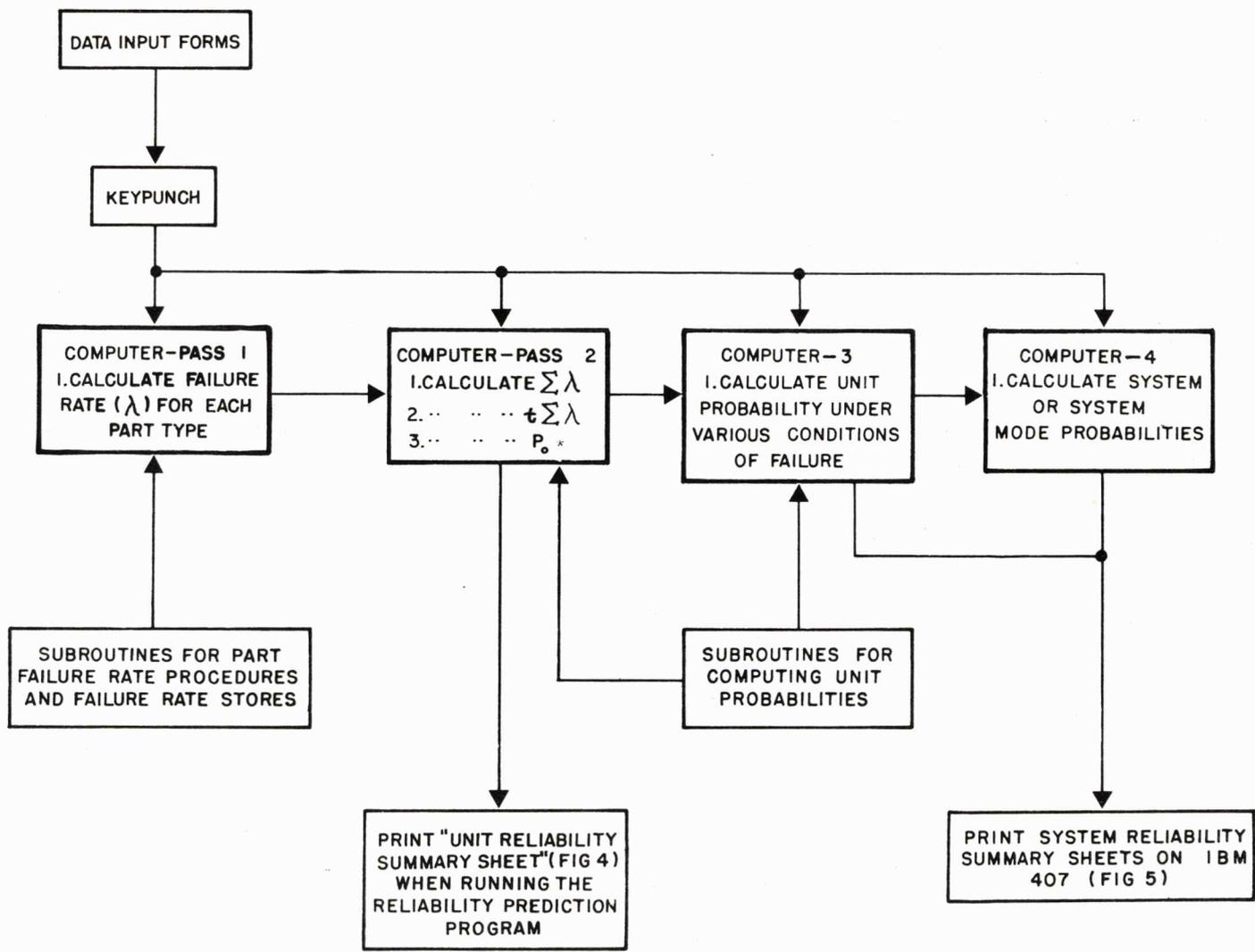
Since the Design Goal Evaluation is basically a repetitious Reliability Prediction, the example demonstrates the application of the computer to perform a Reliability Prediction. However, when there are differences in the application of a program to the two different tasks, they will be brought out in the presentation.

Data Preparation

The program data inputs necessary to enable the computer to perform a Reliability Prediction, or to establish Reliability Design Goals, are provided to the machine via three standard input data forms. The sequential steps that are followed to prepare the data forms are briefly discussed in the following paragraphs:

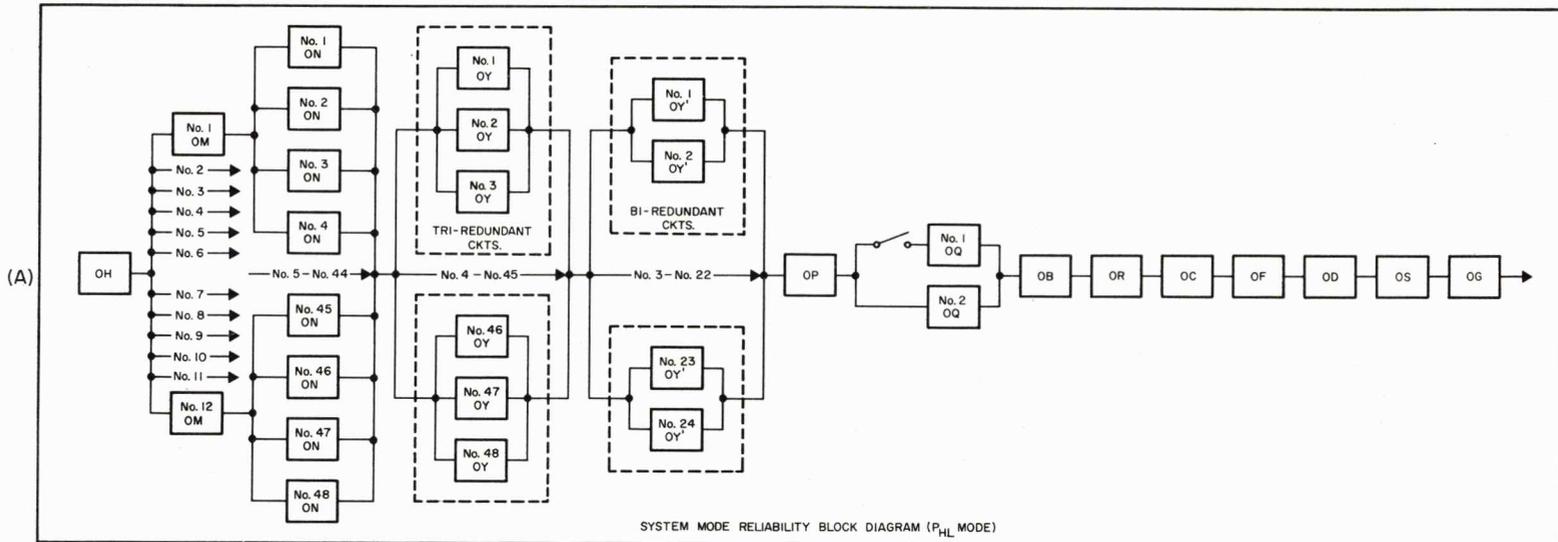
Step 1 - A reliability block diagram is prepared from the functional schematic or logic diagram indicating the functional reliability arrangement of the system components such as series, parallel, standby, etc. Figure 2A shows the reliability block diagram for the example system. Each block of the diagram, hereafter referred to as a "unit", is assigned a two-letter code for identity.

Step 2 - Determine the system and unit reliability trade-offs that are allowable under the contract or system design. The trade-offs will depend, to a great extent, on the type of program being run, i.e., Design Goal or Reliability Prediction. For the Design Goal evaluation various trade-offs could be rather arbitrarily assumed, such as allowable failures and redundancy, to assess different



P₀ IS THE PROBABILITY OF NO FAILURES OCCURRING

Figure 1. Generalized Computer Processes



(B) SYSTEM MODE PROBABILITY EQUATION (P_{HL} MODE)

$$P_{HL} = (e^{-\lambda_{OH}}) \left[(e^{-12\lambda_{OM}}) \left(\sum_{r=0}^4 \frac{(48\lambda_{OM})^r (e^{-48\lambda_{OM}})}{r!} \right) \right] + [12\lambda_{OM} (e^{-12\lambda_{OM}}) (e^{-44\lambda_{OM}})] [1 - (1 - e^{-\lambda_{OY}})^3]^{48} [1 - (1 - e^{-\lambda_{OY}})^2]^{24} (e^{-\lambda_{OP}}) (e^{-\lambda_{OB}}) \left(1 + \frac{1}{K} - \frac{1}{K} e^{-K\lambda_{OQ}} \right) (e^{-\lambda_{OR}}) (e^{-\lambda_{OC}}) (e^{-\lambda_{OF}}) (e^{-\lambda_{OD}}) (e^{-\lambda_{OS}}) (e^{-\lambda_{OG}})$$

(C) COMPUTER INPUT DATA No. 1 (P_{HL} MODE)

IBM COLUMNS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
UNIT MATHEMATICAL FORMULA (NOTE)	UNIT DRAWING NUMBER	UNIT SYMBOL NUMBER	SYSTEM SYMBOL NUMBER	EXACT NO. OF FAILURES	NO. OF CHANNELS	NO. OF PATHS	NO. OF UNITS	NO. OF CHANNELS	NO. OF PATHS	NO. OF UNITS	NO. OF CHANNELS	NO. OF PATHS	NO. OF UNITS	NO. OF CHANNELS	NO. OF PATHS	NO. OF UNITS	NO. OF CHANNELS	NO. OF PATHS	NO. OF UNITS
$e^{-\lambda_{OH}}$	S	C	4	6	5	2	H	L	C	C	C	C	C	0	1	0	0	0	A
$e^{-12\lambda_{OM}}$	C	C	4	6	5	2	H	L	C	C	C	C	C	0	1	2	0	0	B
$\sum_{r=0}^4 \frac{(48\lambda_{OM})^r (e^{-48\lambda_{OM}})}{r!}$	C	C	5	6	5	2	H	L	O	C	C	C	C	4	0	A	0	C	C
$(1 - (1 - e^{-\lambda_{OY}})^3)^{48}$	C	C	4	6	5	2	H	L	O	1	0	C	C	1	2	C	C	C	C
$(e^{-44\lambda_{OM}})$	C	C	5	6	5	2	H	L	C	C	C	C	C	4	4	0	0	E	
$e^{-\lambda_{OP}}$	6	C	4	C	6	5	2	H	L	O	0	0	C	C	C	1	C	C	F
$e^{-\lambda_{OB}}$	6	C	4	C	6	5	2	H	L	O	0	0	C	C	C	1	C	C	F
$e^{-\lambda_{OC}}$	0	1	2	2	7	5	2	H	L	O	0	0	C	C	C	1	C	C	H
$(1 + \frac{1}{K} - \frac{1}{K} e^{-K\lambda_{OQ}})$	4	1	2	2	7	5	2	H	L	C	C	C	C	0	0	0	0	I	
$e^{-\lambda_{OR}}$	4	1	4	2	7	5	2	H	L	C	C	C	C	1	C	1	C	C	J
$e^{-\lambda_{OD}}$	4	1	4	2	7	5	2	H	L	C	C	C	C	1	C	1	C	C	K
$e^{-\lambda_{OS}}$	E	1	2	2	7	5	2	H	L	C	C	C	C	1	0	0	0	L	
$e^{-\lambda_{OG}}$	B	2	2	2	7	5	2	H	L	O	0	C	C	C	1	0	0	M	
$e^{-\lambda_{OH}}$	E	1	2	2	7	5	2	H	L	C	C	C	C	1	0	0	0	N	
$e^{-\lambda_{OH}}$	0	0	0	2	5	2	H	L	C	C	C	C	C	0	0	0	0	O	
$e^{-\lambda_{OH}}$	B	2	2	0	5	2	H	L	O	0	0	C	C	0	0	0	0	P	

(D) COMPUTER INPUT DATA No. 2 (P_{HL} MODE)

$$P_{HL} = A * ((B * C) + (D * E)) * ((1 - (1 - F) ** 3) ** 48) * ((1 - (1 - G) ** 2) ** 24) * H * I * J * K * L * M * N * O * P$$

*The "pieces" of the system formula (Figure 2B) entered on the form of Figure 2C for units OY ("Function Symbols" F and G) do not correspond with the system formula in Figure 2B. Pass #3 of the computer which utilizes the form data (Fig. 2C) is not programmed to perform arithmetic operations. Therefore, only the portion of the formula, of the form $(e^{-\lambda t})$ is calculated in pass #3. The remaining computations, i.e., $[1 - (1 - e^{-\lambda t})^3]^Y$, are done in pass #4. The symbolic system formula at the type in Fig. 2B must take this into account.

Figure 2.

CONDITIONS OF MODE SUCCESS

UNIT*	QTY	CONDITIONS	PROBABILITY FORMULA
OH	1	NO FAILURES PERMITTED.	$e^{-\lambda_{OH}t}$
OM	12	1. ALL OM UNITS MUST WORK AND UP TO 4 ON UNITS MAY FAIL.	$\left[\frac{(e^{-12\lambda_{OM}t}) \sum_{r=0}^4 \frac{(48\lambda_{ON}t)^r (e^{-48\lambda_{ON}t})}{r!}}{[12\lambda_{OM}t (e^{-12\lambda_{OM}t})]} \right]$
ON	48	2. 44 OF 44 ON UNITS MUST WORK AND EXACTLY 1 OM UNIT MAY FAIL.	
OY	48	ALL 48 "PATHS" MUST OPERATE.	$[1 - (1 - e^{-\lambda_{OY}t})^3]^{48}$
OY ¹	24	ALL 24 "PATHS" MUST OPERATE.	$[1 - (1 - e^{-\lambda_{OY}t})^2]^{24}$
OQ	2	STANDBY REDUNDANCY. LOSS OF 1 UNIT PERMITTED.	$(e^{-\lambda_{OQ}t}) \left(1 + \frac{1}{K} - \frac{1}{K} e^{-K\lambda_{OQ}t}\right)$
OP	1	NO FAILURES PERMITTED.	$e^{-\lambda_{OP}t}$
OB	1	NO FAILURES PERMITTED.	$e^{-\lambda_{OB}t}$
OR	1	NO FAILURES PERMITTED.	$e^{-\lambda_{OR}t}$
OC	1	NO FAILURES PERMITTED.	$e^{-\lambda_{OC}t}$
OF	1	NO FAILURES PERMITTED.	$e^{-\lambda_{OF}t}$
OD	1	NO FAILURES PERMITTED.	$e^{-\lambda_{OD}t}$
OS	1	NO FAILURES PERMITTED.	$e^{-\lambda_{OS}t}$
OG	1	NO FAILURES PERMITTED.	$e^{-\lambda_{OG}t}$

* THE UNIT SYMBOLS SHOWN IN THE TABLE CORRESPOND WITH THOSE IN THE RELIABILITY BLOCK DIAGRAM OF FIGURE 2A.

Table 1

reliability approaches. This would assist in determining the least cost to achieve the contractual reliability specifications. When performing a Reliability Prediction, however, the trade-offs are frequently predetermined by agreement with the customer and the system design is fixed.

Table 1 presents the conditions of success related to the example system. The conditions of success are subsequently entered on the form shown in Figure 2C. This data on the form defines the variables and limits associated with the general probability equations available in the computer sub-routines and also informs the computer as to which sub-routine to employ.

Step 3 - Write the over-all probability equation for the system which corresponds to the reliability block diagram and the established conditions of success such as that shown in Figure 2B. The probability equation must be converted into a symbolic form compatible with the computer language. Each "piece" of the formula was assigned a "Function Symbol" on the computer input form shown in Figure 2C (column 19 on the form) which is used to write the symbolic form shown in Figure 2D. This formula is then entered on another computer input form suitable for keypunching.

Steps 1 through 3, which culminated in the filling out of two computer input forms, completes the system design considerations and all that remains is to define the contents of each system unit, in terms of component parts, for the computer. Step 4 below discusses the unit-level aspects.

Step 4 - A tentative components parts list is obtained when running the Design Goal or Preliminary Reliability Prediction, or a final parts lists when employing the Final Reliability Prediction Program. The third, and final, computer input form is then completed which informs the computer of the following:

1. Quantity and type of parts contained in each system unit.
2. Application data for each part employed.
3. Method of computing the basic failure rate.

The unit selected as the example on the input form shown in Figure 3 is unit OH of the reliability block diagram. This unit consists of:

Four	Silicon Transistors
Four	Silicon Diodes
Eight	Deposited Film Resistors
Sixty	Shift-Register Windings
Four	AND Gates in a Quad Circuit Configuration
Four	Transistor Switches in a Quad Circuit Configuration
One	Fixed Carbon Composition Resistor in a Parallel Redundant Configuration

No attempt is made to give details on completing the input form, which is coded, as it is not necessary to the understanding of the program capabilities.

The system, or each operational mode, being assessed has been defined for the computer on the three (3) computer input forms⁴ shown in Figures 2B, 2C, and 3. These data are key punched onto standard 80-column EAM cards and subsequently presented to the computer for processing. The following paragraphs present in more detail the computations performed by each sequential step, or pass, of the computer to arrive at a reliability prediction for the example problem.

Detailed Calculation Processes

Pass Number 1

The inputs to pass 1 are the data obtained from the unit level form (Figure 3). Available in the machine are component part sub-routines which contains instructions for selecting a part failure rate. Table 2 gives a listing of the component part types for which a sub-routine** has been written.

Because of the great variety of available component part types and vendors, each part is categorized by its MIL Specification or closest applicable MIL Specification. In the event that a special or peculiar part is used in a design for which no empirical failure-rate data is available in the machine, sub-routine 26 (Table 1) is used. When this routine is employed it merely picks up a tentative failure rate established by the vendor, placed in columns 76-80 of the unit input form.

When parts, or circuits, are employed in a quaded, series, or parallel redundancy scheme, such as the example unit (OH) which has a quaded AND circuit, quaded switch, and a resistor with parallel redundancy, the configuration is taken into account and the computer modifies the basic failure rate accordingly. The unit input form specifies which calculation configuration (column 23 of the form in Figure 3) is to be employed. The calculation configuration sub-routines available are shown in Table 3.

The net result of pass 1 is to arrive at a basic failure rate, modified in some instances, for each component part type used in each system unit.

** Identical to the manual process given in ASTIA Document AD-148556.

PART TYPES FOR WHICH SUB-ROUTINES ARE AVAILABLE IN PASS I

COMPUTER SUB-ROUTINE NO.	PART TYPE AND CLASS	SPECIFICATION REFERENCE		
		NUMBER	STYLE	CHARACTERISTIC
1 2	Semi-Conductors:			
	Silicon Diodes Silicon Transistors	MIL-S-19500 MIL-S-19500	-- --	----- -----
3 4 5 6 7	Resistors:			
	Fixed Carbon Composition	MIL-R-11-B	RC	GF
	Fixed Accurate Deposited	MIL-R-10509C	RN	A, B
	Fixed Accurate Deposited Film	MIL-R-10509C	RN	C
	Fixed Accurate Wire Wound Variable Accurate Wire Wound	MIL-R-93A MIL-R-19	RB RA	----- -----
8 9 10 11 12 13 14 15	Capacitors:			
	Fixed Paper	MIL-C-25A	GP	A, B, D, E, F
	Fixed Paper	MIL-C-25A	CP	K
	Fixed Paper	MIL-C-26244	CPV	-----
	Fixed Paper	MIL-C-14157	CPM	K
	Fixed Ceramic, Temp. Comp.	MIL-C-20B	CC	-----
	Fixed Ceramic, Gen. Pur.	MIL-C-11015A	CK	-----
	Fixed Tantalum, Electrolytic Fixed Tantalum, Solid	MIL-C-3965B MIL-C-26655A	CL --	----- -----
16	Transformers	MIL-T-27A	TF	-----
17	Magnetic Amplifiers	MIL-T-27A	--	-----
18	Inductors (Power)	MIL-T-27A	TF	-----
19	Inductors (R.F. & I.F.)	MIL-C-15305	LT	-----
20	Transformers (R.F. & I.F.)	MIL-C-15305A	LT	-----
21	Connectors	-----	--	-----
22 23	Relays:			
	Sensitive Type General Purpose	MIL-R-5757C MIL-R-5757C	RY RY	----- -----
24 25	Switches:			
	Large Sensitive Small Sensitive	JAN-S-63 MIL-S-6743	SS --	----- -----
26	Special Part	N/A	--	-----
27	Quad Circuit	N/A	--	-----

Table 2

Pass Number 2

The output of pass 1 constitutes the input for pass 2. The computer solves the following probability equation for each system unit:

$$P_o = e^{-\sum N \lambda_{\text{eff}} t}$$

where:

P_o = Probability of no unit failures

N = Number of each type of component part used in the unit

λ_{eff} = Failure rate of each type of component part used in the unit

t = Operate or Mission Time

When running a Reliability Prediction Program, the output cards from passes Number 1 and 2 are typed out by an IBM tabulating machine on a reproducible master. This master is reproduced on the standard form shown in Figure 4. The data contained in the body of the form was calculated during the first computer pass. The unit failure rate totals and the probability of no failures (P_o) was calculated during the second computer pass.

Pass Number 3

The output of pass 2 and the unit "conditions of success", provided to the computer by the form shown in Figure 2C, constitutes the input to pass 3. The computer will select the applicable probability equation from one of the following sub-routines, which are based on the Poisson Exponential probability distribution, to arrive at the unit probability figure.

1. Employed when a specific number of unit failures are permitted

$$P(r, a) = \frac{a^r e^{-a}}{r!}$$

where:

$P(r, a)$ = The probability of exactly "r" events occurring when the expected number of events is "a".

r = Number of failures permitted

a = $n (\sum N \lambda_{\text{eff}} t)$

n = Number of identical units

$(\sum N \lambda_{\text{eff}} t)$ = Output of pass 2

2. Employed when up to "c" specified number of unit failures are permitted

$$S(r, a) = \sum_{r=0}^{r=c} P(r, a)$$

where:

$S(r, a)$ = Arithmetic summation of the probabilities of exactly "r" events, from $r=0$ to $r=c$.

3. Employed when standby unit redundancy is used

$$P = (e^{-a}) \left(1 + \frac{1}{K} - \frac{1}{K} e^{-Ka} \right)$$

where:

$$K = \frac{\lambda_1}{\lambda}$$

λ_1 = Standby unit failure rate

λ = Operating unit failure (output of pass 2)

Pass Number 4

The unit probabilities from pass 3 and the system probability formula, which was given to the computer via the form shown in Figure 2D, are presented to the computer for the fourth and final pass. The system probability formula instructs the computer on how to combine the unit probabilities to arrive at the over-all system reliability.

The output cards of passes 3 and 4 are printed out on a tabulator in the format shown in Figure 5. The body of the report is provided by pass 3 which are the unit probabilities under the specified conditions of success. The bottom figure (in the box) is the over-all system probability provided by pass 4. The output figures are for the example system.

To assess the effects of the various stresses and operate times, the Design Goal Program is repeatedly run, each time with a different set of parameters. Each time the computer is cycled through its four (4) passes the output of passes Number 3 and 4 are printed out as shown in Figure 5. This gives the probability of each unit relative to its system application and conditions, and the over-all probability of each system mode over the ranges of operate time and electrical and thermal stresses specified. Numerous system block configurations may be assessed also to determine the optimum configuration, reliability-wise.

Advantages of the Automated Program

The major advantages of automating the reliability process are reviewed below.

1. Consistency - The prediction is always done in the same manner and sequence.
2. Accuracy - Human errors, unavoidable when hundreds of manual calculations are made, are eliminated.
3. Cost - Excluding the initial programming, the cost for a prediction is less. Less engineers hours are required and the documentation is provided by the computer requiring much less typing hours for a formal customer report.

CALCULATION CONFIGURATION (PART LEVEL)

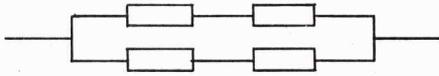
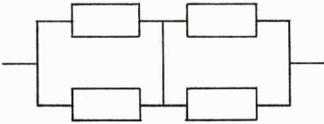
CONFIGURATION METHOD NUMBER	APPLICATION AND FORMULII
Configuration "0"	No change
Configuration 1	<p>For a quad. without center line, used when a part short is the most probable mode of failure:</p>  $\lambda_{\text{eff}} = \frac{-\text{Ln} \left[1 - \frac{2(N^2 + 2)(1 - e^{-\lambda t})^2}{(N + 1)^2} + \frac{4(1 - e^{-\lambda t})^3}{(N + 1)^3} + \frac{(N^3 - N^2 + N - 1)(1 - e^{-\lambda t})^4}{(N + 1)^3} \right]}{t}$ <p>where</p> $N = \frac{Q_s}{Q_o} = \text{FAILURE PROBABILITY RATIO} \quad Q_s = \text{Probability of short}$ $Q_o = \text{Probability of open}$ <p>t = operate time</p>
Configuration 2	<p>For a quad <u>with</u> a center line, used when a part open is the most probable mode of failure:</p>  $\lambda_{\text{eff}} = \frac{-\text{Ln} \left[1 - \frac{2(2N^2 + 1)(1 - e^{-\lambda t})^2}{(N + 1)^2} + \frac{4N^3(1 - e^{-\lambda t})^3}{(N + 1)^3} - \frac{(N^3 - N^2 + N - 1)(1 - e^{-\lambda t})^4}{(N + 1)^3} \right]}{t}$
Configuration 3	<p>For Series Redundancy - Used when the part probability of short is greater than the probability of open.</p>  <p>when $N \leq 99.99$ use the formula below (99.99 is limit of computer space)</p> $\lambda_{\text{eff}} = \frac{-\text{Ln} \left[(e^{-\lambda t})^2 + 2 \left(\frac{N}{N + 1} \right) (1 - e^{-\lambda t}) (e^{-\lambda t}) \right]}{t}$ <p>when N is > 99.99 use</p> $\lambda_{\text{eff}} = \frac{-\text{Ln} \left[2 e^{-\lambda t} - (e^{-\lambda t})^2 \right]}{t}$ <p>(case when $N \rightarrow \infty$)</p>
Configuration 4	<p>For n number of components in parallel when up to one is allowed to fail. Used when the part probability of open is greater than short.</p> $\lambda_{\text{eff}} = \frac{-\text{Ln} \left[n (e^{-\lambda t})^{(n-1)} - (n-1)(e^{-\lambda t})^n \right]}{t}$

Table 3

UNIT RELIABILITY SUMMARY SHEET

EQUIPMENT XXXXXXXXXXXX OPERATE TIME (HRS) 8760.00 DATE 6/29/62
 UNIT NAME XXXXXXXXXXXX UNIT DWG. NO. XXX UNIT SYM. NO. OH
 USED IN SYSTEM MODE (S) H L

	COMPONENT PART TYPE AND CLASS	CONFIG- URATION	NO. OF PARTS		E (%)	T (°C)	λ_{eff}	N X λ_{eff}		
				PART SYM. NO.						
OUTPUT OF PASS #1	DIODE, SILICON		4		10	60	.15000000 -06	.60000000 -06		
	TRANSISTOR, SILICON		4		10	60	.31000000 -06	.12400000 -05		
	RES., F.A.		8		10	60	.20000000 -07	.16000000 -06		
	SHIFT REG. WDGS.		60		10	60	.17000000 -07	.10200000 -05		
	"AND" GATES	QUD 1	4		10	60	.29513235 -09	.11805294 -08		
	TRANSISTOR SW. CKT.	QUD 1	2		10	60	.89647116 -08	.17929423 -07		
	RES., F.C.	PRED	1		10	60	.21020000 -10	.21020000 -10		
OUTPUT OF PASS #2			$\sum N X \lambda_{eff}$				$\sum N X \lambda_{eff} X t = a$		$P_0 = e^{-a}$	
			.30391309 -05				.26622786 -01		.9737285	

Figure 4. Computer Output Format For Passes No. 1 and No. 2

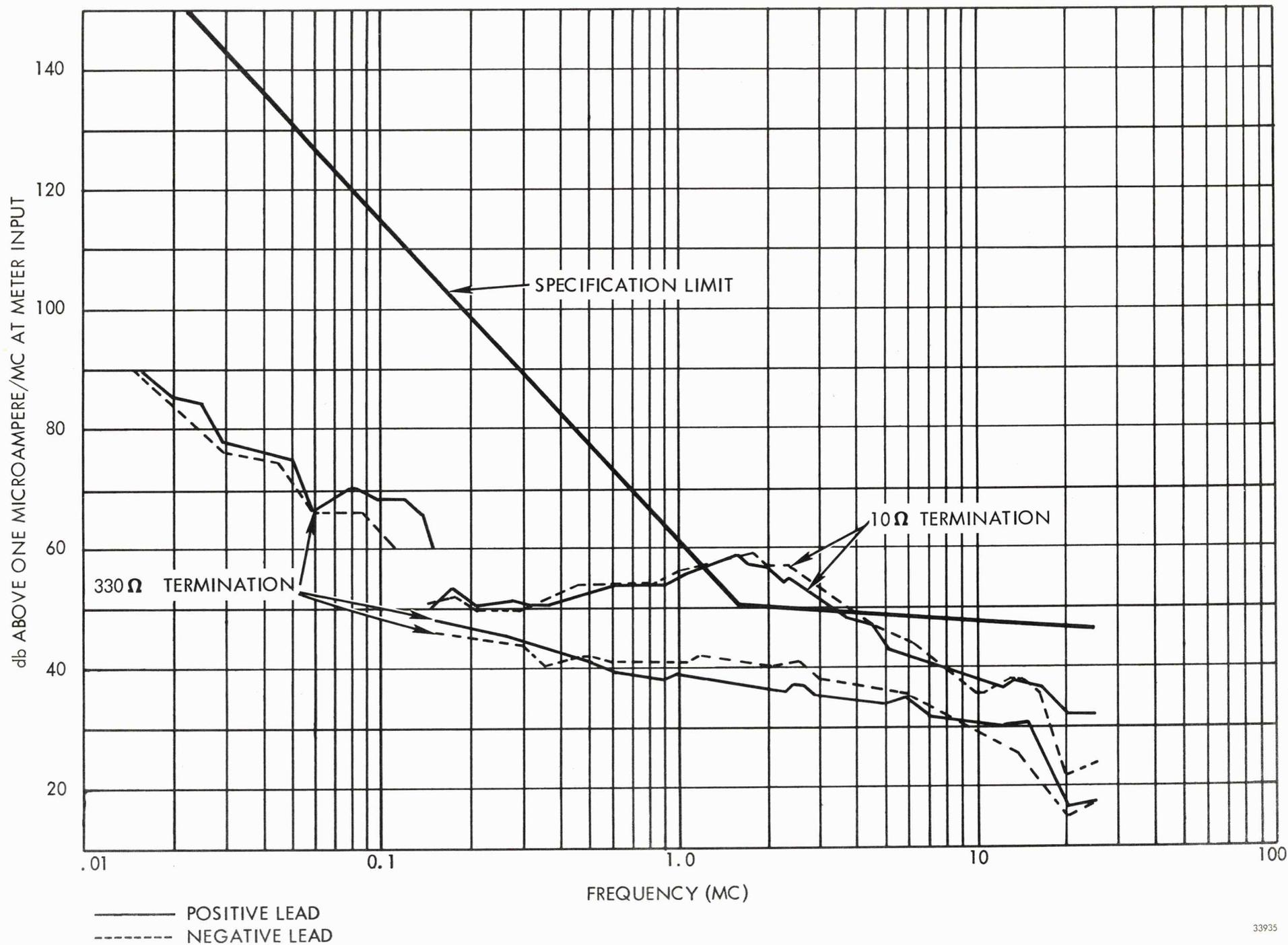


Figure F-3 Broadband and Pulsed Interference

APPENDIX G

PACKAGING ALTERNATE

The approach to be presented here is a result of an intensive effort to provide greater advantages to the Apollo program in the areas of reliability, weight, maintainability, and size. This study has resulted in an alternate packaging philosophy which Radiation gladly shares with CRC as an approach having definite advantages over the design approach specified in AR-104-3. This approach provides the following:

- I Greater reliability than that obtainable under AR-104-3, even if infinite spare modules are assumed for the AR-104-3 approach because of the elimination of module connectors.
- II Lower weight than that obtainable under AR-104-3 for specified minimum reliability.
- III Faster, simpler and easier maintenance by the astronaut than is possible under AR-104-3.
- IV Lower volume than that required under AR-104-3 for the specified reliability.

Further side benefits of this alternate approach include a ready-made spares storage capability and a package concept which has been thoroughly proved by Radiation Incorporated on the aforementioned satellite programs, thus producing minimum risk to schedule and cost. Further, no degradation from the AR-104-3 approach is realized in power consumption, accuracy, or flexibility -- and producibility, though last in importance, is considerably enhanced.

Package Description

The entire telemetry system is packaged in two (2) single SEP's. Each SEP consists of a group of non-replaceable (in-flight) modules held under compression which are hard wired to each other and to the SEP connectors. The SEP, then, becomes the lowest level of in-flight maintenance, being replaced by a spare SEP in case of malfunction. Basic system weight without spares is 20.7 pounds. For a

reliability figure of .997+ (in this case it is actually .9990) after 340 hours; a total of three (3) SEP spares is required, bringing the total system weight to 53.4 pounds, (approximately 12.0 pounds less than for the AR-104-3 approach.) Ultimate reliability of .9999+ is achievable by the addition of two (2) more spares, bringing the total weight to 74.1 pounds. This is still 5.9 pounds under the 80 pound limit.

Maintainability of the system is greatly improved. First, fault isolation is reduced from a total of 54 modules to two units. Second, after location of the fault, replacement of the SEP with a spare requires minimum time and effort. It is only necessary to loosen the captive extractor screws, lift out the SEP, insert a new SEP and tighten the intractor screws. The spare SEP's can be stored in the telemetry equipment rack. This maintenance procedure is contrasted with the following steps under AR-104-3 which must be performed after a more complicated fault isolation procedure:

1. Loosen three (3) extractor bolts
2. Lift out SEP
3. Move to work bench surface
4. Loosen and remove four (4) tie bolts
5. Secure tie bolts if at zero G
6. Break Module Connector contact
7. Pull out module
8. Place faulty module in spares container
9. Locate and remove spare module from container
10. Plug in spare module
11. Remove four (4) tie bolts from container
12. Insert four (4) tie bolts
13. Tighten four (4) tie bolts with wrench
14. Insert SEP into rack
15. Tighten three (3) intractor screws

Specification Deviation

There is one specification deviation that is required by Radiation Incorporated in order to provide the system described. The limit of 250 connector pins per SEP must be raised to 620 maximum, and use of additional connector surface area on the SEP must be allowed. Since a double SEP with 500 pins total is allowed in the specification, it is felt by Radiation Incorporated that the request for 620 pins on a single package is not unreasonable from the insertion-extraction standpoint. Cannon Electric's quoted insertion, withdrawal force per pin is 1 to 8 ounces. For a 500 pin double SEP, the limits of total force required to make or break contact would range from 31.25 pounds to 250 pounds. Radiation's request for 620 pins would increase the limits of this total force to a range of 38.75 pounds to 310 pounds.

The requirement for additional connector surface area on the SEP is a matter of connector pin density limitations. The 620 required pins cannot, with available high reliability connectors, be confined in the connector surface area provided in AR-104-3. We realize the significance of this deviation request to the spacecraft wiring, and, for that reason, propose that a mutually agreeable configuration be arrived at by CRC and Radiation Incorporated. One location acceptable to Radiation Incorporated is the rear chassis zone of the SEP.

This alternate packaging approach is to be considered a firm alternate to the proposal, requiring only the stated connector deviation to the specification. All other specification compliance intents of section 1.1.4 of the prime proposal are valid.