

Chapter 4

COMPONENT THEORY OF OPERATION

4-1 SCOPE

This chapter discusses the operation of individual assemblies by explaining, in detail, the operation of components or circuits in the assemblies. The detailed discussions are generally limited to those components or circuits whose operation is not apparent in the functional descriptions presented in chapter 2.

4-2 APOLLO II INERTIAL REFERENCE INTEGRATING GYRO

The Apollo II IRIG stabilization gyro (figure 4-1) is a fluid and magnetically suspended, single-degree-of-freedom, integrating gyro. It is one of the 25-series of inertial instruments. The 25 designation denotes the case diameter in tenths of inches. The stabilization gyros are the sensing elements of the stabilization loop. Three such gyros are mounted on the stable member so that their input axes are mutually perpendicular. Any change in the attitude of the stable member is sensed by one or more of the gyros. The gyros convert this displacement into an error signal which is amplified and fed into the gimbal torque motors. The gimbal torque motors reposition the stable member until the error signals are nulled and the original orientation of the stable member is re-established.

The Apollo II IRIG consists of a wheel assembly, a spherical float, a cylindrical case, a signal generator ducosyn, and a torque generator ducosyn. The wheel is mounted within the sealed float on a shaft perpendicular to the float axis and spins on preloaded ball bearings. The wheel is driven as a hysteresis synchronous motor in an atmosphere of helium. The float is mounted within the case on a shaft axially coincident with the longitudinal axes of both float and case. Precision hard-alloy pivots and bearings are located at each end of the float shaft, with the bearing being part of the float assembly. The torque generator ducosyn is mounted on one end of the float shaft, while the signal generator ducosyn is mounted on the opposite end. The space between the float and case is filled with a suspension and damping fluid.

Four axes (input, spin, spin reference, and output) are associated with the Apollo II IRIG. While the wheel is spinning, the gyro tends to maintain its attitude with respect to space. If the gyro is forced to rotate about the input axis (perpendicular to the wheel

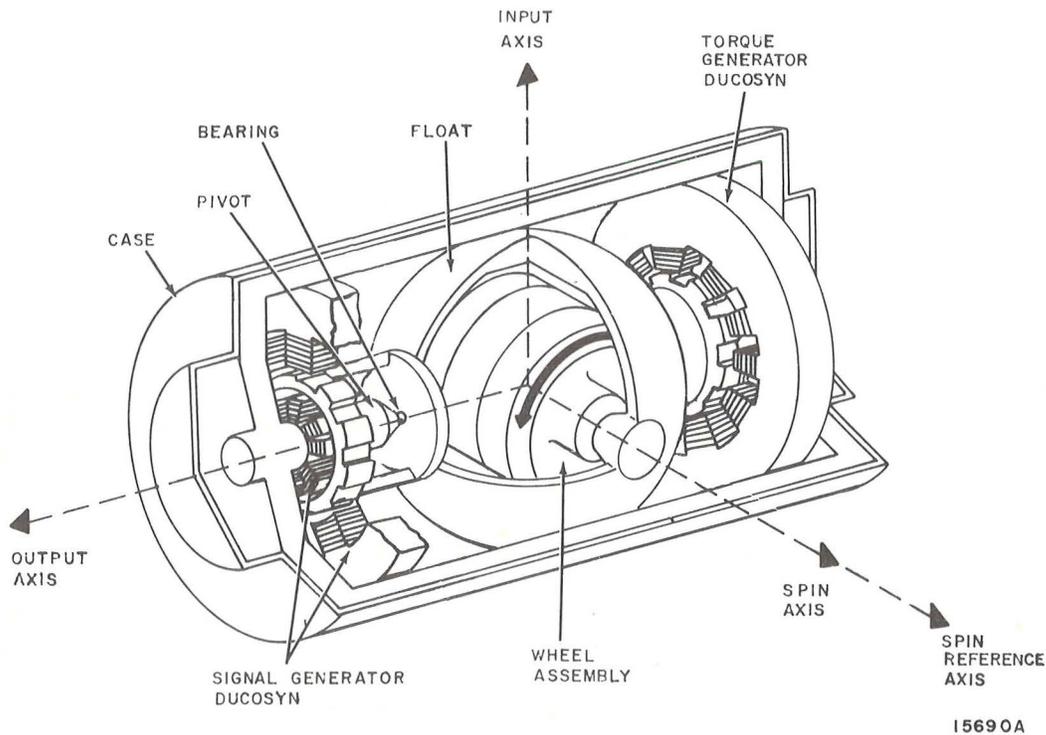


Figure 4-1. Apollo II IRIG, Simplified Cutaway View

spin axis), it will respond with a torque about the output axis (perpendicular to both spin and input axes). The spin axis is displaced from its normal or null alignment with the spin reference axis by an amount equal to the angle through which the output axis has rotated. The spin reference, input, and output axes are always mutually perpendicular. The rotation produced about the output axis in response to a rotation about the input axis in a single-degree-of-freedom gyro is called gyroscopic precession. The output axis is along the float shaft. Rotation of the gyro about its input axis results in a precession of the float.

The signal generator ducosyn is mounted on the positive output axis end of the float to provide magnetic suspension of the float with respect to the case, and to serve as a transducer for providing an electrical analog signal which indicates the amount and direction of the angular rotation of the float about the output axis. The torque generator ducosyn is mounted on the negative output axis end of the float to provide magnetic suspension, and to serve as a transducer for converting electrical error signals to a torque about the output axis when desired.

Since float movement is a measure of angular displacement of the gyro, friction on the float shaft (output axis) is a critical factor of gyro sensitivity. To reduce this friction to a negligible level, the space between the float and case is filled with a fluid which has the same density (specific gravity) as the float. This fluid causes the float to be suspended with respect to the case. Density of the fluid is kept equal to the density of the float by the controlled application of heat. Heating coils attached to the Apollo II IRIG end mounts maintain the density of the fluid. Two sensors submerged in the fluid indicate the temperature of the fluid. The fluid also provides viscous damping of float movement. The fluid suspension is supplemented by magnetic suspension which keeps the pivot centered in the bearing. The magnetic suspension forces are created by the signal and torque generator ducosyns. Under normal environmental conditions the pivot never touches the bearing. Polished precision hard-alloy bearings and pivots are used to minimize the friction which may result if the pivot touches the bearing under extreme environmental conditions.

Since oxygen would rust the ferrous parts in the wheel assembly, the float is filled with helium which will conduct heat away from the wheel motor. Because helium is a light gas it generates little windage, resulting in the additional advantage of low windage losses in the wheel motor. The float is filled with helium at a pressure of one-half atmosphere to further reduce windage losses.

4-2.1 GYRO WHEEL ASSEMBLY. The gyro wheel assembly consists of a wheel, a shaft, hysteresis ring, ball bearings and bearing retainer. The wheel consists of a beryllium hub with a steel rim. The purpose of the composite wheel is to concentrate as much weight as possible in the outside rim, providing the wheel with a high moment of inertia. The hollow steel shaft has female threads on each end and is machined to serve as the inner race for the ball bearings. Preloading of the wheel is achieved and controlled by bolting the bearing retainers to the hub. The bearing retainers press on the outer bearing race exerting a wedging action on the balls. As a result, a deliberate load (preload) is imposed on the wheel bearing to insure that the wheel rotates precisely at a right angle to the shaft. The amount of preload is carefully determined since excessive preload will introduce excessive bearing friction that would limit bearing life. The hysteresis ring, constructed of laminated, specially hardened steel, is fitted on the wheel hub and serves as a rotor for the hysteresis synchronous motor which drives the wheel.

4-2.2 FLOAT ASSEMBLY. The float assembly consists essentially of the float gimbal, two hemispheres, hysteresis motor stator, and bearings. The wheel assembly is bolted to the float by threaded rings. The rings also hold together the float gimbal and the float hemispheres, both of which are made of beryllium. The hysteresis motor stator is placed inside the float gimbal with the power leads brought out through each end of the float gimbal. The float shaft is an integral part of the float gimbal and extends outward from the float to serve as a mount for the float bearings and ducosyn rotors. The bearings, when placed on each end of the float gimbal, define the output axis. The float gimbal also has a hole fitted with a ball and screw seal through which the float is evacuated and filled with helium. Preliminary balance weights are placed on the float gimbal

for rotational balancing prior to the float being inserted into the case. Balance weights along the spin axis and the input axis are accessible from outside the case and are used for rotational balancing after final assembly.

4-2.3 CASE. The case consists essentially of main housing and damping block assemblies, end housing assembly, and main cover assembly. The float assembly is encased by the main housing assembly and is supported with respect to the end housing by the pivot assemblies. Beryllium damping blocks fill the space around the float. These blocks provide the necessary control of the damping gap (the width of the gap between the float assembly and case), thereby controlling the damping coefficient. The end housings are held to the main housing by clamping caps. The end housings contain the pivot assemblies, ducosyn stators, bellows to take up the expansion and contraction of the suspension fluid, and a setscrew and ball seal to allow filling with the suspension fluid. Four balance adjusters, provided in the main housing assembly, allow access to the adjustable balance weights along the spin axis and the input axis. After hermetic sealing and balancing of the unit, the Apollo II IRIG is covered by a main cover assembly which provides a magnetic shield plus a second hermetic sealing.

4-2.4 NORMALIZING NETWORK. The normalizing network (figure 4-2) contains the magnetic suspension capacitors, torque generator normalization resistors, temperature sensor normalization resistor, main heater, auxiliary heater, and signal generator preamplifier with gain normalization resistor attached. The pre-alignment package is added to the signal generator end of the gyro case during final assembly, making the gyro a pre-aligned gyro. The gyro is pre-aligned on a test stand with the input axis aligned about the output axis relative to a slot in the mounting ring. This alignment is carried over to the stable member where a pin is precisely located to pick up the slot. When the gyro is mounted in the stable member, an additional main heater and an additional auxiliary heater are placed on the torque generator end.

The signal generator preamplifier is an ac amplifier with transformer coupled input and output which amplifies the gyro output signal prior to transmission from the stable member to the PSA.

4-2.5 APOLLO II IRIG DUCOSYNS. The Apollo II IRIG uses ducosyns for magnetic suspension of the float, signal generator action, and torque generator action. The ducosyn is a separate magnetic suspension microsyn and separate transducer microsyn in a single unit. The unit contains two separate stators mounted in the end housing and two separate rotors mounted on a common mounting ring of the float assembly. The inside stator assembly consists of eight outwardly projecting tapered poles which are wound and excited to provide magnetic suspension. The outer stator assembly consists of twelve inwardly projecting poles which are wound to provide either signal generator or torque generator action. The outer rotor is the transducer rotor and consists of eight unwound salient poles projecting outward. The inner rotor, which is the magnetic suspension rotor, is cylindrical, tapered, and unwound. A beryllium ring separates the two rotors to reduce cross-coupling effects.

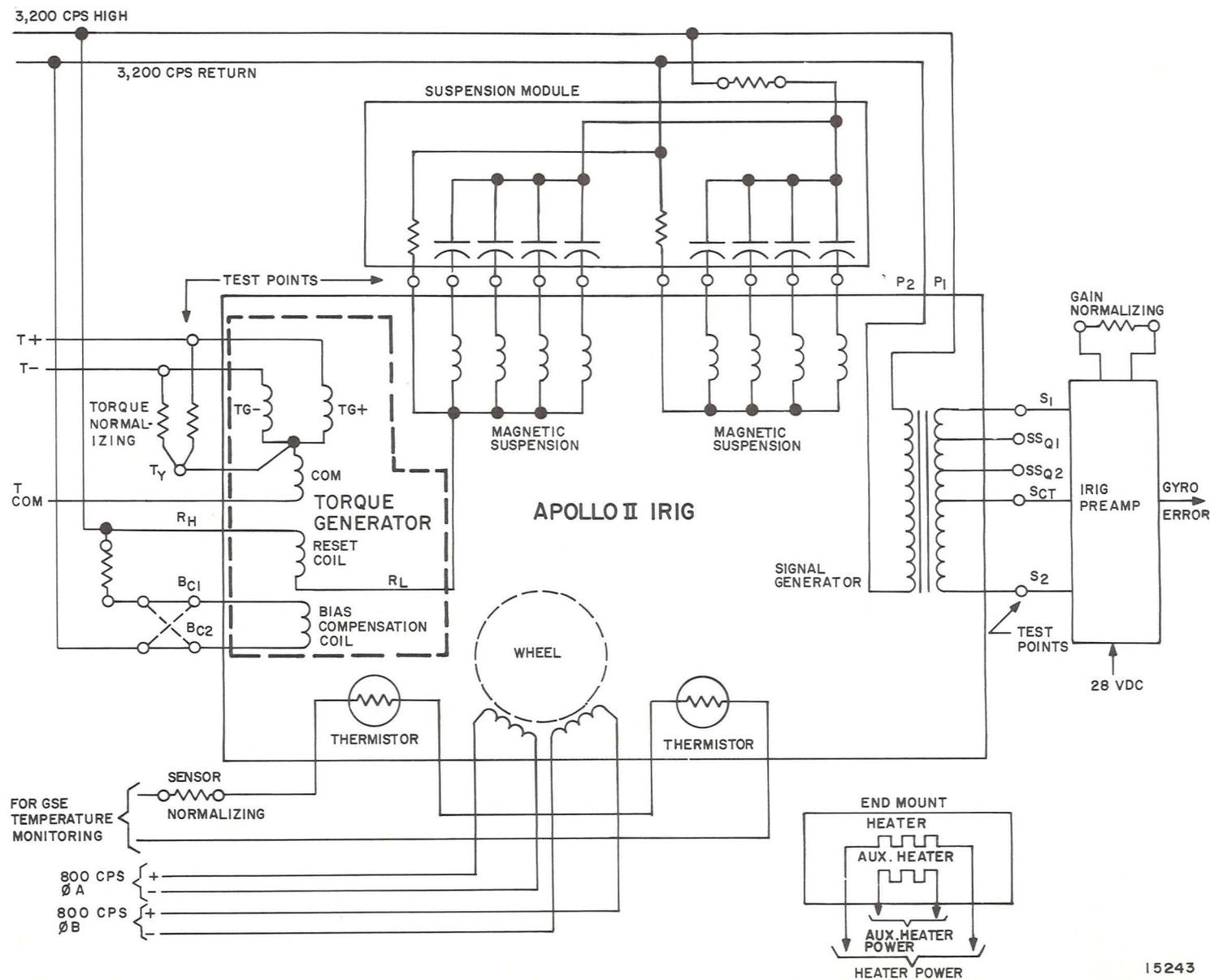


Figure 4-2. Apollo II IRIG Normalizing Network

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4-2.5.1 IRIG Signal Generator Ducosyn. The signal generator ducosyn is mounted on the positive output axis end of the gyro to provide magnetic suspension and to serve as a transducer to provide an electrical analog signal representing the position of the float relative to the case. (See figure 4-3.) Poles 1, 4, 7, and 10 are wound with primary windings which induce a voltage into the secondary windings on the pole pieces on either

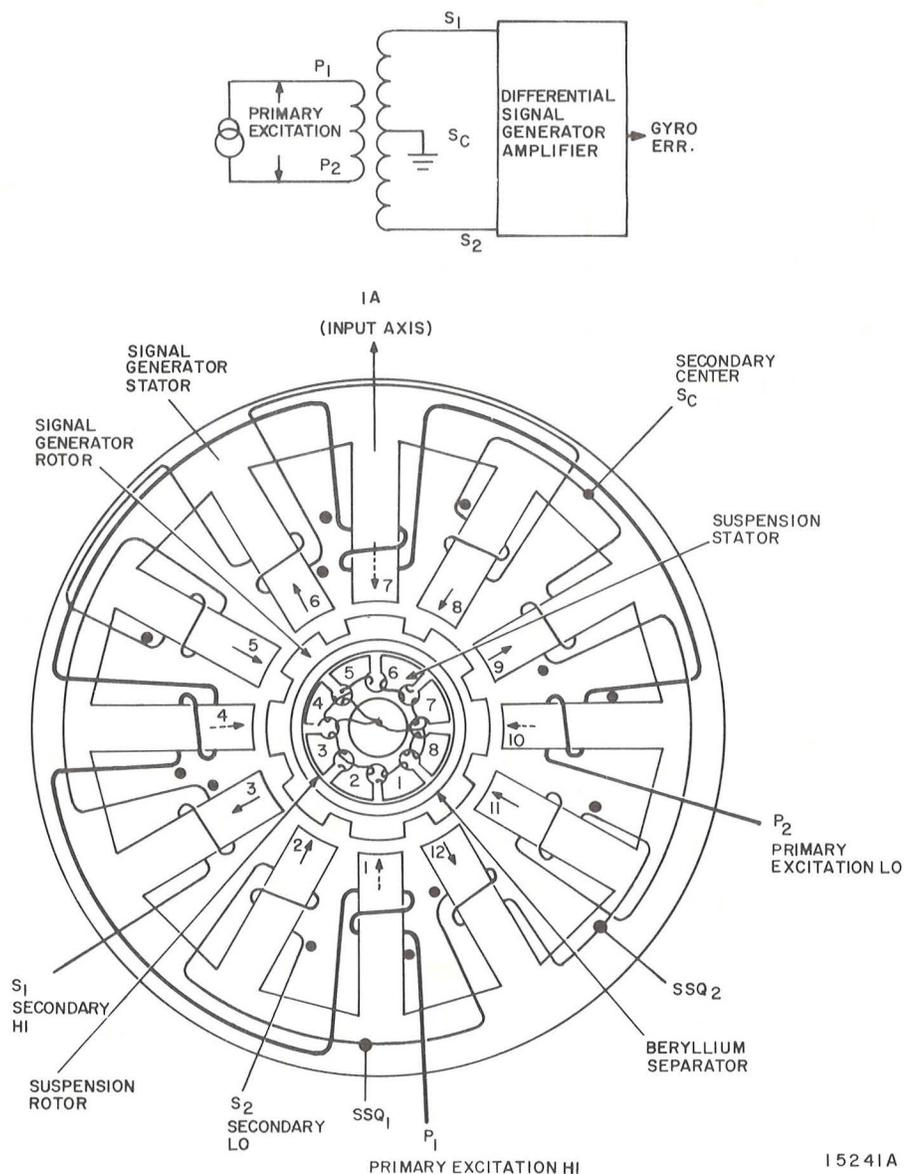


Figure 4-3. IRIG Signal Generator and Suspension Microsyn

side of the primary winding poles. All secondary windings are wound with equal turns. The secondary windings (2-12, 3-5, 6-8, and 9-11) on either side of each primary pole are wound in opposition to each other. When the rotor pole pieces are symmetrically located between the pairs of secondary poles, the flux density in the secondary poles is equal and equal voltage is induced in the secondary windings. Since the secondary windings are wound in opposition, the induced voltages cancel and the net output voltage is zero. This is the null position of the rotor. When the rotor is rotated from the null position as a result of float displacement, the equality of air gap reluctance is disrupted resulting in unequal flux density in the pairs of secondary poles and therefore unequal induced voltages in the windings. The magnitude of the net output voltage depends on the degree of air gap reluctance unbalance; the greater the rotor displacement from null, the greater the net output voltage. The phase of the net output voltage is determined by the direction of rotor rotation. As a result of counterclockwise rotation, higher voltages are induced in the secondary windings that are wound in phase with the primary windings, causing the net output voltage to be in phase with the primary excitation. In the same manner, clockwise rotation produces a net output voltage that is out of phase with the primary excitation.

The Apollo II IRIG ducosyns require a 4 volt, 3,200 cps, single phase excitation for the signal generator primary windings and for the magnetic suspension portions.

4-2.5.2 IRIG Torque Generator Ducosyn. The Apollo II IRIG torque generator ducosyn is mounted on the negative output axis end of the float to provide magnetic suspension and to serve as a transducer to convert an electrical error signal into a torque about the output axis. Figure 4-4 shows the torque generator with the rotor in the null position. To develop torque, current is allowed to flow through the common winding and through either the T+ or the T- winding. The direction of torque is determined by the winding through which current flows. The torque generator stator may be considered as divided into four symmetrical groups of three poles. The center pole of each group (1, 4, 7, and 10) has a common winding only and will always be a north pole when energized. The poles on either side (2-12, 3-5, 6-8, and 9-11) of the center poles have both T+ and T- windings with the polarity of the poles determined by which of the two windings is energized. In either case, one pole in each group will become a north pole and the other a south pole. Since the center pole is always a north pole, each group of three poles will consist of two north poles and one south pole whenever the windings are energized. The rotor will tend to align itself symmetrically between the north and south poles, creating a torque. When the T- winding is energized, pole 12 will become a south pole and pole 2 will become a north pole. The rotor, in attempting to align itself, will tend to rotate clockwise until rotor pole 8 is directly opposite stator pole 12 and rotor pole 1 is directly between stator poles 1 and 2, since 1 and 2 are both north poles. When the T+ winding is energized, stator pole 2 will become a south pole and stator pole 12 will become a north pole. The rotor will tend to rotate counterclockwise attempting to align rotor pole 2 opposite stator pole 2, and rotor pole 1 between stator poles 1 and 12. The other poles attempt to align themselves in the same manner.

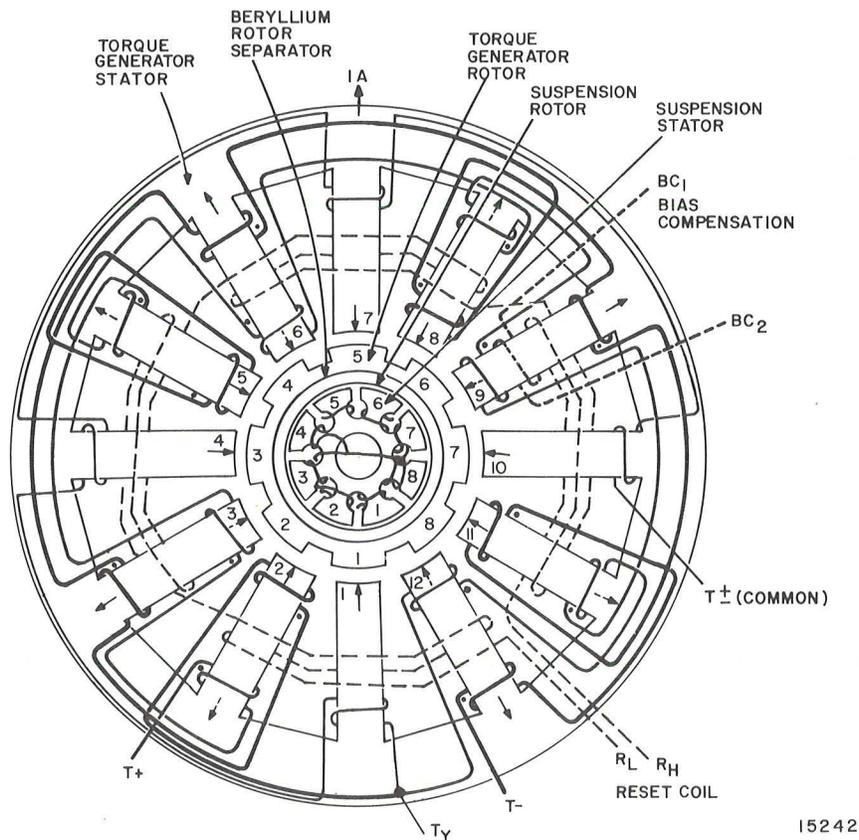


Figure 4-4. IRIG Torque Generator and Suspension Microsyn

The direction of the desired torque is controlled by gyro select pulses from the CMC. The pulses act through a switching network in the gyro calibration module to close the torque current path through either the T+ or the T- winding. The magnitude of the torque current is held constant to develop a constant torque. Torque on the rotor produces torque on the gyrofloat. The resulting float displacement creates an error signal from the ducosyn signal generator. Thus, the position of the IMU stable member is changed by the compensating reaction from the stabilization loops.

The torque generator stator also has a reset coil and a bias compensation coil, both of which are continuously energized by the 4 volt, 3,200 cps magnetic suspension and signal generator excitation voltage. The reset coil serves to keep the magnetic state of the magnetic material constant following any torque commands. This degaussing action prevents the storage of residual magnetic dipoles in the rotor and stator which would create torque. A winding around each group of three stator poles acts as a reset coil

for both rotor and stator. The bias compensation coil creates a torque equal and opposite the non-gravity torques which produce bias drift, such as the torque due to flex leads. In this manner, the bias drift due to these sources may be reduced to zero.

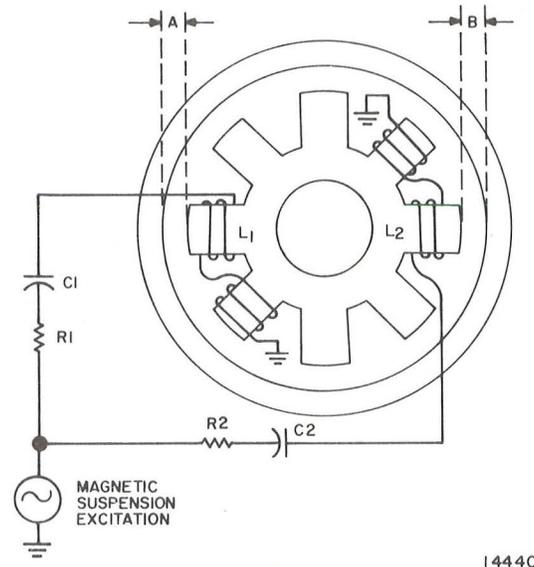
4-2.5.3 IRIG Ducosyn Magnetic Suspension Unit. The Apollo II IRIG ducosyn magnetic suspension units have a tapered cylindrical rotor and tapered stator poles that develop radial and axial magnetic suspension of the gyro float.

Each stator winding is part of a series resistance inductance capacitance (RLC) circuit. (See figure 4-5). Although the equivalent circuit illustrated shows only two poles, it is representative of any of the four pairs of diametrically opposed stator poles. Inductances L_1 and L_2 represent the total inductances of the stator windings. Resistances R_1 and R_2 represent the total resistance of each stator circuit. Capacitors C_1 and C_2 are the external fixed capacitors in series with the resistance and inductance. The values of L_1 and L_2 vary inversely with the size of air gaps A and B respectively.

The excitation to the magnetic suspension unit is maintained at precisely 3,200 cps; the inductance is the only circuit variable. When the inductance is adjusted so the inductive reactance equals and cancels the capacitive reactance, circuit resonance is achieved. At resonance, the total circuit impedance is at a minimum, consisting only of resistance, and the current is thus at a maximum. During construction and testing, a fixed suspension capacitor is selected that develops a value of capacitive reactance that is less than the value of inductive reactance present when the rotor is at null. The resulting impedance allows a current flow that is less than the maximum or resonant current. In operation, translational movement of the rotor from its null point alters the inductance to bring the circuit closer to or further from resonance.

The current flow through the R_1 , L_1 , and C_1 circuit of figure 4-5 increases or decreases according to the inductance which is controlled by air gap A. At some position of the rotor (or value of A) L will produce resonance and maximum current. As the rotor moves in either direction from the resonant point, the current falls off sharply because the value of L (and inductive reactance) changes to make the circuit impedance greater. The current in the stator winding determines the amount of magnetic energy in the stator pole. The attracting force on the rotor is equal to the change in magnetic energy divided by the change in air gap. This relationship of force versus air gap is such that as the rotor moves away from the stator (increasing A), the attracting force rises to a maximum, then decreases sharply as the rotor passes through the resonant point. A negative or repelling force is developed as the rotor is moved beyond the resonant point. In operation, the movement of the rotor is limited by the float pivots so the attracting force only increases as the rotor is moved away from the stator to its maximum allowable displacement. Conversely, as the rotor moves closer to the stator, decreasing the air gap, the attracting force decreases.

As the rotor moves right, air gap A increases and air gap B decreases, and vice-versa. The attracting force at one stator pole changes inversely to the change in attracting force at the other stator pole. When the rotor is displaced from its null point (where



14440

Figure 4-5. Ducosyn RLC Equivalent Circuit

the forces on the rotor from both poles are equal), the force from the pole the rotor is approaching decreases, and that of the opposite pole increases. The direction of the resultant force moves the rotor back to the null position. This action magnetically clamps the rotor between its operating limits. Since the four pairs of stator poles are arranged in a circle within the rotor, their simultaneous action effectively suspends the rotor.

Since the rotor and the stator poles are tapered, end play on the float tends to increase or decrease the air gaps of the magnetic suspension units located at each end of the float. The two magnetic suspension units act together to develop a component of force that supports the float axially.

4-3 16 PULSED INTEGRATING PENDULUM

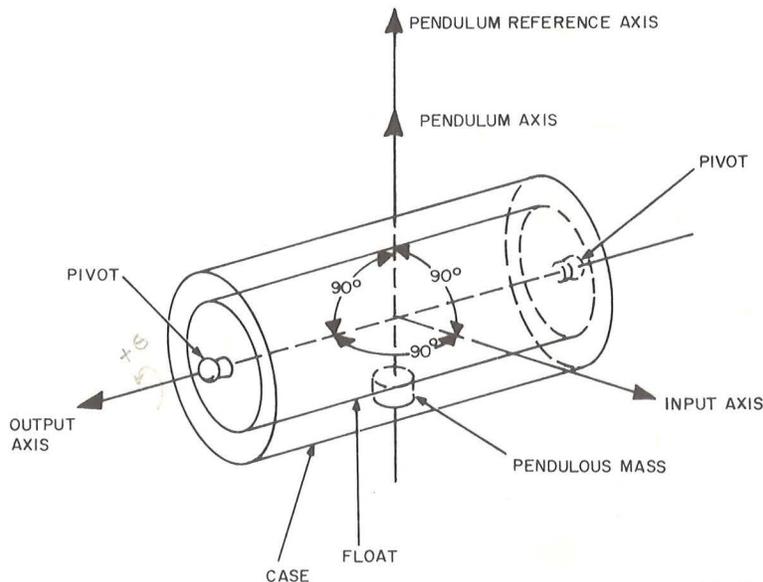
The 16 PIP's are used as accelerometers in the IMU. The 16 PIP in itself is not an accelerometer, but an acceleration sensitive device. In its associated accelerometer loop, the 16 PIP becomes an integrating accelerometer.

The 16 PIP is basically a cylinder with a pendulous mass unbalance (pendulous float) and is pivoted with respect to a case. The pendulous float has no electrical power

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

requirements as it is completely mechanical in operation. The space between the pendulous float and case is filled with a fluid. A signal generator ducosyn, located at one end of the float, provides magnetic suspension of the float with respect to the case and acts as a transducer to convert mechanical rotation of the float with respect to the case into electrical analog signals. A torque generator ducosyn, located at the other end of the float, provides magnetic suspension of the float with respect to the case and acts as a transducer to convert electrical signals into mechanical torque about the float shaft. A 2 volt rms, 3,200 cps, single phase excitation is required for the magnetic suspension portion of each ducosyn and for the transducer portion of the signal generator ducosyn.

The output axis of the 16 PIP is defined by the axis of the pivots which support the float with respect to the case. (See figure 4-6.) The pendulum axis is defined by a line which passes through the mass unbalance and intersects the output axis at a right angle. The input axis is the axis along which the 16 PIP is sensitive to acceleration. The input axis and pendulum axis form a plane that is perpendicular to the output axis. When the float rotates about the output axis, the pendulum axis is displaced proportionately from its normal or null position (pendulum reference axis). The pendulum reference, input, and output axes are always mutually perpendicular.



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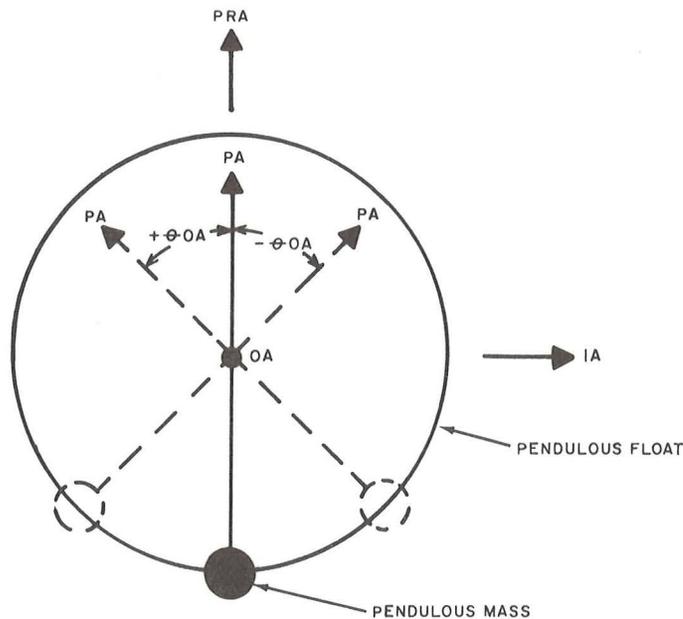
Figure 4-6. Definition of 16 PIP Axes

The mass unbalance hangs below the output axis and is forced by loop torquing to swing like a pendulum. The torquing required to keep the pendulum action oscillatory at no acceleration is a known value. When acceleration is sensed along the input axis, an additional torque is felt by the pendulum and the loop compensates for the acceleration torque by supplying torquing current for additional time.

Figure 4-7 illustrates the direction the pendulous mass tends to swing due to acceleration torque as viewed from the positive end of the output axis or signal generator end of the PIP.

Acceleration in the direction of the positive input axis (the direction in which the arrowhead points) results in a torque on the float about the output axis which tends to rotate it in the negative angular direction ($-\theta_{OA}$) about the output axis. Conversely, acceleration in the direction of the negative input axis produces a torque on the float tending to rotate it in the positive angular direction ($+\theta_{OA}$) about the output axis. When no acceleration is being felt along the input axis, the summation of the angular displacement about the output axis is zero; and by definition, the PIP is at a null.

Maximum sensitivity and linearity of the 16 PIP occur near null. To assure maximum sensitivity and linearity, the accelerometer loop in which the 16 PIP is used restricts the angular displacement about the output axis to very small excursions in either direction from null. The accelerometer loop is designed so that the torque developed



14434

Figure 4-7. Result of Acceleration Along Input Axes

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

by the torque generator is equal to and opposite the pendulous torque resulting from applied acceleration. The signal generator, located at the positive end of the output axis, senses an angular displacement of the float about the output axis. The phase and magnitude of the output signals from the signal generator secondary winding are determined by the direction and amount of float displacement. The error signals are processed by the accelerometer loop into incremental velocity pulses to the CMC and into torquing current to the torque generator.

4-3.1 FLOAT ASSEMBLY. The float is a hollow beryllium cylinder fitted with a shaft on which the float pivots are located. On both ends of the float are salient four pole transducer rotors and cylindrical magnetic suspension rotors with tapered inside diameters. The rotor itself is a solid one piece device. The pendulous mass screws into and protrudes slightly from the float. A pin and screw which provides pendulousity adjustment also serves as a stop to limit float rotation about the output axis to ± 1 degree. Adjustable balance weights for rotational balancing of the float are located along the pendulum axis and the input axis. The completed float assembly is placed in a main housing assembly filled with a suspension fluid. The suspension fluid provides fluid suspension of the float with respect to the case and viscous damping of the float.

4-3.2 HOUSING ASSEMBLY. The housing assembly consists of a main housing assembly and two end housings. Damping blocks line the inner diameter of the main housing so as to surround the float. Four bellows assemblies are located within the damping blocks and take up the expansion and contraction of the suspension fluid resulting from variations in the temperature of the fluid. Each end housing contains a pivot bearing, an eight pole magnetic suspension stator, and either an eight pole signal generator stator or an eight pole torque generator stator. The two end housings are called the signal generator end housing (on the +OA end) and the torque generator end housing (on the -OA end). The magnetic suspension microsins have tapered stator poles and a tapered rotor, developing magnetic suspension forces in both radial and axial directions.

4-3.3 OUTER CASE ASSEMBLY. The housing assembly is completely covered by an outer case which provides magnetic shielding and a hermetic seal for the unit. Heating coils are placed between the main housing and the outer case to heat the suspension fluid to the proper temperature for fluid suspension of the float. All electrical connections for signal generator, torque generator, magnetic suspension microsins, and heaters are brought out through the torque generator end of the case.

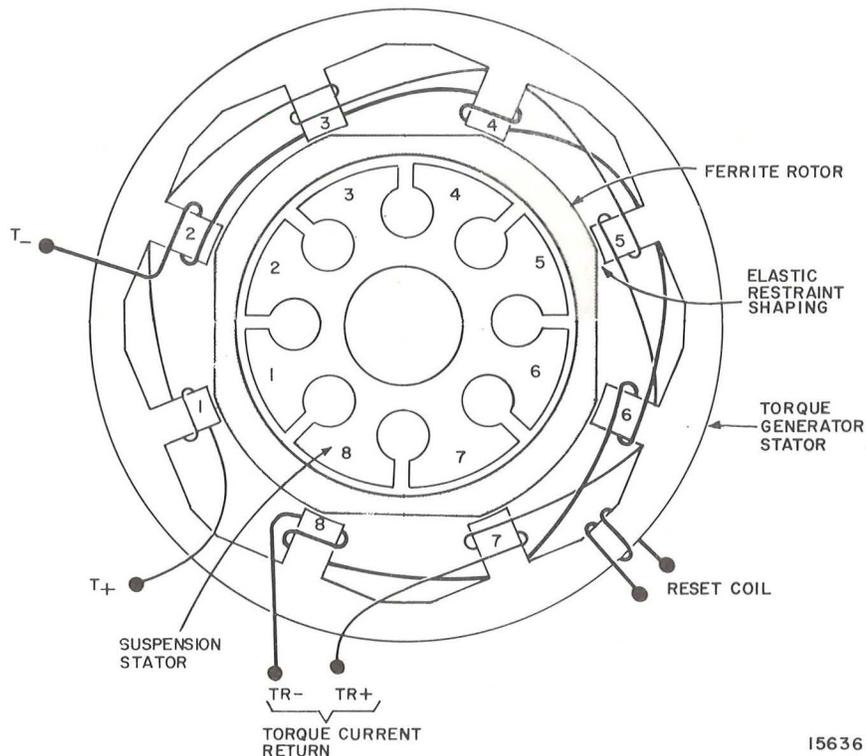
4-3.4 NORMALIZING NETWORK. The 16 PIP normalizing network module contains the suspension capacitors, torque generator normalizing resistors, and temperature sensor normalizing resistors. This module is mounted over the 16 PIP and bridges the 16 PIP end cap. However, to avoid PIP alignment problems this module is fastened to the stable member instead of the 16 PIP.

4-3.5 PIP DUCOSYNS. The 16 PIP ducosyn signal generator and torque generator differ from the Apollo II IRIG units in both construction and operation. The 16 PIP signal generator and torque generator have eight pole stators. The 16 PIP ducosyn rotor is constructed from a solid piece of ferrite. Flats are ground onto the outer diameter of the rotor to create pseudo-salient poles which serve as the transducer rotor. The inner

diameter of the rotor is tapered and serves as the magnetic suspension rotor. There is no magnetic separation between the transducer rotor and the suspension rotor; therefore, the magnetic suspension rotor degausses the torque generator rotor. The degaussing prevents the storage of residual magnetic poles in the magnetic material which could cause unwanted torques to be created.

The torque generator stator has a single winding per pole. (See figure 4-8.) The windings on the even poles develop negative torque and the windings on the odd numbered poles develop positive torque. The accelerometer loop applies constant dc current to either the odd or even poles. The torque generator stator also has a reset winding which degausses the stator, thus preventing the storage of residual magnetic poles which could create unwanted torque.

The signal generator stator poles have both a primary and secondary winding per pole. The secondary windings are wound in opposition so that when the rotor is at null



15636

Figure 4-8. PIP Torque Generator

the air gap reluctance at each pair of stator poles is equal and the net output voltage is zero. When the rotor is displaced from null, the air gap reluctance becomes unequal and a net output voltage proportional to the direction and magnitude of the float displacement is developed. The output of the signal generator is amplified, phase shifted, and applied to the interrogator module in the accelerometer loop which detects the direction of float displacement.

4-4 COUPLING DATA UNIT

The CDU is an electronic device used as an interface element between the PGNCSS subsystems, the PGNCSS, and various displays and controls. The CDU is a sealed unit containing 32 modules of ten types. The ten module types make up five, almost identical, channels; one each for the IMU inner, middle, and outer gimbals and one each for the OUA SXT shaft and trunnion axes. Several of the CDU modules are shared by the five channels.

The CDU functions primarily as an analog to digital (A/D) converter and as a digital to analog (D/A) converter. The A/D converter converts resolver signals into digital information which is stored in a 16 stage binary counter called the read counter. The D/A converter accepts pulses from the CMC, stores them in a 9 stage binary counter called the error counter, and provides ac and dc output signals proportional to the stored pulses. A digital feedback path between the read counter and the error counter is provided to count up as the read counter counts down and vice versa.

The CDU converts the IMU gimbal angular information from 1X and 16X resolver signals into digital information. The resolver angle is digitized into bits, equal to 20 arc seconds each, and stored in the read counter. An error signal proportional to the difference between resolver angle and the CDU angle (the angle registered by the read counter) causes the read counter to count until the error signal is nulled. If the difference between the resolver angle and the CDU angle is greater than 400 arc seconds, the read counter will be incremented at a 12.8 kpps rate. The incrementing rate will be 800 pps if the difference is less than 400 arc seconds. As the read counter is incremented, the overflow output of the first stage (equivalent to 40 arc seconds per pulse) is sent to the CMC to indicate the change in resolver angles.

The CDU converts the optics SXT shaft and trunnion angular information from the shaft 16X and the trunnion 64X resolver signals into digital information. The resolver angle is digitized into bits equal to 2.5 arc seconds for trunnion and 20 arc seconds for shaft and stored in the read counters. The read counters are incremented at the same rate as the read counters used for the IMU gimbal angles. As the read counter is incremented, the overflow output of the first stage (equivalent to 5 arc seconds per pulse for the trunnion and 40 arc seconds per pulse for the shaft) is sent to the CMC to indicate the change in resolver angles.

4-4.1 COARSE SYSTEM MODULE. The coarse system module functions with the read counter to form the coarse analog to digital conversion system. The coarse module is used only in the three IMU CDU channels. The coarse module receives the $\sin \theta$ and $\cos \theta$ signals from the 1X gimbal angle resolver and switches them through attenuation

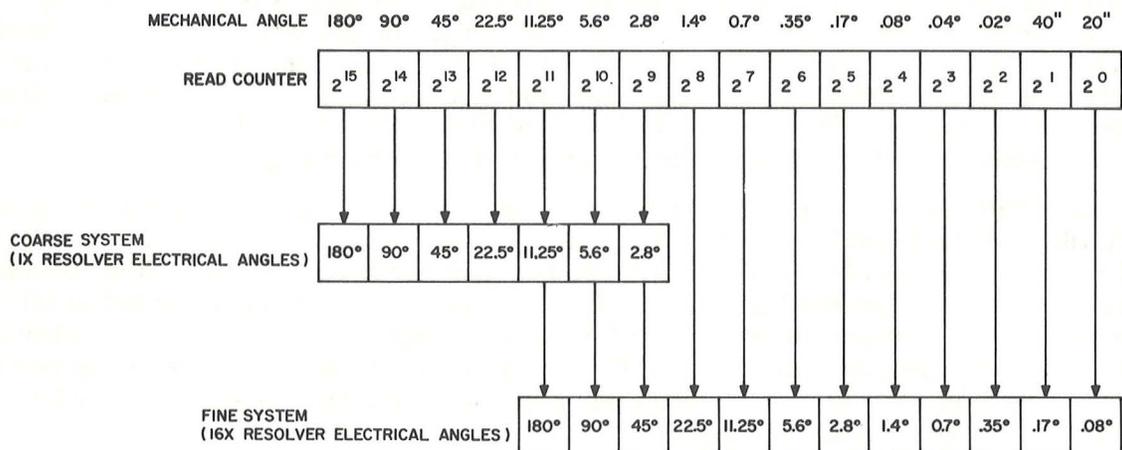
resistors which represent various values of $\sin \psi$ and $\cos \psi$. The resolver angle is compared with the angle registered by the read counter through the mechanization of the following trigonometric identity:

$$\pm \sin (\theta - \psi) = \pm \sin \theta \cos \psi \mp \cos \theta \sin \psi$$

where θ is the gimbal angle and ψ is the CDU angle represented by the accumulation of bits in the read counter. When θ and ψ are equal, the equation goes to zero. If θ does not equal ψ , an error detector in the coarse module produces an output that sends incrementing pulses to the read counter. As the read counter counts up or down, changing the value of ψ , it sends switch control signals from its seven most significant stages to the coarse module. The switch control signals operate switches in the coarse module changing the arrangement of the attenuation resistors for different values of $\sin \psi$ and $\cos \psi$ until a null output from the error detector is obtained. For each read counter angle ψ there is a corresponding switch arrangement which produces a null.

The accumulation of ψ is controlled by three modules within the CDU: the coarse module, the main summing amplifier and quadrature rejection module (MSA&QR), and the quadrant selector module. The coarse module is used in conjunction with the 1X gimbal angle resolver inputs. The other two modules are used in conjunction with the 16X gimbal resolver inputs and function with the read counter to form the fine analog to digital conversion system.

Figure 4-9 illustrates the mechanical angles of the gimbals, read counter bit positions associated with the mechanical angles, and coarse and fine system angles



18922

Figure 4-9. Read Counter Relationship to Coarse and Fine Systems

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

associated with each read counter bit position. Note that bits 2^0 through 2^{11} are associated with fine system switching and bits 2^9 through 2^{15} are associated with coarse system switching. The three bit overlap of the coarse and fine systems provides a smooth transition from one system to the other. The angles above the read counter blocks are the mechanical angles through which the 1X gimbal angle resolver shaft rotates. Note also that 180 electrical degrees of 16X resolver rotation is equal to 11.25 degrees of the 1X resolver angle.

Figure 4-10 provides a functional block diagram of the coarse module. The 1X resolver output signals, 26 v (rms) $\sin \theta$ and 26 v (rms) $\cos \theta$ are applied through transformers which have a transformation ratio of 26:4. A 28 v (rms) 800 cps reference signal is applied through a transformer which has a transformation ratio of 28:4. The maximum voltage available, high to center tap, is 4 v (rms). The gimbal angle is represented by the amplitude of the $\sin \theta$ and $\cos \theta$ signals and by their phase with respect to the 800 cps reference signal. If the gimbal angle were 150 degrees, for example, the $\sin \theta$ and $\cos \theta$ signals at the transformer secondaries would be equal to:

- (1) $(4 \text{ v rms}) (\sin 150^\circ) =$
 $(4 \text{ v rms}) (0.5) = 2.0 \text{ v (rms)}$
- (2) $(4 \text{ v rms}) (\cos 150^\circ) =$
 $(4 \text{ v rms}) (-0.866) = -3.46 \text{ v (rms)}$

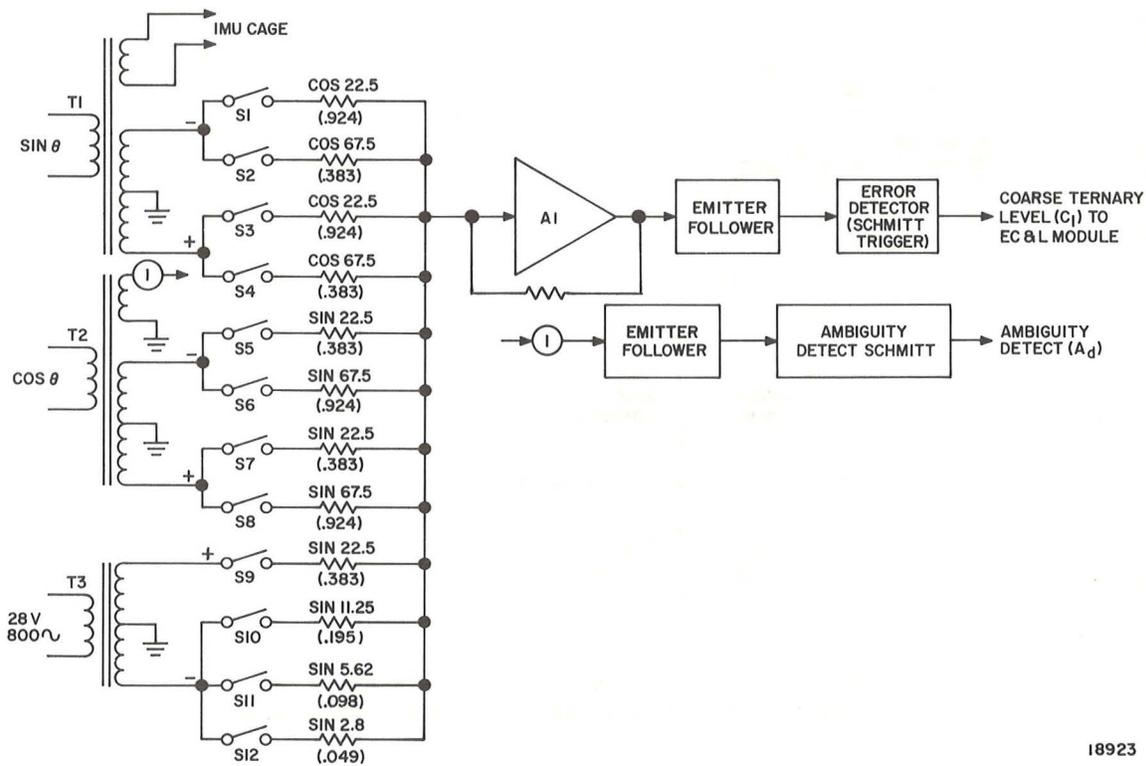
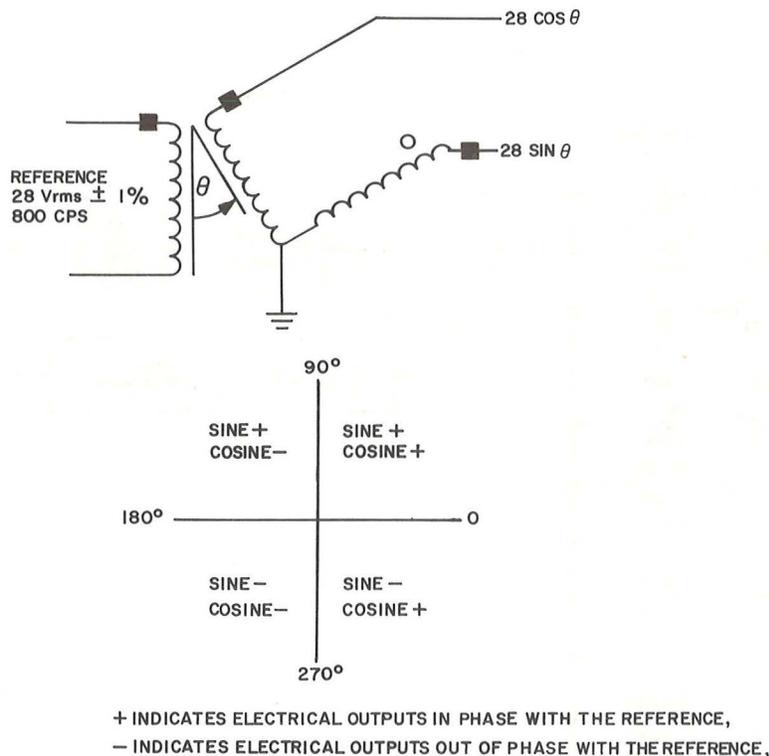


Figure 4-10. Coarse System Module Block Diagram

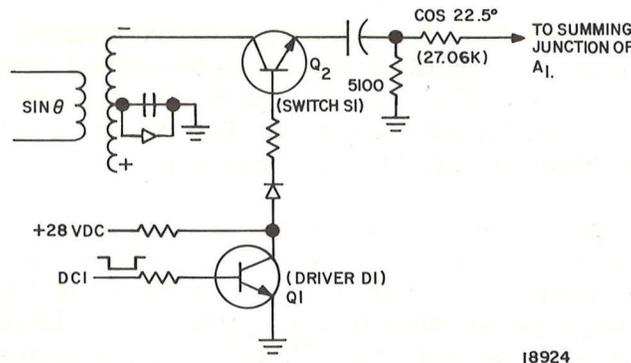
The $\sin \theta$ signal would be in phase with respect to the 800 cps reference. The $\cos \theta$ signal would be out of phase with respect to the 800 cps reference, as is signified by the minus sign. Figure 4-11 shows the phase relationship of the 1X resolver sine and cosine output signals with respect to the 800 cps reference.

Each center tapped secondary of the transformers provides both an in phase and an out of phase signal of equal amplitude, as signified by the plus or minus sign shown on each portion of the secondary winding. (See figure 4-10.) Thus, if the $\cos 150$ degrees signal were to be taken from the out of phase secondary, the signal would be equivalent to $(-4 \text{ v rms}) (-0.866) = 3.46 \text{ v (rms)}$, and would be in phase with respect to the 800 cps reference. The minus sign in front of the 4 v (rms) signifies that the out of phase portion of the transformer secondary was used. The signal from each portion of the T2 and T3 secondary windings is applied to two transistorized switches. The circuit for one of the switches, S1, is shown in figure 4-12. The circuit consists of switching transistor Q2 and the transistor driver Q1. When the logic equation for switch control signal DC1 is not satisfied, DC1 is at a positive voltage level allowing Q1 to conduct to saturation and keeping the base of Q2 grounded. With its base



16154

Figure 4-11. Resolver Sine and Cosine Phase Relationship



$DC1 = \frac{2^{15}}{2^{15}} \frac{2^{14}}{2^{14}} \frac{2^{13}}{2^{13}} + \frac{2^{15}}{2^{15}} \frac{2^{14}}{2^{14}} \frac{2^{13}}{2^{13}}$	$DC7 = 2^{15} (\frac{2^{14}}{2^{14}} \frac{2^{13}}{2^{13}} + \frac{2^{14}}{2^{14}} \frac{2^{13}}{2^{13}})$
$DC2 = \frac{2^{15}}{2^{15}} \frac{2^{14}}{2^{14}} \frac{2^{13}}{2^{13}} + \frac{2^{15}}{2^{15}} \frac{2^{14}}{2^{14}} \frac{2^{13}}{2^{13}}$	$DC8 = \frac{2^{15}}{2^{15}} (\frac{2^{14}}{2^{14}} \frac{2^{13}}{2^{13}} + \frac{2^{14}}{2^{14}} \frac{2^{13}}{2^{13}})$
$DC3 = \frac{2^{15}}{2^{15}} \frac{2^{14}}{2^{14}} \frac{2^{13}}{2^{13}} + \frac{2^{15}}{2^{15}} \frac{2^{14}}{2^{14}} \frac{2^{13}}{2^{13}}$	$DC9 = 2^{12}$
$DC4 = \frac{2^{15}}{2^{15}} \frac{2^{14}}{2^{14}} \frac{2^{13}}{2^{13}} + \frac{2^{15}}{2^{15}} \frac{2^{14}}{2^{14}} \frac{2^{13}}{2^{13}}$	$DC10 = 2^{11}$
$DC5 = \frac{2^{15}}{2^{15}} (\frac{2^{14}}{2^{14}} \frac{2^{13}}{2^{13}} + \frac{2^{14}}{2^{14}} \frac{2^{13}}{2^{13}})$	$DC11 = 2^{10}$
$DC6 = \frac{2^{15}}{2^{15}} (\frac{2^{14}}{2^{14}} \frac{2^{13}}{2^{13}} + \frac{2^{14}}{2^{14}} \frac{2^{13}}{2^{13}})$	$DC12 = 2^9$

Figure 4-12. Coarse Switch Circuit and Logic Equations

grounded, Q2 is turned off (open) preventing the transformer output signal from being applied to the attenuator resistor circuit labeled $\cos 22.5^\circ$. When its logic equation is satisfied, DC1 drops to 0 vdc and Q1 stops conducting, allowing the base of Q2 to rise toward +28 vdc causing Q2 to conduct to saturation. With Q2 turned on, the transformer output is applied through the attenuator resistor circuit to the summing junction of operational amplifier A1. All of the coarse system module switches (S1 through S12) operate in an identical manner. The logic equations for the switch control signals (DC1 through DC12) that activate the switches are given in figure 4-12.

Switches S1 through S8 mechanize the system's nulling identity, $\pm \sin(\theta - \psi) = \sin \theta \cos \psi \mp \cos \theta \sin \psi$, directly by switching the $\sin \theta$ and $\cos \theta$ signals from the transformer secondaries through the attenuator resistors which represent values of $\sin \psi$ and $\cos \psi$. At the same time the switches select either the in phase or out of phase transformer output so that the attenuated signals will always be out of phase with respect to each other at the summing junction, and thus, be consistent with the requirements of the nulling identity. To develop the signal equivalent to the $\sin \theta \cos \psi$ term of the identity, a single switch from the S1 through S4 group of switches will be closed to select either the in phase or out of phase $\sin \theta$ signal and connect it to an attenuator resistor circuit representing either $\cos 22.5$ degrees or $\cos 67.5$ degrees. The $\cos \theta \sin \psi$ signal is developed in the same manner by a single switch in the S5 through S8 group. The transformer outputs selected in each case will cause the $\sin \theta \cos \psi$ and the $\cos \theta \sin \psi$ signals to be out of phase with respect to each other at

the summing junction. When the attenuated signals are summed together at the summing junction, a difference or resultant voltage is developed which represents the $\sin(\theta - \psi)$ side of the identity. The S1 through S8 switches can select values of ψ to match the gimbal angle to within 22.5 degrees. The resultant voltage, therefore, may be a maximum of (± 4 v rms) ($\sin 22.5^\circ = 1.53$ v (rms)).

The resultant voltage can be nulled out by summing it with voltage increments of proper phase supplied by the voltage ladder formed by switches S10, S11, and S12. The ladder, in effect, performs a linear interpolation to match the difference angle $(\theta - \psi)$ to within 2.8 degrees in steps of 2.8 degrees. The ladder switches are activated by switch control signals from the 2^9 , 2^{10} , and 2^{11} stages of the read counter. The signal input to the ladder switches is from the out of phase secondary of the 800 cps reference transformer T3. The remaining switch, S9, is controlled by the 2^{12} stage of the read counter and supplies an in phase reference signal to the summing junction. The operation of the S9 switch will be discussed in more detail later.

The coarse system switches activated at any particular gimbal angle can be determined by first determining what read counter stages will have accumulated bits (see figure 4-9) and applying this information to the logic equations given in figure 4-12 to determine what switch control signals will be generated. A simpler more convenient method is provided by the coarse switching diagram given in figure 4-13. The coarse switching diagram illustrates the range of gimbal angles over which each switch is closed. The S and C designations indicate a sine and cosine attenuator resistor, respectively, with the value of the attenuator resistor given after the designator. The plus and minus signs signify the polarity of the transformer secondary that the attenuator resistor is connected to. The R designation indicates the closure of switch S9. The L designation indicates the closure of one or more of the ladder switches.

A gimbal angle which illustrates the operation of switches S1 through S8 is 67.5 degrees. A gimbal angle of 67.5 ($45 + 22.5$) degrees places a bit in read counter stages 2^{12} and 2^{13} (see figure 4-9) and satisfies the logic equations for DC4 and DC6 (see figure 4-12), which close switches S4 and S6. The coarse switching diagram verifies the closure of a +C67.5 and a -S67.5 switch which correspond to switches S4 and S6. The voltages present at the summing junction as a result of the closure of switches S4 and S6 are:

$$\begin{aligned} (S4) \quad & (4 \text{ v rms}) (\sin 67.5^\circ) (\cos 67.5^\circ) = \\ & (4 \text{ v rms}) (0.924) (0.383) = 1.42 \text{ v (rms)} \end{aligned}$$

$$\begin{aligned} (S6) \quad & (-4 \text{ v rms}) (\cos 67.5^\circ) (\sin 67.5^\circ) = \\ & (-4 \text{ v rms}) (0.383) (0.924) = -1.42 \text{ v (rms)}. \end{aligned}$$

The two voltages are equal in amplitude but opposite in phase and therefore cancel, producing a null.

A gimbal angle which illustrates the use of the ladder is 28.1 degrees. A gimbal angle of 28.1 (22.5 + 5.6) degrees places a bit in read counter stages 2^{12} and 2^{10} satisfying the logic equations for DC3, DC5, and DC11 which close switches S3, S5, and ladder switch S11, respectively. The coarse switching diagram verifies that switch S3 (+ cos 22.5°), S5 (-sin 22.5°), and the ladder are actuated. The voltages present at the summing junction as a result of the closure of switches S3 and S5 are:

$$(S3) \quad (4 \text{ v rms}) (\sin 28.1^\circ) (\cos 22.5^\circ) = \\ (4 \text{ v rms}) (0.471) (0.924) = 1.74 \text{ v (rms)}$$

$$(S5) \quad (-4 \text{ v rms}) (\cos 28.1^\circ) (\sin 22.5^\circ) = \\ (-4 \text{ v rms}) (0.882) (0.383) = -1.35 \text{ v (rms).}$$

The resulting in phase voltage from the S3 and S5 closure is 0.39 v (rms). To null the system this in phase voltage must be summed with an out of phase signal. With ladder switch S11 closed an out of phase voltage equivalent to $(-4 \text{ v rms}) (\sin 5.62) = -0.39 \text{ v (rms)}$ is applied to the summing junction to establish a null.

When the resultant signal at the summing junction (S1 through S8 switch closures) is an out of phase voltage, operation of the ladder switches will affect the out of null condition. An in phase signal is required at the summing junction with which the ladder signals can be summed to obtain a null. This required in phase signal is provided by switch S9 and the + reference side of transformer T3 as shown in figure 4-10. Switch S9 is activated on alternate 22.5 degree segments, as shown on the coarse switching diagram, because it is in those segments that switches S1 through S8 can produce an out of phase resultant. Switch S9 provides a signal equivalent to $(4 \text{ v rms}) (\sin 22.5^\circ) = 1.53 \text{ v (rms)}$ which, in effect, inverts the out of phase resultant to an in phase signal so that the out of phase ladder signals can accomplish a null. Expressing the function of switch S9 in another way would be to say that it creates the effect of a 22.5 degree shift in gimbal angle.

A gimbal angle which would illustrate the use of switch S9 as well as the ladder is 239.1 degrees. A gimbal angle of 239.1 (180 + 45 + 11.25 + 2.8 = 239.05) degrees places a bit in read counter stages 2^{15} , 2^{13} , 2^{11} , and 2^9 . Bits in these positions satisfy the logic equations for DC2, DC8, DC10 and DC12, closing switches S2, S8, S10 and S12. The absence of a bit in read counter stage 2^{12} satisfies the logic equation for DC9 which closes switch S9. The sine and cosine of 239.1 degrees are both negative since the angle lies in the third quadrant. The voltages present at the summing junction as a result of switches S2 and S8 being closed are:

$$(S2) \quad (-4 \text{ v rms}) (-\sin 239.1^\circ) (\cos 67.5^\circ) = \\ (-4 \text{ v rms}) (-0.8581) (0.383) = 1.35 \text{ v (rms)}$$

$$(S8) \quad (4 \text{ v rms}) (-\cos 239.1^\circ) (\sin 67.5^\circ) = \\ (4 \text{ v rms}) (-0.5135) (0.924) = -1.90 \text{ v (rms).}$$

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

The resultant out of phase voltage from the S2 and S8 closure is -0.55 v (rms). Summing this voltage with the out of phase voltages from the ladder switches (S10 and S12) will increase the out of phase resultant at the summing function. The closure of switch S9, however, provides the necessary in phase voltage value to obtain a null. Summing the in phase S9 voltage with the out of phase resultant provides a new resultant of $1.53 - 0.55 = 0.98$ v (rms). The voltages present as a result of the S10 and S12 closures are:

$$\begin{aligned} \text{(S10)} \quad & (-4 \text{ v rms}) (\sin 11.25^\circ) = \\ & (-4 \text{ v rms}) (0.195) = -0.78 \text{ v (rms)} \end{aligned}$$

$$\begin{aligned} \text{(S12)} \quad & (-4 \text{ v rms}) (\sin 2.8^\circ) = \\ & (-4 \text{ v rms}) (0.049) = -0.20 \text{ v (rms)}. \end{aligned}$$

Summing the total ladder signal with the S2, S8 and S9 resultant ($0.98 - 0.98 = 0$ v rms) establishes a null.

In order for the system to be nulled the voltage at the summing junction of amplifier A1 must be low enough to keep the amplifier output ($E_{\text{out}} = E_{\text{in}} \times \text{gain}$) below the triggering level of the schmitt trigger error detector. The amplifier output is referred to as the coarse error signal. When the system is not nulled, the coarse error is large enough (1.58 volts peak-peak nominal) to cause the error detector to fire and to generate an 800 cps square wave output. The 800 cps output, referred to as the coarse ternary level signal (C_1), is sent to the read counter logic section of the error counter and logic module. The coarse ternary level will exist when the error ($\theta - \psi$) is greater than approximately 7 degrees. The logic within the error counter and logic module sends pulses at 12.8 kpps to count the read counter up or down. If the coarse ternary level signal is out of phase with respect to an 800 cps square wave reference signal in the logic, the logic causes the read counter to be counted up and if the coarse ternary level signal is in phase, the read counter is counted down. The read counter in turn will change the configuration of the coarse system switches, choosing different attenuation values ($\sin \psi$ and $\cos \psi$) until $\theta - \psi = 0$ and the system is nulled. The coarse error signal is also supplied to the mode module fail detect circuits where it is monitored internally and to the CDU test point connector for external monitoring. The coarse system module also performs two additional functions: generates the ambiguity detect signal (A_d) and the IMU cage signal. The IMU cage signal is taken from a separate secondary winding of the $\sin \theta$ transformer, T3, and is used during the IMU cage mode to drive the gimbals to their zero positions. To develop the ambiguity detect signal, the output of a separate secondary winding of the $\cos \theta$ transformer, T2, is applied through an emitter follower to a schmitt trigger which fires when its input exceeds a nominal value of approximately 12.25 volts peak-to-peak. The schmitt trigger output is an 800 cps square wave, which exists when the gimbal angle is between 125 and 235 degrees. The ambiguity detect signal is sent to the ambiguity logic circuit in the digital mode module to prevent the CDU from nulling at an ambiguous angle.

4-4.2 QUADRANT SELECTOR MODULE. The quadrant selector module functions with the MSA&QR and with the read counter module to form the fine analog to digital conversion system. The quadrant selector module inverts the 16X or 64X resolver sine or cosine signals as necessary, depending on the quadrant the resolver angle lies in, so that they are always out of phase with respect to each other. A second function of the quadrant selector module is the generation of an 800 cps reference signal.

In order to implement the nulling identity $\pm \sin(\theta - \psi) = \pm \sin \theta \cos \psi \mp \cos \theta \sin \psi$ for the fine analog to digital conversion system, the $\sin \theta$ and $\cos \theta$ signals from the 16X or 64X angle resolver must be switched so that they are always out of phase with respect to each other. Figure 4-11 shows that the resolver signals are out of phase with each other only in quadrants II and IV. The quadrant selector inverts the $\sin \theta$ signal in quadrants I and IV, and the $\cos \theta$ signal in quadrants III and IV. Figure 4-14 is a block diagram of the quadrant selector module. The switch driver circuits and associated switch control signals which operate the various quadrant selector switches are not shown.

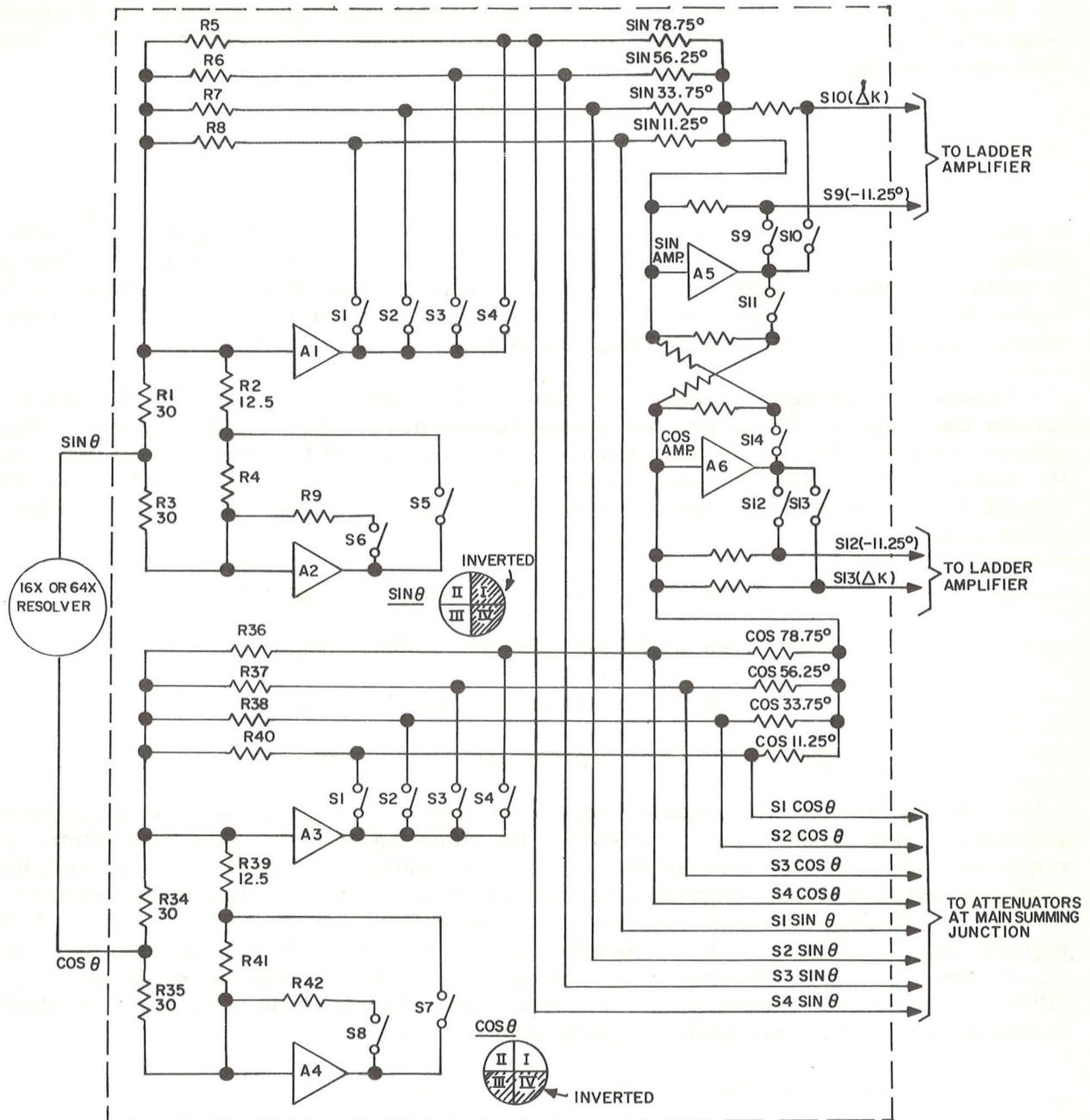
The inversion of the $\sin \theta$ signal is accomplished by operational amplifiers A1 and A2 and switches S5 and S6 in the following manner. Switch S6 is closed and S5 is opened to provide a feedback path around A2 through R9 and to disconnect the output of A2 from the input of A1. The $\sin \theta$ signal, applied to A1 through R1, is inverted by the normal operation of A1 and the desired inverted $\sin \theta$ signal is made available at its output. When no inversion is required, the switch configuration is changed to S5 closed and S6 opened. The feedback path around A2 is closed through R4 and the output of A2, which is also inverted, is applied to the input of A1 through R2. Since the resistance of R2 is half that of the feedback resistor of A1, an inverted $\sin \theta$ signal of twice normal amplitude is applied to the summing junction input of A1. When this signal is summed with the in phase $\sin \theta$ signal from R1, the resultant is an inverted $\sin \theta$ signal of normal amplitude. The inverted $\sin \theta$ signal is again inverted by A1 to re-establish an in phase $\sin \theta$ signal at its output.

Switches S5 and S6 are closed when the following logic equations are satisfied:

$$S5 = 2^{10} \overline{2^{11}} + \overline{2^{10}} 2^{11}$$

$$S6 = 2^{10} 2^{11} + \overline{2^{10}} \overline{2^{11}}$$

The 2^{11} stage of the read counter corresponds to 180 electrical degrees and the 2^{10} stage corresponds to 90 electrical degrees in the fine system. The logic equations then state that S5 is closed when the angle ψ is between 90 and 180 degrees ($2^{10} \overline{2^{11}}$) or between 180 and 270 degrees ($\overline{2^{10}} 2^{11}$) which are the II and III quadrants, respectively. S6 is closed when ψ is between 270 and 360 degrees ($2^{10} 2^{11}$) or between 0 and 90 degrees ($\overline{2^{10}} \overline{2^{11}}$) which are the IV and I quadrants, respectively.



ALL UNSPECIFIED RESISTORS ARE 25K ALL VALUES ARE IN K Ω . REFERENCE DESIGNATIONS CORRESPOND TO SCHEMATIC 2010059.

18925

Figure 4-14. Quadrant Selector Module Block Diagram

Phasing of the $\cos \theta$ signal is performed in the same manner as the $\sin \theta$ signal using A^3 , A^4 , S7, and S8. The $\cos \theta$ signal is inverted in the III and IV quadrants. The logic equations for S7 and S8 are:

$$S7 = \overline{2^{11}}$$

$$S8 = 2^{11}$$

S8 will be closed and S7 will be open when ψ is between 180 and 360 degrees (2^{11}) providing an inverted $\cos \theta$ signal at the output of A^3 . S7 is closed and S8 is open when ψ is between 0 and 180 degrees (2^{11}) providing a non-inverted signal at the output of A^3 . Figure 4-15 illustrates which of the S5 through S8 group of switches are closed over the various segments of 360 electrical degrees of 16X or 64X resolver rotation.

Switches S1 through S4 select resistance values located in the MSA&QR which attenuate the properly phased sine and cosine signals at the inputs of the MSA&QR. The accumulation of bits in the twelve least significant stages of the read counter controls all switches in the fine system. At any angle one and only one switch of the four (S1 through S4) is on, selecting the appropriate value of attenuation. The values of attenuation selected by each switch is given below:

(S1) $\sin 11.25$ degrees and $\cos 11.25$ degrees

(S2) $\sin 33.75$ degrees and $\cos 33.75$ degrees

(S3) $\sin 56.25$ degrees and $\cos 56.25$ degrees

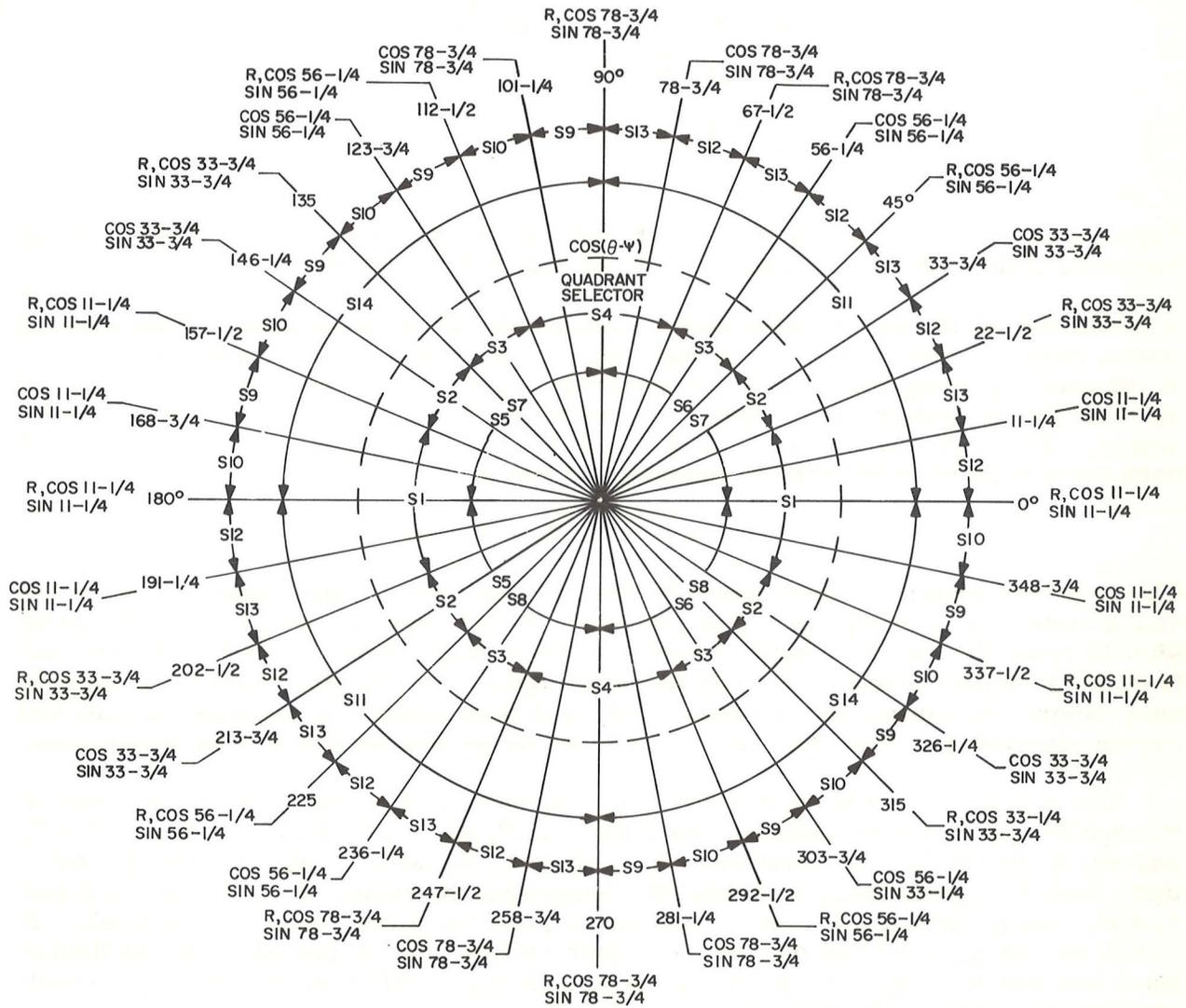
(S4) $\sin 78.75$ degrees and $\cos 78.75$ degrees.

If the resolver angle θ were equal to any of the exact values given above or quadrature multiples, a null would be accomplished at the summing junction of the main summing amplifier in the MSA&QR without the benefit of any additional signals. As an example, assume an angle of 213.75 degrees (equivalent to 33.75 degrees) exists at the resolver. The $\sin 213.75$ degrees signal is a negative quantity (out of phase) as is the $\cos 213.75$ degrees signal. The sine is not inverted in quadrant III and therefore remains as an out of phase voltage. The cosine is inverted in quadrant III and the out of phase $\cos 213.75$ degree signal becomes an in phase voltage. At this value of θ , switch S2 shall be closed, the result at the main summing junction shall be:

$$(\sin 213.75^\circ) (\cos 33.75^\circ) - (\cos 213.75^\circ) (\sin 33.75^\circ) = 0,$$

and the desired null shall be accomplished. If the resolver angle is not equal to any of the attenuation values or their quadrature multiples, the required attenuation cannot be accomplished by switches S1 through S4 alone. Additional switching is then performed in the MSA&QR module ladder circuits.

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM



16182A

Figure 4-15. Fine Switching Diagram

The logic equations mechanized to control the operation of switches S1 through S4 are as follows:

$$\begin{aligned}
 S1 &= 2^8 2^9 2^{10} + \overline{2^8} \overline{2^9} \overline{2^{10}} \\
 S2 &= \overline{2^8} 2^9 2^{10} + 2^8 \overline{2^9} \overline{2^{10}} \\
 S3 &= 2^8 \overline{2^9} 2^{10} + \overline{2^8} 2^9 \overline{2^{10}} \\
 S4 &= \overline{2^8} \overline{2^9} 2^{10} + 2^8 2^9 \overline{2^{10}}.
 \end{aligned}$$

Figure 4-15 illustrates which of the S1 through S4 switches are closed over the various segments of 360 electrical degrees of 16X or 64X resolver rotation.

Switches S1 through S4 also select attenuation values at the inputs of the sine and cosine amplifiers for use in generating an 800 cps reference signal. In obtaining a null at the main summing amplifier it is necessary to supply a reference signal to the ladder network that is in phase with respect to the external 800 cps reference input of the resolver. This reference is equivalent to $\cos(\theta - \psi)$ and is generated in the quadrant selector module by solving the trigonometric identity:

$$\cos(\theta - \psi) = \sin \theta \sin \psi + \cos \theta \cos \psi.$$

The reference identity is mechanized by the sine amplifier A5, the cosine amplifier A6, and switches S9 through S14. The reference identity implies that the sine and cosine signals from the resolver must always be in phase with respect to each other, in contrast to the nulling identity which required the signals to be out of phase with respect to each other. In solving the reference identity it is necessary to re-phase the sine and cosine signals so that they are always in phase and consistent with the equation.

The inputs to the sine amplifier are the attenuated $\sin \theta$ signals from switches S1 through S4, the values of which are $\sin \theta \sin 11.25^\circ$, $\sin \theta \sin 33.75^\circ$, $\sin \theta \sin 56.25^\circ$, and $\sin \theta \sin 78.75^\circ$, respectively. The inputs to the cosine amplifier are the attenuated $\cos \theta$ signals from switches S1 through S4, the values of which are $\cos \theta \cos 11.25^\circ$, $\cos \theta \cos 33.75^\circ$, $\cos \theta \cos 56.25^\circ$, and $\cos \theta \cos 78.75^\circ$, respectively. It should be remembered that only one of the four switches can be closed at any particular time and that the sine and cosine signals are always out of phase with respect to each other at the inputs to the sine and cosine amplifier.

The sine and cosine amplifiers each have two outputs which may be switched to the ladder amplifier in the MSA&QR but the switching logic allows the selection of only one of the four outputs at any particular time. Switch S11 switches the output of the sine amplifier to the input of the cosine amplifier and switch S14 switches the output of the cosine amplifier to the input of the sine amplifier. Switches S11 and S14 will never be closed at the same time. Switch S11 is closed when the angle θ is in quadrant I or III;

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

switch S14 is closed when the angle θ is in quadrant II or IV. Both the sine and cosine amplifiers invert their input signals. The effect is to have one amplifier invert the S1 through S4 input signal that is out of phase with respect to the external 800 cps reference, sum it with the in phase S1 through S4 signal and invert the resultant signal to an out of phase signal at the output of the second amplifier. Switches S9 and S10 switch the sine amplifier outputs to the ladder amplifier and switches S12 and S13 switch the cosine amplifier outputs to the ladder amplifier. Switches S9 and S10 alternate on and off every 11.25 degrees in the second and fourth quadrants (at which time S14 is closed) and switches S12 and S13 alternate on and off in the first and third quadrants (at which time S11 is closed). One output, therefore, is always present at the input to the ladder amplifier. The output signal switched to the ladder amplifier is always out of phase with respect to the external reference and when it is inverted by the ladder amplifier it becomes the in phase $\cos(\theta - \psi)$ reference signal required at the ladder network. The $\cos(\theta - \psi)$ signal is of a nearly constant amplitude for all inputs to the $\cos(\theta - \psi)$ generator circuit.

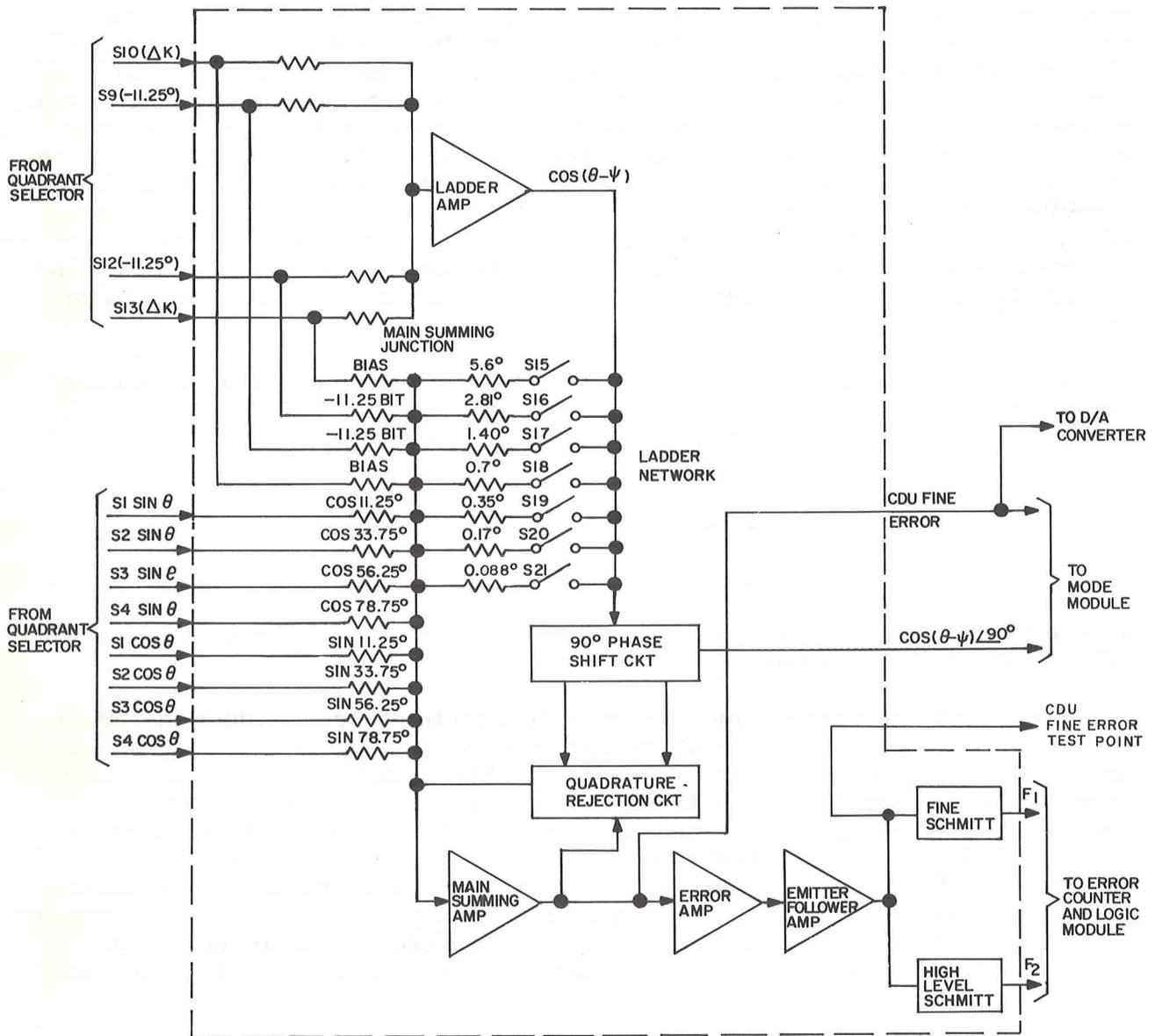
The logic equations mechanized to control the switching in the $\cos(\theta - \psi)$ generator are as follows:

$$\begin{aligned} S9 &= \overline{2^7} 2^{10} & S12 &= \overline{2^7} \overline{2^{10}} \\ S10 &= 2^7 2^{10} & S13 &= 2^7 \overline{2^{10}} \\ S11 &= \overline{2^{10}} & S14 &= 2^{10} \end{aligned}$$

Figure 4-15 illustrates the operation of these switches through 360 electrical degrees of 16X or 64X resolver rotation.

The switches that connect the sine or cosine amplifier outputs to the ladder amplifier also connect these outputs to attenuator resistors at the main summing junction of the main summing amplifier to establish either a bias signal or an out of phase reference signal corresponding to -11.25 degrees at the junction. Switches S9 and S12 provide inputs to the -11.25 degree attenuator resistor. This signal, which is referred to as the -11.25 degree bit, performs a function similar to that performed by the signal from switch S9 in the coarse module. Switches S10 and S13 provide inputs to the bias attenuator. The bias signal, also referred to as a ΔK signal, is applied to the summing junction minimizing any error generated by implementation of the $\cos(\theta - \psi)$ equation. Both the -11.25 degree bit and the bias signal are further discussed in the MSA&QR discussion.

4-4.3 MAIN SUMMING AMPLIFIER AND QUADRATURE REJECTION MODULE. The MSA&QR functions with the quadrant selector module and the read counter module to form the fine analog to digital conversion system. The MSA&QR performs four functions: summing, quadrature rejection, and generation of the F_1 and F_2 ternary level signals and generation of $\cos(\theta - \psi)$. A block diagram of the MSA&QR is given in figure 4-16.



16189B

Figure 4-16. Main Summing Amplifier and Quadrature Rejection Module, Block Diagram

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

In the summing operation the signals from the quadrant selector are summed at the main summing junction with the output of the ladder network and the output of the quadrature rejection circuit. The signals from the quadrant selector module (two signals supplied through the operation of switches S1 through S4) are always out of phase with respect to each other and either the -11.25 degree bit signal or the bias signal from amplifiers A5 or A6. Both the -11.25 degree bit signal and the bias signal are out of phase with respect to the 800 cps reference. If a gimbal angle θ exists that is not an exact multiple of 11.25 degrees, the main summing junction cannot be nulled by the operation of switches S1 through S4 alone. If this condition exists, an in phase signal from the ladder amplifier is supplied through switches S15 through S21 to null the signal at the main summing junction. Switches S15 through S21 are controlled by the accumulation of bits in the 2^0 through 2^6 stages of the read counter. The in phase signal from the ladder network is the $\cos(\theta - \psi)$ reference generated in the quadrant selector module and inverted by the ladder amplifier. The result of the summation of these signals, with the aid of the quadrature rejection circuit, is about a six millivolt rms null at the output of the main summing amplifier.

To illustrate the summing operation, assume that the angle registered by the read counter (ψ) is between 0 and 11.25 electrical degrees. Since the angle lies in the first quadrant, the in phase and relatively small $\sin \theta$ signal is inverted by the quadrant selector and is attenuated by a factor equivalent to $\cos 11.25$ degrees at the main summing junction. The in phase and relatively large $\cos \theta$ signal is attenuated by a factor equivalent to $\sin 11.25$ degrees at the main summing junction. The resultant voltage of these two signals from the quadrant selector is an in phase voltage which must be summed with an out of phase voltage to obtain a null. If the in phase voltage from the ladder switches were summed with the in phase resultant from the quadrant selector signals, the in phase resultant would be increased, affecting the out of null condition. The out of phase voltage necessary to accomplish a null is provided by the -11.25 degree bit signal. The effect of this signal is to invert the resultant from the quadrant selector signals to an out of phase voltage which may be nulled out with increments of in phase voltage from the ladder. The -11.25 degree bit signal performs the same function as the S9 reference signal in the coarse system module.

If ψ is between 11.25 and 22.50 electrical degrees, quadrant selector switch S12 is open and S13 is closed which removes the -11.25 degree bit signal and applies the bias signal to the summing junction. The resultant voltage of the quadrant selector signals will always be an out of phase voltage. The in phase voltage increments from the ladder switches null out the out of phase resultant and the bias signal minimizes errors.

The bias signal minimizes errors incurred in the implementation of the $\cos(\theta - \psi)$ equation. During those times that the -11.25 degree bit signal is switched in and the bias signal is absent, a similar bias is provided through the gain of the ladder amplifier.

As the angle ψ becomes greater, the operation described repeats the S12 and S13 alternating on and off every 11.25 degrees. In the second quadrant the operation continues with switches S9 and S10 alternating on and off. In the third quadrant switches S12 and S13 again are operational and in the fourth quadrant S9 and S10 regain control.

The resolver signals contain a certain percentage of quadrature (reactive) component which, if large enough, could cause the fine schmitt trigger error detector to fire. To eliminate this possibility, a quadrature reject circuit is incorporated into the MSA&QR. The quadrature component is rejected by taking the $\cos(\theta - \psi)$ output of the ladder amplifier and shifting it 90 degrees in phase to obtain a $\cos(\theta - \psi) \angle 90^\circ$ signal which is used as a reference for a phase sensitive demodulator and a modulator (chopper). The 800 cps output of the main summing amplifier is sampled, amplified, and applied to the phase sensitive demodulator. If the main summing amplifier output contains any quadrature component the output will be demodulated and charge a capacitor in a filter circuit. If the output of the main summing amplifier is an out of phase voltage, the dc charge on the capacitor will be negative. If the output of the main summing amplifier is an in phase voltage, the dc charge on the capacitor will be positive.

The dc charge on the capacitor is applied as an input to the chopper which is keyed by the $\cos(\theta - \psi) \angle 90^\circ$ signal. The modulated output from the chopper is 180 degrees out of phase with respect to the quadrature component. The chopper output is amplified and applied to the main summing junction where it tends to buck any quadrature component present. The $\cos(\theta - \psi) \angle 90^\circ$ signal is also sent to the fail detect circuits in the mode module for internal monitoring purposes. In the trunnion loop $\cos(\theta - \psi) \angle 90^\circ$ is sent to the trunnion interrogator generator.

The main summing amplifier output is applied to an error amplifier. The output of the error amplifier is applied to two schmitt triggers. One schmitt trigger generates an 800 cps square wave output, referred to as the high ternary level signal F_2 , which is applied to the read counter logic section of the error counter and logic module causing the read counter to be incremented at a high rate (12.8 kpps). The second schmitt trigger generates an 800 cps square wave output, referred to as the fine ternary level signal F_1 , which causes the read counter to be incremented at a low rate (800 pps). The high level schmitt trigger will fire whenever the error amplifier output is greater than 4 volts peak-peak nominal. When the read counter is within 20 bits (approximately 0.1 degrees) of reading the gimbal angle, the high level schmitt trigger ceases to fire and the fine schmitt trigger takes over to cause the read counter to be incremented at the low rate. As long as the error signal is large enough (1.5 to 2 bits or greater from null) to fire the fine schmitt trigger, the system will not be nulled and incrementing pulses will be sent to the read counter. The read counter will change the switching configuration to select different values of ψ until ψ is within two bits of equaling θ . When this match occurs, the output of the error amplifier will have been reduced to below the 200 millivolt peak-peak nominal triggering level of the fine schmitt trigger and the system will be nulled.

The output of the main summing amplifier is referred to as the fine error signal and is equivalent to $\sin 16(\theta - \psi)$ or $\sin 64(\theta - \psi)$. This signal is applied to the fail detect circuits in the mode module for internal monitoring purposes. For ISS it is sent to the D/A converter module where it is used as a gimbal rate limiting signal during the ISS coarse align and turnon modes of operation. For OSS trunnion applications, the signal is phase shifted and sent to the interrogate module to key a square wave generator. The fine error signal is also amplified, buffered, and routed to a test point on the CDU test connector for external monitoring purposes.

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

4-4.4 DIGITAL MODE MODULE. The digital mode module generates timing and interrogate pulses that are used throughout the CDU for synchronization, switching, and strobing. The digital mode module also contains circuitry for synchronizing incoming CMC moding discrettes with CDU internal timing and circuitry to prevent an ambiguous gimbal position indication. Types of logic circuits in the digital mode module are the clock and decoder logic, the countdown logic, a 25.6 pps generator, interrogate pulse generators, moding sync logic, and ambiguity logic.

4-4.4.1 Basic Counter and Storage Operation. CDU storage and counting are accomplished by NOR gate flip-flops. The basic flip-flop shown in figure 4-16A(a) is set or reset by positive going pulses. Figure 4-16A(b) shows how information (A and \bar{A}) is transferred into a flip-flop by gating with a negative going pulse. The information may also be transferred from another flip-flop as shown in figure 4-16A(c). In this case the state of flip-flop \bar{B} is transferred into flip-flop A by the gate pulse. If flip-flop B is alternately set to \bar{A} , and flip-flop A is alternately set to B, flip-flop A changes state at each gate pulse. Figure 4-16A(d) shows two gated flip-flops cross-connected to do this. The gate pulses are not coincident in time, so only one flip-flop changes state at a time. The gate pulses are also called clock pulses, and, since they occur at two different times, they may be referred to as a two phase clock. (The CDU uses a four phase clock.) The circuit of figure 4-16A(d) is also called a master/slave arrangement since one flip-flop controls the other. Note that the SET A clock pulse always changes the state of flip-flop A. The circuit of figure 4-16A(d) can therefore be used as a toggle flip-flop or binary counter state.

The negative going gate pulses shown in figure 4-16A(e) are not coincident in time, so they can also be used to operate the circuit shown in figure 4-16A(d). The pulse trains were derived from a single clock pulse input since SET B is simply SET A inverted. Figure 4-16A(f) shows a master/slave flip-flop operated by a single clock pulse input. In this case the SET B gate pulse input is inverted to produce gating pulses for flip-flop A. The connections marked W merely insure that there is no time overlap between the two gating signals due to differences in NOR gate delay. This type of binary counter is used in the digital mode module to generate the CDU clock phases.

Additional clock phases may be used to reduce the number of gates required to make a binary counter. The gate marked with an asterisk in figure 4-16A(d) was removed to make the binary counter shown in figure 4-16A(g). Phase 1 ($\emptyset 1$) resets flip-flop B. Phase 2 ($\emptyset 2$) sets $B = \bar{A}$. Phase 3 ($\emptyset 3$) sets $A = B$. This type of binary counter is used to count down from 12.8 kpps to 800 pps in the digital mode module. Figure 4-16A(h) shows two binary counter stages connected for counting up. The dashed lines indicate the connections used for counting down. Figure 4-16A(i) shows an up-down counter stage. The counting direction is determined by the presence of either a high or low level signal at the inputs marked UP and DOWN. UP = DOWN. The UP and DOWN level signals may change state only at $\emptyset 2$ time, allowing the actual counting to take place at $\emptyset 4$ time. Gate 1 generates carry pulses to the next stage when counting up. Gate 2 generates carry pulses to the next stage when counting down. Gate 3 OR's the carry pulses and inverts them. This type of counter stage is used for the read and error angle counters.

4-4.4.2 Clock and Decoder Logic. The clock and decoder logic generates four individual, three microsecond pulse width, 12.8 kpps, timing pulse trains of different phases. The pulse trains are designated phase 1 through phase 4. The pulse trains are generated by dividing the 51.2 kpps clock pulse train from the CMC by four and ANDing appropriate signals. The pulse trains are used throughout the CDU for strobing and control. The clock and decoder logic and related timing diagrams are shown in figure 4-16B.

The clock contains a two stage binary counter. Stage A, driven by the 51.2 kpps clock pulse train, divides the driving signal by two to produce a 25.6 kpps square wave output signal. This signal is used to drive stage B and is also applied to the decoder logic. Stage B divides the frequency of its drive signal by two to produce a 12.8 kpps square wave output that is also applied to the decoder logic.

Signals A and B from the two clock stages produce the repetitive count 00, 01, 10, and 11. Signals A and B and their complements are applied to the decoder network together with the 51KPHI signal. These signals are also shown in the timing diagram. By ANDing appropriate clock output signals the decoder network produces a phase pulse for each of the four binary counts of the clock. The decoder produces a phase 1 pulse ($\emptyset 1$) when the clock is in state 00. Drive signals for the phase pulses $\emptyset 2$, $\emptyset 3$, and $\emptyset 4$ are produced for clock states 01, 10, and 11, respectively. To meet the loading requirements of the $\emptyset 2$, $\emptyset 2$, $\emptyset 3$, and $\emptyset 4$ pulse trains, pulse drivers employing conventional transistors are used. These pulse drivers are located in the mode module.

The four phase pulse trains each have a frequency of 12.8 kpps. The interval between $\emptyset 1$ pulses is approximately 80 microseconds, divided into four intervals by the $\emptyset 2$, $\emptyset 3$, and $\emptyset 4$ pulses. Each interval is, therefore, approximately 20 microseconds.

4-4.4.3 Countdown Circuit. The countdown circuit generates an 800 pps $\emptyset 4$ pulse train used in the read counter rate select logic circuit to develop the low rate of read counter incrementing pulses. The countdown circuit also generates a 6.4 kpps $\emptyset 4$ pulse train, used in place of the normal 12.8 kpps $\emptyset 4$ pulse train, during the coarse align mode to develop the high rate of read counter incrementing pulses. The detail logic diagram for the countdown circuit is shown in figure 4-16C.

The drive signal for the first stage is the 12.8 kpps $\emptyset 4$ pulse train. The frequency of this signal is divided by two in the first stage and the resulting 6.4 kpps signal is used to drive the second stage. The frequency of the 6.4 kpps signal is divided by two to produce the 3200 pps drive signal for the third stage, and so on until the final 800 pps signal is produced. In this manner the 12.8 kpps $\emptyset 4$ pulse train is divided by sixteen to produce an 800 pps $\emptyset 4$ pulse train.

Figure 4-16C also shows the phase 4 select logic circuit. This logic circuit provides $\emptyset 4$ synchronizing pulses (H) used in the read counter rate select logic to develop the high rate of read counter incrementing pulses. The presence of the coarse align enable discrete (CA) during the coarse align mode inhibits the 12.8 kpps $\emptyset 4$ pulse train and replaces it with the 6.4 kpps $\emptyset 4$ pulse train generated by the countdown circuit.

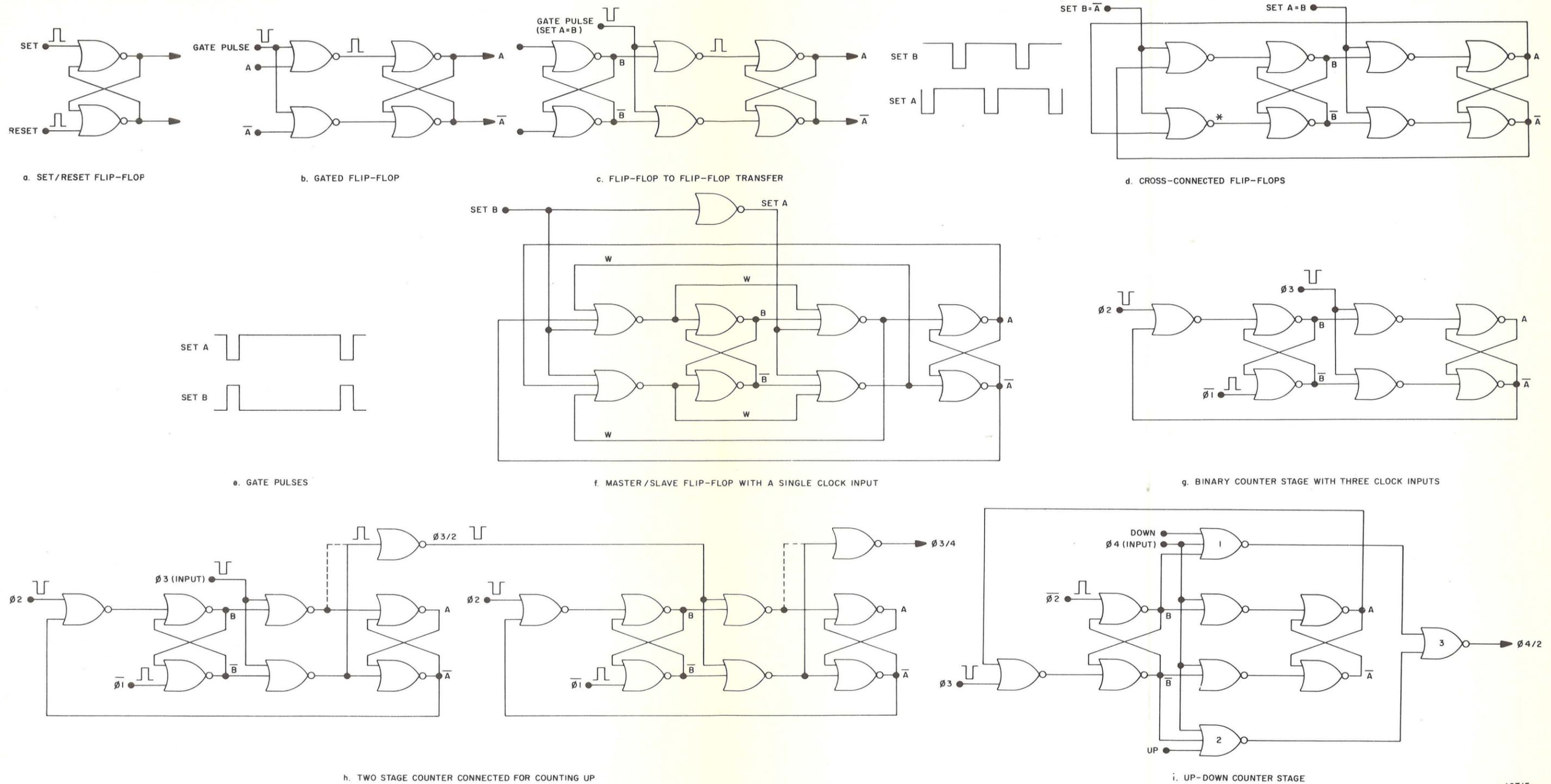
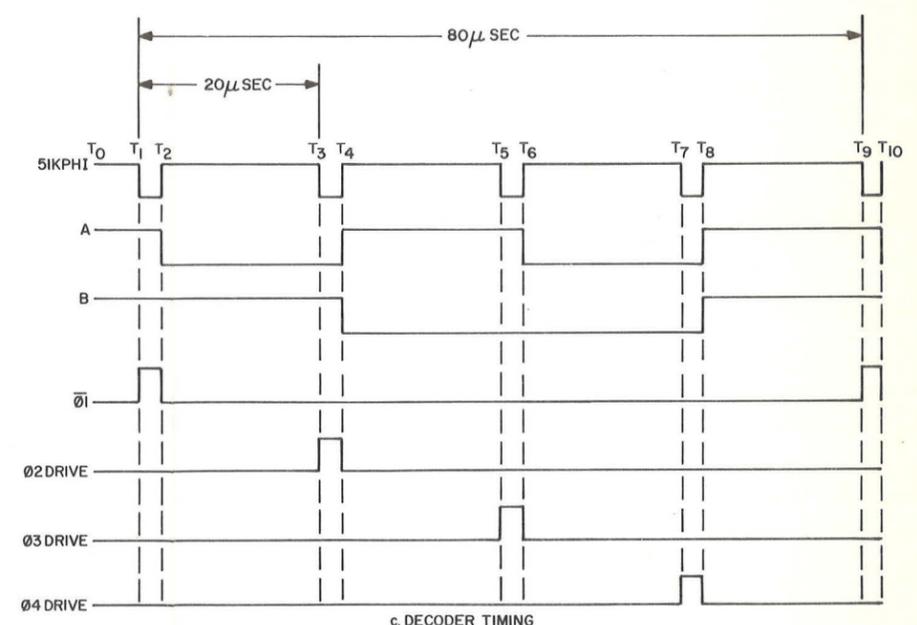
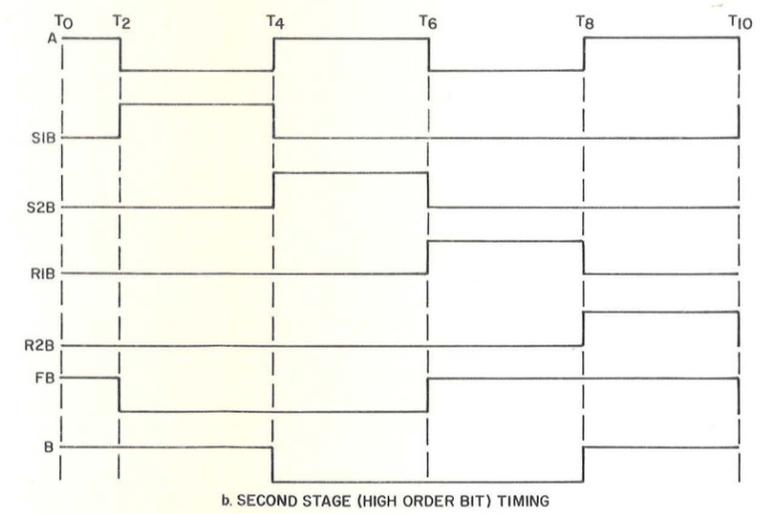
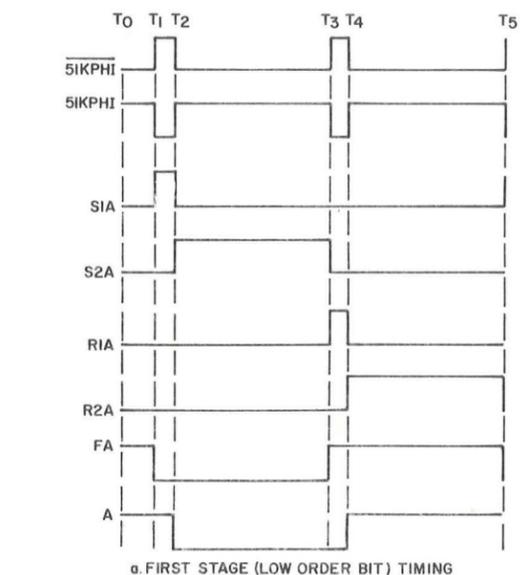
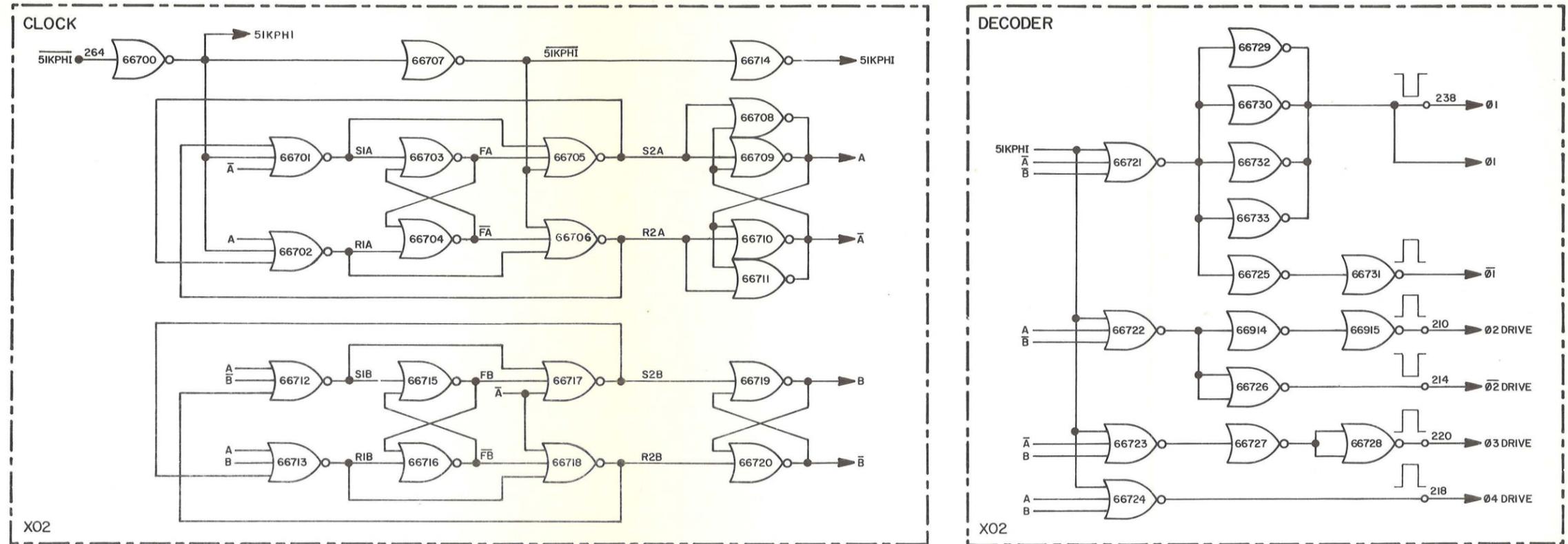
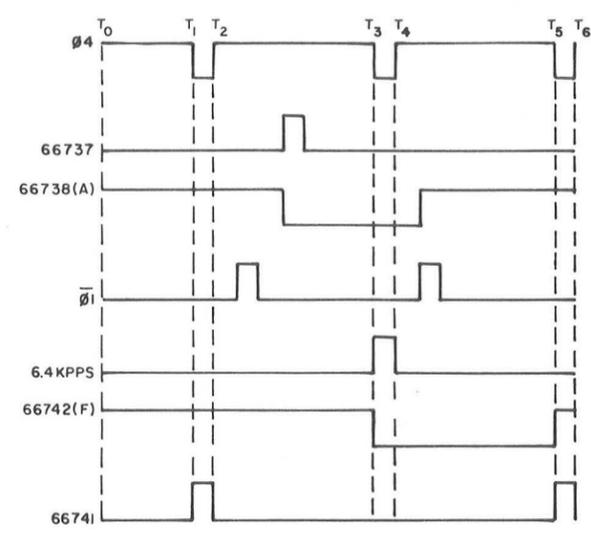
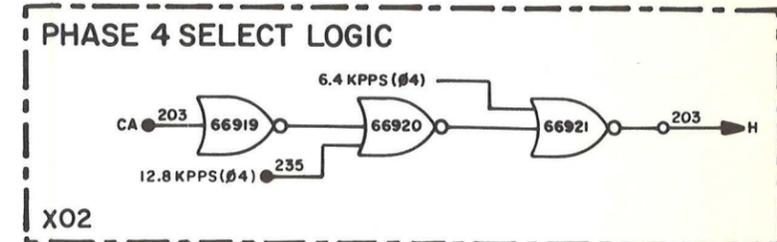
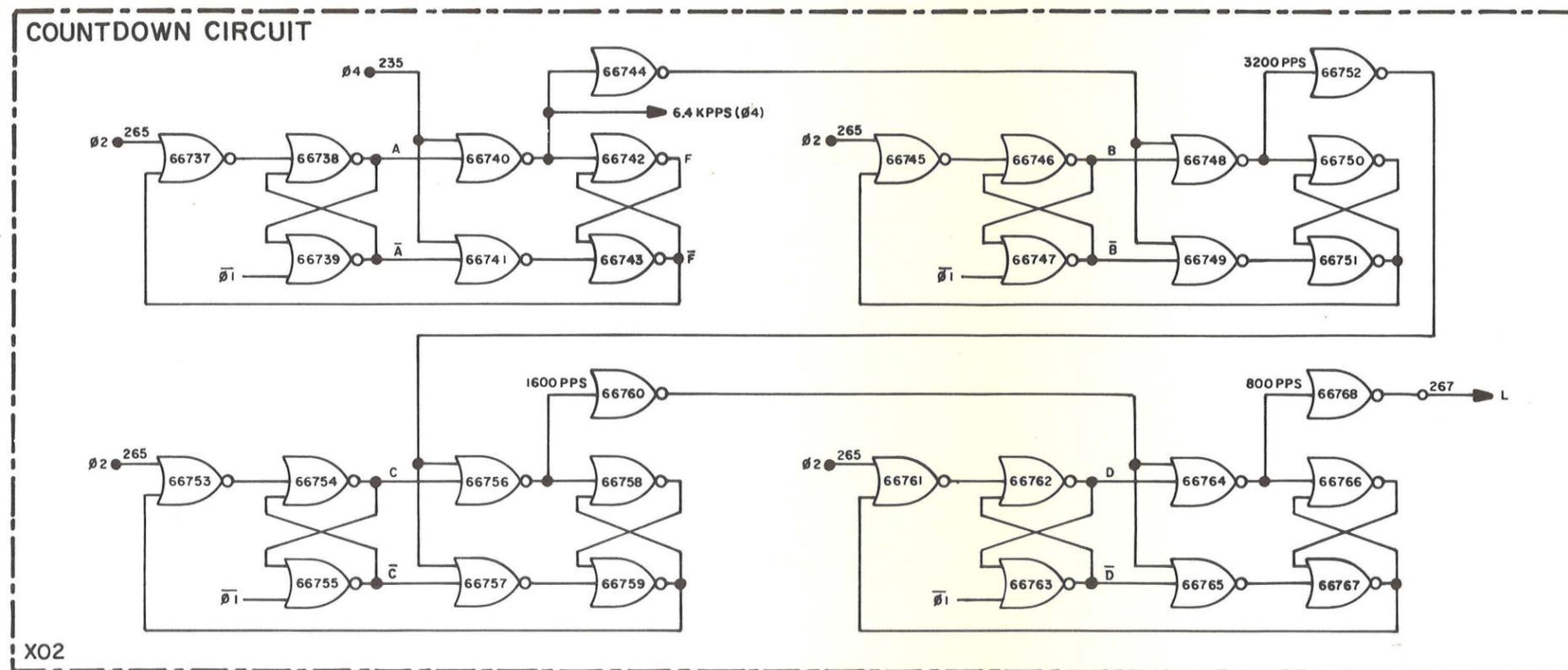


Figure 4-16A. Basic Storage and Counter Circuits, Logic Diagram

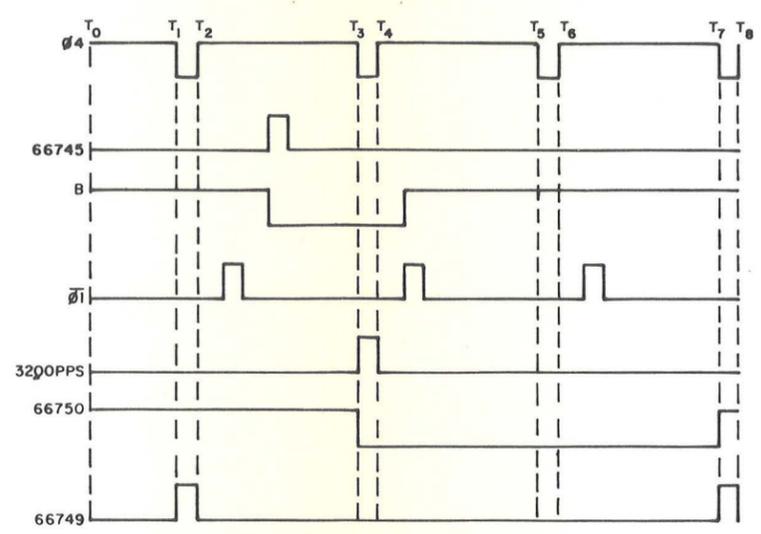


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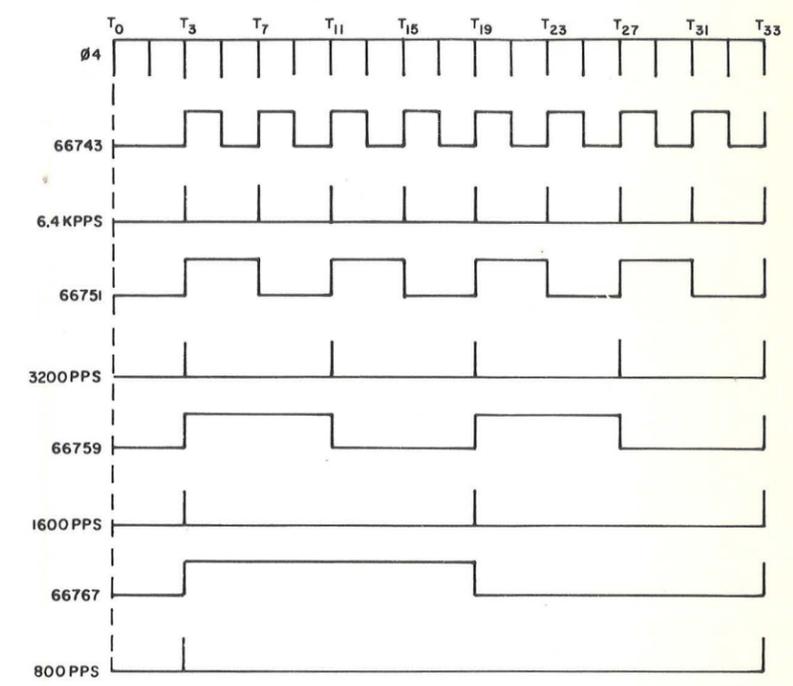
Figure 4-16B. Clock and Decoder Logic, Logic Diagram



a. FIRST STAGE TIMING



b. SECOND STAGE TIMING



c. COUNT DOWN TIMING

16333A

Figure 4-16C. Countdown Circuit, Logic Diagram

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

4-4.4.4 25.6 KPPS Generator. The 25.6 kpps generator (figure 4-16D) produces a 25.6 kpps pulse train used as the synchronization pulse input for the 4 VDC power supply module. The 4 VDC power supply requires a synchronization pulse input derived from the CMC. The only one that the CDU receives, however, is the 51.2 kpps clock pulse. A CMC controlled 25.6 kpps pulse train is therefore produced by ORing the 12.8 kpps $\phi 2$ and $\phi 4$ pulse trains (figure 4-16D). The $\phi 4$ pulse train is also supplied to the ISS I_2, I_3 generator.

4-4.4.5 I_2, I_3 Generators. The ISS I_2, I_3 interrogate generator is used to produce two additional pseudo interrogate pulses; one coincident with the $\phi 2$ timing pulse and the other coincident with the $\phi 3$ timing pulse. ISS interrogate pulses (I) can occur at any time with respect to the 51.2 kpps CMC clock pulses. A synchronization link between the ISS interrogate pulses and the CMC clock pulses is provided by generating two additional interrogate pulses, I_2 and I_3 , at the $\phi 2$ and $\phi 3$ times, respectively, after each occurrence of an I pulse. I_2 and I_3 are then used by other logic circuits for synchronization and control purposes.

The detail logic diagram and related timing diagram are shown in figure 4-16E. The ISS I_2, I_3 generator receives the 1600 pps ISS interrogate pulses from the ISS interrogate generator in the interrogate module and $\phi 2$ and $\phi 3$ from the phase buffers. The $\phi 1$ and $\phi 4$ timing pulses are received from other logic circuits within the digital mode module.

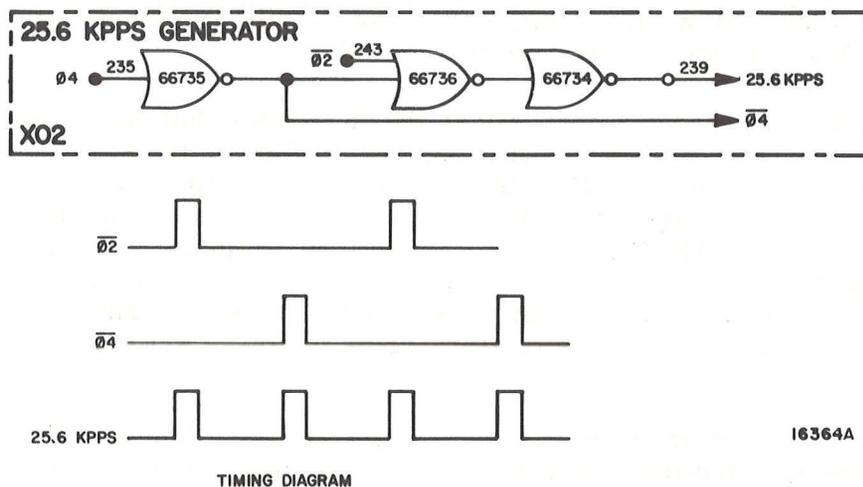


Figure 4-16D. 25.6 KPPS Generator

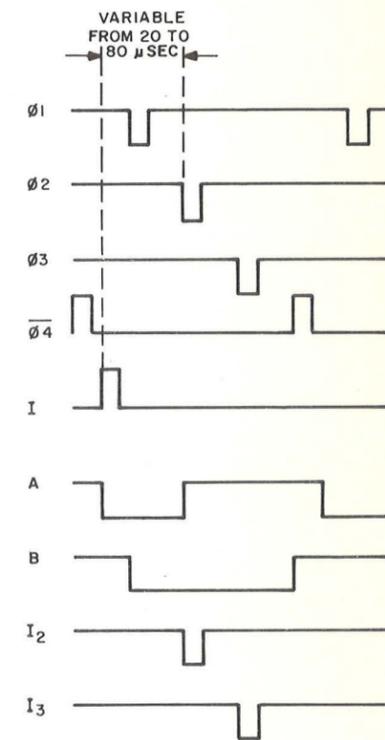
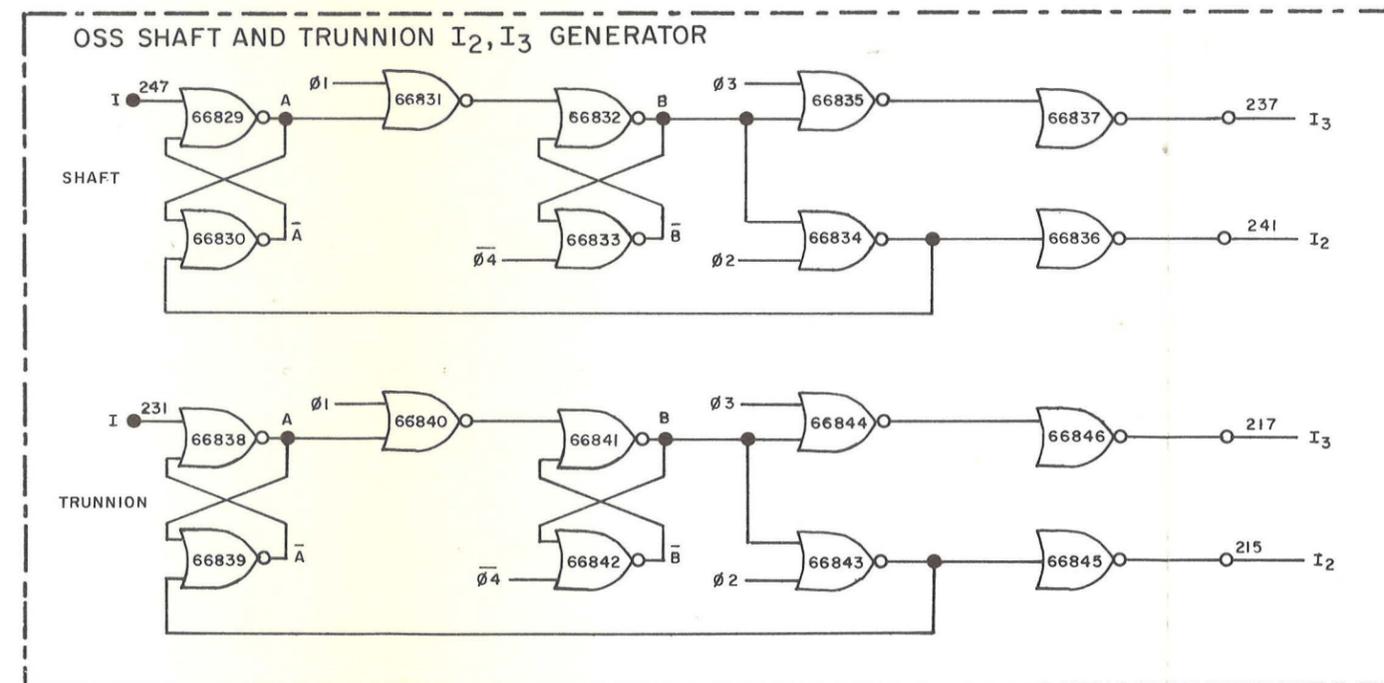
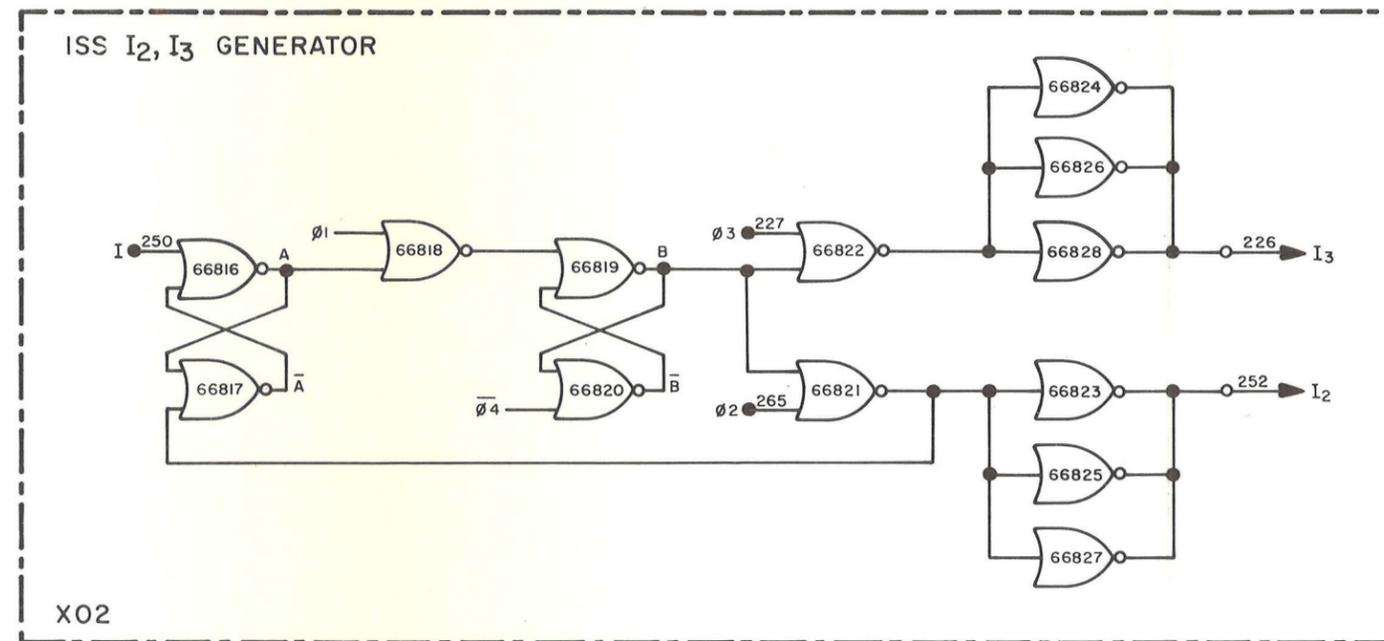
The ISS I_2 , I_3 generator contains two flip-flops. Flip-flop A is set by I and remains set until its content is propagated through flip-flop B and converted into I_2 . The content of flip-flop A is transferred to flip-flop B on the first ϕ_1 that occurs after receipt of I. The set output of flip-flop B is gated by ϕ_2 to produce I_2 and by ϕ_3 to produce I_3 . I_2 is fed back to reset flip-flop A which prepares it for the receipt of the next I. Depending on the delay between the receipt of I and the first occurrence of ϕ_1 , I_2 will follow I within approximately 20 to 80 microseconds. The pulse repetition frequency of I_2 and I_3 will be 1600 pps compared to the 12.8 kpps frequency of ϕ_2 and ϕ_3 . The ϕ_4 pulse following the generation of I_2 and I_3 resets flip-flop B, prohibiting the generation of another I_2 or I_3 until the next occurrence of I. The OSS I_2 , I_3 generator operates like the ISS I_2 , I_3 generator.

4-4.4.6 ISS Moding Sync Logic. The ISS moding sync logic synchronizes the ISS CDU zero, coarse align enable, and error counter enable moding discrettes from the CMC with CDU internal timing prior to their being used to control the ISS modes of operation. The three CMC discrettes when transmitted to the mode module are 0 vdc (CMC ground) and are random with respect to CDU internal timing. The moding buffers in the mode module provide high noise immunity between the CMC-CDU interface and convert the discrettes to logic levels.

The detailed logic diagram for the ISS moding sync logic circuit is shown in figure 4-16F. The circuit receives the enable error counter discrete ISSEEC, the coarse align enable discrete ISSCA, and the ISS CDU zero discrete ISSZ. ISSEEC and ISSCA are synchronized with ϕ_2 timing and supplied to the inner, middle, and outer error angle counter and logic modules. ISSZ is also synchronized with ϕ_2 timing but is returned to the moding buffers as the ISS CDU zero drive signal ISSZDR. ISSZDR is inverted again, amplified by the moding buffers, and supplied to the digital mode module, interrogate module, and the ISS read counter modules.

ISSEEC must be present during all of the ISS modes that employ the error counters. ISSEEC is inverted, ANDed with ϕ_2 , and applied to the set side of flip-flop A. Flip-flop A is reset when ISSEEC is removed. The output from the set side of the flip-flop is inverted and applied to three sets of pulse driver gates to produce enable error counter discrettes AE, BE, and CE, for the inner, middle, and outer gimbal error counters, respectively. The enable error counter discrettes begin coincidentally with the ϕ_2 timing pulse but end randomly with respect to CDU timing. The removal of the enable error counter discrete automatically causes the three error counters to be reset to zero.

ISSCA must be present during the entire ISS coarse align and IMU turnon modes. ISSCA is inverted, synchronized with ϕ_2 , and applied to the set side of the flip-flop (gages 66772 and 66773). The removal of ISSCA causes the flip-flop to be reset at the occurrence of the next ϕ_2 . The output from the reset side of the flip-flop is inverted to produce coarse align enable discrettes, ACA, BCA, and CCA, that are applied to the error angle counter and logic modules for the inner, middle, and outer gimbals, respectively. The coarse align enable discrettes begin and end coincidentally with ϕ_2 timing. An additional coarse align enable discrete DMMCA is produced for use within the digital mode module.



18926

Figure 4-16E. ISS And OSS I₂, I₃ Generators, Logic Diagram

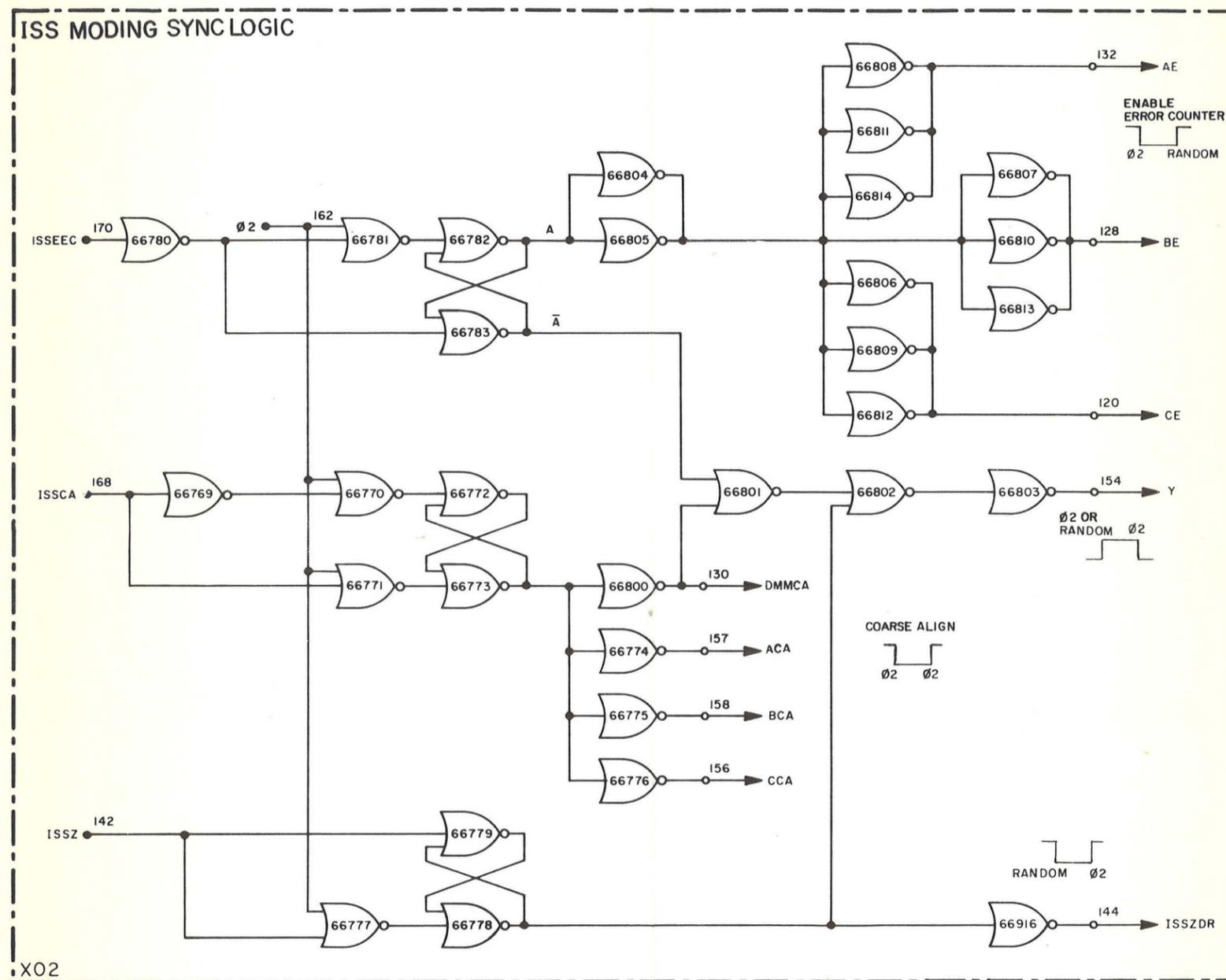


Figure 4-16F. ISS Moding Sync Logic, Logic Diagram

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

ISSZ is applied to the set side of the ISSZDR flip-flop (gates 66779 and 66778). The output from the reset side of the flip-flop is inverted to produce ISSZDR. ISSZDR drives the moding buffers in the mode module to produce the ISS CDU zero discrete (Z) used in the digital mode module, the interrogate module, and the ISS read counters. The ISSZDR flip-flop is reset coincidentally with $\emptyset 2$ after ISSZDR has been removed.

The inhibit read counter signal (Y) is produced during either of the following conditions: a) ISSCA is present and ISSEEC is not present, or b) ISSZ is present. Y is applied to the read counter rate select logic in the error angle counter and logic module where it prevents the generation of read counter incrementing pulses. The inhibit read counter signal begins at $\emptyset 2$ time or at random, depending on which input signals caused its generation, and ends at $\emptyset 2$ time.

4-4.4.7 OSS Moding Sync Logic. The OSS moding sync logic synchronizes the OSS CDU enable error counter, coarse align enable, the thrust vector control disable, and zero moding discrettes from the CMC with CDU internal timing prior to their being used to control the OSS modes of operation. The three CMC discrettes, when transmitted to the mode module, are 0 vdc (CMC ground) and are random with respect to CDU internal timing. The moding buffers in the mode module provide high noise immunity between the CMC-CDU interface and convert the discrettes to logic levels.

The detailed logic diagram for the OSS moding sync logic circuit is shown in figure 4-16G. The circuit receives the enable error counter discrete ODAE, the coarse align and thrust vector control disable discrete TVCDCA, the OSS coarse align enable discrete ECA, and the OSS CDU zero discrete OSSZ. ODAE and OSSZ are synchronized with $\emptyset 2$ timing and supplied to the shaft and trunnion error angle counter and logic modules.

The ODAE discrete must be present during all of the OSS modes that employ the error counters. ODAE is inverted, synchronized with $\emptyset 2$ timing, and applied to the set side of a flip-flop. The removal of ODAE causes the flip-flop to be reset at the next $\emptyset 2$ time. The output from the set side of the flip-flop is inverted and applied to pulse driver gates to produce enable error counter discrettes EEC and DEEC. The enable error counter discrettes begin coincidentally with $\emptyset 2$ timing and end with $\emptyset 2$ timing. The removal of the enable error counter discrete automatically causes the two error counters to be reset to zero.

The OSSZ is applied to the set side of the optics zero drive flip-flop. The output from the reset side of the flip-flop is inverted to produce OSSZDR. OSSZDR drives the moding buffers in the mode module to produce the OSS CDU zero discrete (Z) used in the digital mode module, the interrogate module, and the ISS read counters. The OSSZDR flip-flop is reset coincidentally with $\emptyset 2$ after OSSZDR has been removed.

The inhibit read counter signal OINHRC is produced during either of the following conditions: a) OSS coarse align and thrust vector control disable is present and OSSEEC is not present or b) OSSZ is present. OINHRC is applied to the read counter rate select logic in the error angle counter and logic module where it prevents the generation of read counter incrementing pulses. The inhibit read counter signal begins at $\emptyset 2$ time or at random, depending on which input signals caused its generation, and ends at $\emptyset 2$ time.

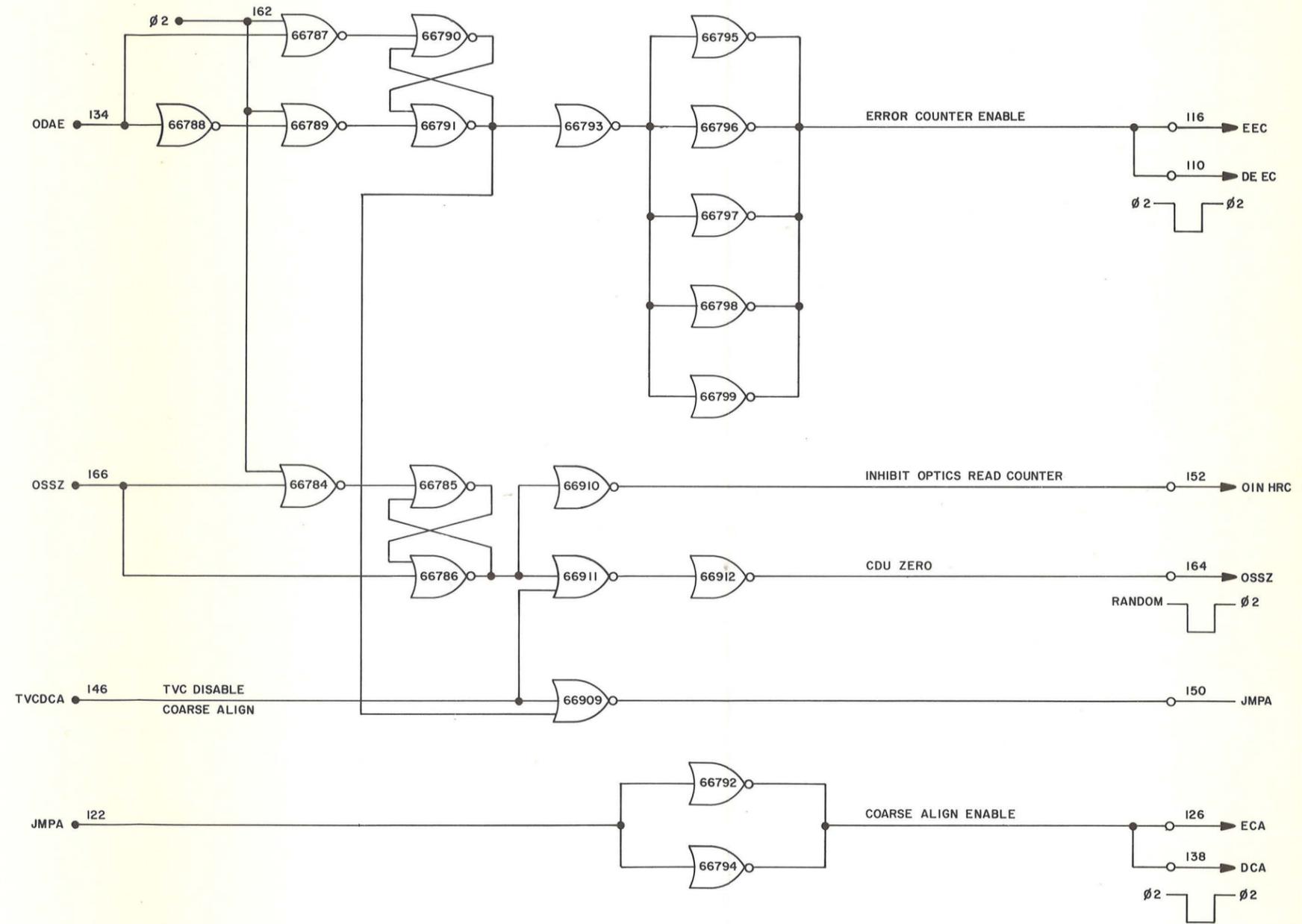
4-4.4.8 Ambiguity Logic. The ISS ambiguity logic prevents the CDU read counters from indicating a false, or ambiguous, gimbal position. The mechanization of the CDU is such that an ambiguous indication can occur only if the read counters and the gimbals are separated by a large angle (135 to 225 degrees). In normal operation, with the analog to digital conversion systems energized, the read counters repeat the gimbal angle within some very small error. The only time that a large angular difference can occur is at initial turnon or during the ISS CDU zero mode. At the initiation of these modes the ISS read counters are set to zero, but the gimbals may be at any arbitrary angle. With the read counters at zero, the only gimbal position that can cause an ambiguous indication is at 225 degrees. To determine whether the gimbals are in the vicinity of 225 degrees, the $\cos \theta$ winding of each 1X gimbal angle resolver is level-detected by a circuit in the applicable coarse system module. The circuit produces an ambiguity detect signal (\overline{Ad}) when the gimbal angle is between 125 and 235 degrees.

In the CDU zero mode the read counters are zeroed and then are allowed to count up again to the gimbal angle. If the gimbal were at 225 degrees, however, the read counter would remain at zero and indicate an ambiguous gimbal position. To prevent this, the ISS ambiguity logic circuit senses Ad and issues an override signal. This forces the read counter rate select logic into high speed (12.8 kpps) and the read counter up-down logic into the countdown command. The read counter then counts down at high speed until it reaches 225 degrees at which time the override signal is removed and the read counter logic is allowed to function normally to complete the operation of matching the read counter angle to the gimbal angle.

The ISS ambiguity logic circuits for the inner, middle, and outer gimbals are shown in figure 4-16H. The three circuits are the same except for a few NOR gates shown in the inner ambiguity logic circuit that invert I, Z, and the 800 cps reference signal (R1) in order to perform necessary logic operations within the three logic circuits. Each ambiguity logic circuit contains two flip-flops, A and B. The two flip-flops form a shift register in that the state of flip-flop A is transferred to flip-flop B during a particular function.

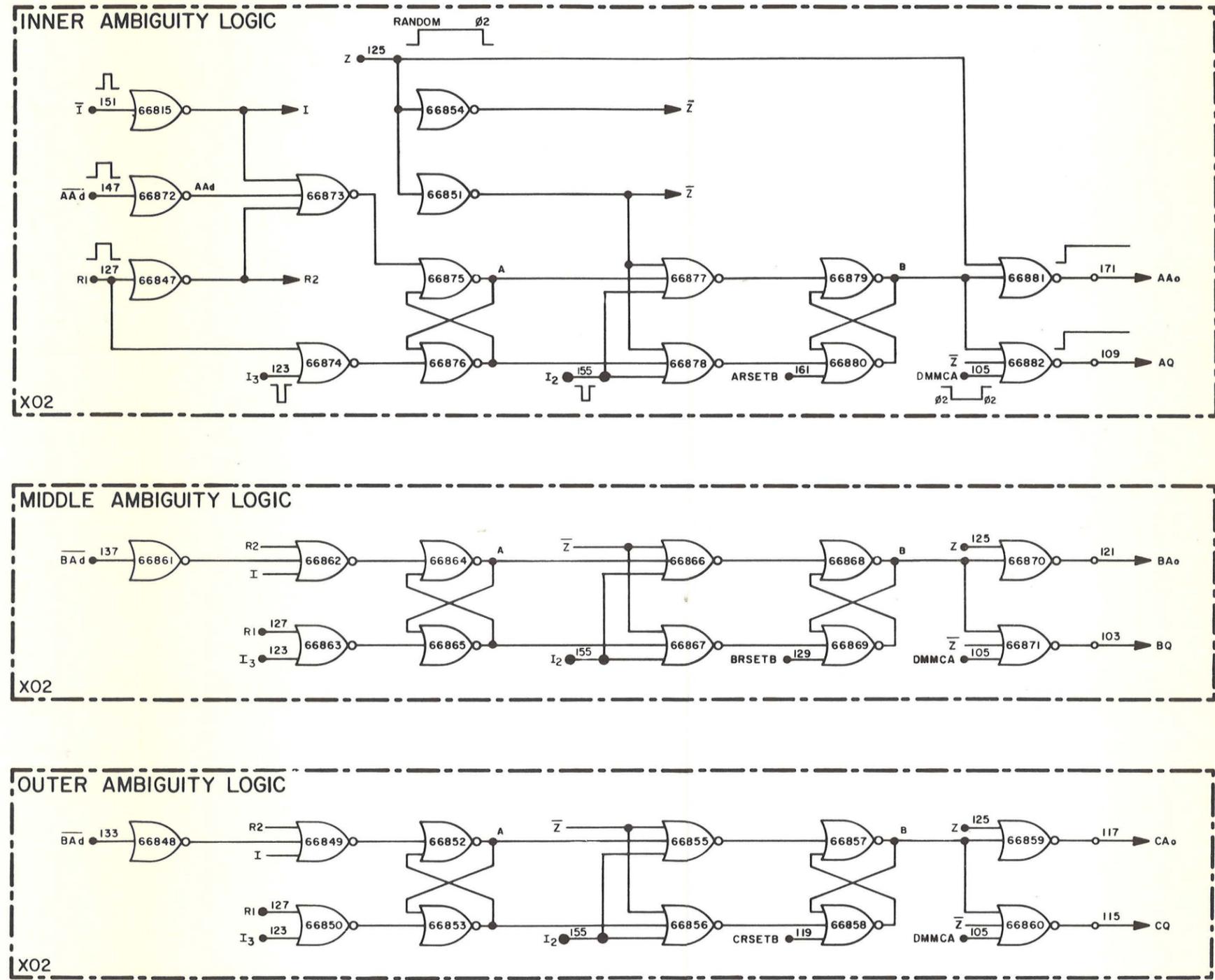
Signals AAd , BAd , and CAd are the 800 pps ambiguity detect signals for the inner, middle, and outer gimbals, respectively. When the particular gimbal is between 125 and 235 degrees the ambiguity detect pulses are out of phase with respect to R1. To detect the presence of Ad at interrogate time and set flip-flop A, Ad is ANDed with the out of phase reference signal (R2) and I. On the second I (1/1600 second later) the state of flip-flop A remains unchanged, but on the I_3 that follows the second I, flip-flop A is reset since R1 changes level.

Regardless of the ISS mode of operation, flip-flop A sets and resets as described as long as the gimbal angle is between 125 and 235 degrees. If the gimbal angle is within this range during the ISS CDU zero mode, the content of flip-flop A shifts into flip-flop B coincident with I_2 . When the CDU zero discrete is removed, an ambiguity override signal (Ao) is produced and sent to the read counter logic circuits in the error angle counter and logic module. Ao forces the read counter logic to count the read counter down at high speed until the read counter reaches 225 degrees, at which time reset signal $ARSETB$, $BRESSTB$, or $CRXSETB$, for the inner, middle, or outer gimbals, respectively, is produced by the read counter and applied to flip-flop B. When flip-flop B resets, Ao is removed. The read counter logic circuits are then allowed to function normally.



18927

Figure 4-16G. OSS Moding Sync Logic, Logic Diagram



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Figure 4-16H. ISS Ambiguity Logic, Logic Diagram

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

During the IMU turnon mode it is desired to clear the read counter and bring the gimbals to their zero position as a reference or starting point. During the IMU turnon mode the sine winding output from the 1X gimbal angle resolver is applied as an error signal to the gimbal servo amplifiers to drive the gimbals to their zero position. This method precludes the possibility of an ambiguous gimbal position indication. The CDU also contains backup circuitry that provides an alternate method of driving the gimbals to their zero positions during the IMU turnon mode but this circuitry is not presently used. This method uses the D/A converter coarse align output in conjunction with the CDU zero and coarse align enable discretes. With this method the gimbal drive signal is essentially the CDU error signal (always present in the coarse align error signal for rate limiting purposes). This method could result in an ambiguous gimbal position indication if the gimbal is initially in the vicinity of 225 degrees. The turnon enable signal (Q) is generated by the ambiguity logic as a result of the presence of Ad, the coarse align enable discrete, and the CDU zero discrete. Q is sent to the read counter where it sets the read counter to 90 degrees and effectively shifts the ambiguity point to 315 degrees, allowing the gimbal to be driven towards 90 degrees. When the gimbal is driven away from the ambiguity detect zone of 125 to 235 degrees the ambiguity detect signal is no longer generated and both ambiguity flip-flops reset to remove Q. The gimbals then continue to drive to the zero position.

4-4.5 READ COUNTER MODULE. The read counter module functions with the coarse system module to form the coarse analog to digital (A/D) conversion system, and functions with the quadrant selector module and the MSA&QR module to form the fine A/D conversion system. These systems convert the gimbal angle represented by resolver signals into digital pulses which are sent to the CMC. The optics does not have a coarse system module in the coarse A/D conversion system. The read counter module, quadrant selector module, and MSA&QR module convert the optics angle represented by resolver signals into digital pulses which are sent to the CMC. The read counter module consists of the read counter, associated buffer units, and the coarse and fine switch logic circuits.

A block diagram of the read counter module is shown in figure 4-16I. The counter contains 16 stages with each bit accumulated by the counter equivalent to approximately 20 arc seconds of gimbal angular rotation or of LOS shaft movement, and 2.5 arc seconds of LOS trunnion movement. The overflow output from the first stage, equivalent to approximately 40 arc seconds for the gimbals and optics shaft, and 5 arc seconds for the trunnion, is sent to the CMC. The content of the read counter is applied to buffer units and coarse and fine switch logic circuits which develop the switch control signals required by the coarse system module, the quadrant selector module, and the MSA&QR module.

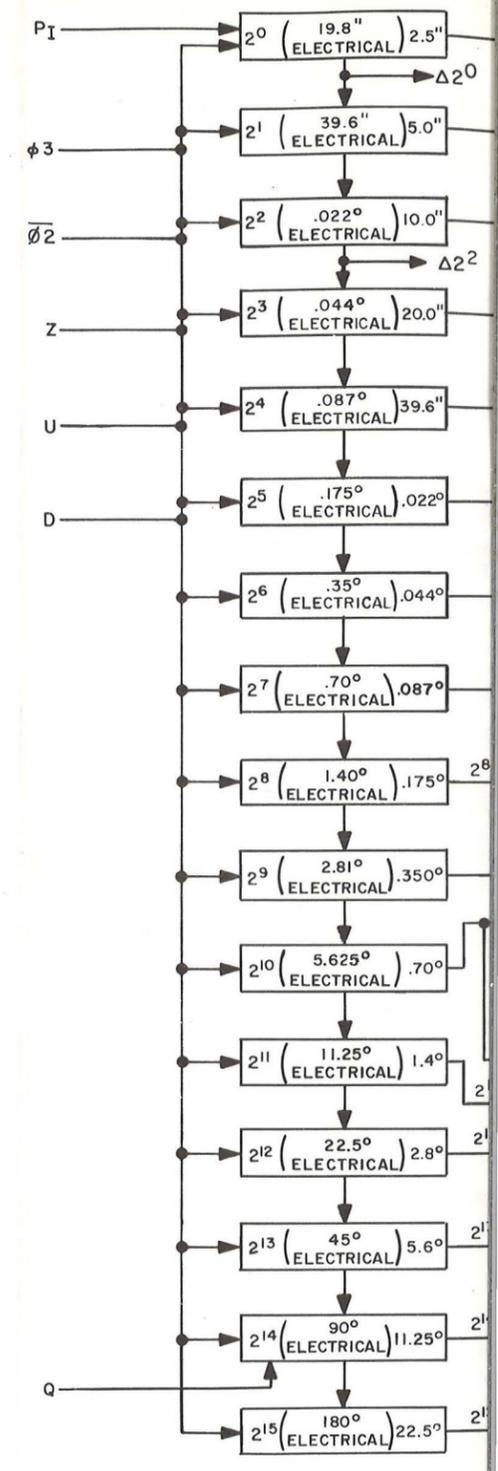
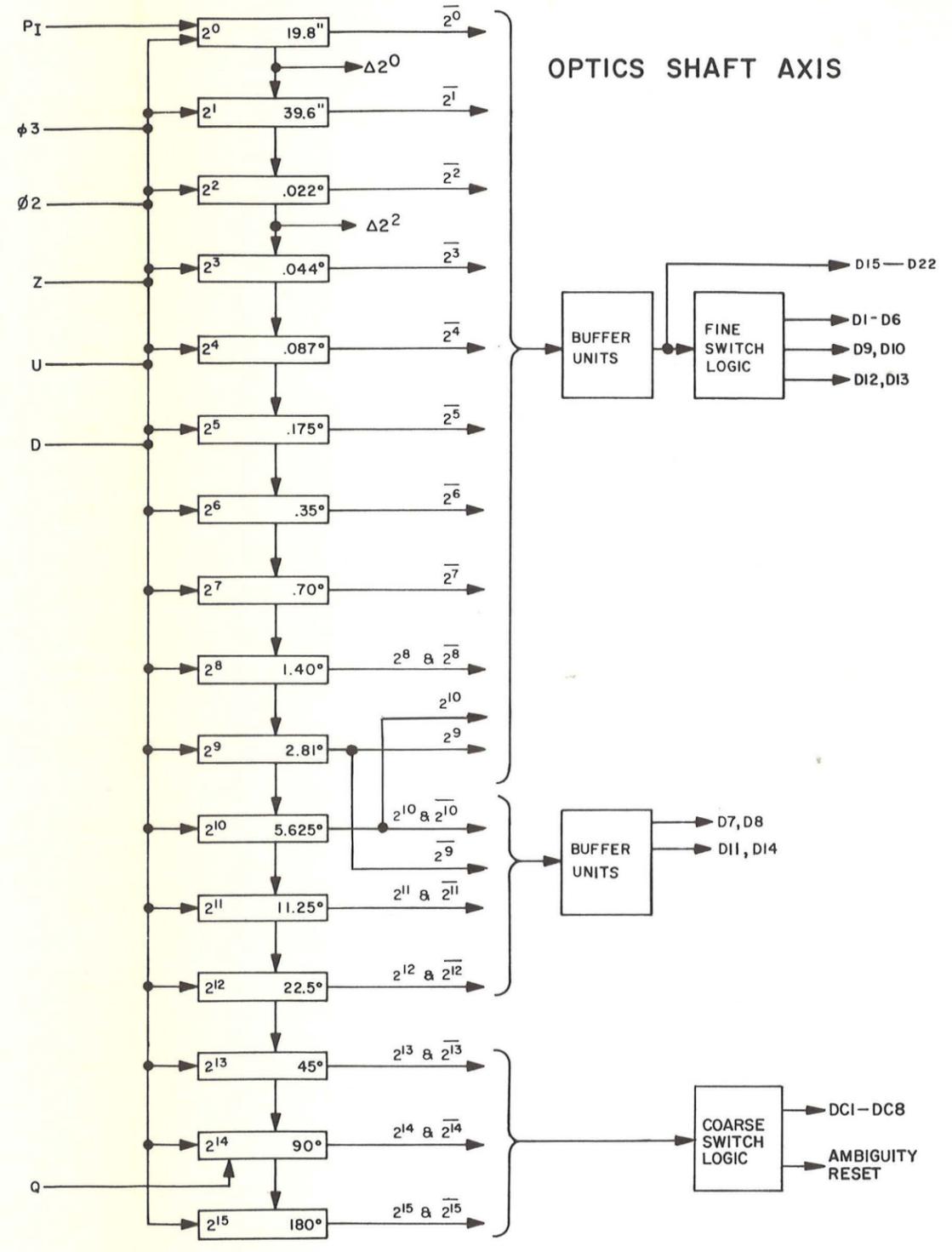
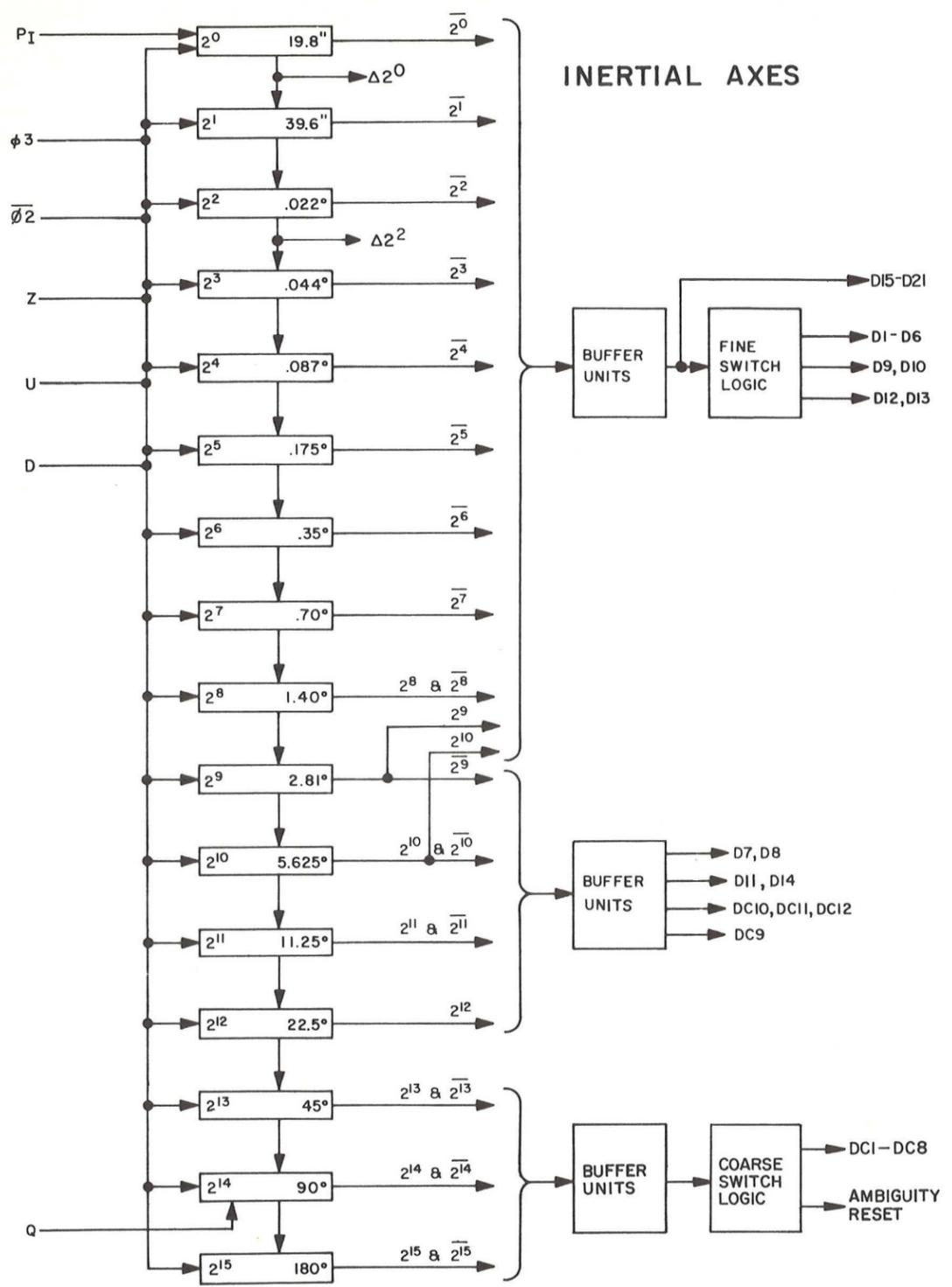
4-4.5.1 Read Counter. The read counter (figure 4-16J) is a 16 stage binary counter. The 16 stages are designated 2^0 through 2^{15} . The largest numerical value the counter can hold is $2^{16}-1$ or 65,535. In the ISS application, the initialized state equals either 0 degree or 360 degrees of gimbal angle rotation with respect to the 1X gimbal angle resolver shaft. The read counter, therefore, subdivides the 360 degrees into 65,536 parts. Each division, or increment, of the counter is equal to approximately 0.0055 degree, or 19.99539 arc seconds. The optics shaft counter operates in the same way. In the optics trunnion application, the initialized state equals either 0 degree or 45 degrees of trunnion angle rotation with respect to the 1X angle resolver shaft. The read counter, therefore, subdivides the 45 degrees into 65,536 parts. Each division, or increment, of the counter is equal to approximately 0.00069 degree, or 2.5 arc seconds of trunnion angle rotation. The counter is incremented or decremented at an 800 pps, 6.4 kpps, or 12.8 kpps rate.

The logic circuits that control the operation of the read counter registers are contained in the error angle counter and logic module. The read counter logic circuits decide in which direction the read counter counts and the rate at which it counts. The read counter logic circuits command the read counter to count up or down and send incrementing pulses at 800 pps, 6.4 kpps, or 12.8 kpps. The decision to count up or down is made at $\phi 2$ time and the increment pulses are issued at $\phi 4$ time.

Each stage of the 16 stage counter is basically the same. Each stage contains a master and slave flip-flop with three additional gates to permit up-down counting.

Signal $\Delta 2^0$ is the incrementing pulse applied to the second counter stage. This pulse is produced each time the first stage overflows and is one-half the frequency rate of P_1 (applied to the first stage). The value of $\Delta 2^0$ is twice the value of P_1 , 0.011 degree or 39.55078 arc seconds of gimbal angle rotation or optics shaft angle rotation with respect to the 1X resolver shaft. The $\Delta 2^0$ pulses are applied to the CMC logic circuit located in the read counter logic section of the error angle counter and logic module. The $\Delta 2^0$ pulses do not contain polarity information so they must be ANDed with the U and D commands produced by the read counter up-down logic circuit. If the counter is being incremented, U is present and $\Delta 2^0$ causes the CMC logic circuit to produce a $+\Delta\theta_G$ pulse. If the counter is being decremented, D is present and $\Delta 2^0$ causes the CMC logic circuit to produce a $-\Delta\theta_G$ pulse. The $\pm\Delta\theta_G$ pulses are supplied to the CMC via transformer driver circuits in the D/A converter module.

Signal $\Delta 2^2$ is the incrementing pulse applied to the fourth stage. This pulse is present each time the third stage overflows and it has one-eighth the frequency rate of P_1 . The value of $\Delta 2^2$ is 0.044 degree or 158.193 arc seconds for gimbal angle or optics shaft angle, or the value of $\Delta 2^2$ is 0.00562 degree or 20.232 arc-seconds for optics trunnion angle. The $\Delta 2^2$ pulse contains no polarity information either; however, the read counter up-down logic provides polarity signals U_G and D_G to the error counter logic circuits to indicate whether the counter is being incremented or decremented.



BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

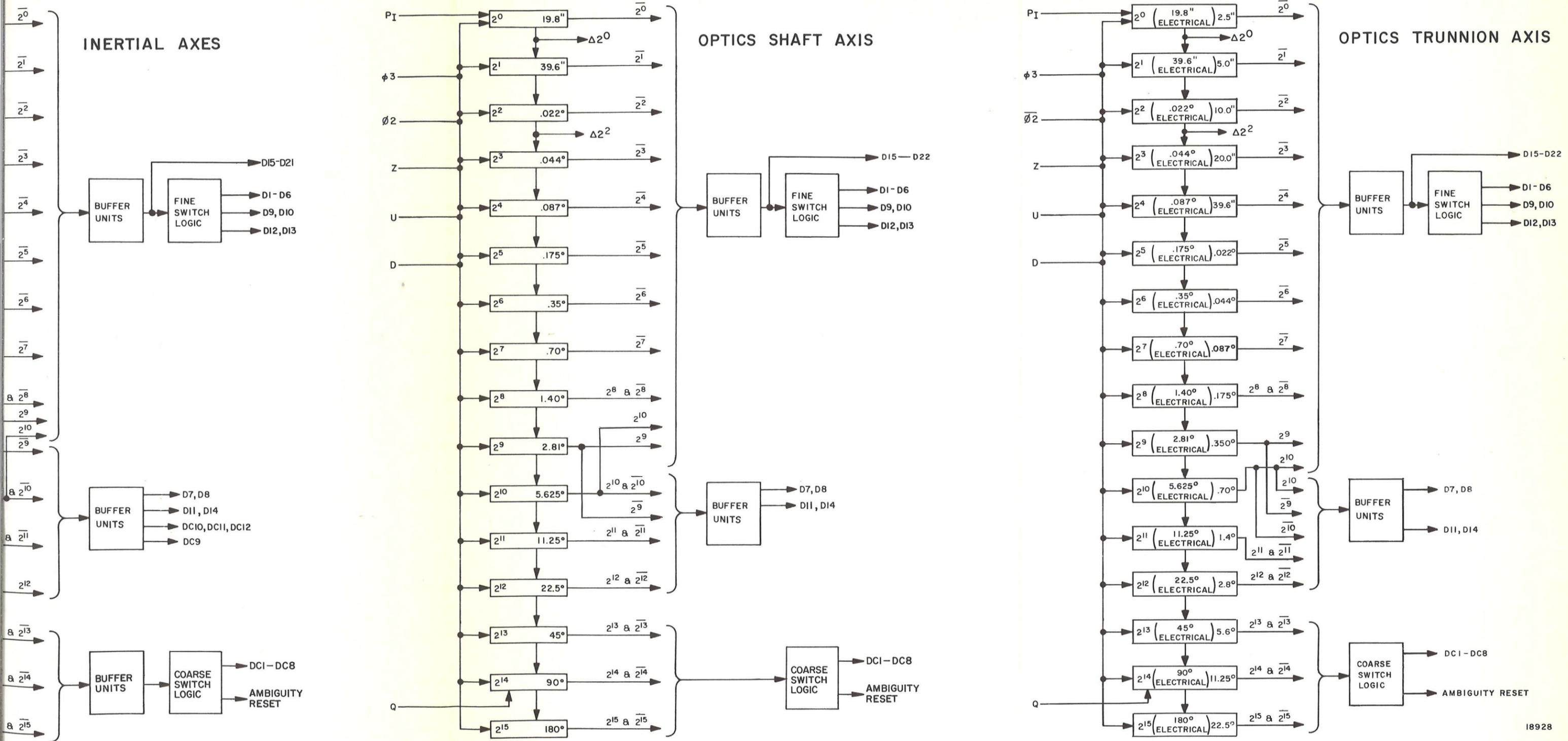
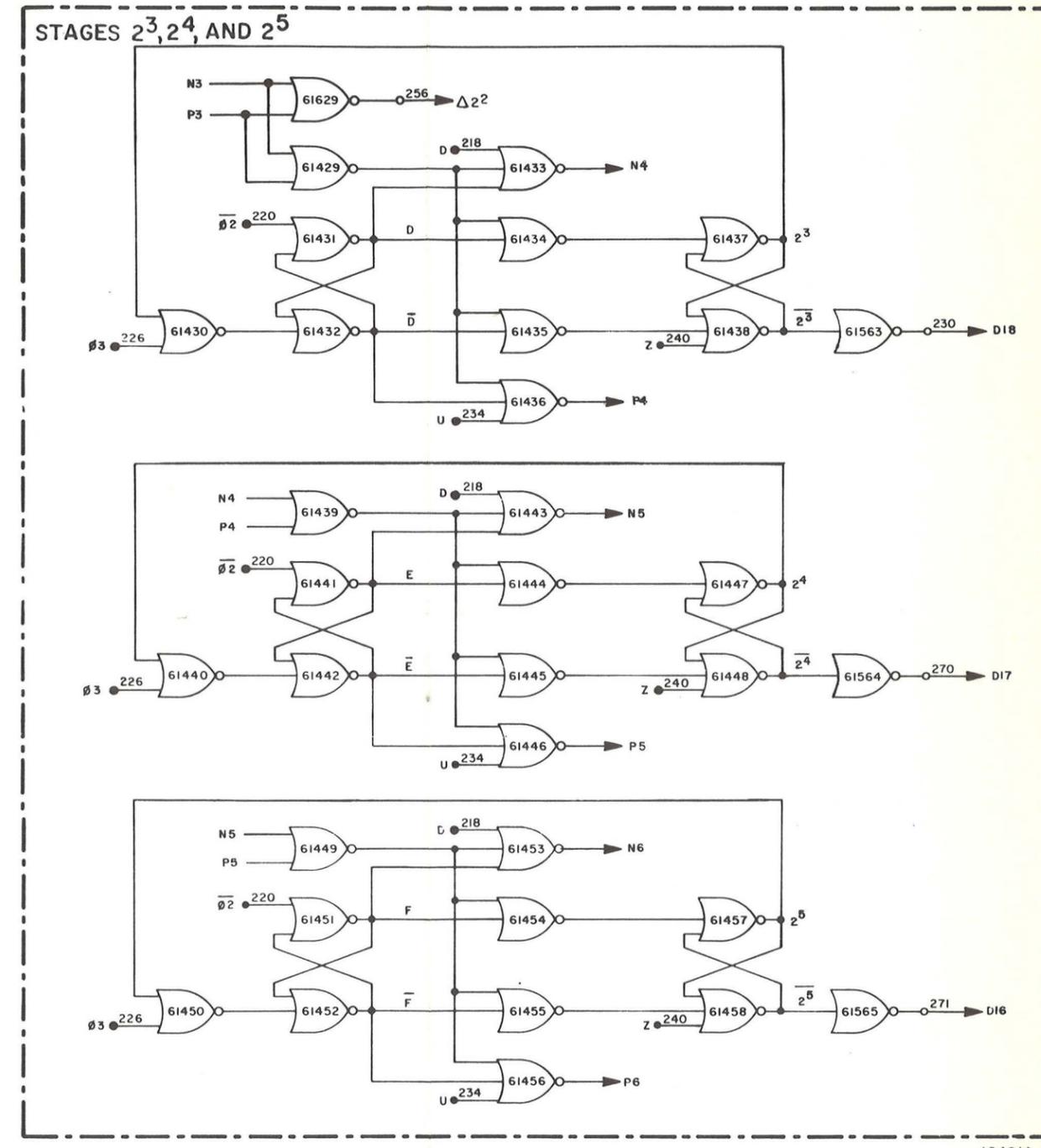
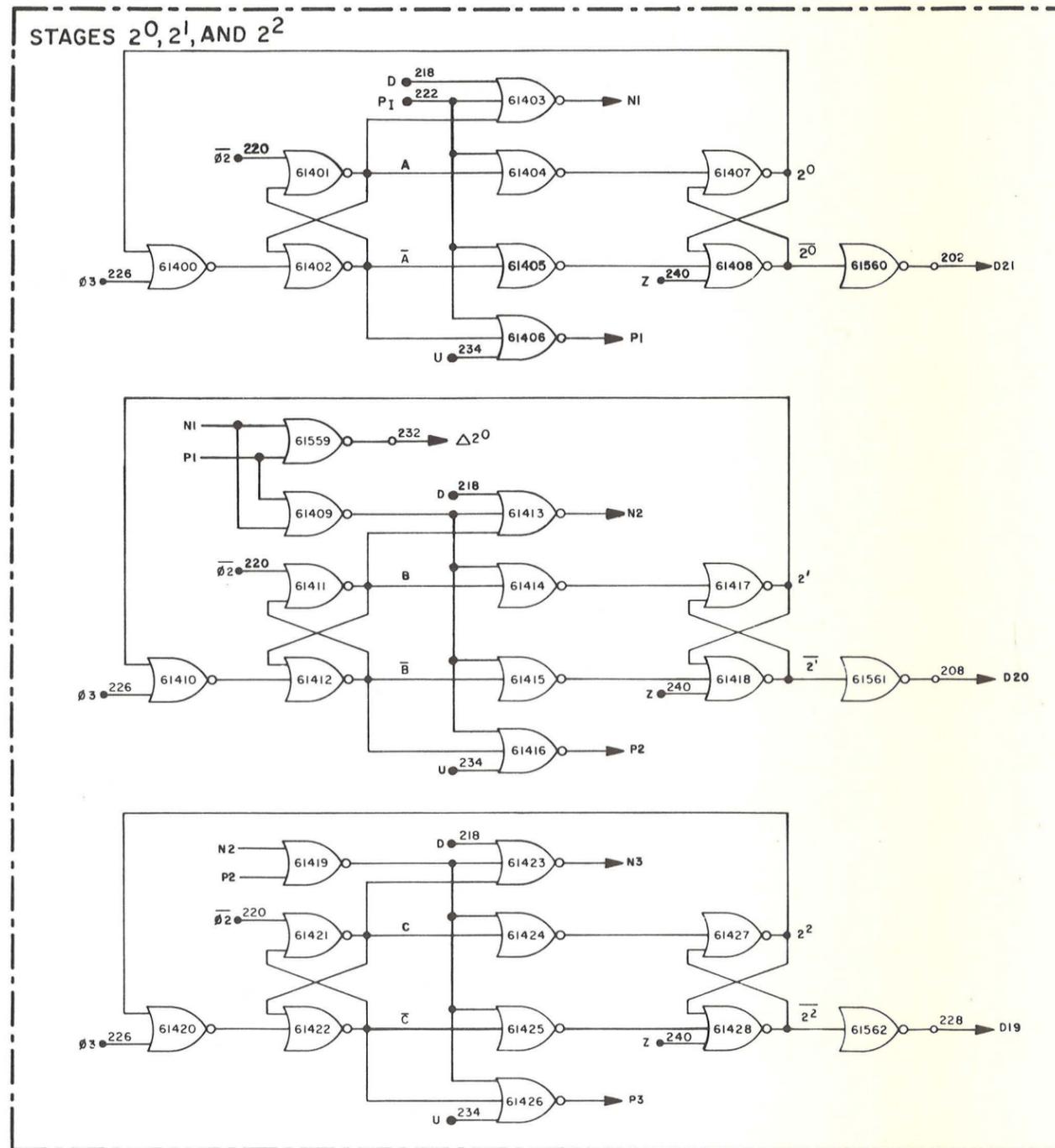


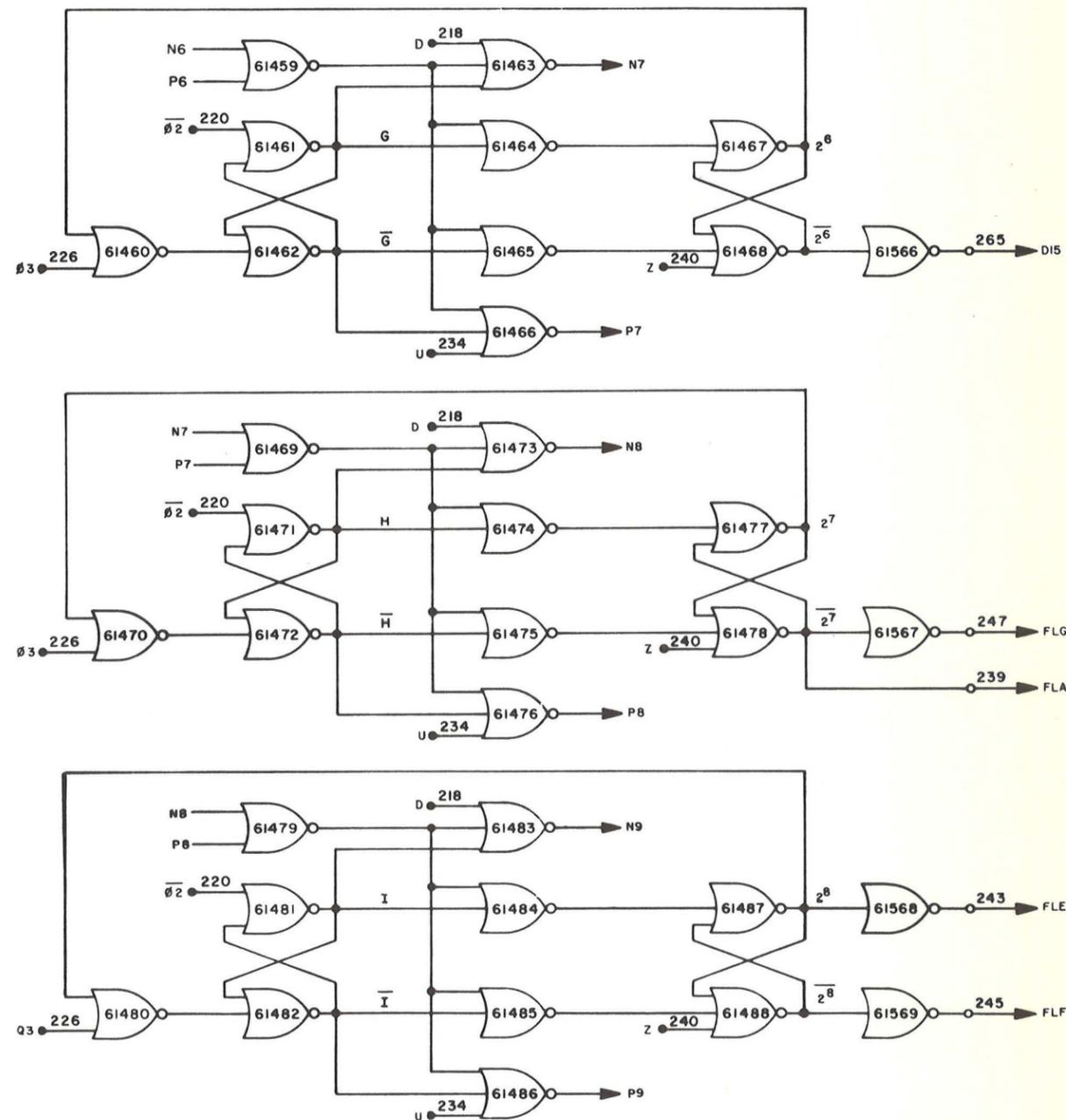
Figure 5-16I. Read Counter Module, Block Diagram



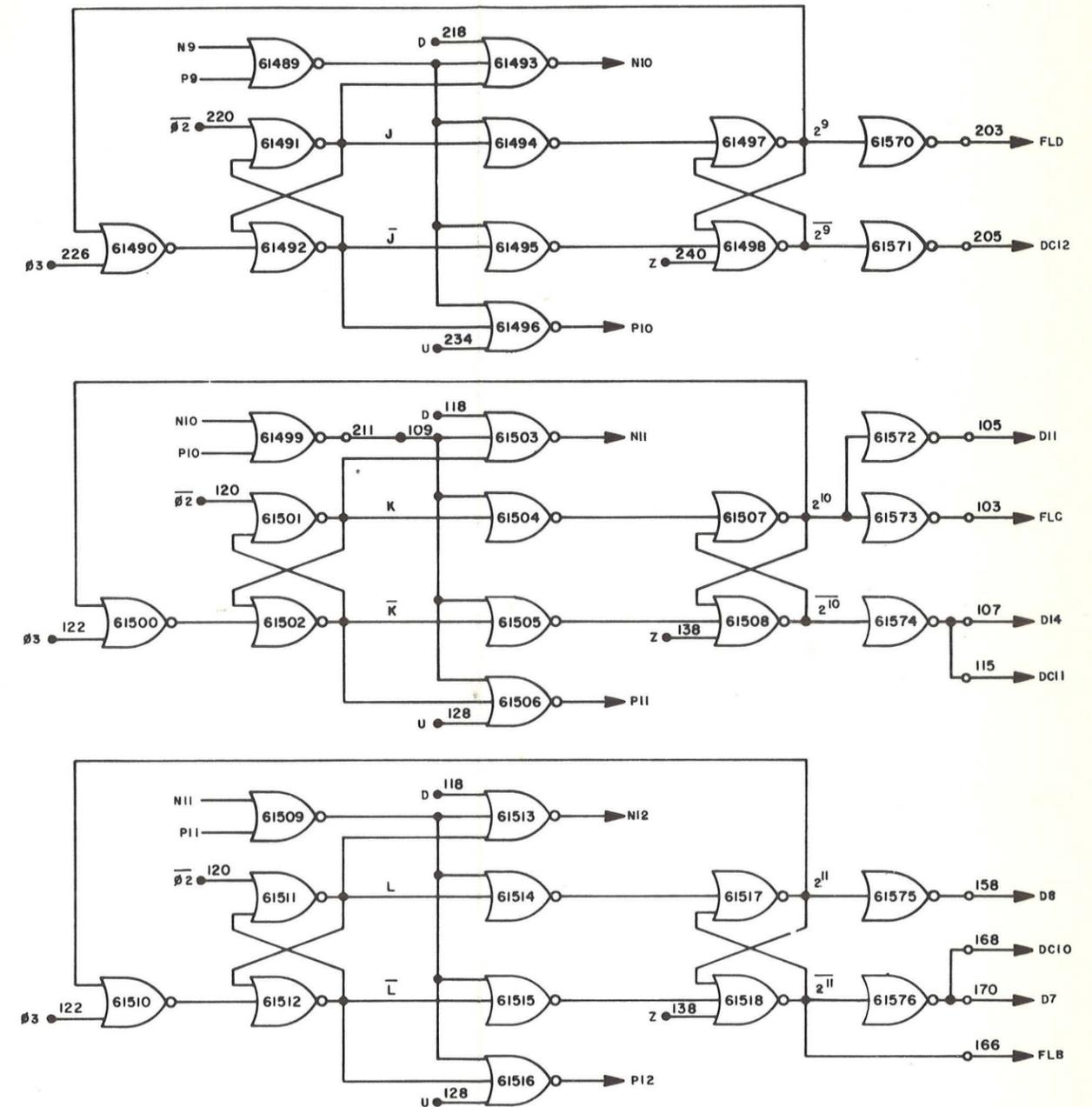
16461A-1

Figure 4-16J. Read Counter Register, Logic Diagram (Sheet 1 of 3)

STAGES 2⁶, 2⁷, AND 2⁸

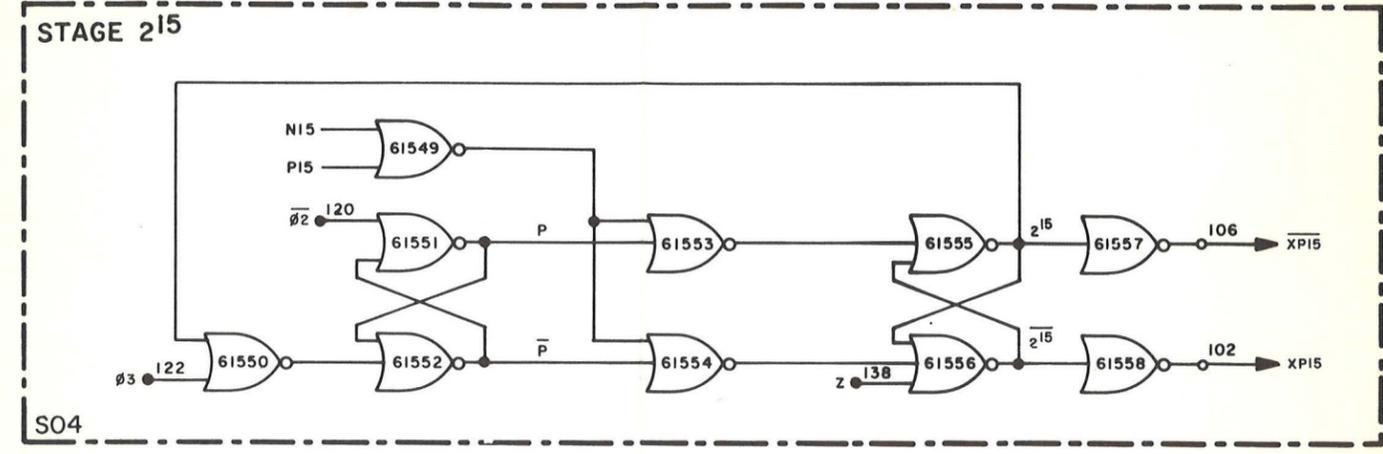
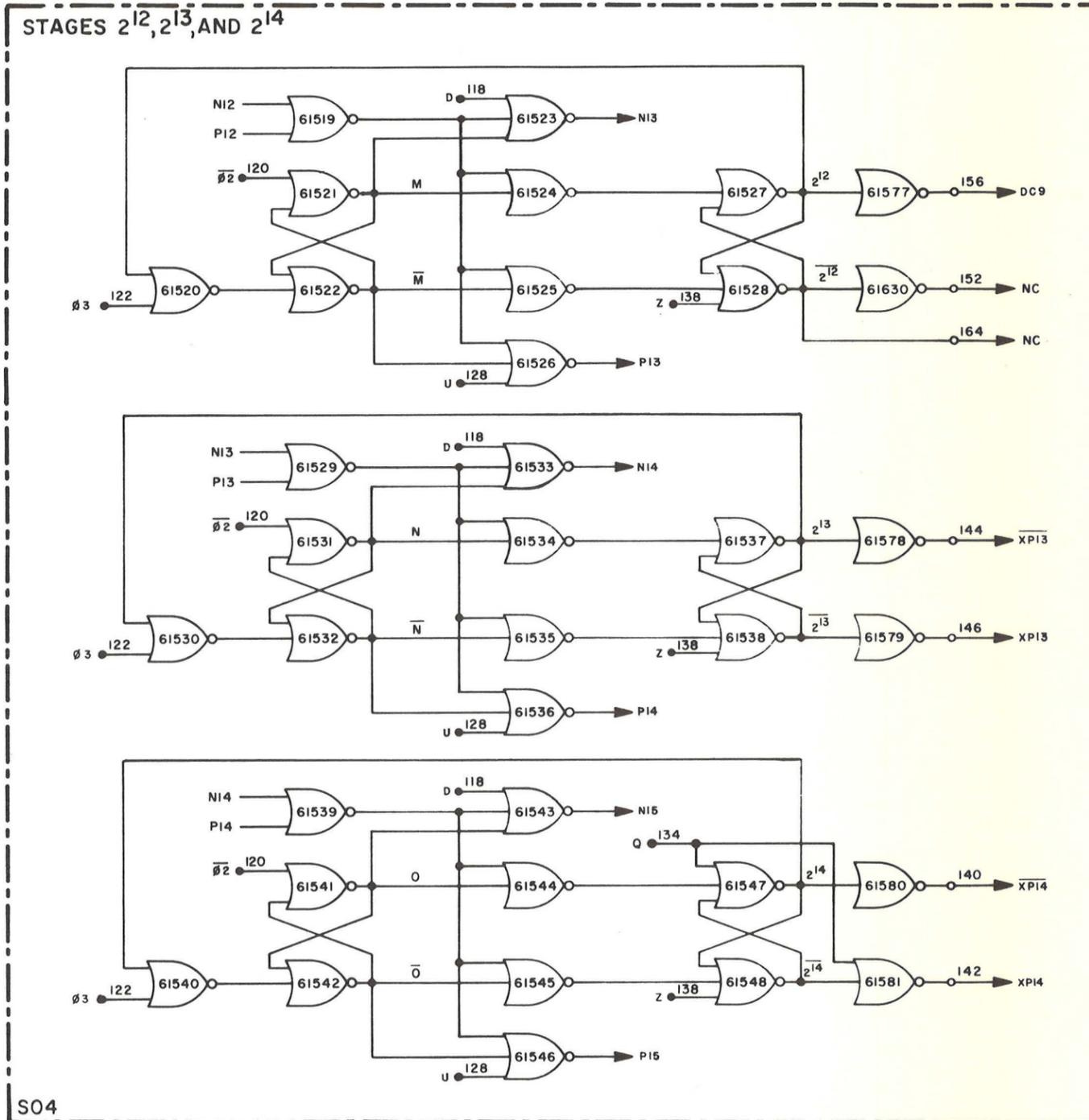


STAGES 2⁹, 2¹⁰, AND 2¹¹



16461A-2

Figure 4-16J. Read Counter Register, Logic Diagram (Sheet 2 of 3)



16461A-3

Figure 4-16J. Read Counter Register, Logic Diagram (Sheet 3 of 3)

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

The CDU zero discrete (Z) is applied to the reset side of flip-flops 2^0 through 2^{15} . When the ISS or OSS zero discrete is present, all 16 stages are held in the zero state. The turn on enable signal (Q) from the ambiguity logic circuit forces signal XP14 and its complement $\overline{XP14}$ to appear as though the 2^{14} stage contains a logic 1 for a 90 degree gimbal angle indication or optics shaft angle indication, or a logic 1 for a 45 degree trunnion angle indication. (Refer to the ambiguity logic portion of the digital mode module theory of operation description.) The 2^{15} stage of the counter does not receive U and D since it is the last stage of the register and does not generate carry signals.

4-4.5.2 Buffer Units. The buffer units are NOR gates that invert the outputs of the 16 stages of the read counter. The inverted outputs are used directly as switch control signals to the switching systems in the A/D conversion systems or are used as inputs to the coarse and fine switch logic. A typical buffer unit (figure 4-16J) is gate 61560 which inverts the 2^0 output of the 2^0 stage to produce switch control signal D21.

4-4.5.3 Coarse and Fine Switch Logic. The coarse and fine switch logic (figure 4-16K) decodes the content of the 16 stage read counter into coarse and fine switch control signals to operate the switches in the coarse system module, the quadrant selector module, and the MSA&QR module. The coarse system module functions with the read counter module to form the coarse A/D conversion system. The switches in the coarse system module are operated by coarse switch control signals DC1 through DC12. DC9 through DC12 are direct outputs from the buffer units in the 2^{12} through 2^9 stages, respectively, of the read counter. DC1 through DC8 are produced by the coarse switch logic circuit. The quadrant selector module, together with the MSA&QR module, functions with the read counter module to form the fine A/D conversion system. The switches in the quadrant selector module are operated by fine switch control signals D1 through D14. D7, D8, D11, and D14 are direct outputs from the buffer units in the 2^{10} and 2^{11} stages of the read counter for the inertial and optics shaft angles and the 2^{11} and 2^{12} stages of the read counter for the optics trunnion angle. D1 through D6, D9, D10, D12, and D13 are produced by the fine switch logic circuit. The switches in the MSA&QR module are operated by fine switch control signals D15 through D21 (D15 through D22 for optics) which are direct outputs from the buffer units in the 2^6 through 2^0 stages, respectively, of the read counter. Figure 4-16J lists the logic equations for all switch control signals. The logic equations are written in terms of the read counter content.

The coarse switch control signals operate switches in the coarse system module that switch the sine and cosine winding outputs from the 1X gimbal angle resolver through various values of attenuator resistors in accordance with a trigonometric nulling identity. The attenuator values represent the content of the read counter and are selected incrementally by the switch control signals. When the read counter value equals the gimbal angle, the attenuator values selected cause the nulling identity to go to zero and the system is nulled. Until a null is accomplished, the coarse system module sends a ternary level error signal to the read counter logic circuits that causes the read counter to count up or down and thereby select different values of

attenuators. For every value of read counter content there is a corresponding switch and attenuator arrangement. After the coarse system is nulled, the fine A/D conversion system performs a similar nulling operation using the 16X gimbal angle resolver sine and cosine winding outputs.

The operations of the coarse and fine switch logic circuits can best be explained by discussing the switch control signal functions. The switch control signals present at any time represent the value of the read counter at that time. In the discussion on the read counter it was stated that the read counter was used to subdivide 360 degrees of gimbal or optics shaft angle rotation into 65,536 segments, each equal to 0.0055 degree, or 45 degrees of trunnion rotation into 65,536 segments, each equal to 0.00069 degree. This analogy may be applied to the switch control signals since each of the segments is represented by a particular combination of signals which select, in turn, a particular combination of attenuation resistors that represent each of the segments. This function is shown graphically in figure 4-16L.

Four of the coarse switch control signals select attenuation values representing the quadrant in which the read counter value lies for the three inertial loops. The four coarse switch control signals, which are DC1, DC8, DC3, and DC6, in effect, divide 360 degrees into four quadrants. Signal DC1 is present when the read counter value is between 135 and 225 degrees. DC8, DC3, or DC6 is present when the read counter value is between 225 and 315, 315 and 45, or 45 and 135 degrees, respectively. DC2, DC5, DC7, and DC4 divide each quadrant into two 45 degree segments. DC2 is present when the content of the read counter is between 90 and 135 degrees or between 225 and 270 degrees. The presence of DC6 together with DC2 establishes the read counter value between 90 and 135 degrees. If, however, DC8 is present instead of DC6, the value of the read counter is established between 225 and 270 degrees. Each 45 degree segment shown in figure 4-16J is represented by a combination of two coarse switch control signals. Each 45 degree segment is further divided into two 22.5 degree segments by the presence or absence of DC9. DC10 through DC12 divide each 22.5 degree segment into eight segments, each equal to 2.81 degrees. Each of the 128 segments (2.81 degrees each) contained in 360 degrees is represented, therefore, by a particular combination of coarse switch control signals.

The coarse and fine A/D conversion systems overlap. Therefore, when the read counter has been matched within approximately 8 degrees of the coarse system module, the quadrant selector module and MSA&QR take over. They match the read counter value to the gimbal angle with a greater degree of accuracy, using the 16X gimbal angle resolver outputs. The fine switch control signals are used to select attenuator values representing a segment equal to 0.088 electrical degree with respect to the 16X resolver shaft or 0.0055 mechanical degree with respect to the 1X gimbal angle resolver shaft. For the remainder of the discussion for the inertial loops, all the angular values will be expressed with respect to the 1X gimbal angle resolver shaft.

OPTICS

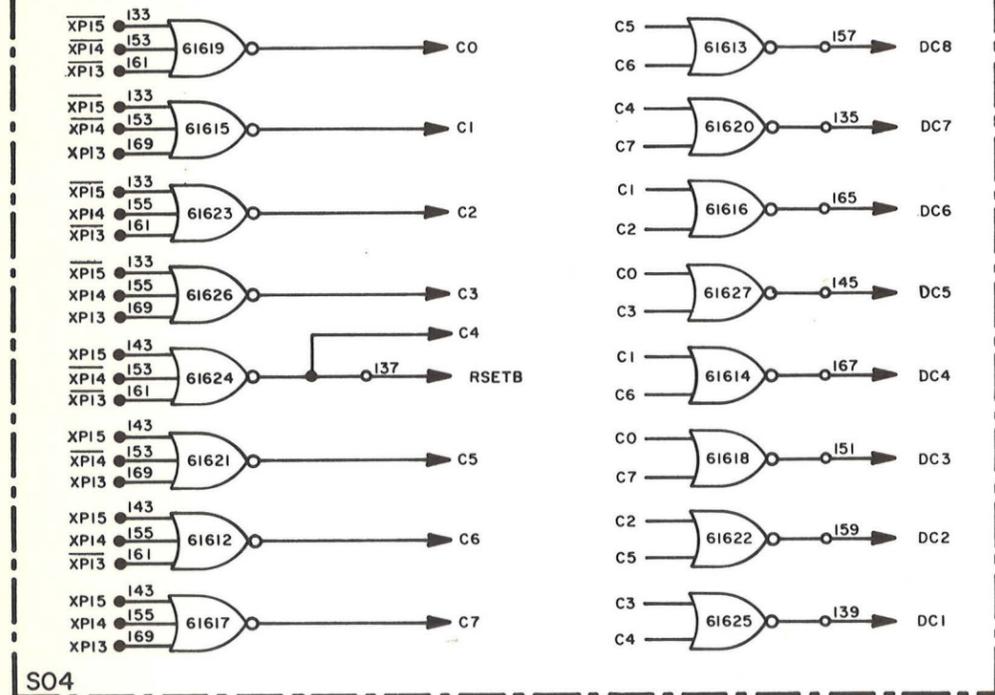
INERTIAL

FINE SWITCH LOGIC		
OPTICS SHAFT AXIS		OPTICS TRUNNION AXIS
D22	LEAST SWITCH DISABLE	2^0
D21	2^0	2^1
D20	2^1	2^2
D19	2^2	2^3
D18	2^3	2^4
D17	2^4	2^5
D16	2^5	2^6
D15	2^6	2^7
D14	2^{10}	2^{11}
D13	$2^{10} \cdot 2^7$	$2^{11} \cdot 2^8$
D12	$2^{10} \cdot 2^7$	$2^{11} \cdot 2^8$
D11	2^{10}	2^{11}
D10	$2^{10} \cdot 2^7$	$2^{11} \cdot 2^8$
D9	$2^{10} \cdot 2^7$	$2^{11} \cdot 2^8$
D8	2^{11}	2^{12}
D7	2^{11}	2^{12}
D6	$2^{11} \cdot 2^{10} + 2^{11} \cdot 2^{10}$	$2^{12} \cdot 2^{11} + 2^{12} \cdot 2^{11}$
D5	$\overline{D6}$	$\overline{D6}$
D4	$2^{10} \cdot 2^9 \cdot 2^8 + 2^{10} \cdot 2^9 \cdot 2^8$	$2^{11} \cdot 2^{10} \cdot 2^9 + 2^{11} \cdot 2^{10} \cdot 2^9$
D3	$2^{10} \cdot 2^9 \cdot 2^8 + 2^{10} \cdot 2^9 \cdot 2^8$	$2^{11} \cdot 2^{10} \cdot 2^9 + 2^{11} \cdot 2^{10} \cdot 2^9$
D2	$2^{10} \cdot 2^9 \cdot 2^8 + 2^{10} \cdot 2^9 \cdot 2^8$	$2^{11} \cdot 2^{10} \cdot 2^9 + 2^{11} \cdot 2^{10} \cdot 2^9$
D1	$2^{10} \cdot 2^9 \cdot 2^8 + 2^{10} \cdot 2^9 \cdot 2^8$	$2^{11} \cdot 2^{10} \cdot 2^9 + 2^{11} \cdot 2^{10} \cdot 2^9$
COARSE SWITCH LOGIC		
DC8	$2^{15} (2^{14} \cdot 2^{13} + 2^{14} \cdot 2^{13})$	
DC7	$2^{15} (2^{14} \cdot 2^{13} + 2^{14} \cdot 2^{13})$	
DC6	$2^{15} (2^{14} \cdot 2^{13} + 2^{14} \cdot 2^{13})$	
DC5	$2^{15} (2^{14} \cdot 2^{13} + 2^{14} \cdot 2^{13})$	
DC4	$2^{15} \cdot 2^{14} \cdot 2^{13} + 2^{15} \cdot 2^{14} \cdot 2^{13}$	
DC3	$2^{15} \cdot 2^{14} \cdot 2^{13} + 2^{15} \cdot 2^{14} \cdot 2^{13}$	
DC2	$2^{15} \cdot 2^{14} \cdot 2^{13} + 2^{15} \cdot 2^{14} \cdot 2^{13}$	
DC1	$2^{15} \cdot 2^{14} \cdot 2^{13} + 2^{15} \cdot 2^{14} \cdot 2^{13}$	
AMB RESET (B) = $2^{15} \cdot 2^{14} \cdot 2^{13}$		

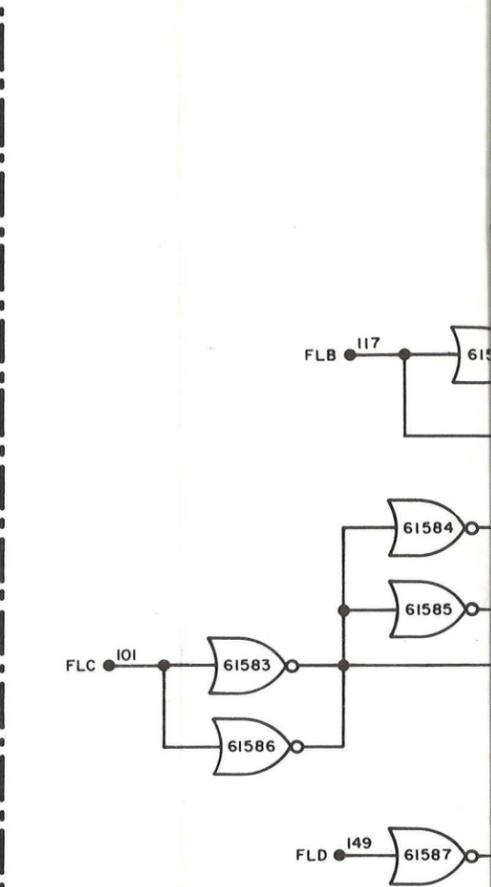
FINE SWITCH CONTROL SIGNALS	
SIGNAL	EQUATION
D21	2^0
D20	2^1
D19	2^2
D18	2^3
D17	2^4
D16	2^5
D15	2^6
D14	2^{10}
D13	$2^7 \cdot 2^{10}$
D12	$2^7 \cdot 2^{10}$
D11	2^{10}
D10	$2^7 \cdot 2^{10}$
D9	$2^7 \cdot 2^{10}$
D8	2^{11}
D7	2^{11}
D6	$2^{10} \cdot 2^{11} + 2^{10} \cdot 2^{11}$
D5	$2^{10} \cdot 2^{11} + 2^{10} \cdot 2^{11}$
D4	$2^8 \cdot 2^9 \cdot 2^{10} + 2^8 \cdot 2^9 \cdot 2^{10}$
D3	$2^8 \cdot 2^9 \cdot 2^{10} + 2^8 \cdot 2^9 \cdot 2^{10}$
D2	$2^8 \cdot 2^9 \cdot 2^{10} + 2^8 \cdot 2^9 \cdot 2^{10}$
D1	$2^8 \cdot 2^9 \cdot 2^{10} + 2^8 \cdot 2^9 \cdot 2^{10}$

COARSE SWITCH CONTROL SIGNALS	
SIGNAL	EQUATION
DC12	2^9
DC11	2^{10}
DC10	2^{11}
DC9	2^{12}
DC8	$2^{15} (2^{14} \cdot 2^{13} + 2^{14} \cdot 2^{13})$
DC7	$2^{15} (2^{14} \cdot 2^{13} + 2^{14} \cdot 2^{13})$
DC6	$2^{15} (2^{14} \cdot 2^{13} + 2^{14} \cdot 2^{13})$
DC5	$2^{15} (2^{14} \cdot 2^{13} + 2^{14} \cdot 2^{13})$
DC4	$2^{15} \cdot 2^{14} \cdot 2^{13} + 2^{15} \cdot 2^{14} \cdot 2^{13}$
DC3	$2^{15} \cdot 2^{14} \cdot 2^{13} + 2^{15} \cdot 2^{14} \cdot 2^{13}$
DC2	$2^{15} \cdot 2^{14} \cdot 2^{13} + 2^{15} \cdot 2^{14} \cdot 2^{13}$
DC1	$2^{15} \cdot 2^{14} \cdot 2^{13} + 2^{15} \cdot 2^{14} \cdot 2^{13}$

COARSE SWITCH LOGIC



FINE SWITCH LOGIC



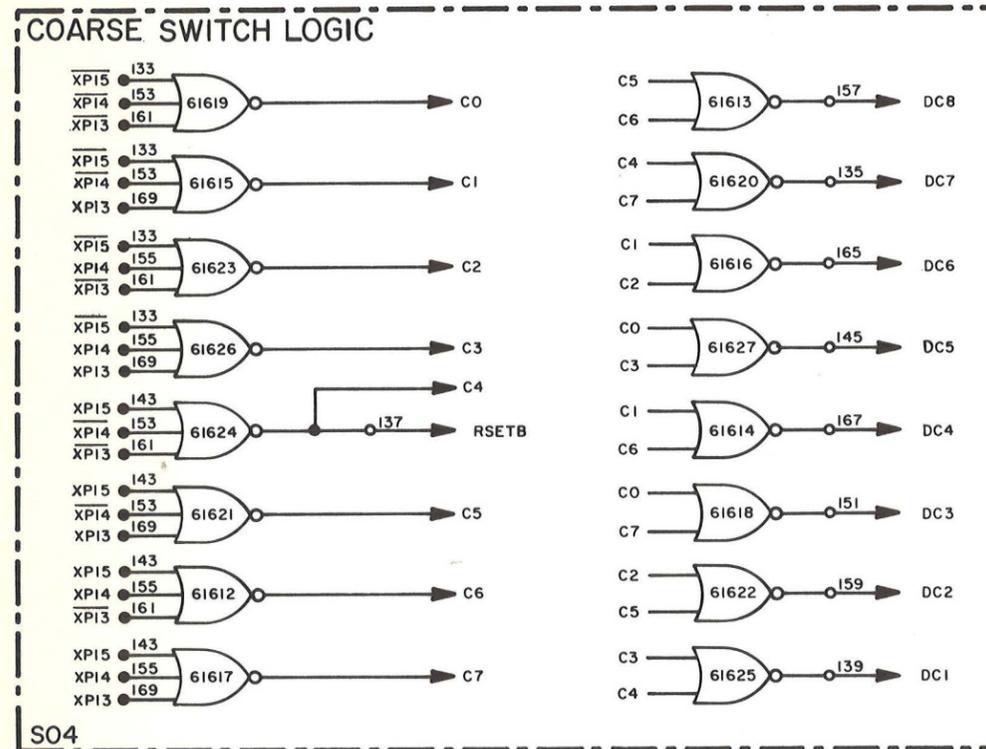
- NOTES:
1. Input signals to coarse and fine switch logic are for interconnection only and not for logic equations. The logic equations are written in terms of the read counter signals 2^0 through 2^{15}
 2. The coarse and fine switch control signals that are listed in the equations but not shown on this logic diagram, are shown on the corresponding read counter register logic diagrams.
 3. The low level (0 vdc) signal to a switch turns the switch on. A logic "1" in the CDU is a low level. The gates are therefore interpreted as NAND gates.

S04

INERTIAL

FINE SWITCH CONTROL SIGNALS	
SIGNAL	EQUATION
D21	2^0
D20	2^1
D19	2^2
D18	2^3
D17	2^4
D16	2^5
D15	2^6
D14	2^{10}
D13	$2^7 \cdot 2^{10}$
D12	$2^7 \cdot 2^{10}$
D11	2^{10}
D10	$2^7 \cdot 2^{10}$
D9	$2^7 \cdot 2^{10}$
D8	2^{11}
D7	2^{11}
D6	$2^{10} \cdot 2^{11} + 2^{10} \cdot 2^{11}$
D5	$2^{10} \cdot 2^{11} + 2^{10} \cdot 2^{11}$
D4	$2^8 \cdot 2^9 \cdot 2^{10} + 2^8 \cdot 2^9 \cdot 2^{10}$
D3	$2^8 \cdot 2^9 \cdot 2^{10} + 2^8 \cdot 2^9 \cdot 2^{10}$
D2	$2^8 \cdot 2^9 \cdot 2^{10} + 2^8 \cdot 2^9 \cdot 2^{10}$
D1	$2^8 \cdot 2^9 \cdot 2^{10} + 2^8 \cdot 2^9 \cdot 2^{10}$

COARSE SWITCH CONTROL SIGNALS	
SIGNAL	EQUATION
DC12	2^9
DC11	2^{10}
DC10	2^{11}
DC9	2^{12}
DC8	$2^{15} (2^{14} \cdot 2^{13} + 2^{14} \cdot 2^{13})$
DC7	$2^{15} (2^{14} \cdot 2^{13} + 2^{14} \cdot 2^{13})$
DC6	$2^{15} (2^{14} \cdot 2^{13} + 2^{14} \cdot 2^{13})$
DC5	$2^{15} (2^{14} \cdot 2^{13} + 2^{14} \cdot 2^{13})$
DC4	$2^{15} \cdot 2^{14} \cdot 2^{13} + 2^{15} \cdot 2^{14} \cdot 2^{13}$
DC3	$2^{15} \cdot 2^{14} \cdot 2^{13} + 2^{15} \cdot 2^{14} \cdot 2^{13}$
DC2	$2^{15} \cdot 2^{14} \cdot 2^{13} + 2^{15} \cdot 2^{14} \cdot 2^{13}$
DC1	$2^{15} \cdot 2^{14} \cdot 2^{13} + 2^{15} \cdot 2^{14} \cdot 2^{13}$



NOTES:

1. Input signals to coarse and fine switch logic are for interconnection only and not for logic equations. The logic equations are written in terms of the read counter signals 2^0 through 2^{15}
2. The coarse and fine switch control signals that are listed in the equations but not shown on this logic diagram, are shown on the corresponding read counter register logic diagrams.
3. The low level (0 vdc) signal to a switch turns the switch on. A logic "1" in the CDU is a low level. The gates are therefore interpreted as NAND gates.

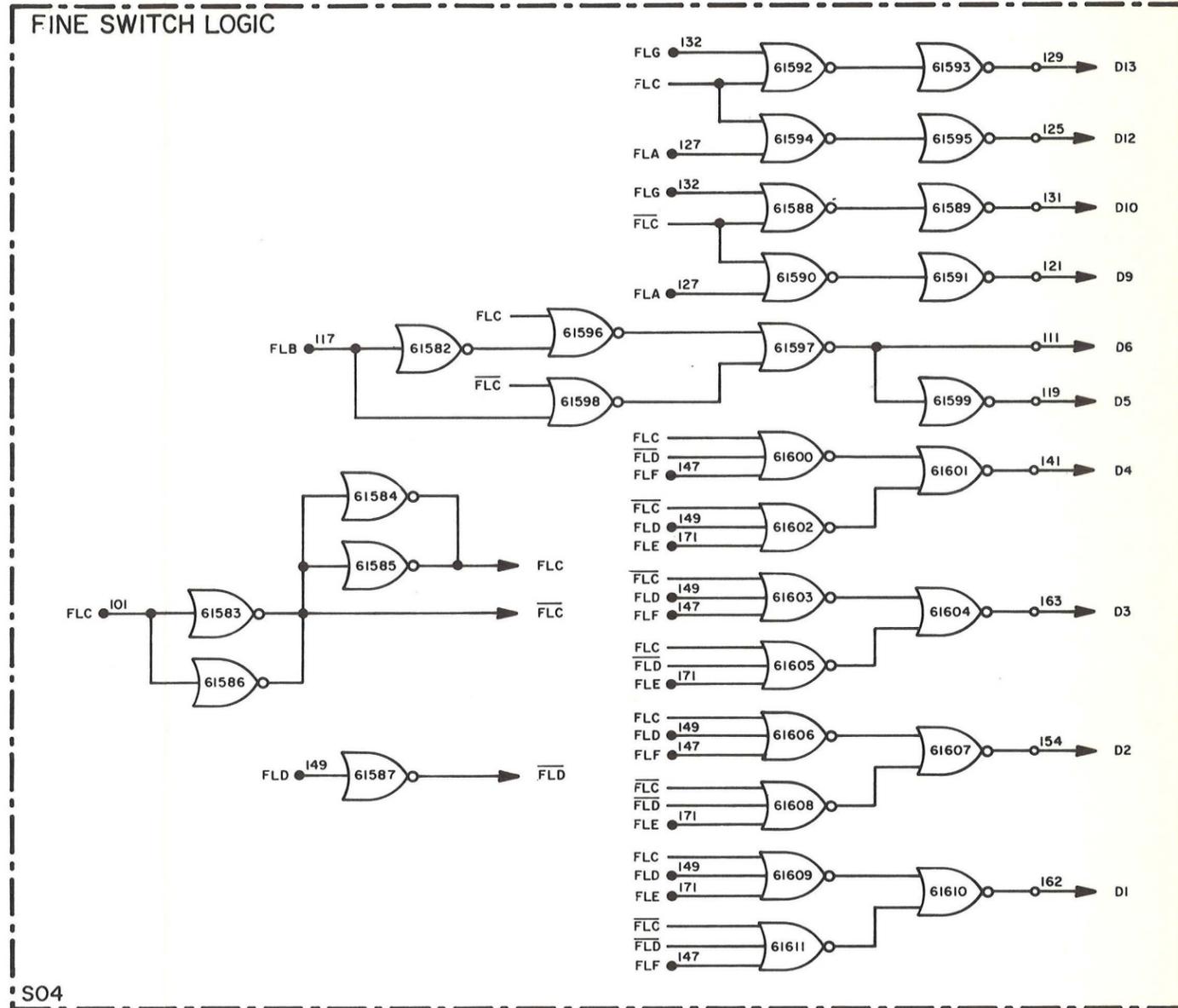
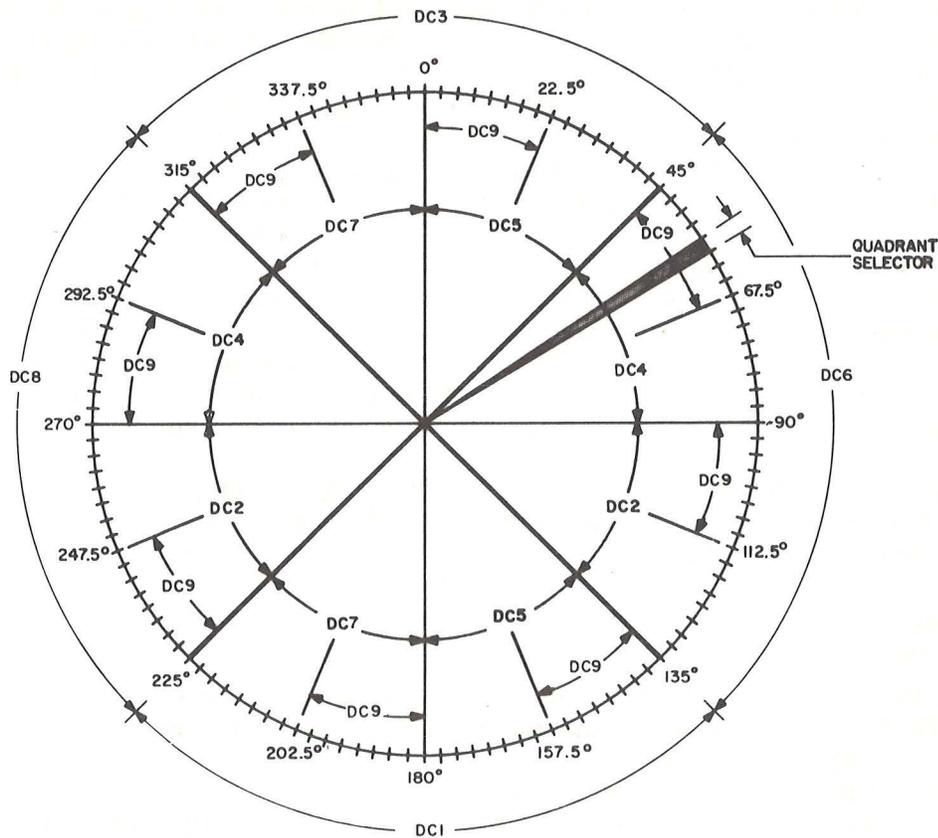


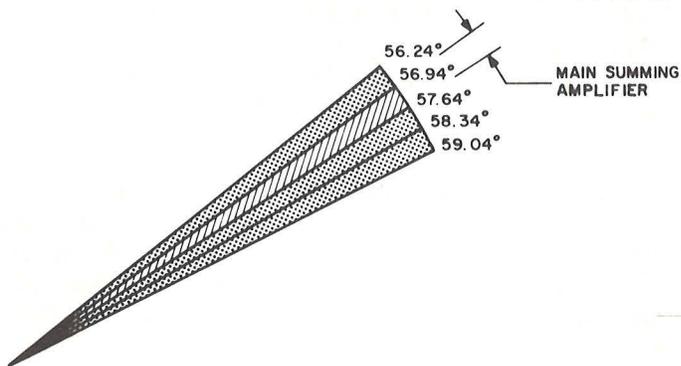
Figure 4-16K. Coarse and Fine Switch Logic, Logic Diagram

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM



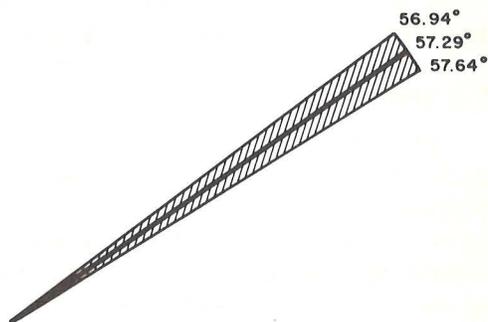
NOTE: COARSE SWITCH SIGNALS DC10—DC12 SELECT ONE OF 8 INCREMENTS EQUAL TO 2.81 DEGREES

COARSE SYSTEM MODULE



NOTE: FINE SWITCH CONTROL SIGNALS D1-D4 SELECT ONE OF 4 INCREMENTS EQUAL TO 0.7 DEGREE

QUADRANT SELECTOR



NOTE: FINE SWITCH CONTROL SIGNALS D15-D21 SELECT ONE OF 120 INCREMENTS EQUAL TO 0.0055 DEGREE

MAIN SUMMING AMPLIFIER

16479

Figure 4-16L. Coarse and Fine Switch Logic, Switching Diagram

Fine switch control signals D1 through D14 operate switches in the quadrant selector module to select attenuator values that divide the 2.81 degree segment (represented by switch control signals DC1 through DC12) into four parts, each equal to approximately 0.7 degree. Assume that the coarse switch control signals select the 2.81 degree segment between 56.24 and 59.04 degrees as shown in figure 4-16L. Assume further that D1 through D14 select the 0.7 degree segment between 56.94 and 57.64 degrees. D15 to D21 are then used to indicate the exact value of the read counter. The fine switch control signals operate the ladder switches in the MSA&QR module to divide each 0.7 degree segment into 128 segments, each equal to 0.0055 degree. The increment shown in figure 4-16L represents 57.29 degrees. For this value of read counter content the following coarse and fine switch control signals are present: DC6, DC4, DC10, D1, D5, D8, D11, D13, and D16 through D20. These signals are generated by the coarse and fine switch logic as a result of the read counter accumulating bits in stages 21, 22, 23, 24, 25, 27, 211, and 213 for a total accumulation representing 56.29 degrees.

An additional function of the coarse switch logic is the generation of the ambiguity reset signal for the ambiguity logic circuits in the digital mode module. The ambiguity reset signal is generated whenever a bit has been accumulated in the 2¹⁵ stage and bits are absent from the 2¹³ and 2¹⁴ stages. These conditions cause the ambiguity reset signal to be present when the value of the read counter content is between 180 and 225 degrees.

For the optics shaft and trunnion loops, the coarse switch control signals DC1 through DC8 are the same as the coarse control signals for the inertial loops. However, the optics shaft uses a 16X rather than a 1X resolver and the optics trunnion uses a 64X rather than a 1X resolver. Therefore, the 45 degree segments of the 16X or 64X resolvers (represented by DC1 through DC8) actually represent 5.6 degree segments of mechanical rotation for the optics shaft and 0.703 degree segments of mechanical rotation for the optics trunnion.

The optics shaft fine control signals D1 through D14 operate switches in the quadrant selector module to select attenuator switches that divide the optics shaft rotation 5.6 degree segment into four parts, each equal to approximately 1.4 degrees. The fine switch control signals operate the ladder switches in the MSA&QR module to divide each 1.4 degree segment into 256 segments, each equal to 0.0055 degree or 19.8 arc seconds.

The optics trunnion fine control signals D1 through D14 operate switches in the quadrant selector module to select attenuator switches that divide the optics trunnion rotation 0.703 degree segments into four parts, each equal to approximately 0.176 degree. The fine switch control signals operate the ladder switches in the MSA&QR module to divide each 0.176 degree segment into 256 segments, each equal to 0.00069 degree or 2.48 arc seconds.

4-4.6 ERROR ANGLE COUNTER AND LOGIC MODULE. The error angle counter and logic module contains the error angle counter (error counter), the logic circuits that control the operation of the error counter, and the logic circuits that control the operation of the read counter. A block diagram of the module is shown in figure 4-16M.

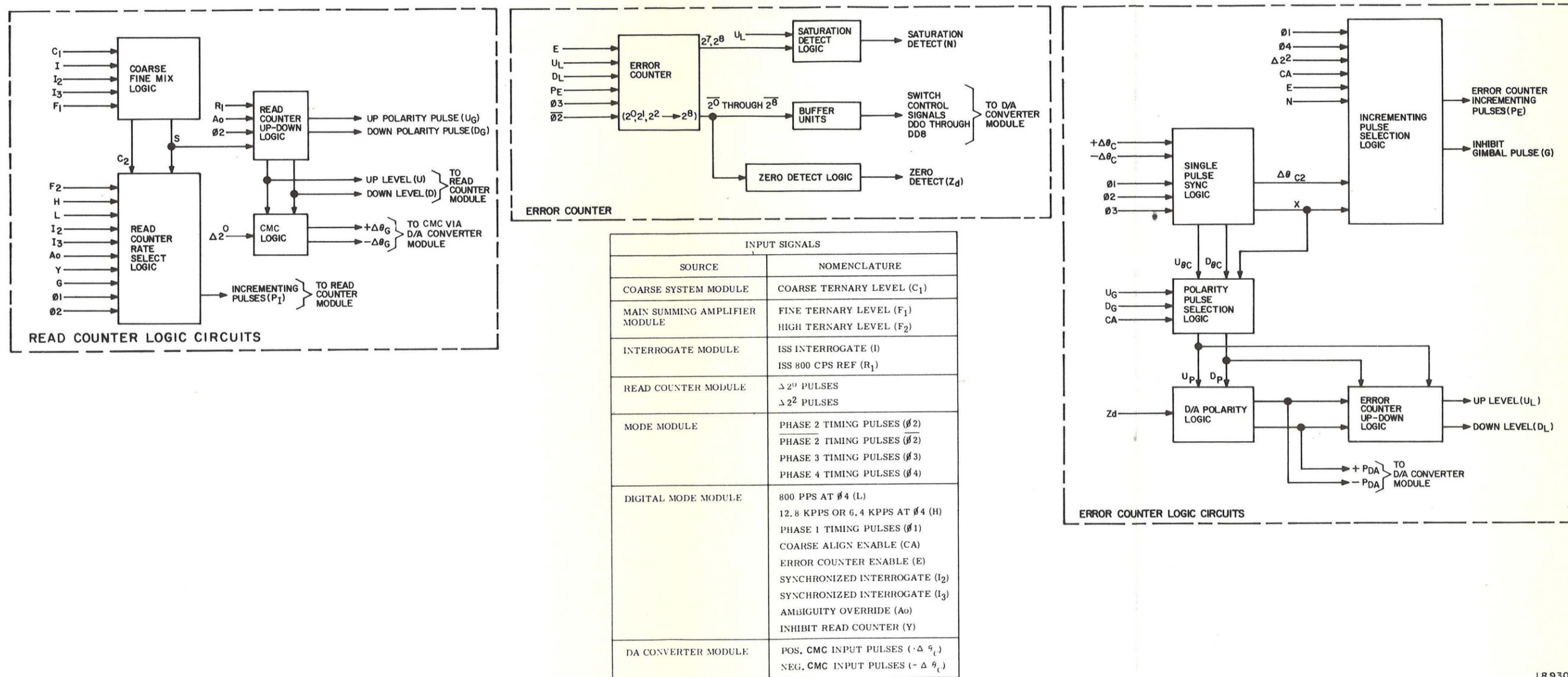


Figure 4-16M. Error Angle Counter and Logic Module, Block Diagram

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

The read counter logic circuits and the error counter logic circuits operate independently of each other except that some interface signals are generated during the inertial coarse align mode.

The read counter logic circuits detect the presence of A/D conversion system ternary level signals and, based on the type of signal detected, determine the proper counter direction and counting rate for the read counter. The read counter logic circuits include the inertial coarse-fine mix logic, optics mix logic, read counter up-down logic, CMC logic, and rate select logic.

The error counter functions with the D/A converter in the conversion of digital command pulses into an equivalent analog signal.

The error counter logic circuits synchronize incoming command pulses with CDU timing, establish the polarity of the D/A converter, command the error counter to count up or down, and generate incrementing pulses for the error counter. The error counter logic circuits include the single pulse sync logic, polarity pulse selection logic, D/A polarity logic, error counter up-down logic, and incrementing pulse selection logic.

4-4.6.1 Inertial Coarse-Fine Mix Logic. The coarse-fine mix logic (figure 4-16N) consists of three separate logic circuits which function together to detect the existence of either the coarse or fine ternary level signals and generate at interrogate time a selected error signal (S) having the same phase as the ternary level signal detected. S is then supplied to the read counter up-down logic and rate select logic circuits as an indication that a read counter error exists and that the read counter must be incremented in the proper direction at the proper rate until the error has been nulled out. The logic circuits included in the coarse-fine mix logic are the coarse select logic, the selected error logic, and the alternate pulse sync logic.

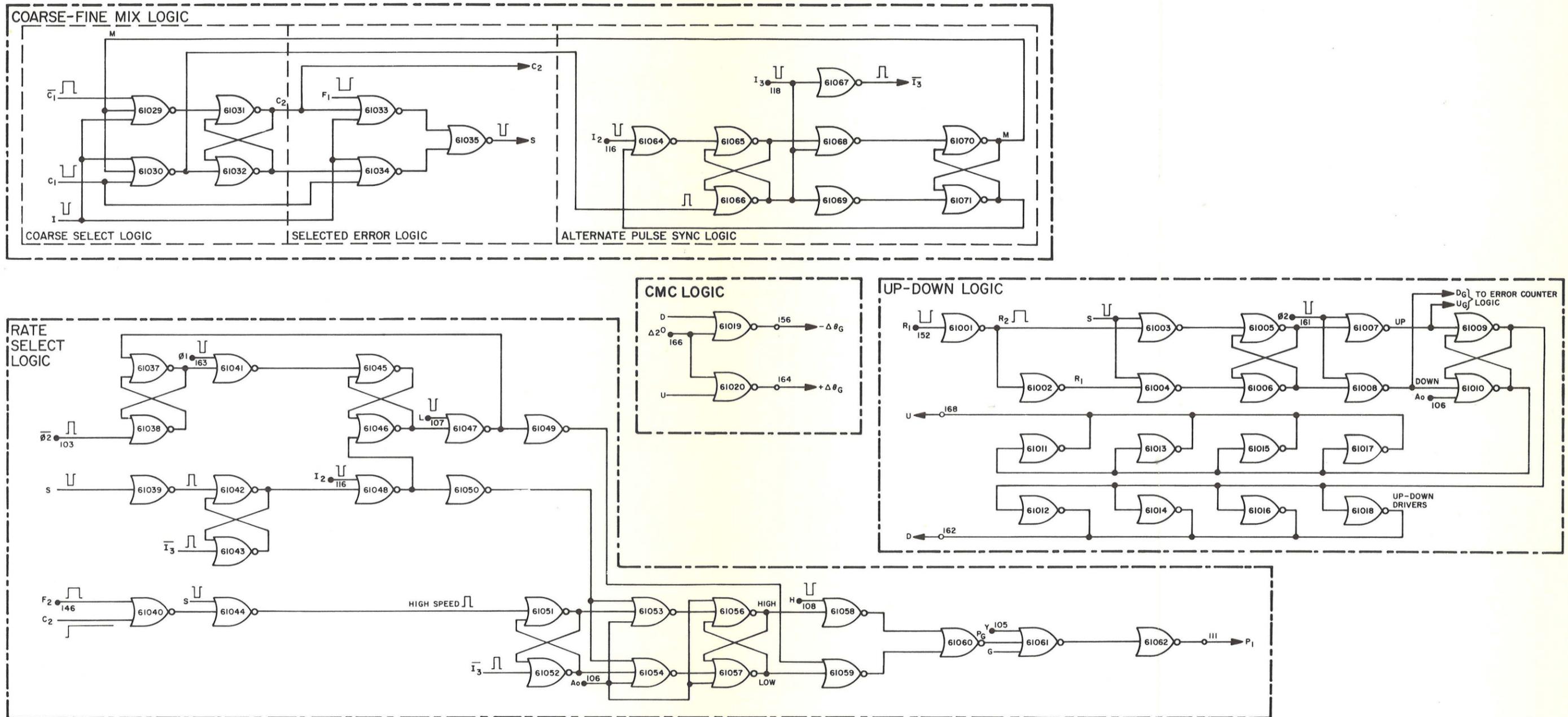
4-4.6.1.1 Coarse Select Logic. The purpose of the coarse select logic circuit is to detect the presence of the coarse ternary level signal (C_1). When C_1 is present, the coarse select logic produces a high speed clamp signal (C_2) that commands the rate select logic to send incrementing pulses at the high rate of 12.8 kpps to the read counter. C_2 is produced by ANDing the interrogate pulses (I) with C_1 in order to reset a flip-flop (gates 61031 and 61032). The output of the set side of the flip-flop is C_2 , supplied to the rate select logic circuit. An interrogate pulse train of 1600 pps is necessary within the selected error logic circuit in order to determine the phase of the 800 cps ternary level signals, but within the coarse select logic circuit the 1600 pps frequency creates a problem. Detection takes place and the coarse select flip-flop is reset on the first occurrence of I and C_1 , but if interrogation is allowed to take place on the second I, 1/1600 of a second later (at which time the 800 cps C_1 changes levels), the flip-flop changes state, resulting in possible erratic operation of the A/D conversion systems. Interrogation is inhibited on alternate interrogate pulses by the application of an inhibiting signal at the input of the coarse select logic circuit. The inhibiting signal, referred to as the clamp next interrogate signal (M), is generated by the alternate pulse sync logic circuit in response to an indication from the coarse select logic circuit that detection has occurred. M is present at the input to the coarse select logic circuit at the I_3 time following the first I on which detection occurs, and

prevents the flip-flop from changing state on the second I. M is removed at the I₃ time following the second I, enabling interrogation to take place on the third I. The flip-flop can change state only on alternate interrogate pulses when M is absent. The requirements for alternate interrogation and the generation of M are discussed in more detail in the alternate pulse sync logic discussion.

4-4.6.1.2 Selected Error Logic. The purpose of the selected error logic circuit is to detect the presence of either C₁ or the fine ternary level signal (F₁) and to produce S with the same phase as the ternary level signal detected at interrogate time. S is required by the up-down logic and the rate select logic circuits to determine the proper direction and rate at which the read counter is incremented. In order to prevent erratic operation of the A/D conversion systems, priority must be given to C₁ to allow it to have complete control of the analog to digital conversion operation until such time as the read counter error is low enough to have the fine A/D conversion system take control. The means of assuring priority for C₁ is the application of C₂ from the coarse select logic circuit. C₂ is a steady state signal that exists for as long as C₁ does. Application of C₂ to the selected error logic circuit, in effect, inhibits the application of F₁. The ternary level signals are detected by ANDing them with the interrogate pulse train. Since only one ternary level signal can be transmitted through the logic circuit, S will have the same phase as C₁ if C₁ is present, or will have the same phase as F₁ if C₁ is not present.

4-4.6.1.3 Alternate Pulse Sync Logic. The alternate pulse sync logic circuit generates M which operates on the coarse select logic circuit to inhibit complete interrogation. This is accomplished by preventing the coarse select flip-flop from changing state on alternate interrogate pulses. M assures that priority is given C₁ to control the analog to digital conversion operation for as long as C₁ exists. The normal CDU operation is to have C₁ and the coarse A/D conversion system in control until such time that C₁ is small enough to have F₂ and the fine A/D conversion system take control. While C₁ is in control, F₁ may be changing phase, at one instant in phase with C₁ and the next instant out of phase. Under these conditions, if complete interrogation (1600 pps) were allowed to take place in the coarse select logic circuit, the A/D conversion system would operate erratically, counting up or down at high speed when interrogating C₁ of a particular phase, and counting in the opposite direction at low speed at the next interrogate time (1/1600 second later) if F₁ of the opposite phase is present. The alternate pulse sync logic prevents this erratic operation by generating M on receipt of an indication from the coarse select logic circuit that C₁ is detected. Application of M at the coarse select logic circuit results in the production of C₂ which holds the rate select logic at the high incrementing rate and prevents the interrogation of F₁ by the selected error logic circuit. In this manner C₁ is given priority to control the A/D conversion system operation.

M is generated as a function of the I₂ and I₃ phase pulses. The I₂ and I₃ pulses occur at the next $\emptyset 2$ and $\emptyset 3$ times, respectively, following the occurrence of I. The alternate pulse sync logic consists of two flip-flops and associated input gates. On receipt of the indication from the coarse select logic that C₁ is detected, the first flip-flop is reset. This enables the I₃ pulse that follows I to reset the second flip-flop which then applies M to the coarse select logic circuit. The next I₂ pulse, which occurs after the second I, sets the first flip-flop, enabling the next I₃ that follows



18931

Figure 4-16N. Read Counter Logic Section, Logic Diagram

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

to set the second flip-flop and remove M. In this manner M is present at the input of the coarse select logic circuit from the I_3 time following the first I causing detection, and remains until the I_3 time following the second I. On the third I and alternate pulses thereafter, detection again occurs and the process is repeated until C_1 no longer exists.

4-4.6.2 Optics Mix Logic. The optics channels do not have coarse-fine mix logic since the error angle counter and logic module does not receive the coarse ternary level signal (C_1). Therefore, only the fine ternary level signal (F_1) and the interrogate pulses produce the error signal (S) with the same phase as F_1 .

4-4.6.3 Read Counter Up-Down Logic. The read counter up-down logic circuit (figure 4-16M) decides in which direction the read counter counts. It tests the phase of S (generated by the error selection logic circuit) by comparing it with the 800 cps reference signal (R_1). If S is out of phase with respect to R_1 , an up level command (U) is generated causing the read counter to be counted up. When S is in phase with respect to R_1 , a down level command (D) is generated causing the read counter to be counted down. The U and D commands are synchronized with the $\emptyset 2$ timing pulses. If the phase of the selected error causes a change in counting direction, the U and D level commands change simultaneously to opposite polarities at $\emptyset 2$ time allowing the read counter to count in the proper direction at the next $\emptyset 4$ incrementing pulse.

An additional controlling input to the read counter up-down logic circuit is the ambiguity override signal, A_o . If the gimbals are in the ambiguity zone (approximately 135 to 225 degrees) following the CDU zero mode, A_o is generated and, when present at the read counter up-down logic circuit, causes a D command to be generated. (The ambiguity logic is not used for the optics shaft and trunnion channels.)

The U and D commands are also supplied to the CMC logic circuit and are used as the controlling inputs for the transfer of $\pm \Delta \theta_G$ pulses to the CMC. The U command line is applied to the mode module and is monitored by the fail detect circuits for excessive read counter limit cycle frequency.

The read counter up-down logic circuit also generates up pulses (U_G) and down pulses (D_G) which are supplied to the error counter polarity pulse selection logic circuit as controlling inputs. The U_G and D_G are unaffected by the presence or absence of A_o , but are synchronized with the $\emptyset 2$ timing pulses.

4-4.6.4 CMC Logic. The CMC logic circuit (figure 4-16N) transfers $\pm \Delta \theta_G$ to the CMC. The CMC logic circuit receives the $\Delta 2^0$ pulses from the first stage of the read counter. Since $\Delta 2^0$ pulses represent only the amount of change in gimbal or optics angle and not the direction of change, they are ANDed with U and D from the read counter up-down logic circuit. With the presence of U and $\Delta 2^0$, the CMC logic circuit sends $+\Delta \theta_G$ to the CMC and, in the same manner, sends $-\Delta \theta_G$ when a $\Delta 2^0$ and D are present.

4-4.6.5 Rate Select Logic. The rate select logic circuit (figure 4-16N) provides the read counter with incrementing pulses. The incrementing pulses are at the high rate of 12.8 kpps when the read counter error is more than 0.1 degree and at the low rate of

800 pps when the read counter error is less than 0.1 degree. During the coarse align mode the high rate is changed from 12.8 kpps to 6.4 kpps. Both the high rate and low rate incrementing pulses are $\emptyset 4$ pulses.

The incrementing pulses (P_I) are generated within the rate select logic circuit as drive pulses (P_G). P_G is sent to the read counter as P_I only if the inhibit read counter command (Y) is not present and the inhibit gimbal pulse command (G) is not present. Command Y is generated in the moding sync logic circuit in the digital mode module during the CDU zero mode at which time it is necessary to prevent the read counter from incrementing. G is generated by the pulse selection logic circuit whenever the error counter receives $\pm \Delta\theta_C$ from the CMC. Since $\pm \Delta\theta_C$ pulses have priority over the gimbal feedback pulses ($\Delta 2^2$) from the read counter, $\Delta 2^2$ must be inhibited when $\pm \Delta\theta_C$ pulses are being received. The $\Delta 2^2$ pulses are inhibited by inhibiting the incrementing pulses to the read counter.

The high rate of P_G is generated whenever S is present together with either F_2 from the MSA&QR module or C_2 from the coarse select logic circuit. The high rate of P_G is also generated whenever A_0 is present. A_0 is present following the CDU zero mode if the gimbal is within the ambiguity zone (approximately 135 to 225 degrees). A_0 causes the read counter up-down logic to generate D , resulting in the read counter counting down at the high rate until the read counter is out of the ambiguity zone, removing A_0 . The high rate of P_G is synchronized with the 12.8 kpps ($\emptyset 4$) pulse train (H) from the digital mode module. During the coarse align mode the 12.8 kpps synchronizing pulses are inhibited and replaced by a 6.4 kpps pulse train within the digital mode module. The 6.4 kpps pulse train is generated by the countdown circuit in the digital mode module.

The high rate of P_G for the optics is generated whenever S is present with F_2 from the MSA&QR module.

The low rate of P_G is generated whenever S is present and no other conditions for the generation of the high rate have been met. The low rate of P_G is synchronized to the 800 pps $\emptyset 4$ pulse train (L) generated by the count down circuit in the digital mode module.

The rate select logic circuit also receives the I_2 and I_3 interrogate pulses and the $\emptyset 1$ and $\emptyset 2$ pulse trains, all of which function to allow a change from one rate to the other at the I_2 time preceding the next H or L synchronizing pulse, or upon receipt of A_0 .

4-4.6.6 Error Counter. The error counter is a nine stage binary counter. The nine stages, designated 2^0 through 2^8 , provide an apparent capability of accumulating 2^9 , or 512 pulses, but the counter is logically mechanized to saturate at 384 pulses. The first three stages are shown in figure 4-16N. The error counter functions with the D/A converter in the conversion of digital command pulses into an equivalent analog signal. The digital pulses are issued by the CMC and stored in the error counter during the coarse align mode, attitude error indication mode, and the display inertial data mode, during which times the pulses represent, respectively, the required change

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

in gimbal angle, the angular attitude error, and a quantity of command module velocity. The output of each stage of the error counter is buffered and used to control the operation of a ladder decoder switch in the D/A converter. The D/A converter analog output is proportional to the binary configuration of the nine ladder decoder switches and thus is equivalent to the accumulation of pulses in the error counter.

The inertial error counter can receive pulse inputs from the CMC or the third stage of the read counter during the inertial coarse align mode. Each pulse sent to the error counter from either source is equivalent to approximately 158 arc seconds or 0.0439453 degree (nominal). The largest possible error angle the error counter can contain is, therefore, 16.875 degrees. The optics error counter can receive pulse inputs from the CMC or the third stage of the read counter during OSS positioning of the optics. Each pulse sent to the error counter is equivalent to 158 arc seconds or 0.0439453 degree (nominal) for the shaft, or 19.8 arc seconds for the trunnion. The largest possible error angle the optics error counters can contain is 16.875 degrees for the shaft and 2.2 degrees for the trunnion. The contents of the error counter represent only the absolute value of the error angle. The sign of the error angle is determined by the polarity of the D/A converter output. All pulse inputs to the error counter are sent to logic circuits that sense the polarity of the pulses, establish the D/A converter polarity, determine the direction in which the error counter counts, and supplies incrementing pulses to the error counter. These logic circuits are not considered an integral part of the error counter itself and are discussed further under separate paragraph headings. Other logic circuits considered a part of the error counter are the buffer units, the zero detect logic, and the saturation detect logic, all of which are shown in figure 4-16O.

The error counter, like the read counter, has the capability of being counted up or down. The error counter, however, does not count down through zero. The up or down counting direction is established by the presence of zero volts on the up lines (UL) or down lines (DL), respectively. The error counter enable discrete (E) is applied to the reset inputs of the second flip-flop in each stage. When E is not present, the flip-flops are held in the reset state. When E is present, the error counter may be incremented.

The output from the reset side of the second flip-flop in each stage is applied to the buffer units and the zero detect logic. The logic diagram (figure 4-16O) shows only the first three stages of the error counter. The remaining stages are identical, with the exception of one additional output taken from each of the last two stages. In the 2⁷ and 2⁸ stages an output is taken from the set side of the second flip-flop and applied to the saturation detect logic.

The buffer units are single input gates that merely invert the outputs from each stage of the error counter to develop the switch control signals (DD0 through DD8) that operate the ladder decoder switches in the D/A converter. The buffer units shown in figure 4-16O are gates 61168, 61169, and 61170.

The zero detect logic circuit checks the contents of each stage of the error counter to detect a zero condition. The zero detect logic circuit is an extended NAND gate that receives an input from each of the nine stages. When all stages of the error counter contain a zero, a zero detect discrete signal is generated. The zero detect signal exists from the ϕ_4 time at which zero is reached until such future ϕ_4 time that the error counter receives one incrementing pulse. The zero detect signal and the polarity of the first CMC pulse received after zero are the controlling factors in establishing the polarity of the D/A converter output. The zero detect signal is also one of the controlling factors in preventing the error counter from being counted down from zero.

The saturation detect logic circuit which consists of a single gate checks the content of the 2^7 and 2^8 stages to detect saturation. When the error counter is in the process of being counted up and the 2^7 and 2^8 stages each contain a bit for a total accumulation of 384 bits ($128 + 256 = 384$), the error counter is saturated and the logic circuit generates a saturation detect signal which prevents additional incrementing pulses from being generated. The saturation detect signal exists from the ϕ_4 time at which saturation occurred until such future ϕ_2 time that the counting direction is changed from up to down. Removal of the saturation detect signal at ϕ_2 time allows the error counter to be decremented at ϕ_4 time to a lower value by the CMC or read counter feedback pulse that caused the change in count direction. The error counter is always held at zero when it is not being used. When a mode is commanded that requires the use of the error counter, E is issued by the CMC. After issuing E the CMC begins sending pulses which the error counter accumulates. The error counter is always incremented (counted up) from zero and contains an absolute value regardless of the polarity of the CMC pulses. The error counter is employed somewhat differently in each mode.

In the attitude error indication mode the CMC calculates the difference between the spacecraft attitude and the IMU angles, and converts this difference into pulses sent to the error counters. The contents of each error counter is decoded by the corresponding D/A converter into an ac analog signal that is sent to the FDAI. If, for example, the CMC sends positive pulses ($+\Delta\theta_C$) the error counter logic senses the polarity of $+\Delta\theta_C$, sends a positive polarity signal to the D/A converter, sends a count up command to the error counter, and increments the error counter to a magnitude equivalent to the absolute value of the attitude error. In this mode the only inputs to the error counter are the CMC pulses, since the feedback pulses from the read counter are inhibited. If command module movement causes the gimbal angle to decrease, decreasing the attitude error, the CMC sends a number of negative pulses ($-\Delta\theta_C$) to decrement the error counter and thereby decrease the magnitude of the D/A converter output. The logic circuits sense the change in pulse polarity, send the countdown command to the error counter, and decrement the error counter to the lower value. The polarity signal sent to the D/A converter is not changed since the error counter still contains a value greater than zero. The polarity signal sent to the D/A converter can change only when sufficient negative CMC pulses are sent to decrement the error counter to zero; then additional negative pulses are sent to increment the error counter to a new absolute value. This incrementing would occur, in the example given, when gimbal movement continued until the attitude error became zero and then increased to a

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

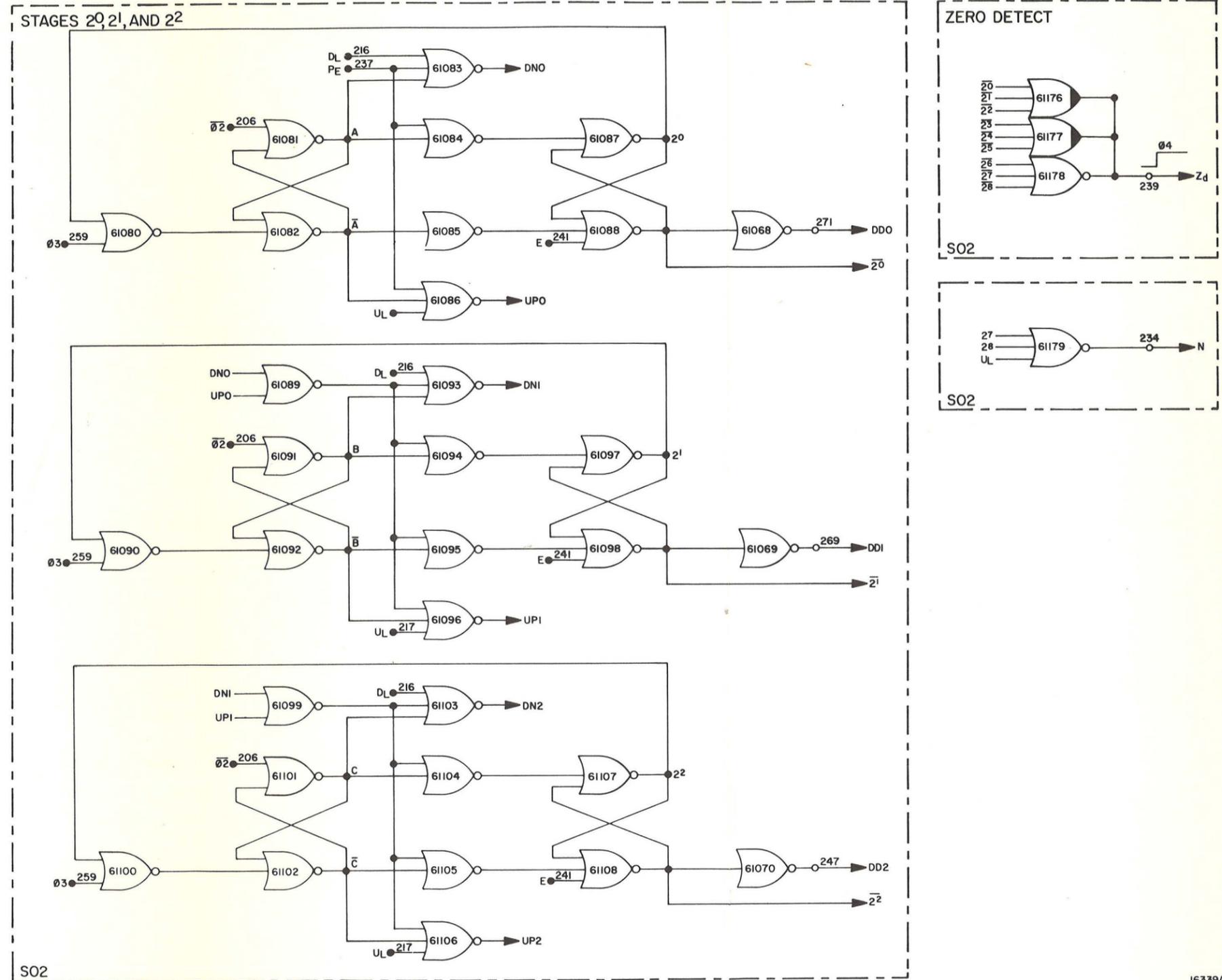


Figure 4-160. Error Counter

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

negative attitude error. The error counter logic circuits are conditioned by the zero detect signal to change the D/A polarity signal from positive to negative and to change the counting direction from down to up on the first $-\Delta\theta_C$ received after zero is reached. Oscillating movements of the gimbal may result in the contents of the error counter being constantly increased or decreased, the D/A polarity signal being changed only when the error counter reaches zero.

In the thrust vector control mode the optics error counters and D/A converters are used to supply a dc analog signal to the SPS engine gimbal amplifiers. In the S-4B takeover mode the ISS error counters and D/A converters are used to supply a dc analog signal to the Saturn guidance system for attitude control. During both modes the error counters and D/A converters are operated in the same manner as those in the attitude control mode, except that the CMC pulses represent a specific positive or negative quantity of spacecraft thrust along a trajectory.

In the coarse align mode the CMC sends the error counter a number of pulses equivalent to the required change in gimbal angle. If, for example, the CMC determines that a particular gimbal must be driven in a negative direction to a new angle, the CMC sends a number of negative pulses ($-\Delta\theta_C$) to the error counter logic. The $-\Delta\theta_C$ pulses cause a negative polarity signal to be sent to the D/A converter and cause the error counter to be incremented to a magnitude equivalent to the absolute value of the change in gimbal angle. The contents of the error counter are decoded by the D/A converter and the gimbal is driven toward the new angle. As the gimbal angle changes, the read counter sends feedback pulses ($\Delta\theta^2$) and polarity pulses to the error counter logic. These pulses count the CMC command out of the error counter and thus close the gimbal position loop. If the desired equivalent change in gimbal angle exceeds 384 pulses, the CMC cannot send all of the required pulses in one burst, since the error counter would be saturated and all pulses in excess of 384 would be lost. To prevent saturation, the CMC sends a portion of the required number of pulses in a burst, allows the gimbal to move reducing the contents of the error counter, and then sends a second burst. The CMC continues this process with as many bursts as necessary until the required number of pulses have been sent. The number of pulses per burst and the time between bursts are limited by the rate at which the gimbals are driven. The error counter logic gives priority to the incoming CMC pulses and prevents the read counter from incrementing and developing $\Delta\theta^2$ during the time a CMC pulse is being processed so that no feedback pulses are lost. After all CMC pulses have been sent, the read counter continues to send $\Delta\theta^2$ until the error counter has been decremented to zero, at which time the gimbal stops moving.

In the optics computer control mode the CMC sends the error counter a number of pulses equivalent to the required change in optics angle. The SXT is driven to the new position with the same loop operation as that explained for the inertial coarse align mode.

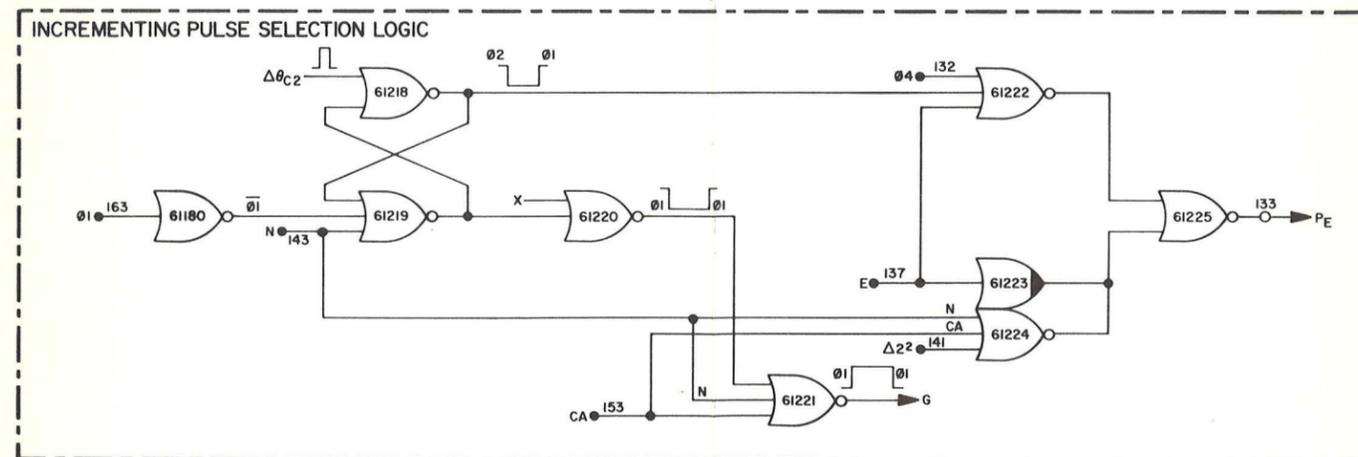
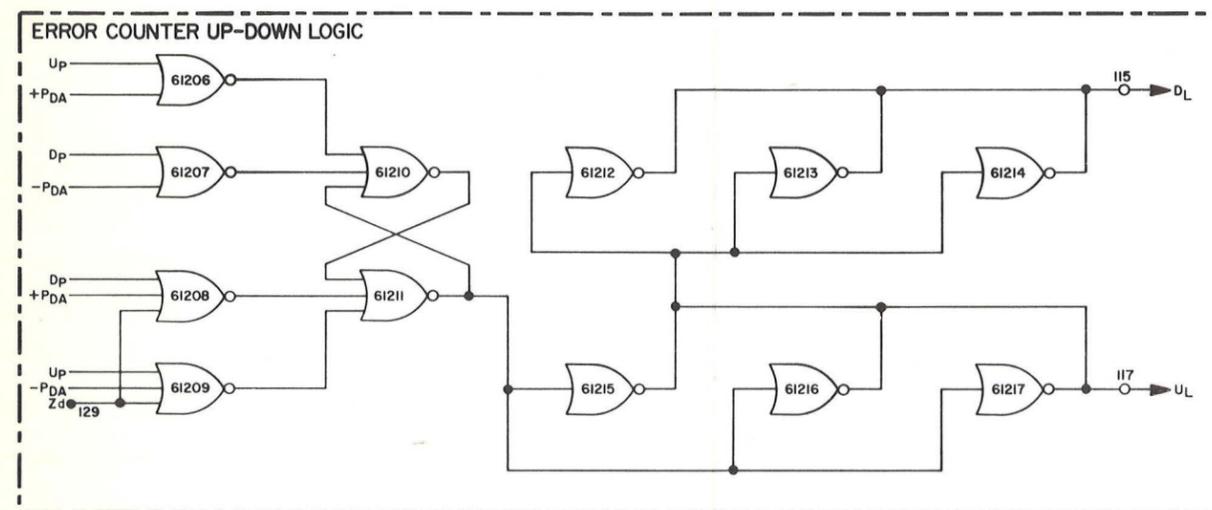
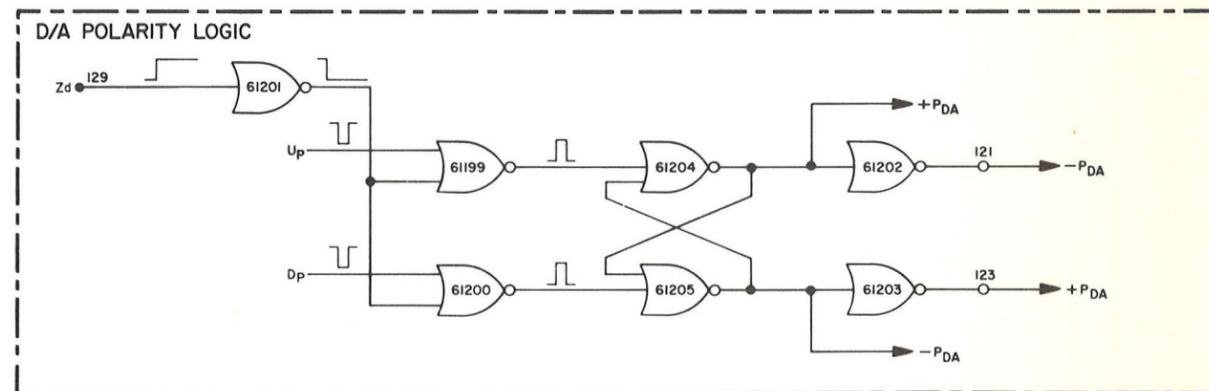
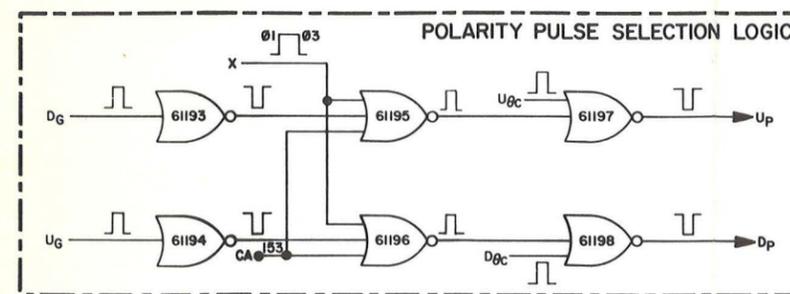
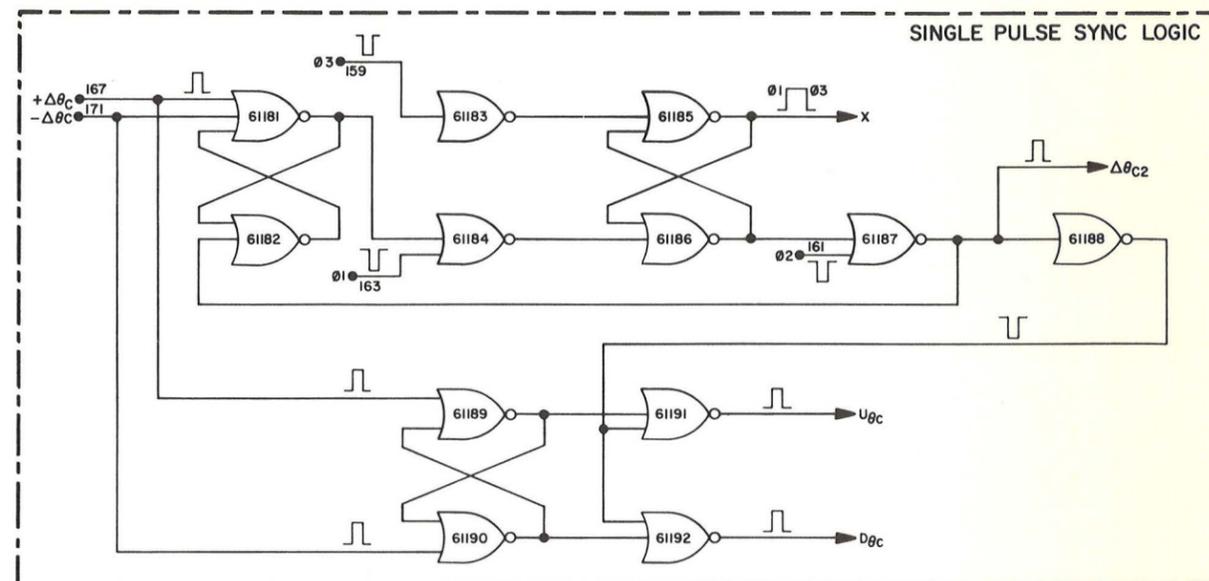
The various error counter logic circuits which control the operation of the error counter are described in detail in subsequent paragraphs.

4-4.6.7 Single Pulse Sync Logic. The single pulse sync logic (figure 4-16P) synchronizes the incoming CMC pulses with the CDU timing pulses. The CDU operates on the four 12.8 kpps phase timing pulse trains, $\phi 1$, $\phi 2$, $\phi 3$, and $\phi 4$. The CDU timing pulses are three microseconds wide and are synchronized with the 51.2 kpps CMC clock pulses. The CMC input pulses are three microseconds wide and are at a relatively slow rate of 3200 pps. While the CMC input pulses are also synchronized with CMC timing they have no specific phase relationship with the CDU timing pulses. The decision for the CDU error counters to count up or down must be made at $\phi 2$ time to allow the actual counting to take place at $\phi 4$ time. To meet these requirements the CMC input pulses must be synchronized to a specific phase relationship with the CDU timing pulses.

The single pulse sync logic detects the presence of an CMC pulse and generates a corresponding $\phi 2$ pulse. Both positive ($+\Delta\theta_C$) and negative ($-\Delta\theta_C$) CMC pulses are applied to the set side of a flip-flop (gates 61181 and 61182). When a pulse of either polarity is present it sets the flip-flop. The flip-flop, in effect, holds the pulse until the next $\phi 1$ timing pulse occurs, at which time the content of the flip-flop is transferred to a second flip-flop (gates 61185 and 61186) causing it to reset. The output from the reset side of the second flip-flop is ANDed with the next $\phi 2$ timing pulse to generate a single pulse ($\Delta\theta_{C2}$). The $\Delta\theta_{C2}$ pulse is transferred back to reset the first flip-flop and prepare it to accept the next CMC pulse. The $\Delta\theta_{C2}$ is applied to the incrementing pulse selection logic where it is used as one of the controlling inputs in the generation of error counter incrementing pulses. The second flip-flop is set on the next $\phi 3$ pulse. The output of the set side of the second flip-flop is, therefore, a 40 microsecond wide pulse that exists from the $\phi 1$ time following the receipt of a CMC pulse until the next $\phi 3$ time. This $\phi 1$ to $\phi 3$ pulse (X) is used by the polarity pulse and incrementing pulse selection logic to inhibit the application of read counter polarity pulses during the time a CMC pulse is being processed.

The incoming CMC pulses are also applied to a third flip-flop with $+\Delta\theta_C$ being applied to the set side and $-\Delta\theta_C$ being applied to the reset side. The contents of the third flip-flop are ANDed with the inverted $\Delta\theta_{C2}$ to produce polarity pulses $U_{\theta C}$ and $D_{\theta C}$, coincident with $\phi 2$ time. The presence of $+\Delta\theta_C$ sets the flip-flop and causes $U_{\theta C}$ to be generated. A $-\Delta\theta_C$ pulse will reset the flip-flop and cause $D_{\theta C}$ to be generated. Successive CMC pulses of the same polarity maintain the state of the flip-flop and the type of polarity pulse generated. $U_{\theta C}$ and $D_{\theta C}$ are applied to the polarity pulse select logic circuit where they are used as a factor in establishing polarities for the D/A converter and counting direction for the error counter.

4-4.6.8 Polarity Pulse Selection Logic. The polarity pulse selection logic (figure 4-16P) functions with the D/A polarity logic and the error counter up-down logic to establish polarities for the D/A converter and counting direction for the error counter. The polarity pulse selection logic generates polarity pulses U_p and D_p by selecting either $U_{\theta C}$ and $D_{\theta C}$ or U_G and D_G . U_G and D_G represent, respectively, the up and down counting directions of the read counter. The presence of these polarity pulses



16338A

Figure 4-16P. Error Counter Logic Circuits, Logic Diagram

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

merely indicates that a counting direction has been established even though the read counter may be inhibited. The read counter polarity pulses occur at a rate of 12.8 kpps. When either type of polarity pulse is present, it is coincident with $\emptyset 2$ time. The CMC polarity pulses occur on the $\emptyset 2$ time following the receipt of a CMC pulse. When both types of polarity pulses are present, the application of the read counter polarity pulses is inhibited by X (generated by the single pulse sync logic) which exists from the $\emptyset 1$ time following the receipt of a CMC pulse until the next $\emptyset 3$ time. In this manner the CMC polarity pulses are given priority over the read counter polarity pulses. An additional requirement placed on the selection of read counter polarity pulses is that the coarse align enable discrete (CA) be present, since the coarse align mode is the only ISS mode in which the digital feedback from the read counter is employed. Up and Dp are applied to the D/A polarity logic where they are used to establish the D/A converter polarity and are applied to the error counter up-down logic where they are used to determine the counting direction for the error counter.

4-4.6.9 D/A Polarity Logic. The D/A polarity logic (figure 4-16P) establishes the polarity or phase of the D/A converter output. The polarity or phase of the D/A converter can only be changed when the contents of the error counter are zero. The D/A polarity logic receives Up, Dp and the zero detect (Zd) signal. The presence of Zd and Up causes the flip-flop (gates 61204 and 61205) to set and apply a positive polarity signal (+PDA) to the D/A converter. The +PDA causes ac outputs from the D/A converter to be in-phase signals and in like manner causes the dc outputs to have positive polarity. Dp and Zd reset the flip-flop and apply a negative polarity signal (-PDA) to the D/A converter causing the D/A converter ac output to become pi phase and the dc output to have negative polarity.

4-4.6.10 Error Counter Up-Down Logic. The error counter up-down logic (figure 4-16P) commands the error counter to count up or down. The decision to count up or down is dependent on the type of polarity pulses received, the polarity established for the D/A converter, and the contents of the error counter. The error counter can be counted up from zero to saturation but may only be counted down when the error counter does not contain zero.

The count up command is established by the presence of Up together with +PDA, or by the presence of Dp together with -PDA. Either of the two conditions set the flip-flop (gates 61210 and 61211) and produce UL. The flip-flop resets and a count down command is generated when Dp and +PDA are present, or when Up and -PDA are present. In normal CDU operation the conditions for resetting the flip-flop and commanding the count down direction is never present when the error counter is zero because the polarity of PDA always results in the count up command being produced at zero. An additional assurance that the count down command is never produced at zero is provided by the application of Zd to the error counter up-down logic flip-flop. Zd is present as soon as the error counter reaches zero and inhibits the selection of the count down command until after the counter has been counted up one pulse.

Both UL and DL are taken from the reset side of the flip-flop. The output of the reset side is inverted once to produce UL and is inverted twice to produce DL. When a change in counting direction is commanded, UL and DL change simultaneously at $\emptyset 2$ time to opposite polarities.

To analyze the operation of the error counter up-down logic in conjunction with the polarity pulse selection logic and the D/A polarity logic, assume that the CMC has commanded an ISS mode other than the coarse align mode. The error counter is held at zero until the application of the error counter enable discrete when it is allowed to accept incrementing pulses. As long as the error counter remains in the zero state Z_d is present. The first CMC pulse received establishes polarity at θ_2 time for the D/A converter and maintains it until the error counter again returns to the zero state. If the first CMC pulse is positive ($+\Delta\theta_C$), U_{θ_C} is produced and it generates a U_p . Since Z_d is present U_p will produce $+P_{DA}$ and the count up command. If the first CMC pulse were negative ($-\Delta\theta_C$), D_{θ_C} , D_p , and $-P_{DA}$ would be generated in that order. The combination of D_p and $-P_{DA}$, however, also produces the count up command. As soon as the error counter receives one incremental pulse (at θ_4 time) Z_d is removed. Each additional CMC pulse generates U_p or D_p at θ_2 time. U_p and D_p cannot change the polarity of P_{DA} as long as the error counter does not contain zero. Additional CMC pulses can, however, change the counting direction of the error counter. Assume, for example, that the CMC had initially sent a number of $+\Delta\theta_C$ pulses to generate U_p , $+P_{DA}$, and the count up command and then began to send $-\Delta\theta_C$. The first $-\Delta\theta_C$ will generate D_p , D_p has no effect on the D/A polarity selection logic since it is inhibited by the absence of Z_d . D_p together with the initially established $+P_{DA}$ resets the flip-flop in the error counter up-down logic to produce the count down command. The count down command allows the incrementing pulse generated at θ_4 time to decrement the counter.

Assume that enough $-\Delta\theta_C$ pulses have been sent to return the error counter to zero. Z_d is again present and allows the first D_p produced (after reaching zero) to reset the flip-flop in the D/A polarity selection logic and produce $-P_{DA}$. The combination of D_p and $-P_{DA}$ sets the flip-flop in the error counter up-down logic to produce the count up command. The incrementing pulse that occurs at θ_4 increments the counter.

When the ISS is in the coarse align mode the coarse align enable discrete is present and allows U_G and D_G to effect the generation of U_p and D_p . Assume the CMC is in the process of sending a burst of $+\Delta\theta_C$ pulses to command a gimbal to move in a positive direction to a larger angle. The first $+\Delta\theta_C$ produces U_p , $+P_{DA}$, and the count up command. This initial condition allows the error counter to begin accumulating incrementing pulses. As the gimbal is driven towards the larger angle, the read counter up-down logic commands the read counter to count up and in the process produces U_G . U_G may be received at the error counter polarity pulse selection logic at the same time $+\Delta\theta_C$ is being received, between $+\Delta\theta_C$ pulses, or during the off period between bursts when no $+\Delta\theta_C$ pulses are being sent. If U_G is received at the same time as $+\Delta\theta_C$ is processed, $+\Delta\theta_C$ will be given priority by inhibiting the application of U_G . If U_G is received between $+\Delta\theta_C$ pulses or during the off period it will cause D_p to be generated. D_p has no effect on the D/A polarity selection logic since the error counter does not contain zero, but combined with $+P_{DA}$ resets the

flip-flop in the error counter up-down logic to produce the count down command. The $\Delta 2^2$ feedback pulse from the read counter now decrements the counter to a lower value. Each additional U_G and $\Delta 2^2$ continues to decrement the error counter until such time as another $+\Delta\theta_C$ is received. When another $+\Delta\theta_C$ is received, any U_G is inhibited and U_P is again produced to change the counting direction to up and increase the contents of the error counter. Since the read counter polarity and feedback pulses decrease the contents of the error counter between CMC pulses and during the off period between bursts, the total number of CMC pulses sent may exceed 384 without causing saturation if the average pulse rate is low enough. By sending an average pulse rate low enough to prevent saturation the CMC does not have to monitor gimbal movement to determine when pulses should be stopped.

4-4.6.11 Incrementing Pulse Selection Logic. The incrementing pulse selection logic (figure 4-16P) provides incrementing pulses to the error counter and an inhibit function to the read counter when a CMC pulse is received by the error counter logic circuits. Incrementing pulses (P_E) for the error counter will be generated at $\phi 4$ time in response to either the CMC pulses or $\Delta 2^2$ from the read counter.

Each time a CMC pulse is sent the incrementing pulse selection logic will receive a single pulse ($\Delta\theta_{C2}$) from the single pulse sync logic circuit at $\phi 2$ time. The presence of $\Delta\theta_{C2}$ sets the flip-flop (gates 61218 and 61219) in the incrementing pulse selection logic. The contents of the flip-flop are then ANDed with the next $\phi 4$ timing pulse and the error counter enable discrete (E) to produce an incrementing pulse. The flip-flop resets on the following $\phi 1$ pulse. Since the flip-flop sets at $\phi 2$ time and resets at the next $\phi 1$ time, the output of the reset side of the flip-flop is a positive pulse that exists from $\phi 2$ time until the next $\phi 1$ time. This pulse is ORed with X, received from the single pulse sync logic. Since X is a positive pulse (that exists from the $\phi 1$ time following the receipt of a CMC pulse until the next $\phi 3$ time), the resultant is a negative pulse that exists from the $\phi 1$ time after a CMC pulse until the next $\phi 1$ time. The $\phi 1$ to $\phi 1$ pulse is ANDed with the coarse align enable discrete and the absence of the saturation detect signal (N) to produce a positive pulse (G). This pulse applied to the read counter rate select logic, inhibits the generation of a read counter incrementing pulse on the $\phi 4$ time occurring between the aforementioned $\phi 1$ times. By preventing the read counter from incrementing in this time period, $\Delta 2^2$ pulses are inhibited giving $\Delta\theta_{C2}$ pulses priority over $\Delta 2^2$.

The $\Delta 2^2$ pulses received are ANDed with E, CA, and \bar{N} to produce incrementing pulses. CA is necessary since the coarse align mode is the only ISS mode in which digital feedback from the read counter is employed. The incrementing pulses generated are in response to a CMC pulse if one has been received, or in response to $\Delta 2^2$.

The saturation detect signal (N) prevents the error counter from counting up beyond 384 pulses. N exists only when a count up command is present and 384 pulses are stored in the error counter. N then remains until a CMC pulse or a read counter polarity pulse is received that can cause the count direction to be commanded.

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

4-4.7 INTERROGATE MODULE. The interrogate module generates a portion of the timing pulses required for CDU operation, produces optics 14 vdc power, and has pulse driver circuitry for data and pulse transmission. The interrogate module provides the following outputs:

- (1) 51.2 kpps pulse train to the digital mode module.
- (2) 1,600 pps interrogate pulse train used in the CDU ISS channels.
- (3) 800 pps $\angle 0^\circ$ reference signal to the ISS inner, middle, and outer error counter and logic module and to the digital mode module.
- (4) 1,600 pps shaft and trunnion interrogate pulses.
- (5) 14 vdc power (optics).
- (6) 25.6 kpps pulse train to 4 vdc trunnion and shaft power supply module.
- (7) 800 pps $\angle 45^\circ$ and 800 pps $\angle 0^\circ$ reference to the optics error counter and logic modules and digital mode module.

4-4.7.1 14 vdc Power Supply. The interrogate module contains two identical 14 vdc power supplies. The input power for the power supplies is 28 vdc. The power supply consists of a single transistor whose bias level is controlled by a zener diode. The 14 volt output is taken from the emitter resistor of the transistor. One 14 vdc power supply provides 14 vdc to the mode module, to the optics D/A converters, and to the CDU test connector for the optics axes. The output of the second 14 vdc supply is used entirely within the interrogate module, providing 14 vdc to the pulse driver circuits.

4-4.7.2 ISS Reference Generator. The ISS reference generator develops an 800 pps square wave voltage of 0 degree phase for use as a reference by the ISS error counter and logic modules and by the digital mode module. The signal input is voltage from the ISS 28 v (rms), 800 cps, 1 percent power supply applied through a 5 to 1 stepdown transformer. The positive half cycles are detected and used to drive a transistor. The output of the transistor is an inverted 800 pps square wave.

4-4.7.3 Optics Reference Generator. The optics reference generator provides 0 degree phase and 45 degree phase reference signals of 800 pps. The 0 degree phase reference signal is supplied to the optics shaft error counter and logic module. The 45 degree phase reference signal is used for the optics trunnion error counter and logic module. The 0 degree phase reference signal is generated in the same manner as the ISS 0 degree phase reference signal. The 45 degree phase reference signal also is obtained in the same manner except that the phase of the 800 cps signal input is first shifted 45 degrees.

4-4.7.4 ISS Interrogate Generator. The ISS interrogate generator provides a 1,600 pps, 3 microsecond pulse width pulse train to the digital mode module and the inner gimbal, middle gimbal, and outer gimbal error counter and logic modules.

The input to the ISS interrogate generator is an ISS 28 v (rms), 800 cps voltage which is applied through a 5 to 1 stepdown transformer. The 5.6 volt signal phase is shifted 90 degrees by a resistance, capacitance, and transistor phase shift network. The phase shifted signal is used to key a square wave generator. The symmetrical square wave output of the square wave generator is applied to a differentiating circuit where the leading edge of the square wave is differentiated and inverted. The trailing edge of the square wave is differentiated only. In this manner two signals are obtained which are then combined to key a transistor output stage that develops the 1,600 pps, 3 microsecond pulse width pulse train output coincident with the peaks of the 800 cps signal.

4-4.7.5 Shaft Interrogate Generator. The shaft interrogate generator provides a 1,600 pps, 3 microsecond pulse width pulse train to the optics shaft error counter and logic module and to the digital mode module. The operation of the shaft interrogate generator is the same as the ISS interrogate generator.

4-4.7.6 Trunnion Interrogate Generator. The trunnion interrogate generator provides a 1,600 pps, 3 microsecond pulse width pulse train to the optics trunnion error counter and logic module and to the digital mode module.

The input to the trunnion interrogate generator is a 90 degree phase shifted trunnion $\cos(\theta - \psi)$ signal from the main summing amplifier and is used to key a square wave generator. The operation of the trunnion interrogate square wave generator is the same as the ISS interrogate square wave generator.

4-4.7.7 Buffer Transformer. A 2 to 1 buffer transformer located in the interrogate module routes the 51.2 kpps pulse train from the CMC to the clock pulse generator in the digital mode module.

4-4.7.8 25.6 kpps Pulse Driver. The 25.6 kpps pulse driver circuit routes a 25.6 kpps pulse train from the digital mode module to the 4 vdc power supply where it is used for synchronization purposes. The output of the transistor pulse driver is transmitted through a 2 to 1 buffer transformer.

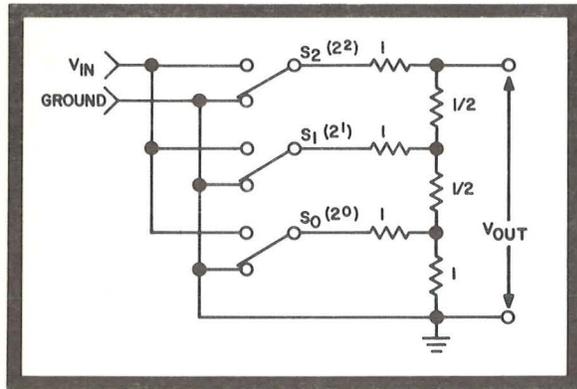
4-4.8 DIGITAL TO ANALOG CONVERTER. The ISS D/A converter converts digital information from the error counter into a dc analog signal and two ac analog signals. One ac signal provides attitude error information to the FDAI. The second ac signal is the coarse align error signal supplied to the gimbal servo amplifiers during the coarse align mode. The dc signal is used during S-4B take-over mode for control of the Saturn booster vehicle by the PGNCS. The OSS D/A converter converts digital information from the error counter into a dc analog signal and an ac analog signal. The ac signal is the positioning signal for the optics shaft and trunnion and is applied to the optics servo loops. The dc signal is used during the thrust vector control mode to provide positioning signals to the service propulsion system engine gimbals.

The D/A converter consists of a voltage ladder decoder, a scaling amplifier, a demodulator, and a mixing amplifier. The conversion of digital information into a dc analog signal by the D/A converter is accomplished in essentially two steps. The digital information is first converted into an 800 cps analog signal by the ladder decoder. The ac signal is then converted to a dc analog signal by a demodulator that rectifies and filters the ac. Before being applied to the demodulator or being used as a direct ac output, the ac signal is routed through the scaling amplifier which controls the gain of the signal. The mixing amplifier combines a feedback signal with the ac analog signal to produce the ac analog output signal.

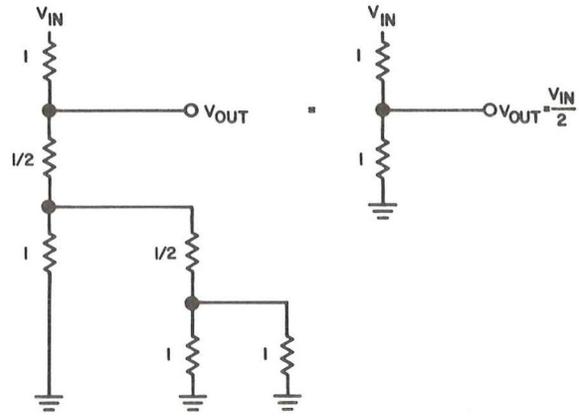
The D/A converter also contains pulse driver circuits and buffer transformers which route the $\pm \Delta\theta G$ pulses from the read counter through the error counter and logic module to the CMC and the $\pm \Delta\theta C$ pulses from the CMC to the error counter and logic module.

4-4.8.1 Ladder Decoder. Accumulated data bits in the error counter control the operation of transistor switches that apply either an ac ground or 800 cps of proper phase to the ladder resistors. In this manner, a voltage proportional to the binary configuration of the switches is developed across the ladder network. For simplicity, the operation will be explained using the 3 bit converter shown at the upper left of figure 4-17; however, the theory of operation presented applies to the 9 bit converter employed by the CDU.

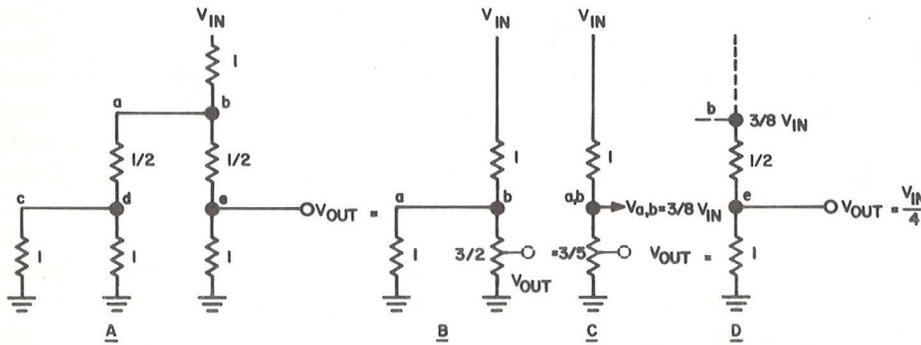
Switches S_2 , S_1 , and S_0 represent transistor switches which are activated by the three data bits from the error counter. (The switch drive circuitry is not shown.)



SIMPLIFIED 3 BIT CONVERTER



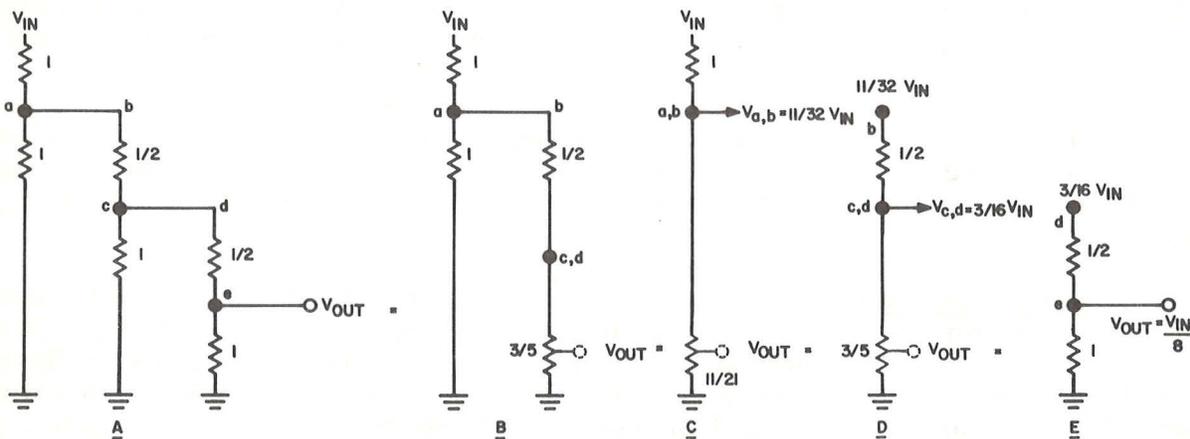
CASE I. SWITCH S_2 CLOSED



CASE 2. SWITCH S_1 CLOSED

S_2	S_1	S_0	
2^2	2^1	2^0	
0	0	1	$1/8 V_{IN}$
0	1	0	$1/4 V_{IN}$
0	1	1	$3/8 V_{IN}$
1	0	0	$1/2 V_{IN}$
1	0	1	$5/8 V_{IN}$
1	1	0	$3/4 V_{IN}$
1	1	1	$7/8 V_{IN}$

TRUTH TABLE



CASE 3. SWITCH S_0 CLOSED

15755A

Figure 4-17. Simplified 3 Bit Converter and Switch Configurations

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

Switch S_2 is closed by a logic 1 (0 volt) in the most significant bit position (100) and has a binary weight of 2^2 . Switch S_1 is closed by a logic 1 in the next most significant bit position (010) and has a binary weight of 2^1 . Switch S_0 is closed by a logic 1 in the least significant bit position (001) and has a binary weight of 2^0 .

If the data bits from the error counter are 100, switch S_2 is closed and applies the 800 cps input voltage (V_{IN}) to the ladder. The remaining switches are left in their normally open position and apply ground. The configuration of the ladder resistors is like that shown in Case 1 (A) of figure 4-9. The solution of the series and parallel groups of resistances shows the resistance above and below the output point to be 1 (as shown in the equivalent circuit B). Therefore, the input voltage V_{IN} is divided by 2 and applied to the scaling amplifier.

With databits 010, switch S_1 is closed and the remaining switches open; the resistor configuration is like that shown in Case 2 (A) of figure 4-9. Combining series and parallel resistances produces the equivalent circuit progression A through D. The voltage at point ab is determined first and applied to point b. The simple divider ratio of resistances above and below the output point is then used to find the output voltage as shown in the final equivalent circuit D. The output voltage shows that V_{IN} is divided by 4 and applied to the scaling amplifier.

With data bits 001, switch S_0 is closed and the remaining switches open; the resistor configuration is like that shown in Case 3 (A) of figure 4-9. Combining series and parallel resistances produces the equivalent circuit progression A through E. The voltage at point ab is found first and applied to point b. In the same manner the voltage cd is found and applied to point d. The output voltage is then found from the divider ratio in the final equivalent circuit E. The output voltage shows that V_{IN} is divided by 8 and applied to the scaling amplifier.

If a combination of switches is closed at the same time, the output voltage will be equal to the sum of the voltages found for each switch individually. For example, if switches S_2 and S_0 are closed simultaneously (by data bits 101), the output voltage would be:

$$\frac{V_{IN}}{2} + \frac{V_{IN}}{8} = \frac{5V_{IN}}{8}$$

The remaining combinations of switch configurations possible from three data bits is shown in the truth table in figure 4-9. In each case the 800 cps output has an amplitude proportional to the data bit controlled switches.

In the actual transistor switching circuit (the remainder of the D/A converter discussion will refer to circuitry shown on schematic 2010028) the data bit inputs to switches (DD0, DD1, etc.) are normally at a positive voltage (logic 0). Therefore, switch driver Q3 is on and ground is applied to the base of switch Q14 to keep it turned off. The ac ground is applied to the ladder resistor network through Q15 which is forward biased by the 3.3 volt zener voltage (applied to the emitter) from CR4 and by

ground applied to the base. If a logic 1 (0 volt) is applied to DD0, Q3 will turn off and Q14 will turn on applying 2.5 v (rms) 800 cps from T₁ to the ladder. The large positive voltage on the base of Q15 will turn off Q7 removing ac ground from the ladder. The theory of operation is the same for the remaining 8 switches.

The D/A converter receives 9 data bits from the error counter as inputs. The error counter also supplies a + and - polarity control signal to the D/A converter. These signals determine whether an in-phase or an out-of-phase 800 cps voltage will be applied to the ladder. This will in turn determine the phasing of the D/A converter ac output signals and the polarity of the D/A converter dc output signals. If a logic 1 is applied to the +D/A polarity input, Q13 turns off and Q12 turns on applying in-phase voltage to the ladder. If a logic 1 is applied to -D/A polarity input, Q1 turns off and Q2 turns on applying out-of-phase voltage to the ladder.

4-4.8.2 D/A Converter Output Stage. The D/A converter output stage consists of the demodulator, the scaling amplifier, and the mixing amplifier. The 800 cps amplitude modulated signal from the ladder is applied to the scaling amplifier and demodulator where the gain is controlled to produce a voltage gradient of 300 mvdc per degree at the output of the D/A converter. In the coarse align mode, the ac voltage from the scaling amplifier is applied as an input to the mixing amplifier.

The scaling amplifier consists of transistors Q33 and Q34 which, along with the feedback network, form an amplifier with an ac gain of approximately 3 to 4. The output of the scaling amplifier is applied to phase sensitive demodulator through transformer T₃. The full wave rectifiers, which consist of both sections of Q38 and Q39, are controlled by an 800 cps reference signal through T₄. If the ladder output is in phase with the reference signal, a positive error voltage will develop at the output of the rectifier. If the ladder output is 180 degrees out of phase with the 800 cps reference signal, a negative error voltage output is produced. The emitter to emitter connection of the transistor sections of Q38 and Q39 produces collector to emitter voltage drops of opposite polarity at each transistor section cancelling the overall voltage drop across the two sections of the transistor. The rectified ac is filtered and applied as the D/A converter dc analog signal. The scaling amplifier also provides an ac analog signal to the FDAI and to the mixing amplifier in the coarse align mode. Transistor Q32 provides a means of inhibiting the output of the D/A converter in case of 4 volt power supply failure. The inhibit action occurs when a logic 1 is removed from the inhibit D/A converter input causing Q32 to turn on and to short the input of the scaling amplifier to logic ground.

In the coarse align mode, the gimbals are limited to a maximum rate to prevent damage to the gyros and to allow the read counter to track the gimbal angle accurately. The fine error signal, $\sin 16(\theta - \psi)$ from the main summing amplifier, is fed back to rate limit the gimbals. The fine error signal is out of phase with the ladder output and has an amplitude proportional to the difference between the actual gimbal angle and the angle registered in the read counter. The fine error feedback signal is summed with

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

the ac output from the scaling amplifier to provide the input to the mixing amplifier. The output of the mixing amplifier is the coarse align error signal to be applied to the gimbal servo amplifiers during the coarse align mode.

4-4.9 MODE MODULE. The mode module is utilized as an interface module. The mode module contains circuits to buffer signals and monitor CDU operation. Direct interface is made between the mode module and the CMC and with other modules within the CDU. The mode module provides the following:

- (1) Buffered moding signals.
- (2) Four timing signals.
- (3) ISS and OSS fail signals.
- (4) ISS 14 vdc power supply input.
- (5) Thrust vector control signals.
- (6) Saturn booster vehicle control signals.

4-4.9.1 Moding Buffer Circuits. The moding buffer circuits receive signals from the CMC and from the digital mode module. These signals are inverted, amplified, or otherwise processed into moding signals to be sent to other modules of the CDU.

Figure 4-17A illustrates the moding buffers used for the ISS discrettes. The signals received from the CMC are five moding discrettes. The discrettes are 0.0 (± 2) vdc CMC ground, applied through a 2,000 ohm source impedance. The buffer circuits for four of the discrettes are identical. These discrettes are the ISS CDU zero, optics CDU zero, ISS error counter enable, and optics error counter enable. In each case the discrete biases a transistor inverter into conduction. The positive dc signal obtained from the inverter is then sent to the moding sync logic of the digital mode module. The fifth discrete, the coarse align enable, has a two stage buffer circuit consisting of an inverter and a relay driver transistor. The inverter has a dual output circuit which provides two positive dc output voltages upon receipt of the coarse align enable discrete from the CMC. One output is sent to the moding sync logic in the same manner as the previous four moding signals. The second output of the inverter stage is applied to the relay driver transistor, causing it to turn on. The relay driver provides a current path to ground which energizes the coarse align relays located in the PSA.

The signals received from the digital mode module are the ISS CDU zero drive and optics CDU zero drive signals. These signals are at positive dc voltage levels. The buffer circuits simply invert the signals and send them to other CDU modules.

4-4.9.2 14 vdc Power Supply. The 14 vdc power supply contained in the mode module is identical to the 14 vdc power supplies described in the interrogate module.

4-4.9.3 Phase Buffer Circuits. The phase buffer circuits (figure 4-17B) receive four phase pulse trains, designated ϕ_2 drive, $\overline{\phi_2}$ drive, ϕ_3 drive, and ϕ_4 drive, from the digital mode module. The buffer circuit for each pulse train is a transistor inverter powered by the 4 vdc power supply. All four inverted signals are sent to the error counter and logic module. The inverted $\overline{\phi_2}$ and $\overline{\phi_3}$ signals are also sent to the read counter module.

4-4.9.4 ISS-CDU Fail Detect Circuit. The ISS-CDU fail detect circuit monitors the tolerance of critical signals. The fail detect circuits can be considered as three independent failure detect and logic circuits, each monitoring a single type of CDU error. If an out-of-tolerance condition is detected by the circuits, a failure signal is applied to a common output OR circuit.

The first ISS-CDU error detect and logic circuit receives the inner, middle, and outer coarse error signals from the coarse system module, and the inner, middle, and outer fine errors from the main summing amplifier. These six signals are applied to a level detector consisting of six voltage divider networks and a common filter section. The input signals are attenuated, half-wave rectified, and filtered. The voltage level at the output of the filter section controls the conduction of an output transistor. If any of the coarse or fine errors exceed tolerance, the voltage level at the output of the filter section reaches a level sufficient to bias the output transistor into conduction. The output transistor in turn supplies a failure indication input to the common output OR circuit.

The second ISS-CDU failure detect circuit monitors the inner, middle, and outer read counter UP level signals to detect an excessive read counter limit cycle frequency. When the read counter alternately counts up, then down, the input transistor of the failure detect circuit alternately turns on and off. The output of the transistor is differentiated so a number of positive and negative pulses, corresponding to the frequency at which the counter changes direction, are developed. The positive pulses are detected and applied to a common filter section. By integrating the positive pulses the filter section develops an output level proportional to the frequency at which the counter changes direction. When the frequency exceeds tolerance, the output level of the filter section is sufficient to bias an output driver transistor into conduction. The driver transistor in turn supplies a failure indication to the common output OR circuit.

The third ISS-CDU failure detect circuit monitors the three $\cos(\theta - \psi)$ error signals from the inner, middle, and outer main summing amplifiers and also monitors the output of the 14 vdc power supply located in the mode module. Each of the three $\cos(\theta - \psi)$ signals is applied to an input transistor which conducts when the applied signal decreases below tolerance. When any of the three input transistors conduct, they turn off a fourth transistor which had been preventing the conduction of the output transistor. The proper state of each of the transistors in the circuit is established by bias levels derived from the 14 vdc supply. If the 14 vdc input decreases below tolerance, bias levels are changed sufficiently to result in the conduction of the output transistor. When the output transistor conducts, it supplies a failure indication to the common output OR circuit.

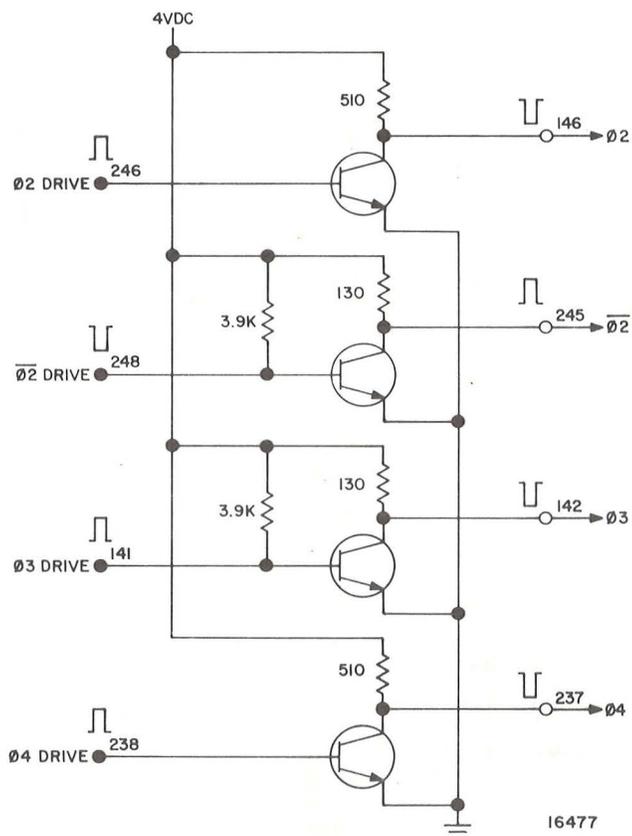


Figure 4-17B. Phase Buffers

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

The output OR circuit accepts inputs from the three failure detect circuits previously mentioned. The output transistors of those three circuits must conduct through the same resistor network so any of the three will develop a voltage drop across the resistor network. The voltage drop causes the conduction of the input transistor in the OR circuit. When this transistor conducts, it supplies an input to a time delay circuit consisting of a resistance-capacitance network and a zener diode. After approximately 7 seconds, the zener diode conducts, supplying proper bias to the output stage of the circuit which consists of two transistors. When the output transistors conduct, the circuit provides a positive 28 vdc CDU failure indication to the CMC.

4-4.9.5 Optics-CDU Fail Detect Circuit. The optics-CDU fail detect circuit functions in exactly the same manner as the ISS-CDU fail detect circuit. The only difference between the two circuits is that the optics-CDU fail detect circuit monitors the 14 vdc power supply located in the interrogate module and only two each from the cos ($\theta - \psi$), fine error, and limit cycle types of signals.

4-4.9.6 Moding Relays. Two sets of two relays are located in the mode module. One set is used to route signals for Saturn steering control after S-4B take-over. The other set of relays is used during the thrust vector control mode. The relays are energized by a CMC discrete acting through a relay driver. The energized relays route the dc error signals from the optics CDU D/A converter to the service propulsion system engine gimbal amplifiers and from the ISS CDU D/A converter to the Saturn guidance system.

4-5 POWER SUPPLIES

The power supplies convert the +28 vdc prime Block II command module power into the various dc and ac voltages required by the PGNCS. The +28 vdc prime power is supplied from the EPS. Prime power will be supplied to the 3,200 cps power supply during both standby and operate modes of the ISS, while it will be supplied to all other power supplies during the operate modes only.

All ac power supplies are synchronized to the CMC clock by means of computer pulses. The dc supplies, using multivibrators as ac sources for transformation, are also synchronized to the CMC. Synchronization is accomplished by a multivibrator which will free run at a lower frequency without the computer pulses, assuring operation of the ISS power supplies in the event of a CMC failure.

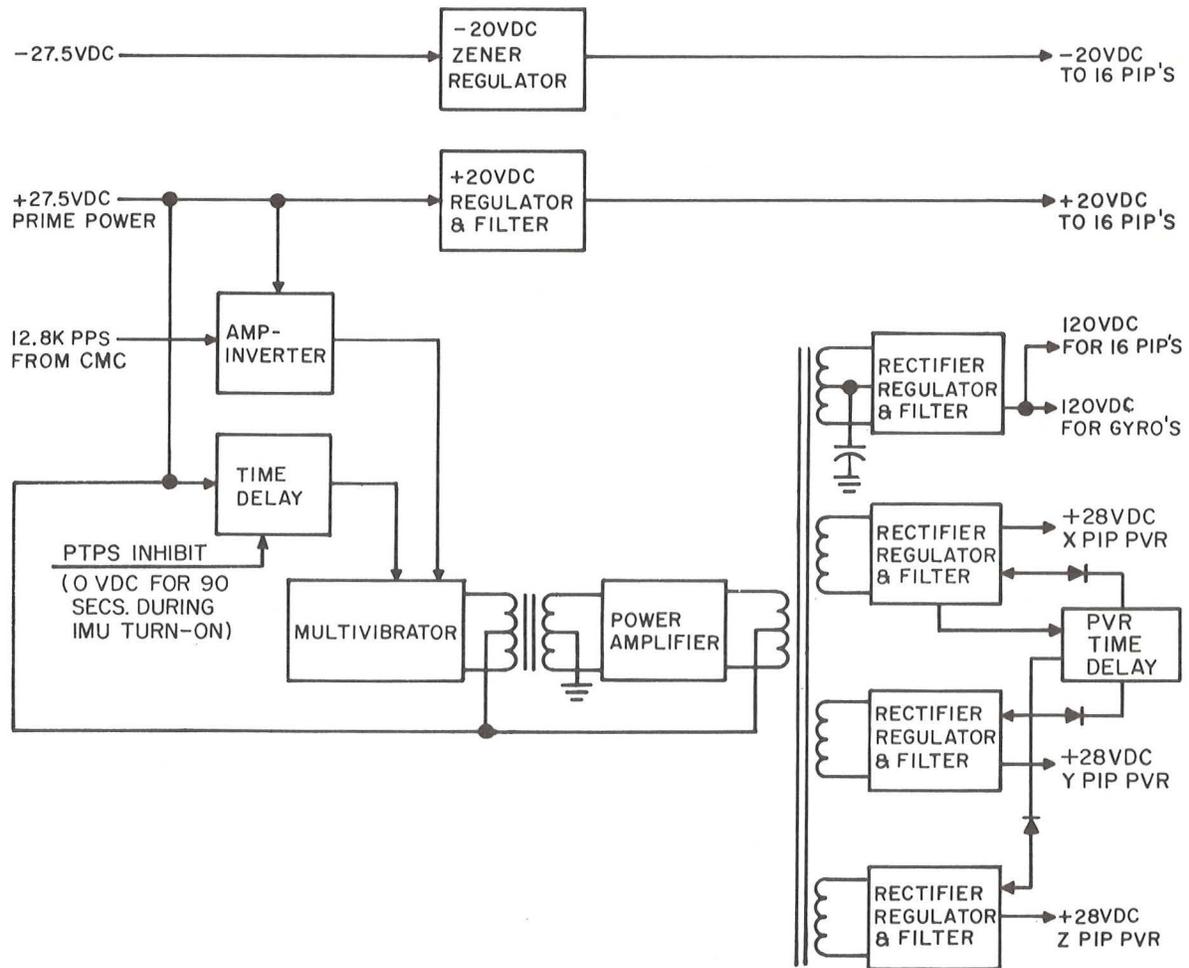
4-5.1 PULSE TORQUE POWER SUPPLY. The pulse torque power supply (figure 4-18) provides 120 vdc to the three binary current switches and three dc differential amplifiers in the accelerometer loops, and the binary current switch and dc differential amplifier in the stabilization loop fine align electronics. The pulse torque power supply also provides three individual 28 vdc outputs to the accelerometer loop PVR's, 20 vdc to the three accelerometer loop ac differential amplifier and interrogator modules and the associated binary current switches, and -20 vdc to the ac differential amplifier and interrogator module in the accelerometer loops.

The -20 vdc output is derived from the -28 vdc power supply by using a zener diode as a voltage divider and regulator. The output is regulated at -20 (± 0.8) vdc.

The 20 vdc output is derived from 28 vdc prime power by the use of a three transistor series regulator which maintains the output voltage at 20 (± 0.55) vdc.

The 120 vdc and 28 vdc outputs are derived from a multivibrator, a power amplifier, and a rectifier and filter. A 12.8 kpps synchronizing pulse is received from the CMC through a buffer transformer in the pulse torque isolation transformer assembly and is applied to an amplifier-inverter. The output of the amplifier-inverter is applied to a multivibrator-chopper causing the multivibrator-chopper to be synchronized at 6,400 cps. A transistorized time delay circuit is incorporated into the emitter circuits of the multivibrator to provide a turnon time delay of approximately 350 milliseconds. During the 90 second IMU turnon mode, 0 vdc is applied through the turnon circuits of the IMU auxiliary assembly module to the time delay circuit which inhibits the 120 vdc and 28 vdc PVR supplies. The multivibrator-chopper output is applied to the primary of a transformer which has 28 vdc prime power applied to its center tap. The secondary of the transformer, which is also center tapped, is coupled to a two stage push-pull power amplifier which operates from 28 vdc prime power. The output of the power amplifier consists of a transformer with four secondary windings; one with center tap return for the 120 vdc power supply, and one each for the X, Y, and Z accelerometer loop 28 vdc PVR supplies. The 120 vdc power supply consists of a full wave rectifier whose output is filtered, regulated, and again filtered. The 28 vdc power supplies are identical and consist of a full wave bridge rectifier whose output is filtered, regulated, and again filtered. The PVR time delay circuit inhibits the operation of the regulator in each 28 vdc PVR circuit to provide a six to eight second time delay in the 28 vdc PVR outputs.

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM



16134A

Figure 4-18. Pulse Torque Power Supply

4-5.2 -28 VDC POWER SUPPLY. The -28 vdc power supply provides input power to the three gimbal servo amplifiers in the stabilization loops and to the pulse torque power supply to generate -20 vdc for use in the accelerometer loops. The -28 vdc power supply consists of a pulse amplifier-inverter, a multivibrator-chopper, a power amplifier, and a rectifier and filter. (See figure 4-19.) The 25.6 kpps synchronization pulse input is amplified and inverted for use in synchronizing the multivibrator-chopper at 12.8 kcps. The multivibrator-chopper output is applied to the primary of a transformer which has 28 vdc prime power applied to its center tap. The secondary of the transformer, which is also center tapped, is coupled to a push-pull power amplifier. The output of the amplifier is transformer coupled to a full wave rectifier and filter whose positive side is referenced to ground to provide a -27.0 (± 1.0) vdc output.

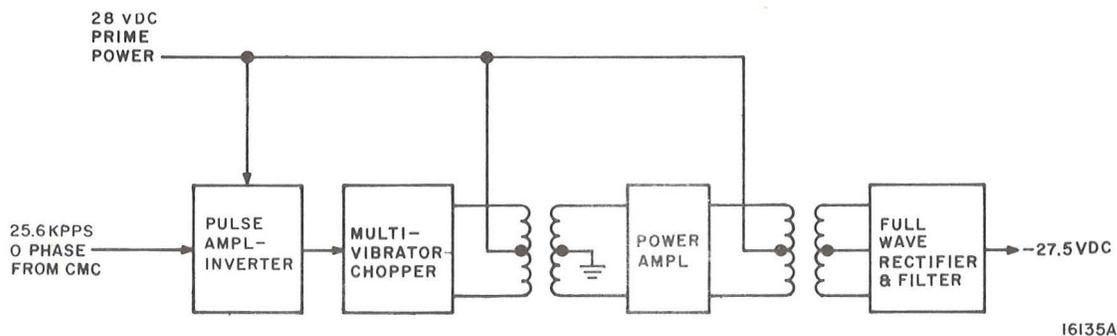
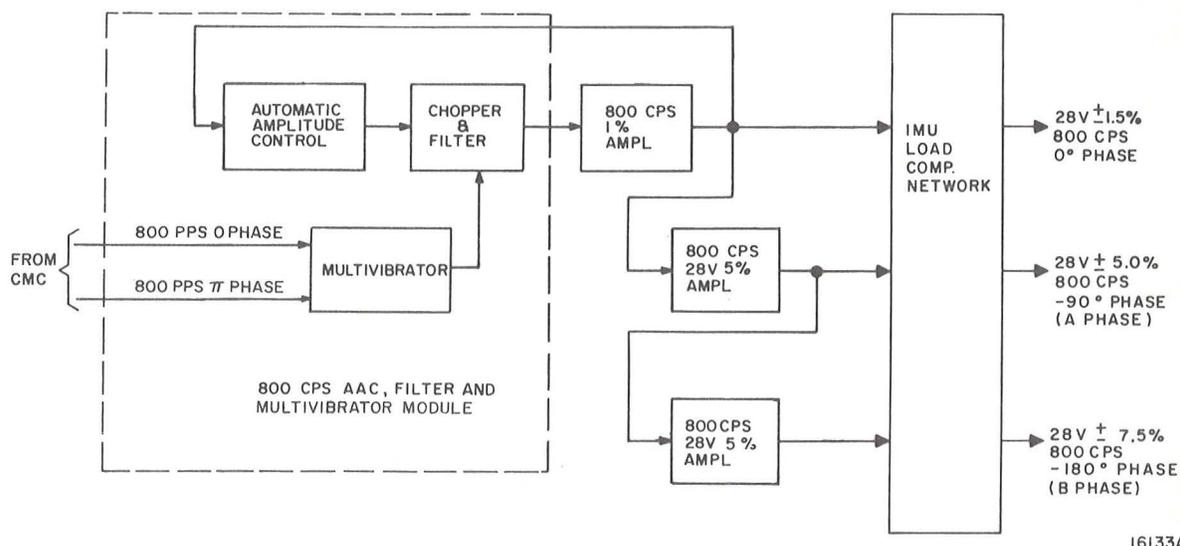


Figure 4-19. -28 VDC Power Supply

4-5.3 ISS 800 CPS POWER SUPPLY. The 800 cps power supply (figure 4-20) consists of four modules: an automatic amplitude control, filter, and multivibrator; a 1 percent amplifier; and two 5 percent amplifiers. The 1 percent amplifier provides IMU gimbal resolver excitation, gimbal servo amplifier demodulator reference, and FDAI and autopilot reference. The two 5 percent amplifiers provide gyro wheel excitation, IMU blower excitation, and accelerometer fixed heater power. The 1 percent amplifier also provides the input to one of the 5 percent amplifiers whose output is phase shifted -90 degrees. The output of this 5 percent amplifier is applied to the second 5 percent amplifier whose output is also phase shifted -90 degrees, or -180 degrees from the output of the 1 percent amplifier. The outputs of the 1 percent amplifier and the 5 percent amplifiers are applied to their respective loads through the IMU load compensation network which provides a power factor correction.



16133A

Figure 4-20. 800 CPS Power Supply

Zero and pi phase, 800 cps pulse trains from the CMC synchronize the multivibrator at 800 cps. In the absence of the synchronizing pulses, the multivibrator will free run between 720 and 790 cps. The output of the multivibrator controls the operation of the chopper and filter circuit. The filtered chopper output is applied to the 1 percent amplifier. The output of the 1 percent amplifier, in addition to its direct uses, is a feedback signal to the automatic amplitude control circuit. The positive peaks of this feedback signal are detected and added to a dc reference signal. The sum is filtered and provides a dc bias to the multivibrator driven chopper. The bias controls the amplitude of the chopped signal.

The 1 percent amplifier is push-pull in operation with transformer coupled input and output and with overall voltage feedback for gain and distortion control.

The two 5 percent amplifiers are identical in operation. The amplifiers are push-pull in operation and have transformer coupled inputs and outputs. The input transformer primary center tap is connected to the input signal low. The input signal high is applied directly to one side of the primary winding and is also applied through a phase shift network to the other, or out of phase, side of the primary. A feedback signal from the secondary of the output transformer is also applied to the out of phase side of the input transformer primary where it is mixed with the phase shifted portion

of the input signal. This mixing results in a -90 degree phase shift in the secondary of the input transformer. The output of the first 5 percent amplifier is used as an input to the second 5 percent amplifier to provide an additional -90 degree phase shift.

4-5.4 OSS 800 CPS POWER SUPPLY. The OSS 800 cps power supply consists of three modules: an automatic amplitude control, filter, and multivibrator; a 1 percent amplifier; and a 5 percent amplifier. The 1 percent amplifier provides resolver and tachometer excitation and the input to the 5 percent amplifier. The 5 percent amplifier provides SXT and SCT motor excitation. The outputs of the 1 percent amplifier and 5 percent amplifier are applied to their respective loads through the optics load compensation network which provides power factor correction.

The operation of the OSS 800 cps power supply is identical to the operation of the ISS 800 cps power supply except that it does not have two 5 percent amplifiers.

4-5.5 3,200 CPS POWER SUPPLY. The 3,200 cps power supply provides excitation voltage for the signal generator and the magnetic suspension portions of the IRIG and PIP ducosyns. The 3,200 cps output is also used as a reference for the demodulator in the gimbal servo amplifiers.

The excitation voltage to the signal generators requires both voltage stability and phase stability. To accomplish this stability, the excitation voltage power transmission to the stable member is through a step down transformer on the stable member which reduces the slip ring current and, therefore, voltage drop effects due to slip ring, cable, and connector resistance. In addition, each wire connecting the output of the transformer to the input terminals of each PIP is cut to exactly the same length. The voltage level at the primary of the transformer is fed back to the power supply and is compared to a voltage and phase reference.

The 3,200 cps power supply (figure 4-21) consists of an amplitude control module and a 1 percent power amplifier. The amplitude control module contains an automatic amplitude control circuit, a multivibrator, a chopper, and a filter.

The 3,200 pps pulse trains of zero degree phase and 180 degree phase synchronize a multivibrator. The output of the multivibrator controls the operation of the chopper circuit. The output of the chopper is applied to the 1 percent power amplifier. The 28 v (rms) output of the amplifier is transmitted through the slip rings to the transformer on the stable member where the voltage is stepped down to 2 volts for the accelerometer ducosyns and 4 volts for the gyro ducosyns. A sample of the 28 volt level at the primary of the transformer is fed back through the slip rings to the input of the automatic amplitude control circuit. The positive peaks of the feedback signal are detected and added to a dc reference signal. The sum is filtered and provides a dc bias to the chopper circuit. The dc bias controls the amplitude of the chopper output to the filter.

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

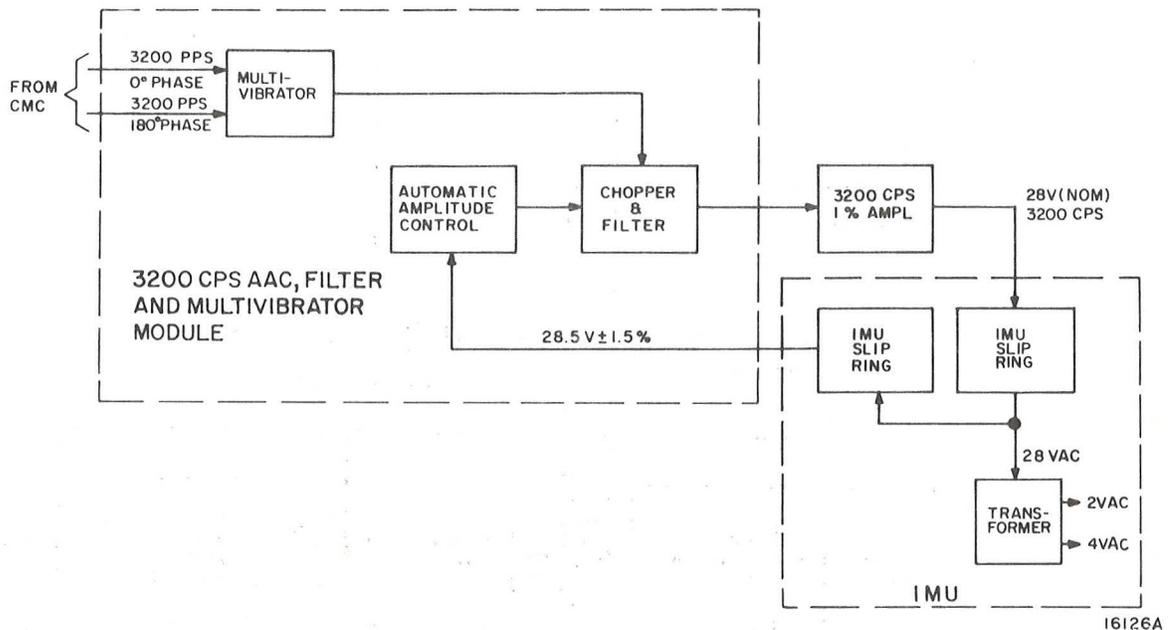
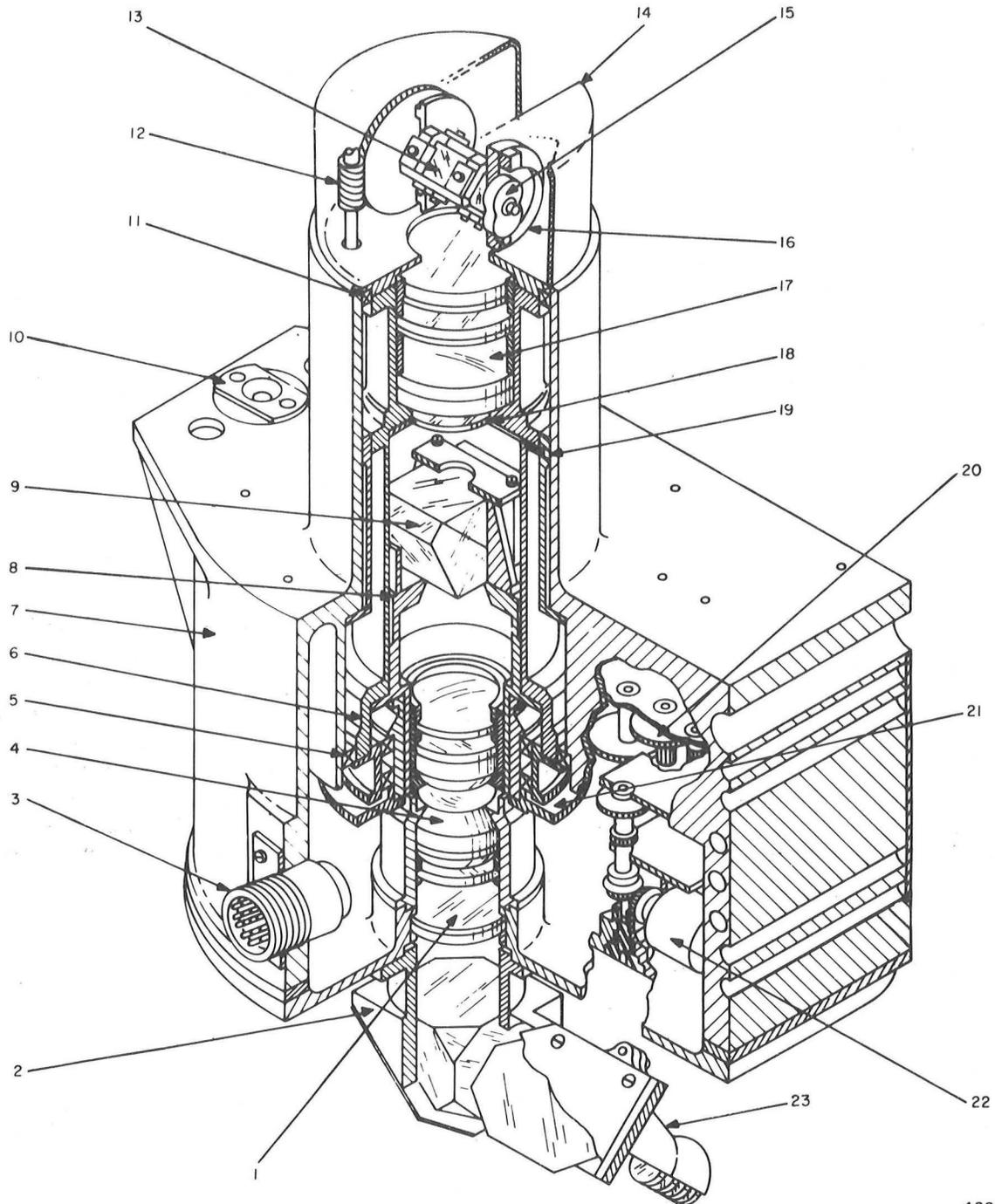


Figure 4-21. 3,200 CPS Power Supply

4-5.6 4 VDC POWER SUPPLY. The 4 vdc power supply (figure 4-22) supplies 4 vdc logic power to the digital logic circuits of the CDU. The 4 vdc power supply is a dc to dc converter type consisting of a pulse amplifier-inverter, a multivibrator-chopper, a power amplifier, a rectifier and filter circuit, and a difference amplifier and series regulator circuit.

A 25.6 kpps synchronization pulse input is amplified and inverted and used to synchronize the multivibrator-chopper, whose natural frequency is 11.5 kcps. The multivibrator-chopper drives the primary of a transformer which has 28 vdc applied to its center tap. The secondary of the transformer is also center tapped and is coupled to a push-pull power amplifier. The dc input to the power amplifier is supplied through a series regulator. The power amplifier drives the primary of a transformer to develop a 12.8 kcps square wave. The output from the transformer secondary is applied to the rectifier and filter circuit where the 4 vdc output is developed.

The 4 vdc output is fed back to a difference amplifier that produces an output error signal proportional to the difference between the 4 vdc output and a reference voltage level obtained from a zener diode and resistor voltage divider network. The output of the difference amplifier controls the operation of the series regulator to increase or decrease the level of the dc input to the power amplifier as necessary to maintain the power supply output at 4 volts.



42277A

Figure 4-23. SCT, Cutaway View (Sheet 1 of 2)

1. Eyepiece window
2. Eyepiece prism housing assembly
3. Electrical connector
4. Relay lens assembly
5. Ball bearing (outer telescope tube assembly)
6. Outer telescope tube assembly
7. Optical base
8. Inner telescope tube assembly
9. Pechan prism
10. Ball mount (3)
11. Ball bearing (outer telescope tube assembly)
12. Trunnion drive worm shaft
13. Dove prism and mount assembly
14. SCT head cover
15. Anti-backlash cam
16. Anti-backlash spring and cam follower
17. Objective lens assembly
18. Reticule assembly
19. Housing and lamp assembly
20. Shaft drive gear box
21. Cluster gear assembly
22. Shaft angle counter
23. Adjustable focus eyepiece assembly

Figure 4-23. SCT, Cutaway View (Sheet 2 of 2)

A housing and lamp assembly, used to illuminate the SCT reticle, is mounted in the optical base around the outer telescope tube assembly. The inner telescope tube assembly contains a pechan prism and relay lens assembly. Contained within the eyepiece prism housing assembly are two right-angle prisms. The adjustable focus eyepiece assembly contains an objective lens assembly. The objective lens assembly and reticle in the outer telescope tube assembly and the pechan prism and part of the relay lens assembly in the inner telescope tube assembly form the optical complex of a minus 4.6-power telescope. The portion of the relay lens assembly in the inner telescope tube assembly, the eyepiece prism housing assembly, and the adjustable focus eyepiece assembly form the optical complex of a plus 4.6-power telescope.

Detailed theory of operation is divided into two general areas of discussion: optical complex and drive assemblies.

4-6.1.1 SCT Optical Complex. The SCT optical complex (figure 4-24) consists of a double dove prism and mount assembly, a minus 4.6-power telescope, and a plus 4.6-power telescope.

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

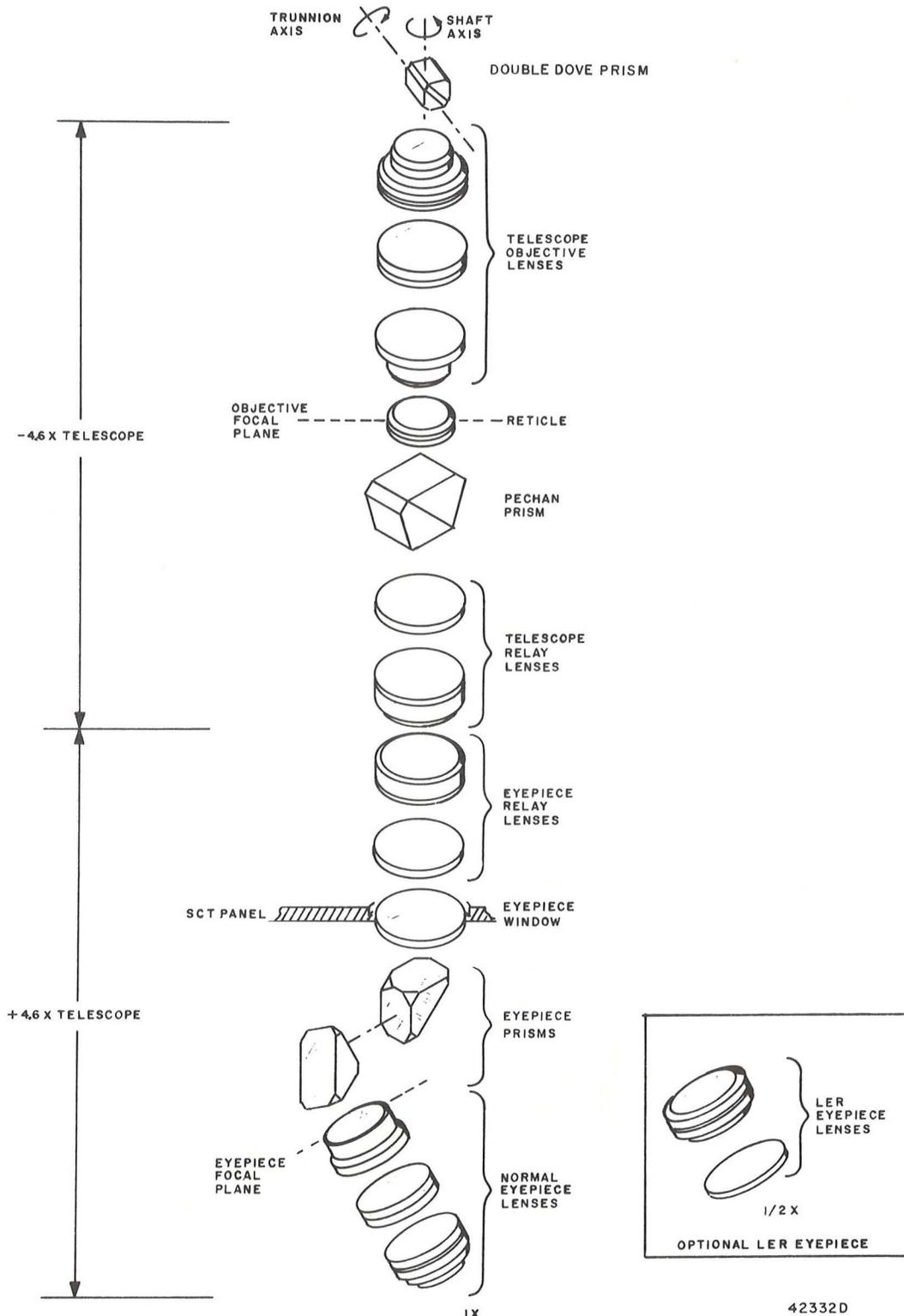
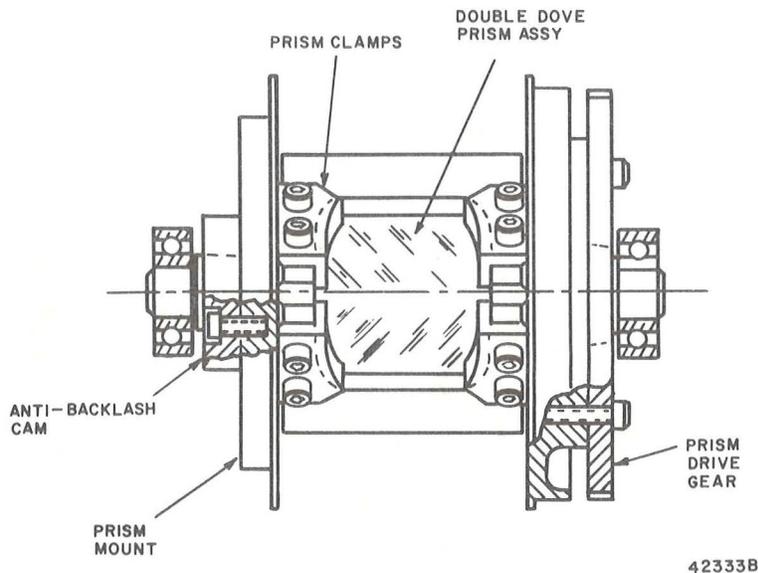


Figure 4-24. SCT Optics

42332D

4-6.1.1.1 Double Dove Prism and Mount Assembly. The double dove prism and mount assembly (figure 4-25) contains two optically matched dove prisms. The prisms are aluminized and cemented together at the hypotenuse and accurately positioned and clamped to a mount. The double dove prism is the first optical element in the SCT optics to pick up the target image. Each dove prism inverts and transmits an image to the objective lens assembly. Optically the prism functions as a compact, wide-angle mirror that is rotatable about two axes, trunnion and shaft. The rotational limitations of the prism about the trunnion axis are from -5 to +50 degrees. At zero degrees, the reflective surface of the prism is parallel to the shaft axis and the selected target, when the selected target is centered on the reticle crosshairs. The images of the targets pass through the angular entrance face of the prism, are refracted toward the prism's reflective surface, and are reflected off the prism's mirrored surface at the angle at which they were received, toward the exit face of the prism. At the angular exit face, the images are refracted again and the now inverted image is transmitted parallel to the shaft axis. When the prism is rotated about the trunnion axis, the selected target increases in angular position to the prism's reflective surface. With an increase in angular position of the selected target, the images entering the prism become increasingly inclined to the prism's angular face. As the images entering the prism increase in inclination to the angular face, the degree of refraction caused by the prism decreases until, at perpendicularity, there is no refraction. However, in use, the prism field-of-view is limited by the SCT head assembly, the command module optics opening, and the size of the objective lens. These limitations restrict the useful field-of-view to 60 degrees and the conic scan to 110 degrees. At all useful positions of the prism, the images reflected off the mirrored surface of the prism are transmitted parallel to the shaft axis by the objective lens assembly.



42333B

Figure 4-25. Double Dove Prism

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

A worm gear and worm shaft drive the double dove prism and mount. The worm shaft is driven by a motor generator in the SCT trunnion drive gearbox. An angle counter, seen through the SCT panel window, displays the trunnion angle and is mounted in the trunnion drive gearbox. The angle counter is set for a zero reading when a resolver, a component of the trunnion drive gearbox, is at the null setting.

An anti-backlash device is used to improve positional accuracy. The device consists of a cam on the double dove prism shaft, a cam-follower, and a spring assembly. The cam-follower is held against the cam by the spring, thereby minimizing the backlash of the worm drive. Preloaded bearings in the double dove prism mount and in the worm drive also assist in precise operation of the trunnion drive.

4-6.1.1.2 Minus 4.6-Power Telescope. The minus 4.6-power telescope consists of an objective lens assembly and reticle assembly mounted in the outer telescope tube assembly and pechan prism and part of the relay lens assembly mounted in the inner telescope tube assembly.

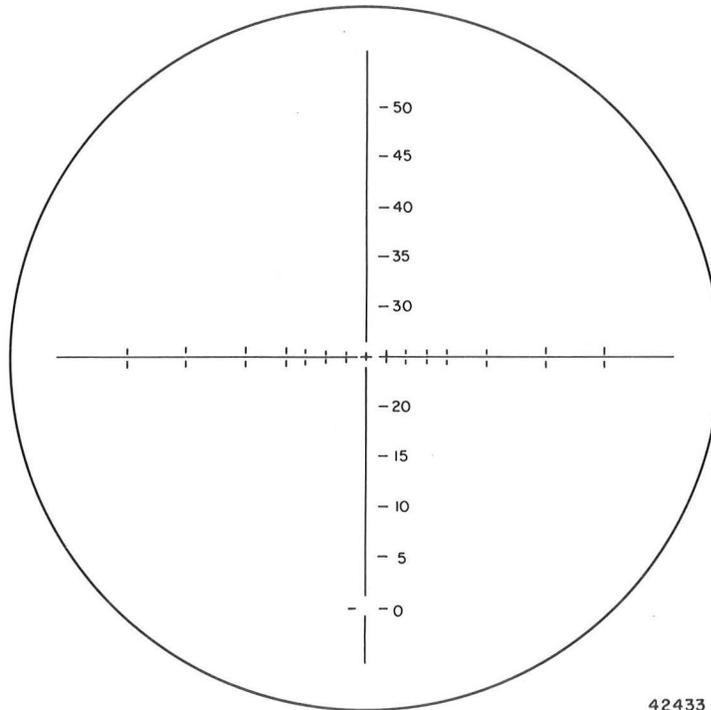
The objective lens assembly consists of three cemented doublets fitted into the upper end of the outer telescope tube assembly. Each doublet is made up of a positive and negative lens. This objective cluster collects light from the double dove prism and produces an image at the reticle plane. A 60-degree field-of-view is obtained with an aperture of approximately 5 millimeters.

The reticle assembly (figure 4-26) is located in the outer telescope tube assembly, is adjacent to the objective lens assembly, and is accurately positioned in the focal plane of the objective lens assembly. The inverted images transmitted by the objective lens assembly are focused onto the reticle. The reticle crosshair intersection is the reference target for the image transmitted from the double dove prism and objective lens assembly.

The reticle is illuminated from the edge by four incandescent lamps located in the housing and lamp assembly. (See figure 4-27.) This assembly is secured to the optical base and envelopes the outer telescope tube assembly. Three light-transmitting rods, assembled 120 degrees apart in the reticle plane, direct the light from the incandescent lamps to the reticle. The rods are fastened to the outer telescope tube assembly and provide uniform illumination at any shaft angle.

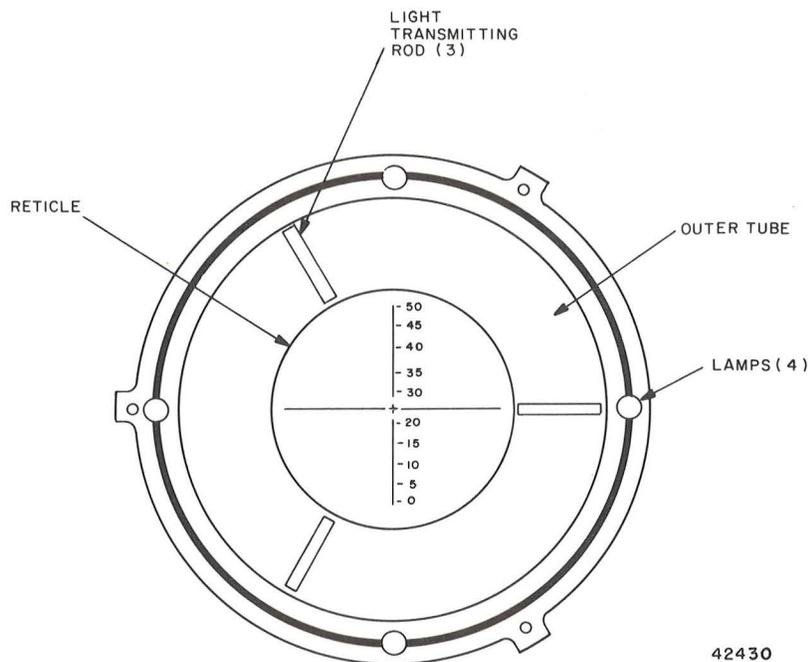
The pechan prism (figure 4-28) (located in the inner telescope tube assembly at the end facing the reticle assembly) erects the inverted images. The prism is in the optical path between the reticle and the relay lens assembly. The pechan prism consists of two sections separated by an air space. This design achieves the erecting of the images and increases the axial length of the optical path and decreases the physical length of the SCT.

The relay lens assembly consists of a group of relay lenses fastened to the end of the inner telescope tube assembly opposite the end holding the pechan prism. The relay lenses receive the erected image from the pechan prism and transfer it without distortion to the relay lenses of the plus 4.6-power telescope.



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Figure 4-26. SCT Reticle



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Figure 4-27. SCT Reticle Housing and Lamp Assembly

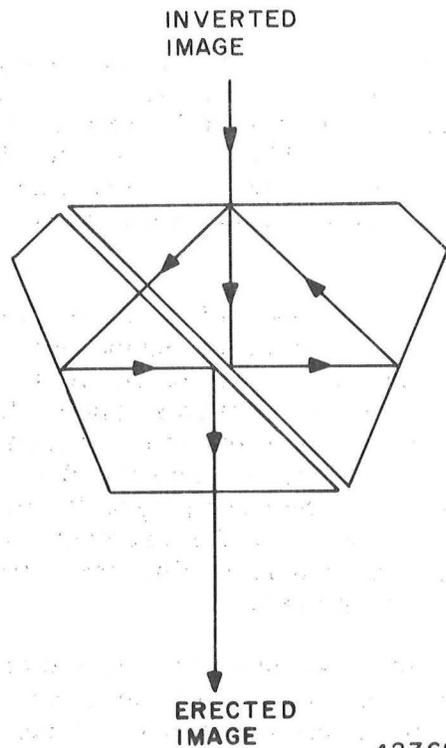


Figure 4-28. Pechan Prism

4-6.1.1.3 Plus 4.6-Power Telescope. The plus 4.6-power telescope consists of part of the relay lens assembly mounted in the inner telescope tube assembly, an eyepiece window, an eyepiece prism housing assembly, and an adjustable focus eyepiece assembly.

The relay lenses receive the images transmitted by the minus 4.6-power telescope relay lenses and transfer them through the eyepiece window to the eyepiece prism housing assembly.

The eyepiece window is mounted in the SCT panel assembly. The eyepiece window acts as a seal between the eyepiece prism housing assembly and SCT components exposed to environmental conditions outside the command module. The eyepiece window has no optical effect and transmits the image directly from the relay lens assembly to the SCT eyepiece prism housing assembly.

The eyepiece prism housing assembly is fastened to the front of the SCT panel assembly. It transfers the image from the relay lens assembly to the eye of the observer. The eyepiece prism housing assembly contains two right-angle prisms, one small and one large. The small prism is mounted in-line with the shaft axis and receives the images from the relay lens assembly and reflects the images 90 degrees

into the large prism. The large prism is mounted in a manner that corrects for this 90 degree image orientation by reflecting the images 90 degrees into the adjustable focus eyepiece assembly parallel to the SCT shaft axis. The prism mountings enable the adjustable focus eyepiece assembly to be mounted in a position that provides the astronaut with the most viewing comfort. Enlarged thumb screws are provided which allow the astronaut to quickly disconnect and remove the prism housing assembly while wearing gloves.

The adjustable focus eyepiece assembly is mounted to the eyepiece prism housing assembly. This assembly contains three telescope objective lens assemblies, heater, thermostat, insulation, and connector. The objective lenses are optically identical to the minus 4.6-power telescope objective lenses. The heater, thermostat, and insulation maintain the adjustable focus eyepiece assembly at a constant temperature to prevent moisture condensation on the eyepiece components. Heater current is provided through the connector when connected to the harness plug on the eyepiece storage unit connector bracket. Focus adjustment compensates for astronaut sight differences and enlarged thumb screws allow the astronaut to quickly disconnect and remove the adjustable focus eyepiece assembly while wearing gloves.

The SCT eyeguard assembly is fastened to the end of the adjustable focus eyepiece assembly. It is made of non-toxic, synthetic rubber and is adjustable in an axial direction. The adjustment allows for differences in facial contours of the astronauts.

The SCT long eye relief (LER) eyepiece assembly is optional equipment that can replace the SCT adjustable focus eyepiece assembly. It contains a lens assembly, a positive lens, heater, thermostat, insulation, and connector mounted into a SCT eyepiece housing. Unlike the contoured eyeguard assembly of the SCT adjustable focus eyepiece assembly, a flat rubber guard is cemented against the end of the SCT LER eyepiece assembly. Enlarged thumb screws allow the astronaut to quickly disconnect and remove the LER while wearing gloves.

4-6.1.2 SCT Optics Light Transmission. The optical efficiency of the SCT allows approximately 40 percent of the light impinging on the double dove prism to be transmitted to the eyepiece. Light losses in the SCT are held to a minimum by the use of multiple anti-reflection coatings which increase the efficiency of all transmitting surfaces.

4-6.1.3 SCT Drive Assemblies. The single speed SCT obtains rotational drive about shaft and trunnion axes through two motor generators, one for each axis. Reduction gearing, motor generators, resolvers, and angle counters for shaft and trunnion axes are assembled in two separate gearboxes located in the optical base. The following paragraphs contain details of SCT gearbox components and their operation.

4-6.1.3.1 Gear Reduction Ratios. Figure 4-29 contains an operational diagram of the SCT reduction gearing. In trunnion axis, the gear reduction ratio between motor generator shaft and double dove prism is 5952:1. Worm mesh lead accuracy is maintained within 30 arc seconds. In shaft axis, the gear reduction ratio between motor generator shaft and double dove prism is 2976:1.

4-6.1.3.2 SCT Differential. SCT shaft and trunnion axis drives are linked by a differential gear assembly. The differential gear assembly permits trunnion axis positioning independent of shaft axis, and shaft axis rotation without introducing errors in the trunnion axis. The differential gear assembly is shown in detail in figure 4-30. The A_S trunnion drive gear and the trunnion positioning planetary gearing system are pinned to the differential drive shaft, while the A_t trunnion drive gear and the trunnion positioning gear can rotate about the differential drive shaft. The SCT shaft axis drive motor restricts rotation of the A_S trunnion drive gear and the trunnion positioning planetary system then permits the trunnion positioning gear to rotate about the differential drive shaft when the A_t trunnion drive gear is rotated (SCT trunnion axis positioning). Likewise, the SCT trunnion axis drive motor restricts rotation of the A_t trunnion drive gear and the trunnion positioning planetary system then permits the trunnion position gear to rotate with the differential drive shaft when the A_S trunnion drive gear is rotated (SCT shaft axis positioning).

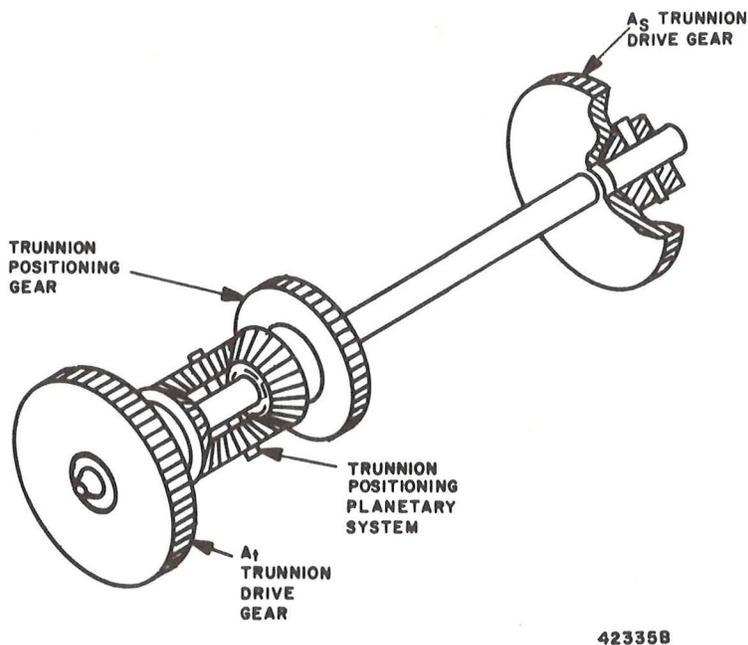


Figure 4-30. SCT Differential Gear Assembly

Shaft Axis Positioning - Positioning the SCT in shaft results in the A_s trunnion drive gear rotating and driving the differential drive shaft. Because the trunnion positioning planetary system gears are pinned to the differential drive shaft and the A_t trunnion drive gear is held stationary by the gear train friction, the planetary gears rotate about the A_t trunnion drive bevel gear. The planetary gears are thus forced to rotate about their own axes (parallel to the planetary gear pin) and force the trunnion positioning gear to rotate. The trunnion positioning gear will rotate in the same direction as the differential drive shaft and drive the trunnion assembly in the same direction and at the same speed as the SCT shaft. Since the rotation of the trunnion assembly is coincident with the rotation of the SCT shaft, rotation about the SCT shaft axis is possible without introducing errors in the trunnion axis.

Trunnion Axis Positioning - Positioning the SCT in trunnion results in the A_t trunnion drive gear rotating about the differential drive shaft and driving the trunnion positioning gear. When the A_t trunnion drive gear is rotated, the trunnion positioning planetary gears are forced to rotate about their own axes and force the trunnion positioning gear to rotate. The trunnion positioning gear rotates and positions the SCT double dove prism about the trunnion axis. Since the A_t trunnion drive gear and the trunnion positioning gear are free to rotate about the differential drive shaft and the A_s trunnion drive gear is held stationary by the gear train friction, rotation of the A_t trunnion drive gear does not result in a rotation of the differential drive shaft. The SCT can thus be positioned about the trunnion axis without introducing errors in the SCT shaft.

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

4-6.1.3.3 SCT Angle Counter. Two identical counters (figure 4-31) displaying SCT shaft and trunnion axis angles are located in the optical base. The counters are viewed through lighted bezel windows in the SCT panel. Each counter contains three drums interconnected through geneva gearing. A flip-up counter shade is geared to the drums to permit continuous numerical display. The counter is calibrated to display readouts from 0 to 359.98 degrees with graduations in 0.02 degree increments. Counter rotation is continuous in either direction. One revolution of the counter input shaft results in a one degree change in counter indication.

4-6.2 SEXTANT. The SXT structure is shown in figure 4-32. For purposes of description, the SXT is divided into the index head assembly and the base section. The SXT index head assembly contains the indexing mirror and mount assembly, SXT right angle mirrors, beam splitter, and trunnion drive electromechanical components.

The SXT portion of the optical base contains the shaft axis assembly, shaft drive electromechanical components (motor-generator, shaft drive gearbox, and resolvers), and SXT eyepiece. Rotating components, mounted on the shaft axis assembly include the SXT telescope tube assembly (with objective and intermediate lens), the SXT reticle assembly, and the shaft resolver rotors. The SXT panel assembly covers the underside (face) of the optical base. This assembly contains the eyepiece window and has provision for mounting the SXT mirror housing and eyepiece assembly. The detailed theory of operation for the SXT is divided into two general areas of discussion: optical complex and mirror housing and eyepiece assembly.

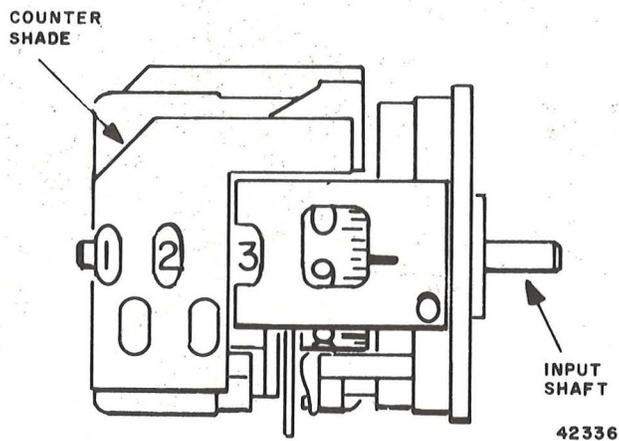
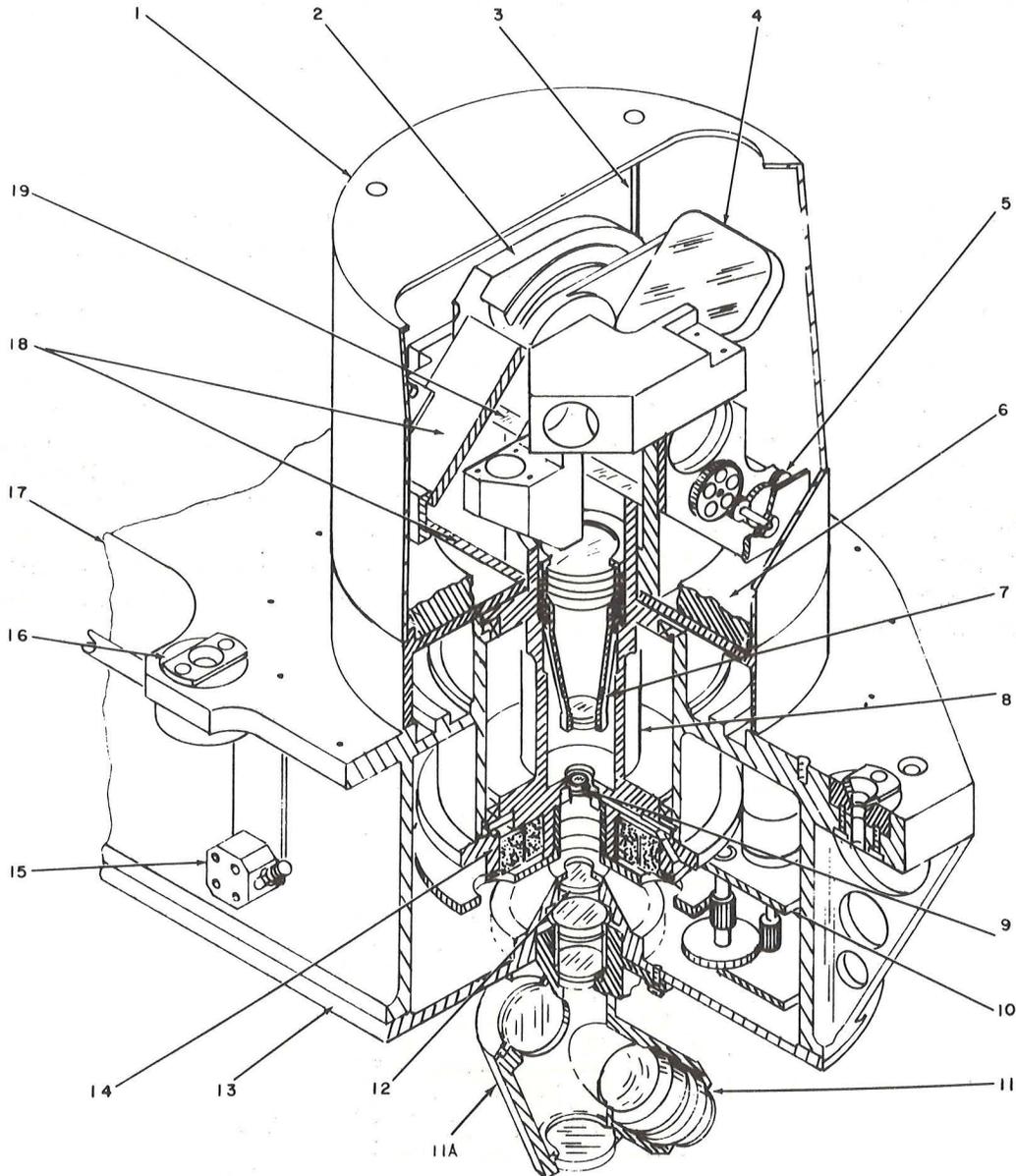


Figure 4-31. SCT Angle Counter



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Figure 4-32. SXT, Cutaway View (Sheet 1 of 2)

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

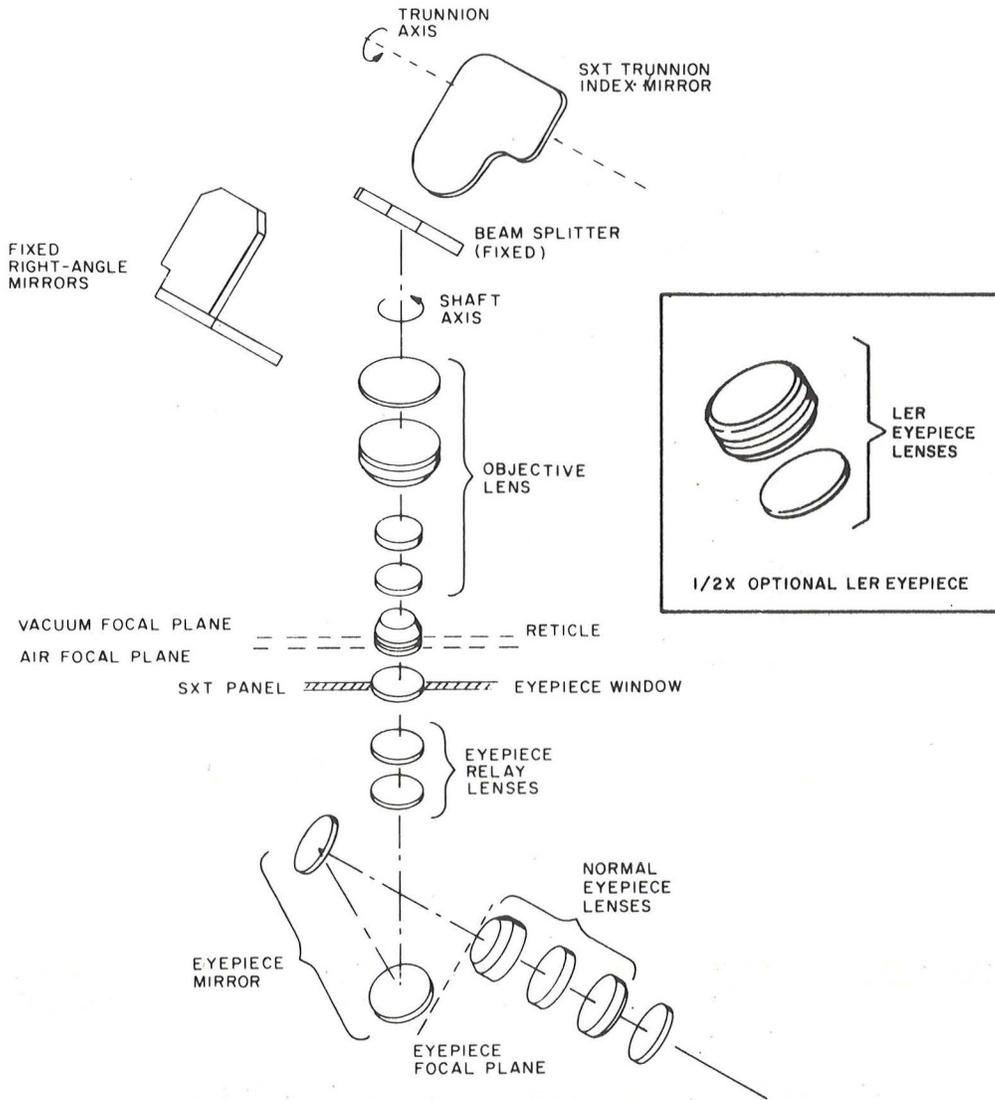
1. SXT head assembly cover
2. Trunnion pancake resolvers
3. Threaded rod (cover support) (2)
4. Trunnion indexing mirrors and mount assembly
5. Trunnion servo gear box
6. Dummy weight
7. Objective lens assembly
8. Shaft axis assembly
9. Reticle assembly
10. Shaft servo gear box
11. SXT eyepiece assembly
- 11A. SXT mirror housing and eyepiece assembly
12. Eyepiece window
13. SXT panel assembly
14. Shaft resolvers
15. Coolant passages (not used)
16. Ball mount (3)
17. Optical base
18. Right-angle mirrors
19. Beam splitter

Figure 4-32. SXT, Cutaway View (Sheet 2 of 2)

4-6.2.1 SXT Optical Complex. The SXT optical complex (see figure 4-33) consists of SXT indexing mirror and mount assembly, right angle mirrors, beam splitter, SXT telescope lenses, and eyepiece assembly.

4-6.2.1.1 SXT Indexing Mirror and Mount Assembly. The SXT indexing mirror is constructed of heat-treated beryllium with a reflective coating and is used to pickup and direct a target star image onto the right angle mirrors. The indexing mirror is mounted in the mirror mount assembly of the sextant head. The assembly rotates on precision ball bearings in the trunnion axis and is provided with counterweights to maintain balance in any position. For every one degree of indexing mirror movement, the StLOS moves two degrees.

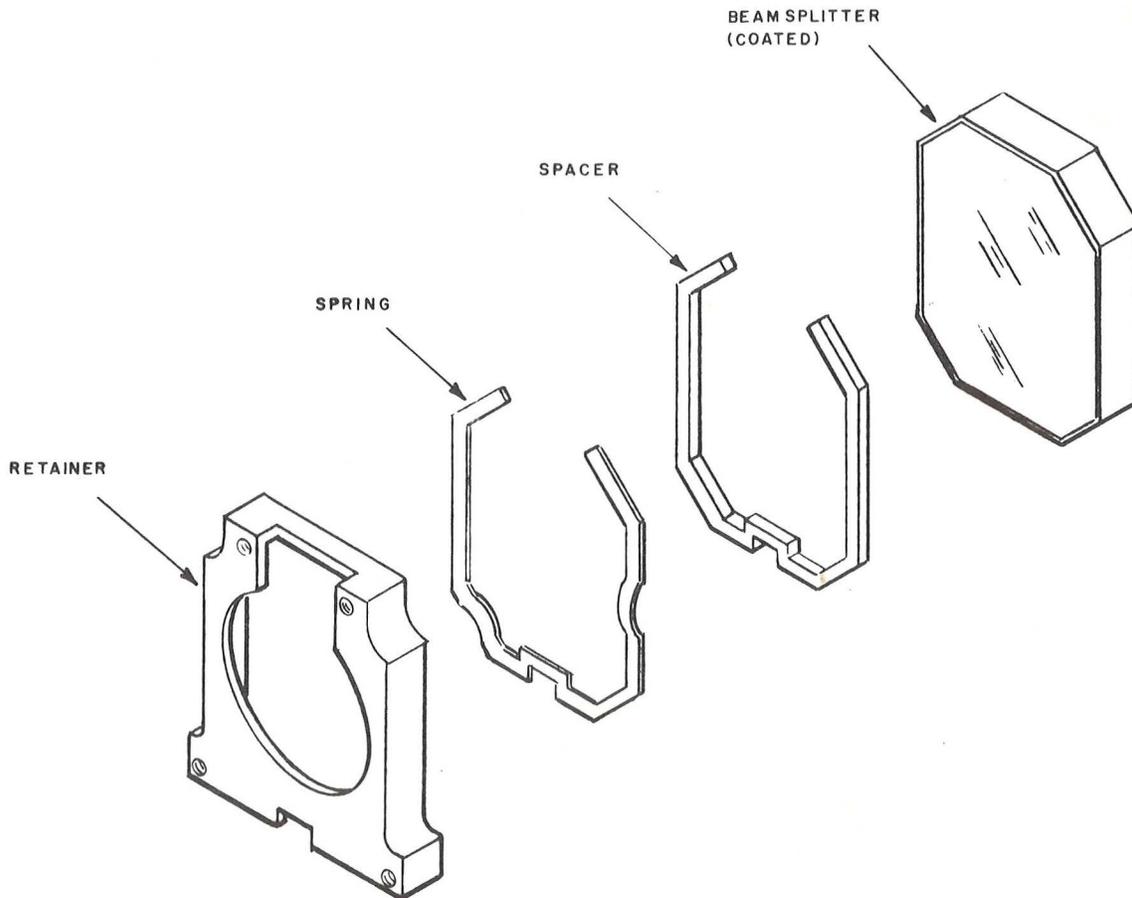
4-6.2.1.2 SXT Head Right Angle Mirrors. Two mirrors are fixed at right angles to each other and reflect the star image onto the reflecting surface on the underside of the beam splitter.



42331E

Figure 4-33. SXT Optics

4-6.2.1.3 Beam Splitter. The SXT optics provides two distinct lines of sight with different degrees of light transmission for two simultaneously viewed images. These capabilities are derived by incorporation of the beam splitter. (See figure 4-34.) The beam splitter is more properly termed a beam combiner since it functions by reflecting the StLOS into the same path as the transmitted LLOS.



42330A

Figure 4-34. Beam Splitter Construction

The landmark image is brighter than the star image, therefore it is necessary to transmit the image intensities at different levels to keep the landmark image from obscuring the star image. The beam splitter provides the required variations in transmission due to its surface reflectivity characteristics.

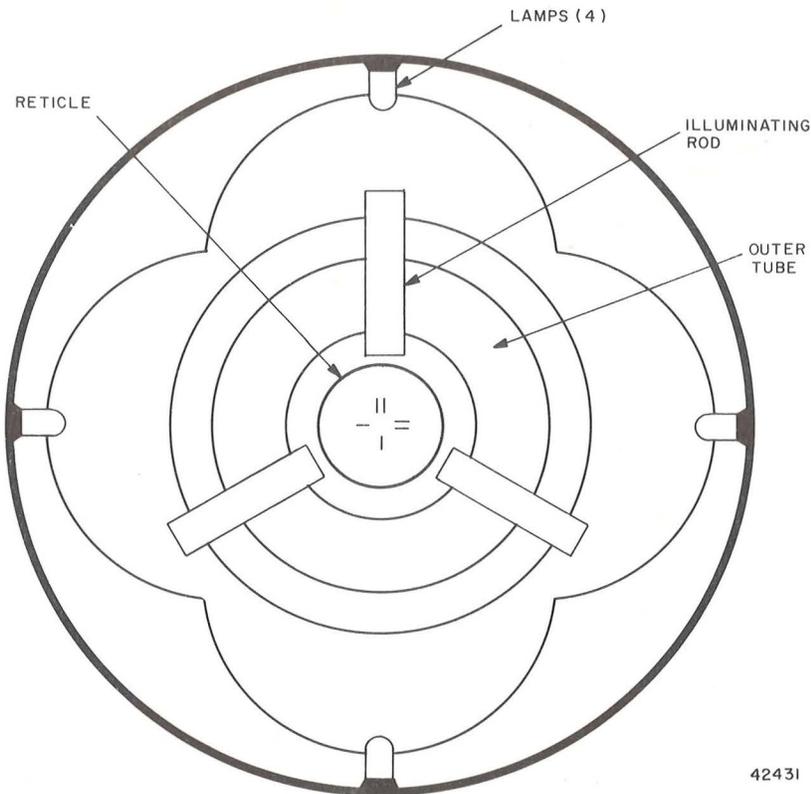
4-6.2.1.4 SXT Telescope Optical Complex. The SXT telescope optical complex, mounted in the SXT shaft axis assembly, consists of an objective lens, the intermediate lens, and reticle assemblies. A triplet and a single lens form part of the telescope objective lens assembly at the upper end of the lens holder which tapers due to the smaller diameter of the intermediate lenses. A set of these intermediate lenses is mounted at the lower end of the lens holder assembly. The objective and intermediate lens assemblies form a telephoto type lens system. The reticle is positioned in the forward vacuum focal plane of the SXT optics. This position provides optimum focus of

the reticle vacuum pattern etched on the forward face of the reticle assembly (figure 4-35). When operating in the earth atmosphere, the reticle vacuum pattern becomes indistinct due to a shift in the focal plane of the SXT optics. An air pattern is etched on the rear face of the reticle and an air focusing shim is inserted between the SXT plate and eyepiece assemblies to compensate for the shift. The air focusing shim is removed prior to launch for vacuum (outer space) operation of the SXT. The edge illumination of the SXT reticle is provided by four lamps which light three transmitting rods spaced evenly around the reticle. (See figure 4-36.) The eyepiece window serves as a seal in the SXT panel. The SXT eyepiece window is similar in function to the SCT eyepiece window.



42432

Figure 4-35. SXT Reticle



42431

Figure 4-36. SXT Reticle Housing and Lamp Assembly

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

4-6.2.1.5 SXT Mirror Housing and Eyepiece Assembly. The SXT mirror housing and eyepiece assembly consists of the mirror housing and heater assembly, and the eyepiece assembly. Enlarged thumb screws allow the astronaut to quickly disconnect and remove the SXT mirror housing and eyepiece assembly while wearing gloves.

The mirror housing and heater assembly consists of the relay lens assembly, two mirrors, heater, thermostat, insulation, and connector. The relay assembly contains two lens doublets which relay the image to the primary of the two mirrors. The mirrors reduce the length of the system and transfer the image into the eyepiece assembly. The heater, thermostat, and insulation maintain the SXT mirror housing and heater assembly along with the attached eyepiece assembly at a constant temperature to prevent moisture from condensing on components. Heater current is provided through the connector when connected to the harness plug on the eyepiece storage unit connector bracket.

The SXT eyepiece assembly contains two lens doublets, a single lens, and an adjustable polaroid filter. The polaroid filter provides landmark (LLOS) image brightness adjustment without affecting star image (S_tLLOS). Enlarged thumb screws allow the astronaut to quickly disconnect and remove the eyepiece assembly while wearing gloves.

In effect, the SXT eyepiece assembly represents a telemicroscope of 0.34 inch focal length and contributes to the SXT 28 power magnification by providing 3.4 power magnification from the relay assembly. Focal length of the eyepiece assembly equals one inch, which results in a total magnification of 28 power.

The SXT eyeguard assembly is fastened to the SXT eyepiece assembly. It is made of non-toxic, synthetic rubber and is adjustable in an axial direction. The adjustment allows for differences in facial contours of the astronauts.

The SXT long eye relief (LER) eyepiece assembly is optional equipment that can replace the SXT eyepiece assembly. It contains a lens assembly and positive lens mounted into a SXT eyepiece housing. Unlike the contoured eyeguard assembly of the SXT eyepiece assembly, a flat rubber eyeguard is attached to the SXT LER eyepiece assembly. Enlarged thumb screws allow the astronaut to quickly disconnect and remove the LER while wearing gloves.

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

4-6.2.1.6 SXT Optics Light Transmittance. When a beam of light passes through a different medium, the intensity will decrease. This loss of intensity is mainly due to absorption. With respect to the SXT S_tLOS (see figure 4-37), incident light impinging on and emerging from the trunnion mirror is reduced by a factor of approximately 4 percent. The resulting 96 percent is passed on to the first fixed mirror, which causes a further reduction of 4 percent passing on 92 percent of the light to the second fixed mirror. The second fixed mirror further reduces transmitted light by 4 percent, leaving approximately 88 percent to be reflected by the beam splitter. The beam splitter will reflect approximately 82 percent of the light principally in the shorter wavelength of the visible spectrum. Light loss in the objective lens assembly and through the eyepiece results in total light transmissions of approximately 25 percent for the S_tLOS.

The total light losses in the LLOS (see figure 4-37) amount to approximately 97 percent, with 89 percent occurring at the beam splitter. The remaining 11 percent emerging from the beam splitter is further attenuated through the objective and eyepiece assemblies. This results in an overall transmittance of 3.2 percent.

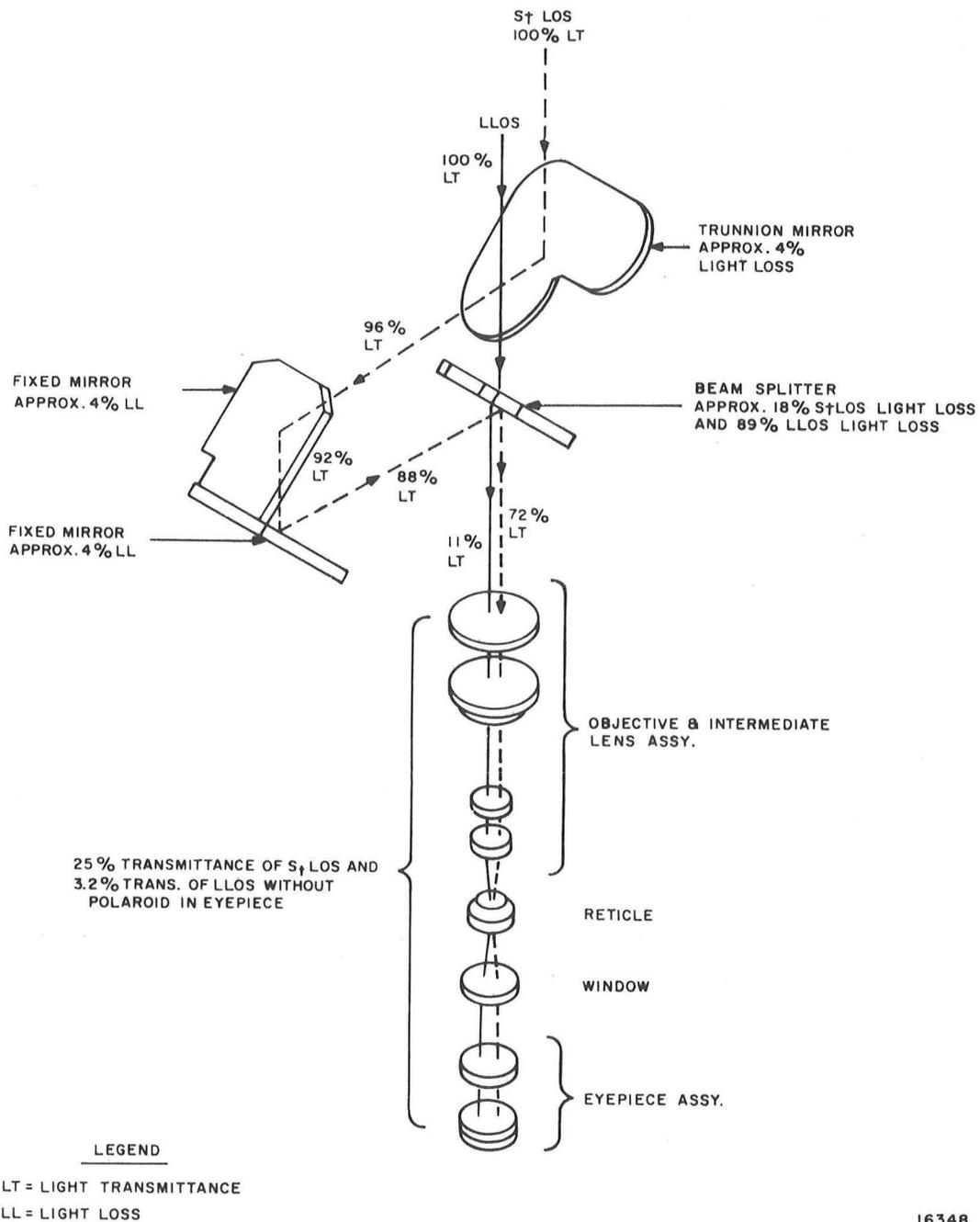
4-6.2.2 SXT Drive Assemblies. The SXT obtains rotational movement about shaft and trunnion axes through two motor generators. Reduction gearing, motor generators, and resolvers are contained in two separate gearboxes. One is located in the optical base; the other is located in the index head assembly (see figure 4-38).

In trunnion axis, positioning of the indexing mirror is restricted mechanically to a range of -5 to +50 degrees through the use of a limit stop. A command torsion spring assembly is provided in the drive assembly to minimize positioning error.

In trunnion axis, the gear reduction ratio between motor generator shaft and indexing mirror is 11780:1. The gear reduction ratio in shaft axis drive between motor generator shaft and indexing mirror is 3010:1.

4-7. COMMAND MODULE COMPUTER

See LEM Primary Guidance, Navigation, and Control System Manual, ND 1021042, paragraph 4-5 for computer theory of operation.



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Figure 4-37. SXT Optics Light Transmittance

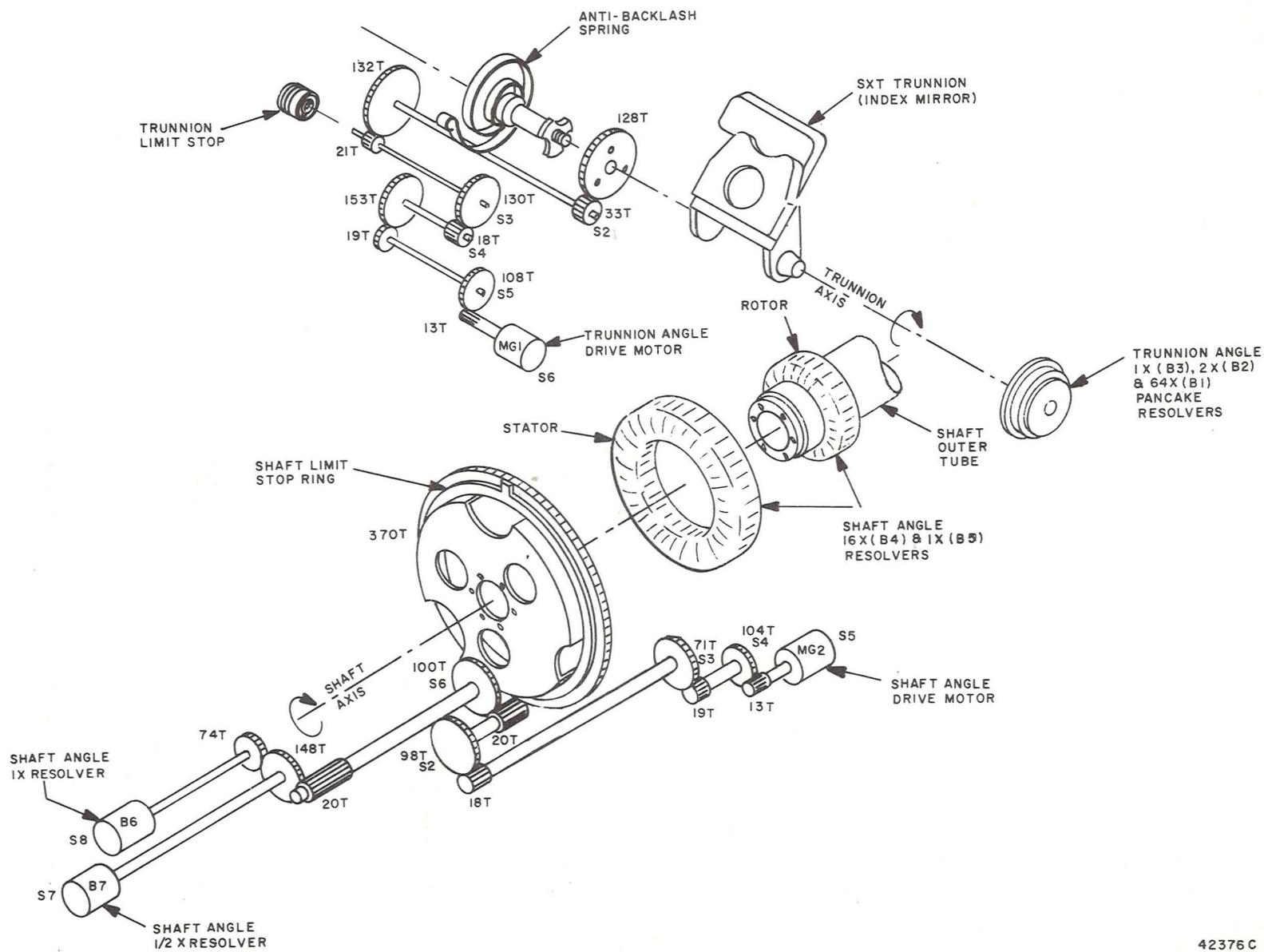


Figure No. 4-38. SXT Gearing Diagram

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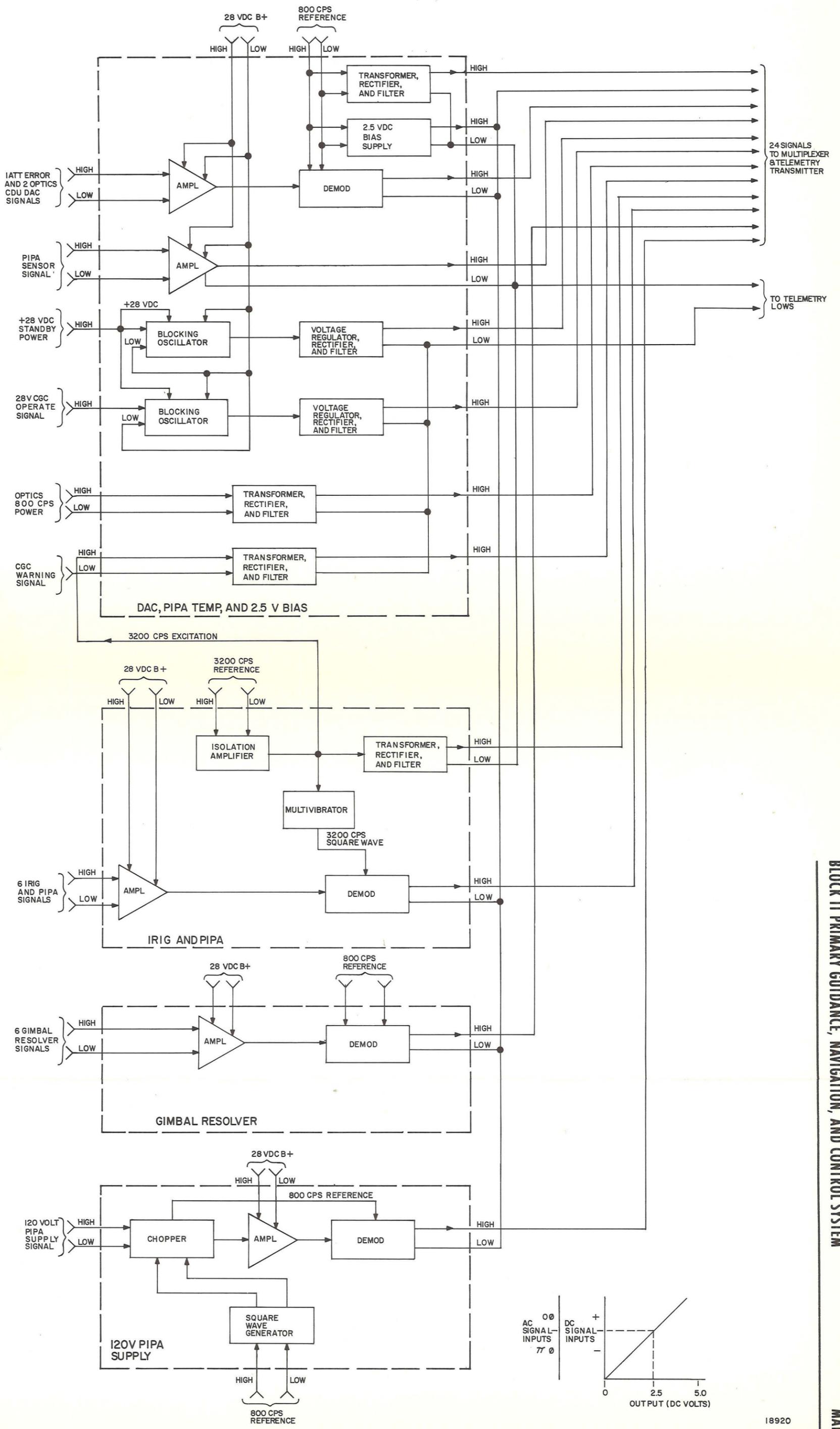
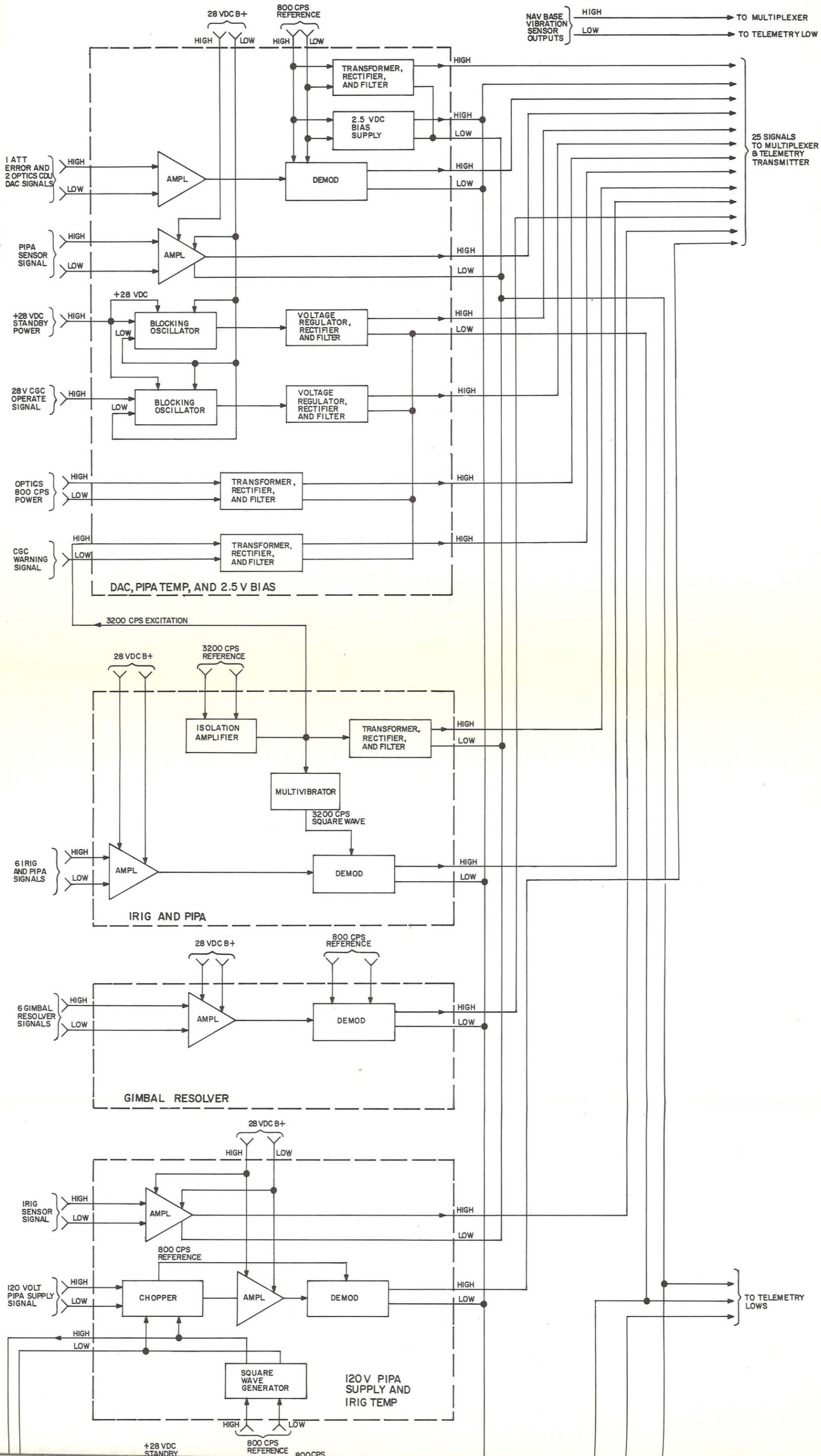
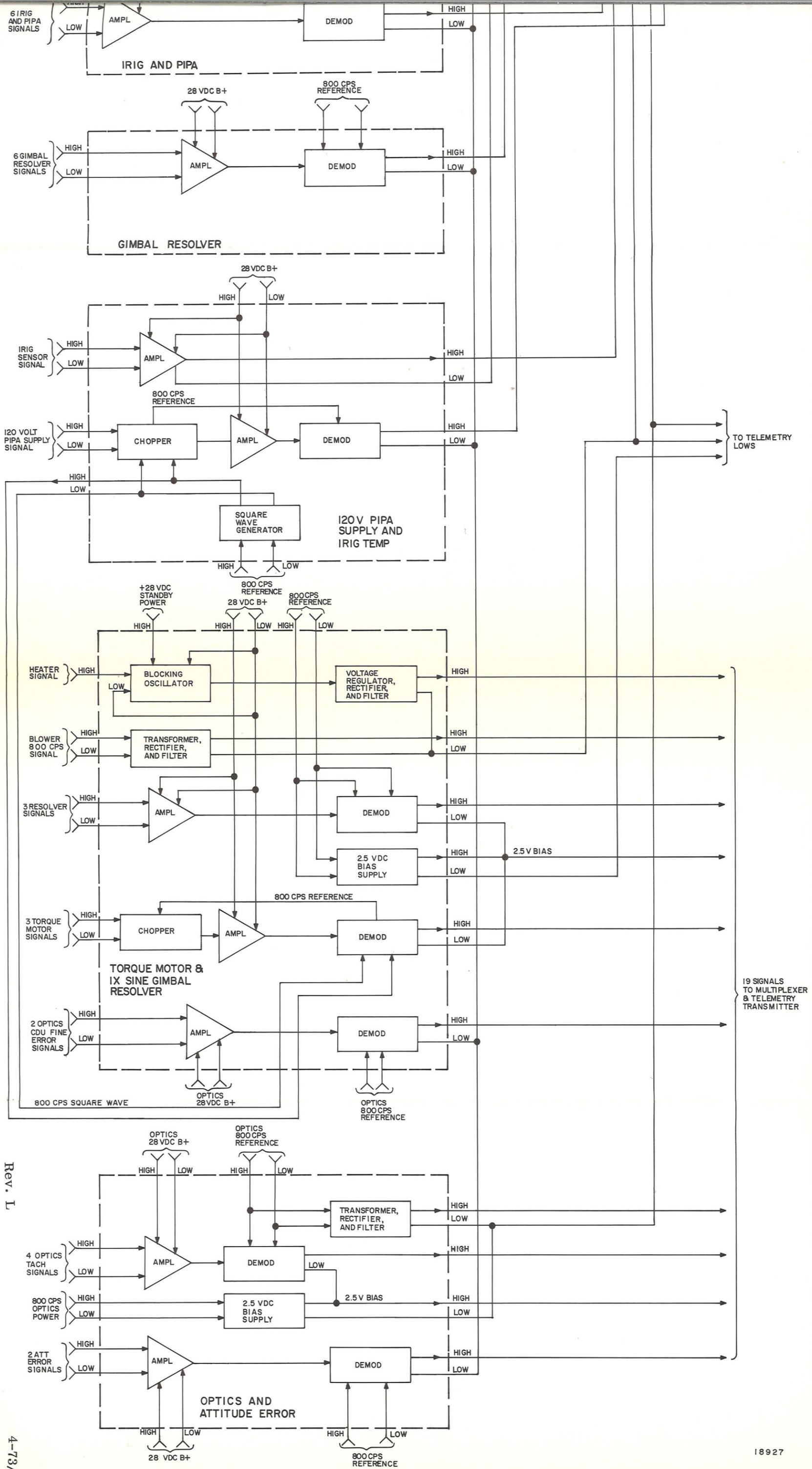


Figure 4-39. Operational Signal Conditioner Assembly Block Diagram

Rev. L

4-71/4-72





Rev. 1

4-73/4-74

Figure 4-40. Flight Qualification Signal Conditioner Assembly Block Diagram

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

ND-1021043
MANUAL

19 SIGNALS
TO MULTIPLEXER
& TELEMETRY
TRANSMITTER

Table 4-I. Circuits in SCA Modules

Name of Module	Name of Signal	Type of Signal Conditioning Circuit	Type of Signal Conditioned	Nominal Output Voltage Range
DAC, PIPA temp, and 2.5 vdc bias	PITCH ATTITUDE ERROR TRUNNION CDU DAC OUTPUT SHAFT CDU DAC OUTPUT	Amplifier-demodulator	800 cps, 0 or pi phase	0 to 5 vdc
	PIPA TEMP	Temperature sensor amplifier	Variable resistance of PIPA temperature sensor	0 to 5 vdc
	IMU STANDBY POWER ON +28 VDC CGC OPERATE	Blocking oscillator-rectifier-filter	0 or 28 vdc discrete	0 or 4.4 vdc
	OPTICS POWER ON	Transformer-rectifier-filter	Optics 28 v, 800 cps power	4.3 vdc (at 28 v input)
	ISS 800 CPS 1% TM	Transformer-rectifier-filter	ISS 28 v, 800 cps power	4.3 vdc (at 28 v input)
	CGC WARNING	Transformer-rectifier-filter	Open or ground discrete	0 or 4.3 vdc
	2.5 V BIAS	2.5 volt bias supply	ISS 28 v, 800 cps power	2.5 vdc

(Sheet 1 of 5)

Table 4-I. Circuits in SCA Modules

Name of Module	Name of Signal	Type of Signal Conditioning Circuit	Type of Signal Conditioned	Nominal Output Voltage Range
IRIG and PIPA	X PIPA Y PIPA Z PIPA IG & Y IRIG ERROR MG IRIG ERROR OG IRIG ERROR	Amplifier-demodulator	3,200 cps, -45 or +135 degree phase	0 to 5 vdc
	3,200 CPS TELEM	Transformer-rectifier-filter	3,200 cps signal from isolation amplifier	4.3 vdc
	3,200 cps sine wave and 3,200 cps square wave used internally in SCA	3,200 cps isolation amplifier and multivibrator	Low voltage 3,200 cps sine wave	3,200 cps sine wave reference and 3,200 cps square wave reference
Gimbal resolver	IG RSLV OUTPUT SIN MG RSLV OUTPUT SIN OG RSLV OUTPUT SIN IG RSLV OUTPUT COS MG RSLV OUTPUT COS OG RSLV OUTPUT COS	Amplifier-demodulator	800 cps, 0 or pi phase	0 to 5 vdc

Table 4-I. Circuits in SCA Modules

Name of Module	Name of Signal	Type of Signal Conditioning Circuit	Type of Signal Conditioned	Nominal Output Voltage Range
120 v PIPA supply and IRIG temp	120 V PVR	Chopper-amplifier-demodulator	High voltage dc	0 to 5 vdc
	IRIG TEMP	Temperature sensor amplifier	Variable resistance of IRIG temperature sensor	0 to 5 vdc
	800 cps reference voltage used internally in SCA	Square wave generator	800 cps sine wave reference	800 cps square wave reference
120 v PIPA supply	120 V PVR	Chopper-amplifier-demodulator	High voltage dc	0 to 5 vdc
	800 cps reference voltage used internally in SCA	Square wave generator	800 cps sine wave reference	800 cps square wave reference
Torque motor and 1X sine wave generator	IMU HEATER CURRENT	Blocking oscillator-rectifier-filter	0 to 28 vdc discrete	0 to 4.4 vdc
	IMU BLOWER CURRENT	Transformer-rectifier-filter	28 v, 800 cps	4.3 vdc (at 28 v input)
	IG RSLV SIN MG RSLV SIN OG RSLV SIN	Amplifier-demodulator	800 cps, 0 or pi phase	0 to 5 vdc

(Sheet 3 of 5)

Table 4-I. Circuits in SCA Modules

Name of Module	Name of Signal	Type of Signal Conditioning Circuit	Type of Signal Conditioned	Nominal Output Voltage Range
Torque motor and IX sine gimbal resolver (cont)	IG TORQUE MOTOR MG TORQUE MOTOR OG TORQUE MOTOR	Chopper-amplifier-demodulator	Positive or negative dc	0 to 5 vdc
	SHAFT CDU FINE ERROR TRUN CDU FINE ERROR	Amplifier-demodulator	800 cps, 50 or 230 degree phase	0 to 5 vdc
	2.5 V BIAS	2.5 volt bias supply	ISS 28 v, 800 cps power	2.5 vdc
Optics and attitude error	SCT TRUN TACH SCT SHAFT TACH SXT SHAFT TACH SXT TRUN TACH ROLL ATT ERROR YAW ATT ERROR	Amplifier-demodulator	800 cps, 0 or pi phase	0 to 5 vdc
	OPTICS 800 CPS 1%	Transformer-rectifier-filter	OSS 28 v, 800 cps power	4.5 vdc (at 28 v input)
	2.5 V BIAS	2.5 volt bias supply	OSS 28 v, 800 cps power	2.5 vdc

(Sheet 4 of 5)

Table 4-I. Circuits in SCA Modules

Name of Module	Name of Signal	Type of Signal Conditioning Circuit	Type of Signal Conditioned	Nominal Output Voltage Range
<p>N/A</p> <p>These signals are routed through flight qualification SCA without conditioning. These are not PGNCS signals.</p>	<p>NAV BASE ROLL (X) VIBRATION</p> <p>NAV BASE PITCH (Y) VIBRATION</p> <p>NAV BASE YAW (Z) VIBRATION</p>	<p>Straight-through wiring</p>	<p>N/A</p>	<p>N/A</p>

4-8.2 SIGNAL CONDITIONING CIRCUITS. The modules used in the flight qualification SCA and operational SCA contain eight types of circuits. Five types of circuits condition the PGNCS signals, and three types of circuits provide reference voltages required to operate the signal conditioning circuits. The five types of signal conditioning circuits are:

- 1) Chopper-amplifier-demodulator.
- 2) Amplifier-demodulator.
- 3) Blocking oscillator-rectifier-filter.
- 4) Transformer-rectifier-filter.
- 5) Temperature sensor amplifier.

A 2.5 volt dc bias is applied to the output of each amplifier-demodulator and chopper-amplifier-demodulator circuit in the SCA. These circuits, which condition 0 or pi phase signals and bipolar dc signals, have an output range of -2.5 to +2.5 volts instead of the 0 to 5 volt range required for all telemetry signals. The required 0 to 5 volt output is obtained from these circuits by connecting a 2.5 volt dc bias in series with the output of each circuit. Therefore, the 2.5 volt dc bias low becomes the common low to the telemetry system (see figures 4-39 and 4-40). The 2.5 volt dc bias high is connected to the signal output low and becomes the reference point for the 0 to 5 volt output of these circuits. In this manner a 0 phase signal, after conditioning, may be represented as a dc voltage above the 2.5 volt reference. A pi phase signal, after conditioning, may be represented as a dc voltage below the 2.5 volt reference. Bipolar dc signals from the PGNCS, which may be positive or negative and have a zero volt reference, may be represented in a similar manner after conditioning. Positive voltages may be represented as a voltage above the 2.5 volt reference and negative voltages may be represented as a voltage below the 2.5 volt reference.

No bias is required for the blocking oscillator-rectifier-filter, transformer-rectifier-filter, and temperature sensor amplifier circuits. The normal output of these circuits is within the 0 to 5 volt range required by the telemetry system.

4-8.2.1 Chopper-Amplifier-Demodulator. The chopper-amplifier-demodulator circuit conditions negative or positive dc signals. The incoming signal is applied to a chopper circuit consisting of two dual-emitter chopper/switch transistors. The chopper modulates an 800 cps square wave reference with the dc input. The modulated square wave, which is representative of the magnitude and polarity of the dc input, is transformer-coupled to an amplifier. The amplified signal is transformer-coupled to a phase-sensitive demodulator circuit consisting of two dual-emitter chopper/switch transistors. The switching action of the transistor pairs in both the chopper circuit and the demodulator circuit is controlled by a switch drive circuit consisting of an

BLOCK II PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

800 cps reference applied through a transformer to the base-collector junction of each transistor. The switch drive alternately turns on one transistor while the other transistor is turned off. The output of the demodulator is a pulsating dc signal whose magnitude and polarity are dependent upon the magnitude and polarity of the input signal. The output of the demodulator is filtered and then biased at 2.5 volts dc. This output, which could vary from +2.5 to -2.5 volts at a zero reference, will, as a result of the 2.5 volt reference, remain in a 0 to 5 volt range.

4-8.2.2 Amplifier-Demodulator. The amplifier-demodulator circuit conditions both 0 and pi phase ac signals. The circuit contains an ac amplifier and a phase-sensitive demodulator. The inputs to the amplifier and demodulator are transformer-coupled. The operation of the demodulator is similar to that in the chopper-amplifier-demodulator circuit described above. The magnitude and polarity of the demodulator output, however, is dependent upon the magnitude and phase of the ac signal, respectively. The output of the demodulator is biased at +2.5 volts to produce an output of 0 to 5 volts dc.

4-8.2.3 Blocking Oscillator-Rectifier-Filter. The blocking oscillator-rectifier-filter circuit conditions a 0 or 28 volt dc discrete without loading down the discrete. The PGNCS discrete is applied to a voltage-controlled blocking oscillator which includes one transistor and a three-winding pulse transformer. When the 28 volt discrete is present at the base of the transistor, the blocking oscillator goes into oscillation and produces an ac voltage across the output winding of the pulse transformer. This ac voltage is regulated at approximately 5.6 volts peak by a zener diode, rectified by a half-wave rectifier, and then filtered into an output of approximately 4.3 volts dc. When the input discrete is not present, the output of the circuit is 0 volt.

4-8.2.4 Transformer-Rectifier-Filter. This type of circuit conditions 28 volt, 800 cps or 3,200 cps power into a dc output. The ac input is applied to a stepdown transformer, rectified by a half-wave rectifier, and filtered into a dc output. Most of these circuits are used to provide a dc output voltage which is representative of the magnitude of the ac input. However, the CGC warning channel in the DAC, PIPA temp, and 2.5 vdc bias module has a discrete input consisting of a ground or an open. This discrete is applied to the low side of the stepdown transformer primary. A 3,200 cps reference voltage from the IRIG and PIPA module is applied to the high side of this transformer primary, and when the ground discrete is present, the transformer produces an output which is rectified and filtered to a nominal output of 4.3 volts dc.

4-8.2.5 Temperature Sensor Amplifier. This amplifier circuit converts the resistance value of a temperature sensor in the IMU to a representative voltage. Each temperature sensor amplifier consists of a small encapsulated module which contains an ac/dc power supply and a magnetic amplifier. The ac/dc power supply converts 28 volt dc power into ac and dc voltages required to operate the magnetic amplifier. As the resistance applied to the amplifier input varies, the amplifier produces an output in the 0 to 5 volt dc range.

4-8.3 REFERENCE VOLTAGE CIRCUITS. Reference voltages required to operate the signal conditioning circuits are developed in the following three types of circuits:

- 1) 2.5 volt power supply.
- 2) 800 cps square wave generator.
- 3) 3,200 cps isolation amplifier and multivibrator.

4-8.3.1 2.5 Volt dc Bias Supply. The 2.5 volt dc bias supply provides dc bias voltage for the phase-sensitive demodulator circuits. Each 2.5 volt dc bias supply is a transformer-rectifier-filter circuit which converts 28 volt, 800 cps power into a regulated 2.5 volt dc output. The ac input is applied to a stepdown transformer, rectified by a half-wave rectifier, voltage-regulated by a zener diode, and filtered into a regulated 2.5 volt dc output.

The flight qualification SCA contains three 2.5 volt dc bias supplies which provide bias to 30 demodulator circuits. The operational SCA contains one bias supply which provides bias to 16 demodulators. The output of each bias supply is also routed to the telemetry system, so that each bias voltage may be monitored by telemetry.

4-8.3.2 800 CPS Square Wave Generator. The 800 cps square wave generator converts an 800 cps sine wave reference into an 800 cps square wave reference. The sine wave input is transformer-coupled to a two stage amplifier. The output stage of this amplifier is an emitter-follower transistor circuit which is driven to saturation, producing a square wave output. The square wave is used as a reference in the switching circuits in the chopper-amplifier-demodulator circuits.

4-8.3.3 3,200 CPS Isolation Amplifier and Multivibrator. This circuit converts a low voltage, high impedance 3,200 cps reference sine wave to a higher voltage 3,200 cps sine wave, and in addition provides a 3,200 cps square wave output. The input to this circuit, which is the 3,200 cps 1% feedback voltage from the IMU, is transformer-coupled to an amplifier consisting of a dual section transistor. The amplified signal is transformer-coupled to another dual section transistor which is in an emitter-follower circuit. The output of the emitter-follower circuit, which is in phase with the 3,200 cps input to the amplifier, is applied to a multivibrator circuit, and is also routed externally to be used as 3,200 cps excitation in the DAC, PIPA temp, and 2.5 volt dc bias module.

The multivibrator, which otherwise would free-run, is synchronized at 3,200 cps by the amplified sine wave input and produces a square wave output. This 3,200 cps square wave is used as a reference signal in the phase-sensitive demodulators in the IRIG and PIPA signal conditioning channels.