

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

# APOLLO

## GUIDANCE, NAVIGATION AND CONTROL

E-1926

A DESIGN PROCEDURE FOR  
RADIATION HARDENING CERTAIN  
NOR GATE LOGIC CIRCUITS

by

Harold E. Maurer

March 1966

**MIT**

CAMBRIDGE 39, MASSACHUSETTS

**INSTRUMENTATION  
LABORATORY**

# APOLLO

## GUIDANCE, NAVIGATION AND CONTROL

Approved: Eldon C Hall Date: 4/4/66  
ELDON C. HALL, DIRECTOR, DDG  
INSTRUMENTATION LABORATORY

Approved: David G Hoag Date: 12 Dec 66  
DAVID G. HOAG, DIRECTOR  
APOLLO GUIDANCE AND NAVIGATION PROGRAM

Approved: Ralph R. Ragan Date: 12 Dec 66  
RALPH R. RAGAN, DEPUTY DIRECTOR  
INSTRUMENTATION LABORATORY

E-1926

### A DESIGN PROCEDURE FOR RADIATION HARDENING CERTAIN NOR GATE LOGIC CIRCUITS

by

Harold E. Maurer

March 1966

**MIT** INSTRUMENTATION  
LABORATORY

CAMBRIDGE 39, MASSACHUSETTS

INDEX...  
DATE  
3-31-66

OPR  
MIT

#  
E-1926

T PGM  
K APO A

SUBJECT

COPY # 71

SIGNATURE  
MAURER  
E-1926  
08A-56

## ACKNOWLEDGEMENT

This report was prepared under DSR Projects 55-191 and 55-238, sponsored by the Manned Spacecraft Center of the National Aeronautics and Space Administration through Contracts NAS9-153 and NAS9-4065.

The author wishes to thank Professor K. S. Fu for his assistance and criticism and the Publications Group of the M. I. T. Instrumentation Laboratory for the preparation of the illustrations.

The publication of this report does not constitute approval by the National Aeronautics and Space Administration of the findings or the conclusions contained therein. It is published only for the exchange and stimulation of ideas.

E - 1926

A DESIGN PROCEDURE FOR RADIATION HARDENING  
CERTAIN NOR GATE LOGIC CIRCUITS

ABSTRACT

A design procedure is developed which increases the radiation tolerance of switching and computing circuits constructed of an RTL Nor gate. Logic diagrams are hardened by the use of a modified Nor gate which is constructed of these RTL gates. A unique concept is introduced and called "minimum fanout" and restrictions are imposed by the design procedure on the minimum fanout of the modified Nor gate. The constraints on the hardening procedure imposed by conventional fanin and fanout restrictions result in a set of equations which can be viewed as an integer linear programming problem. The limitations on the existence of a solution to this programming problem are also the limitations on the existence of this type of permanent damage, radiation hardened logic diagram.

by H. E. Maurer  
March 1966

## INTRODUCTION

If Nor gate logic circuits must withstand a radiation environment which produces permanent damage in the logic elements, then it could become necessary to increase the radiation tolerance of these logic circuits. Nor gates are sufficient to generate any Boolean function of  $n$  variables and their exclusive use can mean that sufficient statistical experience can be accumulated to carry out reliability studies even though only a few computing machines are ever built.

A feasible hardening procedure, explored here, is to substitute the modified (redundant) Nor gate of Fig. 3 for the original Nor gate of Fig. 1. In the range of interest the magnitude of the collector resistor is negligibly affected by the nuclear flux and so the conventional rated fanout of gates in the hardened diagram is identical to that of the original gate. The fanin is limited to one input per active device in the original gate and to one input per input terminal in the modified Nor gate.

The radiation tolerance of the gate increases with increased fanout (Fig. 13). Therefore, the specification on nuclear flux places a lower bound on the allowable fanout. This lower bound shall be referred to as "minimum fanout."

A violation of fanin and fanout restrictions might result from direct substitution of the modified Nor gate in the original logic diagram and so a hardened diagram might prove impossible to construct. The existence of this type of permanent damage radiation hardened logic diagram is considered. As can be seen from Fig. 13, if the logical one voltage level of the original Nor gate is retained for the redundant Nor gate but the magnitude of the logical zero voltage is raised, then the radiation tolerance of a logic diagram constructed of the modified gate can be further improved. This possibility is also explored.

## A NOR GATE AND ITS FAILURE MECHANISM

The modified gate will have the same conventional rated fanout as the original Nor gate since this parameter is determined for both gates by the magnitude of the collector resistor. In the range of interest this magnitude is unaffected by the radiation environment, and so the upper bound on the fanout of each modified gate in the hardened diagram is unchanged from that of the original gates. However, the nuclear environment specification places a lower bound on the allowable fanout. Therefore, the fanout of a modified Nor gate in the hardened diagram must remain in the range defined by the conventional rated fanout of the original Nor gate,  $F_m$ , and the minimum fanout, MFO, i.e.,

$$\text{MFO} \leq \text{fanout} \leq F_M$$

The radiation induced permanent damage failure mechanism for the Nor gate of Fig. 1 was experimentally determined to be an increase in the minimum fanout with increased nuclear particle flux. This effect is sketched in Fig. 12 which is a logical extension of Fig. 13. A measure of the minimum fanout is the minimum number of Nor gates which can be switched from On (low collector voltage) to Off (high collector voltage) by a Nor gate which is switched from OFF to ON.

## RADIATION HARDENING PROCEDURE

If a logic diagram constructed of Nor gates with allowable fanout  $F$ , and fanin  $I$ , does not satisfy its radiation specification, then it has been experimentally verified (1)\* that the threshold of permanent damage can be extended by substituting for each original Nor gate a redundant Nor gate and, if necessary, by redefining the logical zero voltage. This method is especially attractive for use with integrated circuits as the increase in the number of components does not result in a prohibitive increase in physical size, weight, or complexity of interconnections. The procedure is as follows:

1. Given a logic diagram to be hardened, refer to a plot of the Nor gate failure mechanism as illustrated by Figure 4 and choose an input redundancy factor  $M_0$  where  $M_0 < F/I$  and the minimum fanout, MFO, is less than  $F$ . If MFO must be greater than  $F$  if the required level of radiation resistance is to be reached then try  $M_0 \geq F/I$  and proceed. Generate a new diagram by the substituting for each logic element a Nor gate with a redundancy factor  $M_0$  (Figure 3).
2. If fanin restrictions are exceeded, then modify the diagram by repeated application of the logical identity of Figure 5.
3. If fanout restrictions are violated, then provide enough copies of each logic element to satisfy the requirements.
4. Add enough dummy logic elements to provide the required minimum fanout, i. e.,  $F \geq \text{actual fanout} \geq \text{MFO}$ .

The following examples serve to illustrate the hardening procedure.

Example 1. Radiation harden the logic diagram of Figure 6 where  $F = 3$  and  $I = 2$ .

Solution:  $F/I = 3/2 = 1$  so try  $M = 1$  and examine Figure 4 for the possibility of a solution. If such a possibility is seen to exist, then proceed with  $M_0 = 1$ . The basic diagram violates fanout and fanin restriction, so use steps 2, 3, and 4 of the hardening procedure. The results are illustrated in Figure 7, 8, and 9. If the final radiation hardened logic diagram of Figure 9 does not meet radiation specifications then try  $M=2$  and repeat the hardening procedure. If such a logic diagram is found to exist, then the threshold of permanent damage can be further extended.

Example 2. Radiation harden the logic diagram of Figure 10 where  $F=2$ ,  $I=1$ , and the radiation specification clearly requires the  $M_0 \geq 2$ .

Solution: It can be seen that the problem has no solution.

\*Note: Numeral superscripts refer to similarly numbered references in the Bibliography.

## EXISTENCE OF HARDENED LOGIC DIAGRAMS

Does a logic diagram exist, which realizes a given Boolean function at a desired level of particle flux and which is generated with the Nor gates of the preceding section. To establish the limitations on the existence of such a logic diagram, the approach will be to:

- a. demonstrate that a diagram exists which has an input redundancy factor  $M$ , satisfies the fanin requirements, but violates the fanout requirements.
  - b. prove that the diagram of (a) can be modified for the case of  $M < F/I$  and
  - c. demonstrate that the diagram of (b) can be modified, by the addition of dummy logic elements, to withstand a particle flux of  $\phi_M$  as defined by Figure 4.
1. Generate a logic diagram with Nor gates which realizes the given Boolean function and for which no fanin is allowed to exceed  $I$  where  $I \geq 2$ . Since the use of Nor gates only is sufficient to realize any given Boolean function, generate such a logic diagram and if any fanin should exceed  $I$ , reduce it to  $I$ , where  $I \geq 2$  by reference to the logical identity of Figure 5. Next replace each Nor gate by the redundant Nor gate of Figure 3. The resulting logic diagram satisfies fanin requirements but may not satisfy fanout requirements.
  2. Prove that the logic diagram of step 1 can be modified to satisfy fanout requirements if  $M < F/I$ . Consider arbitrary logic elements  $i$  and  $j$  of the logic diagram of step 1 as illustrated in Figure 11. Let  $k_{ij}$  be the number of wires coupling the output of the  $i$ th element to the input of the  $j$ th element.

Then

$$\sum_i k_{ij} \leq I \text{ for all } j \quad (1)$$

but the fanout restrictions,  $0 \leq k_{ij} M \leq F$  may not be satisfied, where  $k_{ij}$ ,  $M$ ,  $F$ , and  $I$  are positive integers. If the fanout restrictions are not satisfied, provide  $X_i$  copies of the  $i$ th logic element so that the fanout restrictions as expressed by equation 2, are satisfied.

$$\sum_j k_{ij} M X_j \leq F X_i \quad (2)$$

It is also desired to minimize the total number of elements,  $N$ ,

$$N = \sum_i X_i \quad (3)$$

where all  $X_i$ 's are positive integers.

Equations 2 and 3 are recognized as an integer linear programming problem<sup>(2)</sup>. Goto<sup>(3)</sup> established the existence of a solution to the above problem for the case  $M=1$ . If the equations are rewritten, then advantage can be taken of his results.

$$\sum_i K_{ij} \leq I \text{ for all } j \quad (4)$$

$$\sum_j K_{ij} X_j \leq \left(\frac{F}{M}\right) X_i \quad (5)$$

If  $F/M$  is substituted for  $F$  in the equations of Goto, then his results can be used directly, i. e., a logic diagram will exist if  $F/M > I$  but if  $F/M \leq I$  then a solution may or may not exist. The resulting logic diagram satisfies the fanin and fanout requirements and has a redundancy factor of  $M$ . The minimum fanout requirement can next be met by providing sufficient dummy logic elements.

Now consider the situation in which logic elements are allowed to have different input redundancy factors,  $M_j$ . The defining equations are:

$$\sum_i K_{ij} \leq I \text{ for all } j \quad (6)$$

$$\sum_j K_{ij} M_j X_j \leq F X_i \quad (7)$$

If it is desired to minimize the total number of elements  $N$ , then equations 3, 6, and 7 are recognized as an integer linear programming problem. The establishment of the existence of a solution to this problem would be of interest.

## SUMMARY

A design procedure was presented which produces reliable switching and computing circuits constructed of a particular Nor gate logic element with its individual, radiation induced, permanent damage failure mechanism. The Nor gate failure mechanism was experimentally determined to be a reduction in minimum fanout with increased nuclear particle flux. The procedure is a flexible building block approach which may allow a given diagram to be hardened with a minimum expenditure of components and assures that adequate statistical information can be accumulated for reliability analyses although the method fails at sufficiently high levels of flux since the transistor current gains approach unity. The results should be applicable to the hardening of other Nor gate logic circuits which are constructed with silicon transistors.

The constraints on the hardening procedure imposed by fanin and fanout restrictions result in a set of equations which can be viewed as an integer linear programming problem. The limitations on the existence of a solution to this programming problem are also the limitations on the existence of this type of permanent damage, radiation hardened logic diagrams.

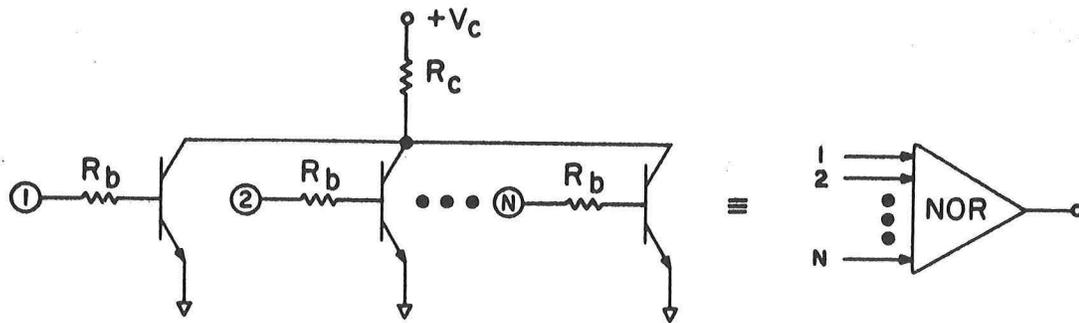


Fig. 1 N input Nor gate

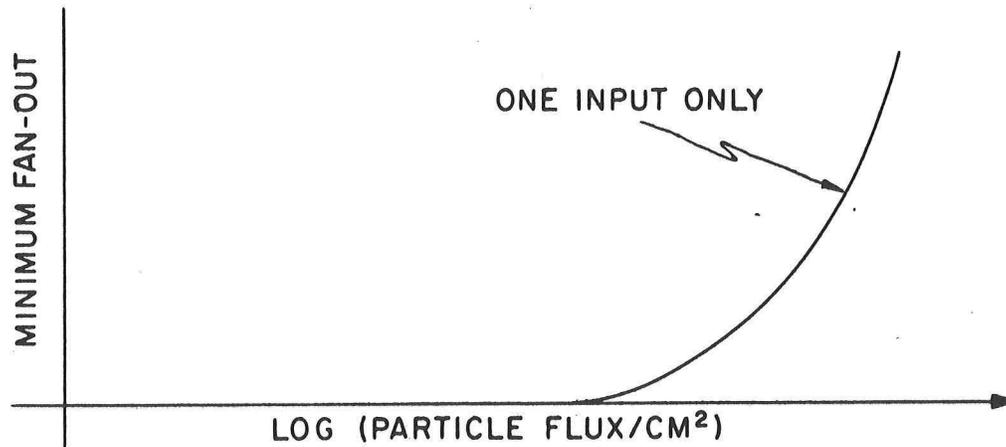


Fig. 2 Nor gate permanent damage failure mechanism.

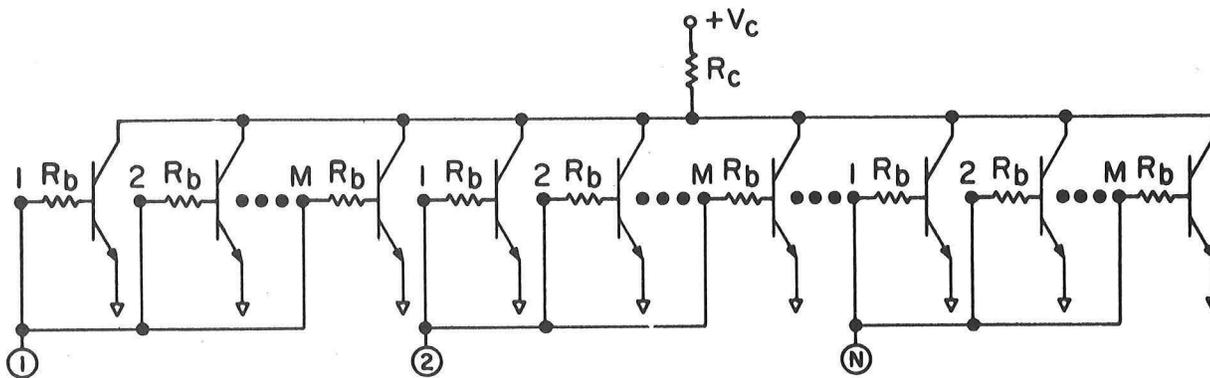


Fig. 3 N input Nor gate with an input redundancy of M.

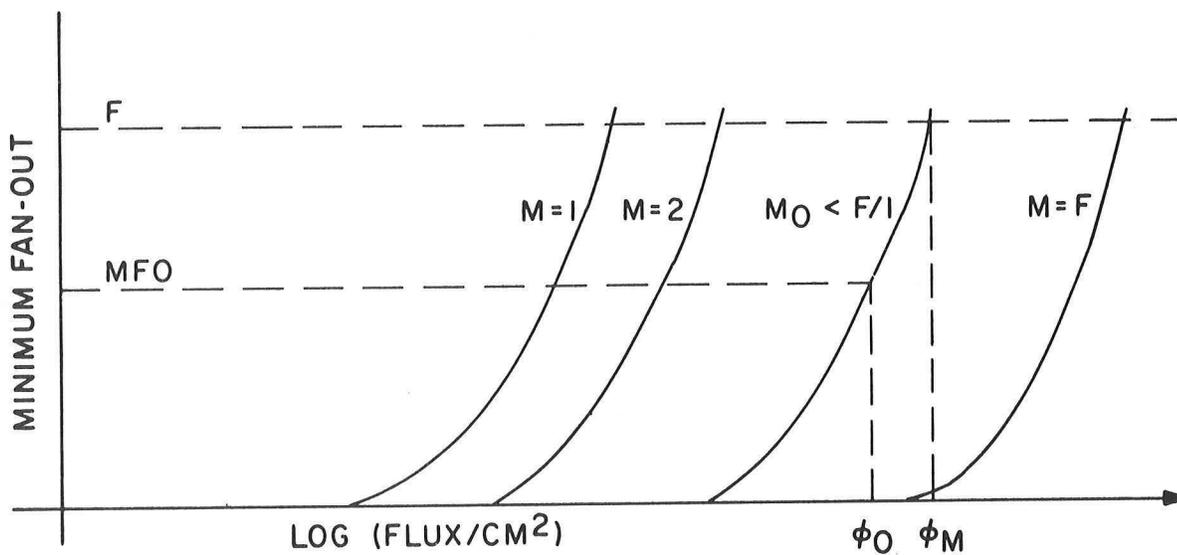


Fig. 4 Sketch of Modified Nor gate failure mechanism as a function of input redundancy for a single input only.

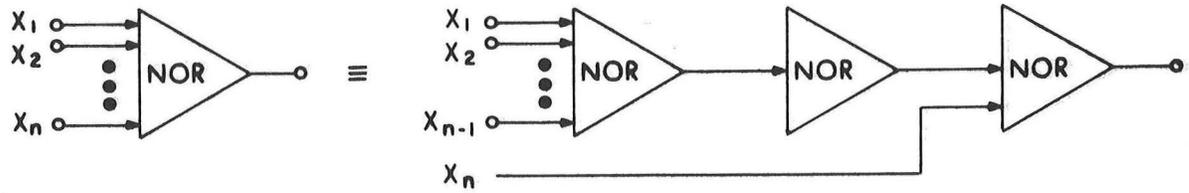


Fig. 5 A logical identity.

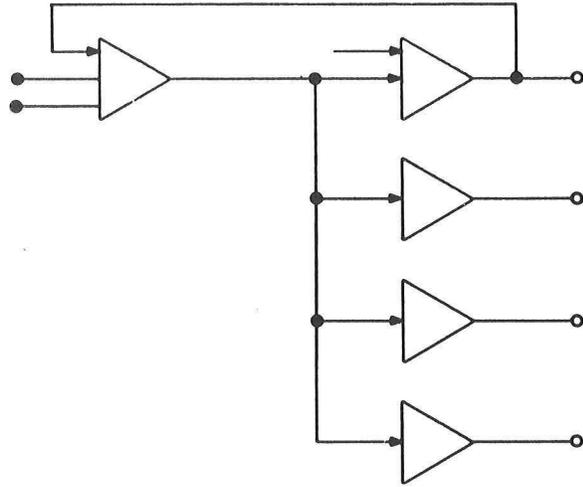


Fig. 6 Basic logic diagram for Example 1.

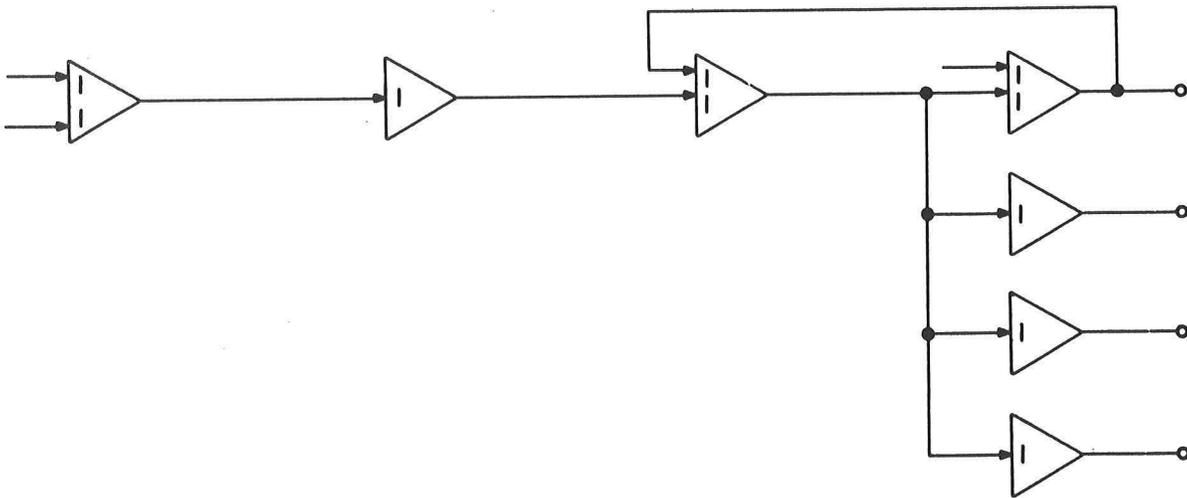


Fig. 7 Modified logic diagram satisfying fan-in requirements.

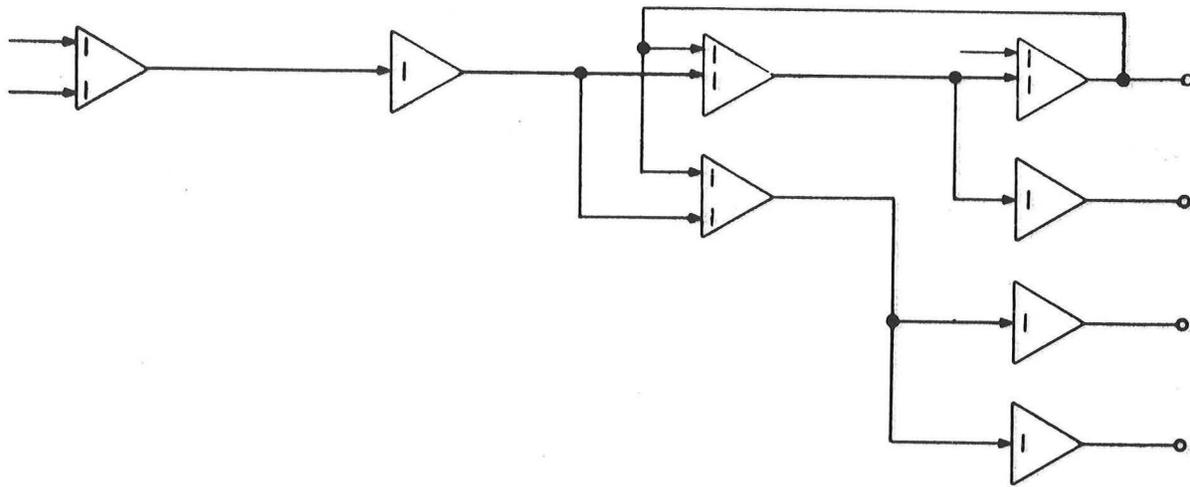


Fig. 8 Modified logic diagram satisfying fan-in and fan-out requirements.

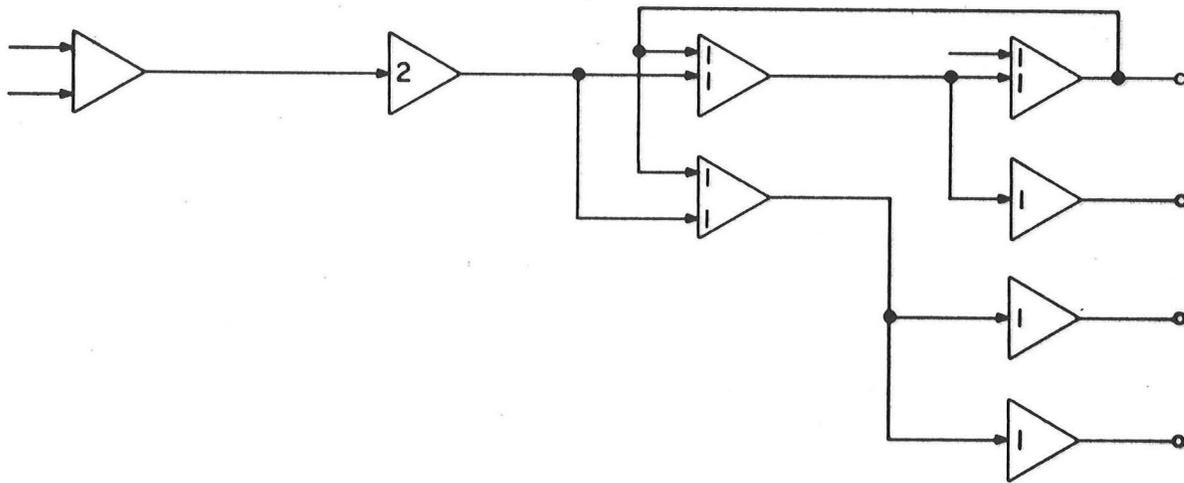


Fig. 9 The final radiation hardened logic diagram.

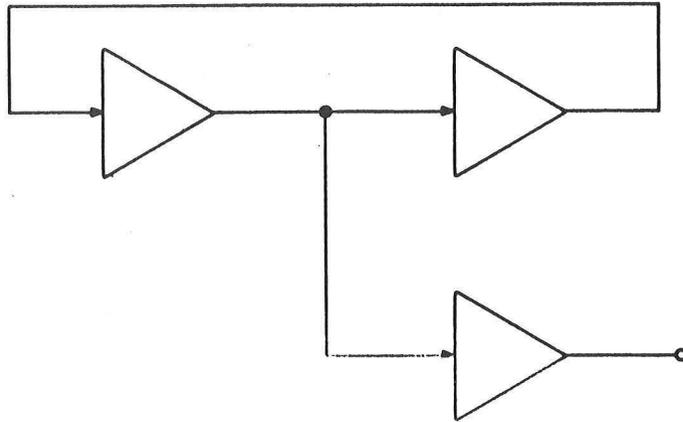


Fig. 10 Basic logic diagram for Example 2.

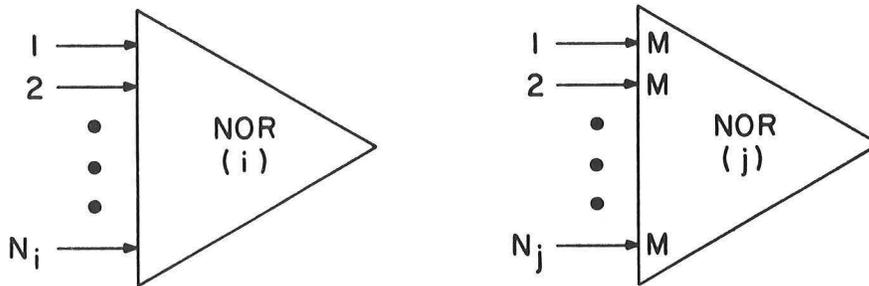


Fig. 11 Arbitrary logic elements of hardened logic diagram satisfying fan-in requirements.

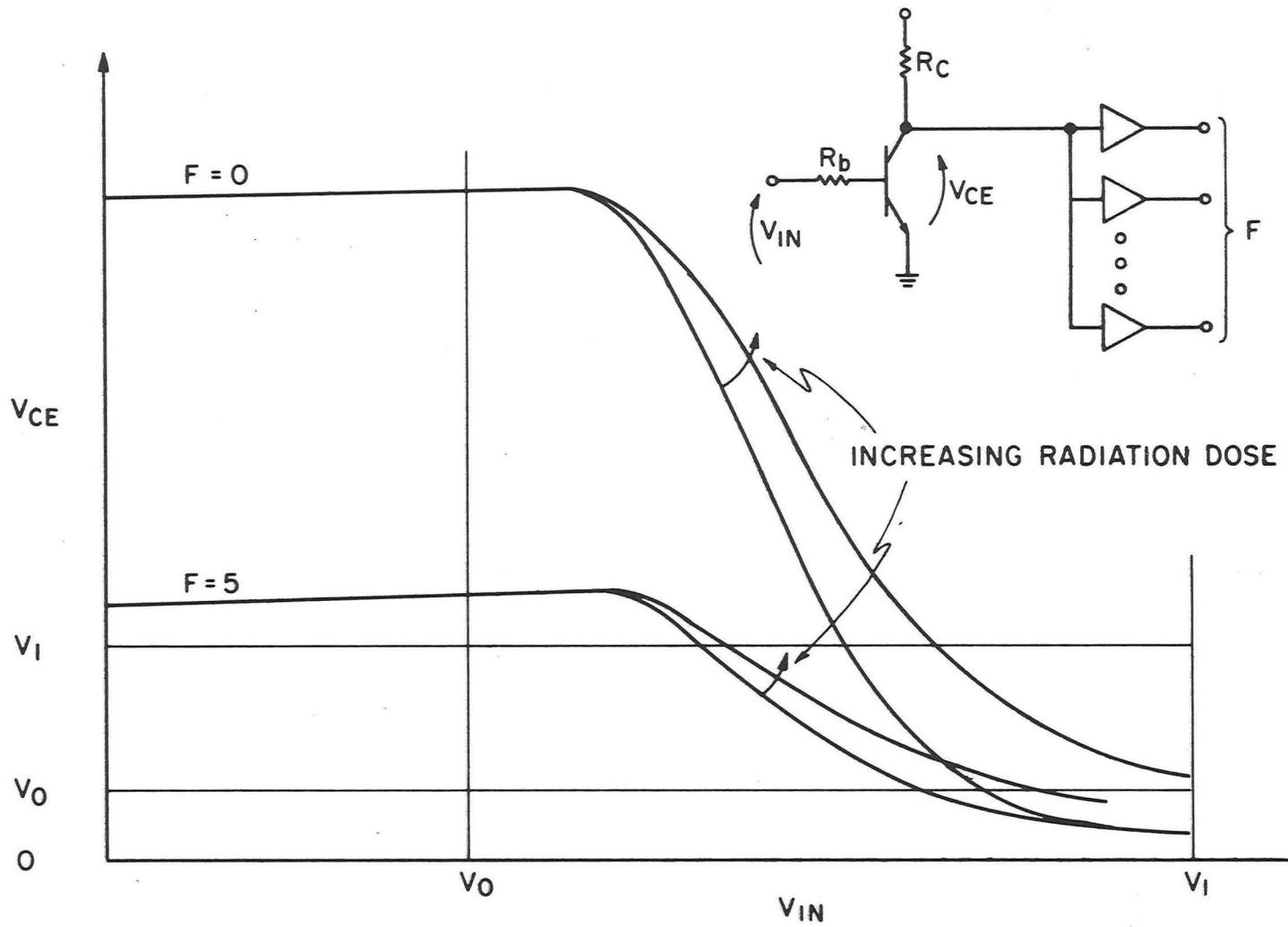


Fig. 12 Permanent Damage Effect of Radiation on Nor Gate S Curve

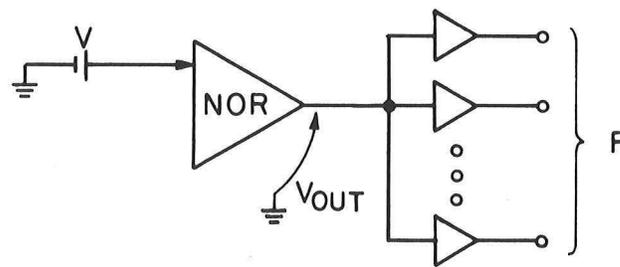
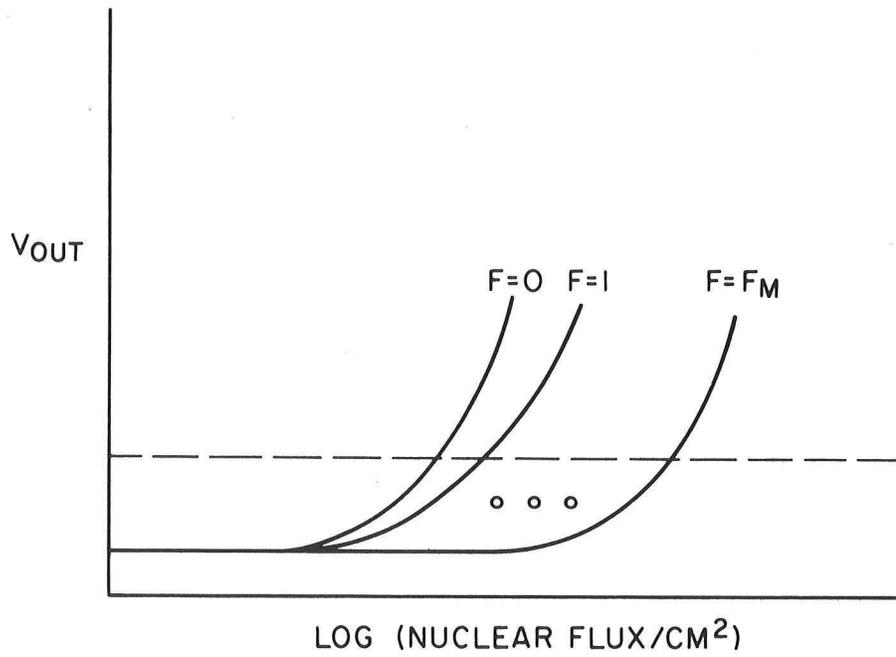


Fig. 13 Response to a Radiation Environment

## BIBLIOGRAPHY

- 1 H. E. Maurer, "An Approach to the Design of Reliable Radiation Hardened Integrated Logic and Sequential Circuits", M. I. T. Instrumentation Laboratory Report T-435, p. 141, August 1965.
- 2 S. Karlin, *Mathematical Methods and Theory in Games, Programming, and Economics*, Reading, Massachusetts: Addison-Wesley, 1962, p. 117.
- 3 E. Goto, "A Note on Logical Gain", *I. E. E. E. Transactions on Electronic Computers*, Vol. EC-13, p. 609, October 1964.

DISTRIBUTION LIST

Internal

M. Adams (MIT/GAEC)	S. Laquidara (MIT/FOD)
J. Alexshun	J. Lawrence (MIT/GAEC)
R. Alonso	T. M. Lawton (MIT/MSC)
R. Battin	J. McKenna
P. Bowditch/ F. Siraco	G. Mayo
D. Bowler	John Miller
E. Copps	J. Nevins
R. Crisp	J. Nugent
J. Dahlen	J. Partridge
J. DeLisle	R. Ragan
E. Duggan	D. Reible
J. B. Feldman	J. Sabo
J. Flanders	N. Sears
Eldon Hall	D. Shansky
D. Hanley	W. Shotwell (MIT/AC)
T. Hemker (MIT/NAA)	W. Stameris
E. Hickey	H. Thaler
D. Hoag	R. Weatherbee
A. Hopkins	L. Wilk
F. Houston	R. Woodbury
A. Koso	W. Wrigley
A. Laats	Apollo Library (2)
A. LaPointe	MIT/IL Library (6)
L. Larson	

External:

W. Rhine (NASA/ MSC) (2)  
NASA/RASPO (1)  
T. Heuermann (GAEC/MIT) (1)  
AC Electronics (3)  
Kollsman (2)  
Raytheon (2)  
Major H. Wheeler (AFSC/MIT) (1)  
MSC: (25 + 1R)  
National Aeronautics and Space Administration  
Manned Spacecraft Center  
Apollo Document Distribution Office (PA2)  
Houston, Texas 77058

LRC: (2)  
National Aeronautics and Space Administration  
Langley Research Center  
Hampton, Virginia  
Attn: Mr. A. T. Mattson

GAEC: (3 + 1R)  
Grumman Aircraft Engineering Corporation  
Data Operations and Services, Plant 25  
Bethpage, Long Island, New York  
Attn: Mr. E. Stern

NAA: (18 + 1R)  
North American Aviation, Inc.  
Space and Information Systems Division  
12214 Lakewood Boulevard  
Downey, California  
Attn: Apollo Data Requirements AE99  
Dept. 41-096-704 (Bldg 6)

NAA RASPO: (1)  
NASA Resident Apollo Spacecraft Program Office  
North American Aviation, Inc.  
Space and Information Systems Division  
Downey, California 90241

ACSP RASPO: (1)  
National Aeronautics and Space Administration  
Resident Apollo Spacecraft Program Officer  
Dept. 32-31  
AC Electronics Division of General Motors  
Milwaukee 1, Wisconsin  
Attn: Mr. W. Swingle

Defense Contract Administration (1)  
Service Office, R  
Raytheon Company  
Hartwell Road  
Bedford, Massachusetts 01730

Mr. S. Schwartz (1)  
DOD, DCASD, Garden City  
605 Stewart Avenue  
Garden City, L.I., New York  
Attn: Quality Assurance

Mr. D. F. Kohls (1)  
AFPRO (CMRKA)  
AC Electronics Division of General Motors  
Milwaukee 1, Wisconsin 53201