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PROJECT



APOLLO

LUNAR EXCURSION MODULE

PRIMARY GUIDANCE, NAVIGATION,
AND CONTROL SYSTEM MANUAL

VOLUME I



ELECTRONICS

DIVISION OF GENERAL MOTORS
MILWAUKEE, WISCONSIN



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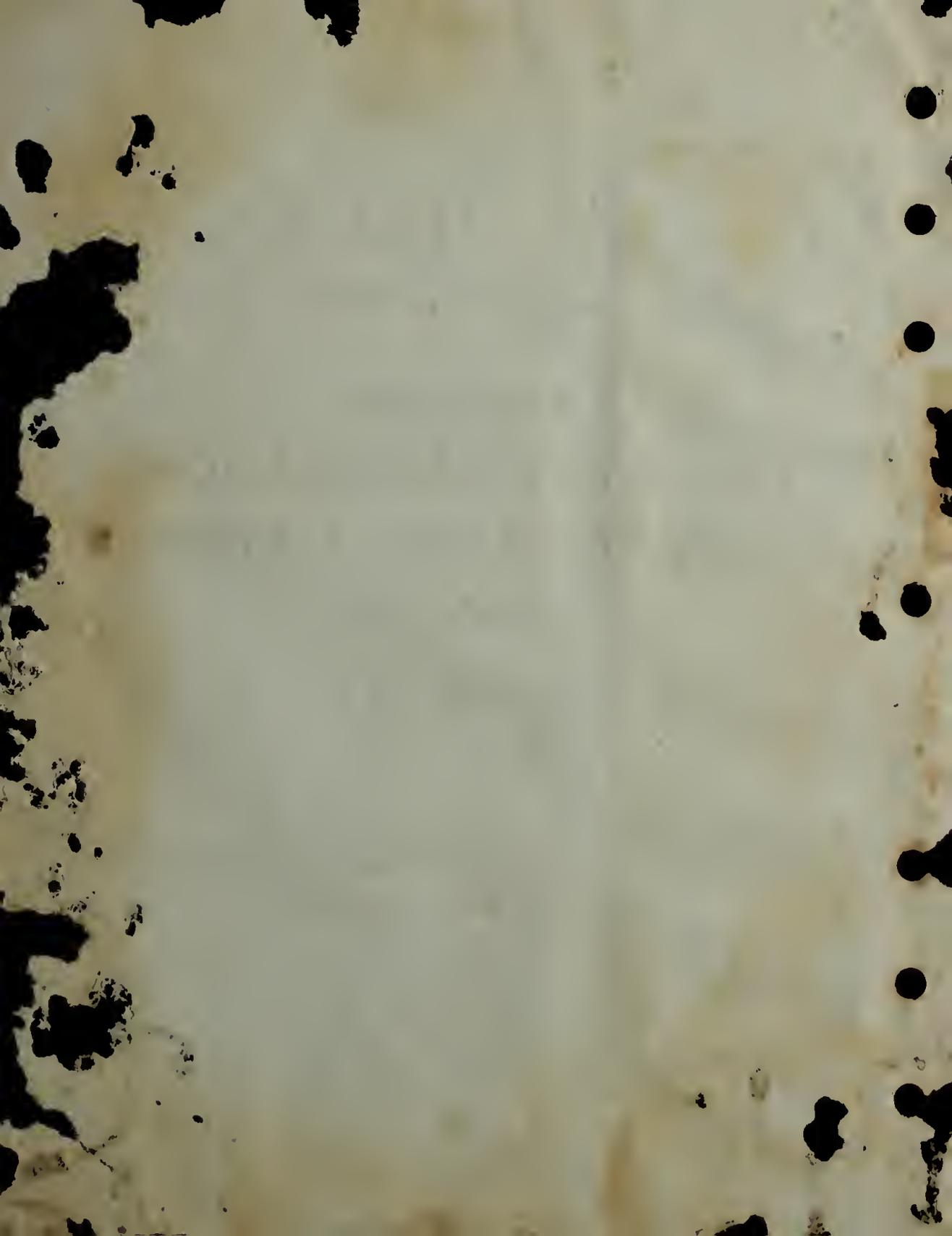
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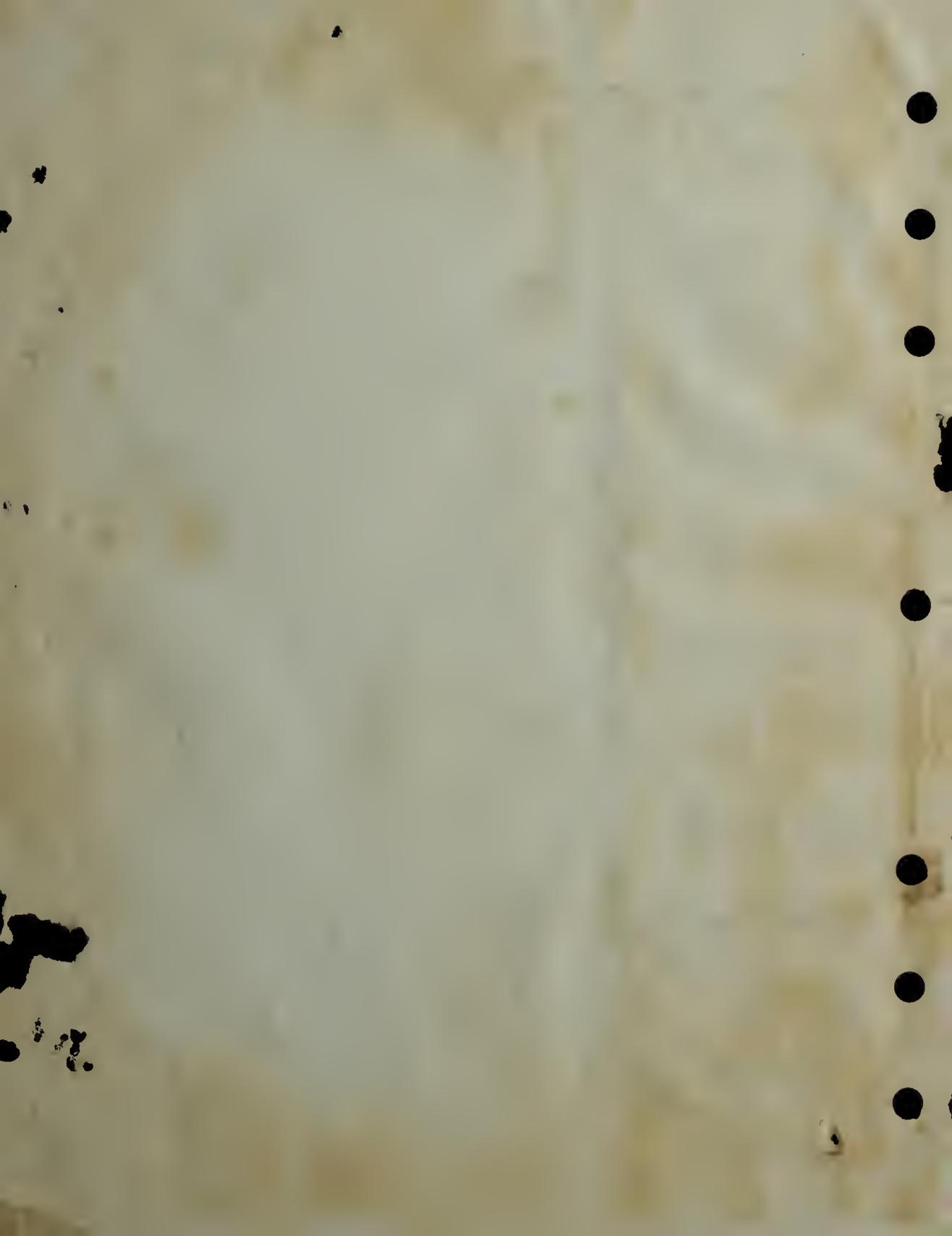
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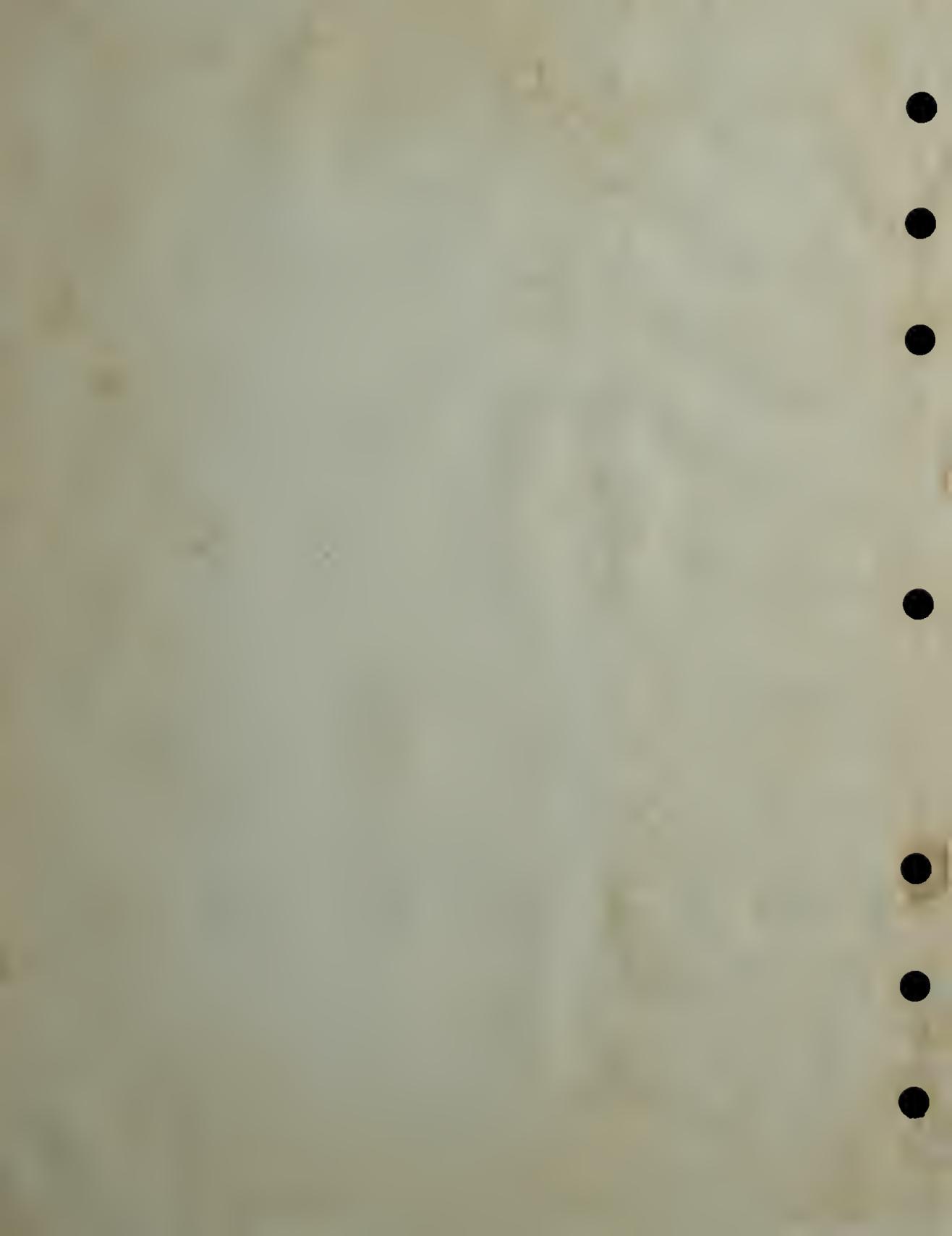
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4-374 Blank	Original	4-424 Blank	Original
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4-376 Blank	Original	4-426 Blank	Original
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7-16 Blank	Original
7-17	Original
7-18 Blank	Original
7-19	Original
7-20 Blank	Original
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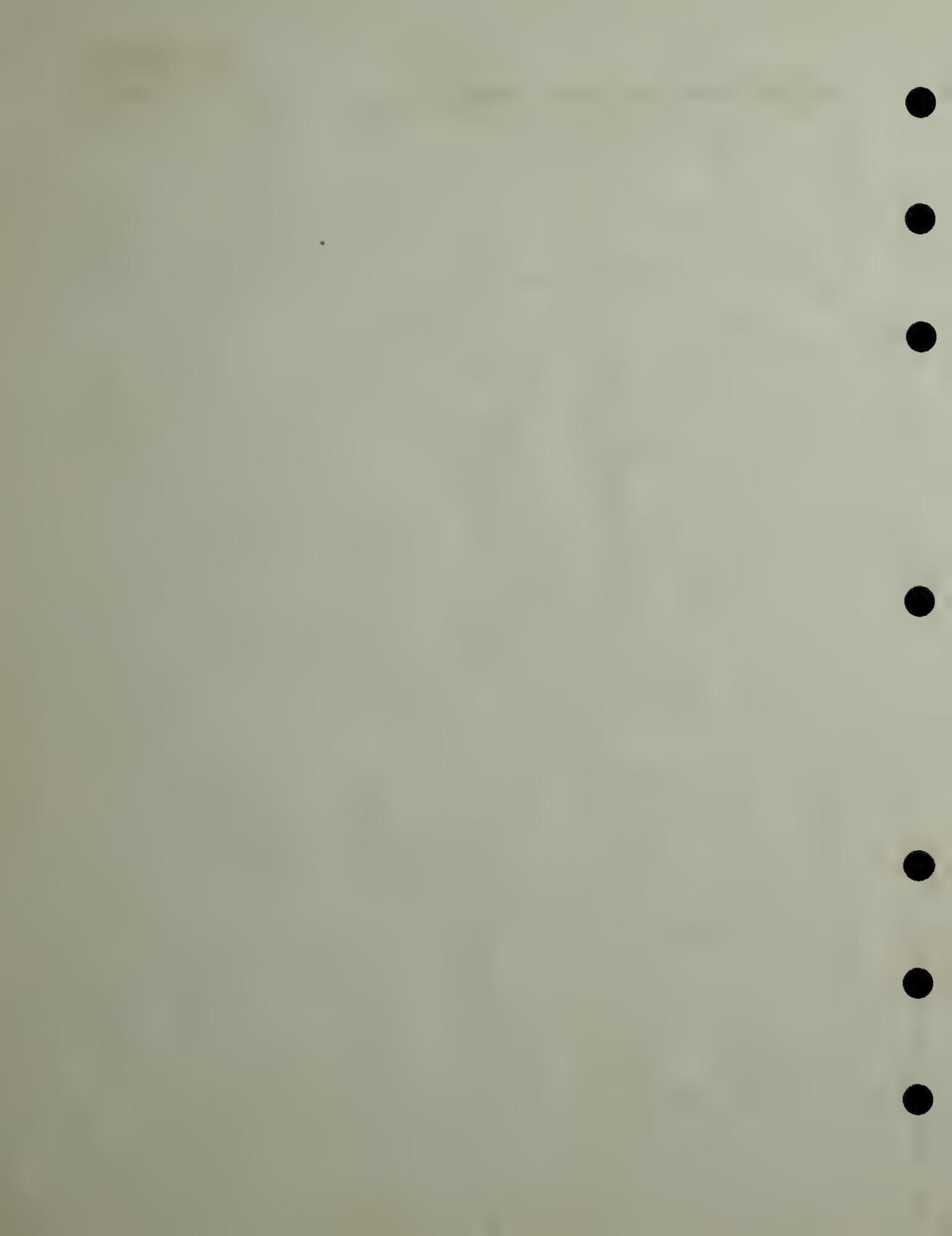
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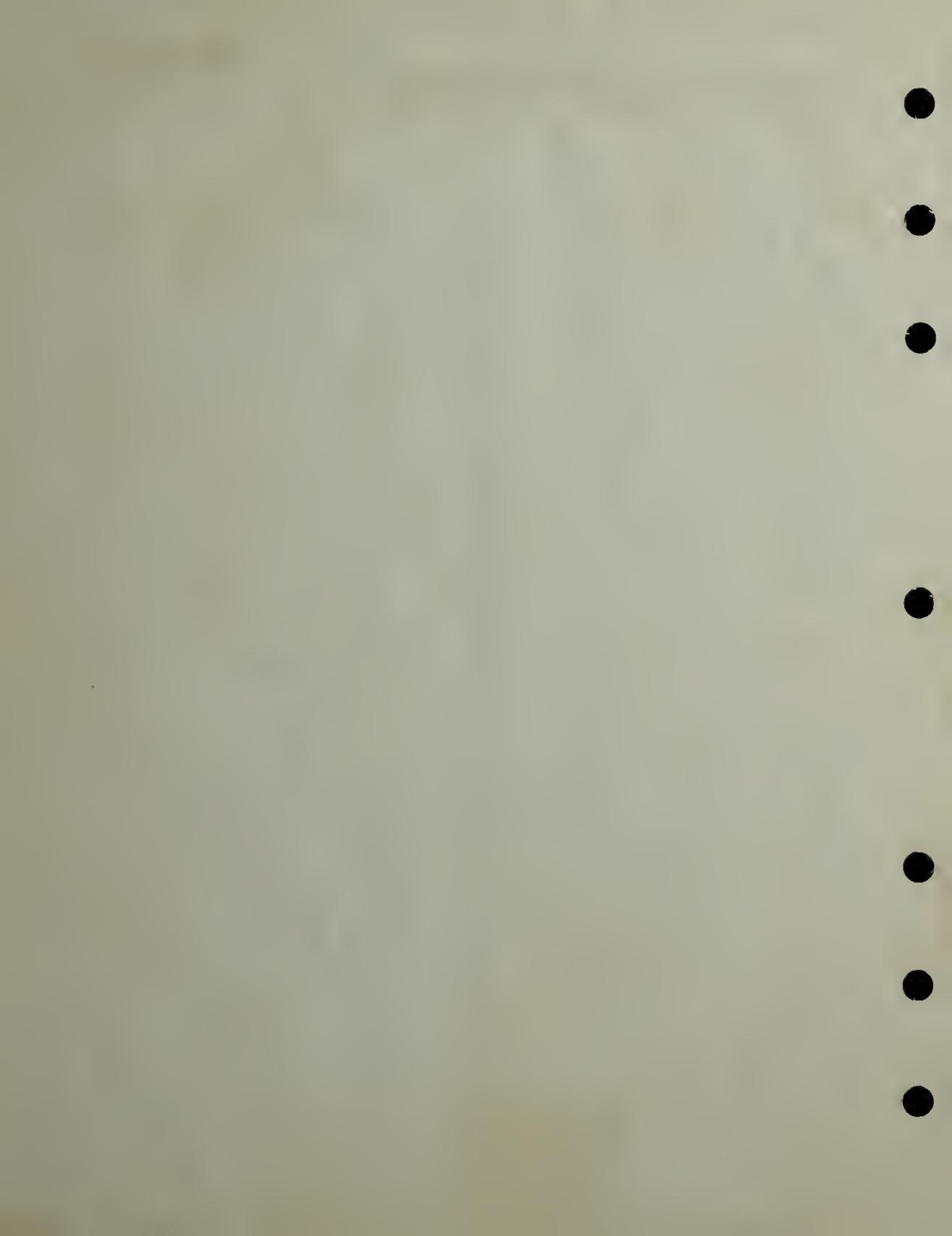
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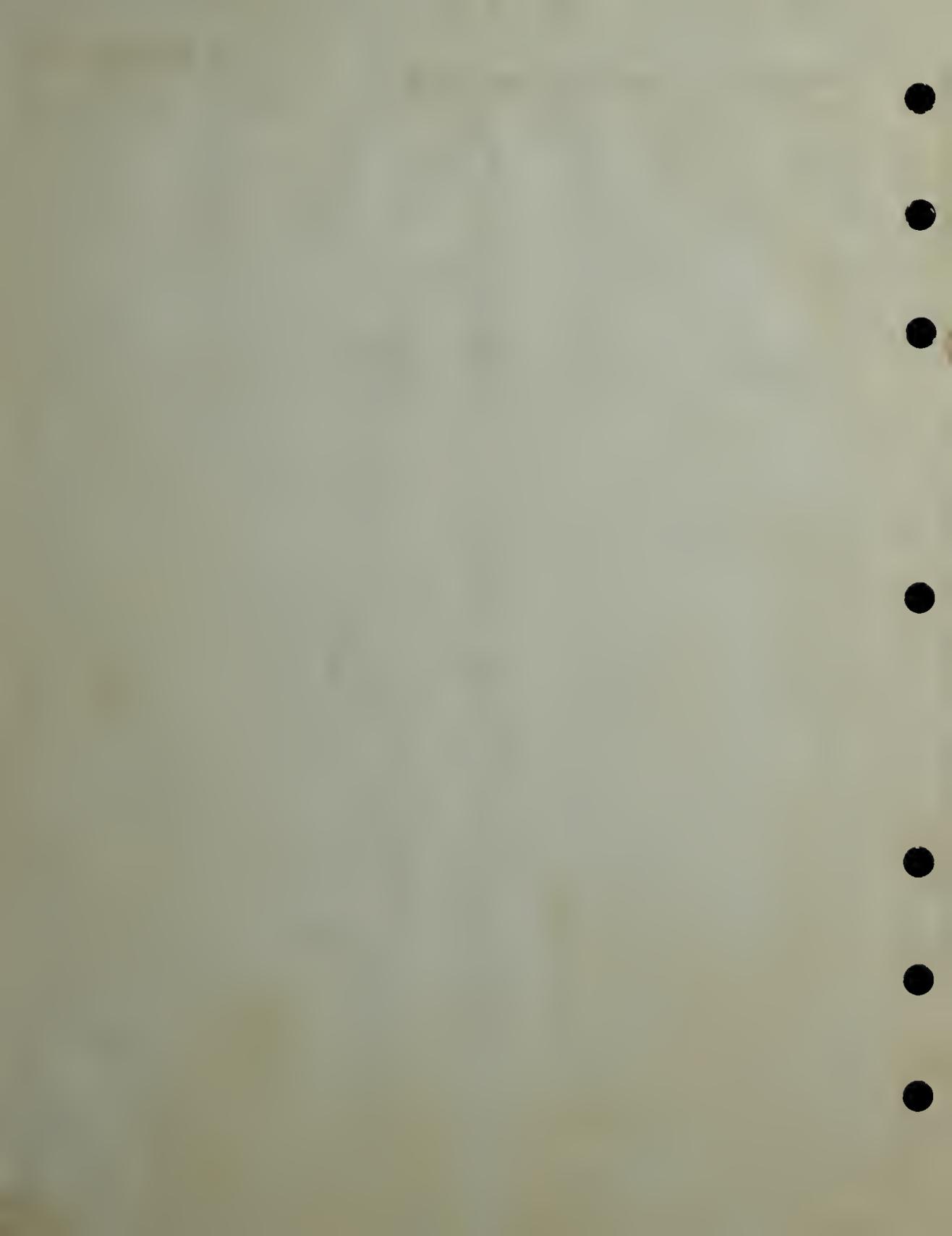
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LIST OF RELATED MANUALS

ND-1021038	Packing, Shipping and Handling Manual
ND-1021039	Auxiliary Ground Support Equipment Manual
ND-1021040	Bench Maintenance Ground Support Equipment Manual
ND-1021043	Block II Primary Guidance, Navigation, and Control System Manual



INTRODUCTION

This manual provides information necessary for checkout, maintenance, and repair of the lunar excursion module (LEM) primary guidance, navigation, and control system (PGNCS) (figure 1-1). Included in the manual are functional analysis, detailed theory of operation, component description, system tie-in, and description of flight operations. The manual also provides for an introduction and complete familiarization with the PGNCS.

Job Description Cards (JDC's) containing detailed step-by-step procedures are contained in separate supplementary volumes. Listings of the JDC's required for given tests and the sequence of performing the JDC's are included in the manual.

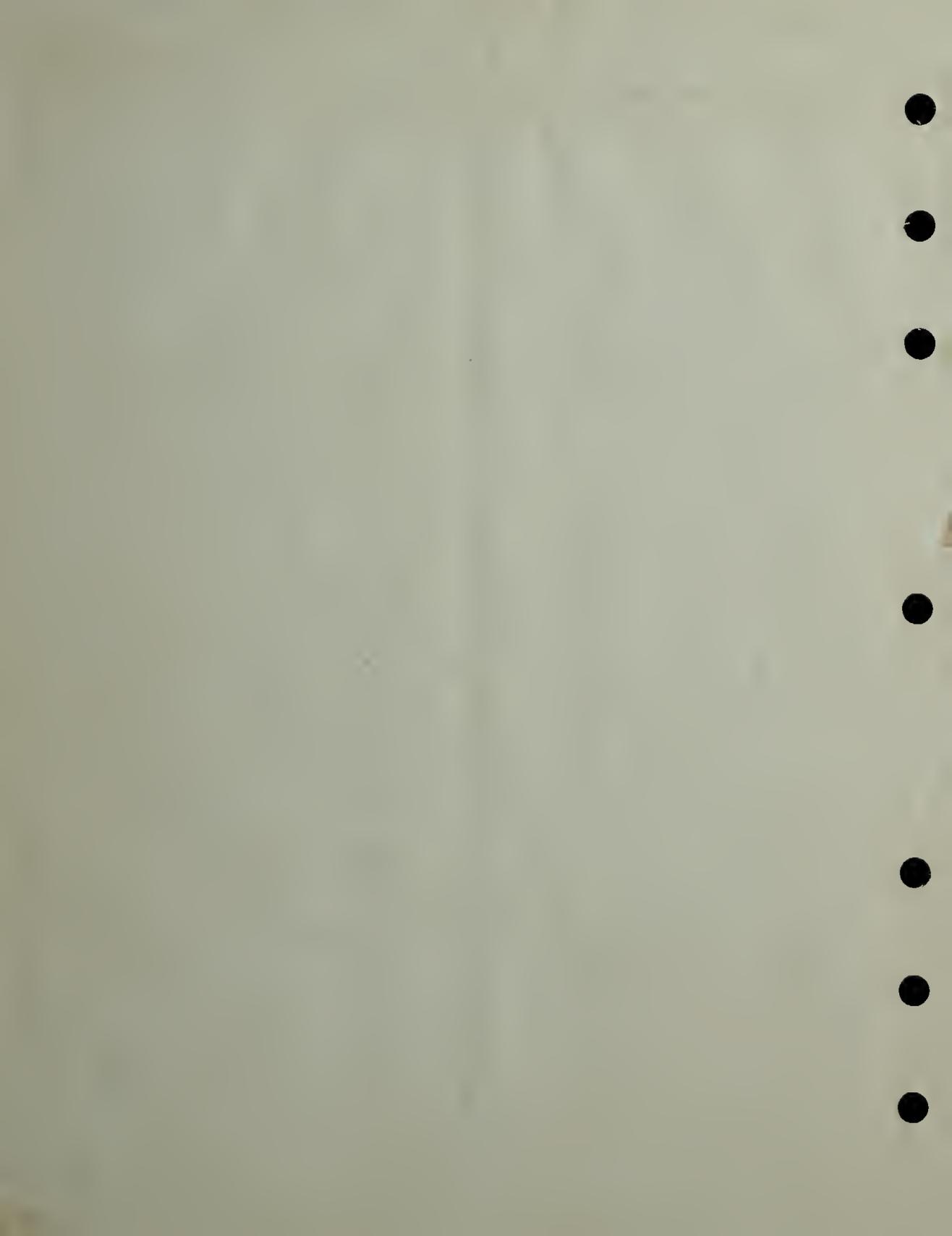
This manual and its JDC's cover PGNCS system part number 6015000-011 and shall be used in the laboratories at Kennedy Space Center, the Manned Spacecraft Center (MSC), and at Grumman Aircraft Engineering Corporation (GAEC). Portions of this manual pertaining to the luminous beacon are also applicable for use in the laboratories at North American Aviation (NAA). Source data available as of 15 January 1966 was used in preparation of the basic issue of this manual.

This manual is prepared in accordance with E-1087 Documentation Handbook and National Aeronautics and Space Administration (NASA) contract NAS 9-497, exhibit D.

Appendix A contains a listing of technical terms and abbreviations used in the manual. Appendix B explains the function and relationship of the System Identification Data List (SIDL) to the manual. Appendix C will contain the logic symbols used in the discussion of the computer logic diagrams.

Changes to the manual are requested by sending a completed Technical Data Change Request (TDCR) form to:

Apollo Field Service Publications, Department 38-01
AC Electronics Division GMC
PLT M1
Milwaukee, Wisconsin 53201



LEM PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

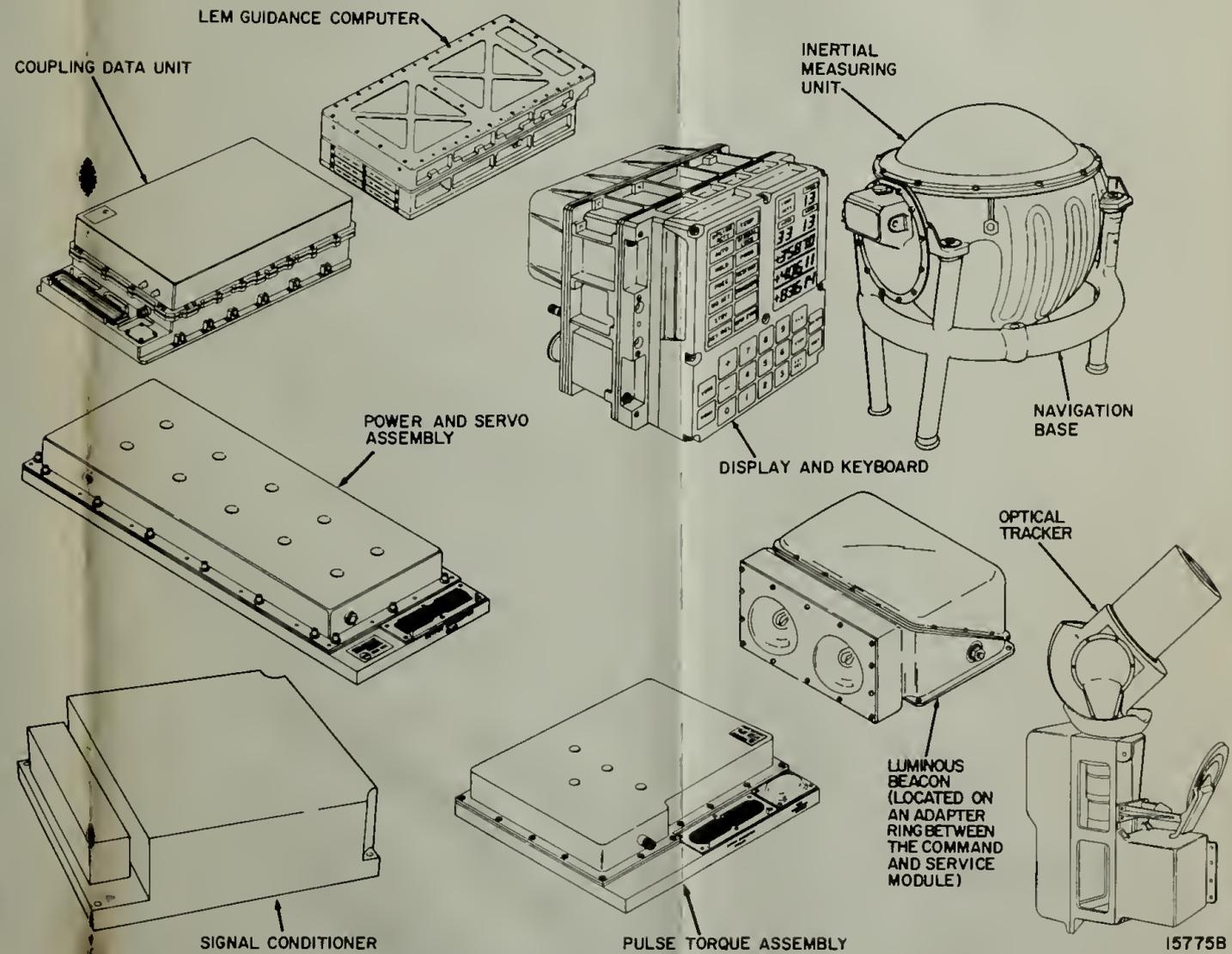


Figure 1-1. LEM Primary Guidance, Navigation, and Control System



Chapter 1

SYSTEM TIE-IN

1-1 SCOPE

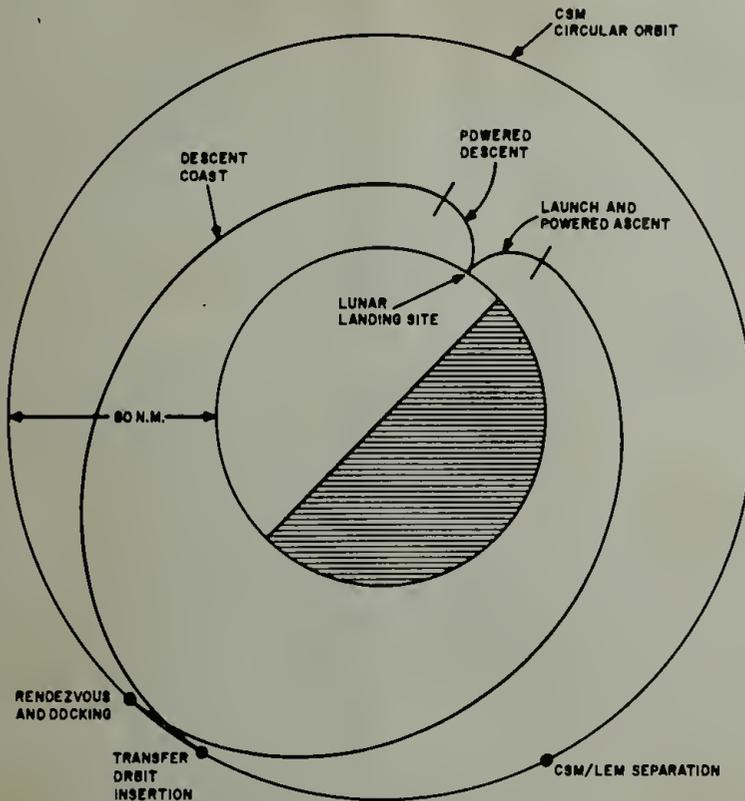
This chapter presents the lunar excursion module (LEM) mission. The chapter also describes the functional interface between the primary guidance, navigation, and control system (PGNCS) and the other spacecraft systems.

1-2 LEM MISSION

The purpose of the LEM mission is to transfer the LEM from a circular lunar orbit into a descent orbit, land two astronauts on the lunar surface, and return them to the orbiting command and service module (CSM). The LEM mission (figure 1-2), with respect to the PGNCS, is best described by dividing it into six phases: separation and transfer orbit insertion, descent coast, powered descent and landing, lunar stay, launch and powered ascent, and rendezvous and docking.

1-2.1 SEPARATION AND TRANSFER ORBIT INSERTION. Approximately one hour before the LEM enters the descent orbit, two astronauts leave the CSM and enter the LEM through the top docking hatch. The crew then checks out the various LEM systems, establishes a voice link, and, after initial PGNCS turnon, establishes a time reference for the LEM guidance computer (LGC), and coarse aligns the inertial measuring unit (IMU) using CSM data. One astronaut then manually commands reaction control system (RCS) jet firing to separate the LEM from the CSM. The IMU is fine aligned. Near the end of the second lunar orbit, the LEM descent engine is fired by the PGNCS and the LEM begins its descent. The timing and duration of LEM descent engine firing is critical, to insure the proper elliptical Hohmann transfer orbit.

1-2.2 DESCENT COAST. During the descent coast phase, the LEM is in free fall on an elliptical flight path. During free fall, the astronauts check out the landing radar (LR). At the perilune of the Hohmann transfer orbit, the LEM is at an altitude of approximately 50,000 feet and has a velocity vector essentially parallel to the lunar surface. During this phase, the PGNCS determines the flight parameters required for powered descent.



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Figure 1-2. LEM Mission Phases

1-2.3 POWERED DESCENT AND LANDING. In preparation for powered descent, an IMU fine alignment is performed. At the perilune of the descent orbit, the PGNCS issues a descent engine start discrete. The descent engine firing slows the LEM which begins the actual descent to the lunar surface. During descent, the PGNCS controls the engine trim and thrust level, controls the LEM attitude, and provides visual displays of the guidance system status. During the final approach and landing, the PGNCS holds the LEM at a constant attitude, allowing the astronaut to view the landing site. The astronaut can select a new landing site by inserting new landing site coordinates into the LGC. The LGC will automatically control the RCS and the descent engine to guide the LEM to the new landing site. Inertially derived flight parameters are updated in the LGC by comparison with the altitude and velocity parameters determined from LR measurements.

LEM PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

1-2.4 LUNAR STAY. After LEM touchdown the astronauts check out all systems for damage and insure that the systems can perform the functions required for a successful ascent. All equipment not required for lunar stay is then turned off. The astronauts survey the surrounding lunar landscape, secure the hatches, and perform a final check on the portable life support system (PLSS). After the LEM is secured, one astronaut, wearing the PLSS, leaves the LEM to explore the lunar surface. The exploring astronaut inspects the LEM and sets up communication antennas. A television system sends pictures of the lunar scene to earth. The astronaut always in direct voice contact with the LEM, explores the lunar surface, makes photographic records, and collects surface samples. After approximately three hours, the astronaut must return to replenish his PLSS. Additional surface explorations depend upon the planned stay time. Near the end of the lunar stay, the PGNCs is brought to an operate condition and the IMU is coarse and fine aligned. The IMU is fine aligned to a known reference coordinate system by making star sighting measurements. The LEM optical device tracks the orbiting CSM and sends data to the LGC which calculates applicable flight parameters in preparation for the launch and powered ascent.

1-2.5 LAUNCH AND POWERED ASCENT. After the astronauts prepare the LEM, the PGNCs determines time of launch and ascent trajectory based on a fixed rendezvous aim point. Mechanical and electrical separation of the two LEM stages takes place and the LGC issues the ascent engine start discrete at a time calculated to effect a successful rendezvous.

During powered ascent, the LEM rises vertically and then is pitched to attain a Hohmann transfer orbit for the rendezvous. Because the ascent engine is a fixed-position, fixed-thrust engine, the LEM attitude during ascent is controlled by the LGC which issues commands to the RCS jets. The LGC determines necessary RCS commands by comparing calculated values with actual flight parameters obtained from the inertial subsystem (ISS), and determines required attitude changes to correct any differences. When the injection of the LEM into the proper elliptical orbit is accomplished, the LGC issues the ascent engine off discrete and the LEM enters the coasting portion of the ascent phase.

1-2.6 RENDEZVOUS AND DOCKING. LEM guidance during this phase is a combination of optical tracking data and inertial data. Azimuth and elevation data from the optical tracking device and velocity and attitude information from the IMU are used by the LGC to control the RCS to maintain attitude and to provide a display of position and velocity information. During rendezvous, the LEM is maintained at an orientation such that the CSM is visible through the vehicle windows.

Terminal rendezvous maneuvers begin when the LEM and CSM are approximately five nautical miles apart. The LGC computes the intercept time and with this data updates the thrust vector and velocity requirements. Three ascent engine burns during terminal rendezvous reduce the closing rate to near zero. The LGC utilizes the RCS

to maintain vehicle attitude during these burns. The final step is docking, which is initiated when the vehicles are approximately 500 yards apart. The astronaut uses the translation controller and attitude controller in a computer-aided manual operation to guide the LEM to hard docking with the CSM. The two astronauts then leave the LEM and transfer to the CSM through the vehicle's forward tunnel to prepare for the return to earth. The LEM is jettisoned following crew transfer to the CSM.

1-3 LEM STRUCTURE

The LEM (figure 1-3) has two stages mated to form one structure: the ascent stage and the descent stage. These stages and the umbilical interconnecting cables can be separated at launch from the lunar surface or because of mission abort during descent.

The approximate LEM external dimensions are shown in figure 1-4. At earth launch, the weight of the LEM is approximately 30,000 pounds.

1-3.1 ASCENT STAGE. The ascent stage, constructed mainly of aluminum alloy, consists of the crew compartment, a midsection, aft equipment bay, tankage sections, associated hatches, and windows.

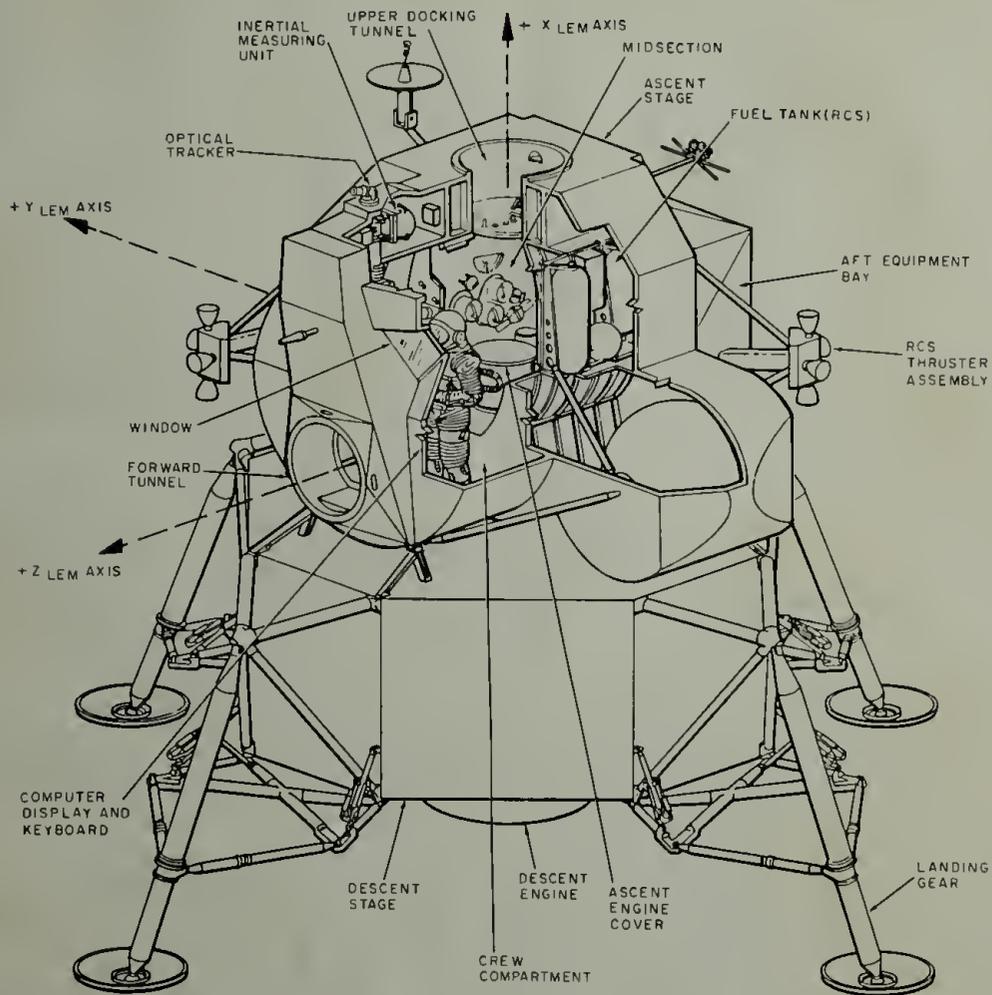
From the crew compartment, the astronauts control all phases of the LEM mission. The crew also uses this compartment as their operations center during their lunar stay.

The displays and controls associated with the PGNCs are located at the front of the crew compartment. The IMU, a portion of its electronics, and the optical tracking device are located in an enclosure above the crew compartment. The remaining PGNCs components are mounted on coldplates to the rear wall of the ascent stage midsection.

The midsection is cylindrical, smaller than the crew compartment, and directly behind it. The ascent engine and related components are in the midsection, the LEM's center of gravity. Also contained in the LEM's midsection are the ascent engine hatch, top hatch, environmental control system (ECS), and equipment that requires crew accessibility.

To transfer from the CSM to the LEM while in lunar orbit, the crew uses the upper docking tunnel at the top centerline of the ascent stage. The forward tunnel, at the lower front of the crew compartment, is used for entering and leaving the LEM while on the lunar surface.

The aft equipment bay, at the rear of the vehicle, is separated from the midsection by a pressure-tight bulkhead. This area houses the glycol loop for the ECS, inverters, batteries, and equipment for the electrical power system (EPS).



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Figure 1-3. LEM

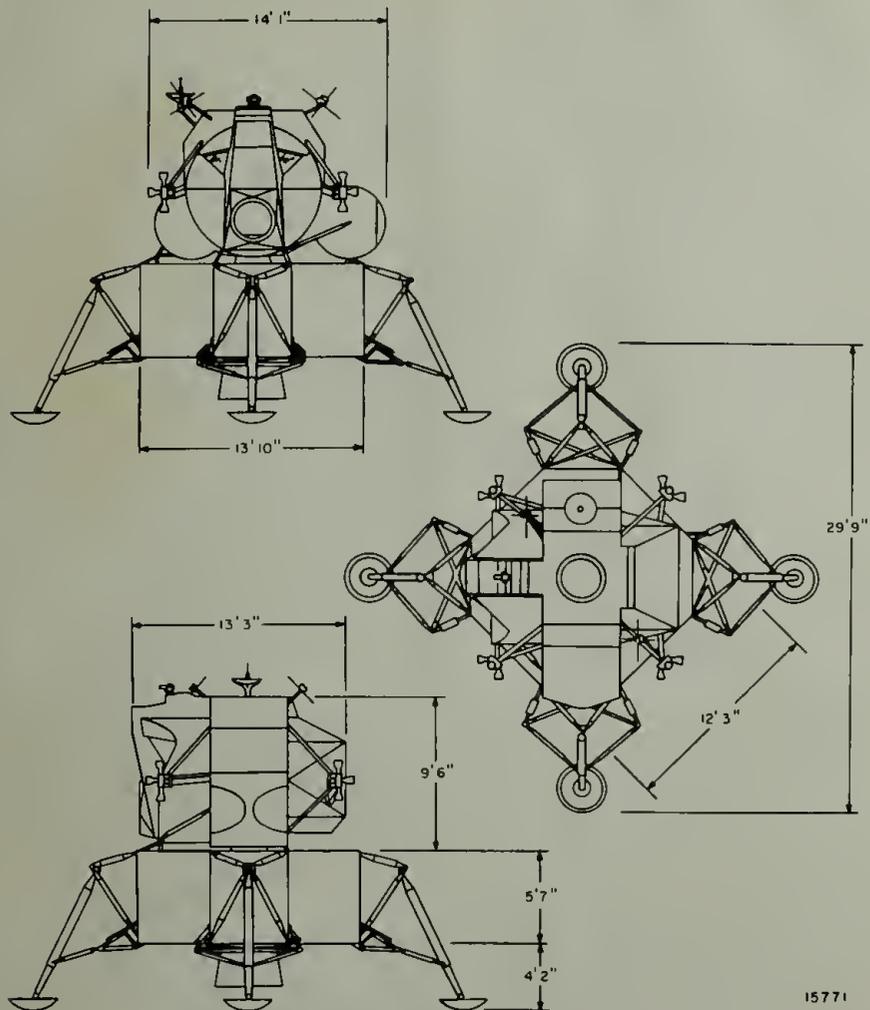


Figure 1-4. LEM External Dimensions

LEM PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

The propellant tankage sections are located on either side of the midsection outside the pressurized area. The tankage sections contain the ascent engine fuel and oxidizer tanks; RCS fuel, oxidizer, and helium tanks; and ECS water tanks. The ratio by weight of oxidizer to fuel is 1.6 to 1; therefore, to maintain the lateral center of gravity on the vehicle X axis, the ascent engine propellant tanks are offset to one side.

Two triangular windows in the front face of the crew compartment provide visibility. Each window has approximately 1.6 square feet of viewing area and are canted down and to the side to increase visibility. Each window consists of two panes.

1-3.2 DESCENT STAGE. The descent stage, constructed mainly of aluminum alloy, has equipment necessary to land on the lunar surface. It is also a platform for the launching of the ascent stage after completion of the lunar exploration. The descent engine is the center of the stage surrounded by its four main propellant tanks. In addition to the descent engine and its related components, the descent stage houses the descent control instrumentation; scientific equipment; EPS batteries; and tanks for water used by the ECS. Landing gear and the LR antenna are attached to the descent stage.

1-4 LEM SYSTEMS

Functionally, there are seven LEM systems. Four of these systems control the LEM flight. The PGNCS or the stabilization and control system (SCS) receives inputs from the crew and electrical inputs from the inertial sensors to generate commands that result in rotation and translation maneuvers. The RCS or propulsion system provides external forces and mechanical couples to maneuver the LEM under the control of the PGNCS or the SCS. The crew obtains information from the LGC (part of the PGNCS), by communications (Manned Space Flight Network), or displays that indicate the necessity to initiate one or more of the basic LEM motions. The three remaining LEM systems are indirectly related to LEM control. They provide the power (EPS), environmental control (ECS), and the communications [communications and instrumentation system (CIS)].

1-4.1 PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM. The PGNCS provides the measuring and data processing capabilities and control functions necessary to accomplish the LEM mission. The PGNCS utilizes inertial components for guidance, an optical device for navigation, and a digital computer for data processing and issuance of flight control signals.

The inertial guidance portion of the PGNCS, the IMU, employs accelerometers mounted on a gyroscopically stabilized gimbal-mounted platform. The IMU senses acceleration and attitude changes instantaneously and provides signals to a digital computer, the LGC, for the generation of attitude control and thrust commands.

For navigation, the PGNCS utilizes an optical tracking device to take star sightings and obtain measurements. These sightings are used by the LGC to establish proper alignment of the stable platform. The LGC contains a catalog of celestial

bodies and is programmed to calculate alignment commands using the information obtained from the optical sightings. In addition to functioning as a data processing unit, the LGC, through its flight programs, performs the function of a digital autopilot in controlling the LEM.

1-4.2 STABILIZATION AND CONTROL SYSTEM. The SCS consists of two major sections: the control electronics section (CES) and the abort guidance section (AGS). The CES processes flight control signals during all mission phases. The AGS provides the CES automatic steering commands, derived from explicit guidance equations, in the event of mission abort due to a PGNCS malfunction.

The CES consists of an attitude and translation control assembly (ATCA), a descent engine control assembly (DECA), rate gyro assembly (RGA), two translation controller assemblies (TCA), and two attitude controller assemblies (ACA). The CES processes and routes signals to fire any combination of the 16 thrusters in the RCS to control LEM attitude and translation. The attitude and translational control inputs originate from any of three sources: the PGNCS during normal automatic operation, the ACA and TCA during manual operations, or the AGS during an abort.

The CES converts the applicable input commands into pulsed or constant level signals and routes them to the RCS to fire the appropriate thrusters. Rate signals from the CES are displayed on the flight director attitude indicator (FDAI).

The CES also processes "ON-OFF" commands for the ascent and descent engines, and routes automatic and manual throttle commands to the descent engine. Trim control of the descent engine insures that the thrust vector operates through the vehicle center of gravity.

The AGS provides abort capability from any point in powered descent or powered ascent and increases crew safety by acting as a backup system to the PGNCS. The AGS has three main assemblies: abort sensor assembly, abort electronics assembly, and data entry and display assembly.

The abort sensor assembly utilizes a strap-down technique employing three single-degree-of-freedom integrating rate gyros and three accelerometers. This backup guidance provides vehicle attitude, angular velocity, and translational acceleration indications. The outputs of the abort sensor assembly go to the abort electronics assembly, a 4,096 word capacity general purpose computer. Computations are performed using the inputs from the abort sensor assembly. When the AGS is in control of the LEM, the results are displayed and control signals are issued to the vehicle's reaction control and propulsion systems.

The abort sensor assembly measures the accelerometer triad rotation from, and resolves the acceleration into, a fixed reference frame. This reference frame is provided by an initial alignment of the AGS with the PGNCS. Initial alignment is required for attitude, velocity, time, and position. Velocity and position vectors are manually entered into the computer by a data entry device available to the astronaut.

Attitude alignment is accomplished by transferring PGNCS IMU gimbal angles to the computer. The abort electronics assembly receives this data from the coupling data unit (CDU) in the same manner and at the same time as the LGC (i.e. incremental angles accumulated from a zero reference after "CDU ZERO").

1-4.3 PROPULSION SYSTEM. The LEM utilizes separate, complete, and independent descent and ascent propulsion systems, which consist basically of a liquid propellant rocket engine and its propellant storage, pressurization, and feed components.

The descent propulsion system is in the LEM descent stage and utilizes a throttle-controlled, gimballed engine. The engine injects the LEM into the descent transfer orbit and is used during powered descent and landing to control the rate of descent. The descent engine, developing 10,500 pounds maximum thrust in a vacuum at full throttle and 1,050 pounds minimum thrust, can be gimballed 6 degrees in any direction. The PGNCS issues the "ON-OFF" commands for the descent engine and also provides signals controlling thrust magnitude and gimbal trim position.

The propellant used in both propulsion systems is a 50-50 fuel mixture of hydrazine and unsymmetrical dimethylhydrazine using nitrogen tetroxide as the oxidizer and helium as the tank pressurant.

The ascent propulsion system utilizes a fixed, constant-thrust engine installed along the centerline of the ascent stage midsection and includes the associated propellant feed tanks and pressurization components. The engine develops 3,500 pounds thrust in a vacuum, sufficient to launch the ascent stage from the lunar surface and place it in orbit. The PGNCS issues the "ON-OFF" commands for the ascent engine.

1-4.4 REACTION CONTROL SYSTEM. The RCS provides rocket thrust impulses that stabilize the LEM during descent and ascent and control the LEM attitude and translation about or along all axes. The RCS has 16 thrust chambers supplied by two separate and independent propellant feed and pressurization sections. The thrust chambers are mounted in clusters of four on outriggers equally spaced around the LEM ascent stage. In each cluster, two thrust chambers are mounted on a vertical axis, facing in opposite directions; the other two are spaced 90 degrees apart, parallel to the LEM's Y and Z axes. The RCS utilizes the same fuel as the ascent engine. In the event of RCS fuel depletion, the remaining ascent fuel can be used for the RCS. The RCS can be operated in any of three modes: manual, automatic, or semi-automatic. The PGNCS supplies "ON-OFF" signals through the SCS to the valves on the desired thrust chambers during the automatic or semi-automatic mode. The automatic mode is normally used to provide attitude control during all mission phases except when manual control is required. It is possible to select manual control in one or two axes and retain automatic control in the other axis during all mission phases. The semiautomatic mode combines automatic attitude hold control with manual control. The LEM attitude is changeable about each axis using the astronaut's attitude controller. This mode is used primarily to control the LEM during the rendezvous and docking phase of the mission. In the manual mode, all control commands originate from the attitude controller, including manual control of the thrust duration.

All automatic translational commands originate in the PGNCS and are routed to the RCS similar to the attitude control signals.

1-4.5 ELECTRICAL POWER SYSTEM. The EPS provides 28 vdc and 115 vac, 400 cps power to the PGNCS. This power originates from six batteries, four in the descent stage, and two in the ascent stage. The batteries, the silver-zinc type, are rated at 80 watts per hour per pound of weight. The 115 vac, 400 cps power is obtained by routing the 28 vdc through an inverter.

1-4.6 ENVIRONMENTAL CONTROL SYSTEM. The ECS sustains life in space by providing breathable atmosphere, acceptable temperatures, food and water, and waste disposal. In addition, the ECS circulates an ethylene glycol-water coolant about the temperature sensitive electronic equipment in the PGNCS and other LEM systems to provide thermal stability. The IMU has coolant circulated through its case while the power and servo assembly (PSA), pulse torque assembly (PTA), signal conditioner, LGC and CDU are mounted on coldplates through which the coolant is circulated to provide temperature control.

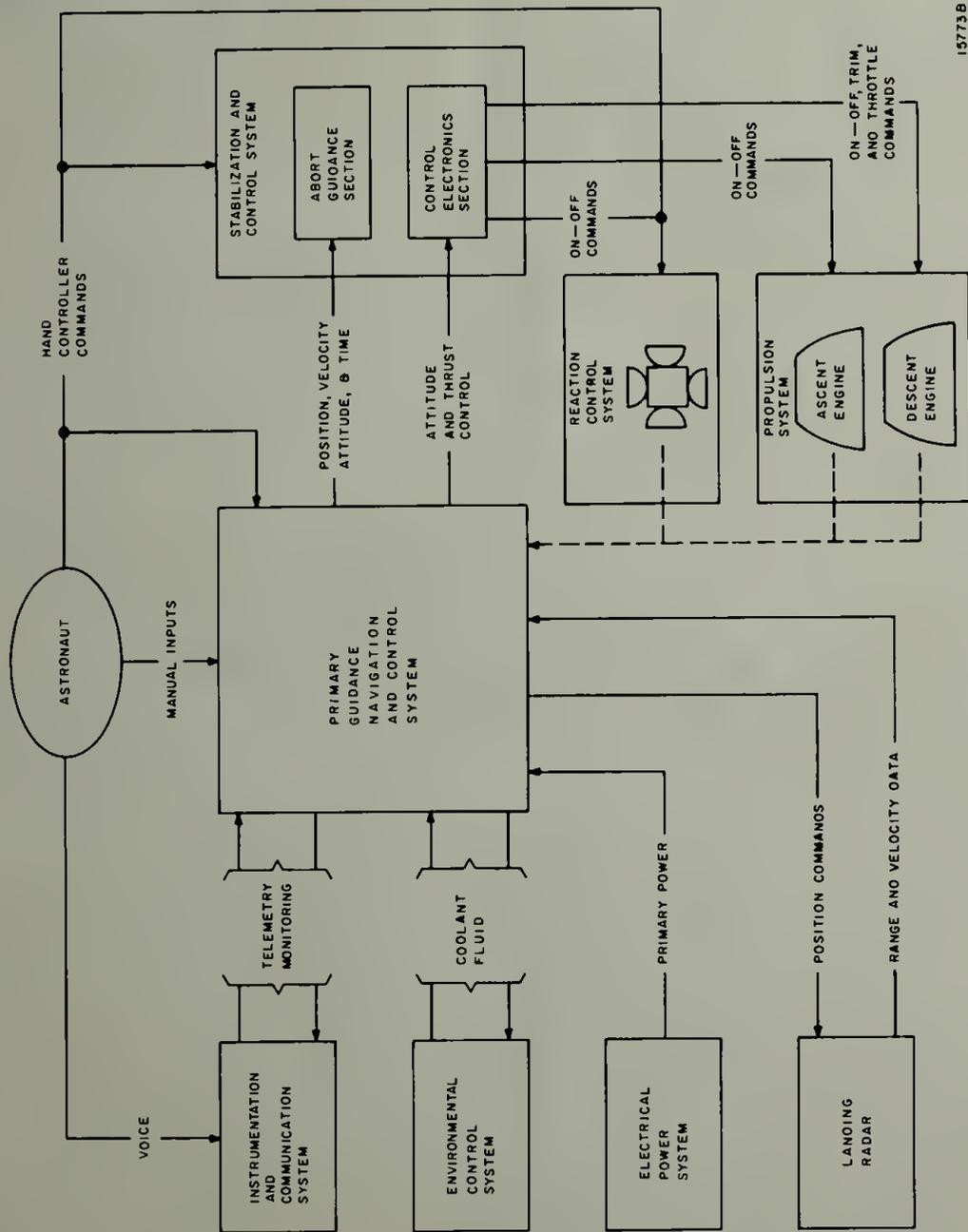
1-4.7 COMMUNICATIONS AND INSTRUMENTATION SYSTEM. The CIS links the lunar astronauts, the orbiting CSM, and earth monitoring stations.

The communications portion contains two radio frequency (RF) sections, one operating in the VHF range and the other in the UHF range; a television section; and a signal processing section. In addition to two-way voice communication, the RF section receives and transmits tracking and range information, biomedical information, and emergency code keying in the event of voice transmission failure. The television section is used by the extravehicular astronaut to televise the lunar surface within an eighty foot radius of the grounded LEM. In the signal processing section, critical signals of the PGNCS are conditioned and supplied to pulse code modulated (PCM) telemetry equipment for transmission to earth. Telemetry data can be stored when direct communication with the earth is not possible.

The instrumentation portion provides the astronauts and ground facilities with LEM performance data during the mission by sensing physical status data, monitoring the various systems, and performing inflight and lunar surface checkout. This system also contains the scientific instruments which are used by the astronauts during their lunar stay.

1-5 PGNCS INTERFACE

PGNCS operation during the LEM mission requires the interface of the PGNCS with the other LEM systems, the displays and controls on the crew display and control panels, the landing radar, and the astronauts. The functional interface of the PGNCS is shown in figure 1-5.



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Figure 1-5. LEM PGNCs Functional Interface, Block Diagram

1-5.1 SYSTEMS. Four LEM systems (SCS, ECS, CIS, and EPS) have direct interface with the PGNCSS and two systems (propulsion system and RCS) have indirect interface with the PGNCSS. The indirect interface of the propulsion system and the RCS occurs through the SCS. These two systems may thus be controlled by the PGNCSS or by the backup control provided by the AGS of the SCS. Descriptions and sources of the SCS interface signals are provided in table 1-I. Descriptions of the interfaces with the other systems are provided in paragraph 1-4.

1-5.2 DISPLAYS AND CONTROLS. Several displays and controls located on the crew control panels, LGC display and keyboard (DSKY) panel, and the SCS control panel interface with the PGNCSS. Two sets of hand controllers are provided for manual control of the LEM and interface with the PGNCSS. Descriptions of the displays and controls are in table 1-II.

1-5.3 LANDING RADAR. The landing radar (LR) provides data to the LGC from which LEM velocity (in antenna coordinates) and LEM altitude may be determined. The data is also available for visual display, independent of the PGNCSS, except that the velocity is in spacecraft coordinates.

The landing radar which operates in the X-band, consists of an antenna assembly, a solid-state electronics assembly, and a control panel. Velocity data is acquired from a three beam continuous wave Doppler radar. Altitude data is provided by a one beam FM continuous wave radar altimeter. The antenna assembly accommodates the requirements of both the Doppler and the altimeter beams.

Landing radar and PGNCSS interface include digital data transfer, scaling, velocity and range sensing, status, and antenna positioning. Descriptions and sources of the interface signals are in table 1-III.

Table 1-I. SCS Interface Signals

Signal Name	Source	Description
Manual translation commands ($\pm x$, $\pm y$, $\pm z$)	SCS	Signals from translation controller which fire RCS jets by LGC control.
Attitude control out of detent	SCS	Signal from attitude controller indicating that it is not in neutral position.
Rate of descent (\pm)	SCS	Discretes commanding an increase or decrease in rate of descent.
Gimbal off (pitch, roll)	SCS	Signal to LGC indicating that descent engine pitch or roll gimbal is off null.
Trim commands (\pm pitch, \pm roll)	LGC	Signals which control trim of descent engine.
Engine on-off	LGC	Signal to turn descent or ascent engine on or off.
Descent engine throttle command (decrease, increase)	LGC	Signal to increase or decrease thrust of descent engine.
RCS jets on-off	LGC	Signals (16) to turn RCS jets on or off.
Increments of IMU gimbal angles ($\pm \Delta \theta_{IG}$, $\pm \Delta \theta_{MG}$, $\pm \Delta \theta_{OG}$)	LGC	Supplies changes in IMU gimbal angles to AGS.
CDU zero (initial clear)	LGC	Sets alignment logic of AGS to zero.
800 cps $\pm 1\%$	PGNCS	Provides reference between PGNCS and SCS.

Table 1-II. Displays and Controls

Display or Control	Function
GUID CONT switch	Selects either primary guidance (PGNS) or abort guidance (AGS). Normally in the PGNS position.
MODE SEL selector	Three position switch used during landing phase to select one of three inputs to be displayed on AZ RT/ELEV RT-LAT VEL/FWD VEL indicator. Inputs are landing radar (LDG RADAR), PGNS and AGS.
RNG/ALT MON switch	Controls display of RANGE/RANGE RATE-ALT/ALT RATE indicator. Positions are RNG/RNG RT and ALT/ALT RT.
RATE/ERR MONITOR switch (2)	Selects one of two inputs for AZ RT/ELEV RT-LAT VEL/FWD VEL indicator and attitude needles of FDAI.
ATTITUDE MON switch (2)	Selects one of two inputs to FDAI total attitude display and attitude error needles during landing.
THR CONT switch	Selects either automatic (AUTO) or manual (MAN) control of descent engine throttle. Normally in AUTO position.
MAN THROT switch	Activates either commander's (CDR) or system engineer's (SE) translation controller for manual throttling of descent engine.
ABORT	Pushbutton to cause mission abort at any point between LEM/CSM separation and touchdown on lunar surface with descent stage still attached.
ABORT STAGE	Pushbutton to cause mission abort using ascent stage.
AZ RT/ELEV RT-LAT VEL/FWD VEL meter (2)	Provides visual displays of vehicle forward and lateral velocity during landing.

Table 1-II. Displays and Controls

Display or Control	Function
RANGE/RANGE RATE- ALT/ALT RATE meter	Provides visual displays of range, altitude, range rate, and altitude rate.
FDAI meter (2)	Provides three visual displays, total attitude, attitude error, and attitude change rate. PGNCS or AGS provides inputs for total attitude and attitude error. Attitude rate signals are provided by SCS rate gyros.
LGC and ISS warning indicators, PGNS caution indicator.	Controlled by instrumentation system which receives discretes from LGC when certain PGNCS troubles exist.
MODE CONTROL selector	A three-position selector located on SCS control panel concerned with attitude control. Positions are OFF, ATT HOLD, and AUTO. In AUTO position, fully automatic attitude control is achieved through PGNCS or AGS control of RCS jets. ATT HOLD position allows crew to manually reposition LEM and have new position automatically maintained by LGC.
IMU CAGE switch	Switch located on DSKY mounting panel to drive IMU gimbal angles to zero.
Attitude controller (2)	Three-axis, pistol-grip, right-hand device for manual attitude control of LEM. Outputs from controller are processed by PGNCS or may be routed directly to RCS.
Translation controller (2)	Three-axis, T-handle, left-hand device for manual translation control of LEM. Using switch located next to T-handle, controller can operate RCS jets or throttle the descent engine.

(Sheet 2 of 2)

Table 1-III. Description of Landing Radar Interface Signals

Signal Name	Source	Description
Antenna positioning command	DSKY and LGC	Changes antenna position.
Antenna position #1 (descent)	LR	Indicates to LGC that antenna is in position #1.
Antenna position #2 (hover)	LR	Indicates to LGC that antenna is in position #2.
Velocity data good	LR	Indicates to LGC that LR velocity trackers have locked on.
Range data good	LR	Indicates to LGC that LR range trackers have locked on.
Range low scale factor	LR	Indicates to LGC that a change in scale factor is necessary. Issued automatically at approximately 2,500 feet.
LR in "0" and LR in "1"	LR	Digital pulses sent to LGC which contain range and velocity data.
Readout command	LGC	Indicates that LGC is ready to receive LR data pulses.
Gate reset	LGC	3,200 cps continuous LGC output to reset LR transfer gates.
Range strobe	LGC	Timing pulses to enable LR transfer gates.
V _{xa} , V _{ya} , V _{za} strobe pulses	LGC	Timing pulses to enable LR transfer gates.

Chapter 2

SYSTEM AND SUBSYSTEM FUNCTIONAL ANALYSIS

2-1 SCOPE

This chapter provides functional descriptions of the PGNCSS and its subsystems. This chapter describes how the PGNCSS subsystems perform the PGNCSS operations.

2-2 PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM.

The PGNCSS is functionally divided into three major subsystems: inertial, optical, and computer. The PGNCSS performs three basic functions: inertial guidance, navigation, and autopilot stabilization and control. Within these functions the subsystems, or combination of subsystems, with assistance from the astronaut, perform the following operations:

- (1) Establish an inertial reference which is used for measurements and computations.
- (2) Aligns the inertial reference by optical measurements and, through interface, aligns the inertial reference with the CSM PGNCSS.
- (3) Calculates the position and velocity of the LEM by inertial navigation.
- (4) Accomplishes a LEM and CSM rendezvous by optical navigation and inertial guidance.
- (5) Generate attitude control and thrust commands to maintain the LEM on a satisfactory trajectory.
- (6) Control throttling of descent engine during lunar landing.
- (7) Display pertinent data related to guidance status.
- (8) Controls ascent engine burn time to obtain proper velocity for rendezvous orbit.

To perform its inertial guidance functions, the PGNCSS employs an IMU containing accelerometers mounted on a gyro stabilized, gimbal-mounted platform. The IMU, three channels of the CDU, the pulse torque assembly (PTA), and the PSA form the ISS of the PGNCSS.

To perform its navigation functions, the PGNCS employs the LEM optical rendezvous subsystem (LORS), which consists of an optical tracker located on the LEM and a luminous beacon located on the CSM. During the powered descent and landing phase, the PGNCS receives altitude and velocity data from the LR, which is used to update or check inertially derived data.

The LGC is a digital computer which serves as both the control element and the primary data processing element of the PGNCS. The LGC and the display and keyboard (DSKY) form the computer subsystem of the PGNCS.

Figure 2-1 illustrates the signalflow and interface between the three PGNCS subsystems.

2-3 LEM AND PGNCS AXES

Several sets of axes are associated with the LEM and PGNCS. Figure 2-2 illustrates these various orthogonal sets which are defined in the following paragraphs. Positive rotation about each axis is as defined by the right hand rule.

2-3.1 LEM SPACECRAFT AXES. The LEM spacecraft axes provide a reference for all other sets of axes and define the point about which attitude maneuvers are performed. The LEM spacecraft axes, designated X_{LEM} , Y_{LEM} , Z_{LEM} , are referred to as the yaw, pitch, and roll axes respectively. The X_{LEM} axis points through the upper docking hatch and the Z_{LEM} axis points through the forward hatch. The Y_{LEM} axis is perpendicular to the X_{LEM} and the Z_{LEM} axes and can be considered to be pointing out of the astronaut's right shoulder as he faces toward the forward portion of the LEM.

2-3.2 NAVIGATION BASE AXES. The navigation base provides a precise alignment of the IMU to the optical tracker and a means of attaching both units to the spacecraft. The navigation base is mounted to the LEM structure so that a coordinate reference system is formed by its mounting points. The Y_{NB} axis is defined by the centers of the two upper mounting points and is parallel to the Y_{LEM} axis. The X_{NB} axis is defined by a line through the center of the lower mounting point, perpendicular to the Y_{NB} axis and parallel to the X_{LEM} axis. The Z_{NB} axis is mutually perpendicular to the X_{NB} and Y_{NB} axes and is parallel to the Z_{LEM} axis.

2-3.3 INERTIAL AXES. The inertial axes provide references for measuring changes in velocity and attitude. At zero degree, the inertial axes are parallel to the navigation base axes.

2-3.3.1 Gimbal Axes. The gimbal axes (outer, middle, and inner) are the axes of the movable gimbals. The axes are defined by the intergimbal assemblies which provide each gimbal with rotational freedom. The attitude of the spacecraft with respect to the stable member is measured by the gimbal resolvers located in the intergimbal assemblies.

2-3.3.2 Stable Member Axes. The stable member axes (X_{SM} , Y_{SM} , Z_{SM}) provide a reference for aligning the inertial components and for defining the angular orientation of the inertial axes during flight.

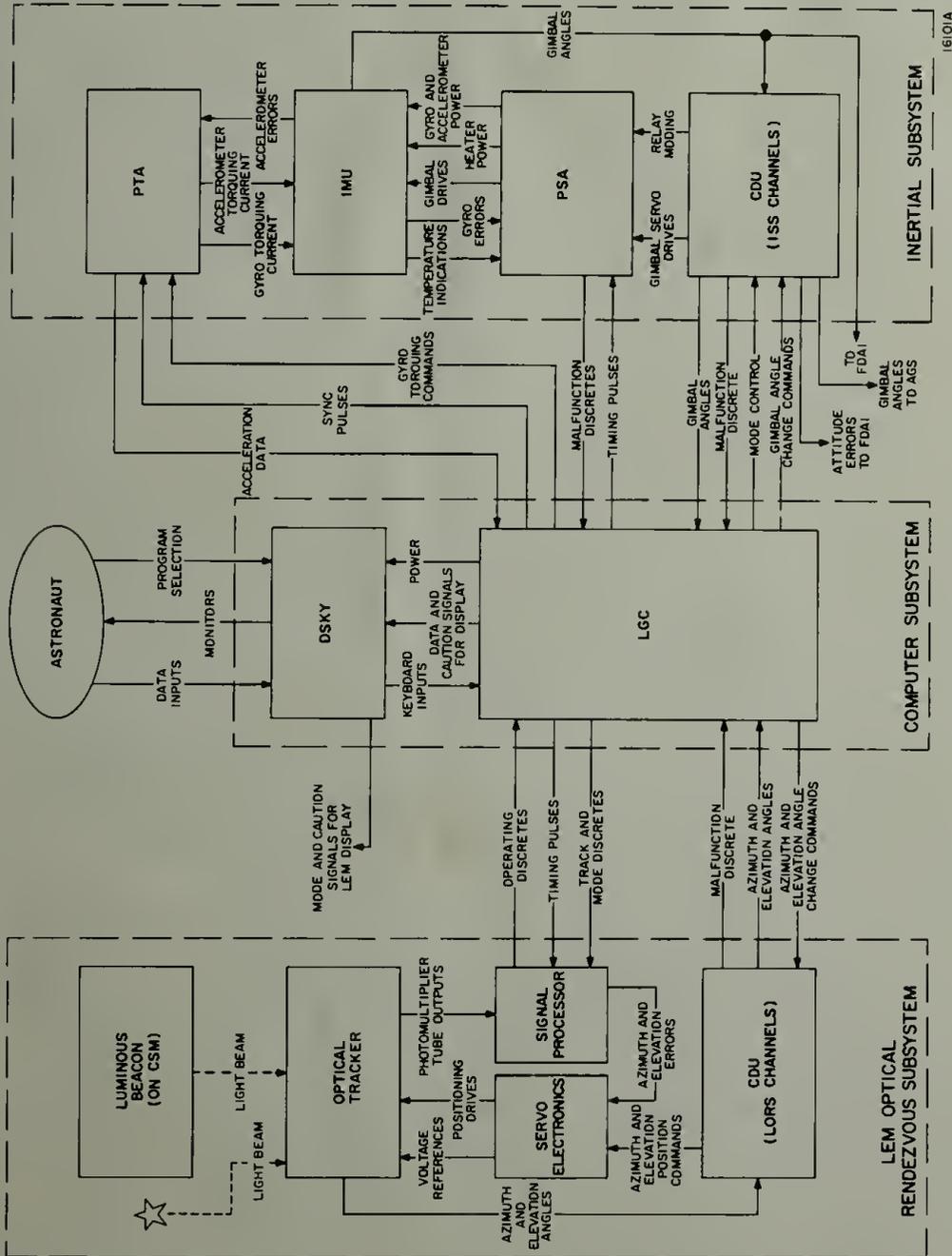


Figure 2-1. PGNCS Subsystems Interface, Block Diagram

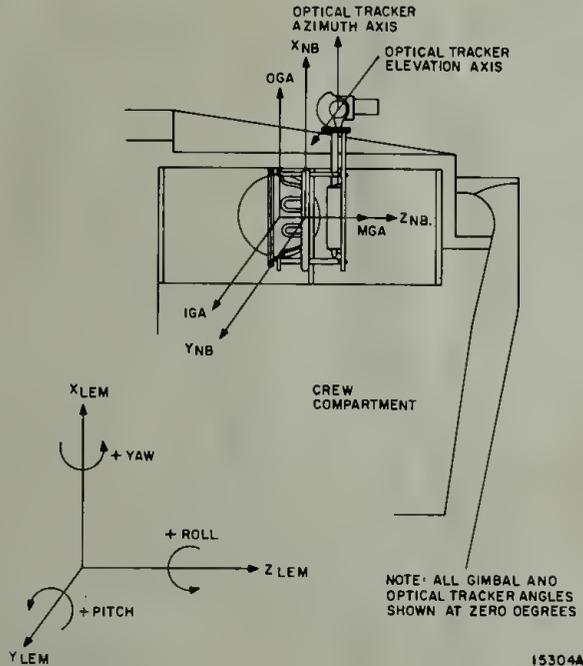


Figure 2-2. LEM and PGNCS Axes

2-3.3.3 Accelerometer Axes. The accelerometer axes (X_a , Y_a , Z_a) are the positive input axes of the accelerometers and are parallel to the stable member axes. Velocity changes are measured along the accelerometer input axes. This velocity data is used to determine spacecraft position and velocity.

2-3.3.4 Gyro Axes. The gyro axes (X_g , Y_g , Z_g) are the positive input axes of the stabilization gyros and are parallel to the stable member axes. If the attitude of the stable member is changed with respect to inertial space, the gyro senses the change about its input axis and provides an error signal to a servo loop which realigns the stable member to its original orientation.

2-4 INERTIAL SUBSYSTEM

The ISS performs three major functions. It measures changes in LEM attitude, assists in generating steering commands, and measures spacecraft velocity due to thrust. To accomplish these functions, the IMU provides an inertial reference consisting of a stable member with a three degree of freedom gimbal system and stabilized by

three rate integrating gyros. Each time the inertial subsystem is energized, the stable member must be aligned with respect to a predetermined reference. During flight and prior to launch from the lunar surface, this alignment is accomplished by sighting the optical instrument on celestial objects.

Once the ISS is energized and aligned, any rotational motion of the LEM will be about the stable member, which remains fixed in space. Resolvers mounted on the gimbal axes act as angular sensing devices and measure the attitude of the LEM with respect to the stable member. These angular measurements are displayed by the FDAI and angular changes are sent to the LGC via the CDU.

The desired LEM attitude is calculated in the LGC and compared with the actual gimbal angles. Any difference between the actual and calculated angles results in the generation of attitude error signals by the ISS channels of the CDU which are sent to the FDAI for display.

Vehicle acceleration is sensed by three pendulous accelerometers mounted on the stable member with their input axes orthogonal. The signals from the accelerometers are supplied to the LGC which calculates the total vehicle velocity.

The modes of operation of the inertial subsystem can be initiated automatically by the LGC or by the astronaut selecting computer programs through the DSKY. The status or mode of operation is displayed on the DSKY.

For purposes of explanation and description, the ISS is divided into functional blocks as shown in figure 2-3 and described in the following paragraphs.

2-4.1 STABILIZATION LOOP. The three stabilization loops (figure 2-4) maintain the stable member in a specific spatial orientation so that three mutually perpendicular 16 pulsed integrating pendulum (16 PIP) accelerometers can measure the proper components of LEM acceleration with respect to the coordinate system established by the stable member orientation. An input to the stabilization loops is created by any change in LEM attitude with respect to the spatial orientation of the stable member. With near zero gimbal angles, the inertia of the stable member tends to maintain the stable member in a fixed spatial orientation. Because of gimbal friction and unbalances, motion of the LEM structure relative to the stable member will produce a torque on the stable member which will tend to change its orientation. This change is sensed by the stabilization gyros. When the gyros sense an input, they issue error signals which are amplified, resolved, if necessary, into appropriate components, and applied to the gimbal torque motors. The gimbal torque motors then drive the gimbals until the stable member regains its original spatial orientation.

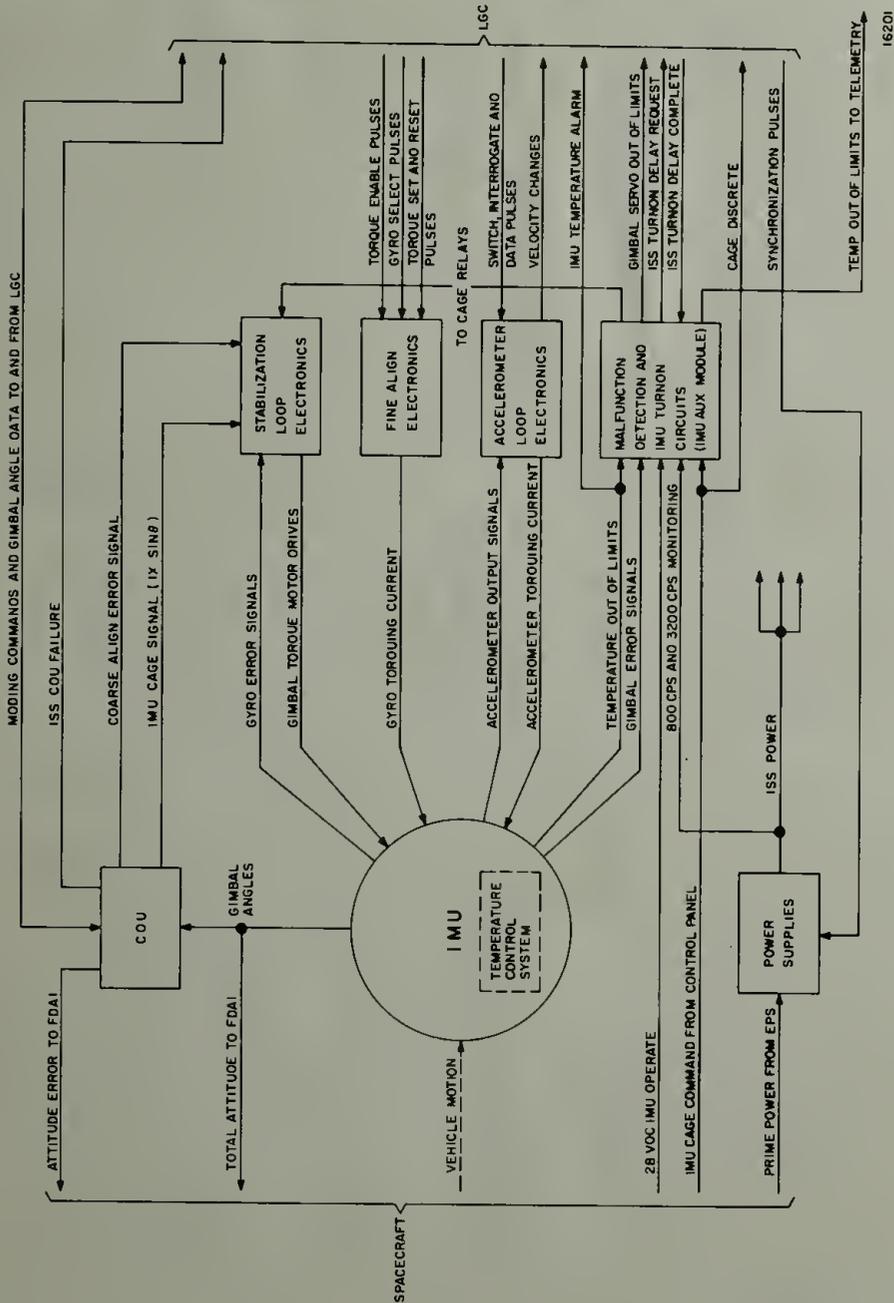
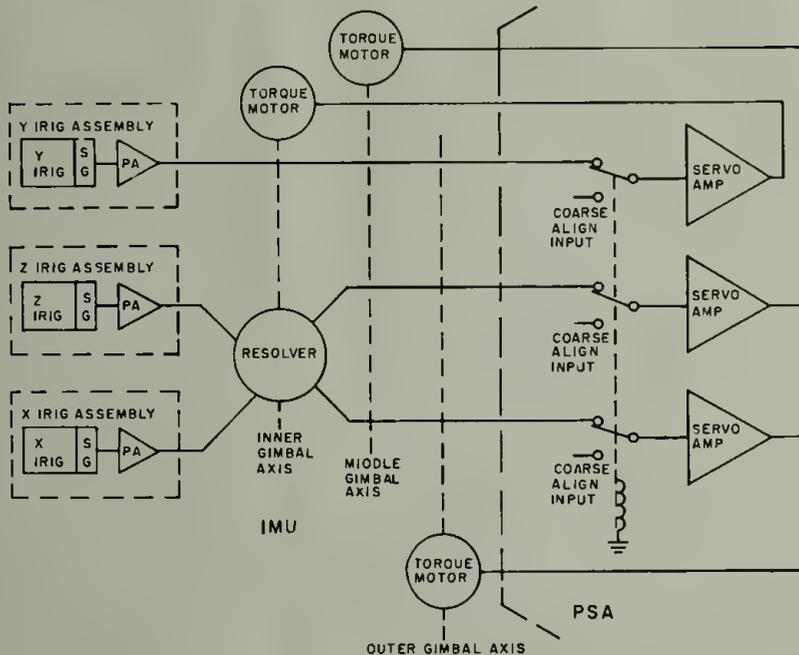


Figure 2-3. ISS, Block Diagram



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Figure 2-4. Stabilization Loop, Block Diagram

The stabilization loop consists of three pre-aligned Apollo II inertial reference integrating gyro (Apollo II IRIG) assemblies, a gyro error resolver, three gimbal servo amplifiers, three gimbal torque motors, three gimbals, and circuitry associated with these components. The inner gimbal is the stable member upon which the three stabilization gyros are mounted. The gyros are mounted with their input axes oriented in an orthogonal configuration. Movement of any gimbal tends to result in a movement of the stable member and rotation about the input axes of one or more of the stabilization gyros.

The stabilization loop contains three parallel channels. Each channel starts with a stabilization gyro (X, Y, or Z) and terminates in a gimbal torque motor. The torque motor drives the gimbals resulting in a movement of the stable member and a movement of the stabilization gyros. When a movement of the IMU support gimbal attempts to displace the stable member from its erected position, one or more of the stabilization gyros senses the movement and issues error signals. The phase and magnitude of the 3,200 cps gyro error signal represents the direction and amount of rotation experienced by the gyro about its input axis. The error signal is fed from the gyro signal

generator ducosyn to the associated IIRIG preamplifier, which is a part of the prealigned Apollo II IIRIG assembly. Amplification of the error signal is required to achieve a high signal-to-noise ratio through the gimbal slip rings.

The amplified gyro error signals also represent motion of the stable member about its axis since the stable member axes (X_{SM} , Y_{SM} , Z_{SM}) and the gyro axes (X_g , Y_g , Z_g) are parallel to one another.* If the middle and outer gimbal axes remain parallel with the stable member axes, then movement of the outer gimbal (a yaw movement of the LEM) is sensed by only the X gyro and movement of the middle gimbal (roll movement of the LEM) is sensed by only the Z gyro. Movement of the stable member about the inner gimbal axis (Y_{SM}), however, changes the relationship of the X and Z gyro input axes to the outer and middle gimbal axes. As a result, a movement of the middle or the outer gimbal is sensed by both X and Z gyros. The input required by the gimbal servo amplifiers to drive the gimbals and move the stable member back to its original position must be composed of components of both the X and Z gyros. The required gimbal error signals are developed by the gyro error resolver. The gyro error signals, $E(X_g)$ and $E(Z_g)$, are applied to the stator windings of the gyro error resolver. The rotor windings are connected to the inputs of the outer and middle gimbal servo amplifiers. Movement of the stable member about the inner gimbal axis (pitch movement of the LEM) changes the position of the resolver rotor relative to the resolver stator. This change corresponds electromagnetically to the change in the relationship of the stable member axes to the outer and middle gimbal axes. The outputs taken from the rotor are the required middle and outer gimbal error signals (E_{mg} and E_{og}). Since the inner gimbal torque motor axis and the Y axis of the stable member are the same axis, the Y gyro error signal, $E(Y_g)$, is equal to the inner gimbal error signal, (E_{ig}), and is fed directly to the inner gimbal servo amplifier.

The three identical gimbal servo amplifier modules are located in the PSA and contain a phase sensitive demodulator, a filter, and a dc operational power amplifier. The phase sensitive demodulator converts either the 3,200 cps gimbal error or 800 cps coarse align error, zero or pi phase, signals into a representative positive or negative dc signal. The dc signal is filtered and applied to a dc operational amplifier with current feedback. The compensation network in the feedback circuit of the amplifier controls the response characteristics of the entire stabilization loop. The output of the dc amplifier has an operating range between +28 vdc and -28 vdc and drives the respective gimbal torque motor directly in either angular direction.

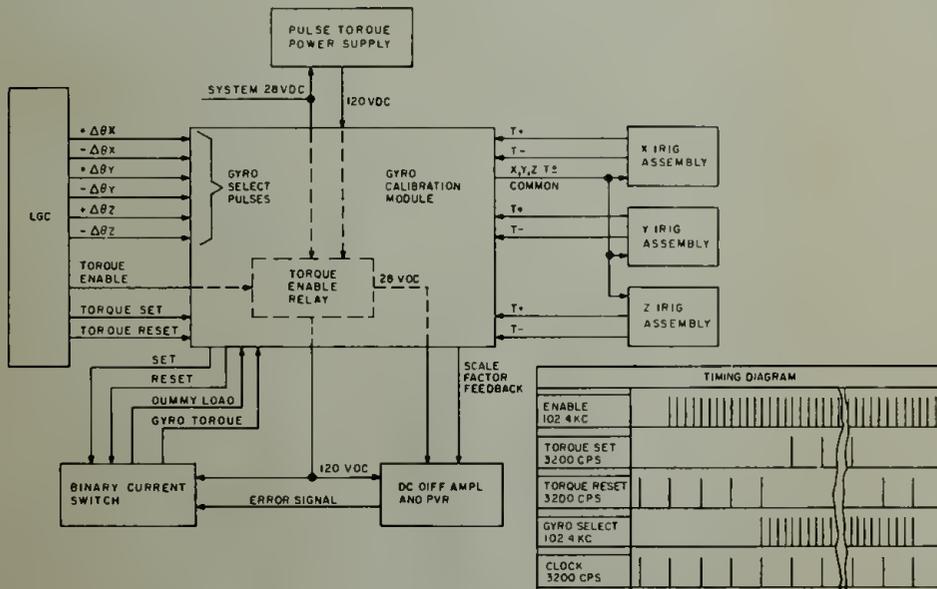
The gain required for each stabilization loop differs. This difference compensates for the differences in gimbal inertia. The proper gain is selected by the connections to the gimbal servo amplifier module. A single torque motor is mounted on each gimbal at the positive end of the gimbal axis. The torque motors drive the gimbals to complete the stabilization loop.

* The Z gyro has its positive input axis aligned to the $-Z_{SM}$ axis but this is compensated for by reversing the polarity of the 3,200 cps excitation to the primary winding of the Z gyro signal generator ducosyn which causes the Z gyro error signal to be representative of the direction and amount of motion about the Z_{SM} axis.

The orientation of the stable member can be changed in either the coarse align, fine align, or IMU cage modes. Signals to reposition the gimbals are injected into the gimbal servo amplifiers from the CDU during the coarse align and IMU cage modes and into the stabilization gyros from the fine align electronics during the fine align mode. During the IMU cage mode and the coarse align mode, the reference signal for the demodulator in the gimbal servo amplifier is externally switched from 3,200 cps to 800 cps.

2-4.2 FINE ALIGN ELECTRONICS. The fine align electronics (figure 2-5) provides torquing current to the stabilization gyros to change the orientation of the IMU gimbals during the fine align mode. The operation of the fine align electronics is controlled by the LGC.

The components of the fine align electronics are common to the three stabilization gyros. The fine align electronics provides torquing signals to the stabilization gyros one at a time on a time shared basis. The fine align electronics consists of a gyro calibration module, a binary current switch module, and a dc differential amplifier and precision voltage reference module, all located in the PTA.

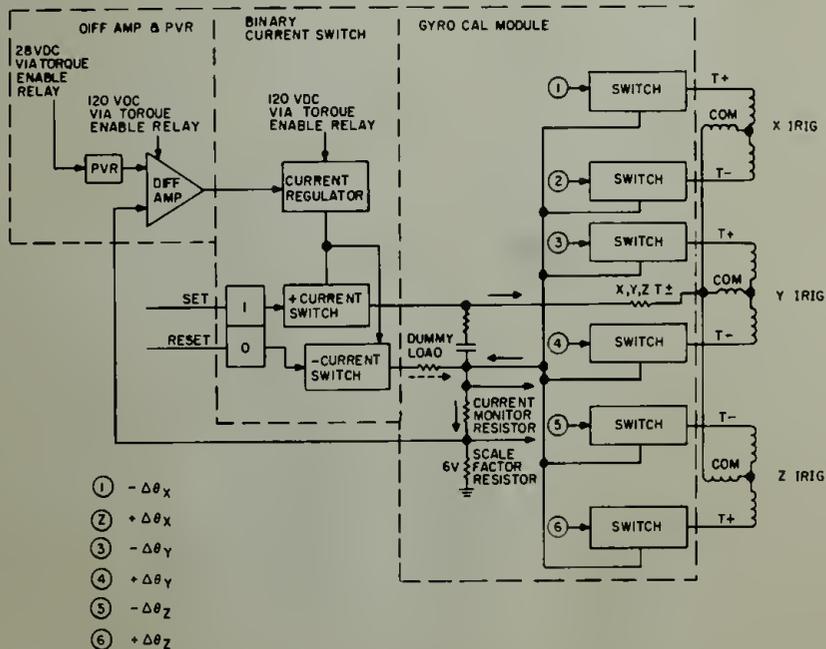


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Figure 2-5. Fine Align Electronics - Computer Inputs

The fine align electronics is enabled and controlled by LGC inputs to the gyro calibration module. The LGC inputs consist of torque enable pulses, gyro select pulses, a torque set command, and a torque reset command. The fine align electronics is enabled by the torque enable pulses. The torque enable pulses are a train of pulses three microseconds in width and occurring at 102.4 kpps. The torque enable pulses are applied through a relay driver to energize the torque enable relay in the calibration module. When the torque enable relay is energized, system 28 vdc is applied to the precision voltage reference (PVR) and regulated 120 vdc from the pulse torque power supply is applied to the dc differential amplifier and the binary current switch. The torque enable pulse train is received 20 milliseconds prior to any gyro set command.

The gyro to be torqued and the direction it is to be torqued is selected by the LGC by sending gyro select pulses to one of the six $+\Delta\theta$ or $-\Delta\theta$ inputs. (See figure 2-6.) The gyro select pulse consists of a train of pulses three microseconds in width and occurring at 102.4 kpps. The pulse train activates a transistor switch network which controls current through the T+ or T- coils of the torque generator ducosyn in the gyro selected. The gyro select pulse train is received 312.5 microseconds (one LGC clock time at 3,200 pps) prior to any torque set command.



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Figure 2-6. Fine Align Electronics - Gyro Selection

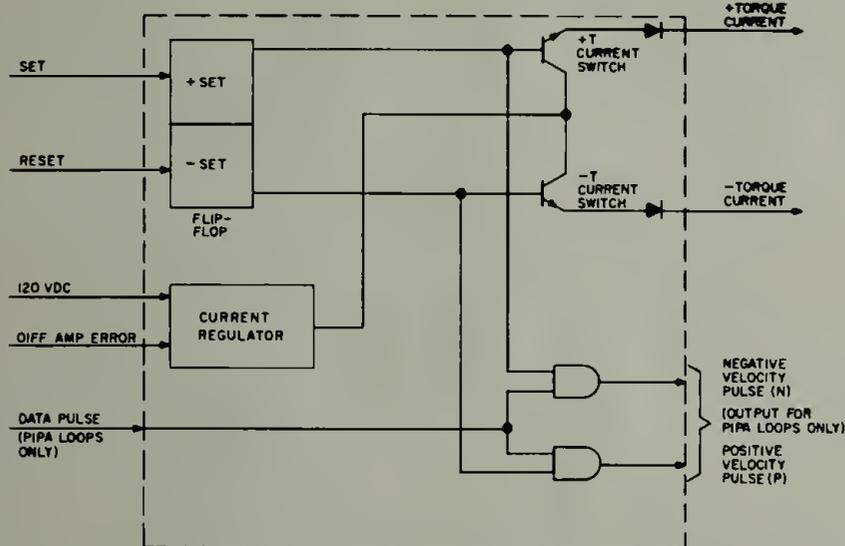
The torque set and reset commands are 3,200 pps pulse trains containing pulses that are three microseconds in width. A 3,200 pps pulse train will be present on the torque set line when any gyro is to be torqued. A 3,200 pps pulse train is present on the torque reset line at all other times. This ensures that the binary current switch is in the reset condition prior to receipt of a torque enable command from the LGC. When the gyro has been torqued the proper amount, a torque reset command is issued which causes the torque current to be cut off. The gyro select pulse train will be removed 312.5 microseconds after the torque reset command has been issued. The torque set and torque reset pulses are fed through a 1:2 step-up transformer in the calibration module to the set and reset inputs of the binary current switch.

The torque current from the binary current switch is applied through a tuned resistive-capacitive compensation network in the calibration module to make the torque generator ducosyn windings appear as a pure resistive load to the binary current switch. The torque current to the gyros is via the T±(common) line. Current will flow only through the selected torque generator coils, the current monitor resistor, and the scale factor resistor. The voltage drop developed across the scale factor resistor is used as a feedback to the differential amplifier to regulate the torquing current. The voltage drop across the current monitor resistor is applied to PTA test points for external monitoring of gyro torque current.

When no gyro is being torqued, the binary current switch provides current flow through a dummy load resistor and through the current monitor and scale factor resistors. In this manner, the binary current switch maintains a continuous flow of torque current. The dummy load resistor simulates the impedance of the torque generator coil and a compensation network.

The torque set and torque reset pulses trigger a flip-flop (bi-stable multivibrator) in the binary current switch (figure 2-7). If the flip-flop is in the +set condition, the +set condition will remain until a reset command resets the flip-flop. The outputs of the flip-flop control two transistor switches. If the flip-flop is in the +set condition, the +set output is present at the base of the +torque current switch, causing the switch to turn on. The +torque current switch closes the path from the 120 volt supply through the current regulator to the proper T+ or T- winding of the selected gyro via the calibration module. If the flip-flop is in the -set condition, the -torque current switch will turn on and close the current path through the dummy load resistor.

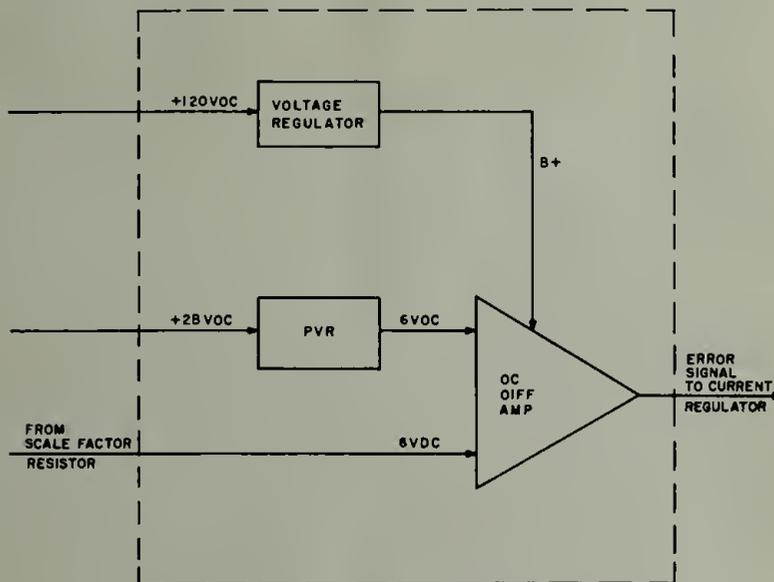
The binary current switch used in the fine align electronics is identical to the one used in the accelerometer loops. The portion of the binary current switch used only for the accelerometer loops is disabled in the fine align electronics application. In the accelerometer loop application, current to the accelerometer T+ torque generator coil is provided by the +torque current switch and current to the T- torque generator coil is provided by the -torque current switch. Therefore, the +torque and -torque designations of the switches have significance. In the fine align electronics application the switch designations have no significance since current to both the T+ and T- coils of the gyro torque generators is provided by the +torque current switch while the -torque current switch provides only the dummy load current.



15188 B

Figure 2-7. Binary Current Switch

The dc differential amplifier and PVR module (figure 2-8) maintains the current through the windings of the torque generator ducosyn at 84 milliamperes. The PVR is supplied with regulated 28 vdc and, through the use of zener diode circuits, develops an accurate 6 vdc for use as a reference voltage. The scale factor resistor in the calibration module also has 6 volts developed across it when 84 milliamperes of current flows through it. A comparison is made by the dc differential amplifier of the PVR 6 volts and the scale factor resistor 6 volts. Any deviation from the nominal 84 milliamperes of torquing current will increase or decrease the voltage developed across the scale factor resistor and cause an output error signal from the dc differential amplifier. This error signal controls the current regulator in the binary current switch. The current regulator, which is in series with the torque generator coils of the selected gyro and the 120 vdc source, will maintain the torquing current at 84 milliamperes.



15178A

Figure 2-8. DC Differential Amplifier and Precision Voltage Reference

The current flow through the windings of the torque generator ducosyn causes the gyro float to rotate about the gyro's output axis. A $+\Delta\theta$ gyro select command from the LGC will allow torque current to flow through a T- torque generator coil which results in a positive rotation of the gyro float about the output axis. A $-\Delta\theta$ gyro select command produces a negative float rotation.* Float rotation results in an error output from the signal generator ducosyn. The error signal is applied to the stabilization loop to reposition the gimbals and the stable member. The change in gimbal angles is transmitted by the CDU read counters to the LGC.

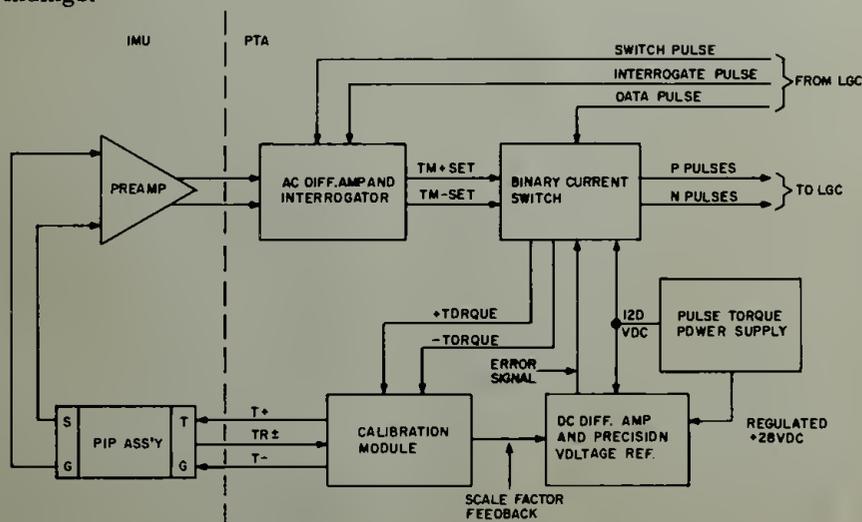
* The positive input axis of the Z gyro is aligned to the $-Z_{SM}$ axis but this is compensated for by reversing the T+ and T- connections to the Z gyro torque generator ducosyn. A $+\Delta\theta Z$ gyro select command from LGC will cause a negative float rotation but since the polarity of the Z gyro signal generator is also reversed the gyro error signal will appear to represent a positive float rotation. The stabilization loops will then drive the gimbals in the desired direction.

2-4.3 ACCELEROMETER LOOP. The three accelerometer loops measure the acceleration of the stable member along three mutually perpendicular axes and integrate this data to determine velocity. The velocity is used by the LGC to determine the LEM velocity vector. Figure 2-9 is a functional diagram of an accelerometer loop.

The three accelerometer loops contain three prealigned 16 PIP assemblies, three PIP preamplifiers, three ac differential amplifier and interrogator modules, three binary current switches, three calibration modules, three dc differential amplifier and precision voltage reference modules, a pulse torque isolation transformer, and associated electronics.

The three mutually perpendicular PIP's are acceleration sensitive devices. When fixed in its associated accelerometer loop, the PIP becomes an integrating accelerometer. The PIP is basically a pendulum-type device consisting of a cylinder with a pendulous mass unbalance (pendulous float) pivoted with respect to a case. The axis of the pivots defines the PIP output axis. A signal generator is located at the positive end of the output axis to provide electrical output signals indicative of the rotational position of the float. A torque generator located at the other end of the float acts as a transducer to convert electrical signals into mechanical torque about the float shaft. The accelerometer loop using a PIP is mechanized to operate in a binary (two state) mode.

In the binary mode, the PIP pendulum is continually kept in an oscillatory motion. Thus the two states: positive rotation or negative rotation. The rotation is accomplished by continuously routing torquing current through the torque generator plus or minus windings.



15177A

Figure 2-9. Accelerometer Loop

The torque generator has two windings, one to produce torque (rotation) in a positive direction, the other to produce torque (rotation) in a negative direction. Only one winding will have current in it at any one time. The torque winding selection is accomplished by the setting of a flip-flop in the binary current switch (figure 2-7). When the loop is first energized, the interrogator sets the flip-flop to route the torquing current to one of the windings, which will rotate the float to null. As the float passes through null, the phase of the output signal of the signal generator changes, which causes the interrogator to issue pulses to reset the flip-flop in the binary current switch and thus route torquing current to the other torque winding. The float is then torqued in the opposite direction until the signal generator output again changes phase as the float passes through null which reinstates the cycle.

The output of the signal generator, after being amplified by the PIP preamplifier is interrogated 3200 times a second by the interrogate pulse. The binary current switch flip-flop can be reset only when the interrogate pulse is present and the signal generator output is of the proper phase.

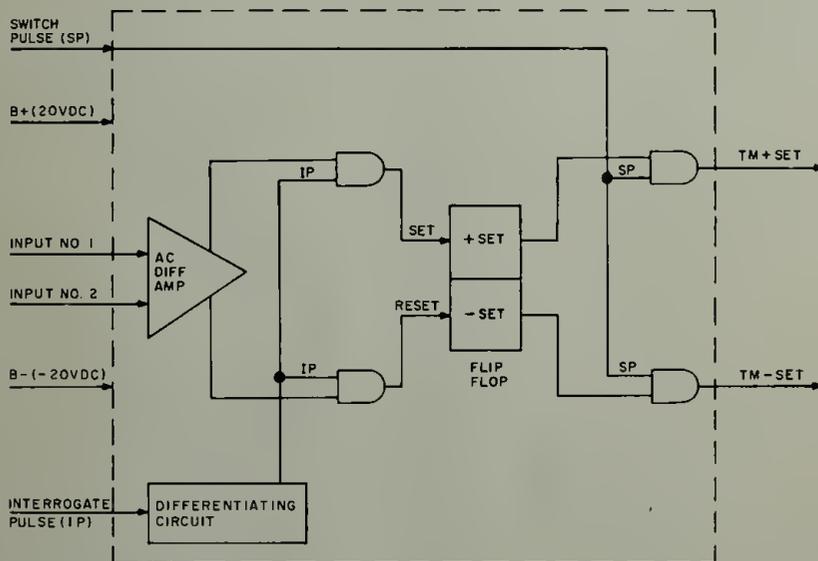
The PIP pendulum motion is an oscillatory motion about its null point and can be measured in cycles per second. As is characteristic of every electro-mechanical loop, there exists some natural resonant frequency. The natural frequency is dependent upon float damping, signal and torque generator sensitivities, and other loop characteristics. In the case of the accelcrometer loop this natural frequency is approximately 500 cps, and the pendulum oscillates at a frequency close to that. At a torque winding selection rate of 3200 pulses per second, the value of this frequency can be any value equal to $3200 \div x$ where x is any even number.

Using the above ratio, it is possible for the pendulum to have a maximum frequency of 1600 cps (x equals 2). A frequency of 1600 cps means that for every torque selection pulse, the torque current would be routed to the opposite torque generator winding. Solving the equation $f = 3200 \div x$, the frequency closest to 500 is 533-1/3. In this case; the value of x is six. Thus one complete pendulum cycle will occur during six torque selection pulses. Dividing the time for the six pulses into positive and negative rotations, it is seen that the PIP functions in a 3-3 mode (positive rotation for three torque selection pulses, negative rotation for three torque selection pulses).

The physical configuration of the PIP is such that the float, when moding in its 3-3 state and sensing no acceleration, rotates an equal angular distance on both sides of an electrical and mechanical null.

The 2 volt rms, 3200 cps, one phase signal generator excitation voltage is synchronized with the LGC clock. The signal generator has a center tapped secondary winding which provides a double ended output, one side having a zero phase reference with respect to the 3,200 cps excitation and the other side a pi phase reference. The center tap is connected to ground. The output signal is representative of the magnitude and direction of the rotation of the pendulous float about the output axis. The error signal is then routed to the preamplifier mounted on the stable member. The phase of the output signal from the preamplifier is -45° from the reference excitation. The phase shifted zero or pi phase signals from the preamplifier are applied as separate inputs to the ac differential amplifier and further amplified. The two signals are then sent to the interrogator.

The ac differential amplifier and the interrogator are packaged in the same module which is located in the pulse torque assembly (PTA) (figure 2-10). The interrogator analyzes the ac differential amplifier outputs to determine the direction of the 16 PIP float movement and generates appropriate torquing commands. The two amplified signals from the ac differential amplifier go to two summing networks and threshold amplifiers (represented in figure 2-10 by AND gates). Interrogate pulses (IP) are continuously being received by the interrogator from the LGC. An interrogate pulse is a two microsecond pulse occurring at 3,200 pps and timed to occur 135 degrees after the positive going zero crossing of the reference excitation. (See figure 2-11.) With this phasing, the interrogate pulse occurs at the 90 degree peaks of the phase shifted zero or pi phase input signals from the PIP preamplifiers. The interrogate pulse occurs at a positive 90 degree peak of the zero phase signal if the float angle is positive and at a positive 90 degree peak of the pi phase signal if the float angle is negative. The zero and pi phase signals and the interrogate pulses are ANDed by the summing network and threshold amplifier. The gated outputs of the threshold amplifier are applied to a flip-flop as set or reset pulses. If the flip-flop is in the +set condition, a succession of set pulses will maintain the +set condition. The +set condition will remain until the float angle passes through null. At this time, a reset pulse is produced to cause the flip-flop to go to the -set condition.



15176B

Figure 2-10. AC Differential Amplifier and Interrogator Module

The outputs of the flip-flop are applied to two AND gates which are also driven by switch pulses received from the LGC. The switch pulses are a train of clock driven 3,200 pps pulses three microseconds in width, timed to occur three microseconds after the leading edge of the interrogate pulse. The flip-flop enables only one output gate at any switch pulse time. The outputs of the AND gates are called the TM + set pulse and the TM - set pulse.

The binary current switch (figure 2-7) utilizes the TM+set and TM-set outputs of the interrogator to generate 16 PIP torquing current. The TM+set and the TM-set pulses furnish the input to a flip-flop. If the flip-flop is in the +set condition, a succession of TM+set pulses will maintain the +set condition. The +set condition will persist until the float angle passes through null. The phase change will cause the flip-flop of the ac differential amplifier and interrogator module to reset to the -set condition. At this time a TM - set pulse is developed and causes the binary current switch flip-flop to go to the -set condition. The outputs of the flip-flop control two transistor current switches. If the flip-flop is in the +set condition, the +set output will be at the base of the +torque current switch and will turn it on. The +torque current switch closes the path from the current regulated 120 vdc supply through the PIPA calibration module to the 16 PIP T+ torque generator coils. If the flip-flop is in the -set condition, the -torque current switch will be turned on, closing the path through the T- torque generator coils.

An acceleration along the PIP input axis causes the pendulous mass to produce a torque which tends to rotate the float about the output axis. The torque produced by the acceleration is proportional to the magnitude of the acceleration. The acceleration produced torque aids and opposes the torque generator forces causing changes in the time required for the float to be torqued back through null. A change in velocity (ΔV) is the product of acceleration and incremental time (Δt), the torque is actually proportional to an incremental change in velocity (ΔV).

$$T_{ACCEL} = K_1 a \Delta t = K_1 \Delta V$$

The float is already in motion due to loop torquing, therefore additional torque is required to overcome the acceleration torque and to keep the pendulum in its oscillatory motion. The additional torque is obtained by supplying torquing current for additional time through one of the torque windings. The current at any one time is a constant, therefore the current must be present for a longer period of time. Thus to determine the amount of acceleration sensed by the PIP, it is necessary only to measure the length of time torquing current is applied to each torque winding.

$$ACCEL_{IND} = K_2 \sum [(T+) - (T-)] \Delta t$$

From the above identities, it is seen that torquing time (Δt) is proportional to the change in velocity (ΔV).

$$K_1 \Delta V = K_2 \Sigma [(T+) - (T-)] \Delta t$$

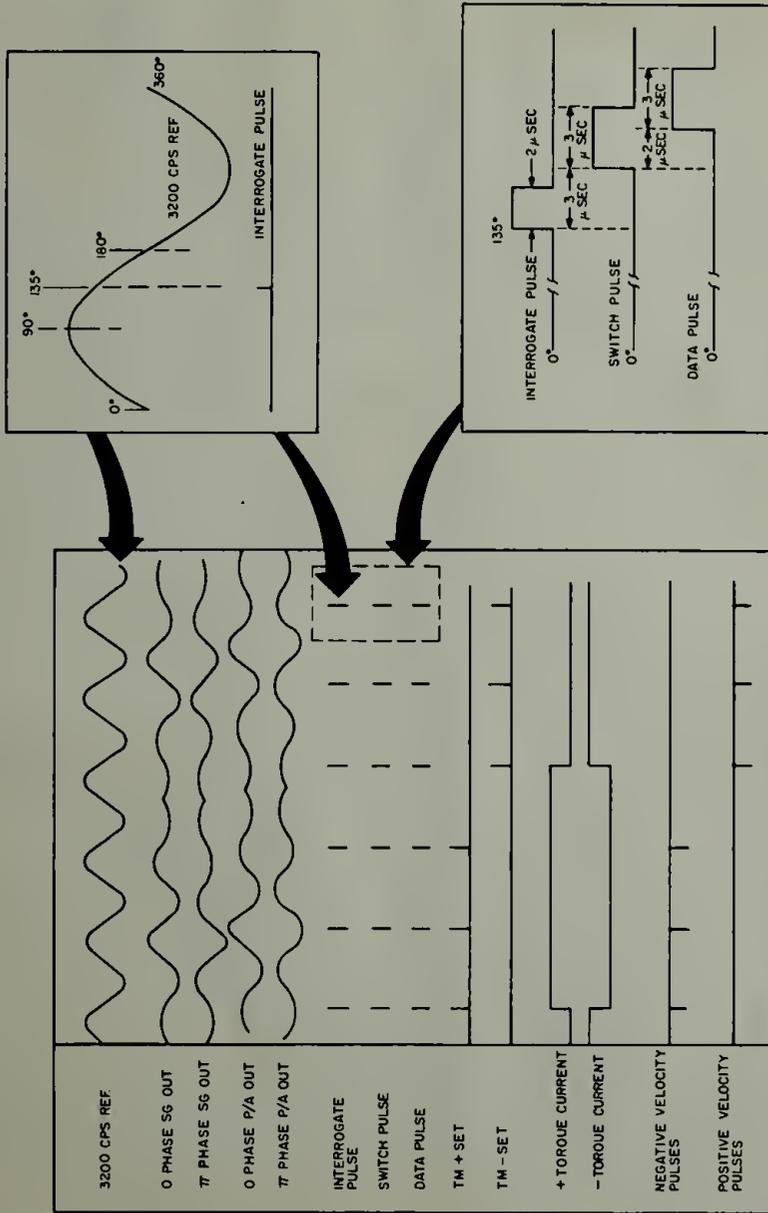
$$\Delta V = \frac{K_2}{K_1} \Sigma [(T+) - (T-)] \Delta t$$

The time (Δt), representative of the ΔV , is sent to the LGC in the form of P and N pulses (figure 2-9).

In addition to selecting the proper torque generator winding, the outputs of the binary current switch flip-flop also go to two AND gates where they are ANDed with the 3,200 cps data pulses from the LGC. The data pulse is three microseconds in width and is timed to occur two microseconds after the leading edge of the switch pulse. (See figure 2-11.) The data pulse and switch pulse are both 3,200 cps, therefore the LGC receives either a P pulse or an N pulse once every $1 \div 3200$ second. When the PIP is sensing no acceleration, the pendulum is oscillating at a frequency of 533-1/3 cps; and the LGC is receiving three P pulses and three N pulses once every cycle or once every $1 \div 533-1/3$ seconds. The LGC contains a forward-backward counter which receives the velocity pulses and detects any actual gain in velocity.

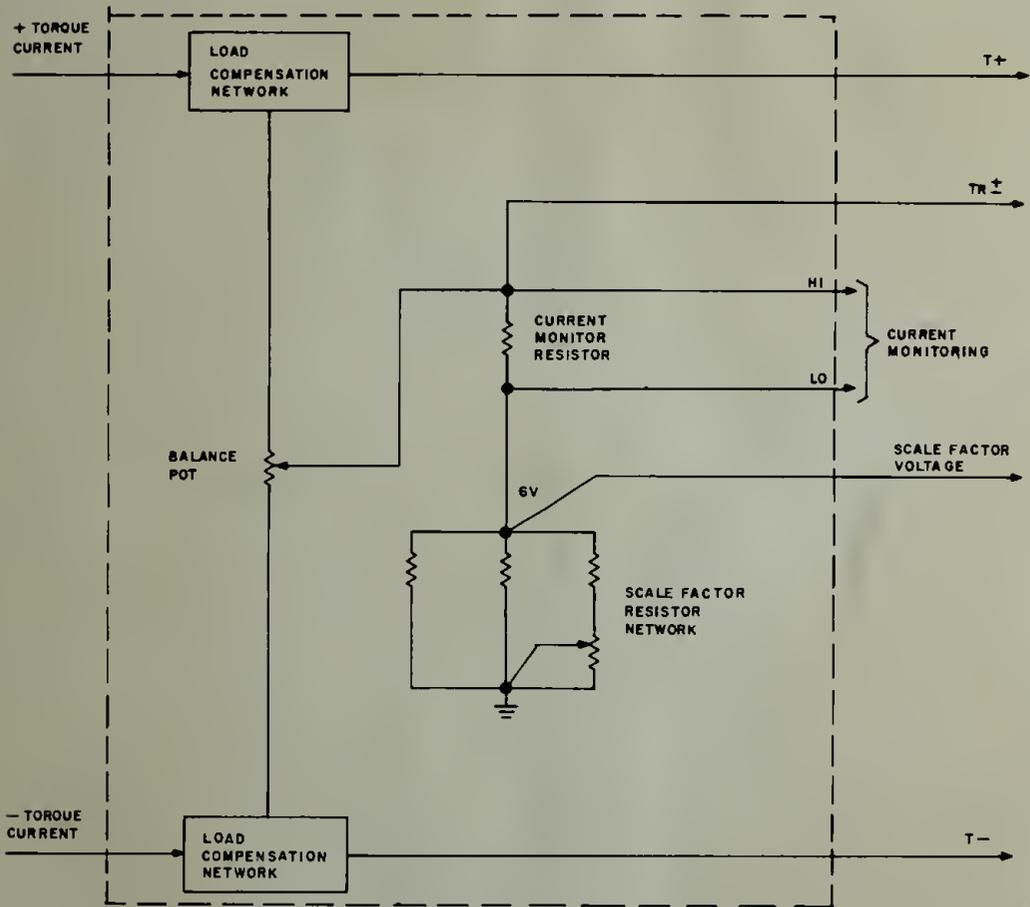
The counter counts forward on the three P pulses and then backward on the three N pulses. The counter continues this operation and generates no ΔV pulses. With an acceleration input to the PIP, however, the loop no longer operates at the 3-3 ratio and the counter exceeds its capacity and reads out the plus or minus ΔV pulses which are then stored and used by the LGC. The additional pulses above the 3-3 ratio are representative of the additional torque supplied by the torque generator to compensate for the acceleration felt by the LEM. Each pulse indicates a known value of ΔV due to the loop scale factor.

The PIPA calibration module (figure 2-12) compensates for the inductive load of the 16 PIP torque generator ducosyns and regulates the balance of the plus and minus torques. The calibration module consists of two load compensation networks for the torque generator coils of the 16 PIP. The load compensation networks tune the torque generator coils to make them appear as a pure resistive load to the binary current switch. A variable balance potentiometer regulates the amount of torque developed by the torque generator coils. Adjustment of this potentiometer precisely regulates and balances the amount of torque developed by the T+ and T- torque generator coils. This balancing insures that for a given torquing current an equal amount of torque will be developed in either direction.



15175C

Figure 2-11. Accelerometer Timing



15192B

Figure 2-12. PIPA Calibration Module

The calibration module also includes a current monitor resistor and an adjustable scale factor resistor network in series with the torque generator coils. A nominal six volts is developed across the scale factor resistor network due to the torquing current and is applied as an input to the dc differential amplifier and precision voltage reference module. The voltage drop across the current monitor resistor is used for external monitoring purposes.

The dc differential amplifier and PVR are identical to the ones used in the fine align electronics. (See figure 2-8.) The dc differential amplifier and PVR module maintain the current through the ducosyn torque generator coils at 43 milliamperes. The PVR is supplied with regulated 28 vdc and, through the use of precision circuits, develops an accurate 6 volts for use as a reference voltage. The scale factor resistor in the calibration module also develops 6 volts when 43 milliamperes of current flows through it. A comparison is made by the dc differential amplifier of the PVR 6 volts and the scale factor 6 volts. Any deviation of the binary current switch torquing current from the nominal 43 milliamperes will increase or decrease the scale factor resistor voltage and result in an output error signal from the dc differential amplifier. This error signal controls the current regulator in the binary current switch. The current regulator, which is in series with the 120 vdc source and the ducosyn torque generator coils, will maintain the torque current at 43 milliamperes.

2-4.4 IMU TEMPERATURE CONTROL SYSTEM

The IMU temperature control system (figure 2-13) maintains the temperature of the stabilization gyros and accelerometers within the required temperature limits during both standby and operating modes of the IMU. The system supplies and removes heat to maintain the IMU heat balance with minimum power consumption. Heat is removed by convection, conduction, and radiation. The natural convection used during IMU standby mode changes to blower controlled, forced convection during IMU operating modes. The IMU internal pressure is maintained between 3.5 and 15 psia to enable the required forced convection. To aid in removing heat, a water-glycol solution at approximately 45.0 degrees Fahrenheit from the spacecraft coolant system passes through the coolant passages in the IMU support gimbal.

2-4.4.1 Temperature Control Circuit. The temperature control circuit maintains the gyro and accelerometer temperature. The temperature control circuit consists of a temperature control thermostat and heater assembly, a temperature control module, three IRIG end mount heaters, three IRIG tapered mount heaters, two stable member heaters, and three accelerometer heaters. The thermostat and heater assembly is located on the stable member and contains a mercury-thallium thermostat, a bias heater, and an anticipatory heater. Except for the bias heater, all heaters (a total of 12) are connected in parallel and are energized by 28 vdc through the switching action of transistor Q2, which completes the dc return path. The thermostat acts as a control sensing element and senses the temperature of the stable member.

When the temperature falls below 130 (± 0.2) degrees Fahrenheit, the thermostat opens and transistor Q1 conducts and drives transistor Q2 to conduction. When transistor Q2 conducts, current will flow through the twelve heaters. Because of the large mass of the stable member, its temperature will increase at a relatively slow rate as compared to the gyros, which have a heater in each end mount. The anticipatory heater improves the response of the thermostat to insure that the magnitude of the temperature cycling of the gyros and the accelerometers is as small as possible. When the temperature rises above 130 (± 0.2) degrees Fahrenheit, the thermostat closes and the base of transistor Q1 is shorted to ground, cutting off transistors Q1 and Q2 and deenergizing the heaters. The thermostat has a 0.5 degree deadband which is the difference between contact closing with rising temperature and contact opening with falling temperature. The temperature control circuit will maintain the average of the gyro temperatures at 135 (± 1.0) degrees Fahrenheit and the average of the accelerometer temperatures at 130 (± 1.0) degrees Fahrenheit under normal ambient conditions. The temperature difference between the gyros and the accelerometers is adjusted by properly proportioning the amount of power in each heater. The balance is obtained by selection of resistor R1.

During IMU operation, power is applied to the fixed accelerometer heaters to compensate for the additional heat supplied to the gyros by the gyro wheel motor heat dissipation. Power is also applied to a bias heater on the control thermostat. The bias heater supplies a fixed amount of heat to the control thermostat to maintain the proper absolute temperature level of the gyros and accelerometers. The amount of bias heat is controlled by the selection of resistor R5. The power for the fixed accelerometer heaters and the thermostat bias heater are the -90 degree and -180 degree outputs, respectively, from the 28 vac power supplies which are also used for gyro wheel power.

The 28 vdc heater power is applied to the heaters through the contacts of a safety thermostat which will provide protection against an extreme overheat condition in case a malfunction occurs in the temperature control circuit. The safety thermostat contacts open at 139.5 (± 3.0) degrees Fahrenheit and close at 137 (± 3) degrees Fahrenheit.

2-4.4.2 Blower Control Circuit. The blowers maintain IMU heat balance by removing heat. The blowers operate continuously during IMU operate modes. The blower control circuit shown on figure 2-13 is inoperative because the contacts of blower control relay K1 are bypassed.

The blowers are supplied from the -90 and -180 degree outputs of the 28 volt, 800 cps, 2.5 percent power supply which also provides gyro wheel motor power. Fused phase shift networks are associated with each blower so that excitation and control current can be supplied from the same source.

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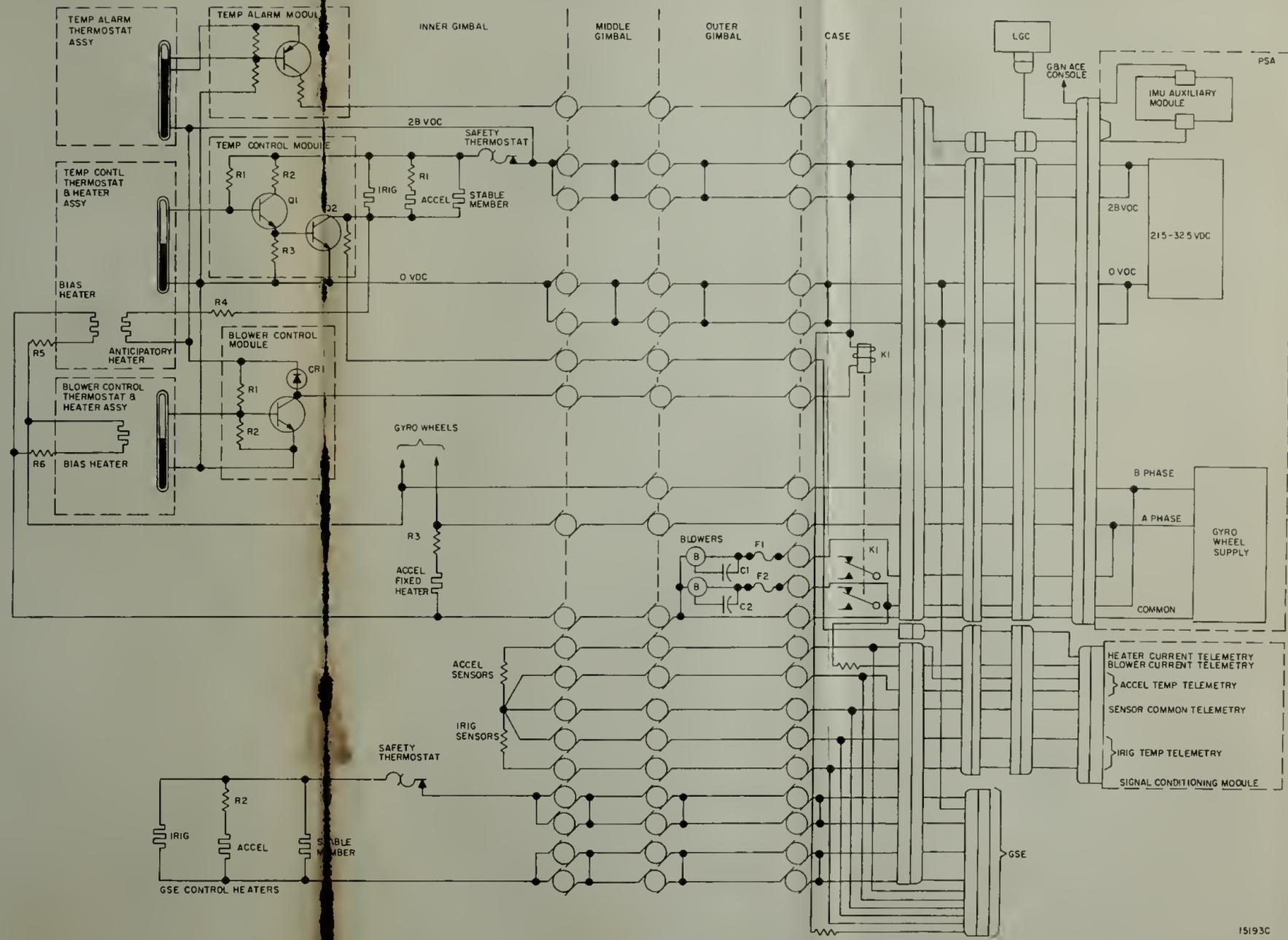
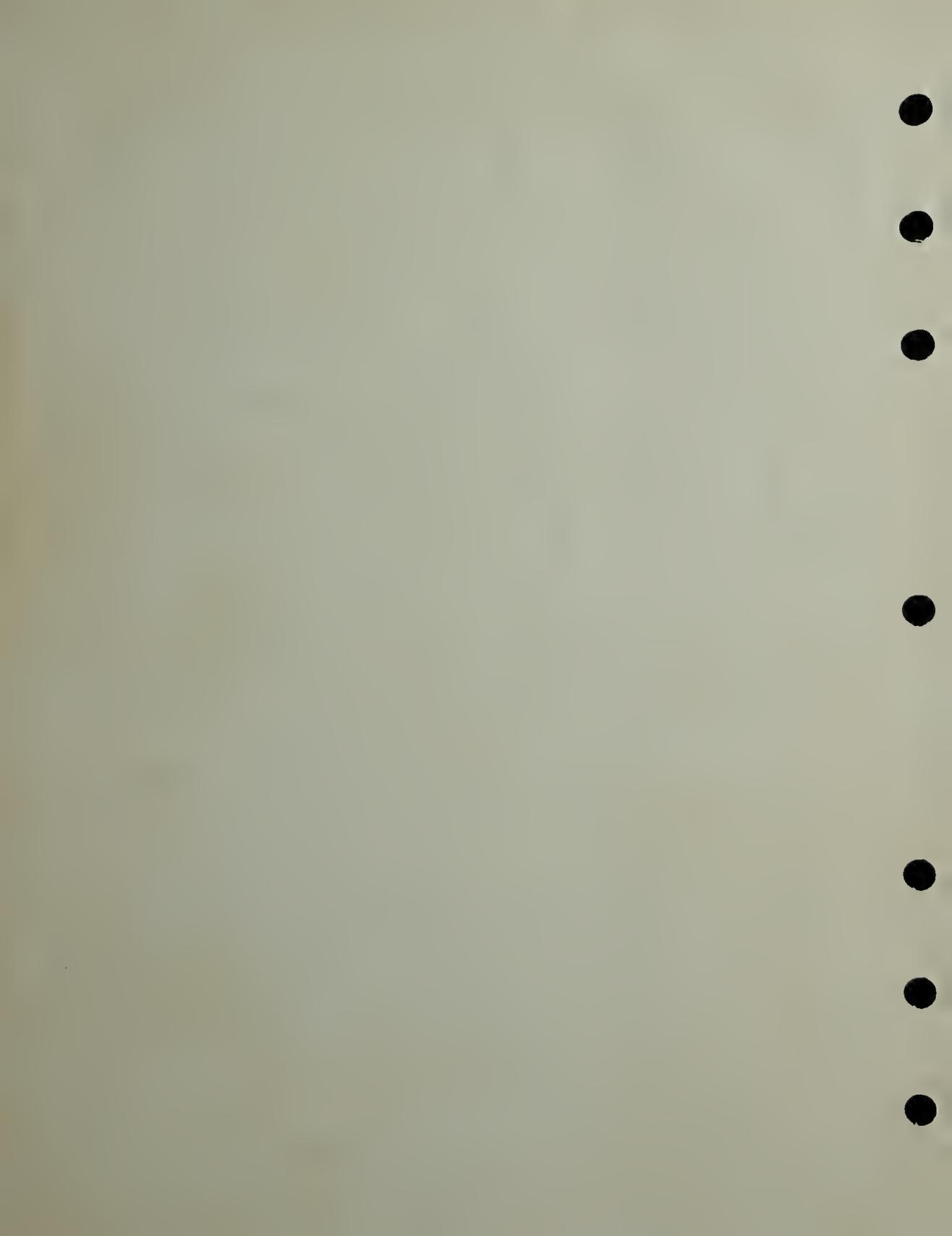


Figure 2-13. IMU Temperature Control System

15193C



2-4.4.3 Temperature Alarm Circuit. The temperature alarm circuit monitors the temperature control system. The temperature alarm circuit consists of a temperature alarm thermostat and a temperature control module. If a high or low temperature is sensed by the temperature alarm thermostat located on the stable member a discrete is sent to the LGC and the IMU auxiliary module. When the temperature is within the normal range of 126.3 to 134.3 degrees Fahrenheit, 28 vdc is applied through the thermostat to the emitter of transistor Q1 causing the transistor to conduct. Transistor Q1 conducts through a grounding system in the LGC.

When the temperature falls below 126.3 degrees Fahrenheit, 28 vdc will be removed from transistor Q1, causing it to stop conducting and thus signaling the LGC of an alarm condition. When the temperature rises above 134.3 degrees Fahrenheit, 28 vdc will be applied directly to the base of the transistor as well as to the emitter. With 28 volts applied to both emitter and base, the base-emitter junction is no longer forward biased and the transistor stops conducting which signals the LGC of an alarm condition. There is no differentiation between a high or low temperature alarm. When the LGC senses a temperature alarm, it causes the IMU TEMP lamp and the PGNCS lamp to light. When the IMU auxiliary module receives a temperature alarm, it sends the information to telemetry.

2-4.4.4 External Temperature Control. External temperature control of the IMU is provided by GSE control heater circuits in the IMU which are controlled externally to the airborne equipment by the portable temperature controller or the temperature monitor control panel of the optics-inertial analyzer (OIA). The GSE control heater circuitry consists of a safety thermostat, six gyro heaters, two stable member heaters, three accelerometer heaters, temperature indicating sensors, and an IMU standby power sensor which disables the GSE when airborne power is on. The temperature indicating sensors act as the control sensing element of the external control and indicating circuitry. The heaters are connected in parallel. The six gyro temperature indicating sensors (two in each gyro) are connected in series to sense the average temperature of the gyros. The three accelerometer temperature indicating sensors (one in each accelerometer) are connected in series to sense the average temperature of the accelerometers. All of the GSE control heater circuitry is electrically independent of the airborne temperature control system and will not be used at the same time that the IMU temperature is being controlled by the airborne temperature control system. The GSE control heater circuitry cannot be used as a backup temperature control system during flight.

2-4.5 ISS MODES OF OPERATION. The ISS has four major modes of operation: IMU turn on, CDU zero, coarse align, and inertial reference. Submodes which will also be discussed are fine align, IMU cage, attitude error indication and display inertial data. An additional mode is the master reset condition which is available during laboratory testing only. All ISS moding is initiated and controlled by computer discrettes to the CDU. (See figure 2-14.) To select an ISS mode of operation, the LGC can send a single discrete, a combination of discrettes, or no discrettes. The display inertial data function utilizes the LORS channels of the CDU, therefore, a description of the discrettes to the LORS channels of the CDU will also be presented.

2-4.5.1 CDU Discrettes. All LGC discrettes issued to the CDU to initiate and control the various ISS modes or functions are 0.0 (± 2) vdc. LGC ground, applied through a 2,000 ohm source impedance to the CDU mode module.

2-4.5.1.1 ISS CDU Zero. The ISS CDU zero discrete zeros or clears all three ISS CDU read counters simultaneously. It also inhibits the transmission of incrementing pulses to the read counters for the period of time the discrete is present. The CDU discrete will be present (minimum duration is approximately 400 milliseconds) for as long as the read counters are to be held at zero. The IMU is not disturbed by the CDU zero discrete.

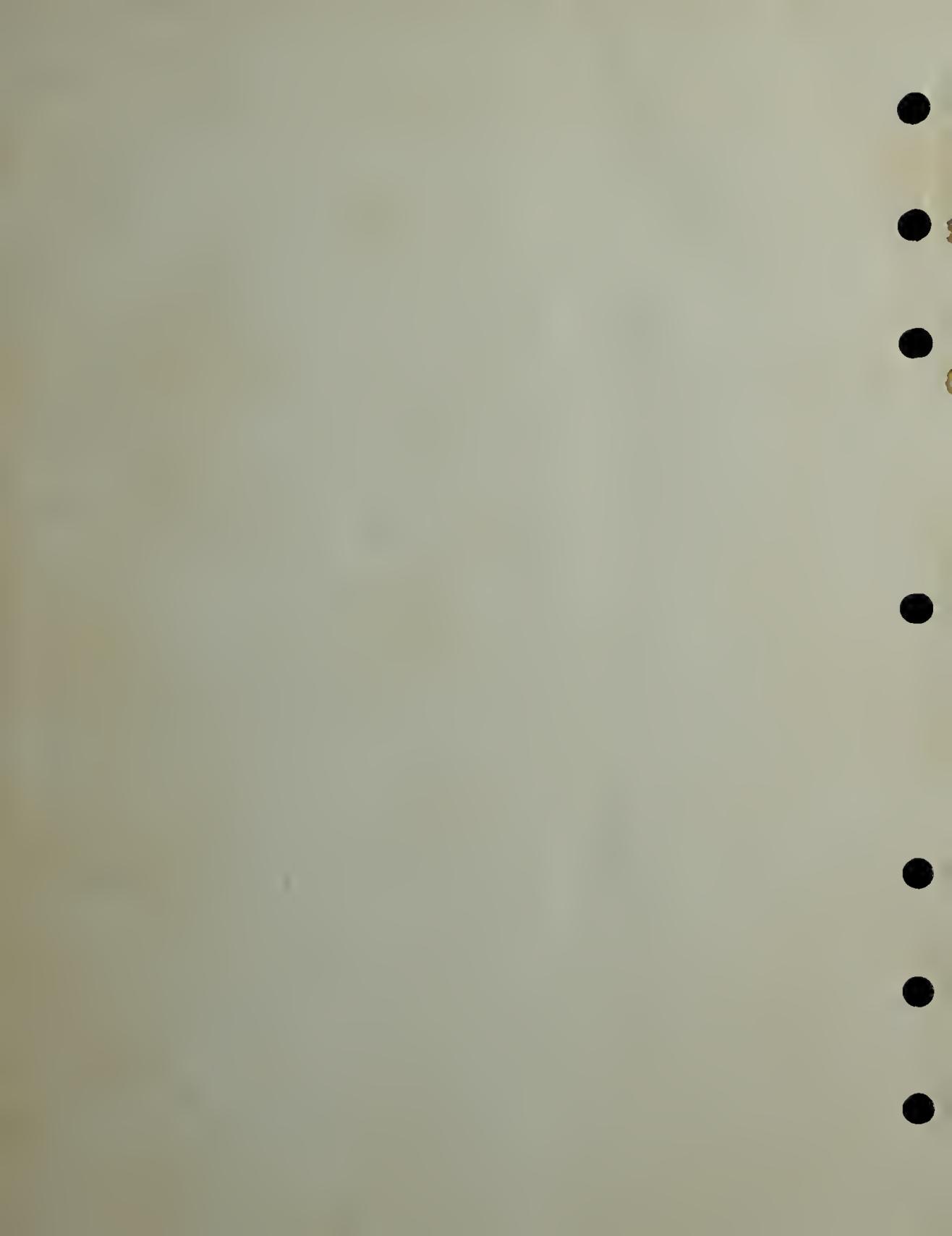
2-4.5.1.2 ISS Enable Error Counter. The ISS enable error counter discrete enables all three ISS error counters simultaneously which allows them to accept incrementing pulses from the LGC. The error counters are normally cleared and inhibited. The ISS enable error counter discrete is used in conjunction with the coarse align enable discrete during the coarse align mode. The ISS enable error counter enable discrete is used alone when display of attitude error signals on the FDAI is required only.

2-4.5.1.3 Coarse Align Enable. The coarse align enable discrete enables a relay driver which energizes the coarse align and demodulator reference relays located in the PSA. This connects the coarse align error signal to the gimbal servo amplifiers and changes the reference voltage for the demodulator in the gimbal servo amplifiers from 3,200 cps to 800 cps. The discrete also enables the digital feedback pulses from the read counter to the error counter. The presence of the coarse align enable discrete and the absence of the enable error counter discrete also inhibit the incrementing pulses to the read counter.

2-4.5.1.4 D/A Enable. The D/A enable discrete enables both LORS CDU error counters simultaneously. The error counters are normally cleared and inhibited. The LGC normally provides positioning signals to the optical tracker through the LORS channels of the CDU. The D/A enable discrete, however, is also used in conjunction with the display inertial data discrete to allow the LGC to feed inertially derived velocity data through the LORS channels of the CDU to meter displays.

2-4.5.1.5 Display Inertial Data. The display inertial data discrete energizes relays which switch the dc output from the digital to analog (D/A) converter in the LORS channels of the CDU to the LEM velocity meters.

2-4.5.1.6 LORS CDU Zero. The LORS CDU zero discrete clears both LORS read counters simultaneously and inhibits the transmission of incrementing pulses to the read counters. This discrete is not used for any ISS flight modes or functions but can be used for CDU test functions.



2-4.5.2 IMU Turn On Mode. The purpose of the IMU turn on mode is to drive the gimbals to their zero position and hold them there. (See figure 2-15.) The IMU turn on mode is initiated upon closure of the ISS OPERATE circuit breaker and allows for a 90 second gyro run up period. The ISS OPERATE circuit breaker routes 28 vdc IMU operate power through the deenergized contacts of the ISS turn on control relay, located in the IMU auxiliary assembly module, to the cage relays. The 28 vdc IMU operate power is also routed through the same deenergized contacts to the LGC as a continuous turn on delay request discrete. The cage relays energize and, in turn, cause the coarse align relays to be energized. The cage relays route the IX gimbal resolver sine winding outputs through the contacts of the coarse align relays to the respective gimbal servo amplifiers. The gimbal servo amplifiers drive the gimbals until the resolver signals are nulled. The operation of the caging loops is discussed further in the IMU cage mode description.

Upon receipt of the ISS turn on delay request discrete, the LGC sends the ISS CDU zero discrete and the coarse align enable discrete to the CDU for a minimum period of 90 seconds. The CDU zero discrete clears the read counters and inhibits the incrementing pulses to the read counters. The coarse align enable discrete provides a redundant means of energizing the coarse align relays.

A second set of deenergized contacts on the ISS turn on control relay routes a ground to the time delay circuit of the pulse torque power supply which inhibits the operation of the power supply and thus prevents accelerometer pulse torquing during the 90 second turn on period. This allows time for the accelerometer floats to become centered and the gyro wheels to run up prior to torquing.

After the 90 second delay has been completed, the LGC sends the ISS turn on delay complete discrete. The ISS turn on delay complete discrete acts through a relay driver to energize and latch in the ISS turn on control relay. Energizing the ISS turn on control relay deenergizes the cage relay, removes the ISS turn on delay request discrete, and removes the inhibit from the pulse torque power supply. The computer program can then place the ISS in the inertial reference mode by removing both the CDU zero and the coarse align enable discrettes, or it can initiate the coarse align mode by removing only the CDU zero discrete and sending the ISS enable error counter discrete. The IMU turn on circuit will be reset whenever 28 vdc IMU operate power is turned off.

2-4.5.3 IMU Cage Mode. The IMU cage mode is an emergency backup mode which allows the astronaut to recover a tumbling IMU by setting the gimbals to zero. (See figure 2-15.) During this mode, the IX gimbal resolver sine winding outputs are fed through the CDU to the gimbal servo amplifiers to drive the gimbals until the resolver signals are nulled.

The IMU cage mode is initiated when the astronaut presses the IMU CAGE switch. The switch is held until the gimbals settle at the zero position (five seconds maximum). The gimbal position may be observed on the FDAI. The IMU CAGE switch routes a 28 vdc discrete signal to the LGC and to the cage relays located in the PSA. (See figure 2-15.) The cage discrete energizes the cage relays, which in turn, cause the coarse align relays, the demodulator reference relay, and a relay in the gimbal servo amplifiers to energize. The relay in the gimbal servo amplifiers switches in additional capacitance into the RC compensation networks to tune them for 800 cps operation. The demodulator reference relay changes the gimbal servo amplifier demodulator reference signal from 3,200 cps to 800 cps. The cage relays switch the 1X gimbal resolver sine winding outputs through the energized contacts of the coarse align relays into the corresponding gimbal servo amplifier inputs. The gimbal servo amplifiers drive the gimbals until the resolver signals are nulled.

Upon receipt of the IMU cage discrete, the LGC will discontinue sending the error counter enable discrete, the coarse align enable, the display inertial data discrete, and the incrementing pulses to the CDU. The LGC will also discontinue sending torquing commands, if any are in process, to the fine align electronics.

After the IMU CAGE switch is released, the LGC will allow the read counters to settle and will then place the PGNCs in an attitude control mode. During the time the IMU cage discrete is present and while the read counters are settling, the NO ATT lamp on the DSKY is lighted.

The cage mode will also be entered automatically if the IMU is turned on when the LGC is off or in standby mode. During the normal turn on sequence, the closure of the ISS OPERATE circuit breaker will route 28 vdc through the deenergized contacts of the ISS turn on control relay to the cage relays. The cage relays energize and cage the gimbals. After the 90 second turn on time delay has been completed, the LGC will send the ISS turn on delay complete discrete which will energize the ISS turn on control relay which, in turn, deenergizes the cage relays. If, however, the LGC is off or in standby when the IMU is turned on, the ISS turn on control relay will remain deenergized and the ISS will remain in the IMU cage mode.

If the IMU cage mode is entered as a result of an IMU turn on with the LGC off or in standby, the ISS can be placed in the inertial reference mode by allowing 90 seconds for gyro runup then pressing the IMU CAGE switch. The IMU CAGE switch will energize and latch in the ISS turn on control relay which removes the 28 vdc which had been energizing the cage relays. With the ISS turn on control relay latched, the cage relays will deenergize and remain deenergized when the IMU CAGE switch is released. Deenergizing the cage relays causes the coarse align relays to be deenergized which connects the gyro error signals to the respective gimbal servo amplifiers. The stabilization loops will maintain the stable member inertially referenced to the orientation established by the caging loops.

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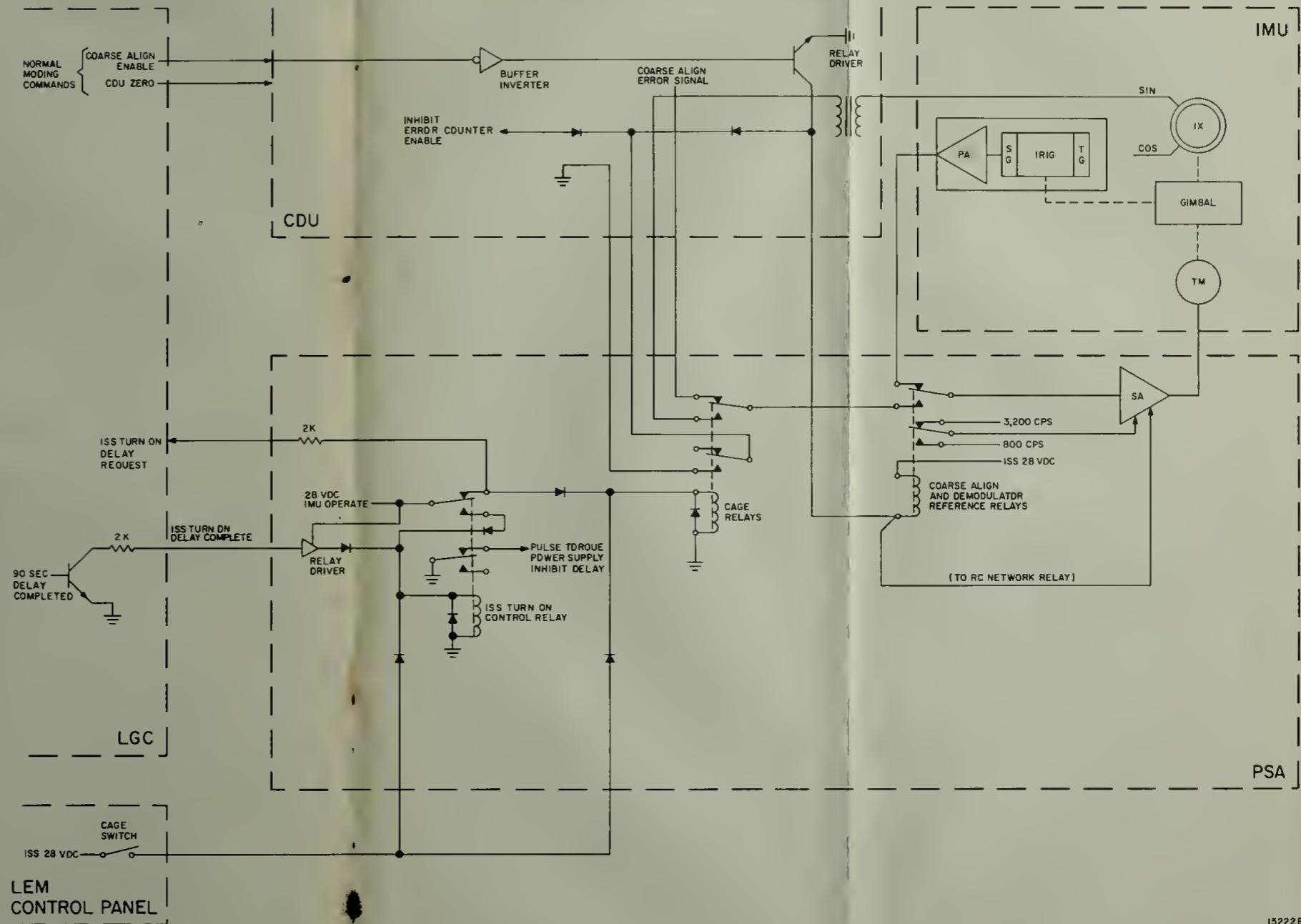


Figure 2-15. IMU Cage Mode

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2-4.5.4 ISS CDU Zero. The purpose of the ISS CDU zero mode is to clear and inhibit the three ISS CDU read counters. (See figure 2-14.) The mode is initiated by the LGC sending the ISS CDU zero discrete. The presence of the discrete is maintained for as long as the read counters are to be held at zero.

2-4.5.5 Coarse Align Mode. The purpose of the coarse align mode is to change the orientation of the gimbals by LGC command. The change in gimbal orientation is accomplished by feeding the CDU error counter computer pulses equal to the required change in gimbal angles. The mode is initiated when the LGC sends the coarse align discrete and, after a short delay, the ISS error counter enable discrete to the three ISS portions of the CDU. When the mode is entered, the CDU read counter will be in the process of repeating the gimbal angle and supplying angular data to the LGC and will continue to do so for the duration of the coarse align mode. The LGC, knowing the actual gimbal angle registered in the read counter, calculates the desired amount of change in gimbal angle required to reposition the gimbal to the desired angle and converts this change into a number of $\pm\Delta\theta_c$ pulses to be sent to the error counter. The $\pm\Delta\theta_c$ pulses are sent to the error counter at a rate of 3,200 pps in bursts of 80 milliseconds duration. Bursts of pulses are sent 600 milliseconds apart. Each $\Delta\theta_c$ pulse is equal to a change in gimbal angle of 160 arc seconds. The error counter, having been enabled, accepts the pulses and counts up or down, as necessary, until all the pulses have been registered.

The digital information in the error counter is converted into an 800 cps, amplitude modulated, analog error signal by the ladder decoder in the D/A converter module. The ladder decoder signal is summed with a feedback signal and applied through a mixing amplifier located in the D/A converter module to the gimbal servo amplifiers to drive the gimbals to the desired angles. The function of the feedback signal and the mixing amplifier will be discussed later. The output of the mixing amplifier, referred to as the coarse align error signal, is applied to the gimbal servo amplifiers through the contacts of the coarse align relays located in the PSA. The coarse align relays, which are energized by the coarse align enable discrete acting through a relay driver, switch the input of gimbal servo amplifiers from the gyro preamplifiers to the coarse align error signal output of the ISS D/A converter. The demodulator reference relay is also energized by the coarse align enable discrete and switches the reference frequency of the demodulator in the gimbal servo amplifiers from 3,200 cps to 800 cps. The coarse align enable discrete also energizes a relay in the gimbal servo amplifiers which switches in additional capacitance into the amplifier's compensation networks to tune them for 800 cps operation.

As the gimbals are driven, $\pm\Delta\theta_c$ pulses, representing the change in actual gimbal angle, are generated by the read counter and applied to the error counter. The $\Delta\theta_c$ pulses are also equal to 160 arc seconds and act to decrease the $\Delta\theta_c$ pulses registered in the error counter. The error counter output to the ladder decoder, therefore, represents the difference between the desired amount of change in gimbal angle and the amount of change actually accomplished. When the error counter reaches a null and the gimbals stop moving, the actual gimbal angle has changed by an amount equal to the total value of the $\pm\Delta\theta_c$ pulses sent by the LGC to the error counter.

The rate at which the gimbals are driven is limited to prevent damage to the gyros and to assure that the read counter can track the gimbal angle accurately. The rate of gimbal movement is limited by feeding back the CDU fine error signal $[\sin 16 (\theta - \psi)]$ to the input of the mixing amplifier located in the D/A converter module. The CDU fine error signal is out of phase with the output of the ladder decoder and has an amplitude proportional to the difference between the actual gimbal angle (θ) and the angle in the read counter (ψ). The fine error signal is applied through a voltage limiting circuit to the summing junction of the mixing amplifier where it is summed with the 800 cps ladder decoder output signal. The D/A converter ladder decoder output is applied to the mixing amplifier through a scaling amplifier and a voltage limiting diode network. The scaling amplifier controls the signal gain to produce a scale factor of 0.3 volt rms per degree. The output of the mixing amplifier will be at a null when the D/A converter ladder decoder output, after limiting, is equal to the fine error feedback signal. The fine error signal will be a constant value only when the gimbal and the CDU are going at the same rate and with the gimbal angle leading the CDU angle. Since the CDU is limited to counting at one of two speeds, the gimbals will be limited to a rate equal to one of these two speeds. During the coarse align mode, the CDU is limited to a high counting speed of 6.4 kpps and a low counting speed of 800 cps. At all other times, the high counting speed is 12.8 kpps.

If the gimbals are moving at a faster rate than the rate at which the CDU is counting, the fine error signal will increase, causing a retarding torque to be developed by the gimbal servo amplifier. If the gimbals are moving at a rate slower than the rate at which the CDU is counting, the fine error signal will decrease, causing the gimbal servo amplifier to apply an accelerating torque to the gimbals. By adjusting the gain of the fine error signal into the mixing amplifier, the gimbal drive rate is limited to either 35.5 degrees per second (6.4 kpps CDU counting rate) or 4.5 degrees per second (800 cps CDU counting rate).

2-4.5.6 Inertial Reference Mode. The inertial reference mode provides a coordinate reference system on which attitude and velocity measurements and calculations may be based. During the inertial reference mode, the stable member is held fixed with respect to an inertial reference by the stabilization loops. The ISS CDU read counters provide the LGC with changes in gimbal angles with respect to the stable member. The ISS is in the inertial reference mode during any operating period in which there is an absence of moding commands. During the inertial reference mode, the fine align electronics is inhibited and the ISS CDU error counters are cleared and inhibited.

2-4.5.7 Fine Align Mode. The purpose of the fine align mode is to reposition the stable member to a fine alignment by torquing the gyros. The fine align mode is actually a gyro torquing function accomplished during the inertial reference mode. The torquing current to the gyros is provided by the fine align electronics located in the PTA. The fine align electronics is enabled and controlled by LGC pulses sent directly to the fine align electronics. The LGC does not send command discrettes to the ISS CDU's during this mode. The ISS is in the inertial reference mode prior to the enabling of the fine align electronics and returns to that mode when the fine align electronics is disabled.

The fine align electronics torques the gyros on a time shared basis. The LGC sends four types of pulse trains to the fine align electronics. The first pulse train sent is the torque enable command which enables the fine align electronics. The second pulse train is a gyro select command which selects a particular gyro and the direction it is to be torqued by means of a switching network which closes the current path through the proper torque ducosyn coil. The third and fourth types of pulse trains are the torque set and torque reset commands which control a binary current switch to start and stop the current flow through the selected torque ducosyn coil. The amount of current flow through the torque ducosyn coils is precisely controlled at a fixed value. The amount of gyro torquing to be accomplished is determined by the amount of time torque current is applied, that is, the time duration between the receipt of the torque set and the torque reset commands. This time duration is calculated by the LGC programs and may be based on optical alignment measurements. The torque ducosyn displaces the gyro float, causing the ducosyn signal generator to apply an error signal to the stabilization loop. The stabilization loops drive the gimbals to reposition the stable member. Upon completion of the torquing, the stable member remains fixed in its inertial reference and in fine align mode until the torque enable command is removed, after which the ISS remains in inertial reference mode until further change is commanded.

During the fine align mode, the ISS error counters remain cleared and inhibited. The read counters continue to repeat the gimbal angles and send angular data ($\pm\Delta\theta_c$) to the LGC.

2-4.5.8 Attitude Error Indication. The attitude error indication mode supplies attitude error signals to the FDAI. The attitude error indication mode is initiated when the LGC sends the ISS error counter enable discrete to the CDU. The LGC will calculate the difference between the actual gimbal angles and the correct angles and convert this into the number of $\pm\Delta\theta_c$ pulses to be sent to the error counter. The error counter, having been enabled, accepts the pulses and counts up or down until it has registered all the pulses.

As the actual gimbal angles increase or decrease, $\pm\Delta\theta_c$ pulses, which represent the change in actual gimbal angle, are generated by the read counter and applied to the error counter. The $\pm\Delta\theta_c$ pulses cause the error counter to count up or down and, in effect, register the difference between the actual gimbal angle and the desired gimbal angle. The digital information in the error counter is converted into an 800 cps, amplitude modulated, analog error signal by the ladder decoder in the D/A converter. This ac signal is applied through a scaling amplifier to the FDAI.

2-4.5.9 Display Inertial Data. The display inertial data mode permits the LGC to provide inertially derived forward and lateral velocity signals through the digital to analog section of the LORS channels of the CDU to the LEM velocity display meters. The display inertial data mode is used during the last phases of the LEM powered descent.

The display inertial data mode is requested by the astronaut closing a switch on the main control panel. (See figure 2-16.) The mode is initiated by the LGC sending the display inertial data discrete to the LORS channels of the CDU. The display inertial data discrete acts through a relay driver to energize relays which connect the D/A converter dc error signal outputs to the LEM velocity display meters. After a brief delay to allow for relay pull in time, the LGC sends the D/A enable discrete followed by incrementing pulses to the error counters. The LGC sends $\pm \Delta \theta_c$ pulses representing LEM forward velocity (motion along the Z_{LEM} axis) to one error counter and $\pm \Delta \theta_c$ pulses representing LEM lateral velocity (motion along the vehicle Y_{LEM}) to the other error counter. The read counters will not send incrementing pulses to the error counters; therefore, the only information registered in the error counters will be the $\pm \Delta \theta_c$ pulses.

The digital information registered in the error counter is converted into an 800 cps, amplitude modulated, analog signal by the ladder decoder in the D/A converter. This signal is converted into a positive dc analog signal by a phase sensitive demodulator circuit also located in the D/A converter. The dc analog signal is applied through the energized relay contacts to the LEM velocity display meters. As the velocity changes, as calculated by the LGC, representative $\pm \Delta \theta_c$ pulses will continue to be sent to the error counter, causing it to count up or down and thereby changing the D/A converter dc signal to the display meters.

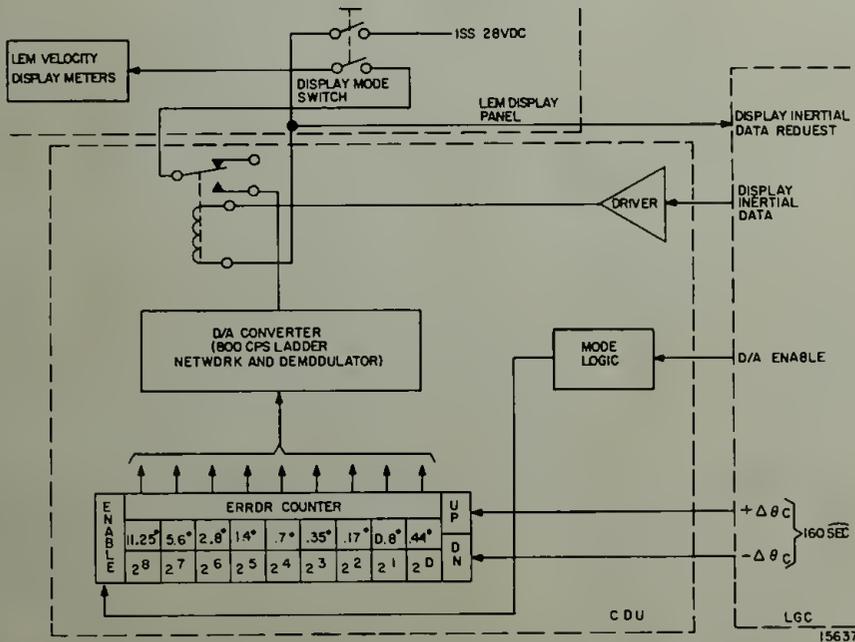


Figure 2-16. Display Inertial Data Mode

2-4.5.10 Master Reset Condition (Test Area Only). The purpose of the master reset condition is to establish preselected standard operating modes in both the airborne equipment and the GSE. The master reset condition is operable in the ISS test configuration only. The master reset condition is initiated when the MASTER RESET pushbutton on the test control panel of the OIA is pressed.

The effects of establishing a master reset condition are dependent upon the particular ISS level of test, power mode status, et cetera, at the time the MASTER RESET pushbutton is pressed. With the ISS STANDBY pushbutton selected, but prior to pressing the ISS OPERATE pushbutton, the MASTER RESET pushbutton will cause the simultaneous closure of the IMU stabilization loops. During the first 90 seconds after pressing the ISS OPERATE pushbutton, the MASTER RESET pushbutton is disabled. Ninety seconds after pressing the ISS OPERATE pushbutton, the MASTER RESET pushbutton is enabled and, if selected, simultaneously performs the following operations: causes the coarse align mode to be commanded, places the gimbals under gimbal positioner control, and removes all IMU caging signals. The master reset condition also discontinues all LORS mode commands and commands the LORS channels of the CDU to repeat the LORS angles.

2-4.6 ISS POWER SUPPLIES.

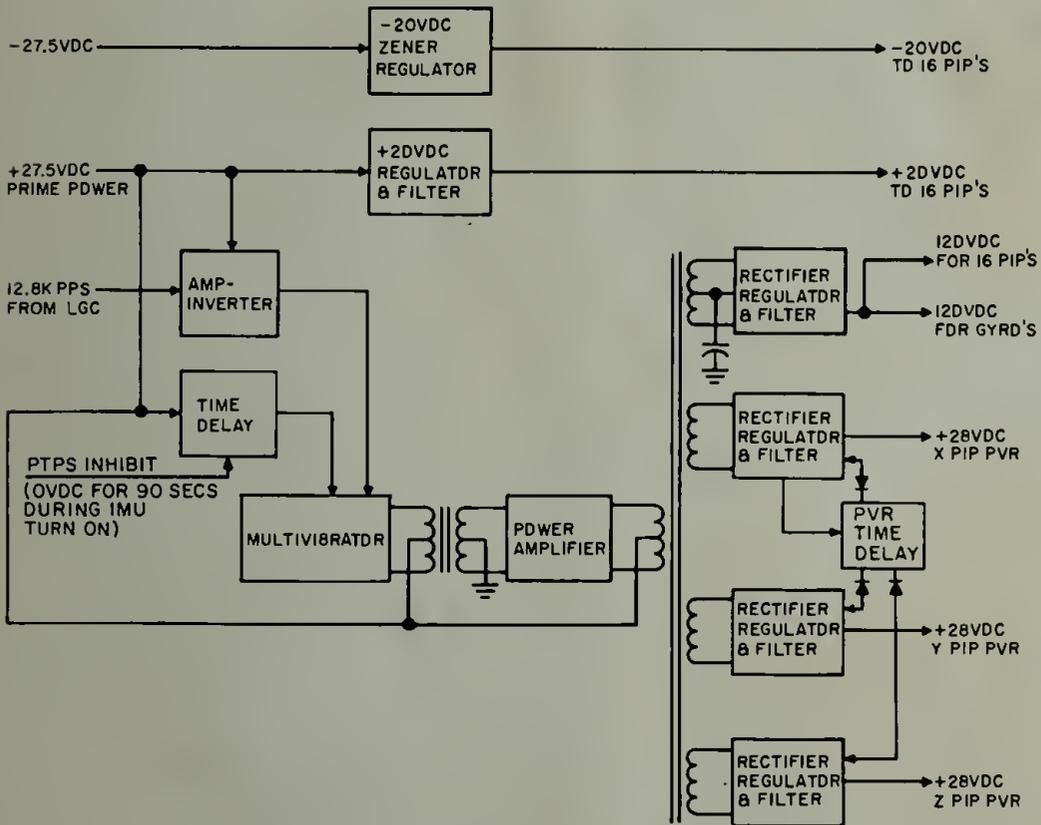
The ISS power supplies convert the +28 vdc prime LEM power into the various dc and ac voltages required by the ISS. The power supplies are the pulse torque power supply; the -28 vdc power supply; the 800 cps, 1 percent power supply; the 800 cps, 5 percent, 2 phase, power supply; and the 3,200 cps power supply. The pulse torque power supply is in the PTA and the remaining power supplies are in the PSA.

The +28 vdc prime power is supplied by the LEM electrical power system through the ISS OPERATE circuit breaker. All ac power supplies are synchronized to the LGC clock by means of computer pulses. The dc supplies, using multivibrators as ac sources for transformation, are also synchronized to the LGC. Synchronization is accomplished by a multivibrator which will free run at a lower frequency without the computer pulses, assuring operation of the ISS power supplies in the event of an LGC failure.

2-4.6.1 Pulse Torque Power Supply. The pulse torque power supply (figure 2-17) provides 120 vdc to the three binary current switches and three dc differential amplifiers in the accelerometer loops and the binary current switch and dc differential amplifier in the stabilization loop fine align electronics. The pulse torque power supply also provides three individual 28 vdc outputs to the accelerometer loop PVR's, 20 vdc to the three accelerometer loop ac differential amplifier and interrogator modules and the associated binary current switches, and -20 vdc to the ac differential amplifier and interrogator module in the accelerometer loops.

The -20 vdc output is derived from the -28 vdc power supply by using a zener diode as a voltage divider and regulator. The output is regulated at $-20(\pm 0.8)$ vdc.

The 20 vdc output is derived from 28 vdc prime power by the use of a three transistor series regulator which maintains the output voltage at $20 (\pm 0.55)$ vdc.



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Figure 2-17. Pulse Torque Power Supply

The 120 vdc and 28 vdc PVR outputs are derived from a multivibrator, a power amplifier, and a rectifier and filter. A 12.8 kpps synchronizing pulse is received from the LGC through a buffer transformer in the pulse torque insulation transformer assembly and is applied to an amplifier-inverter. The output of the amplifier-inverter is applied to a multivibrator-chopper causing it to be synchronized at 6,400 cps. A transistorized time delay circuit is incorporated into the emitter circuits of the multivibrator to provide a turn on time delay of approximately 350 milliseconds. During the 90 second IMU turn on mode, 0 vdc is applied through the turn on circuits of the IMU auxiliary assembly module to the time delay circuit which inhibits the 120 vdc and

28 vdc PVR supplies. The multivibrator-chopper output is applied to the primary of a transformer which has 28 vdc prime power applied to its center tap. The secondary of the transformer, which is also center tapped, is coupled to a two stage push-pull power amplifier which operates from 28 vdc prime power. The output of the power amplifier consists of a transformer with four secondary windings; one with center tap return for the 120 vdc power supply, and one each for the X, Y, and Z accelerometer loop 28 vdc PVR supplies. The 120 vdc power supply consists of a full wave rectifier whose output is filtered, regulated, and again filtered. The 28 vdc power supplies are identical and consist of a full wave bridge rectifier whose output is filtered, regulated, and again filtered. The PVR time delay circuit inhibits the operation of the regulator in each 28 vdc PVR circuit to provide a six to eight second time delay in the 28 vdc PVR outputs.

2-4.6.2 -28 VDC Power Supply. The -28 vdc power supply provides input power to the three gimbal servo amplifiers in the stabilization loops and to the pulse torque power supply to generate -20 vdc for use in the accelerometer loops. The -28 vdc power supply consists of a pulse amplifier-inverter, a multivibrator-chopper, a power amplifier, and a rectifier and filter. (See figure 2-18.) The 25.6 kpps synchronization pulse input is amplified and inverted for use in synchronizing the multivibrator-chopper at 12.8 kcps. The multivibrator-chopper output is applied to the primary of a transformer which has 28 vdc prime power applied to its center tap. The secondary of the transformer, which is also center tapped, is coupled to a push-pull power amplifier. The output of the amplifier is transformer coupled to a full wave rectifier and filter whose positive side is referenced to ground to provide a -27.0 (± 1.0) vdc output.

2-4.6.3 800 CPS Power Supply. The 800 cps power supply (figure 2-19) consists of four modules: an automatic amplitude control, filter, and multivibrator; a 1 percent amplifier; and two 5 percent amplifiers. The 1 percent amplifier provides IMU gimbal resolver excitation, gimbal servo amplifier demodulator reference, and FDA1 and autopilot reference. The two 5 percent amplifiers provide gyro wheel excitation, IMU blower excitation, and accelerometer fixed heater power. The 1 percent amplifier also provides the input to one of the 5 percent amplifiers whose output is phase shifted -90 degrees. The output of this 5 percent amplifier is applied to the second 5 percent amplifier whose output is also phase shifted -90 degrees, or -180 degrees from the output of the 1 percent amplifier. The outputs of the 1 percent amplifier and the 5 percent amplifiers are applied to their respective loads through the IMU load compensation network which provides a power factor correction.

Zero and pi phase, 800 cps pulse trains from the LGC synchronize the multivibrator at 800 cps. In the absence of the synchronizing pulses, the multivibrator will free run at between 720 and 800 cps. The output of the multivibrator controls the operation of the chopper and filter circuit. The filtered chopper output is applied to the 1 percent amplifier. The output of the 1 percent amplifier, in addition to its direct uses, is a feedback signal to the automatic amplitude control circuit. The positive peaks of this feedback signal are detected and added to a dc reference signal. The sum is filtered and provides a dc bias to the multivibrator driven chopper. The bias controls the amplitude of the chopped signal.

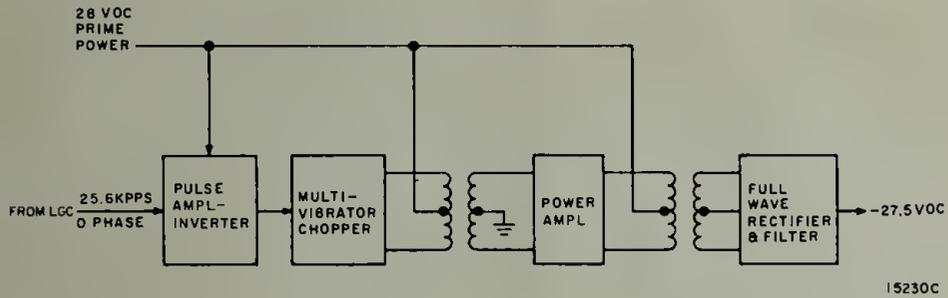


Figure 2-18. -28 VDC Power Supply

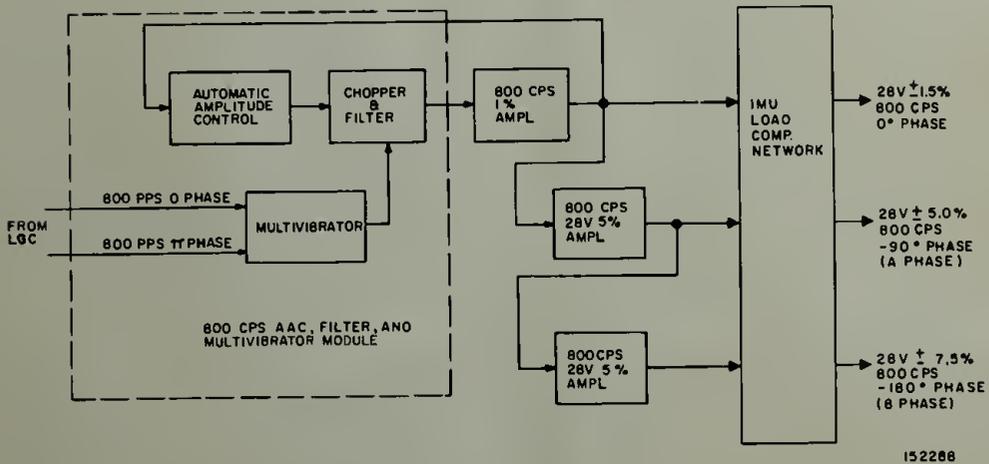


Figure 2-19. 800 CPS Power Supply

LEM PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM

The 1 percent amplifier is push-pull in operation with transformer coupled input and output and with overall voltage feedback for gain and distortion control.

The two 5 percent amplifiers are identical in operation. The amplifiers are push-pull and have transformer coupled inputs and outputs. The input transformer primary center tap is connected to the input signal low. The input signal high is applied directly to one side of the primary winding and is also applied through a phase shift network to the other, or out of phase, side of the primary. A feedback signal from the secondary of the output transformer is also applied to the out of phase side of the input transformer primary where it is mixed with the phase shifted portion of the input signal. This mixing results in a -90 degree phase shift in the secondary of the input transformer. The output of the first 5 percent amplifier is used as an input to the second 5 percent amplifier to provide an additional -90 degree phase shift.

2-4.6.4 3,200 CPS Power Supply. The 3,200 cps power supply provides excitation voltage for the signal generator and the magnetic suspension portions of the IRIG and PIP ducosyns. The 3,200 cps output is also used as a reference for the demodulator in the gimbal servo amplifiers.

The excitation voltage to the signal generators requires both voltage stability and phase stability. To accomplish this stability, the excitation voltage power transmission to the stable member is through a step down transformer on the stable member which reduces the slip ring current and, therefore, voltage drop effects due to slip ring, cable, and connector resistance. In addition, each wire connecting the output of the transformer to the input terminals of each PIP is cut to exactly the same length. The voltage level at the primary of the transformer is fed back to the power supply and is compared to a voltage reference.

The 3,200 cps power supply (figure 2-20) consists of an amplitude control module and a 1 percent power amplifier. The amplitude control module contains an automatic amplitude control circuit, a multivibrator, a chopper, and a filter.

The 3,200 pps pulse trains of zero degree phase and 180 degree phase synchronize a multivibrator. The output of the multivibrator controls the operation of the chopper circuit. The output of the chopper is applied to the 1 percent power amplifier. The 28 volt rms output of the amplifier is transmitted through the slip rings to the transformer on the stable member where the voltage is stepped down to 2 volts for the accelerometer ducosyns and 4 volts for the gyro ducosyns. A sample of the 28 volt level at the primary of the transformer is fed back through the slip rings to the input of the automatic amplitude control circuit. The positive peaks of the feedback signal are detected and added to a dc reference signal. The sum is filtered and provides a dc bias to the chopper circuit. The dc bias controls the amplitude of the chopper output to the filter.

2-5 LEM OPTICAL RENDEZVOUS SUBSYSTEM

This paragraph will give a functional description of the LORS and it will link the LORS operations to systems level operations. This paragraph will be supplied when information is available.

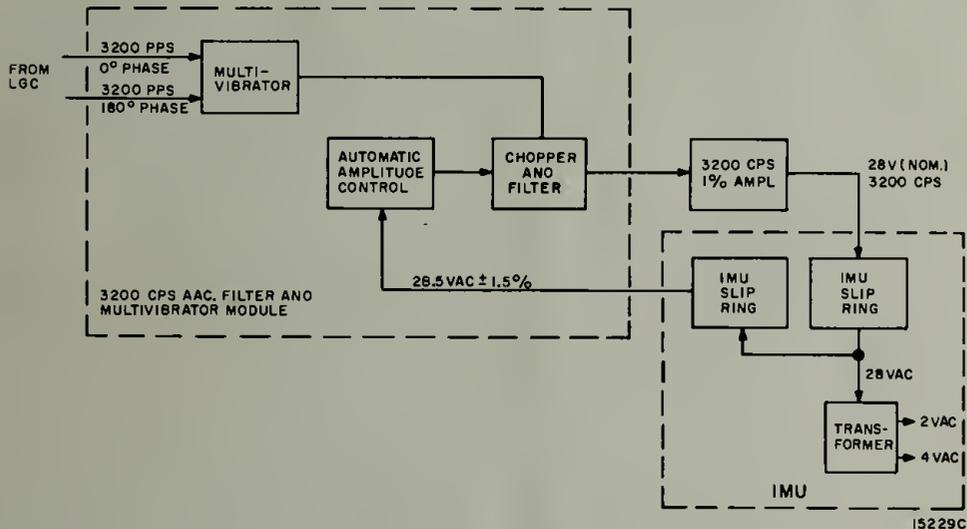
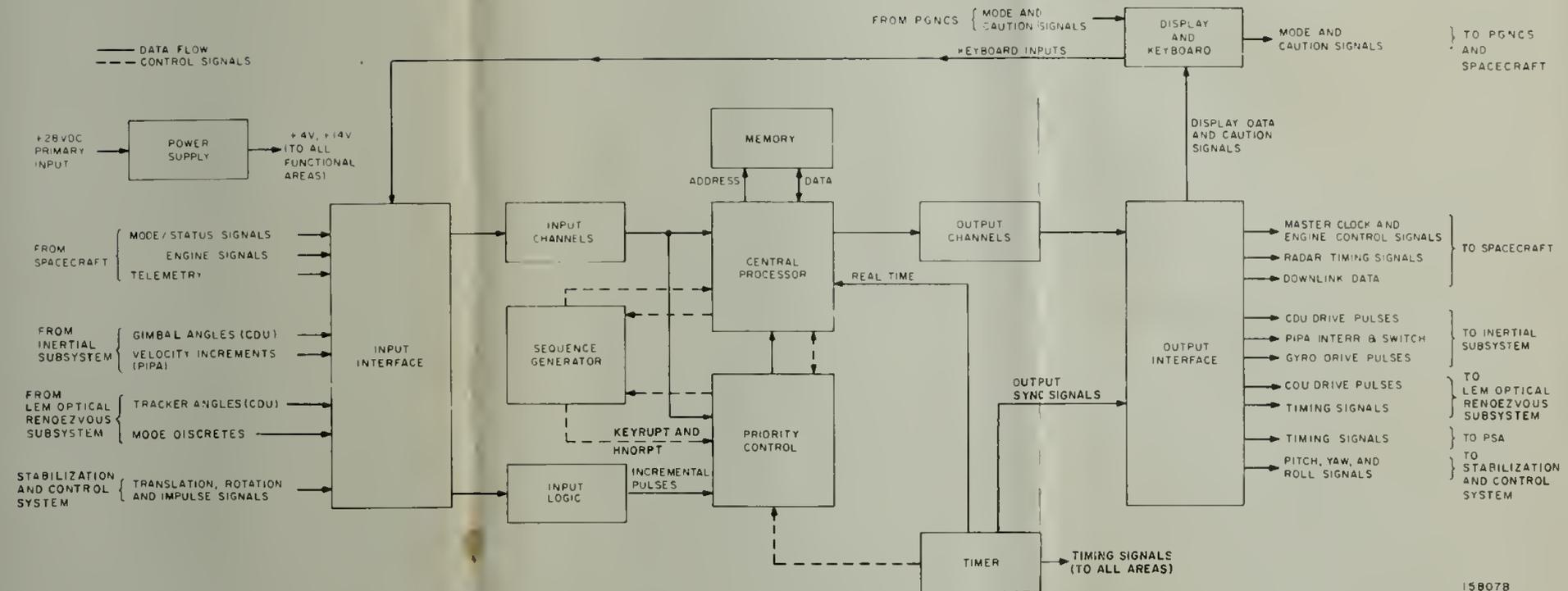


Figure 2-20. 3,200 CPS Power Supply

2-6 COMPUTER SUBSYSTEM

The computer subsystem (CSS) is the control and processing center of the PGNCs. It consists of the LGC and a DSKY. The CSS processes data and issues discrete outputs and control pulses to the PGNCs and other LEM systems. The LGC is a parallel digital control computer with many features of a general purpose computer. As a control computer, the LGC aligns the IMU, positions the optical tracker, and issues control commands to other LEM systems. As a general purpose computer, the LGC solves the guidance and navigation equations required for the LEM mission. In addition, the LGC monitors the operation of the LEM, including the CSS.

The main functions of the LGC (see figure 2-21) are implemented through the execution of the programs stored in memory. Programs are written in a machine language called basic instructions. A basic instruction contains an operation (order) code and a relevant address. The order code defines the data flow within the LGC, and the relevant address selects the data that is to be used for computations. The order code of each instruction is entered into the sequence generator, which controls data flow and produces a different sequence of control pulses for each instruction. Each instruction is followed by another instruction. In order to specify the sequence in which consecutive instructions are to be executed, the instructions are normally stored in successive memory locations. By adding the quantity one to the address of an instruction being executed, the address of the instruction to be executed next is derived. Execution of an instruction is complete when the order code of the next instruction is transferred to the sequence generator and the relevant address is in the central processor.



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Figure 2-21. Computer Subsystem, Block Diagram

The central processor consists of several flip-flop registers. It performs arithmetic operations and data manipulations on information accepted from memory, the input channels, and priority control. Arithmetic operations are performed using the ONE's complement number system. Values of 14 bits, excluding sign, (up to 28 bits during double precision operations) are processed with an additional bit produced for overflow or underflow. All operations within the central processor are performed under control of pulses generated by the sequence generator (indicated by dashed lines in figure 2-21). In addition, all words read out of memory are checked for correct parity, and a parity bit is generated within the central processor for all words written into memory. The LGC uses odd parity, that is, all words stored in memory contain an odd number of ONE's including the parity bit. The central processor also supplies data and control signals through the output channels and provides interface for the various spacecraft subsystems.

The LGC has provision for nine program interrupts. These interrupts are: T6 RUPT, T5 RUPT, T4 RUPT, T3 RUPT, KEYRUPT, UPRUPT, DOWNRUPT, RADAR, and HNRDPT. The T6 RUPT through T4 RUPT programs are initiated by the LGC. The DOWNRUPT program is initiated at the completion of every parallel-to-serial conversion for downlink operation. The remaining interrupt programs are initiated by external inputs to the LGC. The KEYRUPT programs are initiated when a DSKY pushbutton is depressed or when priority control receives a signal (discrete bit) from the optical tracker to indicate a sighting. The UPRUPT and RADAR programs are initiated when a complete UPLINK word (used for unmanned flights) is received. The HNRDPT program is initiated as soon as a hand controller is moved out of detent by the astronaut.

Before a priority program can be executed, the current program must be interrupted; however, certain information about the current program must be preserved. This information includes the program counter contents and any intermediate results contained in the central processor. The priority control produces an interrupt request signal, which is sent to the sequence generator. This signal, acting as an order code, causes the execution of an instruction that transfers the current contents of the program counter and any intermediate results to memory. In addition, the control pulses transfer the priority program address in priority control to the central processor, and then to memory through the write lines. As a result, the first basic instruction word of the priority program is entered into the central processor from memory, and execution of the priority program is begun. The last instruction of each priority program restores the LGC to normal operation, provided no other interrupt request is present, by transferring the previous program counter and intermediate results from their storage locations in memory back to the central processor.

Certain data pertaining to the flight of the LEM is used to solve the guidance and navigation problems required for the LEM mission. This data, which includes real time, acceleration, and IMU gimbal angles, is stored in memory locations called counters. The counters are updated as soon as new data becomes available. An incrementing process which changes the contents of the counters is implemented by

priority control between the execution of basic instructions. Data inputs to priority control are called incremental pulses. Each incremental pulse produces a counter address and a priority request. The priority request signal is sent to the sequence generator, where it functions as an order code. The control pulses produced by the sequence generator transfer the counter address to memory through the write lines of the central processor. In addition, the control pulses enter into the central processor the contents of the addressed counter to be incremented.

Real time plays a major role in solving guidance and navigation problems. Real time is maintained within the LGC in the main time counter of memory. The main time counter provides a 745.65 hour (approximately 31 days) clock. Incremental pulses are produced in the timer and sent to priority control for incrementing the main time counter. The LEM mission requires that the LGC clock be synchronized with the KSC clock. The LGC time is transmitted once every second by downlink operation for comparison with the KSC clock.

Incremental transmissions occur in the form of pulse bursts from the output channels to the CDU, the gyro fine align electronics, the RCS of the spacecraft, the optical tracker and the radar. The number of pulses and the time at which they occur are controlled by the LGC program. Discrete outputs also originate in the output channels under program control. These outputs are sent to the DSKY and various other subsystems. Continuous pulse trains originate in the timing output logic for synchronization of other systems.

The uplink word from the LEM telemetry system (unmanned flights) is supplied as an incremental pulse input to priority control. As this word is received, priority control produces the address of the uplink counter in memory and requests the sequence generator to execute the instructions which perform the serial-to-parallel conversion of the input word. When the serial-to-parallel conversion is completed, the parallel word is transferred to a storage location in memory by the uplink priority program. The uplink program also retains the parallel word for subsequent downlink transmission. Another program converts the parallel word to a coded display format and transfers the display information to the DSKY.

The downlink operation of the LGC is asynchronous with respect to the LEM telemetry system. The telemetry system supplies all the timing signals necessary for the downlink operation. These signals include start, end, and bit sync pulses.

Through the DSKY, the astronaut can load information into the LGC, retrieve and display information contained in the LGC, and initiate any program stored in memory. A keycode is assigned to each keyboard pushbutton. When a keyboard pushbutton on the DSKY is depressed, the keycode is produced and sent to an input channel. A signal is also sent to priority control, where it produces both the address of a priority program stored in memory and a priority request signal, which is sent to the sequence generator. This operation results in an order code and initiates an instruction for interrupting the program in progress and executing the KEYRUPT priority program stored in memory.

A function of this program is to transfer the keycode, temporarily stored in an input channel, to the central processor, where it is decoded and processed. A number of keycodes are required to specify an address, or a data word. The program initiated by a keycode also converts the information from the DSKY keyboard to a coded display format. The coded display format is transferred by another program to an output channel and sent to the display portion of the DSKY. The display notifies the astronaut that the keycode was received, decoded, and processed properly by the LGC.

2-6.1 PROGRAMS. An LGC program performs such functions as solving guidance and navigation problems, testing the operation of the PGNCS, and monitoring the operation of the LEM. Such a program consists of a group of program sections that are classified according to the functions they perform. These functions are defined as mission functions, auxiliary functions, and utility functions. (See figure 2-22.)

2-6.1.1 Mission Functions. Mission functions are performed by program sections that implement operations concerned with the major objectives of the LEM mission. These operations include erecting the IMU stable member and coarse aligning it to a desired heading prior to separating the LEM from the CSM and fine aligning it after separation. In addition, the mission functions include computation of spacecraft position and velocity during coasting periods of the flight by solution of second-order differential equations which describe the motions of a body subject to the forces of gravity.

2-6.1.2 Auxiliary Functions. Auxiliary functions are executed at the occurrence of certain events, requests, or commands. These functions are performed by program sections that provide a link between the LGC and other elements of the PGNCS. This link enables the LGC to process signals from various devices and to send commands for control and display purposes. In addition, the auxiliary functions implement many and varied operations within the LGC in support of the LEM mission functions.

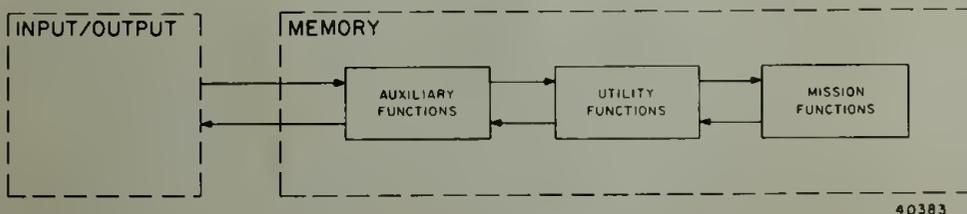


Figure 2-22. Program Organization

2-6.1.3 Utility Functions. Utility functions are performed by program sections that coordinate and synchronize LGC activities to guarantee orderly and timely execution of required operations. These functions control the operation of the LEM mission functions and schedule LGC operations on either a priority or a real-time basis. The utility functions also translate interpretive language to basic machine language which allows complex mathematical operations such as matrix multiplication, vector addition, and dot product computations to be performed within the framework of compact routines. In addition, the utility functions save the contents of registers A and Q during an interrupt condition and enable data retrieval and control transfer between isolated banks in the fixed-switchable portion of fixed memory.

2-6.2 MACHINE INSTRUCTIONS. The LGC has three classes of machine instructions: regular, involuntary, and peripheral (table 2-I). Regular instructions are programmed and are executed in whatever sequence they have been stored in memory. Involuntary instructions (with one exception) are not programmable and have priority over regular instructions. One involuntary instruction may be programmed to test computer operations. No regular instruction can be executed when the LGC forces the execution of an involuntary instruction. The peripheral instructions are used when the LGC is connected to the peripheral equipment. During the execution of any peripheral instruction, the LGC is in the monitor stop mode and cannot perform any program operation.

2-6.2.1 Regular Instructions. Four types of instructions comprise the regular instruction class. They are the basic, channel, extracode, and special instructions. Basic instructions are used most frequently. The instruction words stored in memory are called basic instruction words. They contain an order code field and an address field. Special instructions have predefined addresses and order codes; basic instructions have only predefined order codes. The special instructions are used to control certain operations in the LGC. For example, one special instruction is used to switch the LGC to the extend mode of operation. This mode extends the length of the order code field and converts basic instruction words to channel or extracode instruction words. Channel instructions can only be used with input-output channel addresses. Extra code instructions perform the more complex and less frequently used arithmetic operations.

Regular instructions can also be functionally subdivided into the following:

- (1) Sequence changing.
- (2) Fetching and storing.
- (3) Modifying.
- (4) Arithmetic and logic.
- (5) Input-output.
- (6) Editing.

Table 2-I. Instruction Classes

Class	Type	Control
Regular	Basic Extracode Channel Special	Program
Involuntary	Interrupt Counter	Priority
Peripheral	Keyboard Tape	Operator

The sequence changing instructions alter the sequence in which the instructions stored in memory are executed. One group, called transfer control instructions, changes the program path as defined by the programmer. The other group, called decision making instructions, branches to alternate program paths in response to predefined conditions.

The fetching and storing instructions move data, without alteration, from one location to another. One group, called copy instructions, provides a non-destructive transfer of data from memory to the central processor. Another group, called exchange instructions, transposes data between memory and the central processor. One instruction provides a nondestructive transfer of data from the central processor to memory.

The modifying instructions alter the next instruction to be executed by changing the contents of the order code field, address field, or both.

The arithmetic and logic instructions perform numerical computations. One group, called the basic arithmetic instructions, performs addition, subtraction, multiplication, and division in the ONE's complement number system. Another group, called the add and store instructions, performs single or double precision addition and transfers the resultant from the central processor to memory. The incrementing instructions increment a signed quantity, increment its absolute value, or diminish its absolute value by one. One instruction performs subtraction in the TWO's complement number system for angular data and one instruction performs the Boolean AND operation.

The input-output or channel instructions link the interface circuits to the central processor. One group, called read instructions, transfers the total or partial contents of any channel (register) location to the central processor either directly or accompanied by the Boolean AND, OR, or EXCLUSIVE OR operation. Another group of instructions transfers all new or partially new information to any channel location in the same manner.

The editing or special instructions are address-dependent and control the operation of the program. One special instruction, as mentioned previously, controls the extend mode of operation. Other instructions prevent a program from being interrupted or shift and cycle data to the left or right.

2-6.2.2 Involuntary Instructions. Involuntary instructions contain two types of instructions: interrupt and counter. The interrupt instructions use the basic instruction word format just as the regular instructions do; however, the interrupt instructions are not entirely programmable. The contents of the order code field and the address field are supplied by computer logic rather than the program. The counter instructions have no instruction word format. Signals which function as a decoded order code specify the counter instruction to be executed and the computer logic supplies the address. The address for these instructions is limited to one of 29 counter locations in memory.

There are two interrupt instructions. One instruction initializes the LGC when power is first applied and when certain program traps occur. The other interrupt instruction is executed at regular intervals to indicate time, receipt of new telemetry or keyboard data, or transmission of data by the LGC. This interrupt instruction may be programmed to test the computer.

There are several counter instructions. Two instructions will either increment or decrement by one the content of the counter location using the ONE's complement number system. Two other instructions perform the same function using the TWO's complement number system. Certain counter instructions control output rate signals and convert serial telemetry data to parallel computer data.

2-6.2.3 Peripheral Instructions. There are two types of peripheral instructions. One type deals with memory locations and the other type deals with channel locations. The peripheral instructions are not used when the LGC is in the LEM. They are used when the computer is connected to peripheral equipment during subsystem and preinstallation system testing. The peripheral instructions are not programmable and are executed when all computer program operations have been forcibly stopped. These instructions are used to read and load any memory or channel location and to start the computer program at any specified address. The peripheral instructions and counter instructions are processed identically.

2-6.3 TIMER. The timer generates the timing signals required for operation of the LGC and is the primary source of timing signals for all LEM systems.

The timer is divided into the areas indicated in figure 2-23. The master clock frequency is generated by an oscillator and is applied to the clock divider logic. The divider logic divides the master clock input into gating and timing pulses at the basic clock rate of the computer. Several outputs are available from the scaler, which further divides the divider logic output into output pulses and signals which are used for gating, for generating rate signal outputs, and for accumulating time. Outputs from the divider logic also drive the time pulse generator which produces a recurring set of time pulses. This set of time pulses defines a specific interval (memory cycle time) in which access to memory and word flow take place within the computer.

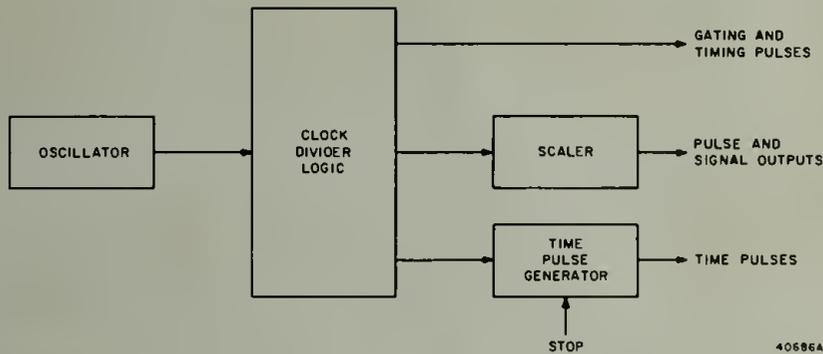


Figure 2-23. Timer, Block Diagram

The start-stop logic senses the status of the power supplies and specific alarm conditions in the computer and generates a stop signal which is applied to the time pulse generator to inhibit word flow. Simultaneous with the generation of the stop signal, a fresh start signal is generated which is applied to all functional areas in the computer. The start-stop logic and subsequent word flow in the computer can also be controlled by inputs from the Computer Test Set (CTS) during pre-installation systems and sub-system tests.

2-6.4 SEQUENCE GENERATOR. The sequence generator executes the instructions stored in memory. The sequence generator processes instruction codes and produces control pulses which regulate the data flow of the computer. The control pulses are responsible for performing the operations assigned to each instruction in conjunction with the various registers in the central processor and the data stored in memory.

The sequence generator (figure 2-24) consists of the order code processor, command generator, and control pulse generator. The sequence generator receives order code signals from the central processor and priority control. These signals are coded by the order code processor and supplied to the command generator. The special purpose control pulses are used for gating the order code signals into the sequence generator at the end of each instruction.

The command generator receives instruction signals from priority control and peripheral equipment and receives coded signals from the order code processor. The command generator decodes the input signals and produces instruction commands which are supplied to the control pulse generator.

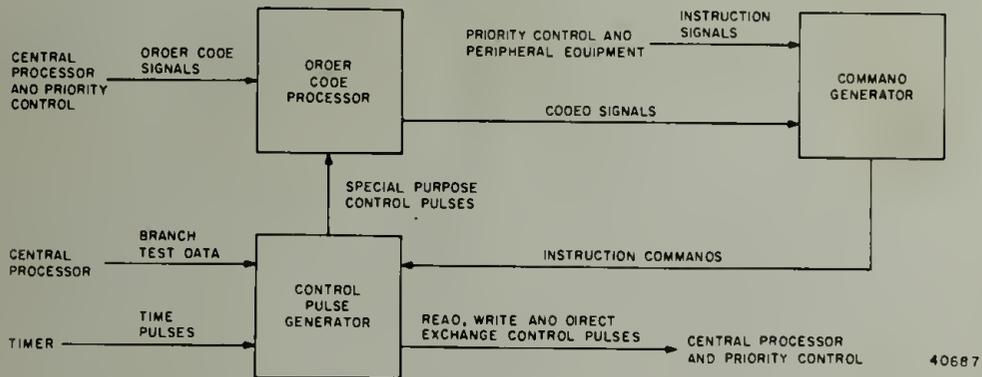


Figure 2-24. Sequence Generator, Block Diagram

The control pulse generator receives twelve time pulses from the timer. These pulses occur in cycles and are used for producing control pulses in conjunction with the instruction commands. There are five types of control pulses: read, write, test, direct exchange, and special purpose. Information in the central processor is transferred from one register to another by the read, write, and direct exchange control pulses. The special purpose control pulses regulate the operation of the order code processor. The test control pulses are used within the control pulse generator. The branch test data from the central processor changes the control pulse sequence of various instructions.

2-6.5 CENTRAL PROCESSOR. The central processor, figure 2-25, consists of the flip-flop registers, the write, clear, and read control logic, write amplifiers, memory buffer register, memory address register, and decoder and the parity logic. All data and arithmetic manipulations within the LGC take place in the central processor.

Primarily, the central processor performs operations indicated by the basic instructions of the program stored in memory. Communication within the central processor is accomplished through the write amplifiers. Data flows from memory to the flip-flop registers or vice-versa, between individual flip-flop registers, or into the central processor from external sources. In all instances, data is placed on the write lines and routed to a specific register or to another functional area under control of the write, clear, and read logic. This logic section accepts control pulses from the sequence generator and generates signals to read the content of a register onto the write lines and to write this content into another register of the central processor or to another functional area of the LGC. The particular memory location is specified by the content of the memory address register. The address is fed from the write lines into this register, the output of which is decoded by the address decoder logic. Data is subsequently transferred from memory to the memory buffer register. The decoded address outputs are also used as gating functions within the LGC.

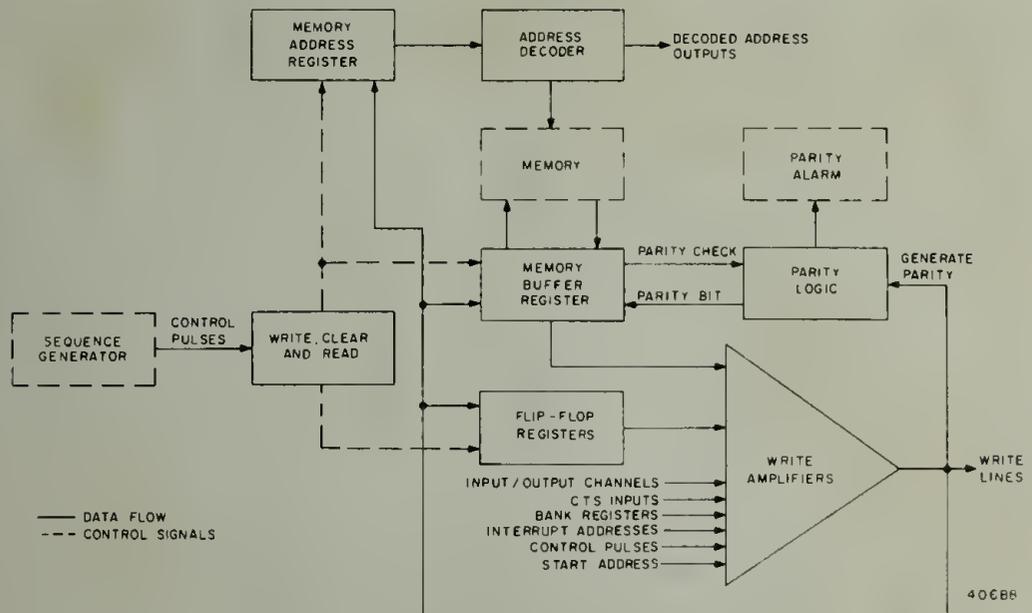


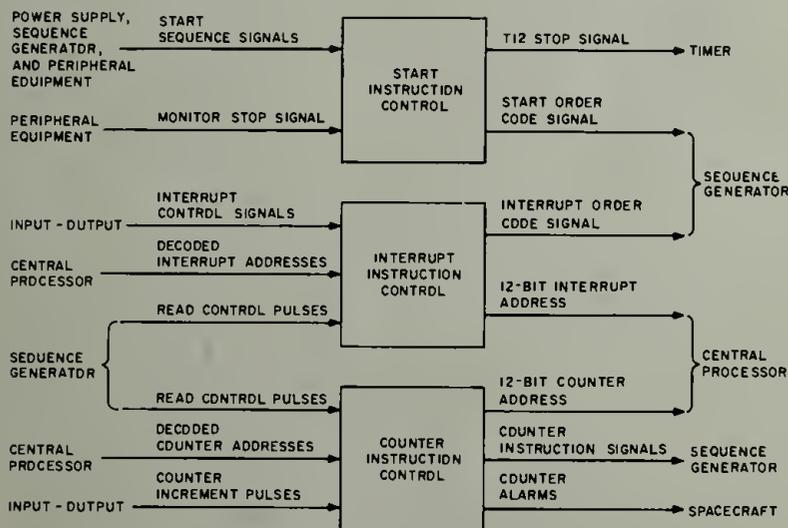
Figure 2-25. Central Processor, Block Diagram

The memory buffer register buffers all information read out or written into memory. During readout, parity is checked by the parity logic and an alarm is generated in case of incorrect parity. During write-in, the parity logic generates a parity bit for information being written into memory. The flip-flop registers perform the data manipulations and arithmetic operations. Each register is 16 bits or one computer word in length. Data flows into and out of each register as dictated by control pulses associated with each register. The control pulses are generated by the write, clear, and read control logic.

External inputs through the write amplifiers include the content of both the erasable and fixed memory bank registers, all interrupt addresses from priority control, control pulses which are associated with specific arithmetic operations, and the start address for an initial start condition. Information from the input and output channels is placed on the write lines and routed to specific destinations either within or external to the central processor. The CTS inputs allow a word to be placed on the write lines during system and subsystem tests.

2-6.6 PRIORITY CONTROL. Priority control is related to the sequence generator in that it controls all involuntary or priority instructions. The priority control processes input-output information and issues order code and instruction signals to the sequence generator and issues twelve-bit addresses to the central processor.

The priority control (figure 2-26) consists of the start, interrupt, and counter instruction control circuits. The start instruction control initializes the computer if the program works itself into a trap, if a transient power failure occurs, or if the interrupt instruction control is not functioning properly. The computer is initialized with the start order code signal, which not only forces the sequence generator to execute the start instruction, but also resets many other computer circuits. When the start order code signal is being issued, the T12 stop signal is sent to the timer. This signal stops the time pulse generator until all essential circuits have been reset and the start instruction has been forced by the sequence generator. The computer may also be initialized manually when connected to the peripheral equipment and placed into the monitor stop mode. In this mode, the time pulse generator is held at the T12 position until the monitor stop signal is released.



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Figure 2-26. Priority Control, Block Diagram

The interrupt instruction control can force the execution of the interrupt instruction by sending the interrupt order code signal to the sequence generator and the twelve bit address to the central processor. There are ten addresses, each of which accounts for a particular function that is regulated by the interrupt instruction control. The interrupt instruction control links the keyboard, telemetry, and time counters to program operations. The interrupt addresses are transferred to the central processor by read control pulses from the sequence generator. The source of the keyboard, telemetry, and time counter inputs is the input-output circuits. The interrupt instruction control has a built-in priority chain which allows sequential control of the ten interrupt addresses. The decoded interrupt addresses from the central processor are used to control the priority operation.

The counter instruction control is similar to the interrupt instruction control in that it links input-output functions to the program. It also supplies twelve-bit addresses to the central processor and instruction signals to the sequence generator. The instruction signals cause a delay (not an interruption) in the program by forcing the sequence generator to execute a counter instruction. The addresses are transferred to the central processor by read control pulses. The counter instruction control also has a built-in priority of the 29 addresses it can supply to the central processor. This priority is also controlled by decoded counter address signals from the central processor. The counter instruction control contains an alarm detector which produces an alarm if an incremental pulse is not processed properly.

2-6.7 INPUT-OUTPUT. The input-output section accepts all inputs to, and routes to other systems all outputs from, the computer. The input-output section (figure 2-27) includes the interface circuits, input and output channels, input logic, output timing logic, and the downlink circuits.

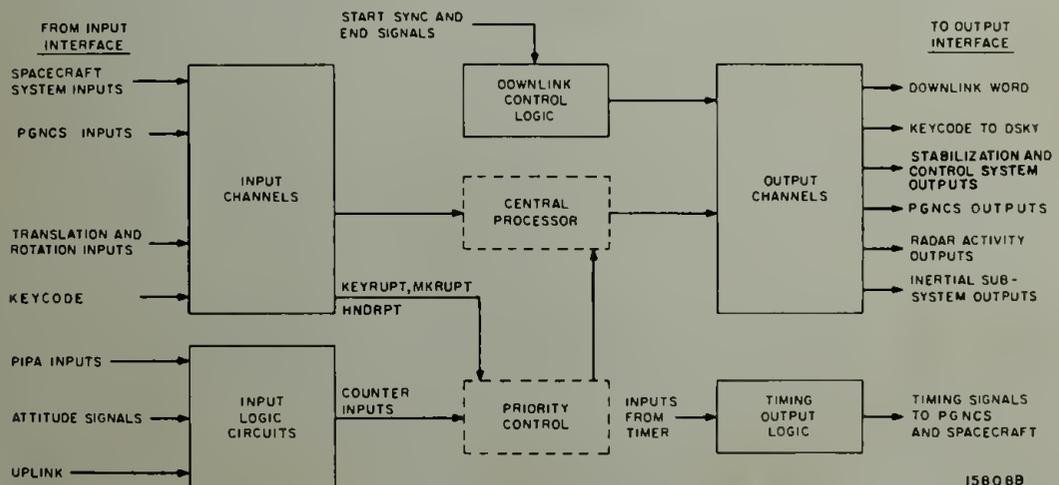


Figure 2-27. Input-Output, Block Diagram

Most of the input and output channels are flip-flop registers similar to the flip-flop registers of the central processor. Certain discrete inputs are applied to individual gating circuits which are part of the input channel structure. Typical inputs to the channels include keycodes from the DSKY and signals from the PGNCS proper and other LEM systems. Input data is applied directly to the input channels; there is no write process as in the central processor. However, the data is read out to the central processor under program control. The input logic circuits accept inputs which cause interrupt sequences within the computer. These incremental inputs (acceleration data from the PIPA's, et cetera) are applied to the priority control circuits and subsequently to associated counters in erasable memory.

Outputs from the computer are placed in the output channels and are routed to specific systems through the output interface circuits. The operation is identical to that in the central processor. Data is written into an output channel from the write lines and read out to the interface circuits under program control. Typically, these outputs include outputs to the stabilization and control system, the DSKY, the PGNCS, et cetera. The downlink word is also loaded into an output channel and routed to the LEM spacecraft telemetry system by the downlink circuits.

The output timing logic gates synchronization pulses (fixed outputs) to the PGNCS and the LEM spacecraft. These are continuous outputs since the logic is specifically powered during normal operation of the computer and during standby.

2-6.8 MEMORY. Memory (figure 2-28) consists of an erasable memory with a storage capacity of 2048 words and a fixed core rope memory with a storage capacity of 36,864 words. Erasable memory is a random-access, destructive-readout storage device. Data stored in erasable memory can be altered or updated. Fixed memory is a nondestructive storage device. Data stored in fixed memory is unalterable since the data is wired in and readout is nondestructive.

Both memories contain magnetic-core storage elements. In erasable memory, the storage elements form a core array; in fixed memory, the storage elements form three core ropes. Erasable memory has a density of one word per 16 cores; fixed memory has a density of eight words per core. Each word is located by an address.

In fixed memory, addresses are assigned to instruction words to specify the sequence in which they are to be executed; blocks of addresses are reserved for data, such as constants and tables. Information is placed into fixed memory permanently by weaving patterns through the magnetic cores. The information is written into assigned locations in erasable memory with the CTS, the DSKY, uplink, or program operation.

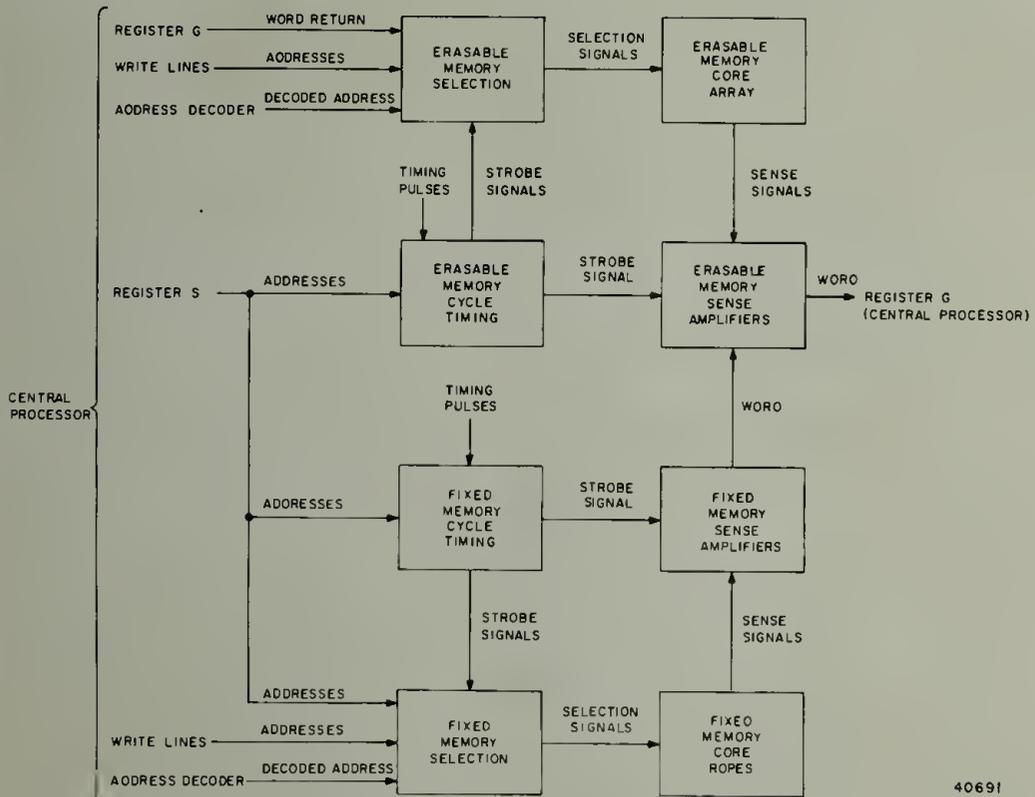


Figure 2-28. Memory, Block Diagram

Both memories use a common address register (register S) and an address decoder in the central processor. When register S contains an address pertaining to erasable memory, the erasable memory cycle timing is energized. Timing pulses sent to the erasable memory cycle timing then produce strobe signals for the read, write, and sense functions. The erasable memory selection logic receives an address and a decoded address from the central processor and produces selection signals which permits data to be written into or read out of a selected storage location. When a word is read out of a storage location in erasable memory, the location is cleared. A word is written into erasable memory through the memory buffer register (register G) in the central processor by a write strobe operation. A word read from a storage location is applied to the sense amplifiers. The sense amplifiers are strobed and the information is entered into register G of the central processor. Register G receives information from both memories.

The address in register S energizes the fixed memory cycle timing when a location in fixed memory is addressed. The timing pulses sent to the fixed memory cycle timing produce the strobe signals for the read and sense functions. The selection logic receives an address from the write lines, a decoded address and addresses from register S, and produces selection signals for the core rope. The content of a storage location in fixed memory is strobed from the fixed memory sense amplifiers to the erasable memory sense amplifiers and then entered into register G of the central processor.

2-6.9 POWER SUPPLIES. The two power supplies (figure 2-29) furnish operating voltages to the LGC and the DSKY. Primary power of 28 vdc from the spacecraft is applied to both power supplies. Regulator circuits maintain a constant output of +4 volts and +4 volts switched from one supply, and +14 volts and +14 volts switched from the other. The regulator circuits are driven by a sync signal input from the timer, each power supply having a different sync frequency. During system and subsystem tests, inputs from the CTS can be used to simulate power supply failures.

The standby mode of operation is initiated by pressing the standby (STBY) pushbutton on the DSKY. During standby, the LGC is put into a RESTART condition and the switchable +4 and +14 voltages are switched off, thus putting the LGC into a low power mode where only the timer and a few auxiliary signals are operative.

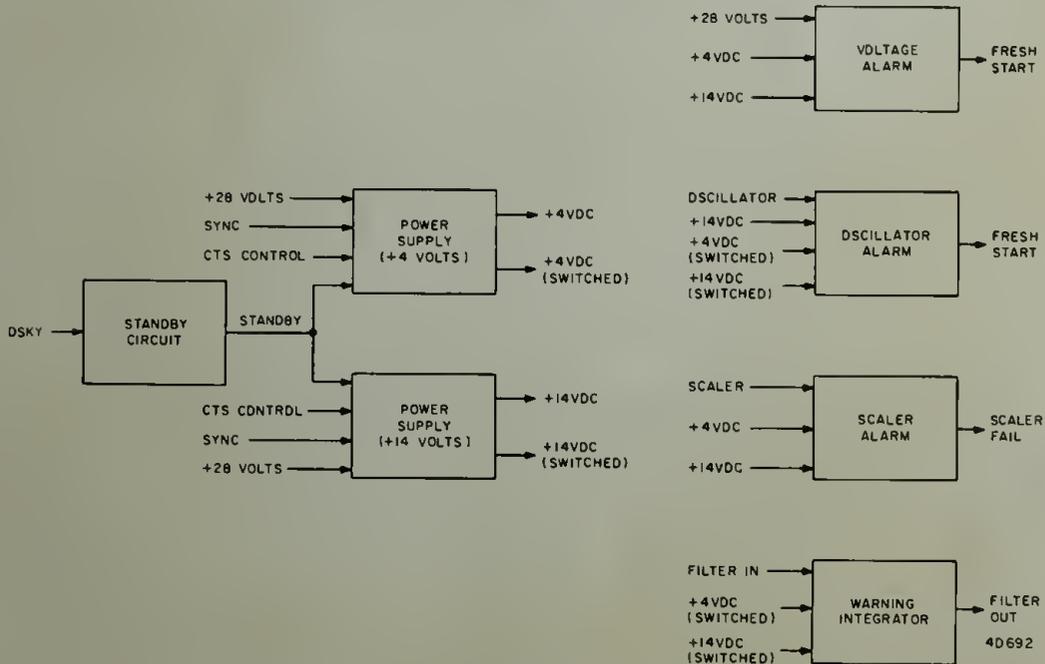
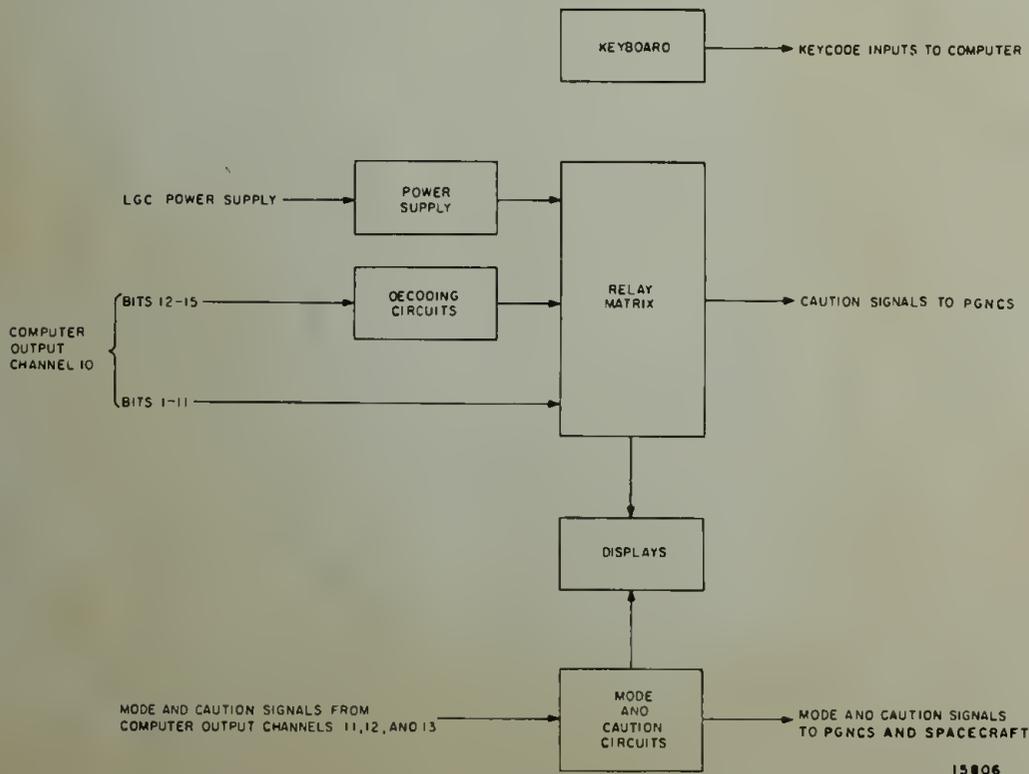


Figure 2-29. Power Supplies, Block Diagram

The voltage alarm circuits monitor the +28, +14, and +4 volt outputs and produce an LGC restart signal (Fresh Start) should any of the voltages deviate from nominal by more than a predetermined amount. The oscillator alarm produces an LGC restart signal (Fresh Start) if the oscillator fails or if the LGC is in the standby mode. The scaler alarm circuit monitors the scaler output of the timer and generates a fail signal if the scaler output fails. The warning integrator monitors certain operations and generates an LGC warning signal (Filter Out) if these operations are frequently repeated or prolonged.

2-6.10 DISPLAY AND KEYBOARD. The DSKY is located below the center panels of the cockpit display and control panels.

The DSKY (figure 2-30) consists of a keyboard; a relay matrix with associated decoding circuits; and a power supply. The keyboard, which contains several numerical, sign, and other control keys, allows the astronaut to communicate with the LGC. The inputs from the keyboard are entered into an input channel and processed by the LGC.



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Figure 2-30. Display and Keyboard (DSKY), Block Diagram

The inputs entered from the keyboard, as well as other information, appear on the displays after processing by program. The display of information is accomplished through the relay matrix. A unique code for the characters to be displayed is formed by fifteen bits from output channel 10 in the LGC. Bits 12 through 15 are decoded by the decoding circuits, and, along with bits 1 through 11, energize specific relays in the matrix which causes the appropriate characters to illuminate. The information displayed is the result of a keycode punched in by the astronaut, or is computer-controlled information. The display characters are formed by electroluminescent segments which are energized by a voltage from the power supply routed through relay contacts. Specific inputs from the PGNCs are also applied, through the LGC to certain relays in the matrix through output channel 10 of the LGC. The resulting relay-controlled outputs are caution signals to the PGNCs.

The mode and caution circuits accept direct input signals from channels 11, 12, and 13, without being decoded. The resulting outputs can give an indication to the astronaut on the DSKY and route the output signal to the PGNCs and spacecraft.

Chapter 3

PHYSICAL DESCRIPTION

3-1 SCOPE

This chapter describes the physical characteristics of the components which comprise the LEM PGNCS. The PGNCS components and their locations within the LEM are listed in table 3-I and illustrated in figure 3-1. The locations of PGNCS component modules are also illustrated and the module functions described.

3-2 PGNCS INTERCONNECT HARNESS

The PGNCS interconnect harness (composed of harnesses A and B) interconnects the components of the PGNCS and provides the electrical interface between the PGNCS and other LEM systems. The IMU and PTA are interconnected by harness B. Harness A interconnects the PSA, CDU, LGC, and signal conditioner. The two harnesses are connected to each other by vehicle cables. Table 3-II lists the harness connectors and the components or cable to which they are mated.

Table 3-I. LEM PGNCS Components

Component	Part Number	Location
CDU	2007222-041	Mounted on coldplate on center section of after crew compartment wall.
PGNCS interconnect harness	6014515-011	
Harness A	6014506	Attached to rear wall of after crew compartment
Harness B	6014507	Located in IMU compartment.

(Sheet 1 of 2)

Table 3-I. LEM PGNCs Components

Component	Part Number	Location
IMU and PTA	6007001-011	Bolted to after end of nav base. Mounted on coldplate on LEM structure immediately aft of IMU/nav base complex.
IMU	2018601-011	
PTA	6007000-011	
LEM guidance computer group	6003001-021	Mounted to front wall of crew compartment below LEM display and control panel. Mounted on coldplate on upper section of after crew compartment wall above CDU.
DSKY	2003985-031	
LGC	2003100-021	
Luminous beacon		Mounted on coldplate on CSM on upper bulkhead of service module.
Nav base	6899950-011	Bolted to LEM structure in unpressurized compartment above astronauts' heads.
Optical tracker		Bolted to forward end of nav base and extending outside LEM.
PSA	6007200-011	Mounted on coldplate on lower section of after crew compartment wall below CDU.
Signal conditioner		Attached to top of PSA.

(Sheet 2 of 2)

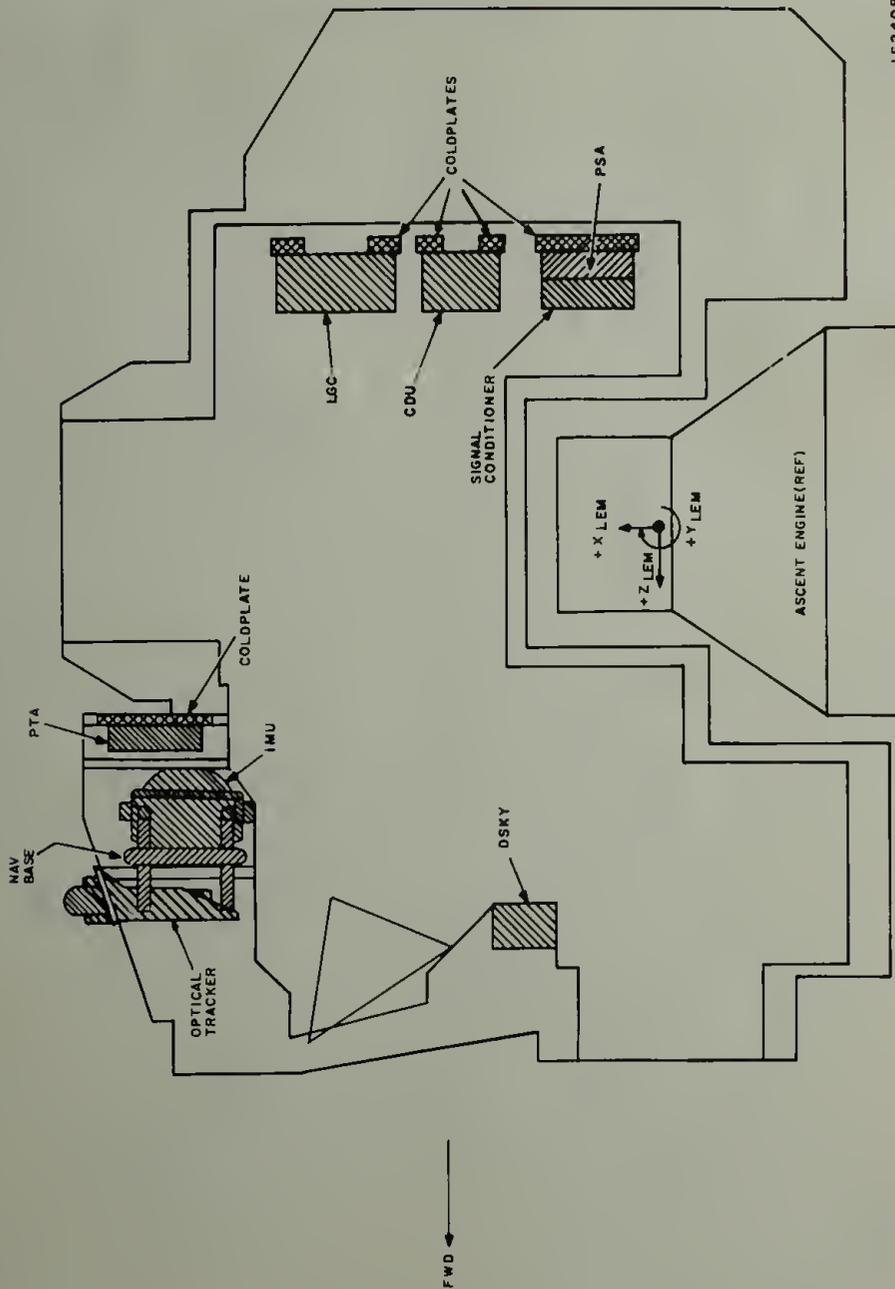


Figure 3-1. Location of LEM PGNC Components

Table 3-II. PGNCS Harness Interconnections

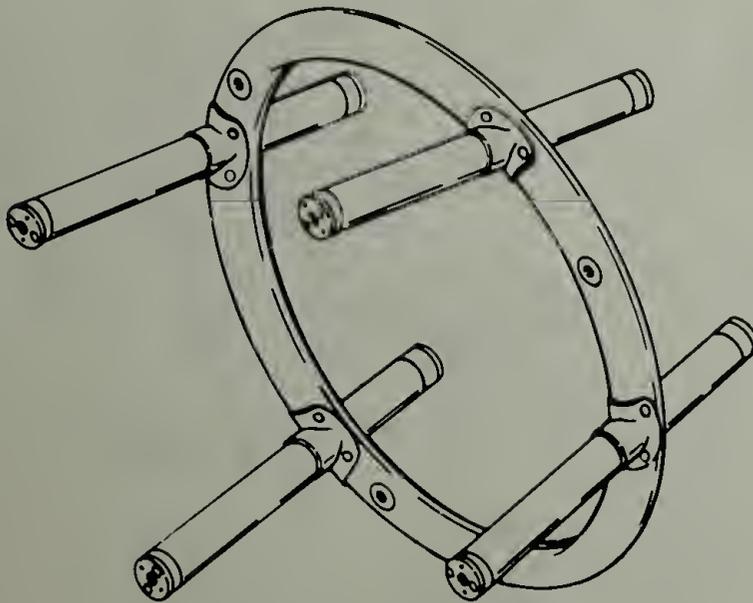
PGNCS Harness Connector	Component	Component Connector
<u>Harness A</u>		
56P1	Signal conditioner	-
56P2	PSA	45J19
56P3	CDU	40J53
56P4	LGC	05A1J51
56P5	LEM spacecraft harness	J221
56P6	LEM spacecraft harness	J220
56P7	LEM spacecraft harness	J219
56P8	LEM spacecraft harness	J222
56P9	LEM spacecraft harness	J218
56P10	LEM spacecraft harness	J217
56P11	LEM spacecraft harness	J223
56P12	LEM spacecraft harness	J224
56P13	LEM spacecraft harness	J215
56P14	LEM spacecraft harness	J216
<u>Harness B</u>		
56P15	LEM spacecraft harness	J226
56P16	LEM spacecraft harness	J227
56P17	LEM spacecraft harness	J228
56P18	LEM spacecraft harness	J225
56P19	PTA	35A2J19
56P20	IMU	35A1J2
56P21	IMU	35A1J1
56J1	LEM spacecraft harness	P230

3-3 NAVIGATION BASE ASSEMBLY

The navigation base assembly (nav base), figure 3-2, is a lightweight mount which supports, in critical alignment, the IMU and optical tracker. The nav base, constructed of one inch diameter, aluminum alloy tubing, weighs approximately three pounds. It consists of a center ring supporting four legs which extend from either side. The ring is approximately 14 inches in diameter and each of the four legs is approximately ten inches long. The IMU is mounted to the ends of the four legs on one side of the ring, and the optical tracker is mounted to the opposite ends of the legs. The nav base is bolted to the LEM structure above the astronauts' heads by three mounting pads on the center ring.

3-4 INERTIAL MEASURING UNIT

The IMU (figure 3-3) is a three gimbal system designed for movement of the LEM about all axes of the gyro-stabilized inner gimbal (stable member). To provide lightweight, rigid construction, the stable member is machined from a beryllium block and the gimbals are constructed of an aluminum alloy. The weight of the IMU is approximately 42 pounds, and the gimbal case is approximately 12.5 inches in diameter.



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Figure 3-2. Navigation Base Assembly

Three Apollo II IRIG's hold the stable member in a stabilized condition. Accelerations along any component of any of the three orthogonal axes of the stable member are sensed by one or more of the three 16 PIP accelerometers. Intergimbal assemblies physically support the gimbals and pass electrical signals between them. The temperature of the IMU is maintained at the desired level by a system of heaters, blowers, and coolant passages. The IMU is pressurized to aid in convection cooling.

3-4.1 STABLE MEMBER. The stable member, or inner gimbal, is suspended by two intergimbal assemblies inside the middle gimbal. It is free to rotate without restriction about the inner gimbal (IG) axis. Holes are machined in the beryllium block to receive the three Apollo II IRIG's and three 16 PIP's. Accelerometer preamplifiers, stable member heaters, temperature control circuitry and thermostats, a ducosyn transformer, and two safety thermostats are all attached to the stable member.

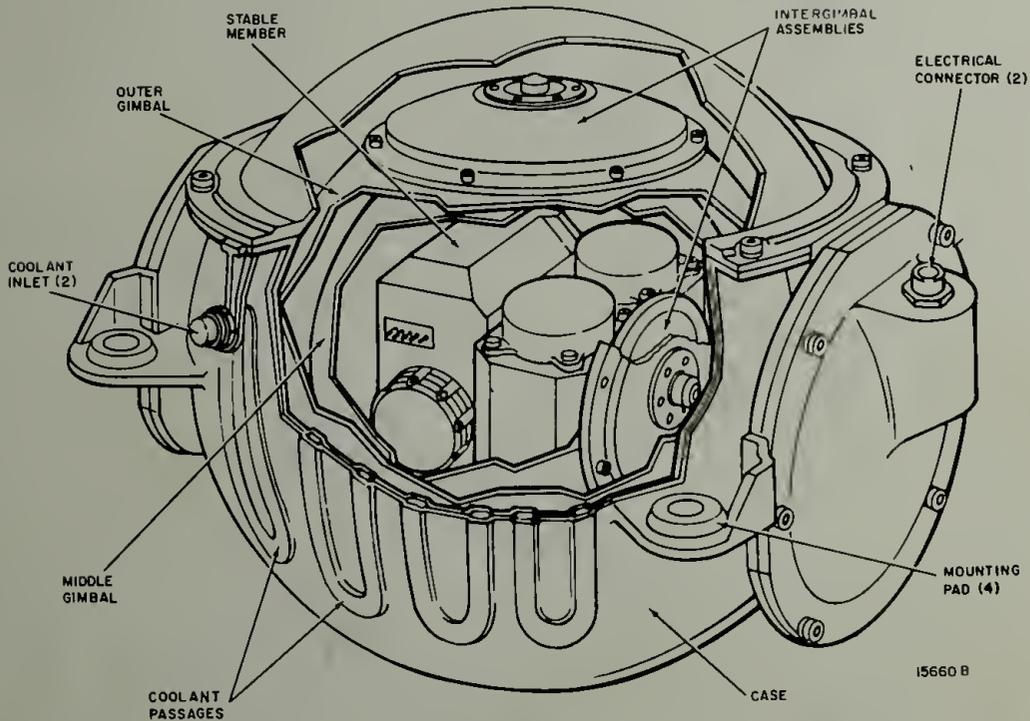


Figure 3-3. Inertial Measuring Unit

3-4.1.1 Gyroscopes. The three gyroscopes (gyros) on the stable member are Apollo II IRIG types. Figure 3-4 shows the location of the gyros on the stable member.

Ducosyns are used for magnetic suspension of the gyro rotor and for signal and torque generation. The signal generator ducosyn is located at one end of the float; the torque generator ducosyn is located at the other end.

The gyro wheel assembly operates as a hysteresis synchronous motor. The hub of the wheel is made of beryllium and the rim is made of heavy steel. This method of construction concentrates the weight at the rim, giving the wheel a high inertial moment.

3-4.1.2 Accelerometers. The LEM IMU uses three 16 PIP devices for sensing acceleration. Figure 3-4 shows the orthogonal placement of the 16 PIP's on the stable member. The 16 PIP is basically a cylindrical float with a pendulous mass unbalance and is pivoted with respect to a case. Ducosyns are located at each end of the float for magnetic suspension and signal and torque generation.

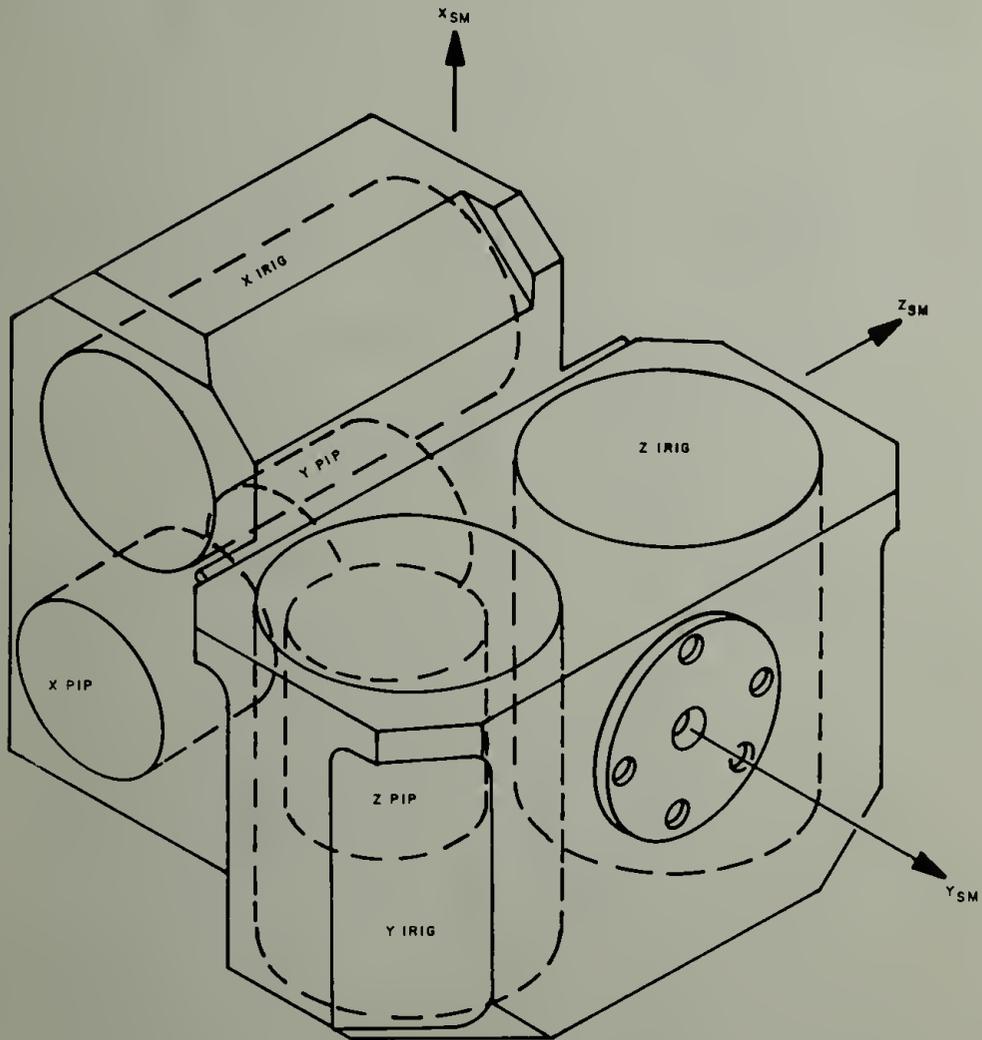
3-4.1.3 Stable Member Mounted Electronics. Table 3-III gives the locations and functions of electronics modules which are mounted in the IMU.

3-4.2 MIDDLE GIMBAL. The middle gimbal is suspended by two intergimbal assemblies inside the outer gimbal. It, in turn, supports the stable member. Slip ring assemblies in the intergimbal assemblies provide a means of carrying electrical signals between the outer gimbal and the stable member.

3-4.3 OUTER GIMBAL. The outer gimbal is similar in configuration to the middle gimbal, being suspended inside the supporting gimbal, or case, by two intergimbal assemblies. The outer gimbal has two thermostatically controlled axial-flow blowers mounted in its walls to force air from the vicinity of the middle gimbal to the walls of the case, where heat is carried away by a coolant solution circulating through passages in the case.

3-4.4 SUPPORTING GIMBAL. The supporting gimbal (case) is a spherical enclosure which supports the three gimbals described in the preceding paragraphs. The outer gimbal is suspended inside the case by two intergimbal assemblies which allow complete freedom of rotation. The walls of the case contain coolant passages through which a water-glycol solution is circulated to dissipate heat generated by inertial components and electronic modules. Two quick-disconnect fittings connect the coolant passages to the LEM coolant supply. The case is surrounded by insulating material to prevent condensation of moisture on the coolant passages.

Electrical interface between the IMU and the remainder of the PGNCS is accomplished by two electrical connectors on the case. A precision resolver alignment assembly module and a blower control relay are mounted on the resolver inter-gimbal assembly of the outer gimbal. Their functions are described in table 3-III. The resolver alignment assembly is accessible from outside the case.



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Figure 3-4. IMU Stable Member

Table 3-III. Locations and Functions of IMU Electronics

Module or Component	Part Number	Location and Function
Blower control module assembly	2007171-011	Stable member (SM): Removes power from blower control relay in response to request from blower control thermostat.
Blower control thermostat and heater assembly	2018635	SM: Controls on-off action of blower motors on outer gimbal.
Temperature control module assembly	2007064-011	SM: Applies power to gyro, accelerometer, and stable member heaters in response to request from temperature control thermostat.
Temperature control thermostat and heater assembly	2018637	SM: Controls operation of temperature control module to maintain proper heat in inertial components.
Stable member heater assembly (2)	2018641	SM: Supplement heat generated by inertial component heaters.
Safety thermostat (2)	1001485	SM: Disable all IMU heaters in the event of an extreme overheat condition.
Temperature alarm module assembly	2007170-011	SM: Signals LGC that an overheat or underheat condition is present.
Temperature alarm thermostat assembly	2018636	SM: Controls operation of temperature alarm module assembly.
Ducosyn transformer assembly	2007019-011	SM: Reduces 28 vac to 2 volts and 4 volts for signal generator excitation of accelerometer and gyro ducosyns, respectively.
PIP preamplifier assembly (3)	2007060-011	SM: Amplifies signals generated by accelerometer signal generator. Also provides 45 degree phase shift from reference voltage.

(Sheet 1 of 2)

Table 3-III. Locations and Functions of IMU Electronics

Module or Component	Part Number	Location and Function
Precision resolver alignment assembly	2007001-011	Outer gimbal resolver intergimbal assembly: Compensates for design anomalies in intergimbal assembly resolvers.
Blower control relay	1010353-10	Outer gimbal resolver intergimbal assembly: Applies power to blower motors at request of blower control module assembly.

(Sheet 2 of 2)

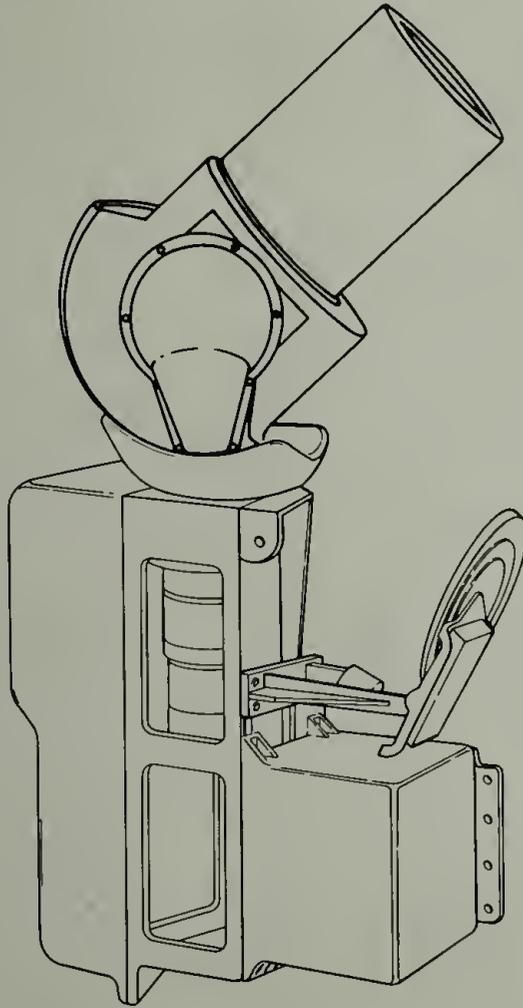
3-4.5 INTERGIMBAL ASSEMBLIES. The intergimbal assemblies serve five basic purposes: the duplex ball bearings support the gimbal with a minimum of friction, the torque motor drives the gimbal in response to an error signal, the multispeed resolver furnishes signals which represent the angular disposition of the gimbal, the slip rings allow passing of electrical signals from the stable member to the external connectors, and the gyro error resolver (inner gimbal only) transforms gyro error signals into gimbal angle error signals.

3-5 OPTICAL TRACKER

The optical tracker, figure 3-5, is the active portion of the LEM optical rendezvous subsystem. The optical tracker and its detection and control circuitry is mounted on the four forward legs of the nav base.

The optical tracker telescope is driven about two axes, elevation and azimuth. The telescope assembly which houses the optics and rotates about the elevation axis (Y), has a direct drive torque motor and tachometer on one side and 1X and 16X resolvers and a potentiometer on the other side. The outer gimbal, which houses the telescope assembly and rotates about the azimuth axis (X), has a direct drive torque motor, 1X and 16X resolvers, and a tachometer mounted along the azimuth axis.

The telescope assembly is free to rotate 360 degrees in either direction in azimuth from the zero position, which is parallel to the $-Y_{LEM}$ axis. Elevation travel is limited to 20 degrees below the LEM +Z axis to 20 degrees above the -Z axis. A flange, bolted to the base of the optical tracker, serves as a mechanical stop to prevent contact of the telescope assembly with the skin of the LEM.



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Figure 3-5. Optical Tracker

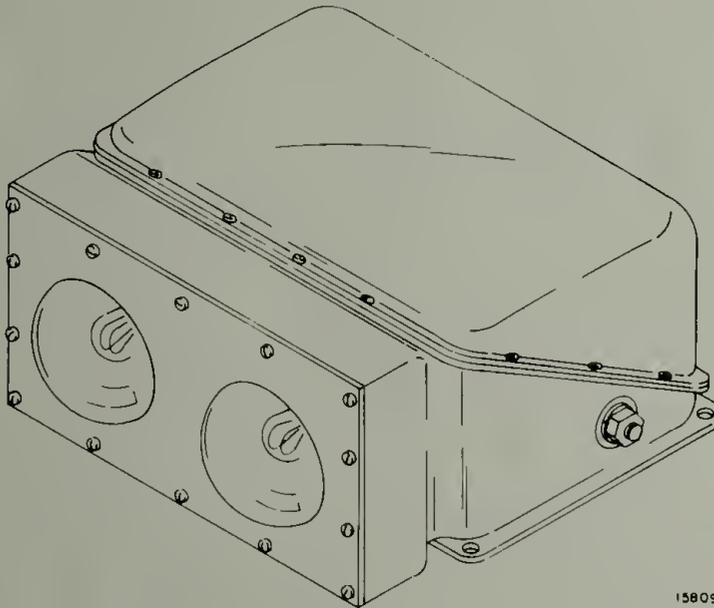


Figure 3-6. Luminous Beacon

3-6 LUMINOUS BEACON

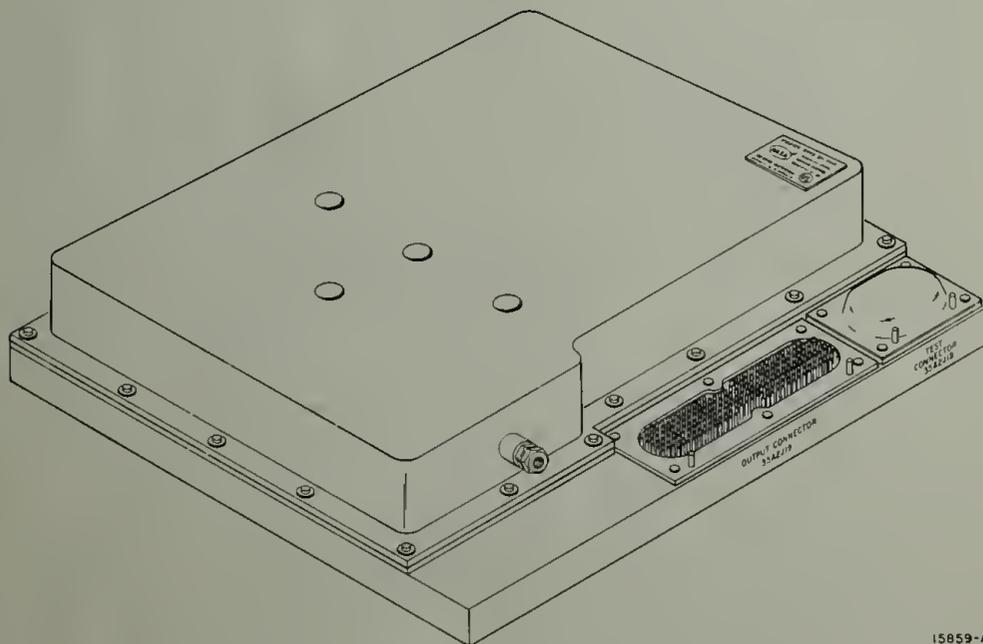
The luminous beacon (figure 3-6) consists of two complete beacon systems and a common controller housed in a single package. Each beacon system consists of a power supply, a xenon flash tube, and the necessary optics to produce a radiant output beam. The luminous beacon is located on the adapter ring between the command and service module.

3-7 PULSE TORQUE ASSEMBLY

The PTA, figure 3-7, consists of 17 electronic modular assemblies mounted on a common base. The cover, which is fitted over the modules and attached to the light-weight magnesium base, has a filler valve that is used to pressurize the unit. The assembled unit, measuring approximately 2.5 inches high, 11 inches wide, and 13 inches deep and weighing approximately 15 pounds, is mounted to a coldplate in the LEM.

The PTA supplies inputs to and processes outputs from the inertial components in the IMU. To avoid line loss in low-level signals, the PTA is mounted close to the IMU. Table 3-IV identifies and lists the functions and locations of the PTA modules.

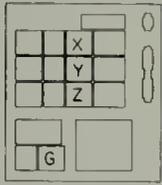
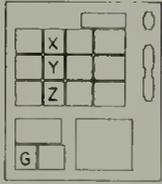
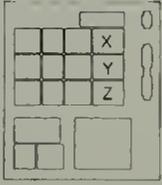
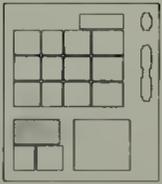
The base, or header, of the PTA has two connectors: J19 which mates with the PGNCS interconnect harness and test connector J18 which breaks out specific signals for monitoring purposes during testing. Table 3-V lists the signals, by pin number, available at jack J18.



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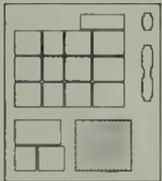
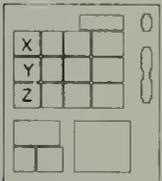
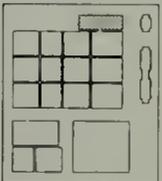
Figure 3-7. Pulse Torque Assembly

Table 3-IV. Locations and Functions of PTA Modules

Module	Part Number	Function	Location
Binary Current switch (4)	2007103-011	One furnishes torquing current to the three Apollo II IRIG's and three furnish torquing current to the individual 16 PIP's.	
DC differential amplifier and precision voltage reference (4)	2007101-011	Regulate torquing current supplied through binary current switches.	
AC differential amplifier and interrogator (3)	2007104-011	Amplify accelerometer signal generator signals and convert them to plus and minus torque pulses.	
Gyro calibration module	2007102-011	Applies plus or minus torque pulses to Apollo II IRIG's when directed by LGC.	

(Sheet 1 of 2)

Table 3-IV. Locations and Function of PTA Modules

Module	Part Number	Function	Location
Pulse torque power supply	2007106-011	Supplies 120 vdc to dc differential amplifier and binary current switch during gyro torquing routines.	
PIPA calibration module (3)	6007105-011	Compensate for differences in inductive loading of accelerometer signal generator windings and regulate balance of plus and minus torques.	
Pulse torque isolation transformer	6007005-011	Couples torque commands, data pulses, interrogate pulses, switching pulses, and synchronizing pulses between LGC and PTA.	

(Sheet 2 of 2)

Table 3-V. PTA Test Points

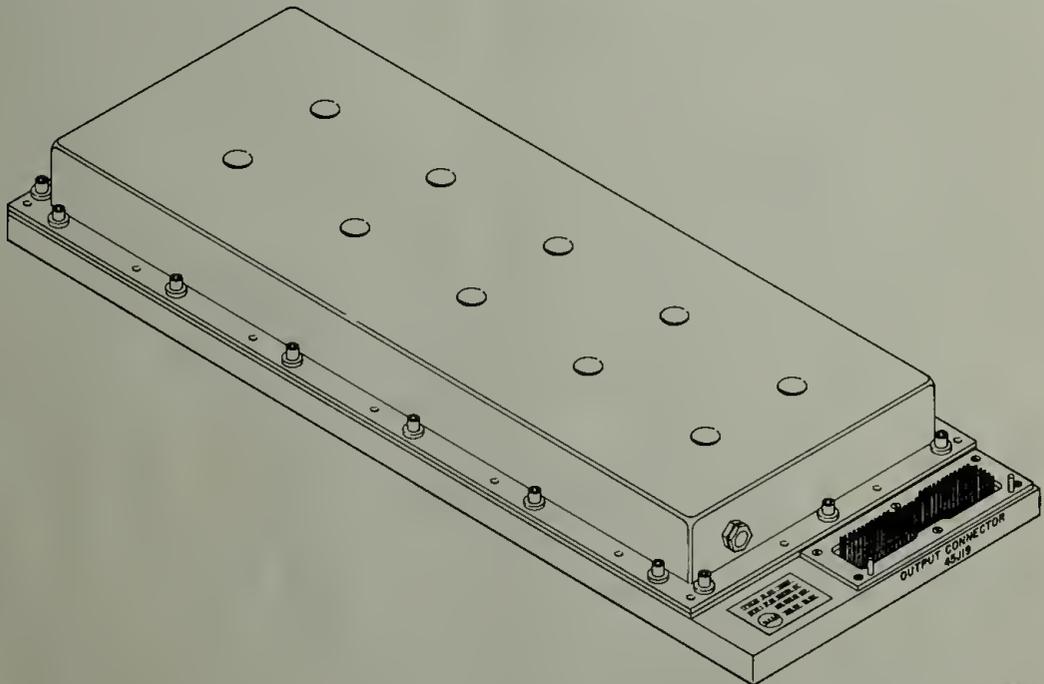
Pin Number	Signal Description	Pin Number	Signal Description
A5	X PIPA P pulses	D2	Y PIPA current monitor (low)
A6	Y PIPA P pulses	D3	Z PIPA current monitor (low)
A7	Z PIPA P pulses	D4	IRIG current monitor (low)
B1	X PIPA PVR (high)	D5	0 vdc IMU X PIPA error monitor (low)
B2	Y PIPA PVR (high)	D6	0 vdc IMU Y PIPA error monitor (low)
B3	Z PIPA PVR (high)	D7	0 vdc IMU Z PIPA error monitor (low)
B4	IRIG PVR (high)	F1	X PIPA current monitor (high)
B5	X PIPA N pulses	F2	Y PIPA current monitor (high)
B6	Y PIPA N pulses	F3	Z PIPA current monitor (high)
B7	Z PIPA N pulses	F4	IRIG current monitor (high)
C1	X PIPA PVR (low)	G5	-20 vdc (high)
C2	Y PIPA PVR (low)	G6	0 vdc IMU (± 20 vdc) (low)
C3	Z PIPA PVR (low)	G7	+ 20 vdc (high)
C4	IRIG PVR (low)		
C5	X PIPA error monitor (high)		
C6	Y PIPA error monitor (high)		
C7	Z PIPA error monitor (high)		
D1	X PIPA current monitor (low)		

3-8 POWER AND SERVO ASSEMBLY

The PSA, figure 3-8, is a group of fourteen electronic modules mounted on a common frame. The electrical connectors and interconnecting harness are an integral part of the frame, or header, which also functions as a heatsink for the electronic components. Mounted to the lightweight magnesium header and filled over the modules is the PSA cover which has a filler valve used to pressurize the unit to one atmosphere and maintain this pressurization during the LEM flight.

The assembled unit, measuring approximately 2-5/8 inches high, 8-7/8 inches wide and 23-1/3 inches deep and weighing approximately 20 pounds, is mounted to a coldplate on the LEM bulkhead behind the astronaut.

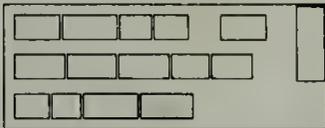
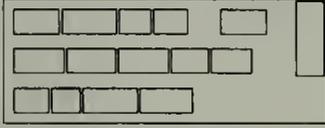
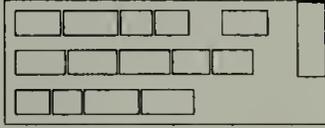
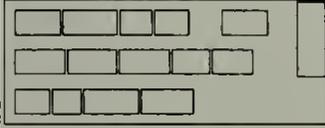
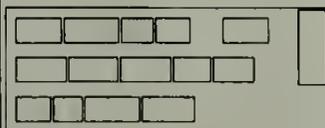
The purpose of the PSA is to provide a central mounting point for the majority of the PGNCS power supplies, amplifiers, and other modular electronic components. Table 3-VI lists the functions and locations of the modules contained in the PSA.



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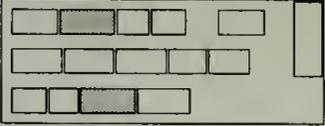
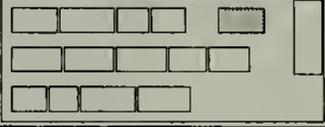
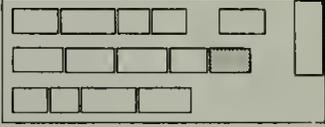
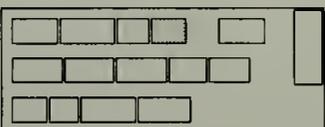
Figure 3-8. Power and Servo Assembly

Table 3-VI. Locations and Functions of PSA Modules

Module	Part Number	Function	Location
-28 vdc power supply	2007107-011	Supplies power to gimbal servo amplifiers and pulse torque power supply.	
3200 cps, 1 percent amplifier	2007108-011	Supplies 28 volts, 3200 cps to ducosyn transformer on stable member.	
3200 cps automatic amplitude control (AAC), filter and multi-vibrator	2007109-011	Regulates operation of 3200 cps, 1 percent amplifier.	
800 cps, 1 percent amplifier	2007110-011	Supplies 28 volts, 800 cps for IMU resolver excitation. (Also supplies this power for FDAI and SCS reference signals.) Provides reference signal for two 800 cps, 5 percent amplifiers.	
800 cps automatic amplitude control (AAC), filter and multi-vibrator	2007112-011	Regulates operation of 800 cps, 1 percent amplifier.	

(Sheet 1 of 2)

Table 3-VI. Locations and Functions of PSA Modules

Module	Part Number	Function	Location
800 cps, 5 percent amplifier (2)	2007111-011	Supplies 28 volts, 800 cps for IMU blower, gyro wheels, and accelerometer heaters.	
PGNCS sub-system supply filter	6007114-011	Filters 0 vdc, 27.5 vdc, and 28 vdc supplies.	
IMU auxiliary assembly	2007117-011	<ol style="list-style-type: none"> Indicates out of tolerance conditions on 3,200 cps 28 v (rms), 800 cps 28 v (rms), and gimbal error signals. Provides IMU turn-on moding discrete. Indicates IMU temperature out of tolerance to telemetry. 	
Gimbal servo amplifier (3)	2007114-011	DC current amplifier with demodulator input for torquing IMU gimbals.	
Relay module	2007123-011	Contains six relays required for moding of IMU.	
IMU load compensation	2007132-011	Provides power factor correction for 800 cps, 1 percent and 5 percent supplies.	

3-9 LEM GUIDANCE COMPUTER

The LGC, figure 3-9, consists of two flat tray assemblies bolted together, module sides facing. The assembled unit measures approximately 6 inches high, 12-1/2 inches wide, and 24 inches deep and weighs approximately 60 pounds. The LGC is mounted on a coldplate on the after cabin wall (pressure bulkhead).

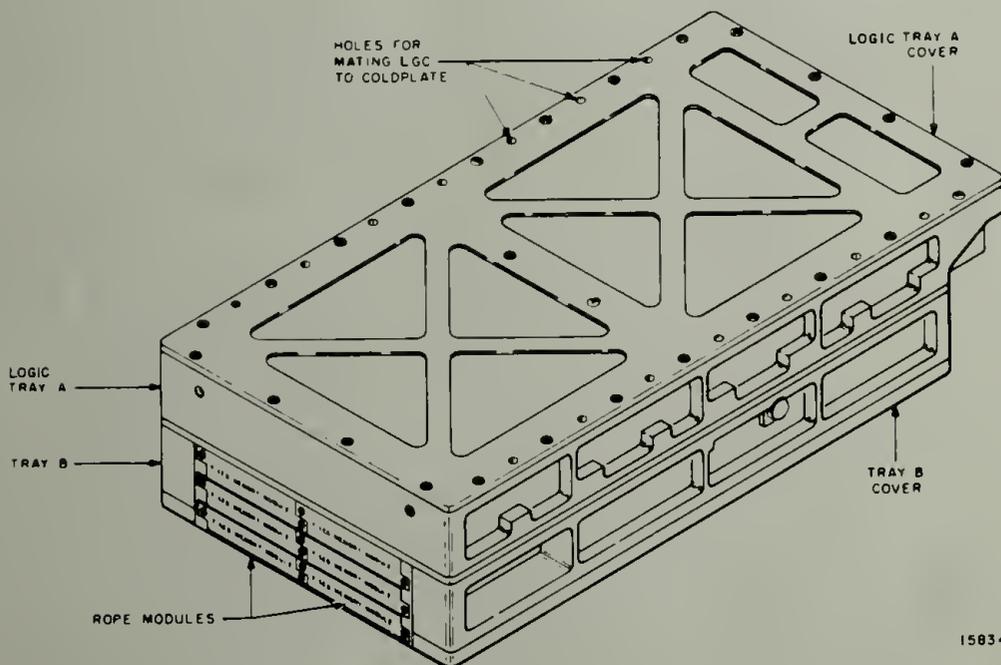


Figure 3-9. LEM Guidance Computer

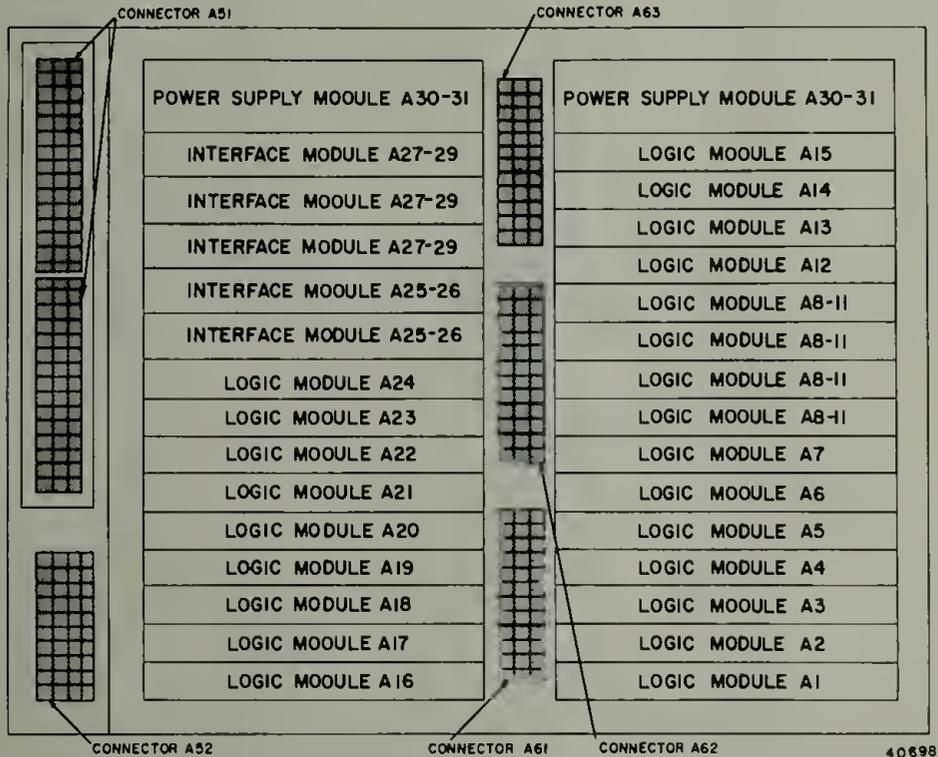


Figure 3-10. Logic Tray A

3-9.1 LOGIC TRAY A. The logic tray A assembly (figure 3-10) contains 31 modules: 24 logic, 5 interface, and 2 power supply modules. All modules are potted with a silastic compound after being mounted on the tray.

The logic tray A assembly has three intertray connectors (A61, A62, and A63) and two intersystem connectors on the rear. The 360 pin rear connector, A51, connects the LGC to the main 28 vdc power source, to the DSKY, to other components of the PGNCS, and to other LEM systems. The 144 pin rear connector, A52, provides interface with ground support equipment for LGC testing.

3-9.2 TRAY B. The tray B assembly (figure 3-11) contains 17 modules, including 6 rope modules. Eleven modules are potted into the tray in a manner similar to that in logic tray A; the six rope modules are plug-in units located at the front of the LGC. The tray B assembly has three intertray connectors (B61, B62, and B63) which interface with those on the logic tray A assembly.

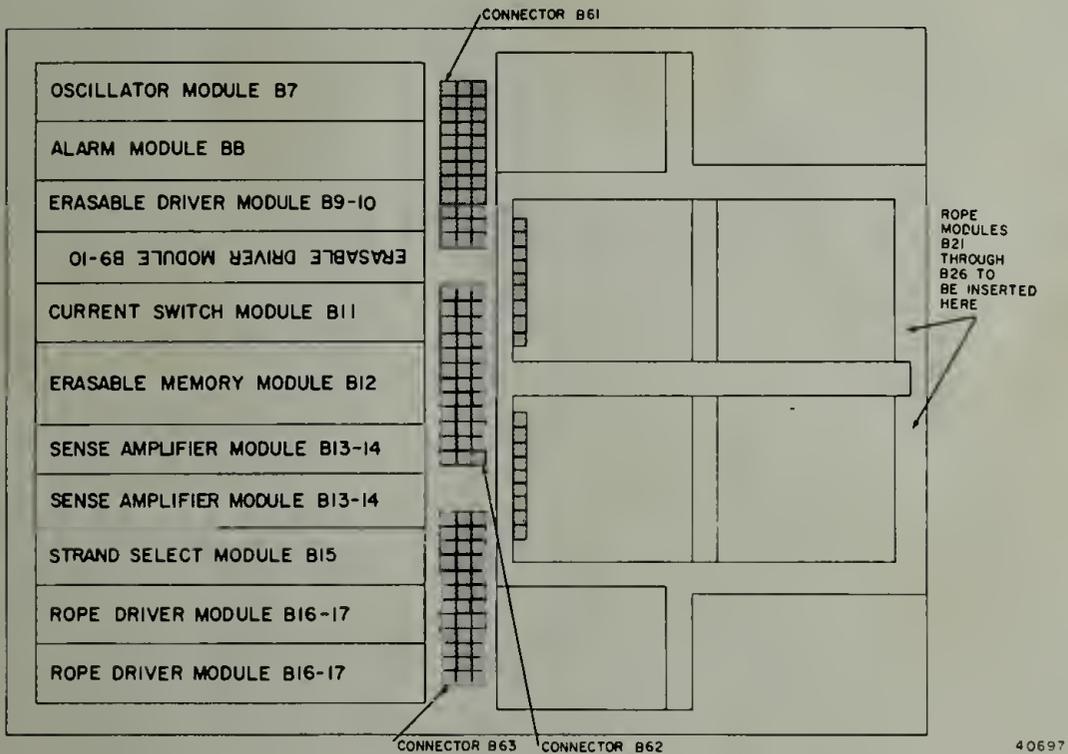
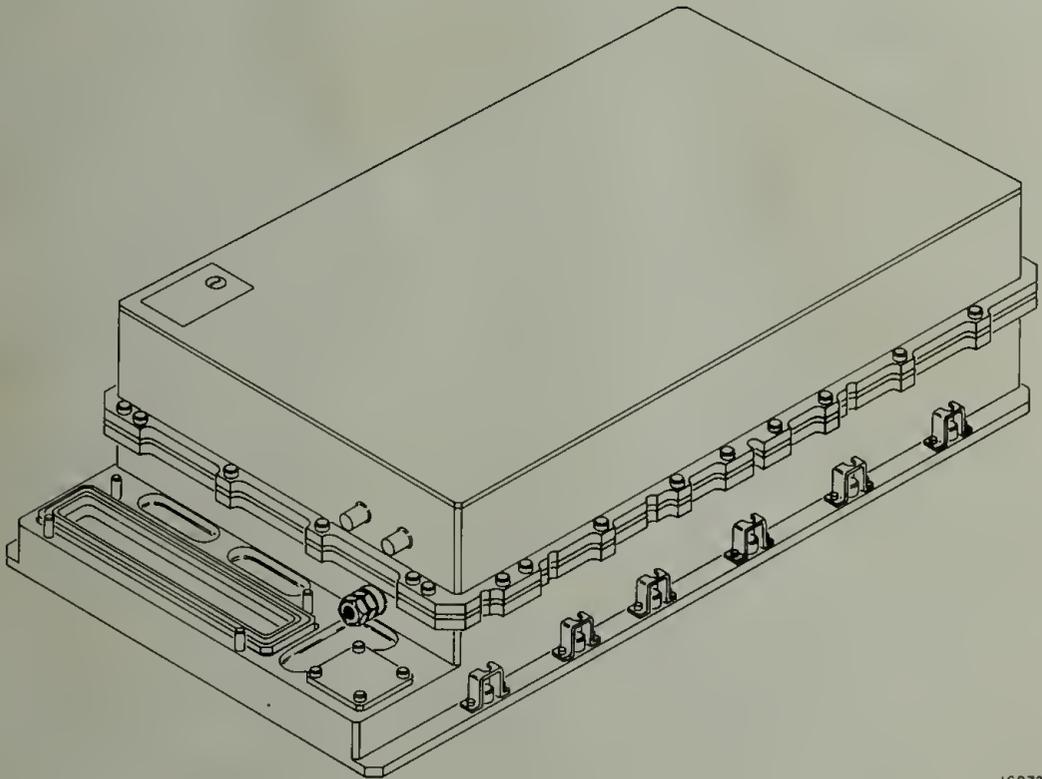


Figure 3-11. Tray B

3-10 COUPLING DATA UNIT

The CDU, figure 3-12, consists of two tray assemblies containing a total of 34 modules. The two tray assemblies, tray X and tray S, are bolted together, module sides facing. The unit is then mounted to a coldplate in the LEM. The assembled unit, constructed mainly of magnesium, measures approximately 5.5 inches high, 11.3 inches wide, and 20 inches deep and weighs approximately 35 pounds.

Tray X has two connectors, one used only for component level testing; the other, J53, used to connect the CDU to the PGNCs interconnect harness. Tray X also has a filler valve used to pressurize the CDU.



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Figure 3-12. Coupling Data Unit

The modules in the CDU provide five separate channels to couple the LGC to the IMU and the optical tracker. In addition to the five separate channels, the CDU contain four modules which are shared by all channels. Basic CDU functions are as follows:

- (1) Interpret commands (digital) from the LGC and convert them to IMU gimbal positioning signals (analog).
- (2) Interpret gimbal positions (analog) and transmit the information to the LGC (digital).
- (3) Couple the IMU to the FDAI.

(4) Interpret optical tracker azimuth and elevation angles (analog) and transmit the information to the LGC (digital).

(5) Interpret commands (digital) from the LGC and convert them to optical tracker positioning signals (analog).

CDU module locations are illustrated in figure 3-13 and their functions described in table 3-VII.

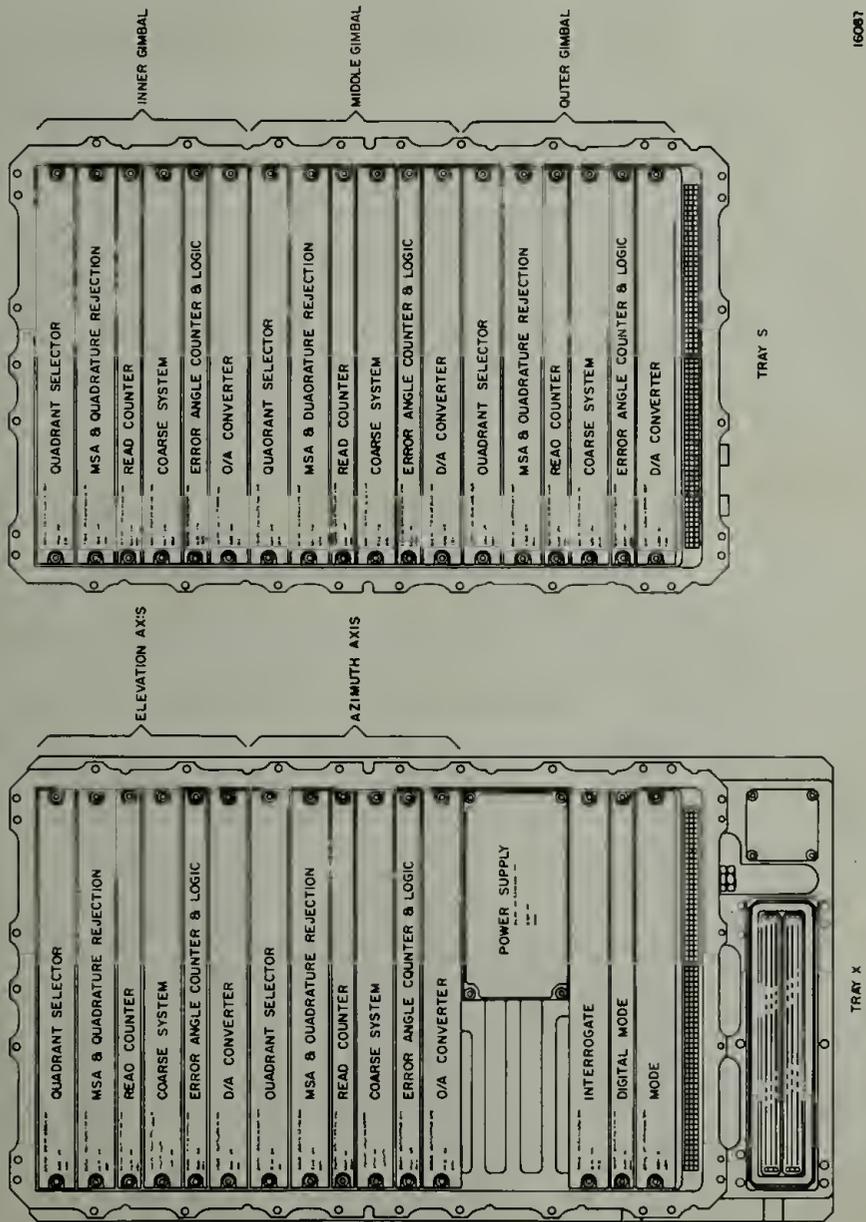
3-11 SIGNAL CONDITIONER

This paragraph will give a physical description of the signal conditioner and will be supplied when information is available.

3-12 DISPLAY AND KEYBOARD

The primary communication link between the astronauts and the PGNCS is the DSKY (figure 3-14). The DSKY is located immediately below the lower center instrument panel. The DSKY is approximately 8 inches high, 8 inches wide, 7 inches deep, and weighs 17 pounds. The upper half of the DSKY is the display and the lower half is the keyboard. The display section contains 14 caution and alarm indicators, 7 operation display indicators, and 18 data display indicators. The words PROG, VERB, and NOUN and the lines separating the three groups of display indicators are illuminated whenever the PGNCS is energized, as are the 19 keys of the keyboard.

There are a 91 pin connector, a filler valve, and a power supply mounted on the rear of the DSKY. The connector interfaces the DSKY with the LGC, other PGNCS components, and with other LEM systems. The filler valve is used to pressurize the DSKY to one atmosphere. The power supply provides voltages for operation of the display indicators. The DSKY controls and indicators and their functions are listed in table 3-VIII.



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Figure 3-13. CDU Module Locations

Table 3-VII. Functions of CDU Modules

Module	Part Number	Function
Coarse system (5)	2007236-011	Provides coarse switching and attenuation circuitry necessary to increment angles.
Main summing amplifier and quadrature rejection (5)	2007238-011	Provides fine switching and attenuation circuitry necessary to increment angles.
Quadrant selector (5)	2007243-011	Converts $\sin \theta$ and $\cos \theta$ resolver signals to phase relationships required by main summing amplifier.
Read counter (5)	2007140-021	Accumulates pulses representing angles and controls switching of coarse system module, quadrant selector module, and main summing amplifier.
Interrogate module	2007263-011	Generates a portion of timing pulses required for CDU operation, produces 14 vdc power, and provides circuitry for data and pulse transmission.
Digital mode module	2007141-021	Provides pulse commands which are used throughout CDU for synchronization, switching, and strobing.
Mode module	2007254-011	Buffers signals and monitors CDU operations.
Error angle counter and logic module (5)	2007139-021	Accumulates pulses representing angular error and provides logic circuitry to control operation of other CDU modules.
Power supply	2007142-011	Supplies 4 vdc logic power to digital logic portions of CDU.
Digital to analog converter (5)	2007237-011	Converts digital information in error counter into a dc analog signal and two ac analog signals.

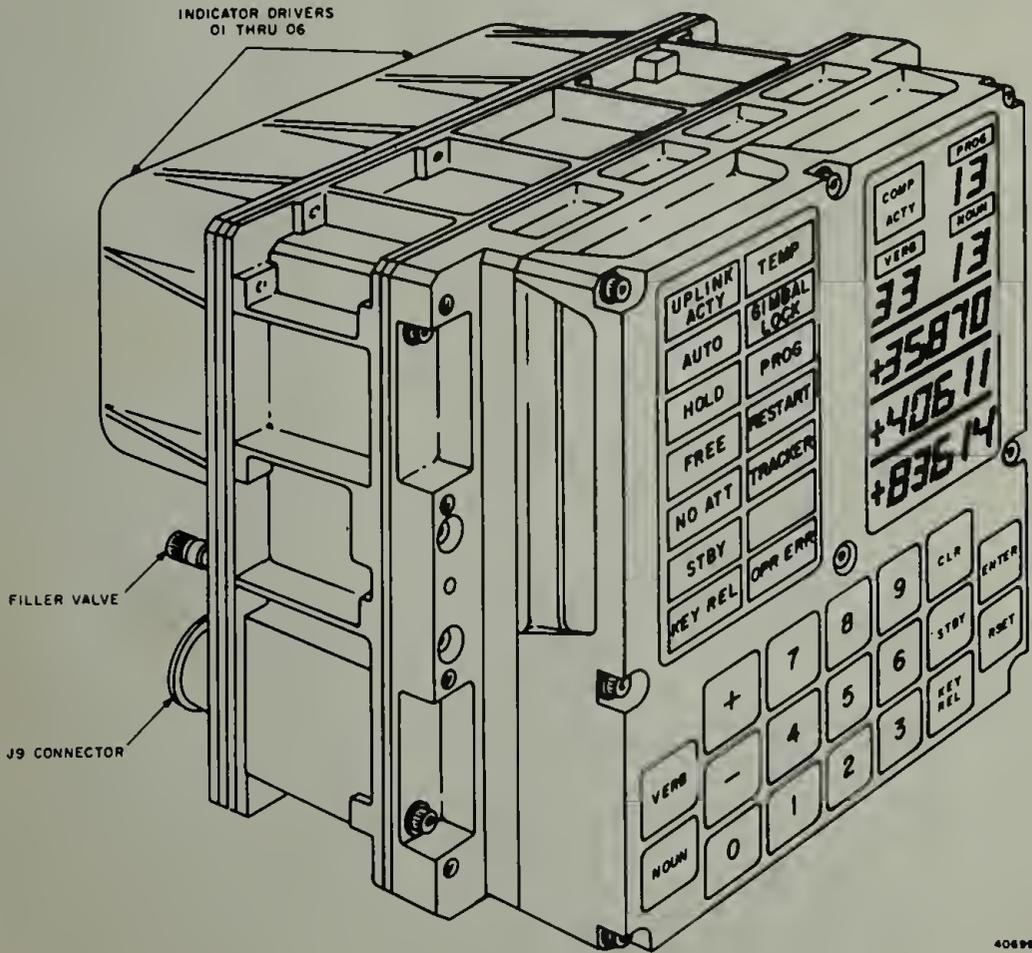


Figure 3-14. Display and Keyboard

Table 3-VIII. DSKY Controls and Indicators

Indicators and Controls	Functions
Caution and Alarm Indicators	
UPLINK ACTY	Indicates information is being received via UPLINK. (Not used for manned flights.)
STBY	Indicates LGC is in restart condition and low power mode.
KEY REL	Indicates that LGC wishes to display program information and has found DSKY in use.
RESTART	Indicates LGC is in restart condition.
OPR ERR	Indicates illegal keyboard operation.
AUTO	Not used.
HOLD	Not used.
FREE	Not used.
NO ATT	Indicates that ISS is not suitable for use as attitude reference.
TEMP	Indicates underheat or overheat condition of IMU stable member.
GIMBAL LOCK	Indicates middle gimbal angle in excess of 75 degrees.
PROG	Indicates that program check has failed. This indicator is controlled by the LGC program.
TRACKER	Indicates failure of LORS channel of CDU or LORS data is not proper.
Spare	Spare.

(Sheet 1 of 3)

Table 3-VIII. DSKY Controls and Indicators

Indicators and Controls	Functions
Operation Display Indicators	
COMP ACTY	Indicates LGC is operating.
PROG	Indicates function or functions of current LGC program.
VERB	Indicates verb code entered at keyboard.
NOUN	Indicates noun code entered at keyboard.
Data Display Indicators	
Data display indications	A plus or minus sign signifies data is decimal; no sign signifies data is octal.
Keyboard Keys	
KEY REL	Releases control of keyboard so that information supplied by program action may be displayed.
STBY	Initiates LGC restart condition and puts LGC into low power mode. Normal operation may be resumed by again pressing STBY.
RSET	Clears caution indicators and OPR ERR indicator.
CLR	Clears data contained in data register currently in use.
VERB	Conditions LGC to accept next two numerical characters as action request.
NOUN	Conditions LGC to accept next two numerical characters as address code.

(Sheet 2 of 3)

Table 3-VIII. DSKY Controls and Indicators

Indicators and Controls	Functions
Keyboard Keys (cont)	
<p>ENTER</p> <p>+ key</p> <p>- key</p> <p>0 through 9</p>	<p>Informs LGC that assembled data is complete; execute requested function.</p> <p>Enters positive sign for decimal data.</p> <p>Enters negative sign for decimal data.</p> <p>Enter data, address code, and action request code into LGC.</p>

(Sheet 3 of 3)

Chapter 4

COMPONENT THEORY OF OPERATION

4-1 SCOPE

This chapter discusses the operation of components or circuits whose operation is not apparent in the functional descriptions presented in Chapter 2.

4-2 APOLLO II INERTIAL REFERENCE INTEGRATING GYRO

The Apollo II IRIG stabilization gyro (figure 4-1) is a fluid and magnetically suspended, single-degree-of-freedom, integrating gyro. It is one of the 25 series of inertial instruments. The 25 designation denotes the case diameter in tenths of inches. The stabilization gyros are the sensing elements of the stabilization loop. Three such gyros are mounted on the stable member with their input axes mutually perpendicular. Any change in the attitude of the stable member is sensed by one or more of the gyros. The gyros convert this displacement into an error signal which is amplified and fed into the gimbal torque motors. The gimbal torque motors reposition the stable member until the error signals are nulled and the original orientation of the stable member is re-established.

The Apollo II IRIG consists of a wheel assembly, a spherical float, a cylindrical case, a signal generator ducosyn, and a torque generator ducosyn. The wheel is mounted within the sealed float on a shaft perpendicular to the float axis and spins on preloaded ball bearings. The wheel is driven as a hysteresis synchronous motor in an atmosphere of helium. The float is mounted within the case on a shaft axially coincident with the longitudinal axes of both float and case. Precision hard-alloy pivots and bearings are located at each end of the float shaft, with the bearing being part of the float assembly. The torque generator ducosyn is mounted on one end of the float shaft, while the signal generator ducosyn is mounted on the opposite end. The volume between the float and case is filled with a suspension and damping fluid.

Four axes (input, spin, spin reference, and output) are associated with the Apollo II IRIG. While the wheel is spinning, the gyro tends to maintain its attitude with respect to space. If the gyro is forced to rotate about the input axis (perpendicular to the wheel spin axis), it will respond with a torque about the output axis (perpendicular to both spin and input axes). The spin axis is displaced from its normal or null alignment with the spin reference axis by an amount equal to the angle through which the output axis has rotated. The spin reference, input, and output axes are always mutually perpendicular.

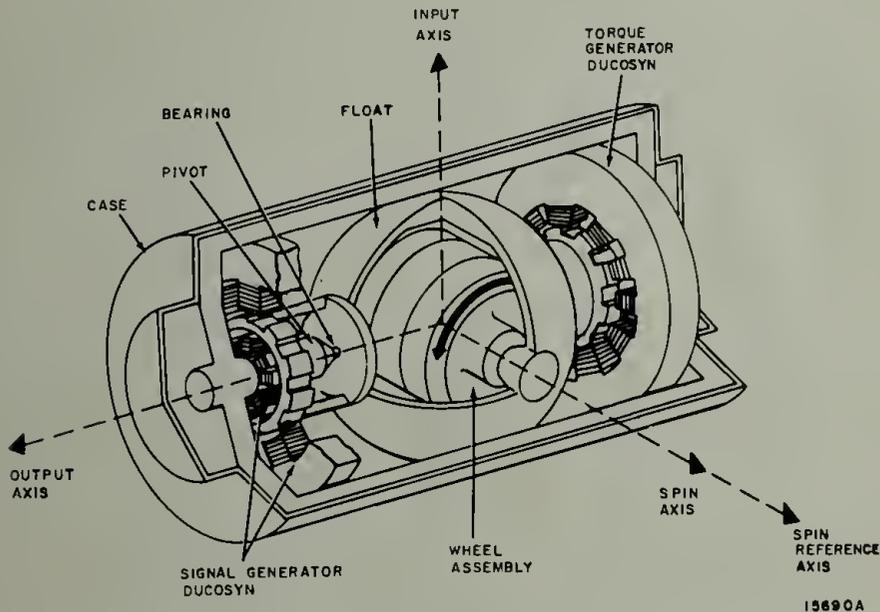


Figure 4-1. Apollo II IRIG, Simplified Cutaway View

The rotation about the output axis in response to a rotation about the input axis in a single-degree-of-freedom gyro is called gyroscopic precession. The output axis is along the float shaft. Rotation of the gyro about its input axis results in a precession of the float.

The signal generator ducosyn is mounted on the positive output axis end of the float to provide magnetic suspension of the float with respect to the case, and to serve as a transducer for providing an electrical analog signal which indicates the amount and direction of the angular rotation of the float about the output axis. The torque generator

ducosyn is mounted on the negative output axis end of the float to provide magnetic suspension, and to serve as a transducer for converting electrical error signals to a torque about the output axis when desired.

Since float movement is a measure of angular displacement of the gyro, friction on the float shaft (output axis) is a critical factor of gyro sensitivity. To reduce this friction to a negligible level, the space between the float and case is filled with a fluid which has the same density (specific gravity) as the float. This fluid causes the float to be suspended with respect to the case. Density of the fluid is kept equal to the density of the float by the controlled application of heat. Heating coils attached to the Apollo II IRIG end mounts maintain the density of the fluid. Two sensors submerged in the fluid indicate the temperature of the fluid. The fluid also provides viscous damping of float movement. The fluid suspension is supplemented by magnetic suspension which keeps the pivot centered in the bearing. The magnetic suspension forces are created by the signal and torque generator ducosyns. Under normal environmental conditions the pivot never touches the bearing. Polished precision hard-alloy bearings and pivots are used to minimize the friction which may result if the pivot touches the bearing under extreme environmental conditions.

Since oxygen would rust the ferrous parts in the wheel assembly, the float is filled with helium which will conduct heat away from the wheel motor. Because helium is a light gas it generates little windage, resulting in the additional advantage of low windage losses in the wheel motor. The float is filled with helium at a pressure of one-half atmosphere to further reduce windage losses.

4-2.1 GYRO WHEEL ASSEMBLY. The gyro wheel assembly consists of a wheel, a shaft, hysteresis ring, ball bearings and bearing retainer. The wheel consists of a beryllium hub with a steel rim. The purpose of the composite wheel is to concentrate as much weight as possible in the outside rim, providing the wheel with a high moment of inertia. The steel, hollow shaft has female threads on each end and is machined to serve as the inner race for the ball bearings. Preloading of the wheel is achieved and controlled by bolting the bearing retainers to the hub. The bearing retainers press on the outer bearing race exerting a wedging action on the balls. As a result, a deliberate load (preload) is imposed on the wheel bearing to insure that the wheel rotates precisely at a right angle to the shaft. The amount of preload is carefully determined since excessive preload will introduce excessive bearing friction that would limit bearing life. The hysteresis ring, constructed of laminated, specially hardened steel, is fitted on the wheel hub and serves as a rotor for the hysteresis synchronous motor which drives the wheel.

4-2.2 FLOAT ASSEMBLY. The float assembly is essentially a float gimbal, two hemispheres, hysteresis motor stator, and bearings. The wheel assembly is bolted to the float by threaded rings. The rings also hold together the float gimbal and the float hemispheres, both of which are made of beryllium. The hysteresis motor stator is placed inside the float gimbal with the power leads brought out through each end of the float gimbal. The float shaft is an integral part of the float gimbal and extends outward from the float to serve as a mount for the float bearings and ducosyn rotors. The bearings, when placed on each end of the float gimbal, define the output axis. The float

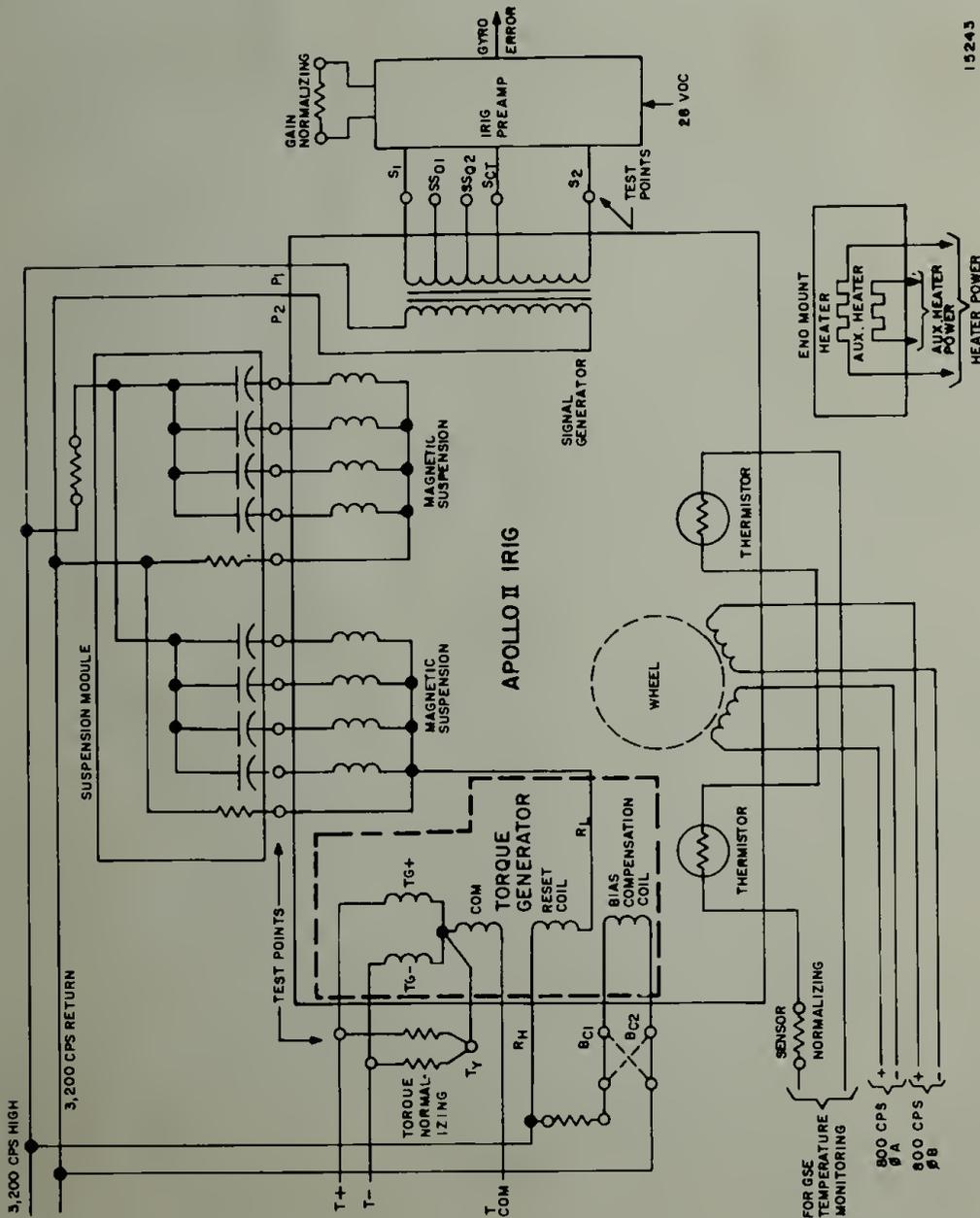
gimbal also has a hole fitted with a ball and screw seal through which the float is evacuated and filled with helium. Preliminary balance weights are placed on the float gimbal for rotational balancing prior to the float being inserted into the case. Balance weights along the spin axis and the input axis are accessible from outside the case and are used for rotational balancing after final assembly.

4-2.3 CASE. The case consists essentially of main housing and damping block assemblies, end housing assembly, and main cover assembly. The float assembly is encased in the main housing assembly and is supported with respect to the end housing by the pivot assemblies. Beryllium damping blocks fill the space around the float. These blocks provide the necessary control of the damping gap (the width of the gap between the float assembly and case), thereby controlling the damping coefficient. The end housings are held to the main housing by clamping caps. The end housings contain the pivot assemblies, ducosyn stators, bellows to take up the expansion and contraction of the suspension fluid, and a setscrew and ball seal to allow filling with the suspension fluid. Four balance adjusters, provided in the main housing assembly, allow access to the adjustable balance weights along the spin axis and the input axis. After hermetically sealing and balancing the unit, the Apollo II IRIG is covered by a main cover assembly which provides a magnetic shield plus a second hermetic sealing.

4-2.4 NORMALIZING NETWORK. The normalizing network (figure 4-2) contains the magnetic suspension capacitors, torque generator normalization resistors, temperature sensor normalization resistor, main heater, auxillary heater, and signal generator preamplifier with gain normalization resistor attached. The pre-alignment package is added to the signal generator end of the gyro case during final assembly, making the gyro a pre-aligned gyro. The gyro is pre-aligned on a test stand with the input axis aligned about the output axis relative to a slot in the mounting ring. This alignment is carried over to the stable member where a pin is precisely located to pick up the slot. When the gyro is mounted in the stable member, an additional main heater and an auxillary heater are placed on the torque generator end.

The signal generator preamplifier is an ac amplifier with transformer coupled input and output which amplifies the gyro output signal prior to transmission from the stable member to the PSA.

4-2.5 APOLLO II IRIG DUCOSYNS. The Apollo II IRIG uses ducosyns for magnetic suspension of the float, signal generator action, and torque generator action. The ducosyn is a separate magnetic suspension microsyn and a separate transducer microsyn in a single unit. The unit contains two separate stators mounted in the end housing and two separate rotors mounted on a common mounting ring of the float assembly. The inside stator assembly consists of eight outwardly projecting tapered poles which are wound and excited to provide magnetic suspension. The outer stator assembly consists of twelve inwardly projecting poles which are wound to provide either signal generator or torque generator action. The outer rotor is the transducer rotor and consists of eight unwound salient poles. The inner rotor, which is the magnetic suspension rotor, is cylindrical, tapered, and unwound. A beryllium ring separates the two rotors to reduce cross-coupling effects.



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Figure 4-2. Apollo II IRIG Normalizing Network

4-2.5.1 IRIG Signal Generator Ducosyn. The signal generator ducosyn is mounted on the positive output axis end of the gyro to provide magnetic suspension and to serve as a transducer to provide an electrical analog signal representing the position of the float relative to the case. (See figure 4-3). Poles 1, 4, 7, and 10 are wound with primary windings which induce a voltage into the secondary windings on the pole pieces on either side of the primary winding poles. All secondary windings are wound with equal turns. The secondary windings (2-12, 3-5, 6-8, and 9-11) on either side of each primary pole are wound in opposition to each other. When the rotor pole pieces are symmetrically located between the pairs of secondary poles, the flux density in the secondary poles is equal and equal voltage is induced in the secondary windings. Since the secondary windings are wound in opposition the induced voltages cancel and the net output voltage is zero. This is the null position of the rotor. When the rotor is rotated from the null position as a result of float displacement, the equality of air gap reluctance is disrupted resulting in unequal flux density in the pairs of secondary poles and therefore unequal induced voltages in the windings. The magnitude of the net output voltage depends on the degree of air gap reluctance unbalance; the greater the rotor displacement from null, the greater the net output voltage. The phase of the net output voltage is determined by the direction of rotor rotation. As a result of counterclockwise rotation, higher voltages are induced in the secondary windings that are wound in phase with the primary windings, causing the net output voltage to be in phase with the primary excitation. In the same manner, clockwise rotation produces a net output voltage that is out of phase with the primary excitation.

The Apollo II IRIG ducosyns require a 4 volt, 3,200 cps single phase excitation for the signal generator primary windings and for the magnetic suspension portions.

4-2.5.2 IRIG Torque Generator Ducosyn. The Apollo II IRIG torque generator ducosyn is mounted on the negative output axis end of the float to provide magnetic suspension and to serve as a transducer to convert an electrical error signal into a torque about the output axis. Figure 4-4 shows the torque generator with the rotor in the null position. To develop torque, current is allowed to flow through the common winding and through either the T+ or the T- winding. The direction of torque is determined by the winding through which current flows. The torque generator stator may be considered as divided into four symmetrical groups of three poles. The center pole of each group (1, 4, 7, and 10) has a common winding only and will always be a north pole when energized. The poles on either side (2-12, 3-5, 6-8, and 9-11) of the center poles have both T+ and T- windings with the polarity of the poles determined by which of the two windings is energized. In either case, one pole in each group will become a north pole and the other a south pole. Since the center pole is always a north pole, each group of three poles will consist of two north poles and one south pole whenever the windings are energized. The rotor will tend to align itself symmetrically between the north and south poles, creating a torque. When the T- winding is energized, pole 12 will become a south pole and pole 2 will become a north pole. The rotor, in attempting to align itself, will tend to rotate clockwise until rotor pole 8 is directly opposite stator pole 12 and rotor pole 1 is directly between stator poles 1 and 2, since 1 and 2 are both north poles. When the T+ winding is energized, stator pole 2 will become a south pole

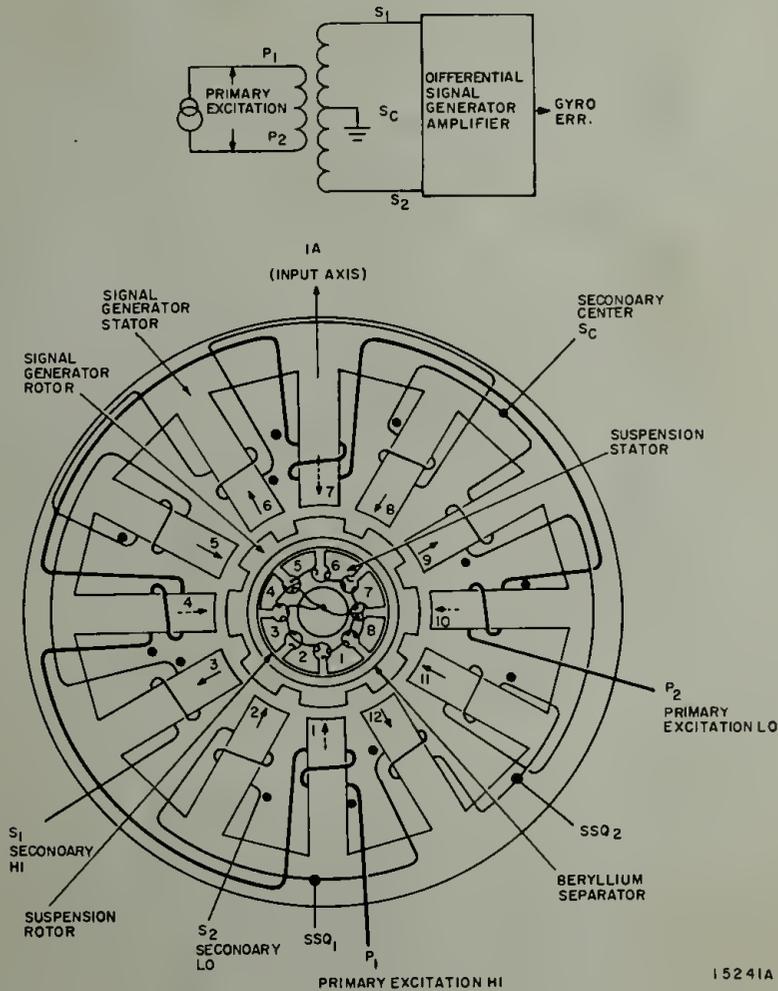


Figure 4-3. IRIG Signal Generator and Suspension Microsyn

and stator pole 12 will become a north pole. The rotor will tend to rotate counterclockwise attempting to align rotor pole 2 opposite stator pole 2, and rotor pole 1 between stator poles 1 and 12. The other poles attempt to align themselves in the same manner.

The direction of the desired torque is controlled by gyro select pulses from the LGC. The pulses act through a switching network in the gyro calibration module to close

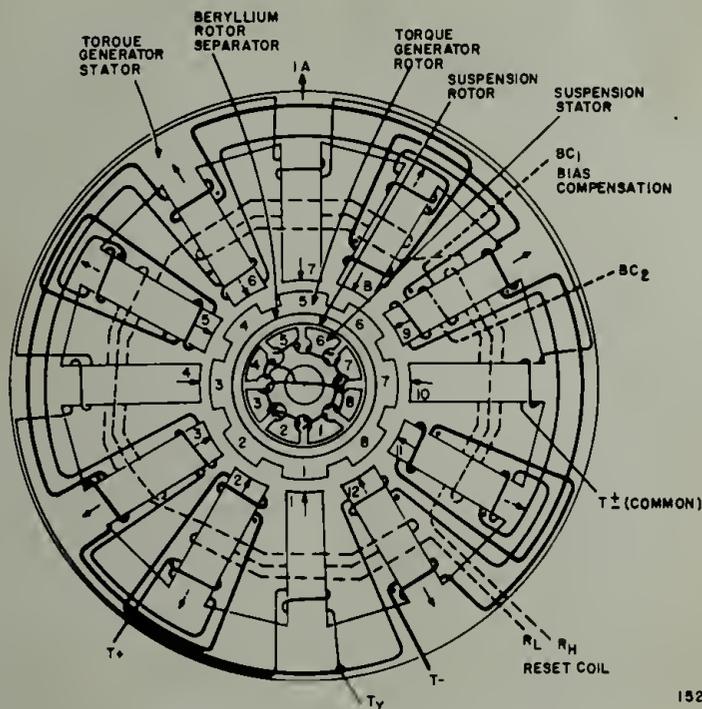
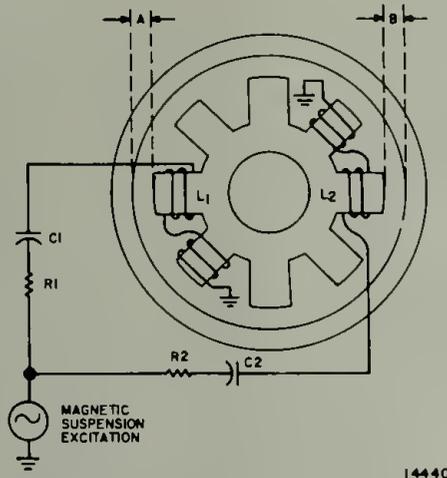


Figure 4-4. IRIG Torque Generator and Suspension Microsyn

the torque current path through either the $T+$ or the $T-$ winding. The magnitude of the torque current is held constant to develop a constant torque. Torque on the rotor produces torque on the gyrofloat. The resulting float displacement creates an error signal from the ducosyn signal generator. Thus, the position of the IMU stable member is changed by the compensating reaction from the stabilization loops.

The torque generator stator also has a reset coil and a bias compensation coil, both of which are continuously energized by the 4 volt, 3,200 cps magnetic suspension and signal generator excitation voltage. The reset coil serves to keep the magnetic state of the magnetic material constant following any torque commands. This degaussing action prevents the storage of residual magnetic dipoles in the rotor and stator which would create torque. A winding around each group of three stator poles acts as a reset coil for both rotor and stator. The bias compensation coil creates a torque equal and opposite to the non-gravity torques which produce bias drift, such as the torque due to flex leads. In this manner, the bias drift due to these sources may be reduced to zero.



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Figure 4-5. Ducosyn RLC Equivalent Circuit

4-2.5.3 IRIG Ducosyn Magnetic Suspension Unit. The Apollo II IRIG ducosyn magnetic suspension units have a tapered cylindrical rotor and tapered stator poles that develop radial and axial magnetic suspension of the gyro float.

Each stator winding is part of a series resistance inductance capacitance (RLC) circuit. (See figure 4-5). Although the equivalent circuit illustrated shows only two poles, it is representative of any of the four pairs of diametrically opposed stator poles. Inductances L_1 and L_2 represent the total inductances of the stator windings. Resistances R_1 and R_2 represent the total resistance of each stator circuit, Capacitors C_1 and C_2 are the external fixed capacitors in series with the resistance and inductance. The values of L_1 and L_2 vary inversely with the size of air gaps A and B respectively.

The excitation to the magnetic suspension unit is maintained at precisely 3,200 cps; the inductance is the only circuit variable. When the inductance is adjusted so the inductive reactance equals and cancels the capacitive reactance, circuit resonance is achieved. At resonance, the total circuit impedance is at a minimum, consisting only of resistance, and the current is thus at a maximum. During construction and testing, a fixed suspension capacitor is selected that develops a value of capacitive reactance that is less than the value of inductive reactance present when the rotor is at null. The resulting impedance allows a current flow that is less than the maximum or resonant current. In operation, translational movement of the rotor from its null point alters the inductance to bring the circuit closer to or further from resonance.

The current flow through the R_1 , L_1 , and C_1 circuit of figure 4-5 increases or decreases according to the inductance which is controlled by air gap A. At some position of the rotor (or value of A), L will produce resonance and maximum current. As the rotor moves in either direction from the resonant point, the current falls off sharply because the value of L (and inductive reactance) changes to make the circuit impedance greater. The current in the stator winding determines the amount of magnetic energy in the stator pole. The attracting force on the rotor is equal to the change in magnetic energy divided by the change in air gap. This relationship of force versus air gap is such that as the rotor moves away from the stator (increasing A), the attracting force rises to a maximum, then decreases sharply as the rotor passes through the resonant point. A negative or repelling force is developed as the rotor is moved beyond the resonant point. In operation, the movement of the rotor is limited by the float pivots so the attracting force only increases as the rotor is moved away from the stator to its maximum allowable displacement. Conversely, as the rotor moves closer to the stator, decreasing the air gap, the attracting force decreases.

As the rotor moves left, air gap A increases and air gap B decreases, and vice-versa. The attracting force at one stator pole changes inversely to the change in attracting force at the other stator pole. When the rotor is displaced from its null point (where the forces on the rotor from both poles are equal), the force from the pole the rotor is approaching decreases, and that of the opposite pole increases. The direction of the resultant force moves the rotor back to the null position. This action magnetically clamps the rotor between its operating limits. Since the four pairs of stator poles are arranged in a circle within the rotor, their simultaneous action effectively suspends the rotor.

Since the rotor and the stator poles are tapered, end play on the float tends to increase or decrease the air gaps of the magnetic suspension units located at each end of the float. The two magnetic suspension units act together to develop a component of force that supports the float axially.

4-3 16 PULSED INTEGRATING PENDULUM

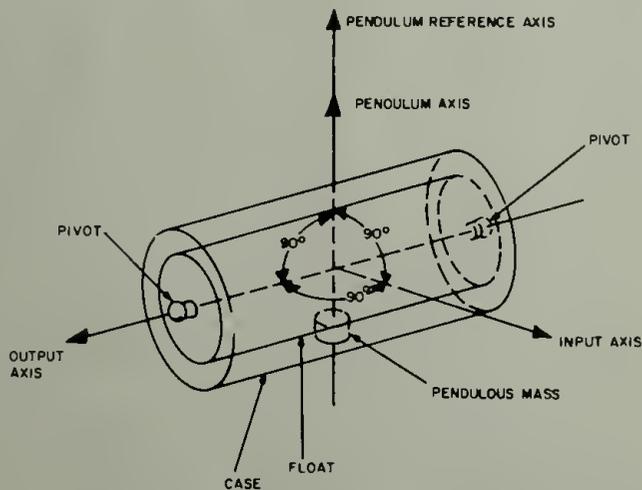
The 16 PIP's are used as accelerometers in the IMU. The 16 PIP in itself is not an accelerometer, but an acceleration sensitive device. In its associated accelerometer loop, the 16 PIP becomes an integrating accelerometer (16 PIPA).

The 16 PIP is basically a cylinder with a pendulous mass unbalance (pendulous float) and is pivoted with respect to a case. The pendulous float has no electrical power requirements as it is completely mechanical in operation. The space between the pendulous float and case is filled with a fluid. A signal generator ducosyn, located at one end of the float, provides magnetic suspension of the float with respect to the case and acts as a transducer to convert mechanical rotation of the float with respect to the case into electrical analog signals. A torque generator ducosyn, located at the other end of the float, provides magnetic suspension of the float with respect to the case and acts as a transducer to convert electrical signals into mechanical torque about the float shaft. A 2 volt rms, 3,200 cps, single phase excitation is required for the magnetic

suspension portion of each ducosyn and for the transducer portion of the signal generator ducosyn.

The output axis of the 16 PIP is defined by the axis of the pivots which support the float with respect to the case. (See figure 4-6.) The pendulum axis is defined by a line which passes through the mass unbalance and intersects the output axis at a right angle. The input axis is the axis along which the 16 PIP is sensitive to acceleration. The input axis and pendulum axis form a plane that is perpendicular to the output axis. When the float rotates about the output axis, the pendulum axis is displaced proportionately from its normal or null position (pendulum reference axis). The pendulum reference, input, and output axes are always mutually perpendicular.

The mass unbalance hangs below the output axis and is forced by loop torquing to swing like a pendulum. The torquing required to keep the pendulum action oscillatory at no acceleration is a known value. When acceleration is sensed along the input axis, an additional torque is felt by the pendulum and the loop compensates for the acceleration torque by supplying torquing current for additional time.



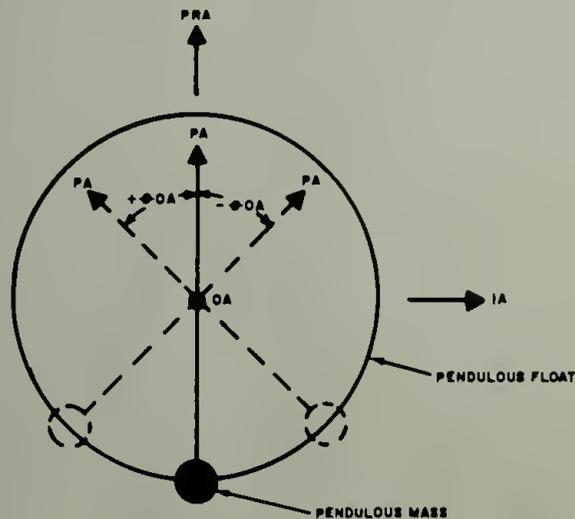
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Figure 4-6. Definition of 16 PIP Axes

Figure 4-7 illustrates the direction the pendulous mass tends to swing due to acceleration torque as viewed from the positive end of the output axis or signal generator end of the PIP.

Acceleration in the direction of the positive input axis (the direction in which the arrowhead points) results in a torque on the float about the output axis which tends to rotate it in the negative angular direction ($-\theta$ OA) about the output axis. Conversely, acceleration in the direction of the negative input axis produces a torque on the float tending to rotate it in the positive angular direction ($+\theta$ OA) about the output axis. When no acceleration is being felt along the input axis, the summation of the angular displacement about the output axis is zero; and by definition, the PIP is at a null.

Maximum sensitivity and linearity of the 16 PIP occur near null. To assure maximum sensitivity and linearity, the accelerometer loop in which the 16 PIP is used restricts the angular displacement about the output axis to very small excursions in either direction from null. The accelerometer loop is designed so that the torque developed by the torque generator is equal to and opposite the pendulous torque resulting from applied acceleration. The signal generator, located at the positive end of the output axis, senses an angular displacement of the float about the output axis. The phase and magnitude of the output signals from the signal generator secondary winding are determined by the direction and amount of float displacement. The error signals are



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Figure 4-7. Result of Acceleration Along Input Axes

processed by the accelerometer loop into incremental velocity pulses to the LGC and into torquing current to the torque generator.

4-3.1 FLOAT ASSEMBLY. The float is a hollow beryllium cylinder fitted with a shaft on which the float pivots are located. On both ends of the float are salient four pole transducer rotors and cylindrical magnetic suspension rotors with tapered inside diameters. The rotor itself is a solid one piece device. The pendulous mass screws into and protrudes slightly from the float. A pin and screw which provides pendulousity adjustment also serves as a stop to limit float rotation about the output axis to ± 1 degree. Adjustable balance weights for rotational balancing of the float are located along the pendulum axis and the input axis. The completed float assembly is placed in a main housing assembly filled with a suspension fluid. The suspension fluid provides fluid suspension of the float with respect to the case and viscous damping of the float.

4-3.2 HOUSING ASSEMBLY. The housing assembly consists of a main housing assembly and two end housings. Damping blocks line the inner diameter of the main housing so as to surround the float. Four bellows assemblies are located within the damping blocks and take up the expansion and contraction of the suspension fluid resulting from variations in fluid temperature. Each end housing contains a pivot bearing, an eight pole magnetic suspension stator, and either an eight pole signal generator stator or an eight pole torque generator stator. The two end housings are called the signal generator end housing (on the +OA end) and the torque generator end housing (on the -OA end). The magnetic suspension microsyns have tapered stator poles and a tapered rotor, developing magnetic suspension forces in both radial and axial directions.

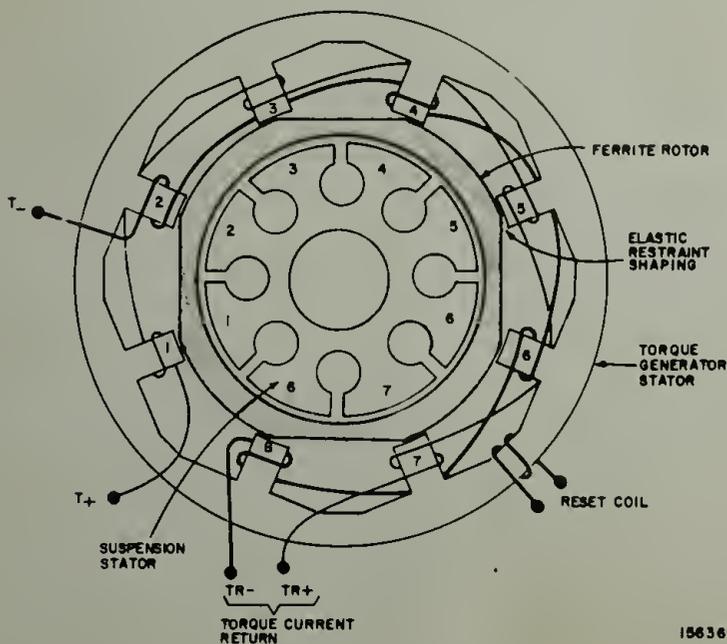
4-3.3 OUTER CASE ASSEMBLY. The housing assembly is completely covered by an outer case which provides magnetic shielding and a hermetic seal for the unit. Heating coils are placed between the main housing and the outer case to heat the suspension fluid to the proper temperature for fluid suspension of the float. All electrical connections for signal generator, torque generator, magnetic suspension microsyns, and heaters are brought out through the torque generator end of the case.

4-3.4 NORMALIZING NETWORK. The 16 PIP normalizing network module contains the suspension capacitors, torque generator normalizing resistors, and temperature sensor normalizing resistors. This module is mounted over the 16 PIP and bridges the 16 PIP end cap. However, to avoid PIP alignment problems, the module is fastened to the stable member instead of the PIP.

4-3.5 PIP DUCOSYNS. The 16 PIP ducosyn signal generator and torque generator differ from the Apollo II IRIG units in both construction and operation. The 16 PIP signal generator and torque generator have eight pole stators. The 16 PIP ducosyn rotor is constructed from a solid piece of ferrite. Flats are ground onto the outer diameter of the rotor to create pseudo salient poles which serve as the transducer rotor. The inner diameter of the rotor is tapered and serves as the magnetic suspension rotor. There is no magnetic separation between the transducer rotor and the suspension rotor which allows the magnetic suspension rotor to degauss the torque generator rotor. The degaussing prevents the storage of residual magnetic poles in the magnetic material which could cause unwanted torques to be created.

The torque generator stator has a single winding per pole. (See figure 4-8.) The windings on the even poles develop negative torque and the windings on the odd numbered poles develop positive torque. The accelerometer loop applies constant dc current to either the odd or even poles. The torque generator stator also has a reset winding which degausses the stator thus preventing the storage of residual magnetic poles which could create unwanted torque.

The signal generator stator poles have both a primary and secondary winding per pole. The secondary windings are wound in opposition so that when the rotor is at null the air gap reluctance at each pair of stator poles is equal and the net output voltage is zero. When the rotor is displaced from null, the air gap reluctance becomes unequal and a net output voltage proportional to the direction and magnitude of the float displacement is developed. The output of the signal generator is amplified, phase shifted, and applied to the interrogator module in the accelerometer loop which detects the direction of float displacement.



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Figure 4-8. PIP Torque Generator

4-4 COUPLING DATA UNIT

The CDU is an electronic device used as an interface element between the PGNCSS subsystems, and between the PGNCSS and various LEM displays and controls. The CDU is a sealed unit containing 34 modules of ten types. The ten module types make up five, almost identical, loops; one each for the inner, middle, and outer gimbals and one each for the optical tracker azimuth and elevation axes. Several of the CDU modules are shared by the five loops.

The CDU functions primarily as an analog to digital converter and as a digital to analog converter. The analog to digital converter converts resolver signals into digital information which is stored in a 16 stage binary counter called the read counter. The digital information is also transmitted to the LGC in the form of pulses. The digital to analog converter accepts pulses from the LGC, stores them in a nine stage binary counter called the error counter, and provides ac and dc output signals proportional to the stored pulses. A digital feedback path between the read counter and the error counter is provided to count the error counter up as the read counter counts down and vice versa.

The CDU converts the angular information from 1X and 16X resolver signals ($\sin \theta$, $\cos \theta$, $\sin 16 \theta$, and $\cos 16 \theta$) into digital information. The resolver angle is digitalized into bits, equal to 20 arc-seconds each and stored in the read counter. An error signal proportional to the difference between resolver angle and the CDU angle (the angle registered by the read counter) causes the read counter to count until the error signal is nulled. If the difference between the resolver angle (θ) and the CDU angle (ψ) is greater than 0.1 degree, the read counter will be incremented at a 12.8 kpps rate. The incrementing rate will be 800 pps if the difference is less than 0.1 degree.

4-4.1 COARSE SYSTEM MODULE. The coarse module functions with the read counter to form the coarse analog to digital conversion system. The coarse module receives the $\sin \theta$ and $\cos \theta$ signals from the 1X gimbal angle resolver and switches them through attenuation resistors which represent various values of $\sin \psi$ and $\cos \psi$. The resolver angle is compared with the angle registered by the read counter through the mechanization of the following trigonometric identity:

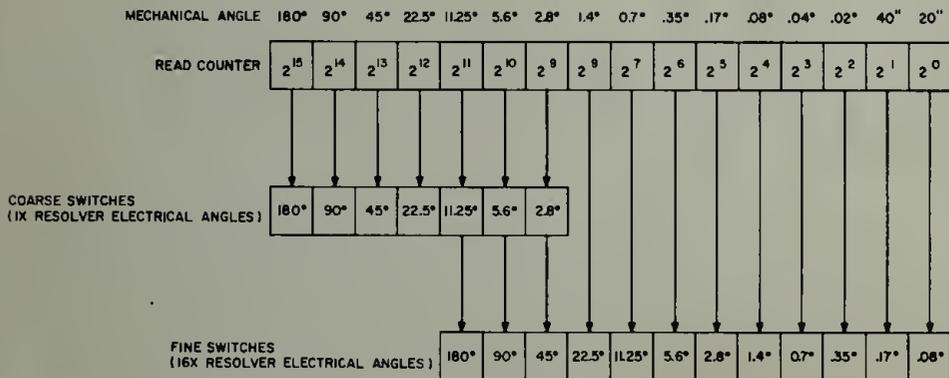
$$\pm \sin (\theta - \psi) = \pm \sin \theta \cos \psi \pm \cos \theta \sin \psi$$

where θ is the gimbal angle and ψ is the CDU angle represented by the accumulation of bits registered by the read counter. The value of ψ can be considered as the gimbal angle as indicated by the read counter. When θ and ψ are equal, the equation goes to zero. If θ does not equal ψ , an error detector in the coarse module will produce an output which will cause incrementing pulses to be sent to the read counter. As the read counter counts up or down, changing the value of ψ , it sends switch control pulses from its seven most significant stages to the coarse module. The switch control pulses operate switches in the coarse module which change the arrangement of the attenuation resistors to obtain different values of $\sin \psi$ and $\cos \psi$ in order to obtain a null

output from the error detector. For each read counter angle ψ , there is a corresponding switch arrangement which will produce a null.

The accumulation of ψ , the read counter indicated gimbal angle, is controlled by three modules within the CDU: the coarse module, the main summing amplifier and quadrature rejection module (MSA & QR), and the quadrant selector module. The coarse module is used in conjunction with the 1X gimbal angle resolver inputs. The other two modules are used in conjunction with the 16X gimbal resolver inputs and function with the read counter to form the fine analog to digital conversion system.

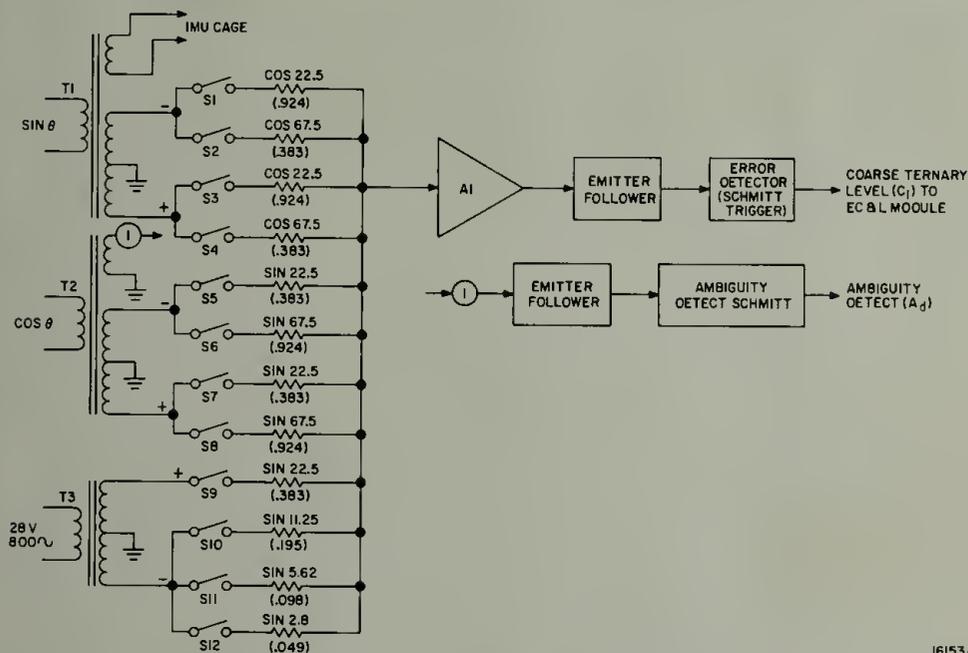
Figure 4-9 illustrates the mechanical angles of the gimbals, the read counter bit positions associated with the mechanical angles, and the coarse and fine system switching associated with each of the read counter bit positions. Note that bits 2^0 through 2^{11} are associated with fine system switching and bits 2^9 through 2^{15} are associated with coarse system switching. The three bit overlap of the coarse and fine systems provides a smooth transition from one system to the other. The angles above the read counter blocks are the mechanical angles through which the 1X gimbal angle resolver shaft rotates. Note also that 180 electrical degrees of 16X resolver rotation is equal to 11.25 degrees of 1X resolver angle.



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Figure 4-9. Read Counter Relationship to Coarse and Fine System Switching

Figure 4-10 provides a functional block diagram of the coarse module. The 1X resolver output signals, $26 \text{ v (rms) } \sin \theta$ and $26 \text{ v (rms) } \cos \theta$, are applied through transformers which have a transformation ratio of 26:4. A 28 v (rms) 800 cps reference signal is applied through a transformer which has a transformation ratio of 28:4. The maximum voltage available at the transformer secondaries, high to center tap, is 4 v (rms). The gimbal angle is represented by the amplitude of the $\sin \theta$ and $\cos \theta$ signals and by their phase with respect to the 800 cps reference signal. If the



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Figure 4-10. Coarse System Module, Block Diagram

gimbal angle were 150 degrees, for example, the $\sin \theta$ and $\cos \theta$ signals at the transformer secondaries would be equal to:

$$\begin{aligned} (1) \quad (4 \text{ v rms}) (\sin 150^\circ) &= \\ (4 \text{ v rms}) (0.5) &= 2.0 \text{ v (rms)} \\ (2) \quad (4 \text{ v rms}) (\cos 150^\circ) &= \\ (4 \text{ v rms}) (-0.866) &= -3.46 \text{ v (rms)} \end{aligned}$$

The $\sin \theta$ signal would be in phase with respect to the 800 cps reference. The $\cos \theta$ signal would be out of phase with respect to the 800 cps reference, as is signified by the minus sign. Figure 4-11 shows the phase relationship of the 1X resolver sine and cosine output signals with respect to the 800 cps reference.

The center tapped secondary of the transformers provides both an in phase and an out of phase signal of equal amplitude, as signified by the plus or minus sign shown on each portion of the secondary winding. (See figure 4-10.) Thus if the $\cos 150$ degrees signal, previously mentioned, were to be taken from the out of phase secondary,

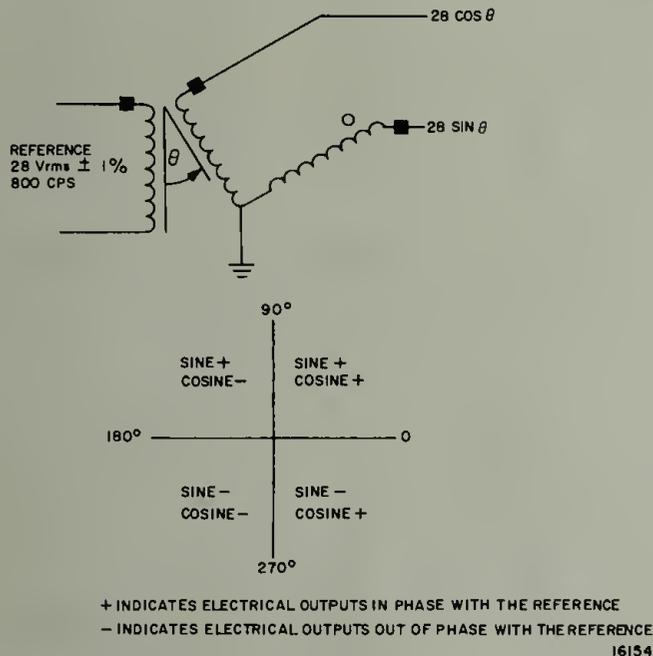
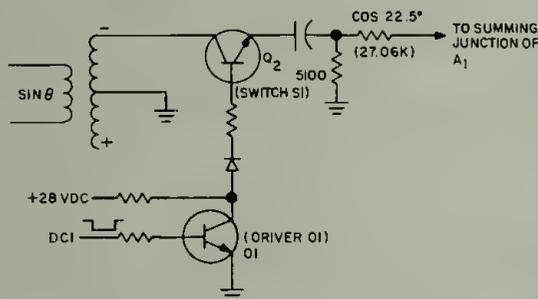


Figure 4-11. Resolver Sine and Cosine Phase Relationships

the signal would be equivalent to $(-4 \text{ v rms}) (-0.866) = 3.46 \text{ v (rms)}$, and would be in phase with respect to the 800 cps reference. The minus sign in front of the 4 v (rms) signifies that the out of phase portion of the transformer secondary was used. The signal from each portion of the T2 and T3 secondary windings is applied to two transistorized switches. The circuit for one of the switches, S1, is shown in figure 4-12. The circuit consists of switching transistor Q2 and the transistor driver Q1. When the logic equation for switch control signal DC1 isn't satisfied, DC1 is at a positive voltage level allowing Q1 to conduct to saturation and thus keep the base of Q2 grounded. With its base grounded, Q2 is turned off (or open) preventing the transformer output signal from being applied to the attenuator resistor circuit labeled $\cos 22.5^\circ$. When its logic equation is satisfied, DC1 drops to 0 vdc, Q1 stops conducting which allows the base of Q2 to rise toward +28 vdc causing Q2 to conduct to saturation. With Q2 turned on, the transformer output is applied through the attenuator resistor circuit to the summing junction of operational amplifier A1. All of the coarse system module switches (S1 through S12) operate in an identical manner. The logic equations for the switch control signals (DC1 through DC12) that activate the switches are also given on figure 4-12.



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$$\begin{array}{ll}
 \text{DC1} = \overline{2^{15} 2^{14} 2^{13}} - 2^{15} \overline{2^{14} 2^{13}} & \text{DC7} = 2^{15} (2^{14} 2^{13}, \overline{2^{14} 2^{13}}) \\
 \text{DC2} = \overline{2^{15} 2^{14} 2^{13}} - 2^{15} 2^{14} 2^{13} & \text{DC8} = \overline{2^{15} (2^{14} 2^{13}, 2^{14} 2^{13})} \\
 \text{DC3} = 2^{15} \overline{2^{14} 2^{13}} - 2^{15} 2^{14} 2^{13} & \text{DC9} = 2^{12} \\
 \text{DC4} = \overline{2^{15} 2^{14} 2^{13}} - 2^{15} 2^{14} 2^{13} & \text{DC10} = 2^{11} \\
 \text{DC5} = \overline{2^{15} (2^{14} 2^{13}, 2^{14} 2^{13})} & \text{DC11} = 2^{10} \\
 \text{DC6} = \overline{2^{15} (2^{14} 2^{13}, 2^{14} 2^{13})} & \text{DC12} = 2^9
 \end{array}$$

Figure 4-12. Coarse Switch Circuit and Logic Equations

Switches S1 through S8 mechanize the systems nulling identity, $\pm \sin(\theta - \psi) = \pm \sin \theta \cos \psi \pm \cos \theta \sin \psi$, directly by switching the $\sin \theta$ and $\cos \theta$ signals from the transformer secondaries through the attenuator resistors which represent values of $\sin \psi$ and $\cos \psi$. At the same time the switches select either the in phase, or out of phase transformer output so that the attenuated signals will always be out of phase with respect to each other at the summing junction and thus be consistent with the requirements of the nulling identity. To develop the signal equivalent to the $\sin \theta \cos \psi$ term of the identity, a single switch from the S1 through S4 group of switches will be closed to select either the in phase or out of phase $\sin \theta$ signal and connect it to an attenuator resistor circuit representing either $\cos 22.5$ degrees or $\cos 67.5$ degrees. The $\cos \theta \sin \psi$ signal is developed in the same manner by a single switch in the S5 through S8 group. The transformer outputs selected in each case will cause the $\sin \theta \cos \psi$ and the $\cos \theta \sin \psi$ signals to be out of phase with respect to each other at the summing junction. When the two attenuated signals are summed together at the summing junction, a difference or resultant voltage is developed which represents the $\sin(\theta - \psi)$ side of the identity. The S1 through S8 switches can select values of ψ to match the gimbal angle to within 22.5 degrees. The resultant voltage, therefore, may be a maximum of $(\pm 4 \text{ v rms}) (\sin 22.5^\circ) = \pm 1.53 \text{ v (rms)}$.

The resultant voltage can be nulled out by summing it with voltage increments of proper phase supplied by the voltage ladder formed by switches S10, S11, and S12. The ladder, in effect, performs a linear interpolation to match the difference angle

($\theta - \psi$) to within 2.8 degrees in steps of 2.8 degrees. The ladder switches are activated by switch control signals from the 2^9 , 2^{10} , and 2^{11} stages of the read counter. The signal input to the ladder switches is from the out of phase secondary of the 800 cps reference transformer T3. The remaining switch, S9, is controlled by the 2^{12} stage of the read counter and supplies an in phase reference signal to the summing junction. The operation of the S9 switch will be discussed in more detail later.

The coarse system switches activated at any particular gimbal angle can be determined by first determining what read counter stages will have accumulated bits (see figure 4-9) and applying this information to the logic equations given in figure 4-12 to determine what switch control signals will be generated. A simpler and more convenient method is provided by the coarse switching diagram given in figure 4-13.

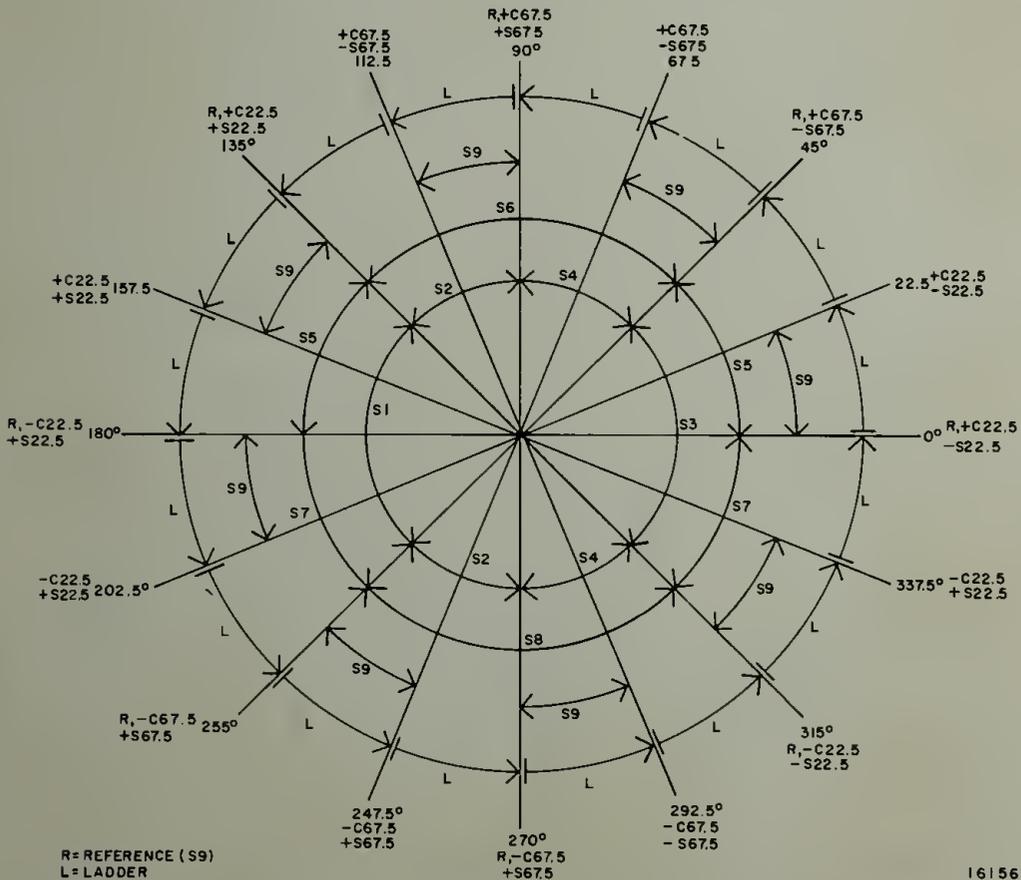


Figure 4-13. Coarse Switching Diagram

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The coarse switching diagram illustrates the range of gimbal angles over which each switch is closed. The S and C designations indicate a sine and cosine attenuator resistor, respectively, with the value of the attenuator resistor given after the designator. The plus and minus signs signify the polarity of the transformer secondary the attenuator resistor is connected to. The R designation indicates the closure of switch S9. The L designation indicates the closure of one or more of the ladder switches.

A gimbal angle which illustrates the operation of switches S1 through S8 is 67.5 degrees. A gimbal angle of 67.5 degrees ($45^\circ + 22.5^\circ$) places a bit in read counter stages 2^{12} and 2^{13} (see figure 4-9) and satisfies the logic equations for DC4 and DC6 (see figure 4-12), which close switches S4 and S6. The coarse switching diagram verifies the closure of a +C67.5 and a -S67.5 switch which correspond to switches S4 and S6. The voltages present at the summing junction as a result of the closure of switches S4 and S6 are:

$$\begin{aligned} (S4) (4 \text{ v rms}) (\sin 67.5^\circ) (\cos 67.5^\circ) &= \\ (4 \text{ v rms}) (0.924) (0.383) &= 1.42 \text{ v rms} \\ (S6) (-4 \text{ v rms}) (\cos 67.5^\circ) (\sin 67.5^\circ) &= \\ (-4 \text{ v rms}) (0.383) (0.924) &= -1.42 \text{ v rms} \end{aligned}$$

The two voltages are equal in amplitude but opposite in phase and therefore cancel and a null is accomplished.

A gimbal angle which illustrates the use of the ladder is 28.1 degrees. A gimbal angle of 28.1 degrees ($22.5^\circ + 5.6^\circ$) places a bit in read counter stages 2^{12} and 2^{10} satisfying the logic equations for DC3, DC5, and DC11 which close switches S3, S5, and ladder switch S11, respectively. The coarse switching diagram verifies that switch S3 (+ cos 22.5°), S5 (-sin 22.5°), and the ladder are actuated. The voltages present at the summing junction as a result of the closure of switches S3 and S5 are:

$$\begin{aligned} (S3) (4 \text{ v rms}) (\sin 28.1^\circ) (\cos 22.5^\circ) &= \\ (4 \text{ v rms}) (0.471) (.924) &= 1.74 \text{ v rms} \\ (S5) (-4 \text{ v rms}) (\cos 28.1^\circ) (\sin 22.5^\circ) &= \\ (-4 \text{ v rms}) (0.882) (.383) &= -1.35 \text{ v rms} \end{aligned}$$

The resulting in phase voltage from the S3 and S5 closure is 0.39 v (rms). To null the system, this in phase voltage must be summed with an out of phase signal. With ladder switch S11 closed, an out of phase voltage equivalent to $(-4 \text{ v rms}) (\sin 5.62^\circ) = -0.39 \text{ v (rms)}$ is applied to the summing junction to establish a null.

When the resultant signal at the summing junction due to the switch closures in the S1 through S8 group of switches is an out of phase voltage, operation of the ladder switches, which always provide out of phase voltages, will aggravate the unnull condition. An in phase signal is required at the summing junction with which the ladder signals can be summed to obtain a null. This required in phase signal is provided by switch S9 and the + reference side of transformer T3 as shown on figure 4-10. Switch S9 is activated on alternate 22.5 degree segments, as shown on the coarse switching diagram, because it is in those segments that switches S1 through S8 can produce an out of phase resultant. Switch S9 provides a signal equivalent to (4 v rms) (sin 22.5) = 1.53 v (rms) which, in effect, inverts the out of phase resultant to an in phase signal so that the out of phase ladder signals can accomplish a null. Expressing the function of switch S9 in another way would be to say that it creates the effect of a 22.5 degree shift in gimbal angle.

A gimbal angle which would illustrate the use of switch S9 as well as the ladder is 239.1 degrees. A gimbal angle of 239.1 degrees ($180^\circ + 45^\circ + 11.25^\circ + 2.8^\circ = 239.05^\circ$) places a bit in read counter stages 2^{15} , 2^{13} , 2^{11} , and 2^9 . Bits in these positions satisfies the logic equations for DC2, DC8, DC10 and DC12, closing switches S2, S8, S10, and S12. The absence of a bit in read counter stage 2^{12} satisfies the logic equation for DC9 which closes switch S9. The sine and cosine of 239.1 degrees are both negative since the angle lies in the third quadrant. The voltages present at the summing function as a result of switches S2 and S8 being closed are:

$$\begin{aligned} (S2) (-4 \text{ v rms}) (-\sin 239.1^\circ) (\cos 67.5^\circ) &= \\ (-4 \text{ v rms}) (-.8581) (.383) &= 1.35 \text{ v (rms)} \\ (S8) (4 \text{ v rms}) (-\cos 239.1^\circ) (\sin 67.5^\circ) &= \\ (4 \text{ v rms}) (-.5135) (.924) &= -1.90 \text{ v (rms)} \end{aligned}$$

The resultant out of phase voltage from the S2 and S8 closure is -0.55 v (rms). It can be seen that summing this voltage with the out of phase voltages from the ladder switches S10 and S12 will increase the out of phase resultant at the summing function. The closure of switch S9, however, provides the necessary in phase voltage value to obtain a null. Summing the in phase S9 voltage with the out of phase resultant provides a new resultant of $1.53 - 0.55 = 0.98$ v (rms). The voltages present as a result of the S10 and S12 closures are:

$$\begin{aligned} (S10) (-4 \text{ v rms}) (\sin 11.25^\circ) &= \\ (-4 \text{ v rms}) (1.95) &= -0.78 \text{ v (rms)} \\ (S12) (-4 \text{ v rms}) (\sin 2.8^\circ) &= \\ (-4 \text{ v rms}) (.049) &= -0.20 \text{ v (rms)} \end{aligned}$$

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Summing the total ladder signal with the S2, S8, and S9 resultant ($0.98 - 0.98 = 0$ v rms) establishes a null.

In order for the system to be nulled, the voltage at the summing junction of amplifier A1, must be low enough to keep the amplifier output ($E_{out} = E_{in} \times \text{gain}$) below the triggering level of the schmitt trigger error detector. The amplifier output is referred to as the coarse error signal. When the system is not nulled, the coarse error is large enough (1.33 volts peak-peak nominal) to cause the error detector to fire and to generate an 800 cps square wave output. The 800 cps output, referred to as the coarse ternary level signal (C1), is sent to the read counter logic section of the error counter and logic module. The coarse ternary level will exist when the error ($\theta - \psi$) is greater than approximately 5 degrees. The logic within the error counter and logic module sends pulses at 12.8 kpps to count the read counter up or down. If the coarse ternary level signal is out of phase with respect to an 800 cps square wave reference signal in the logic, the logic causes the read counter to be counted down and in like manner counts the read counter up if the coarse ternary level signal is in phase. The read counter, in turn, will change the configuration of the coarse system switches, choosing different attenuation values ($\sin \psi$ and $\cos \psi$) until $\theta = \psi$ and the system is nulled. The coarse error signal is also supplied to the mode module fail detect circuits where it is monitored and to the CDU test point connector for external monitoring purposes. The coarse system module also performs two additional functions: generates the ambiguity detect signal (A_d) and the IMU cage signal. The IMU cage signal is taken from a separate secondary winding of the $\sin \theta$ transformer T1 and is used during the IMU cage mode to drive the gimbals to their zero positions. To develop the ambiguity detect signal, the output of a separate secondary winding on the $\cos \theta$ transformer, T2, is applied through an emitter follower to a schmitt trigger which fires when its input exceeds a nominal value of approximately 6 volts (p-p). The schmitt trigger output is an 800 cps square wave, which will exist when the gimbal angle is between 125 degrees and 235 degrees. The ambiguity detect signal is sent to the ambiguity logic circuit in the digital mode module to indicate the possibility of a false or ambiguous gimbal angle.

4-4.2 QUADRANT SELECTOR MODULE. The quadrant selector module functions with the MSA & QR and with the read counter module to form the fine analog to digital conversion system. The quadrant selector module inverts the 16X resolver sine or cosine signals as necessary, depending on the quadrant the resolver angle lies in, so that they are always out of phase with respect to each other. A second function of the quadrant selector module is the generation of an 800 cps reference signal.

In order to implement the nulling identity,

$$\pm \sin (\theta - \psi) = \pm \sin \theta \cos \psi \pm \cos \theta \sin \psi$$

for the fine analog to digital conversion system, the $\sin \theta$ and $\cos \theta$ signals from the 16X gimbal angle resolver must be switched so that they are always out of phase with respect to each other. Figure 4-11 shows that the resolver signals are out of phase with each other only in quadrants II and IV. The quadrant selector will invert

the $\sin \theta$ signal in quadrants I and IV, and invert the $\cos \theta$ signal in quadrants III and IV. Figure 4-14 is a block diagram of the quadrant selector module. The switch driver circuits and associated switch control signals which operate the various quadrant selector switches are not shown.

The inversion of the $\sin \theta$ signal is accomplished by operational amplifiers A1 and A2 and switches S5 and S6 in the following manner. Switch S6 is closed and S5 is opened to provide a feedback path around A2 through R9 and to disconnect the output of A2 from the input of A1. The $\sin \theta$ signal, applied to A1 through R1, is inverted by the normal operation of A1 and the desired inverted $\sin \theta$ signal is made available at its output. When no inversion is required, the switch configuration is changed to S5 closed and S6 opened. The feedback path around A2 is closed through R4 and the output of A2, which is also inverted, is applied to the input of A1 through R2. Since the resistance of R2 is half that of the feedback resistor of A1, an inverted $\sin \theta$ signal of twice normal amplitude is applied to the summing junction input of A1. When this signal is summed with the in phase $\sin \theta$ signal from R1, the resultant signal is an inverted $\sin \theta$ signal of normal amplitude. The inverted $\sin \theta$ signal is again inverted by A1 to re-establish an in phase $\sin \theta$ signal at its output.

Switches S5 and S6 are closed when the following logic equations are satisfied:

$$S5 = 2^{10} \overline{2^{11}} + \overline{2^{10}} 2^{11}$$

$$S6 = 2^{10} 2^{11} + \overline{2^{10}} \overline{2^{11}}$$

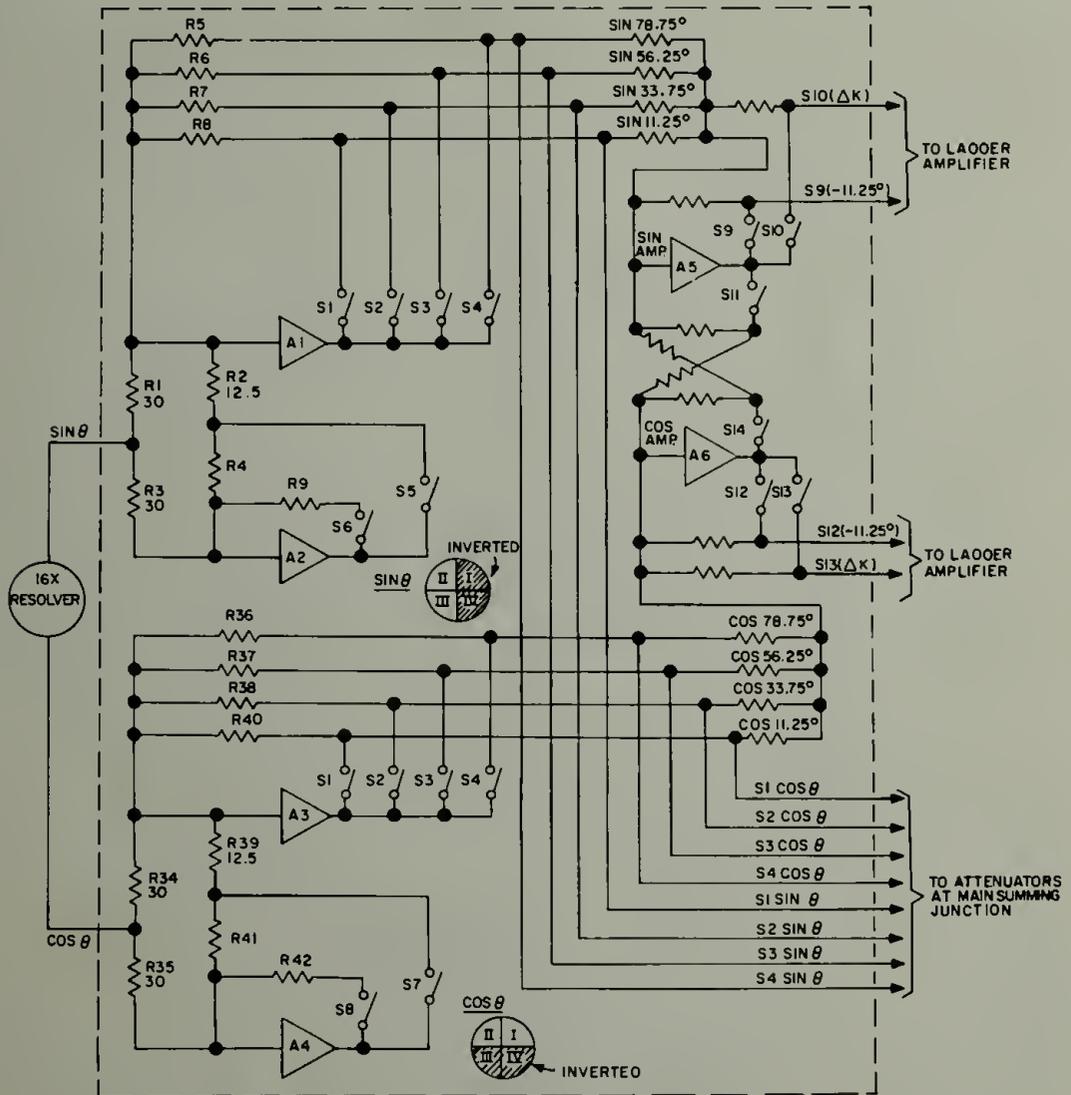
The 2^{11} stage of the read counter corresponds to 180 electrical degrees in the fine system and the 2^{10} stage corresponds to 90 electrical degrees. The logic equations then state that S5 is closed when the angle ψ is between 90 degrees and 180 degrees ($2^{10} \overline{2^{11}}$) or between 180 degrees and 270 degrees ($\overline{2^{10}} 2^{11}$) which are the II and III quadrants, respectively. S6 is closed when ψ is between 270 degrees and 360 degrees ($2^{10} 2^{11}$) or between 0 degrees and 90 degrees ($\overline{2^{10}} \overline{2^{11}}$) which are the IV and I quadrants, respectively.

Phasing of the $\cos \theta$ signal is performed in the same manner as the $\sin \theta$ signal using A3, A4, S7, and S8. The $\cos \theta$ signal is inverted in the III and IV quadrants. The logic equations for S7 and S8 are:

$$S7 = \overline{2^{11}}$$

$$S8 = 2^{11}.$$

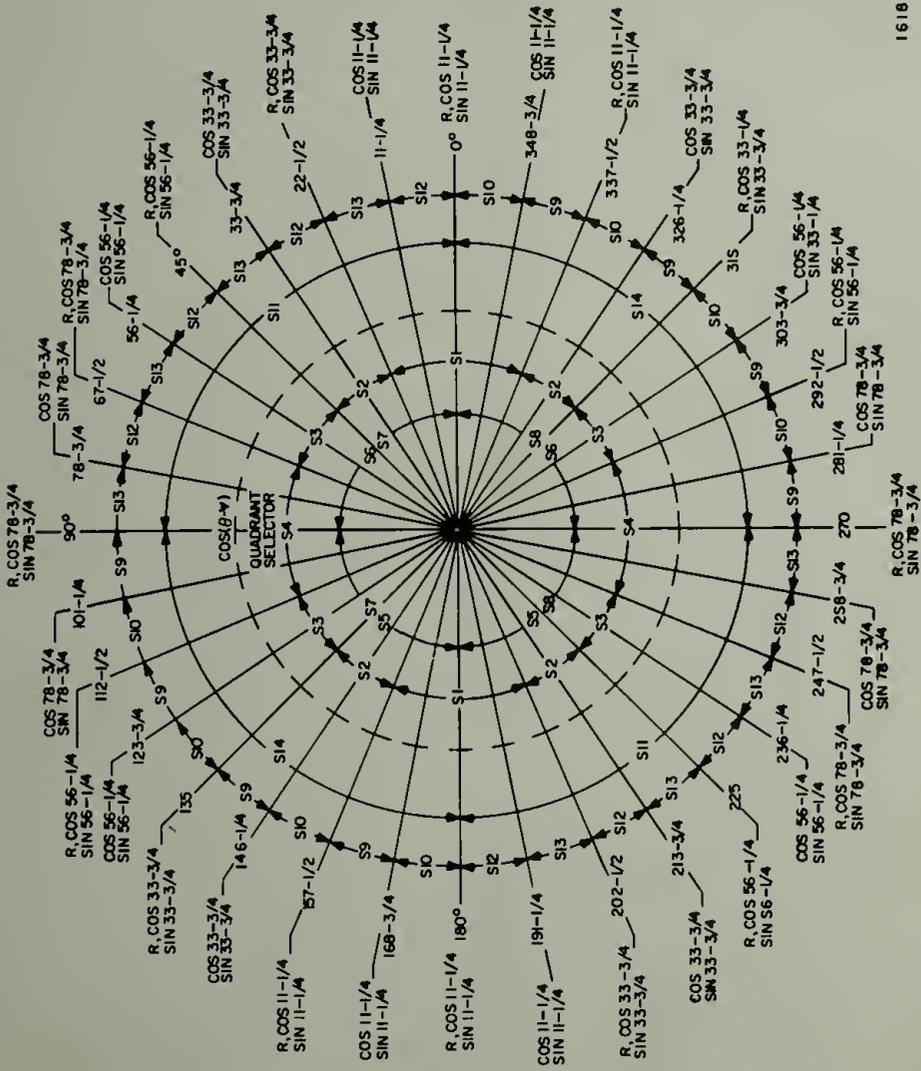
S8 will be closed and S7 will be open when ψ is between 180 degrees and 360 degrees (2^{11}) providing an inverted $\cos \theta$ signal at the output of A3. S7 is closed and S8 is open when ψ is between 0 degrees and 180 degrees ($\overline{2^{11}}$) providing a non-inverted signal at the output of A3. Figure 4-15 illustrates which of the S5 through S8 group of switches are closed over the various segments of 360 electrical degrees of 16X resolver rotation.



ALL UNSPECIFIED RESISTORS ARE 25K ALL VALUES ARE IN K Ω . REFERENCE DESIGNATIONS CORRESPOND TO SCHEMATIC 2010059.

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Figure 4-14. Quadrant Selector Module, Block Diagram



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Figure 4-15. Fine Switching Diagram

Switches S1 through S4 select resistance values located in the MSA & QR which attenuate the properly phased sine and cosine signals at the inputs of the MSA & QR. The accumulation of bits in the twelve least significant stages of the read counter controls all switches in the fine system. At any angle, one and only one switch of the four (S1 through S4) is on, selecting the appropriate value of attenuation. The values of attenuation selected by each switch is given below:

- (S1) sin 11.25 degrees and cos 11.25 degrees
- (S2) sin 33.75 degrees and cos 33.75 degrees
- (S3) sin 56.25 degrees and cos 56.25 degrees
- (S4) sin 78.75 degrees and cos 78.75 degrees

If the resolver angle θ were equal to any of the exact values given above or to quadrature multiples, a null would be accomplished at the summing junction of the main summing amplifier in the MSA & QR module without the benefit of any additional signals. As an example, assume an angle of 213.75 degrees (equivalent to 33.75 degrees) exists at the resolver. The sin 213.75 degree signal is a negative quantity (out of phase) as is the cos 213.75 degree signal. The sine is not inverted in quadrant III and therefore remains as an out of phase voltage. The cosine is inverted in quadrant III and the out of phase cos 213.75 degree signal becomes an in phase voltage. At this value of θ , switch S2 will be closed and the result at the main summing junction would be:

$$(\sin 213.75^\circ) (\cos 33.75^\circ) - (\cos 213.75^\circ) (\sin 33.75^\circ) = 0$$

and the desired null would be accomplished. If the resolver angle is not equal to any of the attenuation values, or their quadrature multiples, the required attenuation cannot be accomplished by switches S1 through S4 alone. Additional switching is then performed in the MSA & QR module ladder circuits. The logic equations mechanized to control the operation of switches S1 through S4 are as follows:

$$\begin{aligned} S1 &= 2^8 2^9 2^{10} + \overline{2^8} \overline{2^9} \overline{2^{10}} \\ S2 &= \overline{2^8} 2^9 2^{10} + 2^8 \overline{2^9} \overline{2^{10}} \\ S3 &= 2^8 \overline{2^9} 2^{10} + \overline{2^8} 2^9 \overline{2^{10}} \\ S4 &= \overline{2^8} \overline{2^9} 2^{10} + 2^8 2^9 \overline{2^{10}} \end{aligned}$$

Figure 4-15 illustrates which of the S1 through S4 switches are closed over the various segments of 360 electrical degrees of 16X resolver rotation.

Switches S1 through S4 also select attenuation values at the inputs of the sine and cosine amplifiers for use in generating an 800 cps reference signal. In obtaining a null at the main summing amplifier, it is necessary to supply a reference signal to the ladder network that is in phase with respect to the external 800 cps reference input of the resolver. This reference is equivalent to $\cos(\theta - \psi)$ and is generated in the quadrant selector module by solving the trigonometric identity:

$$\cos(\theta - \psi) = \sin \theta \sin \psi + \cos \theta \cos \psi$$

The reference identity is mechanized by the sine amplifier A5, the cos amplifier A6, and switches S9 through S14. The reference identity implies that the sine and cosine signals from the resolver must always be in phase with respect to each other, in contrast to the nulling identity which required the signals to be out of phase with respect to each other. In solving the reference identity it is necessary to re-phase the sine and cosine signals so that they are always in phase and consistent with the equation.

The inputs to the sine amplifier are the attenuated $\sin \theta$ signals from switches S1 through S4, the values of which are $\sin \theta \sin 11.25^\circ$, $\sin \theta \sin 33.75^\circ$, $\sin \theta \sin 56.25^\circ$, and $\sin \theta \sin 78.75^\circ$, respectively. The inputs to the cosine amplifier are the attenuated $\cos \theta$ signals from switches S1 through S4, the values of which are $\cos \theta \cos 11.25^\circ$, $\cos \theta \cos 33.75^\circ$, $\cos \theta \cos 56.25^\circ$, and $\cos \theta \cos 78.75^\circ$, respectively. It should be remembered that only one of the four switches can be closed at any particular time and the sine and cosine signals are always out of phase with respect to each other at the inputs to the sine and cosine amplifiers.

The sine and cosine amplifiers each have two outputs which may be switched to the ladder amplifier in the MSA & QR module but the switching logic allows the selection of only one of the four outputs at any particular time. Switch S11 switches the output of the sine amplifier to the input of the cosine amplifier and S14 switches the output of the cosine amplifier to the input of the sine amplifier. Switches S11 and S14 are never closed at the same time. Switch S11 is closed when the angle θ is in quadrant I or III; switch S14 is closed when the angle θ is in quadrant II or IV. Both the sine and cosine amplifiers invert their input signals. The effect is to have one amplifier invert the S1 through S4 input signal that is out of phase with respect to the external 800 cps reference, sum it with the in phase S1 through S4 signal and invert the resultant signal to an out of phase signal at the output of the second amplifier. Switches S9 and S10 switch the sine amplifier outputs to the ladder amplifier and switches S12 and S13 switch the cosine amplifier outputs to the ladder amplifier. Switches S9 and S10 alternate on and off every 11.25 degrees in the second and fourth quadrants (at which time S14 is closed) and switches S12 and S13 alternate on and off in the first and third quadrants (at which time S11 is closed). One output, therefore, is always present at the input to the ladder amplifier. The output signal switched to the ladder amplifier is always out of phase with respect to the external reference and when it is inverted by the ladder amplifier it becomes the in phase $\cos(\theta - \psi)$ reference signal required at the ladder network. The $\cos(\theta - \psi)$ signal is of approximately constant amplitude for all inputs to the $\cos(\theta - \psi)$ generator circuit.

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The logic equations mechanized to control the switching in the $\cos(\theta - \psi)$ generator are as follows:

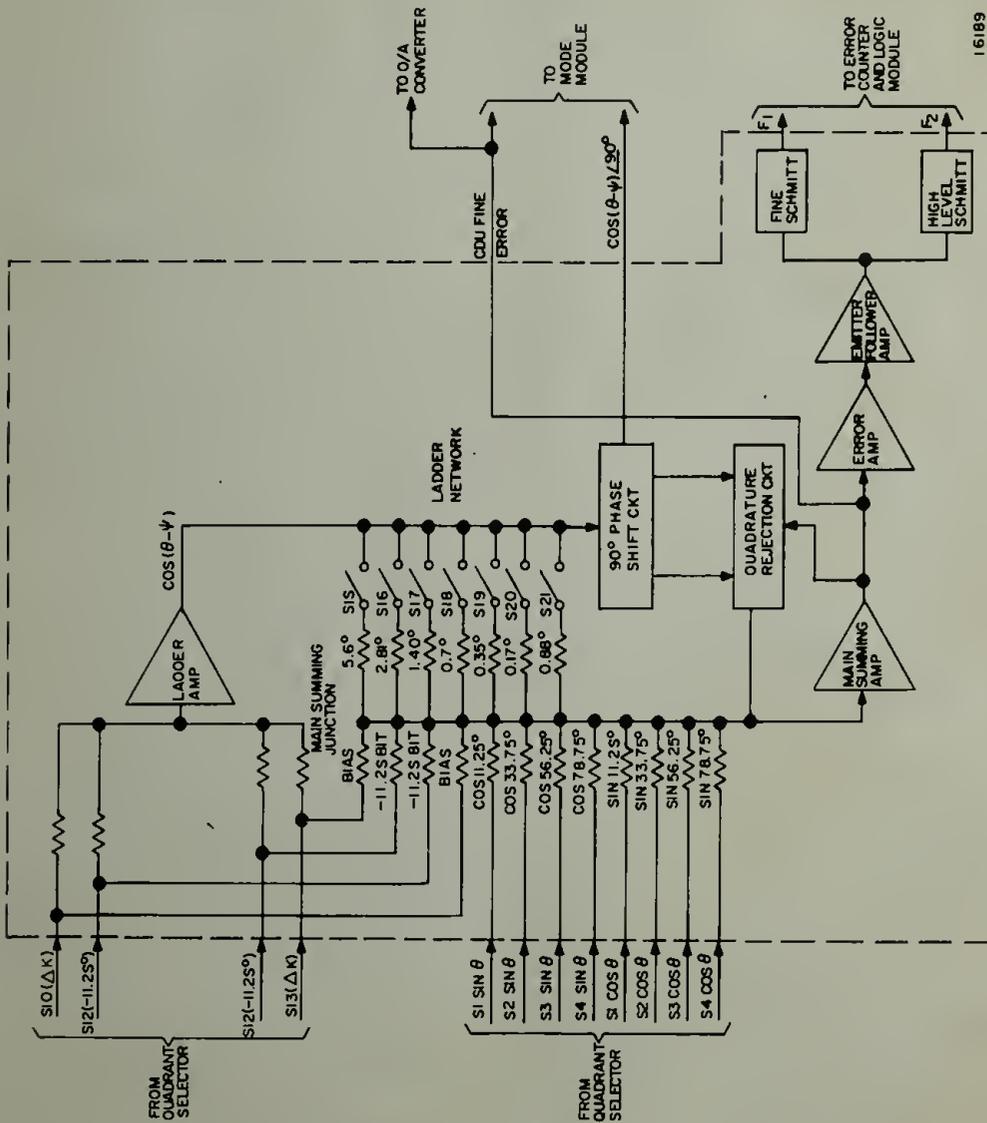
$$\begin{aligned} S9 &= \overline{2^7} 2^{10} & S12 &= \overline{2^7} \overline{2^{10}} \\ S10 &= 2^7 2^{10} & S13 &= 2^7 \overline{2^{10}} \\ S11 &= \overline{2^{10}} & S14 &= 2^{10} \end{aligned}$$

Figure 4-15 illustrates the operation of these switches through 360 electrical degrees of 16X resolver rotation.

The switches that connect the sine or cosine amplifier outputs to the ladder amplifier also connect these outputs to attenuator resistors at the main summing junction of the main summing amplifier to establish at the junction either a bias signal or an out of phase reference signal corresponding to -11.25 degrees. Switches S9 and S12 provide inputs to the -11.25 degree attenuator resistor. This signal, which is referred to as the -11.25 degree bit, performs a function similar to that performed by the signal from switch S9 in the coarse module. Switches S10 and S13 provide inputs to the bias attenuator. The bias signal, also referred to as a ΔK signal, is applied to the summing junction to minimize any error generated by the implementation of the $\cos(\theta - \psi)$ equation. Both the -11.25 bit and the bias signal are further discussed in the MSA & QR module discussion.

4-4.3 MAIN SUMMING AMPLIFIER AND QUADRATURE REJECTION MODULE. The MSA & QR module functions with the quadrant selector module and the read counter module to form the fine analog to digital conversion system. The MSA & QR performs three functions: summing, quadrature rejection, and generation of the F_1 and F_2 ternary level signals. A block diagram of the MSA & QR module is given in figure 4-16.

In the summing operation, the signals from the quadrant selector module are summed at the main summing junction with the output of the ladder network and the output of the quadrature rejection circuit. The signals from the quadrant selector module are the two signals supplied through the operation of switches S1 through S4 that are always out of phase with respect to each other and, secondly, either the -11.25 degree bit signal or the bias signal from amplifiers A5 or A6. Both the -11.25 degree bit signal and the bias signal are out of phase with respect to the 800 cps reference. If a gimbal angle θ exists that is not an exact multiple of 11.25 degrees, the main summing junction cannot be nulled by the operation of switches S1 through S4 alone. If this condition exists, an in phase signal from the ladder amplifier is supplied through switches S15 through S21 to null the signal at the main summing junction. Switches S15 through S21 are controlled by the accumulation of bits in the 2^0 through 2^6 stages of the read counter. The in phase signal from the ladder network is the $\cos(\theta - \psi)$ reference generated in the quadrant selector module and inverted



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Figure 4-16. Main Summing Amplifier and Quadrature Rejection Module, Block Diagram

by the ladder amplifier. The result of the summation of these signals, with the aid of the quadrature rejection circuit, is about a six millivolt rms null at the output of the main summing amplifier.

To illustrate the summing operation, assume the angle registered by the read counter, ψ , is between 0 and 11.25 electrical degrees. Since the angle lies in the first quadrant, the in phase and relatively small $\sin \theta$ signal is inverted by the quadrant selector and is attenuated by a factor equivalent to $\cos 11.25$ degrees at the main summing junction. The in phase and relatively large $\cos \theta$ signal is attenuated by a factor equivalent to $\sin 11.25$ degrees at the main summing junction. The resultant voltage of these two signals from the quadrant selector is an in phase voltage which must be summed with an out of phase voltage to obtain a null. If the in phase voltage from the ladder switches were summed with the in phase resultant from the quadrant selector signals, the in phase resultant would be increased, aggravating the unnullled condition. The out of phase voltage necessary to accomplish a null is provided by the -11.25 degree bit signal. The effect of this signal is to invert the resultant from the quadrant selector signals to an out of phase voltage which may be nulled out with increments of in phase voltage from the ladder. The -11.25 degree bit signal performs the same function as the S9 reference signal in the coarse system module.

If ψ is between 11.25 and 22.50 electrical degrees, quadrant selector switch S12 is open and S13 is closed which removes the -11.25 degree bit signal and applies the bias signal to the summing junction. The resultant voltage of the quadrant selector signals will always be an out of phase voltage. The in phase voltage increments from the ladder switches null out the out of phase resultant and the bias signal minimizes errors.

The bias signal minimizes errors incurred in the implementation of the $\cos(\theta - \psi)$ equation. During those times that the -11.25 degree bit signal is switched in and the bias signal is absent, a similar bias is provided through the gain of the ladder amplifier.

As the angle ψ becomes greater, the operation described repeats with S12 and S13 alternating on and off every 11.25 degrees. In the second quadrant, the operation continues with switches S9 and S10 alternating on and off. In the third quadrant, switches S12 and S13 again are operational and in the fourth quadrant, S9 and S10 regain control.

The resolver signals contain a certain percentage of quadrature (reactive) component which, if large enough, could cause the fine schmitt trigger error detector to fire. To eliminate this possibility, a quadrature reject circuit is incorporated into the MSA & QR module. The quadrature component is rejected by taking the $\cos(\theta - \psi)$ output of the ladder amplifier and phase shifting it 90 degrees to obtain a $\cos(\theta - \psi) / 90^\circ$ signal which is used as a reference for a phase sensitive demodulator and a modulator (chopper). The 800 cps output of the main summing amplifier is sampled, amplified, and applied to the phase sensitive demodulator. If the main summing amplifier output contains any quadrature component, this value will be demodulated

and allowed to charge a capacitor in a filter circuit. If the output of the main summing amplifier is an out of phase voltage, the dc charge on the capacitor will be negative. If the output of the main summing amplifier is an in phase voltage, the dc charge on the capacitor will be a positive potential.

The dc charge on the capacitor is applied as an input to the chopper which is keyed by the $\cos(\theta - \psi) \angle 90^\circ$ signal. The modulated output from the chopper is 180 degrees out of phase with respect to the quadrature component. The chopper output is amplified and applied to the main summing junction where it tends to oppose any quadrature component present at the summing junction. The $\cos(\theta - \psi) \angle 90^\circ$ signal is also sent to the fail detect circuits in the mode module for internal monitoring purposes.

The main summing amplifier output is applied to an error amplifier. The output of the error amplifier is applied to two schmitt triggers. One schmitt trigger generates an 800 cps square wave output, referred to as the high ternary level signal F_2 , which is applied to the read counter logic section of the error counter and logic module causing the read counter to be incremented at a high rate (12.8 kpps). The second schmitt trigger generates an 800 cps square wave output, referred to as the fine ternary level signal F_1 , which causes the read counter to be incremented at a low rate (800 pps). The high level schmitt trigger will fire whenever the error amplifier output is greater than 4 v peak to peak nominal. When the read counter is within 20 bits (approximately 0.1 degree) of reading the gimbal angle, the high level schmitt trigger ceases to fire and the fine schmitt trigger takes over to cause the read counter to be incremented at the low rate. As long as the error signal is large enough (two bits or greater from null) to fire the fine schmitt trigger, the system will not be nulled and incrementing pulses will be sent to the read counter. The read counter will change the switching configuration to select different values of ψ until ψ is within two bits of equaling θ . When this match occurs, the output of the error amplifier will have been reduced to below the 200 millivolt peak to peak nominal triggering level of the fine schmitt trigger and the system will be nulled.

The output of the main summing amplifier is referred to as the fine error signal and is equivalent to $\sin 16(\theta - \psi)$. This signal is applied to the fail detect circuits in the mode module for internal monitoring purposes. The fine error is also amplified, buffered, and routed to a test point on the CDU test connector for external monitoring purposes. The fine error signal is also sent to the D/A converter module where it is used as a gimbal rate limiting signal during the ISS coarse align and turn on modes of operation.

4-4.4 READ COUNTER MODULE. The read counter module consists of the read counter and associated buffer units and switch logic.

The read counter contains 16 identical stages allowing each bit in the counter to be equivalent to approximately 20 arc-seconds. The output of the first stage, 2^0 , equivalent to approximately 40 arc-seconds, is sent to the LGC. The read counter can count up or down. The accumulation of bits in the counter represents ψ (CDU angle) which the CDU is attempting to match to θ (desired angle). The content of the read counter is buffered and used as inputs to the switch logic in the coarse system module, quadrant selector module, and MSA & QR.

4-4.5 ERROR ANGLE COUNTER AND LOGIC MODULE. The error angle counter and logic module contains the error counter and associated logic, error and rate selection logic, and read counter control logic.

4-4.5.1 Error Selection Logic. The error selection logic tests the fine ternary level (F₁) from the main summing amplifier and the coarse ternary level (C₁) from the coarse module. At interrogate time, the logic produces a selected error signal (S) having the same time phase as the selected ternary level signal but inverted. The coarse ternary level (C₁) has priority and, at interrogation, a high speed clamp signal is produced. The high speed clamp causes the rate select logic to count the read counter at high speed (12.8 kpps). The clamp also initiates the inhibit next interrogate logic which inhibits the interrogation of the coarse ternary level signals at the next interrogate time. The coarse ternary level remains in control until the error angle (difference between CDU angle and desired angle) is small enough to allow the fine system to take over control.

4-4.5.2 Inhibit Next Interrogate Logic. The purpose of the inhibit next interrogate logic is to prevent constant interrogation and thus prevent the system from operating erratically up and down when coarse and fine ternary levels of opposite phase are present. The logic provides the error selection logic with a clamp signal at the next interrogate time. Operation of the logic is dependent upon the coarse ternary level detection and phase pulses I₂ and I₃.

4-4.5.3 Rate Select Logic. The rate select logic provides the proper input pulses for operation of the read counter. The logic selects low speed (800 pps) or high speed (12.8 kpps) inputs to the read counter. The high speed clamp from the error selection logic or high ternary level F₂ from the main summing amplifier will initiate the high speed rate. The low rate is provided by the 800 pps output of the auxiliary clock. Ambiguity override signal A₀ forces the rate select logic into high speed.

4-4.5.4 Read Counter Up-Down Logic. The read counter up-down logic tests the phase of the selected error signal generated in the error selection logic and controls the direction in which the read counter will count. The selected error signal is compared with the 800 cps reference signal. A selected error signal in phase with the reference signal causes the counter to count down while a selected error signal out of phase with the reference signal causes the counter to count up. The presence of ambiguity override signal A₀ forces the counter to count down. Read counter pulses and up-down pulses from up-down logic are ANDed and fed to the LGC. Read counter up-down pulses are fed to the error counter input sync logic.

4-4.5.5 Error Counter Input Sync Logic. The error counter input sync logic accepts pulses from the LGC and the read counter up-down logic. To prevent LGC pulses and read counter pulses from occurring simultaneously, an inhibit function is developed which allows LGC pulses priority. The inhibit function is sent to the error counter drive logic where it is further developed and sent to the rate select logic to inhibit pulses to the read counter. When a pulse is being received from the LGC, the read counter and digitizing operation is inhibited.

4-4.5.6 Error Counter Drive Logic. The error counter drive logic provides pulses to the error counter and an inhibit to the read counter when LGC pulses are being accepted. Input pulses to the error counter can originate from the LGC or from the read counter. When input pulses originate from the read counter, the output from the third stage of the read counter is used. The LGC pulses and $\Delta 2^2$ pulses are converted to pulses at $\phi 4$ time for input to the error counter. The change in count direction occurs at $\phi 2$ time and counting occurs at $\phi 4$ time.

4-4.5.7 Error Counter Up-Down Logic. The error counter up-down logic controls the direction in which the error counter will count and determines the phase of the output of the D/A converter. If the error counter is at zero and the next pulse is an up pulse, the D/A converter polarity will be set to "+" and the count-up direction set. If pulses continue, the error counter will continue to count up. When the pulses change to down pulses, the counter will count down, provided the error counter does not contain zero.

4-4.5.8 Error Counter. The error counter has nine identical stages. Its inputs may be LGC pulses or the output of the third stage (2^2) of the read counter. Each pulse sent to the error counter has a weight of 0.044 degree. The error counter can count up or down and is controlled by the error counter up-down logic. Error counter inputs $\phi 2$ and $\phi 3$ are control signals which drive the counter. Bit information is fed through buffer circuits in the error counter to the D/A converter as switch commands.

4-4.6 DIGITAL MODE MODULE. The digital mode module, consists of a clock pulse generator, auxiliary clock, 25.6 kpps generator, ambiguity logic, and pulses after interrogate pulse logic. The digital mode module provides pulse commands which are used throughout the CDU for synchronization, switching, and strobing.

4-4.6.1 Clock Pulse Generator. The clock pulse generator generates the phase pulses required by the CDU. A 51.2 kpps pulse train from the LGC is divided by four. By ANDing appropriate signals, four 3μ sec, 12.8 kpps pulse trains ($\phi 1$, $\phi 2$, $\phi 3$, and $\phi 4$) of different phases are produced. These signals are used throughout the CDU for strobing and control.

4-4.6.2 Auxiliary Clock. The auxiliary clock receives phases $\phi 1$, $\phi 2$, and $\phi 4$ from the clock pulse generator and generates an 800 pps $\phi 4$ signal. The 800 pps $\phi 4$ signal is generated by dividing the normal 12.8 kpps $\phi 4$ signal by 16. The $\phi 1$ and $\phi 2$ signals are control signals which drive the divider. The 800 pps signal provides a low speed counting rate for the rate select logic in the error angle counter and logic module.

4-4.6.3 25.6 KPPS Generator. The 25.6 kpps generator produces a 25.6 kpps drive rate by ANDing two 12.8 kpps pulse trains ($\phi 2$ and $\phi 4$). This 25.6 kpps drive rate is applied to the +4 volt power supply for synchronization.

4-4.6.4 Ambiguity Logic. Ambiguity detect signal Ad from the coarse system module is ANDed with out-of-phase reference pulse R1 and interrogate pulse 1 to produce ambiguity override signal A₀. Signal A₀ is sent to the rate select logic and read counter up-down logic in the error angle counter and logic module. The override signal A₀ forces the rate select logic into high speed (12.8 kpps) and the up-down logic into count-down.

4-4.6.5 Pulses After Interrogate Pulse Logic. The pulses after interrogate pulse logic accepts interrogate pulse I from the interrogate module and phases $\phi 1$ through $\phi 4$ from the clock pulse generator. This logic provides the means of synchronizing interrogate pulse 1 and the 51.2 kpps computer clock pulses by generating phase pulses 1₂ and 1₃ at $\phi 2$ and $\phi 3$ times respectively, after the occurrence of each interrogate pulse. These synchronized pulses are used in the CDU for synchronization and control purposes.

4-4.7 INTERROGATE MODULE. The interrogate module generates a portion of the timing pulses required for CDU operation, produces 14 vdc power, and has pulse driver circuitry for data and pulse transmission. The interrogate module provides the following outputs:

- (1) 51.2 kpps pulse train to the digital mode module.
- (2) 1,600 pps interrogate pulse train used in the CDU ISS channels.
- (3) 800 pps $\angle 0^\circ$ reference signal to the ISS inner, middle, and outer error counter and logic module and to the digital mode module.
- (4) 1,600 pps shaft and trunnion interrogate pulses.
- (5) 800 pps $\angle 0^\circ$ reference signal to the LORS error counter and logic module and the digital mode module.
- (6) 14 vdc power.
- (7) 25.6 kpps pulse train to 4 vdc power supply module.

4-4.7.1 14 VDC Power Supply. The interrogate module contains two identical 14 vdc power supplies. The input power for the power supplies is 28 vdc. The power supply consists of a single transistor whose bias level is controlled by a zener diode. The 14 volt output is taken from the emitter resistor of the transistor. One 14 vdc power supply provides 14 vdc to the mode module, the D/A converter module, and the CDU test connector. The output of the second 14 vdc supply is used entirely within the interrogate module providing 14 vdc to the pulse driver circuits.

4-4.7.2 ISS Reference Generator. The ISS reference generator develops an 800 pps square wave train of zero degree phase for use as a reference by the ISS error counter and logic modules and by the digital mode module. The signal input is voltage from the ISS 28 v (rms), 800 cps, 1 percent power supply applied through a 5 to 1 step down transformer. The positive half cycles are detected and used to drive a transistor. The output of the transistor is an inverted 800 pps square wave.

4-4.7.3 Optics and LORS Reference Generator. The optics and LORS reference generator provides 0 degree phase and 45 degree phase reference signals of 800 pps. The 0 degree phase reference signal is supplied to the LORS azimuth and elevation error counter and logic modules. In the CSM application, this signal is supplied to the optics shaft error counter and logic module. The 45 degree phase reference signal is not used in the LEM application; it is used only in the CSM application for the optics trunnion error counter and logic module. The 0 degree phase reference signal is generated in the same manner as the ISS 0 degree phase reference signal. The 45 degree phase reference signal also is obtained in the same manner except that the phase of the 800 cps signal input is first shifted 45 degrees.

4-4.7.4 ISS Interrogate Generator. The ISS interrogate generator provides a 1,600 pps, 3 microsecond pulse width pulse train to the digital mode module and to the inner gimbal, middle gimbal, and outer gimbal error counter and logic modules.

The input to the ISS interrogate generator is a ISS 28 v (rms), 800 cps voltage which is applied through a 5 to 1 step down transformer. The 5.6 volt signal phase is shifted 90 degrees by a resistance, capacitance, and transistor phase shift network. The phase shifted signal is squared by a diode and used to key a square wave generator. The symmetrical square wave output of the square wave generator is applied to a differentiating circuit where the leading edge of the square wave is differentiated and inverted. The trailing edge of the square wave is differentiated only. In this manner, two signals are obtained which are then combined to key a transistor output stage that develops the 1,600 pps, 3 microsecond pulse width pulse train output.

4-4.7.5 Shaft Interrogate Generator. The shaft interrogate generator provides a 1,600 pps, 3 microsecond pulse width pulse train to the LORS azimuth and elevation error counter and logic module and to the digital mode module in the LEM. In the CSM, the pulse train is supplied to the optics shaft error counter and logic module and to the digital mode module. The operation of the shaft interrogate generator is the same as the ISS interrogate generator.

4-4.7.6 Trunnion Interrogate Generator. The trunnion interrogate generator is not used in the LEM.

4-4.7.7 AGS Pulse Drivers and Logic Circuits. Seven pulse driver circuits in the interrogate module transmit ISS gimbal angle data to the AGS. Six pulse driver circuits transmit $\pm\Delta\theta G$ pulses which represent changes of the inner, middle, and outer gimbal angles. The seventh pulse driver circuit transmits a CDU zero indication to the AGS. The gimbal angle pulse driver circuits receive $\Delta 2^0$ pulses from the read counter, and

up level and down level signals from the error counter and logic module. With the presence of $\Delta 2^0$ pulses and an up level signal, one transistor pulse driver is actuated and $+\Delta\theta G$ pulses, representing increasing gimbal angle, are sent to the AGS. If a down level signal is present, the other pulse driver is activated to send $-\Delta\theta G$ pulses, representing decreasing gimbal angle, to the AGS. The $\pm\Delta\theta G$ pulses are transmitted through 2 to 1 buffer transformers.

The CDU-zero pulse driver transmits a CDU-zero indication consisting of a 51.2 kpps pulse train to the AGS. The application and removal of the CDU-zero indication pulse train provides a zero reference from which the AGS may accumulate the incremental gimbal angle data and thereby obtain initial attitude conditions from the PGNCS.

A 51.2 kpps inverted pulse train from the digital mode module is used with the CDU-zero signal from the mode module to activate a transistor pulse driver circuit. The 51.2 kpps output of the pulse driver is routed to the AGS through a 2 to 1 buffer transformer.

4-4.7.8 Buffer Transformer. A 2 to 1 buffer transformer located in the interrogate module routes the 51.2 kpps pulse train from the LGC to the clock pulse generator in the digital mode module.

4-4.7.9 25.6 KPPS Pulse Driver. The 25.6 kpps pulse driver circuit routes a 25.6 kpps pulse train from the digital mode module to the 4 vdc power supply where it is used for synchronization purposes. The output of the transistor pulse driver is transmitted through a 2 to 1 buffer transformer.

4-4.8 DIGITAL TO ANALOG CONVERTER. The D/A converter converts digital information from the error counter into a dc analog signal and two ac analog signals. One ac signal provides attitude error information to the FDAI. The second ac signal is the coarse align error signal supplied to the gimbal servo amplifiers during the coarse align mode. The dc signal from the three ISS channels of the CDU is not used in the LEM but the same dc signal from the two LORS channels of the CDU provides LEM forward and lateral velocity information to the velocity display meters.

The D/A converter consists of a voltage ladder decoder, a scaling amplifier, a demodulator, and a mixing amplifier. The conversion of digital information into a dc analog signal by the D/A converter is accomplished in essentially two steps. The digital information is first converted into an 800 cycle analog signal by the ladder decoder. The ac signal is then converted to a dc analog signal by a demodulator that rectifies and filters the ac. Before being applied to the demodulator or being used as a direct ac output, the ac signal is routed through the scaling amplifier which controls the gain of the signal. The mixing amplifier combines a feedback signal with the ac analog signal to produce the coarse align error signal.

The D/A converter also contains pulse driver circuits and buffer transformers which route the $\pm\Delta\theta G$ pulses from the read counter through the error counter and logic module to the LGC and route the $\pm\Delta\theta C$ pulses from the LGC to the error counter and logic module.

4-4.8.1 Ladder Decoder. Accumulated data bits in the error counter control the operation of transistor switches that apply either an ac ground or 800 cps of proper phase to the ladder resistors. In this manner, a voltage proportional to the binary configuration of the switches is developed across the ladder network. For simplicity, the operation will be explained using the three bit converter shown at the upper left of figure 4-17; however, the theory of operation presented applies to the nine bit converter employed by the CDU.

Switches S_2 , S_1 , and S_0 represent transistor switches which are activated by three data bits from the error counter. (The switch drive circuitry is not shown.) Switch S_2 is closed by the presence of a bit in the most significant bit position (100) and has a binary weight of 2^2 . Switch S_1 is closed by the presence of a bit in the next most significant bit position (010) and has a binary weight of 2^1 . Switch S_0 is closed by the presence of a bit in the least significant bit position and has a binary weight of 2^0 .

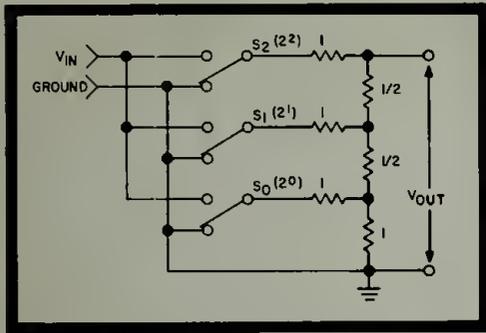
If the data bits from the error counter are 100, switch S_2 is closed and applies the 800 cycle input voltage (V_{IN}) to the ladder. The remaining switches are left in their normally open position and apply ground. The configuration of the ladder resistors is as shown in Case 1 (A) of figure 4-17. The solution of the series and parallel groups of resistances shows the resistance above and below the output point to be 1 (as shown in the equivalent circuit B). Therefore, the input voltage V_{IN} is divided by 2 and applied to the scaling amplifier.

With data bits 010, switch S_1 is closed and the remaining switches open; the resistor configuration is as shown in Case 2 (A) of figure 4-17. Combining series and parallel resistances produces the equivalent circuit progression A through D. The voltage at point a, b is determined first and applied to point b. The simple divider ratio of resistances above and below the output point is then used to find the output voltage as shown in the final equivalent circuit D. The output voltage shows that V_{IN} is divided by 4 and applied to the scaling amplifier.

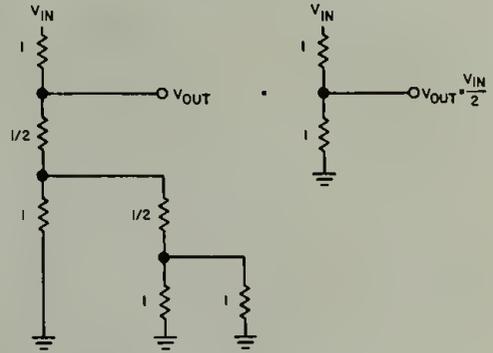
With data bits 001, switch S_0 is closed and the remaining switches open; the resistor configuration is as shown in Case 3 (A) of figure 4-17. Combining series and parallel resistances produces the equivalent circuit progression A through E. The voltage at point ab is found first and applied to point b. In the same manner, the voltage at cd is found and applied to point d. The output voltage is now found from the divider ratio in the final equivalent circuit E. The output voltage shows that V_{IN} is divided by 8 and applied to the scaling amplifier.

If a combination of switches is closed at the same time, the output voltage will be equal to the sum of the voltages found for each switch individually. For example, if switches S_2 and S_0 are closed simultaneously (by data bits 101) the output voltage would be:

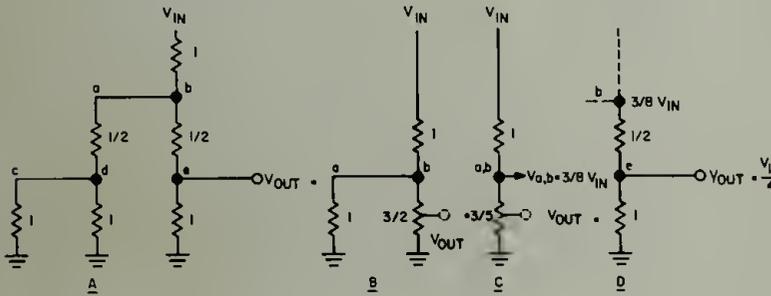
$$\frac{V_{IN}}{2} + \frac{V_{IN}}{8} = \frac{5V_{IN}}{8}$$



SIMPLIFIED 3 BIT CONVERTER



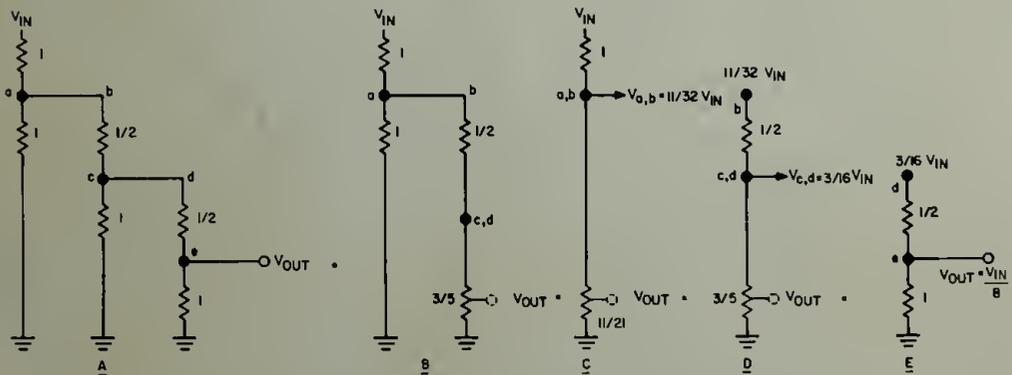
CASE 1. SWITCH S_2 CLOSE



CASE 2. SWITCH S_1 CLOSE

S_2	S_1	S_0	
2^2	2^1	2^0	
0	0	1	$1/8 V_{IN}$
0	1	0	$1/4 V_{IN}$
0	1	1	$3/8 V_{IN}$
1	0	0	$1/2 V_{IN}$
1	0	1	$5/8 V_{IN}$
1	1	0	$3/4 V_{IN}$
1	1	1	$7/8 V_{IN}$

TRUTH TABLE



CASE 3. SWITCH S_0 CLOSE

15755A

Figure 4-17. Simplified 3 Bit Converter and Switch Configurations

The remaining combinations of switch configurations possible from three data bits is shown in the truth table on figure 4-17. In each case, the 800 cycle output has an amplitude proportional to the binary configuration of the data bit controlled switches. The nine bit ladder decoder in the D/A converter provides 2^9 or 512 steps from 0 volts to full output voltage in place of the eight steps provided by the three bit ladder decoder.

In the actual transistor switching circuit (the remainder of the D/A converter discussion will refer to circuitry shown on schematic 2010028), the data bit inputs to switches (DD0, DD1, etc.) are normally at a positive voltage. Therefore, the switch driver Q3 is on and ground is applied to the base of switch Q14 to keep it off. The ac ground is applied to the ladder resistor network through Q15 which is forward biased by the 3.3 volt zener voltage (applied to the emitter) from CR4 and by ground applied to the base. If 0 volts is applied to DD0, Q3 will turn off and Q14 will turn on applying 2.5 volts rms, 800 cycles from T₁ to the ladder. The large positive voltage on the base of Q15 will turn off Q7 removing ac ground from the ladder. The theory of operation is the same for the remaining 8 switches.

The D/A converter receives 9 data bits from the error counter as inputs. The error counter also supplies two polarity control signals (+P_{DA} and -P_{DA}) to the D/A converter. These signals determine if an in phase or an out of phase 800 cycle voltage will be applied to the ladder. This will, in turn, determine the phasing of the D/A converter ac output signals and the polarity of the D/A converter dc output signals. If the +P_{DA} signal (0 volts) is applied to the + D/A polarity input, Q13 turns off and Q12 turns on applying in phase voltage to the ladder. If the -P_{DA} signal (0 volts) is applied to - D/A polarity input, Q1 turns off and Q2 turns on applying out-of-phase voltage to the ladder.

4-4.8.2 D/A Converter Output Stage. The D/A converter output stage consists of the demodulator, the scaling amplifier, and the mixing amplifier. The 800 cycle amplitude modulated signal from the ladder is applied to the scaling amplifier and demodulator where the gain is controlled to produce a voltage gradient of 300 millivolts dc per degree at the output of the D/A converter. In the coarse align mode, the ac voltage from the scaling amplifier is applied as an input to the mixing amplifier.

The scaling amplifier consists of transistors Q33 and Q34 which, along with the feed-back network, form an amplifier with an ac gain of approximately 3 to 4. The output of the scaling amplifier is applied to phase sensitive demodulator through transformer T3. The full-wave rectifiers, which consist of both sections of Q38 and Q39, are controlled by an 800 cycle reference signal through T4. If the ladder output is in phase with the reference signal, a positive error voltage will develop at the output of the rectifier. If the ladder output is 180 degrees out of phase with the 800 cycle reference signal, a negative error voltage output is produced. The emitter to emitter connection of the transistor sections of Q38 and Q39 produces collector to emitter voltage drops of opposite polarity at each transistor section cancelling the overall voltage drop across the two sections of the transistor. The rectified ac is filtered and applied as the D/A converter dc error signal to the LEM velocity display meters. The scaling amplifier also provides an ac analog signal to the FDAI and to the mixing

amplifier in the coarse align mode. Transistor Q32 provides a means of inhibiting the output of the D/A converter even though there is an error accumulation in the error counter. The inhibit action occurs when a positive voltage is applied to the inhibit input causing Q32 to turn on and to short the input of the scaling amplifier to logic ground.

In the coarse align mode, the gimbals are limited to a maximum rate to prevent damage to the gyros and to allow the read counter to track the gimbal angle accurately. The fine error signal, $\sin 16(\theta - \psi)$ from the main summing amplifier, is fed back to rate limit the gimbals. The fine error signal is out of phase with the ladder output and has an amplitude proportional to the difference between the actual gimbal angle and the angle registered in the read counter. The fine error feedback signal is summed with the ac output from the scaling amplifier to provide the input to the mixing amplifier. The output of the mixing amplifier is the coarse align error signal to be applied to the gimbal servo amplifiers during the coarse align mode.

4-4.9 MODE MODULE. The mode module is utilized as an interface module. The mode module contains circuits to buffer signals and monitor CDU operation. Direct interface is made between the mode module and the LGC and with other modules within the CDU. The mode module provides the following:

- a. Buffered moding signals
- b. Four timing signals
- c. ISS and LORS fail signals
- d. 14 vdc power supply output
- e. LEM forward and lateral velocity signals

The mode module contains six general types of circuits, each of which will be discussed.

4-4.9.1 Moding Buffer Circuits. The moding buffer circuits receive signals from the LGC and from the digital mode module. These signals are inverted, amplified or otherwise processed into moding signals to be sent to other modules of the CDU.

The signals received from the LGC are five moding discrettes. The discrettes are 0.0 (± 2) vdc, LGC ground, applied through a 2,000 ohm source impedance. The buffer circuits for four of the discrettes are identical. These discrettes are the ISS CDU zero, LORS CDU zero, ISS error counter enable, and the LORS D/A error counter enable. In each case, the discrete biases a transistor inverter into conduction. The positive dc signal obtained from the inverter is then sent to the moding sync logic of the digital mode module. The fifth discrete, the coarse align enable, has a two stage buffer circuit consisting of an inverter and a relay driver transistor. The inverter has a dual output circuit which provides two positive dc output voltages upon receipt of the coarse align enable discrete from the LGC. One output is sent to the moding sync logic in the same manner as the

previous four moding signals. The second output of the inverter stage is applied to the relay driver transistor, causing it to turn on. The relay driver provides a current path to ground which energizes the coarse align relays located in the PSA.

The signals received from the digital mode module are the ISS CDU zero drive and LORS CDU zero drive signals. These signals are at positive dc voltage level. The buffer circuits simply invert the signals and send them to other CDU modules.

4-4.9.2 14 VDC Power Supply. The 14 vdc power supply contained in the mode module is identical to the 14 vdc power supplies described in the interrogator module.

4-4.9.3 Phase Buffer Circuits. The phase buffer circuits receive four phase pulse trains, designated $\theta 2$ drive, $\theta 2$ drive, $\theta 3$ drive, and $\theta 4$ drive, from the digital mode module. The buffer circuit for each pulse train is a transistor inverter powered by the 4 vdc power supply. All four inverted signals are sent to the error counter and logic module. The inverted $\theta 3$ and $\theta 2$ signals are also sent to the read counter module.

4-4.9.4 ISS-CDU Fail Detect Circuit. The ISS-CDU fail detect circuit monitors the tolerance of critical signals. The fail detect circuits can be considered as three independent failure detect and logic circuits, each monitoring a single type of CDU error. If an out of tolerance condition is detected by the circuits, a failure signal is applied to a common output OR circuit.

The first ISS-CDU error detect and logic circuit receives the inner, middle, and outer coarse error signals from the coarse system module, and the inner, middle, and outer fine errors from the main summing amplifier. These six signals are applied to a level detector consisting of six voltage divider networks and a common filter section. The input signals are attenuated, half-wave rectified, and filtered. The voltage level at the output of the filter section controls the conduction of an output transistor. If any of the coarse or fine errors exceed tolerance, the voltage level at the output of the filter section reaches a level sufficient to bias the output transistor into conduction. The output transistor in turn supplies a failure indication input to the common output OR circuit.

The second ISS-CDU failure detect circuit monitors the inner, middle, and outer read counter UP level signals to detect an excessive read counter limit cycle frequency. When the read counter alternately counts up, then down, the input transistor of the failure detect circuit alternately turns on and off. The output of the transistor is differentiated so that a number of positive and negative pulses, corresponding to the frequency at which the counter changes direction, are developed. The positive pulses are detected and applied to a common filter section. By integrating the positive pulses, the filter section develops an output level proportional to the frequency at which the counter changes direction. When the frequency exceeds tolerance, the output level of the filter section is sufficient to bias an output driver transistor into conduction. The driver transistor, in turn, supplies a failure indication to the common output OR circuit.

The third ISS-CDU failure detect circuit monitors the three $\cos(\theta-\psi)$ $/90^\circ$ error signals from the inner, middle, and outer main summing amplifiers and also monitors

the output of the 14 vdc power supply located in the mode module. Each of the three $\cos(\theta-\psi)$ 90° signals is applied to an input transistor which conducts when the applied signal decreases below tolerance. When any of the three input transistors conduct, they turn off a fourth transistor which had been preventing the conduction of the output transistor. The proper state of each of the transistors in the circuit is established by bias levels derived from the 14 vdc supply. If the 14 vdc input decreases below tolerance, bias levels are changed sufficiently to result in the conduction of the output transistor. When the output transistor conducts, it supplies a failure indication to the common output OR circuit.

The output OR circuit accepts inputs from the three failure detect circuits previously mentioned. The output transistors of those three circuits must conduct through the same resistor network so that any of the three will develop a voltage drop across the resistor network. The voltage drop causes the conduction of the input transistor in the OR circuit. When this transistor conducts, it supplies an input to a time delay circuit consisting of a resistance-capacitive network and a zener diode. After approximately 7 seconds, the zener diode conducts, supplying proper bias to the output stage of the circuit which consists of two transistors. When the output transistors conduct, the circuit provides a positive 28 vdc CDU failure indication to the LGC.

4-4.9.5 LORS-CDU Fail Detect Circuit. The LORS-CDU fail detect circuit functions in exactly the same manner as the ISS-CDU fail detect circuit. The only difference between the two circuits is that the LORS-CDU fail detect circuit monitors the 14 vdc power supply located in the interrogate module and only two each from the $\cos(\theta-\psi)$, coarse error, fine error, and limit cycle types of signals.

4-4.9.6 Moding Relays. Two sets of two relays are located in the mode module. One set is used only in the CSM to route signals for Saturn steering control after SIVB Takeover. The second set of relays are used during thrust vector control mode in the CSM application and during the display inertial data mode in the LEM. The relays are energized by the LGC display inertial data discrete acting through a relay driver. The energized relays route the dc error signals, representing LEM forward and lateral velocity, from the LORS-CDU D/A converter to the LEM velocity display meters.

4-4.10 4 VDC POWER SUPPLY. The 4 vdc power supply (figure 4-18) supplies 4 vdc logic power to the digital logic circuits of the CDU. The 4 vdc power supply is a dc to dc converter type consisting of a pulse amplifier-inverter, a multivibrator-chopper, a power amplifier, a rectifier and filter circuit, and a difference amplifier and series regulator circuit.

A 25.6 kpps synchronization pulse input is amplified and inverted and used to synchronize the multivibrator-chopper, whose natural frequency is 11.5 kcps, at 12.8 kcps. The multivibrator-chopper drives the primary of a transformer which has 28 vdc applied to its center tap. The secondary of the transformer is also center tapped and is coupled to a push-pull power amplifier. The dc input to the power amplifier is supplied through a series regulator. The power amplifier drives the primary of a transformer to develop a 12.8 kcps square wave. The output from the transformer secondary is applied to the rectifier and filter circuit where the 4 vdc output is developed.

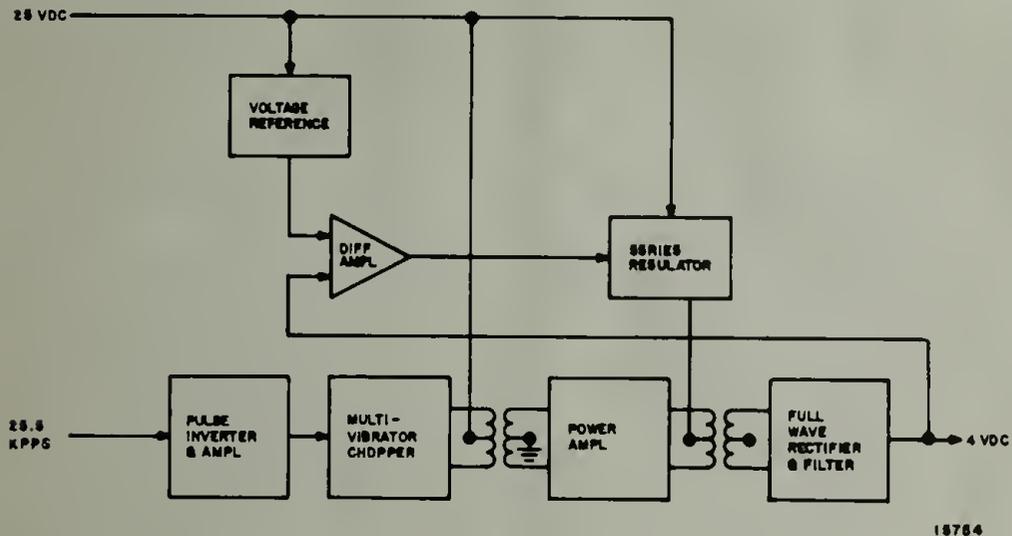


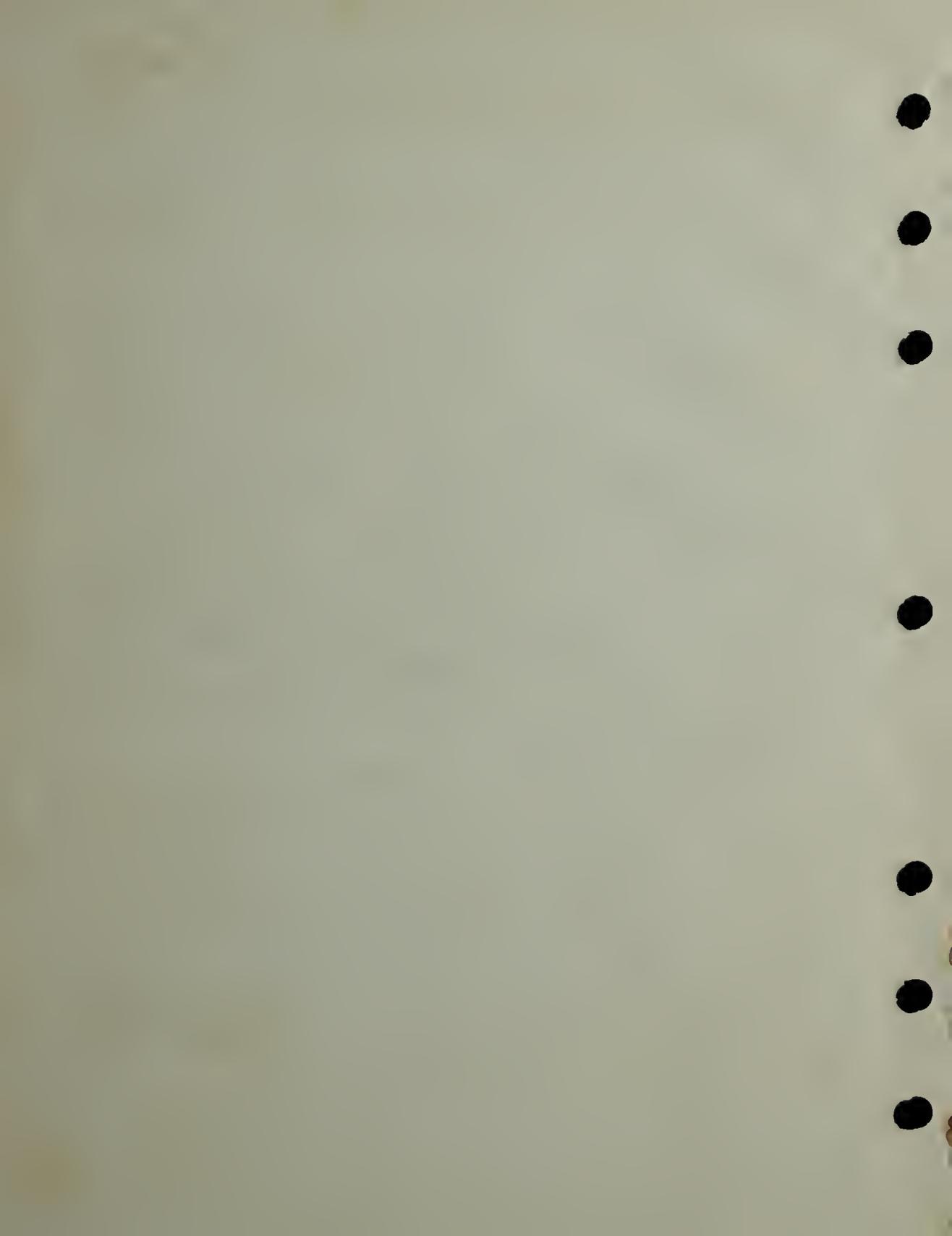
Figure 4-18. 4 VDC Power Supply, Block Diagram

The 4 vdc output is fed back to a difference amplifier that produces an output error signal proportional to the difference between the 4 vdc output and a reference voltage level obtained from a zener diode and resistor voltage divider network. The output of the difference amplifier controls the operation of the series regulator to increase or decrease the level of the dc input to the power amplifier as necessary to maintain the power supply output at 4 volts.

4-5 LEM GUIDANCE COMPUTER

This paragraph contains a discussion of the theory of operation of the LGC. Two levels of theory discussion, functional and detailed, are presented for each element of the LGC. Machine instructions and programs are also described in sufficient detail for support of maintenance activities.

4-5.1 PROGRAMS. The current LGC program consists of 17 program sections listed in table 4-I. (This table also indicates where the program sections are located in fixed memory.) Since the program is not yet complete, the following descriptions are limited to the functions of the existing program sections. Before describing the program sections, the terms routine, job, and task must be defined. A routine is a sequence of machine instructions which requires a request from an outside source to set it into operation. A job is a routine executed according to an assigned priority based



on the relative importance of the job to the overall accomplishment of the mission. Each job is assigned to a job area which is a group of locations in erasable memory into which information relating to the job can be stored. A task is a routine executed at an assigned future time counting ahead from the present time. The following paragraphs contain a brief description of the program sections.

4-5.1.1 Executive. The executive supervises the execution of all requested jobs according to an assigned priority scheme. The job having the highest priority is allowed to operate until displaced by another job of higher priority. When the job having the highest priority is completed, the executive initiates the execution of that job having the next highest priority. If no job is awaiting execution, a dummy job is executed which keeps the LGC idling until the next job request.

In addition, the executive places jobs into a dormant state when they require the occurrence of certain external events before proceeding. The executive then must reactivate these jobs when the external events have been completed.

4-5.1.2 Waitlist. Program section waitlist schedules the execution of tasks which must be executed at a specific time. Waitlist derives its timing from the TIME 3 counter; whenever this counter overflows, program control is transferred to that task which must be executed next. Waitlist maintains a list of tasks to be performed and, if the list is not full, dummy tasks are used to fill it. A dummy task performs the same function for waitlist as the dummy job performs for the executive.

4-5.1.3 Interpreter. The interpreter translates into basic machine language and executes that part of the program written in interpretive language. This translation allows complex operations to be prepared in a compact form at the sacrifice of LGC operational speed. Routines written in interpretive language contain explicit double precision, vector, and matrix operations.

4-5.1.4 RTB Op Codes. The RTB Op (return to basic operation) codes increase the effectiveness of the interpreter. The RTB Op codes provide a convenient link between basic and interpretive language and make possible the execution of subroutines in basic language while operating in the interpretive mode.

4-5.1.5 Fresh Start and Restart. A fresh start initiates most program sections in response to a keyboard entry from the DSKY, when the LGC is turned on, or when a serious error condition exists. A restart initiates most program sections after a GO sequence and returns program control to the beginning of the operation which was interrupted by the error.

4-5.1.6 Interrupt Lead-In Routines. The interrupt lead-in routines save the contents of register A (accumulator) and transfer program control to the routines that must be executed when an interrupt transfer request is recognized. The interrupt transfer routines transfer program control to routines T6RUPT, T5RUPT, T3RUPT, T4RUPT, KEYRUPT, UPRUPT, DOWNRUPT, RADRUPT, and HNDRUPT.

4-5.1.7 T4RUPT. Program section T4RUPT is activated when the TIME 4 counter overflows, and serves as a connection between the program and devices external to the LGC.

4-5.1.8 KEYRUPT and UPRUPT Processor. Program section KEYRUPT and UPRUPT processor accepts data from the DSKY, LORS, and uplink (unmanned flights). A KEYRUPT is initiated each time a DSKY key is pressed or when a specific discrete is received from LORS. An UPRUPT is initiated whenever data is received via uplink. After the data has been accepted, KEYRUPT and UPRUPT processor requests the execution of program section pinball which processes the data.

4-5.1.9 Interbank Communication. Interbank communication allows the transfer of information and/or control between banks in the fixed-switchable portion of fixed memory. This transfer is accomplished by transferring program control to fixed-fixed memory where the bank address can conveniently be changed. Then, register S is set to address the desired location within the proper bank. Program control is then transferred to the correct location in fixed-switchable memory.

4-5.1.10 Pinball. Program section pinball processes information exchanged between the LGC and the astronaut. These exchanges are initiated primarily by keycode action; however, exchanges can also be initiated under internal program control. Various functions are performed in response to requests from the keyboard; information resulting from these keyboard requests or internal requests from other program sections is displayed on the DSKY.

4-5.1.11 Alarm and Abort. Program section alarm and abort causes the display of certain failure messages on the DSKY. These failures are defined as either an alarm or an abort. Except for repeated alarms, an alarm is a failure which does not require a fresh start or restart. In the case of repeated alarms, the astronaut may initiate a manual fresh start via a keyboard entry. An abort is a failure which requires fresh start. Both failure conditions are displayed on the DSKY in a five character code of the form AAANN where AAA identifies the program section or routine in which the failure occurred and NN identifies the specific error which has occurred.

4-5.1.12 Controller and Meter Routines. The controller and meter routines service the hand controller inputs following a hand controller interrupt.

4-5.1.13 Orbital Integration. Orbital integration computes position and velocity of the spacecraft during coasting periods of the mission. Position and velocity are maintained in the LGC in non-rotating rectangular coordinates and referenced to the earth.

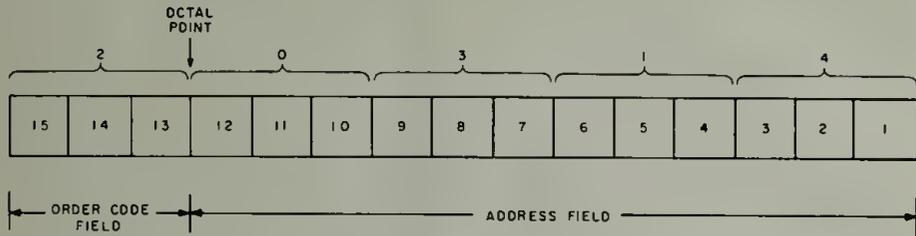
4-5.1.14 In-Flight Alignment. Program section in-flight alignment provides the framework for aligning the IMU. The program section consists of a set of routines written in interpretive language which are used for geometric transformation of the many coordinate axes needed in the in-flight alignment process.

4-5.1.15 Instruction Check. This program section exercises most of the control pulses in the LGC to check its performance. This is accomplished by initiating various program instructions. Most of the control pulses in an instruction are used every time that particular instruction is executed; however, the functions that some of these pulses perform are not utilized until some time later. Therefore, a systematic method is used to exercise those pulses not used immediately.

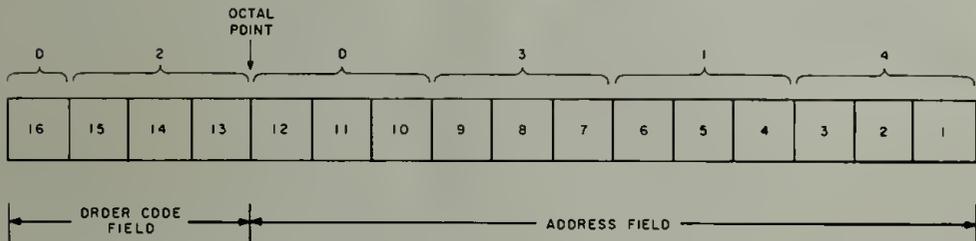
4-5.1.16 Flight Control System Test. This program section is used to execute five chains of tasks to test the LEM Flight Control System (FCS). These tests include turning various LEM engines on and off, issuing various engine control commands, and monitoring the LEM FCS input channels.

4-5.2 MACHINE INSTRUCTIONS. The LGC has three classes of machine instructions: regular, involuntary, and peripheral. Regular instructions can be written into a program and are executed in whatever sequence they have been stored in memory. Regular instructions are subdivided into basic, extracode, channel, and special instructions. Involuntary instructions are not programmable, with the exception of one instruction which may be programmed to test LGC operations. Involuntary instructions have priority over regular instructions and are executed at the occurrence of certain events during normal LGC operation. Involuntary instructions are subdivided into interrupt and counter instructions. The peripheral instructions are used when the LGC is connected to the computer test set (CTS) or other applicable peripheral equipment. During the execution of any peripheral instruction, the LGC is in the monitor stop mode and cannot execute any regular or involuntary instructions.

4-5.2.1 Regular Instructions. The difference between the four types of regular instructions is directly related to the way in which the LGC interprets an instruction word. Instruction words stored in memory are called basic instruction words. As shown in figure 4-19, these words contain a three bit order code field and a twelve bit address field. The content of the order code field defines the instruction and is represented by a single digit octal number with the octal point at the right. The content of the address field defines a location and is represented by a four digit octal number with the octal point at the left. An instruction word in memory therefore maybe written as a five digit octal number, e.g. 2.0314. The order code field is extended an additional bit when the basic instruction is transferred from memory to the central processor. Therefore, the instruction word used in the example changes to 02.0314 in the central processor. This additional high order bit is always logic ZERO for basic instructions. When the LGC is switched to the extend mode, the high order bit is logic ONE indicating an extra code or channel instruction will be executed next.

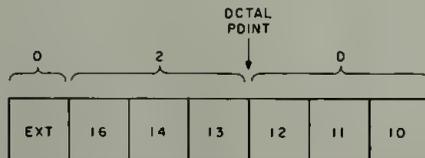


a. BASIC INSTRUCTION WORD IN MEMORY



NOTE: BITS 16 AND 15 ARE ALWAYS EQUAL

b. BASIC INSTRUCTION WORD IN CENTRAL PROCESSOR



c. EXTENDED ORDER CODE FIELD

40700

Figure 4-19. Basic Instruction Word Format

The LGC logic permits the use of the three high order bits (one octal digit) of the address field to further lengthen the order code field. A typical instruction can then be represented as 02.0 numerically. This encroachment on the address field limits the use of some instructions to a certain portion of memory. The high order bits of the address field may be used this way because of the differences between fixed and erasable memory. The instructions which apply only to erasable memory do not copy the two high order bits of the address field into the address register. However, the address register receives the entire address field for those instructions which apply to fixed memory.

The special instructions are address-dependent basic instructions and the order codes are represented as 00.0006 numerically. Those address-dependent instructions which may be combined with any order code are represented, for example, as .0021 which is the entire content of the address field.

4-5.2.2 Involuntary Instructions. Involuntary instructions consist of interrupt and counter instructions. The interrupt instructions are not programmable although they have order codes. The order codes are established by LGC logic and the interrupt instructions are executed on a priority basis. Counter instructions are also interrupt instructions in the sense that they delay the program for a short time. Counter instructions do not have operation codes and are executed involuntarily when the LGC is accepting incremental inputs or is providing incremental pulse rate outputs.

4-5.2.3 Peripheral Instructions. Peripheral instructions consist of keyboard and tape instructions. These instructions are initiated by an operator using the peripheral equipment. One peripheral instruction has an order code which is established by LGC logic. The others do not have order codes and are executed involuntarily like counter instructions.

4-5.2.4 Functional Description. Machine instructions can be divided by function into eight categories. Each category of instructions performs similar operations. For example, the add, subtract, multiply, and divide instructions perform arithmetic operations. The eight functional categories of machine instructions are:

- (1) Sequence changing
- (2) Fetching and storing
- (3) Modifying
- (4) Arithmetic and logic
- (5) Input-output
- (6) Editing
- (7) Priority
- (8) Peripheral

Table 4-II lists the eight functional categories of machine instructions. Also listed in table 4-II are subfunctional grouping, names, and mnemonic instruction words for each instruction. The instruction word addresses are represented by the following letters:

- (1) K for any address
- (2) CP for central processor addresses
- (3) E for erasable memory addresses
- (4) F for fixed memory addresses
- (5) C for counter address
- (6) H for channel addresses

Table 4-II. Functional Organization of Machine Instructions

Type	Instruction	
SEQUENCE CHANGING		
Transfer control	TC K TCF F	Transfer control Transfer control to fixed memory
Decision making	CCS E BZF F BZMF F	Count, compare, and skip Branch on zero to fixed memory Branch on zero or minus to fixed memory
FETCHING AND STORING		
Copying	CA K CS K DCA K DCS K	Clear and add Clear and subtract Double precision clear and add Double precision clear and subtract
Storing	TS E	Transfer to storage
Exchange	XCH E QXCH E LXCH E DXCH E	Exchange A Exchange Q Exchange L Double exchange
MODIFYING		
Indexing	NDX E NDX K	Index basic Index extracode
ARITHMETIC AND LOGIC		
Arithmetic	AD K SU E MP K DV E	Add Subtract Multiply Divide
Adding and storing	ADS E DAS E	Add and store Double precision add and store

Table 4-II. Functional Organization of Machine Instructions

Type	Instruction	
ARITHMETIC AND LOGIC (cont)		
Incrementing	INCR E AUG E DIM E	Increment Augment Diminish
Angular subtraction	MSU E	Modular subtract
Logic	MSK K	Mask or AND
INPUT-OUTPUT		
Read	READ H RAND H ROR H RXOR H	Read channel Read and AND Read and OR Read and EXCLUSIVE OR
Write	WRITE H WAND H WOR H	Write channel Write and AND Write and OR
EDITING		
Control	RELINT INHINT EXTEND RESUME	Release interrupt inhibit Inhibit interrupt Extend order code field Resume interrupted program
Shift and cycle	CYR SR CYL EDOP	Cycle right Shift right Cycle left Edit operator

(Sheet 2 of 3)

Table 4-II. Functional Organization of Machine Instructions

Type	Instruction	
PRIORITY		
Interrupt	RUPT F GOJ F	Interrupt Start
Counter	PINC C MINC C DINC C PCDU C MCDU C SHINC C SHANC C	Plus increment Minus increment or decrement Diminish increment Increment CDU Decrement CDU Shift increment Shift add increment
PERIPHERAL		
Transfer control	TCSAJ K	Transfer control to specified address
Read	FETCH K INOTRD H	Read memory Read channel
Load	STORE E INOTLD H	Load memory Load channel

(Sheet 3 of 3)

4-5.2.4.1 Sequence Changing Instructions. Two categories of sequence changing instructions are:

- (1) Transfer control instructions - TC K, TCF F
- (2) Decision instructions - CCS E, BZF F, BZMF F

The program control instructions determine the path that the program follows. Instruction TC K takes the next instruction from the location designated by the programmer instead of the next higher location. Instruction TCF F can only take instructions from designated fixed memory locations.

The decision instructions branch to alternate program paths in response to precisely defined conditions. Instruction CCS E tests for positive non-zero, plus zero, negative non-zero, and minus zero quantities and branches to one of four corresponding program paths. Instruction BZF F transfers control on a plus zero quantity to an alternate program path in fixed memory. The program follows its normal path if the quantity being tested is not plus zero. Similarly, instruction BZM F branches to an alternate path in fixed memory if the quantity under test is plus zero or negative.

4-5.2.4.2 Fetching and Storing Instructions. Three categories of the fetch and store instructions are:

- (1) Copying instructions - CA K, CS K, DCA K, DCS K
- (2) Storing instruction - TS E
- (3) Exchange instruction - XCH E, LXCH E, DXCH E, QXCH E

The copy instructions are used for duplicating data in another register. The content of any location may be copied into the single or double precision accumulators with instructions CA K and DCA K, respectively. The content of any location may be complemented and then copied into the accumulators with instructions CS K and DCS K. The content of the single precision accumulator may be copied into any erasable memory location with instruction TS E.

The content of registers A, L, or Q may be exchanged with that of any erasable memory location using instructions XCH E, LXCH E, or QXCH E, respectively. The content of the double precision accumulator may be exchanged with that in designated erasable memory locations using instruction DXCH E.

4-5.2.4.3 Modifying Instructions. The modifying instructions are NDX E (basic) and NDX K (extracode). Both instructions derive the next instruction to be executed.

4-5.2.4.4 Arithmetic and Logic Instructions. Five categories of the arithmetic and logic instructions are:

- (1) Basic arithmetic instructions - AD K, SU E, MP K, DV E
- (2) Add and store instructions - ADS E, DAS E
- (3) Angular subtract instructions - MSU E
- (4) Incrementing instructions - INCR E, AUG E, DIM E
- (5) Boolean AND instructions - MSK K

The basic arithmetic operations, addition, subtraction, multiplication, and division in the ONE's complement binary number system are performed with instructions AD K, SU E, MP K, and DV E, respectively. These instructions employ the conventional rules of algebra treating operators, operands, and resultants as signed (positive or negative) quantities. The operands and resultants are contained in the double precision accumulator (registers A and L) and the operators are obtained from any erasable memory location designated by the programmer.

Addition may also be performed with instruction ADS E which stores the resultant in register A and erasable memory. Instruction DAS E is used for double precision addition and storage. The difference between any TWO's complement numbers representing angular or periodic data may be obtained with instruction MSU E. The difference is a ONE's complement number stored in the designated erasable memory location.

The content of any erasable memory location designated by the programmer may be incremented by one with instruction INCR E. Instruction AUG E will increment the absolute value by one, whereas instruction DIM E will decrement the absolute value by one. If the designated address is 0026₈, 0027₈, or 0030₈ and overflow occurs, program control is automatically transferred to a reserved fixed memory location. If the address is 0025₈ and overflow occurs, the T2 time counter is automatically incremented by a counter instruction.

The MSK K instruction follows the basic rules of Boolean algebra and performs the AND operation. The operands and resultants are stored in the accumulator and the operator are obtained from any location designated by the programmer.

4-5.2.4.5 Input-Output Instructions. The two categories of input-output or channel instructions are:

- (1) Read instructions - READ H, RAND H, ROR H, RXOR H
- (2) Write instructions - WRITE H, WAND H, WOR H

Instructions READ H and WRITE H copy the content at the channel location into register A and the content of A into the channel location, respectively.

The logic instructions follow the basic rules of Boolean algebra, performing AND, OR, and EXCLUSIVE OR operations. The operands and resultants are stored in the accumulator and the operators are obtained from the location designated by the programmer.

Instructions RAND H and WAND H also perform the AND operation but the operator must be selected from a channel location. Instruction WAND H stores the resultant in both register A and the designated channel location. Instructions ROR H and WOR H perform the OR operation and RXOR H performs the EXCLUSIVE OR operation with the operator of any channel location. Instruction WOR H stores the resultant in both register A and the designated location. It is important to remember that registers L and Q are channel locations as well as addressable CP locations.

4-5.2.4.6 Editing Instructions. The editing instructions are address dependent instructions and are contained in two categories:

- (1) Control instructions - RESUME, EXTEND, INHINT, RELINT
- (2) Shift and cycle instructions - CYR, SR, CYL, EDOP

Instruction RESUME returns to the program that was being executed when an interrupt occurred. Instruction EXTEND sets the high order bit of the operation code. Instructions INHINT and RELINT respectively inhibit and permit interrupts.

4.5.2.4.7 Priority Instructions. The two categories of priority instructions are:

- (1) Interrupting instructions - RUPT F, GOJ F
- (2) Counter instructions - PINC C, MINC C, PCDU C, MCDU C, DINC C, SHINC C, SHANC C

Instructions RUPT F and GOJ F transfer control to fixed memory. The counter instructions are not programmable and apply to those erasable memory locations listed in table 4-III. Instructions PINC C and MINC C increment and decrement, respectively, the contents of the addressed counter. Instructions PCDU C and MCDU C increment and decrement, respectively, the CDU counters. The CDU counters always contain TWO's complement numbers. Instruction DINC C controls the output rate pulses. Instructions SHINC C and SHANC C perform serial-to-parallel conversion.

4.5.2.4.8 Peripheral Instructions. Three groups of peripheral instructions are:

- (1) Read - FETCH K, INOTRD H
- (2) Load - STORE E, INOTLD H
- (3) Transfer control - TCSAJ K

The peripheral instructions apply only when the LGC is connected to the CTS or the program analyzer console (PAC). Instructions FETCH K and INOTRD H are used for monitoring the content of memory and channel locations, respectively. Instructions STORE E and INOTLD H are used for loading erasable memory and channel locations respectively with data supplied by the peripheral equipment. Instruction TCSAJ K is used for initiating the instruction at any location.

Table 4-III. Counter Instructions

Location	Counter	Instruction
0024	T2	PINC
0025	T4	PINC
0026	T3	PINC
0027	T4	PINC
0030	T5	PINC
0031	T6	DINC
0032	CDUX	PCDU, MCDU
0033	CDUY	PCDU, MCDU
0034	CDUZ	PCDU, MCDU
0035	TRN	PCDU, MCDU
0036	SHAFT	PCDU, MCDU
0037	PIPX	PINC, MINC
0040	PIPY	PINC, MINC
0041	PIPZ	PINC, MINC
0042	BMAGX	PINC, MINC
0043	BMAGY	PINC, MINC
0044	BMAGZ	PINC, MINC
0045	INLINK	SHANC, SHINC
0046	RNRAD	SHANC, SHINC
0047	GYRO	DINC
0050	CDUX	DINC
0051	CDUY	DINC
0052	CDUZ	DINC
0053	TRUN	DINC
0054	SHAFT	DINC
0055	THRST	DINC
0056	EMS	DINC
0057	OTLNK	SHINC
0060	ALT	SHINC

4-5.2.4.9 Alphabetical Listing. Table 4-IV is an alphabetical listing of machine instructions. This table includes the order code, description, and execution time of each instruction. The symbol c(A), c(L), and so forth mean the content of A or the content of L. The letters K, E, H, F, and C refer to memory locations. The execution time is given in memory cycle times (MCT). One MCT equals approximately twelve microseconds.

Table 4-IV. Machine Instructions, Alphabetical Listing

Symbolic Instruction Word	Order Code c(SQ)	Description	Execution Time in MCT's
AD K	06.	Basic instruction; adds c(K) to c(A); stores result in A; takes next instruction from I+1 where I is location of AD K.	2
ADS E	02.6	Basic instruction; adds c(A) to c(E) and stores result in both A and E; takes next instruction from I+1 where I is location of ADS E.	2
AUG E	12.4	Extracode instruction; adds +1 to $ c(E) $, i.e., adds +1 if c(E) is positive and -1 if c(E) is negative; stores result in E; takes next instruction from I+1 where I is location of AUG E.	2
BZF F	11.2 11.4 11.6	Extracode instruction; takes next instruction from F if c(A) is +0; otherwise takes next instruction from I+1 where I is location of BZF F.	1 if c(A) is +0; otherwise 2
BZMF F	16.2 16.4 16.6	Extracode instruction; takes next instruction from F if c(A) is +0 or uegative; otherwise takes next instruction from I+1 where I is location of BZMF F.	1 if c(A) is +0 or negative; otherwise 2
CA K	03.	Basic instruction; copies c(K) into A; takes next instruction from I+1 where I is location of CA K.	2
CCS E	01.0	Basic instruction; if c(E) is non-zero and positive, takes next instruction from I+1 where I is location of CCS E. Also, adds -1 to c(E) and stores result in A. If c(E) is +0, takes uext instruction from I+2 and sets c(A) to +0. If c(E) is non-zero and negative, takes next instruction from I+3, adds -1 to c(E), and stores result in A. If c(E) is -0, takes next instruction from I+4 and sets c(A) to +0.	2

(Sheet 1 of 8)

Table 4-IV. Machine Instructions, Alphabetical Listing

Symbolic Instruction Word	Order Code c(SQ)	Description	Execution Time in MCT's
CS K	04.	Basic instruction; copies $\overline{c(K)}$ into A; takes next instruction from I+1 where I is location of CS K.	2
CY L	.0022	Special instruction; cycles quantity, which is entered into location 0022, one place to left.	2 or 3
CYR	.0020	Special instruction; cycles quantity, which is entered into location 0020, one place to right.	2 or 3
DAS E	02.0	Basic instruction; adds $c(A, L)$ to $c(E, E+1)$; stores result in E and E+1; sets $c(L)$ to +0 and sets $c(A)$ to net overflow if address E is not 0000 ₈ . Net overflow is +1 for positive overflow, -1 for negative overflow, otherwise $c(A)$ is set to +0. Takes next instruction from I+1 where I is location of DAS E.	3
DCA K	13.	Extracode instruction; copies $c(K, K+1)$ into A and L; takes next instruction from I+1 where I is location of DCA K.	3
DCS K	14.	Extracode instruction; copies $c(K, K+1)$ into A and L; takes next instruction from I+1 where I is location of DCS K.	3
DIM E	12.6	Extracode instruction; adds -1 to $ c(E) $, i. e., adds -1 if $c(E)$ is non-zero and positive and +1 if $c(E)$ is non-zero and negative; stores result in E; takes next instruction from I+1 where I is location of DIM E.	2

(Sheet 2 of 8)

Table 4-IV. Machine Instructions, Alphabetical Listing

Symbolic Instruction Word	Order Code c(SQ)	Description	Execution Time in MCT's
DINC C	None	Counter instruction; adds +1 to c(C) if c(C) is negative and provides negative rate output pulses; adds -1 to c(C) if c(C) is positive and provides positive rate output pulses; provides no rate output pulses when c(C) is ± 0 ; stores result in C; delays program execution for 1 MCT.	1
DV E	11.0	Extracode instruction; divides c(A, L) by c(E); stores quotient in A; stores remainder in L; takes next instruction from I+1 where I is location of DV E.	6
DXCH E	05.2	Basic instruction; exchanges c(E, E+1) with c(A, L); takes next instruction from I+1 where I is location of DXCH E.	3
EDOP	.0023	Special instruction; shifts quantity, which is entered into location 0023, seven places to left.	2 or 3
	00.	Interrupting instruction; transfers control to instruction stored in location 4000 _g .	2
EXTEND	00.0006	Special instruction; see TC K.	1
FETCH K	None	Peripheral instruction; reads and displays c(K) as binary numbers on CTS, where K is address supplied by CTS.	2
INCR E	02.4	Basic instruction; adds +1 to c(E); stores result in E; takes instruction from I+1 where I is location of INCR E.	2
INHINT	00.0003	Special instruction; see TC K.	1

(Sheet 3 of 8)

Table 4-IV. Machine Instructions, Alphabetical Listing

Symbolic Instruction Word	Order Code c(SQ)	Description	Execution Time in MCT's
INOTLD H	None	Peripheral instruction; loads data supplied by CTS into location H, where H is channel address also supplied by CTS.	1
INOTRD H	None	Peripheral instruction; reads and displays c(H) as binary number on CTS, where H is channel address supplied by CTS.	1
LXCH E	02.2	Basic instruction; exchanges c(E) with c(L); takes next instruction from I+1 where I is location of LXCH E.	2
MCDU C	None	Counter instruction; adds -1 (two's complement) to c(C); delays program execution for 1 MCT.	1
MINC C	None	Counter instruction; adds -1 to c(C); delays program execution for 1 MCT.	1
MP K	17.	Extracode instruction; multiplies c(A) by c(E); stores result in A and L; c(A, L) agree in sign; takes next instruction from I+1 where I is location of MP E.	3
MSK K	07.	Basic instruction; AND's c(A) with c(K); stores result in A; takes next instruction from I+1 where I is location of MSK K.	2
MSU E	12.0	Extracode instruction; forms the signed one's complement difference between c(A) and c(E) where c(A) and c(E) are unsigned (modular or periodic) two's complement numbers; stores result in A; takes next instruction from I+1 where I is location of MSU E.	2

(Sheet 4 of 8)

Table 4-IV. Machine Instructions, Alphabetical Listing

Symbolic Instruction Word	Order Code c(SQ)	Description	Execution Time in MCT's
NDX E	05.0	Basic instruction; adds c(K) to c(I+1) where I is location of NDX E; takes sum of c(K) + c(I+1) as next instruction.	2
NDX K	15.	Extracode instruction; adds c(K) to c(I+1) where I is location of NDX K; sets extra code switch; sum of c(K) + c(I+1) becomes an extracode instruction which is taken as next instruction.	2
PCDU C	None	Counter instruction; adds +1 (two's complement) to c(C); delays program execution for 1 MCT.	1
PINC C	None	Counter instruction; adds +1 to c(C); delays program execution for 1 MCT.	1
QXCH E	12.2	Extracode instruction; exchanges c(E) with c(L); takes next instruction from I+1 where I is location of QXCH E.	2
RAND H	10.2	Channel instruction; AND's c(H) with c(A); stores result in A; takes next instruction from I+1 where I is location of RAND H.	2
READ H	10.0	Channel instruction; copies c(H) into A; takes next instruction from I+1 where I is location of READ H.	2
ROR H	10.4	Channel instruction; OR's c(H) with c(A); stores result in A; takes next instruction from I+1 where I is location of ROR H.	2
RELINT	00.0003	Special instruction; see TC K.	1
RESUME	05.0017	Special instruction; takes next instruction from return address.	1

(Sheet 5 of 8)

Table 4-IV. Machine Instructions, Alphabetical Listing

Symbolic Instruction Word	Order Code c(SQ)	Description	Execution Time in MCT's
RUPT F	10.7	Interrupting instruction; takes next instruction from location F; stores c(B) (instruction that was to be executed) in location 0017 ₈ ; stores c(Z) = I in location 0015 ₈ , where I is assigned location of instruction stored in 0017 ₈ .	3
RXOR H	10.6	Channel instruction; forms the exclusive OR of c(H) and c(A); stores result in A; takes next instruction from I+1 where I is location of RXOR H.	2
SHANC C	None	Counter instruction; doubles c(C) and adds +1; stores result in C; delays program execution for 1 MCT.	1
SHINC C	None	Counter instruction; doubles c(C); stores result in C; delays program execution for 1 MCT.	1
SR	.0021	Special instruction; shifts quantity, which is entered into location 0021, one place to right.	2 or 3
STORE E	None	Peripheral instruction; data supplied by CTS is stored in location E where E is address supplied by CTS; delays program execution for 2 MCT's.	2
SU E	16.0	Extracode instruction; subtracts c(A) from c(E); stores result in A; takes next instruction from I+1 where I is location of SU E.	2

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Table 4-IV. Machine Instructions, Alphabetical Listing

Symbolic Instruction Word	Order Code c(SQ)	Description	Execution Time in MCT's
TC K	00.	Basic instruction; takes next instruction from K; stores I+1 in Q where I is location of TC K; if K is 0006 (EXTEND), sets extracode switch and takes next instruction from I+1; if K is 0004 (INHINT) sets inhibit interrupt switch and takes next instruction from I+1; if K is 0003 (RELINT), resets inhibit interrupt switch and takes next instruction from I+1.	1
TCF F	01.2 01.4 01.6	Basic instruction; takes next instruction from F.	1
TCSAJ K		Peripheral instruction; takes next instruction from K where K is address supplied by CTS.	2
TS E	05.4	Basic instruction; if c(A) is not an overflow quantity, copies c(A) into K and takes next instruction from I+1 where I is location of TS K; if c(A) is a positive overflow quantity, copies c(A) into K, sets c(A) to +1, and takes next instruction from I+2; if c(A) is a negative overflow quantity, copies c(A) into K, sets c(A) to -1, and takes next instruction from I+1.	2
WAND H	10.3	Channel instruction; AND's c(H) with c(A); stores result in H and A; takes next instruction from I+1 where I is location of WAND H.	2
WOR H	10.5	Channel instruction; OR's c(H) with c(A); stores result in H and A; takes next instruction from I+1 where I is location of WOR H.	2

(Sheet 7 of 8)

Table 4-IV. Machine Instructions, Alphabetical Listing

Symbolic Instruction Word	Order Code c(SQ)	Description	Execution Time in MCT's
WRITE H	10.1	Channel instruction; copies c(A) into H; takes next instruction from I+1 where I is location of WRITE H.	2
XCH E	05.6	Basic instruction; exchanges c(A) with c(E); takes next instruction from I+1 where I is location of XCH E.	2

(Sheet 8 of 8)

4-5.2.5 Subinstruction Commands and Control Pulses. The basic elements which comprise machine instructions are control pulses and subinstruction commands. Control pulses are sequence generator signals which regulate data flow within the LGC. Machine instructions use a large variety of control pulses to accomplish various functions. The data must be regulated in an orderly sequence and certain information must not be destroyed during the execution of an instruction. In addition, the machine instruction must be executed within the memory cycle timing framework which consists of twelve one-microsecond periods. Some instructions are so involved that two or more memory cycle times are required to accomplish a task. Each memory cycle time is controlled by a subinstruction command, regardless of the number of MCT's required to do a job. Instruction TC K for example takes one MCT to be executed and is controlled by subinstruction command TC0. Table 4-V lists all of the machine instructions by order code. The associated subinstructions are also listed. Some instructions use common subinstructions like STD2. Table 4-V also lists the content of the stage counter for each subinstruction. The number after each subinstruction like DAS1 reflects the count of the stage counter.

Information is transferred from one register to another by read, clear, and write control pulses. The clear pulses are generated automatically when a write pulse is generated to clear a register before data is written into it. The control pulses RZ and WS, for instance, occurring simultaneously, duplicate (copy) the content of register Z in register S. There are five types of control pulses: read, write, test, direct exchange, and special purpose control pulses, discussed in the following paragraphs.

4-5.2.5.1 Read Control Pulses. A read control pulse places on the write lines data which is to be transferred (copied) into a register. Most read control pulses such as RA, RB, and RZ read the content of a specific register onto the write lines. Control

Table 4-V. Subinstructions

Order Code c(SQ)	Mnemonic Operation Code	Mnemonic Subinstruction Code	Register SQ Display	Stage Counter Display
REGULAR INSTRUCTIONS				
00.	TC	TC0	000-007	0
00.0003	RELINT	-	000	2
00.00	INHINT	-	000	2
00.0006	EXTEND	-	000	2
01.0	CCS	CCS0	010-011 010-011	0 2
01.2 01.4 01.6	TCF	TCF0	012-017	0
02.0	DAS	DAS0 DAS1 STD2	020-021 020-021 020-021	0 1 2
02.2	LXCH	LXCH0 STD2	022-023 022-023	0 2
02.4	INCR	INCR0 STD2	024-025 024-025	0 2
02.6	ADS	ADS0 STD2	026-027 026-027	0 2
03.	CA	CA0 STD2	030-037 030-037	0 2
04.	CS	CS0 STD2	040-047 040-047	0 2
05.0	NDX	NDX0 NDX1	050-051 050-051	0 1

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Table 4-V. Subinstructions

Order Code c(SQ)	Mnemonic Operation Code	Mnemonic Subinstruction Code	Register SQ Display	Stage Counter Display
REGULAR INSTRUCTIONS				
05.0017	RESUME	NDX0	050-051	0
		RSM3	050-051	3
05.2	DXCH	DXCH0	052-053	0
		DXCH1	052-053	1
		STD2	052-053	2
05.4	TS	TS0	054-055	0
		STD2	054-055	2
05.6	XCH	XCH0	056-057	0
		STD2	056-057	2
06.	AD	AD0	060-067	0
		STD2	060-067	2
07.	MSK	MASK0	070-077	0
		STD2	070-077	2
10.0	READ	READ0	100	0
		STD2	100	2
10.1	WRITE	WRITE0	101	0
		STD2	101	2
10.2	RAND	RAND0	102	0
		STD2	102	2
10.3	WAND	WAND0	103	0
		STD2	103	2
10.4	ROR	ROR0	104	0
		STD2	104	2
10.5	WOR	WOR0	105	0
		STD2	105	2

(Sheet 2 of 5)

Table 4-V. Subinstructions

Order Code c(SQ)	Mnemonic Operation Code	Mnemonic Subinstruction Code	Register SQ Display	Stage Counter Display
REGULAR INSTRUCTIONS				
10.6	RXOR	RXOR0 STD2	106 106	0 2
10.7	RUPT	RUPT0 RUPT1 STD2	107 107 107	0 1 2
11.0	DV	DV0 DV1 DV3 DV7 DV6 DV4 STD2	110-111 110-111 110-111 110-111 110-111 110-111 110-111	0 1 3 7 6 4 2
11.2 11.4	BZF (Plus Zero)	BZF0	112-117	0
11.6	BZF (Non-Zero)	BZF0 STD2	112-117 112-117	0 2
12.0	MSU	MSU0 STD2	120-121 120-121	0 2
12.2	QXCH	QXCH0 STD2	122-123 122-123	0 2
12.4	AUG	AUG0 STD2	124-125 124-125	0 2
12.6	DIM	DIM0 STD2	126-127 126-127	0 2
13.	DCA	DCA0 DCA1 STD2	130-137 130-137 130-137	0 1 2

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Table 4-V. Subinstructions

Order Code c(SQ)	Mnemonic Operation Code	Mnemonic Subinstruction Code	Register SQ Display	Stage Counter Display
REGULAR INSTRUCTIONS				
14.	DCS	DCS0 DCS1 STD2	140-147 140-147 140-147	0 1 2
15.	NDX	NDXX0 NDXX1	150-157 150-157	0 1
16.0	SU	SU0 STD2	160-161 160-161	0 2
16.2 16.4	BZMF (Zero or Negative)	BZMF0	162-167	0
	BZMF (Non-Zero and Positive)	BZMF0 STD2	162-167	0 2
17.	MP	MP0 MP1 MP3	170-177 170-177 170-177	0 1 3
INVOLUNTARY INSTRUCTIONS				
00.	GOJ	GOJ1 TC0	000 000	1 0
10.7	RUPT	RUPT0 RUPT1 STD2	107 107 107	0 1 2
None	PINC	PINC	None	None
None	MINC	MINC	None	None
None	DINC	DINC	None	None
None	MCDU	MCDU	None	None
None	SHINC	SHINC	None	None
None	SHANC	SHANC	None	None

(Sheet 4 of 5)

Table 4-V. Subinstructions

Order Code c(SQ)	Mnemonic Operation Code	Mnemonic Subinstruction Code	Register SQ Display	Stage Counter Display
PERIPHERAL INSTRUCTIONS				
00	TCSAJ	TCSAJ3 STD2	000 000	3 2
None	FETCH	FETCH0 FETCH1	None None	0 1
None	STORE	STORE0 STORE1	None None	0 1
None	INOTRD	INOTRD	None	None
None	INOTLD	INOTLD	None	None

(Sheet 5 of 5)

pulse RSC reads onto the write lines the content of register CP whose address is contained in register S. Other read control pulses place data on the write lines directly through the sequence generator. For instance, control pulse R15 causes the sequence generator to place the octal quantity 000015 on the write lines.

4-5.2.5.2 Write Control Pulses. Each write control pulse clears a register, then writes data from the write lines into this register. Most write control pulses write into a specific register such as control pulse WQ which always writes data into register Q, but never into any other register. Control pulse WSC clears register CP specified by the content of register S, then writes data into this register from the write lines.

4-5.2.5.3 Test Control Pulses. Test control pulses permit branching operations by testing the contents of various registers. For instance, control pulse TMZ tests the contents of a register for minus zero (octal 177777). If the register contains 177777, flip-flop BR2 is set to logic ONE; otherwise, BR2 is set to logic ZERO.

4-5.2.5.4 Direct Exchange Control Pulses. Direct exchange control pulses transfer data from one area to another directly without using the write lines. Control pulse A2X, for example, copies the content of register A directly into register X. Some direct exchange control pulses enter data from the sequence generator directly into particular storage areas. Control pulse CP, for example, enters a logic ONE from the sequence generator into the carry flip-flop of the adder.

4-5.2.5.5 Special Purpose Control Pulses. Special purpose control pulses perform various control functions such as generating read/write operations and resetting counters. For instance, control pulse NISQ causes two other control pulses (RB and WSQ) to be generated at time 12; control pulse RSTSTG resets the stage counter. All control pulses are listed in table 4-VI.

Table 4-VI. Control Pulses

Pulse	Purpose														
A2X	Enter bits 16 through 1 of register A directly (not via WL's) into bit positions 16 through 1 of register X.														
B15X	Enter a logic ONE into bit position 15 of register X.														
CI	Insert carry bit into bit position 1 of the adder.														
CLXC	Clear register X if flip-flop BR1 contains a logic ZERO. (Used in divide instruction.)														
DVST	Advance the Gray code content of the stage counter by complementing the content of the next higher bit position as shown below: <table style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Binary</th> <th>Octal</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>0</td> </tr> <tr> <td>001</td> <td>1</td> </tr> <tr> <td>011</td> <td>3</td> </tr> <tr> <td>111</td> <td>7</td> </tr> <tr> <td>110</td> <td>6</td> </tr> <tr> <td>100</td> <td>4</td> </tr> </tbody> </table>	Binary	Octal	000	0	001	1	011	3	111	7	110	6	100	4
Binary	Octal														
000	0														
001	1														
011	3														
111	7														
110	6														
100	4														
EXT	Enter a logic ONE into bit position EXT of register SQ.														
G2LS	Enter bits 16 through 4 and 1 of register G into bit positions 16, 15, and 12 through 1 of register X. See control pulse ZAP.														
KRPT	Reset interrupt priority cells.														
L16	Enter a logic ONE into bit position 16 of register L.														
L2GD	Enter bits 16 and 14 through 1 of register L into bit positions 16 through 2 of register G; enter a logic ONE (pulse MCRO) into bit position 1 of register G.														
MONEX	Clear register X, then enter logic ONE's into bit positions 16 through 2.														
MOUT	Generate one negative rate output pulse.														
NEACOF	Permit end around carry upon completion of subinstruction MP3.														

(Sheet 1 of 6)

Table 4-VI. Control Pulses

Pulse	Purpose
NEACON	Inhibit end around carry (also during WYD) until NEACOF.
NISQ	Load next instruction into register SQ. Also frees certain restrictions; permits execution of instruction RUPT and counter instructions. See control pulses RB and WSQ.
PIFL	Prevent interflow on control pulse WYD if bit position 15 of register L contains a logic ONE; block writing into bit position 1 of register Y. See control pulse WYD.
PONEX	Clear register X, then enter a logic ONE into bit position 1.
POUT	Generate one positive rate output pulse.
PTWOX	Clear register X, then enter a logic ONE into bit position 2.
R15	Place octal 15 on WL's.
R1C	Place octal 177776 (minus one) on WL's.
RA	Read bits 16 through 1 of register A to WL's 16 through 1.
RAD	Read address of next cycle. RAD appears at the end of an instruction and is normally interpreted as RG. If the next instruction is INHINT, RELINT, or EXTEND, RAD is interpreted as RZ and ST2 instead.
RB	Read bits 16 through 1 of register B to WL's 16 through 1.
RBBK	Read bits 16 and 14 through 11 of register FB to WL's 16 and 14 through 11 and bits 11, 10, and 9 of register EB to WL's 3, 2, and 1.
RB1	Place octal 1 on WL's.
RB1F	Place octal 1 on WL's if flip-flop BR1 contains a logic ONE.
RB2	Place octal 2 on WL's.
RC	Read the complemented contents of register B (bits 16 through 1 of C) to WL's 16 through 1.

(Sheet 2 of 6)

Table 4-VI. Control Pulses

Pulse	Purpose
RCH	Read the contents of the input or output channel specified by the contents of register S; bit 16 is read to WL's 16 and 15 and bits 14 through 1 are read to WL's 14 through 1.
REB	Read bits 11, 10, and 9 of register EB to WL's 11, 10, and 9. See control pulse RSC.
RFB	Read bits 16 and 14 through 11 of register FB to WL's 16 and 14 through 11. See control pulse RSC.
RG	Read bits 16 through 1 of register G to WL's 16 through 1.
RL	Read bit 16 of register L to WL's 16 and 15, and bits 14 through 1 to WL's 14 through 1.
RL10BB	Read low 10 bits of register B to WL's 10 through 1.
RQ	Read bits 16 through 1 of register Q to WL's 16 through 1.
RRPA	Place on WL's the address of the priority program requested.
RSC	Read the content of register CP defined by the content of register S; bits 16 through 1 are read to WL's 16 through 1.
RSCT	Place on WL's the address of the counter to be incremented.
RSTRT	Place octal 4000 (start address) on WL's.
RSTSTG	Reset the stage counter.
RU	Read bits 16 through 1 of adder output gates (U) to WL's 16 through 1.
RUS	Read bit 15 of adder output gates (U) to WL's 16 and 15, bits 14 through 1.
RZ	Read bits 16 through 1 of register Z to WL's 16 through 1.
ST1	Set stage 1 flip-flop to logic ONE at next time 12.
ST2	Set stage 2 flip-flop to logic ONE at next time 12.

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Table 4-VI. Control Pulses

Pulse	Purpose
STAGE	Execute next subinstruction as defined by the content of the divide stage counter.
TL15	Copy bit 15 of register L into flip-flop BR1.
TMZ	Test for minus zero: if bits 16 through 1 are all logic ONE's, set flip-flop BR2 to logic ONE; otherwise set BR2 to logic ZERO.
TOV	Test for overflow: set flip-flops BR1 and BR2 to 01 if positive overflow, to 10 if negative overflow.
TPZG	Test content of register G for plus zero: if bits 16 through 1 are all logic ZERO's, set flip-flop BR2 to logic ONE; otherwise do not change content of BR2.
TRSM	Test for the resume address (0017) during instruction NDX.
TSGN	Test sign (bit 16): if a logic ZERO, set flip-flop BR1 to logic ZERO; if a logic ONE, set flip-flop BR1 to logic ONE.
TSGN2	Test sign (bit 16): if a logic ZERO, set flip-flop BR2 to logic ZERO; if a logic ONE, set flip-flop BR2 to logic ONE.
TSGU	Test sign (bit 16) of sum contained in adder output gates (U): if a logic ZERO, set flip-flop BR1 to logic ZERO; if a logic ONE, set flip-flop BR1 to logic ONE.
U2BBK	Enter bits 16 and 14 through 11 of output gates U directly into register FB and bits 3, 2, and 1 of gates U into bits 11, 10, and 9 of register EB.
WA	Clear register A and write the contents of WL's 16 through 1 into bit positions 16 through 1.
WALS	Clear register A and write the contents of WL's 16 through 3 into bit positions 14 through 1; if bit position 1 of register G contains a logic ZERO, the content of bit position 16 of register G is entered into bit position 16 and 15 of register A; if bit position 1 of register G contains a logic ONE, the content of output gate U 16 of the adder is entered into bit positions 16 and 15 of register A; clear bits 14 and 13 of register L and write the contents of WL's 2 and 1 into bit positions 14 and 13. See control pulse ZAP.

(Sheet 4 of 6)

Table 4-VI. Control Pulses

Pulse	Purpose
WB	Clear register B and write the contents of WL's 16 through 1 into bit positions 16 through 1.
WBBK	Clear registers EB and FB and write the content of WL's 16 and 14 through 11 into register FB and content of WL's 3, 2, and 1 into register EB. See control pulse WSC.
WCH	Clear the channel specified by the contents of register S (bits 9 through 1) and write the contents of WL's 16 through 1 into this channel.
WEB	Clear register EB and write the contents of WL's 11, 10, and 9 into bit positions 11, 10, and 9. See control pulse WSC.
WFB	Clear register FB and write the content of WL's 16 and 14 through 11 into bit position 16 and 14 through 11. See control pulse WSC.
WG	Clear register G and write the contents of WL's 16 through 1 into bit positions 16 through 1 (except if register S contains octal addresses 20 through 23).
WL	Clear register L and write the contents of WL's 16 through 1 into bit positions 16 through 1.
WOVR	Test for positive overflow. If register S contains 0025, counter 0024 is incremented; if register S contains 0026, 0027, or 0030, instruction RUPT is executed.
WQ	Clear register Q and write the contents of WL's 16 through 1 into bit positions 16 through 1.
WS	Clear register S and write the contents of WL's 12 through 1 into bit positions 12 through 1.
WSC	Clear the CP register specified by the contents of register S and write the contents of WL's 16 through 1 into bit positions 16 through 1 of this register.
WSQ	Clear register SQ and write the contents of WL's 16 and 14 through 10 into bit positions 16 and 14 through 10, copy the content of the extend flip-flop into bit position EXT of register SQ. See control pulse NISQ.

(Sheet 5 of 6)

Table 4-VI. Control Pulses

Pulse	Purpose																																																															
WY	Clear registers X and Y; write the contents of WL's 16 through 1 into bit positions 16 through 1 of register Y.																																																															
WY12	Clear registers X and Y; write the contents of WL's 12 through 1 into bit positions 12 through 1 of register Y.																																																															
WYD	Clear registers X and Y; write the contents of WL's 16 and 14 through 1 into bit positions 16 and 15 through 2 of register Y; write the content of WL 16 into bit position 1 of register Y except in SHINC sequence, or unless bit 15 of register L is a logic ONE at PIFL, or if end around carry is inhibited (NEACON).																																																															
WZ	Clear register Z and write the contents of WL's 16 through 1 into bit positions 16 through 1.																																																															
Z15	Enter a logic ONE into bit position 15 of register Z.																																																															
Z16	Enter a logic ONE into bit position 16 of register Z.																																																															
ZAP	Generate control pulses RU, G2LS, and WALS.																																																															
ZIP	Generate control pulses A2X and L2GD; also perform read/write operations depending on the content of bit positions 15, 2, and 1 of register L as shown:																																																															
	<table border="1"> <thead> <tr> <th>L15</th> <th>L2</th> <th>L1</th> <th>Read</th> <th>Write</th> <th>Carry</th> <th>Remember</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>-</td> <td>WY</td> <td>-</td> <td>-</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>RB</td> <td>WY</td> <td>-</td> <td>-</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>RB</td> <td>WYD</td> <td>-</td> <td>-</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>RC</td> <td>WY</td> <td>CI</td> <td>MCRO</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>RB</td> <td>WY</td> <td>-</td> <td>-</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>RB</td> <td>WYD</td> <td>-</td> <td>-</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>RC</td> <td>WY</td> <td>CI</td> <td>MCRO</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>-</td> <td>WY</td> <td>-</td> <td>MCRO</td> </tr> </tbody> </table>	L15	L2	L1	Read	Write	Carry	Remember	0	0	0	-	WY	-	-	0	0	1	RB	WY	-	-	0	1	0	RB	WYD	-	-	0	1	1	RC	WY	CI	MCRO	1	0	0	RB	WY	-	-	1	0	1	RB	WYD	-	-	1	1	0	RC	WY	CI	MCRO	1	1	1	-	WY	-	MCRO
L15	L2	L1	Read	Write	Carry	Remember																																																										
0	0	0	-	WY	-	-																																																										
0	0	1	RB	WY	-	-																																																										
0	1	0	RB	WYD	-	-																																																										
0	1	1	RC	WY	CI	MCRO																																																										
1	0	0	RB	WY	-	-																																																										
1	0	1	RB	WYD	-	-																																																										
1	1	0	RC	WY	CI	MCRO																																																										
1	1	1	-	WY	-	MCRO																																																										
ZOUT	Generate no rate output pulse.																																																															

(Sheet 6 of 6)

4-5.2.5.6 Action. An action is a set of control pulses. By definition, a set may contain from zero to any number of control pulses. Each control pulse set is produced for a 0.977 microsecond period. Twelve control pulse sets or actions are produced during one memory cycle time (11.977 microseconds). Control pulse sets are coincident with time pulses T01 through T12. For example, action 6 of subinstruction STD2 occurs at time 6 and consists of the control pulse set RU and WZ which copies the contents of the adder output gates (U) into register Z. Table 4-VII lists the control pulses generated during the execution of each subinstruction. The subinstructions are arranged by order code number. The binary content of register SQ and the stage counter are listed in table 4-VII. The coincidence of a subinstruction command and a time pulse as STD2 and T06, is referred to as a crosspoint.

4-5.2.6 Data Transfer Diagrams. The LGC instructions are described by subinstruction data transfer diagrams which relate data flow to LGC hardware. Figures 4-20 through 4-116 contain data transfer diagrams for each subinstruction and a diagram for each branch operation except for those in the multiply and divide subinstructions. The quantities shown on these diagrams reflect typical operation conditions. The diagrams are arranged according to order code listed in table 4-V.

Symbols FM and EM at the top of the diagrams designate fixed and erasable memory, respectively, and CH refers to the channel locations. The octal quantities shown in FM and EM represent 15 bit words and those shown in CH represent 16 bit words. Register S is a 12 bit address register. Register G is a 6 bit memory buffer register. Register B is a 16 bit terminal register containing a direct (B) and complement (C) output side. Registers A and L are 16 bit accumulators, Q is a 16 bit return address register, and register Z is a 16 bit program counter. Registers X and Y, output gates U, and flip-flop CI comprise the adder. Registers X and Y, and the output gates U contain 16 bit positions; CI is the end around carry flip-flop. U always contains the sum of $c(X) + c(Y) + c(CI)$. Register SQ is a 7 bit sequence register. Not shown on these diagrams are the 3 bit stage counter and the 2 bit branch register. The content of these registers is specified by notes at the bottom of the data transfer diagrams.

Data shown in the registers prior to time 1 indicate typical starting conditions. Data in the ellipses indicate write line information. The information passing between FM or EM and G does not use the write lines and is therefore indicated by a direct path. Flow lines are not shown for the data which is gated from one register to another by a single control pulse such as A2X or L2GD. Broken flow lines indicate conditional data flow which is dependent on the content of register S.

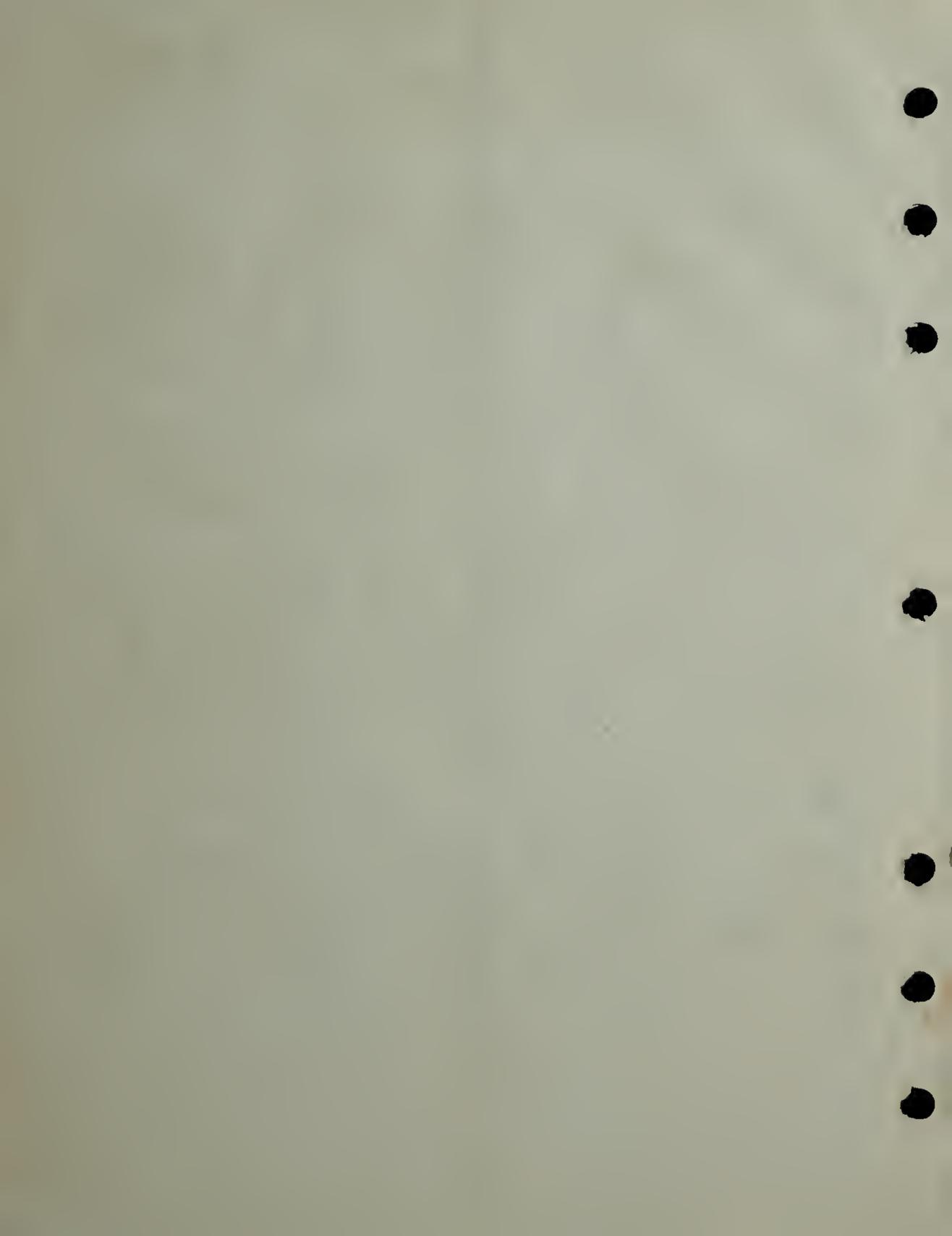


Table 4-VII. Subinstruction Codes and Control Pulses

Subinstruction Command	c(SQ)			c(ST) 3,2,1	Actions												Remarks
	EXT	16 14 13	12,11 10		1	2	3	4	5	6	7	8	9	10	11	12	
STD2	X	X X X	X X X	0 1 0	RZ WY12 CI	RSC WG NISQ				RU WZ			RAD WB WS				Follows any subinstruction which sets c(ST) = 010 with control pulse ST2. Followed by next instruction. See note A.
TC0	0	0 0 0	X X X	0 0 0	RB WY12 CI	RSC WG NISQ	RZ WQ			RU WZ			RAD WB WS				Followed by instruction to which control is transferred. See note A.
CCS0	0	0 0 1	0 0 X	0 0 0	RL10BB WS	RSC WG			RG WB TSC TMZ TPZ	RZ WY12 ① - ② PONEX ③ PTVOX ④ PONEX PTWOX	RU WZ WS	RB WG	WY ST2 ① RB MONEX CI ② - ③ TC MONEX CI ④ -	RU WA			① If c(BR) = 00 at action 5, c(G) is positive non-zero. ② If c(BR) = 01 at action 5, c(G) is plus zero. ③ If c(BR) = 10 at action 5, c(G) is negative non-zero. ④ If c(BR) = 11 at action 5, c(G) is minus zero. Followed by STD2.
TCF0	0 0 0	0 0 1 0 0 1 0 0 1	0 1 X 1 0 X 1 1 X	0 0 0 0 0 0 0 0 0	RB WY12 CI	RSC WG NISQ				RU WZ			RAD WB WS				Followed by instruction to which control is transferred. See note A.

Table 4-VII. Subinstruction Codes and Control Pulses

Subinstruction Command	c(SQ)			c(ST)	Actions												Remarks
	EXT	16.14.13	12.11.10		3.2.1	1	2	3	4	5	6	7	8	9	10	11	
DAS0	0	0 1 0	0 0 X	0 0 0	RL10BB WS WY12 MONEX CI	RSC WG	RA WB	RL WA	RU WL	RG WY A2X	RB WA	RL WB	RU WSC WG TOV	RA WY ST1	RU WA		<p>① If c(BR) = 00 at action 9, U16.15 = 00 or 11.</p> <p>② If c(BR) = 01 at action 9, U16.15 = 01.</p> <p>③ If c(BR) = 10 at action 9, U16.15 = 10.</p> <p>Followed by DAS1.</p> <p>① —</p> <p>② PONEX</p> <p>③ MONEX</p>
OAS1	0	0 1 0	0 0 X	0 0 1	RL10BB WS	RSC WG			RG WY A	RU WG WSC TOV	WA ① — ② RBI ③ RIC	RZ WS ST2	RC TMZ	④ WL ⑤ —	④ — ⑤ RU WA		<p>① If c(BR) = 00 at action 7, U16.15 = 00 or 11.</p> <p>② If c(BR) = 01 at action 7, U16.15 = 01.</p> <p>③ If c(BR) = 10 at action 7, U16.15 = 10.</p> <p>④ If c(BR) = X0 at action 9, $\overline{c(B)}$ = 17777.</p> <p>⑤ If c(BR) = X1 at action 9, $\overline{c(B)}$ = 17777.</p> <p>Followed by STO2</p>
LXCH0	0	0 1 0	0 1 X	0 0 0	RL10BB WS	RSC WG	RL WB		RG WL		RB WSC WG	RZ WS ST2					Followed by STO2.
INCR0	0	0 1 0	1 0 X	0 0 0	RL10BB WS	RSC WG			RG WY TSGN TMZ TPZG	PONEX	RU WSC WG WOVR	RZ WS ST2					TSGN, TMZ, and TPZG at action 5 have no effect. At action 7, WOVR requests RUPT if c(S) is 0026, 0027, or 0030 and U16.15 = 01 Followed by STO2

Table 4-VII. Subinstruction Codes and Control Pulses

Subinstruction Command	c(SQ)			c(ST)	Actions												Remarks	
	EXT	16,14,13	12,11,10		3,2,1	1	2	3	4	5	6	7	8	9	10	11		12
ADSO	0	0 1 0	1 1 X	0 0 0	RL10BB WS	RSC WG				RG WY A2X	RU WSC WG TDV	WA ① — ② RB1 ③ R1C	RZ WS ST2	RC TMZ		RU WA		① If c(BR) = 00 at action 7, U16,15 = 00 or 11. ② If c(BR) = 01 at action 7, U16,15 = 01 ③ If c(BR) = 10 at action 7, U16,15 = 10. RC and TMZ at action 9 have no effect. Followed by STD2.
CA0	0	0 1 1	X X X	0 0 0		RSC WG					RG WB	RZ WS ST2	RB WG	RB WA				Followed by STD2.
CS0	0	1 0 0	X X X	0 0 0		RSC WG					RG WB	RZ WS ST2	RB WG	RC WA				Followed by STD2.
NDX0	0	1 0 1	0 0 X	0 0 0		RSC WG			TR		RG WB	RZ WS	RB WG	ST1				Normally followed by NDX1 Followed by RSM3 if c(S) = 0017 (RESUME) at action 5
NDX1	0	1 0 1	0 0 X	0 0 1	RZ WY12 CI	RSC WG NISQ	RB WZ	RA WB	RZ WA	RU WZ	RG WY A2X	RU WS	RB WA	RU WB				Followed by indexed basic instruction
RSM3	0	1 0 1	0 0 X	0 1 1	R15 WS	RSC WG NISQ				RG WZ	RB WG		RAD WB WS					Followed by instruction at return address. See note A
DXCH0	0	1 0 1	0 1 X	0 0 0	RL10BB WS WY12 MONEX CI	RSC WG	RL WB			RG WL		RB WSC WG	RU WS WB		ST1			Control pulse CI at action 1 causes 000001 plus 177776 to result in 000000 instead of 177777 Followed by DXCH1

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Table 4-VII. Subinstruction Codes and Control Pulses

Subinstruction Command	c(SQ)			c(ST)	Actions												Remarks
	EXT	16 14,13	12,11,10	3,2,1	1	2	3	4	5	6	7	8	9	10	11	12	
DXCH1	0	1 0 1	0 1 X	0 0 1	RL10BB WS	RSC WG	RA WB		RG WA		RB WSC WG	RZ WS ST2					Followed by STD2
TSO	0	1 0 1	1 0 X	0 0 0	RL10BB WS	RSC WG	RA WB TDV	RZ WY12 ① - ② CI ③ CI	① - ② RBI WA ③ RC W	RU WZ	RB WSC WG	RZ WS ST2					① If c(BR) = 00 at action 3, A16,15 = 00 or 11 ② If c(BR) = 01 at action 3, A16,15 = 01 ③ If c(BR) = 10 at action 3, A16,15 = 10. Followed by STD2.
XCHO	0	1 0 1	1 1 X	0 0 0	RL10BB WS	RSC WG	RA WB		RG WA		RB WSC WG	RZ WS ST2					Followed by STD2.
ADO	0	1 1 0	X X X	0 0 0		RSC WG					RG WB	RZ WS ST2	RB WG	RB WY AZX	RU WA		Followed by STD2.
MSK0	0	1 1 1	X X X	0 0 0		RSC WG	RA WB	RC WA			RG WB	RZ WS ST2	RC RA WY	RU WB	RC WA		Followed by STD2.
DV0	1	0 0 1	0 0 X	0 0 0	RA WB TSGN TMZ	① RC WA TMZ DVST ② DVST	RU WB STAGE										① If c(BR) = 0X at action 2, A16 = 0. ② If c(BR) = 1X at action 2, A16 = 1. RU at action 3 has no effect Followed by DV1 after action 3

Table 4-VII. Subinstruction Codes and Control Pulses

Subinstruction Command	c(SQ)			c(ST)	Actions												Remarks
	EXT	16,14,13	12,11,10	3,2,1	1	2	3	4	5	6	7	8	9	10	11	12	
DV1	1	0 0 1	0 0 X	0 0 1				RL WB ① — ② TSGN	WY B15X ③ RB ④ RC Z16	RU WL TDV	RG RSC WB TSGN	RA WY ⑤ PDNEX ⑥ —	⑦ RB WA ⑧ RC WA Z15	RU WB	RL WYD	RU WL	① If c(BR) = X 0 at action 4, c(A) at action 2 of DV0 is non-zero ② If c(BR) = X 1 at action 4, c(A) at action 2 of DV0 is minus zero. ③ If c(BR) = 0 X at action 5, A16 = 0 at action 2 of DV0 or L16 = 0 at action 4 of DV1 ④ If c(BR) = 1 X at action 5, A16 = 1 at action 2 of DV0 or L16 = 0 at action 4 of DV1 ⑤ If c(BR) = X 0 at action 8, U16,15 = 00, 10, or 11. ⑥ If c(BR) = X 1 at action 8, U16,15 = 01. ⑦ If c(BR) = 0 X at action 9, G16 = 0 ⑧ If c(BR) = 1 X at action 9, G16 = 1 ⑨ If c(BR) = 0 X at action 2, U16 = 0. ⑩ If c(BR) = 1 X at action 2, U16 = 1. Followed by DV3 after action 3.
DV1 (cont)	1	0 0 1	0 0 X	0 0 1	L2GD RB WYD A2X PIFL	RG WL TSGU DVST ⑨ CLXC ⑩ RBIF	RU WB STAGE										① If c(BR) = 0 X at action 5, 8, or 11, U16 = 0. ② If c(BR) = 1 X at action 5, 8, or 11, U16 = 1
DV3	1	0 0 1	0 0 X	0 1 1				L2GD RB WYD A2X PIFL ① CLXC ② RBIF	RU WL TSGU CLXC RBIF	RU WB	L2GD RB WYD A2X PIFL	RG WL TSGU CLXC RBIF	RU WB	L2GD RB WYD A2X PIFL	RG WL TSGU CLXC RBIF	RU WB	① If c(BR) = 0 X at action 5, 8, or 11, U16 = 0. ② If c(BR) = 1 X at action 5, 8, or 11, U16 = 1

Table 4-VII. Subinstruction Codes and Control Pulses

Subinstruction Command	c(SQ)			c(ST)	Actions												Remarks	
	EXT	16 14,13	12,11 10	3,2,1	1	2	3	4	5	6	7	8	9	10	11	12		
DV3 (cont)	1	0 0 1	0 0 X	0 1 1	L2GD RB WYD A2X PIFL	RG WL TSGU DVST ③ CLXG ④ RBIF	RU WB STAGE											③ If c(DR) = 0X at action 2, U16 = 0 ④ If c(BR) = 1X at action 2, U16 = 1 Followed by DV7 after action 3.
DV7	1	0 0 1	0 0 X	1 1 1				L2GD RB WYD A2X PIFL	RG WL TSGU ① GLXC ② RBIF	RU WB	L2GD RB WYD A2X PIFL	RG WL TSGU ① CLXC ② RBIF	RU WB	L2GD RB WYD A2X PIFL	RG WL TSGU ① GLXC ② RBIF	RU WB		① If c(BR) = 0X at action 5, 8, 11, or 2, U16 = 0 ② If c(BR) = 1X at action 5, 8, 11, or 2, U16 = 1 Followed by DV6 after action 3
DV7 (cont)	1	0 0 1	0 0 X	1 1 1	L2GD RB WYD A2X PIFL	RG WL TSGU DVST ① CLXG ② RBIF	RU WB STAGE											

Table 4-VII. Subinstruction Codes and Control Pulses

Subinstruction Command	c(SQ)			c(ST)	Actions												Remarks
	EXT	16 14,13	12,11,10	3,2,1	1	2	3	4	5	6	7	8	9	10	11	12	
DV6	1	0 0 1	0 0 X	1 1 0				L2GD RB WYD A2X PIFL	RG WL TSGU CLXC RBIF	RU WB	L2GD RB WYD A2X PIFL	RG WL TSGU CLXC RBIF	RU WB	L2GD RB WYD A2X PIFL	RG WL TSGU CLXC RBIF	RU WB	① If c(BR) = 0X at action 5, 8, 11, or 2, U16 = 0. ② If c(BR) = 1X at action 5, 8, 11 or 2, U16 = 1 Followed by DV4 after action 3.
DV6 (cont)	1	0 0 1	0 0 X	1 1 0	L2GD RB WYD A2X PIFL	RG WL TSGU DVST CLXC RBIF	RU WB STAGE										
DV4	1	0 0 1	0 0 X	1 0 0			L2GD RB WYD A2X PIFL	RG WB WA TSGU CLXC RBIF	RZ TOV	③ — ④ RC WA ⑤ RC WA	RZ WS ST2 TSGN RSTSTG	RU WB WL	⑥ RC WL ⑦ —				① If c(BR) = 0X at action 5, U16 = 0 ② If c(BR) = 1X at action 5, U16 = 1 ③ If c(BR) = 00 at action 7, U16,15 = 00 or 11 ④ If c(BR) = 01 at action 7, U16,15 = 01. ⑤ If c(BR) = 10 at action 7, U16,15 = 10. ⑥ If c(BR) = 0X at action 10, Z16 = 0 ⑦ If c(BR) = 1X at action 10, Z16 = 1

Table 4-VII. Subinstruction Codes and Control Pulses

Subinstruction Command	c(SQ)			c(ST)	Actions												Remarks	
	EXT	16,14,13	12,11,10		3,2,1	1	2	3	4	5	6	7	8	9	10	11		12
BZF0	1 1 1	0 0 1 0 0 1 0 0 1	0 1 X 1 0 X 1 1 X	0 0 0 0 0 0 0 0 0		RSC WG	RA WG TSGN TMZ	TPZG	① — ② RB WY12 CI	① — ② RU WZ		① RZ WS ST2 ② RAD WB WS NISQ						① If c(BR) = X0 at action 4, c(G) ≠ 000000. ② If c(BR) = X1 at action 4, c(G) = 000000. RSC at action 2, and TSGN and TMZ at action 3 have no effect. RAD causes only RG If c(BR) = X0, BZF0 is followed by STD2. If c(BR) = X1, BZF0 is followed by instruction to which control is transferred.
MSU0	1	0 1 0	0 0 X	0 0 0	RL10BB WS	RSC WG			RG WB	RC WY CI A2X	RUS WA TSGN	RZ WS ST2	RB WG	① — ② RA WY MONEX	RUS WA			① If c(BR) = 0X at action 7, U15 = 0. ② If c(BR) = 1X at action 7, U15 = 1. Followed by STD2.
QXCH0	1	0 1 0	0 1 X	0 0 0	RL10BB WS	RSC WG	RQ WB		RG WQ		RB WSC WG	RZ WS ST2						Followed by STD2.
AUG0	1	0 1 0	1 0 X	0 0 0	RL10BB WS	RSC WG			RG WY TSGN TMZ TPZG	① PDNEX ② MDNEX	RU WSC WG WOVR	RZ WS ST2						① If c(BR) = 0X at action 6, G16 = 0. ② If c(BR) = 1X at action 6, G16 = 1. TMZ and TPZG at action 5 have no effect. At action 7, WDVR requests RUPT if c(S) is 0026 0027, or 0030 and U16,15 = 01 Followed by STD2
DIM0	1	0 1 0	1 1 X	0 0 0	RL10BB WS	RSC WG			RG WY TSGN TMZ TPZG	① MDNEX ② PONEX ③ —	RU WSC WG WOVR	RZ WS ST2						① If c(BR) = 00 at action 6, c(G) is positive non-zero. ② If c(BR) = 10 at action 6, c(G) is negative non-zero ③ If c(BR) = 01 or 11 at action 6, c(G) is plus or minus zero. WDVR at action 7 has no effect. Followed by STD2.
DCA0	1	0 1 1	X X X	0 0 0	RB WY12 MONEX CI	RSC WG					RG WB	RU WS	RB WG	RB WL ST1				Followed by DCA1.

Table 4-VII. Subinstruction Codes and Control Pulses

Subinstruction Command	c(SQ)			c(ST)	Actions												Remarks
	EXT	16,14,13	12,11,10	3,2,1	1	2	3	4	5	6	7	8	9	10	11	12	
DCA1	1	0 1 1	X X X	0 0 1		RSC WG					RG WB	RZ WS ST2	RB WG	RB WA			Followed by STD2
DCS0	1	1 0 0	X X X	0 0 0	RB WY12 MDNEX CI	RSC WG					RG WB	RU WS	RB WG	RC WL ST1			Followed by DCS1.
DGS1	1	1 0 0	X X X	0 0 1		RSG WG					RG WB	RZ WS ST2	RB WG	RG WA			Followed by STD2.
NDXX0	1	1 0 1	X X X	0 0 0		RSG WG					RG WB	RZ WS	RB WG	ST1			Followed by NDXX1.
NDXX1	1	1 0 1	X X X	0 0 1	RZ WY12 CI	RSC WG NISQ	RB WZ	RA WB	RZ WA	RU WZ	RG WY A2X	RU WS	RB WA	RU WB EXT			Followed by an indexed extra code instruction
SU0	1	1 1 0	0 0 X	0 0 0		RSC WG					RG WB	RZ WS ST2	RB WG	RG WY A2X	RU WA		Followed by STD2.
BZMF0	1 1 1	1 1 0 1 1 0 1 1 0	0 1 X 1 0 X 1 1 X	0 0 0		RSG WG	RA WG TSGN TMZ	TPZG	① - ② RB WY12 GI ③ RB WY12 GI	① - ② RU WZ ③ RU WZ		① RZ WS ST2 ② RAD WB WS NISQ ③ RAD WB WS NISQ					① If c(BR) = 00 at action 4, c(G) is positive non-zero. ② If c(BR) = 01 at action 4, c(G) = 000000 ③ If c(BR) = 10 at action 4, c(G) is negative RSC at action 2 and TMZ at action 3 have no effect. RAD causes only RG. If c(BR) = 00, BZMF0 is followed by STD2. If c(BR) = 01 or 11, BZMF0 is followed by instruction to which control is transferred.

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Table 4-VII. Subinstruction Codes and Control Pulses

Subinstruction Command	c(SQ)			c(ST)	Actions												Remarks
	EXT	16,14 13	12,11 10	3,2,1	1	2	3	4	5	6	7	8	9	10	11	12	
MP0	1	1 1 1	X X X	0 0 0		RSC WG	RA WB TSGN	① RB WL ② RC WL			RG WB TSGN2	RZ WS	③ RB WY ④ RB WY CI L16 ⑤ RC WY CI L16 ⑥ RC WY	RU WB TSGN ST1 NEACON	⑦ WA — ⑧ RBI RIC		① If c(BR) = 0X at action 3, A16 = 0. ② If c(BR) = 1X at action 3, A16 = 1. ③ If c(BR) = 00 at action 7, A16 = 0 and G16 = 0. ④ If c(BR) = 01 at action 7, A16 = 0 and G16 = 1. ⑤ If c(BR) = 10 at action 7, A16 = 1 and G16 = 0. ⑥ If c(BR) = 11 at action 7, A16 = 1 and G16 = 1. ⑦ If c(BR) = 0X at action 10, U16 = 0. ⑧ If c(BR) = 1X at action 10, U16 = 1. Followed by MP1.
MP1	1	1 1 1	X X X	0 0 1	ZIP	ZAP	ZIP	ZAP	ZIP	ZAP	ZIP	ZAP	ZIP	ZAP ST1 ST2	ZIP		Followed by MP3.
MP3	1	1 1 1	X X X	0 1 1	ZAP	ZIP NISQ	ZAP	RSC WG	RZ WY12 CI	RU WZ TL15 NEACOF	① — ② RB WY A2X	RA0 WB WS	RA	RL	① — ② RU WA		① If c(BR) = 0X at action 6, U15 = 0. ② If c(BR) = 1X at action 6, U15 = 1. Followed by next instruction. See note A.
READ0	1	0 0 0	0 0 0	0 0 0	RL10BB WS	RA WB	WY	RCH WB	RB WA	RA WB		RZ WS ST2					Followed by ST02.
WRITE0	1	0 0 0	0 0 1	0 0 0	RL10BB WS	RA WB WG	WY	RCH WB	RA WCH	RA WB		RZ WS ST2					See note B. Followed by STD2.
RAND0	1	0 0 0	0 1 0	0 0 0	RL10BB WS	RA WB	RC WY	RCH WB	RC RU WA	RA WB	RC WA	RZ WS ST2					Followed by ST02.

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Table 4-VII. Subinstruction Codes and Control Pulses

Subinstruction Command	c(SQ)			c(ST)	Actions												Remarks
	EXT	16,14 13	12,11,10	3,2,1	1	2	3	4	5	6	7	8	9	10	11	12	
WAND0	1	0 0 0	0 1 1	0 0 0	RL10BB WS	RA WB	RC WY	RCH WB	RC RU WA	RA WB	RC WA WCH	RZ WS ST2					See note B Followed by STD2.
RORO	1	0 0 0	1 0 0	0 0 0	RL10BB WS	RA WB	RB WY	RCH WB	RB RU WA	RA WB		RZ WS ST2					Followed by STD2.
WOR0	1	0 0 0	1 0 1	0 0 0	RL10BB WS	RA WB	RB WY	RCH WB	RB RU WA WCH	RA WB		RZ WS ST2					See note B. Followed by STD2.
RXOR0	1	0 0 0	1 1 0	0 0 0	RL10BB WS	RA WB	RC RCH WY	RCH WB	RA RC WG		RG WB	RZ WS ST2	RC WG	RU WB	RC RG WA		Followed by STD2.
RUPT0	1	0 0 0	1 1 1	0 0 0	R15 WS	RSC WG							RZ WG	ST1			RSC at action 2 has no effect. Followed by STD2.
RUPT1	1	0 0 0	1 1 1	0 0 1	R15 RB2 WS	RSC WG	RRPA WZ					RZ WS ST2	RB WG KRPT				RSC at action 2 has no effect. Followed by STD2.
GDJ1	0	0 0 0	X X X	0 0 1		RSC WG						RSTRT WS WB					Initiated by signal GOJAM. RSC at action 2 has no effect. Followed by TC 4000.
PINC	X	X X X	X X X	X X X	RSCT WS	RSC WG			RG WY TSGN TMZ TPZG	PONEX	RU WSC WG WOVR	RB WS					See note C. RSC at action 2, TSGN, TMZ, and TPZG at action 5, and WSC at action 7 have no effect. At action 7, WOVR requests RUPT if c(S) is 0026, 0027, or 0030 and U16,15 = 01. WOVR requests PINC 0024 if c(S) is 0025 and U16,15 = 01.

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Table 4-VII. Subinstruction Codes and Control Pulses

Subinstruction Command	c(SQ)			c(ST)	Actions												Remarks
	EXT	16,14,13	12,11,10	3,2,1	1	2	3	4	5	6	7	8	9	10	11	12	
MINC	x	x x x	x x x	x x x	RSCT WS	RSC WG			RG WY TSGN TMZ TPZG	MONEX	RU WSC WG WOVR	RB WS					See note C. RSC at action 2, TSGN, TMZ, and TPZG at action 5, and WSC and WOVR at action 7 have no effect.
PCOU	x	x x x	x x x	x x x	RSCT WS	RSC WG			RG WY TSGN TMZ TPZG	CI	RUS WSC WG WOVR	RB WS					See note C. RSC at action 2, TSGN, TMZ, and TPZG at action 5, and WSC and WOVR at action 7 have no effect.
MCOU	x	x x x	x x x	x x x	RSCT WS	RSC WG			RG WY TSGN TMZ TPZG	MONEX CI	RUS WSC WG WOVR	RB WS					See note C. RSC at action 2, TSGN, TMZ, and TPZG at action 5, and WSC and WOVR at action 7 have no effect.
DINC	x	x x x	x x x	x x x	RSCT WS	RSC WG			RG WY TSGN TMZ TPZG	① MONEX POUT ② PONEX MOUT ③ ZOUT	RU WSC WG WOVR	RB WS					See note C ① If c(BR) = 00, c(G) is positive non-zero. ② If c(BR) = 10, c(G) is negative non-zero. ③ If c(BR) = 01, or 11, c(G) is plus or minus zero. RSC at action 2, and WSC and WOVR at action 7 have no effect.
SHINC	x	x x x	x x x	x x x	RSCT WS	RSC WG			RG WYO TSGN		RUS WSC WG WOVR	RB WS					See note C. RSC at action 2, and WSC and WOVR at action 7 have no effect. At action 5, TSGN requests RUPT if c(S) is 0045 and G16 = 1.
SHANC	x	x x x	x x x	x x x	RSCT WS	RSC WG			RG WYO TSGN CI		RUS WSC WG WOVR	RB WS					See note C. RSC at action 2, and WSC and WOVR at action 7 have no effect. At action 5, TSGN requests RUPT if c(S) is 0045 and G16 = 1.

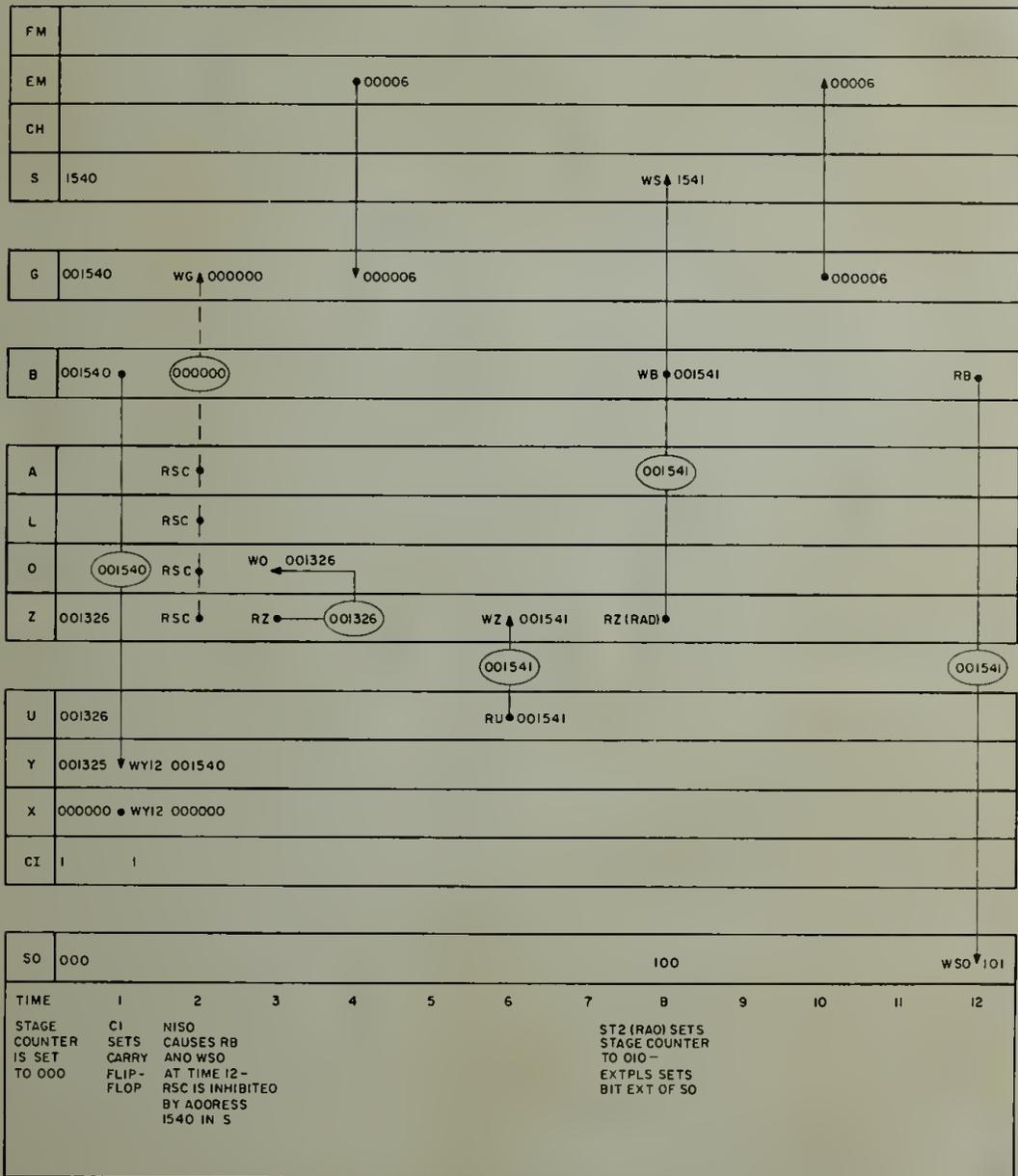
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Table 4-VII. Subinstruction Codes and Control Pulses

Subinstruction Command	c(SQ)			c(ST)	Actions												Remarks		
	EXT	16	14	13	12	11	10	3	2	1	5	6	7	8	9	10		11	12
TCSAJ3	X	X	X	X	X	X	X		RSC WG					WS WZ ST2					See note D Followed by STD2.
INOTRD	X	X	X	X	X	X		WS	RSC WG		RCH			RB WS					See note D.
INOTLO	X	X	X	X	X	X		WS	RSC WG		RCH		WCH	RB WS					See note D.
FETCH0	X	X	X	X		0	0	0	RG WS	RSC WG WY ST1		WSC		WS					See note D. Followed by FETCH1.
FETCH1	X	X	X	X		0	0	1		RSC WG			RG	RB WS U2BBK		RBBK			See note D.
STORE0	X	X	X	X		0	0	0	RG WS	RSC WG WY ST1		WSC		WS					See note D. Followed by STORE1.
STORE1	X	X	X	X		0	0	1		RSC WG		WSC	RG	RB WS U2BBK	WG	RBBK			See note D.

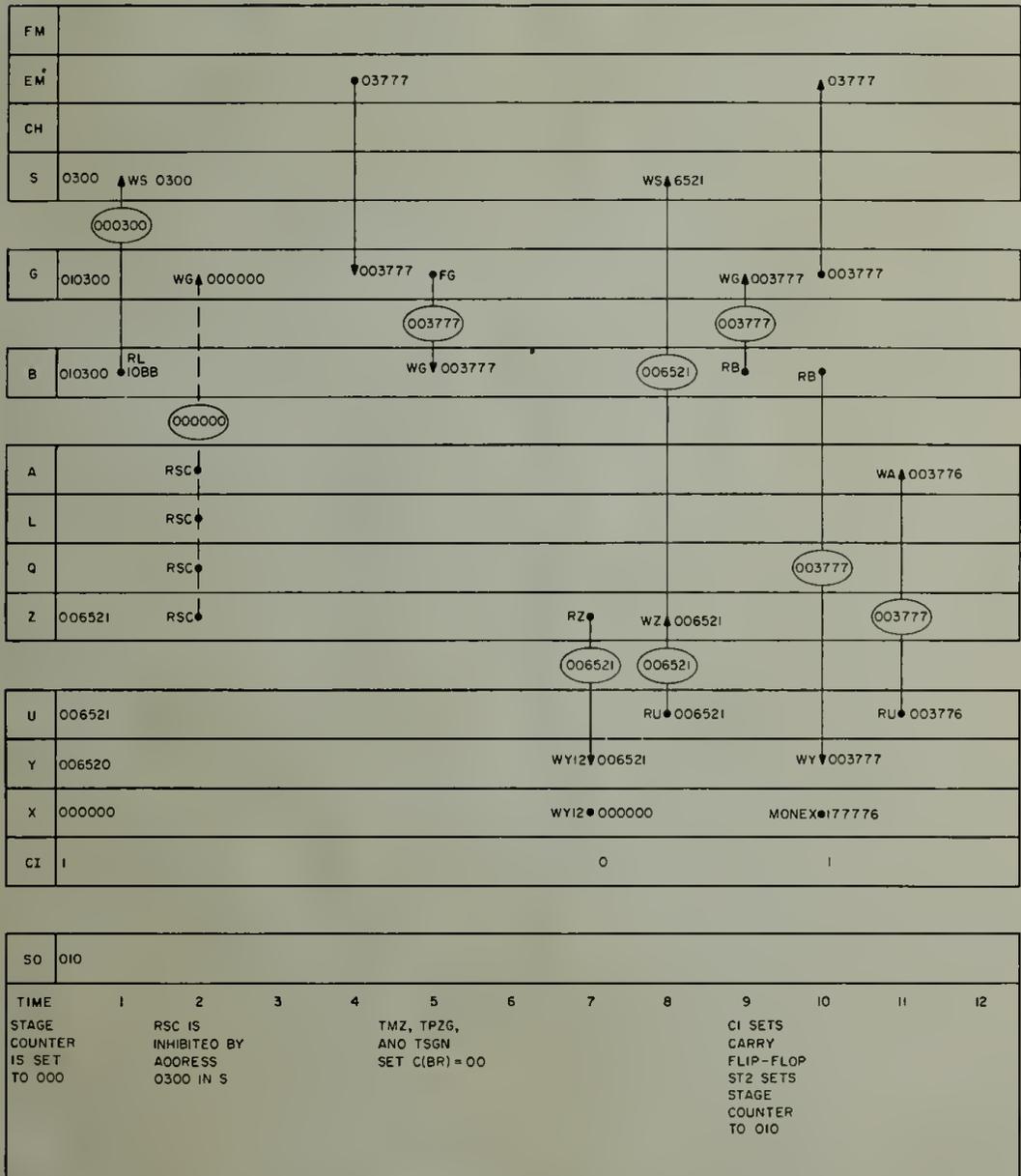
NOTES

- A If c(G) = 000003 (RELINT), 000004 (INHINT), or 000006 (EXTENT), control pulse RAD causes the generation of control pulses RZ and ST2, and subinstruction STQ2 is executed next. If G contains any other quantity, control pulse RAO causes the generation of control pulse RG and the next instruction is executed.
- B The ONE entered into bit position 10 of register S has no effect on addressing channel locations.
- C Counter instructions are executed after any time 12 provided an involuntary or peripheral instruction is not being requested. Each counter instruction delays program execution for one MCT.
- D Peripheral instructions are initiated by a signal from the CTS or the PAC. Normally the LGC time counter is stopped at time 12 before and after the execution of an instruction.



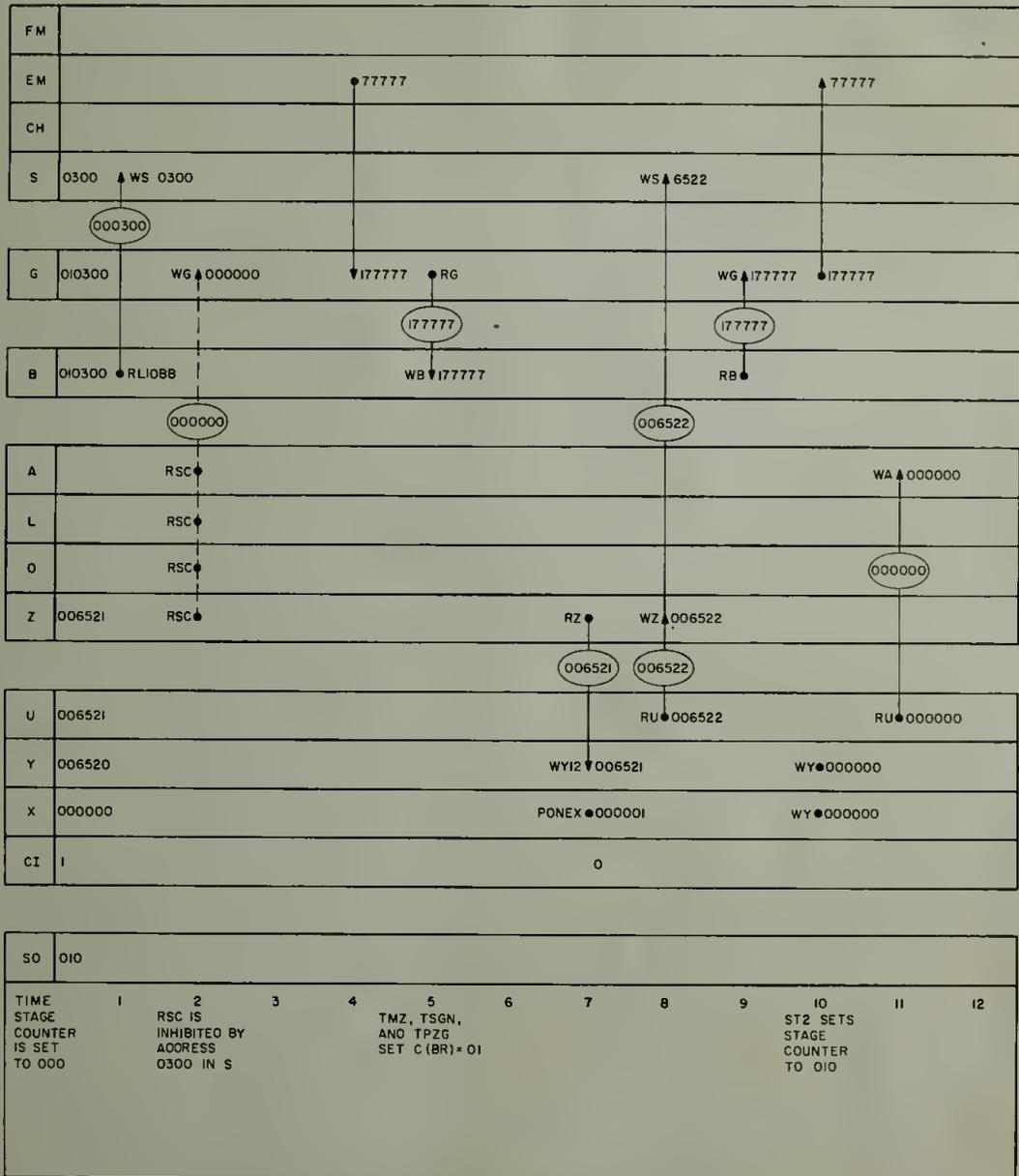
40702

Figure 4-21. Subinstruction TC0, with Implied Address Code EXTEND, Data Transfer Diagram



40703

Figure 4-22. Subinstruction CCS0, Branch on Quantity Greater Than Plus Zero, Data Transfer Diagram



40704

Figure 4-23. Subinstruction CCS0, Branch on Minus Zero, Data Transfer Diagram

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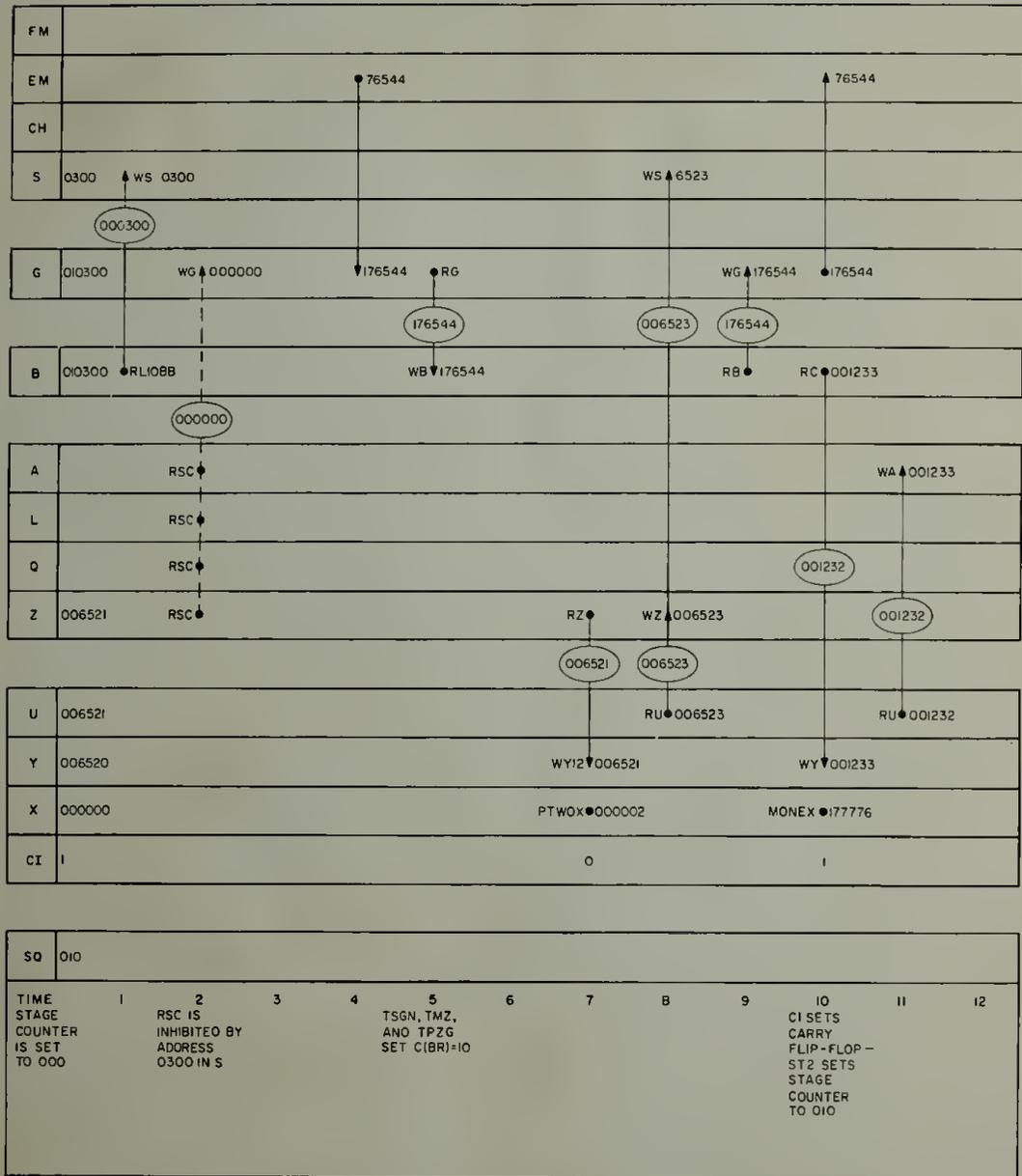
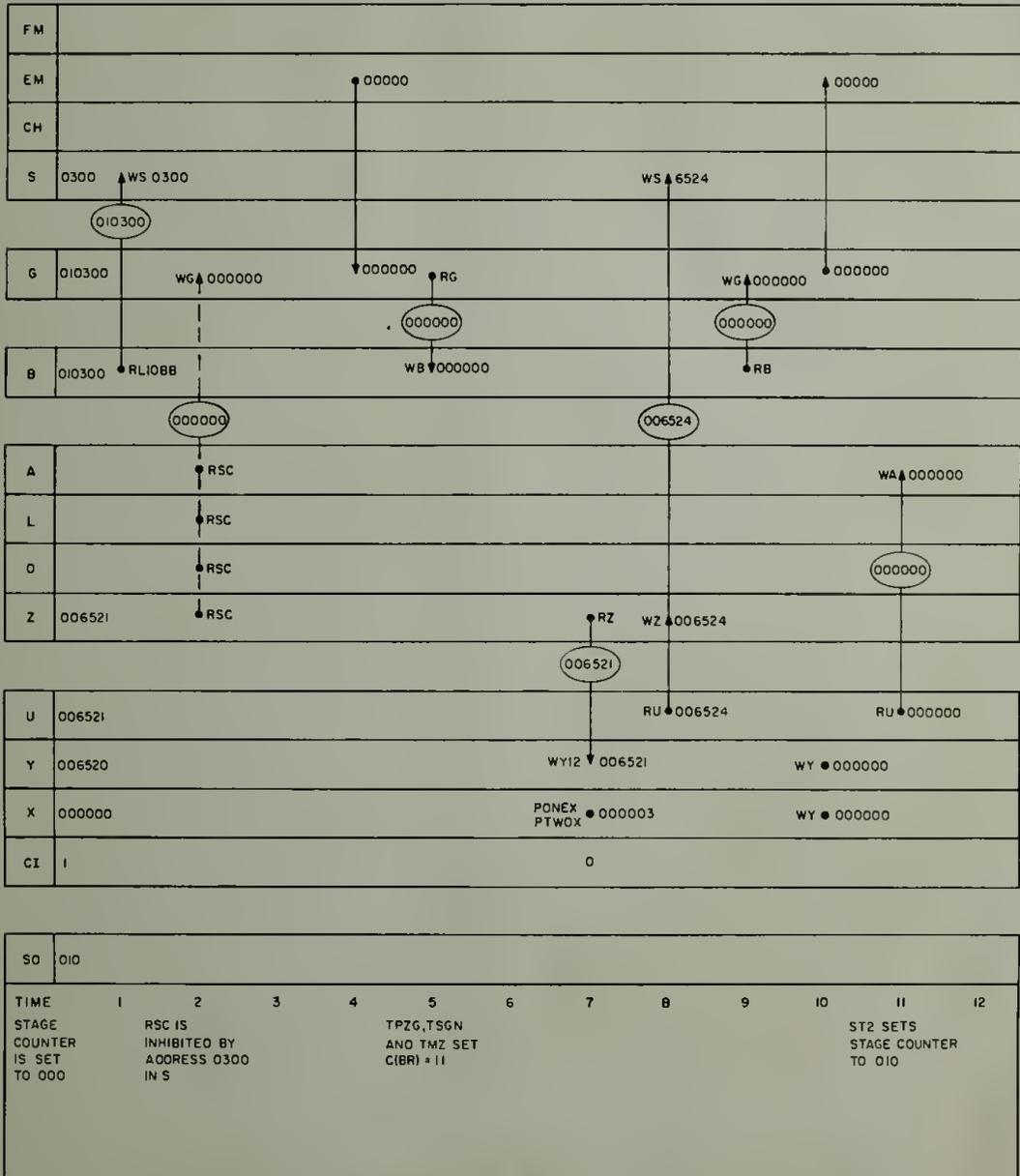


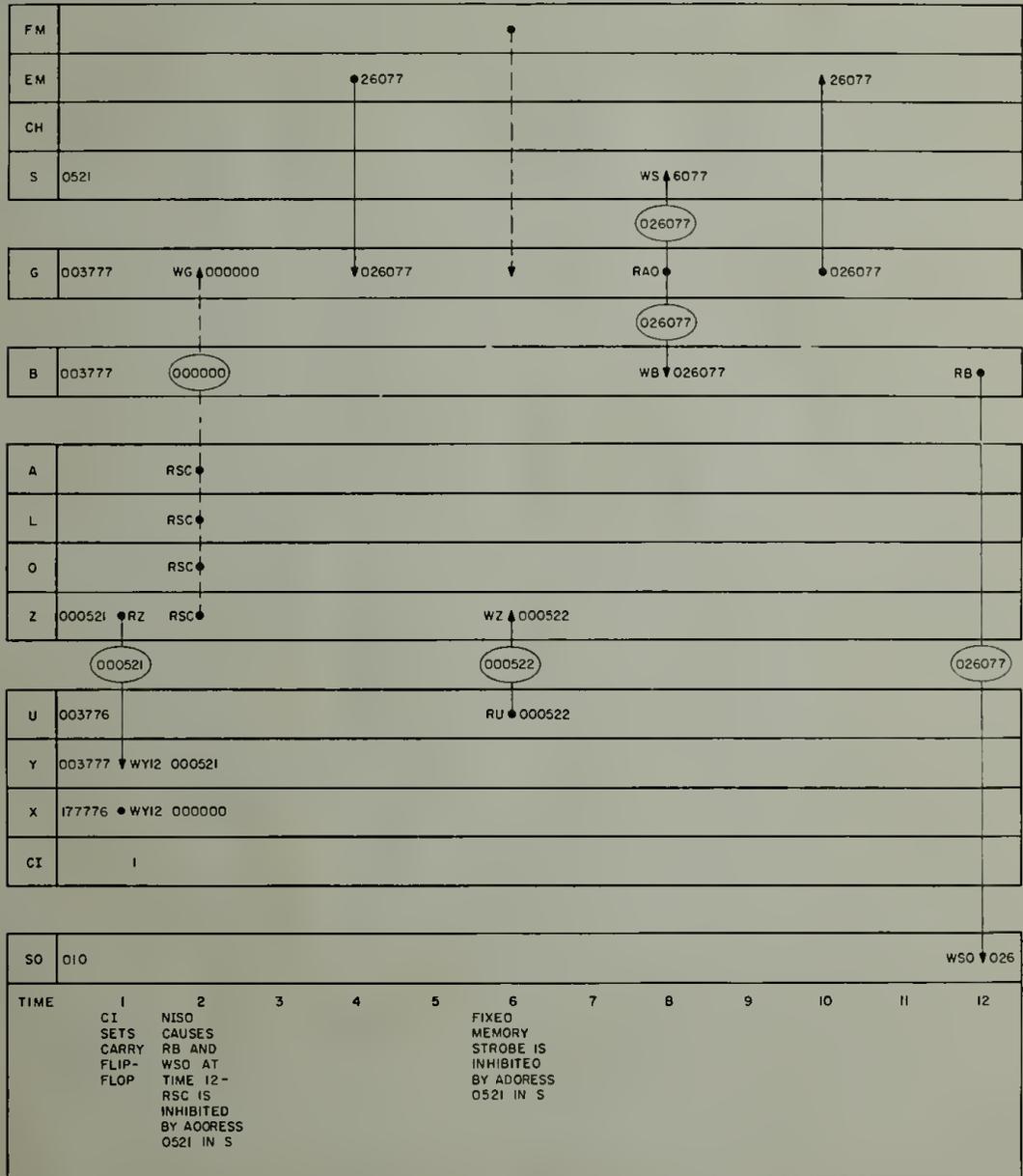
Figure 4-24. Subinstruction CCS0, Branch on Quantity Less Than Minus Zero, Data Transfer Diagram

40705



40706

Figure 4-25. Subinstruction CCS0, Branch on Plus 0, Data Transfer Diagram



40707

Figure 4-26. Subinstruction STD2, Data Transfer Diagram

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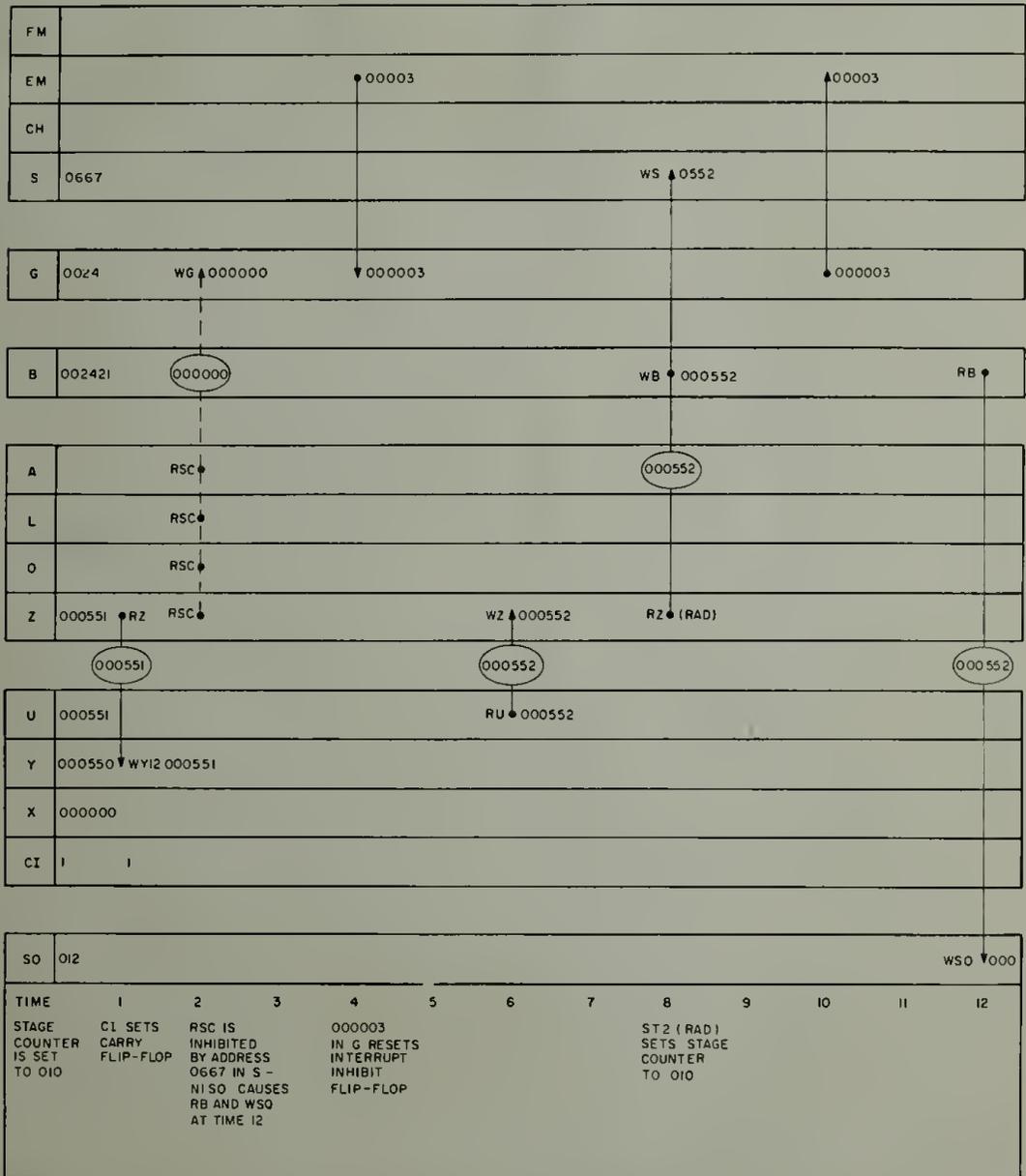


Figure 4-28. Subinstruction STD2, with Implied Address Code RELINT, Data Transfer Diagram

40709

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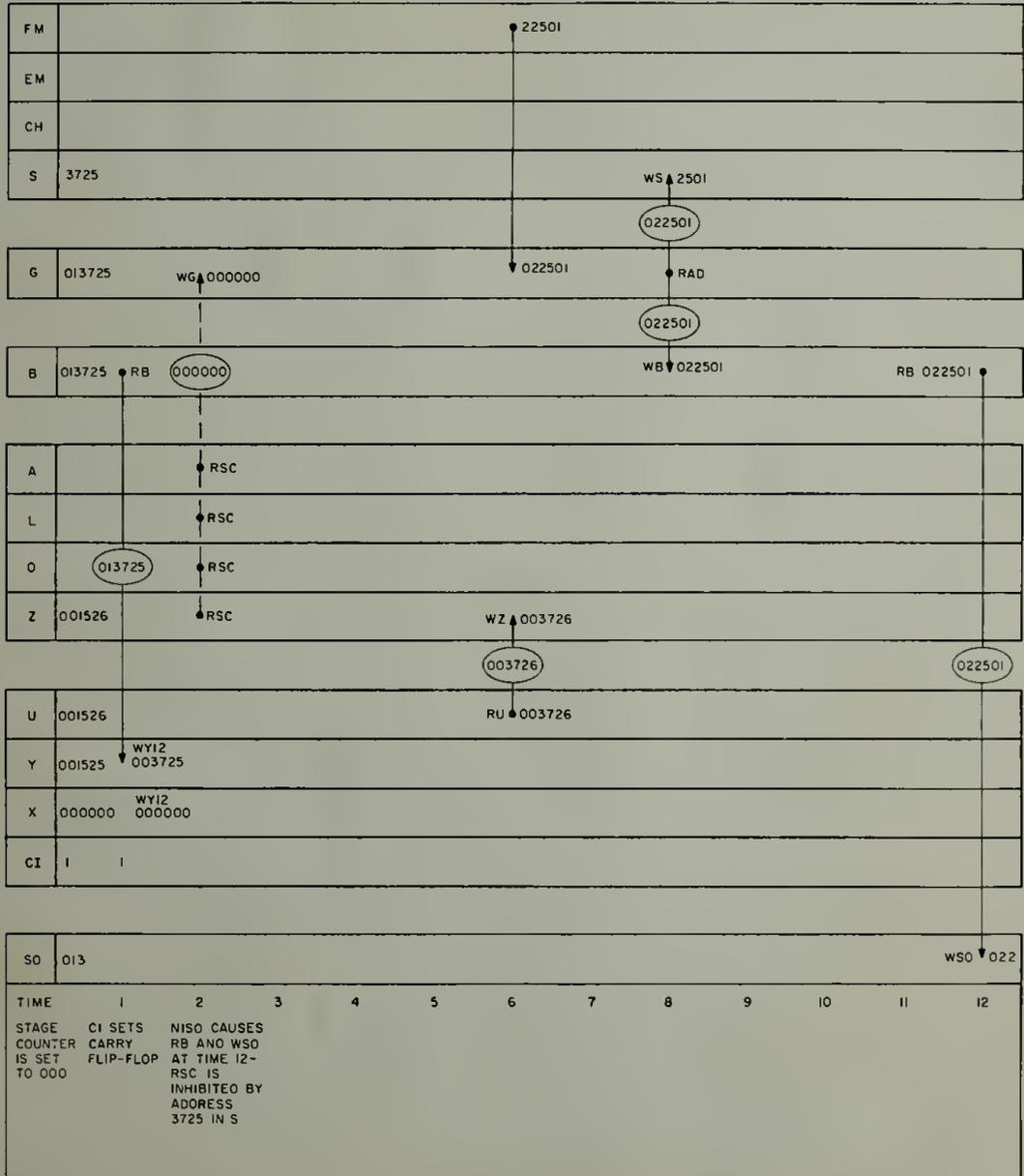
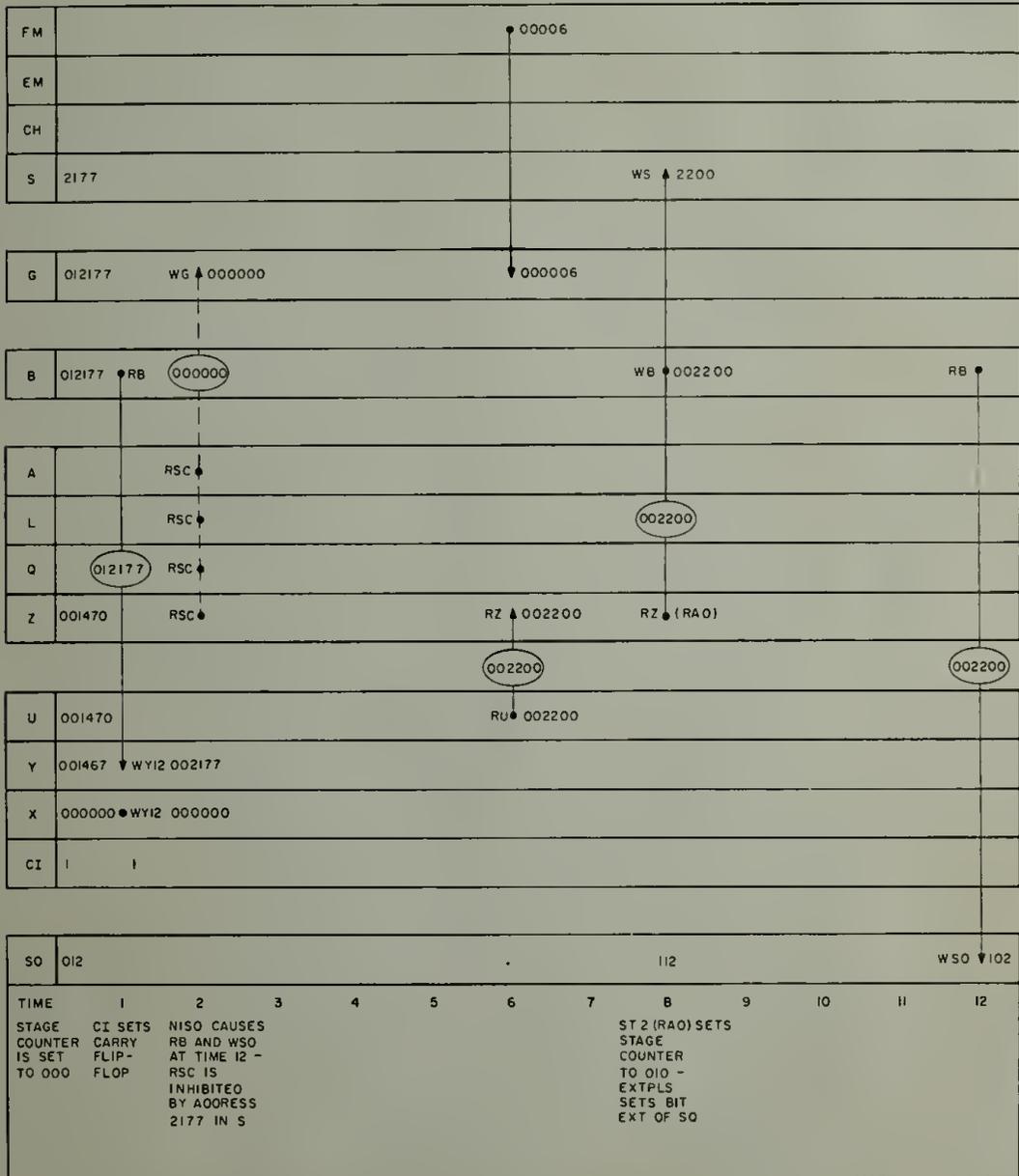


Figure 4-30. Subinstruction TCF0, Data Transfer Diagram

40711



40712

Figure 4-31. Subinstruction TCF0, with Implied Address Code EXTEND, Data Transfer Diagram

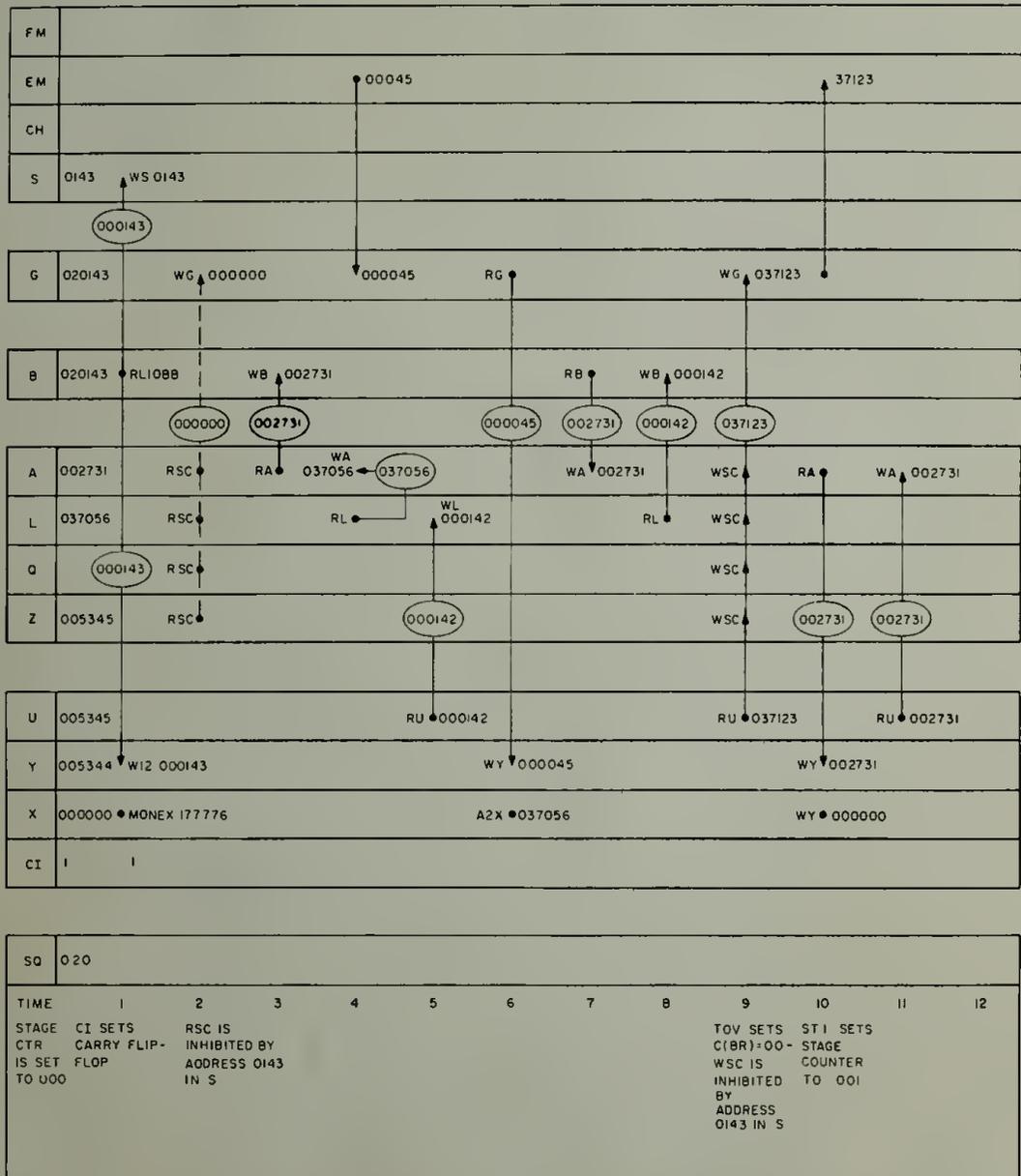
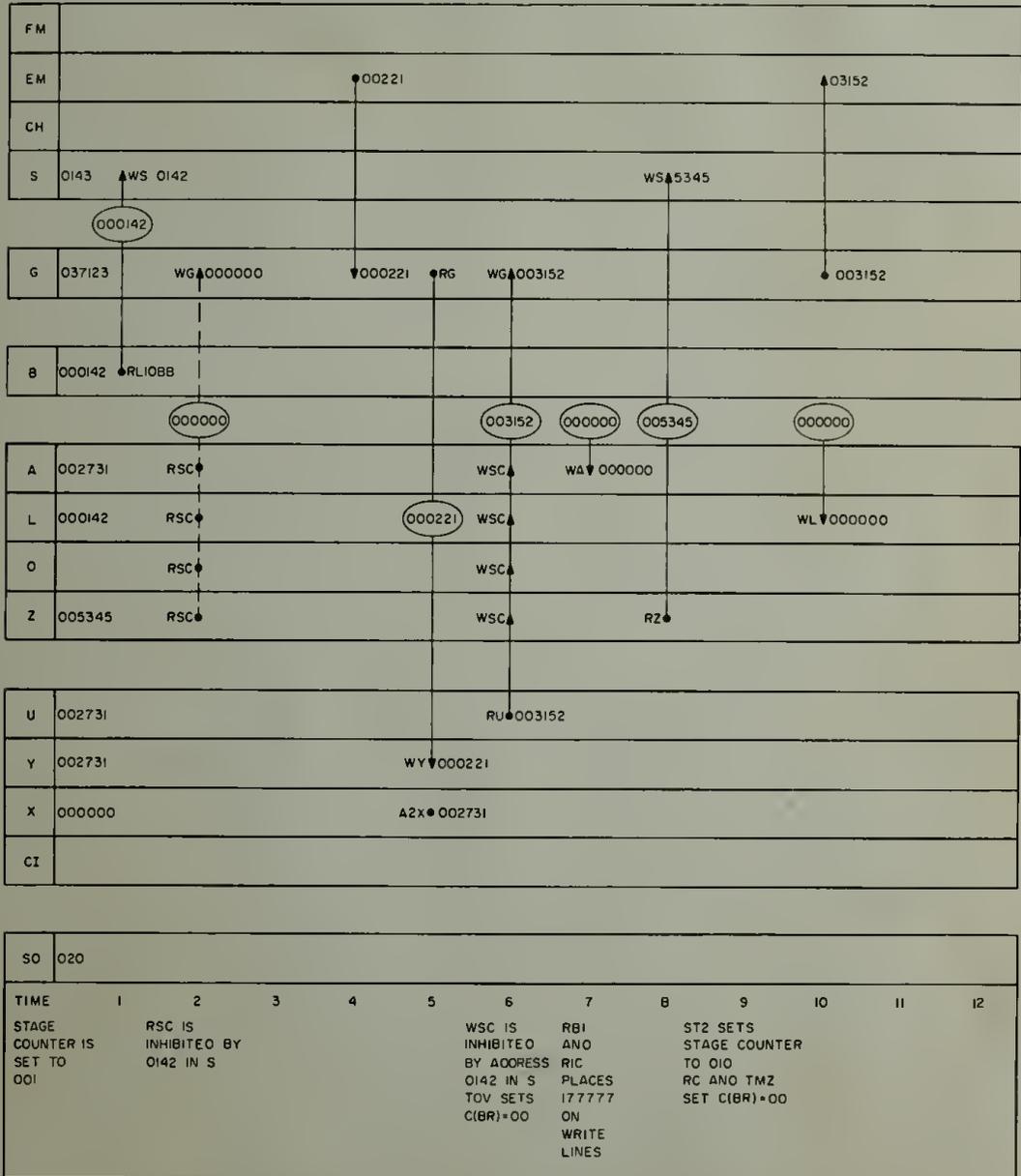


Figure 4-32. Subinstruction DAS0, without Overflow or Underflow, Data Transfer Diagram

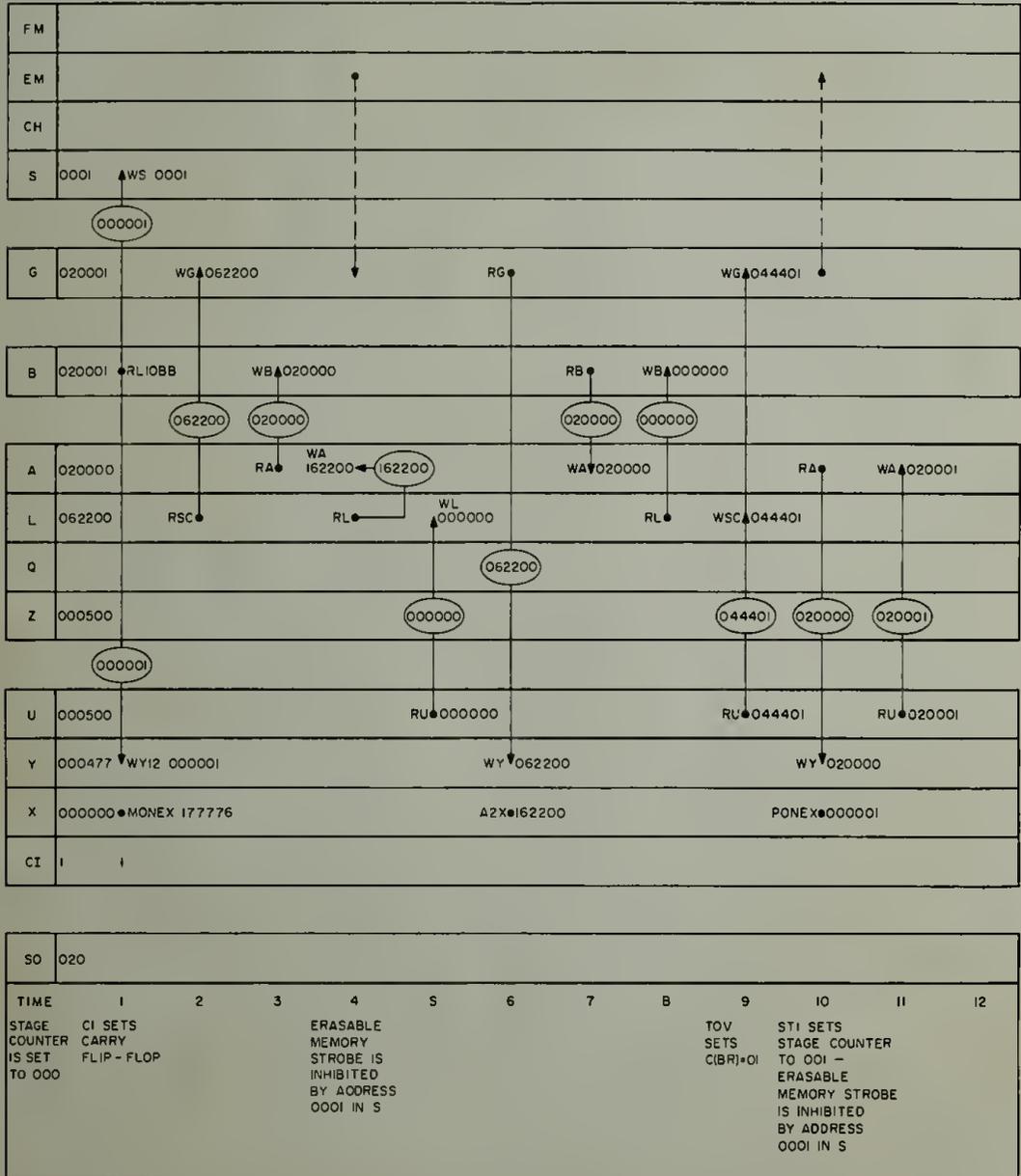
40713



40714

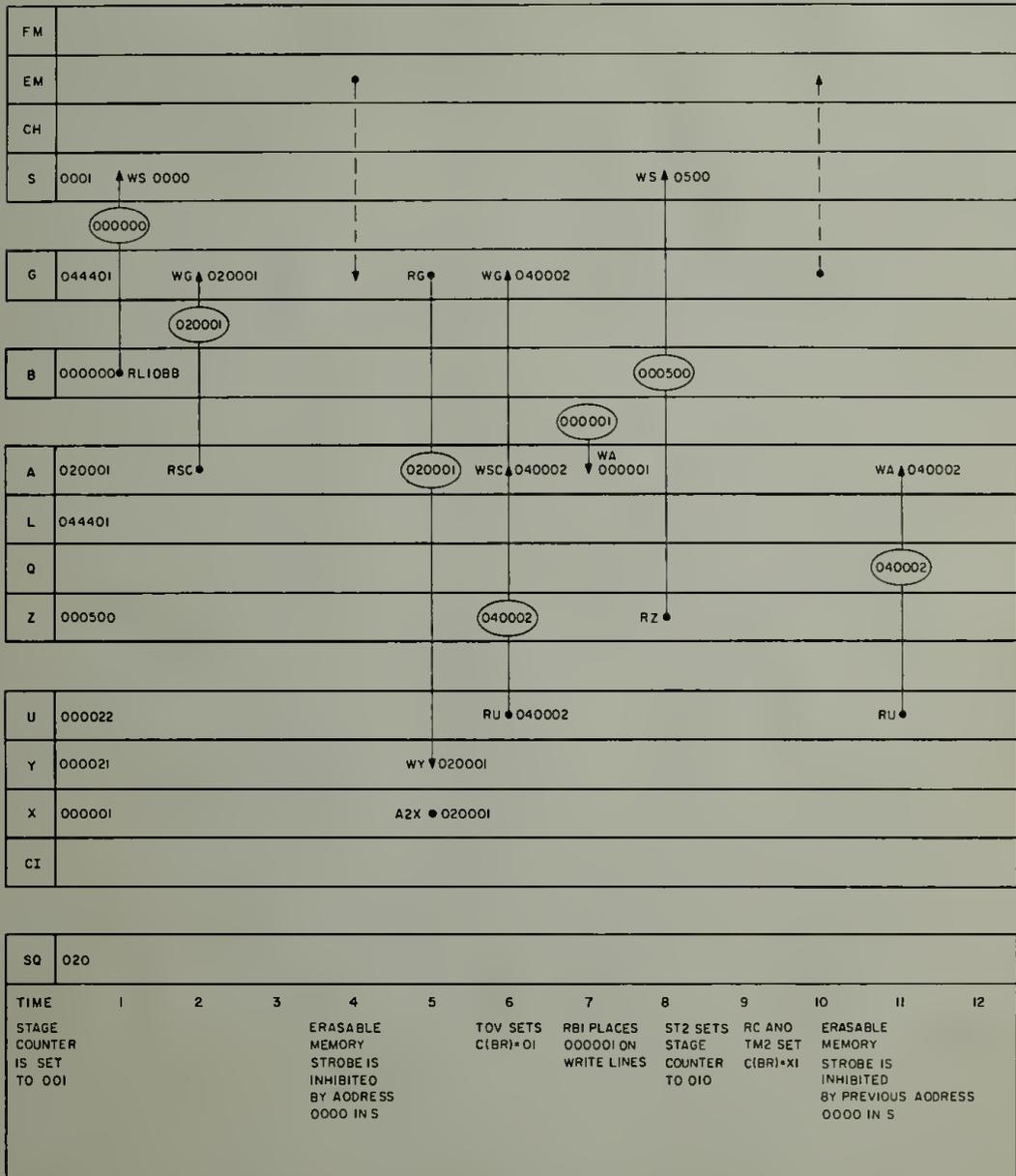
Figure 4-33. Subinstruction DAS1, without Overflow or Underflow, Data Transfer Diagram

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43715

Figure 4-34. Subinstruction DAS0, with Overflow and Implied Address Code DDOUBL, Data Transfer Diagram



40716

Figure 4-35. Subinstruction DAS1, with Overflow and Implied Address Code DDOUBL, Data Transfer Diagram

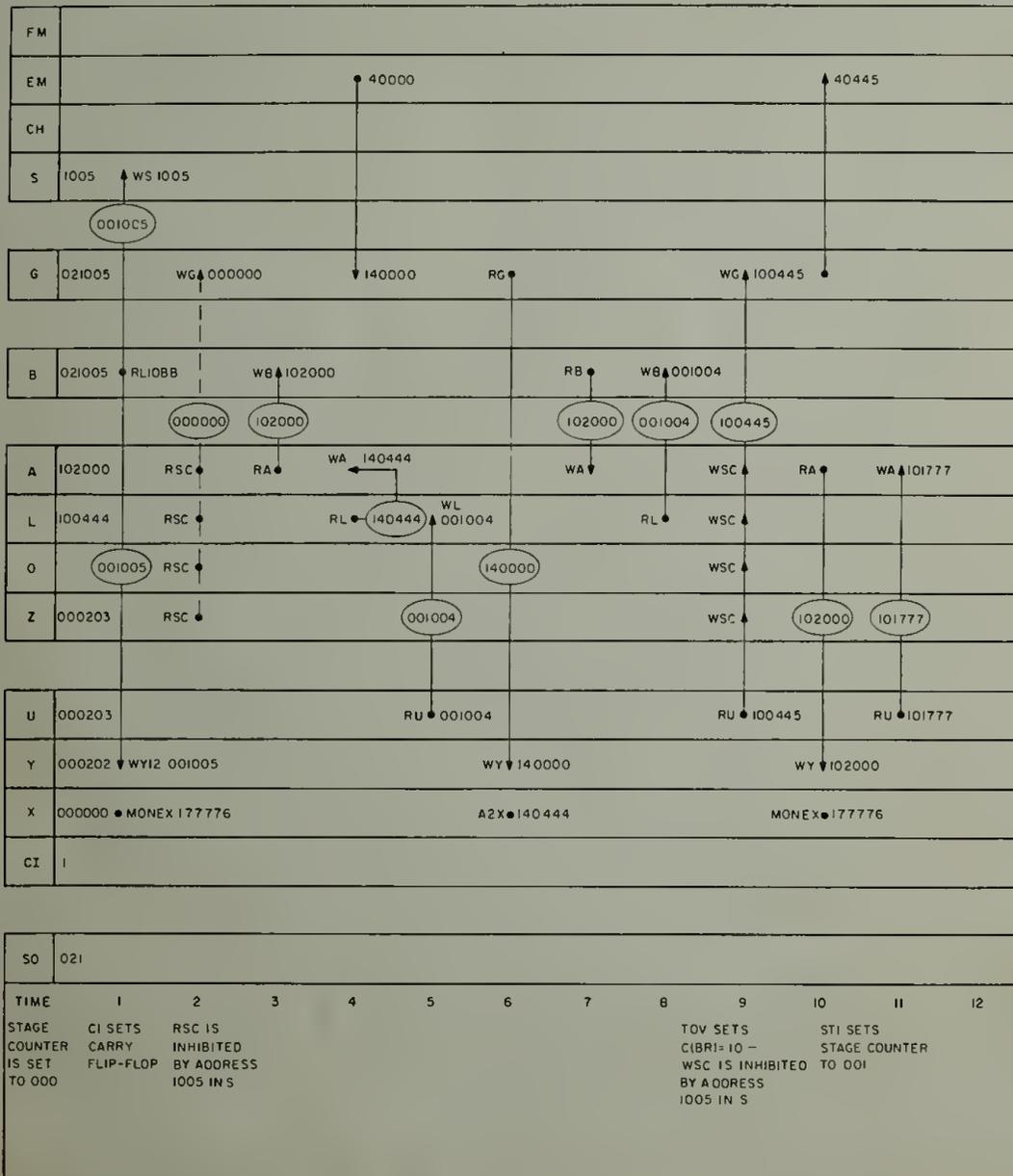


Figure 4-36. Subinstruction DAS0, with Underflow, Data Transfer Diagram

40717

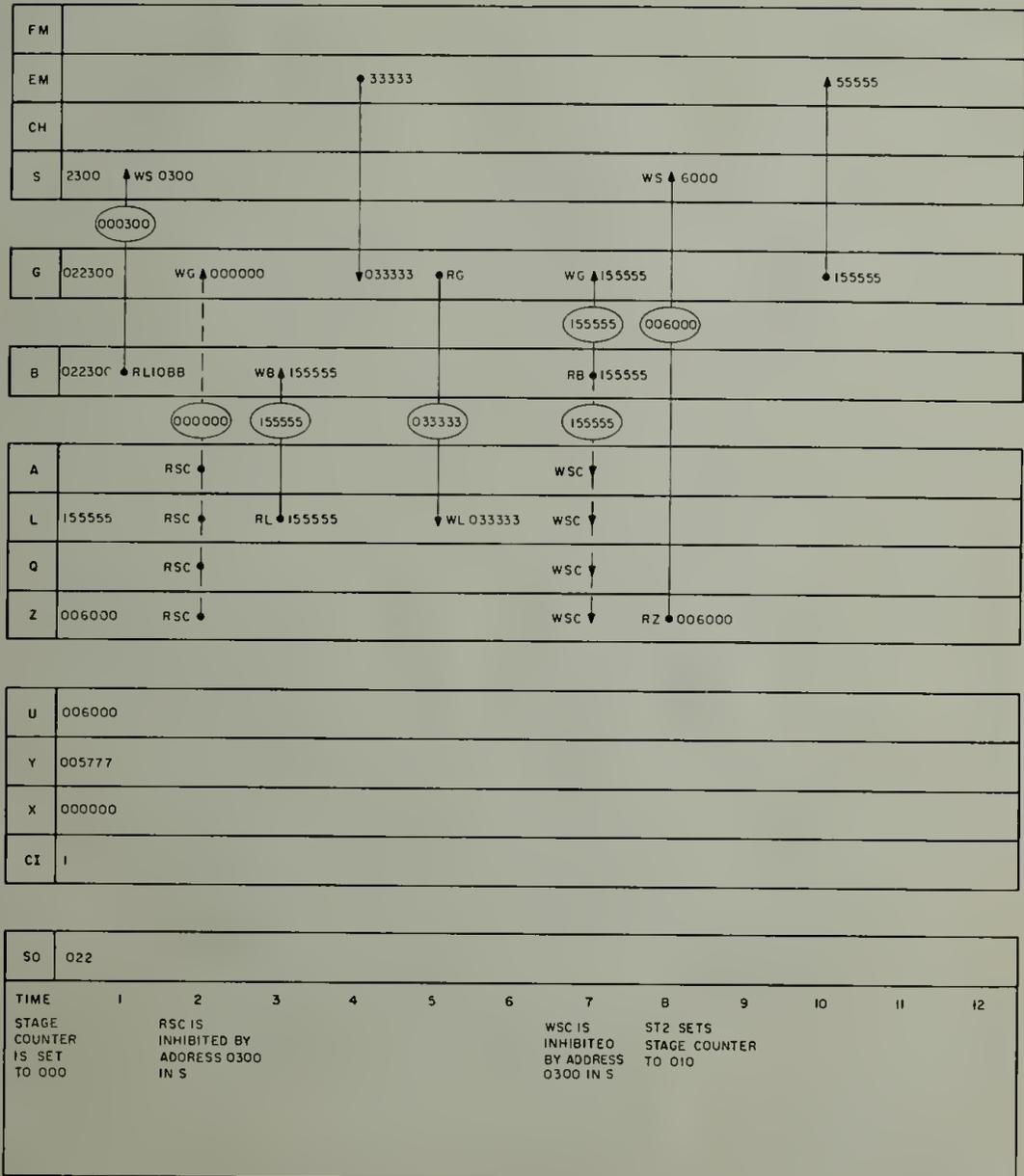


Figure 4-38. Subinstruction LXCH0, Data Transfer Diagram

30719

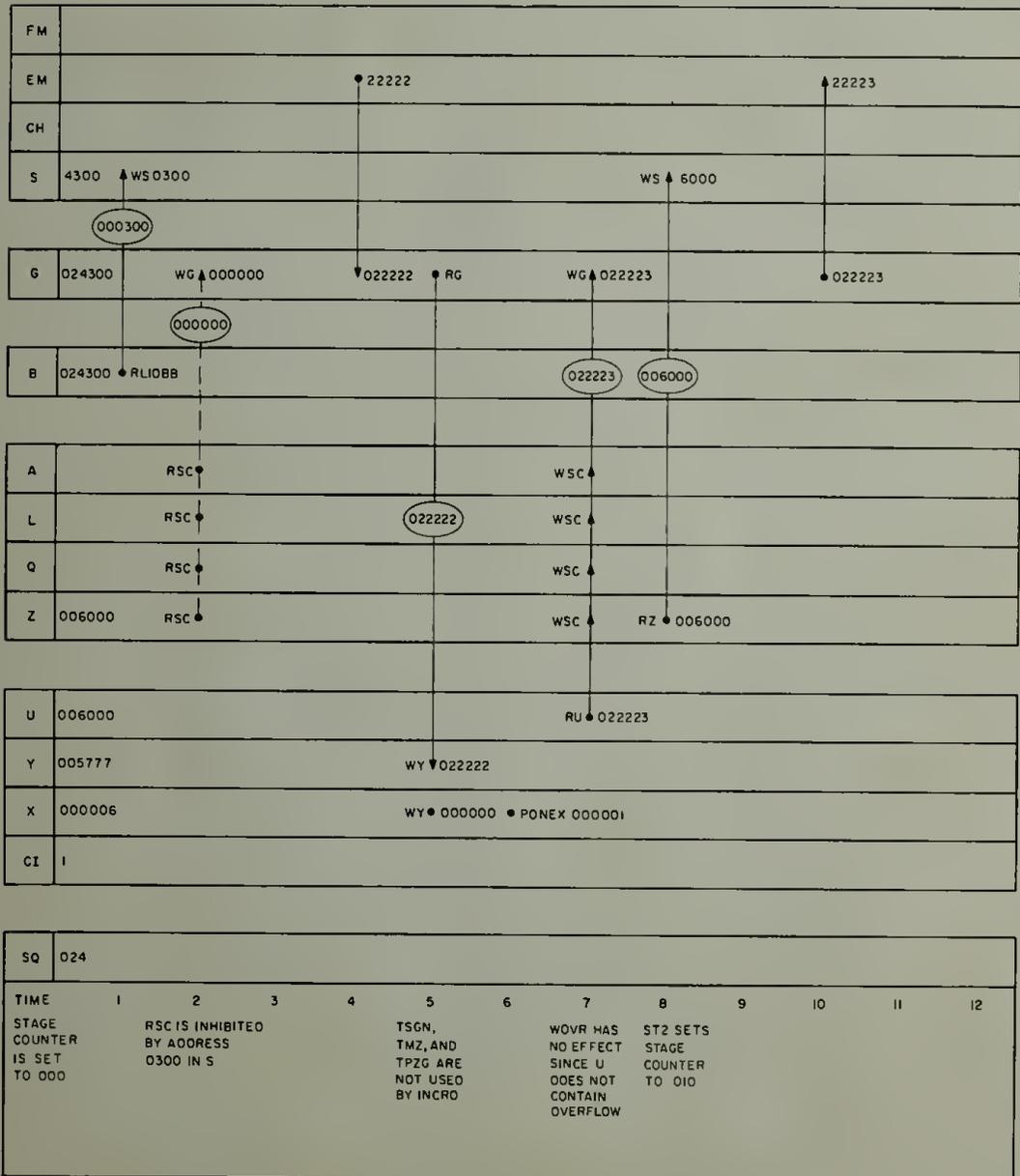


Figure 4-39. Subinstruction INCR0, Data Transfer Diagram

40720

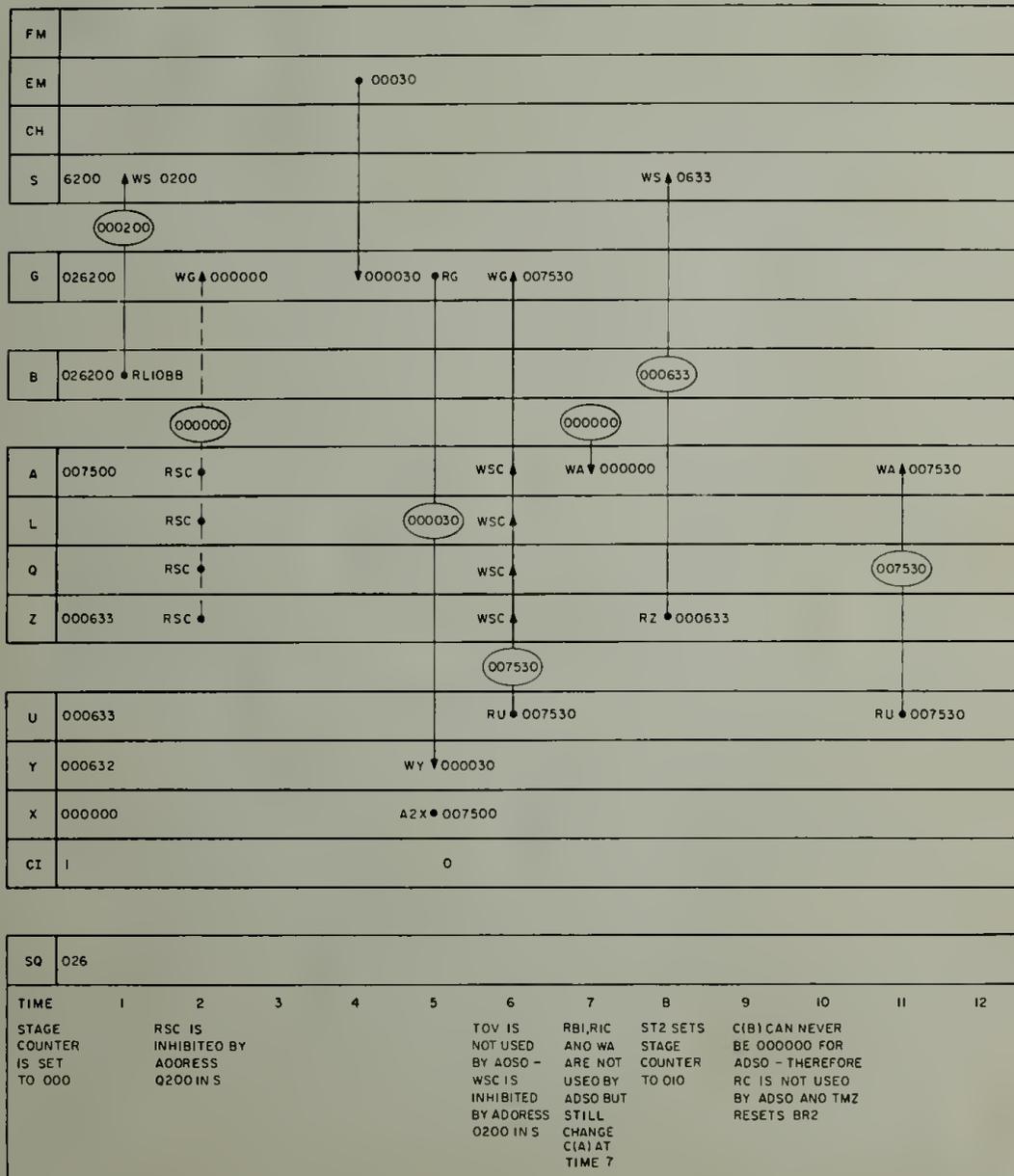
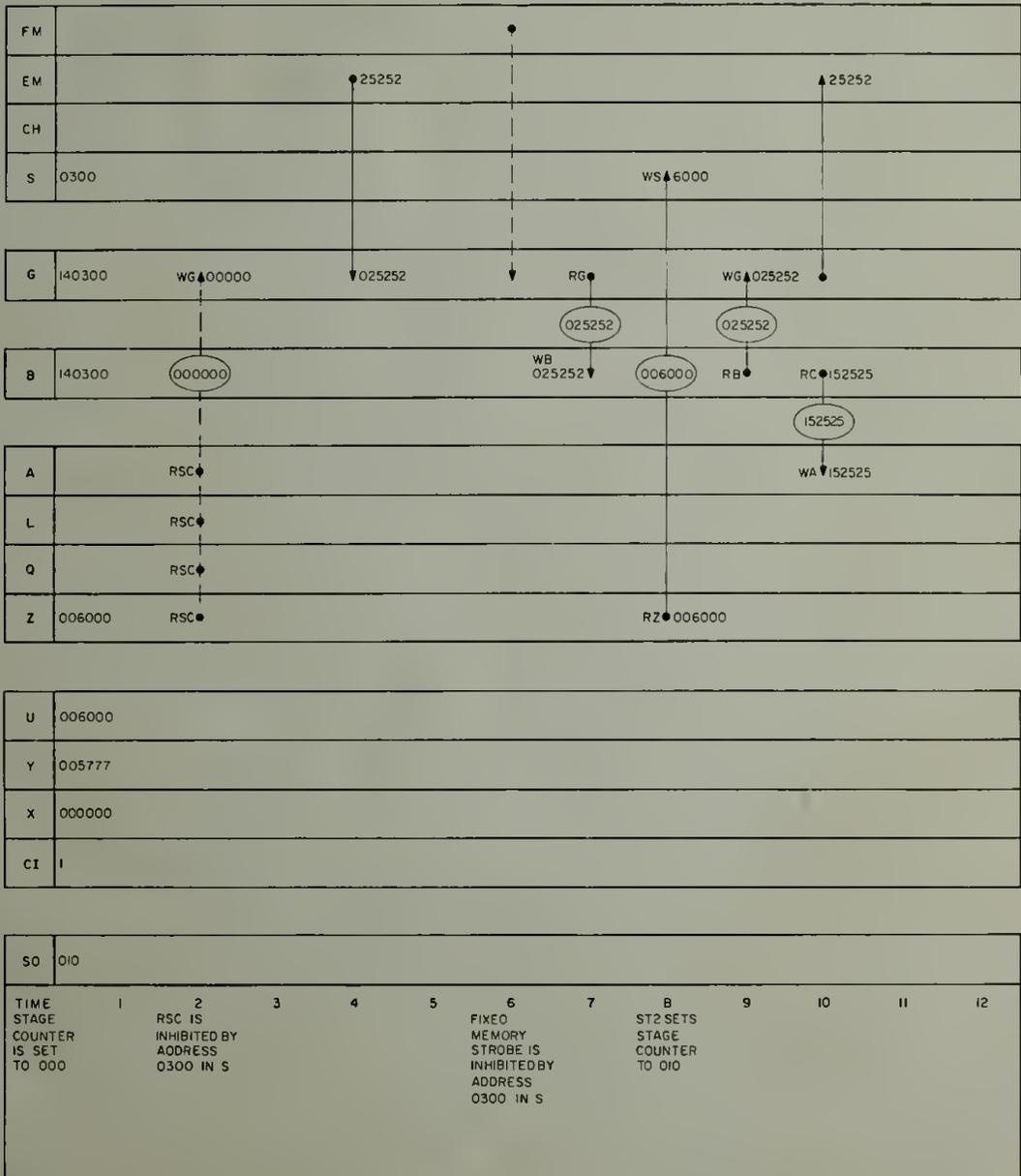


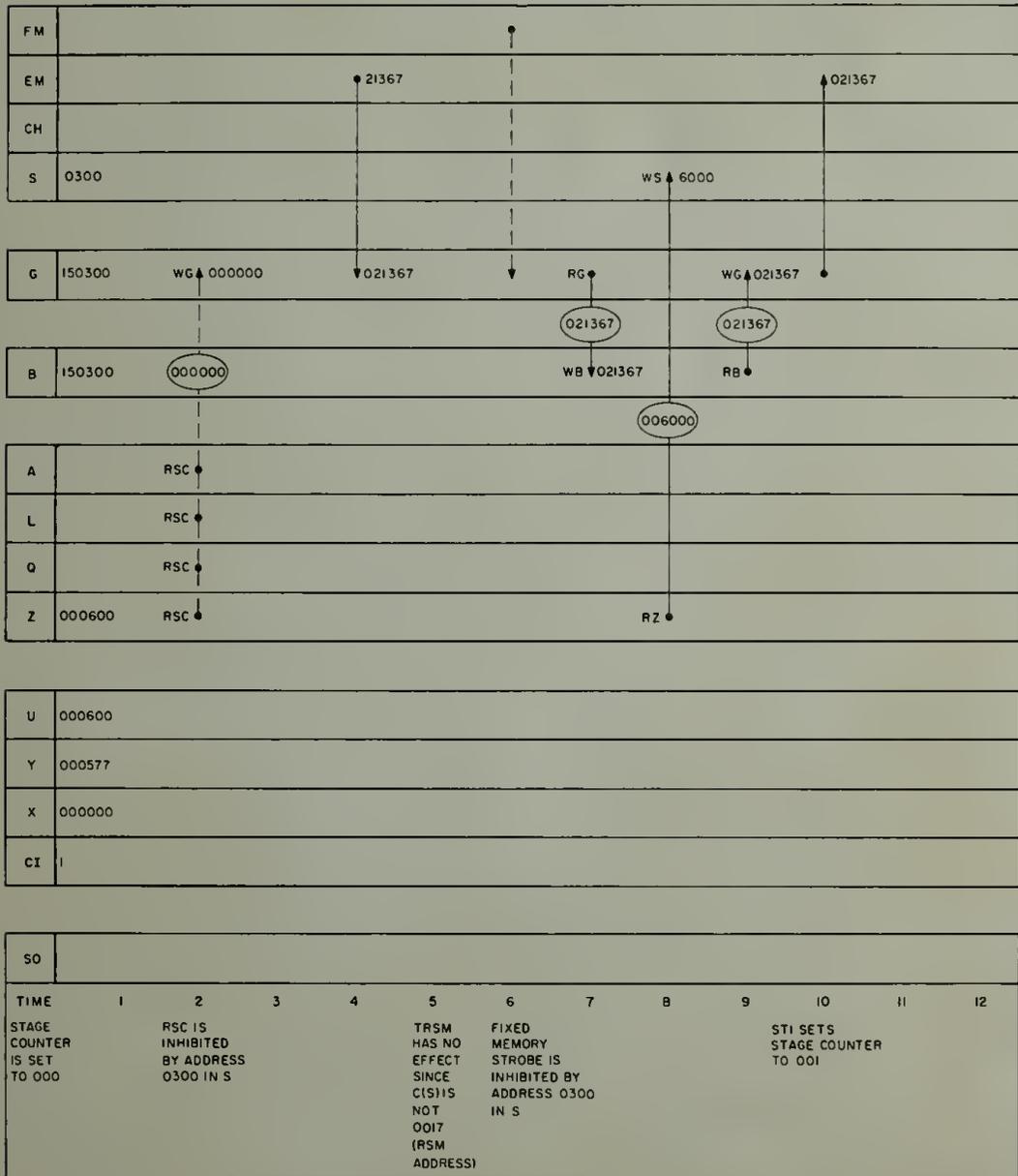
Figure 4-40. Subinstruction ADS0, Data Transfer Diagram

40721



40723

Figure 4-42. Subinstruction CS0, Data Transfer Diagram



40724

Figure 4-43. Subinstruction NDX0, Data Transfer Diagram

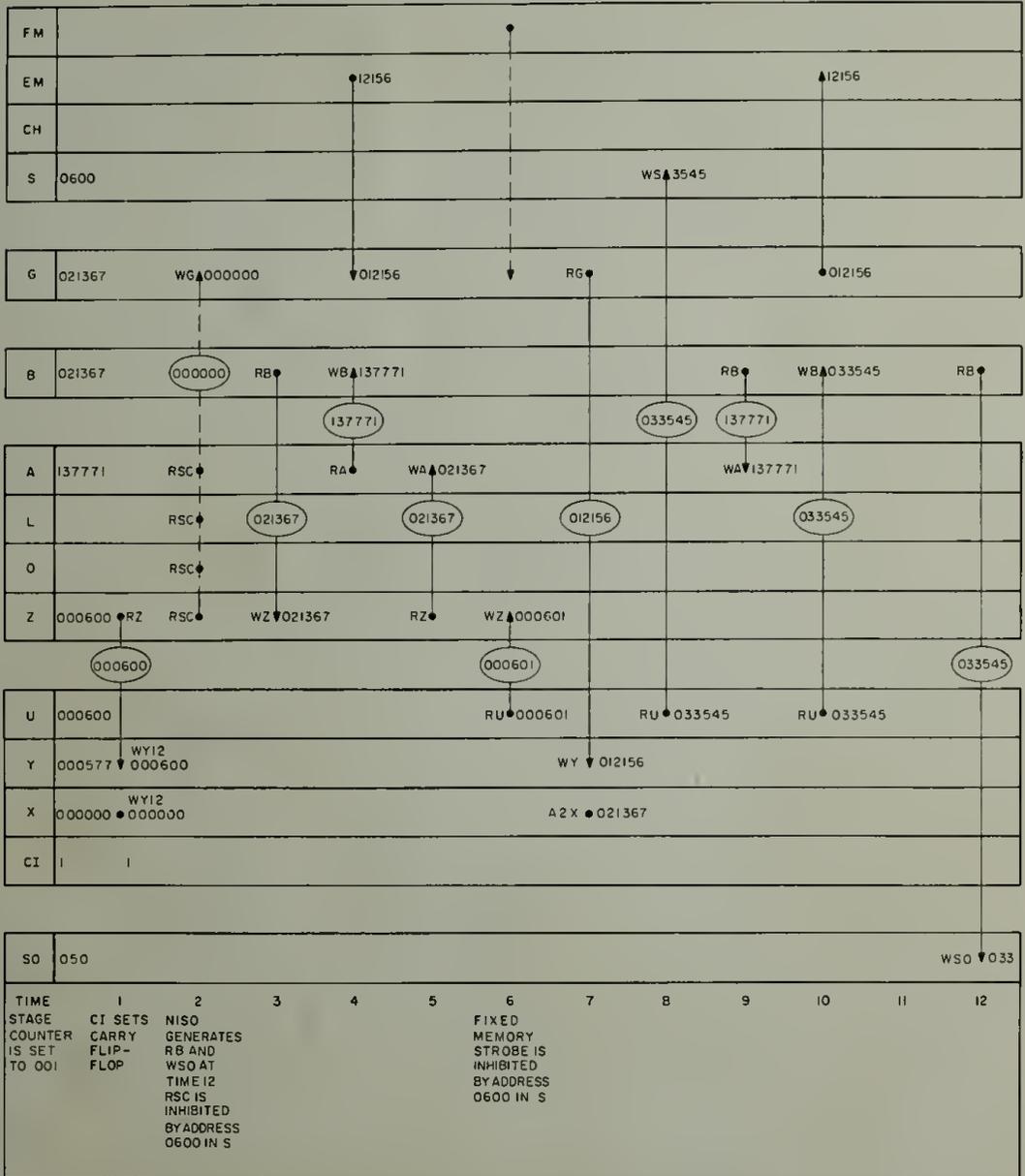


Figure 4-44. Subinstruction NDX1, Data Transfer Diagram

40725

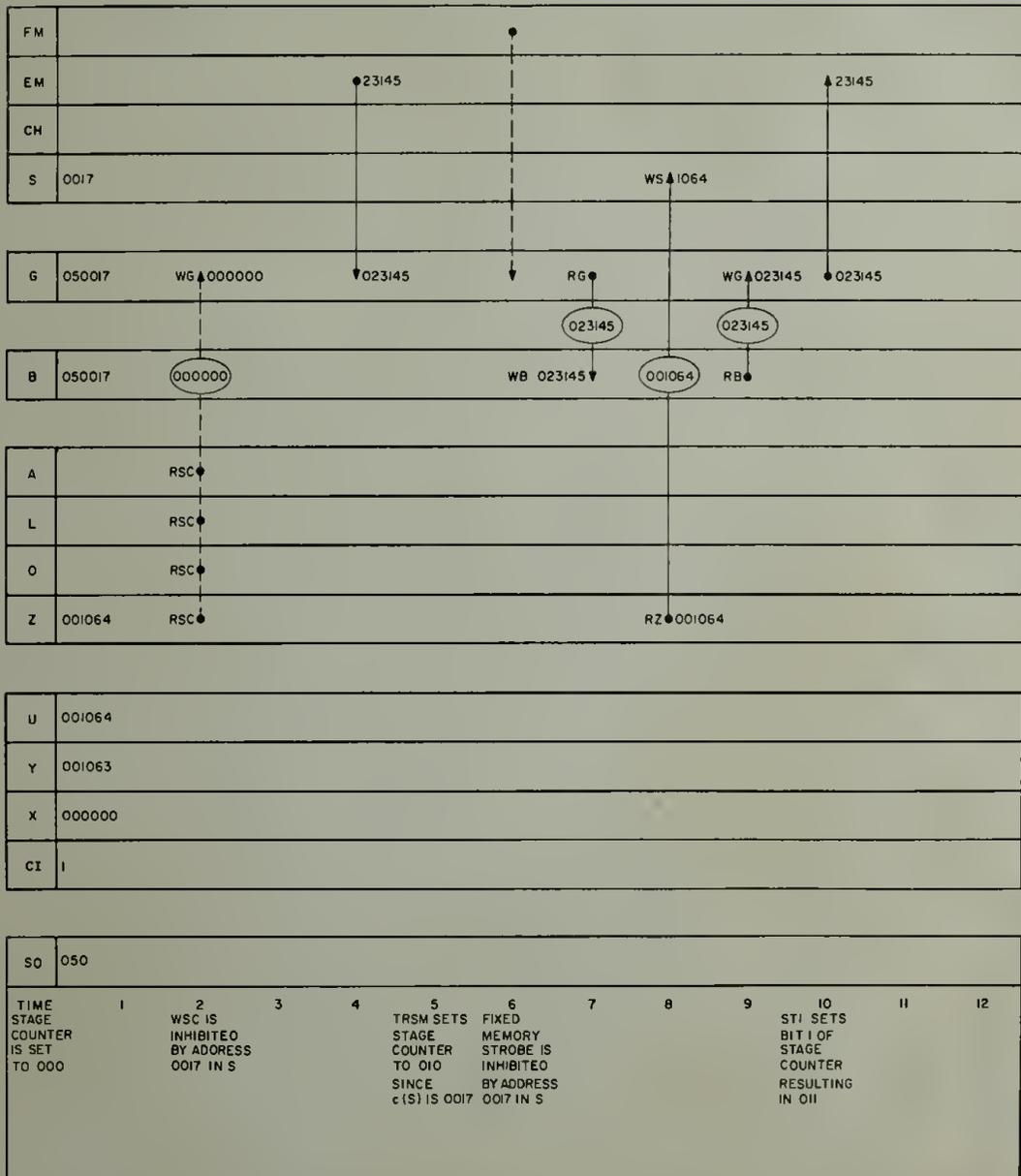
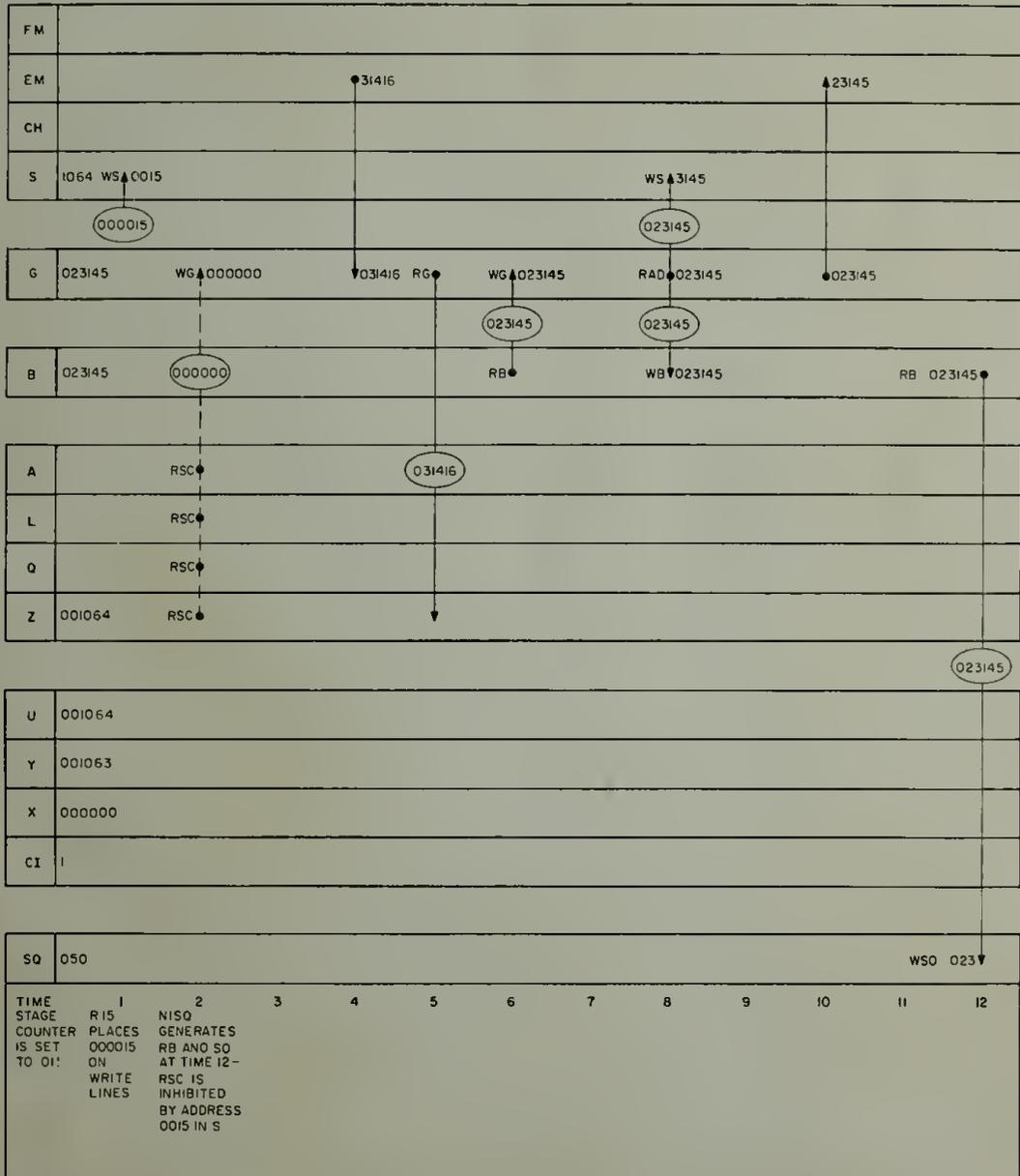


Figure 4-45. Subinstruction NDX0, with Implied Address Code RESUME, Data Transfer Diagram

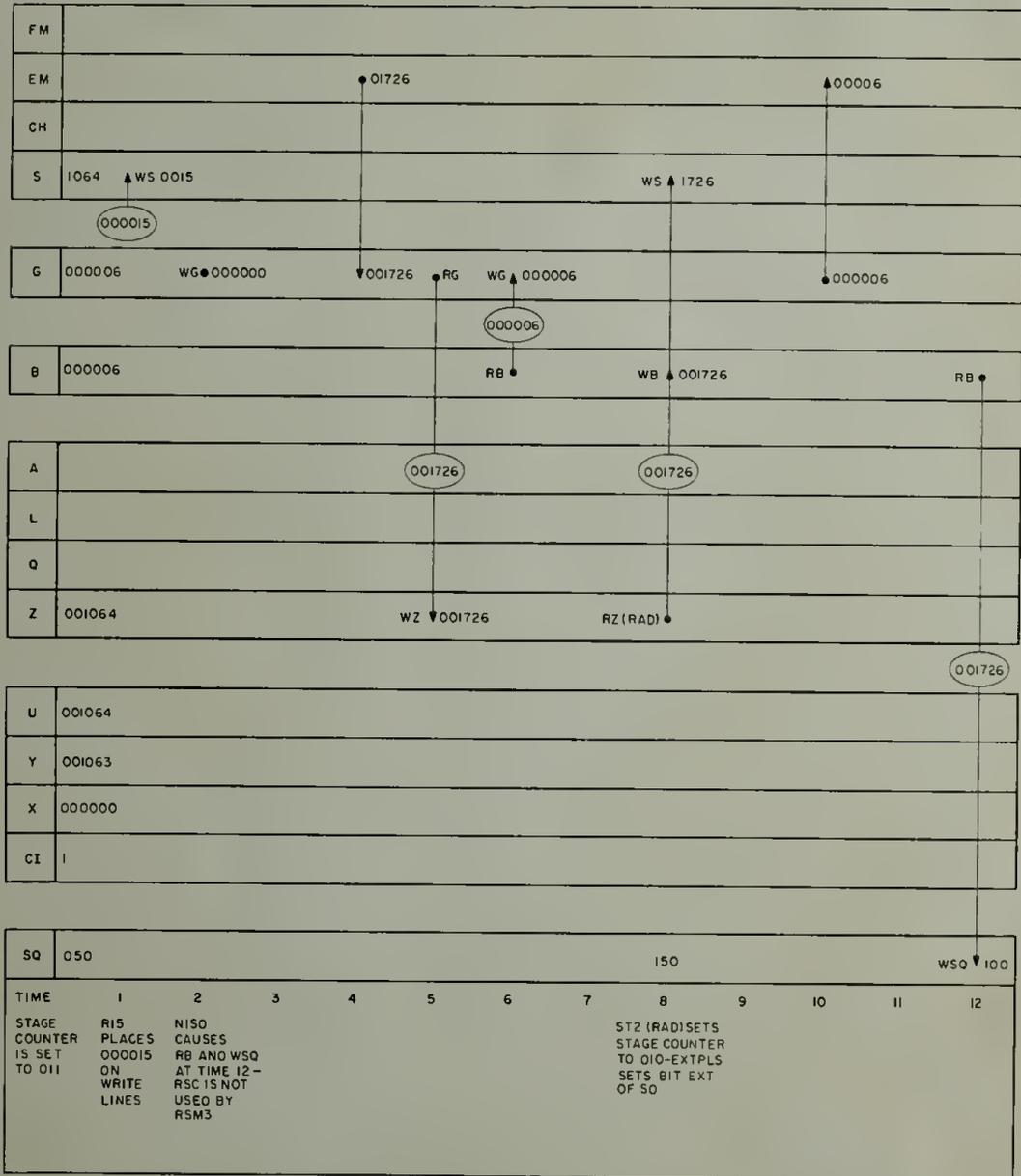
40726

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Figure 4-46. Subinstruction RSM3, Data Transfer Diagram



40728

Figure 4-47. Subinstruction RSM3, with Implied Address Code EXTEND, Data Transfer Diagram

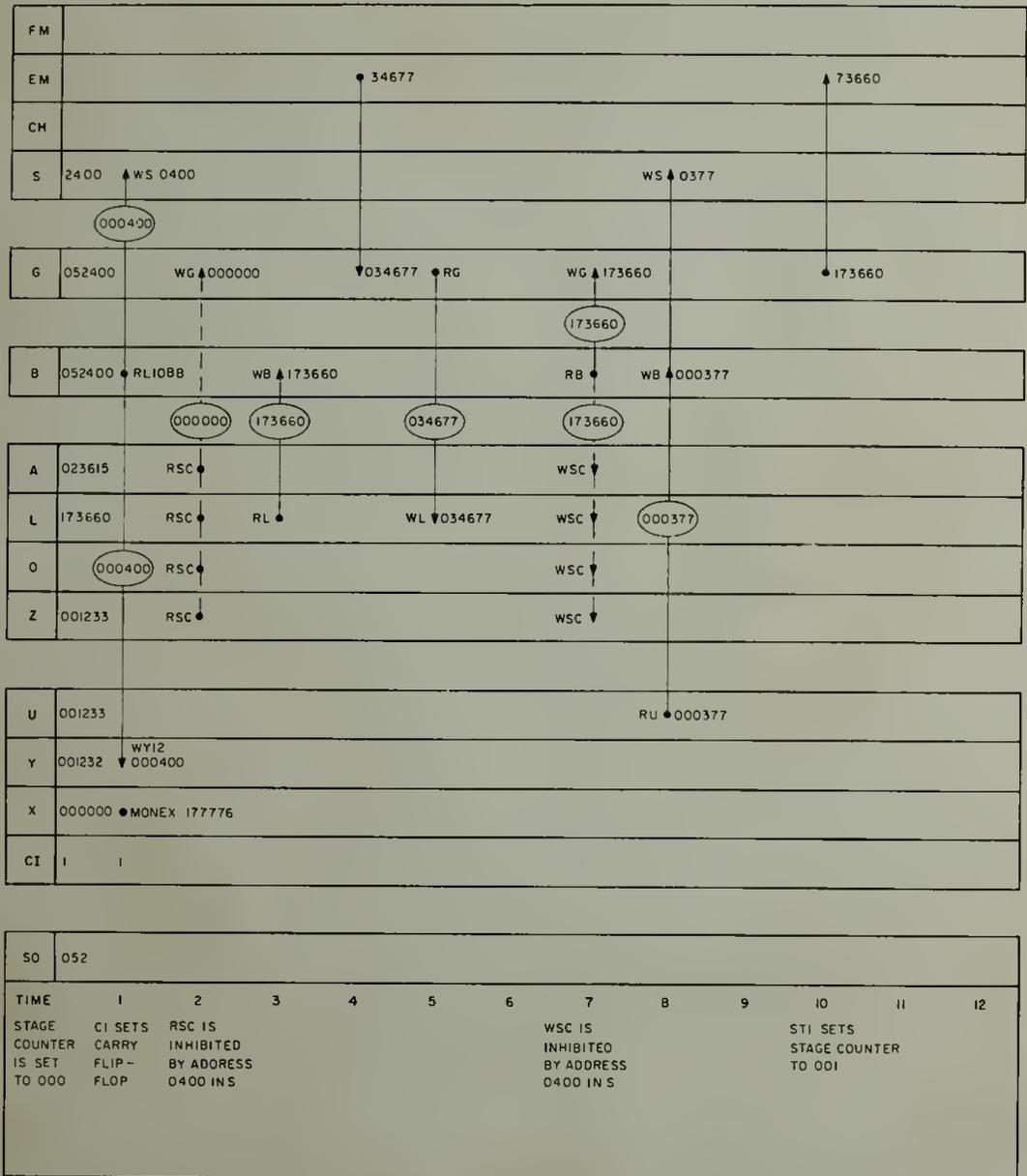


Figure 4-48. Subinstruction DXCH0, Data Transfer Diagram

40729

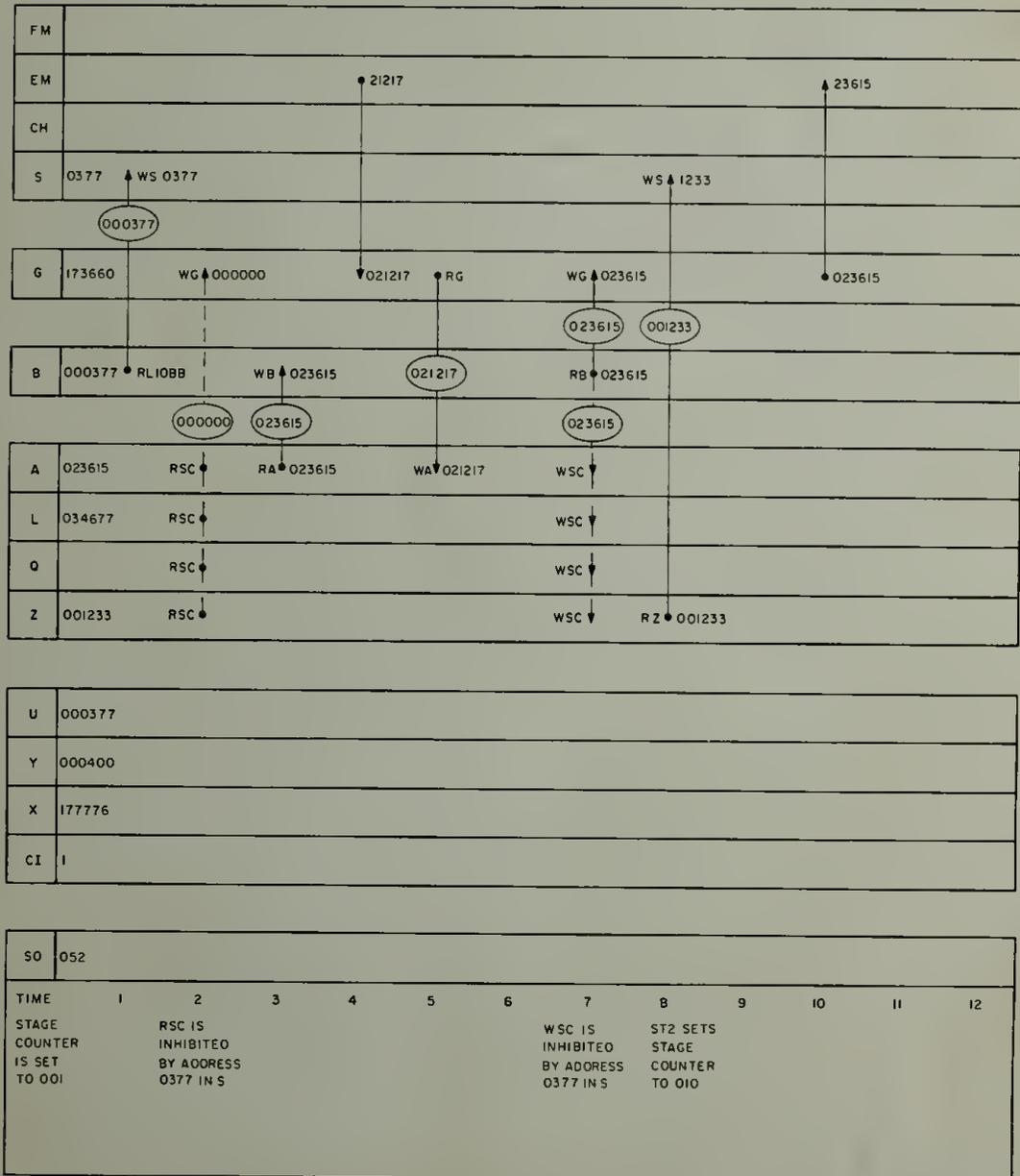
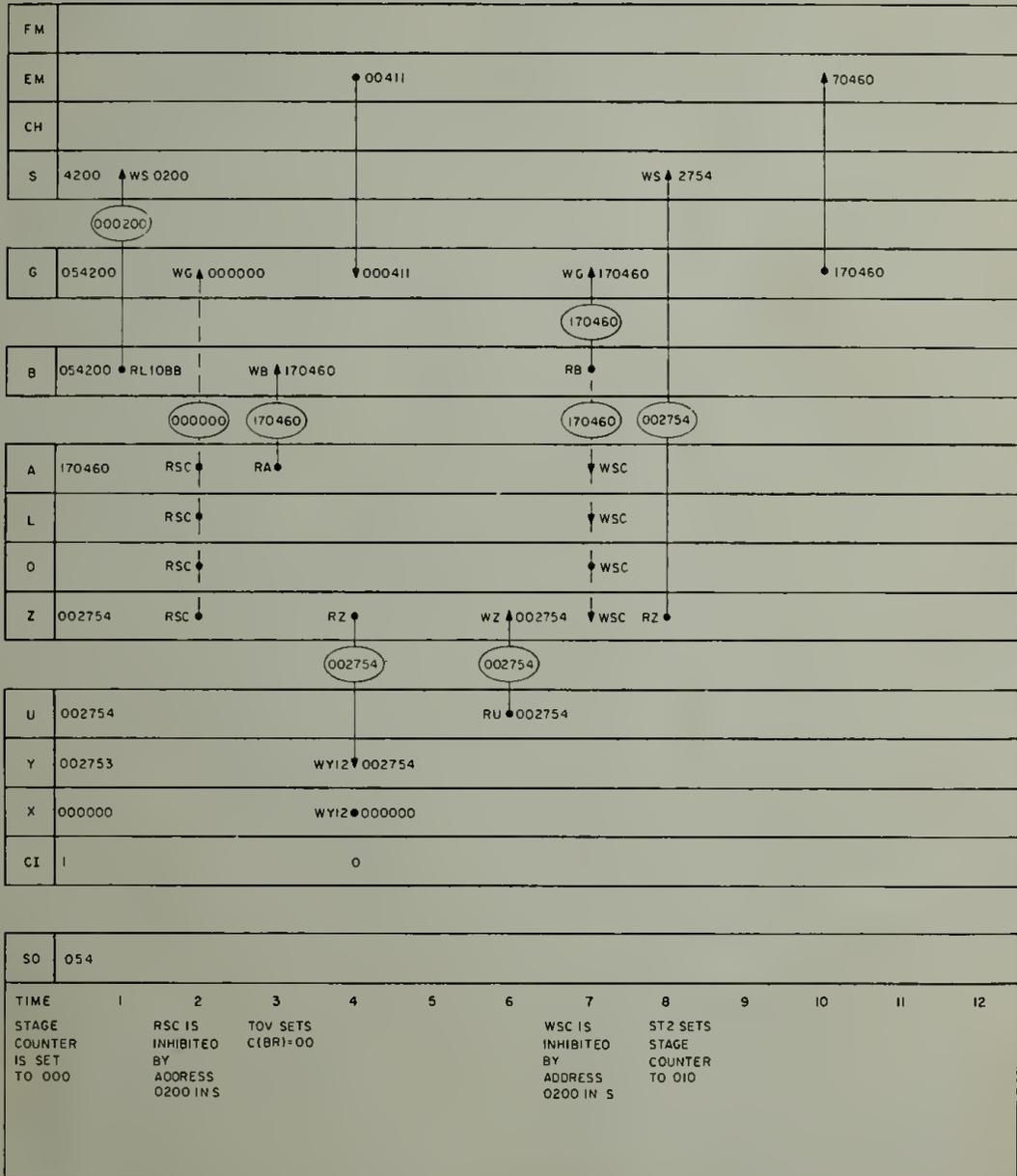


Figure 4-49. Subinstruction DXCH1, Data Transfer Diagram

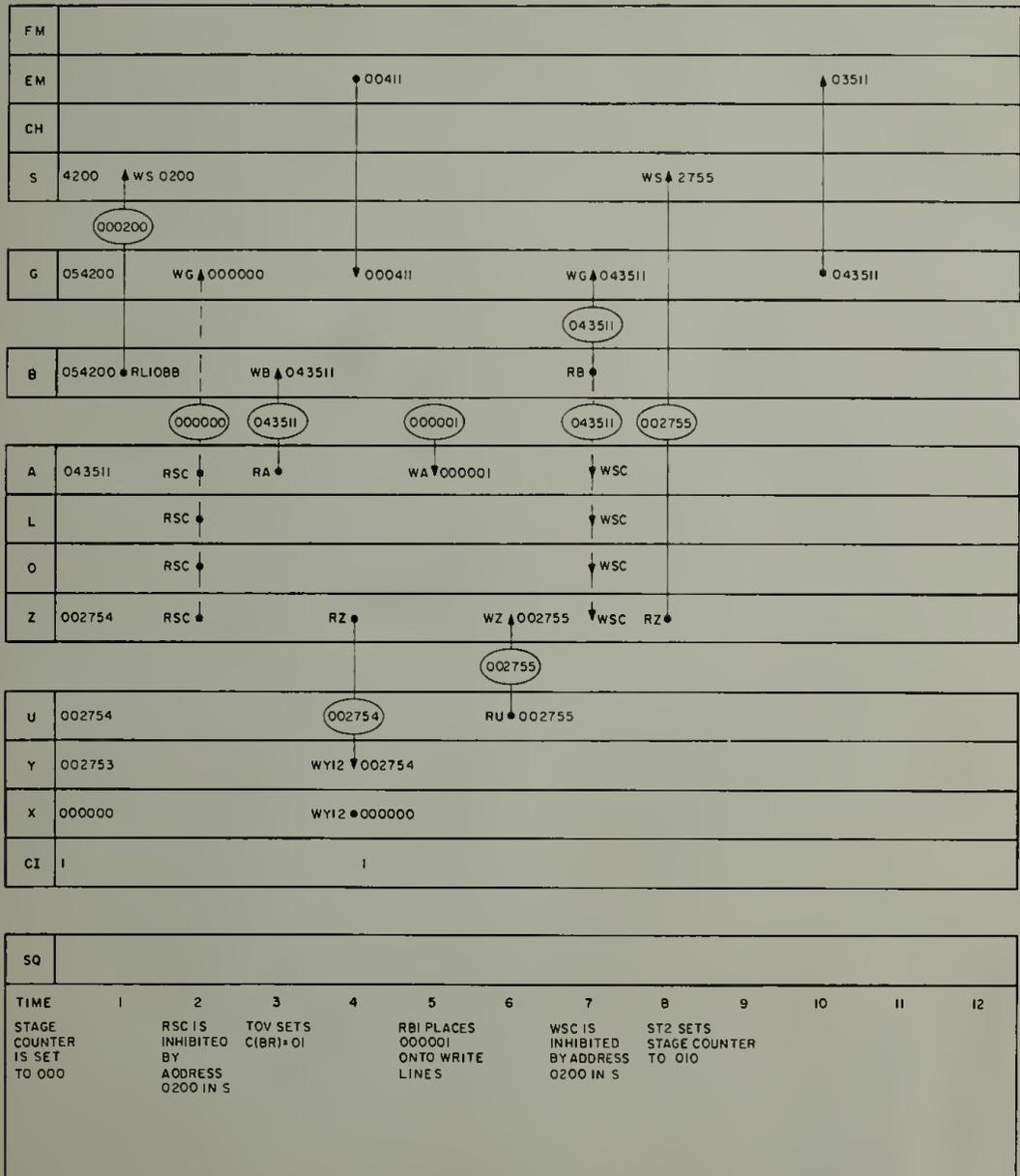
40730

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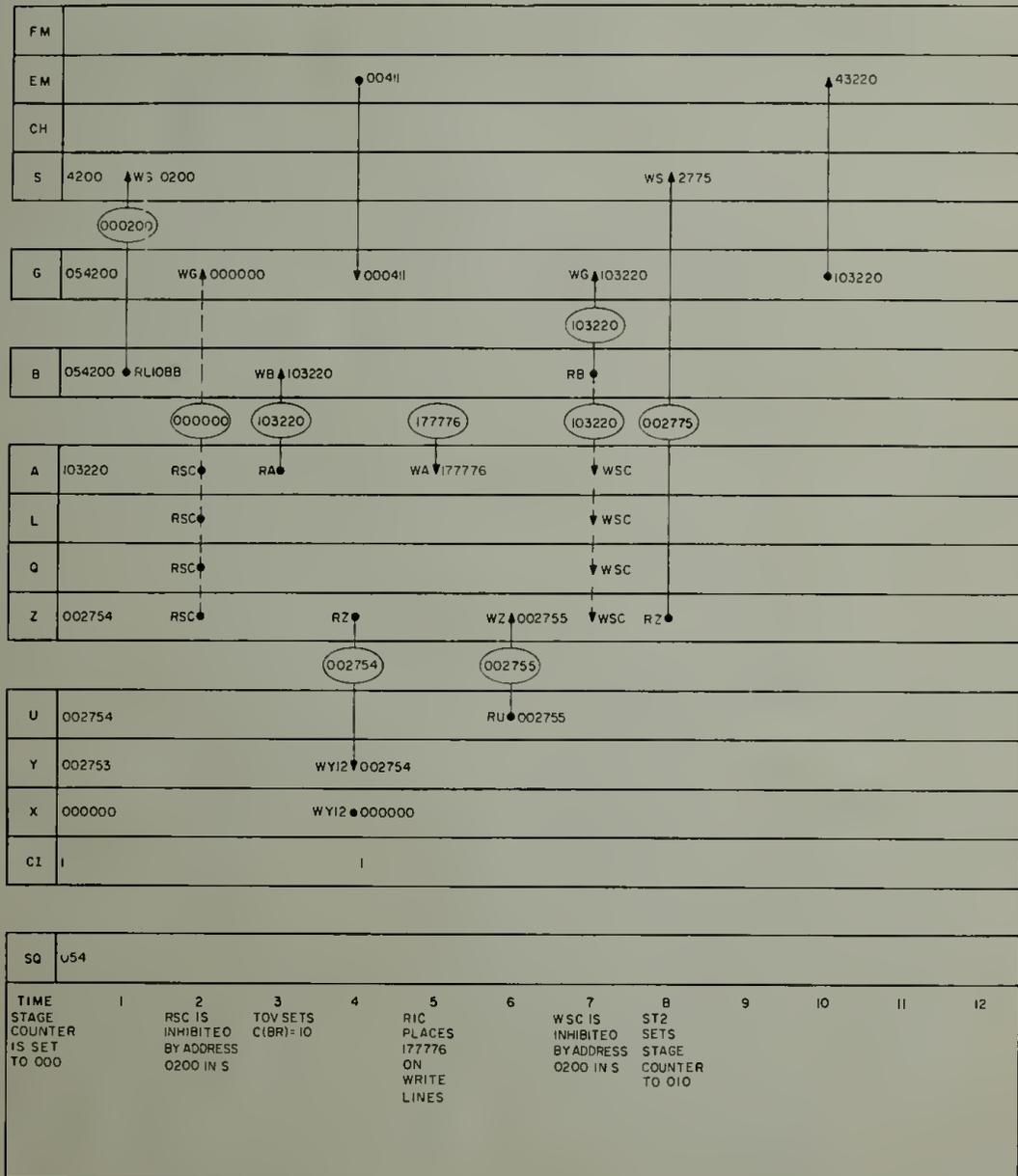
40731

Figure 4-50. Subinstruction TS0, without Overflow or Underflow, Data Transfer Diagram



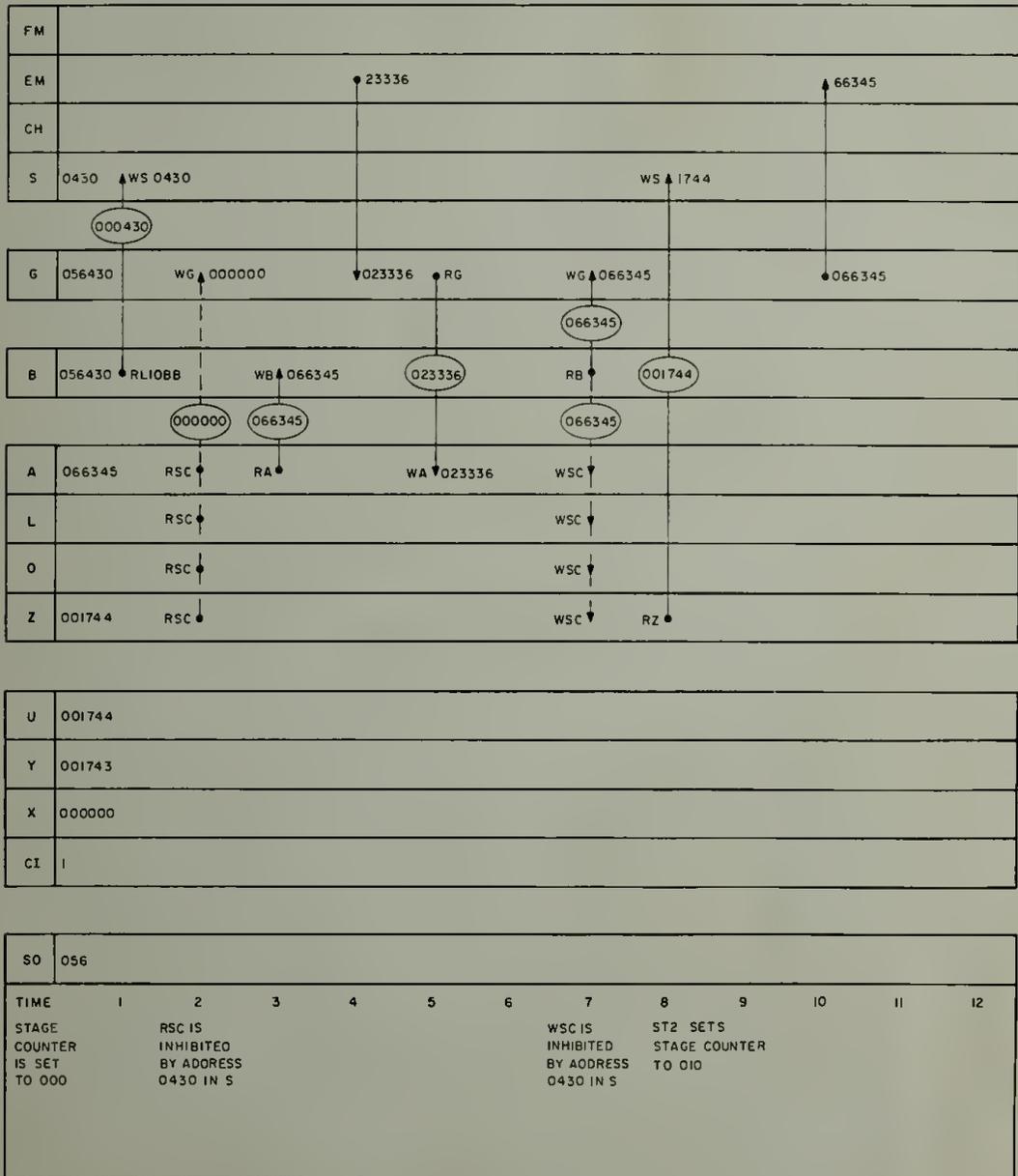
40732

Figure 4-51. Subinstruction TS0, with Overflow, Data Transfer Diagram



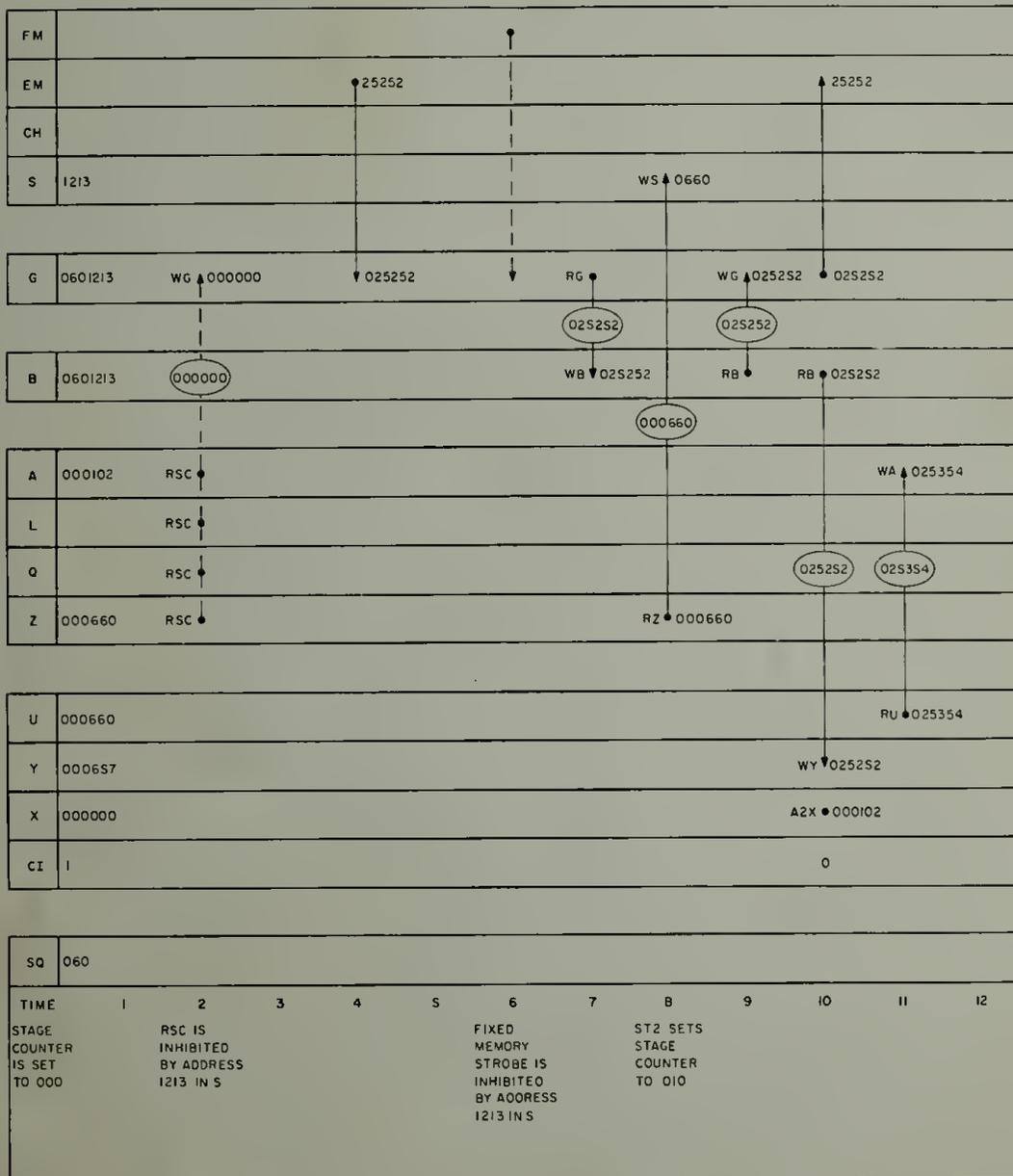
40733

Figure 4-52. Subinstruction TS0, with Underflow, Data Transfer Diagram



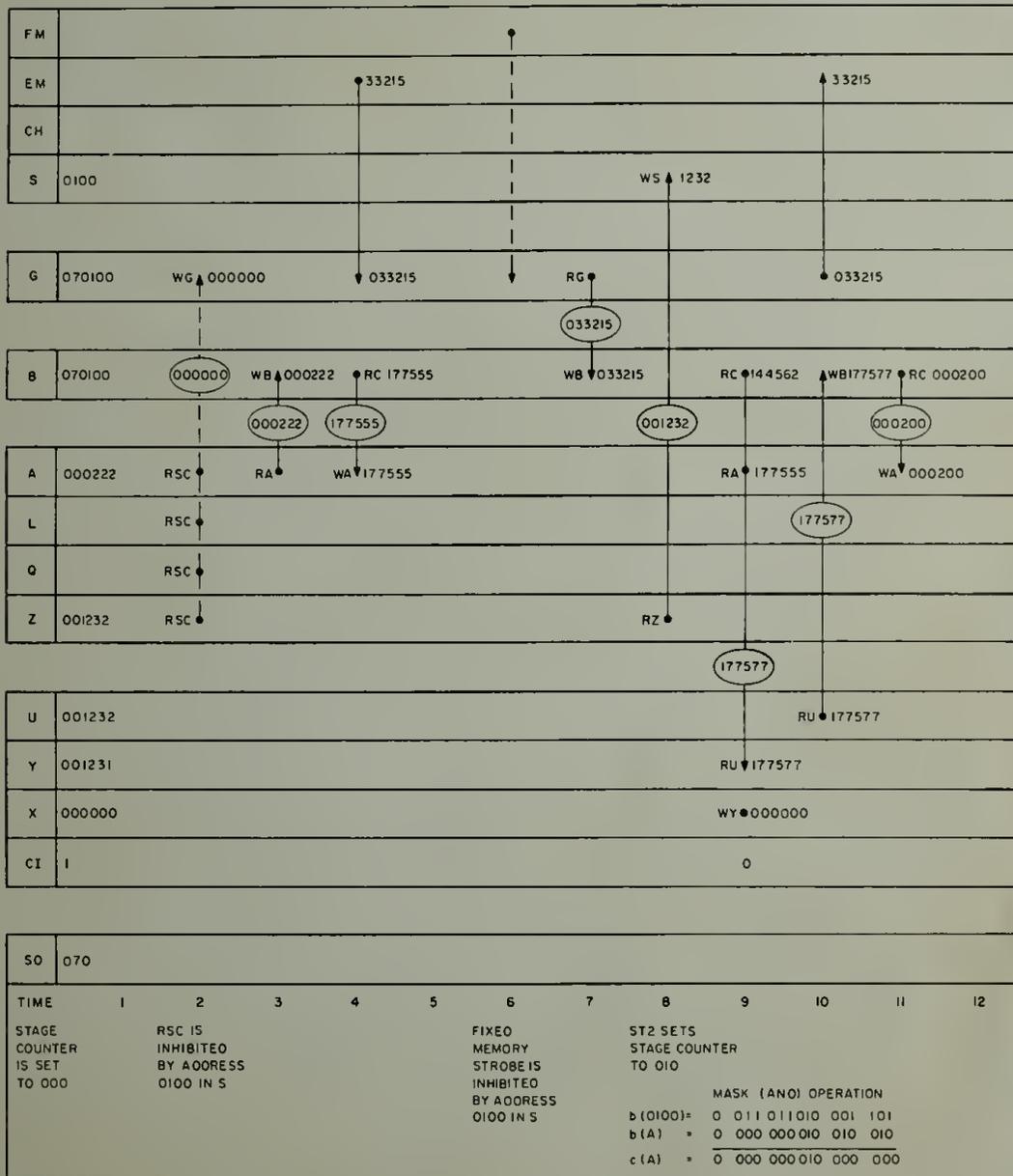
40734

Figure 4-53. Subinstruction XCH0, Data Transfer Diagram



40735

Figure 4-54. Subinstruction AD0, Data Transfer Diagram



4073c

Figure 4-55. Subinstruction MSK0, Data Transfer Diagram

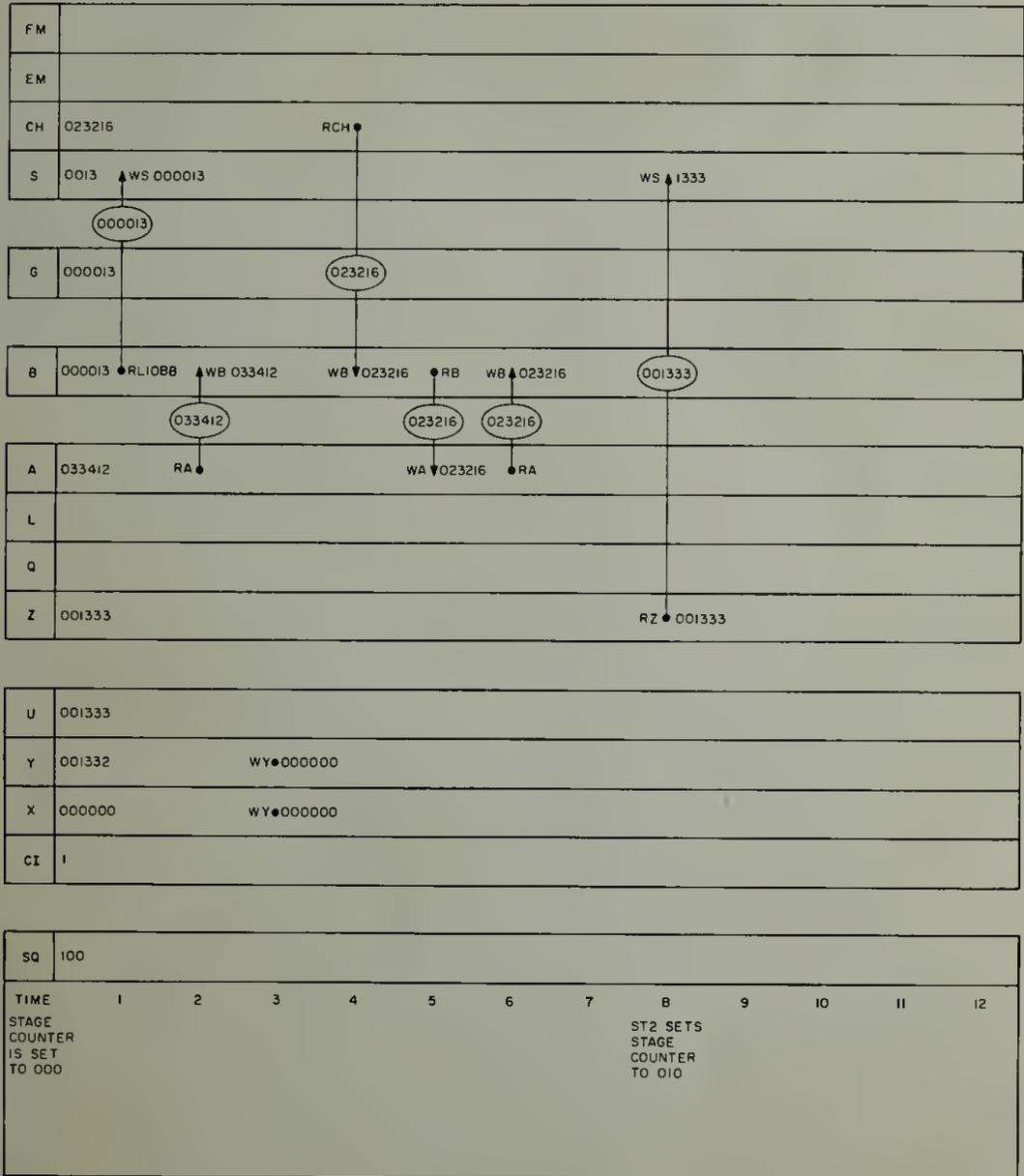


Figure 4-56. Subinstruction READ0, Data Transfer Diagram

40737

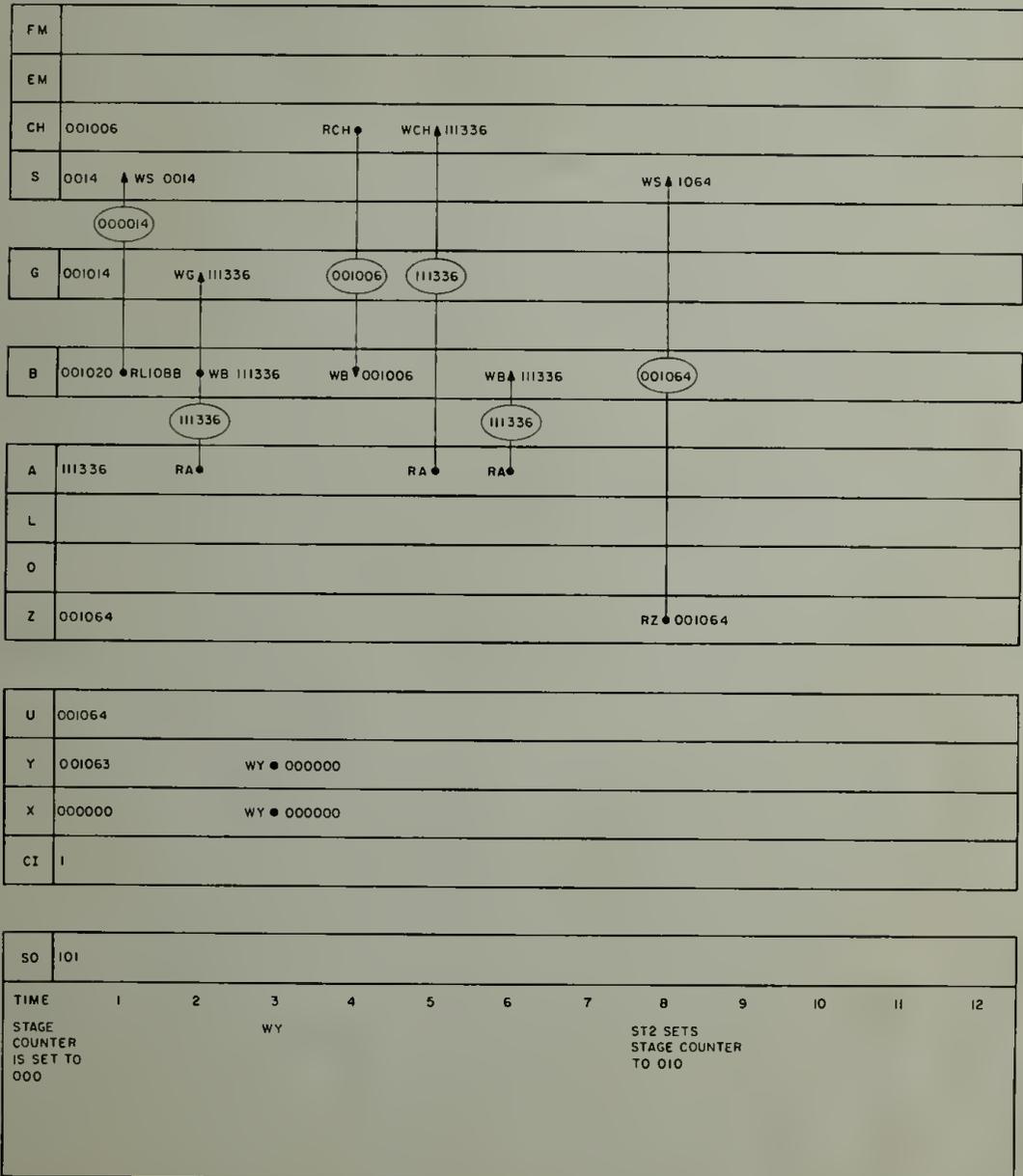


Figure 4-57. Subinstruction WRITE0, Data Transfer Diagram

40738

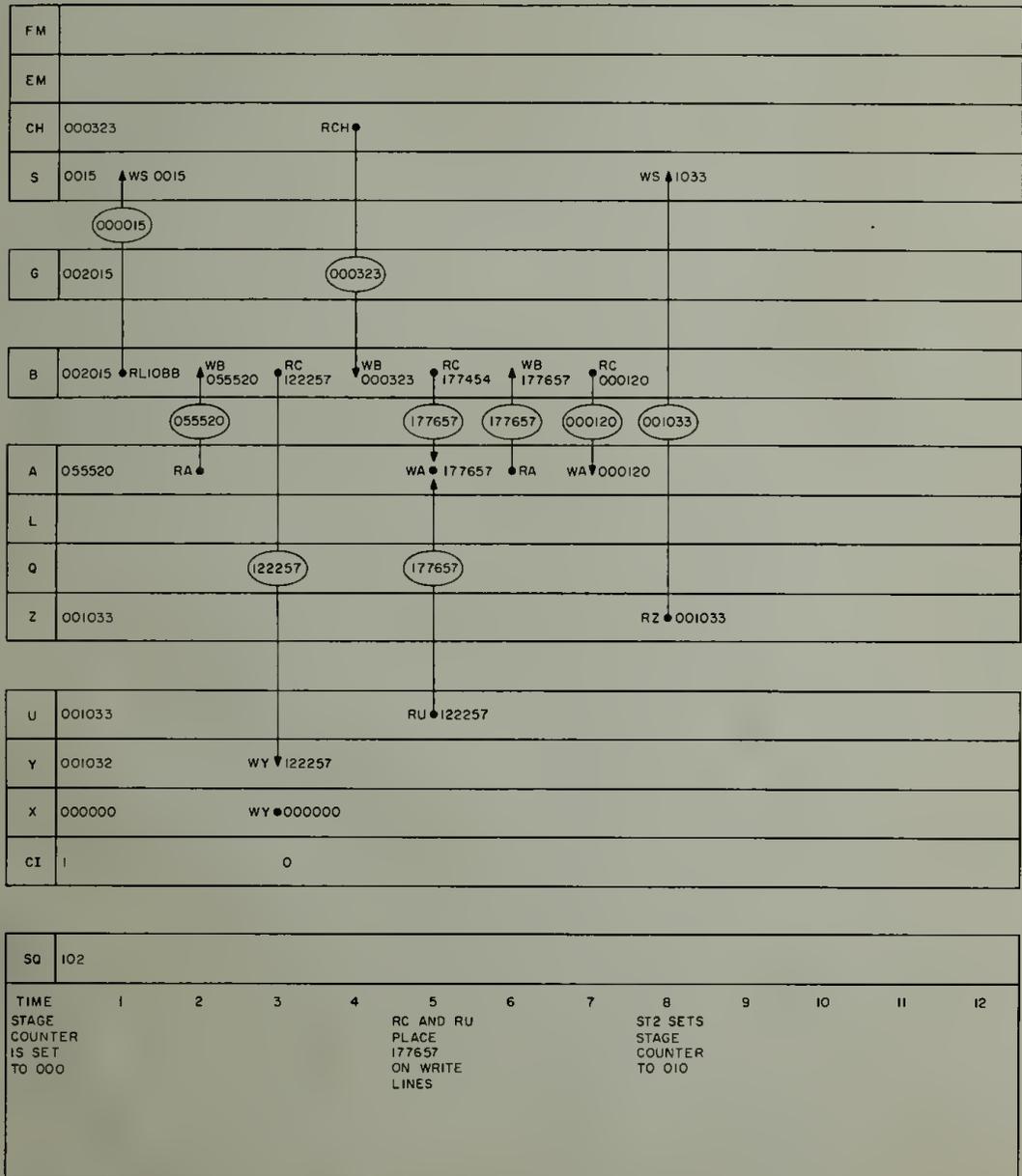


Figure 4-58. Subinstruction RAND0, Data Transfer Diagram

40739

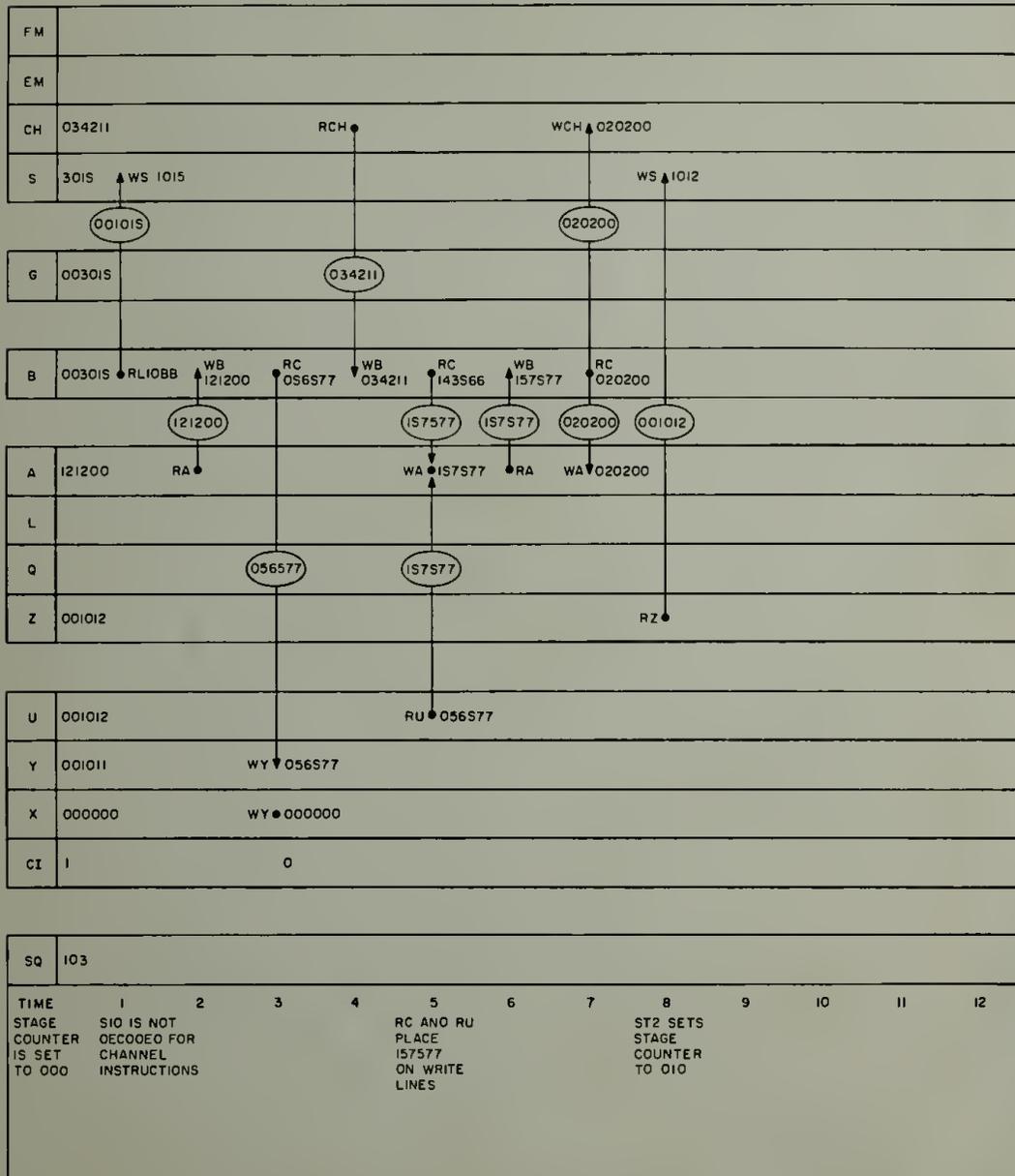


Figure 4-59. Subinstruction WAND0, Data Transfer Diagram

40740

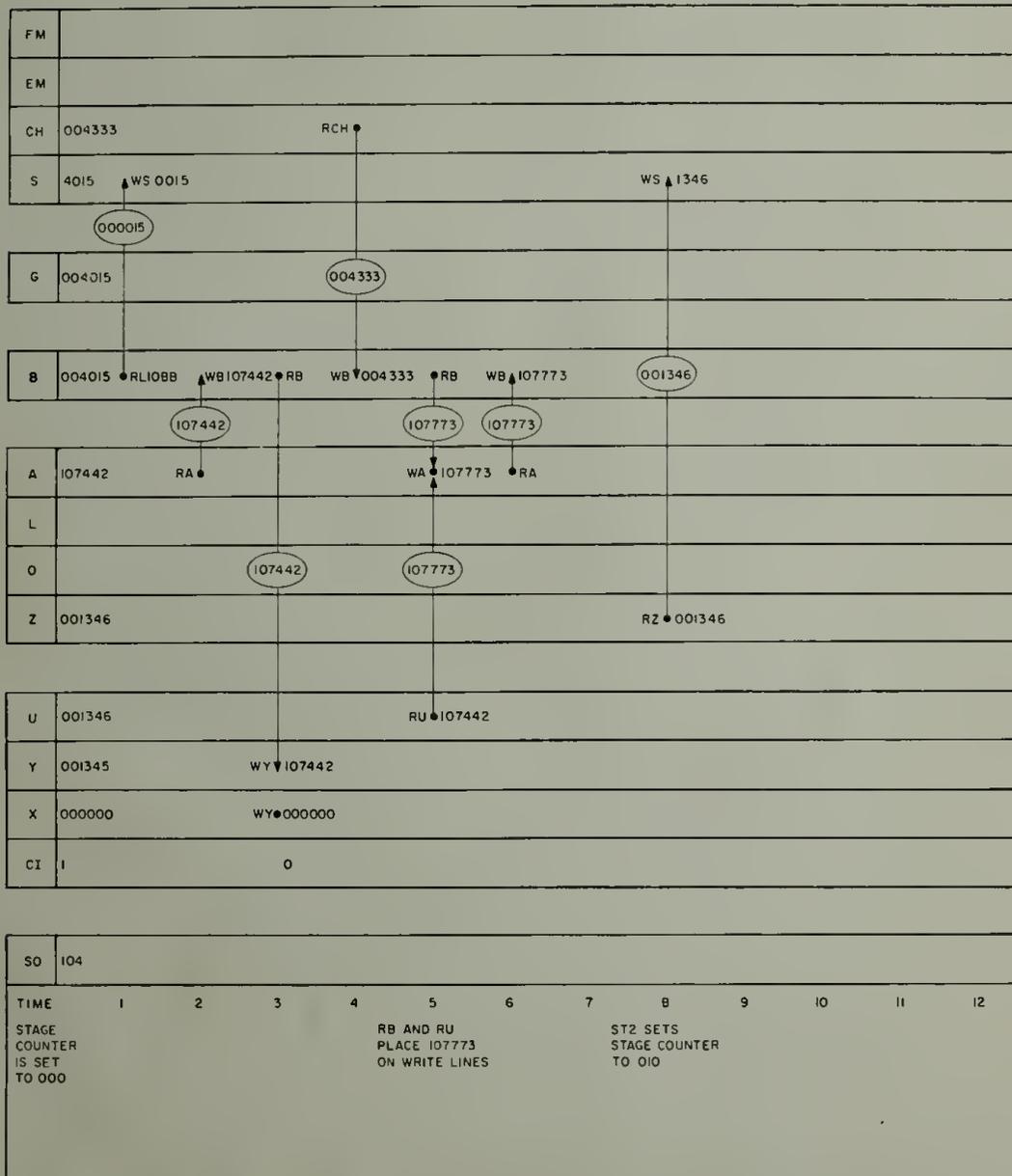


Figure 4-60. Subinstruction ROR0, Data Transfer Diagram

40741

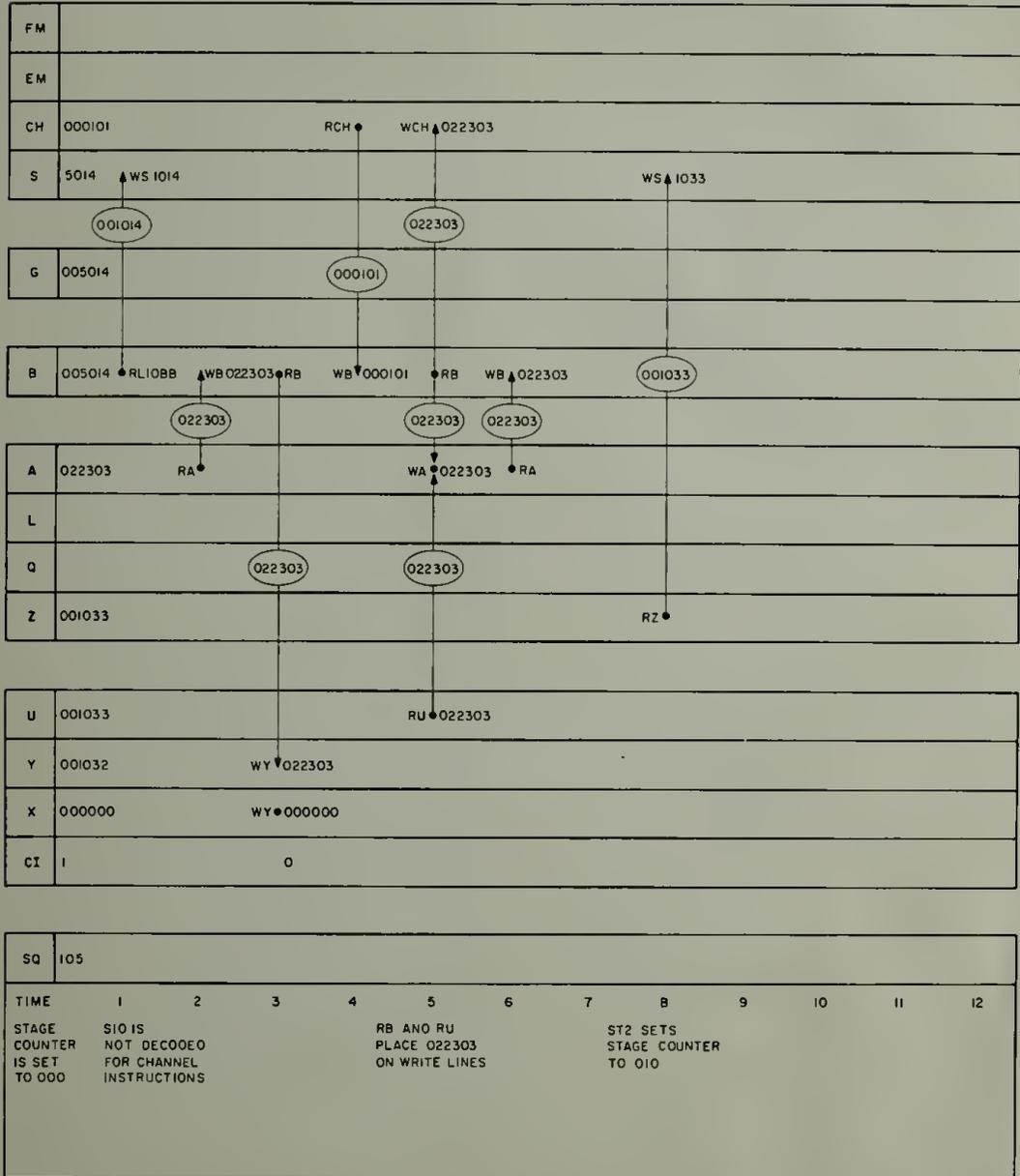
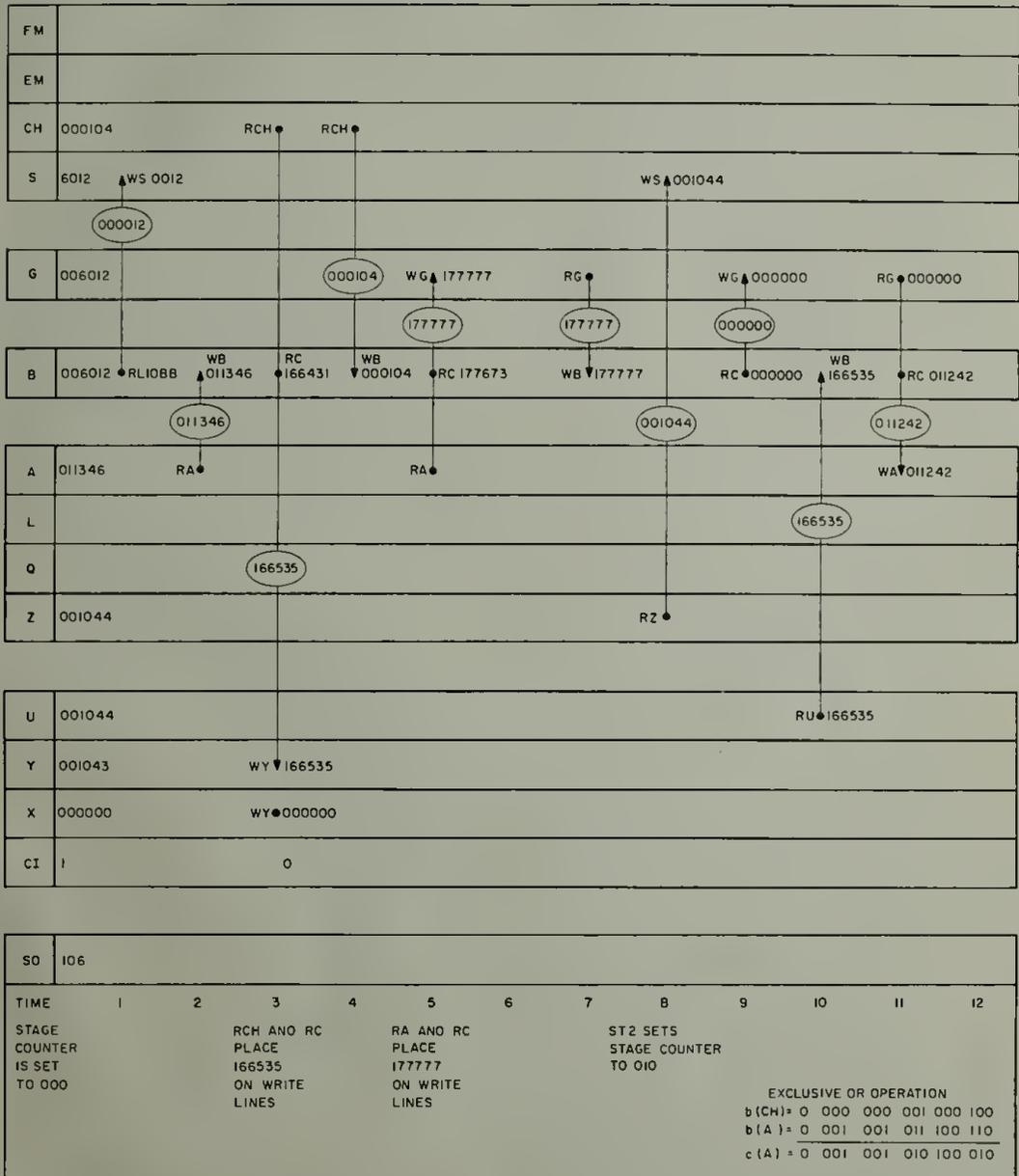


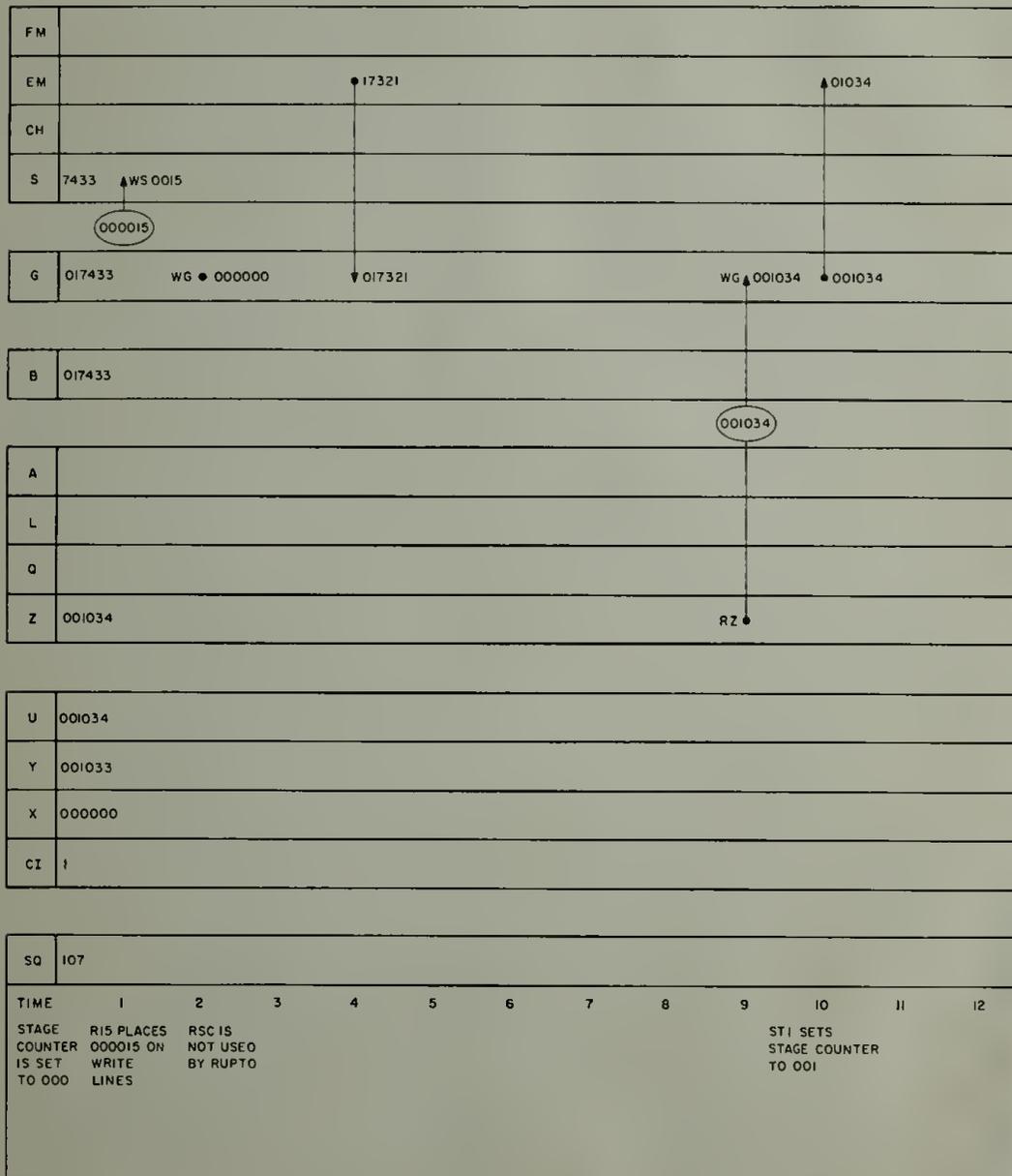
Figure 4-61. Subinstruction WOR0, Data Transfer Diagram

40742



40743

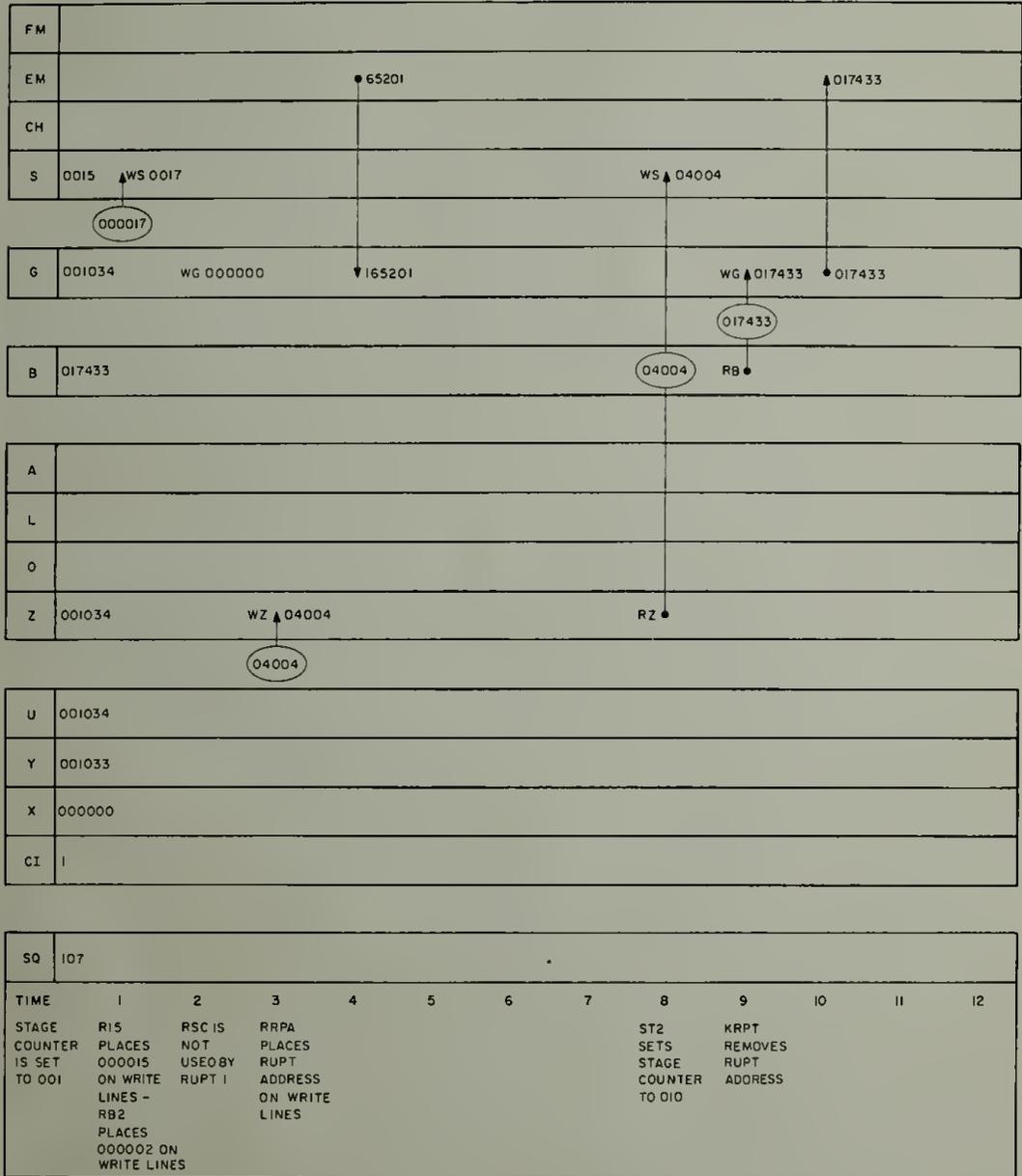
Figure 4-62. Subinstruction RXOR0, Data Transfer Diagram



40744

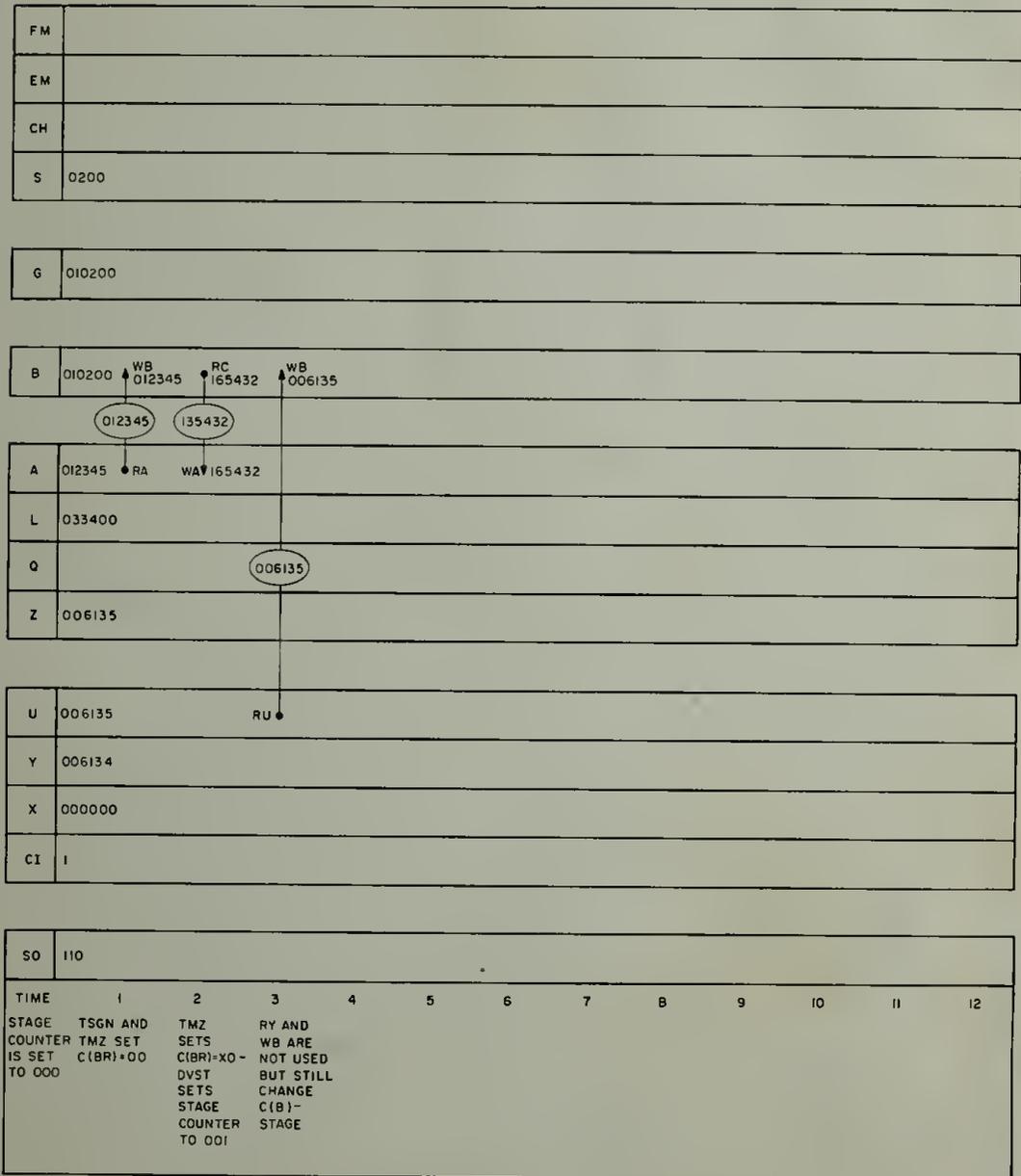
Figure 4-63. Subinstruction RUPT0, Data Transfer Diagram

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40745

Figure 4-64. Subinstruction RUPT1, Data Transfer Diagram



40746

Figure 4-65. Subinstruction DV0, Data Transfer Diagram

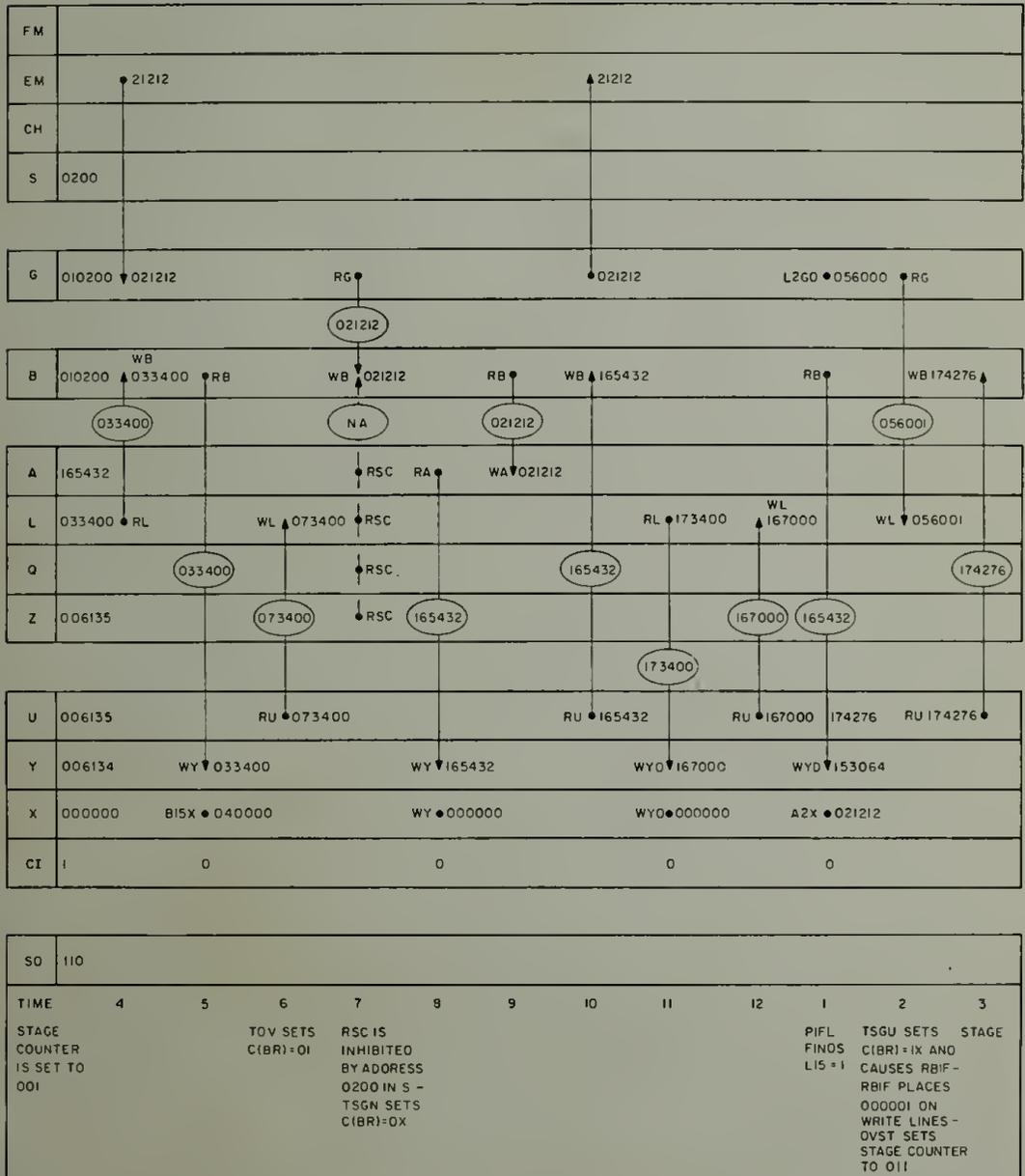
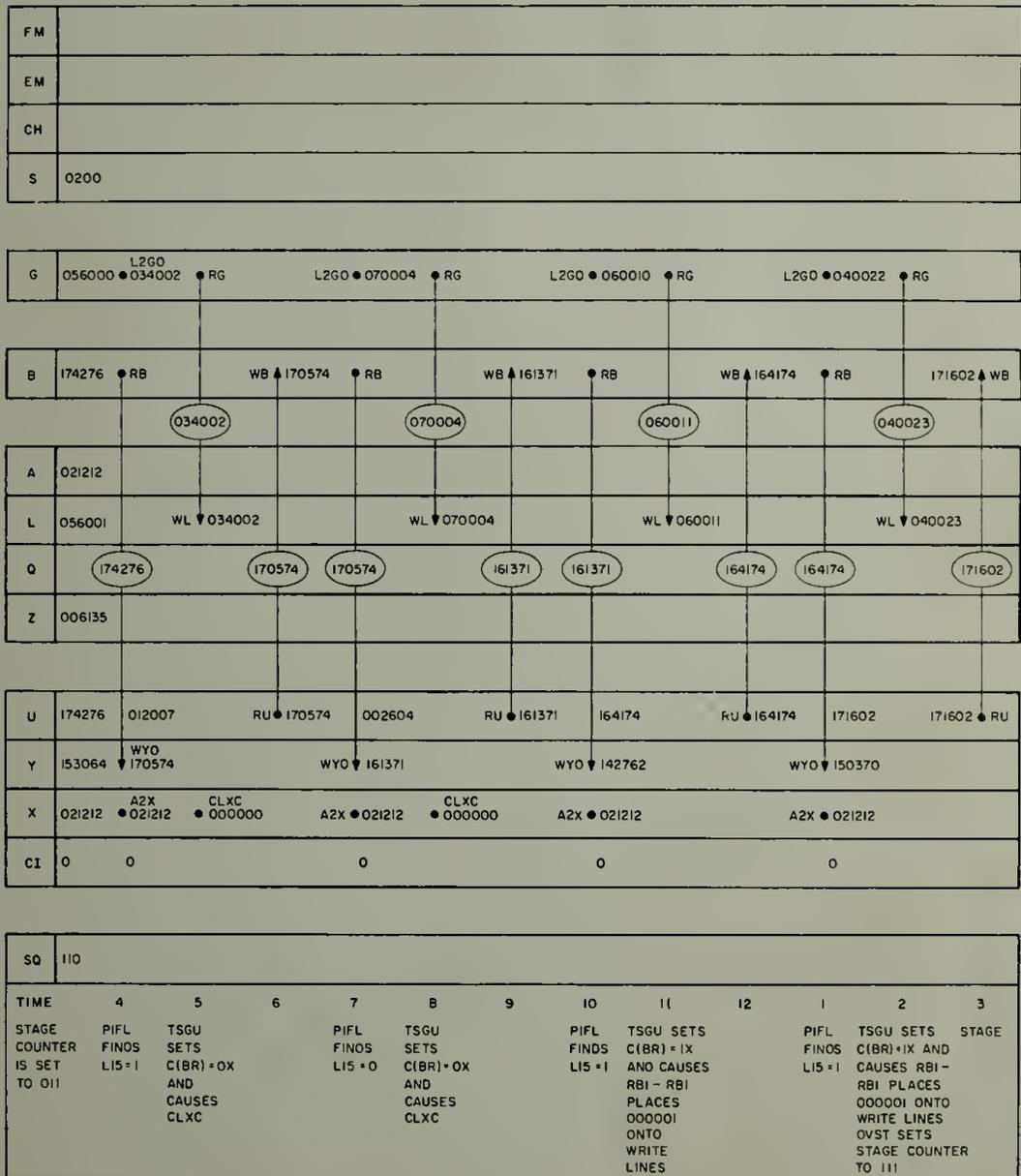


Figure 4-66. Subinstruction DV1, Data Transfer Diagram

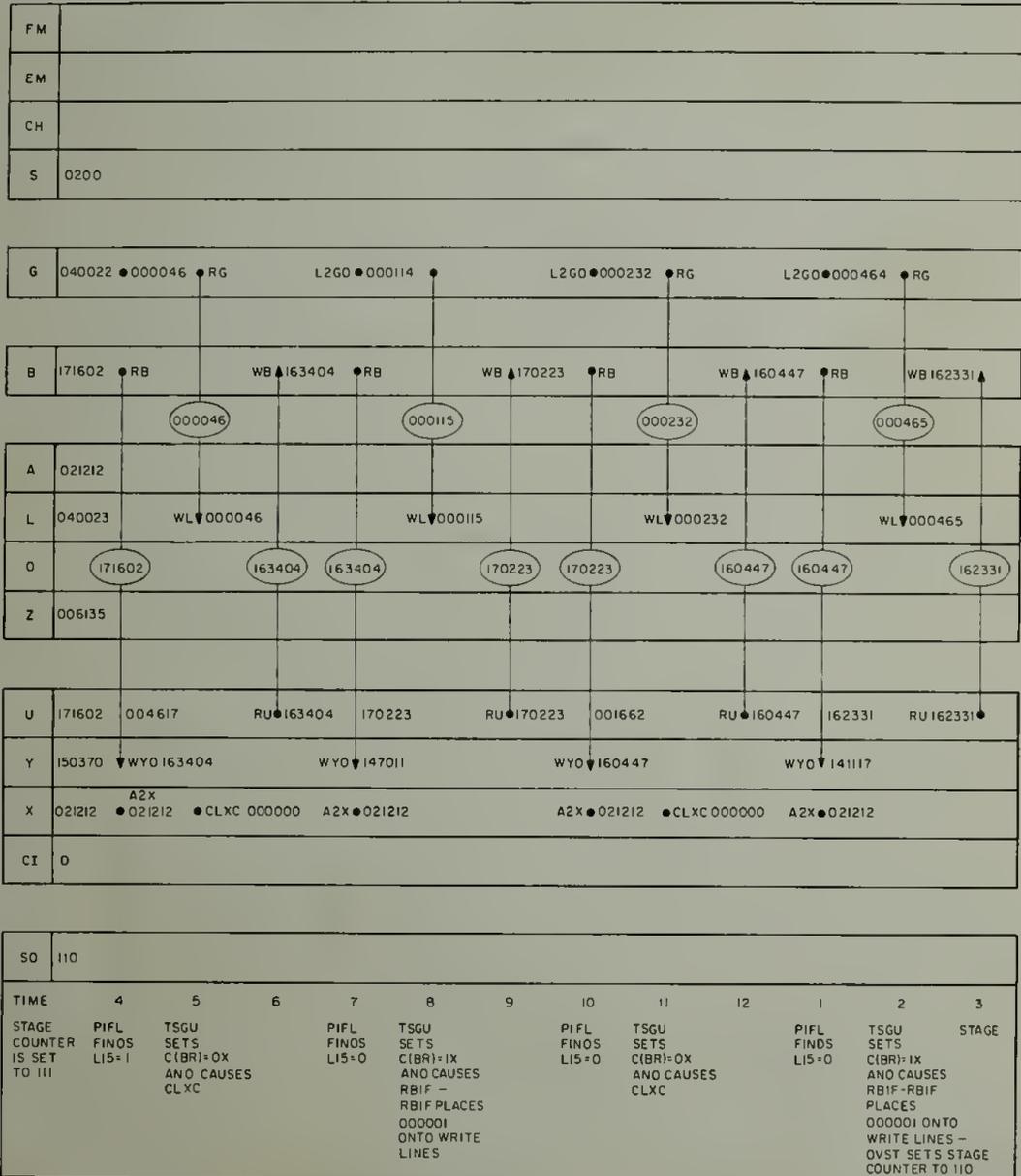
40747



40748

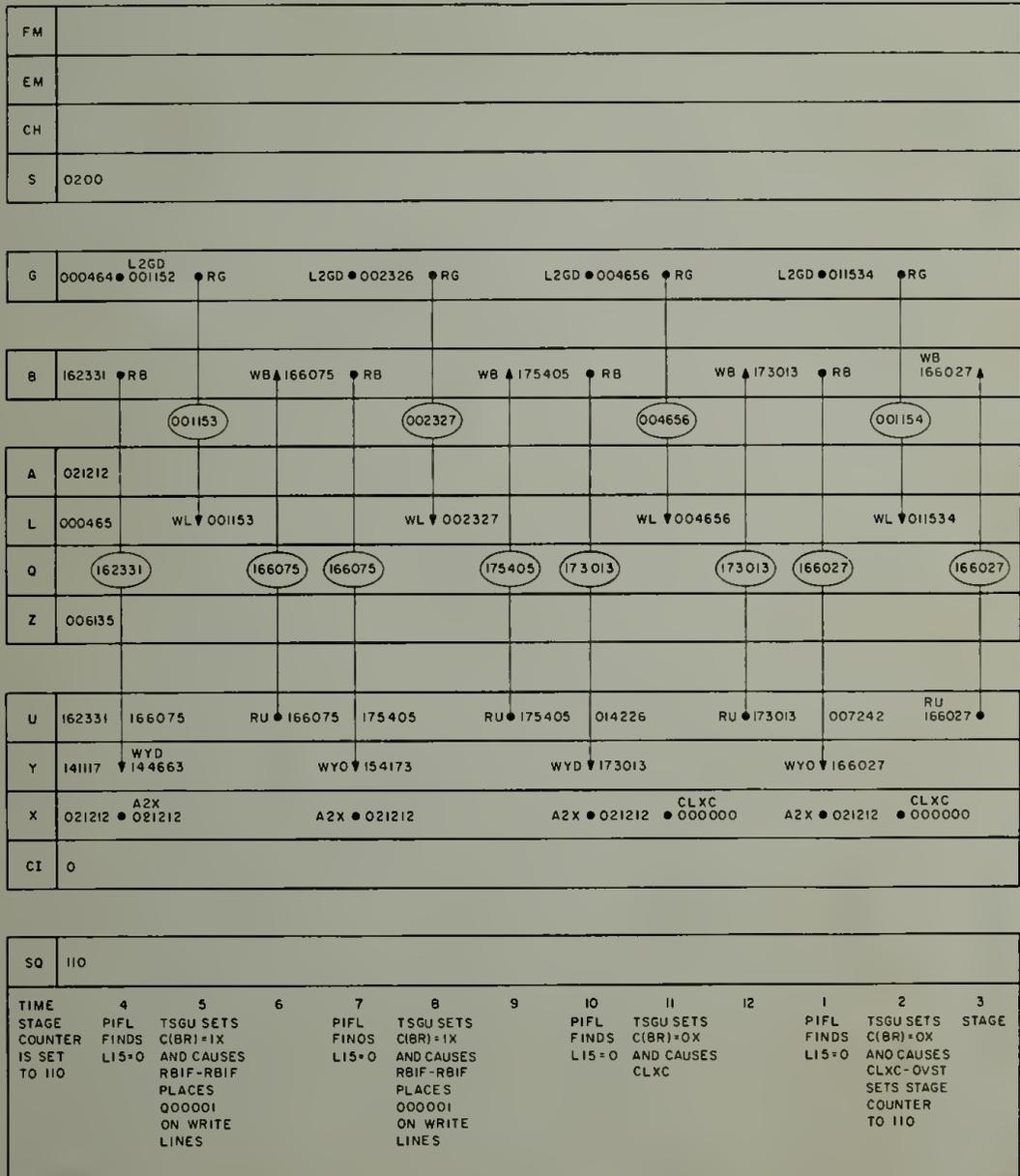
Figure 4-67. Subinstruction DV3, Data Transfer Diagram

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40749

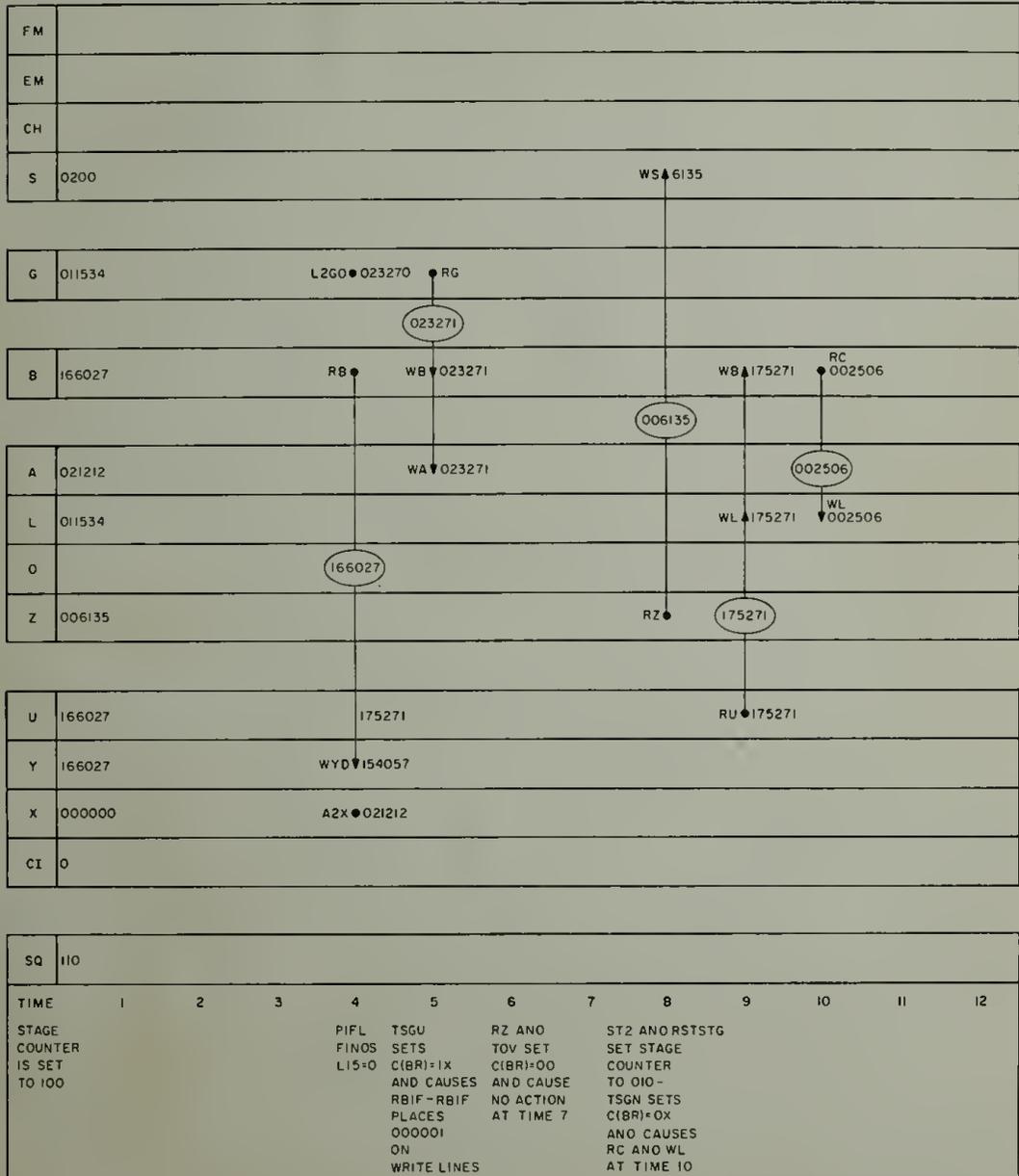
Figure 4-68. Subinstruction DV7, Data Transfer Diagram



40750

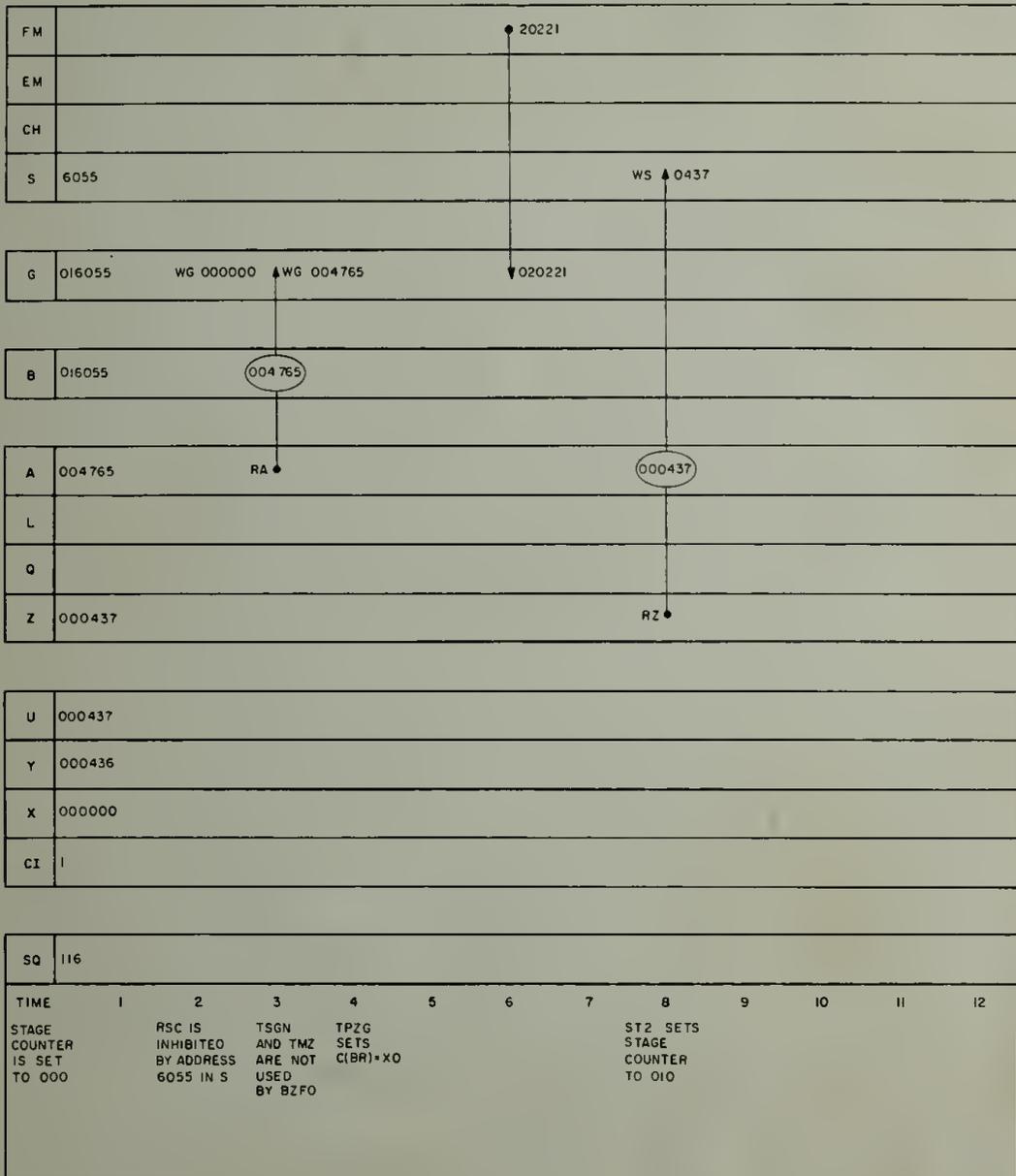
Figure 4-69. Subinstruction DV6, Data Transfer Diagram

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40751

Figure 4-70. Subinstruction DV4, Data Transfer Diagram



40752

Figure 4-71. Subinstruction BZF0, with Branch on Non-Zero Quantity, Data Transfer Diagram

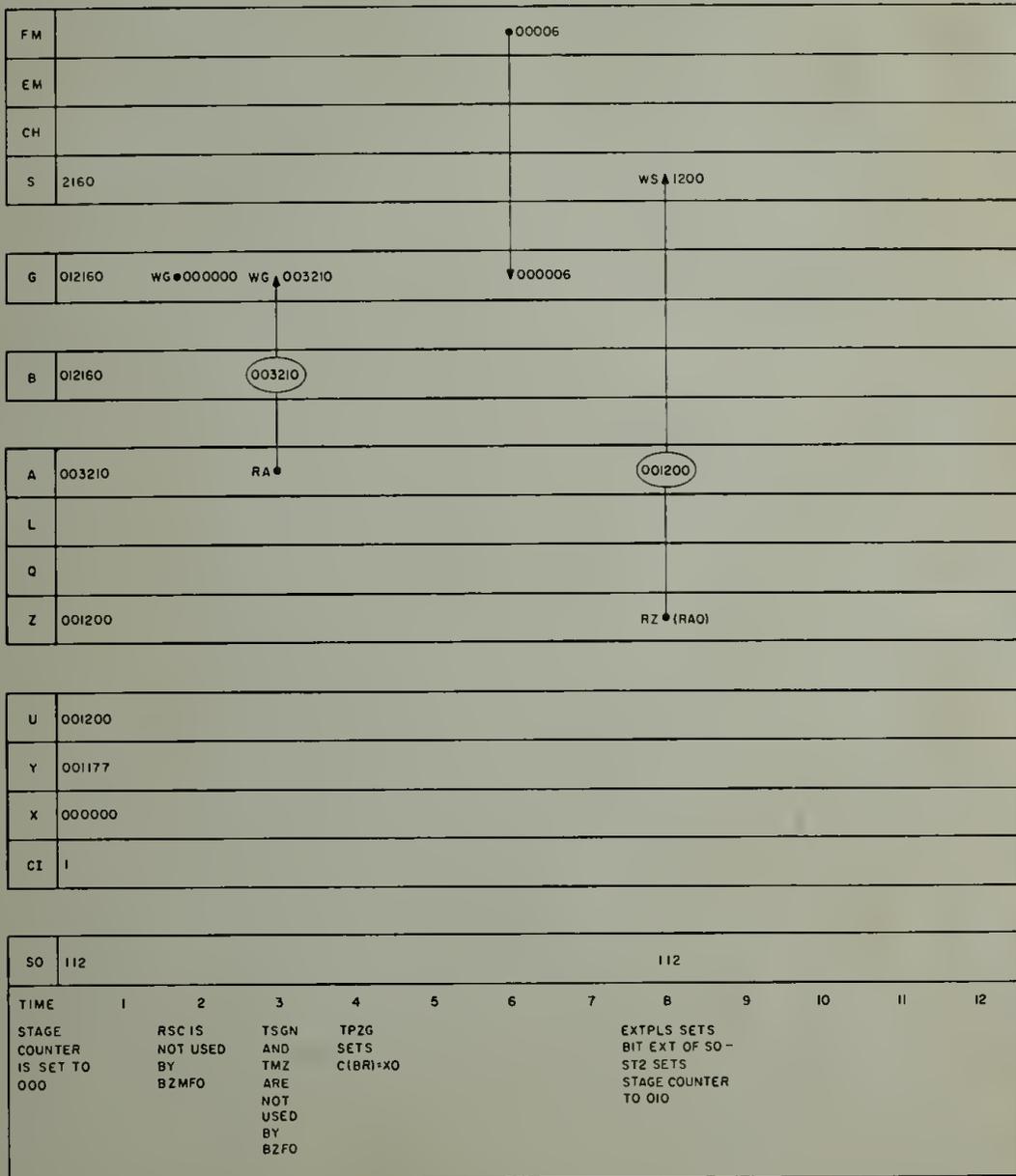
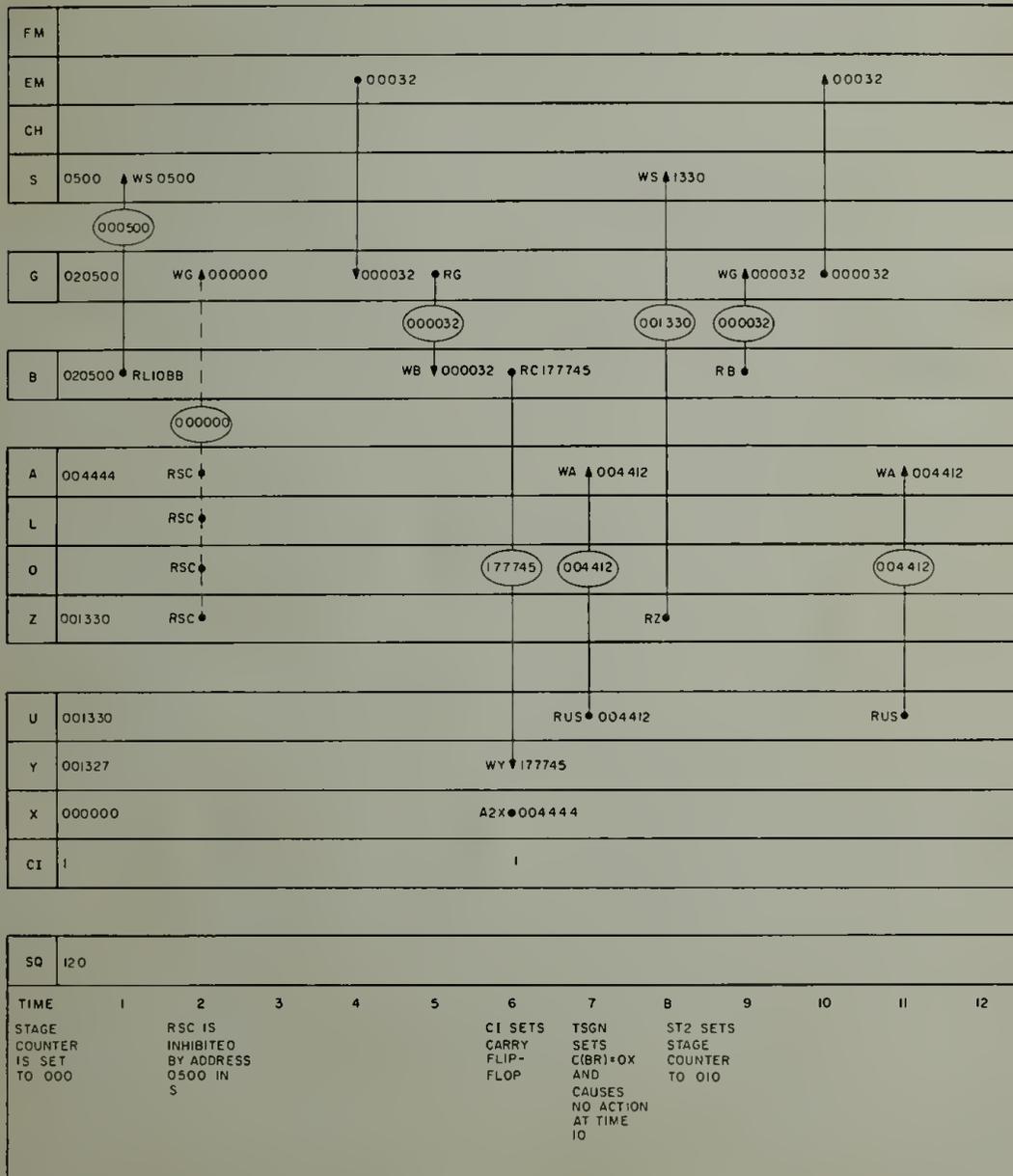


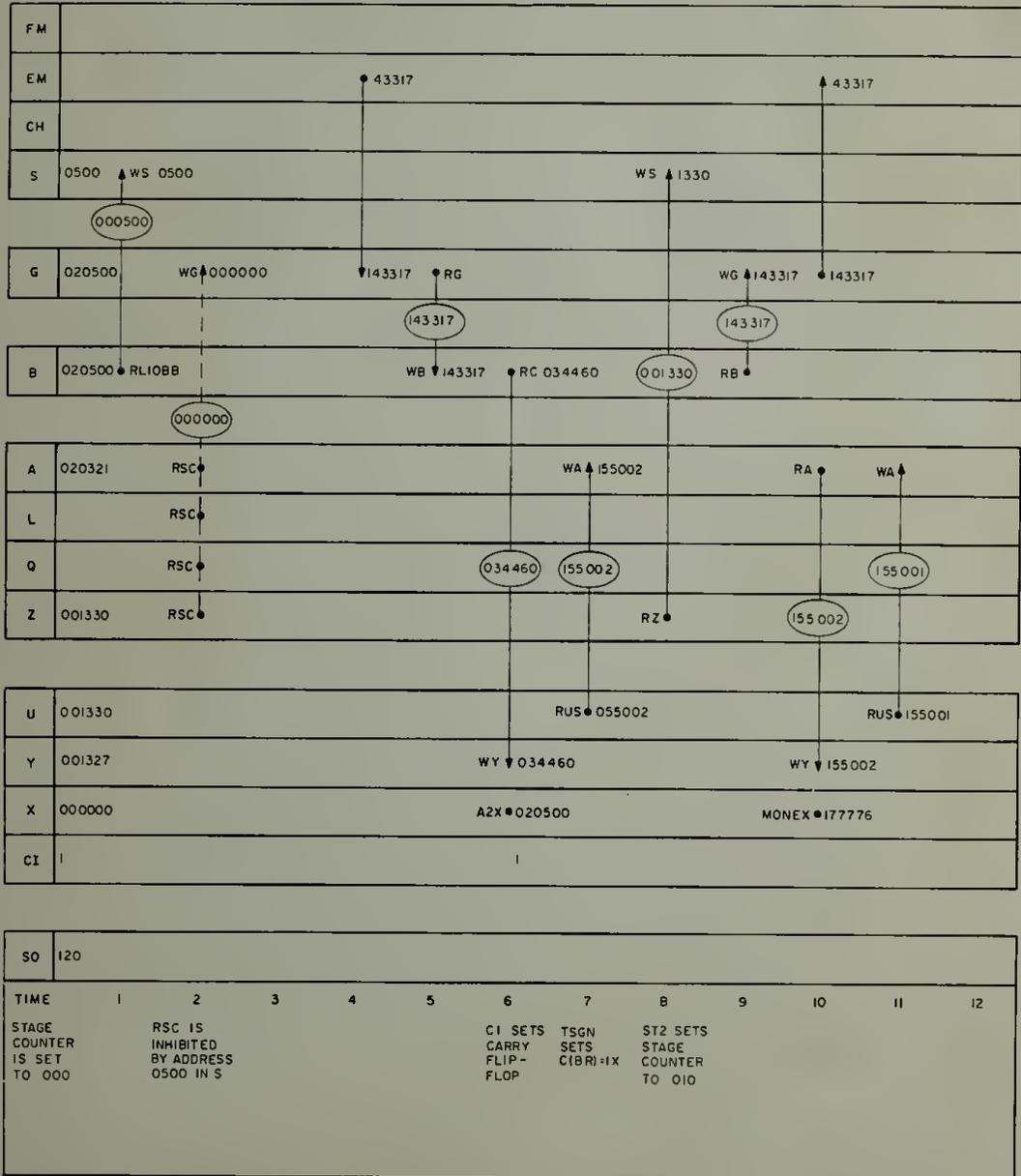
Figure 4-73. Subinstruction BZF0 with Implied Address Code EXTEND, Data Transfer Diagram

40754



40755

Figure 4-74. Subinstruction MSU0 with Positive Resultant, Data Transfer Diagram



40756

Figure 4-75. Subinstruction MSU0 with Negative Resultant, Data Transfer Diagram

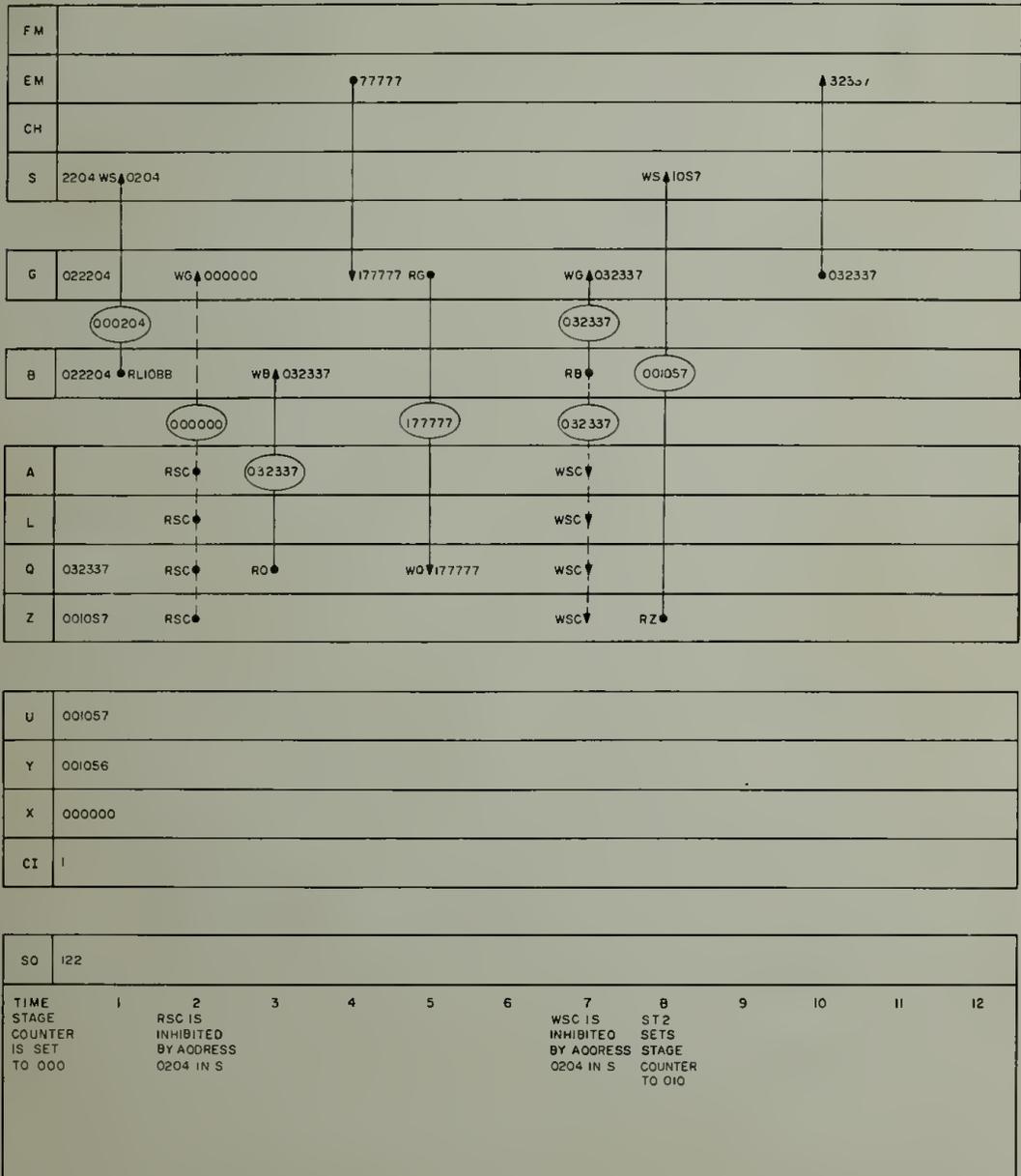
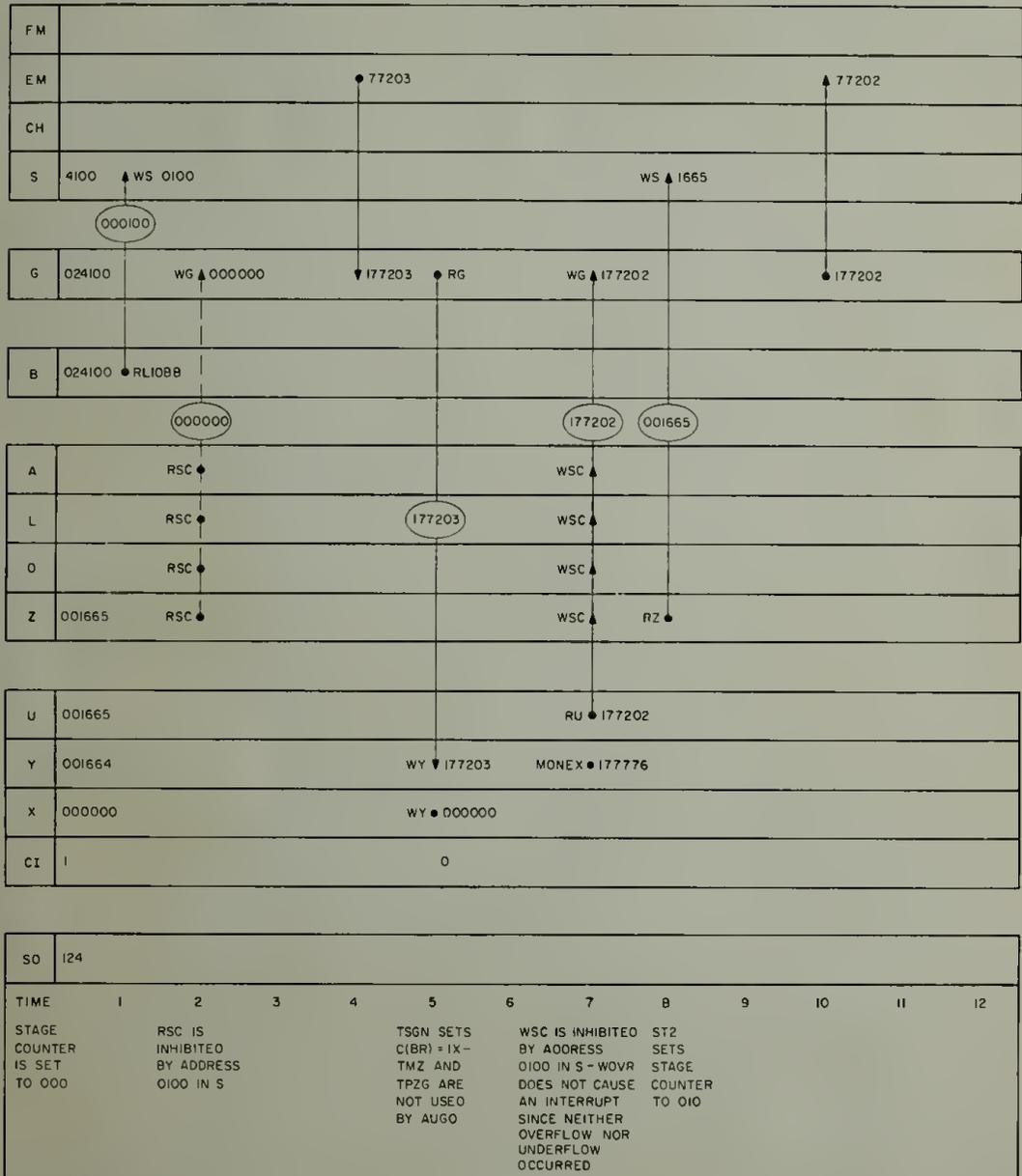


Figure 4-76. Subinstruction QXCH0, Data Transfer Diagram

40757

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Figure 4-78. Subinstruction AUG0 with Negative Quantity, Data Transfer Diagram

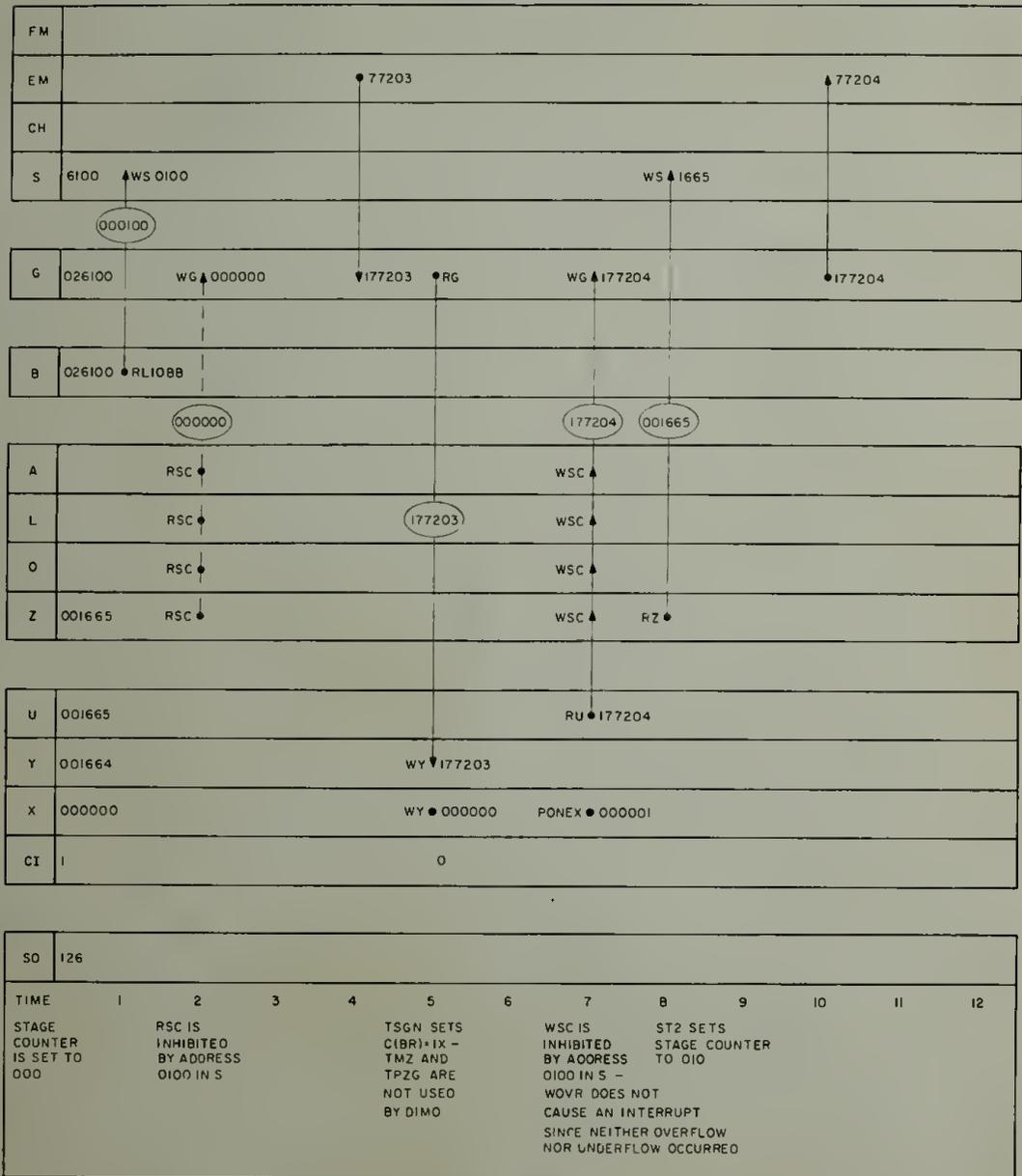


Figure 4-80. Subinstruction DIM0 with Negative Quantity, Data Transfer Diagram

507A1

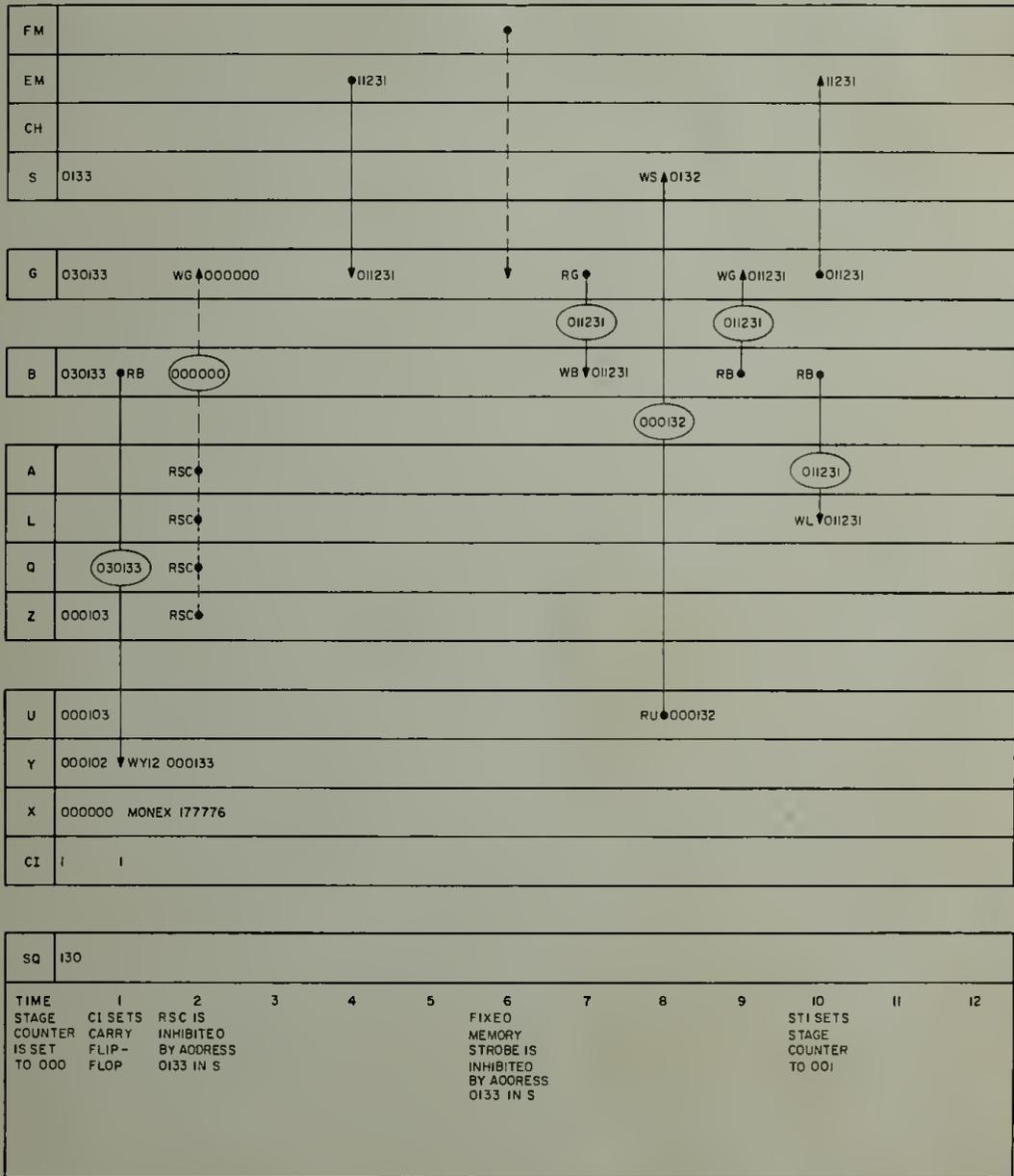


Figure 4-81. Subinstruction DCA0, Data Transfer Diagram

40762

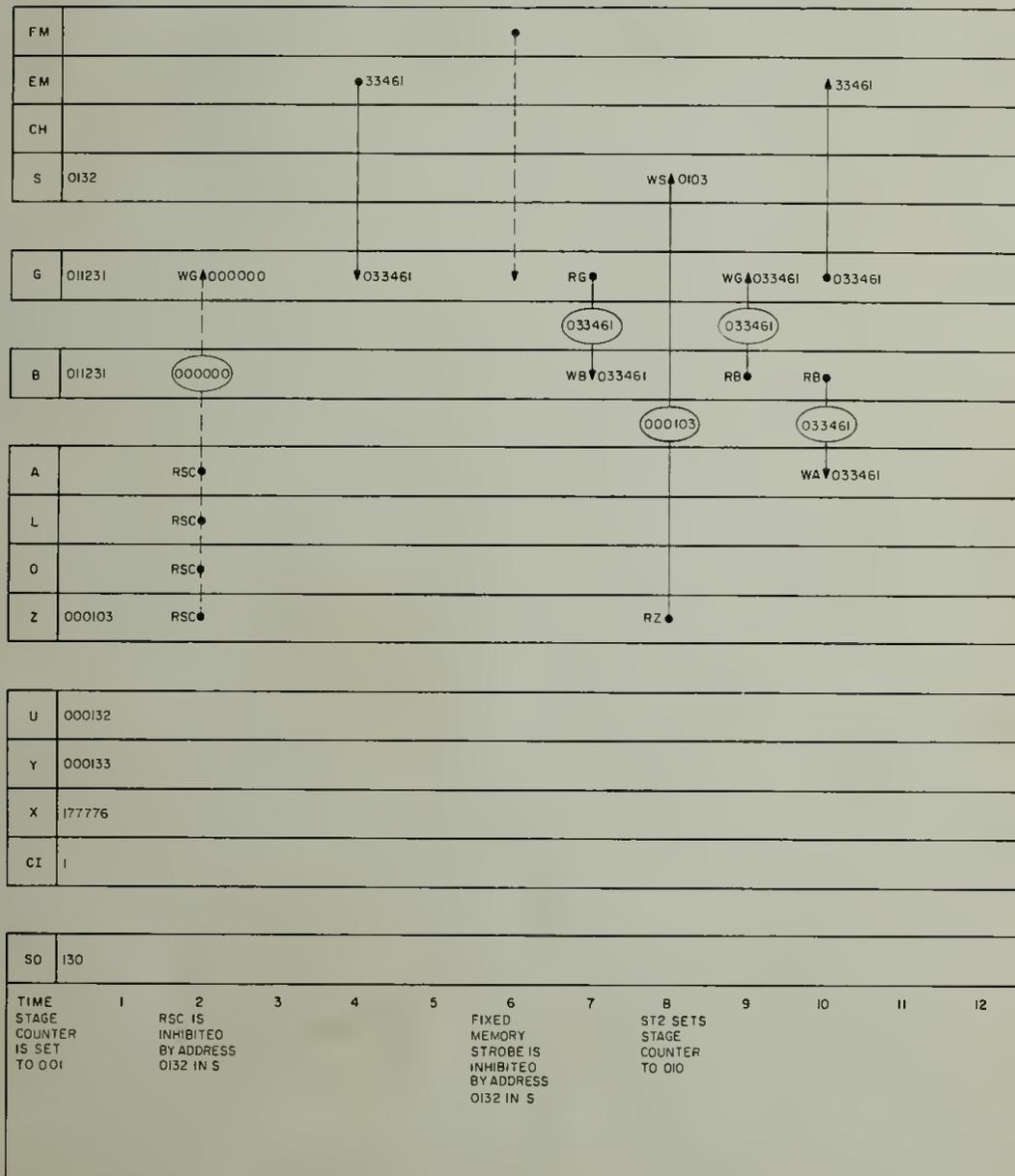


Figure 4-82. Subinstruction DCA1, Data Transfer Diagram

40763

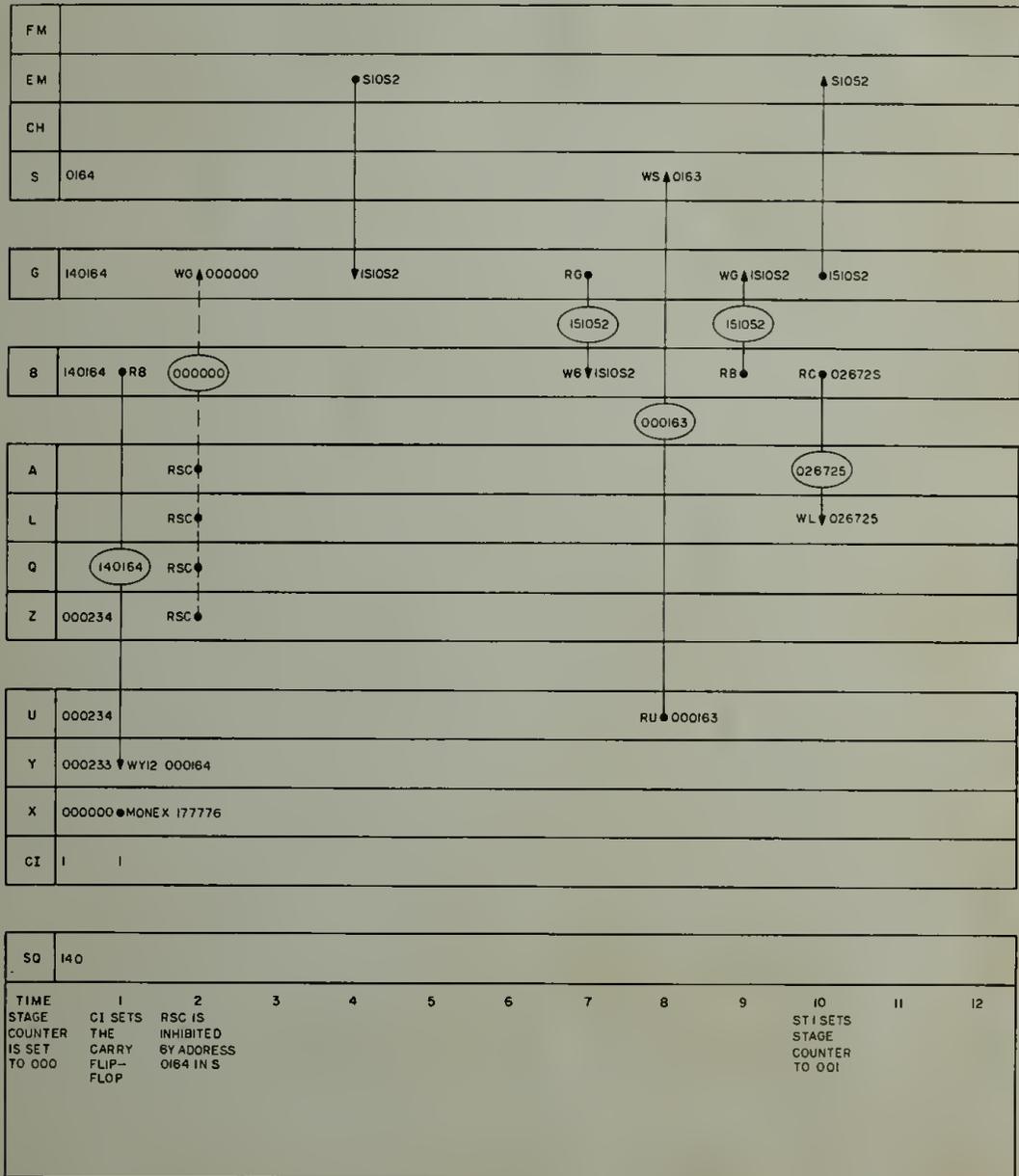


Figure 4-83. Subinstruction DSC0, Data Transfer Diagram

40764

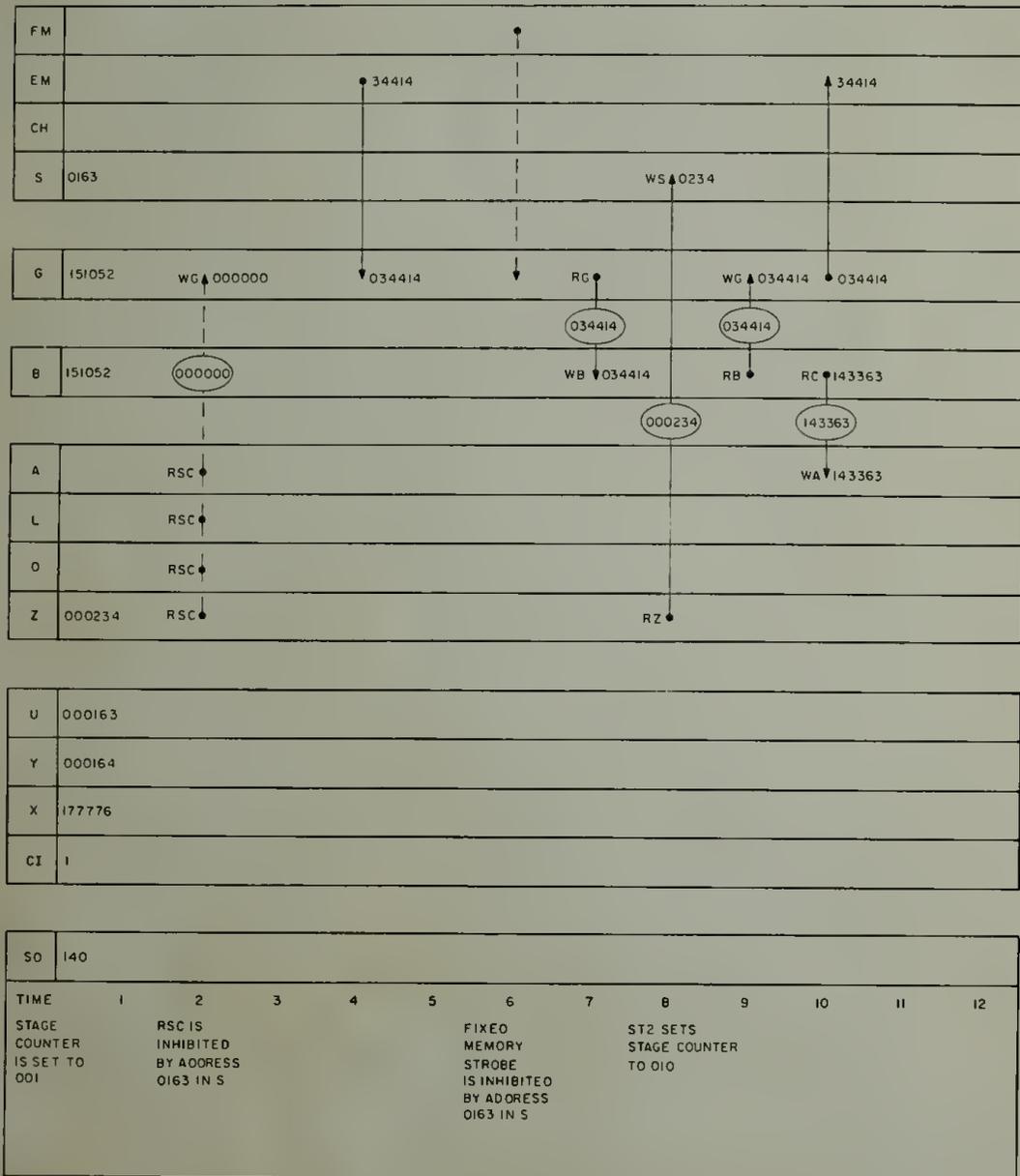
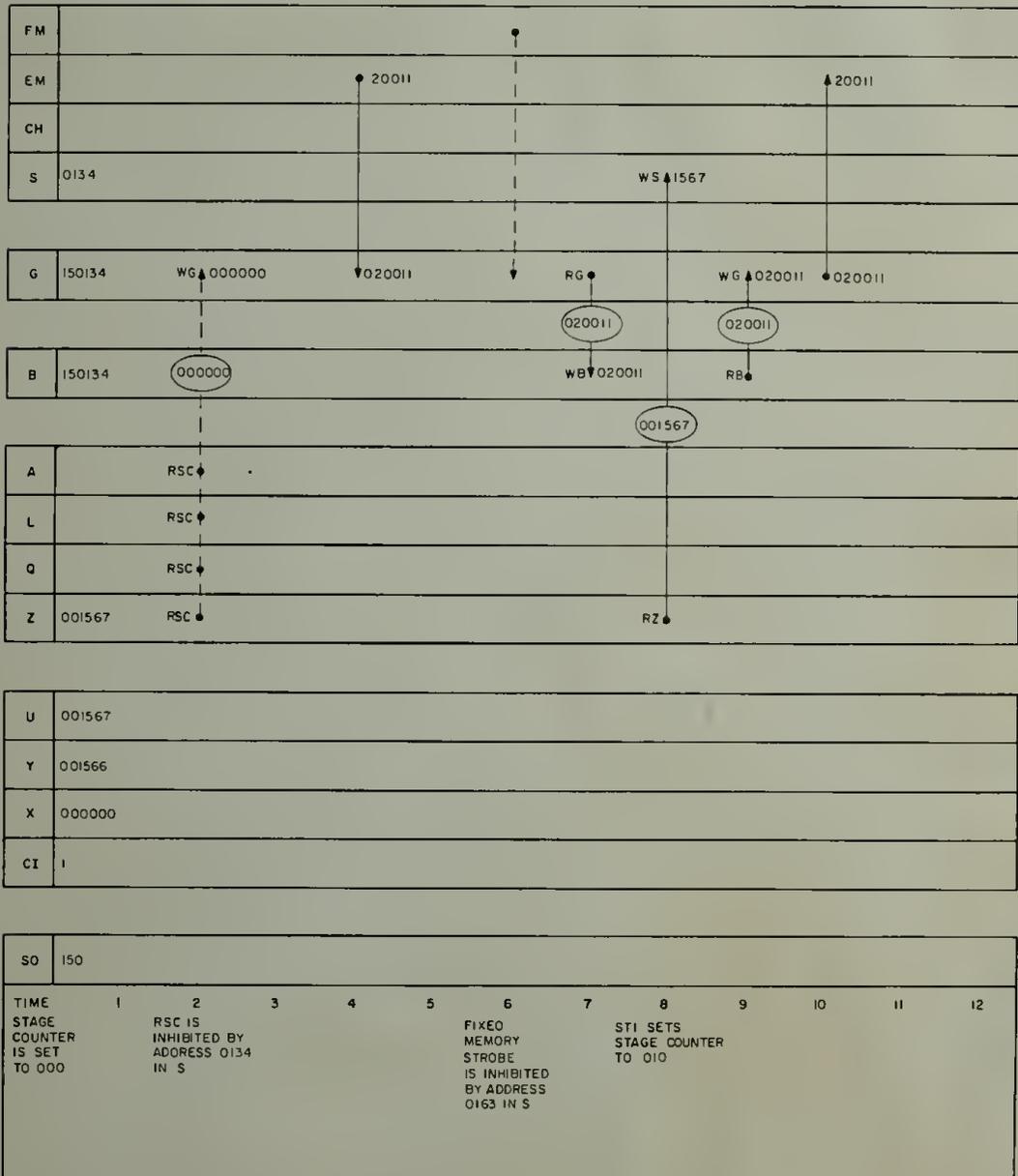


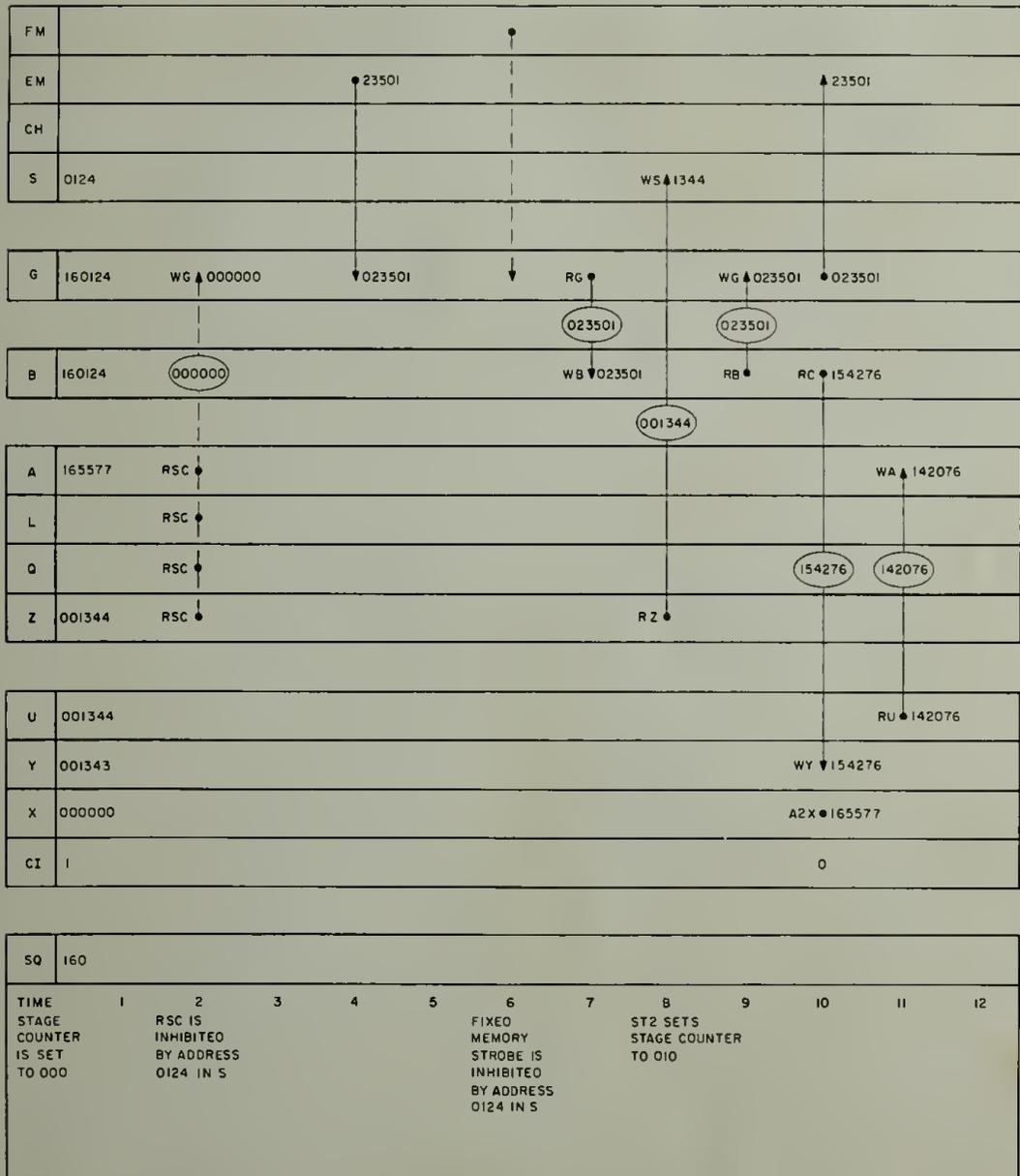
Figure 4-84. Subinstruction DCS1, Data Transfer Diagram

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40766

Figure 4-85. Subinstruction NDXX0, Data Transfer Diagram



40765

Figure 4-87. Subinstruction SU0, Data Transfer Diagram

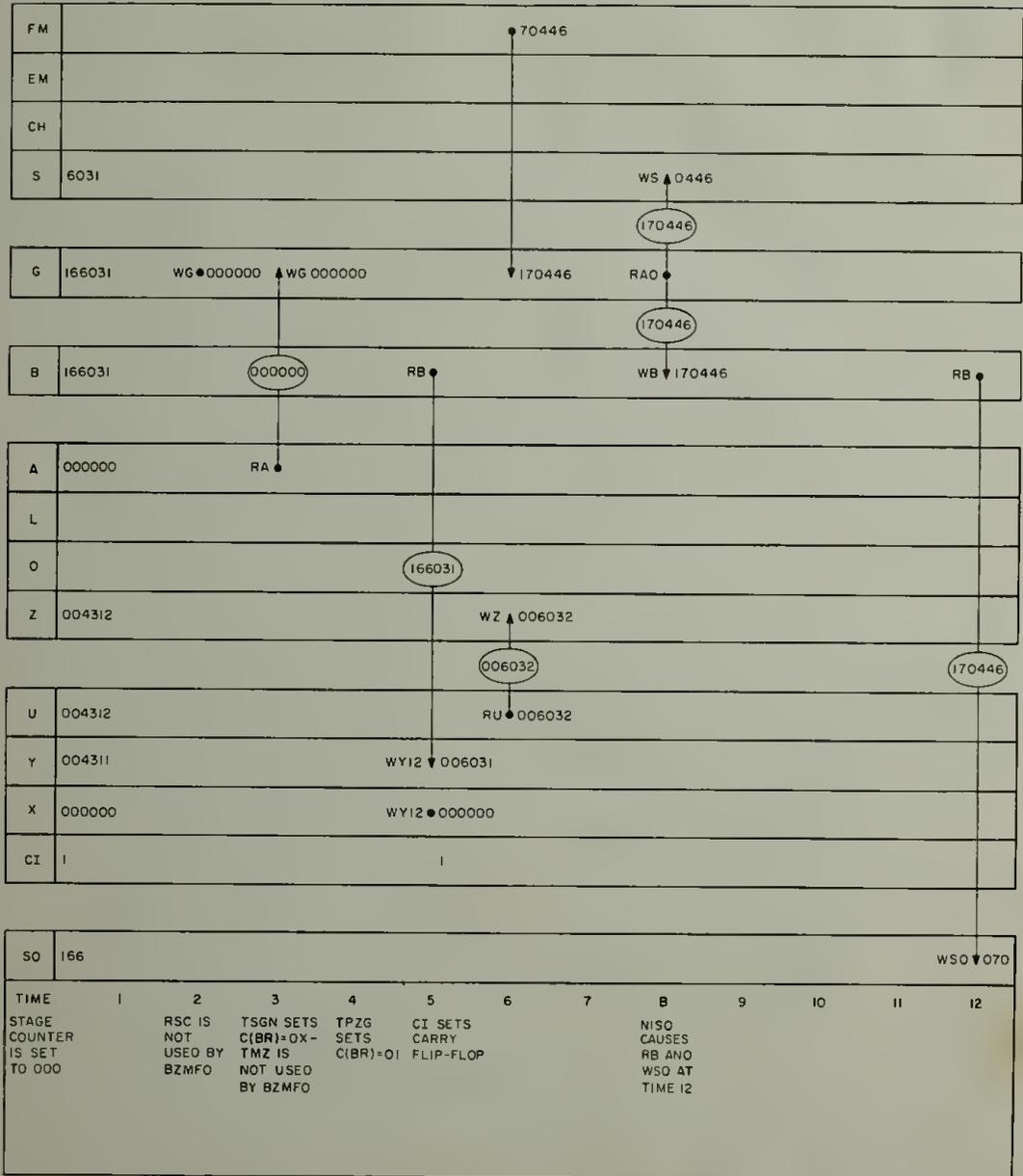


Figure 4-89. Subinstruction BZMF0 with Plus Zero, Data Transfer Diagram

40770

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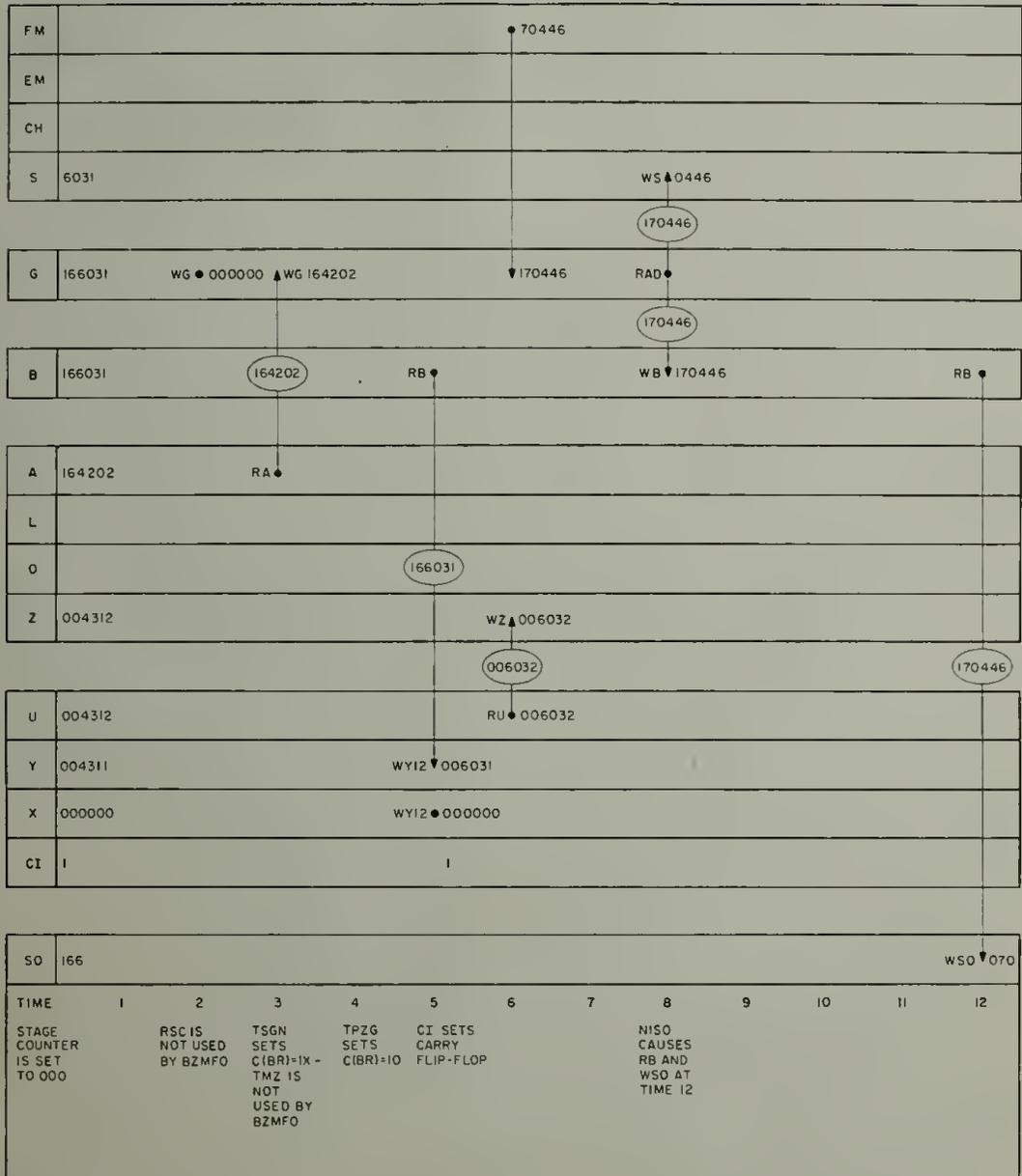
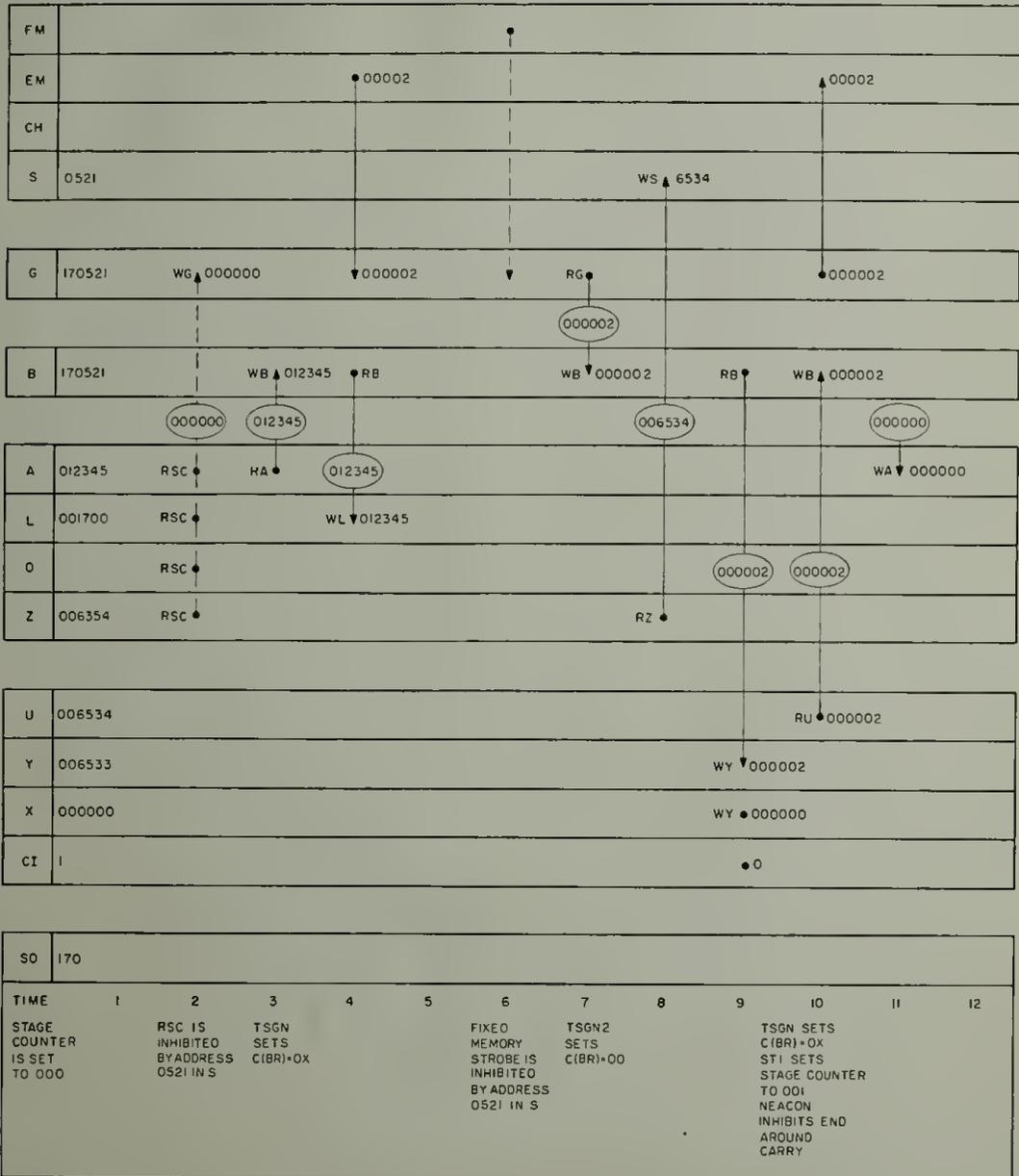


Figure 4-90. Subinstruction BZMF0 with Negative Quantity, Data Transfer Diagram 40771



40773

Figure 4-92. Subinstruction MP0 with Two Positive Numbers, Data Transfer Diagram

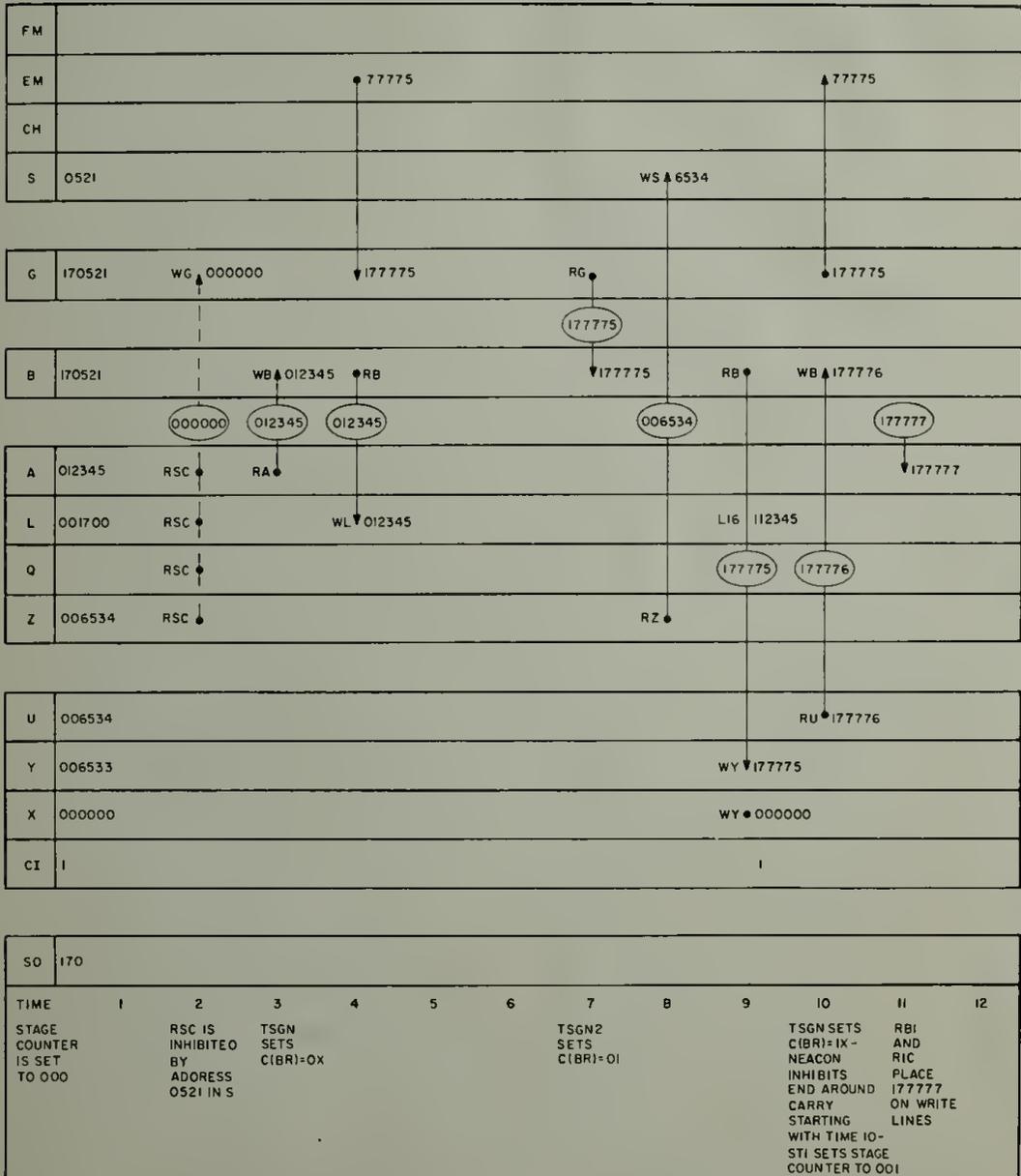


Figure 4-93. Subinstruction MP0 with Positive Number in A and Negative Number in E, Data Transfer Diagram

40774

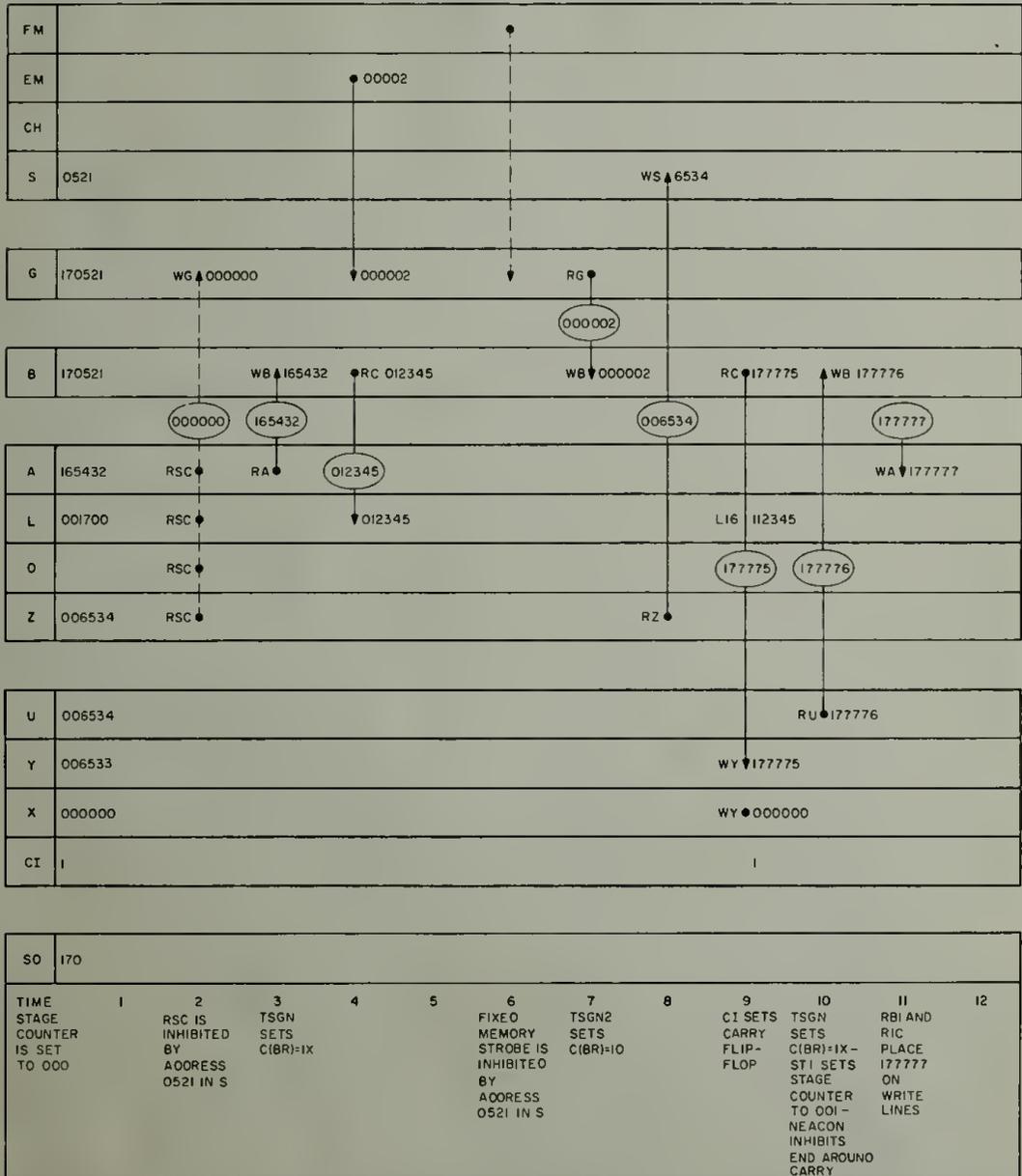
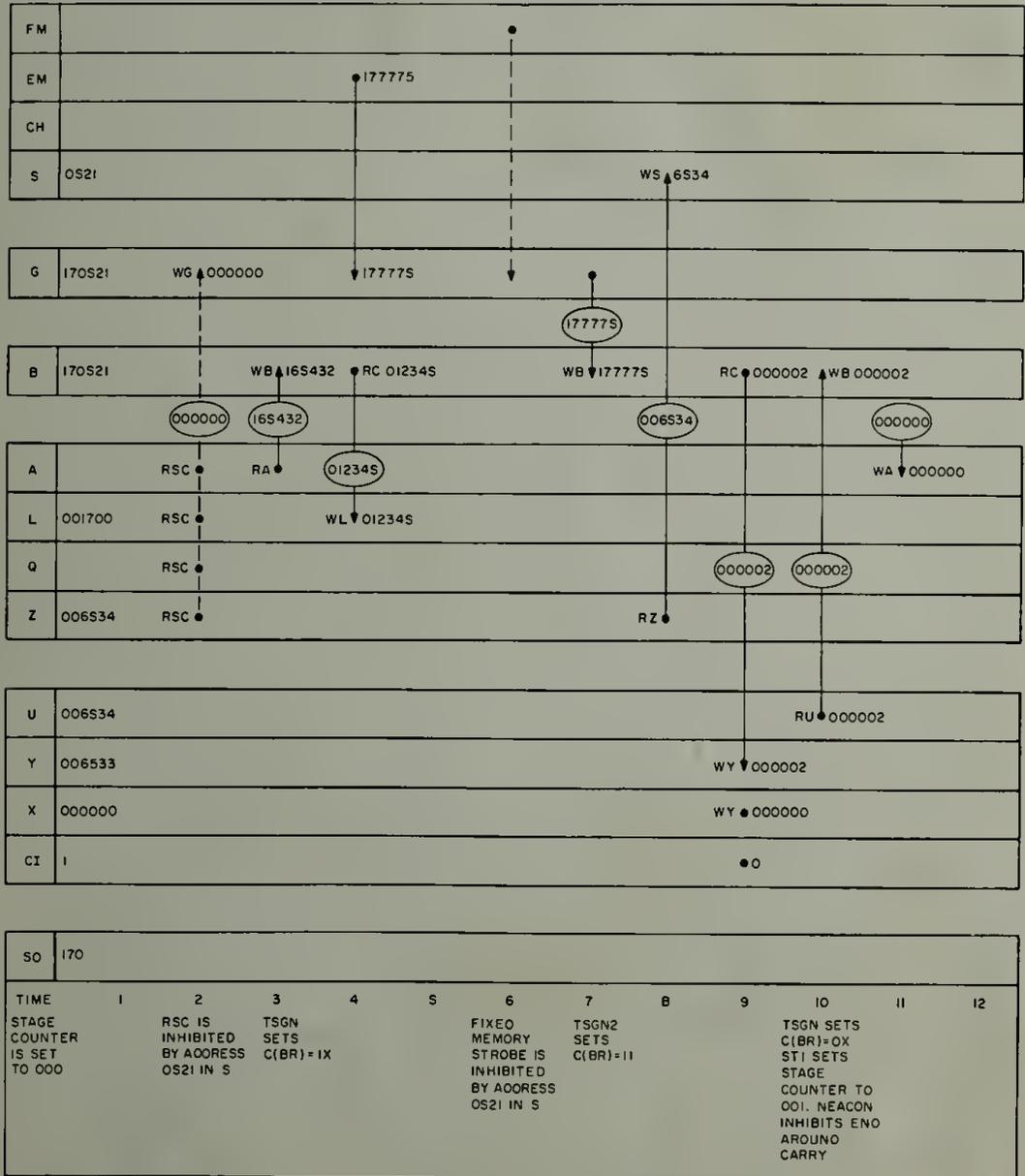


Figure 4-94. Subinstruction MP0 with Negative Number in A and Positive Number in E, Data Transfer Diagram

40775

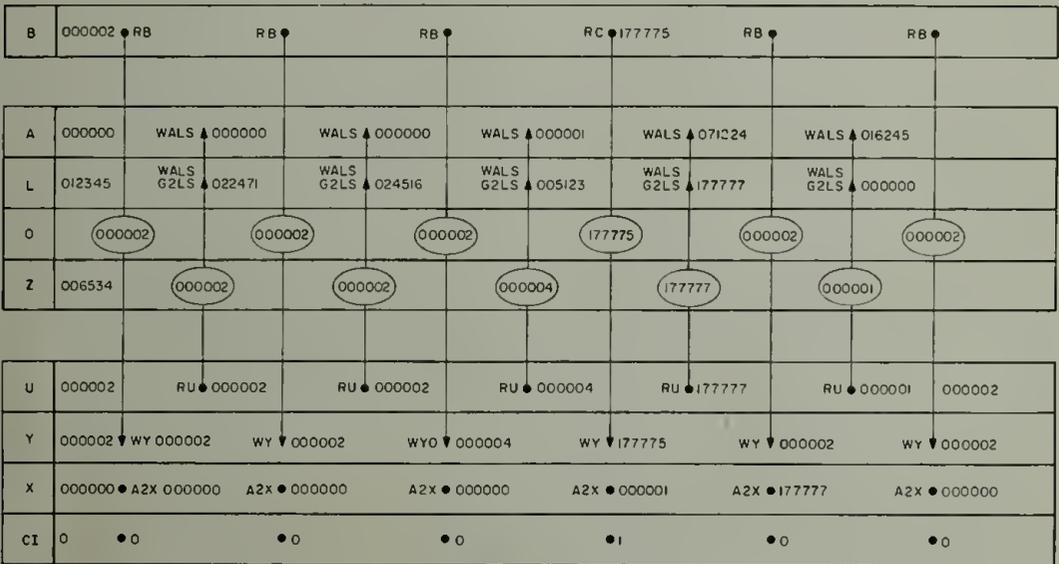


40776

Figure 4-95. Subinstruction MP0 with Two Negative Numbers, Data Transfer Diagram

FM	
EM	
CH	
S	6534

G	L2G0 177775 ● 024712	L2G0 ● 045162	L2G0 ● 051234	MCRO L2G0 ● 012247	L2G0 ● 062450	L2G0 ● 034512
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SO	170											
TIME STAGE COUNTER IS SET TO 001	1	2	3	4	5	6	7	8	9	10	11	12
							CI SETS CARRY FLIP-FLOP			STIANO ST2 SET STAGE COUNTER TO 011		

Figure 4-96. Subinstruction MP1, Data Transfer Diagram

40777

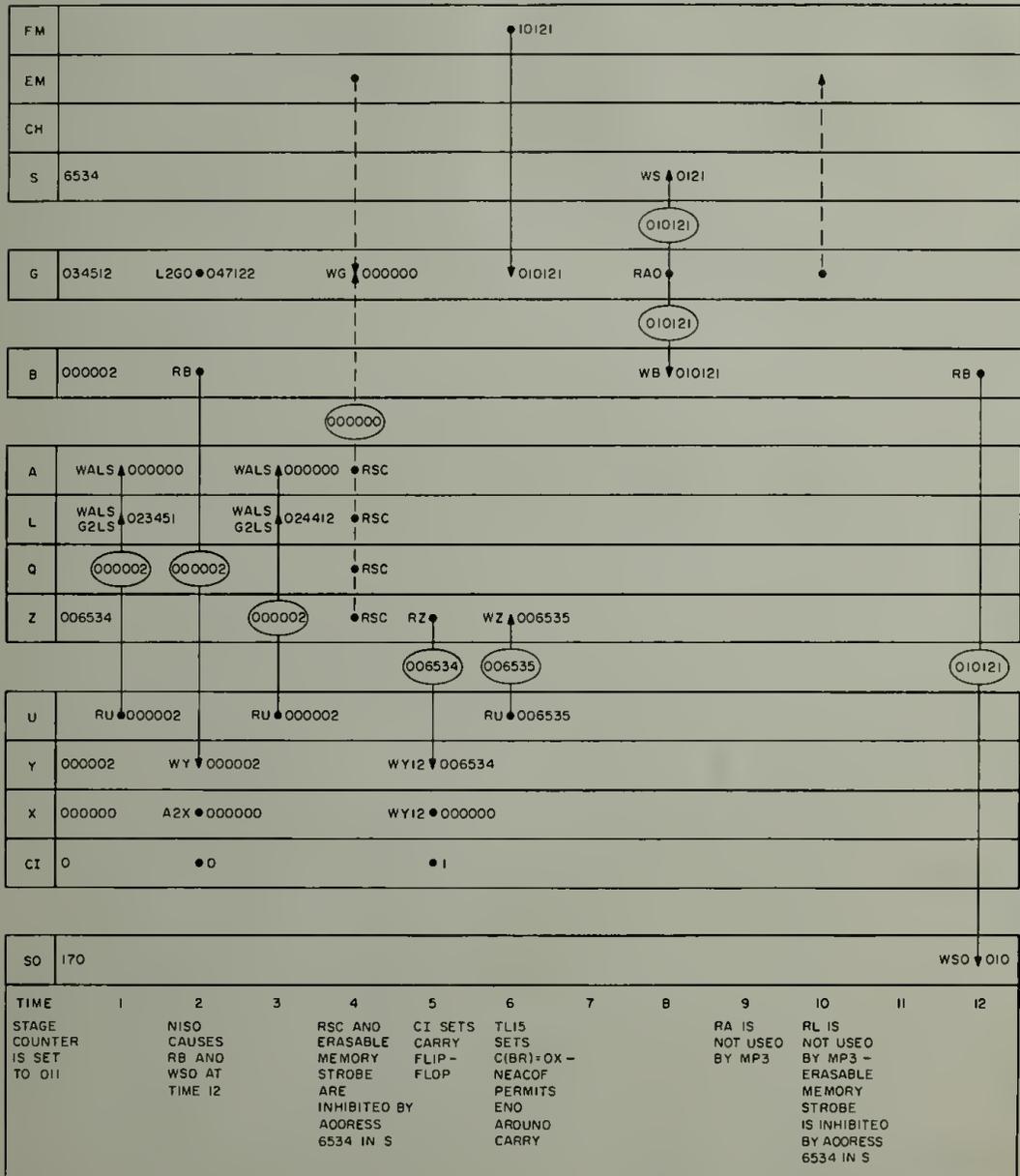
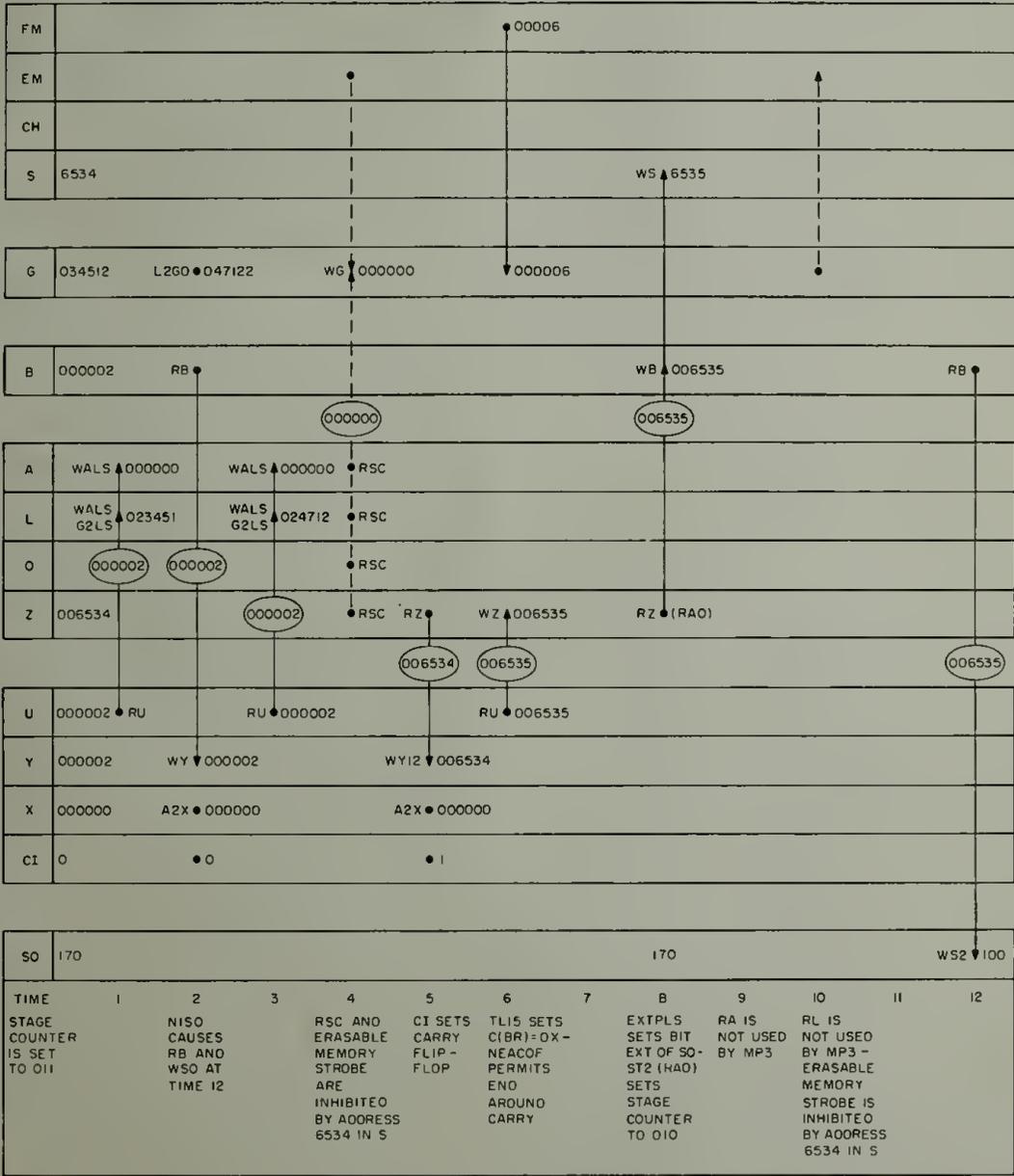


Figure 4-97. Subinstruction MP3, Data Transfer Diagram

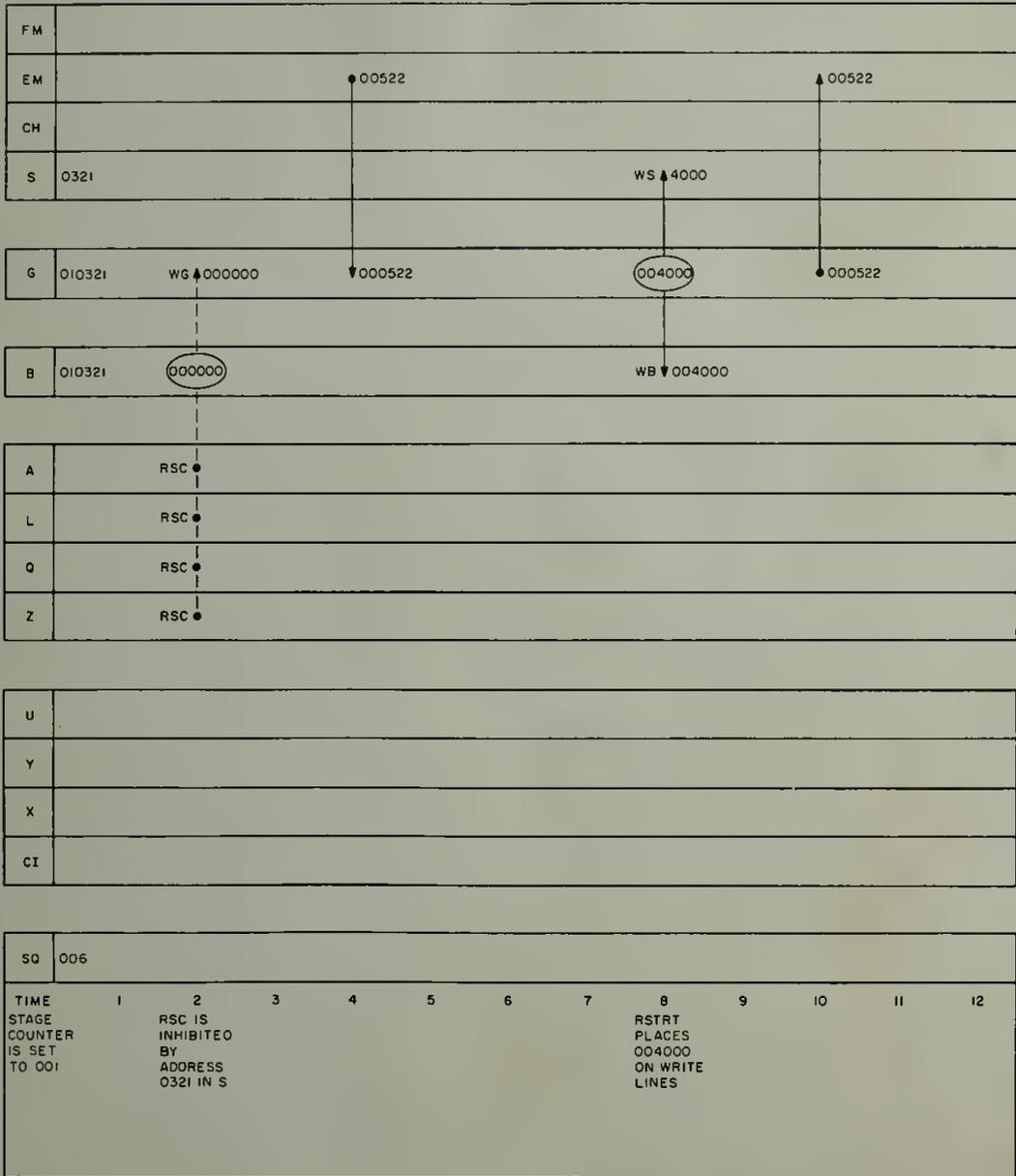
40778

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Figure 4-98. Subinstruction MP3 with Implied Address Code EXTEND, Data Transfer Diagram



40730

Figure 4-99. Subinstruction GOJ1, Data Transfer Diagram

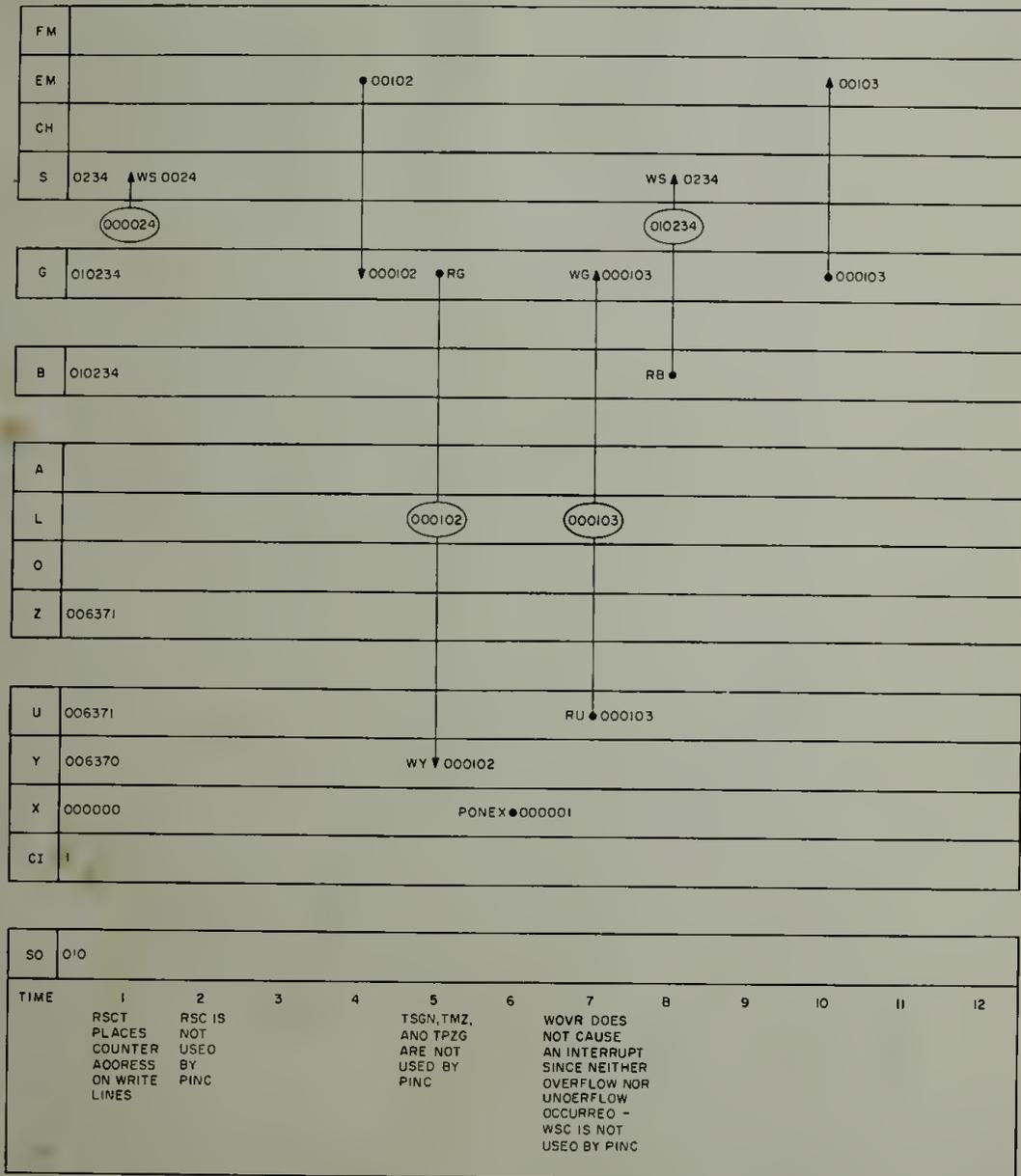


Figure 4-100. Subinstruction PINC, Data Transfer Diagram

40781

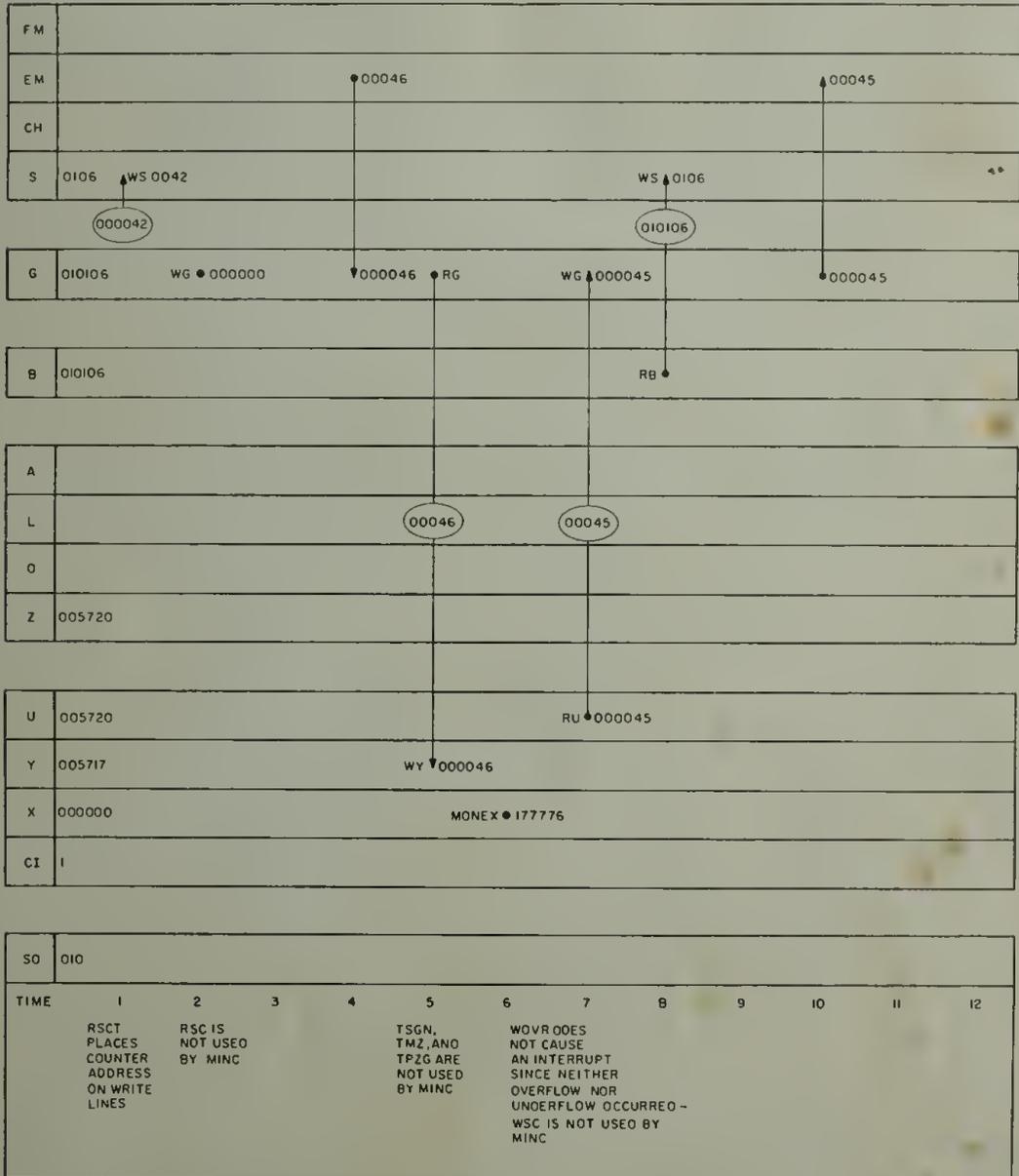
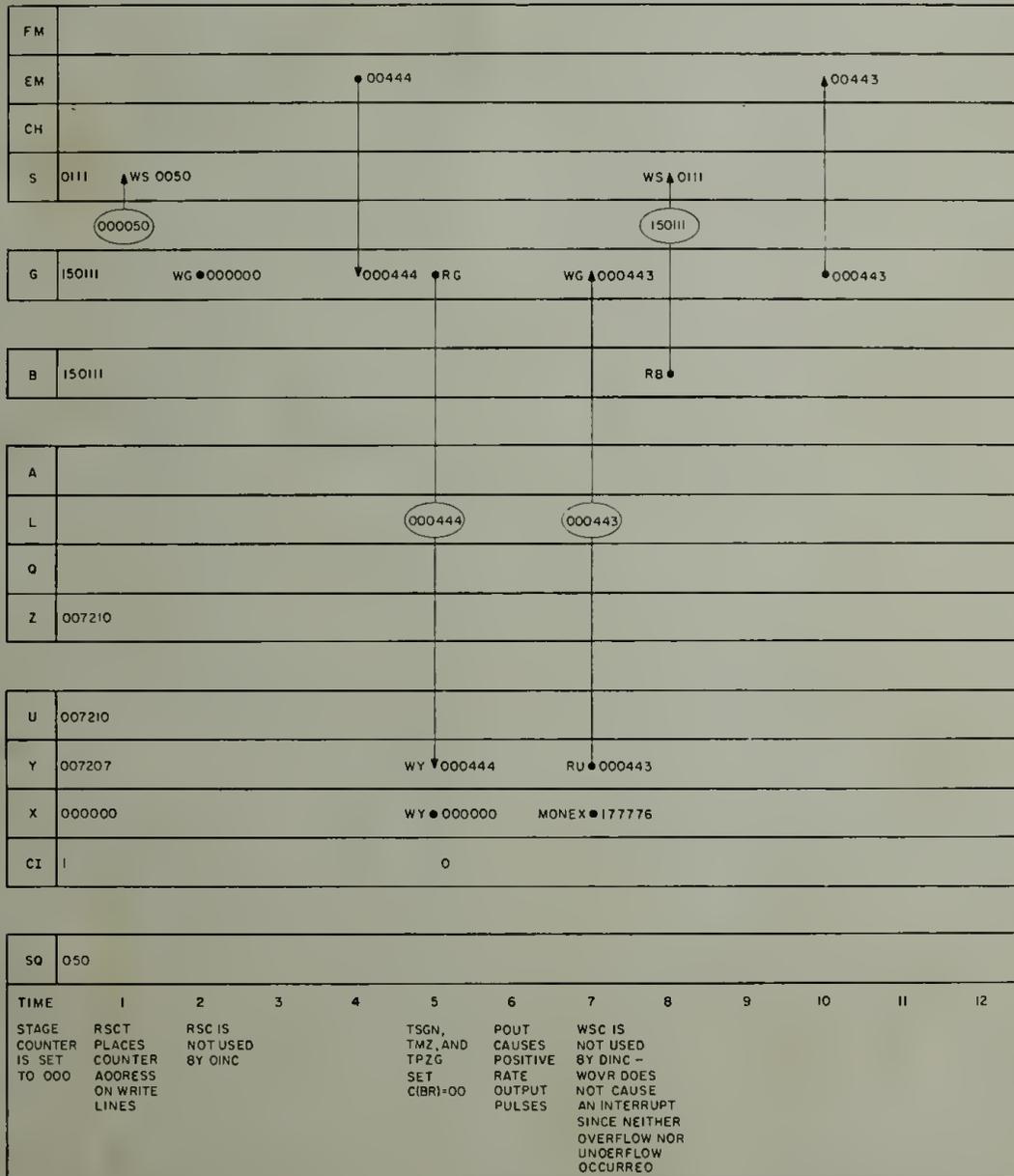


Figure 4-101. Subinstruction MINC, Data Transfer Diagram

40782

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Figure 4-102. Subinstruction DINC with Positive Quantity, Data Transfer Diagram

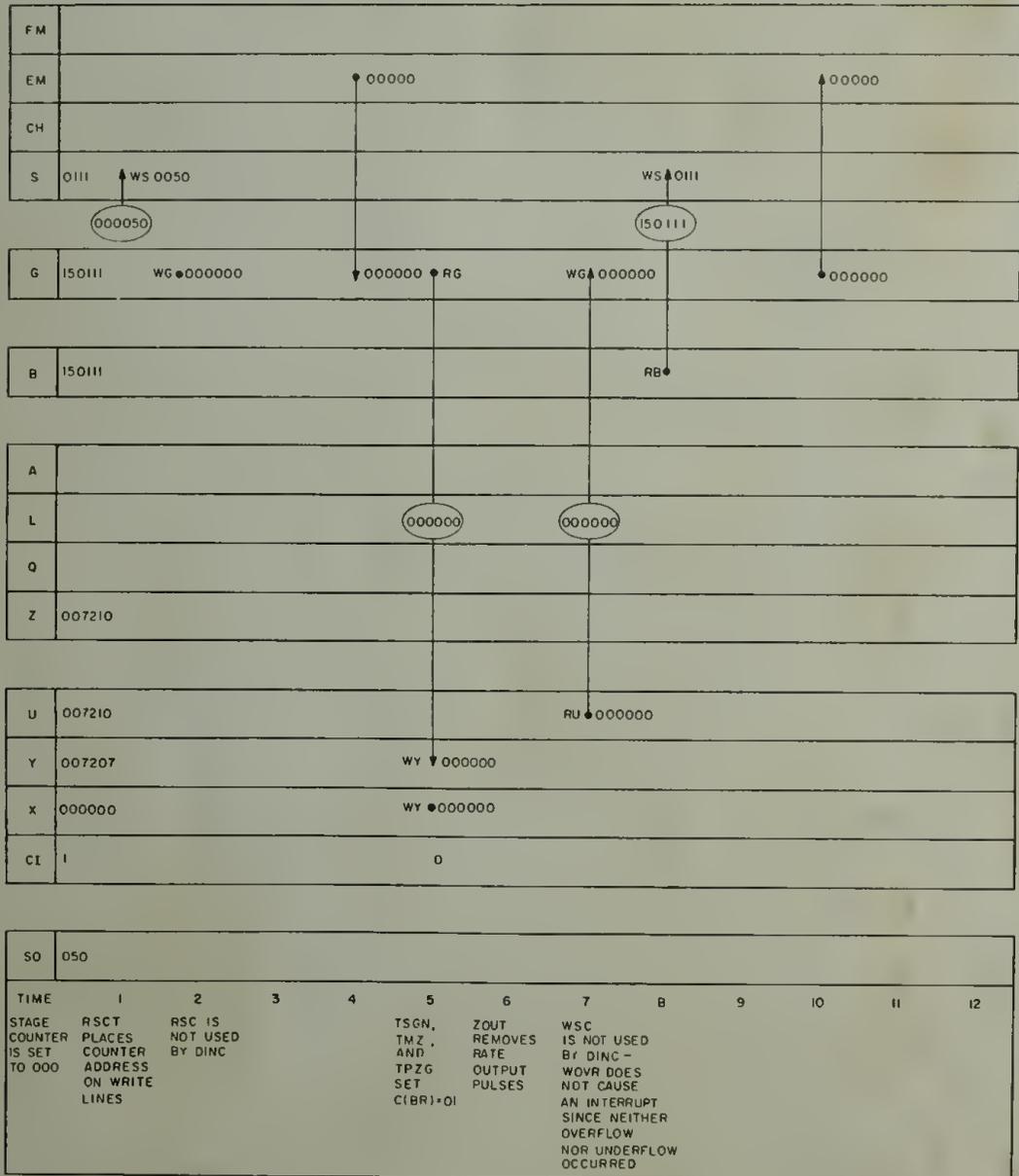
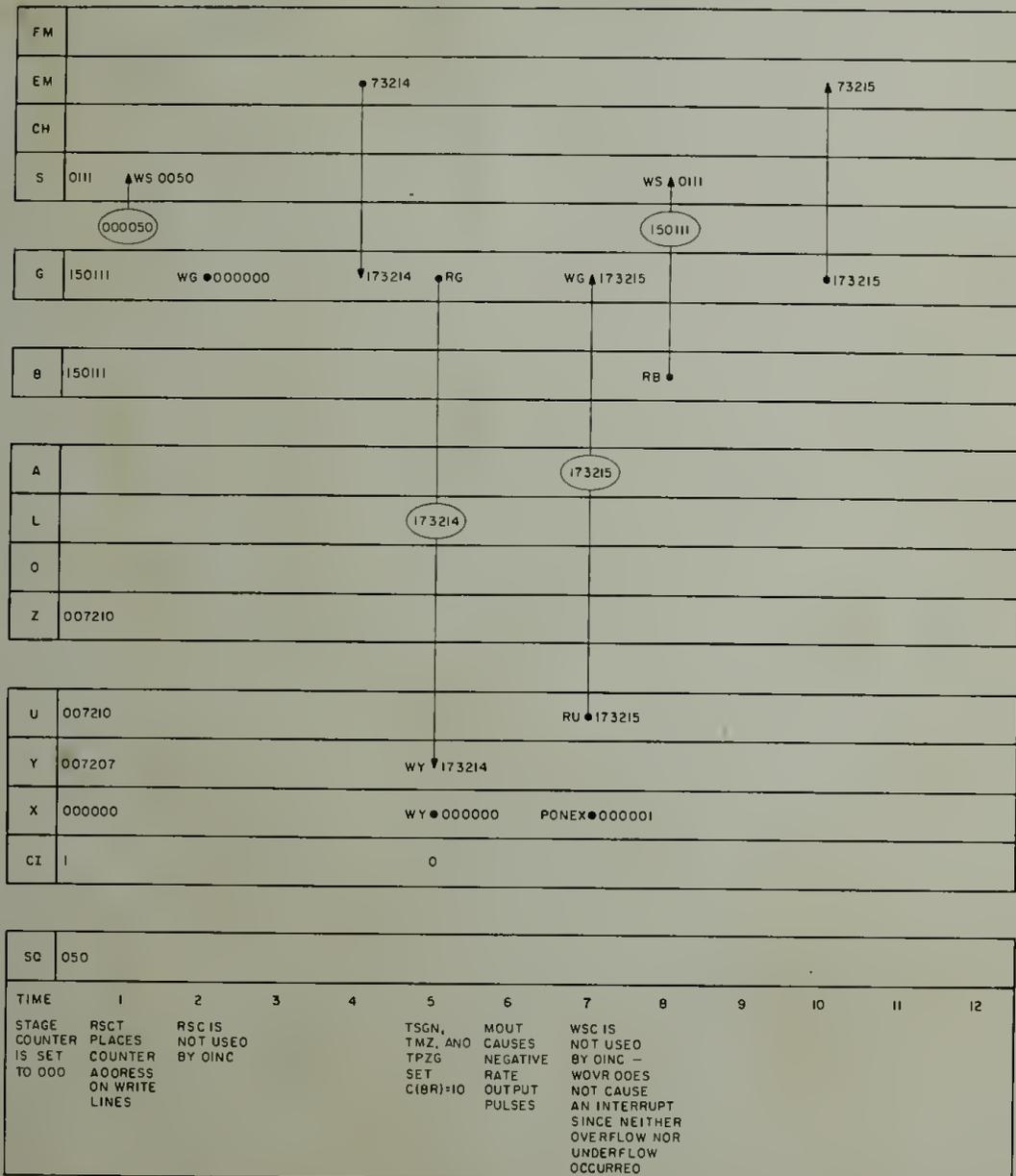


Figure 4-103. Subinstruction DINC with Plus Zero, Data Transfer Diagram

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Figure 4-104. Subinstruction DINC with Negative Quantity, Data Transfer Diagram

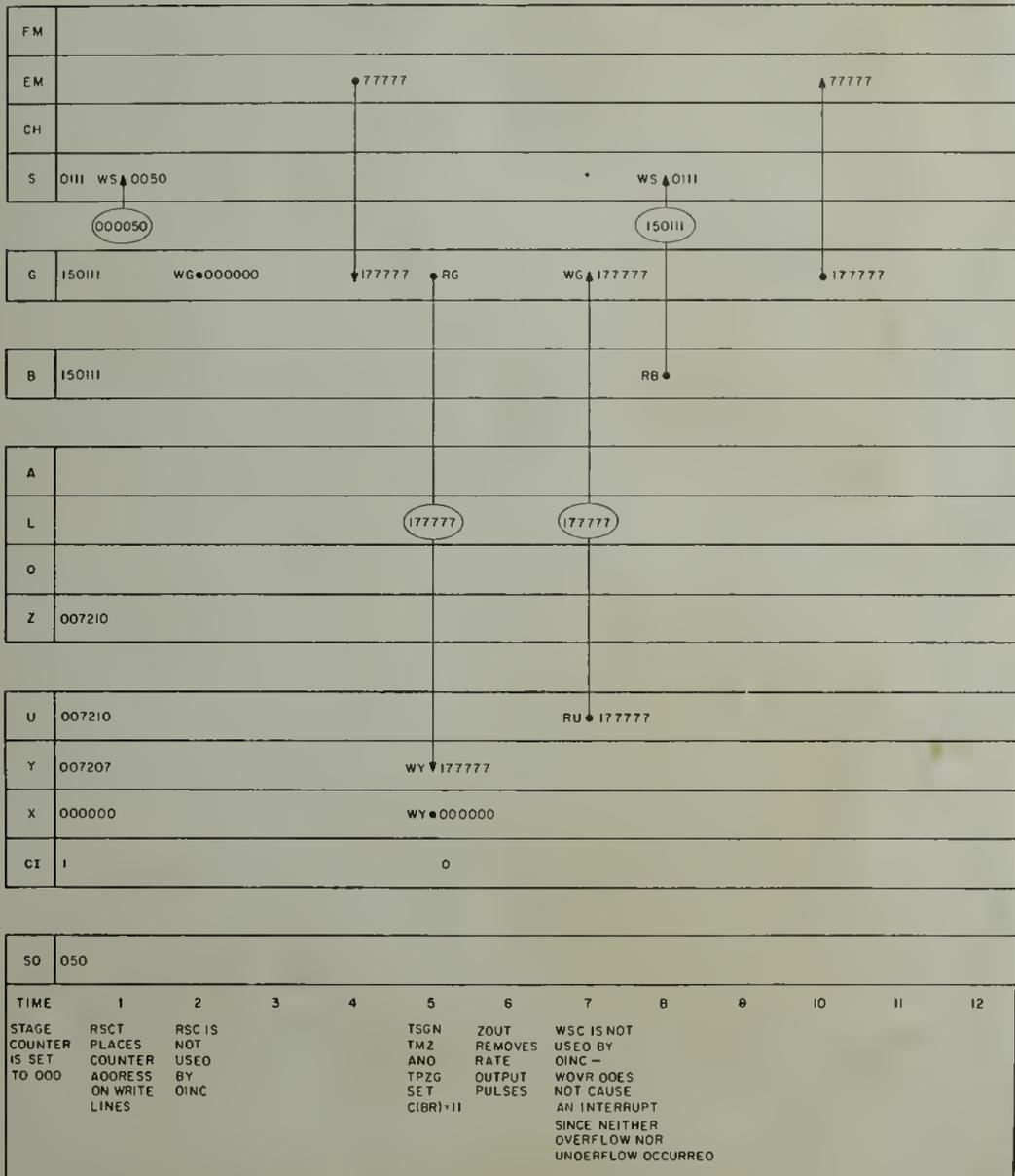
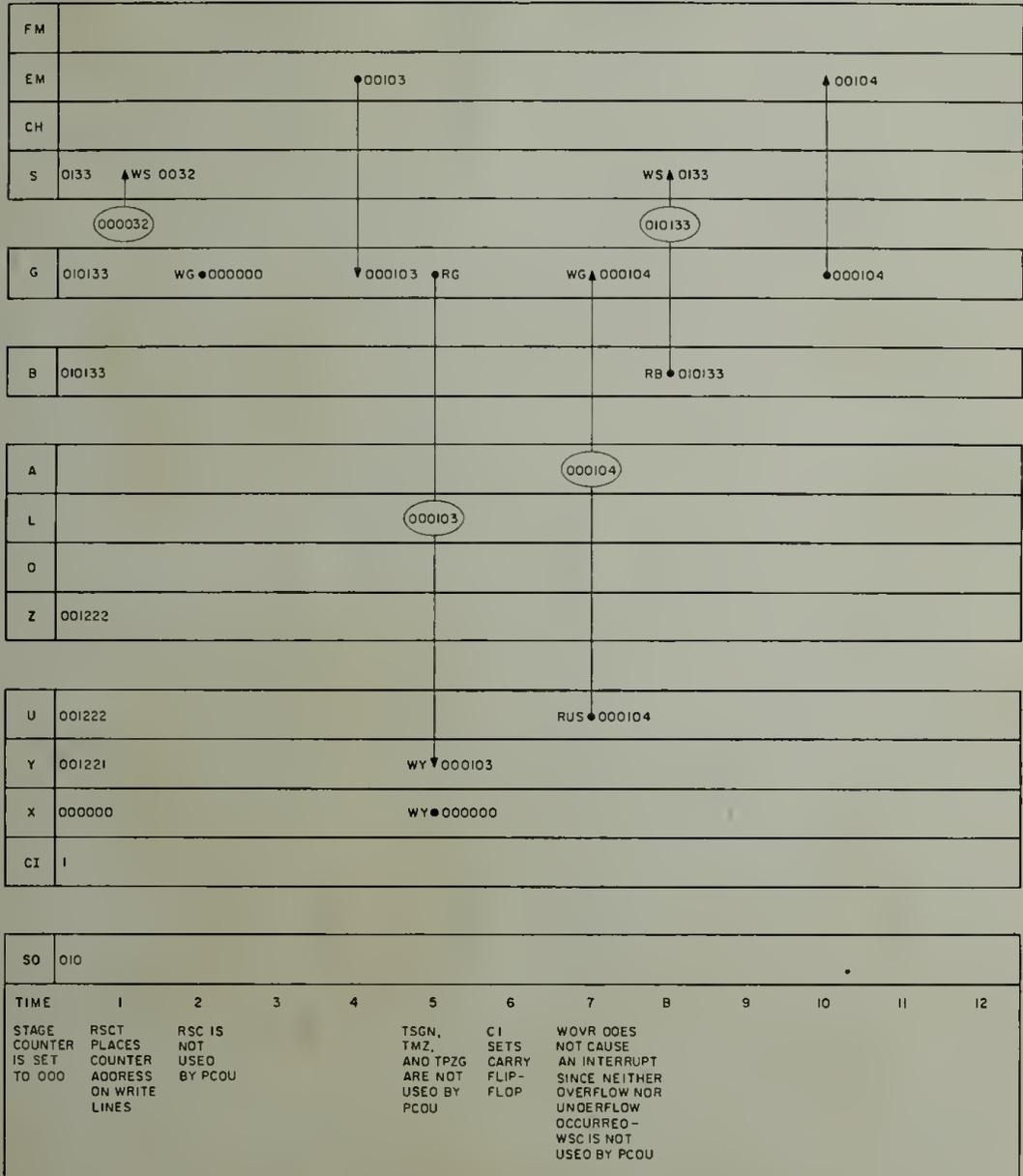


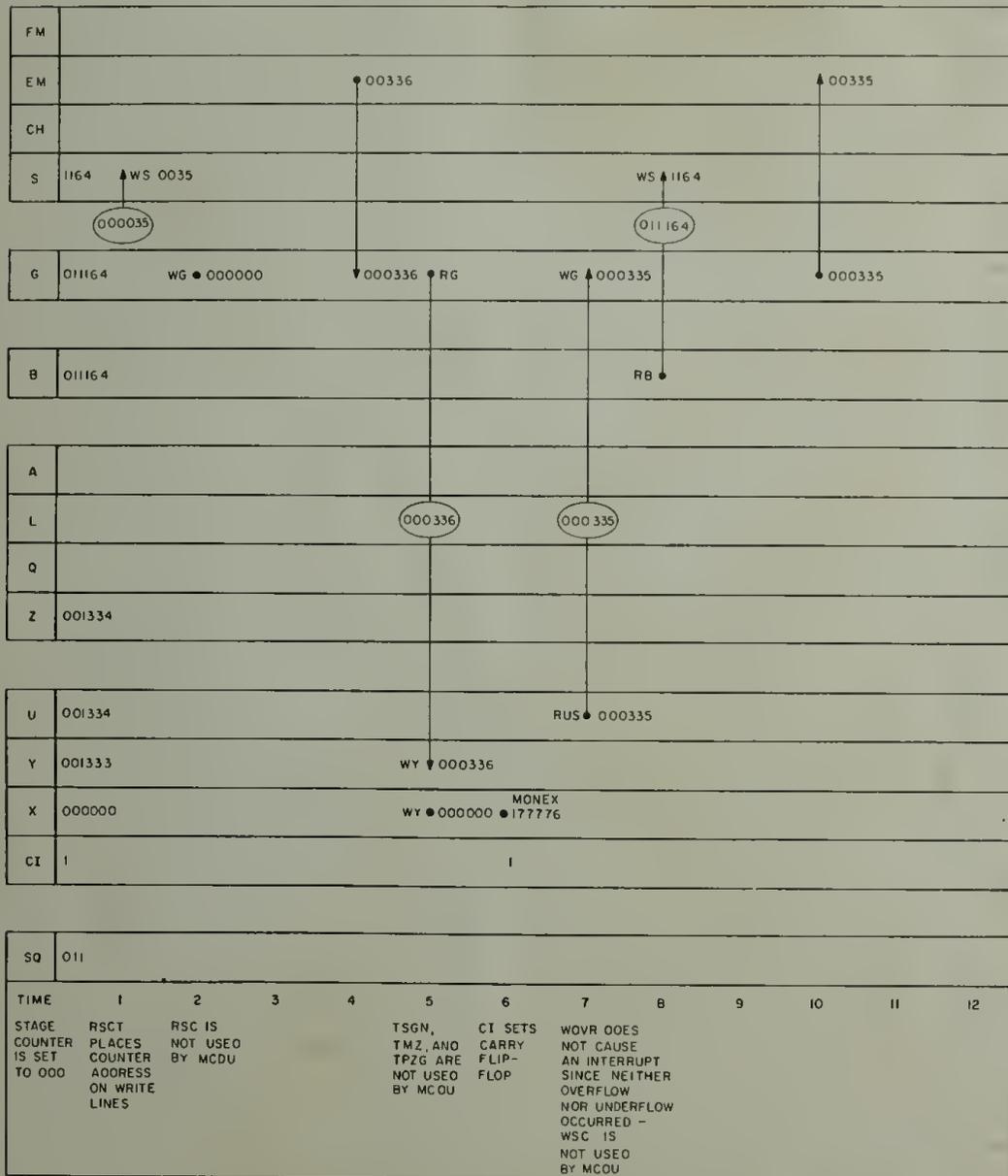
Figure 4-105. Subinstruction DINC with Minus Zero, Data Transfer Diagram

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Figure 4-106. Subinstruction PCDU, Data Transfer Diagram



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Figure 4-107. Subinstruction MCDU, Data Transfer Diagram

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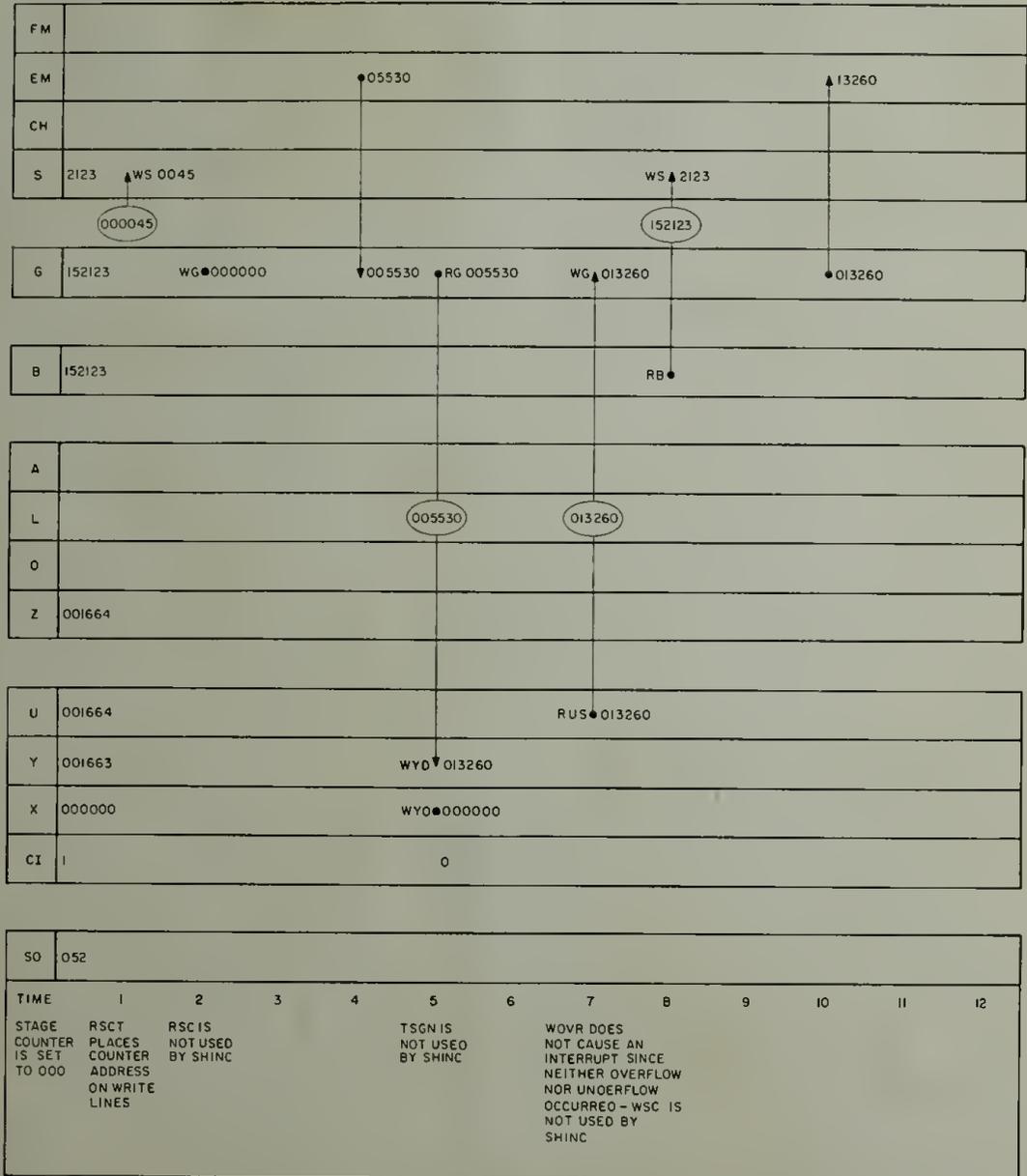


Figure 4-108. Subinstruction SHINC, Data Transfer Diagram

40789

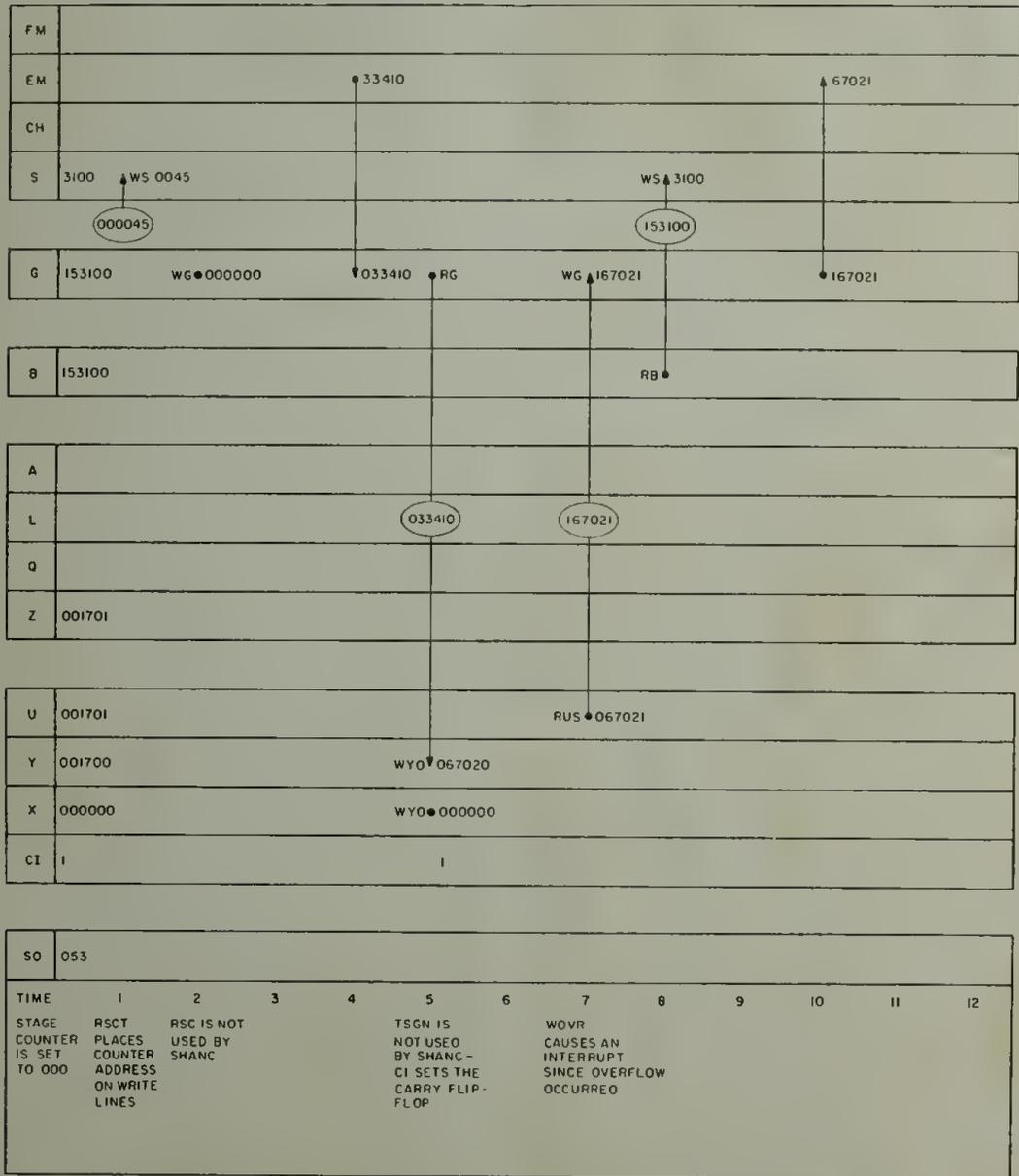


Figure 4-109. Subinstruction SHANC, Data Transfer Diagram

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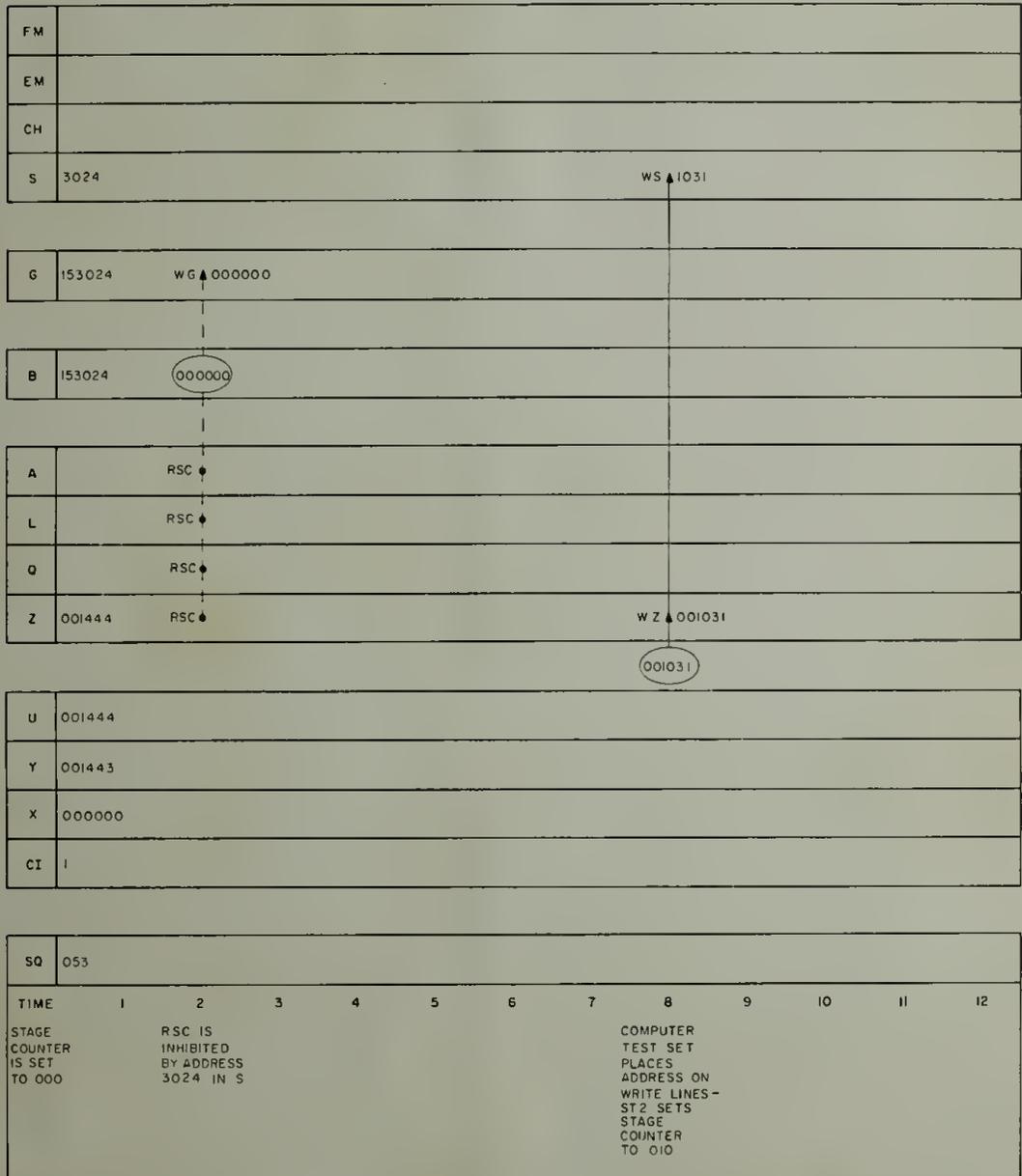


Figure 4-110. Subinstruction TCSAJ3, Data Transfer Diagram

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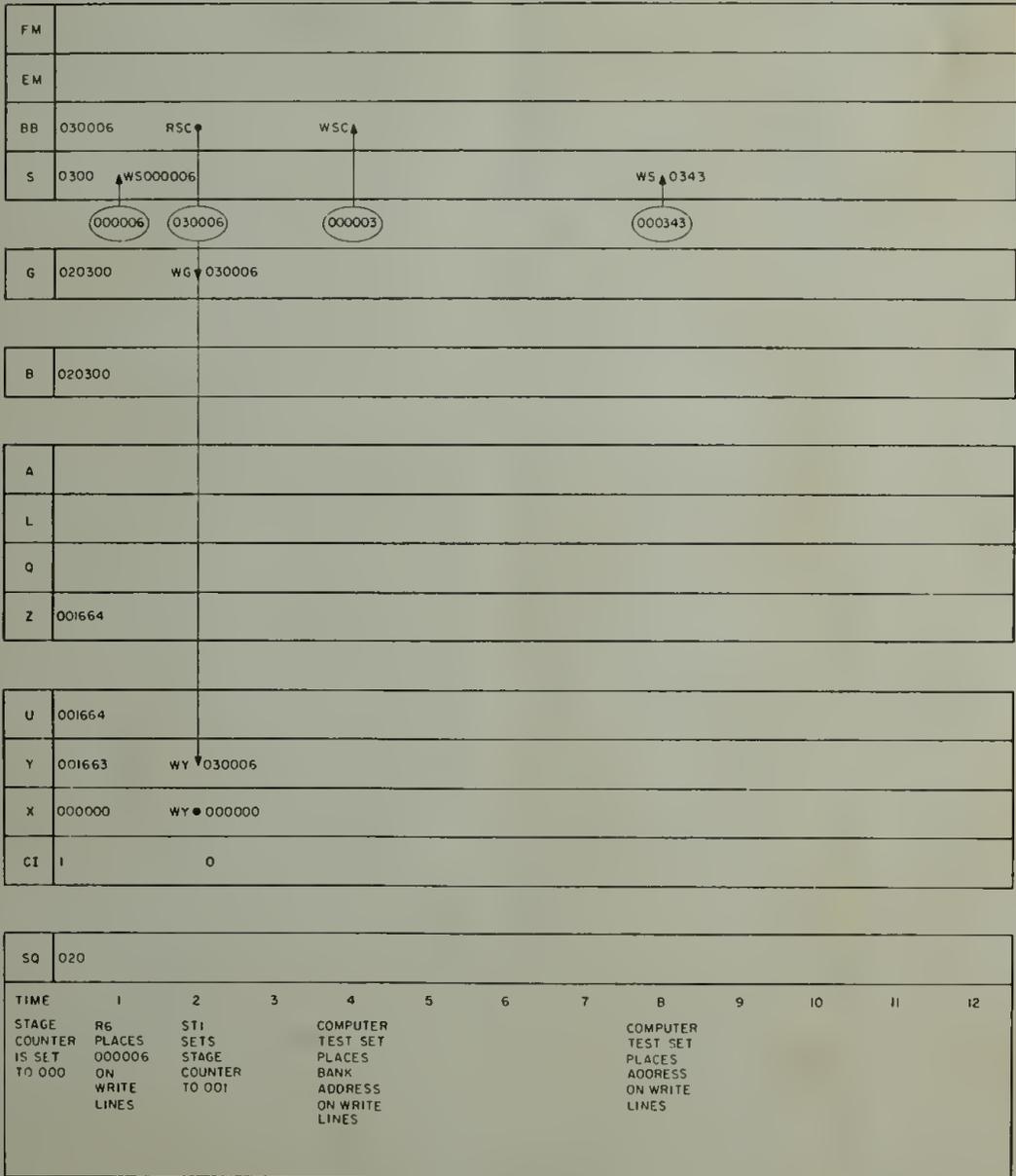


Figure 4-111. Subinstruction FETCH0, Data Transfer Diagram

40792

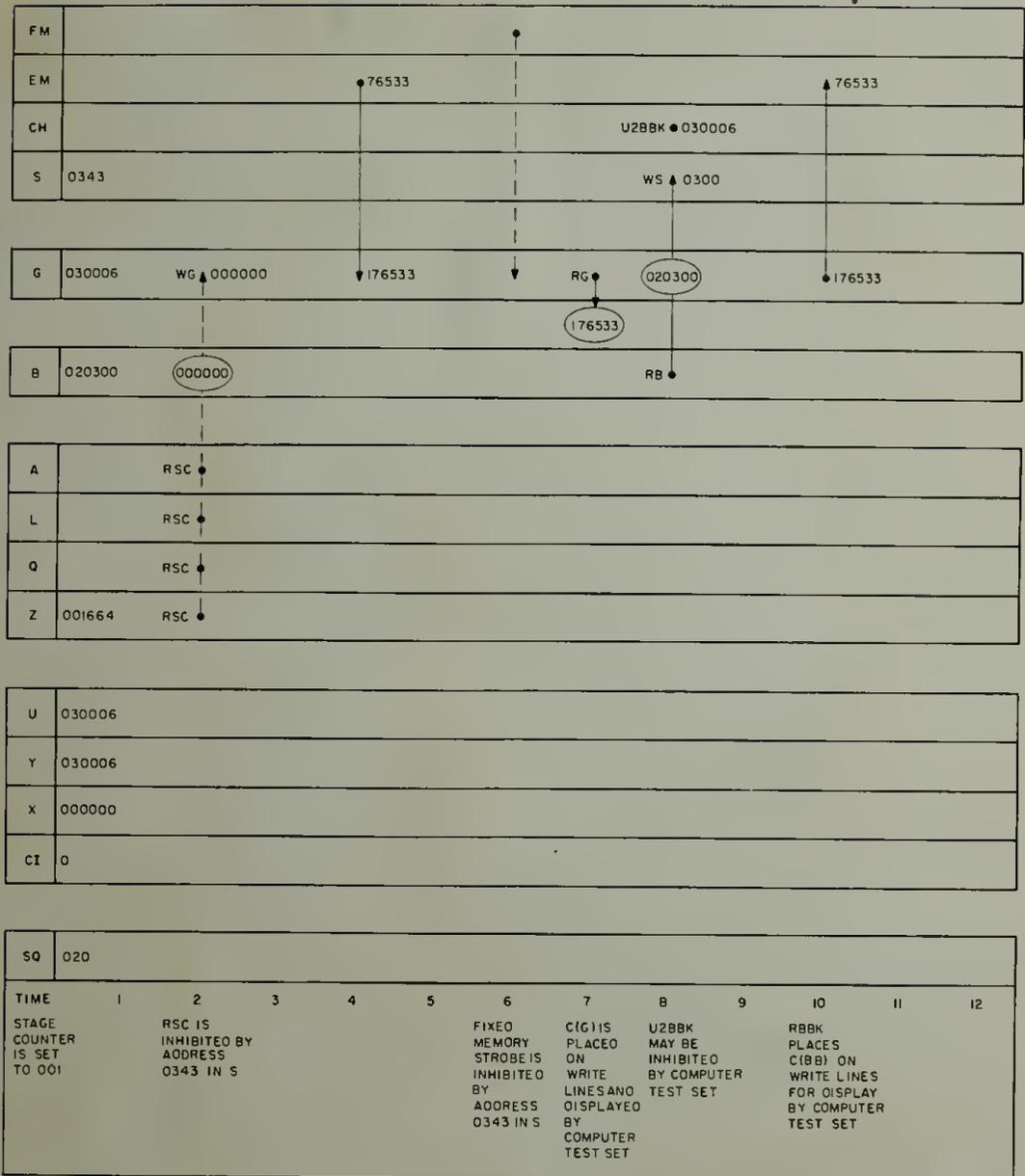


Figure 4-112. Subinstruction FETCH1, Data Transfer Diagram

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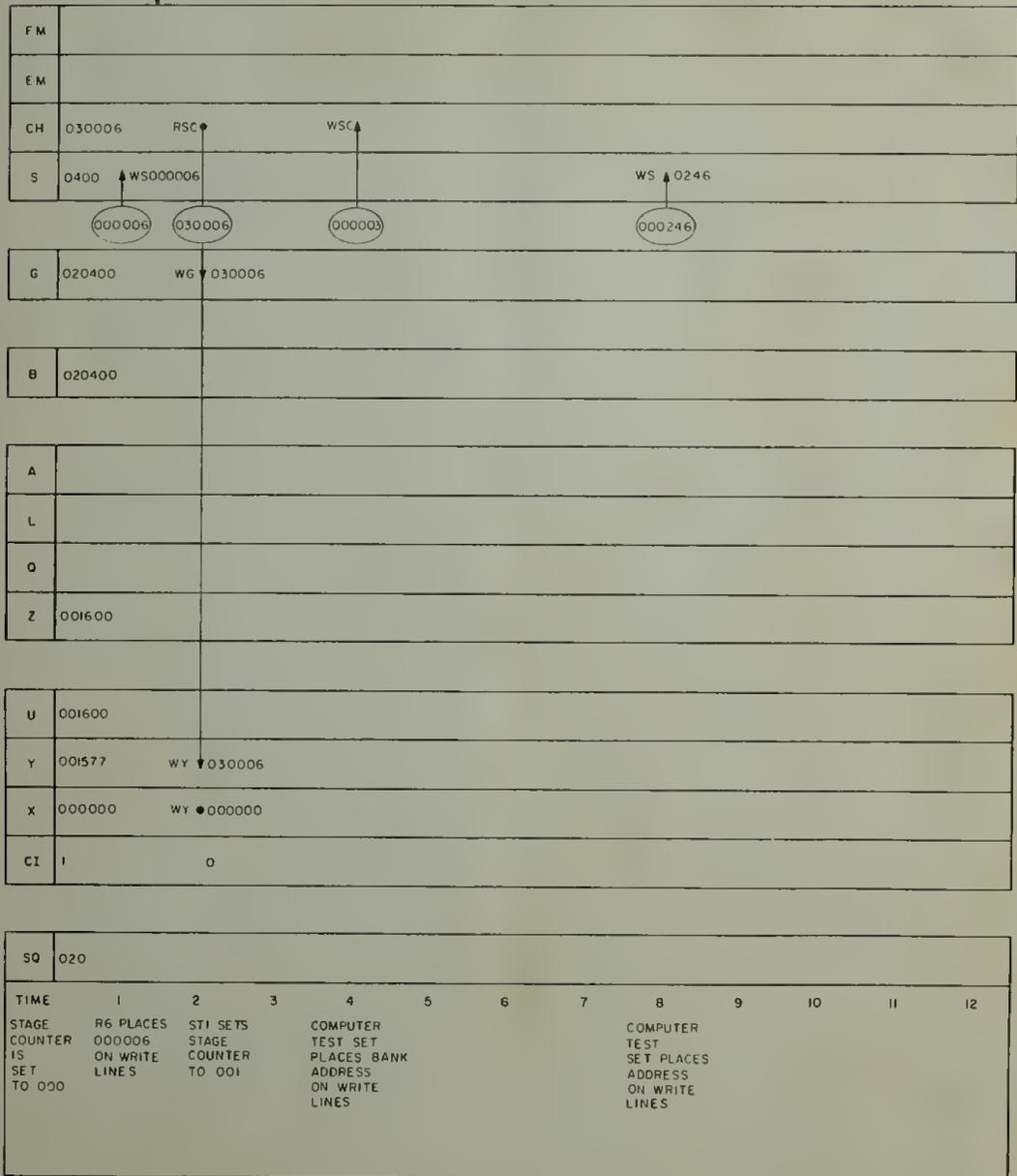


Figure 4-113. Subinstruction STORE0, Data Transfer Diagram

40794

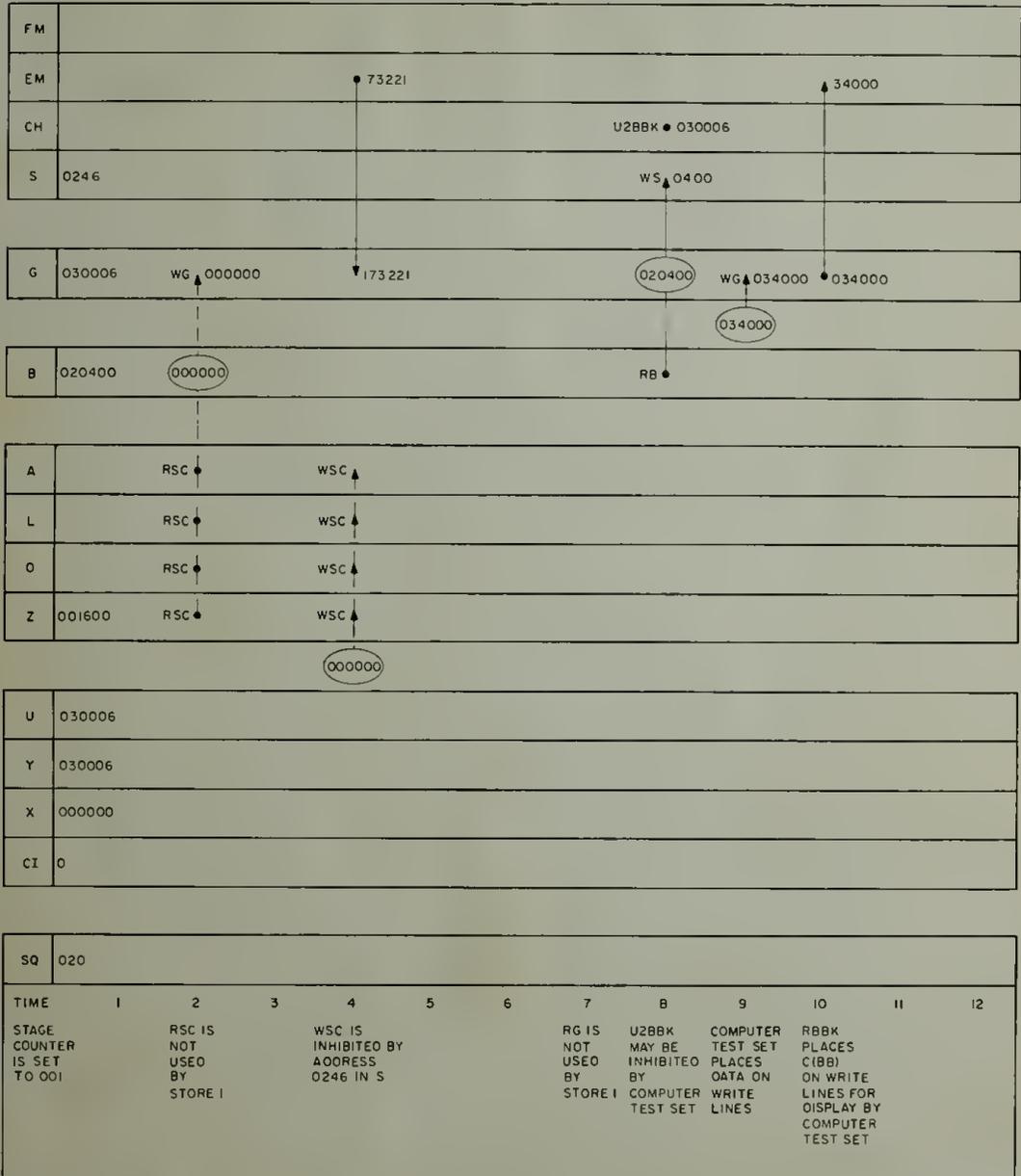


Figure 4-114. Subinstruction STORE1, Data Transfer Diagram

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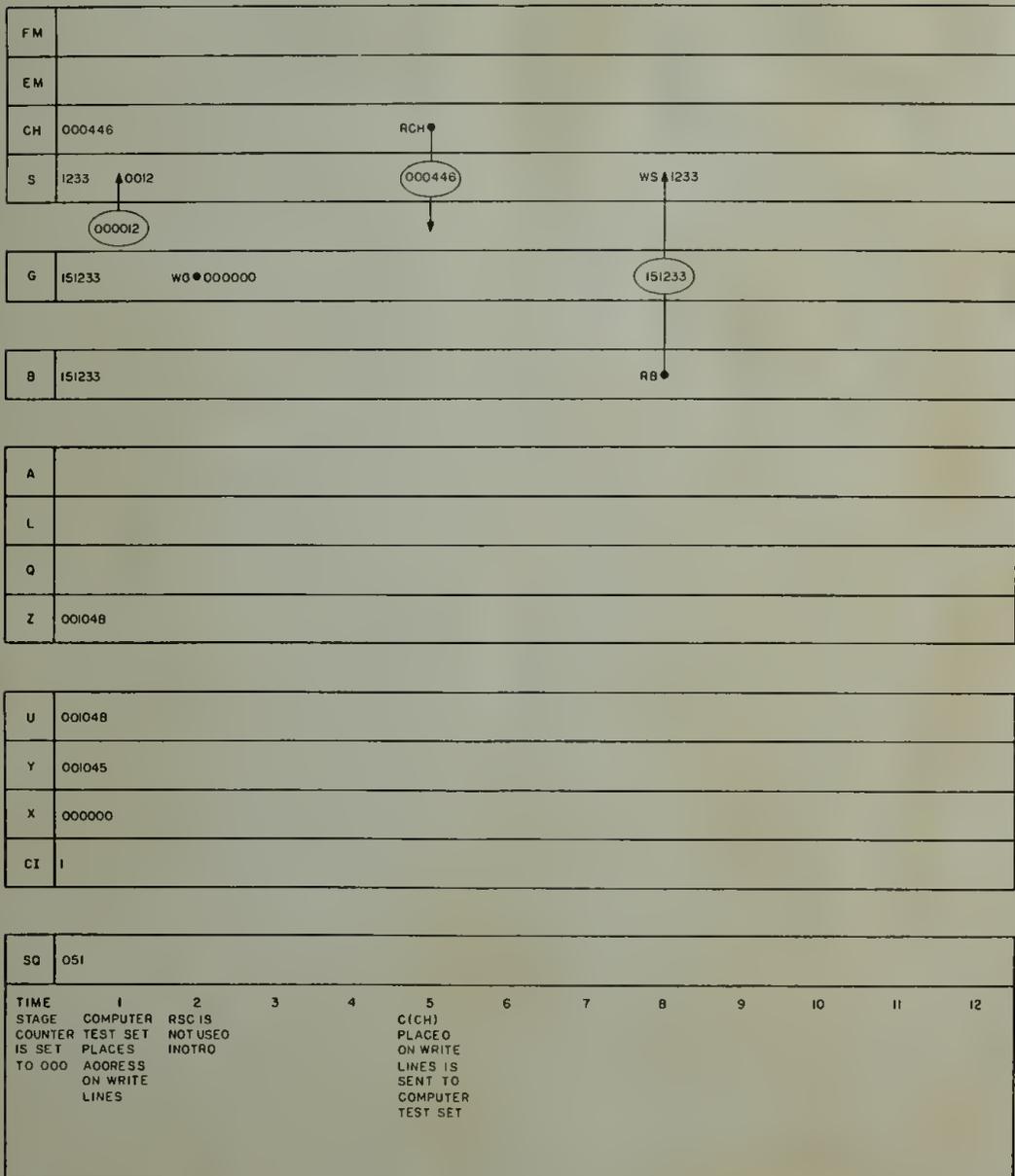


Figure 4-115. Subinstruction INOTRD, Data Transfer Diagram

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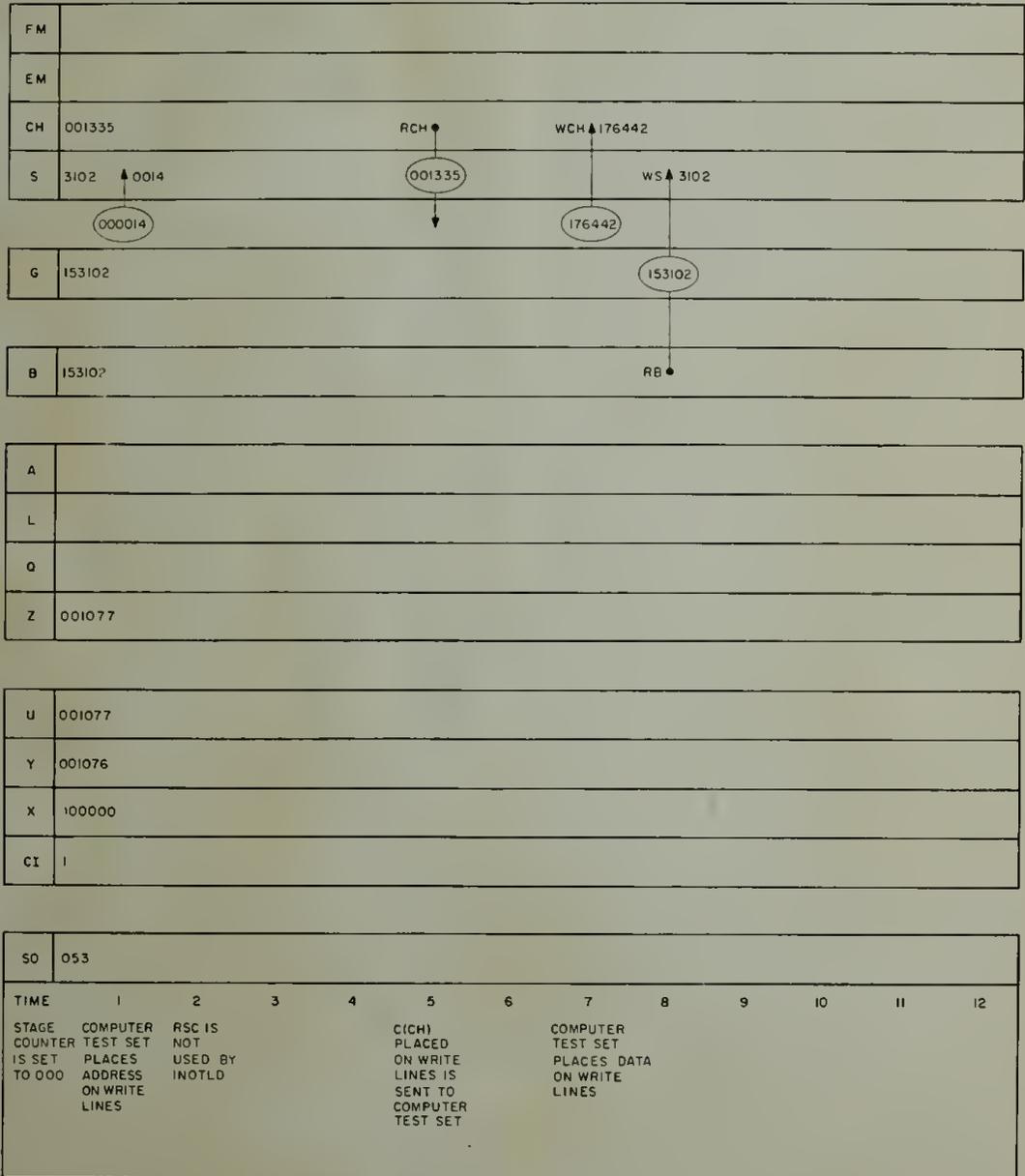


Figure 4-116. Subinstruction INOTLD, Data Transfer Diagram

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4-5.3 TIMER. The timer generates all timing functions required for operation of the LGC. In addition, the timer is the primary source of all timing and sync signals for all the LEM systems.

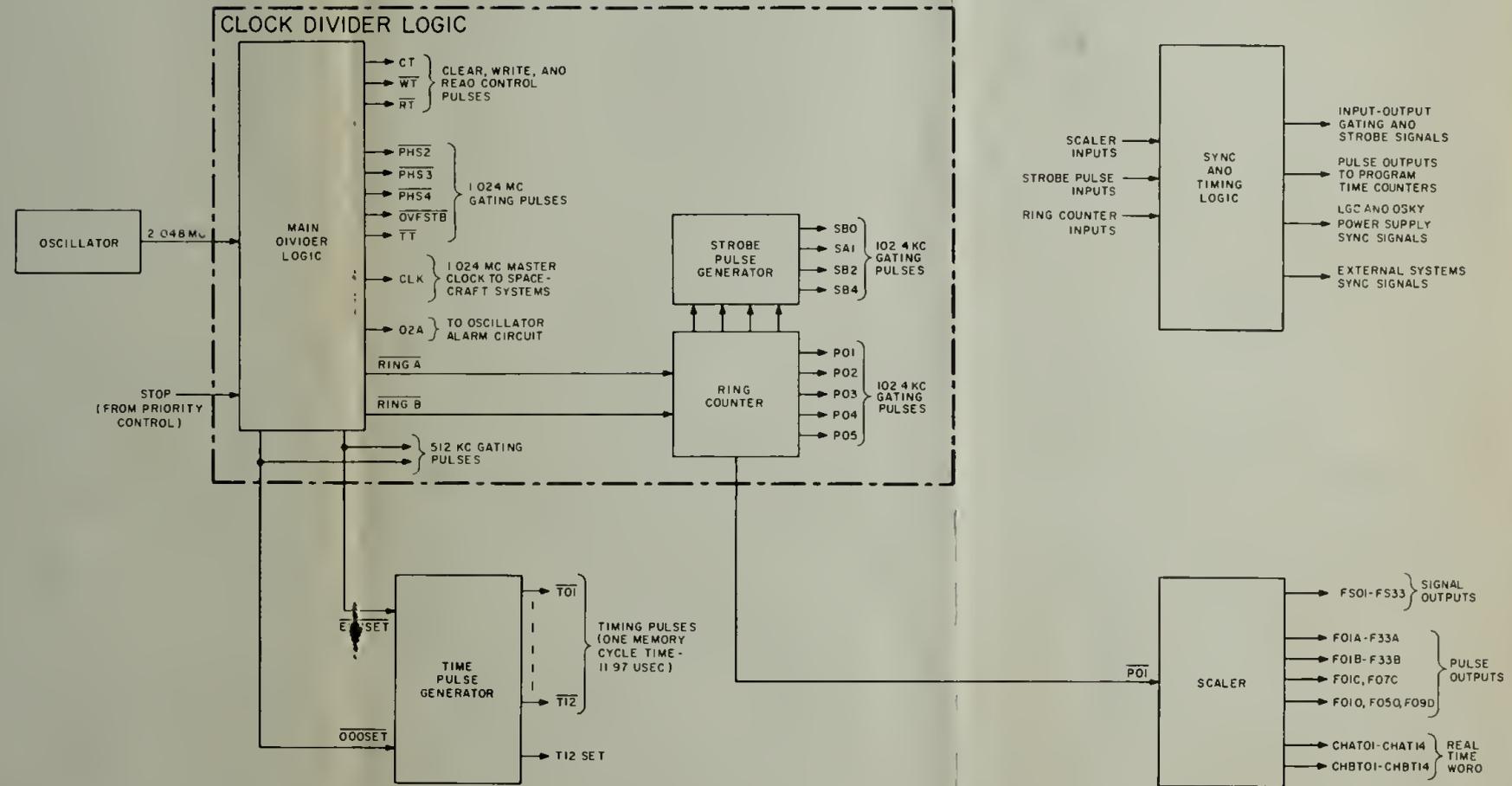
4-5.3.1 Timer Functional Description. Timer operation contains the functional areas indicated in figure 4-117. These functional areas include the LGC oscillator, clock divider logic, scaler, time pulse generator, and the sync and timing logic. The LGC oscillator is a crystal controlled, modified Pierce oscillator design that generates a source frequency of 2.048 mc for the clock divider logic. Temperature compensated components in the LGC oscillator circuit maintain a high degree of stability and assure an extremely accurate output frequency to the clock divider logic.

The clock divider logic is further subdivided into the main clock divider, ring counter, and strobe pulse generator. The 2.048 mc input from the LGC oscillator is applied to the main clock divider. The main clock divider divides the input frequency by two and generates the following outputs: clear, write, and read control pulses (\overline{CT} , \overline{WT} , \overline{RT}) which are applied to the central processor to produce the signals necessary to clear, write into, and read out the flip-flop registers; 1.024 mc gating pulses ($\overline{PHS2}$, $\overline{PHS3}$, $\overline{PHS4}$, \overline{OVFSTB} , \overline{TT}) which are used throughout the LGC; the master clock signal (CLK), a 1.024 mc output used to synchronize the other LEM systems; and signal Q2A which is applied to the oscillator alarm circuit in the power supply to indicate LGC oscillator activity. In addition, the main clock divider supplies signals ($\overline{RING A}$ and $\overline{RING B}$) to drive the ring counter, and signals (\overline{EVNSET} and \overline{ODDSET}) to the time pulse generator. These latter outputs occur at a 512 kc rate, a result of further division of the 1.024 mc gating rate within the main clock divider.

The ring counter generates outputs (P01 through P05) at a 102.4 kc rate. The outputs are 5 microsecond pulses used for gating and for deriving other timing functions in the LGC. Ring counter outputs are also used to derive the strobe pulses (SB0, SB1, SB2, SB4) from the strobe pulse generator. These outputs also occur at a 102.4 kc rate and are 3 microseconds in width with the exception of SB4, which is a 2 microsecond pulse.

The scaler consists of 33 identical divider stages. The stages are cascaded so that the frequency division is successive. The first stage, driven by signal $\overline{P01}$ from the ring counter, generates outputs at a rate of one-half the input or 51.2 kc. This output and the remaining outputs through stage 17 (0.78125 pps) are used for timing and gating. The outputs appear as signal outputs from flip-flop circuits (FS01, etc.), and 10 microsecond pulse outputs (F01A, etc.) at the same frequency as the associated stage. Stages 6 through 19 and 20 through 33 form a 28 bit real time word (CHAT01 through CHAT14, CHBT01 through CHBT14) which indicates time intervals up to 23.3 hours.

The time pulse generator, consisting of 12 flip-flop circuits, generates timing pulses $\overline{T01}$ through $\overline{T12}$. This sequence of timing pulses defines one MCT within the LGC, or a period of 11.97 microseconds, in which word flow takes place. The time pulse generator is driven by inputs (\overline{EVNSET} and \overline{ODDSET}) from the main clock divider.



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Figure 4-117. Timer, Functional Diagram

Signal $\overline{\text{ODDSET}}$ can be inhibited by signal STOP from priority control. Signal STOP, an input from the CTS during preinstallation system and subsystem tests, inhibits the time pulses from being generated thus preventing word flow in the LGC. This feature allows individual memory cycle times to be observed during tests.

The sync and timing logic consists of a gating complex which generates various outputs for use within the LGC, and synchronization signals for systems external to the LGC. The inputs to, and outputs from, this section are extensive, and are grouped by function in figure 4-117.

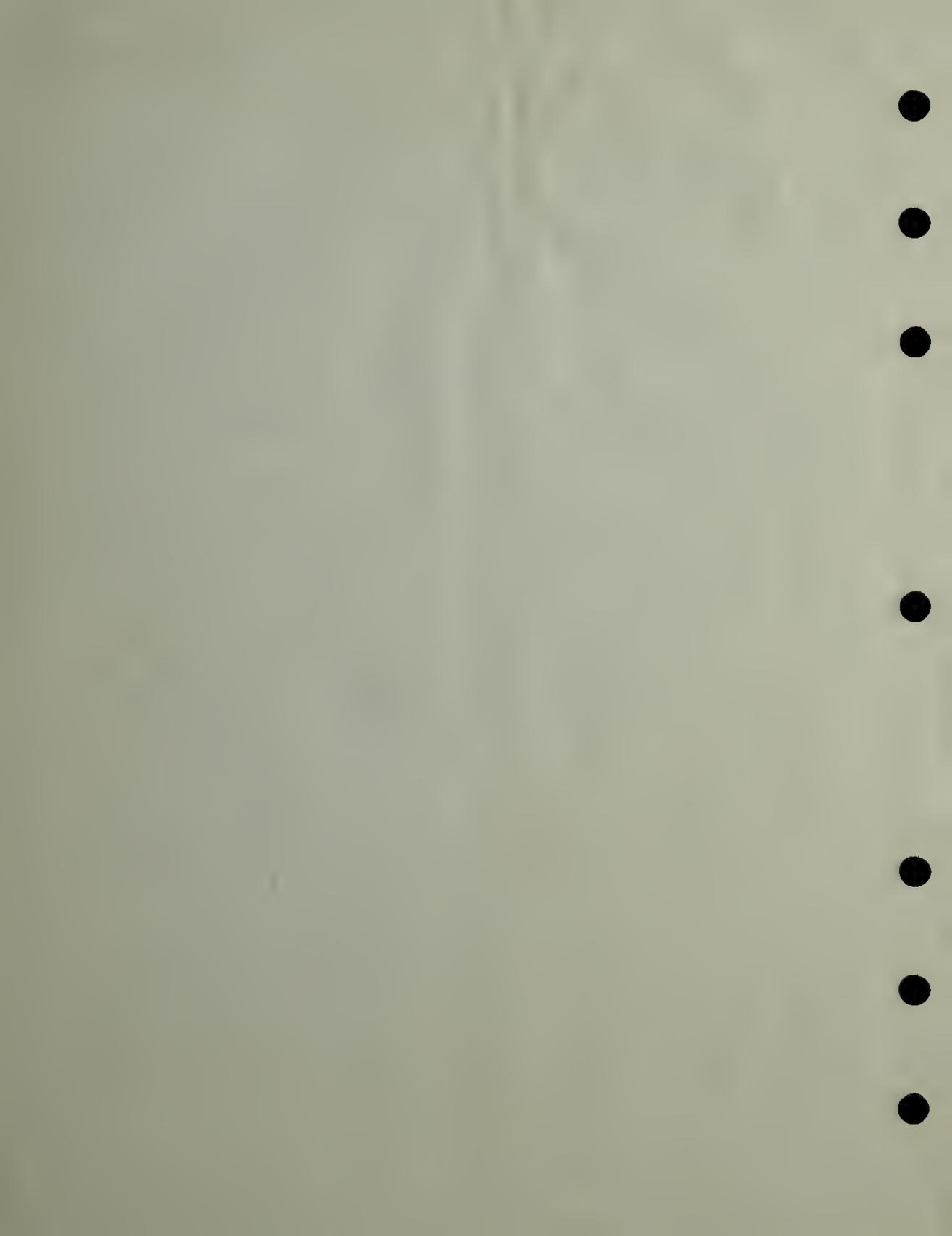
The ring counter, strobe pulse generator, and the scaler supply inputs to the sync and timing logic. These inputs are used to derive gating and strobe signals for the input and output channels, pulse outputs for the program time counters in memory, and synchronization signals for the LGC and DSKY power supplies and for systems external to the LGC.

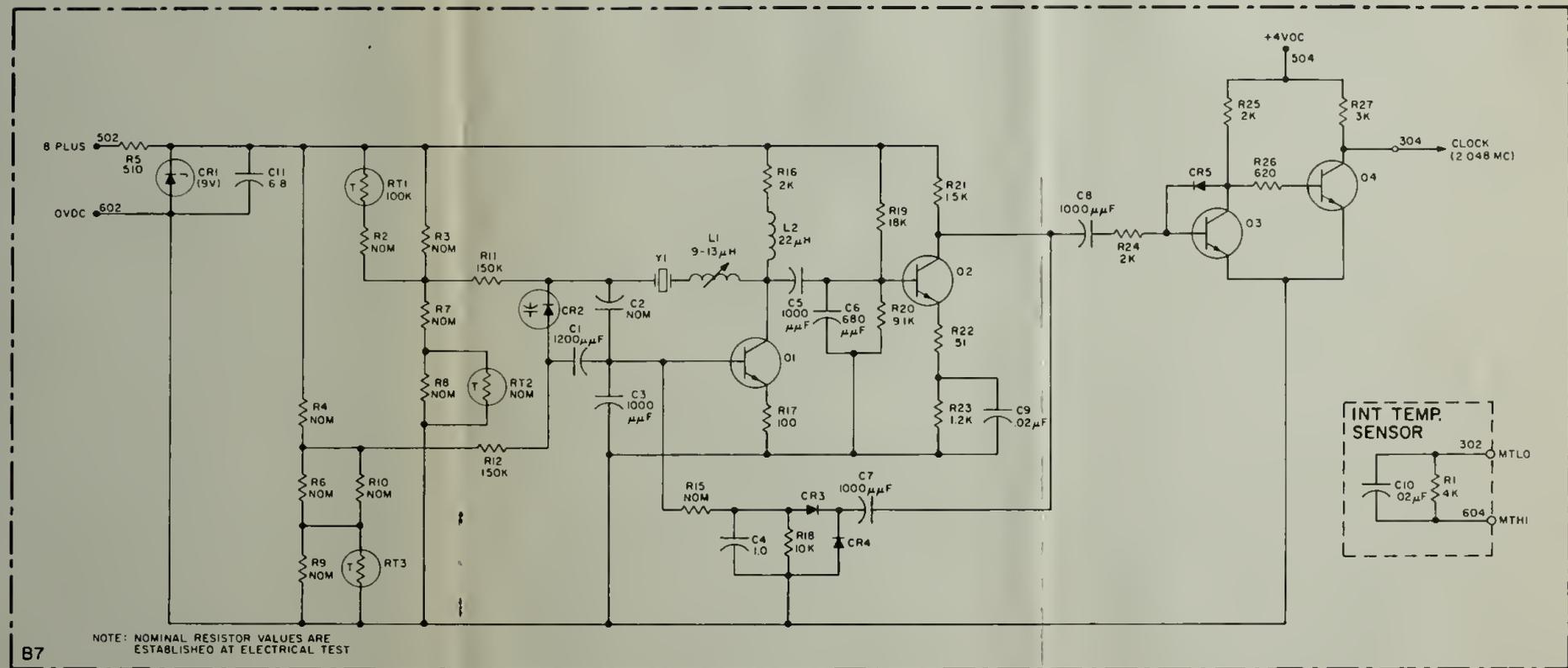
During standby operation, the LGC oscillator, clock divider logic, and the scaler are operative and generate the signals associated with these functional areas. However, the significant outputs during this mode of operation are the real time word from the scaler and the synchronization signals to the other LEM systems. The real time word continues to be accumulated during standby, and the external systems synchronization signals continue to be generated.

4-5.3.2 LGC Oscillator Detailed Description. The LGC oscillator (figure 4-118) generates a master clock frequency of 2.048 mc. The basic LGC oscillator circuit, consisting of crystal Y1, and transistor Q1 and associated components, is a modified Pierce oscillator design. Variable inductor L1, in series with the crystal, compensates for frequency drift due to component aging. The crystal output is amplified by transistor Q1, which operates as a class A amplifier that drives buffer stage Q2. The sinusoidal output of stage Q2 is applied to pulse shaper Q3 and, through capacitor C7, to a dc feedback network. The output of the feedback network controls the peak-to-peak output level of stage Q1. The resultant 2.048 mc square wave output of stage Q3 is amplified by output stage Q4, and is applied to the clock divider logic.

The collector supply voltage for stages Q1 and Q2 is obtained from the +14 volt output (B PLUS) of the power supply. This voltage is applied through resistor R5 and is regulated by zener diode CR1 (rated at 9 volts). The +4 volt power supply output is furnished directly as the collector supply for stages Q3 and Q4.

Two resistor networks (R4, R6, R10, R9, R12 and R2, R3, R7, R8, R11), in conjunction with thermistors RT1, RT2, and RT3 and varicap CR2, comprise the temperature compensation network which improves the stability of the LGC oscillator. The regulated output voltage of diode CR1 is applied across the two resistor networks, the outputs of which are applied across varicap CR2. The varicap is a reverse-biased diode that introduces capacitance into the circuit. Any changes in temperature cause a corresponding change in the reverse bias across the varicap thus varying the effective capacitance in series with crystal Y1, which is also affected by the change in temperature.





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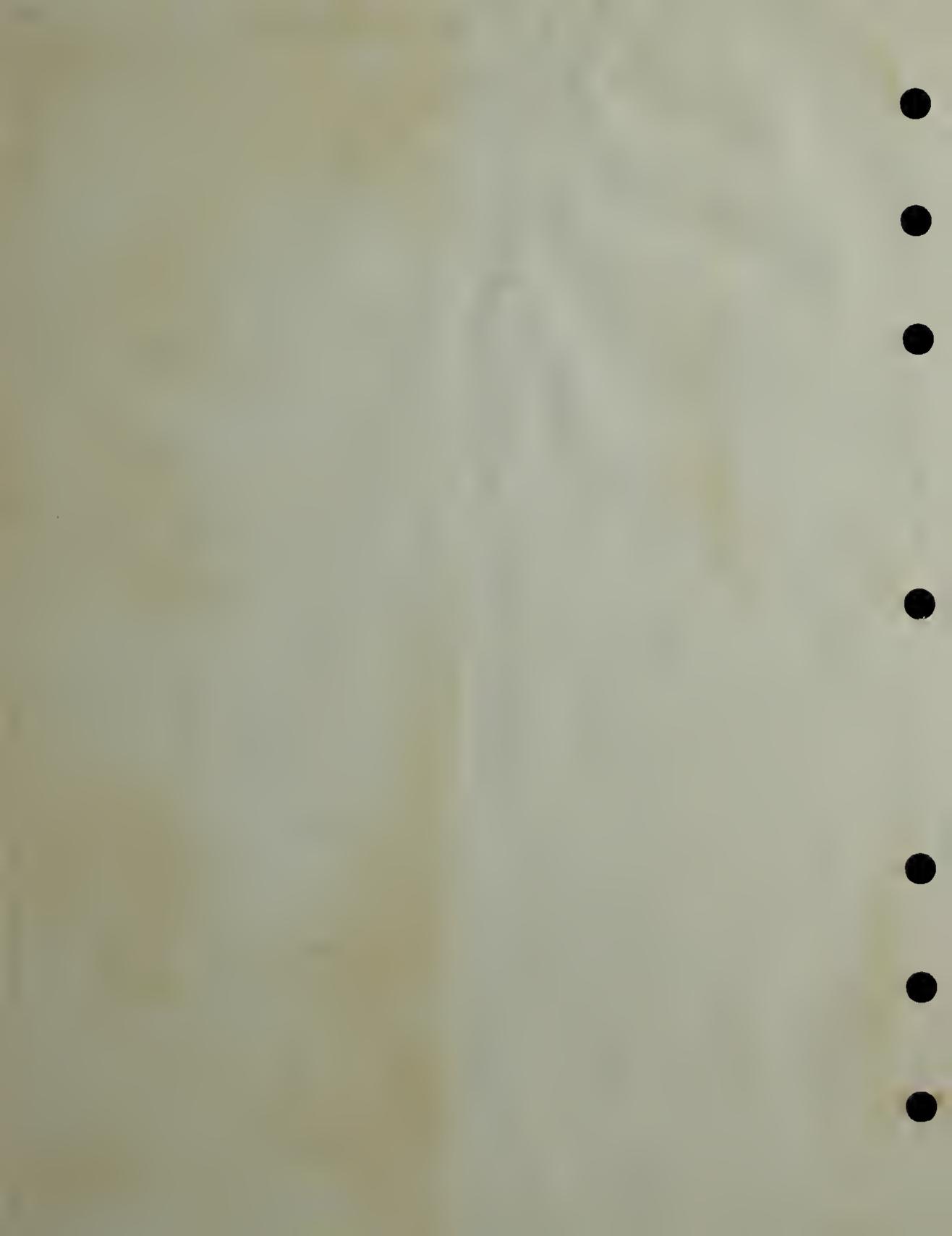
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Figure 4-118. LGC Oscillator, Schematic Diagram

4-5.3.3 Clock Divider Logic Detailed Description. The clock divider logic consists of the main clock divider, ring counter, and strobe pulse generator. The main clock divider (figure 4-119, sheet 1) generates outputs at the basic clock rate of the system, 1.024 mc. In addition, 512 kc outputs drive the ring counter and the time pulse generator. The 2.048 mc CLOCK input from the LGC oscillator is applied to the first main clock divider circuit consisting of gates 37101 through 37106. Gates 37101 through 37104 are interconnected in a manner similar to the basic flip-flop circuit of the LGC. Gates 37105 and 37106 function as a flip-flop; however, gates 37101 through 37104 do not. The waveforms in figure 4-119 indicate that an output occurs from only one of the four gates at each positive and negative transition of the clock input. The other three gates remain in ZERO state. Unlike a flip-flop, in which one side is ZERO while the other side is a ONE and vice-versa, this circuit resembles a ring counter. The outputs of these four gates (37101 through 37104) are used to derive the clear control signal (\overline{CT}), read control signal (\overline{RT}), and the three 1.024 mc gating pulses ($\overline{PHS2}$, $\overline{PHS3}$, and $\overline{PHS4}$) which are 0.25 microseconds wide.

The outputs from gates 37102 and 37103 drive FF37105-37106, which is alternately set and reset at 1.024 mc rate. The write control signal (\overline{WT}) and the 1.024 mc master clock (CLK) signal to the LEM systems are derived from this flip-flop output. Any failure of the LGC oscillator would be most directly indicated by the output of the first main clock divider circuit. Thus, signal Q2A is applied to the oscillator alarm circuit in the power supply to indicate LGC oscillator activity. The output is from an extended NOR gate which has its collector load in the alarm circuit. Figure 4-119 illustrates the timing relationship between the clear and write control signals. The 0.25 microsecond clear pulse is coincident with the first 1/4 microsecond of the 0.5 microsecond write control signal. The read control signal is 0.75 microsecond wide. All three of these control signal outputs are applied to the central processor for clearing, writing into, and reading out of the flip-flop registers. The clear pulse (CT) is used also to derive the overflow strobe signal (\overline{OVFSTB}), a 1.024 mc gating signal. This output is shown wider than the clear pulse since some propagation delay undoubtedly exists to stretch this pulse slightly beyond 0.25 microsecond before FF37148-37149 resets.

The inverted output of gate 37101 drives the second main clock divider circuit which consists of gates 37111 through 37114 and FF37117-37118. Outputs from this circuit drive the ring counter (RING A, RING B) and the time pulse generator (ODDSET, EVNSET). The outputs occur at a 512 kc rate, and are 90 degrees out of phase with each other (see figure 4-119). This main clock divider circuit is identical in operation to the first main clock divider circuit. Each of the gates 37111 through 37114 generates in succession an output on each transition of the output of gate 37107. Output pulses from gates 37112 and 37113 alternately set and reset FF37117-37118. No output signals are derived from this flip-flop. The outputs to drive the ring counter and the time pulse generator are obtained from gates 37111 and 37114. Signals RING A and ODDSET from 37111 occur coincidentally, and RING B and EVNSET from 37114 occur coincidentally. Signal ODDSET, applied to the time pulse generator, can be inhibited by input STOP from priority control, which prevents any outputs from the time pulse generator and subsequently inhibits word flow in the LGC. This feature can be



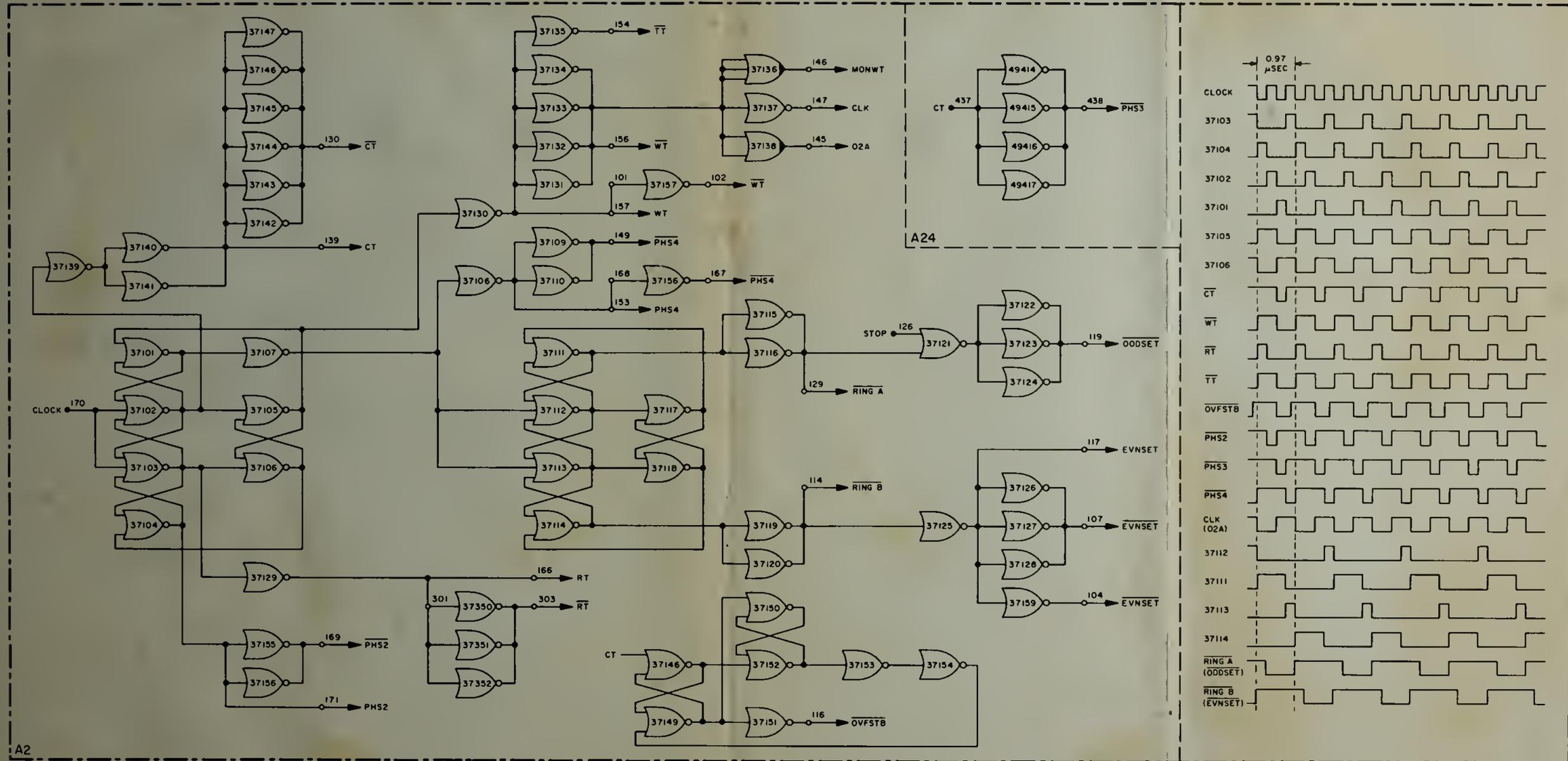
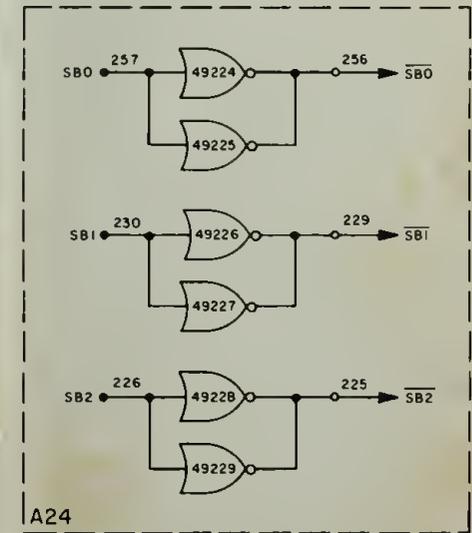
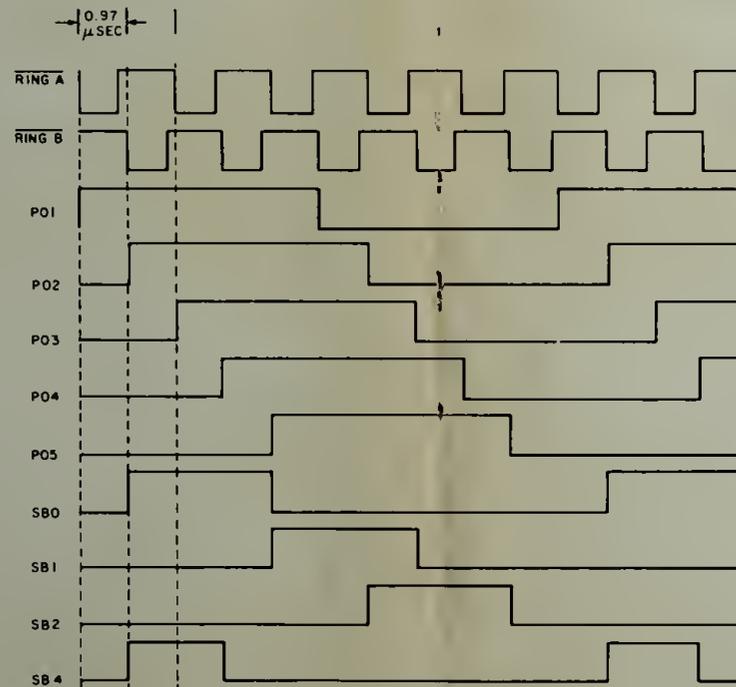
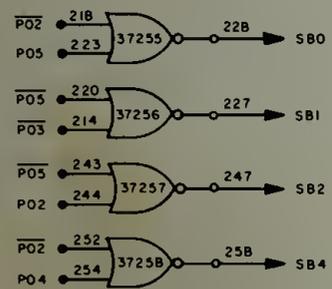
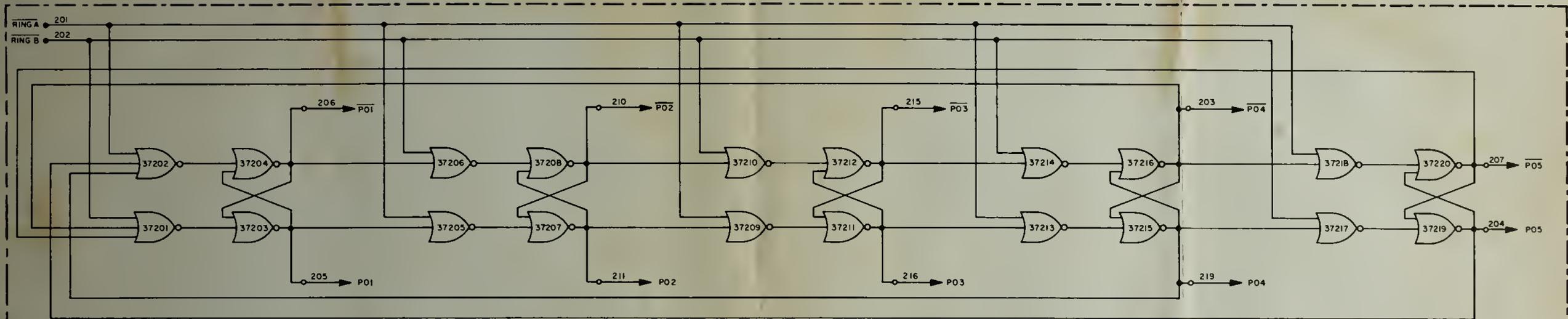


Figure 4-119. Clock Divider Logic
(Sheet 1 of 2)



A24

A2

Figure 4-119. Clock Divider Logic
(Sheet 2 of 2)

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employed during pre-installation system and subsystem tests as a result of a monitor stop (MSTP) input from the CTS.

The ring counter (figure 4-119, sheet 2) consists of five flip-flop circuits with outputs labeled P01 through P05 (and $\overline{P01}$ through $\overline{P05}$). The ring counter is driven by inputs (RING A and $\overline{RING B}$) from the main clock divider. Each of these inputs, described previously, occurs at a 512 kc rate. The ring counter does not accomplish a division-by-two. Rather, the division by the five stages results in five symmetrical outputs, each at a rate of 102.4 kc and 5 microseconds in width. Successive outputs occur 1 microsecond apart; for example, P02 occurs 1 microsecond after P01 etc.

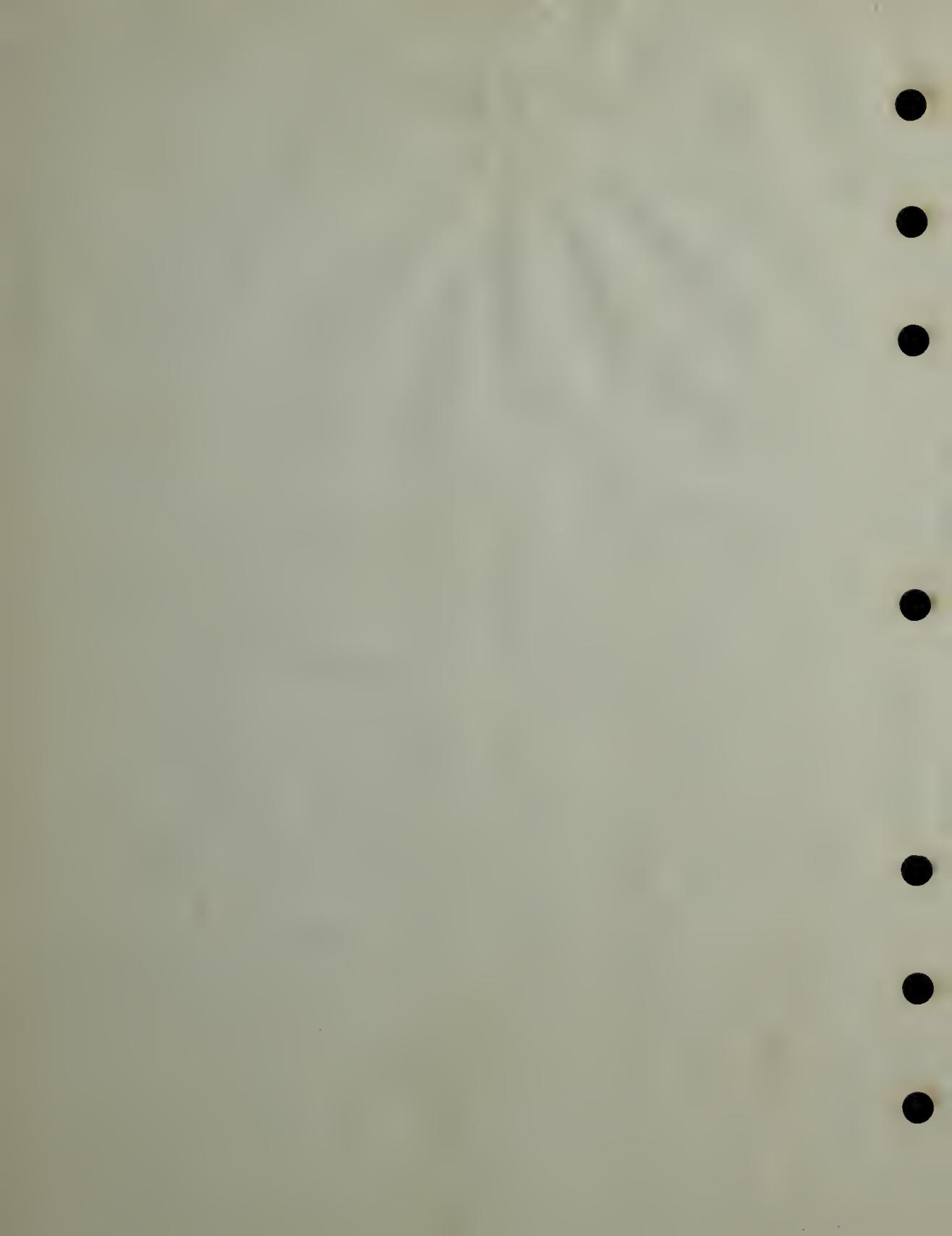
Strobe pulses SB0, SB1, SB2, and SB4 are generated by signals P02 through P05 (and complements) from the ring counter. These strobes are 3 microsecond pulses occurring also at a rate of 102.4 kc, (with the exception of SB4 which is 2 microseconds wide). Strobe signals SB0, SB1, and SB2 are inverted by gates on module A24 (see figure 4-119).

4-5.3.4 Scaler Detailed Description. The scaler, figure 4-120, consists of 33 identical divider stages. The stages are cascaded to provide successive frequency division of the input to the scaler. Stage 2 runs at half the rate of stage 1, stage 3 at half the rate of stage 2, etc. Each of these stages is identical in operation to the main clock divider circuit in the clock divider logic. The input to the scaler, signal $\overline{P01}$ from the ring counter, occurs at a rate of 102.4 kc. It is applied to stage 1 located on module A2 (the remaining stages of the scaler are located on module A1). Stage 1 divides this input by two and generates outputs at a rate of 51.2 kc. There are five outputs available from stage 1: four pulse outputs (F01A through F01D) from the input gates (37221 through 37224), and one flip-flop output (FF37225-37226).

The pulse outputs of stage 1 are 5 microseconds wide. The period of the flip-flop output is approximately 20 microseconds; since the output waveform is symmetrical, the transitions are 10 microseconds apart. The output of the stage 1 flip-flop is the input to stage 2 of the scaler. Stage 2 divides the input by two and generates outputs at a rate of 25.6 kc. Three outputs are available from stage 2: two pulse outputs (F02A, F02B), and the flip-flop output (FS02). The pulse outputs of this stage and all subsequent stages of the scaler, regardless of frequency, are 10 microseconds wide. This width is established by the 10 microsecond input from stage 1 to stage 2 and the fact that a pulse output, not the flip-flop output, feeds stage 3 (F02A). The same is true of the output from stage 3 to stage 4 (F03A) and of the succeeding scaler stages.

Figure 4-121 illustrates the output waveforms from stages 1 and 2 of the scaler. The outputs from stage 2 are typical of the outputs from the remaining stages of the scaler, with the exception of stages 5, 7, and 9. Stages 5 and 9 have one additional pulse output (F05D, F09D) and stage 7 two additional pulse outputs (F07C, F07D). These outputs are generated by gates on module A24 as indicated in figure 4-120.

Most of the pulse outputs designated A and B, which are positive going, are inverted by gates contained in other modules. These gates, and the modules in which they are located, are also illustrated in figure 4-120.



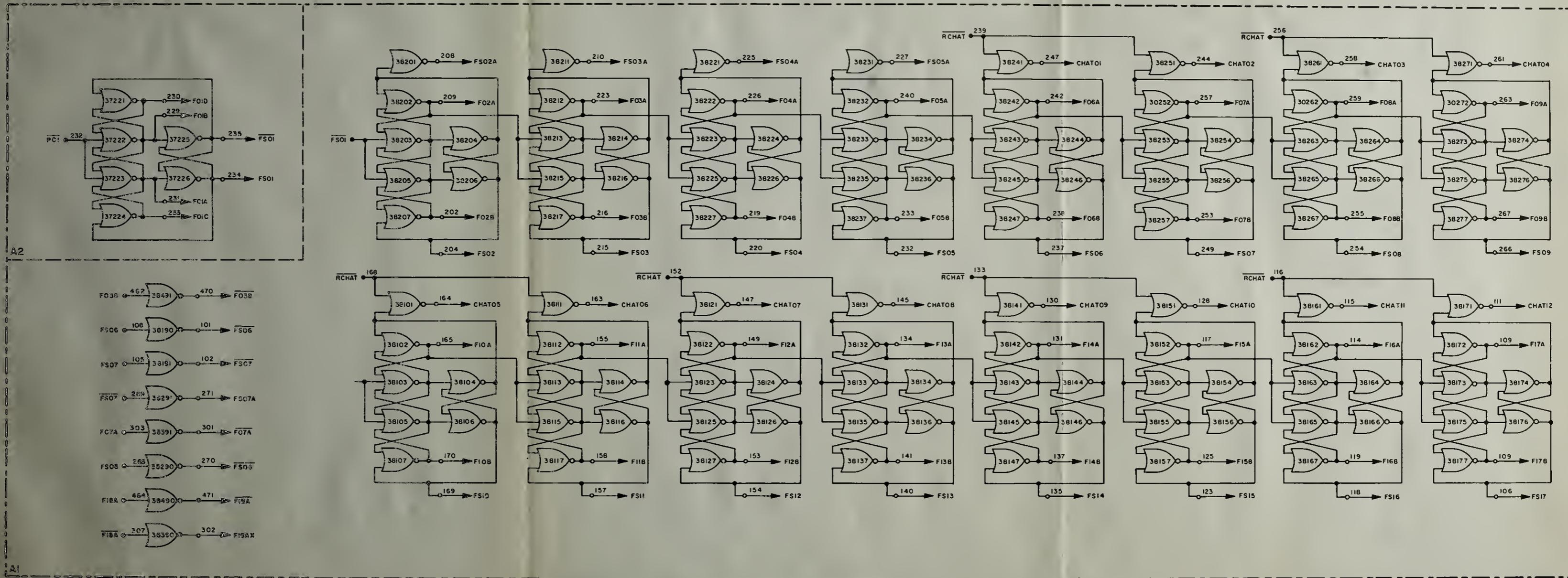
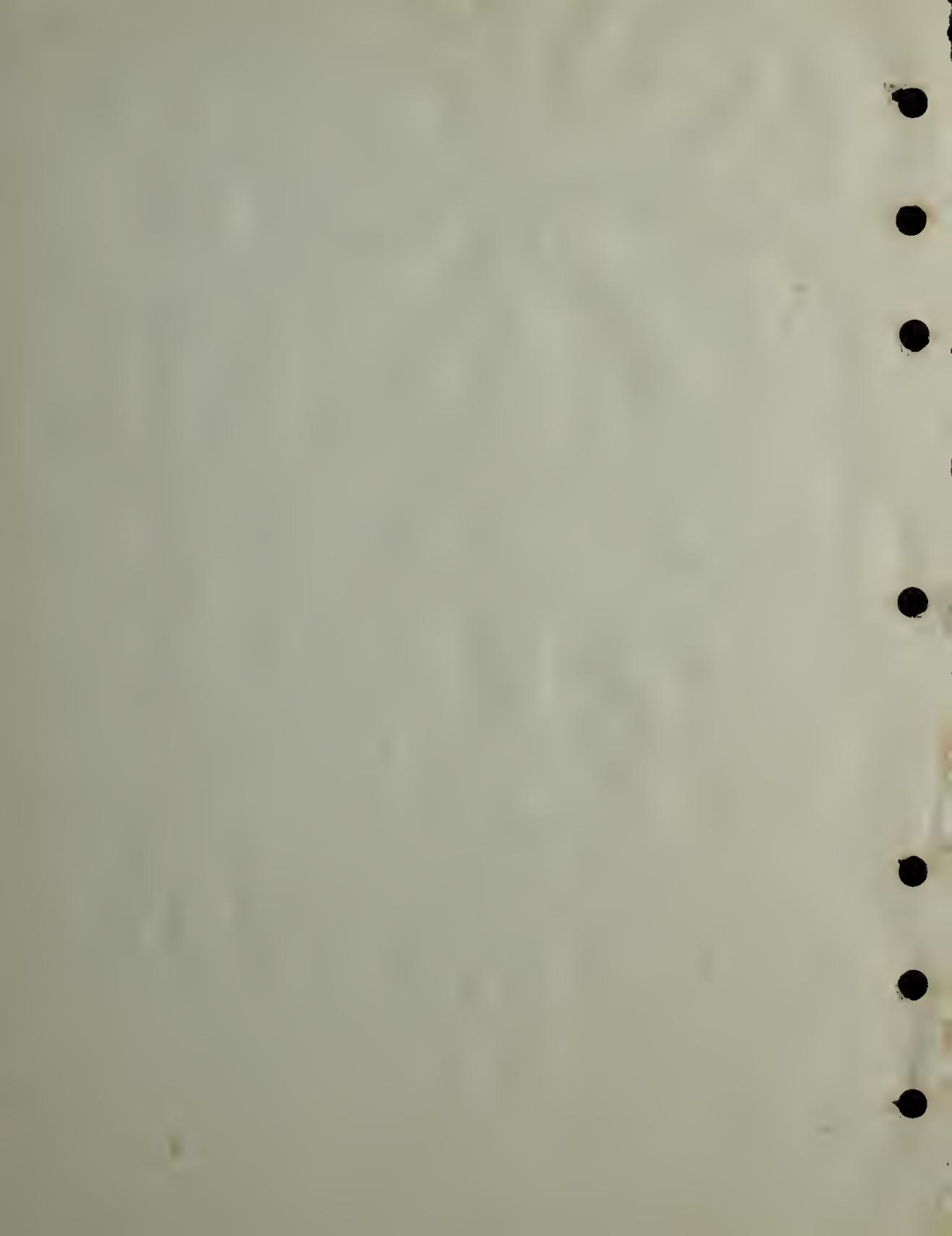


Figure 4-120. Scaler (Sheet 1 of 2)



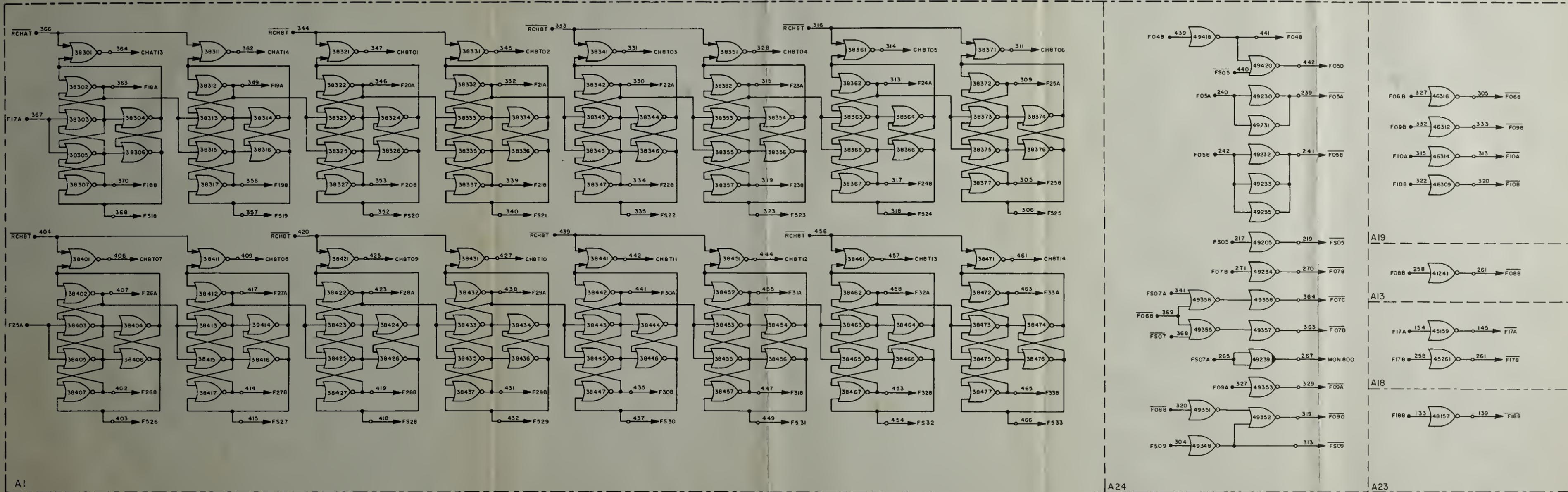
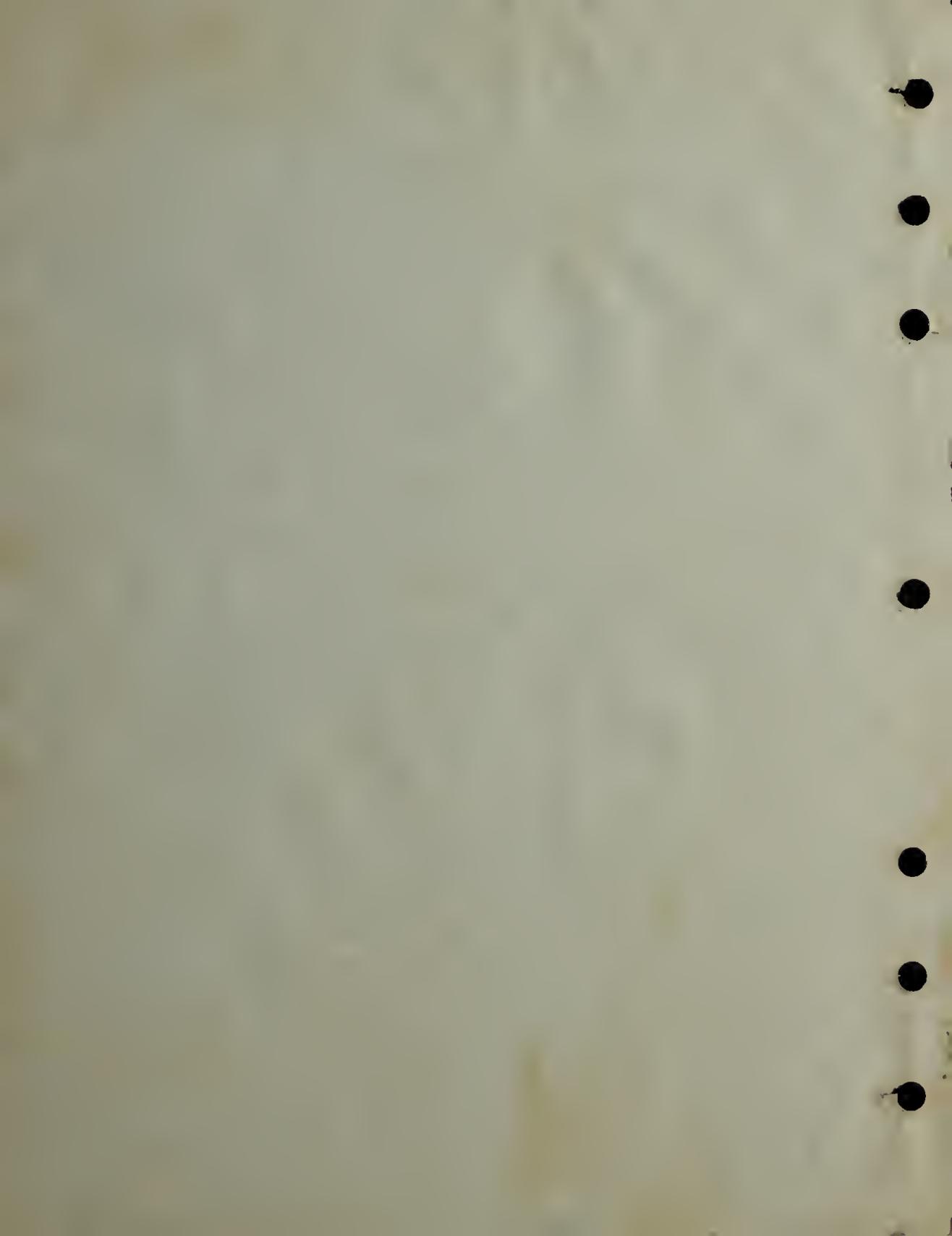
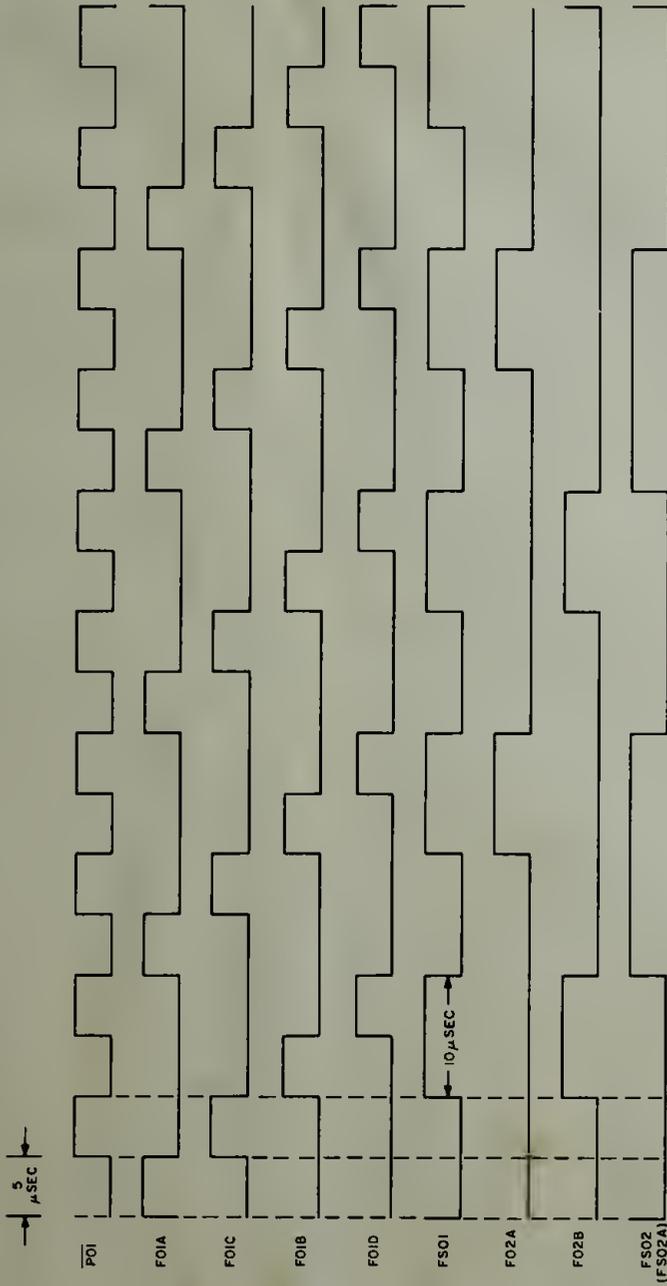


Figure 4-120. Scaler (Sheet 2 of 2)





NOTE: THE OUTPUTS OF STAGE 2 (FSO2,FOZA,FOZB) ARE TYPICAL OF THE OUTPUTS (EXCLUDING FREQUENCY) FROM THE REMAINING STAGES OF THE SCALER.

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Figure 4-121. Scaler Waveforms

The outputs from stages 1 through 17, at rates from 51.2 kpps to 0.78125 pps, are primarily used to derive timing, synchronization, and gating signals for the LGC and other systems. Table 4-VIII lists the frequency, period, and polarity of the outputs of these stages.

The output of stages 6 through 33 provides an indication of real time in the form of two 14 bit words addressable as two channels that are similar to the channels of the input-output section of the LGC. Stages 6 through 19 provide the 14 bit word to the low order channel CHAT01 through CHAT14, while stages 20 through 33 provide the 14 bit word to the high order channel CHBT01 through CHBT14. The two channels together indicate time intervals up to 23.3 hours, in 624 microsecond increments. Both words are formed by the flip-flop outputs of the respective stages, gated by a read channel signal (\overline{RCHAT} or \overline{RCHBT}). Read signal \overline{RCHAT} , generated under program control as a function of octal address 0004, causes the low order bits (stages 6 through 19) to be placed on the write lines in the central processor; read signal \overline{RCHBT} , generated under program control as a function of address 0003, causes the high order bits (stages 20 through 33) to be placed on the write lines.

4-5.3.5 Time Pulse Generator Detailed Description. The time pulse generator, consisting of twelve flip-flop circuits, generates timing pulse outputs $\overline{T01}$ through $\overline{T12}$. This sequence of pulse outputs defines one MCT within the LGC and occupies an interval of exactly 11.97 microseconds, or approximately 12 microseconds. Within this interval, access to memory and word flow take place within the LGC.

Each of the timing pulses is generated by an associated flip-flop circuit shown in figure 4-122. The odd numbered outputs ($\overline{T01}$, etc.) are gated by signal \overline{ODDSET} from the clock divider logic; the even numbered outputs ($\overline{T02}$, etc.) are gated by signal \overline{EVNSET} . Only one pulse output occurs at one time. Consider an initial condition in which signal $\overline{T12 SET}$ is generated. This signal occurs after timing pulses $\overline{T01}$ through $\overline{T11}$ have all been generated. The set output of flip-flops $\overline{T01}$ through $\overline{T11}$ are ORed through gates 37355, 37356, 37357, and 37358. When all these inputs are ZERO, output $\overline{T12 SET}$ is a ONE (coincident with \overline{EVNSET}) and sets the $\overline{T12}$ flip-flop (FF37302-37303). The flip-flop reset output is gated by signal \overline{EVNSET} generating signals $\overline{T12}$ and $\overline{T12}$. Signal $\overline{MT12}$ is made available to the CTS when this unit monitors the LGC during tests. When signal \overline{ODDSET} occurs (0.97 microsecond later), the $\overline{T01}$ flip-flop (FF37305-37306) is set by the output of gate 37304. As this flip-flop sets, the output is fed back to reset the $\overline{T12}$ flip-flop. Simultaneously, signal \overline{ODDSET} gates the flip-flop reset output generating signals $\overline{T01}$ and $\overline{T01}$. Signal \overline{EVNSET} occurs 0.97 microsecond after \overline{ODDSET} and the $\overline{T02}$ flip-flop sets, which in turn resets the $\overline{T01}$ flip-flop.

The remaining timing pulses are generated in this manner except for the $\overline{T12}$ output. Since $\overline{T12}$ is generated as a function of the $\overline{T12 SET}$ signal, there is no feedback from the $\overline{T12}$ flip-flop to reset the $\overline{T11}$ flip-flop. The $\overline{T11}$ flip-flop is set when output $\overline{T10}$ and \overline{ODDSET} are coincident, and reset when signal \overline{EVNSET} is coincident with the set output (now logic ZERO) of the $\overline{T10}$ flip-flop.

Table 4-VIII. Scaler Outputs (Stages 1-17)

Output	Frequency	Period	Pulse Polarity
FS01, $\overline{\text{FS01}}$ F01A, F01B, F01C, F01D	51.2 kpps	19.5 $\mu\text{sec.}$	- Positive
FS02, FS02A F02A, F02B	25.6 kpps	39.0 $\mu\text{sec.}$	- Positive
FS03, FS03A F03A, F03B $\overline{\text{F03B}}$	12.8 kpps	78.0 $\mu\text{sec.}$	- Positive Negative
FS04, FS04A $\overline{\text{F04A}}$, F04B $\overline{\text{F04B}}$	6.4 kpps	156 $\mu\text{sec.}$	- Positive Negative
FS05, $\overline{\text{FS05}}$, FS05A F05A, F05B, F05D $\overline{\text{F05A}}$, $\overline{\text{F05B}}$	3.2 kpps	312 $\mu\text{sec.}$	- Positive Negative
FS06, $\overline{\text{FS06}}$ F06A, F06B $\overline{\text{F06B}}$	1.6 kpps	624 $\mu\text{sec.}$	- Positive Negative
FS07, $\overline{\text{FS07}}$, FS07A F07A, F07B $\overline{\text{F07A}}$, $\overline{\text{F07B}}$, $\overline{\text{F07C}}$, $\overline{\text{F07D}}$	800 pps	1.25 msec.	- Positive Negative
FS08, $\overline{\text{FS08}}$ F08A, F08B $\overline{\text{F08B}}$	400 pps	2.5 msec.	- Positive Negative

(Sheet 1 of 2)

Table 4-VIII. Scaler Outputs (Stages 1-17)

Output	Frequency	Period	Pulse Polarity
FS09, $\overline{\text{FS09}}$ F09A, F09B, F09D $\overline{\text{F09A}}$, $\overline{\text{F09B}}$	200 pps	5.0 msec.	- Positive Negative
FS10 F10A, F10B $\overline{\text{F10A}}$, $\overline{\text{F10B}}$	100 pps	10 msec.	- Positive Negative
FS11 F11A, F11B	50 pps	20.0 msec.	- Positive
FS12 F12A, F12B	25 pps	40.0 msec.	- Positive
FS13 F13A, F13B	12.5 pps	80.0 msec.	- Positive
FS14 F14A, F14B	6.25 pps	160 msec.	- Positive
FS15 F15A, F15B	3.125 pps	320 msec.	- Positive
FS16 F16A, F16B	1.5625 pps	640 msec.	- Positive
FS17 F17A, F17B $\overline{\text{F17A}}$, $\overline{\text{F17B}}$	0.78125 pps	1.3 sec.	- Positive Negative

NOTE: All pulse outputs (F01A, F01B etc.) are 10 μ sec, wide regardless of frequency.

(Sheet 2 of 2)

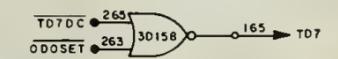
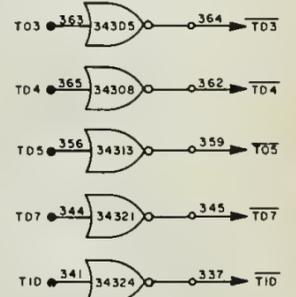
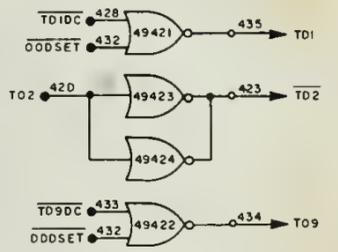
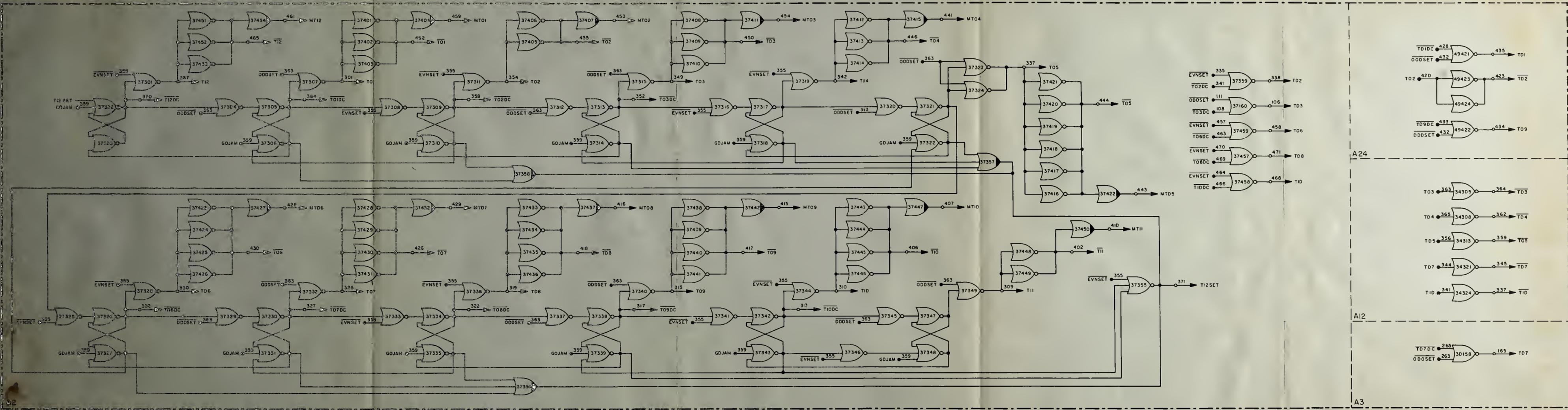
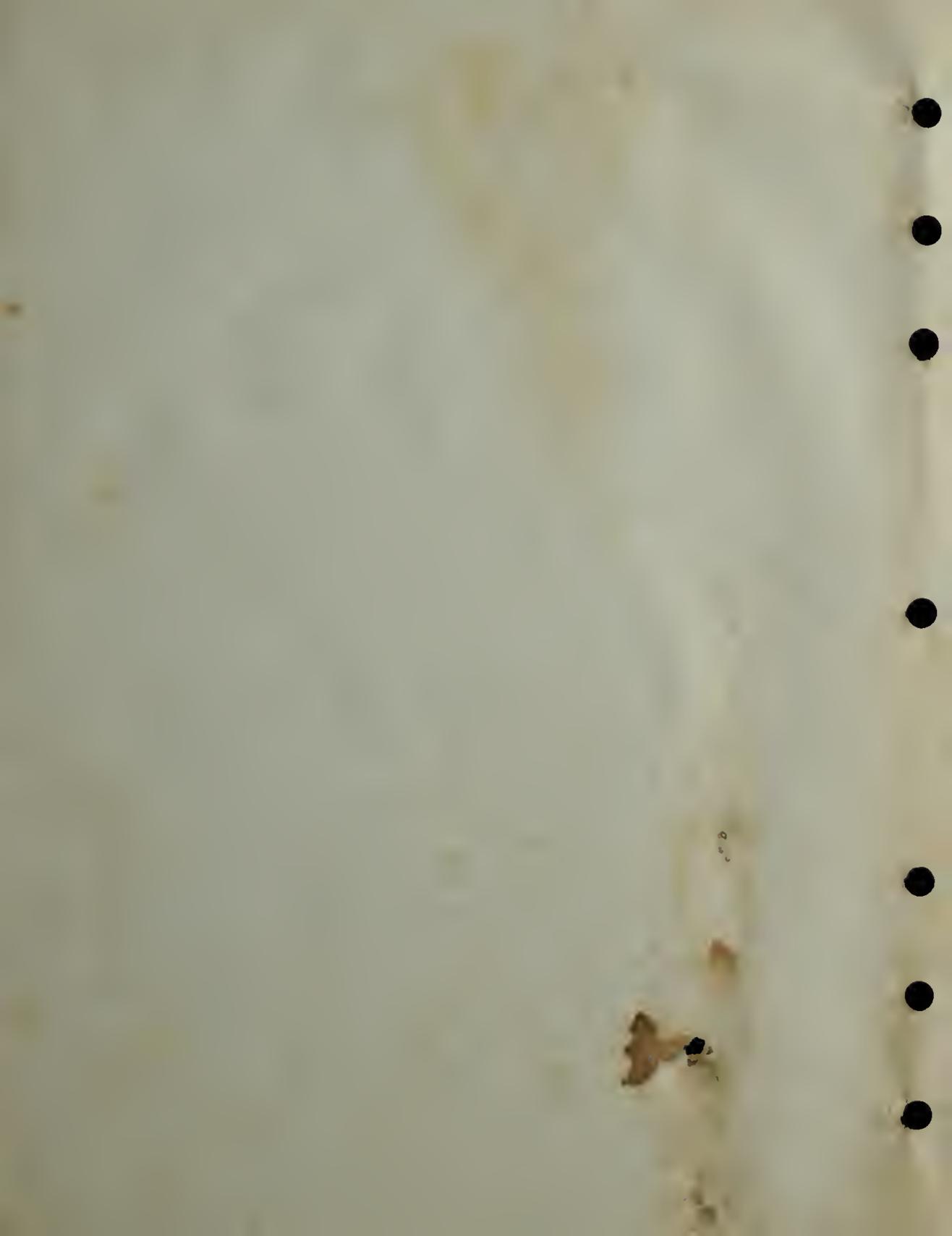


Figure 4-122. Time Pulse Generator Logic



The waveforms for the time pulse generator are shown in figure 4-123. Inputs $\overline{\text{ODDSET}}$ and $\overline{\text{EVNSET}}$ each occur at a 512 kpps rate, but are 90 degrees out of phase with each other. Consequently, even though the driving inputs are 0.75 microsecond wide, the effective drive rate of both inputs combined is twice the rate of the input. The period between each $\overline{\text{ODDSET}}$ and $\overline{\text{EVNSET}}$ pulse is 0.97 microsecond. However, time pulse outputs $\overline{\text{T01}}$ through $\overline{\text{T12}}$ are 0.75 microsecond wide.

Signal GOJAM forces the time pulse generator to indicate T12 time by resetting the T1 through T11 flip-flops, and setting the T12 flip-flop. Forcing the time pulse generator in this manner enables the cycling to be restarted beginning with T01, after a condition occurs which initiated GOJAM.

Additional drive for several of the timing pulse outputs is provided by gates located on modules A2, A3, A12, and A24. These gates are illustrated in figure 4-122. The outputs (for example, T01 from gate 49421 on A24, T02 from gate 37359 on A2, etc.) are in parallel with the outputs developed by the flip-flops on module A2.

4-5.3.6 Sync and Timing Logic. The sync and timing logic, figure 4-124, generates synchronization, timing, and gating pulses for use within the LGC subsystems, and synchronization pulses for systems external to the LGC. These signals are developed as a function of the ring counter, strobe pulse generator, and scaler outputs.

The synchronization outputs to the external systems as well as the LGC oscillator, clock divider logic, and the scaler outputs are generated both during normal operation and during standby. The gates on modules A1, A2, and A24 are controlled so that the supply voltage is uninterrupted when the LGC is switched to standby operation.

4-5.4 SEQUENCE GENERATOR. The sequence generator contains the order code processor, command generator, and control pulse generator. The sequence generator executes the instructions stored in memory by producing control pulses which regulate the data flow in the computer. The manner in which the data flow is regulated among the various functional areas of the computer and between the elements of the central processor causes the data to be processed according to the specifications of each machine instruction.

The order code processor receives signals from the central processor, priority control, and peripheral equipment. The order code signals are stored in the order code processor and converted to coded signals for the command generator. The command generator decodes these signals and produces instruction commands. The instruction commands are sent to the control pulse generator to produce a particular sequence of control pulses depending on the instruction being executed. At the completion of each instruction, the order code signals are sent to the order code processor to continue the execution of the program.

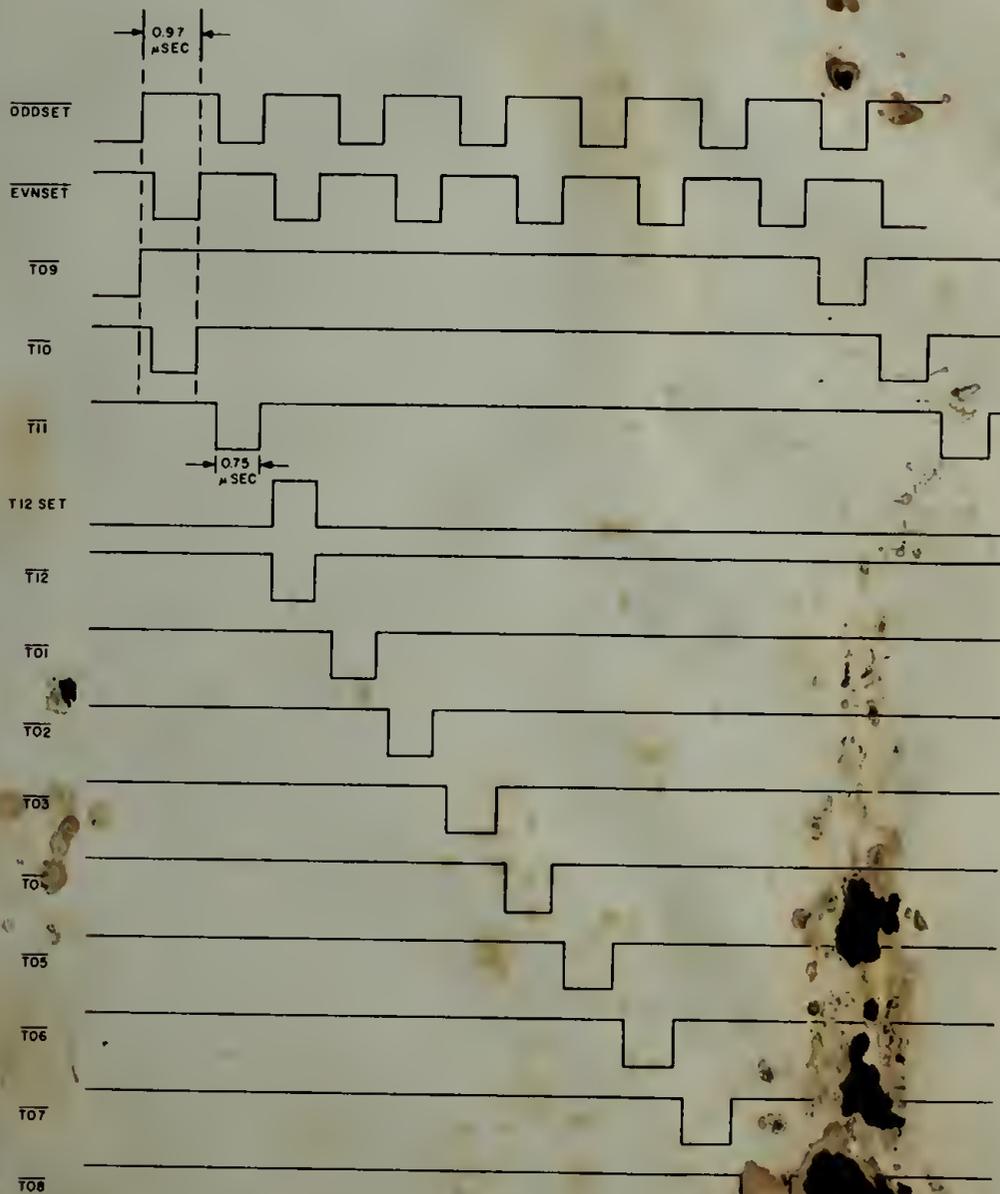


Figure 4-123. Time Pulse Generator Waveforms





