

# Space Shuttle Advanced System/4 Pi Input/Output Processor (IOP)

Principles of Operation for  
PCI/PCO, MSC, and BCE

Prepared for

Rockwell International Corporation  
Space Division  
12214 Lakewood Blvd.  
Downey, CA 90241

26 April 1976

Under Purchase Order No.  
M4J7XMA-483019

IBM No. 6246556A

This submittal includes the following separate  
Principles of Operation documents:

<u>Title</u>
Program-Controlled Inputs & Outputs
Master Sequence Controller
Bus Control Element

**IBM** Federal Systems Division, Owego, New York 13827

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**IBM****CHANGE HISTORY SHEET**

CHANGE NUMBER	SYM	PAGE	REVISION	APPROVED BY	DATE
<u>Part I Program-Controlled Inputs &amp; Outputs</u>					
Class II	A	i&ii	New Page		
Class II	A	iii	Nomenclature Change		
Class II	A	iv	Nomenclature Change		
Class II	A	v	Nomenclature Change		
Class II	A	1	Nomenclature Change		
EDCP-028-1	A	4	Comment Change		
EDCP-028-1	A	6	Comment Deleted		
EDCP-028-2	A	11	Comment Added		
EDCP-028-2 & Class II	A	24	Nomenclature Change		
EDCP-028	A	29	Correct Artwork		
Change Notice #46	A	37	Replace Paragraph		
Class II & EDCP-28-2	A	45	Nomenclature Change		
Class II	A	46	Delete "not"		
<u>Part II Master Sequence Controller</u>					
EDCP-028-1	A	9	Programming Note Added		
Class II	A	11	Paragraph Moved		
Class II	A	20	Nomenclature Change		
Class II	A	24	Nomenclature Change		
EDCP-028-1	A	25	Add Self Test Errors		
Class II	A	38	Nomenclature Change		
Class II	A	39	Nomenclature Change		
Class II	A	57	Nomenclature Change		
Class II	A	58	Nomenclature Change		
EDCP-028	A	59	Nomenclature Change		
EDCP-028	A	62	Nomenclature Change		
EDCP-028	A	63	Nomenclature Change		
EDCP-028	A	67	Nomenclature Change		
EDCP-028	A	70	Artwork Correction		
EDCP-028	A	82	Artwork Correction		
EDCP-028	A	96	Add Note, Add Paragraph, Nomenclature Change		
EDCP-028	A	97	Nomenclature Change		
EDCP-028	A	99	Nomenclature Change		
Class II & EDCP-028	A	101	Nomenclature Change		
Class II & EDCP-028	A	102	Nomenclature Change		
EDCP-028	A	14	Nomenclature Change		
EDCP-028	A	50	Nomenclature Change		
<u>Part III Bus Control Element</u>					
Class II	A	6	Nomenclature Change		
EDCP-028	A	13	Programming Note Added		
EDCP-028	A	20	IBM Manual Number Change, Nomenclature Change		
EDCP-028	A	23	Nomenclature Change		
EDCP-028	A	24	Nomenclature Change		
EDCP-028	A	26	Nomenclature Change		
EDCP-028	A	31	Nomenclature Change		
EDCP-028 & Class II	A	28	Nomenclature Change		
EDCP-028	A	32	Programming Note Added/Deleted		
EDCP-028	A	35	Programming Note Added/Deleted		

NUMBER  
6246556APAGE  
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CHANGE NUMBER	SYM	PAGE	REVISION	APPROVED BY	DATE
<u>Part III continued</u>					
EDCP-	A	37	Programming Note Added/Deleted		
EDCP-028 & Class II	A	38	Paragraph Added, Nomenclature Change		
EDCP-028 & Class II	A	39	Paragraph Moved To Page 40, Nomenclature Change		
EDCP-028	A	41	Artwork Change		
EDCP-028	A	42	Nomenclature Change		
EDCP-028-2	A	44	Three Paragraphs Added		
EDCP-028-2	A	49	Artwork Change		
EDCP-028-1 & Class II	A	50	Programming Note Change, Nomenclature Change		
EDCP-028 1,2,&3	A	52	Programming Note Added, Nomenclature Change		
EDCP-028-2	A	53	Nomenclature Change, Programming Note Added		
EDCP-028 1,2,&3	A	54	#MOUTC Added, Nomenclature Change		
EDCP-028 1,2,&3	A	55	Artwork Change, Nomenclature Change		
EDCP-028	A	56	Nomenclature Change		
EDCP-028	A	57	Artwork Change		
EDCP-028	A	58	Nomenclature Change		
EDCP-028	A	59	Nomenclature Change		
EDCP-028	A	67	Nomenclature Change		
EDCP-028	A	68	Nomenclature Change		
EDCP-028	A	73	Nomenclature Change		
EDCP-028 1,2,3 & Class II	A	74	Note Added, #MINC Added, Nomenclature Change		
EDCP-028	A	75	Nomenclature Change		
EDCP-028	A	76	Nomenclature Change		
EDCP-028	A	78	Nomenclature Change		
EDCP-028-2	A	80	Nomenclature Change		
EDCP-028-2 & Class II	A	85	Paragraph Added, Nomenclature Changes		
Class II	A	88	Page Numbers Change		

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NUM 6246556A  
 PAGE 11

## CONFIGURATION CHART

PRINCIPLES OF OPERATION ISSUE	ECP / PTR	PROGRAM LEVEL
Original 20 December 74		
Revision A 26 April 76	EDCP-028 EDCP-028-1 EDCP-028-2 Change Notice #46	

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TABLE OF CONTENTS

<u>Title</u>	<u>Page</u>
PCI/PCO COMMAND WORD FORMAT-----	2
PCO COMMAND WORD FORMAT SUMMARY-----	4
 PCO FORMATS	
DMA BURST-----	6
BAD PARITY DMA ADDRESS-----	7
BAD PARITY DATA INPUT-----	8
MIA TRANSMITTER-----	9
MIA RECEIVER-----	11
DISCRETE OUTPUT-----	13
CONFIGURE PROCESSORS-----	16
MASTER RESET-----	18
LOAD GO/NO GO TIMER-----	20
LOAD GO/NO GO TIMER TEST-----	21
CONFIGURE TERMINATION CONTROL LATCHES-----	22
LOAD TEST REGISTER-----	23
INTERRUPTS-----	24
RESET STATUS 1 (GO/NO GO)-----	25
LOAD MSC BUSY-----	26
LOAD LOCAL STORE-----	27
TEST DMA 8 MICRO SECOND TIMER-----	29
 PCI FORMATS	
READ MIA TRANSMITTER STATUS-----	30
READ MIA RECEIVER STATUS-----	31
READ DISCRETE OUTPUT STATUS-----	32
READ PROCESSOR HALT STATUS-----	33
READ INTERRUPT REGISTER A-----	34
READ INTERRUPT REGISTER B-----	36
READ INTERRUPT REGISTER C-----	38
READ INTERRUPT REGISTER D-----	39
READ INTERRUPT REGISTER E-----	40
READ RM STATUS REGISTER-----	41
READ DISCRETE INPUT A-----	45
READ DISCRETE INPUTS (33-40)-----	49
READ STATUS 1 (GO/NO GO)-----	50
READ STATUS 4 (BUSY/WAIT)-----	51
READ LOCAL STORE-----	52

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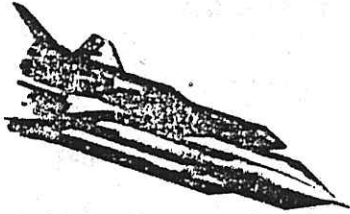
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# SPACE SHUTTLE

## SOFTWARE SYSTEM NOTES

NO.: 556-009  
DATE: 10-25-76  
PAGE 1 OF 2



PROGRAM AFFECTED: Input/Output Programs  
DOCUMENT AFFECTED: Principles of Operation for PCI/PCO, MSC, and BCE (IBM Document #6246556A)  
DISPOSITION: Information and File until Replacement Pages are Issued

If an IOP Master Reset is issued while the IOP is running and doing direct memory accesses (DMA), then an extra DMA is processed after the reset which would result in one of the following operations:

1. Perform write to storage which results in either:
  - An address exception
  - A storage protect violation
  - A modification of unprotected storage
2. Perform read of storage which could result in:
  - An address exception
  - A memory read with no error indication

In addition to the Master Reset, the following additional conditions would also cause the problem:

1. ROS parity error
  2. IOP timing fault
  3. Watchdog timer
  4. Voter fail
- } If termination control  
latches are set

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# SPACE SHUTTLE

## SOFTWARE SYSTEM NOTES

NO.: 556-01

DATE: 10-25-76

PAGE 2 OF 2

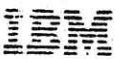


PROGRAM AFFECTED: Input/Output Programs  
DOCUMENT AFFECTED:  
DISPOSITION:

Since the hardware change to eliminate the occurrence of this problem is significant and the frequency of occurrence is low, the Principles of Operation Manual will be updated to state that:

"Prior to issuing a Master Reset PCO, all processors should be halted using the Configure Processors PCO".

There have been no reported instances of this problem so there may not be any impact to the existing software design. However, there may be future designs which could encounter this problem. It is recommended that Rockwell and IBM Houston consider issuing a DPDGRAM or Software Awareness Memo to the appropriate organizations.



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# SPACE SHUTTLE

## SOFTWARE SYSTEM NOTES

NO.: 556-010  
DATE: 11-22-76



PROGRAM AFFECTED: IOP Programming  
DOCUMENT AFFECTED: Principles of Operation for BCE, IBM No. 6246556A  
DISPOSITION: Information and file.

### BCE Listen Mode Operations - Timing Analysis

The purpose of this note is to illustrate the analysis required to establish the time relationships between the commander and the listener for a sample case.

#### COMMANDER PROGRAM

#### LISTENER PROGRAM

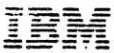
EVENC	#CMDI	LSN, CMD	EVENL	#WIX	TABLE
	#DLYI	0 (For alignment)		:	
	#DLYI	N	ODD	#LTOI	TIME
	#MOUT	DISPL, TWDS		#RDLI	RWDS
	#MOUTC	IUA, CMND		#VAT	0
	#WAT	0		:	
				:	
N	EQU		TABLE	DC	ODD

Note: The labels EVEN and ODD denote that the address is even or odd.

In this sample analysis, DMA activity is assumed to be below the level that would interfere with the process; in actual operational software, a careful analysis of DMA activity is a continuing part of program design.

LISTEN SEQUENCE: Time from recognition of the listen command by the #WIX instruction to acquisition of the BTU command by the #RDLI instruction

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INSTRUCTION	MICRO-INSTRUCTIONS EXECUTED	
	Short loop	Long loop
#MIX	7	0
#LTOI	2	2
#RDLI	3	3
	12 (181.5 usec)	14 (214.5 usec)

The long loop occurs when the MIX just misses detecting the listen command.

COMMAND SEQUENCE: Time from the placement of the last bit of the listen command on the bus to the placement of the last bit of the BTU command on the bus.

INSTRUCTION	MICRO-INSTRUCTIONS EXECUTED	
#CMDI	-	Command transmission is completed at about the second micro in the DLYI 0.
#DLYI 0	2	(N = 0)
#DLYI N	2	(Command transmission is initiated in fourth micro)
#MOUT	4	Command transmission is completed at about the time the first data word transmission starts
Transmission Time	1-2	
Command Available	2	
	11-12	(165.0-181.5 usec)

DELAY COMPUTATION: The calculation of the delay must be based on the listener's long loop and the time that the unit command is available to the listener -

$$N = 14 - 11 = 3$$

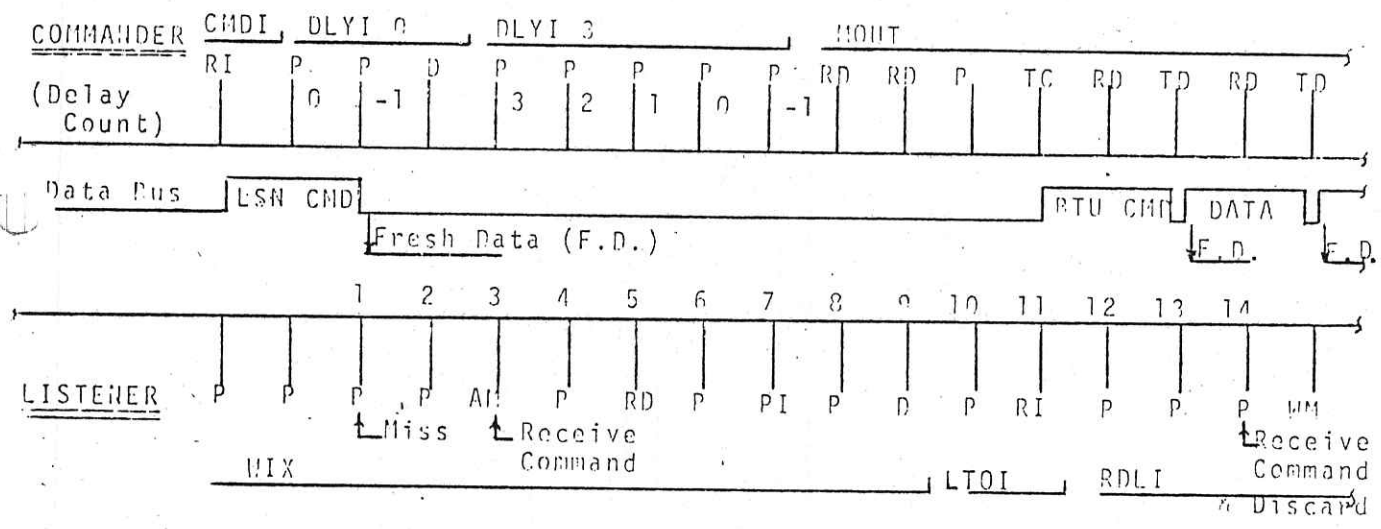
This establishes the DLYI N at 5 cycles, the total command sequence at 14 cycles (214.5 usec) and meets the needs of the listener's long and short loop timing.

DETERMINATION OF INSTRUCTION CYCLE FACTORS: The number of cycles used for each instruction in the sequences above were obtained from references (C) and (D). Reference (A) contains a detailed description

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of bus read/write operations, including a table for "time to first look at data" and a section on listen mode operations. Reference (B) contains some analysis of BCE delay factors for ICC programs. Reference (E) contains detailed descriptions of the micro-orders used in all instructions.

TIME LINE USED IN ANALYSIS: The time line below illustrates the Listen and Command sequences used in this analysis. Note that the "Fresh Data" condition can occur between 1 and 5 microseconds after the trailing edge of the incoming word. This variation will affect the receiving BCE's processing sequence, but will not impact the data transfer.



Definitions for the micro-instruction function symbols:

- AM - Accept MIA data
- D - Decode instruction
- P - Process
- PI - Prefetch Instruction
- RD - Read Data (from storage)
- RI - Request Instruction
- TC - Transmit Command
- TD - Transmit Data
- WI - Wait for MIA data

- Reference:
- (A) Principles of Operation for BCE (IBM No. 6246556A, 26 April 1976)
  - (B) Presentation by L. Killingbeck (IBM) at SD on 7 February 1975
  - (C) Principles of Operation for (Shuttle) Data Processing Subsystem (SD-74-SII-0230R, Sept. 1975) as amended by Change Packages 1, 2, and 3.
  - (D) Shuttle IOP Microcode CLD's (IBM No. 6246008, 16 December 1975)
  - (E) Principles of Operation for IOP Micro-Architecture (IBM, April 1975)

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# SPACE SHUTTLE

## SOFTWARE SYSTEM NOTES

NO.: 556-013  
DATE: 11/27/78



PROGRAM AFFECTED: General Programming Information  
DOCUMENT AFFECTED: Space Shuttle Advanced System 4 Pi IOP (6246556A)  
DISPOSITION: Information and File

In part II - Master Sequence Controller Page 13 of the subject document, the discrete outputs are numbered from one (1) to thirty two (32). The Rockwell International specification MC615-0001 revision D indicates that the thirty-two discrete outputs shall be numbered zero (0) through thirty-one (31). Therefore, Bit 0 through 31 for the PCO, Discrete Output Reset and Discrete Output Set shall be directly related to discrete outputs 0 through 31.

Also, in the same section of the Principles of Operation on Pages 45-49, the same type problem exists with the discrete inputs. They are numbered one (1) through forty (40) and should be numbered zero (0) through thirty-nine (39) as per the Rockwell specification.

The Read Discrete Input A on Page 45 should be ammended so as to read Discrete Input 0 using Bit 0 of the instruction and continuing that sequence through Discrete Input 31.

Read Discrete Inputs on Page 49 should again be renumbered 32 through 39 instead of 33 through 40.

The Automated Logic Drawings (ALD's) have been updated to agree with the nomenclature specified by the MC615-0001 document. In addition, the IOP Cabling Flight & Prototype Model for Space Shuttle document shall be updated to agree with the ALD's and Rockwell specification.

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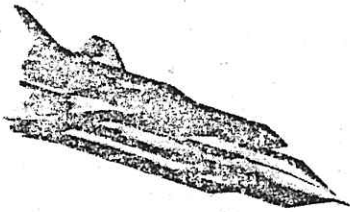
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# SPACE SHUTTLE

## SOFTWARE SYSTEM NOTES

NO.: 556-011

DATE: 1-5-77



PROGRAM AFFECTED: IOP Programming  
 DOCUMENT AFFECTED: Principles of Operation for BCE, IBM No. 6246556A  
 DISPOSITION: Information and File

There is a timing condition in the IOP instruction Wait for Index (WIX) which needs to be corrected in software by inserting a delay between output instructions. This problem was discovered in the SDL (See Discrepancy Report #551) early in November when a Listen Mode BCE missed a poll word which caused a failure to synchronize in a dual string configuration.

There is no change planned to correct this anomaly via a hardware or microcode change to the IOP. The software workaround consists of inserting a delay (33 microseconds) between output instructions (CMD, CMDI, MOUT, TDS, TDL) and the synchronization listen command. For example:

	#CMDI	(Output)
	#BU LISTEN	(Delay)
LISTEN	#CMDI	(Listen Command)

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PART I

**Space Shuttle Advanced System/4 Pi  
Input/Output Processor (IOP)**

**Principles of Operation for  
Program-Controlled Inputs & Outputs**

Prepared for

Rockwell International Corporation  
Space Division  
12214 Lakewood Blvd.  
Downey, CA 90241

26 April 1976

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PCI/PCO PRINCIPLES OF OPERATION

(PRODUCTION MODELS)

This document identifies the specific Program Controlled Input and Output commands available to the Space Shuttle AP101 computer user.

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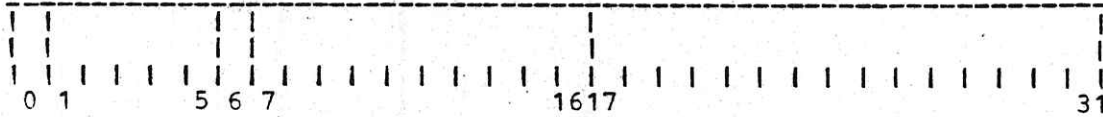
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## PCI/PCO COMMAND WORD FORMAT



## BIT 0; COMMAND ID FIELD

1 = Program Controlled Output (CPU Output)  
 0 = Program Controlled Input (CPU Input)

## BITS 1 Through 5; DEVICE SELECT FIELD

0 0 0 0 1 = Control/Monitor (CM)  
 0 0 0 1 0 = Redundancy Management (RM)  
 0 0 1 0 0 = Data Flow (DF)  
 0 1 0 0 0 = Local Store (LS)  
 1 0 0 0 0 = Channel Control (CC)

## BIT 6; HANDSHAKE CONTROL FIELD

0 = No handshake required  
 1 = Handshake required

## BIT 7 through 16; DATA SELECT FIELD

(See Separate section)

BITS 17 through 31; NOT USED.

## NOTES:

1. The five-bit Device Select Field must contain only the bit specified in the format description for the desired device selected. Additional bits will cause the PCI/PCO data word to be written to all the devices designated with associated loss of IOP control. No attempts to use the hardware configuration should be made since driving circuits are not sized to drive multiple loads and will not operate reliably.

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- 2. Handshaking for a PCI/PCO is required for several operations to allow the device selected to complete an operation before the PCI/PCO command function is implemented. The added operation is accomplished by the IOP and requires no special programming of the GPC. The handshaking operation prevents loss of control of the IOP software because of possible configuration changes during the PCI/PCO implementation.

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## PCO COMMAND WORD FORMAT SUMMARY

1	1000	0010	0000	1000	DMA BURST ENABLE
1	1000	0000	0000	1000	DMA BURST INHIBIT
1	1000	0010	0010	0000	ENABLE BAD PARITY DMA ADDR
1	1000	0010	0100	0000	ENABLE BAD PARITY DATA IN
1	1000	0000	0010	0000	DISABLE BAD PARITY DMA ADDR
1	1000	0000	0100	0000	DISABLE BAD PARITY DATA IN
1	0000	1010	0000	1000	MIA XMTR ENABLE
1	0000	1000	0000	1000	MIA XMTR DISABLE
1	0000	1010	0001	0000	MIA RCVR ENABLE
1	0000	1000	0001	0000	MIA RCVR DISABLE
1	0000	1010	0010	0000	DISCRETE OUTPUT SET
1	0000	1000	0010	0000	DISCRETE OUTPUT RESET
1	0000	1100	0100	0000	PROCESSOR HALT
1	0000	1110	0100	0000	PROCESSOR ENABLE
1	0000	1000	1000	0000	MASTER RESET
1	0001	0000	0000	1000	LOAD GO/NO-GO TIMER
1	0001	0000	0000	1001	TEST GO/NO-GO TIMER
1	0001	0000	0001	0000	TERM.LATCH CONTROL
1	0001	0000	0010	0000	LOAD TEST REGISTER
1	0001	0000	0010	1000	ENABLE INTERRUPTS
1	0001	0000	0011	0000	TEST ALL INTERRUPTS
1	0010	0100	0000	0000	RESET STATUS 1 (GO/NO-GO)
1	0010	0100	0000	1000	LOAD MSC BUSY
				(SEE WITHIN)	LOAD LOCAL STORE
1	1000	0010	0000	0001	TEST DMA TIMER*

\* NOT APPLICABLE TO PROTOTYPES AND CREW TRAINERS

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PCI COMMAND WORD FORMAT SUMMARY (cont.)

0	0000	1000	0000	0000	MIA XMTR STATUS
0	0000	1000	0000	1000	MIA RCVR STATUS
0	0000	1000	0001	0000	READ DISC.OUTPUT STATUS
0	0000	1000	0001	1000	PROCESSOR HALT STATUS
0	0001	0000	0000	0000	INTERRUPT REG. A
0	0001	0000	0000	1000	INTERRUPT REG. B
0	0001	0000	0001	0000	INTERRUPT REG. C
0	0001	0000	0001	1000	INTERRUPT REG. D
0	0001	0000	0010	0000	INTERRUPT REG. E
0	0001	0000	0010	1000	RM STATUS REG
0	0001	0000	0011	0000	D.I. A (1-32)
0	0001	0000	0011	1000	D.I. B (33-40)
0	0010	0000	0000	0000	READ STATUS 1 (GO/NO-GO)
0	0010	0000	0000	1000	READ STATUS 4 (B/W)
				(SEE WITHIN)	READ LOCAL STORE

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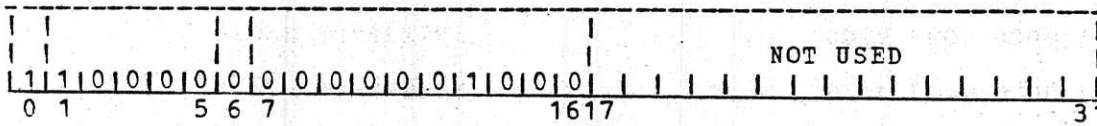
PCO FORMATS

DMA BURST

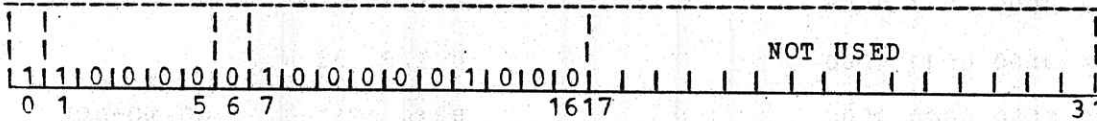
COMMAND WORD

<u>FUNCTION</u>	<u>OCTAL</u>	<u>HEX</u>	<u>DEVICE</u>
DMA BURST INHIBIT	30001000000	C0040000	CC
ENABLE	30101000000	C1040000	

INHIBIT



ENABLE



DATA WORD

BITS

0                   NOT USED.   THESE PCO REQUIRE NO DATA WORD.  
 1                                   .  
 .                                   .  
 .                                   .  
 .                                   .  
 31                                  .

These command words provide control of the Direct Memory Access capability to CPU main memory. When inhibited, the IOP will not access memory using Burst Mode. The commands are provided to allow CPU control of memory operations.

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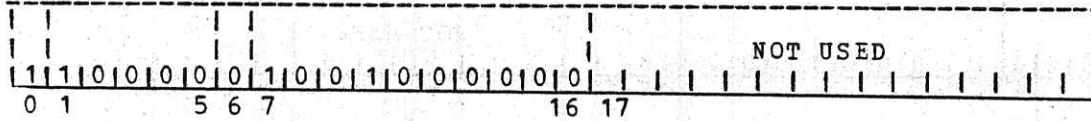
PCO FORMATS

BAD PARITY DATA INPUT

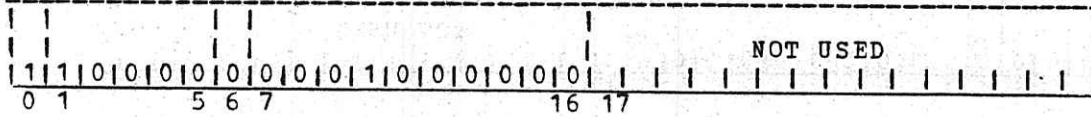
COMMAND WORD

<u>FUNCTION</u>	<u>OCTAL</u>	<u>HEX</u>	<u>DEVICE</u>
BAD PARITY DATA INPUT ENABLE	3011000000	C1200000	CC
BAD PARITY DATA INPUT DISABLE	3001000000	C0200000	CC

ENABLE



DISABLE



DATA WORD

BITS

0 NOT USED. THESE PCO REQUIRE NO DATA WORD.  
.  
.  
.  
31

The Enable command forces the IOP to generate bad parity (even) on data words transferred to the CPU. It also forces the parity on DMA addresses to return to normal (odd) parity. Bad parity may not be generated for both address and data at the same time in a properly operating IOP. This command is part of a set that permits self testing of the GPC.

The Disable command returns the IOP to normal (odd) parity generation.

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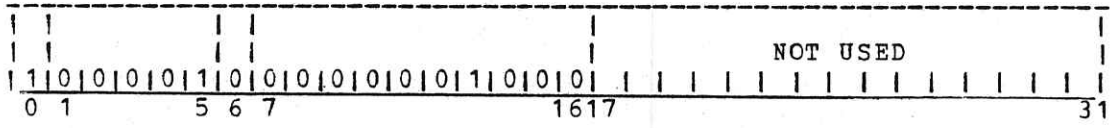
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PCO FORMAT  
MIA TRANSMITTER

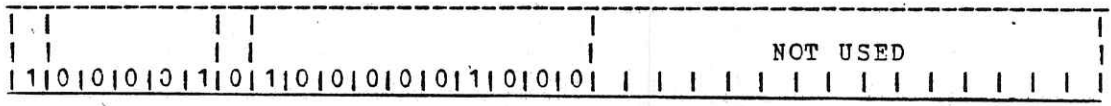
COMMAND WORD

<u>FUNCTION</u>	<u>OCTAL</u>	<u>HEX</u>	<u>DEVICE</u>
MIA TRANSMITTER DISABLE	20401000000	84040000	C/M
ENABLE	20501000000	85040000	

DISABLE



ENABLE



DATA WORD

- 0 = No change of condition. Hardware does not respond.
- 1 = Enable individual MIA transmitter if command word was enable.
- 1 = Disable individual MIA transmitter if command word was disable.

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These words are to control individual MIA transmitters to provide IOP output control of system data buses. The data word is used as a mask for configuring MIA transmitters.

BIT

- 0 NOT USED.
- 1 CHANNEL NO. 1 MIA TRANSMITTER
- .
- .
- 24 CHANNEL NO. 24 MIA TRANSMITTER
- 25 NOT PRESENTLY USED. EXPANSION CAPABILITY
- .
- .
- 31

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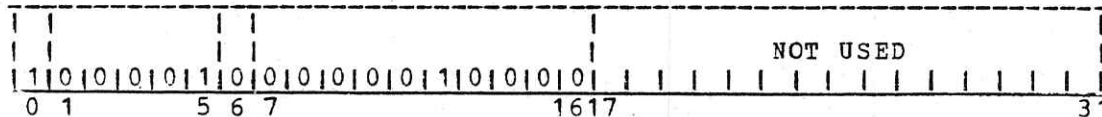
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PCO FORMAT  
MIA RECEIVER

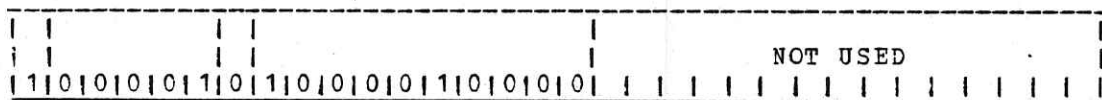
COMMAND WORD

<u>FUNCTION</u>	<u>OCTAL</u>	<u>HEX</u>	<u>DEVICE</u>
MIA RECEIVER DISABLE	2040200000	84080000	C/M
ENABLE	2050200000	85080000	

DISABLE



ENABLE



DATA WORD

<u>BIT</u>	
0	NOT USED. BIT IGNORED
1	CHANNEL NO. 1 MIA RECEIVER
2	CHANNEL NO. 2 MIA RECEIVER
.	.
.	.
23	No.23
24	No.24
25	NOT PRESENTLY USED. BITS IGNORED
.	.
.	.
31	.

- 0 = No Change of status
- 1 = Enable receiver if with enable command\*
- 1 = Disable receiver if with disable command word

\*Should only be used when the associated BCE is in the Halt State.

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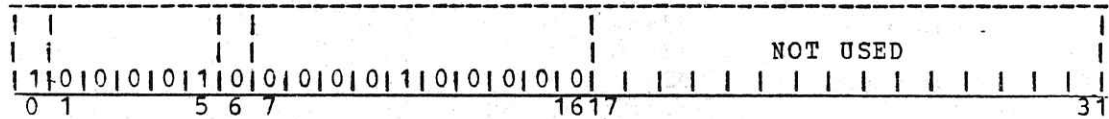


PCO FORMAT  
DISCRETE OUTPUT

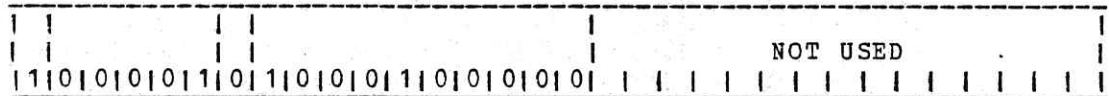
COMMAND WORD

<u>FUNCTION</u>	<u>OCTAL</u>	<u>HEX</u>	<u>DEVICE</u>
DISCRETE OUTPUT RESET	20404000000	84100000	C/M
SET	20504000000	85100000	

RESET



SET



DATA WORD

- \* = Hardwired to IOP internal circuitry. These DO's are not available for software use.
- 0 = No change
- 1 = Set discrete bit if command word is set.
- 1 = Reset discrete bit if command word is reset.

The data word is used as a mask to control the discrete outputs. The discrete outputs are configured as differential drivers. The pin connections to the IOP are indicated for the true (T) and complement (C) outputs.

<u>BIT</u>			
0	(D0-1)	T	J3-51
		C	J3-63
1	(D0-2)	T	J3-18
		C	J3-29
2	(D0-3)	T	J3-28
		C	J3-40
3	(D0-4)	T	J3-30

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4	(D0-5)	C	J3-19
		E	J3-41
		C	J3-52
5	(D0-6)	F	J3-59
		C	J3-60
6	(D0-7)	H	J3-49
		C	J3-50
7	(D0-8)	F	J3-36
		C	J3-48
8	(D0-9)	H	J3-62
		C	J3-61
9	(D0-10)	F	J3-25
		C	J3-37
10	(D0-11)	H	J3-15
		C	J3-26
11	(D0-12)	F	J3-38
		C	J3-39
12	(D0-13)	H	J3-8
		C	J3-16
13	(D0-14)	F	J3-17
		C	J3-27
14	(D0-15)	H	J3-1
		C	J3-2
15	(D0-16)	F	J3-3
		C	J3-9
16	(D0-17)	H	J3-4
		C	J3-10
17	(D0-18)	F	J3-11
		C	J3-5
18	(D0-19)	H	J3-12
		C	J3-6
19	(D0-20)	F	J3-7
		C	J3-13
20	(D0-21)	H	J3-44
		C	J3-43
21	(D0-22)	F	J3-22
		C	J3-14
22	(D0-23)	H	J3-45
		C	J3-33
23	(D0-24)	F	J3-24
		C	J3-23
24	(D0-25)	H	J3-34
		C	J3-35
25	(D0-26)	F	J3-56
		C	J3-55
26	(D0-27)	H	J3-21
		C	J3-32
27	(D0-28)	F	J3-20
		C	J3-31
28	(D0-29)	H	J3-46
		C	J3-47
29	(D0-30)	F	J3-42

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		C	J3-53
* 30	GPC ID (D0-31)	T	J3-58
		C	J3-57

This bit is hardwired to a positive output source and will provide a source voltage for GPC identification in the system.

* 31	IPL (D0-32)	T	J3-68
		C	J3-67

This bit when set (1) indicates that the IPL routine is in progress. When reset (0), the bit indicates that the IPL routine has not been requested or that it is complete depending upon the time/event sequence.

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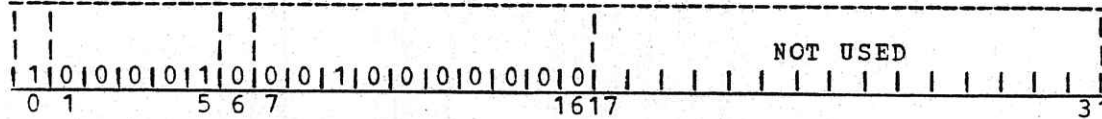
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PCO FORMAT  
 MASTER RESET

COMMAND WORD

<u>FUNCTION</u>	<u>OCTAL</u>	<u>HEX</u>	<u>DEVICE</u>
MASTER RESET	2042000000	84400000	C/M



DATA WORD

There is no data word associated with this command word. The following table indicates the hardware reset by this command word and the resulting condition.

<u>REGISTER</u>	<u>MASTER RESET FUNCTION</u>
STAT1 (GO/NOGO)	RST=GO
STAT4 (BUSY/WAIT)	RST-WAIT
STAT5 (HALT/NO HALT)	RST=HALT MSC/BCE
XMIT ENABLE	RST=DISABLE
RCVR ENABLE	RST-DISABLE
CHANNEL	NO CHANGE
FAIL VOTE	RST=NO FAIL
TERMINATE CONTROL LATCHES	RST=NO TERMINATION
VOTER TEST	RST=OPERATIONAL DATA
FAIL LATCH	NO CHANGE
TIME OUT LATCH	NO CHANGE
DISCRETE OUTPUTS	RST=INACTIVE

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INTERRUPT  
-C/M IDLE  
-IOP FAIL LTCH  
-TIME OUT LTCH  
-ROS PAR  
-IOP FAULT  
-ALL OTHERS

SET  
NO CHANGE  
NO CHANGE  
RESET  
RESET  
RESET

WATCHDOG TIMER

RST=ZERO COUNTER AND  
INHIBIT COUNTING

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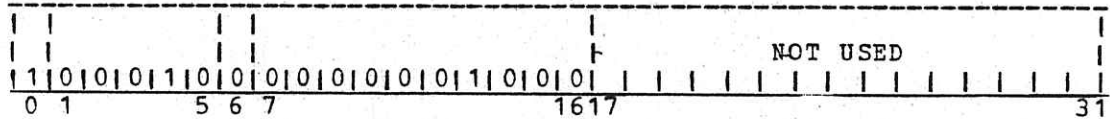
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PCO FORMAT  
LOAD GO/NO-GO TIMER

COMMAND WORD

<u>FUNCTION</u>	<u>OCTAL</u>	<u>HEX</u>	<u>DEVICE</u>
LOAD GO/NO-GO TIMER	21001000000	88040000	RM



DATA WORD

<u>BIT</u>	
0	NOT USED. BITS IF SET ARE IGNORED.
.	.
.	.
19	.
20	GO/NO-GO TIMER BIT 0 MSB
21	1
22	2
23	3
24	4
25	5
26	6
27	7
28	8
29	9
30	10
31	11 LSB = 0.768 msec.

Data word used to load the Go/NO-GO timer in normal system operation. The timer scaling permits 3.145728 seconds maximum to timeout. Timeout sets a timeout latch which is used to drive the Computer Fail output and reset the IOP if the transmission termination logic has been activated. See PCO "CONFIGURE TERMINATION CONTROL LATCHES." Once the timer has been reset, the counter will not operate until loaded via this PCO.

The timer is a countup device. The data loaded must be the twos complement of the desired time. The leading bit positions are ignored and may be set as a result of the complement operation if desired. A data word of all zeros causes an interrupt after a full count (3.145728 sec).

Programming Note: This PCO also resets the Timeout Latch.

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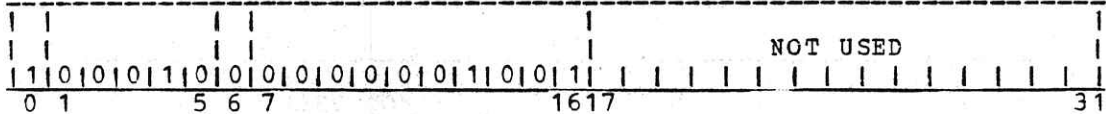
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PCO FORMAT

LOAD GO/NO-GO TIMER TEST

COMMAND WORD

<u>FUNCTION</u>	<u>OCTAL</u>	<u>HEX</u>	<u>DEVICE</u>
LOAD GO/NO-GO TIMER TEST	21001100000	88048000	RM



DATA WORD

<u>BIT</u>	
0	NOT USED. BITS IGNORED
1	.
2	.
3	.
4	.
5	.
6	.
7	.
8	.
9	.
10	.
11	LSB = 0.768 msec.
12	GO/NO-GO TIMER BIT 0
13	MSB
14	1
15	2
16	3
17	4
18	5
19	6
20	7
21	8
22	9
23	10
24	11

This PCO is used to load the Go/No-Go Timer with any chosen value which is incremented by one low order bit and read with a PCI (READ STATUS REGISTER) to determine the operating status of the timer.

The Terminate Output driver is inhibited when the interrupt is generated to prevent an invalid indication of GPC failure from this test.

The Terminate Output latch is reset after the time out interrupt has been generated.

The timer is a countup device. The desired code loaded in the data word must be the twos complement of the desired timeout value. A data word of all zeros causes an interrupt after a full count.

Programming Note: This PCO also resets the Timeout Latch.

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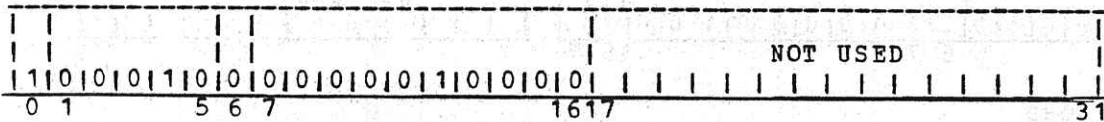
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PCO FORMAT

CONFIGURE TERMINATION CONTROL LATCHES

COMMAND WORD

<u>FUNCTION</u>	<u>OCTAL</u>	<u>HEX</u>	<u>DEVICE</u>
CONFIGURE TERMINATION CONTROL LATCHES	21002000000	88080000	RM



DATA WORD

<u>BIT</u>	
0	NOT USED. BITS IGNORED
.	.
29	.
30	TIMEOUT TERMINATION LATCH
31	VOTER TERMINATION CONTROL LATCH
0	= Reset
1	= Set

These two bits permit control of the associated RM latches by CPU software (PCO) for purposes of testing and to force error indications (Computer Fail and IOP Transmission Termination) for CPU detected faults. The error indications may be inhibited for self testing.

Programming Note: This PCO should not be issued when either the Voter or Timeout Latch is set.

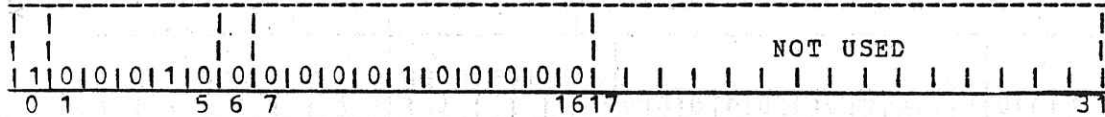
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PCO FORMAT  
LOAD TEST REGISTER

COMMAND WORD

<u>FUNCTION</u>	<u>OCTAL</u>	<u>HEX</u>	<u>DEVICE</u>
LOAD TEST REGISTER	21004000000	88100000	RM



DATA WORD

BIT

0 NOT USED. BITS IGNORED

.

26

27

VOTER TEST CONTROL

0 = Permit normal operation

1 = Inhibit normal inputs (perform test)

This bit inhibits the normal voter inputs (when set) from the other IOP's and inhibits driving of the Computer Fail latch and IOP Transmissions Termination logic. This is used to test the RM voter logic.

28

VOTER TEST INPUT 1

29

2

30

3

31

4

0 = Not failed test input

1 = Failed test input

These bits are used to load a register to provide test inputs to the voter logic for test purposes. Bit 27 (above) must be set to prevent erroneous system failure indications.

The IOP Voter test hardware will respond to these test inputs (Bits 28-31) or to the normal operational inputs. The Test Inputs and Operational Inputs are logically OR'ed.

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PCO FORMAT

INTERRUPTS

COMMAND WORD

FUNCTION

OCTAL

HEX

DEVICE

TEST INTERRUPTS

2100600000

88180000

RM

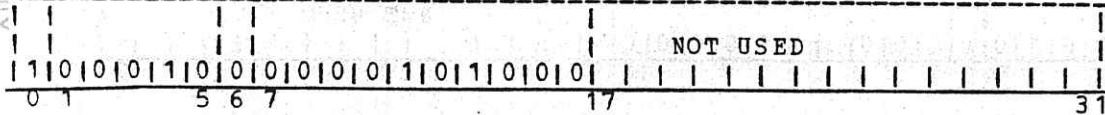
ENABLE INTERRUPTS

2100500000

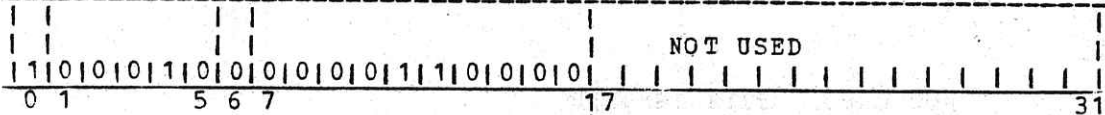
88140000

RM

ENABLE



TEST



DATA WORD

BIT

0

NOT USED. THESE PCO REQUIRE NO DATA WORD.

.

.

31

The TEST command word forces interrupt Registers A, B, D, and E to set all interrupts. The interrupts will stay set until the action described below is taken. This permits self-testing of the interrupt detection circuitry. The interrupt registers will not be reset by reading of the registers as in normal operation.

The ENABLE command must be issued after the TEST command word to remove the test interrupt. After issuing this PCO, each of the four registers must be read to reset them and to permit normal operation.

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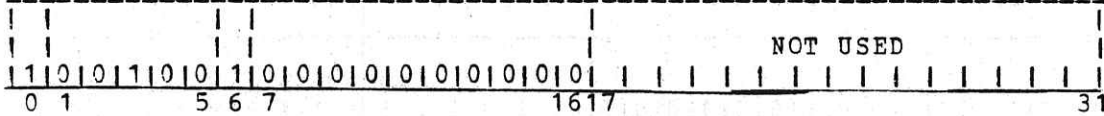
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PCO FORMAT

RESET STATUS 1 (GO/NO-GO)

COMMAND WORD

<u>FUNCTION</u>	<u>OCTAL</u>	<u>HEX</u>	<u>DEVICE</u>
RESET STATUS1 (GO/NO-GO)	22200000000	92000000	DF



DATA WORD

These PCO's provide the capability (data word is used as Mask) to reset Status Register 1 to the normal or GO indicator. The entire word must be configured for each application.

- 0 = No Change
- 1 = Reset Status

BIT

- 0 MSC
- 1 BCE NO. 1
- 2 2
- •
- •
- 23 23
- 24 24
- 25 SELF TEST
- 26 NOT USED. BITS IGNORED
- •
- •
- 31 •

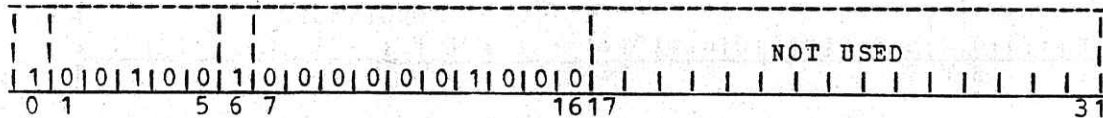
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PCO FORMAT  
LOAD MSC BUSY

COMMAND WORD

<u>FUNCTION</u>	<u>OCTAL</u>	<u>HEX</u>	<u>DEVICE</u>
LOAD MSC BUSY	2220100000	92040000	DF



DATA WORD

No data word required.

This PCO command word forces a BUSY condition to the MSC. It is required to start the micro-processing of MSC/BCE operations after system power-up and initialization.

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<u>BITS</u>	<u>12</u>	<u>13</u>	
	0	0	BANK A
	0	1	BANK B
	1	0	BANK C

Bits 14, 15 and 16

This 3-bit field is used to identify which word in a Bank is loaded. The resolution to a single word is achieved when this field is completed. Banks A and B use only Bits 15 and 16 to control the four words required.

<u>BITS</u>	<u>14</u>	<u>15</u>	<u>16</u>	
	0	0	0	LOCATION 0
	0	0	1	LOCATION 1
	.	.	.	.
	.	.	.	.
	1	1	1	LOCATION 7

DATA WORD

The single data word for this command must contain the data word (18(10) bits) scaled to the LSB portion of the 32-bit data word as indicated below.

PCO DATA  
WORD BIT

0  
1  
.  
.  
13  
14  
15  
.  
.  
31

LOCAL STORAGE  
WORD BIT

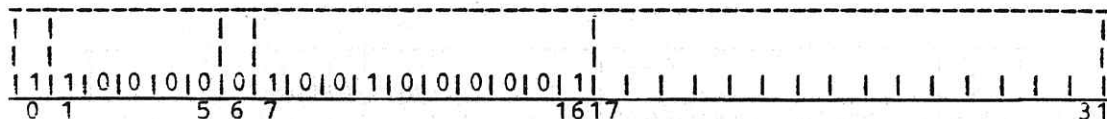
NOT USED  
.  
.  
.  
0 MSB  
1  
.  
17 LSB

PCO FORMAT

TEST DMA 8 MICRO SECOND TIMER\*

COMMAND WORD

<u>FUNCTION</u>	<u>OCTAL</u>	<u>HEX</u>	<u>DEVICE</u>
INHIBIT COMPLETION OF A DMA CYCLE	30100100000	C1008000	CHANNEL



DATA WORD

BIT

0  
 . NOT USED. THIS PCO REQUIRES NO DATA WORD  
 .  
 .  
 31

The Test DMA 8 Microsecond Timer command word causes the channel to inhibit completion of a DMA cycle. This permits self-testing of the DMA 8 microsecond timer and associated interrupt logic. Only the first DMA cycle occurring after reception of the Test DMA 8 Microsecond Timer command word will be inhibited.

\*NOT APPLICABLE TO PROTOTYPES AND CREW TRAINERS

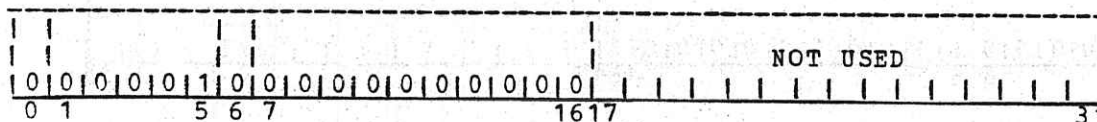
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PCI FORMAT  
 READ MIA TRANSMITTER STATUS

COMMAND WORD

<u>FUNCTION</u>	<u>OCTAL</u>	<u>HEX</u>	<u>DEVICE</u>
READ MIA TRANSMITTER STATUS	0040000000	04000000	C/M



DATA WORD

<u>BIT</u>	
0	CHANNEL NO. 1 MIA TRANSMITTER
1	CHANNEL NO. 2 MIA TRANSMITTER
.	.
.	.
23	CHANNEL NO. 24 MIA TRANSMITTER
24	NOT USED. BITS, IF SET, ARE INVALID.
.	.
.	.
31	.

0	=	Transmitter disabled
1	=	Transmitter enabled

The PCI results in transfer, via the data word, of the configuration of the MIA enable register.  
 Bits 25-27 are available for expansion if required.

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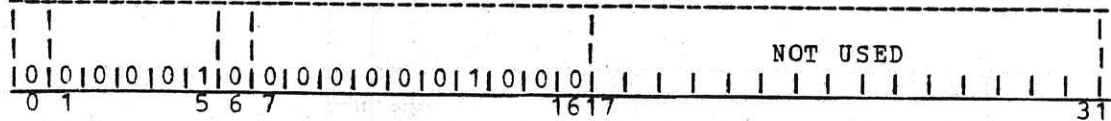
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PCI FORMAT

READ MIA RECEIVER STATUS

COMMAND WORD

<u>FUNCTION</u>	<u>OCTAL</u>	<u>HEX</u>	<u>DEVICE</u>
READ MIA RECEIVER STATUS	00401000000	04040000	C/M



DATA WORD

<u>BIT</u>	
0	MIA CHANNEL NO. 1 RECEIVER
1	2
.	.
.	.
.	.
23	24
25	NOT USED. BITS, IF SET, ARE INVALID.
.	.
.	.
31	.

0 = Receiver disabled  
 1 = Receiver enabled

The PCI results in filling the data word with the contents of the MIA receiver control register.  
 Bits 25-27 are available for expansion of MIA capability if required.

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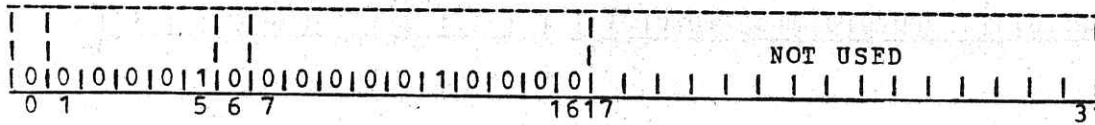
PCI FORMAT  
 READ DISCRETE OUTPUT STATUS

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COMMAND WORD

<u>FUNCTION</u>	<u>OCTAL</u>	<u>HEX</u>	<u>DEVICE</u>
READ DISCRETE OUTPUT STATUS	0040200000	04080000	C/M



DATA WORD

<u>BIT</u>	
0	DISCRETE OUTPUT NO. 1
1	2
.	.
.	.
31	32

0 = Discrete Output Disabled (OFF)  
 1 = Discrete Output Enabled (ON)

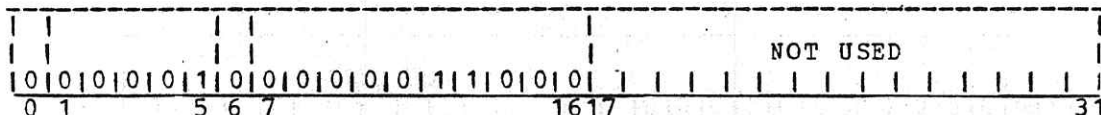
The PCI provides the capability to read the D.O. register.

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PCI FORMAT  
READ PROCESSOR HALT STATUS

COMMAND WORD

<u>FUNCTION</u>	<u>OCTAL</u>	<u>HEX</u>	<u>DEVICE</u>
READ PROCESSOR HALT STATUS	0040300000	040C0000	C/M



DATA WORD

BIT

0	MSC	
1	BCE No. 1	
2	BCE No. 2	
...	...	
24	BCE No. 24	
25	SELF TEST PROCESSOR	
26	NOT PRESENTLY USED.	BITS, IF SET, ARE INVALID.
...	...	
31	...	

0	=	Processor (MSC or BCE) Disabled
1	=	Processor Enabled

The PCI provides access to Status Register 5 (The Halt Register). The data indicates the status (enabled or disabled) of each BCE (25) and the MSC.

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4	IOP FAULT
	The bit is set when the IOP oscillator is stopped.
5	SPARE
6	NOT USED. UNDEFINED
.	.
.	.
31	.

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- 3 NOT USED. HELD AT A ZERO (0) STATE.
- 4 QUEUE OVERFLOW - The 8 usecond timer has detected a DMA that has been in process for more than 8 useconds.
- 5 DMA 8 MICROSECOND TIMEOUT - The Overflow circuitry has detected an attempt to hold more than 64 DMA requests in the Queue.
- 6 NOT USED. UNDEFINED.
- .
- .
- 31 .

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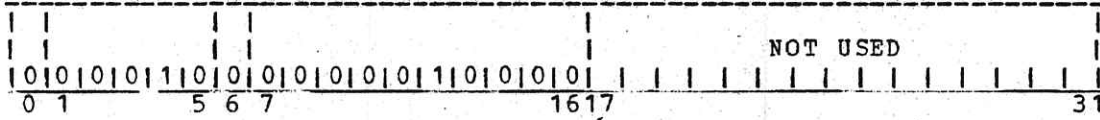
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PCI PCO FORMAT  
READ INTERRUPT REGISTER C

COMMAND WORD

<u>FUNCTION</u>	<u>OCTAL</u>	<u>HEX</u>	<u>DEVICE</u>
READ INTERRUPT REGISTER C	01002000000	08080000	RM



DATA WORD

The bits indicate which of the MSC generated interrupts are present. The PCI transfer causes the bits in Register C to be reset.

- 0 = No interrupt
- 1 = interrupt

BIT

- 0 MSC PROGRAM INTERRUPT 1
- 1 .
- . .
- 11 .
- 12 .
- . NOT USED (ZEROS) UNAVAILABLE.
- . .
- . .
- 31 .

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PCI FORMAT  
READ INTERRUPT REGISTER D

COMMAND WORD

FUNCTION

OCTAL

HEX

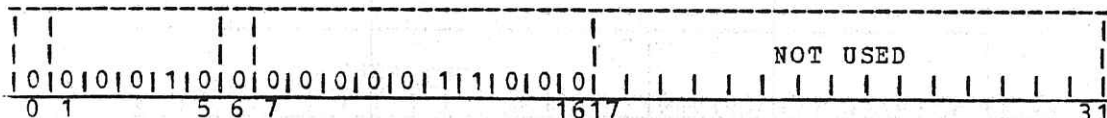
DEVICE

READ INTERRUPT  
REGISTER D

0100300000

080C0000

RM



DATA WORD

This PCI reads a four-bit register and the bits are reset as a result of the PCI.

BIT

- 0 SPARE
- 1 SPARE
- 2 SPARE
- 3 SPARE
- 4 NOT USED (ZEROS) UNAVAILABLE.
- 
- 
- 31

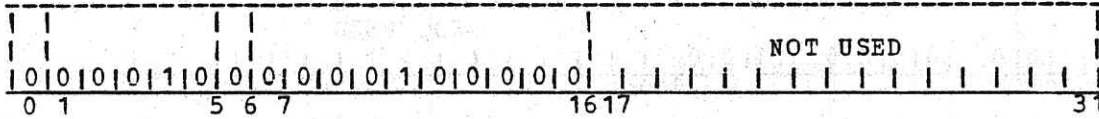
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PCI FORMAT  
 READ INTERRUPT REGISTER E

COMMAND WORD

<u>FUNCTION</u>	<u>OCTAL</u>	<u>HEX</u>	<u>DEVICE</u>
READ INTERRUPT REGISTER E	01004000000	08100000	RM



DATA WORD

This is the read out of a four-bit register presently designated spare.. The PCI transfer resets the register E bits.

BIT

0	SPARE
1	SPARE
2	SPARE
3	SPARE
4	NOT USED. UNDEFINED
.	.
.	.
31	.

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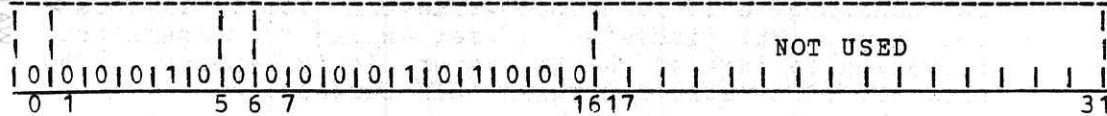
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PCI FORMAT

READ RM STATUS REGISTER

COMMAND WORD

<u>FUNCTION</u>	<u>OCTAL</u>	<u>HEX</u>	<u>DEVICE</u>
READ RM STATUS REGISTER	01005000000	08140000	RM



DATA WORD

Filled from IOP RM status register to provide status of IOP hardware voting logic and data output termination logic. This PCI does not cause reconfiguration of the Status Register.

BIT

- 0 FAIL OR TIMEOUT LATCH
  - 0 = NO FAILURE, NORMAL OPERATION
  - 1 = FAILURE INDICATOR IS SET.

Indicates that RM has detected a failure and set the failure latch or that the watchdog timer has timed out forcing the fail latch. Also set during test modes.
- 1 PCO INHIBIT FAIL VOTE INPUTS FOR TEST
  - 0 = NORMAL OPERATION
  - 1 = PCO inhibiting voter inputs while IOP performs RM logic self testing.
- 2 MSC INHIBIT FAIL VOTE OUTPUTS FOR TEST
  - 0 = Normal operation
  - 1 = MSC inhibiting fail voter output while IOP performs self testing.
- 3 FAILURE VOTE 1 INPUT
  - 41

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4 FAILURE VOTE 2 INPUT

5 FAILURE VOTE 3 INPUT

6 FAILURE VOTE 4 INPUT

0 = NO FAILURE

1 = FAILURE INDICATES

These bits represent the inputs from other IOP's each representing a failure vote while this IOP is in normal operation. The discrettes, if set during test operation, represent failure of the RM voter logic inputs. The bits should be zero during RM self testing.

7 FAILURE VOTE 1 OUTPUT

8 FAILURE VOTE 2 OUTPUT

9 FAILURE VOTE 3 OUTPUT

10 FAILURE VOTE 4 OUTPUT

0 = NO FAILURE

1 = FAILURE VOTE

These bits represent the output (before drivers and output inhibit latches) of the RM software logic to the other IOP's. The register for these bits is set upon PCO from the CPU by the MSC. The data represents output to the other IOP's when in normal system operation.

11 TEST FAILURE VOTE 1 INPUT

12 TEST FAILURE VOTE 2 INPUT

13 TEST FAILURE VOTE 3 INPUT

14 TEST FAILURE VOTE 4 INPUT

0 = NO FAILURE

1 = FAILURE INDICATED (TEST)

These bits represents the RM hardware voter inputs while self testing. A bit set during normal system operation will result in one invalid FAILED VOTE input.

15 VOTER FAIL LATCH

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- 0 = NO FAILURE  
 1 = FAILURE INDICATED

This bit represents the latched output of the RM hardware voter and in normal operation would indicate Computer Failure. The bit is also set during test when the hardware voter receives at least two of four inputs. During test, this voter output is inhibited before reaching the line driver.

16 TIMEOUT LATCH

- 0 = NO TIME OUT  
 1 = TIMEOUT REACHED

This bit indicates that the Watchdog Timer reached a timeout condition. If in normal operation, the bit would trigger the Computer Fail Latch. In test mode, the signal is inhibited prior to the Computer Fail Driver.

17 VOTER TERMINATION CONTROL LATCH

18 TIMER TERMINATION CONTROL LATCH

- 0 = RESET  
 1 = SET

These bits represent the output of the respective latches which are set and reset via PCI/PCO from CPU software. They are used to force IOP transmission termination for CPU detected failures. These outputs are inhibited before the IOP transmission termination when self testing.

19 IOP TRANSMISSION TERMINATION

- 0 = NORMAL  
 1 = TERMINATE

This bit indicates the status of the associated output (which is not a latch). When the bit is present, the output (discretes and MIA transmitters) are disabled to prevent extraneous data transmissions.

20 GO/NO-GO TIMER Bit 0 (MSB)  
 21 1  
 22 2 43

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23  
24  
25  
26  
27  
28  
29  
30  
31

3  
4  
5  
6  
7  
8  
9  
10  
11

(LSB) = 0.768 msec

Bits 20-31 represent the configuration of the Watchdog (GO/NO-GO) Timer. The data is available in normal system operation and during self testing.

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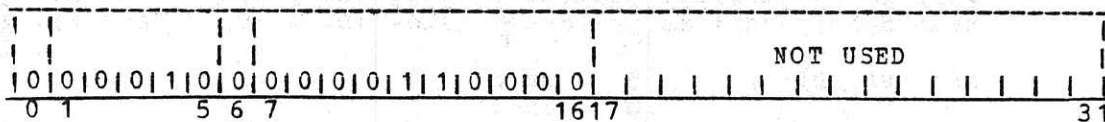
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PCI FORMATS

READ DISCRETE INPUT A

COMMAND WORD

<u>FUNCTION</u>	<u>OCTAL</u>	<u>HEX</u>	<u>DEVICE</u>
READ DISCRETE INPUT A (1-32)	0100600000	08180000	DF



DATA WORD

This PCI provides means to transfer data from the IOP Discrete Input register (32 bits) to the CPU.

- 0 = D.I. RESET
- 1 = D.I. SET

NOTE: All the DI's are software readable. Some also configure hardware. Bit positions designated by \* indicate those discrete inputs which are hardwired to IOP functions and must not be changed from the designated function due to internal or external wiring changes. The discrete inputs are implemented with differential receivers. The input pins are listed with each DI. The T represents the true input pin and C indicates the complement inputs.

BIT

- \*0 HALT (DI-1) T J5-1  
C J5-2

The setting of this bit indicates that the crew panel switch has been sent to 'HALT'. Receipt of this DI causes the IOP to configure all processors to Halt thereby prohibiting IOP operation. The CPU is held in system reset by this discrete.

- \*1 STANDBY (DI-2) T J5-3  
C J5-4

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\*12 INHIBIT CHANS. 10-13 (DI-13) T J5-25  
C J5-26

Receipt of this DI causes the IOP to inhibit the MIA transmitters thereby prohibiting the output of data on Channels 10-13 (MIA's 10-13).

\*13 INHIBIT CHANS. 14-17 and 20-23 (DI-14) T J5-27  
C J5-28

Receipt of this DI causes the IOP to inhibit MIA transmitters 10-14 and 20-23.

14	(DI-15)	T	J5-29
		C	J5-30
15	(DI-16)	T	J3-66
		C	J3-77
16	(DI-17)	T	J3-89
		C	J3-88
17	(DI-18)	T	J3-69
		C	J3-70
18	(DI-19)	T	J3-79
		C	J3-78
19	(DI-20)	T	J3-81
		C	J3-93
20	(DI-21)	T	J3-80
		C	J3-91
21	(DI-22)	T	J3-92
		C	J3-104
22	(DI-23)	T	J3-114
		C	J3-103
23	(DI-24)	T	J3-90
		C	J3-102
24	(DI-25)	T	J3-113
		C	J3-121
25	(DI-26)	T	J3-128
		C	J3-112
26	(DI-27)	T	J3-111
		C	J3-101

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27	(DI-28)	T C	J3-120 J3-127
28	(DI-29)	T C	J3-126 J3-119
29	(DI-30)	T C	J3-99 J3-109
30	(DI-31)	T C	J3-118 J3-125
31	(DI-32)	T C	J3-124 J3-117

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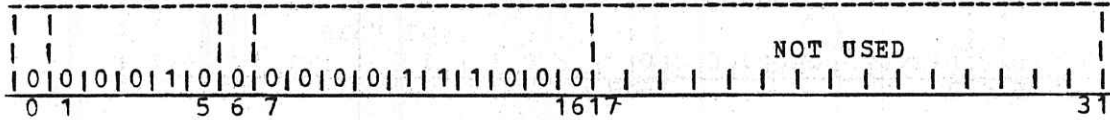
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PCI FORMAT  
 READ DISCRETE INPUTS (33-40)

COMMAND WORD

<u>FUNCTION</u>	<u>OCTAL</u>	<u>HEX</u>	<u>DEVICE</u>
READ DISCRETE INPUTS (33-40)	01007000000	081C0000	RM



DATA WORD

This PCI provides the transfer of Discrete Inputs 33-40 to the CPU.

- 0 = D.I. RESET
- 1 = D.I. SET

BIT

BIT			
0	(DI-33)	T	J3-74
		C	J3-75
1	(DI-34)	T	J3-116
		C	J3-123
2	(DI-35)	T	J3-122
		C	J3-107
3	(DI-36)	T	J3-96
		C	J3-97
4	(DI-37)	T	J3-106
		C	J3-115
5	(DI-38)	T	J3-85
		C	J3-84
6	(DI-39)	T	J3-95
		C	J3-105
7	(DI-40)	T	J3-94
		C	J3-83
8	NOT USED.		UNDEFINED
.			.
.			.
31			.

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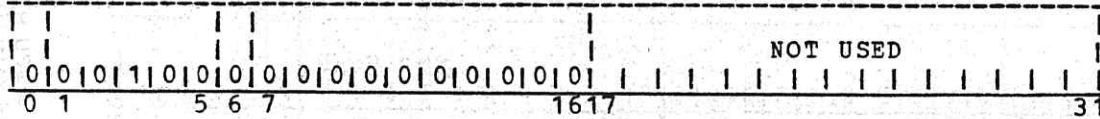
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PCI FORMAT

READ STATUS 1 (GO/NO-GO)

COMMAND WORD

<u>FUNCTION</u>	<u>OCTAL</u>	<u>HEX</u>	<u>DEVICE</u>
READ STATUS1 (GO/NO-GO)	02000000000	10000000	DF



DATA WORD

The data word contains the GO/NO-GO status for each BCE and MSC as determined by IOP BITE.

0 = NO-GO (ERROR)  
 1 = GO

BIT

0	MSC
1	BCE NO. 1
2	BCE NO. 2
.	.
.	.
24	24
25	SELF TEST PROCESSOR
26	NOT USED. UNDEFINED
.	.
.	.
31	.

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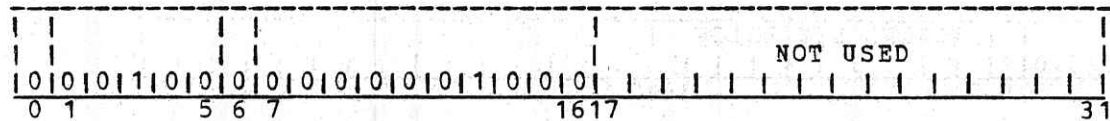
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PCI FORMAT

READ STATUS 4 (BUSY/WAIT)

COMMAND WORD

<u>FUNCTION</u>	<u>OCTAL</u>	<u>HEX</u>	<u>DEVICE</u>
READ STATUS4 (BUSY/WAIT)	02001000000	10040000	DF



DATA WORD

The data word transfers the contents of Status Register 4 to the CPU. The action provides indication of the MSC and BCE's operating states.

0 = WAIT  
 1 = BUSY

BIT

0	MSC
1	BCE NO. 1
.	.
.	.
24	24
25	SELF TEST PROCESSOR
26	NOT USED. UNDEFINED
.	.
.	.
31	.

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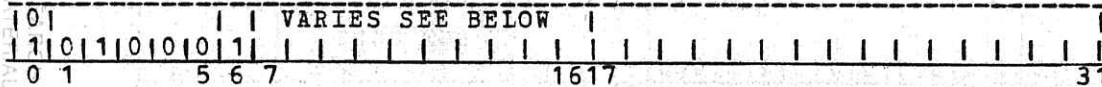
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PCI FORMAT  
 READ LOCAL STORE

COMMAND WORD

<u>FUNCTION</u>	<u>OCTAL</u>	<u>HEX</u>	<u>DEVICE</u>
READ LOCAL STORE			LS



The 10(10) bits (7 through 16) associated with the device select field for this command word varies depending upon the word (location) loaded in Local Store. The command word provides access to the Local Store area associated with the MSC function and the 24 BCE functions of the IOP. The specific data stored in each location is discussed in the MSC and BCE Principals of Operation documents and involve that data required for initializing and operating the MSC and BCE's.

Bits 7 through 11

This 5-bit field is used to designate the MSC or BCE from which the data word must be transferred as shown below:

<u>BITS</u>	<u>7</u>	<u>8</u>	<u>9</u>	<u>10</u>	<u>11</u>	
0	0	0	0	0	0	MSC REGION
0	0	0	0	0	1	BCE NO. 1 REGION
0	0	0	0	1	0	BCE NO. 2 REGION
			.			.
1	1	0	0	0	0	BCE NO. 24 REGION
1	1	0	0	0	1	SELF TEST PROCESSOR

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Bits 12 and 13

This 2-bit field identifies the bank (A, B, or C) in Local Store for the above defined MSC or BCE area from which the data word must be transferred as indicated below.

<u>BITS</u>	<u>12</u>	<u>13</u>	
	0	0	BANK A
	0	1	BANK B
	1	0	BANK C

Bits 14, 15 and 16

This 3-bit field is used to identify which word in a Bank is read. The resolution to a single word is achieved when this field is completed. Banks A and B use only Bits 15 and 16 to identify the four words required.

<u>BITS</u>	<u>14</u>	<u>15</u>	<u>16</u>	
	0	0	0	LOCATION 0
	0	0	1	LOCATION 1
		.	.	
		.	.	
	1	1	1	LOCATION 7

DATA WORD

The single data word for this command contains the data word (18(10) bits) scaled to the LSB portion of the 32-bit data word as indicated below.

PCO DATA  
WORD BIT

0  
1  
.  
.  
13  
14  
15  
.  
.  
31

LOCAL STORAGE  
WORD BIT

UNDEFINED  
.  
.  
.  
0      MSB  
1  
.  
.  
17     LSB

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PART II

**Space Shuttle Advanced System/4 Pi  
Input/Output Processor (IOP)**

**Principles of Operation for the  
Master Sequence Controller**

Prepared for

Rockwell International Corporation  
Space Division  
12214 Lakewood Blvd.  
Downey, CA 90241

26 April 1976

Under Purchase Order No.  
MAJ7XMA-483019

IBM No. 6246556A



Federal Systems Division, Owego, New York 13827

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TABLE OF CONTENTS

<u>Section</u>		<u>Page</u>
1.0	MASTER SEQUENCE CONTROLLER-----	1
1.1	ADDRESSING, DATA, AND INSTRUCTION FORMATS-----	3
1.2	MSC REGISTERS-----	8
1.2.1	MSC PROGRAMMABLE REGISTER-----	8
1.2.2	MSC STATUS REGISTER-----	<del>8</del> 11
1.2.3	OTHER MSC VISIBLE REGISTERS-----	13
1.3	MSC IMPLEMENTATION-----	14
2.0	GENERER MSC OPERATION-----	16
2.1	HALT STATE-----	16
2.2	WAIT STATE-----	20
2.3	BUSY STATE-----	21
2.4	ERROR MODES-----	23
3.0	MSC INSTRUCTIONS-----	26
3.1	ACCUMULATOR/MEMORY INSTRUCTIONS-----	27
3.2	BRANCHING INSTRUCTIONS-----	37
3.3	CONDITIONAL SKIP INSTRUCTIONS-----	45
3.4	BCE REGISTER LOAD INSTRUCTIONS-----	49
3.5	REGISTER OPERATIONS-----	52
3.6	REGISTER IMMEDIATE INSTRUCTIONS-----	67
3.7	REPEAT INSTRUCTIONS-----	79
3.8	SPECIAL INSTRUCTIONS-----	91
4.0	EXTERNAL CALLS-----	98

Appendix A

IOP MSC INSTRUCTION REPERTOIRE-----	101
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LIST OF FIGURES

<u>Figure</u>		<u>Page</u>
1.1	MSC-Computed Main Memory Addresses-----	4
1.2	Basic MSC Instruction Formats-----	5
1.3	Number Representation In MSC Accumulator-----	10
1.4	Number Representation In Index Register-----	10
1.5	MSC Local Store Usage-----	15
2.1	MSC States-----	18
3.1	Sample Code Using @SEC-----	65
3.2	@NIX Instruction Execution-----	70
3.3	General Repeat Instruction Execution-----	82
4.1	MSC Code To Call An External Call Routine-----	100

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LIST OF TABLES

<u>Table</u>		<u>Page</u>
1.1	MSC Characteristics-----	2
1.2	MSC Long Format Modes-----	7
1.3	MSC Status Register-----	11
2.1	MSC States-----	19
2.2	IOP Errors Affecting MSC Operation-----	24
3.1	List Of Register Operations-----	53
3.2	Register Immediate Instruction-----	68
3.3.	Repeat Instructions-----	81

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1.0 MASTER SEQUENCE CONTROLLER

The Master Sequence Controller (MSC) is a micro programmed computer specifically tailored for I/O Management within the Space Shuttle General Purpose Computer (GPC). As such, it has extensive and programmable capabilities for monitoring and controlling the basic I/O operations performed by upwards to 24 Bus Control Elements (BCE's) which are implemented in the baseline GPC. These capabilities include setting up, scheduling, and initiating BCE programs, monitoring the status of BCE operations, and communicating overall completion of these operations to the CPU.

Table 1.1 summarizes the characteristics of the MSC.

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TABLE 1.1  
MSC CHARACTERISTICS

TYPE - Single Accumulator I/O Management Computer  
CONTROL STRUCTURE - Microprogrammed  
PROGRAMMABLE  
REGISTERS -

32 Bit ACCUMULATOR (ACC)  
18 Bit INDEX REGISTER (X)  
18 Bit PROGRAM COUNTER (PC)

PROGRAM 18 Bit STATUS REGISTER  
VISIBLE 25 Bit PROGRAM EXCEPTION REGISTER  
REGISTERS 25 Bit BUSY/WAIT REGISTER  
24 Bit BCE-MSC INDICATORS  
5 Bit FAIL DISCRETES  
12 Bit IOP PROGRAMMABLE INTERRUPT REGISTER  
18 Bit EXTERNAL CALL REGISTER

INSTRUCTION FORMATS - 16 Bit SHORT/32 Bit LONG

INSTRUCTION REPERTOIRE - 47 SHORT FORMAT/10 LONG FORMAT  
(NOT COUNTING ADDRESSING MODES)

ADDRESSING SPACE 131,072 32 Bit FULLWORDS/262,144 16 Bit HALFWORDS

ADDRESSING MODES IMMEDIATE, ABSOLUTE, INDEXED,  
PC RELATIVE

DATA FORMAT SIGNED, TWO'S COMPLEMENT INTEGER

SPECIAL FEATURES INITIALIZE AND MONITOR BCes.  
RESPOND TO CPU REQUESTS TO  
CHANGE PROGRAM (EXTERNAL CALL).

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## 1.1 ADDRESSING, DATA AND INSTRUCTION FORMATS

The MSC may directly address up to 262,144 16-bit halfwords or 131,072 32-bit fullwords. To achieve this, all main memory addresses computed by the MSC are represented as 18-bit absolute numbers, as pictured in Figure 1.1. The upper 17-bits (bits 0 through 16) represent the fullword location, and the lowest bit (bit 17) the halfword portion of the addressed fullword. A 0 in this lower bit refers to bits 0-15 of the 32-bit fullword; a 1 refers to bits 16-31. When used as a fullword address, bit 17 is ignored. Thus, H'276' and H'277' refer to the same fullword.

All data referenced as numbers by the MSC are treated as signed two's complement binary integers.

There are three basic instruction formats used by the MSC and they are depicted in Figure 1.2.

Short format 1 is used primarily by instructions dealing with memory and the MSC accumulator. It has the following fields:

<u>Field</u>	<u>Field Description</u>
OP	This 4-bit field defines the basic operation to be performed by the MSC
I	This bit serves either as an opcode extension or as an index mode specification in address generation
DISP	This 11-bit field serves either as immediate data or as a PC relative address displacement.

Short format 2 is used by the register operation, register immediate, repeat, and conditional branching instruction classes. It has the following fields:

<u>Field</u>	<u>Field Description</u>
OP	This 4-bit field defines the basic operation class to be performed by the MSC
I	This bit serves either as an opcode extension or as an index mode specification in address generation
OPX	This field is an extension of OP
DISP	This field serves as either immediate data or as a PC relative address displacement.

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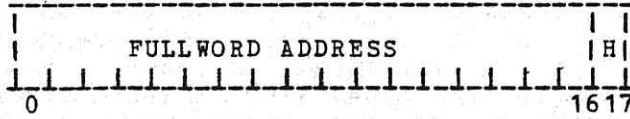
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H = Halfword Selector

Figure 1.1. MSC-Computed Main Memory Addresses.

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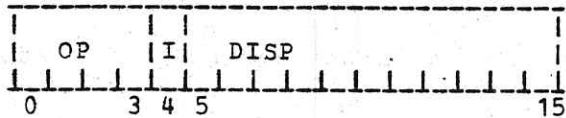
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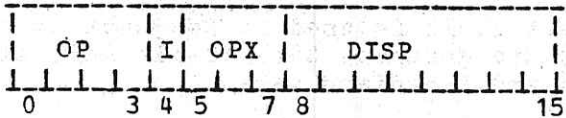
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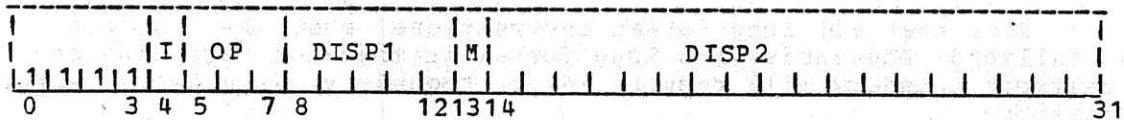
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I = Index Specification or OPX  
 (a) Short Format 1



I = Index Specification or OPX  
 (b) Short Format 2



(c) Long Format

Figure 1.2. Basic MSC Instruction Formats.

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Format 3 is used for all long 32-bit instructions, and has the following fields:

<u>Field</u>	<u>Field Description</u>
OP	This 3-bit field defines the basic operation to be performed by the MSC
DISP1	This 5-bit field defines such things as BCE numbers, short displacements, etc.
DISP2	This 18-bit field is used in conjunction with I and M to generate both 18 bit main memory addresses and immediate data.
I,M	These two bits define the way that DISP2 is to be used in formation of values used by the instruction for main memory addresses and immediate data.

Table 1.2 summarizes the use of I,M and DISP2.

Note that all long format instructions must be located on even fullword boundaries. A long format instruction beginning on an odd halfword boundary will result in a "Boundary Alignment" error termination.

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TABLE 1.2

## MSC LONG FORMAT MODES

<u>I</u>	<u>M</u>	<u>Effective Value</u>	<u>Mode</u>
0	0	DISP2*	IMMEDIATE
1	0	X+DISP2*	INDEXED, IMMEDIATE
0	1	(DISP2)	DIRECT
1	1	(X+DISP2)	INDEXED, DIRECT

Parenthesis used around a quantity indicate that it is to be treated as an 18-bit main memory fullword address (least-significant bit ignored) and that the effective value is found in fullword.

NOTES:

- \* When the effective value is used as immediate data, the most-significant bit is sign-extended 14 places to the left

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## 1.2 MSC REGISTERS

### 1.2.1 MSC PROGRAMMABLE REGISTER

The MSC contains 3 registers under direct program control. They are:

- ACC - A 32-bit accumulator
- X - An 18-bit index register
- PC - An 18-bit Program Counter

The ACC is a 32-bit register capable of accumulating a fullword of data from memory. MSC instructions are available to load, modify, test and store this register. The ACC is also used to contain bit masks for status and polling applications.

Data representation of numbers held by the ACC is a signed, two's complement, 32-bit integer, with the sign bit in bit 0 and the binary point to the right of bit 31 (Figure 1.3).

The Index register may be used both in generating 18-bit main memory addresses and as a holding register for signed two's complement 18-bit integers. When treated as an address, it is formatted as in Figure 1.1. When treated as a number, it is formatted as in Figure 1.4.

The Program Counter is an 18-bit register that indicates the main memory halfword or fullword location of the MSC instruction presently being executed. It is formatted as a standard 18-bit address as in Figure 1.1.

### 1.2.2 MSC STATUS REGISTER

The status of the MSC is kept in the following three registers:

- 1) MSC Busy/Wait Bit - Bit 0 of the IOP Busy/Wait Register. A 1 in this bit indicates that the MSC is currently executing a program located in main memory. A 0 indicates it is not busy. This bit is set via a PCO from the CPU to activate the MSC, and reset by the MSC upon completion of a program.
- 2) MSC Program Exception Bit - bit 0 of the IOP Program Exception Register A 0 indicates that the MSC has encountered some problem in the execution of an MSC program. A 1 indicates that no problems were encountered. This bit is maintained by the MSC microcode.

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- 3) MSC Status Register - An 18-bit register found in register C7 in the MSC segment of Local Store (See Figure 1.5). This register contains copies of the MSC Busy/Wait bit and the MSC Program Exception bit. If the latter bit is set, this register also indicates the exact cause of the exception, as indicated in Table 1.3. It is set automatically upon the detection of an exception or as part of MSC execution of an @REC instruction, and may be read by the MSC with a @LMS instruction.

## PROGRAMMING NOTE

The macro programmer can:

- 1) Reset STAT1 (Hardware register) via a PCO command.
- 2) Clear or change the MSC status register via a PCO command.
- 3) Reload the MSC status register using an @REC instruction.

Execution of any of the three cases above will alter the MSC Status Register. To guard against their possible interference with system operation the following principles should be adhered to:

- 1) While the MSC is busy do not attempt to alter the STAT1 or STAT4 Registers by using PCO commands.
- 2) While the MSC is busy do not attempt to change the MSC Status Register via PCO's.
- 3) Be aware that when the MSC returns from an external call (@REC) the MSC Status Register is loaded.

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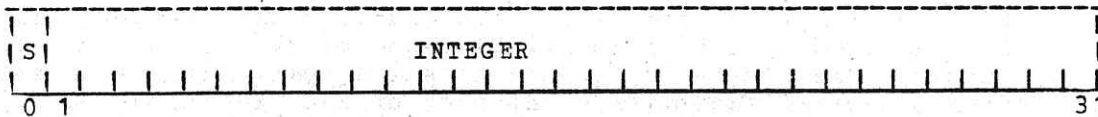
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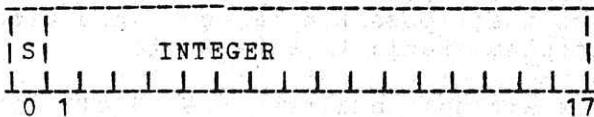
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S = Sign

Figure 1.3. Number Representation in MSC Accumulator



S = Sign

Figure 1.4. Number Representation in MSC Index Register.

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TABLE 1.3

## MSC STATUS REGISTER

RESERVED	S T F	SIO ERR	LBP ERR	LBB EPP	ALIGN	ILL OP	ERR	BUSY/ WAIT	
	89	10	11	12	13	14	15	16	17

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- Bit 17 STAT4 bit 0 - The Busy/Wait bit for the MSC. It will always be 1 while instructions are being executed.
- Bit 16 STAT1 bit 0 - The program exception bit for the MSC. This bit will be set to one only if the execution of some previous instructions resulted in an error of some kind. Bits 15 through 8 catalog the exact error. This bit is the inverse of the MSC program exception bit.
- Bit 15\* Illegal opcode. If set, this bit indicates that an illegal opcode was encountered at some point in the past.
- Bit 14\* Boundary alignment error. If set, this bit indicates that a long format instruction was encountered at an odd halfword boundary.
- Bit 13 LBB error. The BCE that was specified by a previous @LBB instruction was busy or halted at the time the instruction was executed, and consequently its Base Register was not loaded.
- Bit 12 LBP error. The BCE that was specified by a previous @LBP was busy or halted at the time the instruction was executed, and consequently its Program Counter was not loaded.
- Bit 11 SIO error. A previous execution of an @SIO instruction tried to set at least one BCE to busy that was already busy.
- Bit 10,9 Reserved.
- Bit 8 Self test failure. The execution of a previous MSC self test instruction detected a fault in the MSC.

Note that the only way this bit could be set when an @LMS is executed is if this error condition was detected

in the past, and the CPU restarted the MSC without clearing the status word first.

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## 1.2.3 OTHER MSC VISIBLE REGISTERS

In addition to the register described above, there are several other IOP registers that are accessible by an MSC program. These registers include the:

- o Program Exception Register (STAT1 Register) - a 25-bit register containing one bit per processor. A 0 in bit position *i* indicates that processor *i* (0=MSC,1-24=BCE) has encountered some sort of exceptional condition. An exact description of the cause of the exception may be found in processor(*i*)'s status register.
- o Busy/Wait Register - a 25-bit register containing one bit per processor. A 1 in bit position *i* indicates that processor(*i*) is presently executing a program. A 0 indicates that the processor is inactive.
- o BCE-MSD Indicator Register - a 24-bit register containing one bit per BCE. BCE(*i*) may set or reset bit (*i*) under BCE program control (See #SIB, #RIB). Various BCE errors will also set this bit to 1. The MSC @RBI instruction may reset any of these bits. There is no hardware defined meaning for these values. They may be used freely to indicate any programmer specified convention.
- o Fail Discrete Register - these discrettes are grouped as a single register, and are used in the redundancy management process to indicate failed GPC units. The IOP Functional Description (IBM No. 74-A31-026) should be referenced for their exact use.
- o IOP Programmable Interrupt Register - this 12-bit register may be set by the MSC to specify any combination of 12 CPU interrupts. The exact meaning of each interrupt is determined by convention between the MSC program and the CPU interrupt handling program.
- o External Call Register - this 18-bit register may be set by the CPU to point to a program that it wishes the MSC to execute. The MSC resets the register to zero when it has started the program. The Sample For External Call (@SEC) instruction and section 4.0 should be referenced for additional detail.

The Program Exception register may only be read. The Busy/Wait and Fail discrete registers may be both read and set. The BCE-MSD Indicator register may be read or reset. The IOP Programmable Interrupt Register may only be set. The External Call register may be set by the CPU and reset by the MSC.

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1.3 MSC IMPLEMENTATION

The MSC as implemented within the IOP consists of:

- o Segment 0 of Banks A, B and C of Local Store. This contains the ACC, X, PC, Status Register, and all other working registers needed to implement the MSC instruction set.
- o Bit 0 of the IOP Busy/Wait Register.
- o Bit 0 of the IOP Program Exception Register.
- o Bit 0 of the Halt Register
- o Microprogram Counter 0. This contains the ROS address of the next micro-instruction to be executed as part of the execution of the present MSC instruction.

As described in the IOP Functional Description (IBM No. 74-A31-016), the operation of the MSC is time-shared with operations for the BCE's. This time-sharing is performed at the micro-instruction level, where the IOP executes one MSC micro-instruction from ROS (The one indicated by the MSC micro-program counter) then a micro-instruction for several of the BCE's, followed by an MSC micro-instruction, etc. MSC micro-instructions normally occur at 2 microsecond intervals with the exception of every eighth MSC micro-instruction which occurs 2.5 microseconds after the preceding instruction. The only MSC-related operation carried on during non-MSC microcycles are memory operations, previously requested by MSC, and CPU-directed PCI/O.

The general makeup of the Local Store segment dedicated to the MSC is shown in Figure 1.5. All unlabelled words are reserved as temporary working registers during the execution of a single MSC instruction. After each instruction, however, only the labelled contents are assumed to be properly maintained.

The PCI/O operations of reading or writing to any of these locations may occur at any time, although writing into MSC local store while the MSC is busy will generally result in unpredictable MSC behavior.

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BANKA	BANKB	BANKC	WORD
			0
			1
PC	IH	IL	2
X	AH	AL	3
			4
			5
		ECR	6
		ST	7

- PC - MSC Program Counter  
X - MSC Index Register  
IH - Upper 16 bits of present MSC instructions  
(Right justified with Bits 0 and 1 ignored)  
IL - Lower 18 bits of last instruction word that  
was read from memory.  
AH - Bits 0-15 of MSC accumulator (right justified  
into local store. Bits 0,1 ignored).  
AL - Bits 16-31 of MSC accumulator (right justified as for AH)  
ECR - External Call Register  
ST - Bits 0-17 of MSC Status Register (Right justified)

Figure 1.5. MSC Local Store Usage

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## 2.0 GENERAL MSC OPERATION

During normal operation the MSC can be in one of three states: Halt, Wait and Busy. In the Halt state the MSC is physically restrained from performing any operations; in the Wait state the MSC is awaiting a command to execute a program; and in the Busy state the MSC is executing MSC programs from main store. Figure 2.1 and Table 2.1 summarize these states and the transitions between them.

Typical state transitions are as follows:

- 1) During any system or CPU-directed MSC reset, the MSC is in the Halt state.
- 2) Upon release from the Halt state, the MSC enters the Wait state
- 3) A sequence of PCO's from the CPU initializes the MSC, and places it in the Busy state.
- 4) In the Busy state, the MSC is executing a program located in main memory. It exits the Busy state only upon execution of a Wait instruction, detection of an invalid instruction, or some MSC reset signal. In all but the latter case, the MSC re-enters the Wait state; in the latter case it is forced to the Halt state.

The two bits that indicate the current state of the MSC are its Halt bit (Bit 0 of the IOP Halt register) and its Busy/Wait bit (Bit 0 of the IOP Busy/Wait register). In addition, the MSC Program Exception bit indicates if the MSC has found an error during its last period of time in the Busy state. If it has found an error, the MSC Status Register contains a record of the error.

The following sections describe each state in detail.

### 2.1 HALT STATE

The primary purpose of the Halt state is two-fold:

- 1) Allow the external world to reset MSC operation to a known condition.
- 2) Upon the detection of very serious IOP faults (such as failure in the microstore) to isolate the MSC and prevent it from performing potentially erroneous operations.

Entry and exit from the Halt state are controlled by the value of a single "MSC Halt" status bit which is part of the IOP Halt Register. As long as this bit is set, the MSC microprogram counter is

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forced to point to a micro-instruction that performs no operation other than clear the MSC Busy/Wait bit. The Halt bit may be set at any time, and effectively terminates anything that the MSC is doing.

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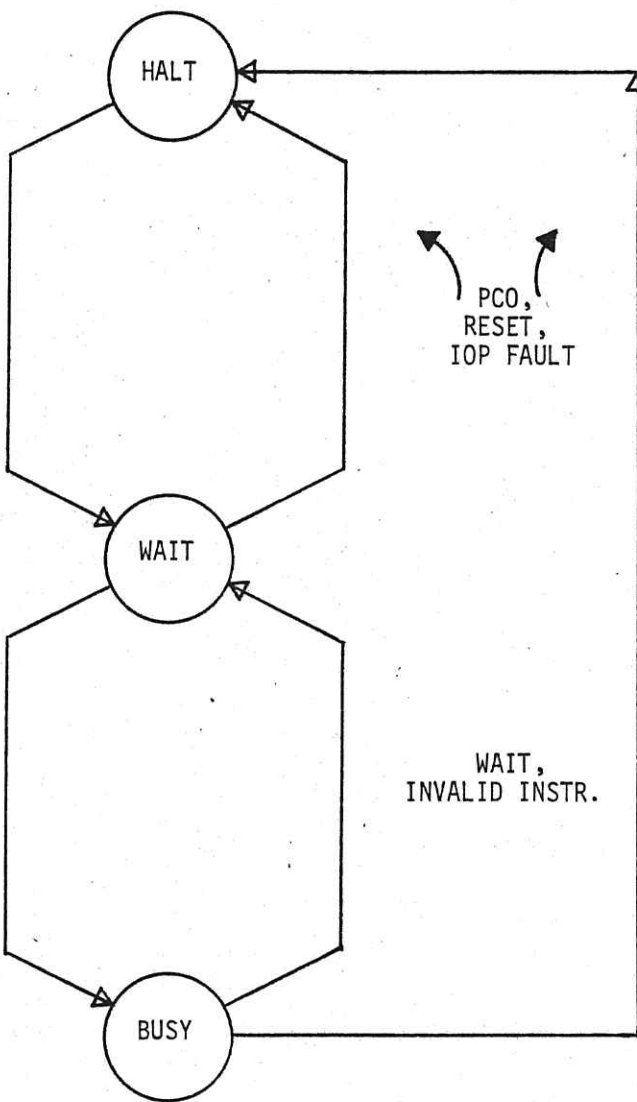


Figure 2.1 MSC States

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TABLE 2.1

## MSC STATES

STATE	ENTERED FROM STATE/WHEN	ACTION TAKEN IN STATE	STATE INDICATORS	
			HALT	BUSY/ WAIT
HALT	ANY STATE - MASTER RESET  - FAIL LATCH SET FOR THIS GPC - PCO SPECIFYING MSC HALT	HARDWARE FORCED MICRO BRANCH TO DO NOTHING MICRO INSTRUCTION.  BUSY/WAIT, STATUS, EXTERNAL CALL REGISTER, AND PROGRAM EXCEPTION BIT CLEARED UPON EXIT.	0	0
WAIT	HALT - PCO TO CLEAR BIT  BUSY - EXECUTION OF "WAIT" INSTR - ILLEGAL OPCODE - BOUNDARY ALIGNMENT ERROR	MONITOR BUSY/WAIT BIT FOR TRANSITION TO BUSY	1	0
BUSY	WAIT - PCO SETS BUSY/WAIT BIT	EXECUTE MSC PROGRAM SET PROGRAM EXCEPTION BIT AND STATUS WORD UPON DETECTION OF ANY PROBLEM	1	1

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The signals that set the MSC Halt bit to 0 (halt MSC) include:

- 1) BCE/MSC disable discrettes or discrete input 0.
- 2) Power-up/down signal.
- 3) Setting of the Fail Latch for this GPC by either the Redundancy Management voting logic or IOP detected serious errors such as ROM parity error or timing failure.
- 4) A "Master Reset" PCO from the CPU.
- 5) A "Halt Processor" PCO from the CPU with a 1 in bit position 0.

The first four signal classes also halt all BCE's.

Exit from this state to the Wait state occurs only when the following occurs:

- 1) "BCE Disable" discrete is reset.
- 2) Power-up sequence is complete.
- 3) Fail latch is reset.

and a CPU "Enable Processors" PCO with bit 0=1 is present.

Upon any exit from the Halt state, the MSC Program Exception bit is set to 1 and the MSC Status Register is cleared to 0 to indicate that no errors exist. The MSC also clears the External Call register at this time.

## 2.2 WAIT STATE

In the Wait state, the MSC is prepared to be told to perform an MSC program. This Wait loop is implemented by a micro-routine that monitors the status of the MSC Busy/Wait bit. The MSC remains in the Wait state as long as this bit is reset to the "wait" value. Setting this bit to a "busy" condition causes the MSC to transit to the Busy state. This transition consists of using the present value of the MSC's Program Counter as the starting address of an MSC program in main store.

Entry to the Wait state occurs either upon exit from the Halt state, as described above, or by a transition from the Busy state. The MSC performs this latter transition when any of the following occur:

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- 1) A "Wait" instruction is executed.
- 2) An instruction with an illegal opcode is encountered.
- 3) A valid long format instruction is found starting on an odd halfword boundary.

In the latter two cases, the following actions are performed prior to entering the Wait state:

- 1) The MSC Program Exception bit is set to 0.
- 2) The MSC Status Register is set to indicate the exact cause of the error.
- 3) The MSC Program Counter is left pointing to the offending instruction.

The Program Exception bit and Status Registers may also be set when other errors are detected while the MSC is in the Busy state; in these cases, however, the MSC continues execution of the program.

Exit from the Wait state is normally to the Busy state. This is done by the CPU via a sequence of PCO's; these typically include:

- 1) A "Load Local store" PCO to clear the MSC Status Register (if set).
- 2) A "Reset Program Exception Register" PCO with a 1 in bit 0 (again used only when MSC has indicated an error).
- 3) A "Load Local Store" PCO to point to the start of the desired MSC program in main store.
- 4) A "Start MSC" PCO to set the MSC Busy/Wait bit.

Note that the first two are needed only to recover from an MSC error, and the third is needed only if the MSC program counter must be reset. They may not always be necessary, since the Wait instruction (@WAT), when executed, leaves the PC pointing to the next sequential instruction, which in turn may be programmed as a simple jump back to the beginning of the MSC program. In this case, the CPU needs only to issue the "Start MSC" PCO to restart the MSC program.

### 2.3 BUSY STATE

In the Busy state, the MSC is in the process of executing a program out of main store. A value of 1 in the 0 bit of the IOP Busy/Wait Register indicates this condition.

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The Busy state may be entered only from the Wait state, as described in the previous section. When the transaction occurs, the MSC uses whatever value is presently in its Program Counter to fetch the first instruction from memory and start executing it. The MSC continues executing instructions until either a Wait instruction or some kind of invalid instruction is encountered. In either case, the MSC transitions back to the Wait state, again as described in the previous section.

While the MSC is in the Busy state, the CPU may execute any PCI without problem. However, all PCO's that write into MSC Local store should be carefully controlled since the MSC is not aware that this action has occurred, and the resulting MSC program execution may be unpredictable.

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2.4 ERROR MODES

During execution of an MSC program, the MSC may encounter one or more errors. These errors may be due to either faulty programming or actual hardware faults. Many can be detected by the IOP microprograms that support the MSC functions, and are reflected by the setting of various status bits in the MSC Status Register and the MSC Program Exception bit. If the error is serious enough, the MSC terminates the instruction and enters the Wait state.

Table 2.2 summarizes all known errors that can affect MSC operation; how they are detected; and the actions taken upon their detection.

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TABLE 2.2

## IOP ERRORS AFFECTING MSC OPERATION

<u>ERROR</u>	<u>DETECTED_BY</u>	<u>ACTION</u>
Illegal MSC Instruction Opcode	Microcode	Set MSC Program Exception Bit, Set Status bits 15, 16, Enter Wait State
32 BIT MSC Instruction Starting on Odd Boundary	Microcode	Set MSC Program Exception Bit, Set Status Bits 14, 16. Enter Wait State
Attempt to Start Busy BCE, or @SIO with ACC[0]=1.	Microcode	Set MSC Program Exception Bit. Set Status Bits 11, 16. Continue Instruction.
Attempt to Load PC of Busy BCE, or @LBP with BCE number=0.	Microcode	Set MSC Program Exception Bit. Set Status Bits 12, 16. Continue Instruction.
Attempt to Load Base of Busy or halted BCE, or @LBB with BCE number=0.	Microcode	Set MSC Program Exception Bit. Set Status Bits 13, 16. Continue Instruction.
DMA Parity Error on Instruction Read	DMA Channel	Make up all 0's instruction and give to MSC. MSC will terminate with "Illegal Opcode" Interrupt CPU.
DMA Parity Error on Data Read, DMA timeout, Queue Overflow.	DMA Channel	No data is given to MSC. MSC loops indefinitely. Interrupt CPU.
IOP Faults IOP Microstore Parity Error, Clock Failure, Terminal Control plus watch-	IOP Hardware	MSC Halt bit set to 0, and MSC enters halt state. Interrupt CPU.

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dog timer time out,  
or fail latch set.

Self Test detected  
MSC fault

MSC Self-Test  
Instruction

Set MSC program exception  
bit. Set status bits 8,16.

Self-Test generated  
parity error.

IOP Hardware

Force all processors to the  
Halt state, set Busy/Wait  
bits of all processors to  
Wait.

NOTE: The MSC Program Exception bit registers an error when it is set to zero.

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## 3.0 MSC INSTRUCTIONS

The following subsections include descriptions of the instructions presently supported by the MSC. The format for the description of each instruction is as follows:

- o The general name of each instruction appears in the upper left of the first page describing that instruction.
- o The assembler abbreviation appears in the upper right hand corner.
- o The format of the instruction, including binary opcode assignments and field designations.
- o A table (where appropriate) relating addressing mode bits to their effect on parameters used in the instruction execution, and how these addressing modes are signalled to the assembler.
- o A textual description of the instruction and its uses.

These instructions are grouped into several classes with a short prologue at the beginning of each class. These classes include:

Paragraph

- 3.1 ACCUMULATOR/MEMORY INSTRUCTIONS
- 3.2 BRANCHING INSTRUCTIONS
- 3.3 CONDITIONAL SKIP INSTRUCTIONS
- 3.4 BCE REGISTER LOAD INSTRUCTIONS
- 3.5 MSC DIRECT REGISTER OPERATIONS
- 3.6 MSC REGISTER IMMEDIATE INSTRUCTIONS
- 3.7 REPEAT INSTRUCTIONS
- 3.8 SPECIAL INSTRUCTIONS

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3.1 ACCUMULATOR/MEMORY INSTRUCTIONS

The Accumulator/Memory Instruction set allows the 32-bit MSC Accumulator (ACC) to be modified by arguments found in memory, and for copies of the ACC to be stored in memory. Most of these instructions are short 16-bit formats of the form of Figure 1.2(a), and allow either PC relative or indexed PC relative addressing. Long format instructions of this class are as shown in Figure 1.2(c), and allow absolute addressing of memory.

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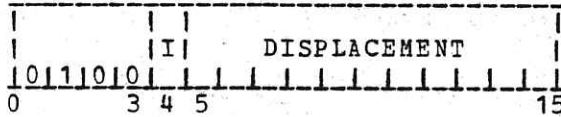
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LOAD ACCUMULATOR

@L

FORMAT:



I	Effective Address ("EA")	INSTR Format
0	PC + Displacement	@L ADDRESS
1	PC + Displacement + X	@L ADDRESS (1)

NOTE:

- 1) PC refers to the updated program counter value - i.e., the address of the next instruction.
- 2) Bit 5 is the sign of the two's complement displacement field. The range of the displacement is -1024 to +1023 halfwords.
- 3) X is the index register.

DESCRIPTION

The fullword operand addressed by EA is loaded into the accumulator. The program counter is incremented by one.

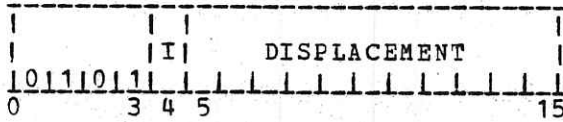
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ADD TO ACCUMULATOR

DA

FORMAT:



<u>I</u>	<u>Effective Address ("EA")</u>	<u>INSTR Format</u>
0	PC + Displacement	DA ADDRESS
1	PC + Displacement + X	DA ADDRESS(1)

NOTE:

- 1) PC refers to the updated program counter value - i.e., the address of the next instruction.
- 2) Bit 5 is the sign of the two's complement displacement field. The range of the displacement is -1024 to +1023 halfwords.
- 3) X is the index register.

DESCRIPTION

The fullword operand addressed by EA is added to the accumulator. The program counter is incremented by one.

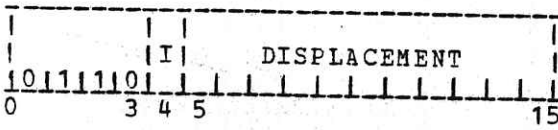
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@N

AND TO ACCUMULATOR

FORMAT:



I	<u>Effective Address ("EA")</u>	<u>INSTR Format</u>
0	PC + Displacement	@N ADDRESS
1	PC + Displacement + X	@N ADDRESS(1)

NOTE:

- 1) PC refers to the updated program counter value - i.e., the address of the next instruction.
- 2) Bit 5 is the sign of the two's complement displacement field. The range of the displacement is -1024 to +1023 halfwords.
- 3) X is the index register.

DESCRIPTION

The fullword operand addressed by EA is logically anded to the accumulator. The program counter is incremented by one.

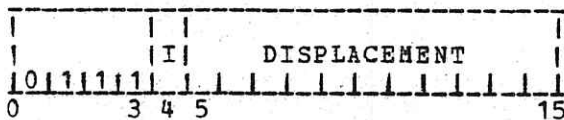
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EXCLUSIVE OR

@X

FORMAT:



<u>I</u>	<u>Effective Address ("EA")</u>	<u>INSTR Format</u>
0	PC + Displacement	@X ADDRESS
1	PC + Displacement + X	@X ADDRESS (1)

NOTE:

- 1) PC refers to the updated program counter value - i.e., the address of the next instruction.
- 2) Bit 5 is the sign of the two's complement displacement field. The range of the displacement is -1024 to +1023 halfwords.
- 3) X is the index register.

DESCRIPTION

The fullword operand addressed by EA is Exclusive Or'ed with the accumulator. The program counter is incremented by one.

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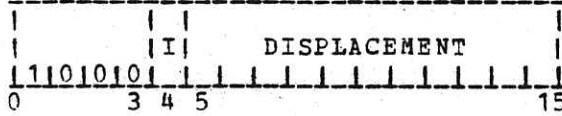
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STORE ACCUMULATOR

@ST

FORMAT:



I	Effective Address ("EA")	INSTR Format
0	PC + Displacement	@ST ADDRESS
1	PC + Displacement + X	@ST ADDRESS (1)

NOTE:

- 1) PC refers to the updated program counter value - i.e., the address of the next instruction.
- 2) Bit 5 is the sign of the two's complement displacement field. The range of the displacement is -1024 to +1023 halfwords.
- 3) X is the index register.

DESCRIPTION

A copy of the contents of the accumulator is stored in the fullword specified by EA. The accumulator is unchanged. The program counter is incremented by 1.

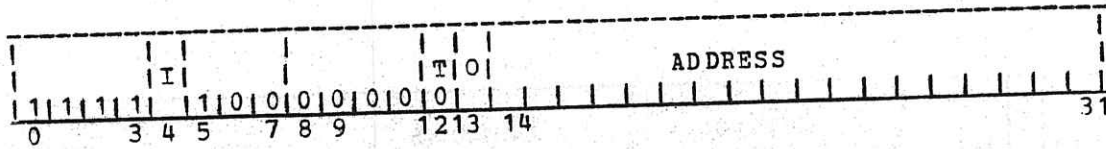
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LOAD ACC WITH FULLWORD

@LF

FORMAT:



I	EFFECTIVE ADDRESS (EA)	INSTR Format
0	Address	@LF ADDRESS
1	Address+X	@LF ADDRESS (1)

DESCRIPTION

This instruction loads the MSC Accumulator with a fullword from the memory location whose address is defined above. In a fullword load (T=0), the least-significant bit of the effective address is ignored.

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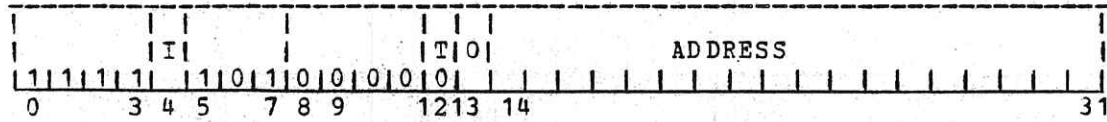




STORE ACC FULLWORD

@STF

FORMAT:



I	EFFECTIVE VALUE E.V.	INSTR Format
0	Address	@STF ADDRESS
1	Address+X	@STF ADDRESS (1)

DESCRIPTION

This instruction stores the MSC Accumulator into the memory location whose address is defined above. In a fullword store (T=0), the least-significant bit of the effective address is ignored and the entire MSC accumulator is stored in the addressed fullword.

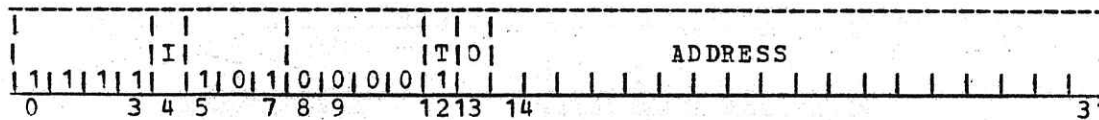
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STORE ACCUMULATOR HALFWORD

@STH

FORMAT:



I	<u>EFFECTIVE VALUE E.V.</u>	<u>INSTR Format</u>
0	Address	@STH ADDRESS
1	Address+X	@STH ADDRESS (1)

DESCRIPTION

This instruction stores the MSC accumulator into a memory location whose address is defined above. In a halfword store, the effective address is used as a complete halfword address. The lower 16 bits of the MSC Accumulator are stored in this halfword location.

PROGRAMMING NOTE:

In the above instruction format, any non-zero value in bits 8 thru 12 is treated as a valid "STORE HALFWORD" Opcode.

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### 3.2 BRANCHING INSTRUCTIONS

MSC instructions are normally executed in sequential order. A branch instruction allows a departure from this sequential operation. The branches included in the MSC instruction set provide mechanisms for conditional branches, unconditional branches and subroutine calls, and returns from external calls (See Appendix A).

The conditional branches are short format instructions of the form of Figure 1.2(b). This format provides an 8-bit signed displacement that is added to the PC if the specified condition is true.

The unconditional branches and subroutine calls are 32-bit long format, as shown in Figure 1.2(c). These instructions provide an absolute 18-bit address that is loaded into the MSC PC when the instruction is executed. As options, these addresses may be indexed or used as pointers to fullwords in memory containing the addresses. The latter option allows direct return from subroutines.

The instruction to return from an external call loads the MSC Accumulator, Index, and Status registers and in addition, causes the MSC to branch to a new location.

The result of executing any branch instruction places a new 18-bit address in the MSC PC. This address points to the next instruction to be executed, and may point to either an even or odd halfword boundary.

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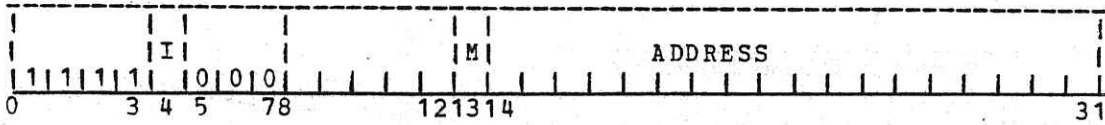




BRANCH UNCONDITIONAL

@BU

FORMAT:



I	M	EFFECTIVE VALUE E.V.	INSTR Format	
0	0	Address	@BU	ADDRESS
0	1	(Address)	@BU@	ADDRESS
1	0	Address + X	@BU	ADDRESS(1)
1	1	(Address + X)	@BU@	ADDRESS(1)

DESCRIPTION

The MSC program counter is loaded with the lower 18 bits of the effective value. A branch to either an even or odd halfword is permitted.

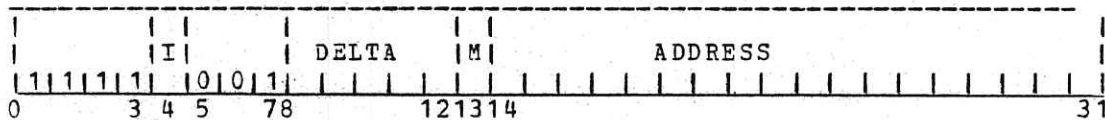
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SUBROUTINE CALL

@CALL

FORMAT:



I	M	EFFECTIVE VALUE E.V.	INSTR Format
0	0	Address	@CALL DELTA, ADDRESS
0	1	(Address)	@CALL@ DELTA, ADDRESS
1	0	Address + X	@CALL DELTA, ADDRESS (1)
1	1	(Address + X)	@CALL@ DELTA, ADDRESS (1)

DESCRIPTION

This instruction implements a subroutine call. The current value of the MSC program counter plus the five bit positive integer delta (bits 8-12) is stored in the fullword specified by the lower 18 bits of E.V. This quantity is zero padded on the left to fill the entire fullword. The MSC program counter is then loaded with the sum of the lower 18 bits of E.V. and two.

PROGRAMMING NOTE

This instruction is typically used to call a subroutine. A typical subroutine sequence is:

```

    .
    .
    .
    @CALL 4, SUB
    +
    .
    .
    .
    SUB      +0
    .
    .
    .
    @BU@ SUB
    .
    .
    .
    
```

ARGUMENT  
FIRST INSTRUCTION AFTER RETURN

USED FOR RETURN ADDRESS

SUBROUTINE BODY

SUBROUTINE RETURN

The effective value used in the subroutine call may be either even or odd. With an odd address, the least-significant bit is ignored when the return address is stored, but is considered when the

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branch is taken. Thus a @CALL 2,101 will cause the return address to be stored in fullword 100, but a branch to 103 will be taken.

As with any instruction that writes information into memory, the affected memory location must not be storage protected.

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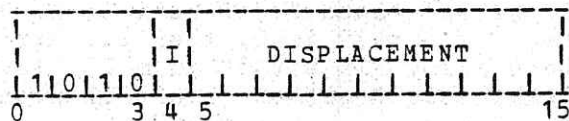
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RETURN FROM EXTERNAL CALL

@REC

FORMAT



I	<u>Effective Address ("EA")</u> 2	<u>INSTR Format</u>
0	PC1 + Displacement	@REC Address
1	PC1 + Displacement + X	@REC Address (1)

NOTE:

- 1) PC is updated PC, i.e. address of instruction following @REC.
- 2) EA is treated as a fullword address.

DESCRIPTION

This instruction loads the MSC Status Register, Accumulator, Index Register, and Program Counter from 4 consecutive fullwords starting at the memory location specified by EA. These registers are loaded as follows:

<u>Fullword Location</u>	<u>Register</u>
E.A. bits 14 to 31	MSC Status Register
E.A. + 2, bits 0 to 31	MSC Accumulator
E.A. + 4, bits 14 to 31	MSC Index Register
E.A. + 6, bits 14 to 31	MSC Program Counter

The load of the PC causes the MSC to branch to whatever location was specified by the contents of location E.A. + 6. Additionally the load of the Status Register also causes the MSC Program Exception Bit (bit 0 of STAT 1 Register) to be set to match the conditions indicated by bit 30 of the fullword addressed by E.A. If bit 30 is 1, then the Program Exception Bit is set to 0 (error logged into Status Register); if bit 30 is 0, then the Program Exception bit is set to 1 (no errors).

PROGRAMMING NOTE

This instruction allows an orderly and complete return to a program whose execution was suspended by the execution of a @SEC (Sample for External Call) instruction with a non-zero Local Store Register C6. The @SEC instruction should be seen for more detail on this use.

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An @REC may also be used to reload the MSC to a completely known state. This allows an MSC program to completely reset all registers including the Status Register, after it has found that, for example, it executed a @SIO with a busy BCE. However, care must be taken in such circumstances to make what is placed into the Status Register meaningful. Bit 31 of fullword addressed by EA must be 1 -- the MSC is still busy. Likewise, if bit 30 is 0, then all error indication in bits 25 to 29 should be 0 also. If bit 30 is a 1, then what is loaded into the rest of the Status Register should indicate the kind of error being flagged.

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3.3 CONDITIONAL SKIP INSTRUCTIONS

MSC instructions are normally executed in sequential order. A conditional skip instruction allows this normal sequential operation to be slightly modified. On the basis of some condition specified by the instruction, one or more sequential instructions following the conditional skip may be ignored. Execution is resumed at the instruction immediately following the skipped instructions.

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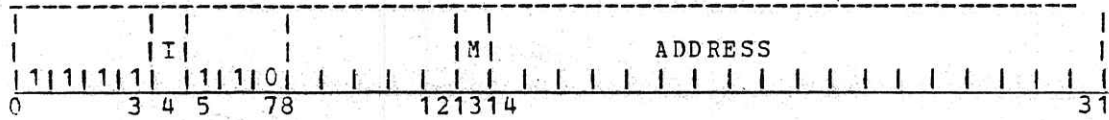
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COMPARE

@CI,@C

FORMAT:



M	EFFECTIVE VALUE E.V.	INSTR Format
0	Address*	@CI VALUE
0	(Address)	@C ADDRESS
1	Address + X*	@CI VALUE(1)
1	(Address + X)	@C ADDRESS(1)

\* This 18-bit quantity is treated as a two's complement number, and the most-significant bit is sign extended 14 places to the left to fill 32 bits.

DESCRIPTION

The 32-bit effective value is arithmetically compared to the accumulator. The present program counter is incremented by:

- +2 If ACC > E.V.
- +3 If ACC < E.V.
- +4 If ACC = E.V.

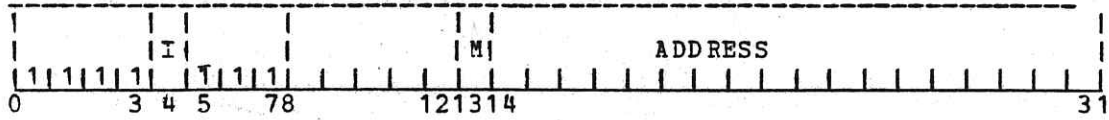
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TEST UNDER MASK

@TMI, @TM

FORMAT:



I	M	EFFECTIVE VALUE E.V.	INSTR Format
0	0	Address*	@TMI VALUE
0	1	(Address)	@TM ADDRESS
1	0	Address + X*	@TMI VALUE (1)
1	1	(Address + X)	@TM ADDRESS (1)

\* This 18-bit quantity is treated as a two's complement number, and is right-justified with 14 leading 1's to fill 32 bits.

DESCRIPTION

The effective value is logically anded with the accumulator. If the result is not zero, then the program counter is incremented by 3 (skip next halfword). Otherwise, the program counter is incremented by two (execute next instruction). The original accumulator contents are not changed by this instruction.

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3.4 BCE REGISTER LOAD INSTRUCTIONS

The MSC is responsible for initializing Bus Control Elements (BCE's) in the IOP. These operations include loading certain BCE registers, and starting BCEs. The instruction to start a BCE (@SIO) is listed under Register Operations. Those instructions listed in this section allow the MSC to initialize BCE Base and PC registers.

These instructions are long formats (Figure 1.2(c)), that specify which BCE is to be loaded, and an 18-bit absolute address to be loaded into the specified register. Options allow the number of the BCE to be loaded to come from either the instruction or the MSC Accumulator. Other options allow the 18-bit addresses to come directly from the instruction or from the lower 18-bits of a fullword from memory. Indexing may be specified to facilitate table lookups of these quantities.

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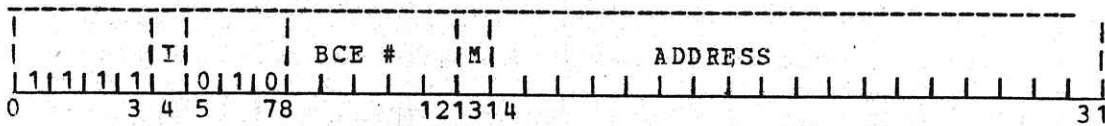
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LOAD BCE BASE REGISTER

@LBB

FORMAT:



I	M	EFFECTIVE VALUE E.V.	INSTR Format
0	0	Address	@LBB BCE, ADDRESS
0	1	(Address)	@LBB@ BCE, ADDRESS
1	0	Address + X	@LBB BCE, ADDRESS (1)
1	1	(Address + X)	@LBB@ BCE, ADDRESS (1)

DESCRIPTION

Field "BCE NUMBER" (Bits 8 through 12) specifies a BCE processor. If the field is non-zero, the field value selects the BCE. If the field is zero, the lower 5 bits of the MSC accumulator, (Bits 27 to 31) specify the desired BCE.

If the specified BCE is in the Wait State, the effective value, computed according to the above table, is stored in the BCE's base register. If the specified BCE is busy or is halted, bit 13 in the MSC status register is set, the MSC Program Exception bit is set to 0 (error), and nothing is done to the specified BCE processor.

In both cases, the MSC program counter is incremented by 2, and the next sequential instruction is executed.

PROGRAMMING NOTE

The IOP interprets a BCE number of 0 as the MSC, and consequently, if an @LBB instruction is executed with a final BCE number of 0 (a possibility only if the ACC = 0), the MSC will test itself and find itself busy. This results in the previously described error action being taken.

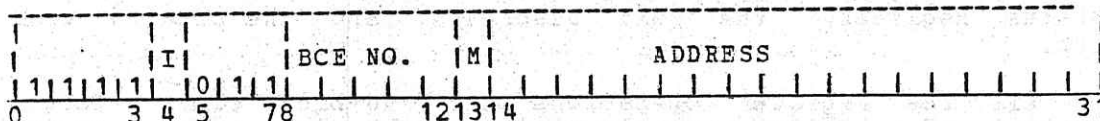
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LOAD BCE PROGRAM COUNTER

@LBP

FORMAT:



I	M	EFFECTIVE VALUE E.V.	INSTR Format
0	0	Address	@LBP BCE,ADDRESS
0	1	(Address)	@LBP@ BCE,ADDRESS
1	0	Address + X	@LBP BCE,ADDRESS(1)
1	1	(Address + X)	@LBP@ BCE,ADDRESS(1)

DESCRIPTION

Field "BCE NUMBER" (Bits 8 through 12) specify a BCE processor. If the field is non-zero, the field value selects the BCE. If the field is zero, the lower 5 bits of the MSC accumulator (bits 27 to 31) specify the desired BCE.

If the specified BCE is in the Wait State, the effective value, computed according to the above table, is stored in that BCE's program counter. If the specified BCE is busy or halted, bit 12 of the MSC status register is set, the MSC Program Exception bit is set, and nothing is done to the specified BCE processor.

In all cases, the MSC program counter is incremented by 2, and the next sequential instruction is executed.

PROGRAMMING NOTE

The IOP interprets a BCE number of 0 as the MSC, and consequently, if an @LBP instruction is executed with a final BCE number of 0 (a possibility only if the ACC = 0), the MSC will test itself and find itself busy. This results in the previously described error action being taken.

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3.5 REGISTER OPERATIONS

The MSC instruction set includes a class of instructions that allow the MSC to read or set various IOP registers, not all of which are associated with the MSC. These registers include the Busy/Wait register, the Program Exception Register, the BCE-MSD Indicators, the MSC Status Register, the Fail Discretes, and the External Call register.

All the Register Operations are 16-bit short format instructions of the form shown in Figure 1.2(b) with a common opcode of 1110, and an I-bit of 0. Each Register Operation has a separate OPX field, as shown in Table 3.1.

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TABLE 3.1

## LIST OF REGISTER OPERATIONS

<u>OPX</u>		<u>OPERATION</u>
0	LAR	Load MSC ACC with specified IOP register
1	SFD	Set Fail Discrete Register by ORing it with MSC accumulator bits 0,1,2,3 and 4.
2	RFD	Reset Fail Discrete Register A 1 in ACC Bit i will clear Fail Discrete Register Bit i. A 0 in the ACC causes no change.
3	LMS	Load MSC ACC with MSC Status Word.
4	SIO	Start BCE's by Or'ing accumulator with busy/wait register (STAT4). A one in bit position i of the ACC will place BCEi in busy state.
5	XAX	SWAP ACC AND X. The lower 18 bits of ACC go into X, and X is sign extended to fill ACC.
6	SEC	Sample for External Call. Check MSC Local Store register C6. If non-zero, save MSC register and branch to specified program.
7	RBI	Reset BCE indicator. Reset the specified BCE's indicator bit to 0.

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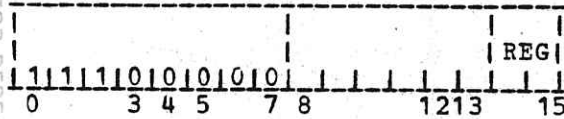
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## LOAD MSC ACC. WITH AN IOP STATUS REGISTER

@LAR

## FORMAT:

INSTR Format

@LAR REGISTER

## DESCRIPTION

This instruction allows the MSC ACC to be loaded, under program control, with a specified IOP register. The REG field determines which IOP register is involved. The following table summarizes the REG field assignments.

<u>REG</u>	<u>IOP REGISTER</u>
0	Program Exception Indicators - STAT 1
1	BCE-MS C Indicators
2	FAIL DISCRETES
3	BUSY/WAIT INDICATORS - STAT4

In all cases, bit *i* of the indicated register goes into bit *i* of the ACC. ACC bits with no corresponding IOP register bits are zero filled.

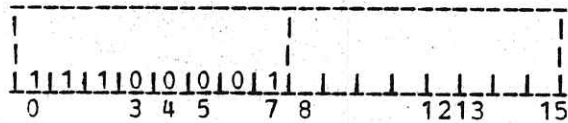
Fail Discrete register bits are assigned as follows:

Bit 0	-	MSC inhibit Fail Discrete outputs
Bit 1-4	-	Input Fail Discrettes 1-4
Bit 5-8	-	Output Fail Discrettes 1-4
Bits 9-31	-	Zero

SET FAIL DISCRETES

@SFD

FORMAT:



INSTR Format

@SFD

DESCRIPTION

This instruction allows the MSC ACC bits 0,1,2,3, and 4 to be logically OR'ed with the Fail Discrete register. Thus, a 1 in bit *i* of the ACC (*i*=1,2,3,4) will set the equivalent Fail Discrete bit. A 0 will cause no change.

Setting bit 0 will inhibit the output of the four fail discrettes from bits 1-4 of the four Fail Discrete registers, but will not affect the way these bits may be changed by @SFD or @RFD.

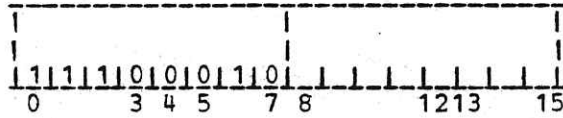
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RESET FAIL DISCRETES

@RFD

FORMAT:



INSTR Format

@RFD

DESCRIPTION

This instruction allows the Fail Discrete Register to be selectively reset. A 1 in MSC Accumulator bit  $i$  ( $i=0,1,2,3,4$ ) will cause bit  $i$  in the Fail Discrete Register to be reset. A 0 in the MSC Accumulator causes no change.

Resetting bit 0 of the Fail Discrete Register allows activation of the four fail discrettes from the Fail Discrete Register bits 1-4.

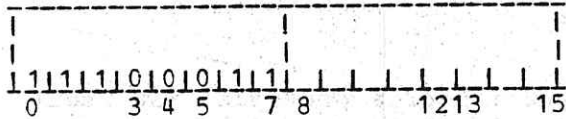
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## LOAD ACC WITH MSC STATUS

@LMS

## FORMAT:

INSTR Format

@LMS

## DESCRIPTION

This instruction allows the MSC ACC to be loaded under program control, with the MSC status word. The format of this status word as it is loaded into the ACC is as follows:

- Bit 31 STAT4 bit 0 - The Busy/Wait bit for the MSC.. It will always be 1 when this instruction is executed.
- Bit 30 STAT1 bit 0 - The Program Exception bit for the MSC. This bit will be set to 1 only if the execution of some previous instructions resulted in an error of some kind. Bits 29 through 26 catalog the exact error. Note that a 1 in this bit corresponds to a 0 in bit 0 of the Program Exception register. The converse is also true.
- Bit 29 Illegal opcode. If set, this bit indicates that an illegal opcode was encountered at some point in the past. Note that the only way this bit could be set when an @LMS is executed is if an illegal opcode was detected in the past, and the CPU restarted the MSC without clearing the status word first.
- Bit 28 Boundary alignment error. If set, this bit indicates that a long format instruction was encountered at an odd halfword boundary.
- Bit 27 LBB error. The BCE that was specified by a previous @LBB instruction was busy at the time the instruction was executed, and consequently its Base Register was not loaded.

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- Bit 26 LBP error. The BCE that was specified by a previous @LBP was busy at the time the instruction was executed, and consequently its Program Counter was not loaded.
- Bit 25 SIO error. A previous execution of a @SIO instruction tried to set busy at least one BCE that was already busy.
- Bit 24,23 Reserved
- Bit 22 Self-Test Fault. The execution of a previous MSC self test instruction detected a fault in the MSC.
- Bits 21-14 Reserved.
- Bits 13-0 Set to zero.

## PROGRAMMING NOTE

The MSC Status Register may be set to any desired value as part of the execution of a Return From External Call (@REC) instruction.

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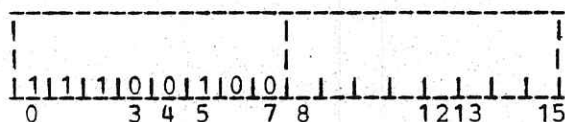
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START I/O

@SIO

## FORMAT:

INSTR Format

@SIO

## DESCRIPTION

This instruction starts execution of BCE's by ORing the Accumulator with the Busy/Wait register (STAT4). A 1 in bit position *i* of the ACC will place BCE(*i*) in a busy state.

If any of the BCE's designated by the ACC are already busy (their bit in the Busy/Wait Register is already set) bit 11 of the MSC Status Register is set and the MSC Program Exception bit is set.

In any case, the ACC is still OR'ed into STAT4 and the next sequential instruction is executed.

## PROGRAMMING NOTE

Bit 0 of STAT4 is the MSC Busy/Wait bit, and is set to 1 whenever the MSC is executing instructions. Consequently, execution of this instruction with a 1 in bit 0 of the ACC will cause the error status bits to be set (Program Exception bit and Status Register bit 11). As before, execution continues with the next instruction.

Although an @SIO instruction will set a BCE's Busy/Wait bit to busy within the time frame of the instructions' execution in the MSC, the BCE will not necessarily begin immediate execution of the first instruction.

## Possible execution delays include:

- 1) The time required for the BCE to recognize that its Busy/Wait bit is set (up to 16.5 usec).
- 2) The time required to bring out the PC and request the instruction word from memory (up to 33 usec.)

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- 3) Any time required for the memory read request to reach the DMA channel, be read from memory and be returned to the BCE.

The last case delays the BCE setup only when it requires over 16 usecs to be handled. This may occur whenever several BCE/MSD processors have requested memory reads at the same time.

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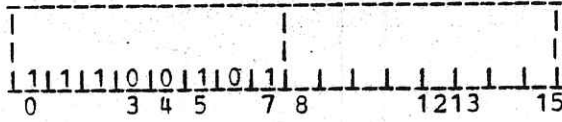
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EXCHANGE ACC AND X

@XAX

FORMAT:



INSTR Format

@XAX

DESCRIPTION

This instruction allows a swap between ACC and X. The lower 18-bits of the ACC go into X, and X is sign extended to fill the ACC.

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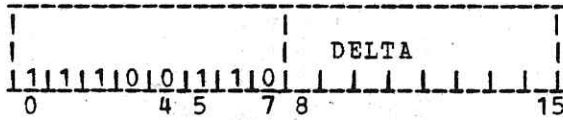
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## SAMPLE FOR EXTERNAL CALL

@SEC

## FORMAT:

INSTR Format

@SEC ADDRESS

## NOTE:

Address = PC + DELTA, where PC is updated Program Counter and DELTA is an integer between -128 and 127.

## DESCRIPTION:

In conjunction with the MSC instruction, Return from External Call (@REC), this instruction allows the CPU to request that the MSC suspend execution of its present program and initiate a new one. Further, the suspension of the present program is done in a fashion that allows an orderly return to it once the CPU-designated program is complete. The program specified by the CPU is termed an "external call".

The point of communication between the MSC and the CPU is MSC Local Store Register C6. To request a program to be executed, the CPU loads C6 with the (fullword) address of the program's start in main memory. Whenever the MSC executes an @SEC it samples C6. If C6 is zero, the MSC continues with the next instruction. The @SEC is a no-operation in this case.

If, however, the MSC finds a non-zero C6 when it executes an @SEC, it takes the contents as a main memory address, and stores in the 4 fullwords addressed by C6 the following quantities:

- \*Fullword C6 -- MSC Status Register right justified and padded on left with 0's.
- Fullword C6 + 2 -- MSC Accumulator
- Fullword C6 + 4 -- MSC Index Register right justified and padded on left with 0's.

\*If C6 is odd, registers are stored on EVEN word boundaries (Low Order Address bit is ignored).

Fullword C6 + 6 -- MSC Program Counter plus DELTA right justified and padded on left with 0's. (PC is updated PC, i.e. points to next instruction after @SEC.)

These quantities are used by @REC at the end of the new program to restore the MSC to its original condition.

After this, PC is loaded with C6 + 8, C6 is zeroed, the MSC Status Register is set to 1 (busy but no errors) and the MSC Program Exception bit (bit 0 of STAT 1) is set to 1 (no errors). The MSC thus branches to the program beginning at C6 + 8 with a clean status. Any errors made by the MSC while executing this new program will be reflected in the Status Register, but with no confusion with the status of the original program. Note that if C6+8 points to an odd halfword, the MSC will branch to that halfword.

The fullword at C6 + 6 contains the return address to the program containing the @SEC. Adding the DELTA field to PC when the store is made allows the original program the option of being informed when an external call is actually taken. A 0 DELTA will always return the MSC to the instruction immediately following the @SEC with the result that the MSC program would never know when a call was taken. A non-zero DELTA will return the MSC to a programmer-specified location after the CPU specified program is complete. This would allow, for example, the original MSC program to update a timer or clock to take into account the time spent in the CPU specified program.

Once C6 has been zeroed, the CPU is free to reload it again with another program address, which in turn will be accepted by the MSC the next time it executes an @SEC.

PROGRAMMING NOTE

Figure 3.1 lists a possible MSC program segment using @SEC's. The @SEC at location 100 allows an external call from the CPU to be accepted, but with a 0 DELTA, control will always return to 101.

Following 100 is a section of code that monitors the STAT 4 (Busy/ Wait) Register for a maximum of about 10 msec. This could be done by a single @RAW with a time out count of about 300. However, CPU issued external calls would be ignored for the entire 10 msec. period. The segment shown here waits at most 1 msec. between @SEC's. It executes a @RAW for about 1 msec. and then branches to 300 where an @SEC permits the acceptance of a CPU-specified external call. If no external call is present, the @TSZ at 301 increments a counter

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(initialized to -10) and returns to repeat the @RAW if less than 10 msec. have passed. If an external call is taken at 300, the non-zero DELTA will cause the return from the call to be to location 310 where the counter is decremented an extra time to account for time spent in the external call. This can obviously be elaborated if more accurate timing is required.

Also on Figure 3.1 is an outline of a MSC program "PGM" that may be started by an external call. The first four fullwords are allocated to holding the MSC registers at the time of the @SEC. The program to execute the desired function starts at PGM + 8 and ends with the @REC PGM, which returns the MSC to the original program.

Section 4.0, External Calls, contains further information on the use of the @SEC instruction.

As with any instruction that writes information into memory, the affected memory locations (C6,C6+2,C6+4,C6+6) must not be storage protected.

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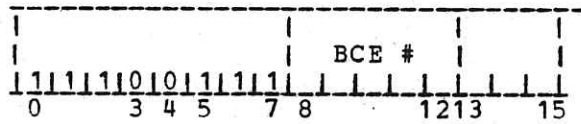
<u>LOCATION</u>	<u>INSTRUCTION</u>	<u>COMMENT</u>
Main Program:		
100	@SEC 0	
	@LI -10	Initialize REPEAT
	@S COUNT	Count.
200 LOOP:	@DRAW 30	Watch for some condition
201	@BC 0, TIMECHECK	-time out
202		Condition fulfilled
300 TIMECHECK:	@SEC UPDATETIME	Allow an interrupt
301	@TSZ COUNT	decrement timer
302	@BC 0, LOOP	timer not zero yet
303 TIMEOUT:		COUNT reached 0
	Start of timeout routine	
310 UPDATETIME:	@TSZ COUNT	An interrupt was taken,
311	@BC 0, TIMECHECK + 1	decrement clock one
312	@BC 0, TIMEOUT	extra time.
Program specified by External Call		
400 PGM:	DS 4F	Allocate 4 fullwords of
401		storage for MSC Registers.
		Execute desired function
	@REC PGM	Return to original
		MSC Program

Figure 3.1. Sample Code Using @SEC



@RBI

## RESET BCE INDICATOR

INSTR Format

@RBI      BCE#

## DESCRIPTION

This instruction resets the specified BCE's BCE/MSC indicator bit to zero. For BCE *i*, this is bit *i* of the BCE/MSC indicator register. If the BCE specified in the instruction word is zero, the lower 5 bits of the MSC Accumulator (bits 27-31) indicate the desired BCE.

After resetting the specified indicator bit, the MSC increments its Program Counter by 1 and continues with the next sequential instruction.

## PROGRAMMING NOTE

No check is made as to whether or not the specified BCE number is valid (i.e., between 1 and 24). If the specified BCE does not exist, this instruction is effectively a "no-operation".

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3.6 REGISTER IMMEDIATE INSTRUCTIONS

Many common programming sequences involve the use of small constants in operations involving the MSC ACC and X registers. To facilitate such operations without the penalty of constant references to memory, the MSC instruction set includes a class of 16-bit short format instructions that has, as part of the instruction, an 8-bit signed integer. All such instructions have the format shown in Figure 1.2(b), with an opcode of 1110 and an I-bit of 1. The OPX field determines what is to be done with the constant found in bits 8 through 15 of the instruction. Table 3.2 lists the OPX fields and their interpretation.

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TABLE 3.2

## REGISTER IMMEDIATE INSTRUCTION

<u>OPX</u>		<u>OPERATION</u>
0	@NIX	Normalize and Increment X. The ACC is shifted left until it becomes $\leq 0$ . Each time the ACC is shifted X is incremented by the Immediate constant.
1	@TAX	Tally Accumulator to X. Store the sum of the Immediate and ACC into X.
2	@TXI	Tally X. Add Immediate to X. If result is $\leq 0$ , skip next instruction.
3	@LXI	Load X Immediate. Load the X register with the Immediate constant.
4	@TXA	Tally X to ACC. The sum of the X register and the Immediate constant is loaded into the Accumulator.
5	@TI	Tally Accumulator Immediate. The Immediate constant is added to the ACC.
6	@SAI	Subtract ACC from Immediate. The Immediate constant minus the Accumulator is loaded into the Accumulator.
7	@LI	Load Immediate. The Immediate constant is loaded into the Accumulator.

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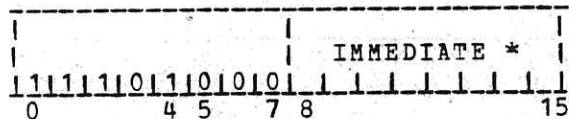
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NORMALIZE AND INCREMENT X

@NIX

FORMAT:



\* Two's complement number between -128 and +127. Forms a 32-bit constant by sign extending bit 8.

INSTR Format

@NIX IMM

DESCRIPTION

The NIX instruction shifts the ACC left until either the ACC sign bit (bit 0) is one, or the ACC. equals zero. Each time the ACC is shifted, the signed immediate value is added to the index register X. The shift and increment operation is done before either test. If the ACC. reaches zero, the index register is cleared. The following figure flowcharts the operation of this instruction.

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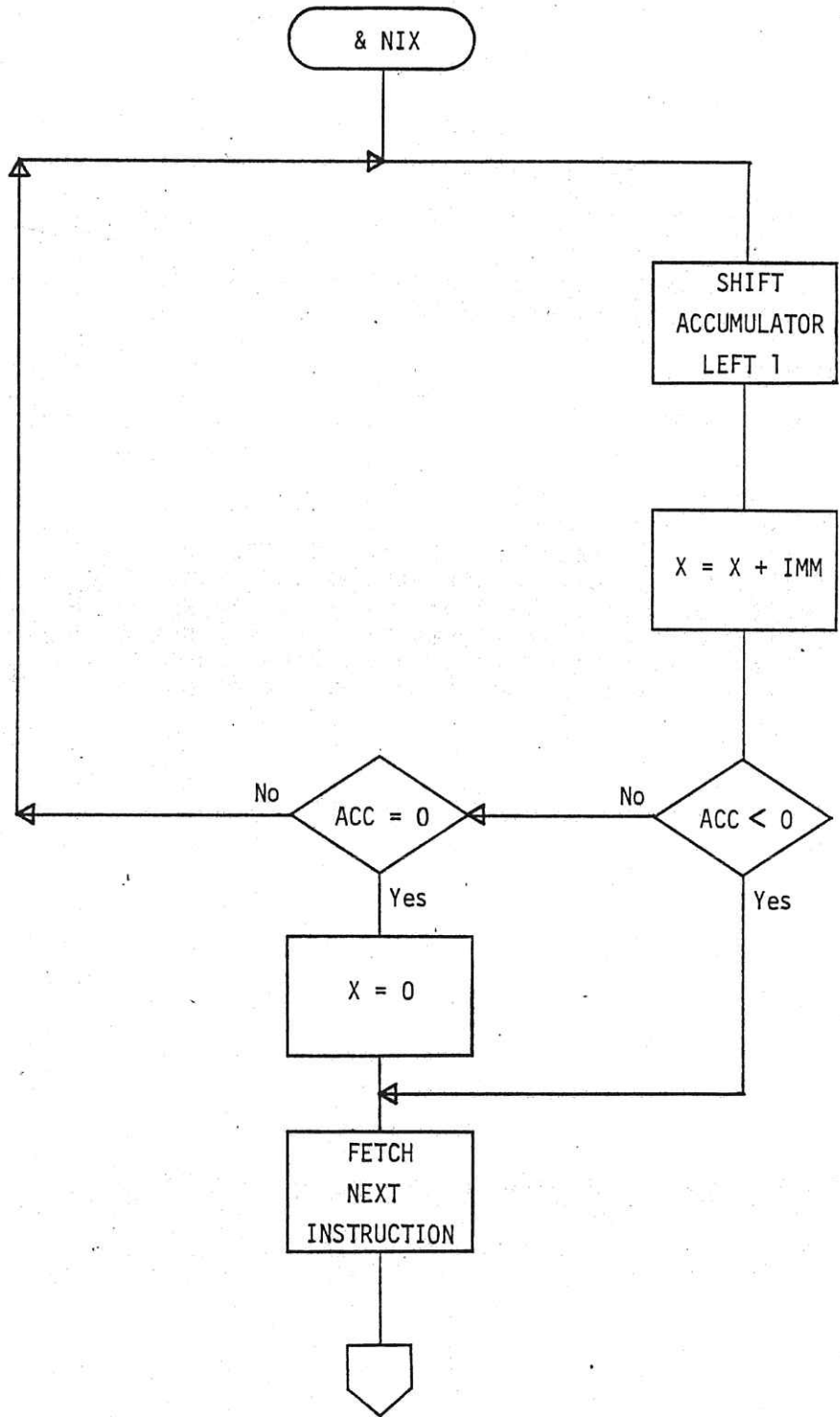


Figure 3.2 & NIX Instruction Execution

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## PROGRAMMING NOTE

A typical use of the NIX instruction would be to determine which BCE's have set their NOGO bit. The following sequence performs this process:

```

      .
      .
      .
LOOP: @LXM      0      INITIALIZE X TO ZERO
      @LAR      0      LOAD ACC WITH GO/NOGO BITS
      @SAI     -1      INVERT SO THAT: 1=ERROR, 0=OK
      @NIX      1      FIND NEXT BAD BCE
      @BC       4,DONE  EXIT WHEN NO MORE
      .
      .
      .

```

PROCESS BAD BCE. X REG. CONTAINS BCE NUMBER. NOTICE THAT FIRST EXECUTION OF NIX BYPASSES MSC POSITION WITH INITIAL SHIFT, AND ALL FUTURE NIX'S ELIMINATE BCE PROCESSED ON PREVIOUS ITERATIONS.

```

      .
      .
      .
@BU      LOOP

```

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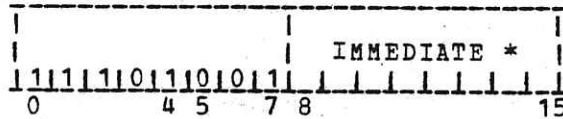
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TALLY ACC TO X

@TAX

FORMAT:



\* Two's complement number. Between -128 and +127. Forms a 32-bit constant by sign extending bit 8.

INSTR Format

@TAX IMM

## DESCRIPTION

The Lower 18 bits of the sum of the ACC and the IMM field is stored in the Index Register (X). An IMM value of 0 permits X to be loaded directly from the ACC. The ACC is unchanged.

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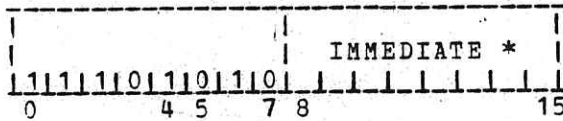
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TALLY X

@TXI

FORMAT:



\* Two's complement number. Between -128 and +127. Forms a 32-bit constant by sign extending bit 8.

INSTR Format

@TXI IMM

DESCRIPTION

The TXI instruction allows the Index Register plus IMM to be loaded back into X. If the new X is  $\leq 0$  the next halfword instruction is skipped. (program counter incremented by 2). Otherwise, the next halfword instruction is executed (program counter incremented by 1).

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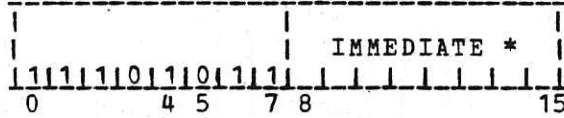
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LOAD X IMMEDIATE

@LXI

FORMAT:



\* Two's complement number. Between -128 and +127. Forms a 32-bit constant by sign extending bit 8.

INSTR Format

@LXI IMM

DESCRIPTION

The LXI instruction allows the data in IMM (sign extended to 18 bits) to be loaded into the Index Register (X). The MSC program counter is incremented by 1.

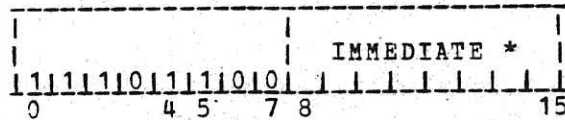
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TALLY X TO ACC

@TXA

FORMAT:



\* Two's complement number. Between -128 and +127. Forms a 32-bit constant by sign extending bit 8.

INSTR Format

@TXA IMM

## DESCRIPTION

The TXA instruction allows the X plus IMM to be stored in ACC (sign extended to 32 bits) IMM equal to zero allows sign extended X to be stored in ACC. X is treated as an 18-bit two's complement number with the sign in its most-significant bit. The MSC program counter is incremented by 1. The contents of X are not changed.

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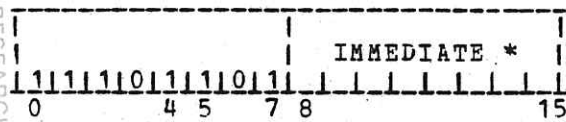
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@TI

TALLY ACC IMMEDIATE

FORMAT:



\* Two's complement number. Between -128 and +127. Forms a 32-bit constant by sign extending bit 8.

INSTR Format

@TI IMM

DESCRIPTION

The TI instruction allows ACC plus IMM (sign extended to 32 bits) to be loaded in ACC. The MSC program counter is incremented by 1.

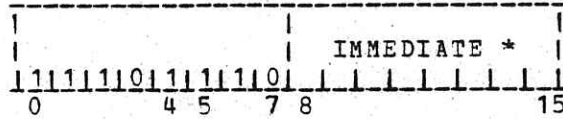
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SUBTRACT ACC FROM IMM

@SAI

FORMAT:



\* Two's complement number. Between -128 and +127. Forms a 32-bit constant by sign extending bit 8.

INSTR Format

@SAI IMM

DESCRIPTION

The SAI instruction allows the contents of the ACC to be subtracted from IMM (sign extended to 32 bits) and loaded in ACC. If IMM is equal to zero, a two's complement of ACC is performed. If IMM is equal to minus one, a one's complement of ACC is performed (each bit is inverted). The MSC program counter is incremented by 1.

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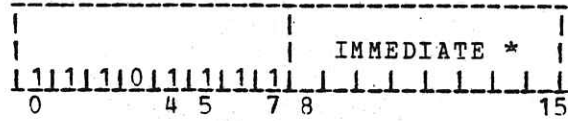
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## LOAD ACCUMULATOR IMMEDIATE

@LI

FORMAT:



\* Two's complement number. Between -128 and +127. Forms a 32-bit constant by sign extending bit 8.

INSTR Format

@LI IMM

## DESCRIPTION

The LI instruction allows the contents of IMM (signed extended to 32 bits) to be loaded into ACC. The MSC program counter is incremented by 1.

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### 3.7 REPEAT INSTRUCTIONS

One of the major tasks of the MSC is to monitor the BCEs. A typical MSC program involves initiating and starting some BCEs and then waiting for the BCEs to complete their assigned tasks. The Repeat Instructions perform this task directly, namely they wait until a set of BCEs specified by the ACC reach some condition. In addition, they include a programmable time-out check to prevent them from waiting indefinitely if some BCE never reaches the desired state.

All Repeat instructions use the same 16-bit short formats (Figure 1.2(b)) with an Opcode of 1101. The lower 8-bits, bits 8 through 15, and the I-bit are used to compute a count of the maximum time the instruction will spend waiting. If the time is exceeded, the next sequential instruction is executed. If the desired condition is reached before the time out, the next halfword instruction is skipped. Figure 3.3 diagrams the operation of any Repeat.

A time out value of zero will cause the Repeat instruction to test once, and only once, for the desired condition. If the condition is true, the next instruction is skipped. If the condition is false, the next instruction is executed.

A non-zero time out value will cause the specified test to be tried three times every 33 usec, or roughly, once every eight microseconds with 8 usec used to check for a time out. Every 33 usec the time out value is decremented, and the test is repeated until either the time out value reaches zero or the desired condition is reached.

A 33 usec period corresponds roughly to the rate at which a BCE can transmit or receive a word of data. This allows the programmer to estimate the time a Repeat should loop by analyzing how many data words are transferred through the MIA's by the relevant BCE's before the desired condition is reached. This time out value must also take into account the time required by BCE's to fetch and execute any none transmit/receive instructions that might be present in the BCE program.

The OPX field determines exactly which condition will be tested. These conditions are listed in Table 3.3.

#### PROGRAMMING NOTES:

An accumulator value of 0 will cause both the @RAI and @RAW to reach their specified conditions the first time that the test is made. Consequently, the PC will be incremented by 2 and the next halfword skipped. A zero accumulator will never allow an @RNI or @RNW to reach their repeat conditions. Consequently, each repeat will loop

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until the maximum repeat count is reached, at which point the next sequential instruction is begun.

Since processor 0 corresponds to the MSC, (which is busy during instruction execution), the MSC execution of an @RAW instruction will correspond to a loop until the maximum repeat count is reached.

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TABLE 3.3  
REPEAT INSTRUCTIONS

<u>OPX</u>		<u>CONDITION</u>
000	ØRAW	Repeat until all BCEs for which there is a 1 in the ACC reset their Busy/Wait bits to Wait.
001	ØRNW	Repeat until any BCEs for which there is a 1 in the ACC reset their Busy/Wait bits to Wait.
100	ØRAI	Repeat until all BCEs for which there is a 1 in the ACC set their BCE-MSK Indicators to 1.
101	ØRNI	Repeat until any of the BCEs for which there is a 1 in the ACC set their BCE-MSK Indicators to 1.

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T1 = Minor Loop (33 usec) Timer

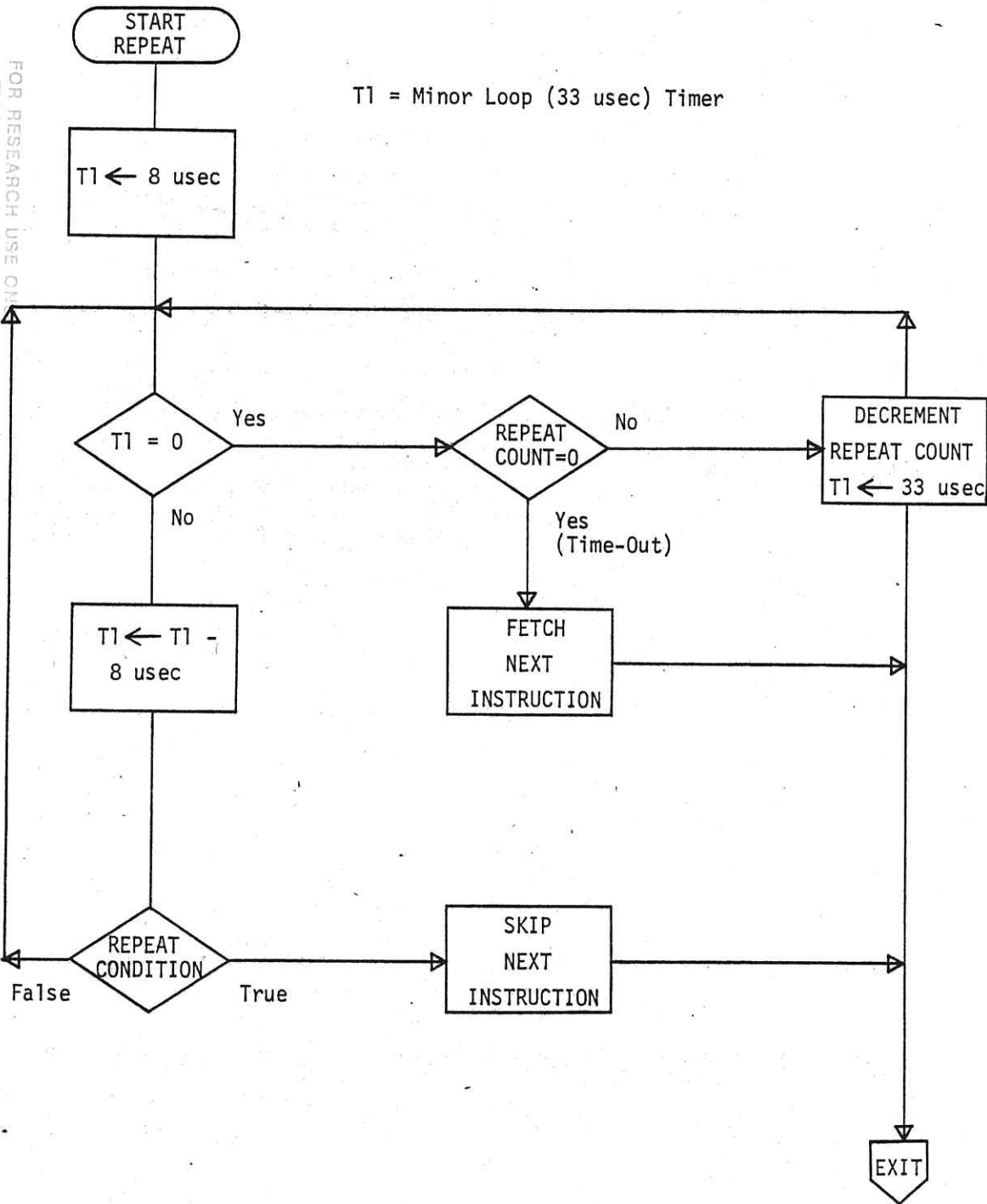


Figure 3.3 General Repeat Instruction Execution

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REPEAT UNTIL ALL INDICATORS

@RAI

FORMAT:

-----															
1	1	1	1	0	1	1	1	0	1	0	1	1	1	1	1
0		3	4	5		7	8								15

<u>I</u>	<u>MAXIMUM REPEAT COUNT</u>	<u>INSTR Format</u>
0	Count	@RAI COUNT
1	X + Count	@RAI COUNT(1)

## DESCRIPTION

This instruction causes a delay in MSC program execution until either:

- 1) All of a set of specified BCE's have set their BCE - MSC indicator bits to 1.
- 2) A maximum wait time has been reached.

If condition 1) is reached before the time out, the MSC skips the next halfword instruction and resumes program execution. If the maximum wait time, as specified by the maximum repeat count, is reached first, the MSC begins execution of the next halfword instruction.

The condition "are all specified BCE indicator bits set" is tested by logically ANDING the MSC accumulator with the complement of the BCE-MSC indicator register. If the result is all zeros, the desired condition has been reached.

The maximum wait time has a basic resolution of 33 microseconds and is derived from the maximum repeat count. In non-index mode, the maximum repeat count of 255 corresponds to a maximum wait time of 8.4 milliseconds. In index mode, the maximum possible count of 262143 corresponds to 8.65 seconds.

At the time this instruction is executed, the MSC accumulator is presumed to contain a bit mask specifying which BCE's are to be involved in the test for the desired repeat condition. A 1 in bits i of the accumulator specifies that the status of BCE(i) is to be included in the test; a 0 indicator that BCE(i) can be ignored.

Figure 3.3 diagrams the exact operation of this and the other Repeat instructions.

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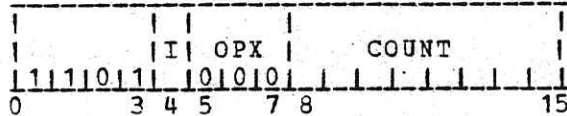
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REPEAT UNTIL ALL WAITING

@RAW

FORMAT:



I	MAXIMUM REPEAT COUNT	INSTR Format
0	Count	@RAW COUNT
1	X + Count	@RAW COUNT(1)

## DESCRIPTION

This instruction causes a delay in MSC program execution until either:

- 1) All of a set of specified BCE's have set their busy/wait status bits to "wait"
- 2) A maximum wait time has been reached.

If condition 1) is reached before the time out, the MSC skips the next halfword instruction and resumes program execution. If the maximum wait time, as specified by the maximum repeat count, is reached first, the MSC begins execution of the next halfword instruction.

At the time this instruction is executed, the MSC accumulator is presumed to contain a bit mask specifying which BCE's are to be involved in the test for the desired repeat condition. A 1 in bit i of the accumulator specifies that the status of BCE(i) is to be included in the test; a 0 indicates that BCE(i) can be ignored.

The maximum wait time has a basic resolution of 33 microseconds and is derived from the maximum Repeat count. In non-index mode, the maximum Repeat count of 255 corresponds to a maximum wait time of 8.4 milliseconds. In index mode, the maximum possible count of 262143 corresponds to 8.65 seconds.

The condition "are all specified BCE's waiting" is tested by logically ANDING the MSC accumulator with STAT4 (the Busy/Wait register), and testing for all zeros. A 1 in bit i of STAT4 indicates that BCE(i) is busy; a 0 indicates that it is not. Consequently, if

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the result of this "and" operation is all zeros, then all the specified BCE's will be in the desired state.

Figure 3.3 diagrams the exact operation of this and the other Repeat instruction.

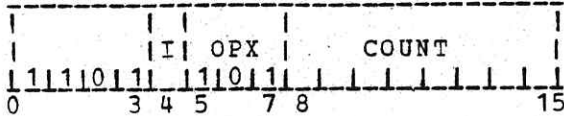
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REPEAT UNTIL ANY INDICATORS

@RNI

FORMAT:



I	MAXIMUM REPEAT COUNT	INSTR Format
0	Count	@RNI COUNT
1	X + Count	@RNI COUNT(1)

DESCRIPTION

This instruction causes a delay in MSC program execution until either:

- 1) Any of a set of specified BCE's have set their BCE-MSD indicator bits to 1 or,
- 2) A maximum wait time has been reached.

If condition 1) is reached before the time out, MSC skips the next halfword instruction and resumes program execution. If the maximum wait time; as specified by the maximum repeat count, is reached first, the MSC begins execution of the next halfword instruction.

The condition "are any of the specified BCE indicators set" is tested by logically ANDING the MSC accumulator with the BCE-MSD indicator register. If the result is non-zero, the desired condition has been reached.

The maximum wait time has a basic resolution of 33 microseconds and is derived from the maximum Repeat count. In non-index mode, the maximum Repeat count of 255 corresponds to a maximum wait time of 8.4 milliseconds. In index mode, the maximum possible count of 262143 corresponds to 8.65 seconds.

At the time this instruction is executed, the MSC accumulator is presumed to contain a bit mask specifying which BCE's are to be involved in the test for the desired repeat condition. A 1 in bit i of the accumulator specifies that the status of BCE(i) is to be included in the test; a 0 indicates that BCE(i) can be ignored.

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Figure 3.3 diagrams the exact operation of this and the other Repeat instructions.

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of the accumulator specifies that the status of BCE(i) is to be included in the test; a 0 indicates that BCE(i) can be ignored.

Figure 3.3 diagrams the exact operation of this and the other Repeat instructions.

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3.8 SPECIAL INSTRUCTIONS

In addition to the instructions described earlier, the MSC instruction set includes a variety of instructions that place the MSC in the Wait state, delay MSC execution for program-settable periods of time, and cause an interrupt in the CPU. This section describes these instructions.

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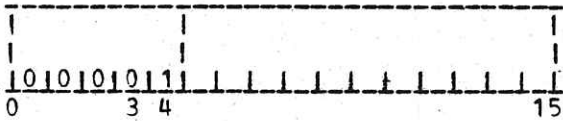
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WAIT

@WAT



DESCRIPTION

This instruction causes the MSC to go into the WAIT state (bit 0 of STAT4 and bit 17 of the MSC Status Register set to zero). No more instructions are executed. The MSC program counter is updated to point to the next instruction. No other MSC register is changed.

PROGRAMMING NOTE

The MSC does not reference any of its Local Store registers once it is in the Wait State. During this time, the CPU is free to PCO or PCI any MSC register. However, once the CPU performs a PCO (to set the MSC busy), the MSC will detect the setting of its busy bit within 2 microseconds, and will use whatever is in its PC as the address of the first instruction. Therefore, once the MSC has been set to busy, CPU PCOs to the MSC Local Store should be avoided.

Note that if there is no PCO to the MSC's PC (MSC Local Store register A2), then the MSC will start with the first instruction following the last #WAT instruction.

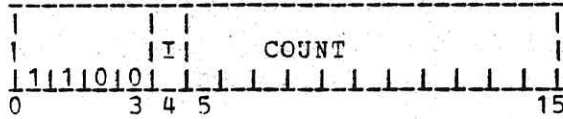
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DELAY

@DLY

FORMAT:



I	<u>Effective Count ("EC")</u>	<u>INSTR Format</u>
0	Displacement	@DLY COUNT
1	X+Displacement	@DLY COUNT(1)

NOTE:

- 1) Displacement is a positive number in the range 0 to 2047.
- 2) X refers to the index register.

DESCRIPTION

This instruction performs no operation other than delaying the execution of the next instruction. The time period delayed is indicated by the 18-bit EC, with a resolution of 2 microseconds. The maximum delay is roughly .54 sec. At the end of this delay, the program counter is incremented by one, and the next instruction is executed.

Note that after every eighth MSC microcycle the time between MSC microcycles is 2.5, not 2, microseconds.

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6246556A

16  
16  
16  
16

4  
3  
2  
1

UNASSIGNED

09  
08  
07  
06  
5-0

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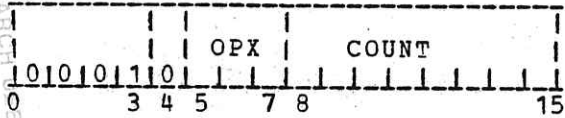
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@STP

## SELF TEST - MSC\*

## FORMAT:

INSTR Format

@STP

## NOTE:

- 1) The COUNT field is at a don't care state unless the OPX field equals 001.
- 2) Use of the OPX field selects one of three tests as follows:
  - a) OPX = 000 - Normal STP sequence
  - b) OPX = 001 - Queue-overflow test
  - c) OPX = 010 - ROS parity error test

## DESCRIPTION

If OPX equals 000, this instruction initiates execution of a special micro program to perform self tests on the hardware supporting the MSC. These tests include checks of the:

- 1) MSC Local Store Registers
- 2) MSC Data Flow operations
- 3) Ability of MSC to read and write from memory
- 4) Redundancy Management Fail discrettes
- 5) IOP ROS parity circuit.

If any faults are detected, the MSC Program Exception bit is set to 0 (fault detected) and the MSC status registers bit 8 is set to 1 (Self Test failure).

In any case, after completion of these tests, the MSC updates its Program Counter by 1 and continues with the next instruction.

If OPX equals 001, the instruction performs a queue-overflow test by placing the number of memory requests specified by the COUNT field in the queue. If the queue overflows, the channel interrupts the CPU and the request is lost. The program loops on this instruction.

If OPX equals 010, the instruction receives a bad-parity micro-word. This sets the HALT bit of all processors and sets BUSY/WAIT to WAIT.

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## 4.0 EXTERNAL CALLS

The MSC allows the CPU to request the MSC to suspend execution of its current program and to start another program. When this action is undertaken, the MSC saves enough information to allow a full restart of the displaced program at the point of suspension. The stored information is similar to that stored by the CPU when it is interrupted. However, unlike an interrupt, the CPU specified program will only be recognized by the MSC at the discrete instances when the MSC is executing a Sample For External Call (@SEC) instruction. The CPU requested superseding program is termed an 'external call'.

The contact point between the MSC and the CPU is the MSC Local Store Location C6 - The External Call Register (ECR). When the CPU wishes the MSC to perform an 'external call', it should perform a PCO to write the starting address of the requested program into the MSC. If the MSC has been programmed to accept external calls, it will periodically execute an @SEC that will sample the ECR. If it finds a 0 in the ECR, it will continue with the next instruction. In this case, the @SEC is equivalent to a "no operation".

If the MSC finds a non-zero ECR, it uses the value in the ECR as a memory address and stores its Accumulator, Index, Program Counter, and Status Registers in the four words following this memory address. It will also clear the Status Registers and Program Exception bit of any error flags that they might contain. Program execution begins at the fifth fullword after the ECR (ECR+8). The MSC will also clear the ECR to zero. Register storage is defined in this document's description of the @SEC instruction.

The clearing of the ECR by the MSC may be used by the CPU as an indication that the MSC has accepted an external call, and that the CPU is now free to PCO out a new external call address, if it so desires. Any attempt by the CPU to PCO out a new external call before the MSC resets the ECR to zero will result in at least one of the external calls being lost. Therefore, the CPU should check that the ECR is zero before PCO'ing a new external call address.

An externally called program may return to the original program at any time by executing a Return from External Call (@REC) instruction. This instruction reloads the MSC Accumulator, the Program Counter, the Index Register, the Status Register, and the Program Exception bit to the exact condition that they were in at the time the original @SEC instruction accepted the External Call. This allows the original MSC program to continue as if no external call had been accepted.

The description of the @REC instruction indicates which memory words are loaded into what MSC registers.

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The reason for clearing the MSC Status Register and Program Exception bit to an error free indication, after an @SEC has found a non-zero ECR and before entering the requested program, is to avoid confusing an original program error with any error the external call program may make. If the externally called program performs any erroneous operations (such as attempting to start a busy BCE) the error will be flagged in the Status Register and may be detected and diagnosed in the usual fashion. Yet, when the MSC returns to the original program, via an @REC, the Status Register will contain only the original program error indicators and none from the externally called program. The original program can proceed with no concern for sorting out what, if any, errors it made and what, if any, errors any externally called program may have made.

As mentioned before, the MSC will accept external calls only when it executes @SECs. Consequently, if external calls are expected, the operational MSC programs should include periodic @SEC's in places where they will give timely response to an external call and yet not unduly delay the execution of the main function. Since an @SEC normally acts as a no operation (or a @DLY 0), a convenient location for an @SEC would be just before a long format instruction in a situation where an extra short instruction is needed to align the long format instruction on a fullword boundary.

The only place where an @SEC should be avoided is within the body of an externally called program. In this situation, the CPU may request a second execution of that same program before the first execution is complete. Since storage is available for only one set of return information, acceptance of the second external call would destroy the return information from the first call.

An MSC program designed for external calls may also be called by another MSC program in a fashion similar to that used for subroutines. The calling program would simulate an @SEC by initializing PGM, PGM + 2, and PGM + 4 to whatever values it desires upon return, and then do a @CALL PGM + 6. The @CALL will store the return address at PGM + 6 and start execution at PGM + 8, just as @SEC does. Note, however, that upon return from the @REC the MSC Status Register and Program Exception bit will be set according to what is in fullword PGM, which if not initialized correctly may not match the original status at the time of the call. Figure 4.1 diagrams a segment of MSC code to do this set-up properly. Note that three of these instructions can be eliminated if the contents of ACC and X are of no concern after return from PGM.

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@ST	PGM + 2	Save the Accumulator
@TXA	Zero	
@ST	PGM + 4	Save the Index Register
@LMS		
@ST	PGM	Save the Status Register
@CALL	2, PGM + 6	Start the routine

Figure 4.1. MSC Code to Call an "External Call" Routine

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## APPENDIX A

## IOP MSC INSTRUCTION REPERTOIRE

<u>NAME</u>	<u>MNEMONICS</u>	<u>FORMAT</u>	<u>PAGE</u>
Accumulator/Memory Operations			27
Load Accumulator	@L	Short	28
Add Accumulator	@A	Short	29
And Accumulator	@N	Short	30
Exclusive OR	@X	Short	31
Store Accumulator	@ST	Short	32
Load Fullword	@LF	Long	33
Load Halfword	@LH	Long	34
Store Fullword	@STF	Long	35
Store Halfword	@STH	Long	36
Branch Instructions			37
Branch on Accumulator	@BC	Short	38
Branch on Index	@BXC	Short	39
Branch on Unconditional	@BU	Long	40
Call Subroutine	@CALL	Long	41
Return from External Call	@REC	Short	43
Conditional Skips			45
Tally and Skip Zero	@TSZ	Short	46
Compare	@CI, @C	Long	47
Test Under Mask	@TMI, @TM	Long	48
BCE Register Loads			49
Load BCE Base	@LBB	Long	50
Load BCE PC	@LBP	Long	51

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## IOP MSC Instruction Repertoire (Cont.)

<u>NAME</u>	<u>MNEMONICS</u>	<u>FORMAT</u>	<u>PAGE</u>
Register Operations			52
Load IOP Status Register	@LAR	Short	54
Set Fail Discretes	@SFD	Short	55
Reset Fail Discretes	@RFD	Short	56
Load MSC Status	@LMS	Short	57
Start I/O	@SIO	Short	59
Exchange ACC and X	@XAX	Short	61
Sample for External Calls	@SEC	Short	62
Reset BCE Indicator	@RBI	Short	66
Register Immediates			67
Normalize and Increment X	@NIX	Short	69
Tally ACC to X	@TAX	Short	72
Tally X Immediate	@TXI	Short	73
Load X Immediate	@LXI	Short	74
Tally X to ACC	@TXA	Short	75
Tally ACC Immediate	@TI	Short	76
Subtract ACC from X	@SAI	Short	77
Load ACC Immediate	@LI	Short	78
Repeat Instructions			79
Repeat Until All Indicators	@RAI	Short	83
Repeat Until All Waiting	@RAW	Short	85
Repeat Until Any Indicators	@RNI	Short	87
Repeat Until Any Waiting	@RNW	Short	89
Special Instructions			91
Wait	@WAT	Short	92
Delay	@DLY	Short	93
Interrupt	@INT	Short	94
Self Test	@STP	Short	96

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