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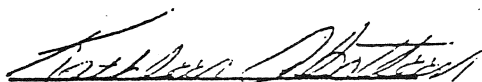
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MISSION OPERATIONS DIRECTORATE

SHUTTLE FLIGHT OPERATIONS MANUAL
Volume 5 - Data Processing Systems

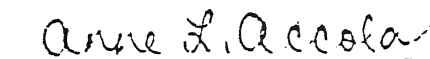
March 21, 1984

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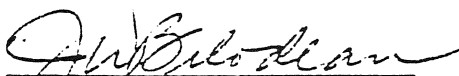
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DOCUMENT ORGANIZATION

The Shuttle Flight Operations Manual (SFOM) will be published in separate individually bound volumes. Publication of updated editions of the volumes will be staggered.

The following list of all SFOM volumes shows the responsible book managers to whom all technical questions should be addressed. Requests for single copies of specific SFOM volumes should be addressed to the book manager in writing or by telephone. Multiple-copy requests for a specific volume must be addressed to the book manager in writing stating the number of copies required and giving a brief statement of justification. Requests for a complete set of SFOM volumes must be addressed to the Division Chief/TD in writing including a statement of justification.

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18	Inertial Upper Stage System	DG6/ H. Hall	-3291
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SECTION 1

INTRODUCTION

1.1 PURPOSE

The successful performance of a complicated spaceflight depends heavily on the use of a computerized system for controlling and monitoring the entire space vehicle. The Data Processing System (DPS), through the use of its various hardware components and its self-contained computer programming (software), provides the vehicle with this monitoring and control support. Some of the functions of the DPS are as follows:

- Supports the guidance, navigation, and control (GNC) requirements of the vehicle, including calculation of trajectories, engine burn data, and vehicle attitude control data.
- Provides for the monitoring and control of vehicle subsystems such as electrical power and environmental control.
- Processes vehicle data and provides this data for transmission to the ground. It also allows for ground control of the vehicle via transmitted commands.
- Provides for checking of data transmission errors and crew control input errors, and supports the annunciation of vehicle systems failures and out-of-tolerance conditions.

The purpose of the Shuttle Flight Operations Manual (SFOM), Vol. 5 - Data Processing Systems, is to provide a compilation of the functional description of the DPS, including hardware, system software, crew station controls and displays pertaining to the DPS, and Cathode Ray Tube (CRT) displays affecting or affected by any of the above. The CRT displays will be explained as required to support functional aspects of the DPS. Explanation of each area of a particular CRT display can be found in the DPS Dictionary. More detail concerning the DPS can also be found in SD 74-SH-0230C, DATA PROCESSING SUBSYSTEM, PRINCIPLES OF OPERATION, as published by Rockwell International, April 1978.

1.2 SCOPE

This SFOM provides DPS hardware and systems software reference information specifically for the flight crew and flight operations personnel. It is comprised of the following sections:

- Section 1.0, Introduction. This section describes the purpose, scope, authority, control, publication, and revisions of this volume.
- Section 2.0, DPS Hardware. This section provides a functional description of the operational aspects and the interfaces for the following Shuttle hardware: General Purpose Computer (GPC), Mass Memory Unit (MMU), Computer Data Bus Network, Backup Flight Controller (BFC),

Multiplexer/Demultiplexer (MDM), Display Electronics Unit (DEU), Display Unit (DU), and Keyboard Unit (KBU). A brief description is also provided for the Computer Interface Conditioning Unit (CICU), Annunciator Display Unit (ADU), Data Bus Coupler (DBC), and Data Bus Isolation Amplifier (DBIA). Although the Engine Interface Unit (EIU), Pulse-Code Modulation Master Unit/Master Timing Unit (PCMMU/MTU), and Caution and Warning (C&W) Electronics Unit (EU) process data, they will be described in SFOM Volumes 8A, 4B, and 4D, respectively.

- Section 3.0, Displays And Controls. The crew station displays and controls pertaining to the DPS are functionally described according to designed usage and results to the system if used non-nominally.
- Section 4.0, System Software. This section provides a functional description of system software terms (e.g., Memory Configuration table, freeze-dried), GPC synchronization and Redundancy Management (RM), Input/Output (I/O) Management, time management, memory modification, downlist, and uplink.
- Section 5.0, BFS System Software. The Backup Flight System (BFS) system software modules are functionally described with emphasis on capabilities provided in various BFS modes of operation (e.g., OPS 0, disengaged-stand alone).

1.3 AUTHORITY

The Training Division within the Mission Operations Directorate (MOD) has the responsibility to provide documentation necessary to support training operations as defined in the Mission Operations Directorate Program Support and Management Plan (JSC 10750).

1.4 CONTROL

The Shuttle Flight Operations Manual (SFOM) is controlled by the Training Control Board as defined in the Space Shuttle Training Management Plan (JSC 0993L).

1.5 PUBLICATIONS AND REVISIONS

This document will be revised as required via Page Change Notices (PCN's) or, if extensive changes are required to a milestone edition, the document will be issued again as a Revision. The Flight Training Branch of the Training Division has the responsibility for preparing, coordinating, and maintaining this document.

Any organization having requests for changes in distribution, comments, questions, suggestions, or proposal changes concerning this document should contact K. M. Abotteen (phone 713-483-5348 or FTS 525-5348).

1.6 ACKNOWLEDGEMENTS

The author extends her own outstanding performance rating to the following persons for their contributions in preparing this volume:

- P. Beauregard
- D. Beckman
- L. Burke
- M. Erminger
- S. Feeney
- S. Hamm
- S. M. Lamb
- R. Lanier
- B. McNealy
- S. O'Roark



SECTION 2

DATA PROCESSING SUBSYSTEM HARDWARE

The Shuttle Data Processing Subsystem (DPS) hardware consists of several Line Replaceable Units (LRU's) (as illustrated in figure 2-1). Although there are several devices onboard the Shuttle Orbiter which process data, categorization of such hardware is made with respect to the type of data processed and to the principal use of the processed data. The DPS hardware elements not included in this SFOM will be included in other SFOM's relating to this categorization and are outlined with dashed lines in figure 2-1.

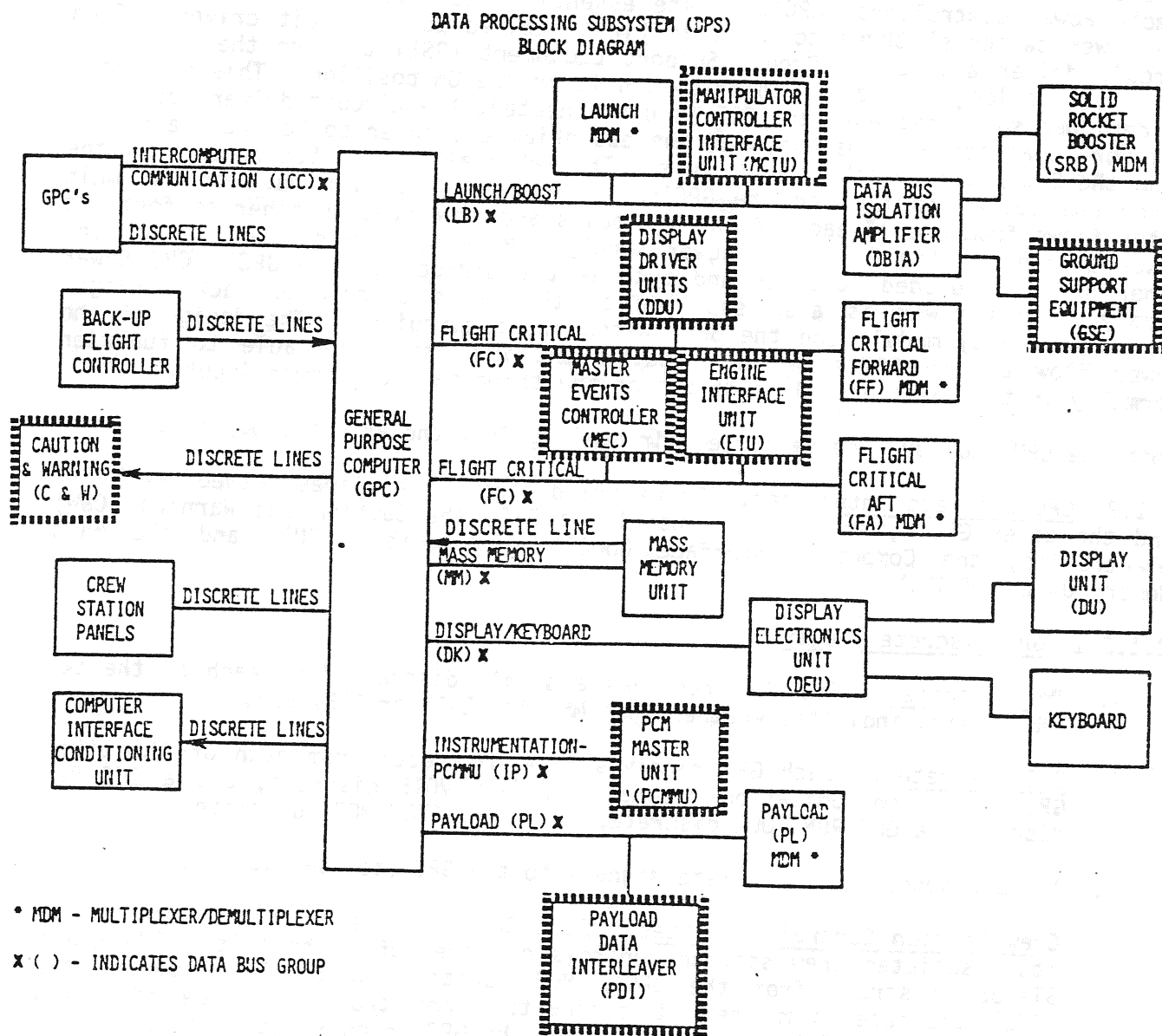


Figure 2-1. DPS block diagram

2.1 GENERAL PURPOSE COMPUTER (GPC)

Each of the five GPC's onboard the Orbiter is composed of two separate units: an IBM AP-101 Central Processing Unit (CPU) and an IBM 4PI Input/Output Processor (IOP). Each of these units contains a memory area for storage of software and data. These two memory areas are collectively referred to as the GPC's Main Memory.

2.1.1 GPC Power and Cooling Interfaces. The GPC power switches are two-position (ON, OFF) toggle switches which, when placed in the ON position, allow essential bus power (from three essential buses) to flow to three pairs of Remote Power Controllers (RPC's). The essential bus power provided by each of the power switches' three contacts is first applied to a circuit driver. Each circuit driver allows the Ground Support Equipment (GSE) to turn the GPC power on or off as long as the GPC power switch is in the ON position. This circuitry is designed such that when the GSE is disconnected, the circuit drivers do nothing more than act as a pathway for the essential bus power to be transferred on from the GPC power switch to the RPC's. The RPC's allow main bus power from the three main buses to flow to the GPC's. Main bus power from each of the main buses flows from one of each of the RPC pairs and is dioded together to form the power source for the GPC's IOP power supply. Main bus power from each of the other RPC's is dioded together and becomes the source for the GPC's CPU power supply. This power is also supplied to the GPC's associated Backup Flight Controller (BFC) module and the BFC switch input circuitry. The design of the power flow to the GPC's is such that a GPC will still be able to function normally in the event of a loss of two of the three main bus power inputs.

Both the CPU and IOP receive forced air cooling from the avionics bay fans.

2.1.2 GPC Discrete Interfaces. There are discrete data lines between each GPC and the other GPC's, crew station panels, a BFC, the Caution and Warning (C&W) electronics, the Computer Interface Conditioning Unit (CICU), and the Mass Memory Units (MMU's).

2.1.2.1 GPC Discrete Inputs

- A. MMU Discrettes. Each GPC receives a single discrete from each of the two MMU's which indicates whether that MMU is READY or OFF/BUSY.
- B. GPC Discrettes. Each GPC receives five discrettes from each of the other GPC's: a synchronization discrete, a FAIL VOTE discrete, and a BFS RUN discrete, a GPC RUN MODE discrete, and a GPC STBY MODE discrete.
- C. The BFC sends seven discrete signals to the GPC (see section 2.6.2).
- D. Crew Station Control Discrettes. Each GPC receives discrete signals from its associated crew station controls on panel 06. There is a RUN and a STANDBY discrete from the GPC's MODE switch, an Initial Program Load (IPL) discrete from the IPL pushbutton, and two IPL source discrettes from the IPL SOURCE switch which tell the GPC which MMU to access for the IPL sequence. The GPC also receives a HALT command from its GPC MODE switch. This discrete is separated from the other MODE switch discrettes because it is relayed to the GPC via its BFC as discussed in section 2.6.2.

Figure 2-2 illustrates the GPC discrete inputs. A summary of all GPC discrete inputs is contained in table 2-1.

2.1.2.2 GPC Discrete Outputs

- A. Crew Station Display Discretes. Each GPC issues a single discrete to its OUTPUT talkback on panel 06. This talkback, which is either barberpole (not energized) or gray (energized), is normally gray when the designated GPC is either processing Primary Avionics Software System (PASS) software and maintaining Input/Output (I/O) operations on the FC data bus network, or when the designated GPC is processing Backup Flight System (BFS) software after BFS is engaged. Each GPC also issues two discrete outputs to its respective GPC MODE talkback on panel 06. These discretes drive this talkback to one of three positions: barberpole (not energized), IPL (when the designated GPC is involved in an IPL sequence), or RUN (when the designated GPC is processing system software).
- B. GPC Discretes. Each GPC outputs five specific discretes to each of the other GPC's. These discretes, which consist of one synchronization discrete, a BFS RUN discrete, GPC FAIL discrete (or FAIL VOTE), a GPC STBY MODE discrete, and a GPC RUN MODE discrete will be discussed in sections 4.2 and 5.2.
- C. GPC STATUS MATRIX Discretes. Each GPC transmits its GPC FAIL discretes via the CICU to the GPC STATUS matrix on panel 01. The GPC STATUS matrix is a five-by-five light matrix (consisting of 20 white lights, and five yellow lights on the main diagonal) which is used to annunciate these GPC discretes. The yellow diagonal lights are illuminated when a GPC determines itself failed via voter hardware and/or synchronization, or GPC Redundancy Management (RM) software. One of the remaining white lights (referred to as non-diagonal lights) is illuminated when a GPC determines another GPC has failed via synchronization or GPC RM software.
- D. GPC SELF-FAIL Discrete. When a GPC issues a SELF-FAIL discrete, this signal is also transmitted to the vehicle's C&W electronics. This signal is used to illuminate the red GPC light on the 40-light C&W light matrix (panel F7), as well as a GPC SELF-FAIL indication on the C&W 120-status light matrix on panel R13. The five lights on this 120-light matrix correspond to the diagonal (yellow) lights on the GPC STATUS matrix (Channels 5, 15, 25, 35, and 45: GPC's 1-5). When a GPC's software has determined that either a self-failure or a failure in another GPC has occurred, a BACKUP C&W ALARM light located in the lower left-hand corner of the 40-light C&W matrix on panel F7 will be illuminated. Depending upon the failure case, either or both the GPC light and BACKUP C/W ALARM light can be illuminated at any one time.

Figure 2-3 illustrates the GPC discrete outputs. The only discrete output which has not been mentioned is the BFS RUN discrete. The BFS GPC is the only GPC to issue this discrete, which is used to tell the other GPC's to release control of the payload (PL) data buses.

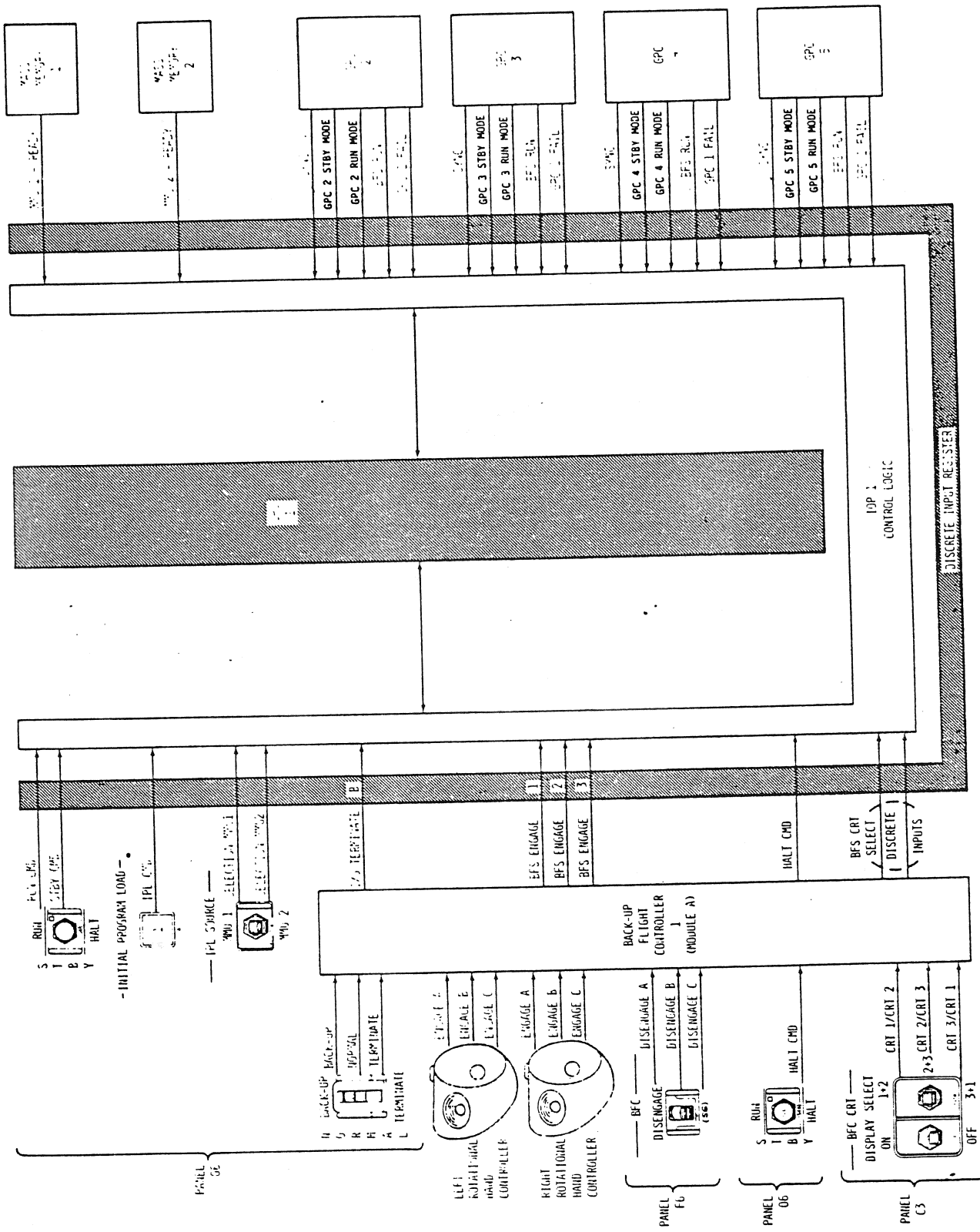


Figure 2-2. GPC Discrete Input Lines (Typical of All 5 GPC's)

TABLE 2-1

GPC DISCRETE INPUT SUMMARY
(TYPICAL OF 5)

DISCRETE INPUT SOURCE	DISCRETE INPUTS	GPC ACTION		
MASS MEMORY 1	Ready	<ul style="list-style-type: none"> MMU 1 is ready to respond to GPC commands; not powered OFF MMU 2 is ready to respond to GPC commands; not powered OFF Directs inputs to voter and main memory Processed by systems software to maintain synchronized GPC operations PASS GPC's inhibit MIA transmitters on PL data buses BFS assumes command of PL data buses 		
MASS MEMORY 2	Ready			
GPC's 2-5	GPC-1 FAIL 1 sync discrete			
	BFS RUN			
Backup Flight Controller	GPC RUN MODE			
	GPC STBY MODE from each GPC			
	BFS ENGAGE 1 BFS ENGAGE 2			
INITIAL PROGRAM LOAD pushbutton (momentary)	2 BFS CRT SELECT discretes		<ul style="list-style-type: none"> If all=1 and I/O TERMINATE B=1 PASS GPC's inhibit MIA transmitters BFS ENGAGE 3 on FC data buses. Halt software and set GPC self-fail discrete output BFS GPC assumes command of FC data buses if 2 of 1, 2, or 3=1 and I/O TERMINATE B=1 PASS GPC's inhibit MIA transmitters on OK data buses selected by BFS CRT SELECT switch BFS GPC assumes command of OK data buses selected by BFS CRT SELECT switch Inhibit MIA transmitters on all FC data buses see MODE switch below Initiates IPL sequence if <ul style="list-style-type: none"> POWER = ON MODE = HALT An MMU is selected and ready Allows nominal GPC operations Transition to "STBY" from "RUN" allows only limited system software execution in PASS and GNC & SM execution in BFS Transition from "RUN" to "STBY" cancels any application software execution in PASS and SM Command (PL buses) in BFS unless engaged Inhibits software execution Resets hardware logic and discrete outputs Permits IPL to occur Directs GPC to select MMU 1 for IPL Directs GPC to select MMU 2 for IPL 	
	MODE switch (3 positions)			I/O TERMINATE B
	IPL SOURCE (3 positions)			HALT IPL CMD
RUN STANDBY				
IPL SOURCE (3 positions)	HALT (from BFS)			
	MMU-1 MMU-2			

O ₂ PRESS	H ₂ PRESS	FUEL CELL REAC (B)	FUEL CELL STACK TEMP	FUEL CELL OVERLOAD
CABIN ATM (H)	O ₂ HEATER (H)	MAIN BUS UNDERVOLT (H)	AC VOLTAGE	AC OVERLOAD
FRON LOOP	AV BAY CABIN AIR	HMU	FWD RCS (H)	RCS AT
H ₂ O LOOP	RGA/ACCEL	AIR DATA (H)	LEFT RCS (H)	RIGHT RCS (H)
PAYLOAD WARNING (H)	LEFT PNC (H)	RHC (H)	LEFT OMS (H)	RIGHT OMS (H)
PAYLOAD WARNING (H)	GPC	ECS (H)	OMS HIT (H)	OMS TVC (H)
BACKUP CH ALARM (H)	PRIMARY CW	SATURATION CHANNEL	MPS (H)	
	SOL TEMP	SOL OVERSPEED	MPU UNDERPEED	HYD PRESS

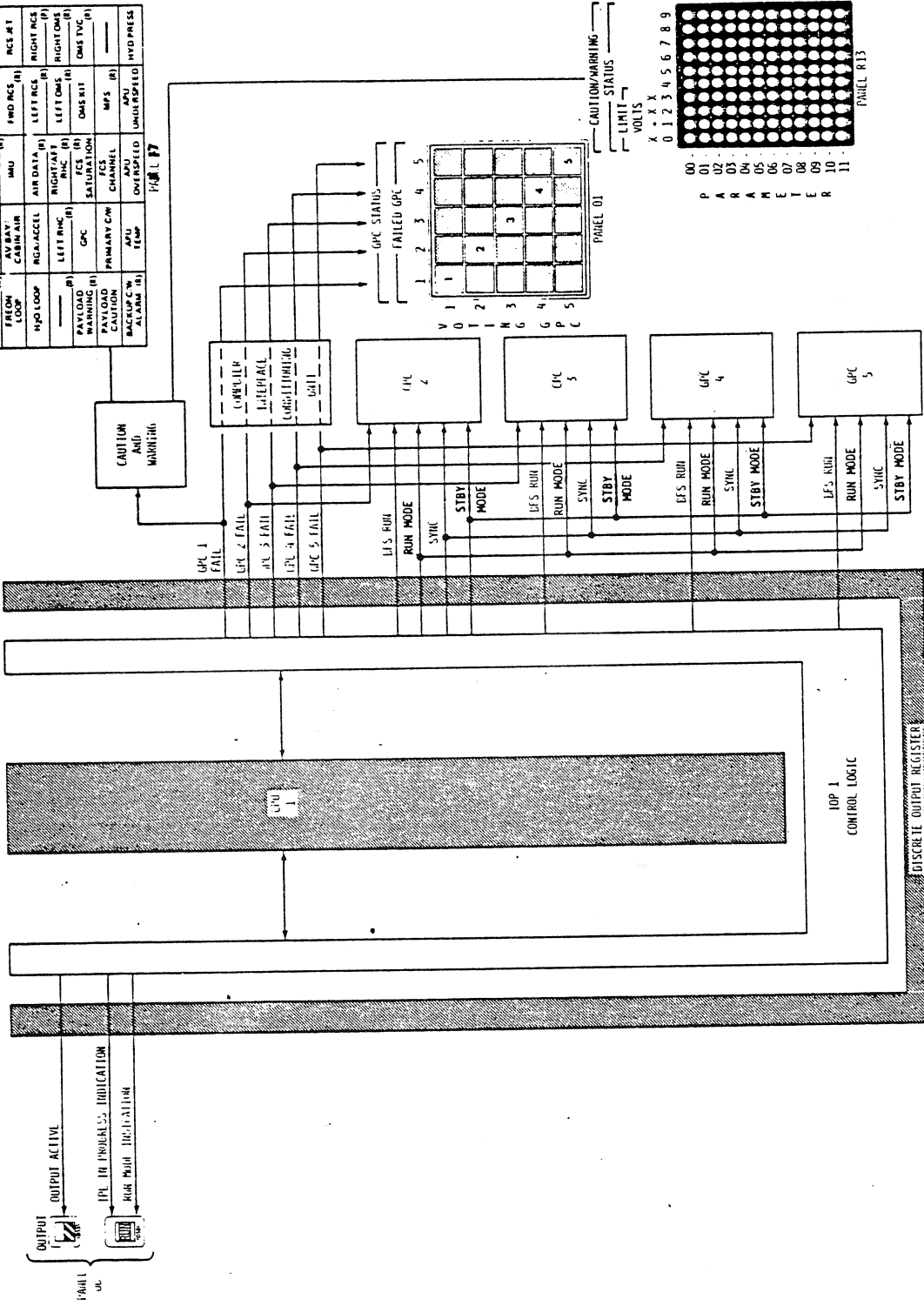


Figure 2-3. GPC 1 Discrete Output Lines (Typical of All 5 GPC's)

There are some specifics about each of the other discrete outputs where the BFS GPC differs from the PASS GPC's. These specifics will be discussed in the software portions of this SFOM (sections 4.0 and 5.0).

A summary of all of the GPC-1's OUTPUT discretes is presented in table 2-2.

2.1.2.3 Computer Interface Conditioning Unit (CICU) and the Annunciator Display Unit (ADU). The CICU receives the GPC FAIL VOTE discretes, conditions them, and passes them on to the ADU. The ADU uses these discretes (or the annunciator lamp test inputs from the lamp test switches on panels 06 and 08) to illuminate the appropriate GPC STATUS light(s). The intensity of these lights can be controlled via intensity control inputs from switches on panel 06 to intensity control circuitry in the ADU. When a GPC is powered off, that GPC will reset its discrete outputs and will inhibit FAIL VOTE discrete inputs from other GPC's to itself (i.e., that GPC's GPC STATUS matrix row and column will not illuminate).

2.1.3 Central Processing Unit (CPU) Functional Description

The CPU has the following purposes:

- Assigns DPS resources to process data and perform systems control tasks.
- Controls access to GPC main memory for data storage and software execution.
- Executes instructions to perform vehicle systems control and data manipulation.

Figure 2-4 illustrates a functional block diagram of a GPC CPU.

2.1.3.1 CPU Control Logic. The CPU control logic schedules, supports, and maintains the status of GPC hardware and software tasks. It also allocates the use of DPS hardware to accomplish scheduled tasks. It executes hardwired (microprogram) and software instructions and maintains two clocks (one for Greenwich Mean Time/Mission Elapsed Time (GMT/MET) and one for simultaneous GPC operations). A 20-MHz oscillator within each CPU supplies timing signals to the CPU components.

2.1.3.2 CPU Main Memory. The CPU's main memory section uses nonvolatile (bit structure is maintained when power is interrupted) iron ferrite cores, arranged in five modularized two-page sections. Each section can store 32,768 18-bit half-words for a total storage capability of 212,992 18-bit half-words. The terminology used in reference to GPC data words is to call each 18-bits a half-word and two consecutive half-words a GPC full-word. Each half-word is composed of 16 data bits, a parity bit which is used to ensure data is read properly, and a storage protect bit which is used to prevent an unintentional alteration of that half-word. Main memory is addressable and accessed by the IOP control logic and the CPU control logic, regardless of location.

2.1.3.3 Main Memory Control Logic. The CPU main memory control logic controls access to main memory by the CPU and IOP control logic and commands the power

TABLE 2-2
 GPC DISCRETE OUTPUT SUMMARY
 (TYPICAL OF ALL 5 GPC'S)

DISCRETE OUTPUT	DISCRETE OUTPUT SOURCE	DESTINATION/EFFECT
I/O active	<ul style="list-style-type: none"> POWER = ON OUTPUT = NORMAL MODE = RUN (PASS) BFS NOT ENGAGED (PASS) BFS ENGAGED (BFS GPC) POWER = ON MODE = RUN (from STBY PASS) BFS in RUN OR STBY (BFS GPC) POWER = ON MODE = HALT IPL sequence active BFS GPC logic when POWER = ON MODE = RUN (not ENGAGED) MODE = HALT (BFS ENGAGED) 	<ul style="list-style-type: none"> OUTPUT talkback driven gray Panel 06 MODE talkback driven RUN Panel 06 MODE talkback driven IPL Panel 06 Identifies to PASS GPC's which GPC is designated BFS GPC PASS GPC's inhibit VJA transmitters on PL data buses
1 synchronization discrete	<ul style="list-style-type: none"> Systems software synchronization logic Systems software* <ul style="list-style-type: none"> - synchronization - GPC RM Systems software* <ul style="list-style-type: none"> - synchronization IOP hardware voter 	<ul style="list-style-type: none"> Systems software synchronization logic in other PASS GPC's Indicated GPC CICU - drives white light in GPC-1 row under indicated GPC CICU-drives yellow light in GPC-1 row GPC-1 column C&W-drives GPC light in F7 matrix and Light 5 in aft C&W status matrix on RI3
GPC-2 FAIL GPC-3 FAIL GPC-4 FAIL GPC-5 FAIL GPC-1 FAIL		

*Systems software also generates the GPC fault messages appearing on the Fault summary page and Fault Message Line and drives "BACKUP C/W ALARM" in F7 C&W matrix.

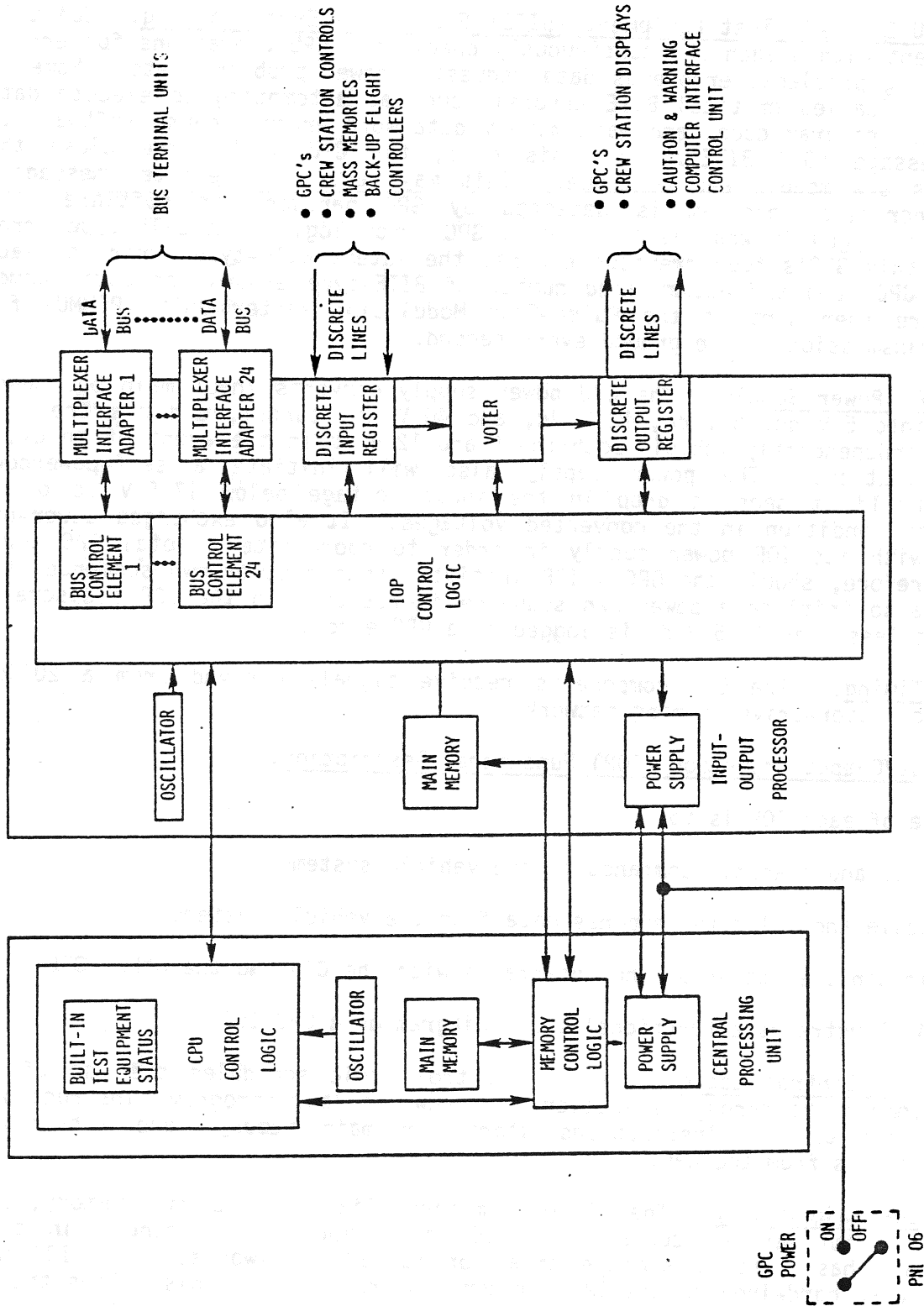


Figure 2-4. GPC Functional Block Diagram

supply to place main memory sections in a minimum-power-usage stage when data is not being accessed.

2.1.3.4 CPU Built-In Test Equipment (BITE) Status and Error Logging. Built-in test equipment within each CPU continuously checks the CPU operations for errors such as timing problems, erroneous data requests, power problems, etc. Some of these errors (called critical BITE errors), such as attempting to execute data as if it were program code, and main memory data word errors, cause software to issue a message "GPC BITE". In this case, the CPU will force close the applications s/w module and continue. This may result in repeated messages. When a noncritical problem is detected by GPC hardware or software, the condition is logged in what is known as a GPC error log. This BITE-type error along with this GPC's four previous errors, the latest BITE-type error for each common set GPC, and the accumulated number of BITE-type errors for each common set GPC, are then sent to the Pulse-Code Modulation Master Unit (PCMMU) for eventual transmission to the ground every second.

2.1.3.5 CPU Power Supply. The CPU power supply converts input main bus power (28 V dc) into 5 V dc, 6 V dc, 12 V dc, and 40 V dc sources, and has the capability to independently inhibit both the 5 and 12 V dc in the event of an over-current situation. The power supply also will initiate a self-powerdown sequence should it sense a drop in the input voltage below 17.5 V dc or an undervoltage condition in the converted voltages. It also exchanges power-off discrettes with its IOP power supply in order to coordinate a total GPC power down. Therefore, should the GPC's IOP initiate its own powerdown sequence, the CPU would also initiate a powerdown sequence in response to the IOP's discrete. Power input less than 17.5 V dc is logged as a GPC error.

2.1.3.6 Timing. The CPU components receive signals derived from a 20 MHz crystal oscillator-driven timing network.

2.1.4 Input/Output Processor (IOP) Functional Description.

The purpose of each IOP is to:

- Format and transmit commands to the vehicle systems
- Receive and validate response data from the vehicle systems
- Maintain the status of the interfaces with the CPU and the other GPC's

Figure 2-4 illustrates a functional block diagram of a GPC IOP.

2.1.4.1 IOP Control Logic. The IOP control logic schedules the use of IOP hardware components through execution of hardwired (microprogram) instructions, schedules the use of instructions stored in main memory, and sets/resets discrete outputs from the GPC.

2.1.4.2 IOP Main Memory. The IOP main memory, like the CPU main memory, uses nonvolatile iron ferrite cores. The IOP main memory is arranged in three sections and has a total storage area for 49,152 half-words. The IOP main memory is also hardwired to the CPU's memory control logic. This allows the CPU and the IOP to address both memory areas as if they were a single unit.

2.1.4.3 IOP Power Supply. The IOP power supply, like that of the CPU, converts 28 V dc main bus input power into 5, 12, 6, and 40 V dc. It also can inhibit its 5 and 12 volt outputs in the event of an overcurrent situation and can initiate a powerdown sequence when its input power drops below 17.5 V dc or when it senses an undervoltage condition in the dc/dc converted voltages. It also sends power-off discrettes to its companion CPU to coordinate a total GPC powerdown. The IOP power supply will initiate a powerdown sequence if it receives a power-off discrete from the CPU.

2.1.4.4 Timing. IOP components receive signals derived from a 16 MHz oscillator-driven timing network. The signals are the basis for timesharing of the software processing components in the IOP control logic.

2.1.4.5 IOP Voter. The IOP contains a hardware voter. The function of this voter is to monitor discrete inputs from the other GPC's. Should it receive a FAIL VOTE from two other GPC's, it will cause the GPC to consider itself failed, and that GPC will cease any attempt to vote against the other GPC's.

2.1.4.6 IOP Discrete Input and Output Registers. The IOP discrete input register accepts and buffers discrete inputs from the other GPC's, crew station controls, the MMU's, and the BFC's. The discrete output register sets or resets discrete outputs (as directed by the control logic and voter) to the other GPC's, crew station displays, the C&W subsystem, and the CICU.

Under certain GPC failure conditions, a GPC's discrete outputs will be reset to zero. If a condition to set the discrete output persists via hardware (e.g. VOTER), the discrete output will be set to 1.

2.1.4.7 IOP/Serial Digital Data Bus Interface. The IOP interfaces with the serial digital data buses via two sets of hardware components: Bus Control Elements (BCE's) and Multiplexer Interface Adapters (MIA's). The BCE's execute instructions to transmit commands to and receive data from other vehicle hardware items called Bus Terminal Units (BTU's). A BTU can be considered to be any piece of hardware which communicates over a data bus through an MIA. The BCE's add the appropriate BTU address and a special bit pattern to words scheduled for transmission prior to shipping the data to its associated MIA. The BCE's also validate data received from and transmitted to their associated MIA's and notify the IOP control logic in the event an error is detected.

MIA's, which are commonly referred to as "ports," have two modes of operation: TRANSMIT and RECEIVE. During the RECEIVE mode, a MIA validates the received data (notifying the IOP control logic when an error is detected), reformats the data, and sends it to the BCE. During a RECEIVE operation, the MIA's transmitter is inhibited unless that particular GPC is in command of that data bus.

During the TRANSMIT mode, a MIA, which always transmits and receives 28-bit words over the computer data buses, adds the appropriate parity and SYNC code bits to the data word, reformats the data, and sends the data out over the data bus. In this mode, both the MIA's receiver and transmitter are enabled.

Any BTU on the other end of the data bus also has its own MIA whose functions are the same as those of the IOP MIA.

2.2 COMPUTER DATA BUS NETWORK

The Orbiter computer data bus network consists of a group of twisted, shielded wire pairs (data buses) which support the transfer of serial digital commands from the GPC's to vehicle hardware and the transfer of vehicle systems data to the GPC's. The computer data bus network is divided into specific groups which perform specific functions. These groups are as follows:

- Inter-Computer Communication (IC or ICC) data buses for GPC to GPC transactions.
- Display/Keyboard (DK) data buses for GPC/Display Electronics Unit (DEU) transactions.
- Mass Memory (MM) data buses for GPC/MMU transactions.
- Instrumentation/PCMMU (IP) data buses for GPC/PCMMU transactions.
- Flight Critical (FC) data buses which tie the GPC's to the FC Multiplexer/Demultiplexers (MDM), Display Driver Units (DDU), Engine Interface Units (EIU), and Master Events Controllers (MEC).
- PL data buses which tie the GPC's to the PL MDM's, the flex MDM's, and the Payload Data Interleaver (PDI).
- Launch/Boost (LB) data buses which tie the GPC's to the GSE, Launch Forward (LF) and Aft (LA) MDM's, Solid Rocket Booster (SRB) MDM's, and the Manipulator Controller Interface Unit (MCIU).

Figure 2-5 illustrates the GPC/data bus network interface.

2.2.1 Inter-Computer Communication (IC or ICC) Data Buses (Ports 1-5). There are five ICC data buses on the Orbiter. Each GPC transmits data over one data bus and receives data over a separate ICC data bus from each of the other GPC's. All GPC's which are processing PASS software (PASS GPC's) and which are members of the common set exchange status information over the ICC data buses. During on-orbit operations, the Systems Management (SM) GPC will receive Guidance, Navigation, and Control (GNC) data from the GNC GPC's. The GPC which is processing BFS software (BFS GPC) will not transmit or receive data over the ICC data buses.

Communications over the ICC data buses is unique in respect to the data traffic which is transmitted over the other types of computer data buses. ICC data bus traffic occurs in one direction only. A GPC transmits over its own ICC bus, and receives data from the other GPC's over each of their dedicated IC buses. The commands and data, which are carried on the other types of computer data buses, are of the command-response type. A GPC requests data over a specific data bus before the data is sent from the appropriate hardware device back to the GPC over the same data bus.

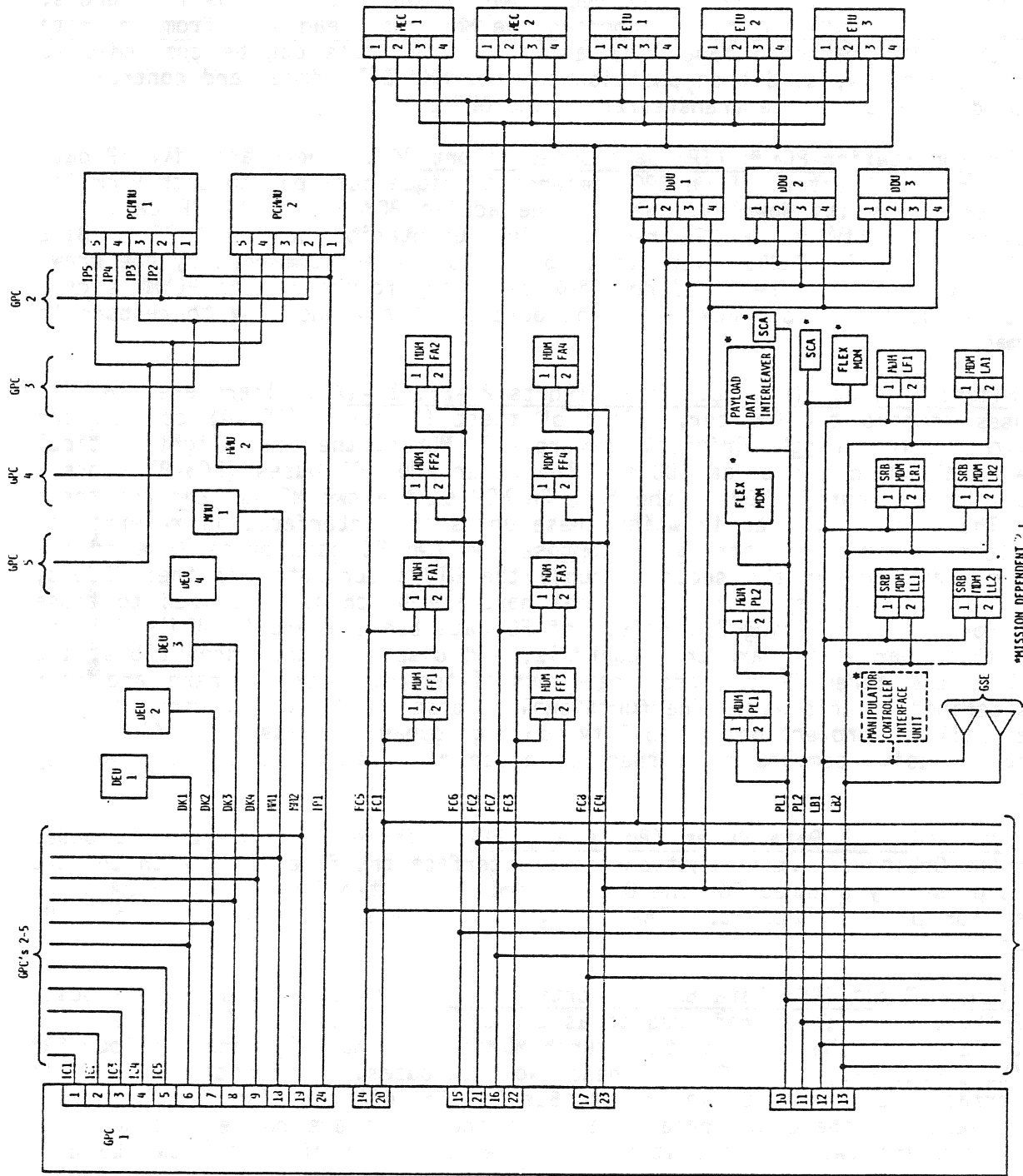


Figure 2-5. Computer Data Bus Network

MISSION DEPENDENT

2.2.2 Display/Keyboard (DK) Data Buses (Ports 6-9). There are four DK data buses onboard the Orbiter. Each DK data bus connects one of the four DEU's to the five GPC's. The GPC's provide serial digital data and commands to the DEU's via these data buses and receive inputs from the Orbiter keyboards on these data buses via the DEU's.

2.2.3 Mass Memory (MM) Data Buses (Ports 18,19). There are two MM data buses onboard the Orbiter. Each MM bus connects one of the MMU's to the five GPC's. The GPC's, via these MM buses, can command the MMU's to read data from or write data to the MMU's magnetic tape. In addition, the MMU's can be commanded to position their tapes, send tape position data or MMU BITE data, and control the amount of data which can be transferred to the GPC's.

2.2.4 Instrumentation/PCMMU (IP) Data Buses (Port 24). There are five IP data buses onboard the Orbiter. Each GPC commands a unique data bus to both PCMMU's. Each GPC transmits its downlist data to the active PCMMU via its IP data bus. As required by software, a GPC receives instrumentation data and PCMMU BITE status from the active PCMMU over its IP data bus. When commanded by the crew, a GPC will transmit the required downlink telemetry format to the PCMMU's over the IP data bus. Only one PCMMU will be powered at any one time to respond to GPC commands.

2.2.5 Flight Critical (FC) Data Buses (Ports 20-23, 14-17). There are eight FC data buses onboard the Orbiter. Four of these FC buses (FC1-4) connect the GPC's with the four Flight Critical Forward (FF) MDM's, the four Flight Critical Aft (FA) MDM's, and the three DDU's. The other four FC buses (FC5-8) connect the GPC's to the four FF MDM's, the four FA MDM's, the two MEC's, and the three EIU's. The specific manner in which these units are interfaced is referred to by the term "string." A string is composed of two FC data buses (one of the first group and one of the second group), the BTU's connected to them (DDU's, MDM's, MEC's, and EIU's), and all of the hardware which is hardwired to those BTU's. For example, String 1 consists of FC data buses 1 and 5, MDM's FF1 and FA1 and their hardwired hardware, controls, and displays, the three EIU's, the two MEC's, the three DDU's, and their associated displays. There are four strings defined in this way. The functional purpose of the string concept is to provide failure protection capability during dynamic phases of flight by allowing exclusive command of a specific group of Shuttle vehicle hardware by one GPC.

2.2.6 Payload (PL) Data Buses (Ports 10, 11). There are two PL data buses onboard the Orbiter. Their function is to interface the five GPC's with the two PL MDM's presently planned for the Orbiter and one or two flex MDM's (FMDM's) as required for payload support. The PDI will interface with the GPC's over PL Data Bus 1.

2.2.7 Launch/Boost (LB) Data Buses (Ports 12,13). There are two LB data buses onboard the Orbiter (also referred to as Launch Data Buses or LDB's). Each GPC can interface with the GSE, the two launch MDM's (LF1 and LA1), and the four SRB MDM's (LL1, LL2, LR1, and LR2) via these two data buses. In addition, the GPC's can interface with the MCIU via LB Data Bus 1. The GSE can also interface with this hardware via these two data buses when the GPC's are not executing software. There are two hardware items which serve to interface the two LB data buses with the GSE and the SRB MDM's. These are called Data Bus Isolation Amplifiers (DBIA's).

2.2.8 Data Bus Isolation Amplifier (DBIA). There are two DBIA's onboard the Orbiter. The purpose of these units is to isolate data bus stubs which are left open by the GSE (T-0) disconnect and the SRB disconnect. This isolation protects the LB data buses from unwanted interference and noise. Each DBIA consists of two independently powered and controlled channels - a GSE channel and SRB channel. Upon receipt of a signal at one receiver, the control logic inhibits the other receiver (to avoid a wrap-around effect), validates the input data, improves the signal strength of the received data, and then transmits the data to the appropriate destination. Since the GSE channel receives its power through the preflight test buses (via the T-0 umbilical), it becomes inoperative when the T-0 disconnect occurs at launch. The SRB channels receive main bus power via the MEC switching circuitry and power switches located on panel 017. Each MEC power switch permits control bus power to activate a RPC which then allows main bus power to flow to the SRB channels in both DBIA's. Therefore both SRB channels receive main bus power via either one of the two MEC switches. Power flow to the DBIA's is illustrated in figure 2-6.

2.2.9 Data Bus Coupler (DBC). A DBC is a small device which provides DC isolation and transformer coupling between a data bus and an MIA.

2.3 MASS MEMORY UNIT (MMU)

Onboard the Orbiter, there are two BTU's which are known as Mass Memory Units (MMU's). Each of these MMU's is a coaxially-mounted reel-to-reel digital magnetic tape storage device which provides storage for computer software and Orbiter systems data and can be accessed by the flight crew as required.

2.3.1 MMU Interfaces.

2.3.1.1 MMU Power/Cooling Interfaces. Each MMU receives electrical power via separate MMU power switches on panels 014 (MMU 1) and 015 (MMU 2). Each MMU power switch is a two-position toggle switch which permits control bus power to activate an RPC. The RPC allows main bus power to flow to the designated MMU power supply. The status of the power switch is made available for downlink through the Operational Instrumentation Forward (OF) MDM's.

Each MMU is cooled via the water loop coldplates in the forward avionics bays.

2.3.1.2 MMU/GPC Interface. Each MMU interfaces with all five GPC's via one of the MM data buses. In addition, each MMU has a separate discrete interface line to each of the GPC's to inform the GPC's of the state of the MMU (busy or ready to accept command inputs).

The GPC's, via the MM data buses, can command the MMU's to read data from or write data to the MMU's magnetic tape. In addition, the MMU's can be commanded to position their tapes, to send the GPC's BITE data or tape position data, and to extend, by a factor of eight, the limit on the amount of data which can be transferred. (The normal amount is 2,048 16-bit words in SM OPS 2).

2.3.2 MMU Functional Description. The following is an analysis of the components of an MMU and the functions of these components. Figure 2-7 illustrates a functional block diagram of an MMU.

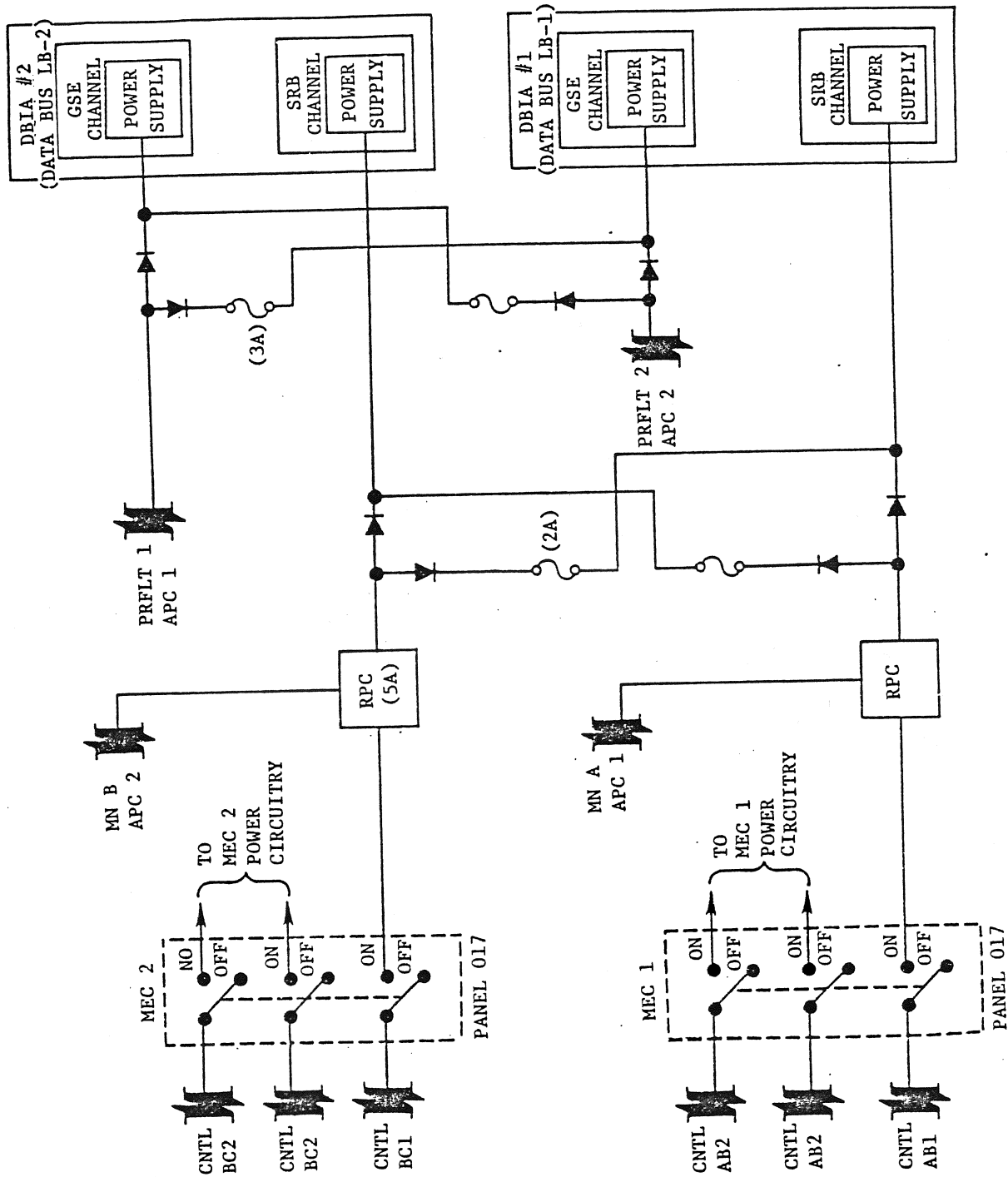


Figure 2-6. DBIA Power

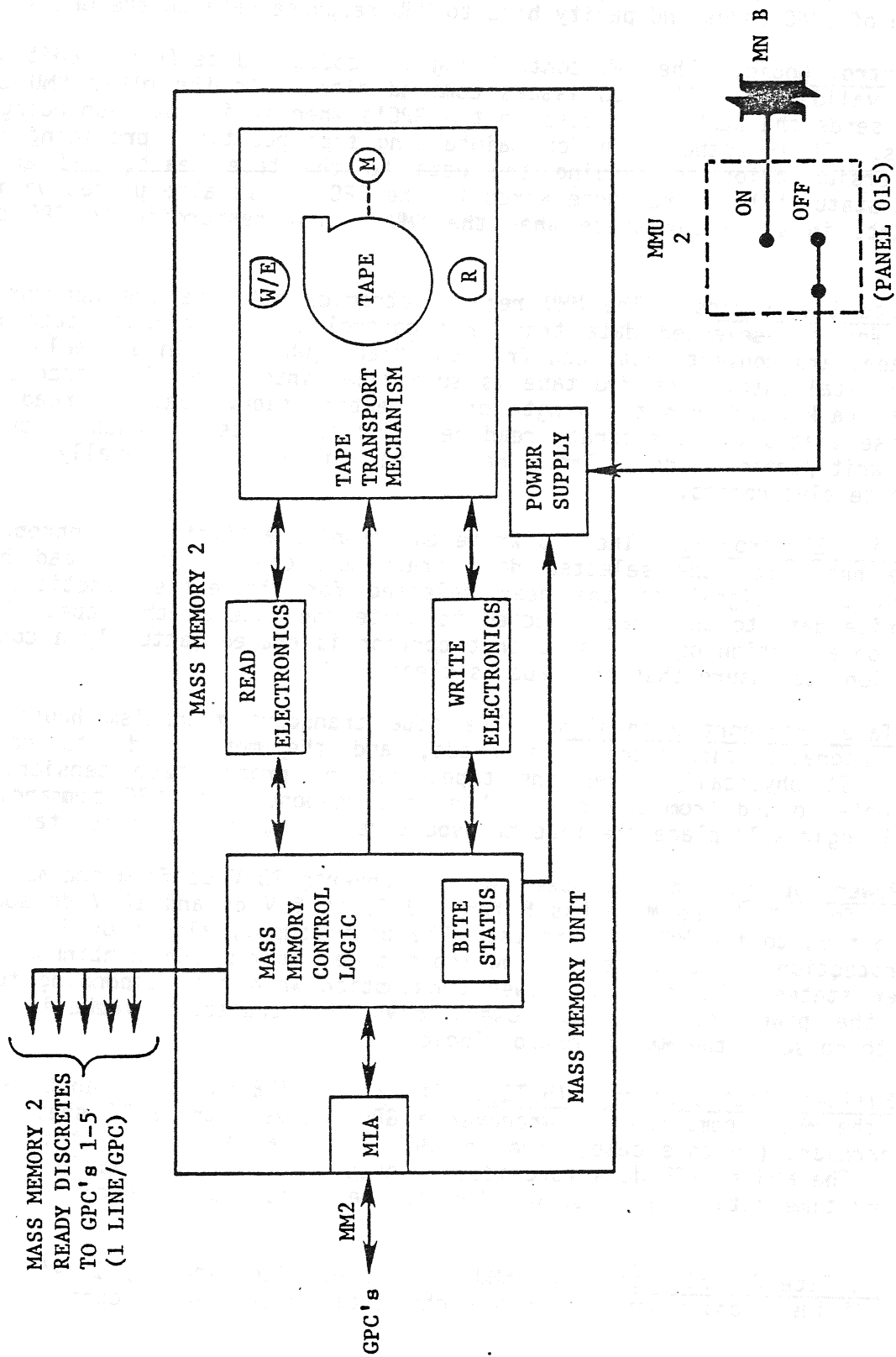


Figure 2-7. MMU Functional Block Diagram

2.3.2.1 Multiplexer Interface Adapter (MIA). Each MMU interfaces with its MM data bus via an MIA. The functions of the MMU MIA are the same as those listed for the IOP MIA; that is, GPC command validation, data format conversion, and the addition of SYNC codes and parity bits to MMU response data to the GPC's.

2.3.2.2 Control Logic. The MMU control logic decodes and performs additional GPC command validation. It also issues command signals to the other MMU components and sends the READY discretes to the GPC's when it is not responding to GPC commands. It is responsible for maintaining tape position, providing data format conversion prior to issuing the data to the tape heads, and adding address and status bits to response words to the GPC's. It also places various MMU components in a standby state when the MMU is not responding to GPC commands.

2.3.2.3 Read Electronics. The MMU read electronics activate the appropriate read heads for the selected data track and control track, validate data read from the tape, and convert data read from the track (which is in an analog format) into digital data. The MMU tape is subdivided into eight data tracks and one control track which run the length of the entire tape. Data is read from each of these tracks via a separate read head and is written to each track via individual write/erase heads. These heads are activated individually by the Read and Write electronics.

2.3.2.4 Write Electronics. The MMU write electronics activate the appropriate write/erase heads for the selected data track and control track read head, transmit an erase signal to the head selected for the erase function, and transmit write data to the head selected to write the data on the tape. Prior to writing on a portion of the tape, that portion is erased (actually a continuous operation) to insure that the tape is clean.

2.3.2.5 Tape Transport Mechanism. The tape transport mechanism houses the nine-track magnetic tape, the tape heads, and the motor and its control mechanism. It physically moves the tape, retains proper tape tension, and transfers data to and from the tape. When not responding to GPC command, the MMU control logic will place the tape transport mechanism in a standby state.

2.3.2.6 Power Supply. The MMU power supply converts 28 V dc from one main bus (Main Bus A for MMU 1 and Main Bus B for MMU 2) to 5 V dc and 12 V dc sources for distribution to the MMU components. The power supply also provides under-voltage protection for both severe low-input power spikes and continuous low-input power states. To minimize power consumption when not responding to GPC commands, the power supply also powers down the transport mechanism when commanded to do so by the MMU's control logic.

2.3.2.7 Built-in Test Equipment (BITE). The MMU's BITE maintains an OK/NOT OK status of the MMU's components. Whenever a GPC requests the BITE status of a piece of hardware (in this case, from an MMU), it is a request for this OK/NOT OK status. The MMU's BITE data (provided in appendix B) is updated in GPC main memory every time data is read or written to the MMU's and is downlisted every second.

2.3.2.8 MMU Tape Description. The MMU tape is 602 feet long by 1/2-inch wide and is subdivided longitudinally into eight data tracks and a control track.

These tracks are then further divided into files, subfiles, and blocks of data which serve as an aid to finding specific tape locations during read and write operations. Each tape can store over 8,000,000 16-bit words, which at the present time, is more than sufficient for storing three copies of all software for a flight in each MMU.

2.3.2.9 MMU Tape Data Layout. Software stored on MMU is organized according to operational groups called phases. A phase of software is designed to be a group of software code and data which is transferred to the GPC's during normal Orbiter operations (e.g., GNC OPS 1 to OPS 2 transition). Each phase is divided into load blocks of data and load blocks of code to be stored in unprotected and protected main memory, respectively. A load block can contain up to 32 MMU blocks of data (one subfile) within the same file of the same track. Data transfers between MMU's and GPC's occur in load blocks.

2.3.2.10 Checksum. Checksum refers to a method by which data transfers from the MMU's to the GPC's are validated. When each load block is stored on MMU, the sum of 1's in all the 16-bit words of the load block are added and the sum is stored as the last word of the load block, the checksum word. When a GPC reads the load block, it sums the number of 1's in all the 16-bit words as received and compares its checksum to the stored checksum. If a miscompare occurs, the software is not executed, and an I/O ERROR MMU fault message is generated.

2.4 MULTIPLEXER/DEMULTIPLEXERS (MDM's)

There is a total of 32 MDM's onboard the Orbiter. Of these MDM's, 18 are classified as DPS MDM's and the other 14 are classified as instrumentation MDM's.

The 18 DPS MDM's have names which are derived from their locations and their hardware interfaces. They are the:

- Flight Critical Forward (FF) MDM's - (4)
- Flight Critical Aft (FA) MDM's - (4)
- Payload (PL) MDM's - (2)
- Launch-SRB LEFT (LL) MDM's - (2)
- Launch-SRB Right (LR) MDM's - (2)
- Launch-Forward (LF) MDM - (1)
- Launch-Aft (LA) MDM - (1)
- Flexible MDM's (FMDM's) - (1) or (2) depending on payload needs

The 14 instrumentation MDM's have names which are derived from the instrumentation systems and their locations. They are the:

- Operational Instrumentation Forward (OF) - (4)
- Operational Instrumentation Aft (OA) - (3)
- Developmental Instrumentation Center (DC) - (2)
- Developmental Instrumentation Forward (DF) - (1)
- Developmental Instrumentation Left (DL) - (2)
- Developmental Instrumentation Right (DR) - (2)

The DPS MDM's serve the following purposes: they convert and format serial digital GPC commands into parallel discrete, digital, and analog commands for

transfer to vehicle subsystem hardware. This operation is commonly referred to as an MDM's demultiplexing function. The other function of the MDM, which is known as the multiplexing operation, is to convert and format parallel discrete, digital, and analog data from vehicle systems into serial digital data for transmission to the GPC's.

2.4.1 MDM Interfaces

The MDM interfaces are as follows:

- A. Cooling. Water-loop coldplate cooling to those MDM's in the forward avionics bays (the FF, PL, and LF1 MDM's); Freon-loop coldplate cooling to the MDM's in the aft avionics bays (the FA and LA1 MDM's) and the payload bay pallet (FMDM) and passive coldplate cooling to the SRB MDM's (LL1, LL2, LR1, and LR2).
- B. The MDM's interface with the GPC's via serial digital data buses and with Orbiter systems hardware via hardwired lines. While most DPS MDM's have two MIA's for redundant data paths to the GPC's, FMDM's have only one MIA each for one data path to the GPC's. For a complete description of MDM/LRU interfaces see the MDM Tables in appendix A.
- C. Power. Main bus power (28 V dc) to the FF, FA, and PL MDM's, preflight test bus power to the LF and LA MDM's primary payload bus power to the FMDM's and SRB bus power to the SRB MDM's (LL1, LL2, LR1, LR2). There are 11 FC and PL MDM power switches on panel O6. The function of these two-position, dual-contact toggle switches (with the exception of the PL3 switch which is unwired) is to permit control bus power to activate two RPC's which in turn allow power from two main buses to flow to the designated MDM's. The MDM power switch status is made available for downlink via the OF and OA MDM's (FF1-4, FA1-4, PL1-3). The LF and the LA MDM's receive their power through the preflight test buses, (there is no crew station control for these MDM's). The four SRB MDM's receive power through SRB Buses A and B. These buses are tied to the Orbiter main buses and controlled by the MEC. The FMDM's are controlled like other pallet hardware through the standard switch panel by a circuit breaker and a two-position toggle switch. With the circuit breaker closed and the SYS toggle switch on, a power control box allows primary payload bus power to flow to the FMDM's and other pallet systems.

2.4.2 MDM Functional Description. The typical DPS MDM is redundant in several ways. Each MDM can communicate on one of two different data buses via two separate MIA's. Each MDM has two separate power supplies, each fed by a different main bus power source. Furthermore, each power supply can provide power to all components within the MDM; therefore a power supply failure will not inhibit the operation of either MDM channel. Each MDM has two analog-to-digital converters. Inputs from each of the I/O modules (there can be up to 16 I/O modules in each MDM) are available to both MDM channels. Since each MDM has two MIA's or ports and the other redundant components, the loss of an MIA would not mean the permanent loss of data to the GPC's since the data can be accessed through the other port on the other data bus upon action of the crew. Switch-over is not automatic. The I/O modules which reside in an MDM are based on the

hardware components and types of data that the particular MDM is required to access. This allows inflight switching of like MDM's that can be reached. For instance, one FF MDM can be exchanged for another FF MDM, but an FF MDM and an FA MDM would not be interchangeable.

Figure 2-8 illustrates a functional block diagram of an MDM.

2.4.2.1 MDM MIA. Each of the two MIA's within an MDM are functionally identical with the GPC's IOP MIA.

2.4.2.2 Sequence Control Unit (SCU). Either of the MDM SCU's validates GPC commands (for proper address, operation, and time between words) and decodes those commands into instructions to control MDM operations. They also execute instructions which are stored in a programmable read-only memory (PROM) if required and maintain the BITE status of the MDM components. MDM BITE is updated in GPC main memory only when requested by crew or uplink command and is not nominally downlisted. Self-check tasks are cyclically performed to terminate MDM operations if invalid. If requested by GPC Command, an SCU will perform a BITE subtest of itself, A/D converter power supply, or any I/O modules. These tests are independent of each other, but currently the only subtest used is the discrete output I/O module subtest to ensure no discrete outputs are locked up and to provide a status of the discrete outputs to software.

2.4.2.3 Analog-to-digital (A/D) Converter. The function of the A/D converter is to convert analog data inputs from the input modules into serial digital data for transfer to the SCU. The reverse process (digital-to-analog conversion) is not performed by this device but is accomplished instead in the appropriate MDM output module.

2.4.2.4 MDM Power Supply. Each of the MDM power supplies convert 28 V dc main bus input power into regulated 18.6 V dc power, and then converts the 18.6 V dc into 5, 10, 12, and 20 V dc. These power supplies also provide undervoltage detection, and their power inputs are dioded together to supply all the MDM components. Failure of one power supply will not effect MDM operations. Failure of both power supplies will cause the MDM to reset all discrete outputs, to reset all analog outputs and, when power is reapplied, to invalidate the first MDM response to GPC commands. Cycling MDM power will restore normal MDM functions.

2.4.2.5 MDM Input/Output (I/O) Modules. There are six basic types of I/O modules which may be installed in an MDM. These I/O modules are often referred to as I/O cards. They are as follows:

- Discrete input module converts up to 48 parallel +5 V dc inputs or up to 48 +28 V dc inputs into three serial, 16-bit data words.
- Discrete output module converts serial, digital commands into parallel discrete signals to Orbiter systems hardware.
- Analog input module conditions +5.11 V dc to -5.12 V dc analog inputs from Orbiter systems hardware for digital conversion by the A/D converter.

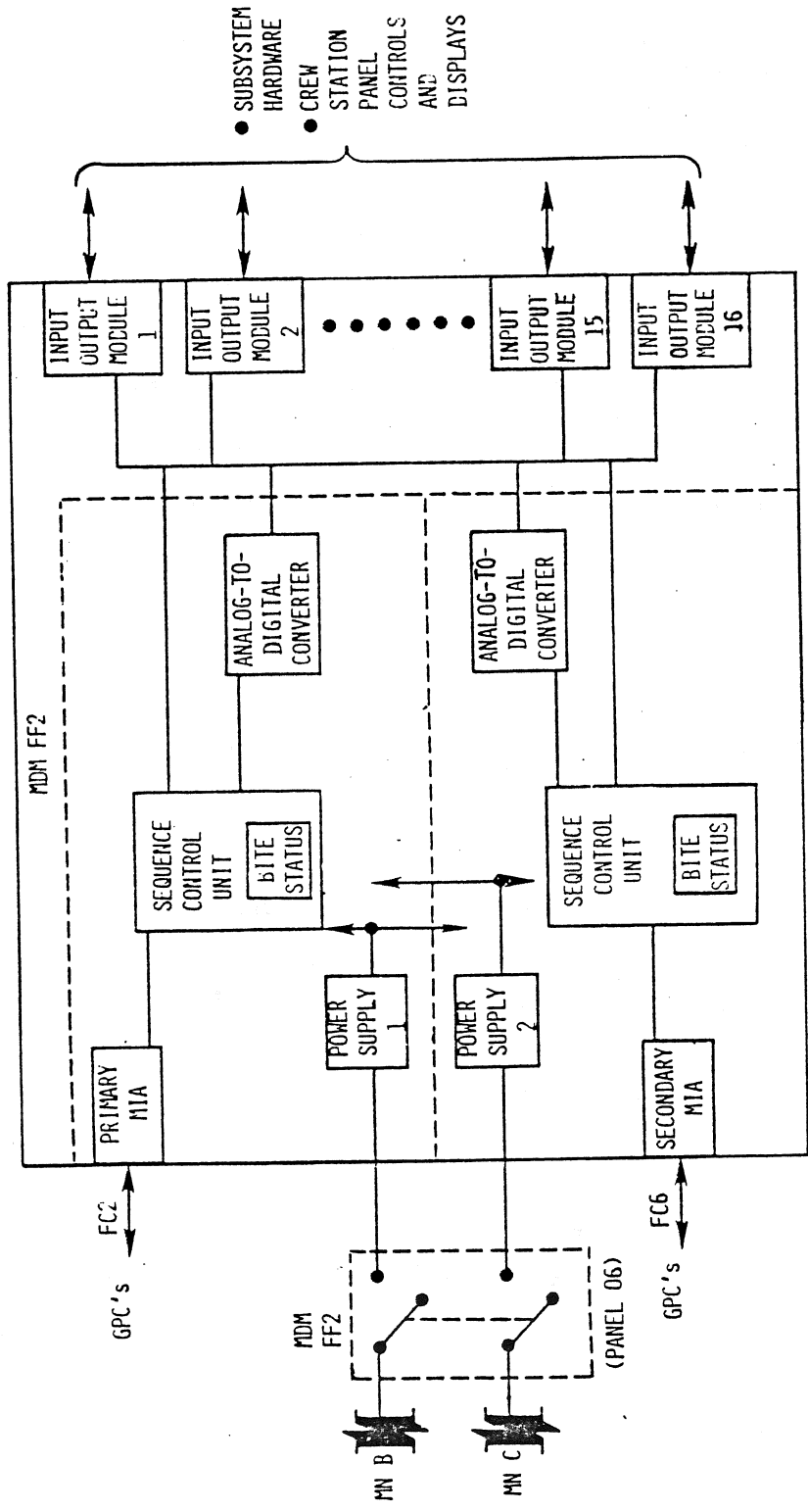


Figure 2-8. MDM Functional Block Diagram

- Analog output module converts 10-bit digital commands into +5.11 V dc to -5.12 V dc analog outputs to Orbiter systems hardware.
- Serial, digital input/output module:
 - Notifies Orbiter systems hardware to receive commands or to send data.
 - Converts NRZ commands into Manchester II commands for transmission to Orbiter systems hardware (waveform conversion).
 - Adds SYNC code and parity bits to commands for systems hardware.
 - Converts Manchester II data into NRZ data from systems hardware (waveform conversion).
- TACAN/radar altimeter module (applicable to FF MDM's only):
 - Continuously transfers control panel inputs or GPC commands to TACAN.
 - Continuously requests, receives, and buffers radar altimeter data.
 - Continuously receives and buffers TACAN and TACAN control panel data.
 - Converts buffered data to NRZ for transmission to GPC when requested.

2.4.2.6 Flexible MDM (FMDM). FMDM's are used to interface between the GPC's and payload bay pallet systems and experiments. Their function is the same as other DPS MDM's except each FMDM has only one MIA, one SCU, one A/D converter, one power supply, and eight I/O modules. The I/O modules are interchangeable, making FMDM's more flexible in their use than other DPS MDM's.

2.5 MULTIFUNCTION CRT DISPLAY SYSTEM (MCDS)

The MCDS onboard the Orbiter is the system which allows for onboard monitoring of Orbiter systems and computer software processing, and provides the flight crew with manual control for data and software manipulation. The MCDS consists of three types of hardware - the DEU's, the Display Units (DU's), and the Keyboard Units (KBU's), which communicate with the GPC's over the KBU's data bus network. Figure 2-9 illustrates the KBU's and the DU's and their locations in the Orbiter crew stations. Additional KBU's, DEU's, and DU's may be added to the vehicle as the Shuttle program develops.

2.5.1 MCDS Interfaces

2.5.1.1 Power/Cooling. The CRT POWER switch has two contacts for three positions: OFF, STBY, and ON. The STBY position activates two RPC's to allow main bus power from one bus to the DEU and DU power supplies. Only the DU high-voltage power supply is activated to use for CRT filament heaters. In the ON position, the DEU power supply receives a POWER UP signal discrete input to activate its logic circuitry and sends a POWER UP signal to the DU voltage power supply to activate its logic circuitry. A 3-amp circuit breaker allows the 115 V ac input to the respective instrumentation lamp potentiometer to control lamp intensity via dimmer circuitry. The dimmer circuitry output is transformed to 5 V ac and protected by a 5-amp fuse for keyboard lamp power.

The DEU and DU pairs receive forced-air cooling via the cabin fans. The KBU's are cooled by passive heat dissipation.

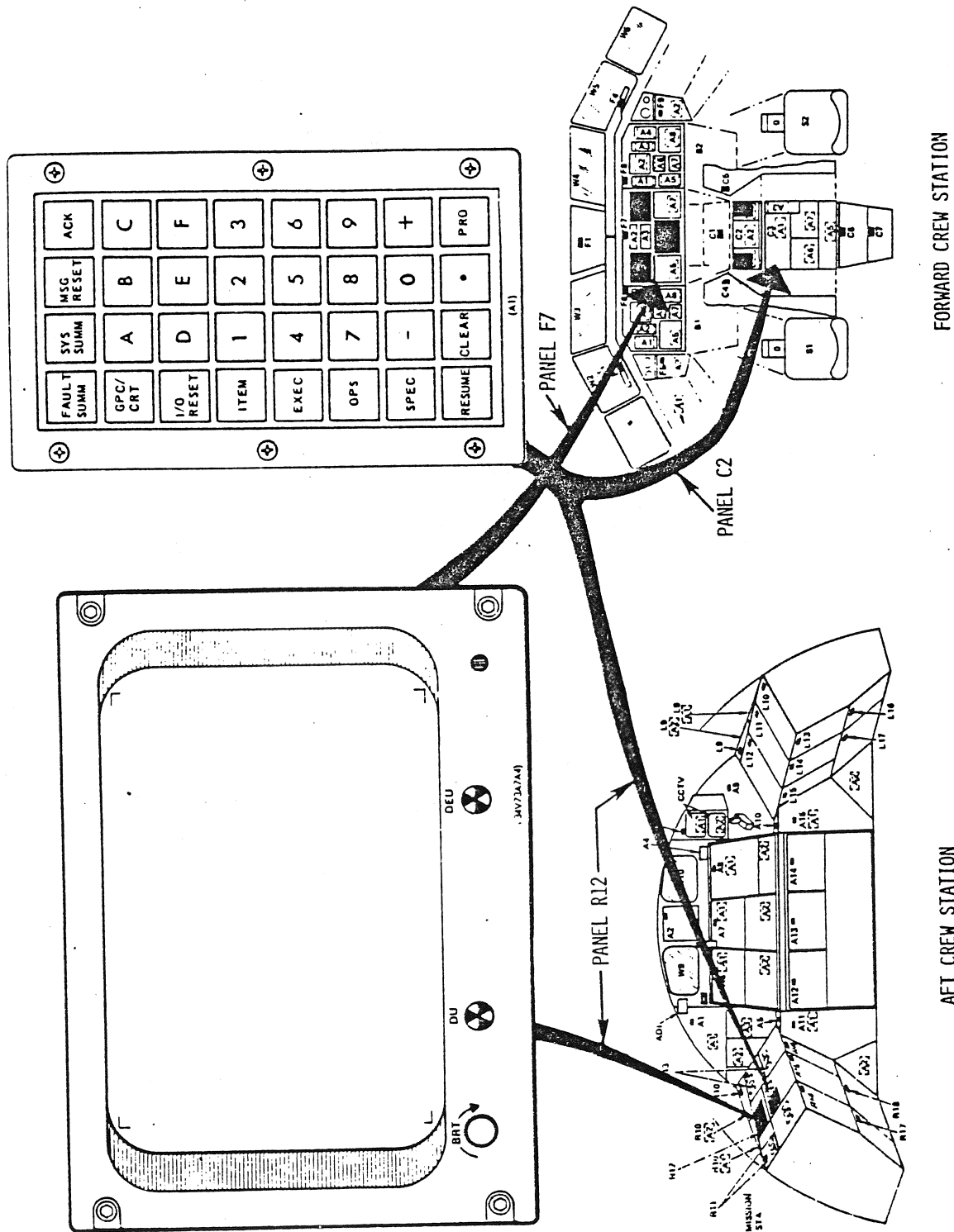


Figure 2-9. DPS Keyboard and CRT Locations

2.5.1.2 Crew Station Controls. The following is a brief explanation of each of the MCDS controls.

- A. DEU LOAD Switches. Prior to beginning normal operations, each DEU must receive a memory load from an MMU through a GPC. This procedure is accomplished through the use of the DEU LOAD switches on panel 06. Each of these four switches (one for each DEU) is a two-position momentary toggle switch which sets a flag which will initiate a GPC request for data stored in the MMU. These data will be shipped from the MMU to the GPC and then loaded from the GPC into the DEU's own memory. This DEU data load request will only be recognized immediately after GPC initialization or in PL OPS 901. During this initialization sequence, the words DEU LOAD will appear on the appropriate Cathode Ray Tube (CRT). If the load is successful, the words IPL COMPLETE will appear on the CRT, followed shortly thereafter by the appropriate CRT display. IPL INCOMPLETE will appear on the CRT if the attempted load is unsuccessful.
- B. Major Function (MAJ FUNC) Switches. On the basis of the phase of the Shuttle mission there may be different functional groups of software being processed at the same time. These three-position toggle switches (one for each KBU) tell the GPC's which of these software groups is meant to process the KBU inputs and drive the data presented on the CRT: GNC, SM, or PL.
- C. CRT SELECT Switches. There are three CRT's (three DU's hardwired to three DEU's) in the forward station and only two KBU's. The forward station KBU's are each connected to two of these DEU/DU pairs. The function of the CRT SELECT switches is to identify to the system which DEU/DU pair is to process keystrokes from each of the keyboards. The LEFT CRT SELECT switch allows the left keyboard to talk to either DEU/DU-1 (the left CRT) or DEU/DU-3 (the center CRT), and the RIGHT CRT SELECT switch allows the right keyboard to talk to either DEU/DU-2 (the right CRT) or DEU/DU-3.
- D. CRT POWER Switches. Each DEU/DU pair has a DEU/DU POWER switch associated with it. Each of these is a three-position dual-contact toggle switch which permits control bus power to activate a pair of RPC's, and allows main bus power to flow to the designated DEU and DU. The ON and STBY CRT POWER switch status is available through the OF MDM's (OF4).
- E. Keyboard Lamp Power Switches. Each set of keyboard lamps is part of an instrumentation lighting system which responds to crew station circuit breakers and potentiometers. Three 3-amp circuit breakers protect the ac phase power bus inputs to the left/center, right, and Mission Specialist (MS) instrumentation lamps (including keyboard lamps). The potentiometers permit variable control of instrumentation lamp intensity.

2.5.1.3 GPC interface. Figure 2-10 illustrates the GPC/MCDS interfaces via the DK data buses. Note the inclusion of a proposed fifth DEU/DU pair and a fourth KBU (for the PL specialists station in the aft crew station). When and if a fifth DEU/DU pair is added to the vehicle, it will interface with the GPC's over DK-2, and provisions will be made to ensure that only DEU/DU-2 or DEU/DU-5 will be active at any one time. If two GPC's send commands to the DEU to drive different displays and data, frequently the viewer will see a flashing effect on the CRT. This is referred to as CRT dual commands.

DISPLAY ELECTRONICS UNIT (DEU) - KEYBOARD
 (DK) DATA BUS/GPC PORT
 ASSIGNMENTS

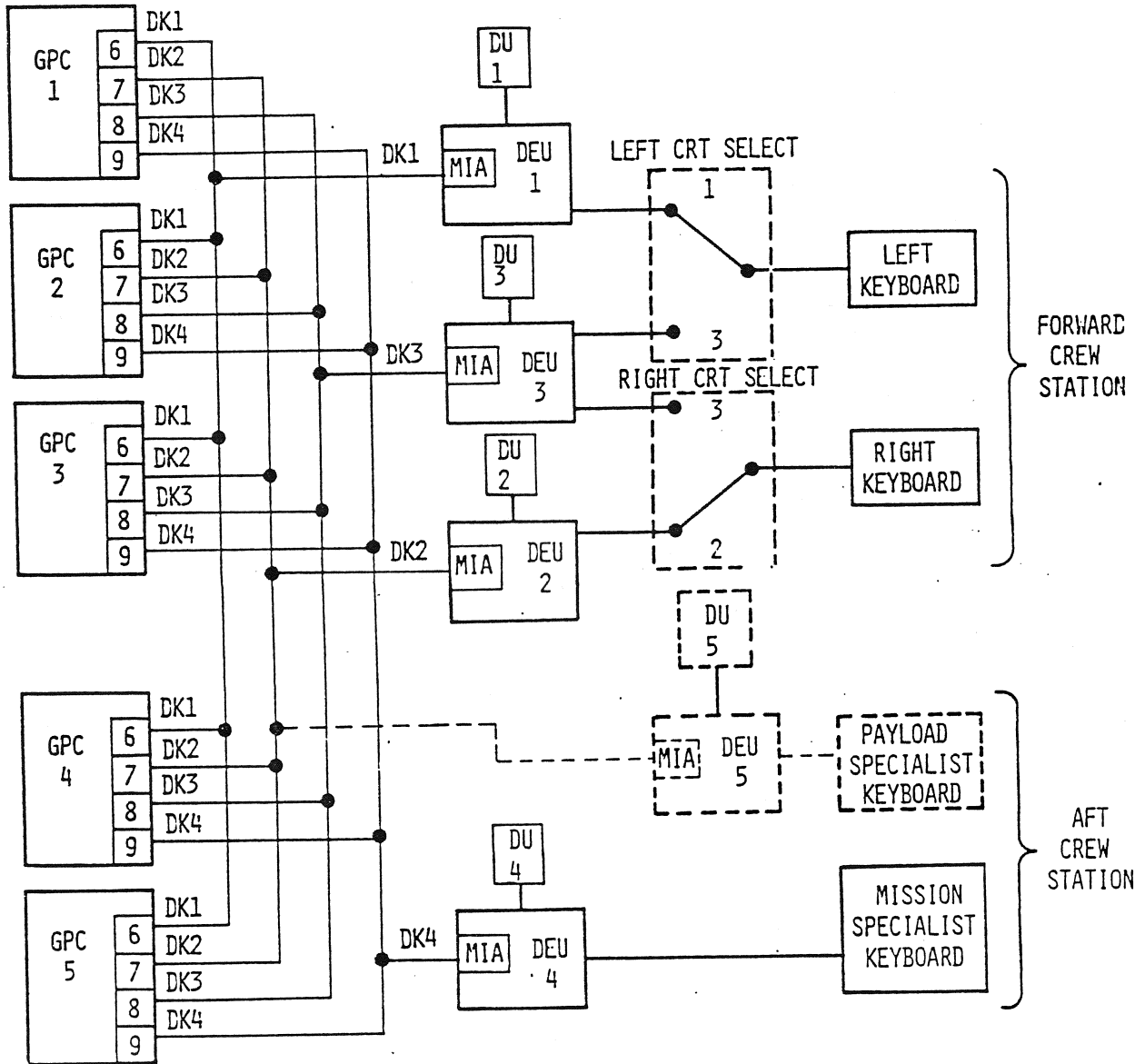


Figure 2-10. GPC/MCDS Interface

2.5.1.4 Fault Detection and Annunciation. The DEU maintains a capability via software and hardware logic to detect and annunciate certain MCDS problems and keyboard input errors:

- A. BITE. Each CRT contains DEU and DU GO/NO-GO flags on its front panel. These flags go to a NO-GO state (black and white) when a BITE-detected condition exists for 6 seconds but may be reset manually. If the problem is considered a critical situation (e.g. DEU memory parity error, power failure), the GPC DEU interface software will detect the appropriate BITE bits set and drive the CRT BITE fault message. At this time, PASS will cease to drive the CRT, but the BFS will continue to drive it.
- B. Flashing ERR. The DEU control logic performs certain syntax checks on keyboard messages before transmission to the GPC's. Input of an unexpected character (e.g. letter in an OPS request) or termination of a sequence without the required previous keystrokes will result in a flashing ERR on the scratch pad line after the offending keystroke. Using the CLEAR key or starting the message again will recover from the error.
- C. Big X. When a DEU detects that a GPC has not sent CRT data for 3 seconds, a corner-to-corner X will be drawn on its associated CRT and freeze all data on the screen. This state remains until a CRT data update command is received.
- D. POLL FAILURE. When a DEU detects that a GPC has not polled it for 3 seconds, the words POLL FAILURE appear on the left of the scratch pad line. This state remains until the DEU is polled by a GPC.
- E. Stand-alone Self-Test Program (STP). A special CRT display and DEU software can be used to verify the operation and interfaces involved in DEU operations immediately after GPC IPL and prior to initiating normal GPC/DEU operations.

2.5.2 Display Electronics Unit (DEU) Functional Description

Figure 2-11 illustrates a functional block diagram of an Orbiter DEU and the crew station control inputs to the DEU. The following is a functional description of these DEU components.

2.5.2.1 DEU MIA. The functions of the DEU MIA are the same as those of the IOP MIA.

2.5.2.2 DEU Control Logic. The DEU control logic validates GPC commands (address, operation, and word timing) and stores CRT display information from GPC commands in its own memory. The control logic also checks the crew station control discretes to determine which keyboard adapter to read, if a DEU memory load has been requested, and which major function software should be processing KBU's and processing display data. It also sends CRT display information to the symbol generator, provides timing signals for DEU operations and DU BITE, validates keyboard message inputs (syntax), and executes software to accomplish GPC command tasks.

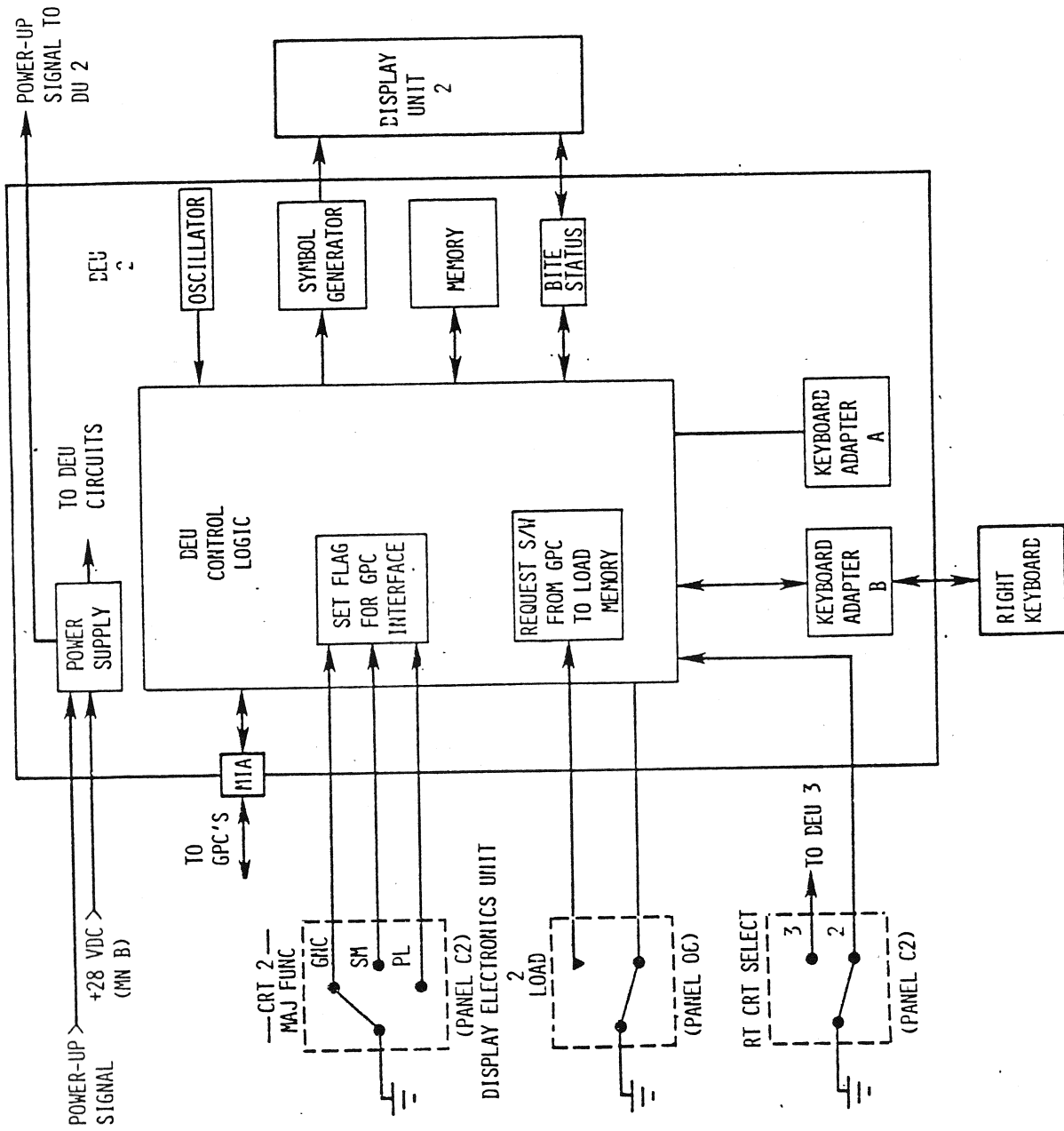


Figure 2-11. DEU Functional Block Diagram

2.5.2.3 DEU BITE. The DEU BITE maintains an OK/NOT OK status of its components.

2.5.2.4 Symbol Generator. The symbol generator transforms data from the control logic into control signals which are then sent to the display unit.

2.5.2.5 DEU Memory. The DEU has a memory area which provides storage for 8192 17-bit words (16 data bits and parity). This memory area is used to buffer keyboard messages, GPC input and output data, the CRT scratch pad and fault message lines, and CRT refresh data. This memory area also stores critical background CRT display formats. (NOTE: Not all CRT background formats are critical. The non-critical formats come from the GPC in use.)

2.5.2.6 Keyboard Adapter. The DEU keyboard adapter (of which there are two in each DEU) notifies the DEU control logic when a keyboard input is made and formats the status of all the keys for transmission to the control logic as requested.

2.5.2.7 Power Supply. The DEU power supply filters the main bus 28 V dc input power and converts this power into 5 V ac, 12 V dc, and 15 V dc. It also provides undervoltage detection for converted voltages and initiates a powerdown sequence when the input power drops below 17.5 V dc. The CRT attached to this DEU will blank should this powerdown sequence occur. It provides a POWER-UP discrete to the DU low-voltage power supply when its control logic circuitry is activated.

2.5.2.8 DEU Oscillator. The DEU oscillator provides 24 MHz timing signals to the DEU components, and also increments the time in DEU memory. Should the GPC stop sending time updates to the DEU, the time shown on the associated CRT will continue to update as a function of this oscillator.

2.5.3 Display Unit Functional Description. The functions of the DU components are outlined below. Figure 2-12 illustrates a functional block diagram of a DU.

2.5.3.1 X and Y Deflection Amplifier. The X and Y deflection amplifier amplifies the X- and Y-direction deflection signals to drive the CRT beam to the correct screen location.

2.5.3.2 Video Amplifier. The video amplifier amplifies analog signals from the symbol generator to control CRT beam intensity. It also scales total CRT screen brightness on the basis of brightness control inputs. The brightness control unit bases its inputs to the video amplifier on signals from the manual brightness control dial and the ambient light sensor located just below the CRT screen.

2.5.3.3 CRT. The CRT displays alphanumeric characters, graphic symbols, and vectors on a green-on-green phosphorus screen which is activated by a magnetically controlled beam.

2.5.3.4 DU BITE. The DU BITE maintains an OK/NOT OK status of the DU components. The status of both the DU and DEU BITE is also reflected on a pair of mechanical flags located just below the CRT screen.

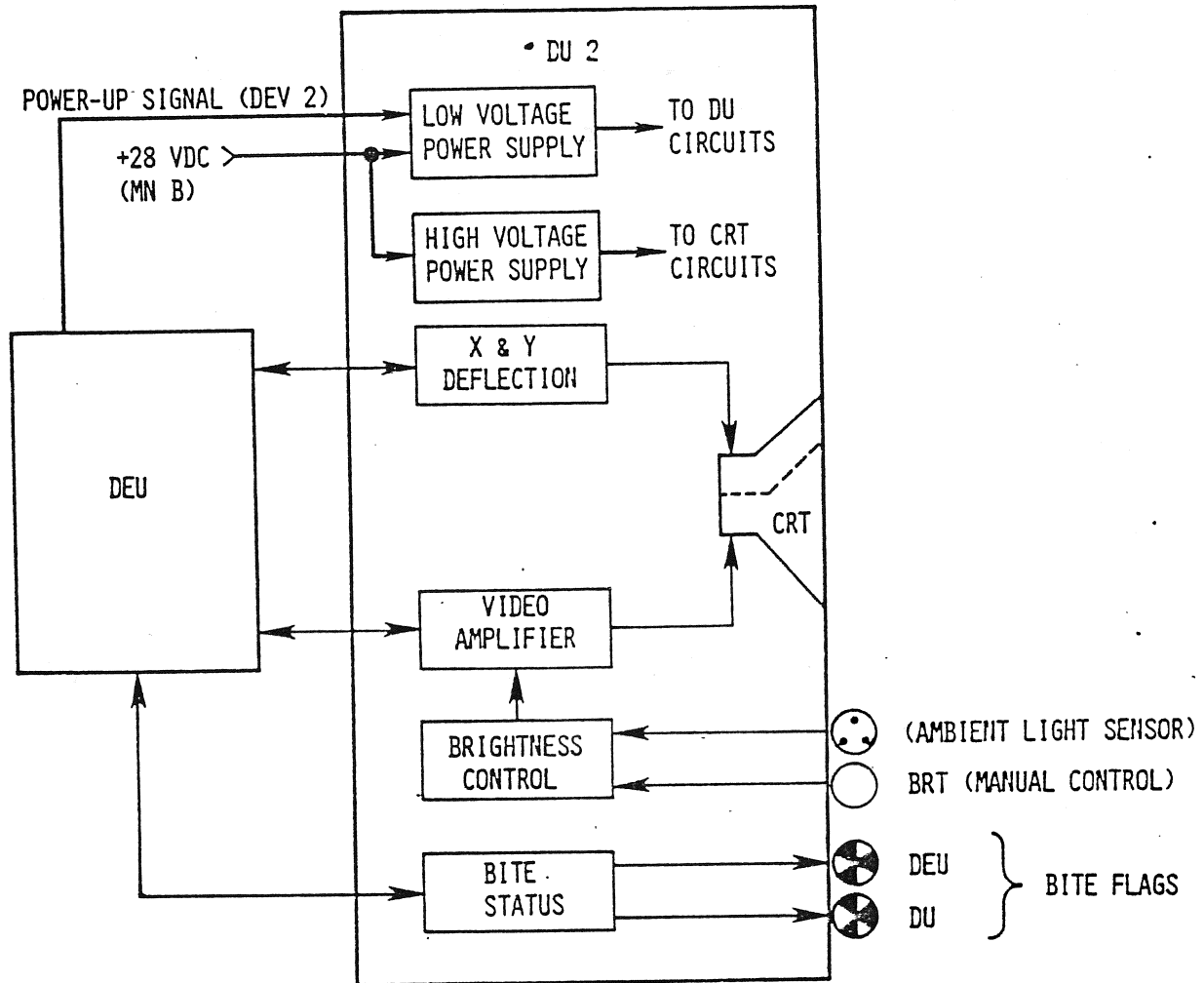


Figure 2-12. DU Functional Block Diagram

2.5.3.5 DEU Power Supply. The DEU power supply converts 28 V dc main bus power to 5, 15, 28 and 80 V dc sources for DU logic and amplifier needs, to 16,000 V dc to drive the CRT beam, and to 600 V dc for focus control. It also provides overvoltage/undervoltage detection and overcurrent protection.

2.5.4 Keyboard Unit. Figure 2-13 is a schematic of an Orbiter keyboard, and figure 2-9 indicates the locations of the three keyboards presently onboard the Orbiter vehicle. There are 10 number keys, 6 letter keys (used for hexadecimal data inputs), 2 algebraic-sign keys, a decimal key, and 13 special-function keys. Each keyboard consists of 32 momentary double-contact pushbutton keys. Each key utilizes its double contacts for communicating on separate signal paths to two DEU's (only one set of contacts on the aft station KBU keys is actually wired because this keyboard can only communicate with one DEU) and is illuminated by dual lamps driven by Orbiter ac power (5 V ac).

2.6 BACKUP FLIGHT CONTROLLERS (BFC'S)

There are three BFC's onboard the Orbiter. Each of these hardware devices contains two independently powered modules, and each of these modules provides the interface between one GPC and the crew station controls. The BFC interfaces are illustrated in figure 2-14. These interfaces consist of the GPC HALT command, the BFC ENGAGE discrettes, the BFC DISENGAGE discrettes, the BACKUP/NORMAL/TERMINATE discrettes, and those discrettes which control assignment of the forward DK bus(es) to the BFS GPC. Each BFC module is powered independently, with use of the same power source as the CPU of its associated GPC. For example, Module A of BFC 1, which transmits its discrettes to GPC 1, receives its power from the same source as GPC 1's CPU.

2.6.1 GPC/BFC Power Flow. A GPC receives its power when its associated GPC POWER switch is moved to the ON position. The power that is supplied to the GPC's CPU power supply is also supplied to that GPC's BFC module and to the BFC switch input circuitry (to be discussed later on in this section). A total loss of power to a GPC's CPU would also result in a total loss of power to that GPC's associated BFC module. There is a 5-amp fuse in the power supply line to the BFC module. Destruction of this fuse could cause the loss of a BFC module even though the CPU is still receiving its required power.

2.6.2 BFC Discrete Inputs

2.6.2.1 BFC ENGAGE Discrettes. The BFC ENGAGE pushbutton is a momentary pushbutton switch located on each of the two forward station Rotational Hand Controllers (RHC's). This pushbutton, when depressed, issues discrete signals to the BFC modules, which request that control of the vehicle be turned over to the BFS GPC. Although this pushbutton is momentary in physical design, the BFC ENGAGE discrettes are latched inside the BFC modules and remain in that state unless the BFC DISENGAGE switch is toggled, power is removed from the BFC module, or no GPC's OUTPUT switch is in the BACKUP position.

2.6.2.2 BFC DISENGAGE Discrettes. The BFC DISENGAGE switch is a simple two-position momentary toggle switch located on panel F6. The purpose of this switch is to request that control of the vehicle be given back to the PASS GPC's. This switch resets the BFS ENGAGE discrettes which were latched inside the BFC modules.

RIGHT KEYBOARD SCHEMATIC

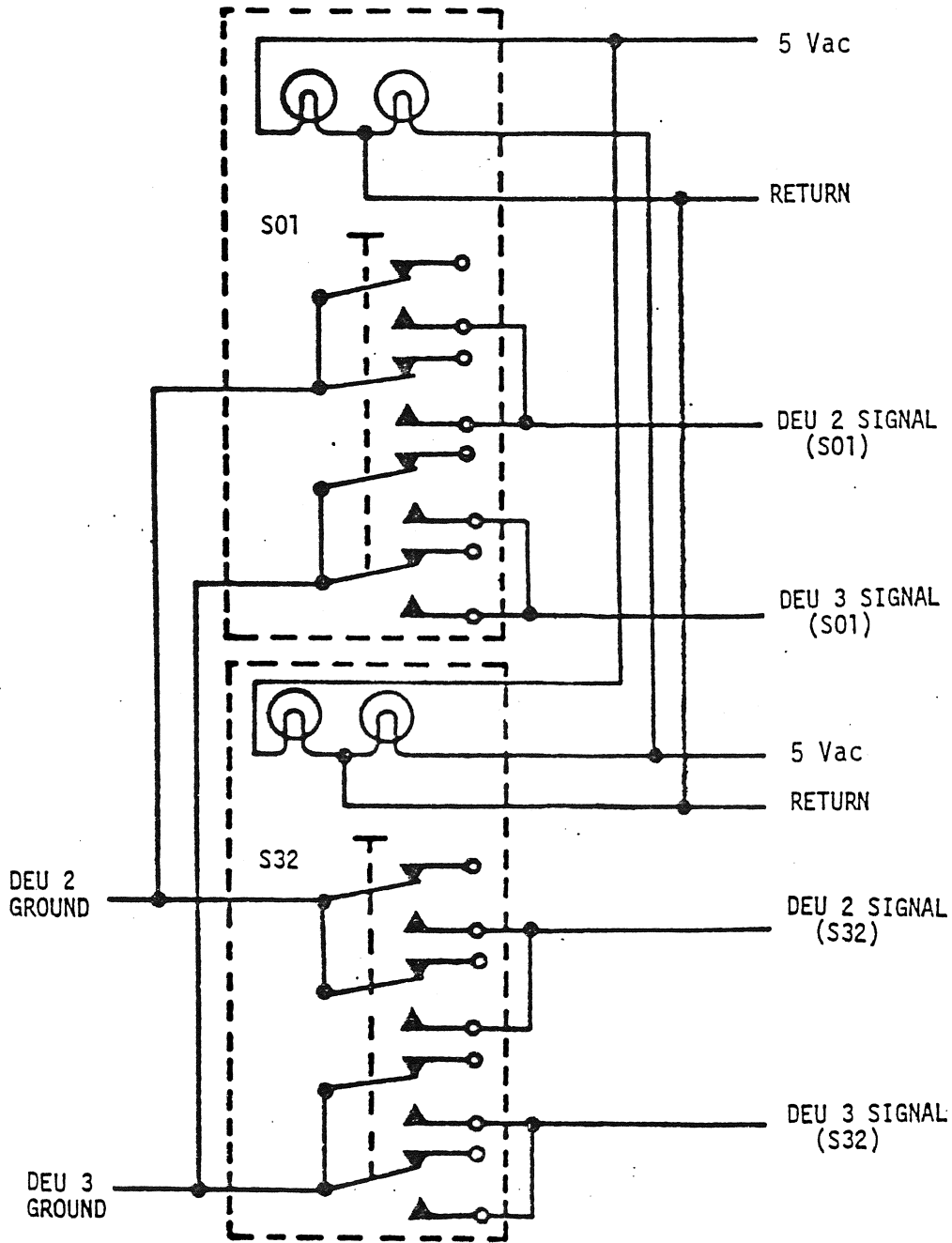


Figure 2-13. Keyboard Unit Schematic

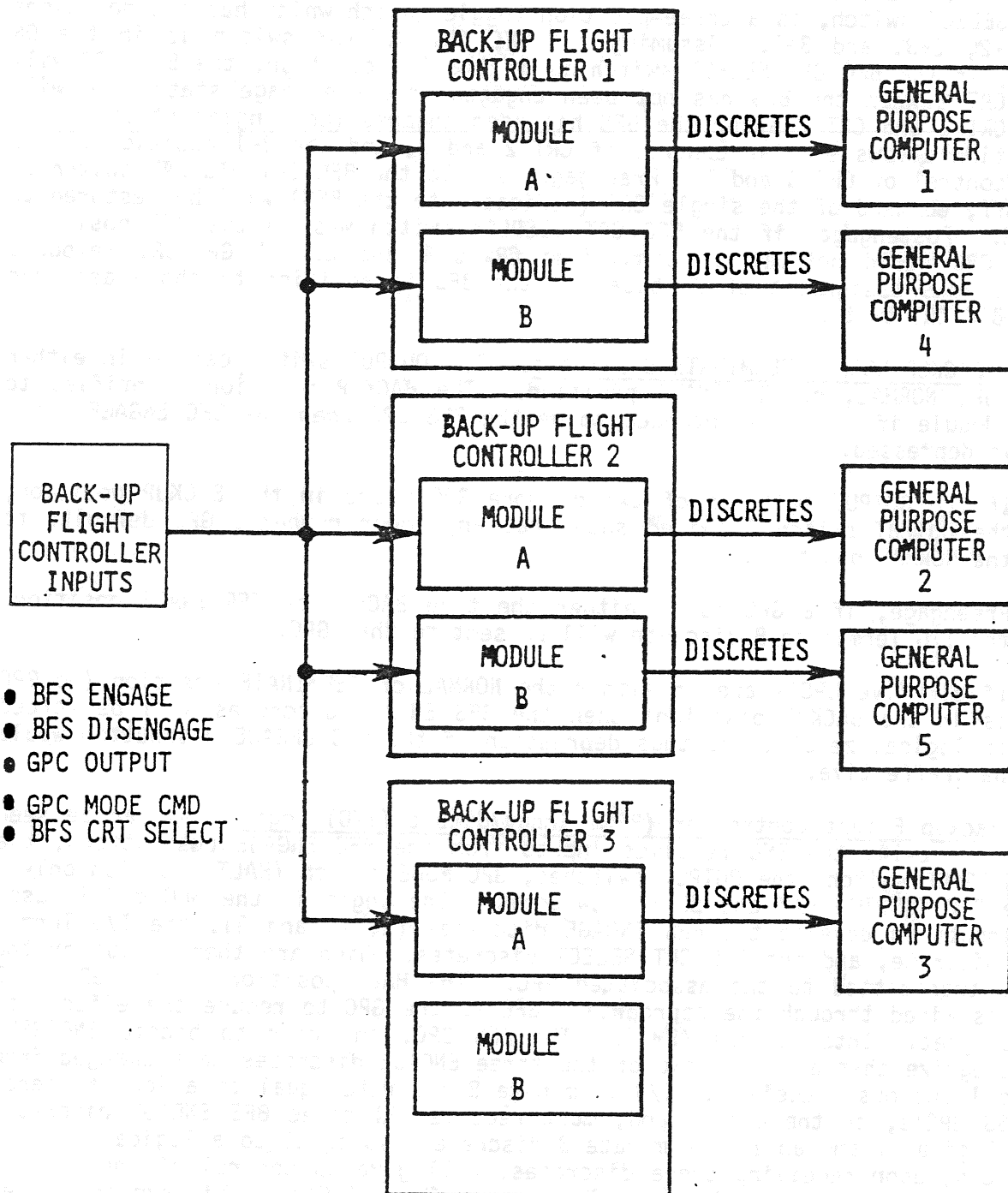


Figure 2-14. BFC Unit Data Interfaces

2.6.2.3 BFC CRT Discrettes. There are two switches on panel C3 which are known collectively as the BFC CRT switches. The left-hand switch, or BFC CRT DISPLAY switch, allows power from the three control buses (dioded together to form a single source) to flow to the BFC CRT SELECT switch. The right-hand switch, or BFC CRT SELECT switch, is a three-position toggle switch which has its positions marked 1+2, 2+3, and 3+1. Assuming the BFC CRT DISPLAY switch is in the ON position, if the BFC CRT SELECT switch is in the 1+2 position, the BFS GPC will command CRT 1 when the BFS has not been engaged (the preengage state) and will command CRT 1 and CRT 2 after the BFS has been engaged (postengage state). The 2+3 position allows similar control of CRT 2 and 3, and the 3+1 position allows similar control of CRT 3 and 1. Preengage, should the BFC CRT DISPLAY switch be turned off, command of the single CRT (dedicated to the BFS) will be restored to the PASS. Postengage, if the BFC CRT DISPLAY switch was in the OFF position, the BFS GPC would default to commanding CRT's 1 and 2. A GPC/CRT keyboard message allows assignment of DK buses to the BFS in addition to those assigned via the BFC CRT switches.

2.6.2.4 BACKUP/NORMAL/TERMINATE Discrettes. The OUTPUT switch can be in either the BACKUP, NORMAL, or TERMINATE position. The BACKUP position identifies to the BFC Module if a GPC is intended to be the BFS GPC when the BFC ENGAGE pushbutton is depressed.

- A. If the OUTPUT switches of two or more GPC's are in the BACKUP position, the OUTPUT switch is wired such that any lower numbered GPC defaults to the NORMAL position.
- B. Preengage, if a GPC is in either the true BACKUP or TERMINATE position, the I/O Terminate B discrete will be sent to that GPC.
- C. If all five GPC's are in either the NORMAL or TERMINATE position (no GPC is in the BACKUP position) then the BFS ENGAGE discrettes will be forced to logical zero's, and thus depression of the BFC ENGAGE pushbutton would be ineffective.

2.6.3 Backup Flight Controller (BFC) Input/Output (I/O) Logic. As can be seen from figure 2-14, the BFC receives inputs from the BFC ENGAGE pushbuttons, the BFC DISENGAGE switch, the OUTPUT switches, GPC MODE switch (HALT position only), and the BFC CRT DISPLAY and SELECT switches. The logic in the BFC module uses these inputs to develop the BFS ENGAGE discrettes (1, 2, and 3), the I/O Terminate B discrete, and the BFS CRT SELECT discrettes, which are then output by the BFC and transmitted to the associated GPC. The HALT position of the GPC MODE Switch is wired through the appropriate BFC to the GPC to reduce the effects of Electromagnetic Interference (EMI). The BFS GPC, in order to become ENGAGED, must recognize that at least two of the three ENGAGE discrettes have changed from zero to 1 and must receive an I/O Terminate B discrete equal to a logical zero. The PASS GPC's, on the other hand, must receive all three BFS ENGAGE discrettes set to logical 1 and an I/O Terminate B discrete also equal to a logical 1. The PASS GPC's, upon receiving these discrettes, will give up control of their dedicated buses and enter a software halt state. These GPC's would have to be re-initialized with an IPL sequence before they could be used again with any guarantee of success.

Each GPC interrogates the ENGAGE discrettes and the I/O Terminate B discrete inputs to determine if a valid BFS Engage or Disengage condition exists. Also, the I/O Terminate B discrete provides for hardware control of the FC data bus transmitters; i.e., if a GPC detects its I/O Terminate B discrete = 1, it cannot transmit on the FC data buses. Furthermore, a PASS GPC must receive an I/O Terminate B discrete = 1 as well as the BFS ENGAGE discrettes 1 = 2 = 3 = 1 to recognize the BFS ENGAGE condition.

The GPC OUTPUT switch logic shows that if the OUTPUT switch is in the TERMINATE position, or if the OUTPUT switch is in the BACKUP position and there is no higher numbered GPC with its OUTPUT switch in BACKUP, a logical one will be transmitted via a 1 second time delay to the BFC. Therefore on the assumption that the three BFS ENGAGE discrettes are set to a logical 1 only the highest numbered GPC with its OUTPUT switch in the BACKUP position will receive the correct discrete pattern in order to assume control as the BFS GPC. All the other GPC's, assuming no failures, will receive the correct discrete pattern which will tell them to surrender control of their buses.

2.7 DPS ACTIVATION

The following is a series of activation procedures showing an acceptable order of activating the DPS. These procedures assume that the power and cooling subsystems have previously been activated. FMDM's will be powered on when the pallet is activated.

2.7.1 MMU Activation. The only activation required for the MMU is to place the MMU 1 (2) POWER switches to ON on panels O14 (O15). The MMU's may require as much as 34 seconds before indicating RDY on the DPS utility display.

For non-IPL use, the IPL SOURCE switch should be in the OFF position on panel O6.

2.7.2 MDM Activation. The activation procedure for the DPS MDM's is to place the eleven POWER switches on panel O6 to ON.

FLT CRIT AFT (four)	- ON
FLT CRIT FWD (four)	- ON
PL (three)	- ON

Note: MDM's should be powered up before the GPC's are activated to prevent I/O errors from occurring.

2.7.3 MCDS Activation. The four DEU/CRT's are normally activated by placing the appropriate CRT POWER switch on panels C2 and R12 in the STANDBY position for 30 seconds and then in the ON position.

CRT 1 (2,3) Power	- ON panel C2
CRT 4 Power	- ON panel R12

If the DEU memories have never been loaded, then a DEU memory load is required. The procedure for this process is included in the GPC Activation section (section 2.7.4.2).

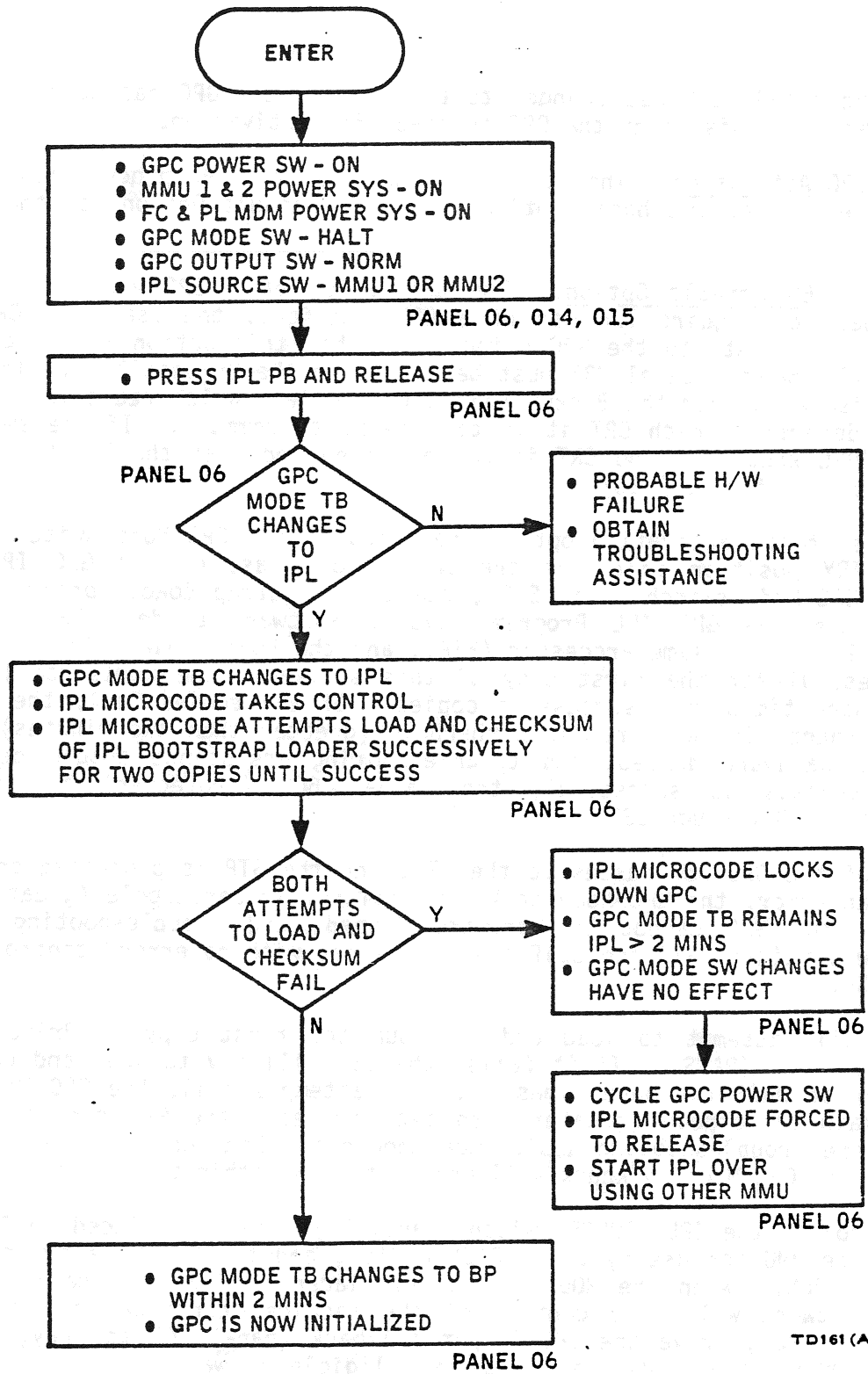
2.7.4 GPC Initialization and Activation. This section concerns itself with the processes of Initialization and Activation, collectively referred to as the Initial Program Load (IPL) process. Regardless of the activation option used, all GPC's are initialized in the same manner.

2.7.4.1 GPC Initialization. The first consideration in GPC initialization is switch configuration. The GPC Power switch (panel 06) for the GPC to be IPL'd, the MMU 1 and MMU 2 Power switches (panels 014 and 015), and the MDM Power switches (panel 06) must be placed in the ON position. The MODE switch (panel 06) for the GPC to be IPL'd must be placed in HALT. This will put the GPC in a hardware controlled state. The Output switch (panel 06) for the GPC to be IPL'd must be placed in the NORMAL position, allowing the GPC command capability on the Flight Critical data buses. The IPL Source switch (panel 06) must be placed in the position for the Mass Memory that is to be used as the source for the initialization software (see figure 2-15).

It should be noted that the position of the IPL source switch is monitored by any other processing GPC's and can affect their operation. If the IPL source switch is in the MMU 1 or MMU 2 position, the BFS GPC (if a BFS GPC is currently active) will be unable to command the CRT specified by the first number of the position selected with the BFC CRT DISP and SEL switches (panel C3). This is done to make it possible to perform a Menu Load IPL (2.7.4.2.2). If the IPL source switch is in the MMU 1 or MMU 2 position, the PASS GPC's operating in Common Set will redundancy manage the switch discretely. If a majority of the CS recognizes the switch in MMU 1 or MMU 2, all the CS GPC's will be software inhibited from accessing that Mass Memory; if an equal number of CS GPC's defect the discrete as those that do not, no change in the availability state of the MMU will occur; and if a minority of the CS GPC's or no CS GPC detects the discrete, no software inhibit is set. In the latter cases, a race condition could exist between MMU requests by the IPLing GPC and a CS GPC.

At this point, the necessary switches have been configured for initialization, and the process may be started. (It should be noted that only one GPC may be IPL'd at one time.) The process is started by pressing and releasing the Initial Program Load pushbutton (panel 06) for the GPC to be IPL'd. The Mode talkback for the GPC to be IPL'd will change to IPL, indicating the start of the initialization process. If the Mode talkback does not change to IPL, this indicates a probable hardware failure of some kind.

Once the Mode talkback has changed to IPL, the IPL Microcode (firmware) takes control of the GPC. The Microcode will load the value C9FB (protected half-words) into locations 00000 to 1FFFFF. The Microcode will then load copy number 1 of the IPL Bootstrap Loader and checksum it. If the checksum is not good, the Microcode will load and checksum a second copy of the Bootstrap Loader. If either checksum is good, the Microcode releases control of the GPC, and the Mode talkback changes back to barberpole. If neither checksum is good, the Microcode retains control and locks down the GPC. If this happens, the Mode talkback will remain IPL longer than two (2) minutes, and changes in the Mode switch position will have no effect. The only way to force the Microcode to release control at this point is to cycle the GPC Power switch. After doing this, the IPL process may be tried again; however, the other MMU should be used.



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Figure 2-15. GPC Initialization

When the Mode talkback has changed to barberpole, the GPC has been successfully initialized. At this point the GPC is ready for activation.

2.7.4.2 GPC Activation. The activation phase of the IPL process may be accomplished by either of two basic options, the DEU Default Option, or the Menu Load Option.

2.7.4.2.1 DEU Default Option. The activation of a GPC via the DEU Default Option does not require the use of a CRT; in fact, the use of a CRT is precluded. To indicate to the GPC being IPL'd that this option is being used, the BFC CRT DISP switch (panel C3) must be placed in the OFF position. The GPC will monitor discretes from the Backup Flight Controller (which reads this switch) in order to determine which CRT it is to attempt to command. If the switch is in OFF, the GPC knows that no CRT is to be driven and that the DEU Default Option is desired (see figure 2-16).

Regardless of the activation option used, moving the GPC Mode switch (panel O6) to the STBY position initiates the activation phase of the GPC IPL process. Once the GPC Mode switch is in STBY, the IPL Bootstrap Loader program will load and checksum the GPC IPL Program, System Software Loader (SSL), Self Test Program (STP), Real Time Processor (RTP), and the Load Table. If the process is not successful for the first copy of this software, the Bootstrap Loader will try two more times with successive copies. If all copies fail, the GPC's Mode talkback (panel O6) will remain barberpole (greater than two minutes). The GPC cannot be hardware dumped, and troubleshooting assistance should be obtained. If the process is successful, the value C6C6 (protected) is loaded into addresses 20000 through 33FFF.

Control of the GPC now passes to the STP, and the STP is processed once. If it detects an error, the GPC Mode talkback will remain barberpole (greater than two minutes), the GPC cannot be hardware dumped, and troubleshooting assistance should be obtained. If the self test completes with no error, control will pass to the SSL.

The SSL will attempt to load and checksum the first copy of Primary Avionics System Software (PASS). If it fails, the SSL will try to load and checksum the same copy of PASS two more times. If all attempts fail, the GPC Mode talkback will remain barberpole (greater than two minutes), the GPC cannot be hardware dumped, and troubleshooting assistance should be obtained. If the load is successful, the GPC Mode talkback will change to RUN within two minutes.

At this point, the IPL SOURCE switch (panel O6) should be placed in OFF (thereby freeing the MMU for use by other PASS GPC's), and the GPC Mode switch should be placed in RUN. When the MODE switch is placed in RUN, the newly loaded PASS system software will take control of the machine, continue to drive the Mode talkback to RUN, drive the GPC Output talkback (panel O6) to gray, and attempt to drive the OPS 000 display onto any eligible forward CRT. These DEU/CRT's which are eligible are those which are loaded with software and not designated by the BFC CRT Display and Select switches to be BFS CRT's (assuming no CRT is

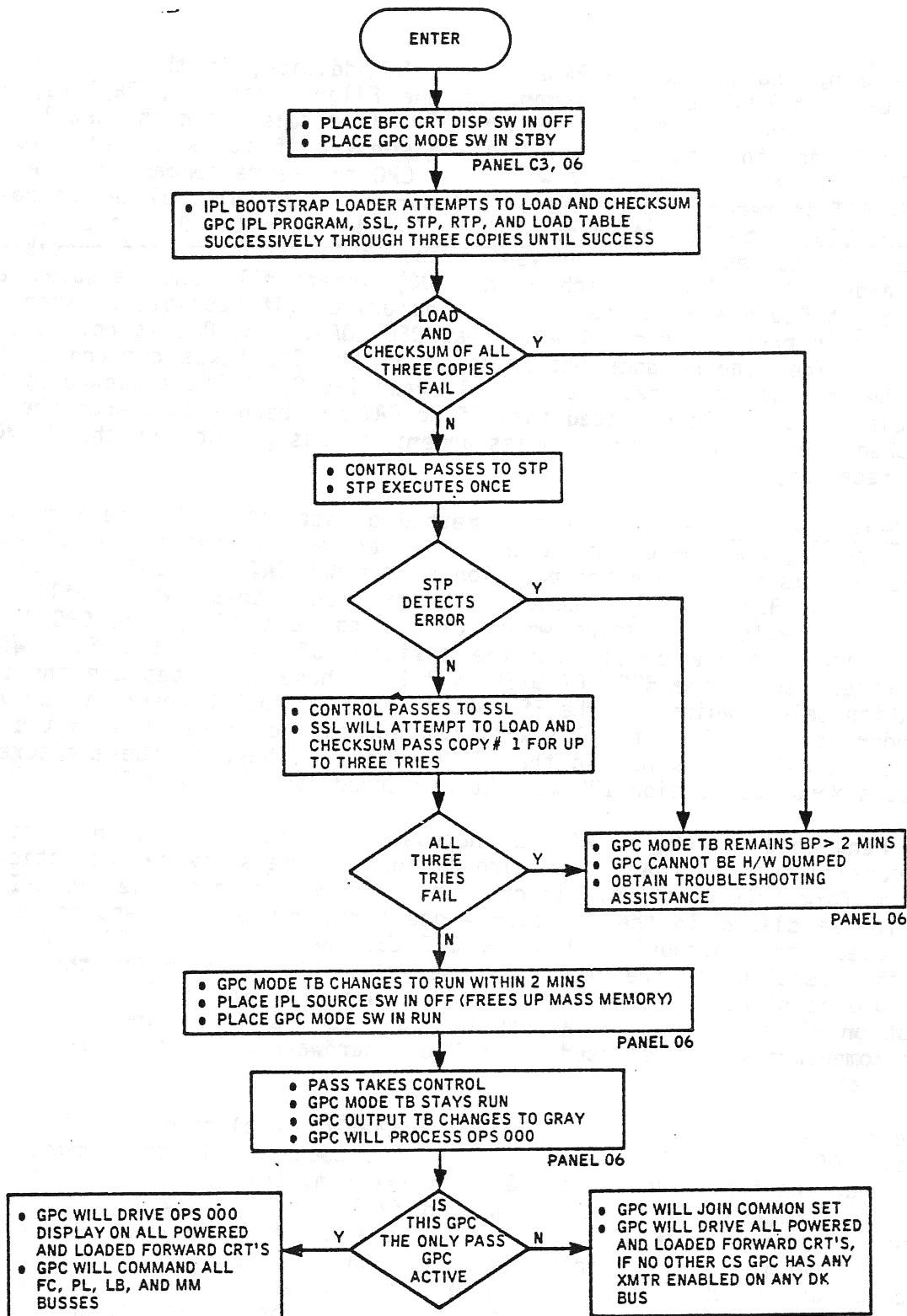


Figure 2-16. DEU Default Option

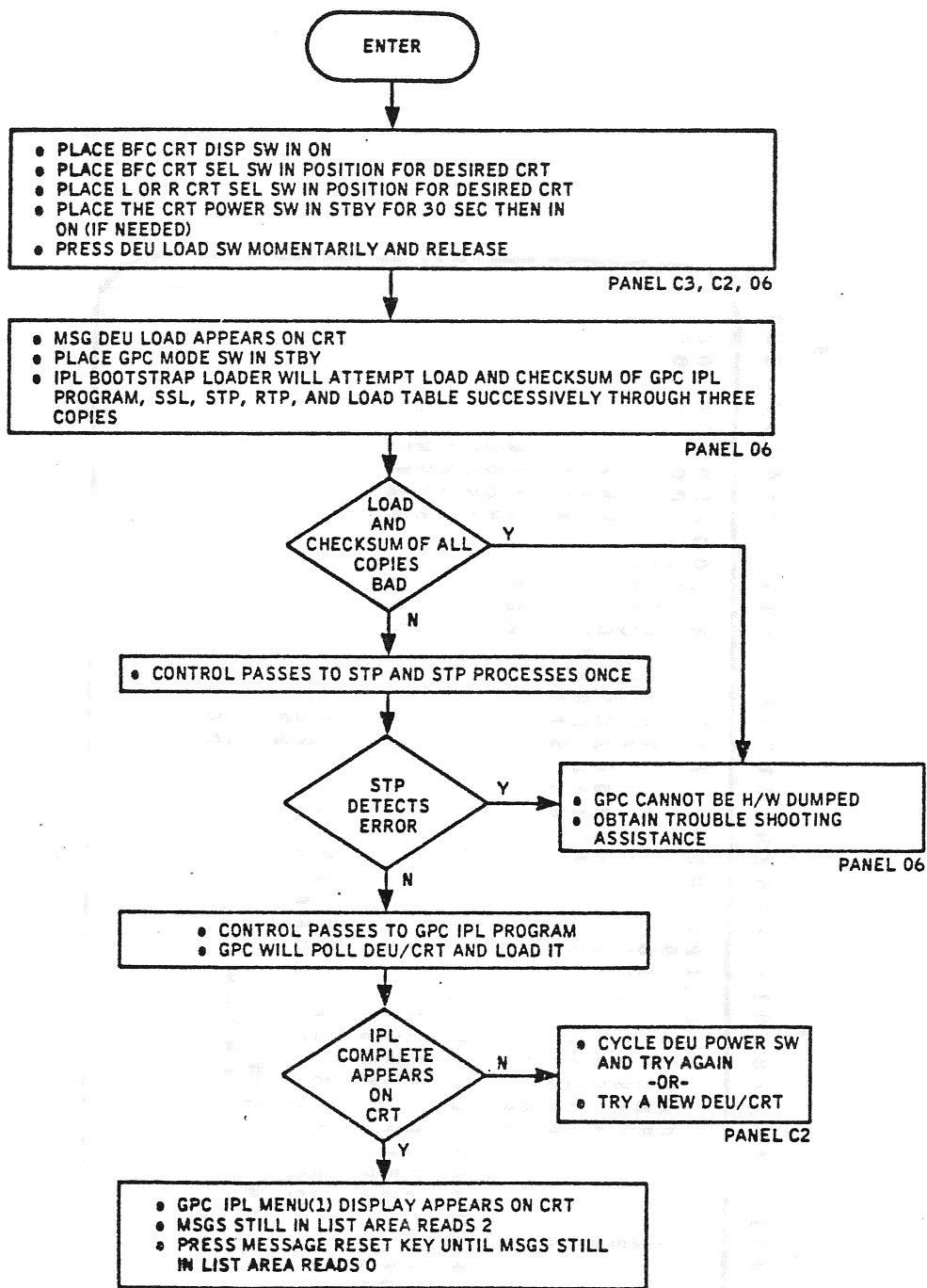
TD161 (B)

being commanded by another active PASS GPC). In addition, if this GPC is the only active GPC, it will assume command of the Flight Critical, Payload, and Launch Buses. At this point the activation phase is complete and the GPC IPL is complete. It is possible to load a DEU at this point if it is needed. To do this, it will be necessary for the newly IPL'd GPC to assume command of the CRT while the DEU/CRT is requesting a load of software. To do this, place the power switch for the DEU to be loaded (panel C2) in ON, deassign the DEU to be loaded via a CRT that is currently being driven by the newly IPL'd GPC (if possible), press the target DEU's LOAD switch (panel O6) momentarily and release, and assign the target DEU via a CRT currently being driven (if possible). When the DEU load switch is pressed, the CRT will read DEU LOAD. The DEU is not loading at this point. The loading does not begin until the GPC takes command of the CRT. When the load is complete, the DEU will read IPL COMPLETE, followed by the OPS 000 display. It should be noted that if no CRT has been loaded when the GPC is IPL'd, then the steps requiring deassignment or assignment via the GPC/CRT key are not necessary.

2.7.4.2.2 Menu Load Option. The second method of activation is the Menu Load Option and does require the use of a CRT. As before, the indication of which option to be used is based upon the position of the BFC CRT DISP switch. If the switch is on, the Backup Flight Controller that reads this switch will send discretes to the GPC's, indicating which CRT is to be used by the GPC to be IPL'd. The discretes are based upon the position of the BFC CRT SEL switch which is located beside the BFC CRT DISP switch. These discretes are the same discretes which select which CRT the BFS GPC is to command. However, to prevent dual commanders on this CRT, the BFS will not attempt to drive it when the IPL SOURCE switch (panel O6) is not in the OFF position. Thus, if these discretes are present, a Menu Load Option IPL will be performed (see figure 2-17).

To use the Menu Load Option, it will be necessary to load the DEU in question. This is necessary even if the DEU is already loaded; the software automatically expects to perform this function. In order to prepare for this, the BFC CRT SEL switch should be placed in the position whose first number corresponds to the CRT to be used, the appropriate L or R CRT SEL switch (panel C2) should be placed in the position for the CRT to be used, the POWER switch for the CRT to be used should be placed in STBY for 30 seconds and then in the ON position (if it were not on already), and the appropriate DEU LOAD switch (panel O6) should be pressed momentarily and released. The DEU's hardware will drive DEU LOAD on the CRT's scratch pad line.

At this point the activation phase can be initiated by placing the GPC's MODE switch (panel O6) in the STBY position. The IPL Bootstrap Loader program will attempt to load the first copy of the GPC IPL Program, the SSL, STP and the Load Table and then checksum them. If it should fail, it will try two more times (copies two and three). If all should fail, the GPC MODE talkback (panel O6) will remain barberpole greater than 2 minutes, the GPC cannot be dumped via a hardware dump, and troubleshooting assistance should be obtained. If the load and checksum are good, the value C6C6 (protected) will be loaded between addresses 20000 and 33FFF and control will be passed to the STP.



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Figure 2-17. MENU Load Option

1	2	3	4	5
12345678901234567890123456789012345678901				
PASS1	1*	GPC IPL MENU (1)	4	000/00:00:00
BFS1	2	PASS5	9	000/00:00:00
PASS2	3	BFS5	10	STP CYCLE COUNT
BFS2	4	PASS6	11	ERROR/MSG CODE
PASS3	5	BFS6	12	ERROR/MSG CODE CNT
BFS3	6	PASS7	13	TOTAL ERR/MMSG CNT
PASS4	7	BFS7	14	MSGG STILL IN LIST
BFS4	8	PASS8	15	MCDG BITE
		BFS8	16	MODE
17 DEU FORMAT LOAD				BSR1
START GPC SELF TEST 18				BSR2
STOP GPC SELF TEST 19				SWSW
START DEU SELF TEST 20				BITE
				PCM
START D/L OF TOGGLE BUFFER 1				
STOP D/L OF TOGGLE BUFFER 5				
START D/L ON ERROR				
STOP STOP ON ERROR				
CONTINUE STP ON ERROR				
INHIBIT CKPT LOAD				

Figure 2-18. GPCIPL MENU (1) Typical Display

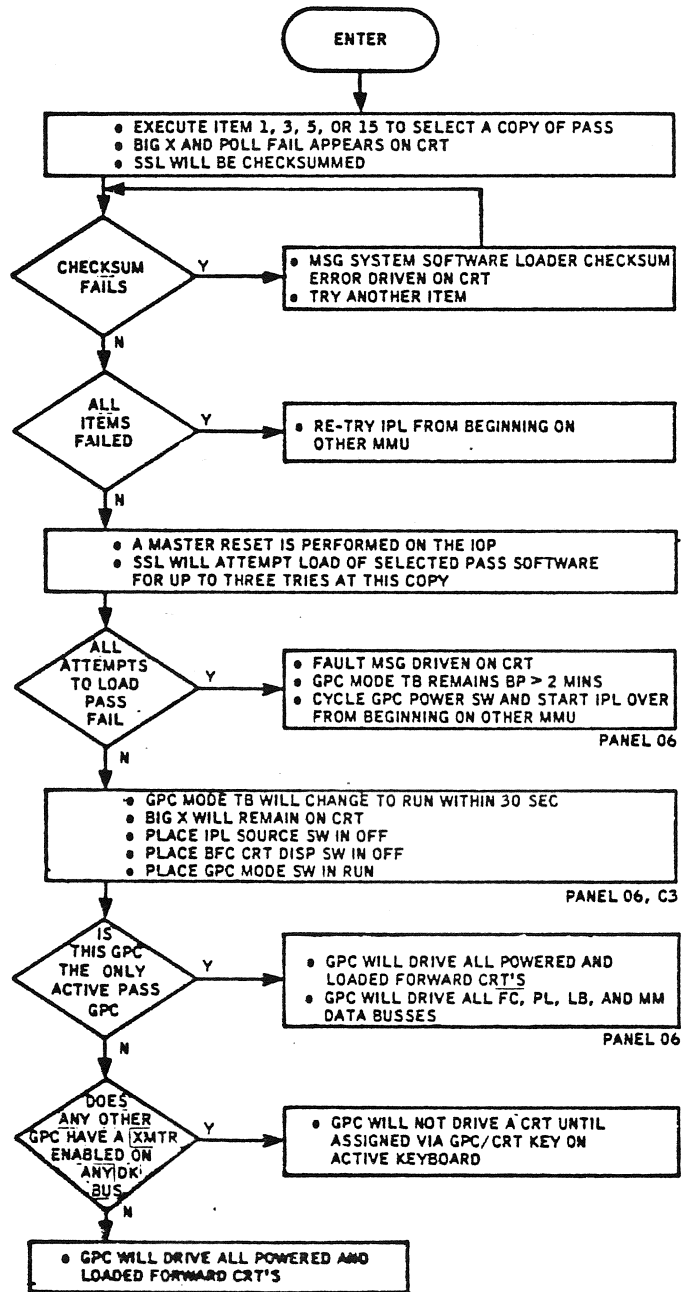
The Self Test Program will cycle once to perform a diagnostic on the GPC. If this fails, the indications are the same as those for failure of the GPC IPL Program, etc., load, and checksum. If the self test is good, control will pass to the GPC IPL Program. The GPC will poll the CRT specified by the BFC CRT SEL switch and recognize the DEU load request. The GPC will obtain the DEU's software load from mass memory and load it into the DEU. If this is successful, the message IPL COMPLETE will be driven on the CRT followed by the GPC IPL MENU (1) display (see figure 2-18). If it is not, the message IPL INCOMPLETE will be driven on the CRT. If this happens, cycling the power on the CRT and pressing the DEU LOAD switch may help. If it does not, it will be necessary to set all the appropriate switches for another DEU to be used and attempt to load that DEU. If this is not successful, obtain troubleshooting assistance.

At this point the GPC will start updating the time and display its GPC driver number on the CRT. On the GPC IPL MENU (1) display the STP CYCLE COUNT area will be set to 1 to indicate the single execution of the self test; the TOTAL ERR/MSG CNT and MSG's STILL IN LIST areas will be set to 2 to indicate the two expected fault messages currently in the stack; and the ERROR MSG CODE area will be set to 203 to identify the fault message currently flashing on the fault message line. The message will read GPCIPL AA.BB.CC.DD.EE LOADED (where AA = S/W release number, BB = version number, CC = patch set number, DD = I-Load set number, EE = mass memory area number). Pressing the Message Reset Key will erase this message, change the ERROR/MSG CODE to 208, and display the next message. The next message will read DCP AA.BB.CC.DD.EE LOADED (where AA, BB, CC, DD, EE have the same meanings as in the previous example). The MSGS STILL IN LIST and ERROR/MSG CODE areas should be set to 0 at this point. If they are not and the value in the ERROR/MSG CODE area is 130 or 149, the process will still succeed normally. In this case press the Message Reset Key until the MSGS STILL IN LIST area displays 0. If some message code other than the two above appears, the IPL process may not succeed. In this case, you should start over from the beginning of the IPL process. (It should be noted that all the message codes used here refer to version 6 IPL software, only.)

From this point on it is possible to complete the activation phase by loading either PASS or BFS software. The following sections will describe the processes for the two cases.

2.7.4.2.2.1 PASS Load Via Menu Load Option. The selection of a PASS load is accomplished via an item entry to the GPC IPL MENU display (see figure 2-19). There are three copies of the PASS software on each memory. The selection of the item determines which copy will be used for the load of PASS software and for all future mass memory accesses with this GPC (such as OPS transitions, IFL's, etc.). Items 1 and 15 will select PASS copy number 1, Item 3 will select PASS copy number 2, and Item 5 will select PASS copy number 3. All other PASS items are not active, and their selection will result in a fault message.

After the item is executed, the CRT will display the BIG X and POLL FAIL. The System Software Loader will be checksummed. If the checksum fails, the message System Software Loader Checksum Error will be driven on the CRT, and another PASS item should be tried. If all PASS items fail, the IPL must start over from the beginning. If the checksum is good, the value C6C6 (protected) will be loaded into addresses 09000 to 33FFF, a master reset will be performed on the IOP, and the PASS ID (from the item) is stored for use by the SSL.



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Figure 2-19. Pass Menu Load Option

The SSL will attempt to load the selected PASS software load and checksum it. If it fails the attempt, it will try this copy two more times. If all attempts fail, a fault message will be driven on the CRT and the GPC's MODE talkback will remain barberpole greater than 2 minutes. Then it would be necessary to cycle the GPC POWER switch and start the IPL process over again. If the load and checksum are successful, the MODE talkback will change to RUN within 30 seconds. The BIG X will remain on the CRT.

At this point, the IPL SOURCE switch should be placed in OFF, the BFC CRT DISP switch should be placed in OFF, and the GPC MODE switch should be placed in RUN. If the PASS load and the DEU load work correctly, the GPC is capable of driving a CRT with PASS displays. If this GPC is the only PASS GPC active (first to be IPL'd) or if no other PASS GPC has a transmitter enabled on any forward DK (CRT) bus, then this GPC will attempt to drive all three forward CRT's. If any other PASS GPC has a transmitter enabled on any DK bus, it may be necessary to assign the newly IPL'd GPC a CRT via a GPC/CRT key entry to an active PASS CRT. When the GPC does drive a CRT, the OPS 000 display should appear. If this GPC will not drive a CRT, obtain troubleshooting assistance.

2.7.4.2.2 BFS Load Via Menu Load Option. The selection of a BFS load is also accomplished via an item entry to the GPC IPL MENU display (see figure 2-20). There are three copies of the BFS software on mass memory, and they are accessed via items 2, 4, and 6, respectively. Before an item is selected, the GPC OUTPUT switch (panel 06) should be placed in BACKUP.

When a BFS item is selected, the GPC will attempt to load and checksum the BFS Phase Table and the Backup System Loader 1 (BSL 1). If the load and checksum fail, a fault message will be driven on the CRT, and a new copy of the BFS should be selected. If the load and checksum are good, the BSL 1 will load the BSL 2 and checksum it. If this checksum fails, the same events as above apply. If the load and checksum are good, the BSL 2 load will be protected and control will pass to the BSL 2.

The title of the display should change to BSL 2 IPL MENU within two minutes. If it does not, it will be necessary to cycle the GPC POWER switch and begin the IPL process over again. After the display title changes, MET will start counting from zero and the message BSL AA.BB.CC.DD.EE LOADED (where AA = release number, BB = version level, CC = patch level, DD = I-load level, and EE = MMU area number) will be driven on the CRT. The Message Reset Key should be pressed at this time until the MSG's still in list area reads 0. The fault message will blank and an attempt to load and checksum the selected copy of BFS will be made. If it is not successful, the fault message MMU COMPUTED CHECKSUM MISCOMPARE will be driven on the CRT, the GPC POWER switch will need to be cycled, and the IPL process will need to be repeated from the beginning. If it is successful, the DEU/CRT will not be updated during the BFS load and checksum, the BIG X and POLL FAIL will appear on the CRT, and the BFS load will be protected.

If the BFS load was completed successfully, the BIG X and POLL FAIL will no longer be driven, and the message BFS AA.BB.CC.DD.EE LOADED-SET MM SEL SW TO OFF (where AA, BB, CC, DD, EE mean the same as before) will be driven on the CRT. The BSL will now monitor the IPL SOURCE switch. When the IPL SOURCE switch is

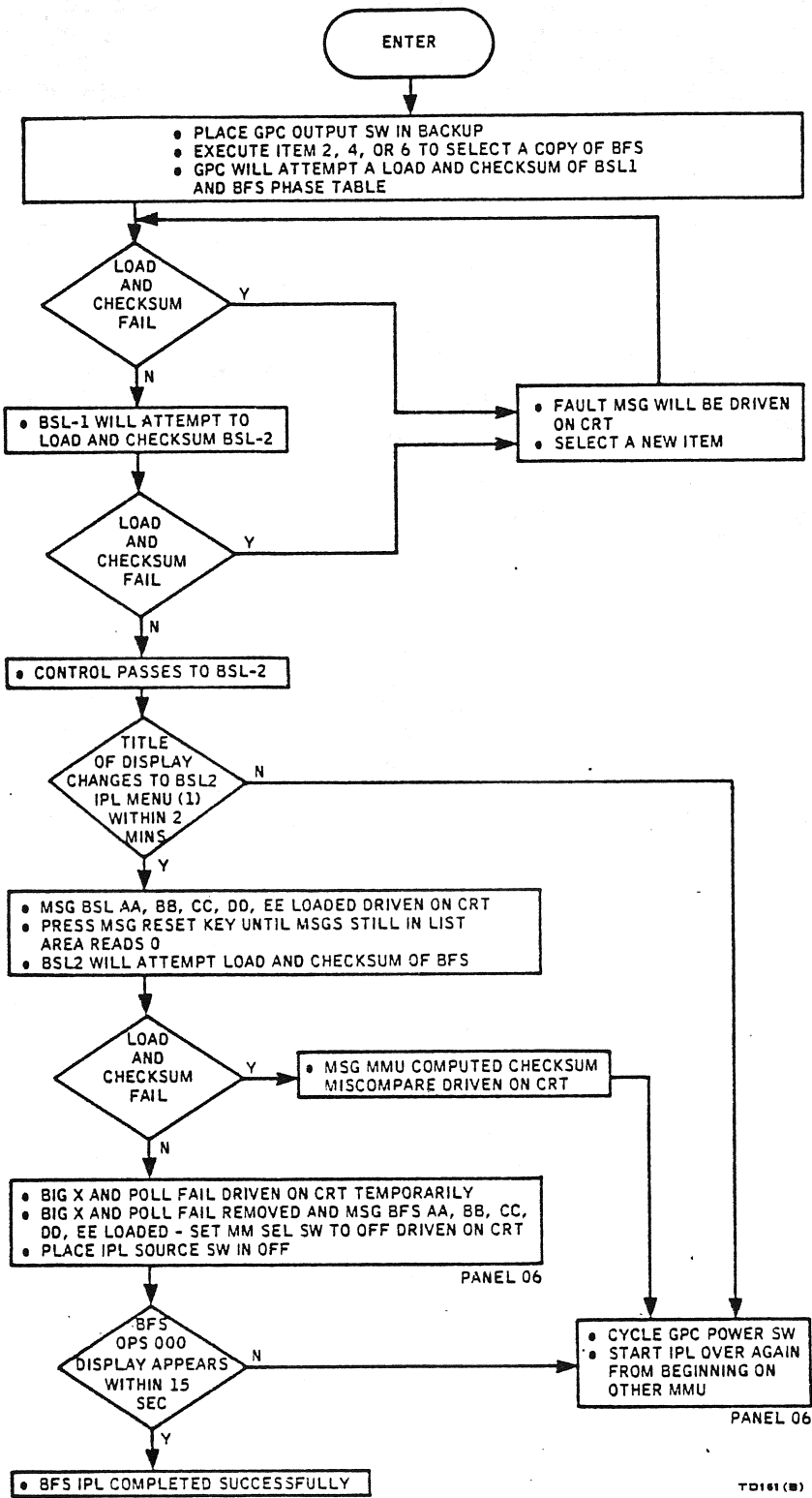


Figure 2-20. BFS Menu Load Option

placed in OFF, the BIG X and POLL FAIL may appear on the CRT, the GPC Preferred Storage Area is loaded with the BFS PSA and protected, and control is passed to the BFS software. The BFS OPS 000 display should appear within 15 seconds after the IPL SOURCE switch is placed in OFF. The newly IPL'd BFS GPC should be driving the same CRT since the BFC CRT DISP and SEL switches assign a CRT to the BFS (disengaged) when the IPL SOURCE switch is in OFF.

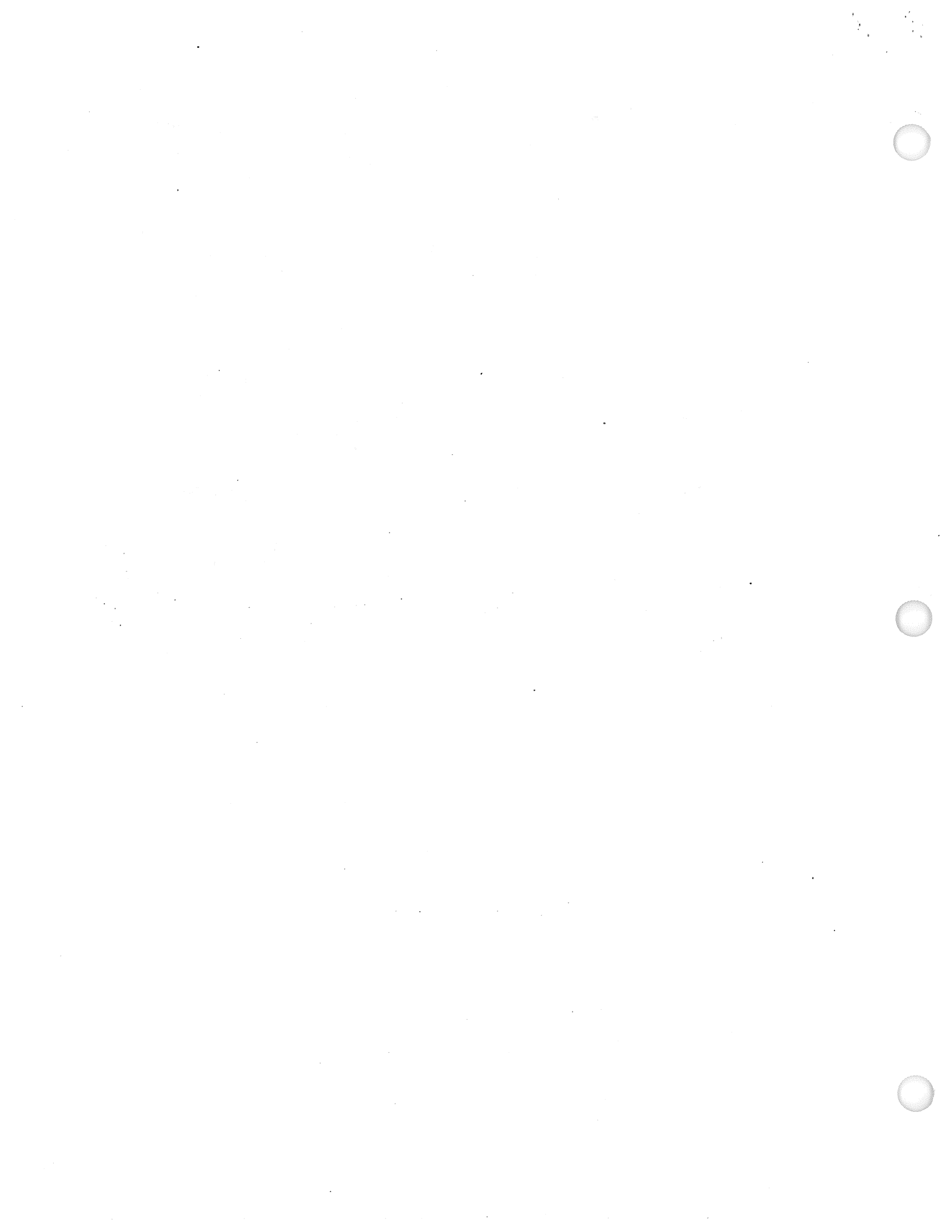
2.7.4.3 Extended Self Test and DEU Self Test. To perform this procedure, a GPC initialization (section 2.7.4.1) and a Menu Load Option (section 2.7.4.2.2) will need to be performed prior to the Extended Self Test procedure. The Self Test procedure is controlled via the GPC IPL MENU (2) display. To call up this display, press the SYS SUMM key, while the GPC IPL MENU (1) display is up. If the MSGS STILL IN LIST area is not 0, press the MSG RST key until it is.

The GPC Self Test is initiated via Item 18. When the item is entered, an asterisk will be driven beside Item 18, the GPC Self Test will be cycled in an infinite loop, the DEU will be polled as required, and the STP CYCLE COUNT area will be incremented with each cycle of the STP. If GPC errors are detected, the ERROR/MSG CODE, ERROR MSG CODE CNT, TOTAL ERROR/MSG CNT, and MSG'S STILL IN LIST areas will be updated. If errors occur, obtain troubleshooting assistance. When it is desired to stop the GPC Self Test, execute Item 19.

The DEU Stand Alone Self Test Program (SASTP) is initiated from the same display via Item 20. When the item is executed, the CRT will display a variety of moving and varying graphics displays. There are some crew controllable capabilities on the display. As each key is pressed on the keyboard, a code identifying the key will appear behind the KBUA or KBUB area, depending on which keyboard adapter is being used to talk to the CRT. Also, the position of the MAJOR FUNCTION switch is displayed behind the MF area and will change with the position of the switch. (It should be noted that the display cannot be resumed back to GPC IPL MENU (2), unless this switch is returned to its original position. If it is not, ERR will be displayed behind the Major Function upon the attempt to resume to the GPC IPL MENU (2) display.) A BITE test may also be performed via an Item 1 EXEC, and an asterisk will appear beside the TEST 1 area.

The DEU SASTP may be terminated via pressing the RESUME key, and the GPC IPL MENU (2) will reappear. To return to the GPC IPL MENU (1) display, press the SYS SUMM key. It should be noted that the DEU SASTP overlays the PASS critical formats in the DEU and that these will automatically be reloaded in the PASS load from the Menu Load Option.

An additional capability has been added to the GPC IPL MENU (1) display in the Version 6 IPL software. It is possible to prevent the loading of IMU calibration data into the BFS during IPL. This is accomplished by executing Item 26 on the GPC IPL MENU (1) display. If this is not done, the software will automatically load the IMU calibration data from the GNC checkpoint on mass memory for a BFS IPL.



SECTION 3

CREW STATIONS PANEL CONTROLS AND DISPLAYS

Each switch will be shown on its crew station accompanied by a functional description and operational limitations as necessary.

3.1 PANEL C2

Refer to figure 3-1 for panel C2.

3.1.1 CRT 1 (CRT 2, CRT 3)

3.1.1.1 POWER (3-Position Toggle Switch).

- ON Allows 28 V dc to designated display electronics unit (DEU) and display unit (DU) power supplies.
- STBY Allows 28 V dc only to high-voltage power supply to warmup cathode ray tube (CRT) filament in designated DEU and DU.
- OFF Inhibits all power inputs to designated DEU and DU.
- NOTE CRT warmup occurs in ON or STBY position. Once warmed up, if no GPC commands are received, a CRT screen will show an X and a POLL FAIL message.

3.1.1.2 MAJ FUNC (3-Position Toggle Switch). Changes which major function software is to process keystrokes and to drive CRT data for the designated DEU/DU.

Operational Limitations

- A. The selected major functions's operational sequence (OPS) display will appear on the designated CRT unless overlaid by a specialist function (SPEC).
- B. Moving the switch from one major function to another, then back to the original major function returns the underlying major mode or SPEC display to the CRT. DISP displays are not retained.
- C. Moving the switch to another major function in primary avionics software system (PASS) causes that major function's major mode display to appear on the CRT unless:
 1. A SPEC was active on the CRT the last time the major function was selected; then the SPEC appears on the CRT if an OPS transition has not occurred.

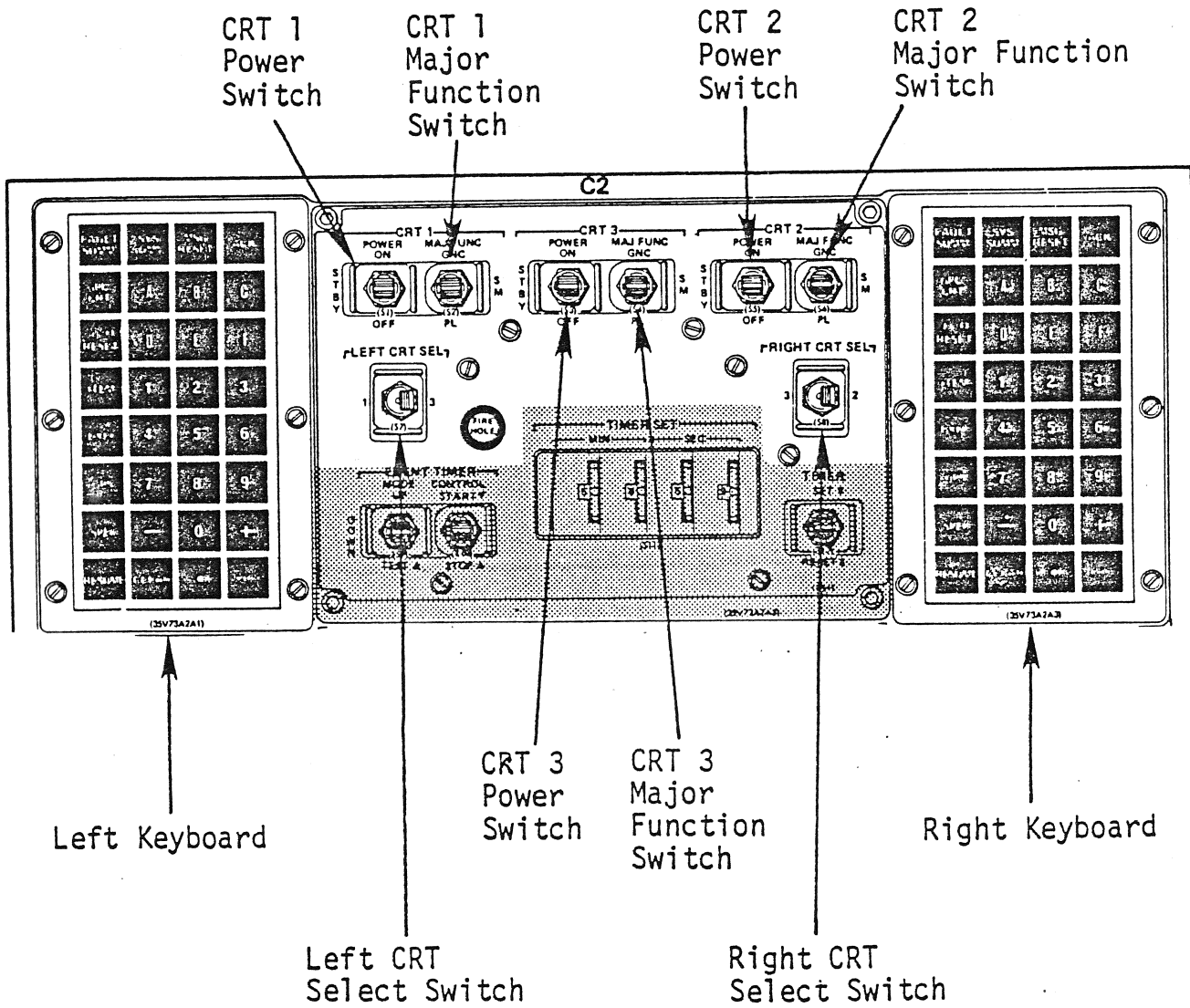


Figure 3-1. Panel C2

2. The new major function isn't active, then the display on the CRT will be the OPS 0 SPEC, GPC MEMORY.

D. Moving a MAJ FUNC switch of a CRT assigned to the backup flight system (BFS) to SM will cause the THERMAL display to appear on the CRT, unless a SPEC was active the last time BFS SM was selected on this CRT.

1. GNC will cause the appropriate guidance, navigation, and control (GNC) major mode display to appear on the CRT unless a SPEC was active the last time the GNC was selected; then the SPEC appears on the CRT if no OPS transition has occurred. If GNC is in OPS 000, the BFS MEMORY display appears.

2. PL will cause the current display to remain on the CRT and go static. If the CRT is assigned to BFS from PASS with the MF switch in PL, a blank display (displaying only GPC driver number and times) is displayed.

3.1.2 LEFT CRT SEL (2-Position Toggle Switch). Directs DEU/DU 1 or DEU/DU 3 to process keystrokes from the left keyboard in the forward station.

3.1.3 RIGHT CRT SEL (2-Position Toggle Switch). Directs DEU/DU 2 or DEU/DU 3 to process keystrokes from the right keyboard in the forward station.

A. Operational Limitation. DEU/DU 3 will process keystrokes from both keyboards if both CRT SEL switches are in position 3. Hence, if the combined keyboard inputs pass DEU syntax checks, an unwanted message or command could be transmitted to GPC's listening to DEU 3 response messages.

3.2 KEYBOARD

Refer to figure 3-2 for keyboard.

- A. FAULT SUMM. A single keystroke input which calls the FAULT display in any OPS. SPEC 99 PRO invokes the FAULT display and clears all messages.
- B. GPC/CRT. The first keystroke of a keyboard message (e.g., GPC/CRT 43 EXEC) which assigns a specific multifunction CRT display system (MCDS) to a particular general purpose computer (GPC). A DEU/CRT may be isolated from the PASS GPC's by entering 0 for the GPC in this input. Isolation of a CRT from the BFS is similarly done via a BFS or PASS keyboard. The BFS responds to CRT reassignment via this keyboard message and the proper configuration of the BFC CRT display and select switches on panel C3. During ascent and entry, the BFS will respond to selected inputs made on a PASS keyboard but the PASS will never respond to inputs made on a BFS keyboard. Thus, all GPC/CRT key assignments should be made to a PASS keyboard.
- C. I/O RESET. The first key of a keyboard message (I/O RESET EXEC) which restores bypassed bus control element (BCE) chains and resets any bus terminal unit (BTU) port masks. PASS responds to inputs from a PASS keyboard while the BFS responds to inputs from a BFS keyboard.
- D. ITEM. The first key of a keyboard message which acts as a software switch (e.g., ITEM 14 EXEC), or allows data to be input for software processing (e.g., ITEM 13 + 1099 EXEC) for supporting SPEC's and OPS.
- E. EXEC. The last key of a keyboard message to:
 - 1. Enter data on SPEC's and OPS displays (e.g., ITEM 13 + 7099 EXEC).
 - 2. Assign a specific CRT to a particular GPC (e.g., GPC/CRT 43 EXEC).
 - 3. Enable or inhibit software processes (e.g., ITEM 14 EXEC).
 - 4. Restore bypassed BCE chains and reset BTU port masks (e.g., I/O RESET EXEC).
- F. OPS. The first key of a keyboard message to initiate a new OPS (e.g., OPS 301 PRO), change major modes (e.g., OPS 302 PRO), or restart the current OPS major mode while changing one GPC set configuration (only in GNC OPS major modes 201, 301, 801, and 901, and SM OPS major modes 201 and 202). The latter technique is referred to as OPS mode recall. An OPS mode recall in a major mode other than those listed above is called re-stringing and only causes software to assign data buses according to the data bus assignment portion of the memory configuration table on GPC MEMORY. OPS 0 PRO cancels any systems management (SM) and payload (PL) OPS when SM and PL, respectively, are selected via the major function switch, but cancels only GNC OPS 2 and 9 when those GNC OPS are active.
- G. SPEC. The first key of a keyboard message to invoke SPEC's or DISP's (e.g., SPEC 50 PRO). PASS software can support a maximum of three CRT's

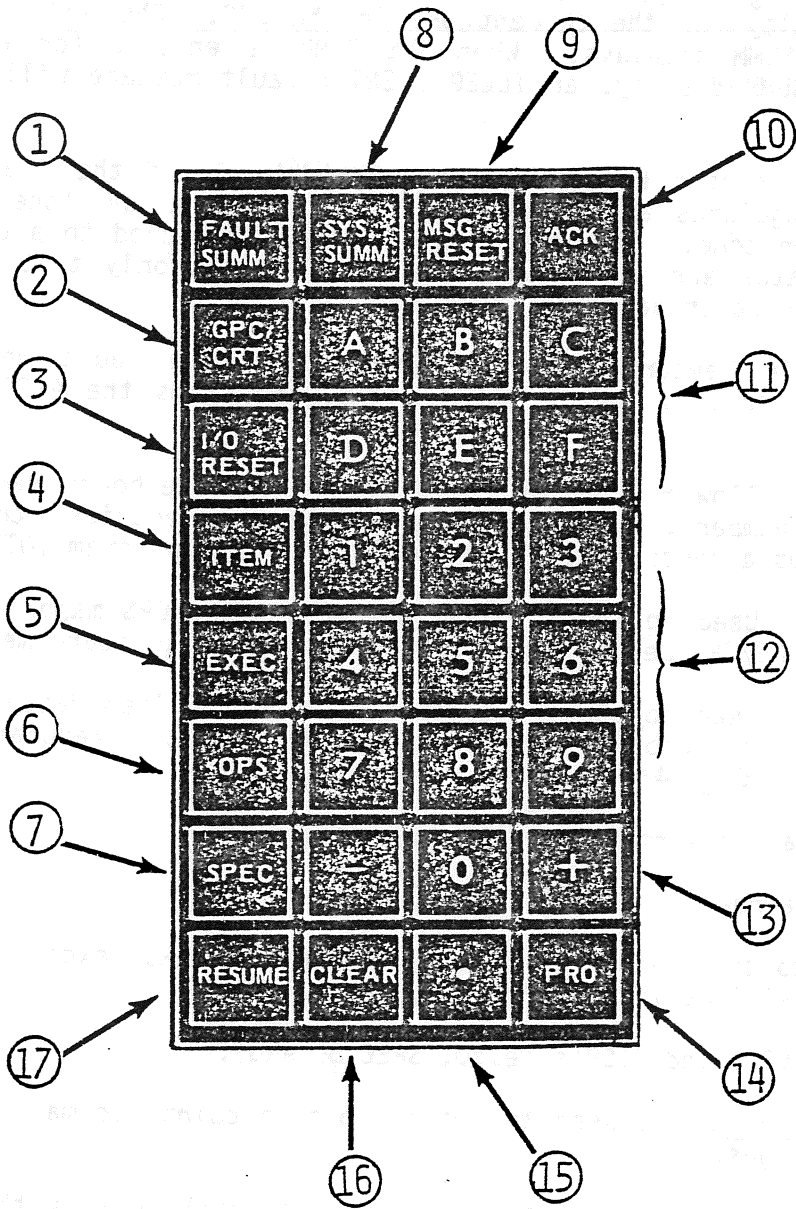


Figure 3-2. Keyboard

with two SPEC's, and/or three displays (DISP's). A SPEC may overlay an OPS while a DISP may overlay a SPEC or OPS. The same SPEC may be driven on two CRT's for the same major function (using the maximum of two SPEC's for the major function). Systems software SPEC's count against the major function in which they were called.

- H. SYS SUMM. A single keystroke input which invokes the system summary (SYS SUMM) CRT display for the current OPS in the GPC. GNC and PL OPS 9 do not have SYS SUMM displays. When SYS SUMM is entered for an OPS not having a SYS SUMM display, an ILLEGAL ENTRY fault message will be generated.
- I. MSG RESET. A single keystroke message which clears the fault message line and extinguishes any software driven C/W light and tone or the SM ALERT light and tone. If entered on a keyboard attached to a CRT showing class 5 (operator error) message, MSG RESET clears only that CRT's message line, no scratch pad line (SPL) echo.
- J. ACK. A single keystroke message which stops the fault message from flashing, extinguishes the SM ALERT light, and stops the ALERT tone (no SPL echo).
- K. Letters A-F. Allow hexadecimal data entries for keyboard sequences involving item numbers. When used as single item entries, the keyboard invokes various aspects of the DEU operational test program (OTP).
- L. Digits 0 - 9. Used to specify item numbers, data, OPS major modes, SPEC numbers, and GPC/CRT designation for the associated keyboard messages.
- M. Signs (+, -). Used to specify algebraic value for item data entries and to separate item numbers from data entries on item keyboard messages (e.g., ITEM 1 \pm 6 \pm 14 \pm 12 EXEC).
- N. PRO. The final keystroke in keyboard messages to:
 1. Initiate a new OPS (e.g., OPS 301 PRO).
 2. Proceed to the next major mode (e.g., OPS 302 PRO) except for certain mode transitions in GNC OPS 6, 3, and 1.
 3. Invoke SPEC's and DISP's (e.g., SPEC 50 PRO).
- O. Decimal Point (.). Is used to enter floating point decimal data in item keyboard messages.
- P. CLEAR. A single keystroke message which generally blanks the last keystroke or ERR and the erroneous keystroke. If the last keystroke is a PRO or EXEC, entering CLEAR will blank the entire SPL (no SPL echo).
- Q. RESUME. A single keystroke used to terminate the current CRT overlay and to return the underlying SPEC or OPS display.

3.3 FORWARD STATION ROTATIONAL HAND CONTROLLERS (RHC)

Refer to figure 3-3 for the RHC's.

3.3.1 BFS Engage Pushbutton. The BFS engage pushbutton engages the BFS and disengages the PASS if the BFS GPC's output switch (panel O6) is in BACKUP. If no GPC output switch is in BACKUP, PASS remains in control of the vehicle. If a GPC output switch is in BACKUP but is not powered, active GPC contains BFS software, the PASS GPC's with OUTPUT = NORMAL will give up vehicle control, but the PASS GPC with OUTPUT = BACKUP remains in operation. However, this GPC may not be such that vehicle control exists (e.g. an SM GPC).

3.3.2 Operational Limitation. Loss of any one BFS ENGAGE discrete line from an RHC inhibits BFS from being engaged via that RHC.

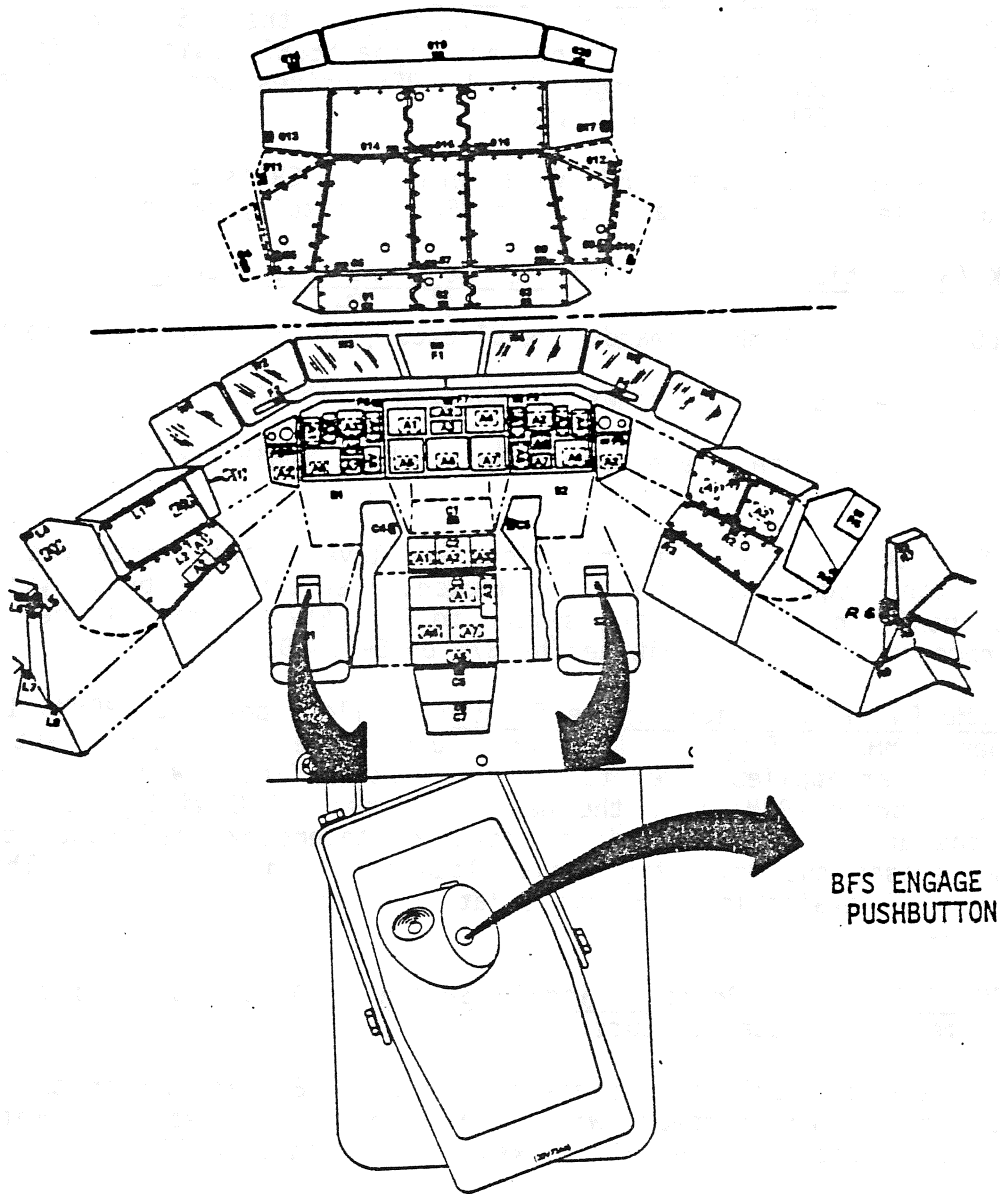


Figure 3-3. Rotational Hand Controllers

3.4 PANEL C3

Refer to figure 3-4 for panel C3.

3.4.1 BFC CRT DISPLAY (2-Position Toggle Switch)

- ON Provides power to the SELECT switch.
- OFF BFS CRT selection can be accomplished with GPC/CRT key when the display switch is OFF.

3.4.2 BFC CRT SELECT (3-Position Toggle Switch). Allows onboard control of which CRT's are to be driven by the BFS. Preengaged, the BFS drives CRT 2 in the fwd station indicated by the first number in the SELECT switch position (CRT 2 in figure 3-4). After BFS is engaged, the BFS drives both forward station CRT's indicated by the SELECT switch position.

NOTE: If the BFS is engaged, the BFS will default to CRT's 1 and 2 if the BFC CRT display and select switches fail, or the BFC CRT display switch is OFF.

3.4.3 UPLINK (3-Position Toggle Switch: 2 Positions Lever-Locked)

- NSP BLOCK. All uplink commands are blocked (not processed) by the NSP.
- GPC BLOCK. All uplink commands are blocked by the GPC.
- ENABLE. All commands are processed (unless inhibited by S/W on SPEC 001).

NOTE: The NSP BLOCK and GPC BLOCK positions are lever-locked (note the "0") to prevent inadvertant toggling. Once lever-locked, a switch must be pulled out to change switch positions. Moving the switch to ENABLE automatically reinitiates GPC uplink processing (unless inhibited by S/W on SPEC 001).

3.4.4 OI PCMMU PWR (3-Position Toggle Switch). Allows power to PCMMU 1, PCMMU 2, or neither PCMMU. Toggling from one pulse code modulation master unit (PCMMU) to the other applies power to the designated PCMMU power supplies. The random access memories (RAM's) in the newly selected PCMMU will have to be re-loaded with the appropriate operational downlink telemetry load since powering off the PCMMU erases the telemetry format load (TFL) in the RAM's. The fixed HDR format is still available to retrieve data from toggle buffers 1 and 5 only. (GNC and BFS downlist).

3.4.5 OI PCMMU FORMAT (3-Position Toggle Switch). Allows onboard control of the PCMMU telemetry formatter outputs.

- A. GPC. The PCMMU logic can update either the 128 kb/s RAM or the 64 kb/s RAM and select which memory will be read by the 128 kb/s telemetry formatter as directed by the GPC via keyboard inputs or uplink.
- B. FIXED. The 128 kb/s telemetry formatter reads the fixed 128 kb/s PROM format while the 64 kb/s telemetry formatter reads the 64 kb/s RAM Format. The PCMMU logic can update either the 128 kb/s RAM or the 64 kb/s RAM.

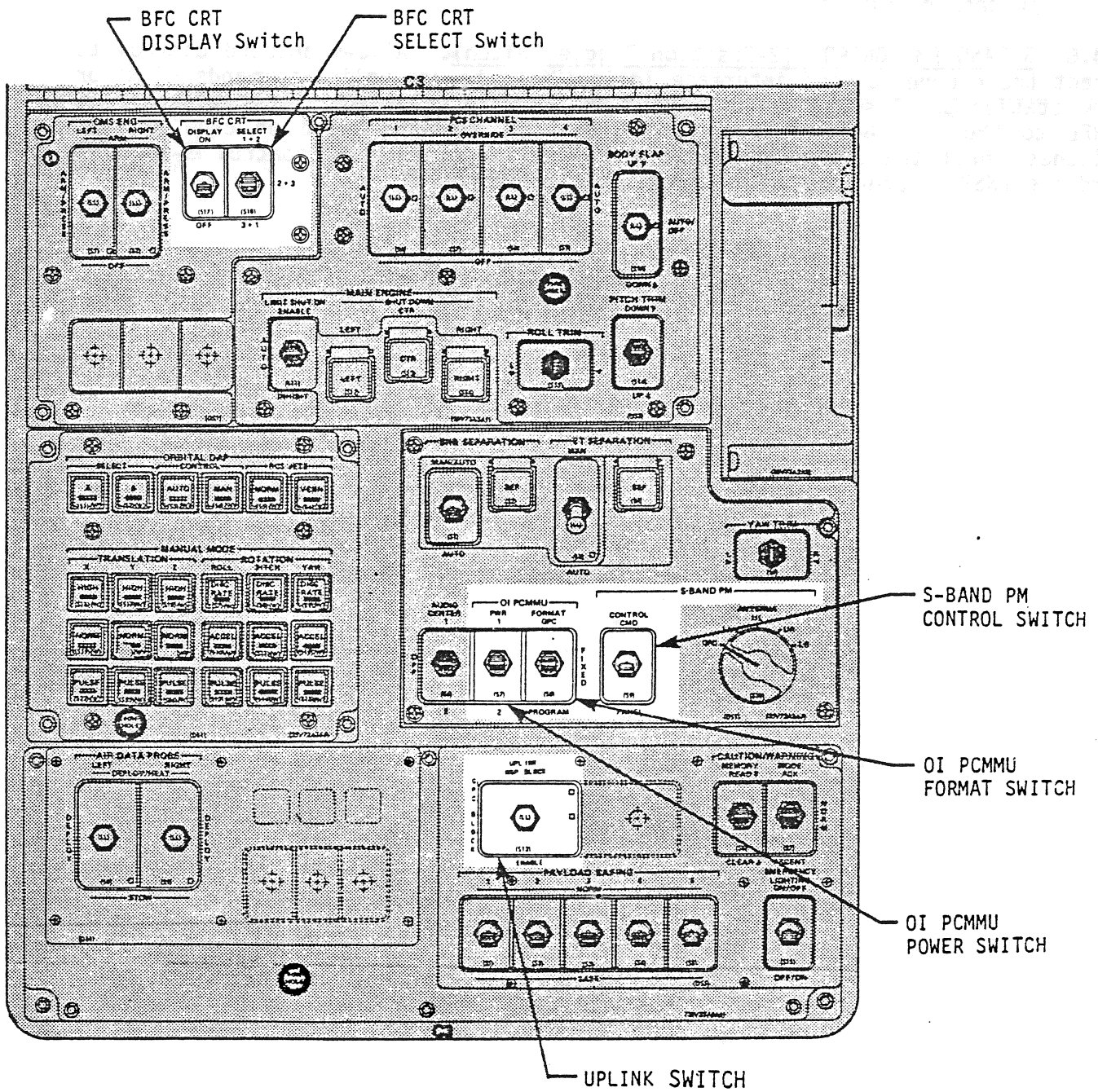


Figure 3-4. Panel C3

C. PROGRAM. Both PCMMU telemetry formatters (64 and 128) read the programmable TFL RAM formats to build the telemetry output to the network signal processors (NSP's).

3.4.6 S-BAND PM CONTROL (2-Position Toggle Switch). Allows onboard control to direct the ground command interface logic (GCIL) to use uplink commands (CDM) or crew station panel switches for S-Band PM hardware selection. When placed from PANEL to CMD, the GCIL will control S-Band PM hardware based on crew station switches until the GPC processes a valid uplink command to control S-Band PM hardware (NSP's, pre-amps, power-amps, and transponders).

3.5 PANELS F2, F4, and M052J.

Refer to figure 3-5 for these panels.

3.5.1 MASTER ALARM (Black Letters on Red Background). Illuminated by the caution and warning (C&W) electronics upon detection of a class 2 problem. Data processing subsystem (DPS) class 2 problems involve GPC fail-to-sync and fail-to-halt cases. Extinguished only by depression of any MASTER ALARM pushbutton indicator. Accompanied by a MASTER ALARM tone.

3.5.2 BFC (Yellow Letters on Black Background). Illuminated by the BFS GPC when BFS is engaged or flashing when the BFS is in the disengaged stand-alone mode.

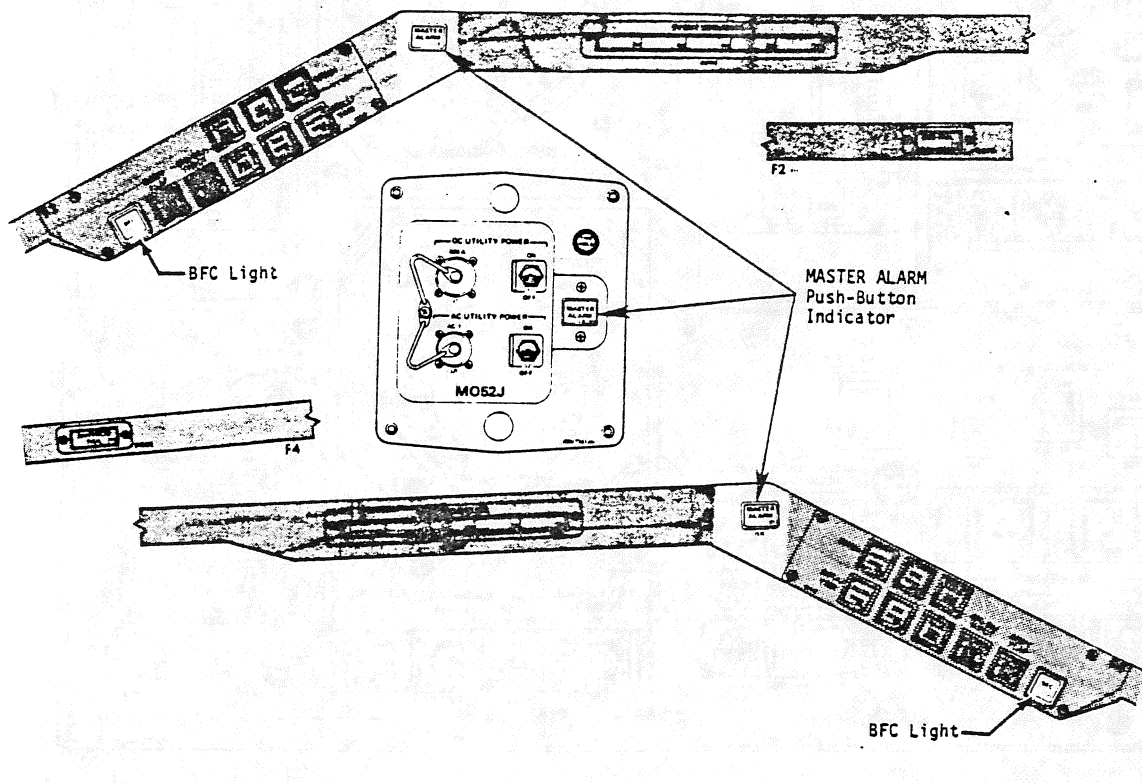


Figure 3-5. Panels F2, F4, and M052J

3.6 PANEL F6

Refer to figure 3-6 for panel F6.

3.6.1 BFC DISENGAGE (2-Position, Momentary, Guarded Toggle). Sets three discrete inputs to all five backup flight controller (BFC) modules to disengage the BFS.

NOTE: The PASS will not assume control of the vehicle without an overt action onboard to prepare the PASS for vehicle control (e.g., reinitialize and/or reformation of PASS redundant set).

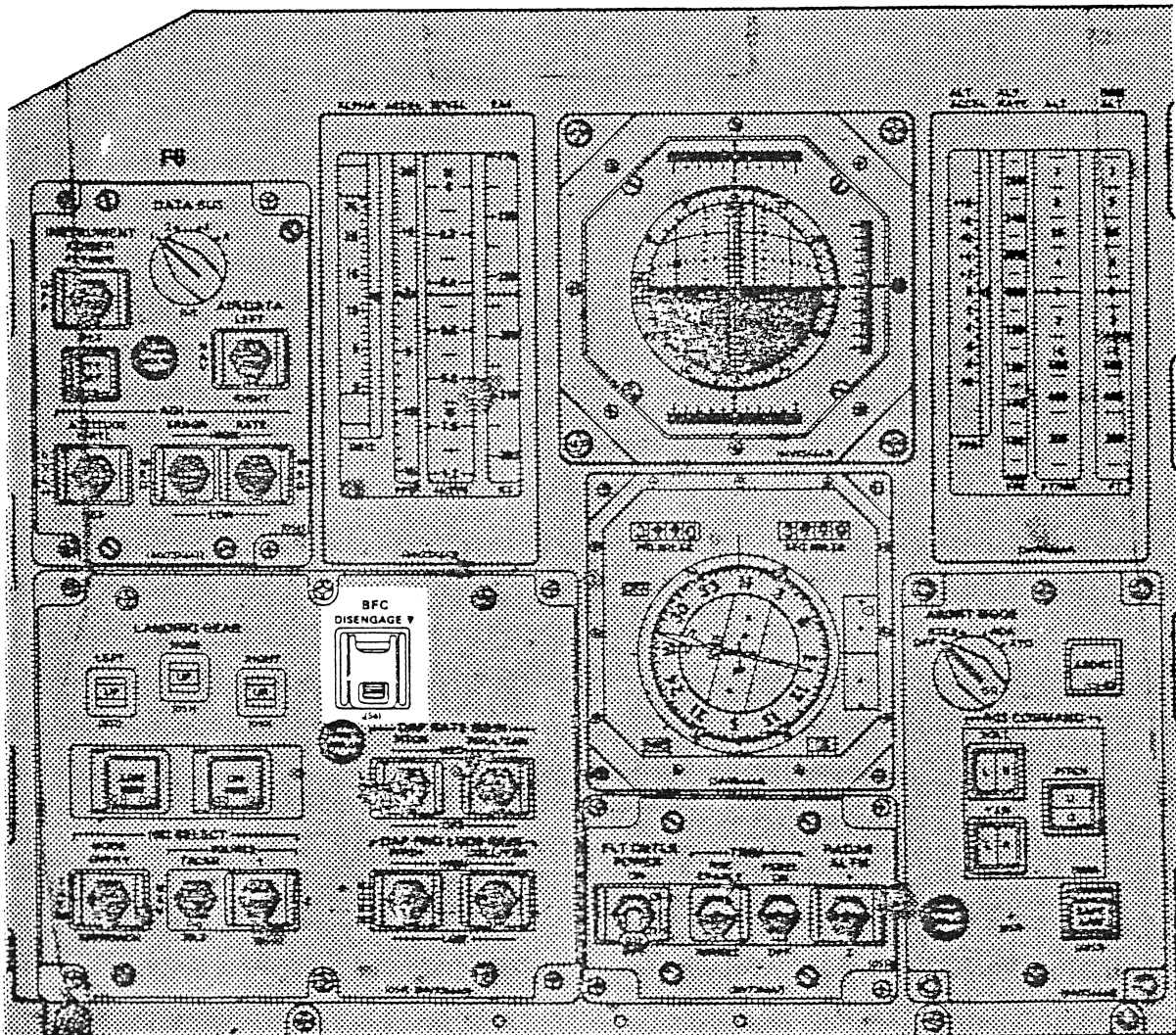


Figure 3-6. Panel F6

3.7 PANEL F7

Refer to figure 3-7 for panel F7.

3.7.1 CRT 1 (CRT 2, CRT 3). (5" x 7" phosphorus screen activated by magnetically positioned electron beam). Presents alphanumeric characters and graphics as directed by a GPC via a DEU.

3.7.1.1 BRT (Potentiometer). Allows onboard control of associated total CRT screen brightness from blackout to full brightness.

3.7.1.2 DEU, DU (2-Position Talkback). Indicates illustrated NO-GO state when the BITE detects that a problem has existed for at least 6 seconds in the associated device. To return the flag to black (no problem detected), the flag must be manually twisted in a counterclockwise direction and returned. If the problem still exists, the flag will return to illustrated NO-GO state. Accompanied by CRT BITE class 3 fault message and associated annunciations if critical built-in test equipment (BITE) problem. The talkbacks are not continuously monitored inflight.

3.7.2 SM ALERT (Black Letters on Blue Background). Illuminates when a class 3 alert problem is detected by software. DPS class 3 problems include input/output (I/O) error, BCE chain bypass, GPC configuration, BITE, and time-keeping cases. Accompanied by alert tone, and fault message. LIGHT & TONE extinguished by depression of ACK or MSG RESET keys. Tone independently terminated by software in 3 seconds.

3.7.3 GPC (Red Letters on Black Background). Illuminated by C&W when any GPC issues its SELF-FAIL discrete output based on voter hardware, synchronization software logic. Normally accompanied by GPC STATUS matrix yellow diagonal light, MASTER ALARM lights and tone, panel R12 CAUTION/WARNING STATUS matrix light (when status requested), BACK-UP C/W ALARM light on panel F7 C&W matrix, and fault message. Extinguished by correction of problem or by powering-off faulty GPC.

3.7.4 BACKUP C/W ALARM (Red Letters on Black Background). Illuminated by C&W via DPS MDM's when a class 2 C&W problem is detected by software. DPS class 2 problems are manifested as GPC fail-to-sync and fail-to-halt cases.

Normally accompanied by GPC STATUS matrix light, MASTER ALARM lights and tone, and fault message. Extinguished by MSG RESET key depression.

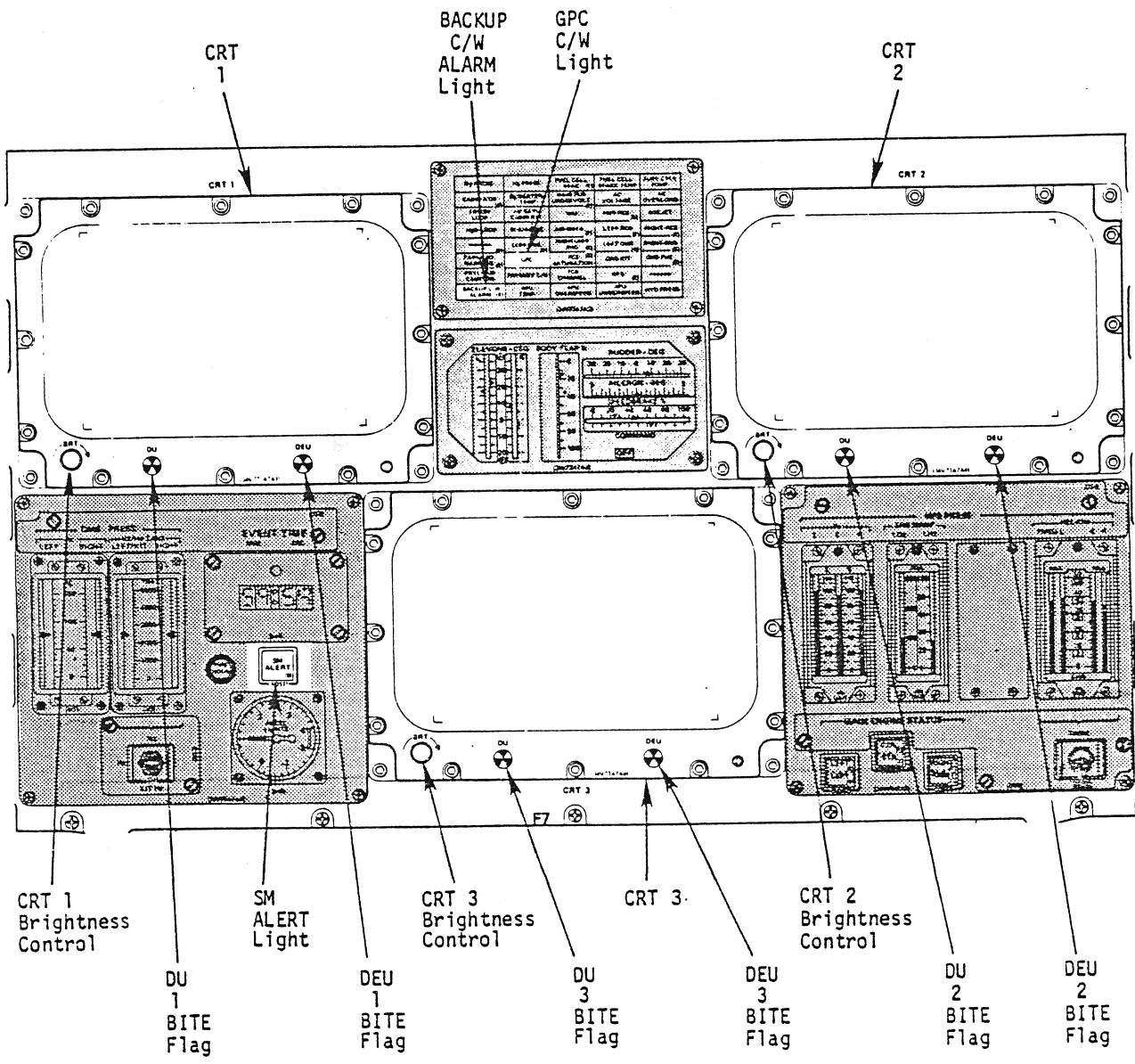


Figure 3-7. Panel F7

3.8 PANEL L4

Refer to figure 3-8 for panel L4.

3.8.1 INST R (cb). Permits power to the panel 08 potentiometer for instrumentation intensity control in the right forward station (e.g., right keyboard) instrumentation lamps.

3.8.2 INST L/CTR (cb). Permits power to the panel 06 potentiometer for instrumentation intensity control in the left and center forward stations (e.g., left keyboard) instrumentation lamps.

3.8.3 PANEL MS. Permits power to the panel R10 potentiometer for intensity control in the mission specialist (MS) station (e.g., keyboard) panel lamps.

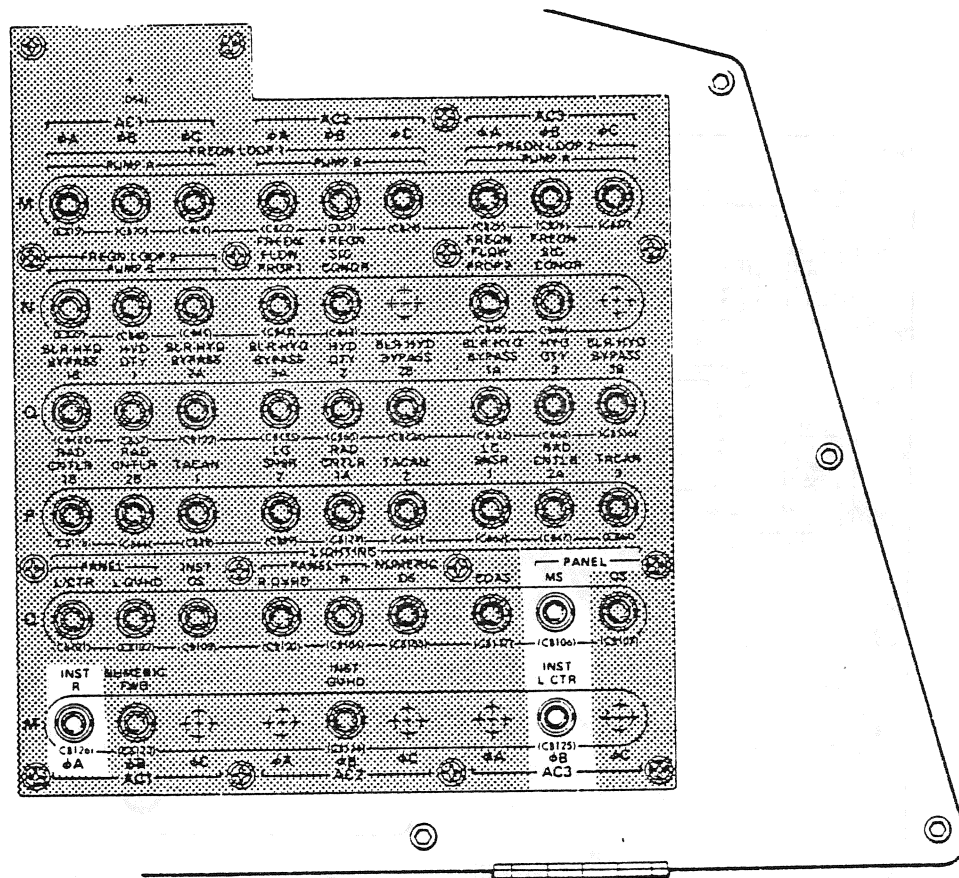


Figure 3-8. Panel L4

3.9 PANEL M042F

Refer to figure 3-9 for this panel.

3.9.1 GPC MEMORY DUMP (6 Position Rotary Switch). Identifies a GPC to be selected for a special hardware initiated stand-alone memory (HISAM) dump capability. The selected GPC's output switch (panel O6) must be in TERMINATE, and the mode switch must be in HALT. If a PASS GPC is selected for a HISAM dump, that GPC's memory contents will replace the downlist of the GNC GPC after the crewmember changes the DOWNLIST GPC. When the mode switch is moved to STBY, the GPC begins sending a 128 half-word frame downlist to the PCMMU's toggle buffer 1. If the PCMMU 128 kb/s fixed format or a TFL which reads toggle buffer 1 is used, the contents of the selected GPC's memory will be included in the operational telemetry downlink until the selected GPC's mode switch is moved to HALT or power is turned off. A dump of a PASS GPC main memory using this method will require about 1½ minutes to complete while a dump of a BFS GPC will require about 6 minutes to complete.

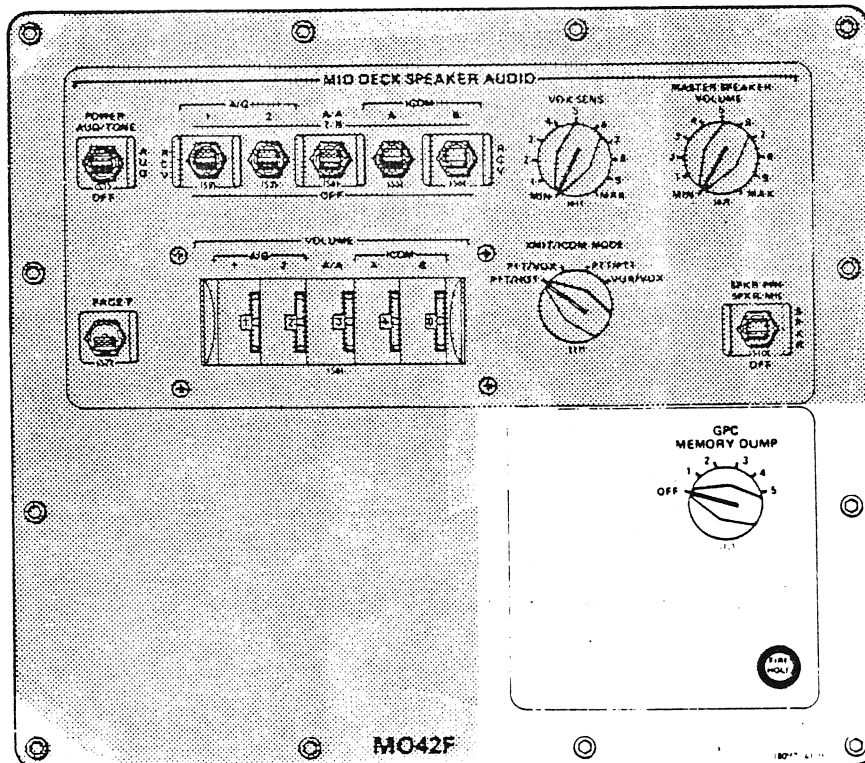


Figure 3-9. Panel M042F

3.10 PANEL 01, GPC STATUS MATRIX

5 x 5 light matrix with yellow lights on the main diagonal and white lights elsewhere (refer to figure 3-10).

A yellow, main diagonal light indicates a GPC has voted itself failed. A white light indicates a GPC has voted another GPC as failed. Normally, during ascent and entry phases, a failed PASS GPC will be indicated with its GPC STATUS matrix column, the GPC and BACKUP C/W ALARM lights (panel F7), the MASTER ALARM lights (panels F2, F4 and A7) and GPC fault messages on PASS driven CRT's. If the BFS GPC fails during ascent or entry, only its GPC STATUS yellow diagonal light, the GPC C&W light, and the MASTER ALARM lights will illuminate. During on-orbit operations, failure of one of the two GNC GPC's or the SM GPC may be indicated with the yellow GPC STATUS diagonal light, the GPC and BACKUP C/W ALARM lights, the MASTER ALARM lights, and/or GPC fault messages. In each instance, the C&W alarm will also occur. Different situations may involve different combinations of the annunciations mentioned above with other annunciations not mentioned (e.g., fault messages).

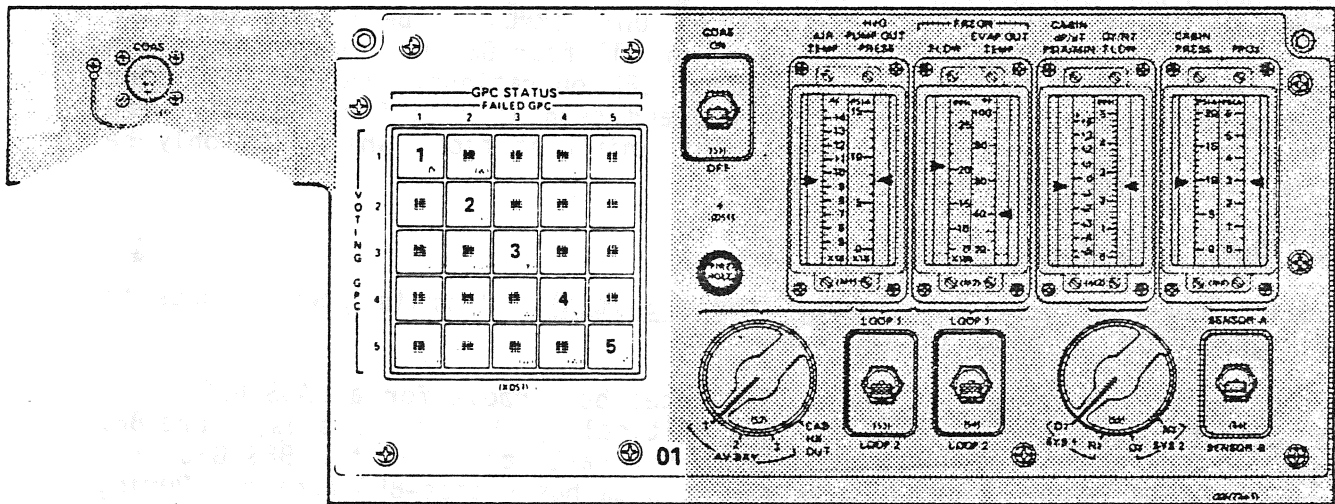


Figure 3-10. Panel 01, GPC STATUS Matrix

3.11 PANEL 06

Refer to figure 3-11 for panel 06.

3.11.1 LEFT/CTR INSTRUMENT (Potentiometer). Permits variable input to control brightness of left/center instrumentation lamps in the forward station; e.g., left keyboard lamps.

3.11.2 ANNUNCIATOR LAMP TEST (3-Position Momentary Toggle Switch). Permits power to the forward station annunciator lamps (including the panel 01 GPC STATUS matrix when in the LEFT position) for bulb test.

3.11.3 ANNUNCIATOR INTENSITY (2-Position Toggle Switch and Potentiometer). Permits onboard intensity control of annunciator lamps (including panel 01 GPC STATUS matrix). When the INTENSITY toggle switch is in BRIGHT, the forward station annunciator lamps are driven to full brightness. When the INTENSITY toggle switch is in VAR, the LOW-MED potentiometer controls the variable annunciator lamp intensity level from low to medium.

3.11.4 MDM PL1, (PL2, PL3, FF1-4, FA1-4) (2-Position Toggle Switch). Permits power inputs to the designated multiplexer/demultiplexer (MDM) (typical of all 10 DPS MDM's). The PL3 MDM power switch is not wired.

3.11.5 DEU Load (2-Position, Momentary Toggle Switch). Requests the initial program load (IPL) software in a mass memory unit (MMU) to be stored in a GPC for transfer to the designated DEU (typical of all four DEU's). When the switch is momentarily placed in LOAD during nominal DEU operations, the GPC will stop responding to keyboard inputs from that DEU and sending data for the CRT. The DEU/DU will be lost for nominal usage until initialization (which can only be performed via a GPC just after GPC IPL).

3.11.6 General Purpose Computer

3.11.6.1 POWER (2-Position, Guarded Toggle Switch). Permits power inputs to the designated GPC (typical of all 5 GPC's).

3.11.6.2 OUTPUT (2-State Talkback). Indicates barberpole for a PASS GPC if it stops output over its assigned flight critical (FC) data bus(es) (pre-BFS engage) or when the BFS is engaged. Indicates barberpole for the BFS GPC pre-BFS engage or if it stops output over the FC data buses post-BFS engage. During nominal operation of a GPC a loss of power, critical failure halting software, output switch = TERMINATE or mode switch = HALT will cause a GPC's OUTPUT talkback to go barberpole. Nominal state is gray.

3.11.6.3 OUTPUT (3-Position, Guarded Switch). Terminates FC output for the indicated GPC and allows onboard acknowledgement of BFS GPC for coordination of PASS to BFS handover of vehicle control (engage). Selection of BFS GPC occurs during GPC IPL/activation and not with this switch. If all five GPC OUTPUT switches (often called the BACKUP/NORMAL/TERMINATE switch) are in either NORMAL or TERMINATE, the PASS GPC's will retain control of the vehicle if BFS ENGAGE is requested via an RHC pushbutton. If more than one GPC's OUTPUT switch is in BACKUP, the higher numbered GPC's OUTPUT switch will be acknowledged to be in BACKUP; all others will default to NORMAL.

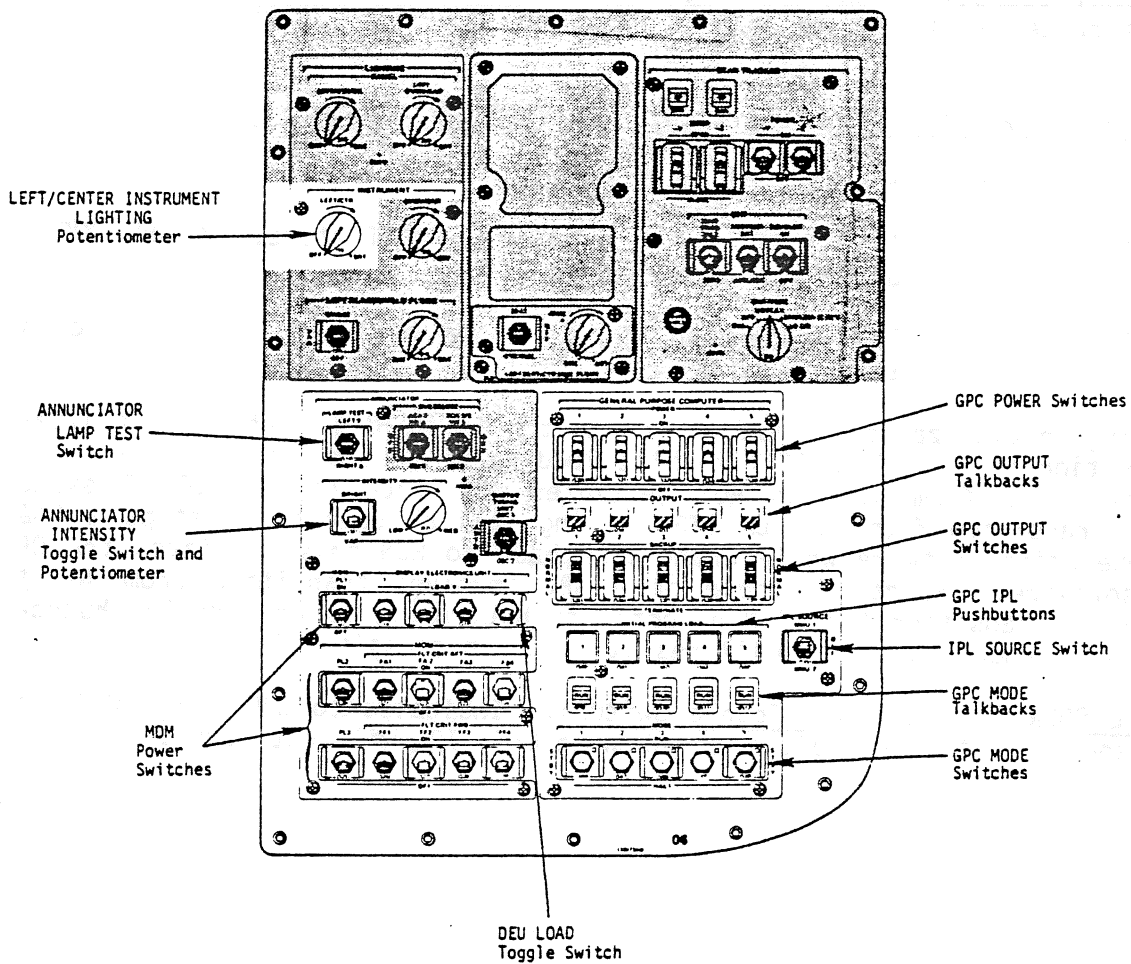


Figure 3-11. Panel 06

3.11.6.4 IPL (Pushbutton). Initiates IPL for the indicated GPC if power is on, MODE = HALT, an MMU is selected, and the selected MMU is ready. Depression of the IPL pushbutton during nominal GPC operations will not be recognized. Only one GPC at a time is initialized since command of the MM 1 and 2 data buses is required.

3.11.6.5 MODE (3-State Talkback). Indicates status of software processing for designated GPC. During the IPL sequence, IPL will be driven on the talkback. During nominal operations RUN will be driven unless power is off, a critical failure has halted software, or MODE = HALT, in which case barberpole will be displayed.

3.11.6.6 MODE (3-Position Toggle Switch: One Position Lever-locked).

- RUN The designated GPC is under software control.
- STBY A PASS GPC is in a software WAIT state. A BFS GPC is under software control.
- HALT The designated GPC is under hardware control, processing no software.

NOTE: During initialization, a GPC's mode switch is in HALT. After initialization, transition from HALT to STBY enables loading of system software while subsequent transition from STBY to RUN initiates execution of the OPS 0 system software. Transition from RUN to STBY during nominal operations stops a PASS GPC from executing software while transition back to RUN only initiates the OPS 0 system software. Normal shutdown of a GPC involves transition from RUN to STBY to HALT. Transition from RUN directly to HALT prevents an orderly shutdown of the GPC to a known state and will result in the necessity of an IPL.

3.11.7 IPL SOURCE (3-Position Toggle Switch). Indicates to GPC's which MMU is to be the source of the IPL software. When in OFF, IPL will not occur.

3.12 PANEL 08

Refer to figure 3-12 for panel 08.

3.12.1 RIGHT INSTRUMENT (Potentiometer). Permits variable input to control brightness of right forward station instrumentation lamps; e.g., right keyboard lamps.

3.12.2 ANNUNCIATOR LAMP TEST (3-Position Toggle). Permits power to the forward station annunciator lamps (including the panel 01 GPC STATUS matrix when in the LEFT position) for bulb test.

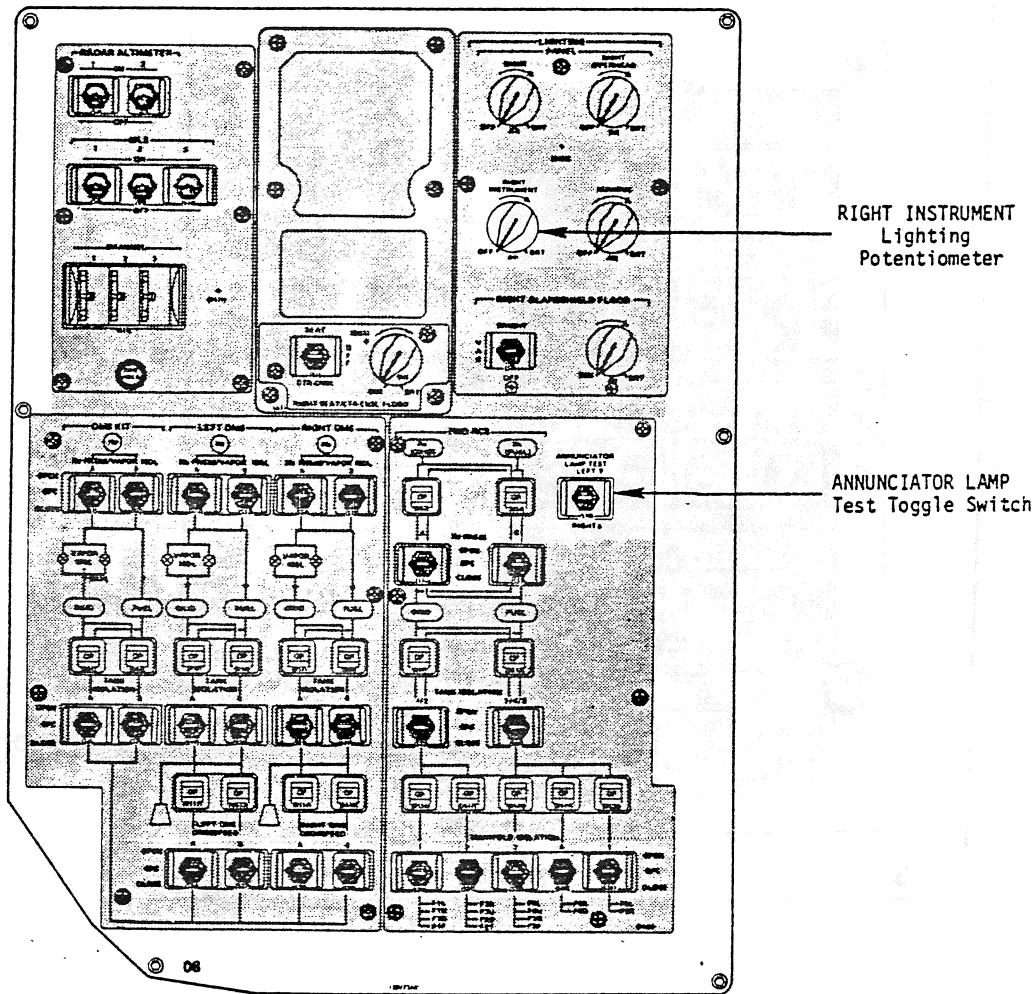


Figure 3-12. Panel 08

3.13 PANEL 013

3.13.1 GPC STATUS (cb). Permits essential bus power to the logic and onboard controls which drive the GPC STATUS matrix annunciators (refer to figure 3-13).

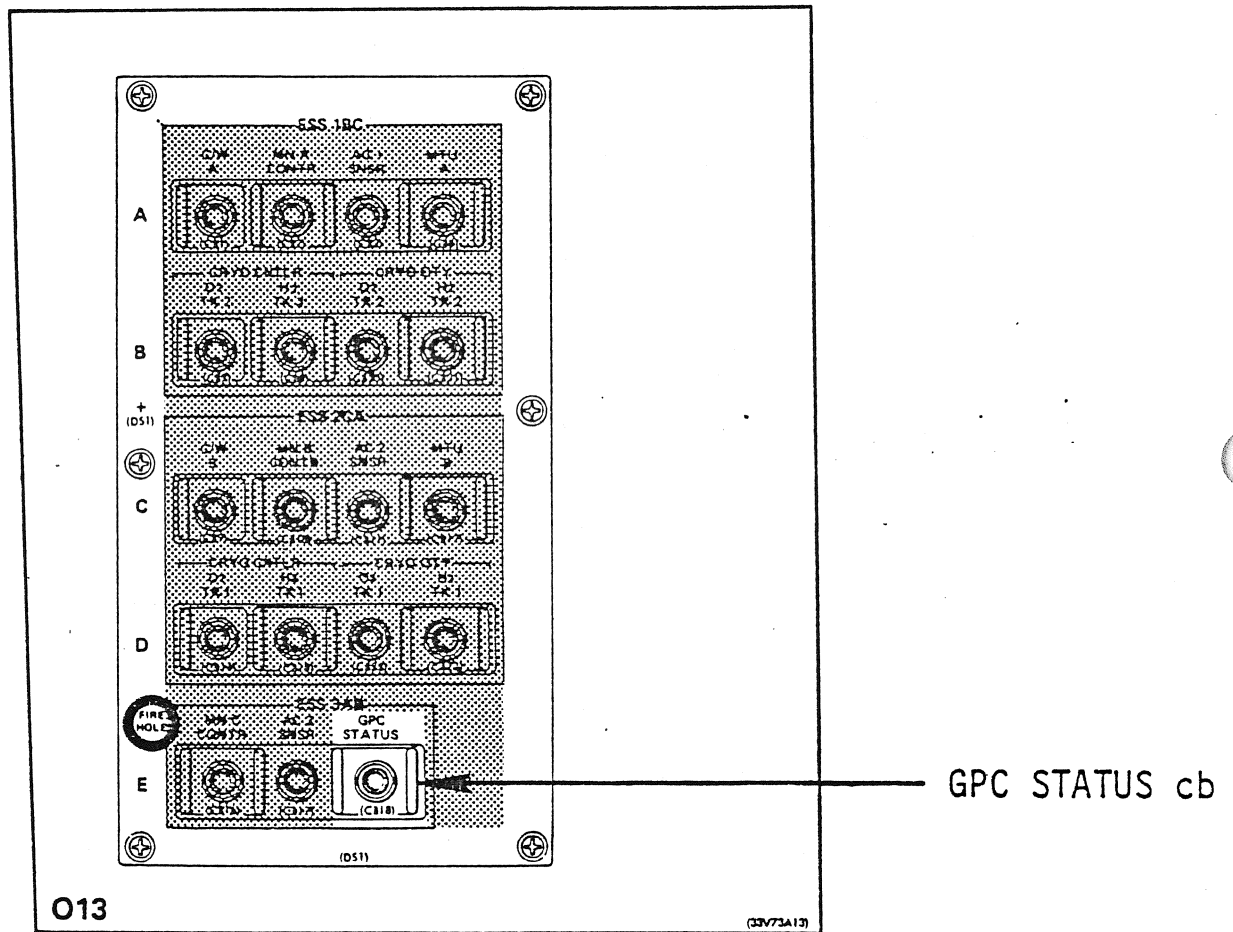


Figure 3-13. Panel 013

3.14 PANEL 014

3.14.1 MMU 1. Permits 28 V dc to MMU 1 power supply (2-position toggle switch, refer to figure 3-14).

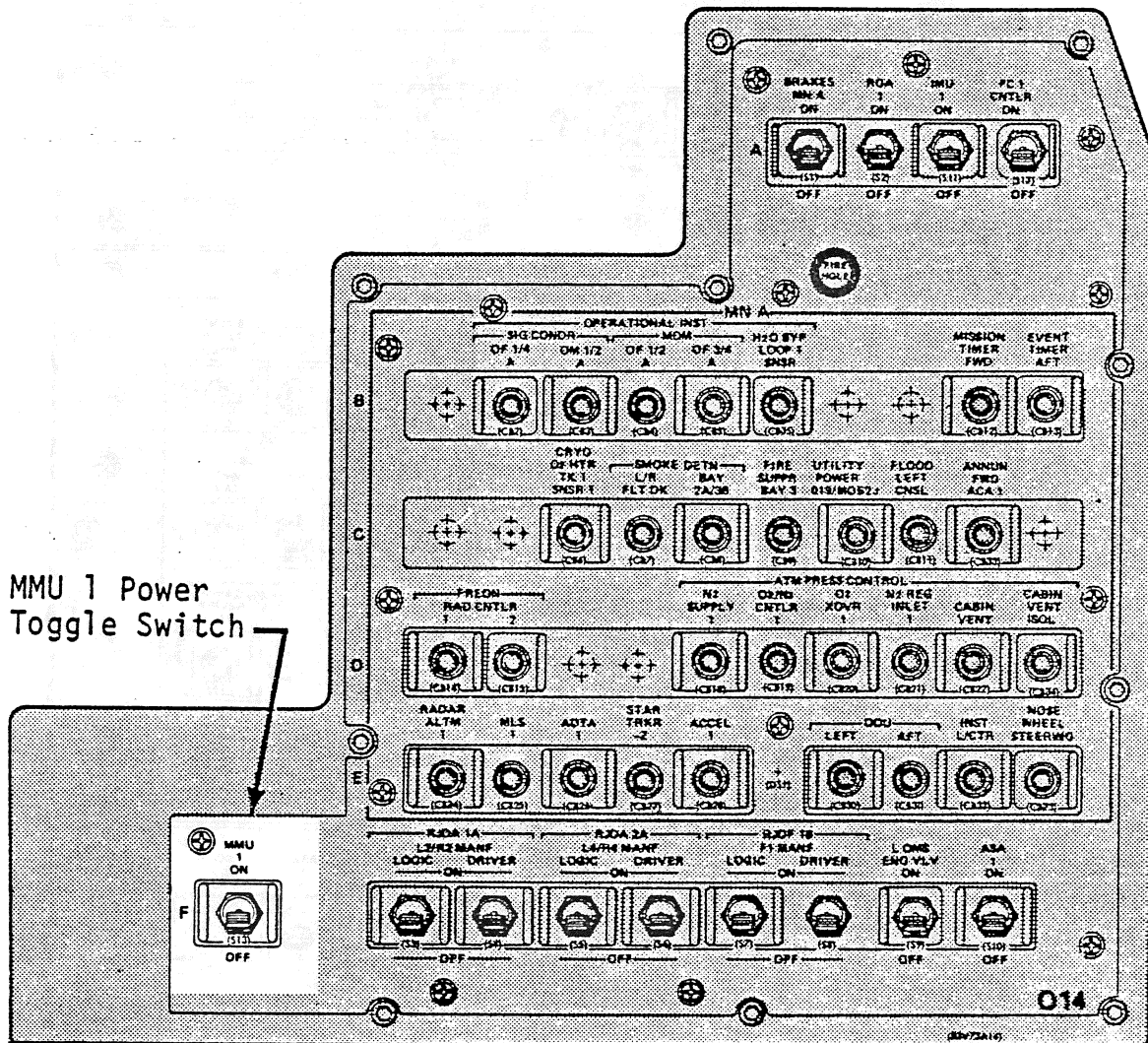


Figure 3-14. Panel 014

3.15 PANEL 015

3.15.1 MMU 2. Permits 28 V dc to MMU 2 power supply (2-position toggle switch, refer to figure 3-15).

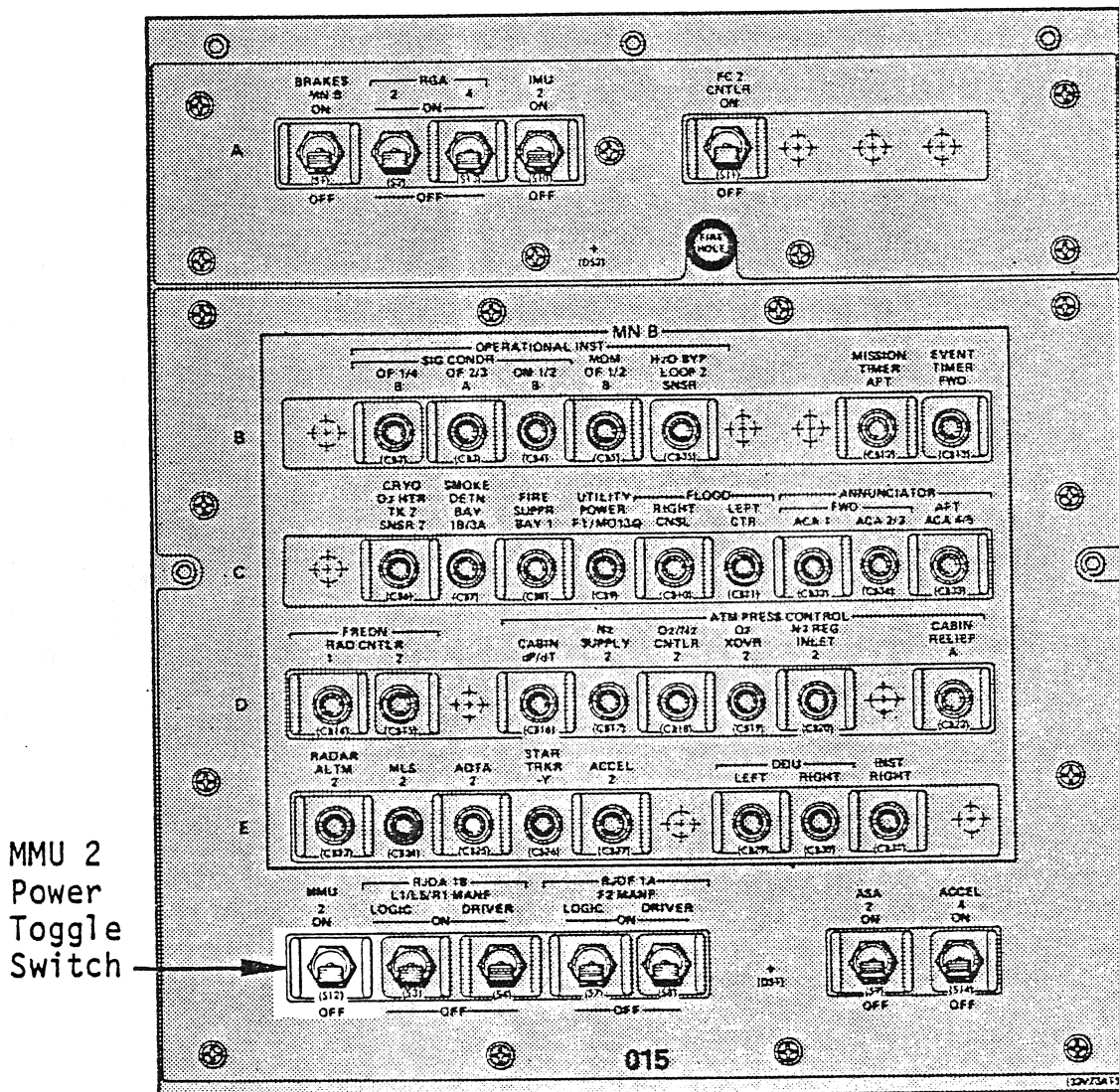


Figure 3-15. Panel 015

3.16 PANEL R10

3.16.1 MS LIGHTING PANEL (Potentiometer). Permits variable input to control brightness of MS panel lamps; e.g., MS keyboard lamps. Refer to figure 3-16 for panel R10.

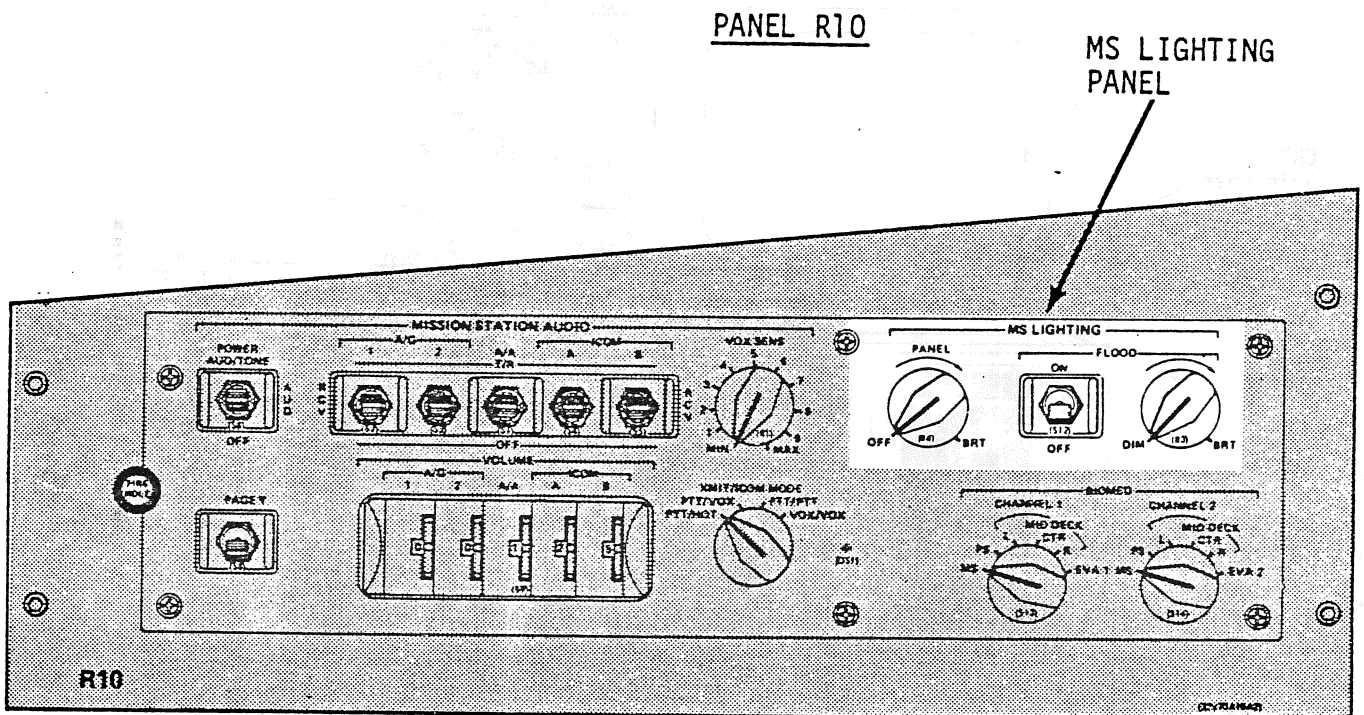


Figure 3-16. Panel R10

3.17 PANEL R12

The controls on panel R12 (see figure 3-17) provide the same function for DEU/DU/CRT 4 as similar controls on panels C2 and F7 provide for DEU/DU/CRT's 1, 2, and 3. The MS keyboard functions are the same as those defined for the panel C2 keyboards.

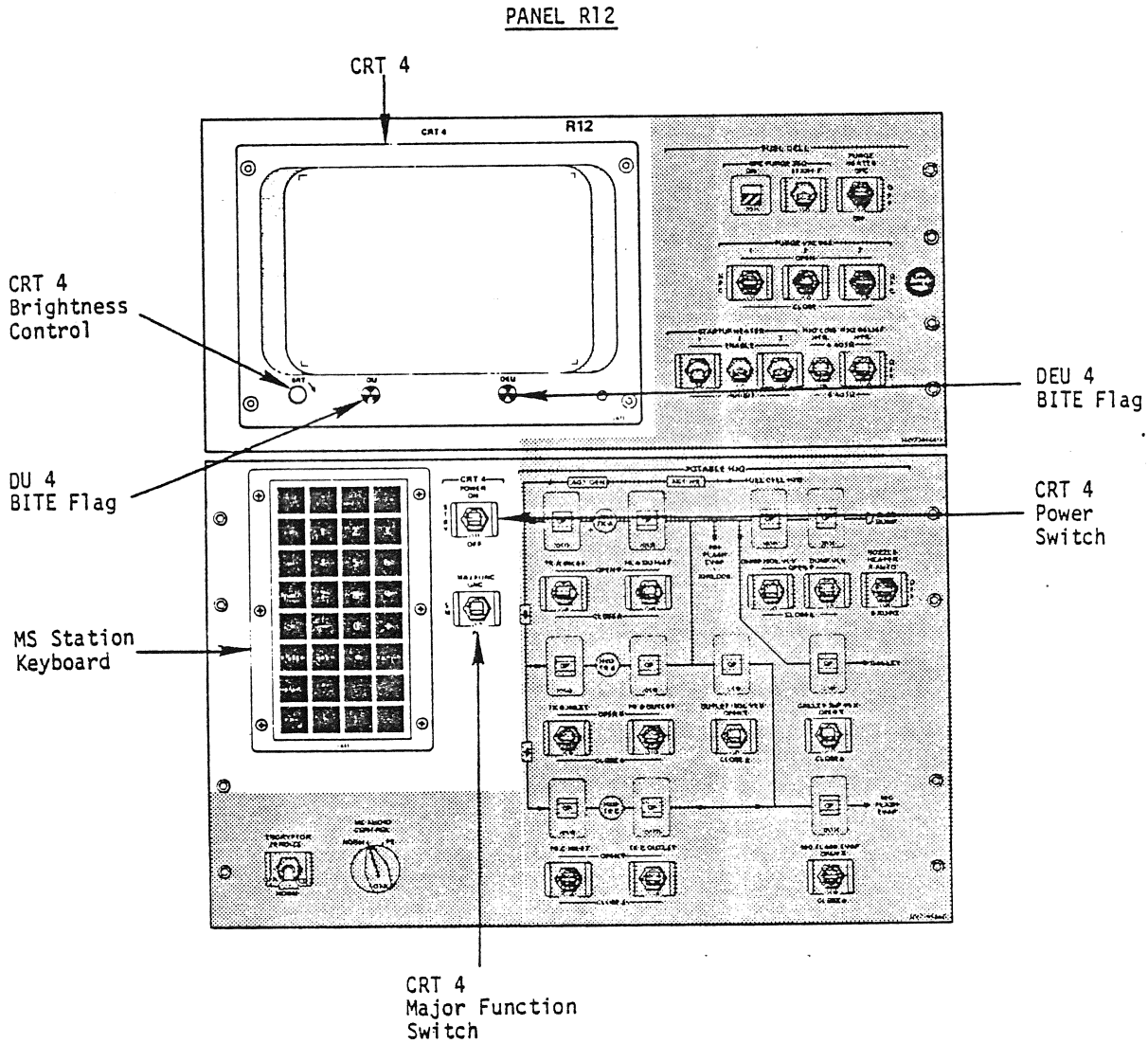


Figure 3-17. Panel R12

3.18 PANEL R13

3.18.1 CAUTION/WARNING PARAMETERS STATUS Light Matrix (120 White Lights). Lights 05, 15, 25, 35, and 45 represent self-fail for GPC's 1, 2, 3, 4, and 5, respectively. Provides aft station status to accompany any GPC status matrix (panel 01) yellow diagonal light and panel F7 C&W matrix red GPC light (with MASTER ALARM annunciation, refer to figure 3-18).

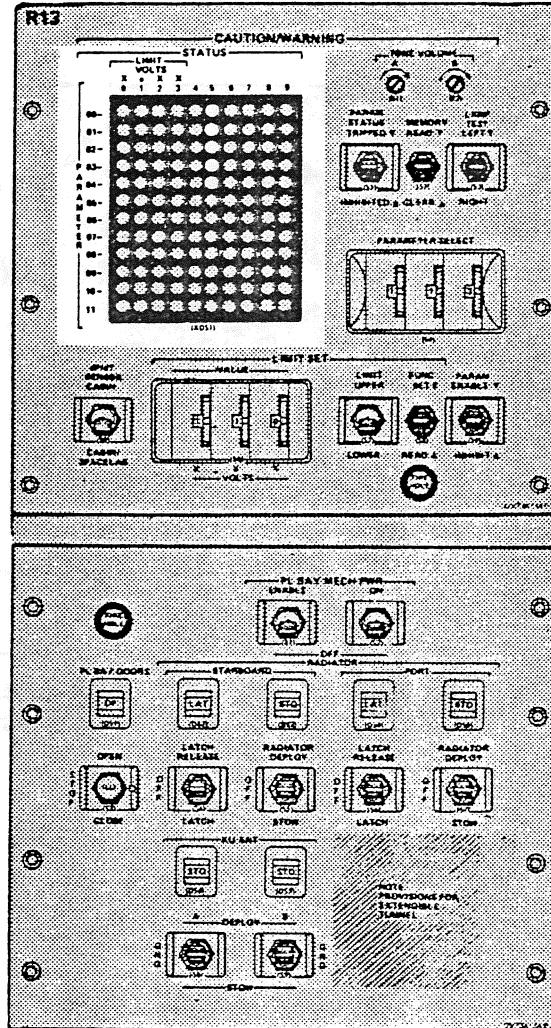


Figure 3-18. Panel R13

3.19 PANEL A1

Refer to figure 3-19 for panel A1.

3.19.1 DATA RATE XMIT (2-Position Toggle Switch). Directs the GCIL to command the NSP to transmit data at 128 kb/s (HIGH) or 64 kb/s if the S-Band PM hardware is under crew station control (refer to panel C3, S-Band PM control toggle switch).

3.19.2 POWER (3-Position Toggle Switch). Directs the GCIL to permit power to NSP 1, NSP 2 or neither NSP if the S-Band PM hardware is under crew station control (refer to panel C3, S-Band PM control toggle switch).

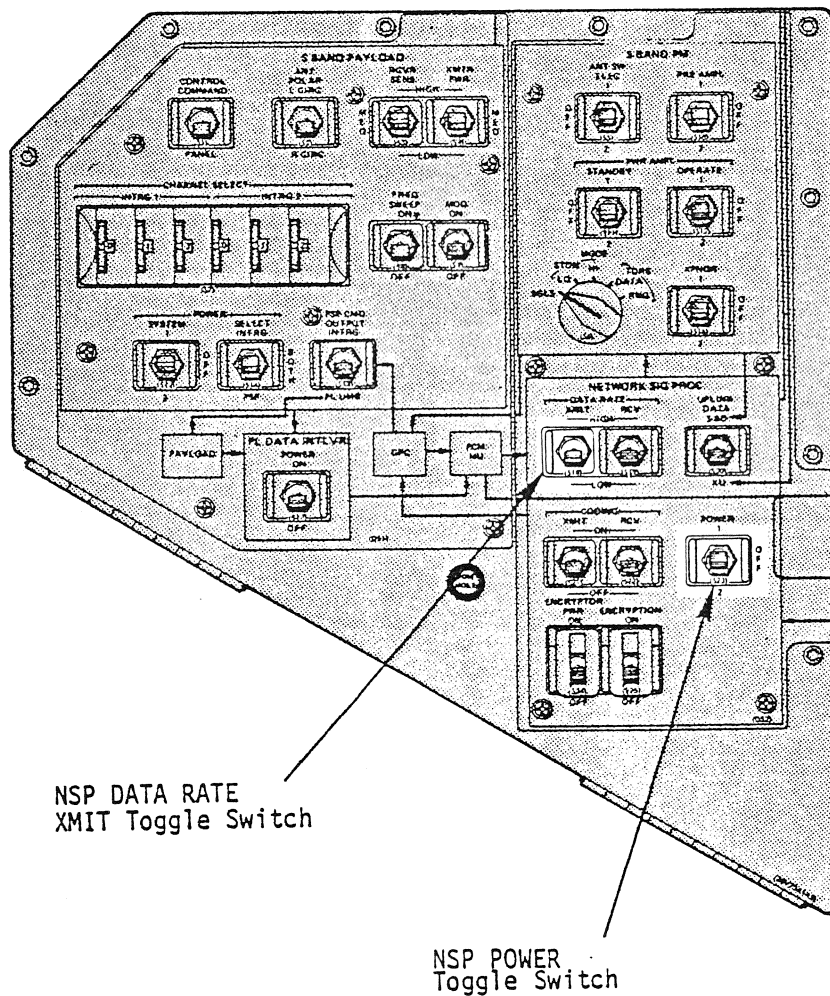


Figure 3-19. Panel A1

3.20 PANEL A7

3.20.1 MASTER ALARM (Black Letters on Red Background). Illuminated by C&W electronics upon detection of a class 2 problem (DPS class 2 involves GPC fail-tc-sync). Extinguished only by depression of any MASTER ALARM pushbutton indicator. Normally accompanied by a MASTER ALARM tone (see figure 3-20).

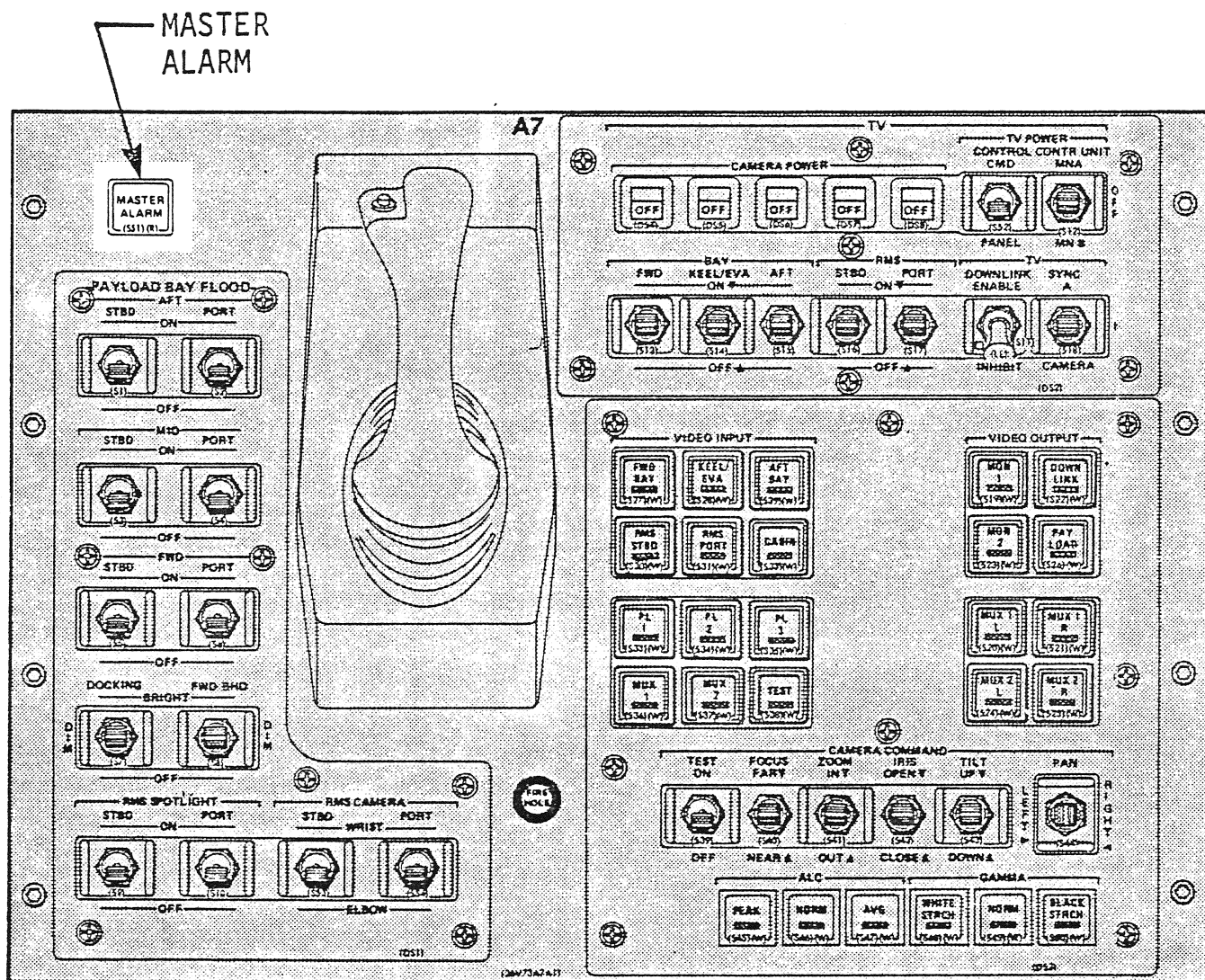


Figure 3-20. Panel A7



SECTION 4

FLIGHT COMPUTER SOFTWARE

4.1 OVERVIEW

The flight computer software consists of system software and applications software modules.

The system software modules consist of the software required to control the PASS GPC's and to provide the input, output, and operational control services to the applications software, ground users, and flight crew. It is resident in all PASS GPC's following Initial Program Load (IPL) and is partitioned into the Flight Computer Operating System (FCOS), the User Interface module, and the Systems Control module. As this last subdivision is transparent to the user, no distinction will be made in this document between the FCOS, User Interface, and Systems Control modules. Instead, they will collectively be referred to as the system software. The system software provides the following services:

- Starts and coordinates the initialization process
- Coordination of General Purpose Computer (GPC) and data bus configuration
- Discrete input monitoring and distribution
- Main memory modification
- Main memory overlays
- Synchronization
- Redundancy Management
- Timekeeping
- Input/Output (I/O) management and I/O error processing
- Multifunction CRT Display System (MCDS) interface software
- Uplink processing
- Downlist formatting
- Ground Support Equipment (GSE) processing
- System-level Specialist Function (SPEC) interface
- Post-IPL (before any Operational Sequences (OPS) overlays) contains Display Electronics Unit (DEU) loader software, and DEU self-test package

The Backup Flight System (BFS) software also includes system software modules which perform many of these same functions and will be discussed in section 5.

In order to conserve memory in each GPC, the software used to perform the mission (applications software) is divided into the Guidance, Navigation, and Control (GNC) major function, the Systems Management (SM) major function, and the Payload (PL) major function. The GNC, SM, and PL major function software blocks are further subdivided into mission-phase-oriented blocks called OPS. Each OPS is given a number to identify it. For example, the GNC launch OPS is called OPS 1 while the entry OPS is called OPS 3, as illustrated in figure 4-1.

Each of these OPS is subdivided further into software blocks called major modes, which relate to a specific portion of a mission phase. For example, Major Mode OPS 1 (often referred to as OPS 101 or Major Mode 101) contains the software pertaining to that part of the launch sequence known as the terminal count period, which extends from approximately 20 minutes prior to ignition until lift-off. Each major mode has an associated OPS display, which will be displayed on a CRT if it is in the appropriate major function.

A transition from one mission phase (OPS) to another is referred to as an OPS transition. These transitions are always initiated by flight crew intervention.

Depending upon the individual case, a major mode may be initiated automatically (based on specific events) or through a keyboard entry to a DEU which is assigned to the appropriate GPC(s). Under certain conditions, the current major mode may be requested for purposes of reassigning data buses and changing the redundant set. Note that a complete keyboard entry must be made to initiate a major mode. If the transition from OPS 2 Major Mode 1 to OPS 2 Major Mode 2 is desired, a crew entry of OPS 202 PRO will be required. Also, only certain of these OPS/mode transitions are allowed by software. The current legal OPS/mode transition table is in appendix G. The Class 5 fault message ILLEGAL ENTRY will appear if an illegal OPS/mode transition is requested.

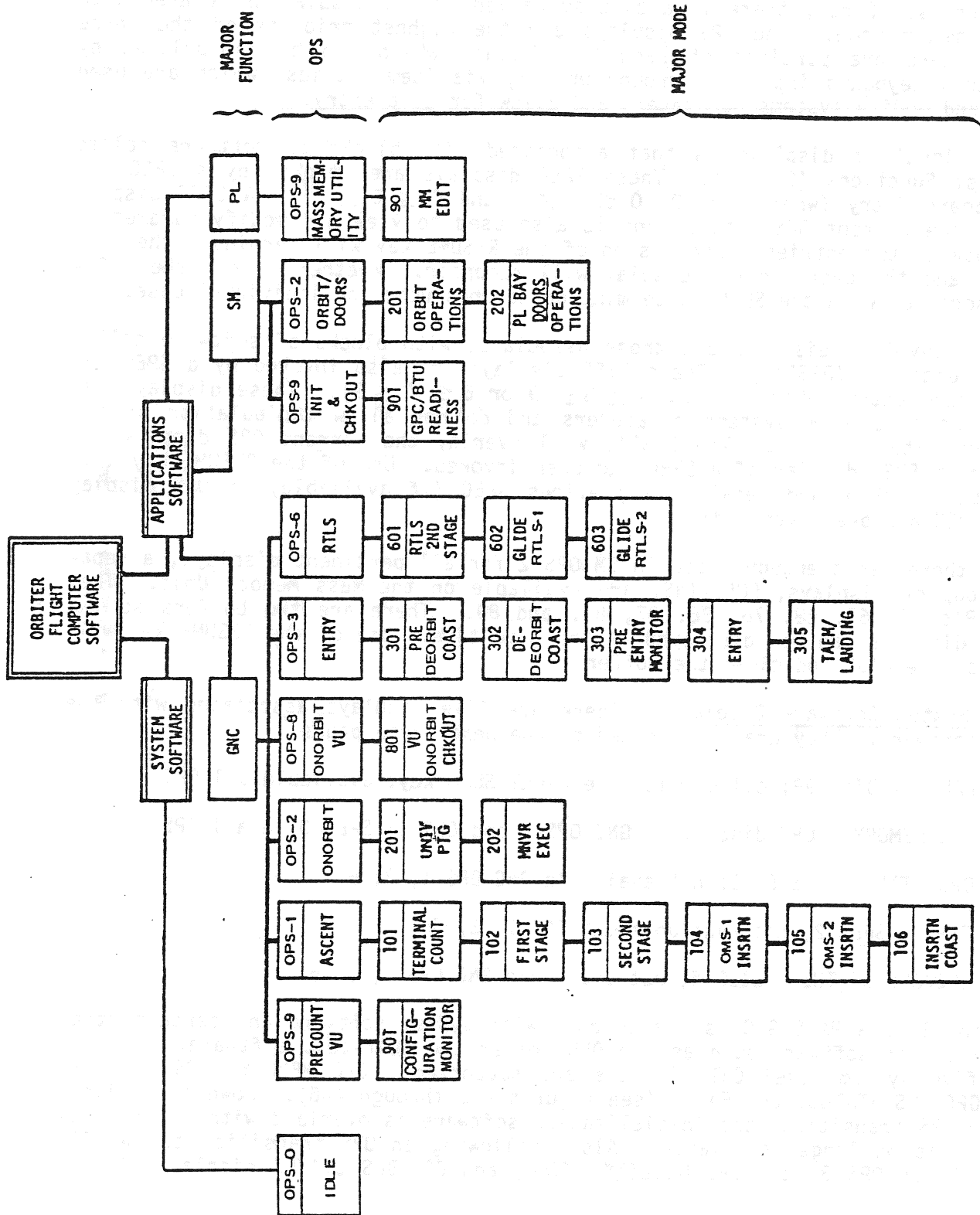


Figure 4-1. Orbiter Flight Computer Software

4.2 CONCEPTS AND DEFINITIONS

4.2.1 Displays. There are three display levels which can be used by the flight crew for observation of systems' data and status and for SM and control via keyboard entries. First, there is a display called an OPS display associated with each OPS/major mode. The OPS displays are the highest priority of the three types. There are portions of each OPS display which can be manipulated by flight crew keyboard input (or ground uplink) via item entries, which are used to view and modify systems parameters and allow for data entry.

The next level of displays is that associated with blocks of software called Specialist Functions (SPEC's). These SPEC displays are invoked by a SPEC ABC PRO Keyboard Entry (where $A \neq 9$, $0 \leq B \leq 9$ and $0 \leq C \leq 5$). A SPEC display overlays the current OPS display and is also used to view and modify parameters via keyboard item entries. Depression of the RESUME key will terminate the SPEC display, and the overlaid OPS display will reappear. Whether or not the software associated with the SPEC is terminated depends upon the individual case.

The third level of displays are those associated with blocks of software called display functions (DISP's). These DISP displays are also invoked by a SPEC ABC PRO keyboard entry (where $A = 9$, $0 \leq B \leq 9$ or $6 \leq C \leq 9$). These displays can only be used to view systems parameters and do not allow manipulation of the system via item entries. The DISP's will overlay the current OPS display and the current SPEC display if a SPEC had been invoked. Use of the RESUME key will terminate the DISP and recall the previous SPEC (if available) or OPS display (if no SPEC had been overlaid).

Because there isn't enough space in SM OPS 2 for all pertinent displays, a separate group of displays, ROLL-INS, are available on the Mass Memory Unit. They are DISP's 66, 67, 68, 76, 86, 87, 88, and 89. There are two buffers so two roll-in displays can be displayed at the same time. Use of the RESUME key will terminate the DISP and clear the buffer.

4.2.2 System Software Displays. There are five displays associated with the systems software. They are illustrated on the next three pages.

- FAULT - DISP 99; called with the FAULT SUMM key; available all OPS
- GPC MEMORY - OPS display in GNC OPS 9 and OPS 0; SPEC 0 in all OPS
- DPS UTILITY - SPEC 1; not available GNC OPS 1, 3, 6
- TIME - SPEC 2; not available GNC OPS 1, 3, 6
- GPC/BUS STATUS - DISP 6; not available GNC OPS 1, 3, 6

Following IPL, a PASS GPC is loaded only with system software and certain other initialization software such as the DEU loader and self-test software. At this time, five system level CRT displays are supported - GPC MEMORY, DPS UTILITY, TIME, GPC/BUS STATUS, and FAULT (see figures 4-2 through 4-6). However, following any OPS transition, the initialization software is overlaid with other software and is no longer available. Also, following an OPS transition to GNC OPS 6, OPS 1, or OPS 3, the DPS UTILITY, TIME, and GPC/BUS STATUS display software

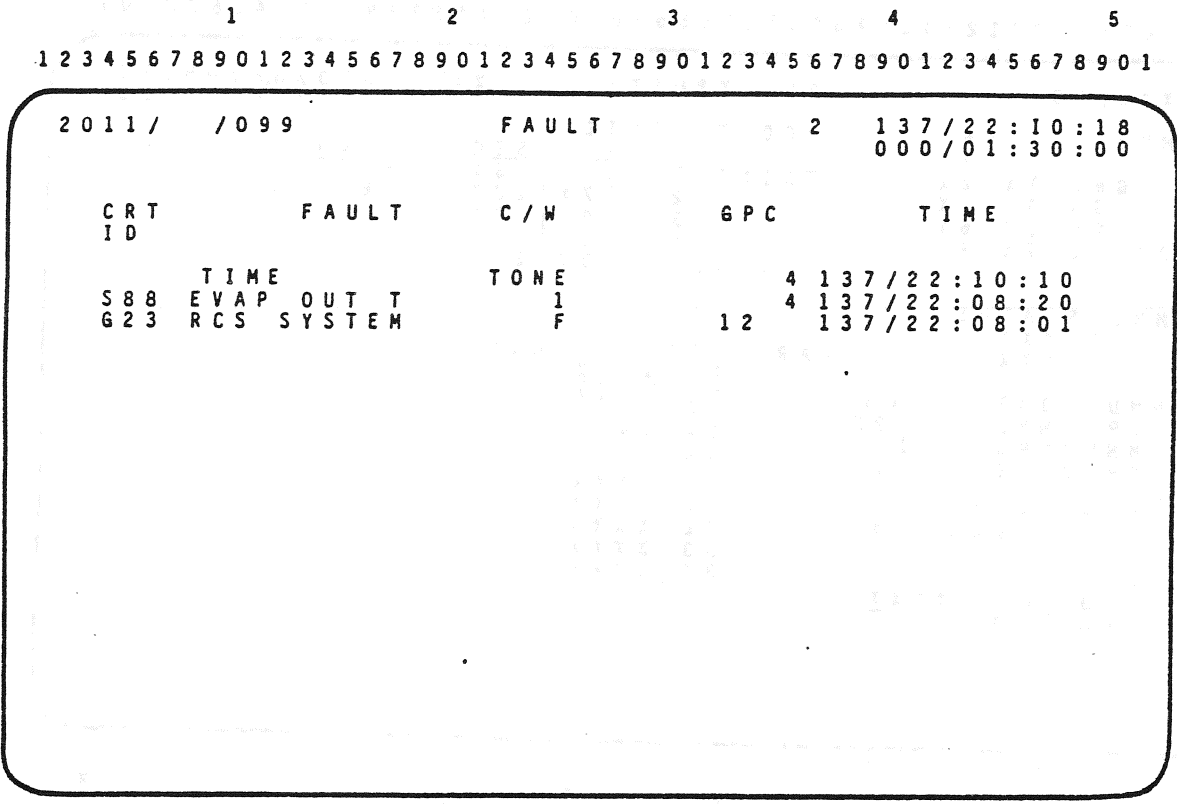


Figure 4-2. FAULT Display

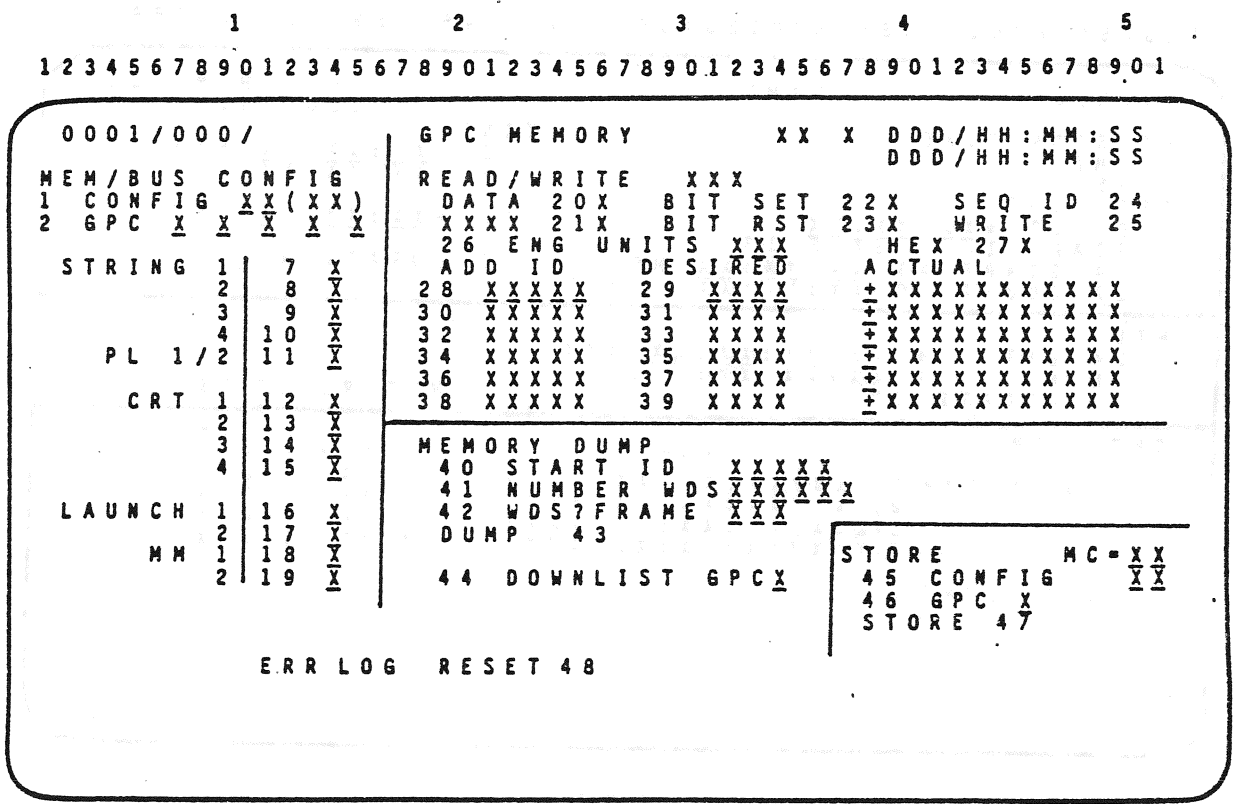


Figure 4-3 GPC MEMORY Display

```

1 2 3 4 5
1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1
XXXX/001/          DPS UTILITY          XX X DDD/HH:MM:SS
                                DDD/HH:MM:SS
MMU ASSIGN          PORT ASSIGN
  1 2
GNC 1X 2X          STRING 1 15X 16X
SM 3X 4X           2 17X 18X
PL 5X 6X           3 19X 20X
OPS 0 7X 8X        4 21X 22X
                                PL 1/2 23X 24X
                                UL CNTL
                                A AUTO 35X
                                ENA 36X
                                INH 37X

MMU STATUS
  1 XXX
  2 XXX
MMU SOURCE / BUS
GPC/MMU          9X
MMU/MMU          10X
GPC/LDB          11X
CKPTRETRV
  ENA 12X
RTC
  13 XXXX XXXX
  CMD 14
  
```

Figure 4-4. DPS UTILITY Display

```

1 2 3 4 5
1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1
XXXX/002/          TIME          XX X DDD/HH:MM:SS
                                DDD/HH:MM:SS
MISSION TIME          TONE
GMT 1X               3 XX:XX:XX HSM T
MET 2X               6 XX:XX:XX
CRT TIMER
9 SET +XX:XX:XX     20 +XX:XX:XX CRT T
START 12 STOP 13
14 START AT XX:XX:XX MSN T 23 DURATION XX
17 COUNT TO XX:XX:XX MSN T

MTU
24 GMT +XXX/XX:XX:XX.XXX
28 MET +XXX/XX:XX:XX.XXX
UPDATE 32 MET RESET 33

GPC TIME
MTU ACCUM 1 XXX/XX:XX:XX.XXXS
2 XXX/XX:XX:XX.XXXS
3 XXX/XX:XX:XX.XXXS
GPC XXX/XX:XX:XX.XXXS
TRY 1 GPC
34 2 XX
35 3 XX
36 4 XX
37 5 XX
TIME SYNC 38 (X X)
  
```

Figure 4-5 TIME Display

2011/000/006		GPC/BUS STATUS					4 000/00:07:20 000/00:00:00	
GPC		1	2	3	4	5		
MODE		RUN	RUN	HALT	RUN	HALT		
OPS		G2	G2	0	S2	0		
STRING 1	FF	*			↓			
	FA	*			↓			
2	FF		*		↓			
	FA		*		↓			
3	FF		*		↓			
	FA		*		↓			
4	FF	*			↓			
	FA	*			↓			
PL 1		↓	↓		↓			
	2	↓	↓		↓			
LAUNCH 1		↓	↓		*			
	2							
CRT 1		*			↓			
	2		*		↓			
	3	↓	↓		*			
	4	↓	↓		↓			

Figure 4-6. GPC/BUS STATUS Display

will be overlaid and will not be available. When an OPS other than GNC OPS 6 or 3 is loaded, these three displays (DPS UTILITY, TIME, GPC/BUS STATUS) are again included in the overlay and are available for use.

The statement that a PASS GPC is in OPS 0 means that it is processing system software but is not processing any applications (GNC, SM, PL) software. Thus, in OPS 0, a GPC can perform certain tasks including downlist, uplink, time-keeping, DEU polling, GSE polling, as well as tasks initiated by crew interface with one of the available system level displays. The OPS display for OPS 0 is the GPC MEMORY display.

A GPC will be placed in OPS 0 by a crew entry of OPS 000 PRO to a DEU to which it is listening if it is in one of the following major modes: GNC OPS 201 or 901; SM OPS 201, 202, or 901; or PL OPS 901.

Note that if a GNC redundant set exists, in GNC OPS 2 or 9, an OPS 000 PRO input to a PASS GNC DEU will result in all members of the redundant set going to OPS 0 (i.e., ceasing to process GNC application software). A single PASS GPC may be placed in OPS 0 at any time by moving that GPC's MODE switch from RUN to STBY (STANDBY) and back to RUN, or from RUN to STBY to HALT and back to RUN. If a GPC were running in a specified major function (GNC, SM, PL) and it was not a target GPC for a new OPS in that major function, then it would be forced to OPS 0 at that transition. Thus, it will stop processing major function software.

To leave OPS 0, a PASS GPC must be moded to GNC OPS 201, 301, or 901; SM 201, 202 or 901, or PL OPS 901. These are the only legal OPS transitions from PASS GPC OPS 0 as illustrated in figure 4-7.

4.2.3 GPC MODE - HALT, STBY, and RUN. Each GPC has its own three-position toggle-type MODE switch located on panel 06. Each of these switches has a HALT, a STBY, and RUN position; and the position of this switch determines the software processing available from that GPC's as illustrated in table 4-1.

In the HALT mode, the GPC is in a hardware-controlled state in which no software can be executed. The GPC MODE switch, the IPL SOURCE switch, the Mass Memory Units (MMU) Ready discrettes, and the GPC IPL pushbutton discrettes are all monitored in this state.

In the RUN mode, the GPC supports its normal OPS-assigned vehicle operations.

With the exception of the IPL case, a PASS GPC in STBY is in a state in which no software is executed. In this state, the GPC MODE switch discrettes are cyclically monitored. Also, a GPC in STBY cyclically resets its diagonal light on the GPC status matrix. If two or more other GPC's are still sending fail votes to that GPC, however, the diagonal light will remain on. It is necessary, as a matter of procedure, that a GPC being moded from RUN to HALT be moded to STBY prior to going to HALT (long enough for the STBY discrete to be monitored for 1-2 seconds), since moding to STBY allows for an orderly software cleanup, which will then allow a GPC to be correctly reinitialized without the necessity of performing an IPL. Should a GPC be moded from RUN to HALT (without pausing in STBY), there would be no guarantee that it could correctly perform its functions upon being remoded to RUN.

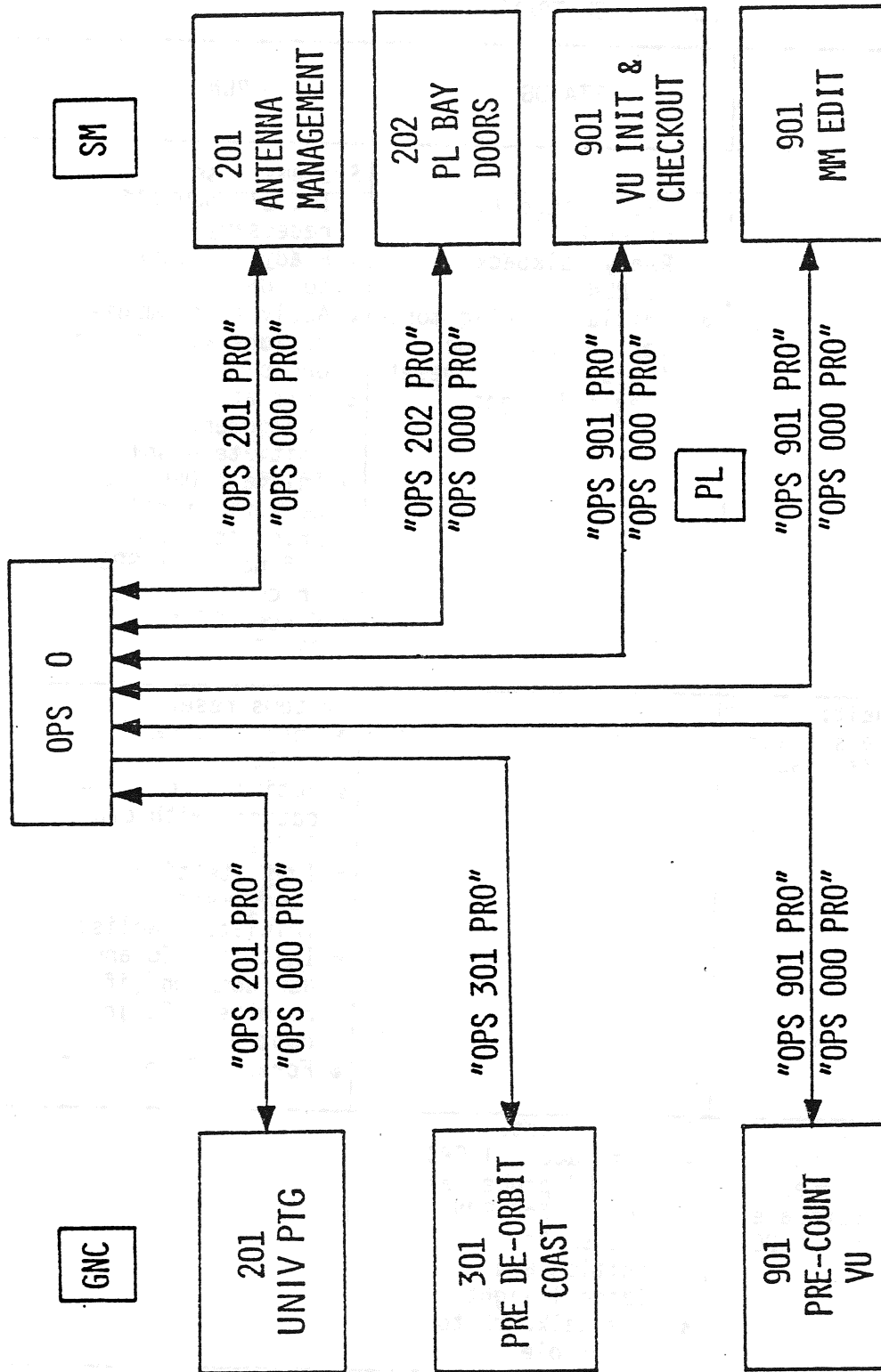


Figure 4-7. Transitions Involving OPS 0

TABLE 4-1
MODE SWITCH TRANSITIONS

TO FROM	HALT	STANDBY	RUN
HALT		<p>Systems reset:</p> <ul style="list-style-type: none"> ● IPL cleanup (if necessary) ● Ready talkback (TB) to RUN ● Initiate cyclic monitor for RUN mode transition and reset diagonal light 	<p>Systems reset:</p> <ul style="list-style-type: none"> ● IPL cleanup (if necessary) ● Ready talkback to RUN ● Activate communications with other GPC's ● Initiate time management ● Initiate downlist ● Initiate DEU and network signal processor command (if no other GPC in control) ● Force GPC to OPS-0.
STBY	<p>Hardware halt:</p> <ul style="list-style-type: none"> ● No active software ● GPC IPL (if required) 		<p>Systems reset:</p> <ul style="list-style-type: none"> ● Ready talkback to RUN ● Activate communications with other GPC's ● Initiate time management ● Initiate downlist. ● Initiate DEU and NSP command (if no other GPC in control) ● Force GPC to OPS-0
RUN	<p>Same as STBY HALT transition (not a preferred sequence; software downmode in STANDBY is proper)</p>	<p>Systems reset:</p> <ul style="list-style-type: none"> ● Terminate all CPU and IOP processes ● Monitor for RUN mode switch position and reset diagonal light ● Mode talkback to barberpole 	

The current GPC MODE of each of the PASS GPC's will appear on the GPC/BUS STATUS display (available during all mission phases except GNC OPS 1, 3, and 6). See figure 4-6. Note that only RUN or HALT will be displayed as STBY is not distinguished from HALT.

4.2.4 Synchronization. Synchronization (sync) refers to the software scheme which is used to ensure simultaneous intercomputer communication of necessary GPC status information among the Primary Avionics Software System (PASS) GPC's. It is also utilized to ensure that all the appropriate GPC's have received certain data and error information.

4.2.4.1 Common Set. A Common Set (CS) is a set of PASS GPC's which cyclically (6.25 times per second) exchanges certain status information over the Intercomputer Communication (IC) data buses at specified common set sync points. This exchanged status information includes fault messages, OPS overlay requests, input/output errors, GPC status matrix data, DEU Major Function switch settings, GPC/CRT keyboard entries, uplink information, and MTU time. The GPC's in the common set can be executing different software. For example, on orbit, the CS may include a GPC executing GNC software and a GPC executing SM software. Except for GPC failure situations, all PASS GPC's will be in the common set.

4.2.4.2 Redundant Set. A Redundant Set (RS) is a set of PASS GPC's simultaneously executing identical software with the use of identical inputs and producing identical outputs. In order to maintain the redundant set, these GPC's will exchange status information between 400 and 600 times per second, the frequency depending on their operating software load. RS GPC's are always members of the CS but are limited to those GPC's executing GNC software. The software automatically forms the redundant set at specified OPS transitions (e.g., ascent (OPS-1) to on-orbit (OPS-2) transition), and at specified OPS/mode recalls. This topic will be discussed later on in this section.

4.2.4.3 Simplex GPC. A simplex GPC is a GPC which is in RUN and is not a member of the redundant set. It may be a member of the common set, but it does not have to be. For example, the BFS GPC would be a simplex GPC which is not a member of the common set.

4.2.5 Downlist GPC (Prime GPC). All GPC's which are operating in a redundant set are processing identical software, using identical inputs, and processing identical outputs. Therefore only the downlist from one member of the redundant set needs to be incorporated into the telemetry and sent to the ground. The redundant set GPC whose downlist is incorporated into the telemetry and sent to the ground is called the downlist GPC or prime GPC. This GPC will drive PCMMU toggle buffer 1 with downlist data.

Selection of the downlist GPC can occur automatically according to a selection hierarchy based upon certain conditions or as a result of a flight (or ground) crew entry to a CRT display. The first PASS GPC to complete IPL and be moded to RUN will be the downlist GPC. The selection of a new downlist GPC is automatically initiated at OPS transitions and OPS mode recalls involving redundant set formation. Furthermore, if the redundant set had three or more members, the downlist GPC is in the redundant set and if the downlist GPC fails to sync with all other redundant set GPC's, a new downlist GPC is automatically selected by the software.

In both of these situations, the software selects the lowest numbered GPC in the redundant set as the new downlist GPC. In addition, the crew can select any GPC in the common set to be the prime GPC and thus, to command toggle buffer 1. This is done via Item 44 on the GPC MEMORY display (Spec 0). While software protection does exist to ensure that the crew put a number between 1 and 5 for Item 44, it does not offer protection against assigning the prime GPC function outside the common set. In this case, the function is lost (no GPC drives toggle buffer 1).

The current downlist GPC ID appears in ITEM 44 on the GPC MEMORY display.

4.2.6 Data Bus Network. Figure 4-8 illustrates, in block diagram form, the DPS data bus network. Each GPC communicates with the other GPC's and the pictured Orbiter hardware over seven different generic groups of data buses. Each data bus (with the exception of the intercomputer data buses) is a bidirectional data bus. That is to say, the traffic on that data bus can flow in either direction. More than one GPC may be required to receive information transmitted over a data bus, but problems might develop if more than one GPC attempted to issue commands over the same bus at the same time. These requirements led to the command and listen modes of GPC communication over a data bus. Figure 4-9 illustrates five GPC's which are communicating over flight-critical Data Bus 1 to flight-critical forward MDM 1. Let us assume that this figure illustrates the arrangement during the launch phase of a flight. In this mission phase, GPC's 1-4 will be operating in a redundant set and GPC-5 will contain Backup Flight System (BFS) software. In addition, GPC-1's transmitter is enabled on FC1. As you have learned previously, the four GPC's operating in the redundant set all need to receive the same information at the same time. All four of these GPC's, therefore, must listen on the data bus; i.e., their receivers must be enabled on FC1. In addition, GPC-5 requires certain information in order to perform its functions as the BFS GPC. It too must listen to the transactions on this data bus.

In this case, when all the GPC's require a time update from the Master Timing Unit (MTU), GPC-1 is the only GPC that actually issues the command to the MTU because GPC-1 is in command of the bus. All of the GPC's receive this time update, however, because they are all listening to the response data transmitted over this data bus.

4.2.6.1 Flight Critical Data Buses. Of particular interest are the Flight Critical (FC) data buses, since they are required to maintain flight control of the Orbiter. Figure 4-10 illustrates the Orbiter FC data buses and their interfaces with the GPC's, flight-critical MDM's DDU's MEC's, and EIU's. Each of the MDM's has two ports (MIA's), labeled in the diagram as 1 (primary) and 2 (secondary). Each of the eight Flight Critical data buses is connected to a port of a Flight Critical Forward (FF) MDM and a port of a Flight Critical Aft (FA) MDM. FC's 1-4 are each connected to the primary ports of their FF MDM's, the secondary ports of their FA MDM's and all three Display Driver Units (DDU's) and FC's 5-8 are each connected to the secondary ports of their FF MDM's, the primary ports of their FA MDM's and all the MEC's and EIU's.

Only one port of an MDM is accessed at a time. In the primary mode, only the primary ports of the FF and FA MDM's are being accessed. In the secondary mode,

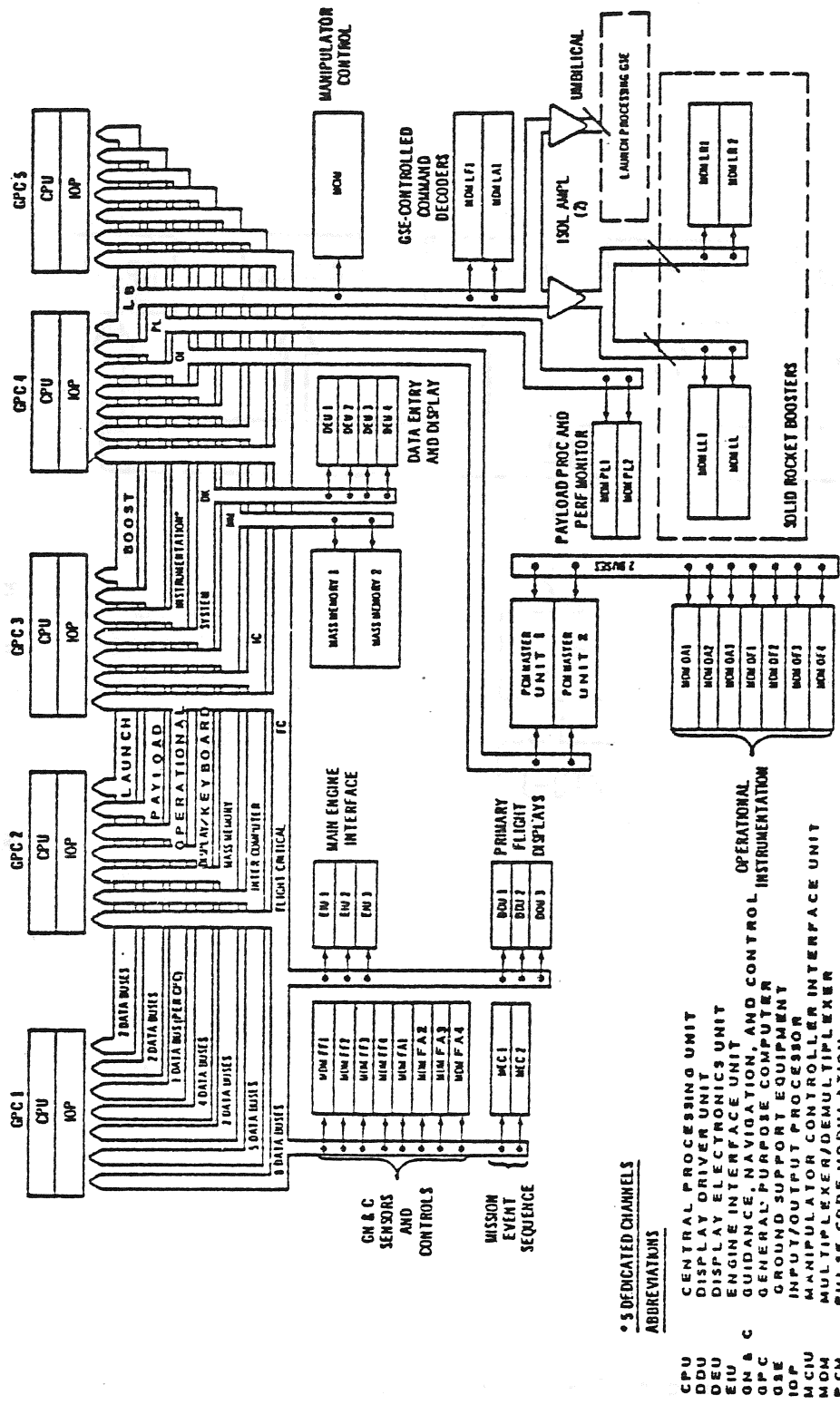


Figure 4-8. DPS Data Bus Network

5 DEDICATED CHANNELS
ABBREVIATIONS

- CPU
- DDU
- DEU
- EU
- GN & C
- GPC
- ISE
- IOP
- MCNU
- MDM
- PCM
- CENTRAL PROCESSING UNIT
- DISPLAY DRIVER UNIT
- DISPLAY ELECTRONICS UNIT
- ENGINE INTERFACE UNIT
- GUIDANCE, NAVIGATION, AND CONTROL INSTRUMENTATION
- GENERAL PURPOSE COMPUTER
- GROUND SUPPORT EQUIPMENT
- INPUT/OUTPUT PROCESSOR
- MANIPULATOR CONTROLLER INTERFACE UNIT
- MULTIPLEXER/DEMULTIPLEXER
- PULSE CODE MODULATION

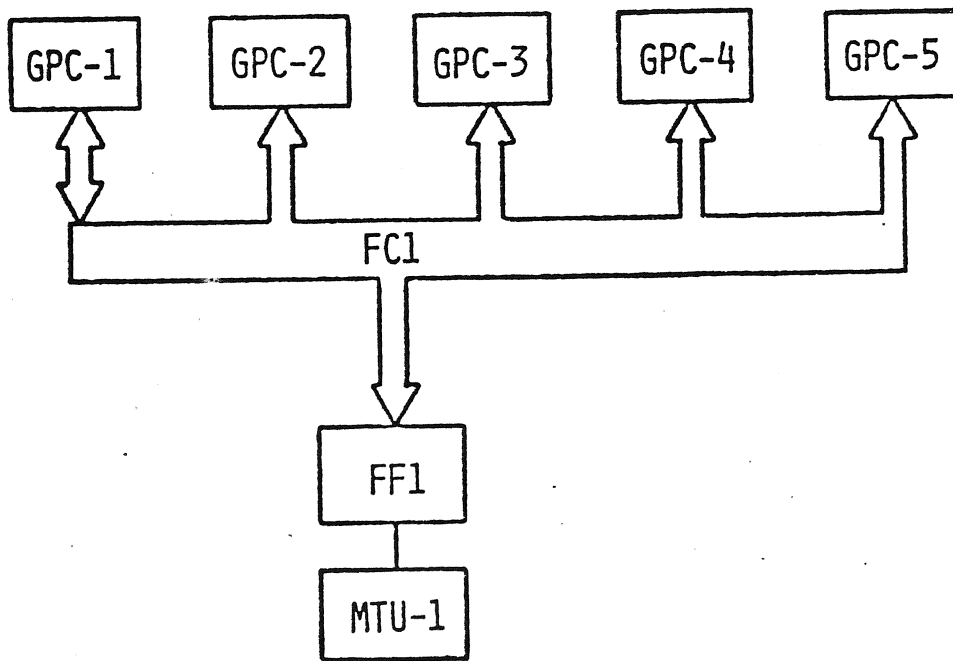


Figure 4-9. Five GPC's

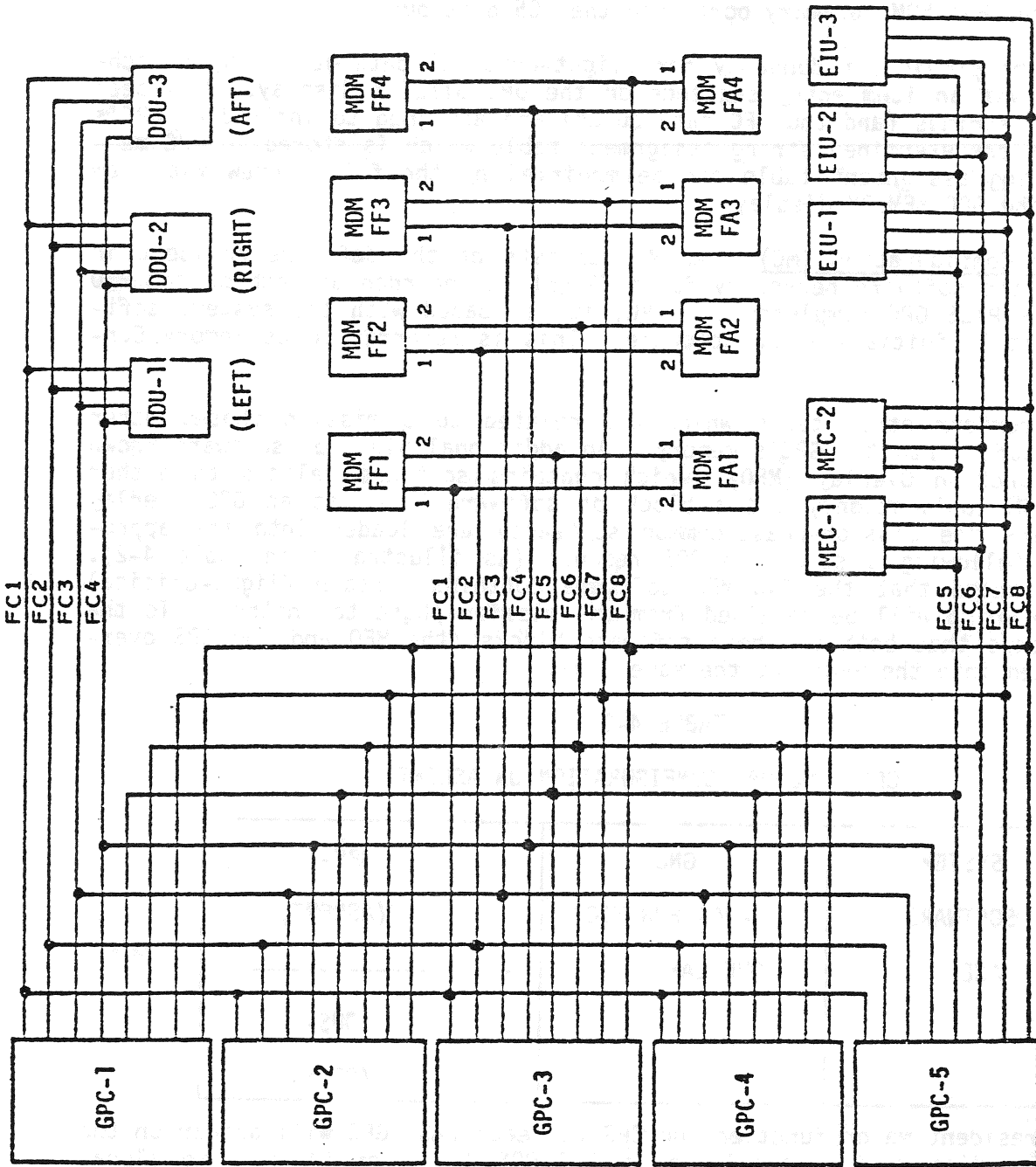


Figure 4-10. Orbiter Flight Critical (FC) Data Buses

only the secondary ports are accessed. Therefore, if (as in the previous figure) GPC-1 is in command of String 1 in the primary mode, it will issue its commands to the DDU's and to the hardware connected to the FF1 MDM (primary port) via flight-critical Data Bus 1 and to the MEC's, EIU's, and the hardware connected to the FA1 MDM (primary port) via the FC5 data bus.

This arrangement provides redundancy for flight-critical data access by switching MDM ports via an item entry sequence on the DPS UTILITY display. As seen in figure 4-11 strings (and thus FC data buses) are assigned to individual GPC's according to a predetermined string assignment table which is stored in GPC memory. The string assignment table can be modified by the flight crew via item entries into the GPC MEMORY display.

4.2.7 Memory Configuration (MC). An MC consists of the software resident in the GPC. All the software necessary for a flight is recorded on each of the MMU tapes. When a PASS GPC completes its IPL, it is loaded with the systems software, plus certain initialization software. This is referred to as Memory Configuration 0.

In order to perform other tasks which are related to a mission phase, other software is loaded into the GPC's memory. An additional block of software known as a Major Function Overlay (MFO) (which contains software related to either GNC, PL, or SM applications) and a block of software known as an OPS overlay (which contains the mission-phase-common software) are loaded into the appropriate GPC's following a specified OPS request (as illustrated in table 4-2). It should be noted that the GNC MFO software contains certain flight-critical (FC) software which will be retained from one mission phase to another. To the user, it appears that both of these software blocks (the MFO and the OPS overlay) are loaded into the GPC's at the same time.

TABLE 4-2

GPC-1 MEMORY CONFIGURATION ON ASCENT

SYSTEM	GNC	OPS-1
SOFTWARE	MAJOR FUNCTION	(ASCENT)
BASE	OVERLAY	-----
		OPS-6
		(RTL5)

The current resident major function and OPS for each PASS GPC will appear on the GPC/BUS STATUS display (not available in GNC OPS 1, 3, or 6) with an alphanumeric indicator in which the left-most character will be a G(GNC), S(SM), P(PL), or a blank (IPL), and the right digit will indicate the number of the current or last resident OPS.

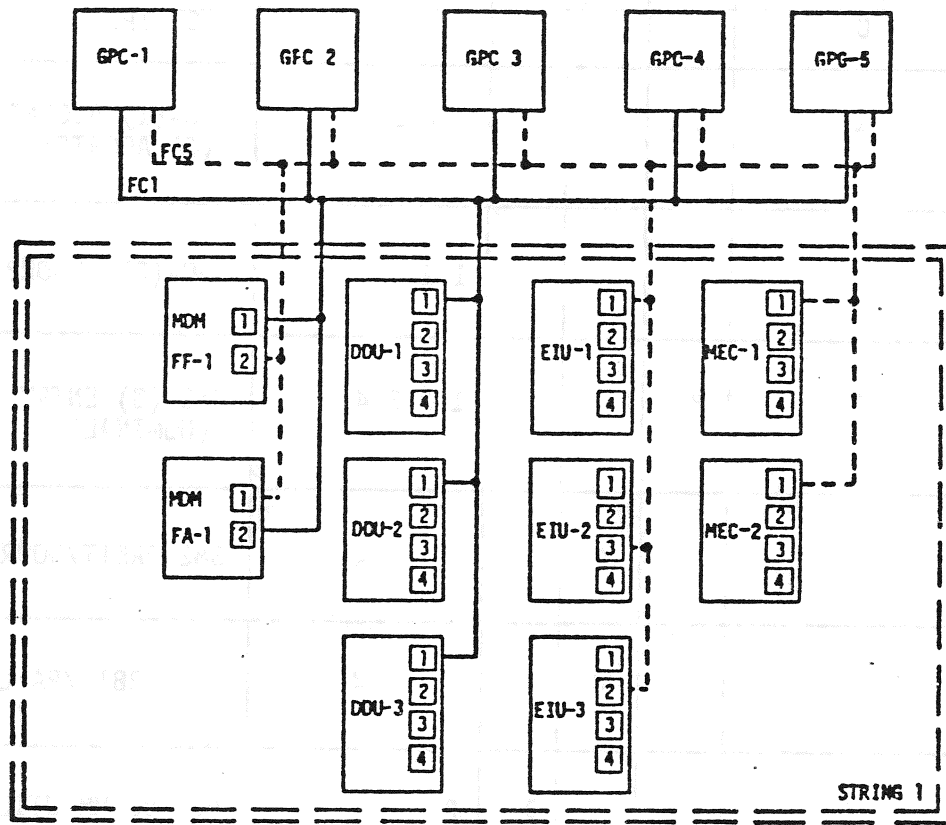


Figure 4-11. String 1

TABLE 4-3

NOMINAL MEMORY CONFIGURATION TABLE

SELECTION OF OPS			CAUSES	WHICH CONTAINS OPS #'S			TO BE LOADED INTO	CONTENTS
GNC	SM	PL	MEMORY CONFIG #	GNC	SM	PL	GPC#S:	
			0					POST IPL
1			1	1,6			1 2 3 4	GNC-(1) ASCENT, (6) ABORTS
2			2	2			1 2	GNC-(2) ON-ORBIT
3			3	3			1 2 3 4	GNC-(3) ENTRY (NOMINAL)
	2		4		2		4	SM2 ORBIT/DOORS
	4		5		4		4	SM4 ORBIT/PAYLOADS
		9	6			9	2	PL9 VU MM UTILITY
8			8	8			1 2	GNC 8 - VU ON-ORBIT CHKOUT
9			9	9			1 2 3 4	GNC 9 - VU PRECOUNT

4.2.7.1 Memory Configuration Table. Each PASS GPC maintains a software memory configuration table, which contains the initiating OPS and the numbers of the GPC's that are scheduled to receive the software for each MC. Those GPC's are often referred to as the target GPC's or selected GPC's for that MC. The memory configuration table (table 4-3) includes the Nominal Bus Assignment Table (NBAT) which specifies which of the target GPC's will control which buses when the memory configuration is requested. The memory configuration table is used at OPS transitions involving memory configuration or upon a legal OPS/Mode Recall.

The new MC is called into the target GPC's when a crew entry is made to a keyboard unit, based on the position of the associated MAJ FUNC switch. For example, a crew entry of OPS 301 PRO with a MAJ FUNC switch setting of GNC would bring Memory Configuration 3 into GPC's 1, 2, 3, and 4.

4.2.7.2 Nominal Bus Assignment Table (NBAT). Associated with each MC is the NBAT for that MC which governs the assignment of the FC, PL, Launch Boost (LB), Mass Memory (MM), and Display/Keyboard (DK) data buses (as illustrated in table 4-4).

This internally stored table indicates which buses will be commanded (transmitters enabled) by which target GPC's for that MC.

The assignment of strings and data buses to GPC's is accomplished during OPS transitions and OPS/mode recalls. The current GPC/bus assignment may be observed on the GPC/BUS STATUS display (SPEC 6) (not available GNC OPS 1, 3, 6) for the Strings, PL, Launch, and DK (also referred to as CRT) data buses.

The Multiplexer/Demultiplexer's (MDM's) on the Strings and PL data buses are dual port devices. The hardware is designed, however, to allow only one port to be accessed at a time. Still, if it were determined that one port of one of these MDM's had failed, it would be advantageous to switch and send commands to the other port. This capability is available in all OPS except GNC OPS 1, 3, and 6 via inputs to the DPS UTILITY display (figure 4-4). On this display, an asterisk by the appropriate item number (15-24) indicates which ports (Primary or Secondary) are being accessed on that String or PL data bus. When this display is available, it is possible to switch ports being accessed with the appropriate item entry.

The flight crew (and ground controllers via an uplink capability known as DEU EQUIVALENT) have the capability to observe and modify the memory configuration and bus assignment tables by making keyboard entries to the GPC MEMORY display. This display is a system level SPEC which is available in all OPS. In order to observe or modify the selected GPC's and data bus assignments for a particular MC, the number (x) of that MC must be entered with Item 1 (ITEM 1 + x EXEC). At this time the appropriate numbers will appear to indicate the target GPC's and assigned command GPC's for each of the data buses. To modify this table, the appropriate item numbers and, for data bus assignments, GPC numbers must be entered. Note that the command GPC for a data bus must also be a target (selected) GPC for that MC for the assignment to take effect. Also, modification of the table is not effective until an OPS transition involving the MC or a legal OPS/Mode Recall.

TABLE 4-4
NOMINAL BUS ASSIGNMENTS

MEMORY CONFIGURATION	1 (G1, G6)	2 (G2)	3 (G3)	4 (S2)	6 (P9)	8 (G8)	9 (G9)
TARGET GPC's	1,2,3,4	1,2	1,2,3,4	4	2	1,2	1,2,3,4
STRING 1	1	1	1	0	0	1	1
STRING 2	2	2	2	0	0	2	2
STRING 3	3	1	3	0	0	2	3
STRING 4	4	0	4	0	0	1	4
PL1/2	1	0	1	4	0	0	1
LBD-1	1	1	1	0	0	1	1
LDB-2	2	2	2	0	0	2	2
MMU-1	1	1	1	4	2	1	1
MMU-2	2	2	2	4	2	2	2
DK-1	1	1	1	4	2	1	1
DK-2	2	2	2	4	2	2	2
DK-3	3	2	3	4	2	2	3
DK-4	0	0	0	0	0	0	0

4.2.8 Freeze-dried GPC. A GPC which is loaded with the OPS overlay for a particular MC without the software overlay being executed and then placed in STBY (and then HALT or powered off) is said to be freeze-dried with that MC. Prior to the OPS transition to that MC, the freeze-dried GPC can be moded back to RUN, (it will now be in OPS 0 not processing any application software), and then the appropriate OPS requested. Thus, the freeze-dried GPC would serve as a safeguard in case the MMU and/or MM buses failed. Also, it would be possible to reactivate the freeze dry computer rapidly on orbit if the PASS GNC GPC's failed. Thus, prior to the transition from OPS 1 to OPS 2, a PASS GPC will be freeze-dried with MC 3 (GNC OPS 3).

4.2.9 Memory Reconfiguration. Systems software may perform GPC Main memory reconfiguration with the use of an MMU or another GPC as the memory source. This reconfiguration is initiated by user selection of an MFO and OPS overlay software via a keyboard entry - OPS ABC PRO.

Although the system software is loaded into a GPC following IPL, a transition to Memory Configuration 1 or 3 overlays part of the system software, including the software associated with the DPS UTILITY, GPC/BUS STATUS, and TIME displays. Thus, these displays are not available in GNC OPS 1, 3, or 6. However, when a transition is made from OPS 1, 3, or 6 to another OPS (such as GNC OPS 2 or 9, SM OPS 2, etc.), it will be necessary to reload these areas of system software, as well as possibly reload a major function or OPS overlay. Still, current estimates indicate that an OPS MFO with no errors will take less than 15 seconds. With errors, it will take up to 75 seconds. During the overlay, the GPC memory SPEC will be displayed on any CRT commanded by a GPC involved in the transition.

If a legal OPS transition is requested (the legal OPS transitions are included in appendix G), the necessary OPS overlay and the necessary major function/system software overlay, if not already present, will be loaded into all target GPC's in the common set as specified in the memory configuration table. However, a user input requesting that a simplex MC (SM OPS 2, PL OPS 9, and SM OPS 9) be loaded into multiple GPC's (via modification of the memory configuration table) will be rejected and an ILLEGAL ENTRY fault message will be generated. Thus, neither PL nor SM software can be run redundantly. Also, if a target GPC is new to the major function configuration and is not in OPS 0 when the reconfiguration is requested, the request will be rejected and the Class 3 alarm and GPC CONF fault message will be generated. In addition, if a GPC specified as a target GPC in the memory configuration table is not a member of the common set, (the BFS GPC, for example) a Class 3 alarm, and a GPC CONF fault message will be generated when the reconfiguration is requested.

If an OPS transition is requested which is not legal, the fault message ILLEGAL ENTRY will appear. Also, it should be pointed out that if a GPC is running in a certain major function, then that GPC will be forced to OPS 0 (i.e., stop application software processing) when that OPS is requested. Thus, within a major function only one OPS may be active.

4.2.10 OPS/Mode Recall. OPS/Mode recalls can be divided into two categories. The first is a GPC reconfiguration which involves changing the target set and can only be done in major modes: GNC's 201, 301, 801, and 901. In any other

major mode, the request will be denied with the class 5 fault message ILLEGAL ENTRY. The second is a restrung which involves changing only the commanders on the busses and can be done in any major mode.

4.2.11 Memory Source Selection

4.2.11.1 IPL. During an IPL, an MMU is selected for the memory load via the IPL SOURCE switch on panel 06. This switch is a three-position toggle switch which will be either on the MMU 1 or MMU 2 position during the IPL sequence. At all other times, this switch will be in the OFF position.

4.2.11.2 OPS Transition/Mode Recall Source Selection. Under nominal conditions, upon request for a memory reconfiguration, the software will first ascertain if the requested software overlay is already resident in a GPC in the common set which is in OPS 0 or which is a target GPC for the requested overlay. If either the requested major function overlay or the OPS overlay is resident in such a GPC, that GPC will be used as the source for the part of the overlay that it contains. If there is more than one such GPC, the lowest numbered ID GPC is used. This means, for example, that in the transition from OPS 1 to OPS 2, GPC 1 will be the source for the major function overlay while a mass memory unit will be accessed for the OPS overlay. Note that even when another GPC is used as the source for the overlay, the actual transaction will occur over the mass memory data buses under the nominal configuration. This configuration is controlled via Items 9-11 on the DPS UTILITY display. Nominally, ITEM 9, GPC/MMU is selected.

It is possible, in certain OPS, to force the software to retrieve both the major function and OPS overlays from mass memory. This is done via crew input to the DPS UTILITY spec to select the MMU/MMU option (Item 10). Care must be exercised with this option, however, as it will result in a mass memory resident major function overlay being loaded in the GPC's. If this were a GNC memory configuration, it could result in the loss of current, accurate flight critical data, such as the vehicle state vector.

It is also possible to request that another GPC be used as the source for the reconfiguration and that the transaction be made over the Launch Data Buses (LDB) instead of the MM buses. This is done via Item 11, GPC/LDB, on DPS UTILITY. This would be preferable if there were a problem with the MM buses. Following any OPS transition involving a member of the common set, each common set GPC will be reinitialized to the GPC/MMU option. Furthermore, in an OPS where the DPS UTILITY display is available (not in GNC OPS 1, 3, 6), the selection of the GPC/LDB or MMU to MMU option to any GPC in the common set will be effective in all GPC's in the common set. These options are part of the ICC traffic. When a GPC is first moded to RUN and joins the common set, it will assume the option currently selected by the common set.

4.2.12 Checkpoint. Blocks of data, called checkpoint data, can be reserved for future use by storing these data on MMU. These data represent a snapshot look at the appropriate systems data taken at the time the checkpoint is made. Prior to launch, an initialized set of checkpoint data is loaded on the MMU's. At

specified times during a flight, these data can be updated in order to provide a more accurate data source should retrieval of this information be required. A checkpoint can be made for each major function. However, the software required to support a GNC or PL checkpoint will not be available in the early Shuttle flights, so only an SM checkpoint capability will be discussed here. This SM checkpoint is initiated by user entry to the SM TABLE MAINTENANCE display. The data in this checkpoint include current Fault Detection and Annunciation (FDA) status, including limit values, noise filter constants, telemetry constants, parameter annunciation inhibits, and current time. The checkpoint is initiated by an ITEM 18 EXEC input to the SM TABLE MAINTENANCE display as shown in figure 4-12. If the checkpoint is successfully written, the time and status (GOOD) will appear.

Item 12 on the DPS UTILITY display (figure 4-4) is the control which enables the incorporation of checkpoint data upon an OPS transition or an OPS/mode recall. This capability will be inhibited when the display is first initiated. This particular item number (12) is a SET/RESET type of item. The first entry of ITEM 12 EXEC will enable the checkpoint retrieval capability and place an asterisk next to the item number on the display. The next entry of ITEM 12 EXEC will inhibit the capability and cause the "*" to disappear. After the checkpoint has been used during an OPS transition or recall, the capability will again be inhibited automatically.

2011/060/

SM TABLE MAINT

2 237/14:35:02

000/01:30:00

PARAM

1 ID 0470215

VALUE = +58000.00+

LIMITS

ALERT

LOW

HI

BACKUP C&W

LOW

HI

2 *[+]14000.00

3 [+]50000.00

11 *[+]12000.00

12 [+]57500.00

4 []

5 [+]52500.00

6 []

7 []

8 FILTER 03

13 FILTER 03

ENA 9*

ENA 14*

INH 10

INH 15

CONSTANT

16 ID 0914123

17 VALUE = [+]75541.0000

CHECKPT 236/00:05:00

FDA

INITIATE 18

ENA 19*

STATUS GOOD

INH 20

Figure 4-12. SM TABLE MAINT Display

4.3 SYNCRONIZATION/GPC REDUNDANCY MANAGEMENT

The SYNC and GPC RM schemes employ both hardware and software methods to ensure that the GPC's operate together properly. The software controlled SYNC scheme is used to ensure simultaneous GPC operation, intercomputer communication (ICC) of specified GPC status information, and that all of the appropriate GPC's have received their required data. Software detected discrepancies in the above schemes may result in a FAIL discrete being sent to the erring GPC from the detecting GPC(s) via a dedicated FAIL discrete line(s). A software controlled sumword comparison is made to ensure that the redundant set GPC's are issuing identical critical output commands.

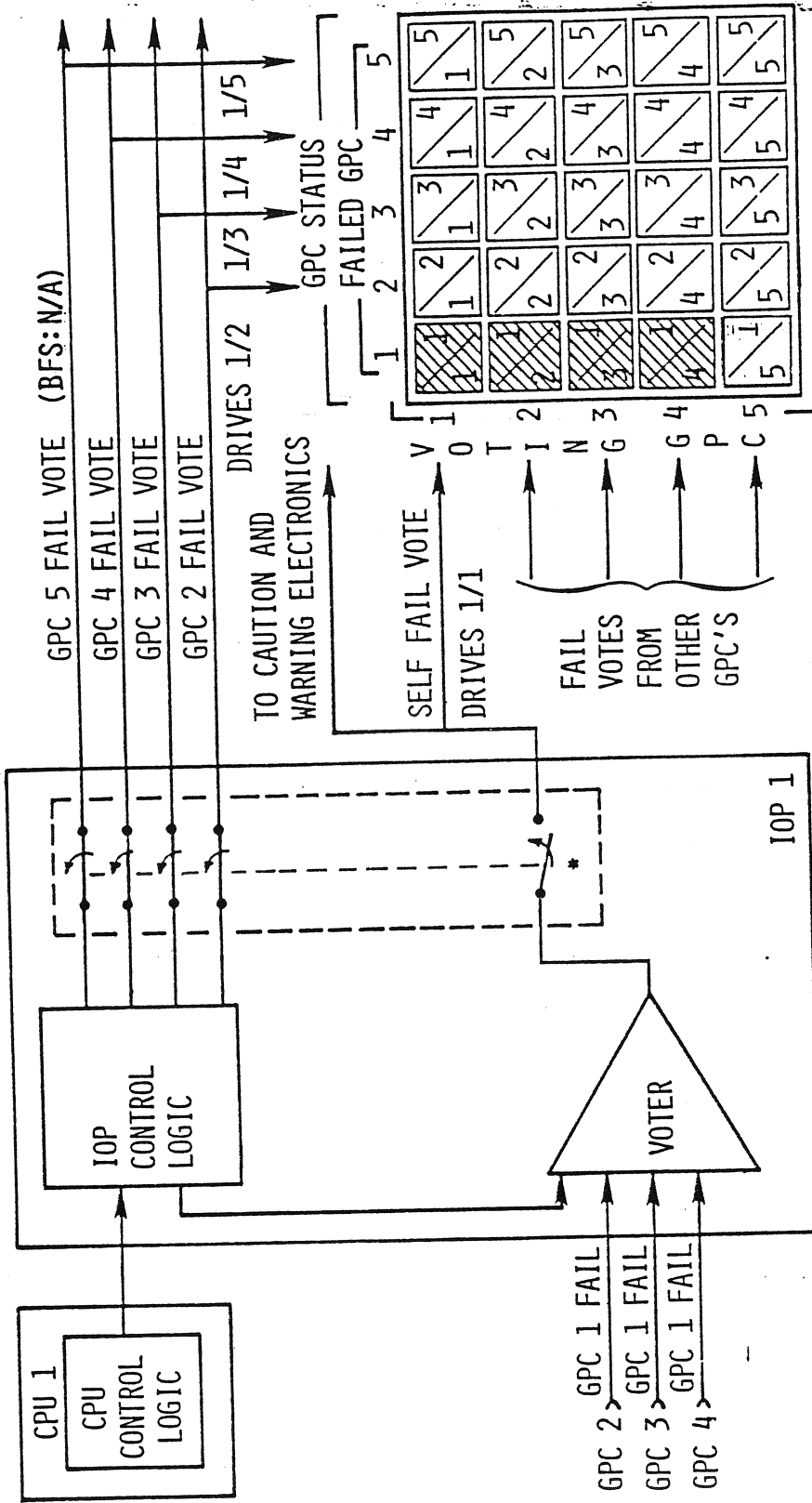
A hardware voter in each GPC is used to initiate GPC self-fail annunciation as a result of its receiving two or more of the above-mentioned FAIL discrettes from other GPC's or by the GPC's own software SYNC indicating a self-failure.

4.3.1 SYNC/GPC RM Failure Indicators. A failure detected by the hardware or software SYNC/RM scheme will be annunciated in one or more of the following ways: A Class 2 alarm which includes GPC x (x = GPC ID) fault messages, illumination of the MASTER ALARM lights on panels F2, F4, M042J and A7, illumination of the BACKUP C/W ALARM light on panel F7, the sounding of a C&W tone, the illumination of a light or lights on the GPC STATUS matrix on panel O1, the GPC light on panel F7, and illumination of a light or lights on the 120-light C&W matrix on panel R13. Also, a "↓" and M's may appear on the GNC SYSTEM SUMMARY displays and the GPC/BUS STATUS displays (if available).

4.3.1.1 GPC STATUS Matrix. The GPC STATUS matrix, located on panel O1, is a 5x5 matrix of lights used to annunciate the GPC status when a GPC has failed to SYNC with another GPC. Each nondiagonal element lighted represents one GPC's FAIL discrete (vote) for another GPC. For example, if GPC 1 sends a FAIL discrete to GPC 3, Element 1/3 will light (refer to figure 4-13). All of the lights that can illuminate as a result of one GPC voting against another are white in color. Those lights which would be illuminated due to GPC self-failure recognition are yellow in color, and they form the upper-left to lower-right diagonal. When a GPC lights its own diagonal as a result of either 2 or more GPC's voting against it or an internally detected failure, it will also automatically reset any FAIL discrettes it had sent to other GPC's. Thus, its non-diagonal row will be extinguished. The cross-hatched column of lights in figure 4-13 illustrates a GPC STATUS matrix indication if GPC 1 failed in a nominal ascent or entry configuration. If a GPC goes to software halt, it will, depending on the failure, light its diagonal light. All GPC's in the current and resultant redundant set will reset their fail votes at any OPS transition involving memory reconfiguration of any of the redundant set members. A GPC which is placed in STBY will attempt to reset its CAM diagonal element cyclically. Once again, if two other GPC's are still sending fail votes to that GPC, that attempt will be unsuccessful.

It is also possible to reset a GPC's fail vote discrete outputs as well as its I/O error log and sync history log via an item input (ERR LOG RESET - Item 48) to the GPC MEMORY display. This is not a common set wide item; i.e., Item 48 has to be done in every processing MF and to OPS 0 machines separately. (Any

GPC VOTER HARDWARE



*SELF FAIL VOTE DISABLES CAPABILITY TO SEND VOTES TO OTHER GPC'S
THERE ARE NO PASS ↔ BFS VOTES CAST OR REGISTERED ON THIS MATRIX

Figure 4-13. GPC Fail Votes Output

GPC which goes to software halt (as a result of crew station panel configuration, hardware detected problems, or BFS engage) should light its diagonal light.)

Note here that whenever a diagonal element on the GPC STATUS matrix is lit, the GPC light on the 40 light F7 C&W matrix will light.

4.3.1.2 120-Light Caution and Warning Matrix. There is a 120-light C&W matrix located on panel R13. Five of the elements on this matrix parallel the main diagonal elements (SELF-FAIL discrettes) of the GPC STATUS matrix. For example, Element 005 (the first two digits indicate the row, the last digit indicates the column) corresponds to the GPC 1 SELF-FAIL light (1/1) on the GPC STATUS matrix. Likewise, Element 015 corresponds to the 2/2 diagonal, 025 corresponds to the 3/3 diagonal, and so forth.

Indications on panel R13 become useful only when there would be a crewmember available to access this panel, since a manual change to the parameter-status toggle switch (to the "tripped" position) must be made in order to read these status lights.

4.3.2 Mechanization of Synchronization. SYNC is the software scheme used to ensure adequate intercomputer communication of GPC status, data and error information between PASS GPC's. Two types of GPC operations in which SYNC plays a part are common set and redundant set operations.

4.3.2.1 Common Set Operations. A common set is a set of PASS GPC's which cyclically exchange certain status information at a rate of 6.25 times per second over the ICC data buses at specified sync points. This exchanged status information includes the following:

- I/O errors
- Fault messages
- GPC STATUS matrix data
- DEU MAJOR FUNCTION switch settings
- GPC/CRT keyboard entries
- Current Central Processing Unit (CPU) duty cycle
- Resident MC
- Memory configuration table
- OPS overlay request
- Master Timing Unit (MTU) Time
- Internal GPC time

- System-level display information
- Network Signal Processor (NSP) read data (uplink)
- Memory Source Selection

The GPC's in the common set may be executing different applications software, as the on-orbit case in which GPC's executing GNC software and the GPC executing SM software will all be operating as members of the common set. Each PASS GPC attempts to join the common set when it is moded from HALT to STBY to RUN, or from STBY to RUN. Each GPC maintains an internal table of the other GPC's with which it has achieved common set sync (its common set sync set or common set mask). Except under GPC failure conditions, all active PASS GPC's will be members of the common set. As an example, during ascent, there are typically four GNC GPC's (1, 2, 3, 4) at the common set level, whereas, on orbit there are 2 or 3 GPC's at the common set level (GNC in 1, 2, SM in 4).

4.3.2.2 Redundant Set Operations. A redundant set is a set of two or more GPC's which are performing identical tasks using identical inputs and producing identical outputs. Therefore, except for the Instrumentation/PCMMU (IP) data bus, (each GPC is assigned a dedicated IP data bus) any bus assigned to a member of the redundant set will be listened to by all members of the redundant set. Thus, if GPC 1 commands String 1 and DK 1, all of the redundant set GPC's will receive the data transmitted over String 1 and DK 1, since they are listening on those buses.

The redundant set SYNC schemes ensure that the redundant set software processing is done simultaneously in all redundant set GPC's and also that all redundant set GPC's are receiving the requested data. This requirement ensures identical inputs to the redundant set GPC's and, if any redundant set GPC detects an error, no redundant set GPC will process the input data. Such an I/O transaction is called a "protected" transaction.

The above requirements result in sync being exchanged between the redundant set GPC's at a rate of 200 to 400 times per second (at redundant set sync points). Each GPC maintains a table of the other GPC's with which it will attempt to maintain redundant set sync (its redundant set sync set or redundant set mask). The Sync rate varies per MC (e.g. G2 sync rate is 309.8 times/sec).

Only GNC programs can be executed by a redundant set. An attempt to load an SM or PL MC into multiple GPC's will result in the generation of an ILLEGAL ENTRY fault message. The redundant set is formed automatically by systems software at specified OPS transitions and legal OPS/mode recalls. During ascent there are four GPC's (1, 2, 3, 4) at the redundant set level whereas on Orbit there are only two GPC's (1,2) in the redundant set, nominally.

4.3.2.3 Synchronization Operation. Each GPC is connected to the other four GPC's with a dedicated set of three discrete sync lines (refer to figure 4-14). Over such a set of discrete lines, each GPC periodically (as specified sync points) will broadcast a three-bit binary signal called a sync code. A GPC which is powered off is in STBY or HALT (according to the GPC MODE switch position), software HALT (internal failure of BFS-engage command), or is the BFS

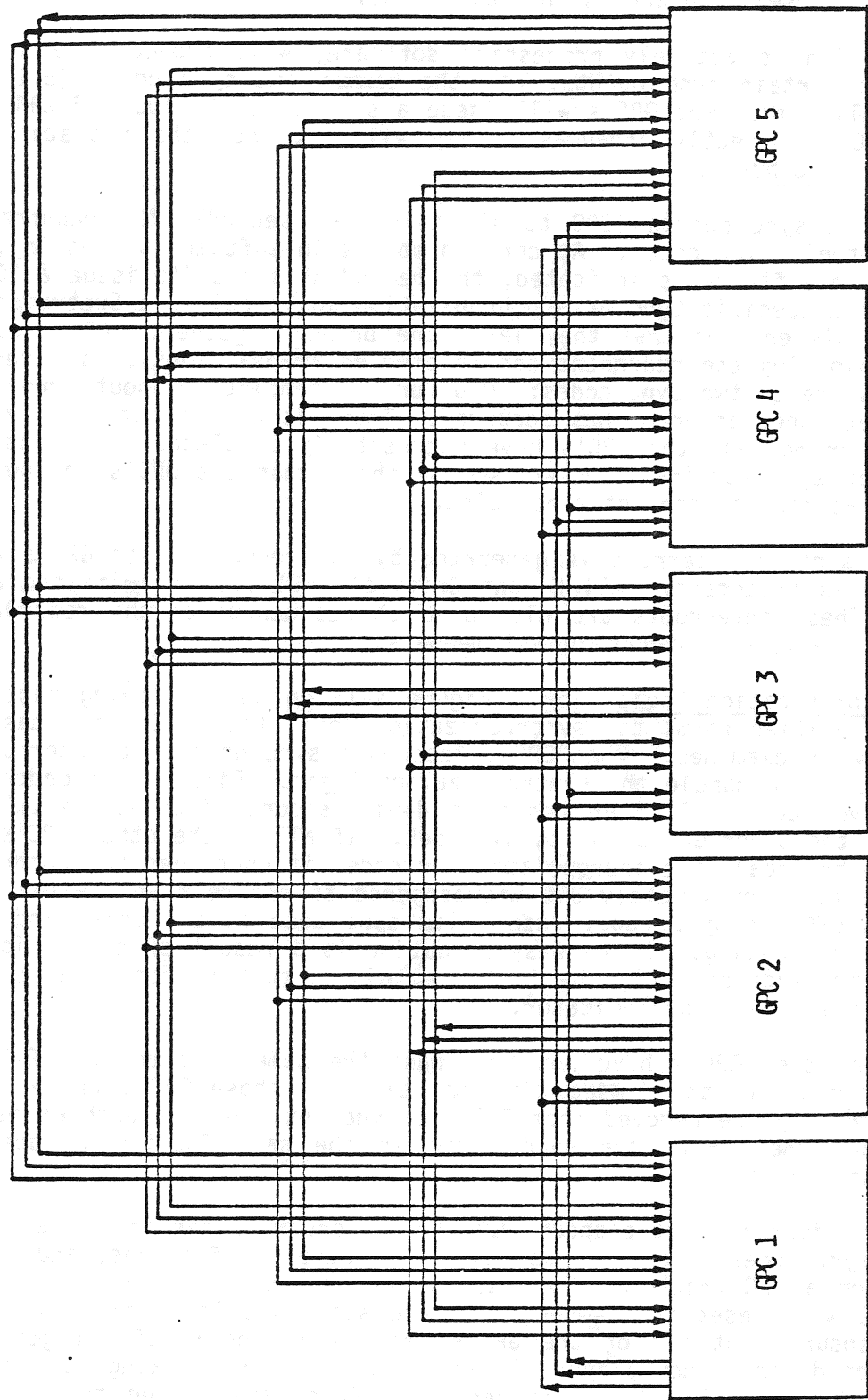


Figure 4-14. Discrete Sync Lines

GPC, will broadcast a sync code of 000. This 000 sync code will tell the other GPC's that the transmitting GPC is in STBY or HALT.

A PASS GPC, which is actively processing software, will broadcast a 111 sync code except at certain sync points. At the common set sync point (6.25 times per second), all common set GPC's will issue a sync code of 110. If all of the common set GPC's correctly broadcast, they will exchange their status information over the ICC buses.

At redundant set sync points (200 to 400 times per second), the redundant set GPC's compare their sync codes. At certain points in software processing, whenever a branch in software is indicated, the redundant set GPC's issue a 100 sync code and enter a specific type of synchronization logic called a Supervisor Call (SVC) sync. This ensures that they leave the branch together. After each I/O transaction involving the redundant set (protected transactions), each redundant set GPC issues one of two sync codes: 010 for I/O complete without error or 011 for I/O complete when an error has occurred. Thus, it can be immediately determined whether or not all the GPC's have successfully completed the transaction. This particular sync routine is also used by the common set GPC's following ICC data transfer at each common set sync point.

Periodically, another interrupt is generated by the redundant set GPC's and the sync code 101 is broadcast. All Flight Critical (FC) I/O is initiated at such interrupts. These interrupts are also used to resynchronize the redundant set following OPS overlays to redundant set members.

4.3.2.4 Synchronization Logic Flow. Figure 4-15 on the following page illustrates, in simplified form, the synchronization logic flow. In this case, GPC-1's logic flow is examined. When GPC-1 reaches a sync point, it interrupts its normal processing to handle the synchronization logic. First, it broadcasts the appropriate sync code. It then resets a 4-millisecond timer and examines the sync codes of the other GPC's in its sync set. If all of the other GPC's in its sync set have broadcast the appropriate sync code, it continues to broadcast its own sync code for approximately 300 microseconds to ensure that the other GPC's have detected GPC-1's sync code, resets its sync code to all ones, and returns to its normal processing. If this sync routine is a result of completion of an input/output transaction, only the first two digits must be identical since the third digit is an I/O error indicator.

If all of the other GPC's have not broadcast the same sync code, GPC-1 checks its 4-msec timer. If the 4-msec time has elapsed, those GPC's which have not responded correctly are removed from GPC 1's sync set, and the problem is annunciated. GPC-1 then exits the sync logic in the same fashion it does under nominal circumstances.

If the 4-msec timer had not elapsed, GPC-1 will check to see if it has received any correct sync codes since the last time it checked. If it has, and this sync code came from a GPC which had not issued its sync code before (in this logic cycle), GPC-1 will reset its 4-msec timer and start its logic flow cycle again. This is to ensure that all of the GPC's leave the sync routine together. If GPC-1 does not detect a new player, it will stay in this checking loop until its timer runs out or until all of the required GPC's have issued the appropriate

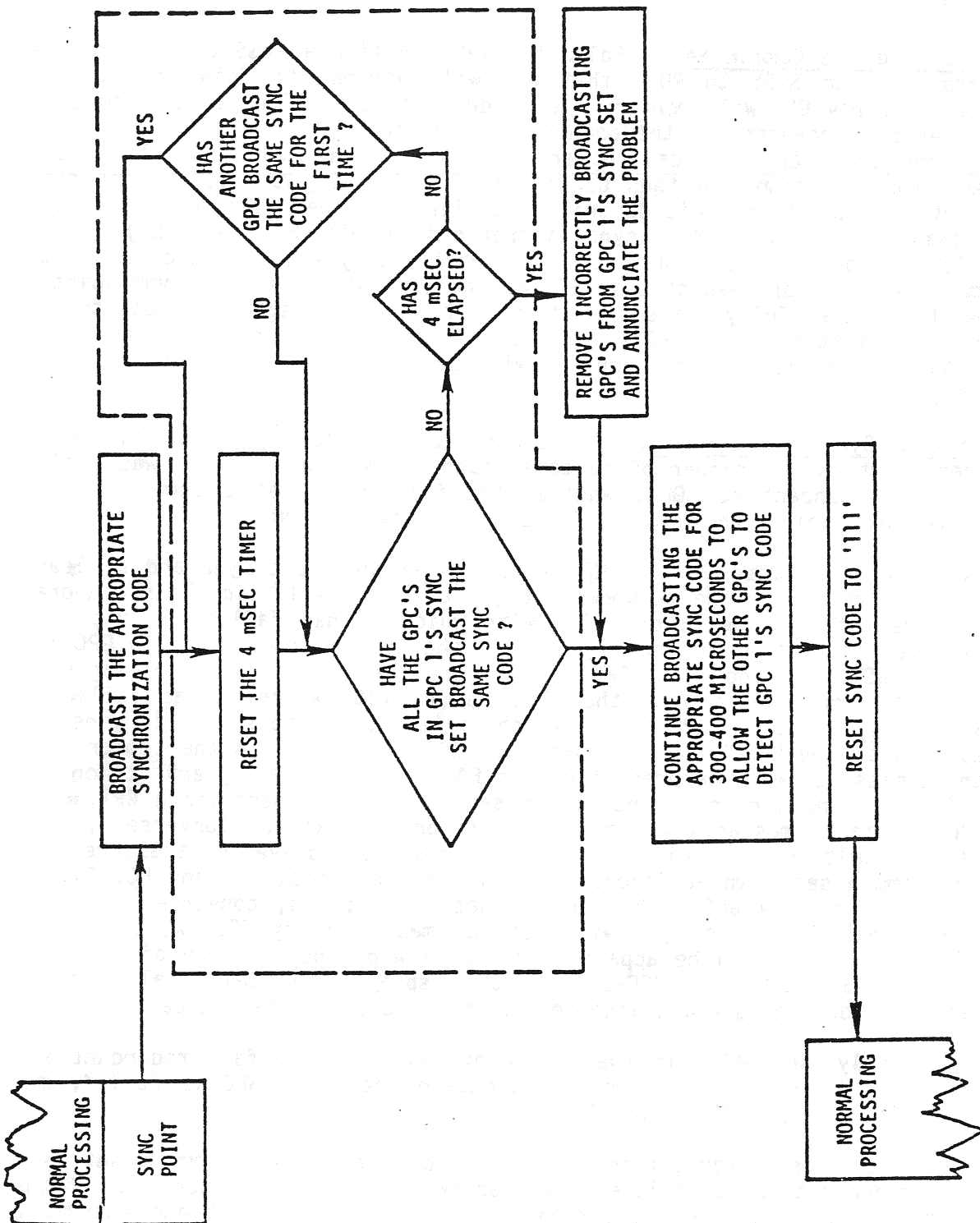


Figure 4-15. Simplified Sync Logic Flow for GPC 1

sync codes. At this time, GPC-1 will exit this sync logic flow and return to its normal processing.

4.3.2.5 Joining the Common Set. Following IPL, anytime a PASS GPC is transitioned from HALT to STBY to RUN, that GPC will attempt to join the current common set. The new GPC will monitor the other GPC's sync lines to determine if and when they are broadcasting the common set sync code. If it does not detect that the other GPC's are broadcasting the common set sync code, it will wait a prescribed amount of time and then begin also broadcasting the common set sync code and entering the sync logic described earlier. If the old common set GPC's note the change in another GPC's sync discrettes from 000 (HALT or STBY) to 111 (RUN) to 110 at consecutive common set sync points, they will add such a GPC to their common set sync and expect that GPC at the current and future sync points. If the new GPC successfully joins the common set, it will begin ICC data transfer with the old common set GPC's. If a GPC does not detect any other GPC broadcasting the common set sync code, it will begin operations as the initially powered GPC.

4.3.3 Fail to Sync Annunciation. The annunciation following a GPC failing to sync is dependent upon a number of factors, such as, whether the GPC was a simplex GPC or a redundant set GPC, whether the failure was at a common set or redundant set sync point, and which GPC's detected the problem.

The software logic ensures that if GPC X fails redundant set sync and at least two other GPC's remain in the redundant set, then GPC X will light its diagonal element on the GSM and the other GPC's with which it has failed to sync will send fail votes, resulting in the lighting of the appropriate lights in GPC X's column on the GSM. In addition, GPC X will generate Class 2 fault messages of the GPC N ↓ X format where N is the ID of a GPC with which it has failed to sync. Similarly, the other GPC's with which it has failed to sync will generate fault messages of the GPC X ↓ N format. If GPC X is still in the common set, all of these messages will be present on the FAULT page driven by any common set GPC. If GPC X is no longer in the common set and is still driving a CRT, only the GPC N ↓ X fault messages will be available on its CRT's. Conversely, only the GPC X ↓ N fault messages will be available on any CRT driven by a GPC remaining in the common set. In addition, GPC X will set bus masks on any FC, DK, or PL data bus driven by a GPC with which it has failed; and, conversely any GPC with which it has failed to sync will set bus masks on any FC, DK, or PL bus driven by GPC X. This will be apparent to the crew by the presence of "↓" and M's on the GNC SYS SUMM and GPC/BUS STATUS displays. If GPC X also failed common set sync, bus masks would also be set on the appropriate ICC data buses.

If there are only two GPC's in the redundant set and they fail redundant set sync, each will drive a fault message indicating the other GPC is failed, and each sends a fail vote to the other GPC.

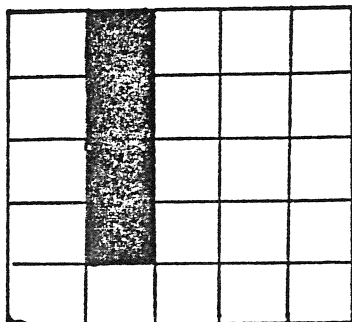
Thus, two kinds of synchronization levels may be present - a common set sync level and a redundant set sync level. The software is designed such that if the redundant set is the same as the common set (as it is in ascent and entry), a GPC which fails redundant set sync will automatically fail common set sync.

Also, if a GPC fails common set sync and is in the redundant set, it will also fail redundant set sync. If a GPC fails common set sync it cannot reestablish sync without going to HALT first.

Examples:

1 On ascent, with GPC's 1, 2, 3, 4 in the redundant set, GPC 2 fails to sync. GPC 2 will no longer be in the common set. This causes:

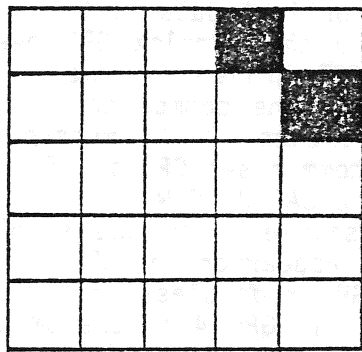
- GPC 1 ↓ 2, GC 3 ↓ 2, G PC 4 ↓ 2 on a CRT driven by GPC 2
- GPC 2 ↓ 1 3 4 on CRT driven by GPC 1, GPC 3 or GPC 2
- Lights 1/2, 2/2, 3/2, 4/2 on GSM and GPC light



- " ↓ " under GPC 2 on GNC SYS SUMM
- M's by LRU's lost by bus masking

2 On orbit, with GPC's 1 and 2 in GNC OPS 2, GPC 3 in STBY (freeze dried) GPC 4 in SM OPS 2, GPC's 1 and 2 fail redundant set sync, GPC's 1 and 2 are still in the common set sync. This causes

- GPC 1 ↓ 2, GPC 2 ↓ 1 fault messages
- Lights 1/2 and 2/1 on the GMS



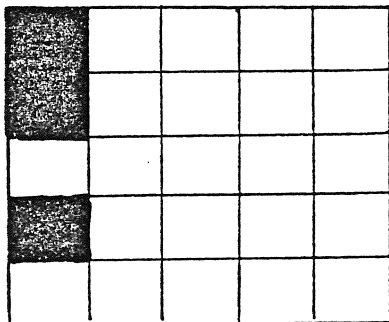
- M by LRU's lost due to bus masking

3 On Orbit, with GPC's 1 and 2 in GNC OPS 2, 3 freeze dried GPC 4 in SM OPS 2, GPC 1 fails common and redundant set sync. This causes:

- GPC 1 ↓ 2 4 fault messages on CRT driven by GPC 2 or 4
- GPC 2 ↓ 1, GPC 4 ↓ 1 fault messages on CRT driven by GPC 1

(Note, if GPC 1 failed completely, a big X would appear on a CRT formerly driven by GPC 1).

- Lights 1/1, 2/1, 4/1 on the GSM

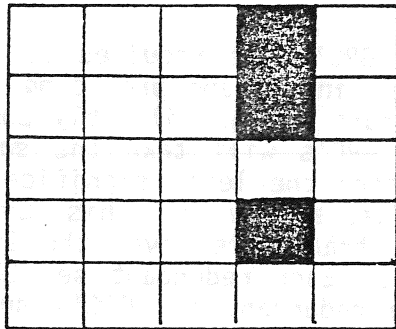


- M's by LRU's lost due to bus masking on GNC System Summary
- " ↓ " under GPC 1 on GNC SYS SUMM and GPC/BUS STATUS displays
- Also ↓'s on GPC/BUS STATUS display indicating bus masking

During Ascent and Entry, with four GPC's in the redundant set, if the set splits in a 2 on 2 manner, the fault annunciation will follow the same principles as described above; however, the annunciation on the GSM will be a function of IOP hardware signal timing.

If a simplex GPC fails common set sync, the ICC exchange between the GPC and the other GPC's cease. This means that if the simplex GPC is not in control of FC 1, 2, or 3, it will not receive MTU or NSP (uplink) data as this data was passed from the GPC's in control of those buses to the simplex GPC over ICC. Thus, information such as fault messages on a CRT driven by the simplex GPC will differ from that driven on a GPC remaining in the common set. The simplex GPC will drive the BACKUP C/W ALARM light and a Class 2 GPC message(s) on its CRT indicating it has disagreed with the other common set GPC's. Similarly, each of the remaining common set GPC's will drive the BACKUP C/W ALARM light and a Class 2 combined message indicating that they disagreed with the simplex GPC. If a GPC has lit its diagonal light, a " ↓ " will appear on the GPC/BUS STATUS and the GNC SYS SUMM 1 display under the simplex GPC regardless of which GPC was commanding the display. For example, on-orbit, if GPC 4 is the SM GPC and GPC's 1 and 2 form a GNC redundant set, failure of GPC 4 to sync with GPC's 1 and 2 will result in the following annunciation:

- Light 1/4, 2/4, and 4/4 on the GMS



- CLASS 2 ALARM (BACKUP C/W ALARM light, MASTER ALARM light/tone)
- GPC light on F7 C/W matrix
- On a CRT driven by GPC 4 - GPC 1 ↓ 4 fault message
GPC 2 ↓ 4 fault message
" ↓ " for GPC 4 on the GPC/BUS STATUS display and GNC Sys Summ 1
- On a CRT driven by GPC 1 or GPC 2 - GPC 4 12 fault message
" ↓ " for GPC 4 on the GNC SYS SUMM 1 and GPC/BUS STATUS displays

If GPC 4 failed hard in the above case, a big "X" would appear on any CRT formerly driven by GPC 4.

4.3.3.1 Force Fail To Sync. A GPC will force itself to fail to sync (both from the common set and the redundant set) by setting a non-zero static sync code under each of the following conditions:

- A redundant set GPC which has an I/O error when all the other redundant set GPC's have successfully completed the transaction will fail to sync the set upon the detection of a second consecutive error.
- After certain ICC data bus I/O errors (to be discussed in section 4.4.9.).
- If that GPC (but not all target GPC's) fails to correctly receive an OPS overlay after the retry options are exhausted, that GPC will fail to sync (from the redundant set only) and go to OPS 0.

A GPC which forces fail to sync continues to command on any data buses to which it was assigned and sets bus masks on any bus commanded by another GPC remaining in the common set.

4.3.3.2 Downlist GPC Impact. As discussed in section 4.2.5, if there are 3 or more GPC's in the redundant set and the downlist GPC fails to sync, a new downlist GPC will be selected. The new downlist GPC will be the lowest numbered GPC in the redundant set.

4.3.3.3 Sumword Comparison. The redundant set GPC's are required to execute identical software simultaneously, using identical inputs and producing identical outputs. Although the redundant set GPC outputs are not directly compared, the GNC applications software in each of these GPC's will take the sum of a specified set of critical output commands and store the least significant bits of this sum in a 64-bit double-precision word called a sumword. This sumword is passed to the systems software from which it is transferred over the ICC data buses to the other GPC's, 6.25 times per second. Each redundant set GPC then performs a bit-by-bit comparison of each of the redundant set GPC's sumwords. This operation is referred to as a sumword comparison.

Each RS GPC differences its sumword from the sumwords of every other RS GPC and logs a fault condition pass on other GPC's or on itself, based on sumword non-zero differences. The other criteria for logging self faults is that no other RS GPC can be matched to self's sumword. The logic contains transient filtering by requiring three consecutive fault condition passes before it is annunciated with a GPC Sum message. After the fault message generation against a particular GPC, the logic will not annunciate further mismatches by that GPC unless the sumwords have been detected to agree. Then, in order to fail again it will have to fail the three pass filter.

The Software also maintains a table of the cumulative number of fault condition passes logged against every GPC in the RS by each GPC of the RS. Each GPC's counters are transferred to the other GPC's no less than once per second. These parameters are available for downlist display. The cumulative counters are set to zero for new RS formation or by doing a manual Item 48 (Error Log Reset) via the GPC Memory display.

The sumword computed by the GNC applications program has an OPS-dependent composition. For example, the following items are included in the entry (Memory Configuration 3) sumword: OMS commands, inboard/outboard elevon commands, rudder, bodyflap and speed brake commands, and accelerometer assembly data. Also included in this sumword are the forward and aft vent commands, the Orbital Maneuvering System (OMS), Main Propulsion System (MPS), and Reaction Control System (RCS) commands, the Reaction Jet Driver Forward (RJDF) commands, and the Doppler Extractor data.

4.4 INPUT/OUTPUT MANAGEMENT

One of the responsibilities of systems software is the management of input and output operations. This function includes the assigning of GPC's as commanders and listeners on the data buses, and the logic involved in sending commands to these data buses at specified rates upon requests from the applications software. Furthermore, systems software I/O Management function includes the I/O error processing techniques and some special tests for certain failure conditions. This software will also provide failure annunciation to the ground and to the flight crew, should an I/O error be detected.

The I/O Management logic related to bus assignment and I/O error processing varies between the data bus groups. Therefore, these data bus groups and their associated I/O Management logic will be examined separately. Prior to doing this, however, some of the major concepts which are basic to the entire subject of I/O Management will be discussed.

4.4.1 I/O Transaction. An I/O transaction is an operation which is initiated by a software request for the initiation and the execution of a data transfer into or out of a GPC. This request can be based upon a request from the applications software or can come directly from the systems software. An I/O transaction may involve multiple data buses connected to multiple Bus Terminal Units (BTU's), each of which is connected to multiple sensors or effectors.

In order to maintain consistently identical inputs for the redundant set GPC's, input transactions involving these redundant set GPC's are protected. This means that either all of the redundant set GPC's correctly receive and process the input data, or they ignore the data. Following the detection of an input error, the transaction typically will be tried again in the next data cycle.

Special logic is incorporated to ensure that a faulty GPC cannot prevent the other redundant set GPC's from receiving necessary data. If a GPC in the redundant set is the only redundant set GPC to detect the same I/O error 2 consecutive times, the GPC will force fail to sync, and therefore, drop out of the redundant set.

The protected transaction capability is maintained through the use of synchronization codes and certain I/O error processing techniques. Prior to the I/O transaction execution, synchronization occurs to ensure time coincident sampling of data and that the GPC's are still together. Following an input transaction over the FC data buses, which involves the redundant set GPC's, a special sync code is issued by each of the involved GPC's: 010, if the transaction was completed without any errors, and 011 if an error was detected on the transaction. This ensures that the GPC's leave the I/O transaction together. Also, I/O errors are quickly discovered via the sync patterns which are called I/O Problem Report (IPR) sync codes. If one of the involved GPC's broadcasts the IPR sync code which indicates an I/O error, an ICC transaction is initiated in order to transfer information among the participating GPC's as to the specific source of the problem. This ICC transaction is also called an IPR. Thus, if any member of the redundant set detects an error during an I/O transaction, that information is exchanged among all of the redundant set GPC's. How this information is utilized is a subject which will be discussed in greater detail later on in this section.

While protected transactions are used primarily for redundant set transactions, there is also one case where the same philosophy is invoked: ICC transactions involving the common set. Here again, if one GPC in the common set detects an I/O error on an ICC transaction, this information will be revealed to the other common set GPC's using the appropriate IPR sync code, and no common set GPC will use the data that was received over the involved ICC bus.

4.4.2 Minor Cycle/Major Cycle. Within the software system there are certain high-rate cyclic processes which are critical to both the safety and the performance of the vehicle. The principle example of such applications software processing is that which relates to the GNC flight control and flight control-related operations. The period over which one cycle of these processes can be performed is called a minor cycle. It will be 40 msec in duration since the highest rate of cyclic processing used is 25 Hz.

A major cycle is a time period consisting of 24 minor cycles, during which a majority of the cyclic software processing is scheduled. Thus, a major cycle is of 960 msec in duration and is initiated at 1.04 Hz.

4.4.3 I/O Transaction Rates. Many commands and requests for data are sent to hardware devices at specified rates. These rates vary from once per minor cycle (25 Hz) to once every major cycle (1.04 Hz). Some examples are as follows:

- A. There is a transaction consisting of a set of flight control commands and requests for data which is sent over the FC data buses. This transaction, which is known as the GNC High Frequency Executive (HFE) transaction and which involves all eight of the FC data buses, includes requests for data from the Engine Interface Units (EIU's), Air Data Transducer Assemblies (ADTA's), the RCS, the MPS, and the OMS once every minor cycle (25 Hz).
- B. Since many navigation computations run at 6.25 Hz (every fourth minor cycle), data from many of the avionics sensors, such as the Inertial Measurement Units (IMU's), Tactical Air Command and Navigation System (TACAN), and the Radar Altimeters (RA's) are requested at this 6.25 Hz rate. These data requests are a part of the Mid Frequency Executive (MFE) transaction, which consists of the set of commands and data requests that are sent out over the eight FC data buses at 6.25 Hz.
- C. Once every minor cycle (25 Hz), each GPC, which is actively processing software, sends its downlist to the Pulse-Code Modulation Master Unit (PCMMU).
- D. Commands are sent to the MTU, for the current Greenwich Mean Time (GMT), Mission Elapsed Time (MET), and Built-In Test Equipment (BITE) status data, once every major cycle (1.04 Hz).

However, not all I/O transactions are cyclic in nature. Certain of these transactions are initiated only on a specific non-cyclic request from an applications or a systems software program.

4.4.4 MDM PROM Segment. An MDM has two modes of operations for both output and input. The modes are referred to as direct and indirect. In the direct output

mode, the MDM is sent one command word followed by 1 to 32 command data words. The direct mode for input consists of one command word from the GPC, initiating the transmission of one to 32 NON-BITE (1-64 BITE) MDM response data words.

The indirect mode allows more than 32 words of information to be sent to or received from the Shuttle subsystem as a result of the issuance of a single command word from the IOP. This technique involves the use of a Programmable Read Only Memory (PROM) hardware sequence in the MDM. The content of the PROM is alterable as a result of wired changes. Once the PROM is mounted in the MDM and vehicle, the contents are not alterable.

Each PROM consists of a number of fixed programs called PROM segments. Each program consists of a number of words (up to 32). When a command is sent to the MDM, it will specify whether the PROM is to be used (indirect mode). It also specifies at which point in the PROM (program) to start as well as the number of consecutive PROM instructions to be executed. Note also that the PROM in an MDM can be used for both output (from the GPC/MDM to Shuttle subsystems) and inputs (from the Shuttle subsystem to the GPC/MDM). A given PROM segment, however, is used solely for inputs or outputs - not both. An input PROM stored in MDM FF1 is shown in table 4-5.

4.4.5 Bus Control Element (BCE) Chain. An I/O transaction thus consists of the acquisition of groups of subsystem data from one or more BTU's.

A BCE chain is a sequential set of software instructions in the IOP, each of which accesses a group of subsystem data from one or more BTU's, which is initiated through a single BCE and, thus, through a single data bus. These groups are segregated in the transaction according to data type. Thus, Analog Input Single-Ended (AIS) data, Discrete Input High (DIH) data, etc., are brought into the computer grouped together into elements. These elements are requested by a technique known as BCE chaining, in which individual data requests for the AIS, DIH, etc. data types are grouped together into a single transaction. Since the requests are grouped together, the data responses or elements likewise are grouped together.

Each of the software instructions and the acquired subsystem data in a BCE chain is called a BCE chain element or, more simply, a BCE element. The associated subsystem data may include an MDM return word (discussed in the next section), a segment of an MDM PROM, MDM stored data associated with an external device or data from an individual BTU (such as an EIU). For example, at 6.25 Hz, the following BCE chain may be initiated over FC1 (BCE 20) by each GNC GPC.

TABLE 4-5
FF INPUT PROM

PROM segment	Description of input	Frequency	Word count
1	RCS tank temp/press RCS manf. press	6.15 Hz	6 2
2	Discrettes	6.25 Hz/ 25 Hz	13
3	RSC thrust inj. temp.	25 Hz	8
4	LH RHC CMDS LH RPTA CMD LH SBTC CMD AFT RCH CMDS	25 Hz	3 1 1 3
5	DUMMY INPUT (STS-1)	25 Hz	5
6	Lateral acc'm Normal acc'm	25 Hz	1 1

An I/O transaction may involve several BCE chains. For example, the MFE transaction (6.25 Hz) discussed earlier in section 4.4.3, is composed of eight BCE chains (one for each of the FCE data buses 1 through 8).

Through the use of certain validity checks (performed by the IOP's Multiplexer Interface Adapter (MIA), BCE, and the I/O error processing logic in the systems software), a problem with a BCE chain may be identified as an error from a specific element of the BCE chain or from the involved MDM/databus. Currently, BCE chains have been identified for the FC and PL data buses as presented in Appendix C.

4.4.5.1 MDM Return Word. The first element of certain BCE chains is called an MDM Return Word. This word is used to determine whether or not the MDM is capable of communicating and is used by the I/O error processing logic to determine whether or not an I/O error is the result of an MDM failure or a particular BCE chain element failure.

If there are multiple BCE chains associated with a BCE and an MDM, the BCE chain which has the highest frequency will have the MDM Return Word as its first element. The philosophy here is that if the MDM Return Word is correct (which indicates that the MDM is still communicating with the GPC) on the highest frequency transaction, it would also be correct for the lower frequency transactions. For example, tables 4-6 and 4-7 both show input transactions through BCE 20 (FC1), but the MDM Return word is only on the faster (HFE) transaction.

TABLE 4-6

MFE INPUT TRANSACTION for BCE 20 Ø (FC1)

BCE element	Request for data from:
31	FF1 PROM segment 1, 2
32	IMU 1
33	TAC/RA 1
34	MSBLS 1
35	STU 1 (-z Star tracker)

4.4.5.2 BCE Element Bypass. A BCE chain is composed of multiple BCE elements which relate to multiple hardware line replaceable units (LRU's) and which usually involve at least one BTU/MDM. Special I/O error processing logic is invoked to determine if a detected problem is a result of a GPC, a BTU/MDM, or an individual hardware item (LRU) problem. If, as a result of this I/O error processing logic, the GPC is determined to be at fault, that GPC may be forced to fail to sync. This topic will be discussed in greater detail later in this section.

If the problem is at the BTU/MDM level (as detected by an incorrect or absent MDM return word), the problem will be downlisted and annunciated and no further

I/O transactions would be attempted involving that BTU/MDM port. This action is called a BTU segment bypass. If the problem existed with FF MDM 1, for example, a Class 3 alarm would be generated along with the fault message I/O ERROR FF 1. Also, additional information concerning this failure will be displayed on the current GNC SYS SUMM 1 display and the GPC/BUS STATUS display, if available.

If the problem is determined to be at the individual LRU level (BCE element level), the problem will be annunciated by a Class 3 alarm and fault message. The fault message will indicate whether the bypass was on a PL or FC chain. If the problem is on a FC chain, the string and element will be identified in the message. The problem will also be downlisted and that BCE element will be bypassed on subsequent transactions. An appropriate time delay will be inserted in the chain to replace that particular request for data.

For example, in the HFE transaction, the BCE chain being executed for BCE 20 attached to FC 1 is illustrated in table 4-7.

TABLE 4-7
FC1 HFE TRANSACTION

BCE element #	Request for data from:	BCE element #	Request for data from
7	FF1 RTN WD	7	FF1 RTN WORD
8	PL/SNSR	8	PL/SENSR
9	ADTA 1	9	DELAY
10	FF1 PROM SEG 2-6	10	FF1 PROM SEG 2-6
BEFORE BYPASS		AFTER BYPASS	

If ADTA 1 fails and does not respond to the BCE 9 request for data (two consecutive times to insure that it is not just a transient problem), then that element will be bypassed and a time delay substituted for that request for data (as illustrated in table 4-7). The Class 3 fault message BCE STRG 1 ADTA will be generated.

4.4.6 Bus Masking. Bus masking is a software controlled technique which results in a GPC terminating its command and listen mode on a given data bus. It is used when a bus is no longer controlled by a GPC within the GPC set (i.e., common set or redundant set) performing the transaction. For example, if on Ascent, GPC 3 fails to sync with GPC's 1, 2, and 4 (assuming the nominal string assignment on Ascent), then GPC's 1, 2 and 4 will mask FC buses 3 and 7 (String 3) which are commanded by GPC 3. Similarly, if GPC 3 is still processing software, it will mask FC 1, 2, 4, 5, 6, and 8 buses (Strings 1, 2, and 4) which are commanded by GPC's 1, 2, and 4, respectively.

Bus masks of this type will be reset following a GPC being moded from HALT or STANDBY to RUN, following an OPS transition (which involves memory reconfiguration or redundant set formation), or following a legal OPS/mode recall in which memory reconfiguration or string reassignment is performed. Thus, in the previous example, if String 3 was reassigned to GPC 2 with an OPS/mode recall, GPC's 1, 2, and 4 would remove their bus masks on FC 3 and 7 (String 3).

When the BFS GPC is engaged, the PASS GPC's go to a state of SOFTWARE HALT. If an attempt is made to reinitialize a PASS GPC (via a new IPL sequence), that PASS GPC will set bus masks on all of the data buses being used by the BFS GPC (FC, PL, and DK buses). These bus masks will be removed following recognition by the PASS GPC of the BFS DISENGAGE condition. This ensures that the newly IPL'd PASS GPC does not interfere with the data buses until the BFS is disengaged.

Also, bus masks are normally set by systems software when a GPC is required neither to transmit nor receive data on a particular data bus. For example, the GNC GPC's will set masks on the PL data buses during the orbital flight phase when the PL buses are assigned to the SM GPC.

There is no special fault annunciation associated with the bus masking except, in some cases, the use of "↓" 's on the GPC/BUS STATUS and GNC SYS SUMM 1 displays and M's on other displays to indicate missing data.

4.4.7 I/O Error Handling

4.4.7.1 General Description. The I/O error handling logic is designed to detect data transmission errors. It is not designed to determine any other data validity. Data validity determination is the responsibility of the application software.

The specific way that I/O errors are handled is dependent on the type of data bus involved. Some similar concepts exist, and they will be discussed here. In general, only input errors are detected and annunciated directly by the systems software. The exception is with the output of the GPC downlist to the PCMMU over the IP data buses.

For protected-input transactions, the general logic is as follows: The IPR report from all of the redundant set GPC's are compared per bus. If only one GPC detects the same I/O error two consecutive times, it will force fail to sync (both the common set sync and the redundant set sync) with the other GPC's. If more than one GPC detects a particular I/O error two consecutive times, each GPC will perform the BTU segment of BCE element bypass as required.

For non-protected transactions (transactions for a simplex GPC), no special logic is necessary to determine which GPC is responsible for detecting the error. Following two consecutive errors of a particular type, the GPC will do either a BTU segment or a BCE element bypass, depending on the nature of the problem.

Special I/O error handling checks exist to protect against certain hardware states and failures. For example, a specific test is made, following any I/O

error, to insure that only the assigned command GPC has its transmitters enabled. If another GPC's transmitter is detected to be ON, that GPC will go to software halt. A special test is also made following any I/O error to determine if the BFS had been engaged (the switches which determine the BFS engage condition are monitored at a once-per-second rate). If the BFS has been engaged, the PASS GPC's will go to software halt.

4.3.7.2 General Annunciation. I/O errors on any of the seven groups of data buses will initiate Class 3 alarms. This means that, along with a fault message, the blue SM ALERT light will be generated. The fault message will be one of two forms: I/O ERROR ABC if the error is attributable to a BTU (ABC refers to which BTU is at fault, such as FF 1, PL 1, MMU, etc.), or BCE ----- if the problem results in a BCE element bypass on a string or the PL data buses. Furthermore, the fault message will indicate which GPC's detected the problem and at what time (MET) the problem was detected. For example, the fault message:

I/O ERROR FF 1 1 2 3 4 05:01:00

indicates that GPC's 1, 2, 3, and 4 each detected a problem with MDM FF1 at 05:01:00 MET.

4.4.7.3 Error Logging For Downlist Purposes. The systems software in each PASS GPC will log any I/O error in a memory stack which will contain the latest five I/O errors. The total number of I/O errors detected by a GPC will be maintained by a counter. At common set sync, the latest I/O error, its timetag, and the cumulative number of all I/O errors will be exchanged between the GPC's over the ICC data buses. Each GPC then, will make available for downlist, its own 5-deep log of I/O errors, each common set GPC's last I/O error, and each GPC's I/O error cumulative counter. In addition, the first five I/O errors following clearing of the Fault Summary Page (SPEC 99 PRO) are maintained for diagnostic purposes but are not normally available to downlist.

4.4.7.4 Commfault. The systems software provides status information on I/O errors called communications fault (commfault) indicators to the appropriate applications (GNC, SM, PL) software. It is then the responsibility of the application software to determine whether or not to use this data. Typically, such data will be flagged as missing, and an M will appear on the appropriate display.

Commfault indicators are set as the result of bus masking, BCE element bypasses, and BTU segment bypasses. The logic involved is as follows: When an I/O error is detected on a BCE chain by any GPC, the data on the entire chain is flagged as invalid (commfaulted) for the applications software. On subsequent transactions, if the problem is isolated, only the faulty element(s) is flagged as invalid. In a similar way, if a bus mask is set, all BCE elements and data associated with that bus are indicated via commfault as being in error.

4.4.7.5 Resetting I/O Error Indications. The BCE chains and error counters associated with the I/O error processing logic are reset by the appropriate GPC's under the following conditions:

- OPS transitions and OPS/mode recalls involving memory reconfiguration or new redundant set formation, and OPS/mode recalls involving bus reassignments, will reset all counters to zero and reset the BCE chains to their nominal configurations.
- A keyboard entry of I/O RESET EXEC will reset the counters and BCE chains in all of the GPC's listening to that particular keyboard.
- If a string or PL bus is moded from one port to another, all counters will be zeroed, but only the BCE chains associated with the moded strings or buses will be reset.
- Reassigning a CRT to a new GPC via GPC/CRT key input will reset the appropriate counter (and I/O error) for that DK Bus.
- On the IP data buses, a single good data cycle resets the counters.
- Moding a GPC from HALT to RUN or STANDBY to RUN will reset the counters and BCE chains in that GPC.
- Item 48 on the GPC MEMORY SPEC causes reset of the error logs (first five and last five entries), as well as the GPC STATUS matrix and the sync history log (trace).

4.4.8 Flight Critical (FC) Data Buses. The first GPC to complete an IPL will assume command of all eight FC data buses. This setup remains in effect until the first OPS transition to an MC where the strings would normally be reassigned. Following an OPS transition to an MC which supports string to GPC assignments, a nominal bus assignment table is used to determine the commanding GPC for each string. This table originally contains I-loaded values for each MC which can be observed at any time by the crew via the GPC MEMORY display. The observation and modification of these tables was discussed in sections 4.2.7 and 4.2.8.

With one exception, there is no automatic way to reassign the strings other than at certain OPS transitions or OPS/mode recalls. Only in the case of a redundant set of GPC's, which is moded to OPS 0 via an OPS 000 PRO keyboard entry, will the strings be automatically reassigned to the lowest numbered GPC in that set. Therefore, with that case excluded, if a GPC fails, the string(s) that GPC commanded cannot be reassigned to another GPC until an OPS transition or an OPS/mode recall in that major function.

Note that it is possible to assign multiple strings to a single GPC. No matter how many GPC's are available, all strings should be assigned to a GPC. Optimally, each string would be assigned to a different GPC. Thus, during ascent or entry when there are 4 GNC GPC's, if a GPC failed, at most one string would be lost; the attached sensors and effectors would receive, at most, one set of erroneous data from the failed GPC. However, there are certain cases, such as on-orbit, where there are only two GNC GPC's and where each string will be assigned to a GPC. Typically GPC 1 will command Strings 1 and 4, and GPC 2 will command Strings 2 and 3. It is customary to split up the IMU's and NSP's if possible. This is sometimes referred to as balancing the strings. The current string assignments for the common set GPC's will be indicated on the GPC/BUS STATUS display (available all OPS except GNC OPS 1, 3, 6).

4.4.8.1 String Moding. As mentioned earlier, each of the FA and FF MDM's has dual ports. Only one port of an MDM may be active at any one time. When only the primary (number 1) ports are accessed, the string which interfaces with those MDM's is said to be in the primary mode. When only the secondary (number 2) ports are being accessed, the string is said to be in the secondary mode. This concept of primary and secondary modes is a software restriction (not a hardware limitation), which pertains to the FF and FA MDM's and also to the PL MDM's. Thus, regardless of whether a string is in the primary or secondary mode, the commands to the other BTU's on the string Display Driver Units (DDU's), EIU's, Master Events Controllers (MEC's) are not affected.

Initially, all of the strings will be in the primary mode. However, following certain types of failures, it is possible in any OPS (except GNC OPS 1, 3, 6) to mode an individual string to the secondary mode (or back to the primary mode) through the use of Items 15-22 on the DPS UTILITY display. In OPS 1 and 6, port moding may be done via GPC read/write via an uplinked DEU equivalent. These changes take effect immediately. Execution of these item numbers includes an automatic I/O RESET.

4.4.8.2 I/O Error Handling. All of the I/O transactions involving the FC data buses are implemented using the BCE chain concept described earlier. Thus, the I/O error handling functions involved with FC bus transactions include BCE element bypasses and BTU segment bypasses. Also, status indicators in the form of down-arrows (↓) will appear in the appropriate locations on the GPC/BUS STATUS display beside the involved FF or FA MDM if a BTU segment bypass has occurred. No " ↓ " will appear for a BCE element bypass. In the same way, on the GNC .SYS SUMM 1 display, a " ↓ " will appear under the appropriate FF or FA MDM in order to indicate which MDM was at fault. In addition, for either BCE element bypasses or BTU segment bypasses, M's may appear in other portions of this display and others to indicate missing data.

4.4.9 Intercomputer Communication (ICC or IC) Data Buses. There are five unidirectional ICC data buses - one for each GPC to transmit messages to the other GPC's. (All other data buses carry data both to and from the GPC.) Any transmissions over these data buses are processed only by the common set GPC's. Therefore the BFS GPC will not process data received over the ICC data buses and will also not transmit information over its own ICC bus.

The ICC bus traffic includes the assorted GPC status information necessary to keep the common set GPC's running together. Such information as OPS overlay requests, GPC/CRT assignment, the MAJ FUNC switch setting on each DEU, and the current fault messages are exchanged. Also, the MTU time, uplink data, and the current vehicle state vector are sent to the SM GPC on-orbit. In order to maintain the redundant set, SUMWORDS are exchanged over ICC as well as I/O errors as they are detected (IPR).

As mentioned earlier, all transactions involving the ICC buses are protected. If an I/O error is detected by any involved GPC, that error will be indicated to the other GPC's via the appropriate IPR sync code. The transaction is automatically retried, and the exchanged data over the ICC buses will include the error status from the previous transaction. The general logic which is then invoked is as follows:

- If a single GPC detects an error over an ICC bus, that GPC will be presumed in error and will force fail to sync.
- If multiple GPC's report an error over a particular ICC bus, the commanding GPC for that bus will be assumed at fault, and will force fail to sync.
- If multiple GPC's report ICC errors with no agreement on the buses, all such GPC's will force fail to sync.

In any of the above cases, there will be the Class 2 alarm (section 4.3.3.) and annunciation associated with a GPC's failure to sync. This problem will also be logged in the GPC error log.

4.4.10 Mass Memory (MM) Data Buses. There are two identical Mass Memory Units (MMU's) connected to the GPC's via two MM data buses. The assignment of these MM buses is dependent upon a number of factors. In most cases, only one MMU and its MM data bus will be assigned to respond to commands from a GPC in a specific major function. These assignments can be controlled by the flight crew or the ground via Items 1-6 on the DPS UTILITY display.

The MASS MEMORY READ/WRITE display which is the OPS display in the Payload major function (PL OPS 9) and a SPEC display in SM OPS 2 allows access to either of the MMU's by either the PL OPS 9 GPC or by the SM OPS 2 GPC. Recall that Items 7 and 8 on the DPS UTILITY display refer to the assignment of an MMU to an OPS 0 GPC for such functions as retrieving the DEU initialization logic from the MMU following a GPC IPL. Note that Items 1 and 2, 3 and 4, 5 and 6, 7 and 8 on the DPS UTILITY display are mutually exclusive.

Thus, which MMU is to be used by a given major function and which GPC in the major function will command a specific MM bus is determined by one of two factors. During a GPC-to-GPC overlay, the source GPC for that overlay will automatically assume command of that MM data bus. In the other kinds of transactions involving the MM buses, the command GPC is determined by a nominal bus assignment table which specifies, per MC, which GPC will command an MM bus. This table may be observed and modified via Item 1, 18, and 19 on the GPC MEMORY display. Also, there is an automatic MM bus switching capability should I/O or checksum errors be encountered during MMU access for a memory reconfiguration.

4.4.10.1 I/O Error Handling. All MMU transactions are protected. A single occurrence of a checksum or I/O error during an MMU transaction which does not involve GPC memory reconfiguration causes a Class 3 alarm and annunciation and an I/O ERROR MMU fault message. As in all protected transactions, the software in each of the members of the GPC set will reject the transaction. In this case, the transaction will not be retried automatically.

I/O error handling during memory reconfiguration involves the following: Upon the detection of an I/O error (by any participating GPC) on one data bus, the transaction will be automatically retried on the same data bus. If the error is detected again, a Class 3 alarm and fault message I/O ERROR MMU will be generated. The transaction will be automatically retried on the other MM bus. If the error occurs again, the transaction will once again be retried. If any GPC

still detects the error, the I/O ERROR MMU fault message will again be generated and the GPC detecting the error will force fail to sync and go to OPS 0.

4.4.11 Payload (PL) Data Buses. There are two PL data buses, PL 1 and PL 2, each of which is attached to all five GPC's and to a port in each of the two PL MDM's (PL 1 and PL 2). For later flights, a third PL MDM may be added to the PL 1 and PL 2 data buses, and a PAYLOAD DATA INTERLEAVER (PDI) may be added to the PL 1 data bus. The type of data transferred through the PL MDM's include commands concerning the PL Bay Doors, fuel cell purges, the antenna management system and the PL and SM C&W. Data from PL test articles and experiments may also be accessed through the PL data buses. Note here that the PL MDM's are also referred to as PF1 and PF2 in some documentation.

4.4.11.1 PL MDM Port Moding. As was the case for the FC MDM's, each of the PL MDM's is a dual port device. Note that PL data bus 1 is attached to the number 1 port in both of the PL MDM's, and PL2 is attached to the number 2 port in both the PL1 and PL2 MDM's (figure 2-5). As before, only one port of an MDM may be accessed at a time, and the systems software in the GPC's is designed such that this restriction is not violated. Thus, the PL MDM's may be accessed in one of two modes - primary or secondary. In the primary mode, Port 1 of MDM PL1 is accessed via the PL1 data bus, and port 2 of MDM PL2 is accessed by the PL2 bus. In the secondary mode, Port 2 of MDM PL1 is accessed by the PL2 data bus and port 1 of MDM PL2 is accessed by the PL1 bus. As with the strings, the PL MDM's will initially be operating in the primary mode. There is a capability using Items 23 and 24 on the DPS UTILITY display to select which mode is used. However, the uplink capability to mode the PL MDM's is not currently approved during GNC OPS 1, 3, and 6.

4.4.11.2 I/O Error Handling. As with the FC MDM's, BCE chains will be used for I/O transactions on the PL data buses. Upon two consecutive I/O errors with a PL BCE element, a Class 3 alarm and fault message BCE PL will be generated. There also is a PL MDM Return Word. If two consecutive I/O errors are detected with a Payload MDM Return Word, a Class 3 alarm and a fault message will be generated. The fault message will be of the I/O ERROR ABC type, where ABC will read either PL1 or PL2, depending upon which MDM caused the problem. Also, a " ↓ " will appear on the GPC/BUS STATUS display under the detecting GPC in the PL row.

4.4.12 Display Electronics Unit/Keyboard (DK) Data Bus I/O Management. There are four DK data buses (one for each DEU) connected to each of the five GPC's.

A GPC in command of a particular DK data bus polls the DEU attached to that DK bus twice every major cycle. In this way, the GPC can keep track of the current MAJ FUNC switch setting of that DEU. Changes in that switch setting may result in the change of commanders on that DK bus.

The DK data buses are assigned to GPC's according to a hierarchy based upon several factors: the MAJ FUNC switch position, the nominal bus assignment table, GPC/CRT keyboard input, the BFC DISPLAY/SELECT switches, and the moding of the BFS.

The assignment of CRT's (DK buses) to the BFS GPC will be discussed in section 5. However, in summary, if the BFS GPC is moded from HALT to STBY or RUN, it will begin commanding a CRT/DK 4 whether or not the PASS is commanding on that bus. If the BFC DISPLAY switch is ON, the BFS GPC will command on the first indicated CRT if it is not engaged, and on both indicated CRT's if it is engaged. If the BFC DISPLAY switch is OFF, the BFS GPC takes no forward CRT if it is not engaged, and CRT's 1 and 2 if the BFS is engaged. The GPC/CRT key can also be used to assign a CRT to the BFS GPC via either a PASS or BFS controlled keyboard. User care must be taken to insure that no multiple commanders on a DK bus occur. Pre-engaged, the BFS GPC listens to PASS-controlled DK buses to acquire major mode transitions and certain display data. However, the PASS never listens to BFS controlled keyboards or DK buses. Thus, the PASS may not be assigned a CRT via a BFS controlled keyboard.

For the PASS, the MAJ FUNC switch is used in connection with the Nominal Bus Assignment Table (NBAT), which is MC dependent, to specify which PASS GPC will command a given CRT. If the switch-selected major function is supported by only one PASS GPC, that GPC will receive command of the CRT regardless of the NBAT assignment, with the exceptions which are described below. If the switch-selected major function is supported by a redundant set, then the NBAT should specify which GPC in the redundant set will command the CRT. However, if the NBAT-specified GPC is not in the redundant set, or if the NBAT GPC ID is 0 (with the exceptions described below), the involved DEU will be assigned to the lowest numbered GPC in the redundant set, and these new assignments will be reflected in the NBAT. If the GPC MEMORY display is currently displaying that memory configuration, it will not change until the next time that MC is called (ITEM 1+X EXEC). If the switch-selected major function is not supported by any member of the common set, no change in CRT commanders will occur; however, the OPS 0 display will appear. The exceptions to the above are as follows:

- A. Only three DK buses may be assigned at any time to the common set. An attempt to assign a fourth DEU to the common set will result in a Class 3 alarm and fault message > 3 DEU. Unlike the PASS, the BFS can control all four DEU's at the same time.
- B. If a DEU currently has no commander in the common set and an OPS transition is requested, then no matter what is specified in the NBAT no GPC in the common set will attempt to command that DEU following the OPS transition. In other words, DEU's not commanded by a GPC in the common set can only be acquired via GPC/CRT key input to a commanded keyboard.

The above Major Function switch logic is initiated at OPS transitions and following GPC/CRT key input, as well as when a DEU poll response indicates a change in MAJ FUNC switch setting.

The GPC/CRT key is also used to reassign CRT's (DK buses) among the PASS GPC's. Following a GPC/CRT input, the software automatically will transfer control of the CRT to the requested GPC. No check is made by the former commander's software to see if the newly assigned GPC is in the common set or in a matching major function. Also, no check is made to ensure against multiple command GPC's on the same DK bus if control handover of a CRT is requested which has a current commander not in the common set. However, if the newly assigned GPC is not in

the indicated major function, and another GPC in the common set is, it will immediately give control to the GPC supporting that major function. The GPC/CRT key is also used to make BFS DK bus assignment changes as described in section 5.2.5.

Multiple commanders on a CRT will be readily apparent to the user as two CRT background formats will be loaded and the DEU will flash. If this happens you usually turn the BF CRT SW off, cycle the CRT PWR, turn the BFC CRT SW on, and reselect the CRT.

It is also the case that the first running GPC will assume control DK buses 1, 2, and 3. When the first memory configuration is loaded (following an OPS request), the logic described above will be invoked. Finally, any PASS GPC moded from HALT or STBY to RUN will automatically take control of any uncommanded DK buses, as in the case of activating the freeze-dry GPC or the recovery from a GPC failed with all CRT's assigned.

4.4.12.1 I/O Error Handling. If a DEU is assigned to an redundant set GPC, all of the members of the redundant set will listen on that DK data bus, and all the transactions on that bus will be protected. When an I/O error is detected by any GPC on that data bus, all the participating GPC's will ignore the input. After one I/O error is detected on a DK bus, the Class 3 alarm and the fault message I/O ERROR CRT X will be generated (where X indicates on which DK bus the problem was detected). Also a "*" or "↓" will appear on the GPC/BUS STATUS display by the appropriate DK (CRT) bus and under the detecting GPC(s).

Since transactions involving the redundant set are protected, if only one redundant set GPC detects an I/O error on a DK bus transaction, that GPC will force fail to sync with the corresponding annunciation.

4.4.13 Instrumentation/PCMMU (IP) Data Bus I/O Management. Each GPC is assigned a dedicated IP data bus which connects that GPC with each of the two PCMMU's. Over these IP data buses, each active GPC sends its downlist to the active PCMMU. Also, the SM GPC accesses certain instrumentation and systems data through the active PCMMU over its IP data bus. Note that each IP data bus is hardwired to both PCMMU's, but only one PCMMU may be powered-up (active) at any one time. I/O error annunciation exists for the IP data buses if a GPC detects an error in the downlist transaction. If two consecutive errors are detected, a Class 3 alarm will be annunciated, and the fault message I/O ERROR PCM will be generated. The detecting GPC will continue sending its downlist data to the PCMMU after this problem has been annunciated. Also, the SM applications software will drive the Class 3 I/O ERROR PCM message following three consecutive input errors detected on its IP data bus. The SM GPC performs some logic to determine which parameters are missing and flags these with M's. It continues to retry IP transactions. The M's are removed upon a good parameter sample. The I/O error count is not removed until a single error-free data cycle is received.

4.4.14 Launch Data Bus (LDB) I/O Management. There are two Launch/Boost (LB) data buses (LDB's), each of which is connected to all five GPC's. They are primarily used for ground checkout and launch phase activities. In particular, there is an interface with the GSE launch processing subsystem through both LDB

data buses. The Launch Forward (LF) and Launch Aft (LA) MDM's, also known as the command decoder MDM's, are connected to these LDB buses, and are used only during the preflight (and possibly during the postflight) phases for checkout of various Orbiter systems. There is also an interface with the left and right Solid Rocket Boosters (SRB's) for obtaining certain data which are incorporated into the downlist. The LL and LR MDM's (in the left and right SRB's, respectively) are used for this function prior to SRB separation. In addition, LDB 1 is attached to the Manipulator Controller Interface Unit (MCIU) which is associated with the remote manipulator system (RMS). The MCIU may be accessed preflight for checkout and for on-orbit operations. The LDB's may also be used for a GPC to GPC memory overlay if so commanded via an entry to the DPS UTILITY display.

Initially, the command GPC for the LDB's is the first GPC to complete IPL and be placed in RUN. After the first OPS transition, the command GPC for the LDB's will be as specified in the nominal bus assignment table for that MC (unless altered by a GSE command or following certain types of I/O errors). The current command GPC for the LDB's is shown with an "*" under the command GPC on the GPC/BUS STATUS display. The only exception to the above is when the LDB's are specified for use in a GPC-to-GPC memory overlay. In this case, the LDB used (LDB 1 or 2) has the same number as the MMU/MM bus specified in Items 1-6 on the DPS UTILITY display. The command GPC for such a transaction would be the source GPC for the memory overlay.

4.4.14.1 I/O Error Handling. The I/O error handling for the LDB's is dependent upon whether the transaction failures occurred during a GPC-to-GPC transaction, or during a transaction with the LA or LF MDM's. In the first case, I/O errors on GPC-to-GPC transactions are handled similarly with GPC-to-GPC transactions using the MM data buses. There is an automatic retry on the same bus, and there can be up to two retries on the other LDB. In the second case, for I/O errors on LF or LA MDM transactions, a Class 3 alarm and a fault message are generated following two consecutive I/O errors. The message would be either I/O ERROR LF1 or I/O ERROR LA1. The software response is to switch data buses and retry the transaction. This automatic switching does not come into play for the SRB (LL and LR) MDM's.

4.5 TIME MANAGEMENT

The GPC complex requires a stable, accurate time source, since the software within the PASS GPC's uses GMT for scheduling software processing. Each of the five GPC's uses the MTU to update its internal clock since the MTU provides the most accurate timing source. The MTU, which provides precise frequency outputs for various timing and synchronization purposes to the GPC complex and many Orbiter subsystems, includes three time accumulators. Each of these MTU accumulators provide both GMT and MET which can be updated by external control.

The software Time Management Processor (TMP), which is a part of each GPC's systems software, provides external control over the MTU through synchronizing and/or updating the MTU accumulators, as well as requesting the current time and BITE status from the MTU. The TMP is also responsible for comparing the internal GPC time with the MTU time sources, selecting the best source, and updating its internal clock as necessary.

A systems level SPEC, called TIME (figure 4-5), provides the capability to the user to observe the current MTU and GPC clock status, synchronize or update the MTU and GPC clocks, select MET or GMT as the CRT mission time, and set CRT timers and alert tone duration/timers. This SPEC is available in all OPS except GNC OPS 1, 3, and 6.

4.5.1 Master Timing Unit (MTU). The MTU is a device which provides GMT and MET for all Orbiter applications and provides precise frequency outputs for various timing purposes. The MTU outputs serial digital time data (GMT/MET) on demand to the GPC's, which use this time for a computer reference time and indirectly for time tagging of GNC and SM processing. The MTU also provides continuous digital timing outputs for driving the four digital timers in the crew compartment (there are two mission timers, one on panel O3 and one on panel A4, which have an associated switch to display GMT or MET, and an event timer on panel A4 and on panel F7).

There are three timing terms that are used when discussing time management.

- A. Runtime - Runtime is the time derived from a GPC's internal clock (in GMT). All software processing in a GPC is scheduled according to that GPC's runtime. Therefore, adjustments to a GPC's runtime affects its software processing. A GPC's runtime is also referred to as internal time.
- B. Clocktime - Clocktime is a commonly derived value of time which is used during redundant set operations for applications software computations which require time (such as state vector propagation, IMU reads, etc.). This time is computed 25 times a second, and thus is accurate to 40 msecs. It is then stored in a location which can be accessed by the application software.
- C. Mission Time - Mission Time is the time value which is displayed in the upper right hand corner of each CRT display. This time can be displayed in either GMT or MET. Items 1 and 2 on the TIME SPEC control whether GMT

or MET is displayed for all common set GPC's. Note that in the on-orbit case, for example, when there are both GNC major function software and SM major function processing simultaneously, a change in the mission time selection to a GNC GPC controlled keyboard will be seen on both GNC and SM driven displays. An * will be displayed next to the type of time used as the mission time.

4.5.1.1 MTU Hardware. The MTU is a stable, crystal-controlled frequency source with an accuracy of one part in 10^9 per day, after a 16-hour warm-up (as illustrated in figure 4-16). The MTU uses two 4.608 MHz oscillators as redundant frequency sources. The signals from one of these sources (selectable via the MASTER TIMING UNIT OSC select switch on panel 06) are passed to the three GMT/MET accumulators. These accumulators keep track of time in days, hrs, min, sec, and msec. The GMT can be accumulated for up to a total of 365 days, 23 hrs, 59 mins, 59 secs, and 999.875 msec. The MET can be accumulated for up to 364 days, 23 hrs, 59 mins, 59 secs, and 999.875 msec.

The MTU sends its BITE status to the GPC's and PCMMU's. The MTU BITE word is incorporated into the operational instrumentation downlink, and some of the MTU status derived from the BITE word is displayed in the TIME SPEC. More detail about the MTU operational aspects is presented in SFOM Volume 4B.

4.5.1.2 GPC/MTU Operational Interface. Each of the MTU accumulators is tied to a Flight Critical Forward (FF) MDM. (Accumulator 1 to MDM FF1, etc.)

Because of this arrangement, any one of the GPC's which is listening on Strings 1, 2, or 3 will receive MTU time and BITE status directly. The redundant set GPC's will receive the MTU timing inputs simultaneously, thereby allowing them to keep their timing and processing within the limits required for redundant set operations. Note that each GPC will receive timing inputs from each of the three MTU accumulators.

A software module in each GPC, called the Time Management Processor, attempts to obtain GMT, MET, and BITE from all three accumulators 1.04 times per second. The GPC which is in command of the appropriate FC bus (and FF MDM) actually sends the command for data to the corresponding MTU accumulator, and all GPC's listening on that data bus will hear the MTU response. If an I/O error causes data loss from that accumulator, an M will be displayed next to the MTU accumulator time word on the TIME SPEC. The current MTU accumulator times will also be exchanged among the common set GPC's at the next common set sync point over the ICC data buses. This ICC exchange will also include the current time value for each common set GPC. Thus, each common set GPC may have as many as seven sources of time available: the three MTU accumulators and four common set GPC runtimes (itself included).

It should be noted that although the GPC's receive GMT, MET, and BITE from the MTU, they only utilize the MTU's MET at initialization. Otherwise, a new value, $GPC\ MET\ REF = GPC\ GMT - MTU\ MET$ is defined, and thereafter the GPC's use $GPC\ MET = GPC\ GMT - GPC\ MET\ REF$.

4.5.1.3 MTU Accumulator Status. If an accumulator fails to incorporate an update signal from the MTU oscillator, as detected by the MTU BITE,

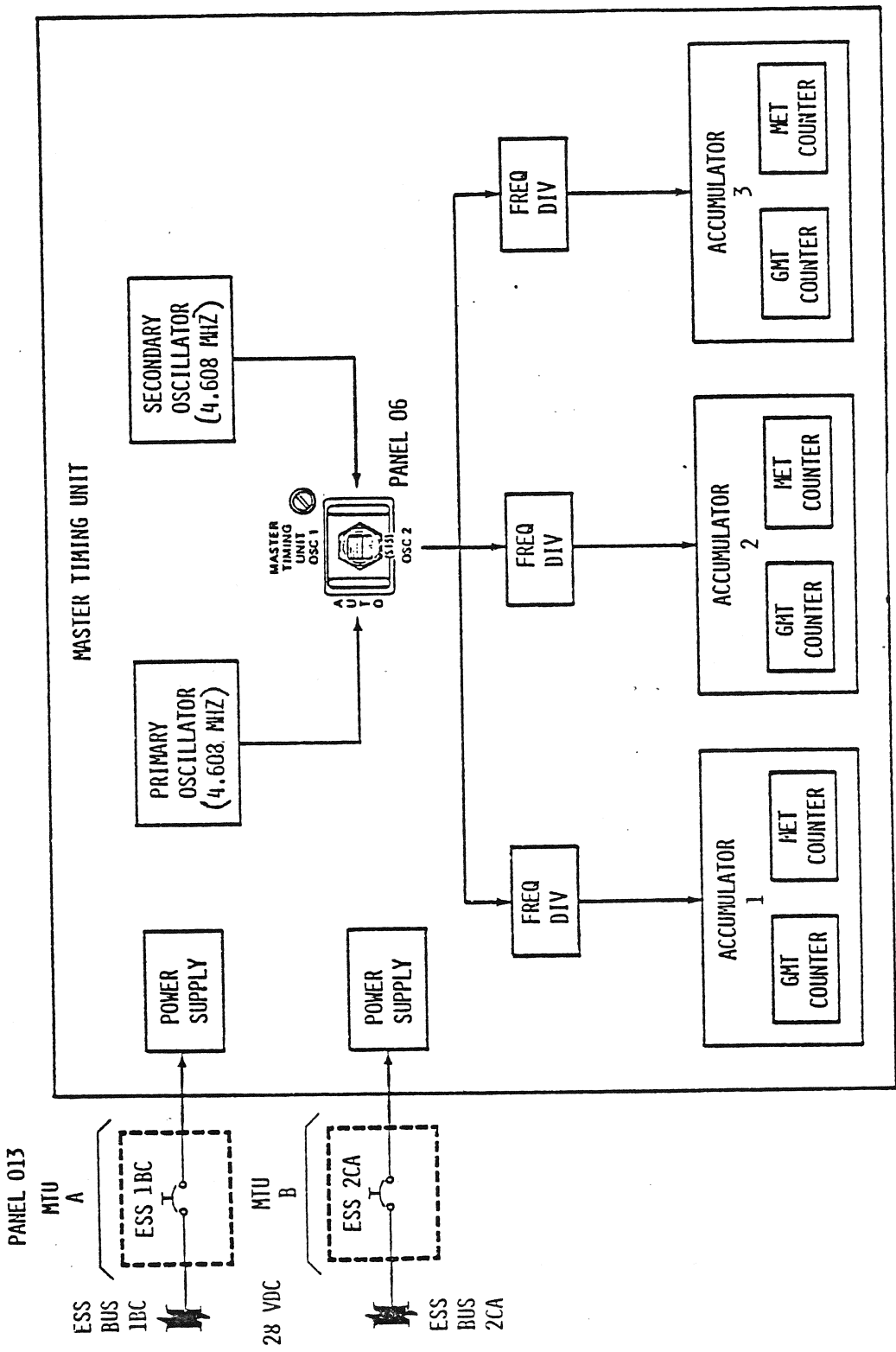


Figure 4-16. MTU Hardware

an appropriate bit will be set in the MTU BITE word sent to the GPC's and the PCMMU's. In addition, a "↓" will appear next to the accumulator time word, should this accumulator failure cause the GPC to fault down to another time source when it goes through its time selection process. (This would be accompanied by a TIME MTU Class 3 fault message on the CRT's fault message line.)

4.5.2 Time Management Processor (TMP). The systems software module known as the TMP is initiated once every major cycle (1.04 Hz). Its purpose is to gather and adjust time source information from the three MTU accumulators and from the other common set GPC's. It then selects a time source (either automatically or through a crew entry to the TIME SPEC) with which to correct its internal clock. Whether the selected time source is an MTU accumulator or another GPC's runtime is based upon several factors.

If a GPC has selected an MTU source on the previous cycle, it will compare its internal runtime with that of the MTU source on this cycle and see if the difference is less than a tolerance factor, K1. K1 typically is 800 μ sec. This K1 or credibility test is used to insure that a GPC's runtime is corrected for drift.

If the difference is greater than K1, that GPC will initiate a Class 3 alarm and TIME MTU fault message. Also, a "↓" will appear next to the former MTU time source's time word on the TIME SPEC. Next, the GPC will sequentially compare its runtime with the other two MTU accumulators. The first one to pass the K1 test will be the new selected time source for that GPC and will be used to update its runtime. Starting with the next cycle, the GPC will then begin its comparison with the newly selected accumulator. If no MTU accumulator passes the K1 test, that GPC will then select a GPC source with which to correct its runtime. Once this happens, the GPC will not check an MTU source on future time management cycles until user intervention. Items 34, 35, and 36 on the TIME SPEC can be used to force all commonset GPC's to retry their K1 tests, starting with the MTU accumulator selected by the item number (ITEM 34 EXEC forces a retry with MTU A1, Item 35 forces a retry with MTU A2, and Item 36 forces a retry with MTU A3).

In order to select a GPC source, the following logic is incorporated: after faulting from an MTU source, K1 is set to 5 msec for that cycle only. The two lowest numbered common set GPC's times are compared. If the difference for both is less than K1, the lowest numbered common set GPC's time is compared with this GPC's time; otherwise, the third lowest numbered common set GPC's time is compared with this GPC's time. In either case, if this difference is less than K1, this GPC will correct its runtime based upon the selected GPC's internal time; otherwise, it will fault down to its own internal time (i.e., update its time by zero).

If the GPC selected a GPC time source on the previous cycle, then it will again go through the logic described above to select a GPC source again on the next cycle. The only exception here is that K1 will be once again 800 μ sec.

If there were a crew entry of one of Items 34, 35, 36, or 37 to the TIME SPEC, all common set GPC's will begin their time source selection process using the source selected on the TIME SPEC. However, such a user entry changes the value

of K1 to 5 msec for that cycle and thus increases the probability that the user selected time source passes the K1 test and will be used to update the common set GPC's internal clocks. On future TMP cycles, K1 is again reduced to 800 μ sec.

In any case, the time source (MTU A1, A2, or A3, GPC 1, 2, 3, 4, 5) selected by the GPC will appear in the lower right hand corner of the TIME SPEC.

4.5.2.1 Time Sync. It is possible, via a single user entry (Item 38 EXEC) to the TIME SPEC, to synchronize the three MTU accumulators to the time source used by the lowest numbered GPC which has control of at least one of FC Data Buses 1, 2, and 3. The runtime of all common set GPC's will be set equal to this time source, as will the time values in the three accumulators. All the GPC's would then, at least temporarily, attempt to use MTU A1 as their time source.

4.5.2.2 Initialization. The first PASS GPC to complete IPL and be moded to RUN will request the current MTU accumulator times. This GPC will set its runtime equal to the first available MTU source. If none is available (the MTU is off), it will continue to process, using its own runtime. However, if the GPC's runtime is less than 30 minutes, it may default to GMT DAY 1 and MET DAY 0.

If the GPC's OUTPUT switch is in TERMINATE, or the BFS is engaged, the PASS GPC will not be transmitting or receiving on the FC data buses, and so will not be listening to the MTU. In this case (initialization only), the PCMMU will be substituted for the MTU as a time source. This is done to synchronize the GPC's downlist with the PCMMU.

If one PASS GPC is already in RUN and is in control of at least one of FC Data Buses 1, 2, and 3, when another GPC is moded from HALT or STANDBY to RUN, it will set its runtime equal to that of the lowest numbered GPC in control of one of FC 1-3. This new GPC will also initiate its TMP software, using the same time source as the lowest numbered GPC in control of one of the FC 1-3 Data Busses.

4.5.3 MTU/GPC Clock Update. It is possible to update the GMT and/or the MET clocks in the MTU and the GPC's by entering a delta time update via a user entry to the TIME SPEC. The MET may also be updated via the applications software. An example of this occurs at liftoff when the MET clocks are automatically set to zero.

Items 24-27 (25-27 are implied item numbers) on the TIME SPEC allow for user entry of a desired GMT delta update in days, hours, minutes, seconds, and milli-seconds. Similarly, Items 28-31 allow for a user entry of a desired MET delta update. MET is actually derived from the GMT, so a GMT update would result in a corresponding MET REF update.

The sign of the update (+ or -) will correspond to the sign of the lowest entered item number with non-zero data for the GMT or MET set. Therefore, if an MET delta update is entered using a + key for the Item 24 entry (assuming non-zero data) and the - key as a delimiter for the rest of the entries, the sign of the delta update would be positive.

Entry of Item 32 EXEC initiates the time update, using the values entered in the previous locations, with the actual update occurring from 1-2 minutes later at the MTU coincidence time. The coincidence time is computed by rounding the current time to the next minute and adding 1 minute. After ITEM 32 EXEC is entered, Items 24-31 will be blanked. Another point to note is that following a GMT update, the TMP in each GPC will select MTU Accumulator 1 for its time source.

A GMT update request of more than 15 msec will be rejected, and an ILLEGAL ENTRY fault message generated. Since each PASS GPC bases its processing on its internal GMT runtime, this limitation insures that no GPC will go inactive for more than 15 msec. An exception to this limitation is an update to a single running GPC in OPS 0. In such a case, the GMT may be updated by days, hrs, mins, secs, and msec, and the MET will be reset to zero. Furthermore, GMT and MET updates cannot be entered at once.

Executing ITEM 33, MET RESET initiates a resetting of the MET in both the MTU and the common set GPC's. This results in equalization of GPC and MTU MET.

4.5.4 CRT Timer. Each major function is provided a separate CRT timer. This timer's current value is displayed on the second line in the upper right-hand corner of all displays within the applicable major function. This timer can be controlled by a specific OPS sequence or SPEC software.

Figure 4-17 illustrates a typical XXXXX MNVR XXXXX display (in this case, the ORBIT MNVR EXEC display), which is an OPS display. On this display, The Time of Ignition (TIG) of a burn can be entered using Items 10-13 and loaded into the appropriate GPC's for execution using Item 22. When the timer is started (ITEM 23 EXEC), the difference between the TIG and the current mission time will appear in the CRT timer, and the CRT timer will begin counting down, reaching zero at the burn TIG.

A specified time can be placed in the CRT timer by using item entry controls on TIME SPEC. This entry can be positive or negative, and can include hours, minutes, and seconds. Items 9-11 are used to enter this data, and the sign of the lowest entered item number with non-zero data defines the sign of the entire time string. A minus entry here, when started, will cause the CRT timer to count down to zero and then begin counting up. A positive entry will simply count up from the entered value.

This CRT timer value is loaded into the timer, and the timer started in one of two ways. An entry of ITEM 12 EXEC will start the timer, at which time the data entered in Items 9-11 will blank. Item 13 can be used to stop and zero the CRT timer.

Another method for loading the CRT timer is to enter a mission time value, in hours, minutes, and seconds, into Items 14-16. This time is then compared with the value of the current mission time. When these two times are equal, the previously loaded time in Items 9-11 will be loaded into the CRT timer, Items 9-11 and Items 14-16 will blank, and the timer will begin counting.

2021/ /	ORBIT MNVR EXEC	1 009/16:52:33
OMS BOTH 1*		000/00:37:31
L 2	BURN ATT	
R 3	24 R 336	ΔVTOT 56.7
RCS SEL 4	25 P 134	TGO 3:02
5 TV ROLL 180	26 Y 15	VGO X + 43.20
TRIM LOAD	MNVR 27	Y - 7.60
6 P [-]1.2	REI	Z + 15.40
7 LY [-]0.7	TTA 15:25	
8 RY [-]1.2	GMBL	
9 WT 209265	L R	HA HP
10 TIG	P +1.5 +2.3	TGT 147 +132
009/17:30:04.8	Y +0.6 +1.1	CUR 147 +129
TGT PEG 4	PRI 28* 29*	
14 C1 -----	SEC 30 31	FWD RCS
15 C2 -----	OFF 32 33	ARM 35
16 HT -----	GMBL CK 34	DUMP 36
17 T -----		OFF 37*
18 PRPLT -----		SURF DRIVE
TGT PEG 7 -----		ON 38
19 VX [-] 56.7		OFF 39*
20 VY [-] 0.0		
21 VZ [-] 0.0		
LOAD 22/TIMER 23		
	5	

Figure 4-17. ORBIT MNVR EXEC Display

There is another method of setting the CRT timer which like the controls on the XXXXX MNVR XXXXX display, sets the timer to count down to a specific event or mission time.

This is done by entering the target mission time into Items 17, 18, and 19. Upon completion of this command sequence, the difference between the target mission time and the current mission time is loaded into the CRT timer, and the timer begins counting down. The CRT timer will reach zero when the current mission time and the target mission time are equal. When this happens, the data fields for Items 17-19 will blank.

Whenever the CRT timer is required to count down to zero, it will start counting up again, as soon as the zero point is reached.

Note that a separate CRT timer is available within each major function. Thus, using some of the controls previously mentioned, the user may set up one timer in the GNC major function, one in the SM major function, and a third timer in the PL major function.

4.5.5 Alert Tones. The TIME SPEC also contains controls to set times at which alert tones will be sounded (two for selected mission times and one for CRT timer), and also to set the duration of the SM alert tone (used in Class 3 alarms).

Item 23 is used to set the duration of the SM alert tone, using an ITEM 23 + XY EXEC type entry, where XY represents the tone duration in seconds. This value can be set in a range from zero (which would inhibit the tone) to 99 sec. Note that this tone duration control alters the tone duration for all applications of the SM alert tone, and not just those related to those on the TIME SPEC. Also, the tone duration will be in effect for any GPC in the comon set.

The initial time duration is 1 second. This duration is programmed in the software source code of all GPCs.

There are three sets of item controls on the TIME SPEC which allow the user to enter time values at which the alert tone will be sounded. Two of these sets (Items 3-5 and 6-8) allow the user to enter mission times for sounding the alert tone. When the current mission time equals the time input to one of these data sets, the alert tone will be activated for the time period specified by the duration item. At the same time, a fault message (TIME TONE) will be generated on the appropriate CRT's, and the SM alert light will be illuminated. The involved data field will also blank at this time.

The third data set (Items 20-22) allows the user to activate the alert tone a specified CRT timer value. A negative value will result in a tone when the CRT timer counts down to that value, and a positive input event time will result in a tone when the CRT timer counts up to that value. The same responses and actions that pertain to the mission time event timers also pertain to the CRT time event timer.

These event timers are based on a 24-hour clock; therefore if an event time input is made which is less than the current time, the alert tone will not be activated until the following day, when the current time and the event time are again equal.

4.6 DATA PROCESSING SYSTEM GPC MAIN MEMORY MODIFICATION

The contents of memory within the GPC's (main memory) can be modified by the ground support personnel as well as by the crew. During prelaunch operation main memory can be modified via the LDB interface with the GSE computers, in-flight via uplink commands from the mission control and at any time by the crew via the GPC MEMORY display - SPEC 0 (see figure 4-3).

The following discussion will not cover the LDB interface but will cover uplink and the GPC MEMORY SPEC.

4.6.1 Uplink Commands. The ground can uplink three distinct and separate types of uplink data to modify main memory. The first type is for modifying either contiguous or scattered locations in memory containing code as well as data. Note that this method directly modifies memory without interfacing with the MCDS system. As a result, it is not as visible to the crew, nor is it constrained as much as using the GPC MEMORY SPEC for memory modification; i.e., 64 16-bit words at a time versus 6 32-bit words KEYED IN ONE WORD AT A TIME. The second type of uplink data comes via the DEU equivalent command capability of the ground. The ground can call SPEC's, execute item numbers, and/or modify main memory via the GPC MEMORY SPEC, etc., the same way that the crew would with the GPC MEMORY CRT display. The third type of uplink commands from the ground that modify memory are those that change certain groups of variables in core such as state vectors, refsmats, guidance polynomials, launch targets, IMU gyro biases, IMU accelerometer biases, quaternions, deorbit landing site parameters, etc. These commands do not change code but alter data that is regularly used by the flight software.

4.6.2 GPC MEMORY CRT Display. The read/write portion of the GPC MEMORY display provides the user interface to review and change the value contained in any specified GPC MEMORY location. The general use of this portion of the display is to first read the present value of a given location. The value then may be changed using a two-step load sequence. Additional control items allow the user to read sequential memory locations with minimal keystroke inputs and to select the mode in which the reading and writing is performed. This part of the display is initialized with all fields blank except the mode, which will indicate DATA, and the major function indicator which will show which major function software is being addressed. Changes made to main memory via the read/write portion of this SPEC affect only those GPC's which are listening to the involved DEU/CRT. Thus, if the DEU's MAJ FUNC switch is in the GNC position, only the GNC GPC's will be affected. Similarly, if the MAJ FUNC switch is in the SM position, only the SM GPC will be affected. If the DEU has been assigned to an OPS 0 GPC, only that GPC will hear the transactions from this part of the SPEC.

4.6.2.1 Operational modes. The spec has four modes of operation; the DATA, CODE, BIT SET, and BIT RESET modes. In the DATA mode, the crew or the ground can review or modify any data location in main memory. In the CODE mode, the crew or the ground can review or modify any instruction location in main memory. Instructions or code can only be changed by having the software clear the storage-protect bit that is normally set for all code locations. The protect bit is cleared upon execution of Item 21 and input of an address on the GPC MEMORY Spec. That action causes the word CODE to flash and also allows complete

freedom in altering main memory. The protect bit is not cleared when in DATA mode and thus prevents accidental alteration of flight software instructions.

The read/write part of the GPC MEMORY display is primarily intended to address the data sections of main memory which are unprotected. For this reason, the display is initialized with Item 20 (DATA) enabled. Items 22 and 23 are designed to allow the user to set and reset individual bits of memory.

Upon executing any of Items 20, 21, 22, or 23, the active mode will be indicated by an asterisk to the right of the corresponding item number, and all the data fields will blank (ADD ID, DESIRED, and ACTUAL). This "*" will remain next to the selected mode until changed by another mode item entry, or until the display is dropped. The four mode item numbers are mutually exclusive.

4.6.2.2 Memory Read Operations. The contents of any memory location may be observed after the selection of the appropriate operational mode is made (DATA, CODE, BIT SET, or RESET). This display is initialized with DATA (Item 20) and half-word hex (Item 27) selected. A read is accomplished by entering the appropriate memory location address (ADD ID) and an appropriate scaling factor of engineering units or half-word hex. The ADD ID is a five-digit hexadecimal number which identifies the memory location being addressed.

A scaling factor of engineering units or half-word hex may be selected via Items 26 or 27 for the display of the contents of addresses specified in Items 28-38. However, the desired contents for such an address must be input in half-word hex. Selection or reselection of either Item 26 or 27 will blank all the data fields. A three-digit number may be input to Item 26 to indicate that the contents of the addresses in Items 28-38 are to be viewed in the specified Engineering Units. The first digit identifies fixed or floating point. The second and third digits select the desired unit conversion.

Digit 1

- 1 - 16 bit/fixed
- 2 - 32 bit/floating

Digits 2 and 3

- 00 - Units in Memory (no conversion)
- 01 - NM from feet
- 02 - NM from K feet
- 03 - Feet from MN
- 04 - K feet from NM
- 05 - Feet/Sec² from G
- 06 - Deg/Sec from M Rad/Sec

- 07 - Deg from Arc Sec
- 08 - Feet/Sec² from Micro G
- 09 - Deg from Rad
- 10 - KFT from feet

Upon the entry of a correct ADD ID, the current value of that memory location will be displayed in the ACTUAL column.

Item 24 (Sequential ID) provides the capability to read sequential memory locations in the GPC without requiring the crew to input data for individual locations. Before executing Item 24 the desired ENG UNITS or HEX selection must be made and the ADD ID specifying the starting memory location must be entered.

Upon execution of Item 24 the sequential locations following the starting locations are displayed and the corresponding desired fields are blanked. If multiple locations are being displayed when the sequential read is executed, the most recently entered ADD ID is assumed to be the starting address, and the GPC READ/WRITE table will be filled starting at this point. The sequential capability is for readout only and does not apply to the WRITE function. However, the capability is provided to write into an ACTUAL list of valves that has been displayed using the sequential read function.

4.6.2.3 Bit Set/Reset Operations. The capability also exists to set individual bits to a logical 1 (bit set) or to a logical zero (bit reset), as opposed to writing over a memory location with new data. This capability is only available when half-word hex (Item 27) is selected.

In order to perform the bit set function, ITEM 22 EXEC must be entered to initiate the BIT SET mode. ITEM 27 (half-word hex) must be entered if it is not already selected, and the appropriate ADD ID must then be entered, bringing the value in that memory location into the ACTUAL column on the display. A 16-bit mask word, represented by four hexadecimal characters, is then placed in the DESIRED column. This mask word identifies the individual bits which are to be set with a logical 1, and the bits which are to remain unchanged with a logical zero.

ITEM 25 EXEC initiates the bit set function, and the specified memory word is altered accordingly, with the new representation displayed in the ACTUAL field.

The bit reset function works the same way except that Item 23 must be selected, and a logical 1 in the mask word resets the appropriate bit in memory to a zero; a logical zero in the mask word leaves its corresponding memory word bit unaltered.

These two functions are especially useful when a specific data word is partially dynamic, and the user wishes to alter only part of the data word, while allowing the rest of the data word to update freely. In addition, bit set and bit reset apply only to the unprotected areas of memory.

4.6.2.4 Memory Write Operations. All changes to GPC main memory are done in an ARM/FIRE method. In order to perform a write operation, the appropriate mode (DATA or CODE) must be selected, and then the appropriate scaling factor and ADD ID entered, resulting in the display of the present data value in the ACTUAL column. The user then must enter the value to be written into ACTUAL in the DESIRED column in half-word hex. The user can verify the new value prior to writing this new value into memory. An entry of ITEM 25 EXEC will send this desired value to the specified memory location for storage. The ACTUAL field will then reflect the new stored value, which can be compared to the desired field. The desired field will not blank until the mode is changed, reselected, or the display dropped.

Selected values in the ACTUAL list can be changed by supplying desired data only for those values and then executing a WRITE command. Blank rows in the desired column are skipped, and their current values remain unchanged. If no desired value has been entered prior to a WRITE command, the ILLEGAL ENTRY fault message will be generated.

If the DATA mode is selected, and the user attempts to write into a CODE location (these locations are protected), the ILLEGAL ENTRY fault message will be generated. However, there is no software protection to stop the user from writing into a DATA location while in the CODE mode. This would result in the DATA location being transformed into a CODE (protected) location. This could result in the loss of the involved GPC's or the loss of that data word with unknown results (e.g., state vector).

4.7 DATA PROCESSING SUBSYSTEM MASS MEMORY MODIFICATION

The data contained on Mass Memory magnetic tape can be modified by the ground support personnel as well as by the crew, via the LDB's (during prelaunch operations) or inflight via uplink commands or crew controls on the MASS MEMORY R/W SPEC display (figure 4-18). The inflight techniques involving uplink commands and crew controls will be discussed here.

When required to update Mass Memory, a GPC must be executing SM OPS 2 or PL OPS 9 software to provide enough GPC main memory storage to perform the function. This is necessary because modification of Mass Memory occurs by reading a software load block into a special storage area of the GPC (available in special SM and PL OPS), modifying the load block, and writing the modified load block back onto Mass Memory. The special storage area of main memory is 2,048 16-bit words in SM OPS 2, 16,384 16-bit words in PL OPS 9, and non-existent in any other major function OPS.

4.7.1 Uplink Commands. Mass Memory is modified via direct write commands or DEU equivalent command using the MASS MEMORY R/W display. The direct write capability is mechanized without interfering with any MCDS operations. The DEU equivalent method requires activating the MASS MEMORY R/W display and interfacing with the MCDS input processor.

4.7.2 MASS MEMORY R/W CRT Display. The MASS MEMORY R/W display allows reading and changing of data stored on an MMU, comparing a load block between MMU 1 and MMU 2 and dumping MMU data to the ground via downlist. The area on the right third of the display selects which MMU data to change or dump and maintains the status of the operation. The area on the left two-thirds of the display shows the current data in the specified location, allows entry of the data desired to be in the specified location, and indicates the hexadecimal checksum of the operation in progress. The display is initialized with blanks in all data slots when the Spec is activated as SPEC 85 in SM OPS 2 or as the OPS display in PL OPS 9.

4.7.2.1 Memory Write Operation. An MMU write initially requires specification of which MMU (Item 40 or 41) and which software system contains the data to be changed.

<u>Software System ID</u>	<u>Software System</u>
0	Display Text and Graphics
1	PASS Version 1
2	PASS Version 2
3	PASS Version 3
4	BFS
5	DEU
6	SSME
7	TCS Sequences (OFT, KS)
8	Not Supported
9	Not Supported

0801

MASS MEMORY R/W

1 273/15:35:02

000/01:30:00

DESIRED	ACTUAL	DESIRED	ACTUAL
1	<u>43AC</u>	53AC	21
2			22
3			23
4			24
5			25
6			26
7			27
8			28
9			29
10			30
11			31
12			32
13			33
14			34
15			35
16			36
17			37
18			38
19			39
20			CHECKSUM

SELECT

MMU 1	40*
MMU 2	41
42 S/W SYSTEM	<u>4</u>
43 PHASE	<u>11</u>
44 LOAD BLK	<u>12</u>
45 OFFSET	--- <u>45</u>
46 NUMBER	<u>1</u>
47 PATCH ID	<u>1111</u>
VIOLATE	NO
READ LOAD BLK	48*
MERGE	49
WRITE LOAD BLK	50
COMPARE	51
STATUS	CPLT
ERROR CODE	
REGISTER A	
B	
MM VERSION	12.11
DUMP VIA DL	52

Figure 4-18. MASS MEMORY R/W Display

Only one MMU can be modified at a time. The particular software phase (Item 43) and load block (Item 44) within the specified system must be identified since MMU-to-GPC data transfers occur in load blocks consisting of up to 16,384 16-bit words at a time for modification. Hence, the words of the load block to be changed must be identified relative to the first word of the load block by specifying the offset (Item 45) into the load block and the number of contiguous words (Item 46) to be changed.

Each time an MMU load block is read into GPC main memory, the version of the MMU contents is displayed (MM VERSION). Whenever a particular load block is modified, a log of MMU changes is updated by assigning a hexadecimal ID (Item 47) to the particular load block modification or patch.

A read operation is initiated by transferring the identified load block from the MMU to the GPC (Item 48). The STATUS (IP, CPLT, ERR) is presented to indicate a successful or unsuccessful data transfer operation (and a numerical CODE to identify error if unsuccessful). The MMU BITE status REGISTER A and B data (which are transferred to the GPC with the load block transfer) and the checksum word are displayed in hexadecimal notation. When loaded into the special main memory storage area, the hexadecimal data values to be changed (as specified via Items 40-46) appear in the slots on the display beside the appropriate item numbers under the ACTUAL column. A DESIRED hexadecimal value must be entered for each ACTUAL data value before the DESIRED values overlay or merge with (Item 49) the ACTUAL data value, making the ACTUAL column = the DESIRED column.

The STATUS of the merge operation is presented during the data transfer operation. If more than 39 16-bit words or a different set of 16-bit words are to be modified, Items 45 and 46 are reentered for the next set of 16-bit words to be changed, blanking Items 1-39. When all DESIRED values have been merged with the ACTUAL values of the load block, the load block is written back into the selected MMU (Item 50). A problem with the write operation attempting to VIOLATE restrictions of patch ID or simultaneous MMU read will be indicated as would the STATUS of the write operation itself. As part of the write operation, the load block will be read back into the GPC to perform a word-by-word comparison check to verify proper coordination and allow user retry if necessary.

4.7.2.2 Memory Compare Operations. The particular load block of one MMU identified via Items 40-44 can be compared to the same load block on the other MMU using a word-by-word comparison (Item 51) and any error conditions displayed as STATUS and CODE. The capability to dump Mass Memory via downlist is described in section 4.8.4.

4.8 DOWNLIST

A downlist is a set of data transferred from a GPC to the PCMMU. The downlist system software executive in each GPC organizes data obtained directly, or via one of the DPS MDM's, and data from the various systems software modules, into sets of data called downlist formats (also referred to as the GPC's downlist). Each GPC transmits its downlist format to the PCMMU's as illustrated in figure 4-19. The PCMMU's interleave Operational Instrumentation (OI) data from OI MDM's and PL data (from the payload data interleaver and Spacelab) with the downlist telemetry data into telemetry data formats for transmission to the Network Signal processors (NSP's). The NSP's combine the PCMMU telemetry data with onboard voice into operational downlink telemetry formats. The S-band subsystem converts the NSP operational downlink telemetry format into the proper waveform for transmission to the ground by a transponder transmitter (XPNDR XMTR).

One of the several Spacecraft Tracking and Data Network (STDN) remote site stations receives the operational downlink telemetry and separates voice from data. In addition, the STDN remote site documents and reformats the operational downlink telemetry before transmitting the voice and data to Goddard Space Flight Center (GSFC) in Greenbelt, Maryland. Goddard manages the STDN remote sites and transfers the voice and data to JSC's Mission Control Center (MCC).

The communication interface system in MCC validates and preprocesses downlink data prior to shipping it to the Shuttle Data Processing Complex (SDPC). The SDPC performs data manipulation and processing of downlink data before transmission of the realtime data to the display control system for routing to the appropriate MCC console.

During later OFT flights and the OPS flights, the STDN downlink system will become the secondary downlink method. The primary downlink system will be a Tracking Data Relay Satellite (TDRS) system. The formation of downlink telemetry will follow the same data flow as that in the early OFT phase as far as the Orbiter NSP's. The NSP's will transfer the operational downlink to the S-band system or to the Ku-band system for processing. The S-band system or the Ku-band system transmits operational downlink telemetry to a TDRS as the primary telemetry path, while the STDN remote sites will remain functional as secondary telemetry paths.

The TDRS system will transfer the operational downlink telemetry to a TDRS remote site for relay to the Domestic Satellite (DOME SAT). The DOME SAT will transfer the telemetry to the DOME SAT receiver which will relay the combined voice and data to the MCC communication interface system for separation and validation processing by the SDPC.

4.8.1 Composition of The Downlist. The groups of data included in a typical GPC downlist format are shown below. The composition of a typical downlist varies as a function of the GPC's MC. The DPS hardware and systems software data are available in every downlist format. Furthermore, anytime a GPC is executing software, it is sending downlist data to the PCMMU's for inclusion into the operational downlink telemetry to the ground.

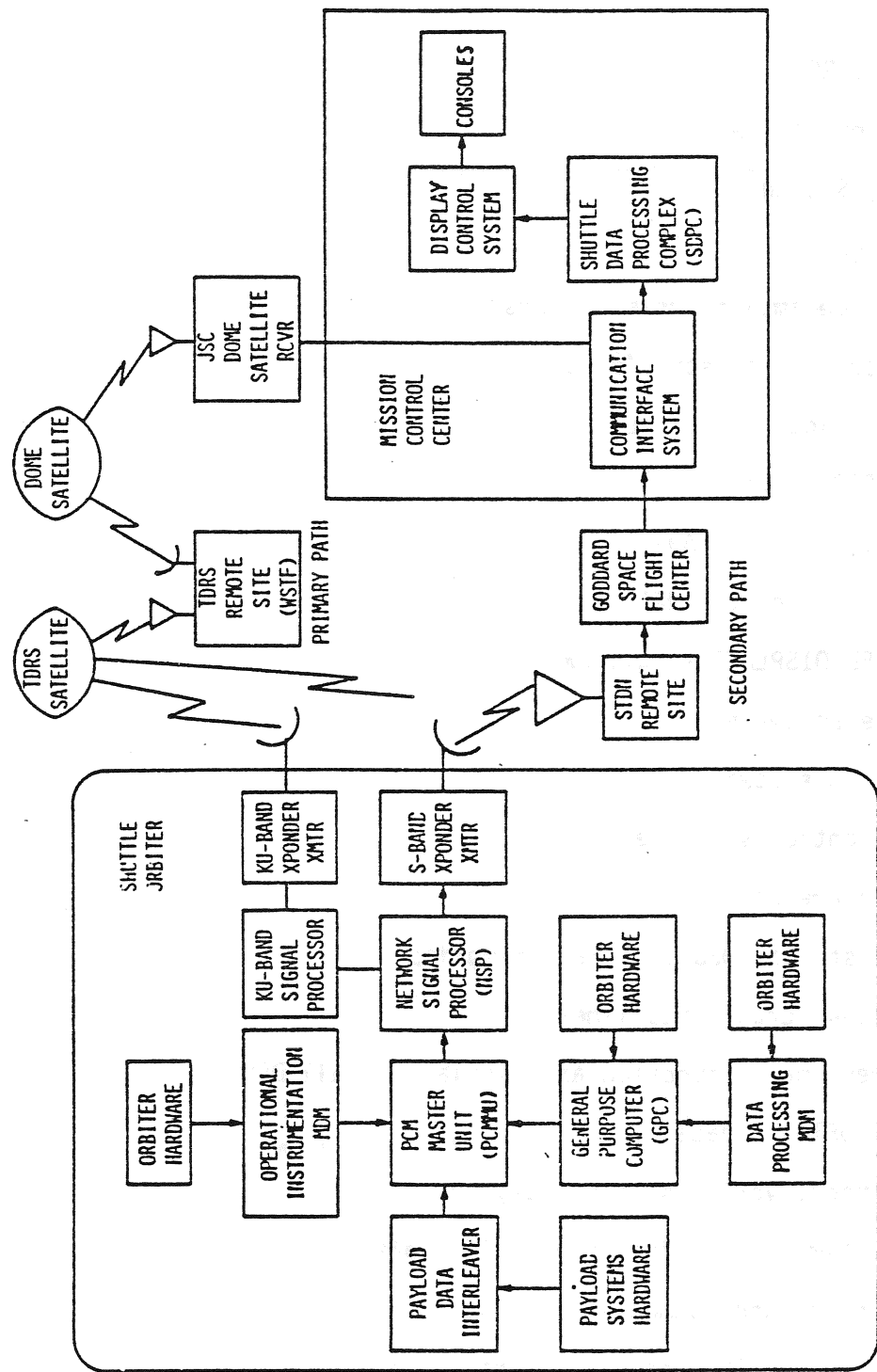


Figure 4-19. Functional Realtime Downlink Data Flow

- Crew station controls and displays
- MTU
- MPS, OMS, RCS
- SM sequence software
- Ku-band, S-band
- Landing gear
- Aerosurface amplifiers/actuators
- Flight control sensors (e.g., RGA)
- Vents, payload bay doors
- NAV SENSORS (e.g., IMU)
- NAV AIDS (e.g., TACAN)
- CONTROLLERS (e.g., RHC)
- DEDICATED DISPLAYS (e.g., AMI)
- Guidance software
- Navigation software
- Flight Control software
- DPS hardware data
 - BITE status (DEU 1-4, Mass Memories 1-2)
 - DEU 1-4 scratch pad lines
 - Current major function and display for all DEU's
- SYSTEM SOFTWARE data
 - GPC mode, voting status, duty cycle
 - GMT, time source for timekeeping software
 - Redundant and common set status
 - Latest five GPC and I/O Errors of Self
 - Accumulated # and last I/O Error for common set GPC's

- Accumulated # and last GPC Error for common set GPC's
- BCE chain element status and BUS masks
- Latest five fault messages
- Discrete outputs and inputs
- NSP Status word, NSP power status
- GPC Command validity word
- 2-stage buffer contents

4.8.2 Downlist Format Composition. Data parameters (in GPC main memory) to be downlisted are selected preflight and organized into frames. One frame of data is transmitted to the PCMMU's every 40 msec. Fifty of these frames comprise one complete data cycle, which is 2 secs in length.

Sample rates for the downlist parameters can be 1, 5, 12.5, or 25 samples per sec. A one sample per sec (S/S) parameter will appear once in the first 25 data frames and once again in the same relative frame of the second group of 25 frames. For example, DEU BITE, which is sampled once per sec, may appear in Frame 3 and again in Frame 28. A parameter which is sampled 25 times per sec will appear in every frame of the downlist.

Each frame is composed of 16, 32, 64, or 128 16-bit words, depending on the MC software. The first frame in each group of 25 frames has a header identifying the downlist format, GMT, and other associated data. Each frame then has a counter to allow time tagging of downlist on the ground within 40 msec.

4.8.2.1 Downlist Formats. The GPC's MC determines which downlist format will be transmitted to the PCMMU's. The MC software downlist format specifies which parameters (as a function of GPC main memory location) and how many 16-bit words per frame (the frame length) will be sent to the PCMMU's.

Each format is allowed only in one MC except for the memory dump formats. Memory dumps from the Orbiter replace the nominal downlist data during the dump for at least one data cycle. Mass Memory and main memory dumps are discussed in section 4.8.3.

A table which presents the downlist formats as a function of format identification number (FMT ID), data rate size, and memory configuration is presented in table 4-8.

4.8.3 GPC Downlist/PCMMU Interface. The GPC's downlist is transmitted to the active PCMMU for incorporation with payload and instrumentation data into the operational downlink. This is mechanized as follows: The PCMMU control logic receives the downlist data from each GPC and stores the data in the toggle buffer assigned to that GPC. There are five toggle buffers, each with two halves (maximum 128 16-bit word storage per half) which are alternately read and loaded by the PCMMU control logic module. Typically, the Downlist GPC is

TABLE 4-8 - DOWNLIST FORMATS

Format Certification	High Data Rate Size	Low Data Rate Size	Memory Configuration	Program	Usage
12	12.8	6.4	B		Backup flight computer- ascent
13	12.8	6.4	B		Backup flight computer- entry
20	12.8	6.4	0	0-00	Post-initialization program load, KSC release. Computer is in this format when started.
21	51.2	25.6	1	GNC 1,6	Primary computer set - ascent and orbit.
22	44.8	22.4	2	GNC 2	Primary computer set - orbit.
23	51.2	25.6	3	GNC 3	Primary computer set - entry.
24	(1)	(1)	4	SM 2	Systems management computer - orbit.
42	51.2	---	7	SM 9	Systems management computer-initialization and checkout.
44	44.8	---	9	GNC 9	Primary computer set - precount.
46	51.2	---	7	SM 9	Frequency response test - KSC release.
48	12.8	6.4	6	PL 9	Mass memory utility- loading and verifying the mass memory KSC release.
49	51.2	---	-	Self test	Primary computer set - self test.
52	51.2	---	6	PL 9	Mass memory utility - loading and verifying the mass memory, KSC release.

TABLE 4-8 - DOWNLIST FORMATS

Format Certification	High Data Rate Size	Low Data Rate Size	Memory Configuration	Program	Usage
53	51.2	---	9	GNC 9	Primary computer set-flight control system checkout. KSC release.
55	51.2				DIT-Ascent
56	51.2				DIT-Entry
58	12.8				DIT-BFS Ascent
59	12.8				DIT-BFS Entry
90	Note 1	---	Note 2	Note 2	Main memory dump.
91	Note 1	---	4.6	SM 2	Main memory dump.
92	Note 1			PL 9	Spacelab Computer Memory dump
93	44.8			GNC 9	HISAM Dump
97	51.2	---	7	SM 9	PCM master unit checkout - the address of the word is loaded as the data.
98	51.2	---	7	SM 9	PCM master unit checkout - 052525 (octal) is repeated in the data.
99	51.2	---	7	SM 9	PCM master unit checkout - 0125252 (octal) is repeated in the data.

NOTES:

1. Main and mass memory dumps assume the window size of the previous downlist format. Information in the dump header defines the amount of valid data contained in the window. The remainder is filled with zero's.
2. Main memory may be dumped in memory configurations 0, 2, 4, 6, 8, and 9 programs: 0-00; GNC 1, 6, 2, 3, 8, and 9 and SM 8 and 9.

assigned Toggle Buffer 1, the SM GPC Toggle Buffer 2, and BFS Toggle Buffer 5. The control logic in the PCMMU also determines which payload and instrumentation data is to be stored in the PCMMU's payload RAM and instrumentation RAM. Another module in the PCMMU is the telemetry formatter which determines which and how much toggle buffer, payload, and instrumentation data is to be included in the output to the NSP's for downlink. Each PCMMU has two telemetry formatters - a high data rate (HDR) 128 Kb/s one and a low data rate 64 Kb/s one. Whether the high or low data rate output is chosen to be used depends upon ground station acquisition and transmitting signal strength during each portion of the flight. Selection of the high or low data rate is performed by the NSP's as directed by Ground Control Interface Logic (GCIL) which is controlled by the NETWORK SIG PROC XMIT DATA RATE control (panel A1) if the S-BAND PM CNTL switch (panel C3) is in PANEL, or via ground uplink command if the S-BAND PM CNTL switch is in CMD.

To determine the allocation of GPC downlist data (in the toggle buffers), payload data, and instrumentation data to include in the downlink, the selected telemetry formatter reads the currently selected Telemetry Format Load (TFL). For the HDR telemetry formatter, two TFL's are available. One, the HARD or FIXED format; is pre-mission developed and programmed into a hardware PROM. It cannot be changed in flight. Its ID is 129 and is sometimes identified as HDR-H). It was developed primarily for pre-launch through ascent. It also contains the critical parameters for ground monitoring necessary for safe continuation of the flight. It is selected via the FIXED position of the panel C3 OI PCMMU FORMAT switch. It can also be selected when the FORMAT switch is in GPC and the SM GPC software is directed to select FIXED via Item 1 on SPEC 62 (PCMMU/PL COMM). (See figure 4-20.)

The other available HDR TFL is called the Soft, or Programmable, format. It is loaded in the PCMM programmable RAM and is changeable during flight. The different TFL's allow the ground to see more data for the particular mission phase (except ASCENT) than the fixed format. The programmable format is selected when the OI PCMMU FORMAT switch is in PROGRAM or when that switch is in GPC and the programmable format is selected via Item 2 on SPEC 62 (PCMMU/PL COMM). The SM GPC contains the logic request to load a new programmable TFL. The MMU's contain the actual TFL data and are accessed by the SM GPC in order to load a TFL. To load the selected TFL, the crew places the OI PCMMU FORMAT switch to GPC, selects ITEM 1-FXD on SPEC 62, enters the required TFL ID in ITEM 3-SEL ID and then does an ITEM 4 EXEC to initiate the process. During the load, the field on the display next to Item 4 will display RUN. At the completion of the load, it will display CPLT or FAIL. The crew then selects ITEM 2-PGM to enable the use of the soft format. Of interest is that the PCMMU RAM's are volatile. Thus, if the power to a PCMMU is cycled or the active PCMMU switched, the programmable TFL must be reloaded to be regained.

The LDR 64 Kb/s telemetry formatter only uses the programmable format found in the RAM. The panel C3 OI PCMMU FORMAT switch does not affect the LDR formats. The 64 Kb/s (versus 128 Kb/s) is achieved by only using the first half of the data contained in the toggle buffers for combination with the payload and instrumentation data. It is loaded via the SM GPC in the same way as the HDR programmable format. In addition, the BFS GPC can be used. Assuming that ITEM 29 - TFL ENA is selected on the BFS MEMORY display, the BFS will automatically initiate LDR Telemetry Format Load when a power switchover to the PCMMU is

1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1

```

XXXXXXXX/062/          PCMMU/PL COMM      XX X DDD/HH:MM:SS
SM COM BUFF XXX      DFI BITE          DDD/HH:MM:SS
PCMMU                PCMMU 1 X          PDI
BITE                 PCMMU 2 X          5 SEL DECOM X
FRMT                 RCDR PCM X          6 SEL FRMT XXX
SEL                 WB-ASC X            8 SEL INPUT X
                   WB-MSN X            LOAD 7 XXXX
                   ID 64 XXX           LOAD 9 XXXX
                   128 XXX            DECOM INPUT FRMT
3 SEL ID XXXX        1 X XX
LOAD 4 XXXX         2 X XX
                   3 X XX
                   4 X XX
                   5 - FPM            XXXX

PSP
1 ENA 10X
2 ENA 11X
1&2 INH 12X
SYNC BIT XXXXS
FRAME XXXXS

PL INTRG
1 CHANNEL XXXXS
2 CHANNEL XXXXS
PHASE LOCK XXXXS
ERR +XXXS
XMIT PWR XX.XXS
PL SIG STR X.XXS

```

(X X)

Figure 4-20. PCMMU/PL COMM Display

detected. It loads the ascent LDR format (002) if it is in OPS 1, MM 601, or GNC OPS 0 and loads the entry LDR format (005) during OPS 3 or MM602/603. If an error is detected in the load, a class 3 fault message TFL FAIL is generated. The PCMMU power switchover can be accomplished by the crew by moving the OI PCMMU PWR switch on panel C3. Note that these two LDR formats are stored in the BFS GPC Main Memory and do not require the MMU interface. Normally, the TFL ENA item is enabled during OPS 1 and 3 but is disabled when a PASS SM GPC is available to load TFL's. The BFS auto TFL load feature is used primarily if the current PCMMU fails during Ascent, RTLS or Entry, or during an AOA switch from the Ascent to Entry format. (See figure 4-21.)

Table 4-9 shows the DOWNLINK/DOWNLIST COMBINATIONS for STS 2. For example, combination 5 in the table is the 128 kbps PROM (HDR-H) format 129 of which 50 percent (64/128) is OI data, 40 percent (51.2/128) is data from toggle buffer 1, and 10 percent (12.8/64) is data from toggle buffer 5. Combination 6 is the 64-KBPS RAM (LDR) format 002 which maintains the relative percentages but reduces the amount of data output (and therefore, reduces the amount of data downlisted). Appendix B includes descriptions of the data included in the commonly used TFL's.

4.8.3.1 OPS 0 GPC Downlist. A non-prime OPS 0 GPC normally has its downlist disabled. This is implemented through a flag set in software. There are occasions when it is necessary for the ground to see an OPS 0 GPC's downlist. To do this, on Version 18 flight software, a memory read/write is done to reset the flag. Procedurally, the crew assigns a CRT to the OPS 0 GPC, calls up SPEC 0 on that CRT, enters the appropriate address for the downlist inhibit flag, and then does a WRITE to set the flag to allow downlist (See following information).

FREEZE-DRY GPC MEMORY DUMP

- 1 TFL FOR FD GPC MEMORY DUMP
 Perform LOAD PCMMU FORMAT (GPC Dump)
 Cue Card, then

- 2 GPC READ/WRITE - ENABLE GPC 3 DNLIST
 O6 GPC MODE 3 - RUN (tb-RUN)
 C2 CRT X MAJ FUNC - PL
 CRT GPC/CRT 3 X EXEC
 X: PL 0 GPC MEMORY
 DATA, ITEM 20 - (*)
 HEX, ITEM 27 - (*)
 ADD ID - ITEM 28 +9 A 8 7 EXEC
 ACTUAL - 0000
 DESIRED - ITEM 29 +8 0 0 0 EXEC
 WRITE - ITEM 25 EXEC
 ACTUAL - 8000

4.8.3.2 Loss Of Downlist. If a PASS GPC detects a problem with its downlist (called the downlist command message) prior to transmission to the PCMMU's, I/O

1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1

```

XXXX/000/          BFS MEMORY          XX X DDD/HH:MM:SS
          BFS DDD/HH:MM:SS
READ/WRITE
DATA 1X BIT SET 3X SEQ ID 5
CODE 2X BIT RST 4X WRITE 6
7 ENG UNITS XXXX HEX 8X
ADD ID DES TRED ACTUAL
9 XXXXX 10 XXXXX +XXXXXX
11 XXXXX 12 XXXXX +XXXXXX
13 XXXXX 14 XXXXX +XXXXXX
15 XXXXX 16 XXXXX +XXXXXX
17 XXXXX 18 XXXXX +XXXXXX
19 XXXXX 20 XXXXX +XXXXXX

```

```

MEMORY DUMP          LAUNCH BUS          1 26X
21 START ID          XXXXX                2 27X
22 NUMBER WDS        XXXXX                OFF 28X
23 WDS/FRAME         XXXX
DUMP 24
PASS/BFS XFER ENA 25X

```

(X X)

Figure 4-21. BFS MEMORY Display

TABLE 4-9

DOWNLINK/DOWNLIST COMBINATIONS

Combinations phase no.	Operational instrumentation			GPC toggle buffer 1			GPC toggle buffer 2			GPC toggle buffer 3			GPC toggle buffer 4			GPC toggle buffer 5			MEM. COMP.
	FMT ID	Type	BW	OPS	DL	BW	OPS	DL	BW	OPS	DL	BW	OPS	DL	BW	OPS	DL	BW	
Prelaunch	1	129	HDR-H	64	59	42	51.2												7.6
	2	160	HDR	64	59	42	51.2						P9	48	12.8	B-S	12	12.8	7.6
	3	129	HDR-H	64	69	44	51.2									B-S	12	12.8	9.8
	4	160	HDR	64	69	44	51.2						P9	48	12.8				9.6
Ascent	5	129	HDR-H	64	61	21	51.2									B-A	15	12.8	1.8
	6	002	LDR	32	61	21	25.6									B-A	15	6.4	1.8
Orbit	7	129	HDR-H	64	62	22	51.2									B-A	15	12.8	2.8
	8	002	LDR	32	62	22	25.6									B-A	15	6.4	2.8
	9	161	HDR	64	62	22	51.2	S2	24	12.8									2.4
	10	003	LDR	32	62	22	25.6	S2	24	6.4									2.1
	11	129	HDR-H	64	62	22	51.2									S-2	24	12.8	2.4
	12	002	LDR	32	62	22	25.6									S-2	24	6.4	2.4
Entry C/O	13	162	HDR	64	68	32	51.2	S2	24	12.8									2.4
	14	004	LDR	32	68	32	25.6	S2	24	6.4									2.4
Entry	15	129	HDR-H	64	63	23	51.2									B-E	13	12.8	8.8
	16	164	HDR	32	63	23	51.2									B-E	13	12.8	8.8
	17	005	LDR	32	63	23	25.6									B-E	14	12.8	3.8
	18	162	HDR	64	63	23	51.2	S2	24	12.8									3.4
	19	004	LDR	32	63	23	25.6	S2	24	6.4									3.4
GPC Utility	20	163	HDR	51.2	62	22	51.2	S2	24	12.8					OPS 0	20	12.8		2.4,0
	21	006	LDR	25.6	62	22	25.6	S2	24	6.4					OPS 0	20	6.4		2.4,0
GPC/MM C/O	22	163	HDR	51.2	62	22	51.2	S2	24	12.8					P9	48	12.8		2.4,6
	23	006	LDR	25.6	62	22	25.6	S2	24	6.4					P9	48	6.4		2.4,6
"SICK GPC" or HISAM DUMP	163 (note 6)	HDR LDR	51.2 25.6	62 62	22 22	51.2 25.6	S2 S2	24 24	12.8 12.8					NA NA	90 90	12.8 6.4			2.4 2.4

- NOTES: 1. The main and mass memory dump downlist ID's are considered special cases and do not require additional combinations.
2. HDR-H equals high data rate in the IARD 128 KBPS PROM format. All other ID formats are Telemetry Format Load (TFL) RAM formats.
3. B-S equals Backup in standby, B-A equals backup in ascent mode, and B-E equals backup in entry mode.
4. Combinations 11 and 12 require a manual toggle buffer assignment change for S2.
5. Band Width (BW) refers to the share of the telemetry allotted to the data.
6. Downlist dump may be skewed with respect to PCM telemetry output frame.

ERROR PCM fault message will be generated and will appear on all CRT's driven by the PASS. A loss of downlist could also be caused by the loss of an IP data bus or a PCMMU MIA. These last two problems would cause a downlist which would only be detectable by the ground.

If the downlist GNC GPC fails hard (loss of sync, software halt, etc.), the PASS software will automatically reassign a healthy GPC to take over the role of supplying downlist data to toggle buffer 1. The PCMMU would then have a good set of PASS GNC downlist data to incorporate into the PCMMU output.

If the loss of downlist is caused by an IP or PCMMU failure, this failure may be corrected by switching over to the other PCMMU via the OI PCMMU power switch on panel C3. This switchover may be done during the dynamic flight phases but requires using only the fixed format for the 128 kbps formatter since the RAM's are volatile in the new PCMMU. Loading Telemetry Format Loads (TFL's) into the new PCMMU during ascent or entry requires BFS to reestablish the RAM.

During coasting flight, downlist may be recovered in similar ways. The PCMMU toggle buffer designations may also be reassigned via uplink or GPC MEMORY SPEC keyboard entries.

4.8.3.3 Downlist Variable Parameter List. Item entries 25-34, located in the lower right-hand corner of the DPS UTILITY SPEC, are used to control which parameters are placed in 10 variable parameter slots of each downlist format. Items 25-34 identify which parameters according to their hexadecimal main memory addresses are to be placed into the variable parameter list (one 16-bit word per slot). An entry of an improper address will result in an ILLEGAL ENTRY fault message.

An entry for one of Items 25-34 would immediately tell the downlist formatter to incorporate the parameter identified into the variable parameter slot for inclusion in the downlist. Any changes to the VARIABLE PARAMETER ID LIST become effective immediately. Typically, the ground uses its DEU Equivalent uplink capability to change these during flight.

4.8.4 Memory Dumps. The capability exists to DUMP selected equivalent of GPC main memory and portions of the Mass Memory to the ground by replacing the nominal downlist data with the specific DUMP data. GPC main memory may be dumped using controls on the GPC MEMORY SPEC or via uplink commands. Mass Memory may be dumped via inputs to the MASS MEMORY R/W SPEC, or via uplink commands. In both cases, if the dumps are performed by the flight crew, all of the keyboard entries will be coordinated with the MCC flight control team. For any dump operation, the dump format will replace the nominal data for at least one data cycle but only as long as it takes to get the data dumped once.

In the case where the dump request would require more than one data cycle to complete, the dump downlist format would remain in effect until the dump was completed. As soon as the dump is completed, the nominal downlist format would be restored. These memory dumps would result in the loss of at least one downlist format data cycle, which would be replaced by the dump frames and fill data.

4.8.4.1 GPC Main Memory Dump. A GPC main memory dump would normally be used for MCC verification of selected portions of a GPC's main memory after an OPS transition caused a change in the software content of that GPC. Presently, the capability to dump a GPC's main memory exists in all MC except MC1 (Ascent) GPC MEMORY SPEC keyboard entries (via onboard or uplink). The dump will occur in those GPC's which are listening to the DEU which is supporting this SPEC at the time of the dump. A dump of a GNC GPC requires about 2 minutes to complete in High Bit Rate (HBR).

The capability also exists to dump a GPC using the panel M042F GPC MEMORY DUMP rotary switch when a GPC has been moded from HALT to STBY with its OUTPUT switch in TERMINATE (panel 06). This specialized configuration will be primarily used to dump memory of GPC's which have failed and takes about 4 minutes in HBR to complete.

4.8.4.2 Mass Memory Dump. The Mass Memory dump capability, which can be accomplished either via uplink commands or via crew keyboard entries to the MASS MEMORY R/W SPEC, will not normally be used inflight. This capability exists only in MC 4 (SM OPS 2) and in MC 6 (PL OPS 9).

The MASS MEMORY R/W SPEC, illustrated in figure 4-18, is available as SPEC 85 in SM OPS 2 and as the PL OPS 901 major mode (OPS) display. It can allow the crew or ground control the capability to observe selected Mass Memory data on the CRT, modify this data, and dump selected Mass Memory data to the ground via the downlist. Once the MMU software system, phase, and load block (Items 40-44) are specified, the dump is initiated (Item 52). STATUS indicators and the checksum value are displayed when the data is read from the MMU, and the dump operation occurs.

Dumps of Mass Memory data are limited to 2048 16-bit words in SM OPS 2 and limited to 16,384 16-bit words during PL OPS 9. As you will recall, the downlist frame length for both GPC main memory dumps and for Mass Memory dumps is controlled via the control in the GPC MEMORY SPEC. The Mass Memory to be dumped, the data to be dumped, and the request for the dump are controlled via the MASS MEMORY R/W display.

4.9 UPLINK

Uplink is the method by which ground commands, originating in the Mission Control Center, are formatted, generated, and transmitted to the Orbiter for validation, processing, and eventual execution by onboard software. This capability allows the ground to control software processing, effect mode changes in Orbiter hardware, and to store or change software in GPC main memory and Mass Memory.

Figure 4-22 illustrates the functional operational uplink data flow. Commands are issued at MCC consoles which request uplink communications. These command requests are formatted by the Shuttle Data Processing Complex into what is called a command load and transmits this command load to the Network Output Multiplexer (NOM).

The primary method of uplink involves the output of the NOM being transmitted to the JSC DOME SAT Transmitter (XMTR), which transmits the operational uplink to a TDRS remote site through a DOME SAT. The TDRS remote site XMTR then relays the operational uplink to the Orbiter through a TDRS, to either a Ku-band receiver or an S-band receiver onboard the Orbiter.

The Ku-band XPONDER RCVR demodulates the received data and voice and ship it to the Ku-band signal processor where the signal is validated and the commands separated from the voice. The uplink commands are then transferred to the NSP. If received by the S-band XPONDER RCVR, the operational uplink will be sent to the NSP's, which separates commands from voice. An NSP will buffer the uplink commands until requested by GPC system software.

The Orbiter's S-band transponder receiver (XPNDR RCVR) demodulates this received operational uplink and transmits it to the NSP which validates and separates the commands from the voice. The DPS MDM's format the commands and transmit them to the GPC's when requested by systems software. The uplink processor software within the GPC(s) executes commands to control software operations, store, or change software in GPC or Mass Memory, and effect mode changes in Orbiter hardware.

In the secondary uplink method the NOM mixes the command loads with voice and ships this operational uplink to the GSFC, which distributes it to the appropriate STDN remote site for transmission to the Orbiter.

4.9.1 Uplink Command Description. Uplink commands can be issued to a GPC by number (GPC 1, GPC 2, etc), by major function (ALL GNC, ALL SM, ALL PL), all active GPC's in the common set, or to the BFS GPC. An OP CODE identifies which operation is to be performed. MCC builds commands loads to perform certain functions as identified by the OP code of the command.

There are three types of uplink command loads. These are the single stage commands, the critical (or two-stage) commands, and the stored program commands (which are actually a special case of the critical commands).

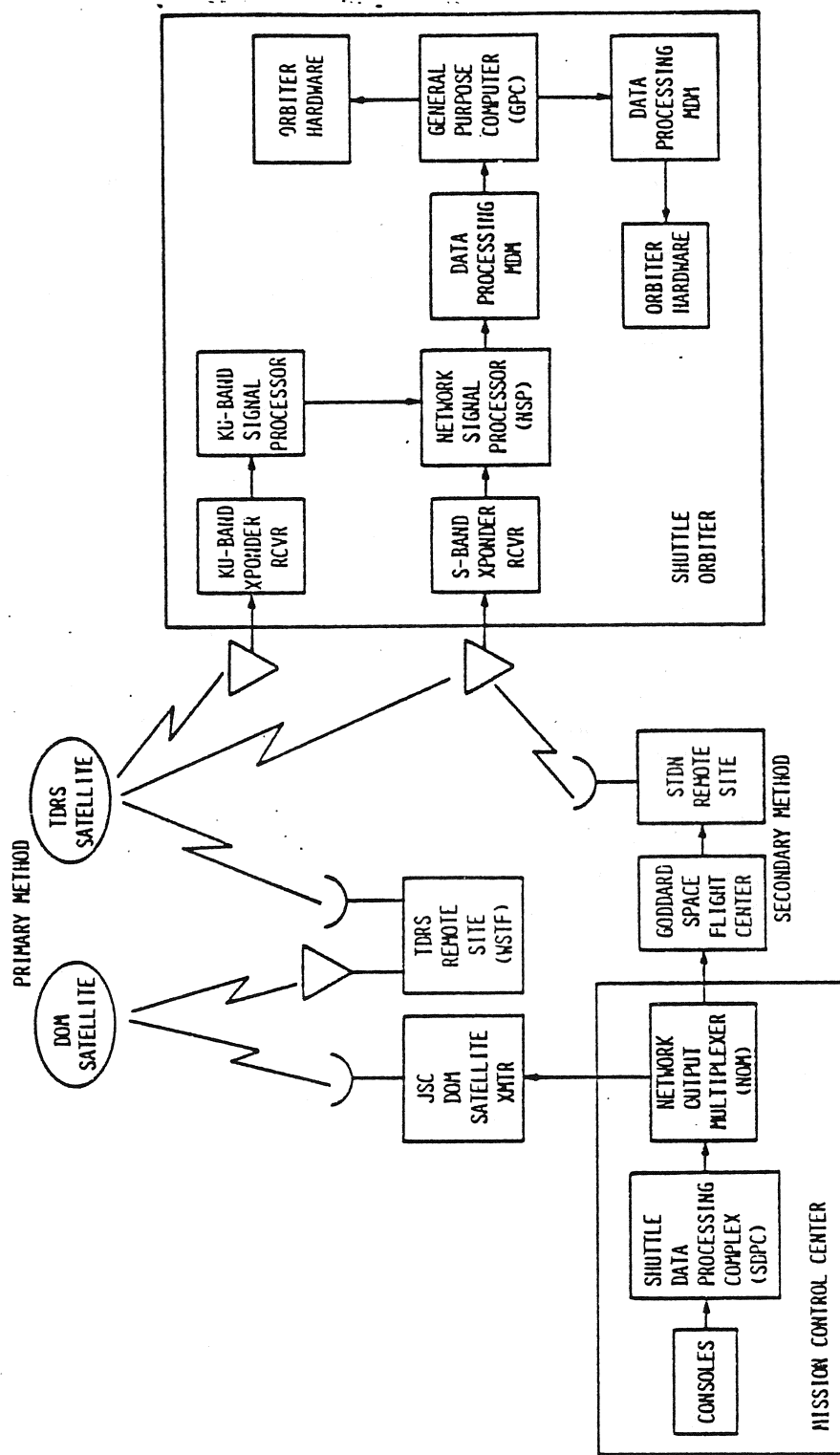


Figure 4-22. Functional Uplink Data Flow

Single stage commands, upon reception, will be buffered and executed by the uplink processor software.

All critical commands, when received, will be buffered by the uplink processor software. The content of this buffer is then downlisted for command verification (onboard verification is available via the GPC MEMORY SPEC). While a command is stored in the 2-stage buffer, the UL indicator appears on all CRT displays associated with the GPC. When the uplink processor software receives a BUFFER EXECUTE single stage command, it will send a flag to the appropriate software modules to execute the buffered command and blank the UL indicator.

The stored program commands are buffered in the same fashion as the two-stage commands, except that they are time-tagged, and will be executed when the GMT in the command load equals the GPC's GMT. These stored program commands are used to set or reset MDM discrete outputs.

The following table shows a subset of the commonly used types of uplink commands.

TABLE 4-10. UPLINK COMMANDS

SINGLE STAGE	TWO STAGE	STORED PROGRAM
TWO STAGE BUFFER CLEAR SPEC BUFFER CLEAR TWO STAGE BUFFER EXECUTE WORD BY WORD CORRECTION OF TWO STAGE BUFFER MDM DISCRETES (REAL TIME COMMAND) UL INDICATOR ON/OFF	GPC MEMORY WRITE MULTIPLE MDM DISCRETES EQUIVALENT DEU MASS MEMORY WRITE KU BAND ANTENNA CONTROLS/BIAS IMU REFSMMAT/BIAS TABLE MAINTENANCE BLOCK UPDATE GUIDANCE POLYNOMIALS LAUNCH/ON-ORBIT/ENTRY TARGETING LOADS TDRS/TACAN/LANDING SITE PARAMETERS ADI QUATERNIONS PAYLOAD CONFIGURATION DATA ATTITUDE TIMELINE VEHICLE INERTIA MATRIX ORBITER STATE VECTOR RENDEZVOUS VEHICLE STATE VECTOR	MDM DISCRETES

4.9.1.1 DPS Uplink Commands. The uplink commands which relate directly to the DPS include commands used to set or reset discrete outputs for a particular DPS MDM discrete output module channel. Up to 16 discrete outputs can be set or

reset in a single command load. This process is also known as a Real Time Command (RTC). Two DPS MDM discrete output module channels can have their outputs set or reset each time the two-stage command is executed (either via a buffer-execute command or a GMT time of execution). The MDM's in consideration for these last two items are the four FF MDM's, the four FA MDM's, the PL MDM'S, and the LF and LA MDM's. An RTC load includes an RTC to reset the MDM discrete output channels to zero and a second RTC to set the appropriate MDM discrete output channels to one.

The DPS uplink commands can also be used to write over GPC main memory, either in contiguous or in scattered locations except in Memory Configuration 1. The capability also exists to read, write, or dump Mass Memory words in SM OPS 2 or PL OPS 9.

One form of DPS uplink commands, known as the DEU equivalent commands, allows the ground to perform most of the functions the flight crew could perform, as if the ground had its own keyboard. The DEU equivalent commands from the ground go through the NSP to the GPC two-stage buffer and when executed are transferred to the equivalent DEU input table. An event is set to signal the MCDS input processor that a message is waiting, and the input processor transfers the data into the DEU input table, and the standard keyboard message processing takes over. At this point, the ground interacts with the GPC in exactly the same manner as the crew. In other words, the ground has the capability, via uplink, to activate or deactivate SPEC software, mode the current OPS, make item entries, etc., as if keyboard entries were made onboard. A CRT format activated via uplink is charged to the major function addressed (e.g., one of the SPEC's is used). In addition, if the DEU/DU combination is powered up, the SPEC or DISP activated via uplink will appear on the CRT.

DPS uplink commands can also clear or execute the two stage command buffer, clear the stored program command buffer, correct the two stage command buffer, and turn the UL (uplink) indicators (on the title line of the CRT display formats) on or off. Single stage and stored program commands are allowed in every MC, whereas two-stage commands are processed only in specified MC's.

4.9.2 NSP/MDM/GPC Interface. The Orbiter NSP's 1 and 2 are hardwired to the DPS FF MDM's FF1 and FF3, as shown in figure 4-23. The NSP's store the uplinked command loads until they are requested by the GPC's via these two MDM's. The GPC's also read the NSP BCE bypass status and power status in order to determine which NSP is powered up and therefore is to be polled.

The GPC that is in charge of the string containing the active NSP initiates the request for the NSP to send its data over the FC data buses (referred to as polling the NSP). The NSP responds by sending the data to all of the GPC's which are listening to the critical data buses. Assuming the BFS GPC is tracking the PASS, it too can receive uplink commands. Those PASS GPC's which are not listening to the FC data buses will receive the NSP status and command over the ICC data buses as it is sent to them by the other GPC's. At the next processing cycle, all GPC's will initiate their processing of the uplink command.

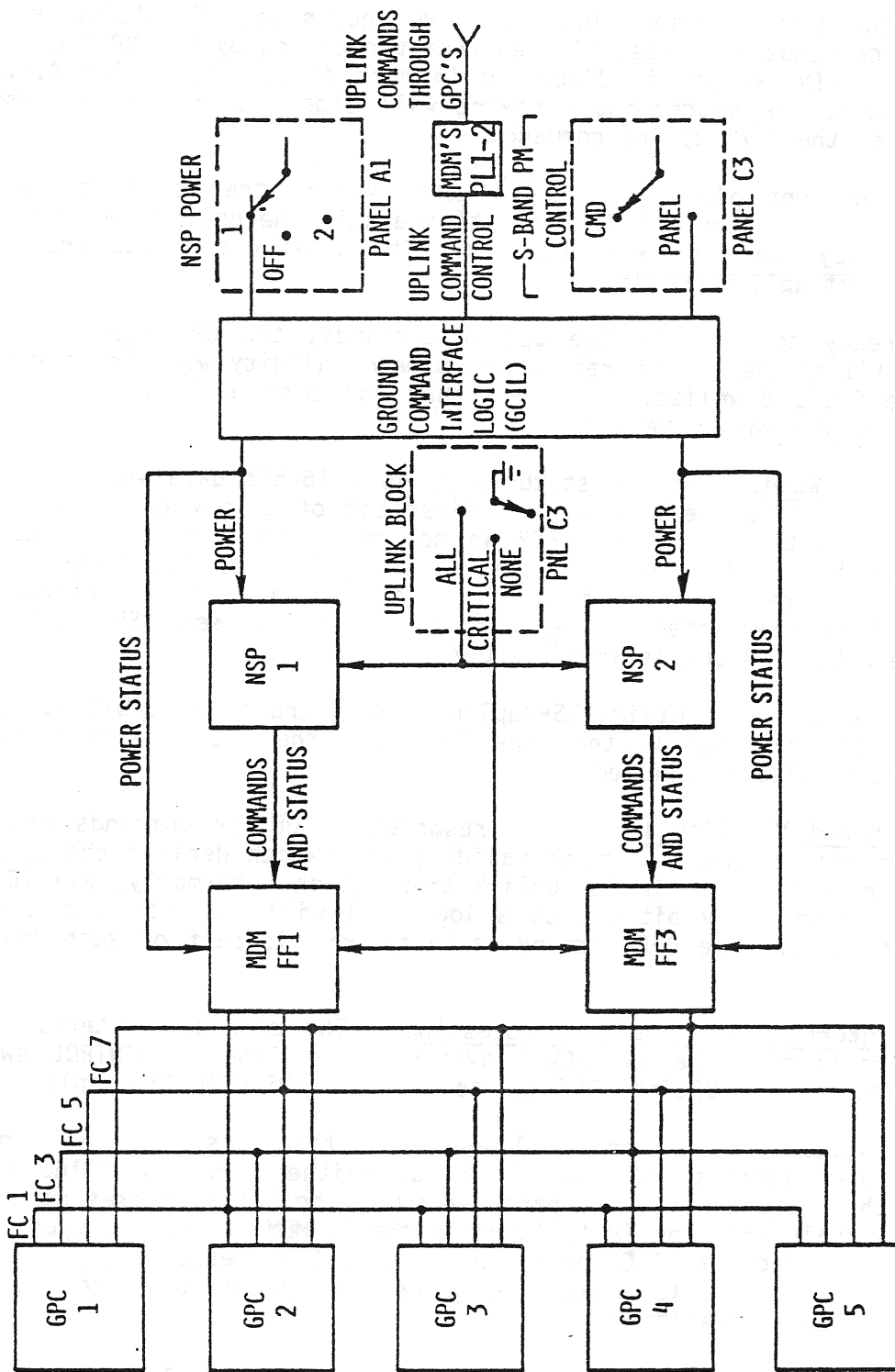


Figure 4-23. NSP/MDM/GPC Interface Diagram

After receiving the uplink command load, the GPC checks the NSP status word to determine if all commands have been blocked from processing by the UPLINK switch (panel C3). The UPLINK switch is discussed in more detail in section 4.9.2.3. If they have, the uplink processing software will stop its command processing and wait to process the next uplink command.

If all commands are not blocked by the UPLINK switch, the uplink processing software checks to see if the NSP is ready to transmit the uplink commands. If the NSP is not ready, the uplink processing software will stop its processing and wait for the next uplink command.

If the NSP is ready to transmit the uplink commands, the GPC receives these commands and validates them. The resulting command validity word is stored for inclusion in the GPC's downlist. Assuming that the command is valid, the GPC proceeds to perform the valid operation.

4.9.2.1 NSP Status Word. The NSP status word is a 16-bit data word that conveys the NSP condition to the GPC's. The first bit of this word, if set to a logical 1, tells the GPC's that the NSP is not ready to transmit its command data. The second bit of this word is controlled by the NSP BLOCK position of the UPLINK switch. The remaining bits (3-16) contain NSP status information. This status word is downlisted and allows the ground to see NSP status and determine if the UPLINK switch is in NSP BLOCK.

The NSP Validity Word also contains NSP/uplink status and is a 16-bit word. In particular, bit 16 indicates whether the GPC sees the UPLINK switch in GPC BLOCK. This word is also downlisted.

4.9.2.2 GPC Command Validity Word. In response to uplink commands from the NSP, each GPC creates a 16-bit command validity word which defines the possible errors that may have occurred in the uplink transaction. Normally, all 16 bits of this word are zero. Any bit set to a logical 1 will indicate a problem in the command processing. The GPC command validity word is part of each downlist at a 1 Hz rate.

4.9.2.3 Crew Interface With Uplink Processing. The crew can interface with uplink processing through the NSP POWER switch, the S-BAND PM CONTROL switch, the UPLINK SWITCH, and the UPLINK CONTROL items on the DPS UTILITY display.

The NSP POWER switch, located on panel A4, is a three-position dual contact switch which allows power to NSP 1, NSP 2, or neither, as controlled by the GCIL. Whether the GCIL looks at the panel A4 switch position or uses reconfiguration control signals from the GPC's (through the PL MDM's) depends upon the S-BAND PM CONTROL switch on panel C3 being in PANEL or CMD, respectively. The CMD position is used primarily to allow the ground to reconfigure the S-BAND/PM switches without crew intervention.

The UPLINK switch, located on panel C3, is a three-position toggle switch. The possible switch positions are NSP BLOCK, GPC BLOCK, and ENABLE. In the NSP BLOCK position, a signal is sent to each NSP which causes the NSP to respond to GPC polling invalidly which then causes the GPC to declare an I/O ERROR on that NSP with a resulting BCE BYPASS. In this mode, the GPC stops polling the NSP's

and thus is blocked from UPLINK. If the switch is moved to either of the other two positions, an I/O RESET EXEC input must be received in order for the GPC to resume contact with the NSP. This switch position will not normally be used during NASA missions and will only be required on some DOD flights where uplink is required to be terminated in the hardware.

Selection of the GPC BLOCK switch position provides two discrete signals (one via FF1, one via FF3) to the GPC which will cause the uplink software to not be scheduled and thus no uplink data to be processed. Signals from both FF1 and FF3 must be present for this to occur. This switch position will be used during the Ascent and Entry phases which use the STDN (TDRS has a secure uplink capability which will not require this switch). Crew selection of this position will be called for by the CAPCOM when CONFIGURE LOS is requested. In going from GPC BLOCK to ENABLE, no I/O RESET EXEC is necessary to reenabling uplink processing.

Selection of the ENABLE switch position allows for all uplinks to be processed by the uplink software, depending upon the state of the SITE IN VIEW flag. During Ascent and Entry (with STDN) this position will be selected when the CAPCOM requests CONFIGURE AOS. For TDRS passes, this position is always selected since an encrypted uplink capability is available. The SITE IN VIEW flag is initialized enabled but can be set ON or OFF by the SM GPC, as determined by ANTENNA MANAGEMENT. Essentially, antenna management software determines whether the vehicle is AOS (Acquisition of Signal) or LOS (Loss of Signal), depending upon the vehicle's state vector and the location of predefined ground sites, and then sets the SITE IN VIEW flag appropriately. The software uses the SITE IN VIEW flag depending upon the software UPLINK CONTROL function. The crew interface with this function is through the UL CNTL items on the DPS UTILITY (Spec 1) display which is available in all OPS except OPS 1, 3, and 6. These items are only enacted if the UPLINK block switch is in ENABLE:

ITEM 35 - AUTO - Results in the GPC accepting or rejecting uplink processing depending upon the SITE IN VIEW flag.

ITEM 36 - ENA - Permits uplink processing regardless of the SITE IN VIEW flag.

ITEM 37 - INH - Inhibits the uplink software processing.

DPS UTILITY, SPEC 1, is initialized with Item 35 selected; however, when the GPC's are transitioned to GNC OPS 9 (prior to launch), Item 36 is selected. The selected items carry across OPS transitions. Operationally, it is important to have the ITEM 36 (ENA) selected when transitioning to an OPS in which no SM GPC is available to update the SITE IN VIEW flag.

4.9.2.4 Loss Of Uplink To the GPC's. A loss of uplink from the NSP's to the GPC's may occur if a problem exists either with the NSP, the data path between the NSP and the FF MDM it is hardwired to, with the MDM itself, with the data path between the GPC's and the MDM, or with the GPC(s) itself. Obviously, the cure for this loss of uplink is a function of what kind of failure caused this loss and where the failure occurred. An I/O error, detected when the NSP is polled by the GPC, will cause a BCE STRING X NSP fault message (X = 1, 3 implies

NSP 1 or NSP 2, respectively) to be generated, which will indicate that a problem exists with the specified NSP. If only one GPC of a four GPC redundant set (on ascent or entry) detects a problem, that GPC will force fail to sync and will be removed from the set.

If the NSP itself has failed, the NSP POWER switch on panel A1 may be used to select the other NSP if the S-band PM hardware is under panel control. Since this switch is in the aft crew station, this onboard fix would be unavailable during dynamic flight phases. During on-orbit phases the ground could send commands via the DPS UTILITY SPEC commands to the GCIL to select the correct NSP if the S-band PM hardware were under command control.

4.9.3 Real-Time Commands. A real-time command is the capability to set or reset discrete outputs for one channel of one discrete output module in one of the FF, FA, PL, LA, or LF MDM's. The onboard capability involves the DPS UTILITY SPEC and an item entry corresponding to the second word of an MDM single stage uplink command, which identifies the MDM, the I/O module, the discrete output channel, and whether the bits are to be set or reset and the third word of the MDM single-stage uplink command, which identifies which bits are to be set or reset as directed by the first four digits. All eight of the digits entered are hexadecimal notation via Item 13.

ITEM 14 EXEC sends the command to the system software which sets-up and transmits the required output word to the specified MDM.

SECTION 5

BACKUP FLIGHT SYSTEM SOFTWARE

5.1 BACKUP SYSTEMS SERVICES (BSS)

The BSS is the software in the backup flight system (BFS) which plays the same role in the BFS as the system software or FCOS does in the primary avionics software system (PASS). BSS software forms the interface between the applications program (guidance, navigation, and control (GNC), systems management (SM), and sequencing) and the outside world through uplink, downlink, the multifunctions CRT display system (MCDS), and the ground support equipment (GSE). The BSS provides for the output of commands and/or the retrieval of data from the PASS and the hardware external to the general purpose computers (GPC's) such as the avionics devices, caution and warning (C&W) electronics, the master timing unit (MTU), etc. BSS is also responsible for updating the BFS GPC's internal clock and making Greenwich Mean Time (GMT) and mission elapsed time (MET) available to the BFS applications programs.

5.2 ACTIVE PASS/BFS INTERFACE

The BFS is designed to perform limited SM during the ascent and entry phases and to take over vehicle control in case of a major failure in the PASS. When the BFS is not engaged (pre-engaged), the PASS GPC's control the flight critical (FC) data buses. Therefore, during GNC OPS 1, 3, and 6 the BFS GPC must track the PASS GPC's for receipt of data over the FC data buses and certain PASS-loaded or computed parameters such as the current vehicle state, the bus control element (BCE) chain element bypass status, Relative Velocity at ME OUT, the inertial measurement unit reference stable member matrix (REFSMMAT), etc. In order to accomplish this, the BFS GPC listens on the FC data buses. This also ensures that the BFS GPC can receive uplink and the MTU updates. In addition, the PASS GPC's send data known as PASS transfer data to the BFS GPC over the FC data buses up to 25 times-per-second.

To perform its SM functions, the BFS GPC assumes command of the payload (PL) data buses when the BFS GPC's mode switch is in RUN or when the BFS is engaged. The BFS GPC sends a BFS RUN discrete to the PASS GPC's which ensures the PASS will not also command on the PL data buses. Even without PL buses, BFS receives OI data.

The BFS GPC may also be assigned display keyboard (DK) DATA bus 4 and another DK DATA bus as a function of the BFC CRT display and select switches, the BFS GPC mode switch, or a GPC/CRT keyboard message. The BFS listens to all PASS-controlled DK buses in the preengaged state.

Once the BFS is engaged, no further interface is made between the BFS and the PASS GPC's. Figure 5-1 illustrates the PASS/BFS functional configuration.

5.2.1 PASS/BFS Discrete Interface. In addition to the interfaces previously mentioned the PASS and BFS GPC's have specialized discrete interfaces. The BFS

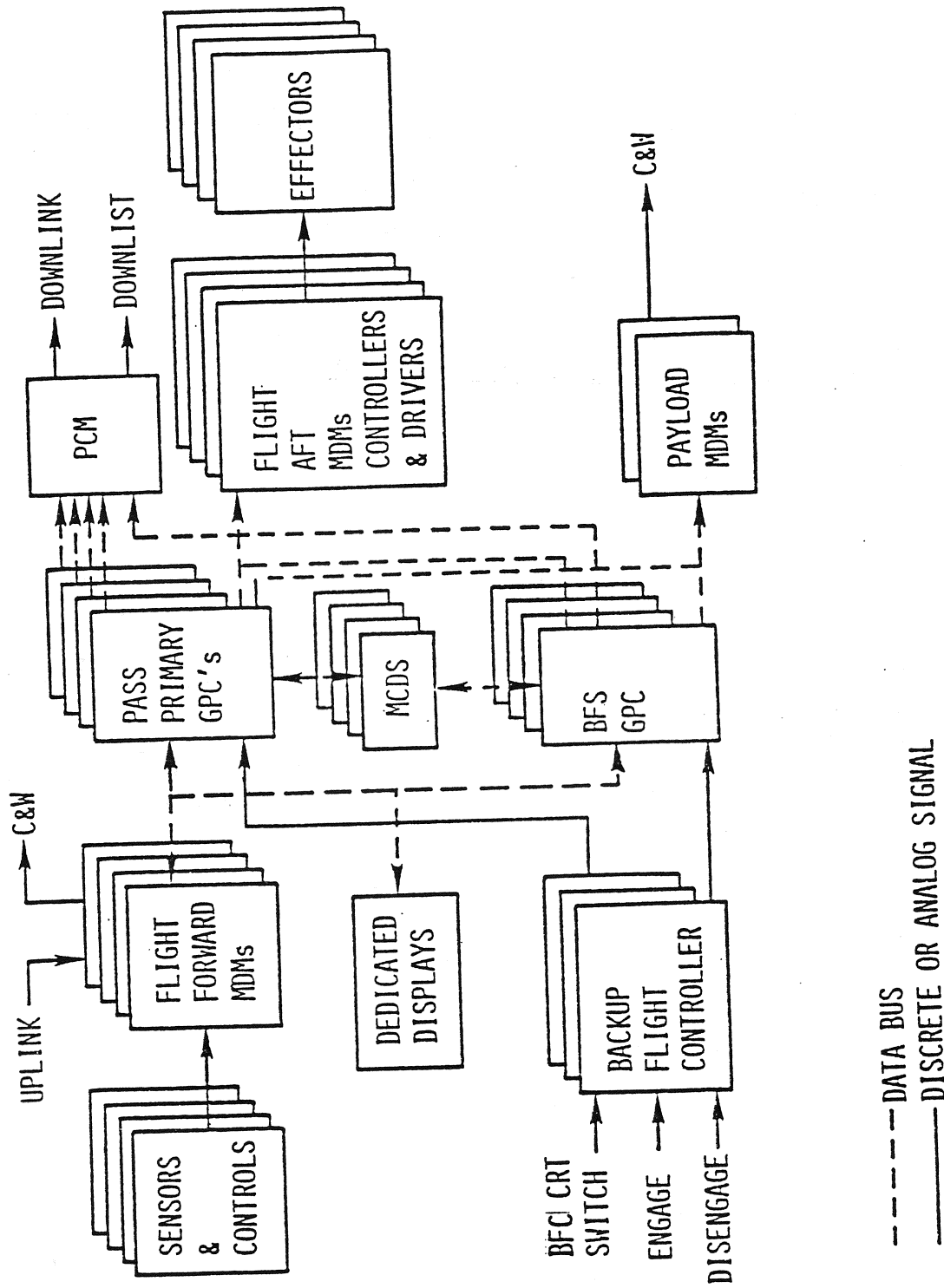


Figure 5-1. PASS/BFS Functional Configuration

must not interfere with the PASS GPC's synchronization schemes. Therefore the BFS GPC holds its three sync discrettes to a 000 pattern. When in the RUN mode, the BFS GPC issues its BFS RUN discrete to the PASS GPC's which tells the PASS to surrender control of the PL data buses and results in the BFS taking command of the PL data buses.

The BFS GPC will also not drive any GPC FAIL discrettes or any GPC STATUS matrix lights other than its own diagonal. It will drive its own diagonal if its watchdog timer times out. Conversely, the PASS GPC's will not issue GPC FAIL discrettes or light GPC STATUS matrix lights for the BFS GPC.

5.2.2 BFS ENGAGE Condition. The BFS GPC is engaged following the BFS GPC's OUTPUT switch being placed in the BACKUP position and depression of the ENGAGE pushbutton on either the left or right RHC. The outputs of these switches (the OUTPUT switch and ENGAGE pushbutton) are sent to the backup flight control (BFC) modules. The BFC outputs the BFS ENGAGE discrettes (1, 2, 3) and I/O TERMINATE B. PASS notification of the BFS GPC ENGAGE condition is discrete output I/O TERMINATE B = 1 and discrete inputs 1, 2, 3 = 1. The PASS responds by relinquishing command capability on all data buses within 200 msec and by entering software HALT. The BSS changes BFS operations from disengaged to engaged when at least two BFS ENGAGE 1, 2, and 3 discrettes change to 1's from zeroes and the I/O TERMINATE B discrete = 0. At this time, the BFS GPC will takeover command of the FC data buses, an additional cathode ray tube (CRT) and the PL data buses, (if it were not already in command of the PL data buses), and assumes vehicle control.

The Orbiter flight crew has available to them a series of indications which show that the BFS has been engaged. The BFS software illuminates a BFC light on panel F2 and on panel F4 (the eyebrow panels) via the PL forward MDM PF2. The BFS GPC OUTPUT talkback on panel O6 will go gray, while the OUTPUT talkbacks of the PASS GPC's go to barberpole. Any PASS GPC's in RUN will light their diagonal lights on the GPC STATUS matrix, and illuminate the GPC light on the 40-light C&W matrix (panel F7). The two CRT's indicated on the BFC CRT select switch will be driven by the BFS GPC if the BFS CRT display switch is in the ON position. If this switch is in the OFF position, the BFS GPC will drive CRT's 1 and 2. Those CRT's which are not controlled by the BFS GPC will show a big X across the CRT screen, and the message POLL FAIL will appear on the right side of the scratch pad line. These are the same indications that occur under other circumstances when a DEU does not receive GPC update commands for a 3-second period.

5.2.3 BFS DISENGAGE Condition. The BFC DISENGAGE switch, located on panel F6, is used to disengage the BFS. Response to this switch inverts the BFS ENGAGE 1, 2, and 3, and I/O TERMINATE B discrete inputs. When the BFS GPC detects the I/O TERM B = 1 and BFS ENGAGE 1=2=3=0, the BFS enters the DISENGAGED-STAND ALONE STATE (stops FC output, continues software processing independent of the PASS and releases control of the second Display Electronics Unit).

If the PASS has undergone initial program load (IPL), has been moded to RUN and to the appropriate GNC OPS/Major Mode, and sees the BFS ENGAGE 1, 2, 3, and I/O TERMINATE B discrettes = 0, the PASS will assume control of the FC data buses and

the vehicle. If the PASS has not undergone a new IPL, it may remain in software HALT, resulting in no vehicle control.

A BFS GPC power transient could cause an inadvertent BFS GPC disengage due to the BFC power reset. The BFS GPC can again be engaged via a repeat of the BFC ENGAGE command via a BFC ENGAGE pushbutton.

When the BFS is disengaged the BFC light on panels F2 and F4 will be extinguished and the BFS GPC's OUTPUT talkback will go to barberpole. If the PASS had undergone a new IPL, the PASS GPC's will extinguish their GPC STATUS matrix lights and thus the GPC light on the C&W panel. The PASS GPC's will also take control of their assigned DK buses, except for the first CRT allocated to the BFS via the BFC CRT switches. In addition, the PASS GPC's OUTPUT talkbacks will go gray.

5.2.4 Effects of GPC MODE Switch. When the BFS GPC receives HALT discrete, its active software is terminated, which puts it in a hardware controlled state. The OUTPUT talkback and MODE talkback will go barberpole. Note that a GPC must be in HALT in order to begin the IPL sequence. The transition from STANDBY or RUN to HALT is illustrated in figure 5-2.

When the BFS GPC's mode switch is in STANDBY, (and it is not engaged), the software processing is identical to that done in the RUN position except that the BFS GPC will not take control of the PL data buses. A BFS GPC in STANDBY and engaged is operationally the same as if it were in the RUN mode. It will gain control of the PL data buses as well as the FC data buses and the two selected DK buses.

When the BFS GPC is in the RUN mode, it sets the BFS RUN discrete output and assumes command of the PL data buses within 2 seconds. The PASS GPC's accordingly, set bus masks on the PL data buses upon receipt of the BFS RUN discrete. In the RUN mode, the BFS GPC continues the software processing associated with its current major mode and state (tracking PASS or not).

5.2.5 BFS CRT Selection. BFS GPC control of the selected forward station CRT's is controlled by the BFC CRT display and select switches which are illustrated in figure 3-4 and by a backup method using the GPC/CRT key. The BFC CRT display switch permits power to the select switch which allows BFS GPC control of the designated DK data bus and therefore the designated CRT. When the BFS is engaged, the BFS GPC will take control of CRT's 1 and 2. Note here that if the IPL source SELECT switch on panel 06 is moved to either the MMU 1 or MMU 2 position, the BFS GPC will give up control of the first indicated CRT/DK bus. The reason for this bus surrender is the IPL procedure. If another GPC undergoes IPL at this time (with the BFC CRT DISPLAY switch ON), it will take control of this DK bus in order to generate the GPC IPL MENU display. If the BFS GPC has not given up this DK bus, both GPC's would be commanding over the same data bus with unpredictable results (one indication is a flashing CRT).

Input of the GPC/CRT key, followed by two digits corresponding to the desired GPC commander (first digit) and the desired CRT (second digit) is another method

TO FROM	HALT		STANDBY		RUN		
	PRE-ENGAGE	POST-ENGAGE	PRE-ENGAGE	POST-ENGAGE	PRE-ENGAGE	POST-ENGAGE	
HALT	<ul style="list-style-type: none"> ● RETURN TO A HARDWARE CONTROLLED STATE 		<ul style="list-style-type: none"> ● PERFORM SYSTEMS RESET ● ATTEMPT TO "TRACK" THE PASS GPC's ● ENTER BFS OPS 0 STATE (DISCUSSED LATER) ● OUTPUT TALKBACK TO GRAY IF ENGAGED ● OUTPUT TALKBACK REMAINS BARBERPOLE PRE-ENGAGE ● GENERATE "BFS RUN" DISCRETE AND GAIN CONTROL OF THE PL DATA BUSES IF IN RUN OR STANDBY ENGAGED 		<ul style="list-style-type: none"> ● GENERATE "BFS RUN" DISCRETE AND GAIN CONTROL OF THE PL DATA BUSES 		RUN IS THE SAME AS STANDBY
STANDBY	<ul style="list-style-type: none"> ● OUTPUT TALKBACK TO BARBERPOLE ● RESET "BFS RUN" DISCRETE AND RELINQUISH CONTROL OF THE PL DATA BUSES 		STANDBY IS THE SAME AS RUN		RUN IS THE SAME AS STANDBY		
RUN	<ul style="list-style-type: none"> ● RESET "BFS RUN" DISCRETE AND RELINQUISH CONTROL OF THE PL DATA BUSES 		STANDBY IS THE SAME AS RUN		RUN IS THE SAME AS STANDBY		

Figure 5-2. BFS GPC Mode Transitions Post-IPL

for assigning/deassigning BFS control of any DEU. This method would be used following BFC CRT select switch failure or in case the user desires to assign more than one CRT to the BFS. The BFS GPC will respond to GPC/CRT key inputs from either a PASS or BFS keyboard as long as the desired GPC commander is BFS GPC. The BFS GPC uses DK listen to receive inputs from a PASS keyboard. The reverse, however, is not true, so the GPC/CRT command should be made on a PASS keyboard.

5.3 BFS OPS/MAJOR MODES/DISPLAYS

Essentially, the BFS will support identical GNC OPS/major modes as the PASS does during ascent, entry, R_{TLS}, and TAL Abort entry, (memory configurations 1, 3, and 6). In the SM major function, the BFS only supports one OPS/major mode. It should be noted that the BFS also supports a transition state called BFS OPS 0, which is not the same as the PASS GPC OPS 0 state.

5.3.1 BFS OPS 0. BFS OPS 0 is the state which is used to begin scheduled software processing following IPL or a HALT to STANDBY or RUN transition (System Reset). It can also be entered in MM 106,305, and 603 by crew entry of OPS 000 PRO to a BFS-controlled keyboard. The transition from BFS OPS 0 to OPS/major mode 101 or 301 is, in turn, initiated by an OPS 101 PRO or OPS 301 PRO BFS keyboard entry.

In BFS OPS 0, all outputs over the FC data buses are inhibited. If the BFS is tracking the PASS, it will receive FC data inputs through the active PASS/BFS interface, but the BFS GPC will not process any GNC software in OPS 0. However, it will support monitoring of the GPC mode and GPC output switches and display of the FAULT SUMM display, the BFS MEMORY SPEC, and the SM displays. This software state will also support downlist, SM processing, and if the active PASS/BFS interface exists (and therefore BFS communication with the network signal processors), it will also support uplink. It also supports data bus configuration control, ENGAGE/DISENGAGE monitoring, DK data bus input/output (I/O), and instrumentation data I/O via the IP data bus. The OPS display for BFS OPS 0 is the BFS MEMORY SPEC.

Regardless of the ENGAGE condition, no GNC software processing takes place in BFS OPS 0. It requires a keyboard entry of OPS 101 PRO or OPS 301 PRO to a BFS keyboard to leave OPS 0.

5.3.2 BFS OPS/Major Mode Transitions. The BFS GPC can be moded from one OPS to another only by a crew input of OPS XYZ PRO to a BFS controlled keyboard. This includes transitions to OPS 0, OPS 1, and OPS 3. Within an OPS, transitions between major modes may be made several ways. The BFS does listen on PASS controlled DK buses as well as BFS controlled DK buses for keyboard entries to sequence major modes. Also, the BFS monitors other systems such as the solid rocket boosters (SRB's) to determine if moding is appropriate. Based on these factors, the BFS will sequence from one major mode to another. A transition from OPS 0 to OPS 3 causes the BFS to sync up with the MTU and re-initialize IMU RM. Table 5-1 indicates the criteria for OPS/major mode transitions.

5.3.3 BFS CRT Displays. The BFS GPC supports a limited number of specialist functions (SPEC's) and display functions (DISP's). As is the case with the

TABLE 5-1
OPS TRANSITION/SELECTION

IF GPC-IPL=====	OPS 000;
IF SYSTEM-RESET=====	OPS 000;
OPS 000: If BFS not engaged	
then if OPS 101 PRO entered=====	OPS 101;
OR if OPS 301 PRO entered=====	OPS 301;
If BFS engaged	
then if OPS 301 PRO entered=====	OPS 301;
OPS 101: If SRB chamber pressure > 50 PSIA=====	OPS 102;
If -3.2 sec timer expired=====	OPS 102;
If OPS 000 PRO entered=====	OPS 000;
OPS 102: If SRB-SEP completed=====	OPS 103;
If OPS 103 PRO entered=====	OPS 103;
If OPS 103 PRO entered in PASS=====	OPS 103;
If OPS 601 PRO entered=====	OPS 601;
If OPS 601 PRO entered in PASS=====	OPS 601;
If RTLS selected=====	OPS 601;
OPS 103: If DELTA-V-Z-AUTO-TRANS completed=====	OPS 104;
If OPS 104 PRO entered=====	OPS 104;
If OPS 104 PRO entered in PASS=====	OPS 104;
If OPS 601 PRO entered=====	OPS 601;
If OPS 601 PRO entered in PASS=====	OPS 601;
If RTLS selected=====	OPS 601;
OPS 104: If OPS 105 PRO entered=====	OPS 105;
If OPS 105 PRO entered in PASS=====	OPS 105;
If OPS 602 PRO entered=====	OPS 602;
If OPS 602 PRO entered in PASS=====	OPS 602;
If RTLS selected=====	OPS 602;
If OPS 301 PRO entered=====	OPS 301;
OPS 105: If OPS 106 PRO entered=====	OPS 106;
If OPS 106 PRO entered in PASS=====	OPS 106;
If OPS 301 PRO entered=====	OPS 301;
OPS 106: If OPS 301 PRO entered=====	OPS 301;
If OPS 000 PRO entered=====	OPS 000;
OPS 301: If OPS 302 PRO entered=====	OPS 302;
If OPS 302 PRO entered in PASS=====	OPS 302;
If OPS 000 PRO entered=====	OPS 000;

TABLE 5-1 (Continued)
OPS TRANSITION/SELECTION

OPS 302:	If OPS 303 PRO entered=====	OPS 303;
	If OPS 303 PRO entered in PASS=====	OPS 303;
	If OPS 301 PRO entered, and prior to OMS Burn "EXEC" or after OMS purge complete=====	OPS 301;
OPS 303:	If OPS 304 PRO entered=====	OPS 304;
	If OPS 304 PRO entered in PASS=====	OPS 304;
	If OPS 301 PRO entered=====	OPS 301;
	If OPS 301 PRO entered in PASS=====	OPS 301;
OPS 304:	If TAEM-Interface achieved=====	OPS 305;
	If OPS 305 PRO entered=====	OPS 305;
	If OPS 305 PRO entered in PASS=====	OPS 305;
OPS 305:	If OPS 000 PRO entered and rollout flag set=====	OPS 000;
OPS 601:	If ET SEP complete=====	OPS 602;
	If OPS 602 PRO entered=====	OPS 602;
	If OPS 602 PRO entered in PASS=====	OPS 602;
OPS 602:	If Velocity x FPS and no ET Fast Sep=====	OPS 603;
	If OPS 603 PRO entered=====	OPS 603;
	If OPS 603 PRO entered in PASS=====	OPS 603;
OPS 603:	If OPS 000 PRO entered and rollout flag=====	OPS 000;

PASS, each BFS SPEC and DISP is given a three-digit number by which the SPEC or DISP is called up using a SPEC ABC PRO keyboard entry to the BFS-controlled keyboard. The distinction between SPEC's and DISP's is the same as that of the PASS SPEC's and DISP's, and the BFS SYS SUMM displays (GNC and SM) are called using the SYS SUMM key on the BFS keyboard. Also, as in the PASS, the FAULT page may be called via the FAULT key on the keyboard or via SPEC 99 PRO to clear the FAULT page. Any BFS display will contain the notation BFS in the upper-right portion of the display next to the CRT timer (line 2).

5.3.3.1 System Displays. The following displays are available at all times in any supported major function where the keyboard invocation is also listed:

<u>Display</u>	<u>Keystrokes</u>
BFS MEMORY (figure 5-3)	SPEC 0 PRO
FAULT	SPEC 99 PRO, FAULT

5.3.3.2 Payload Displays. No displays are supported for this major function. If payload is selected as the new major function from the requesting MCDS, and if the previous major function was not payload, the previous major function is maintained.

5.3.3.3 GN&C Displays. The BFS Memory display is supported for OPS 0, major mode 000.

The following major mode displays are supported for OPS 1:

<u>Display</u>	<u>Major Mode</u>
LAUNCH TRAJ 1	101
ASCENT/ATO/RTLS/TRAJ 1	102
ASCENT/ATO/RTLS/TRAJ 2	103
OSM/ATO/AOA 1 MNVR EXEC	104
OSM/ATO/AOA 2 MNVR EXEC	105
OSM/ATO/AOA 2 MNVR COAST	106

The following SPEC displays are available at any time during OPS 1. The keyboard selection required to invoke the displays is also listed.

<u>Display</u>	<u>Keystrokes</u>
GNC SYS SUMM 1	SPEC 18 PRO, SYS SUMM
GNC SYS SUMM 2	SPEC 19 PRO, SYS SUMM
HORIZ SIT	SPEC 50 PRO
BFS OVERRIDE	SPEC 51 PRO

The following major mode displays are available in OPS 3:

<u>Display</u>	<u>Major Mode</u>
DEORB MNVR COAST	301, 303
DEORB MNVR EXEC	302
ENTRY TRAJ 1, 2, 3, 4, 5	304
VERT SIT 1, 2	305

The following major mode displays are available in OPS 6:

<u>Display</u>	<u>Major Mode</u>
RTLS TRAJ 2	601
VERT SIT 1/2	602
VERT SIT 2	603

The following displays are available in OPS 6 (keyboard invocation is also listed).

<u>Display</u>	<u>Keystrokes</u>
HORIZ SIT	SPEC 50 PRO
GNC SYS SUMM 1	SPEC 18 PRO, SYS SUMM
GNC SYS SUMM 2	SPEC 19 PRO, SYS SUMM
BFS OVERRIDE	SPEC 51 PRO

5.3.3.4 SM Displays. The following displays are available at all times in the SM major function. The keyboard input necessary to invoke the display is also listed.

<u>Display</u>	<u>Keystrokes</u>
THERMAL/PL	MAJOR MODE DISPLAY/OO0
SM SYS SUMM 1	SPEC 78 PRO, SYS SUMM
SM SYS SUMM 2	SPEC 79 PRO, SYS SUMM
PL BAY DOORS	SPEC 63 PRO

Since there is only one OPS in the SM major function, the THERMAL/PL display is active at all times as the underlying OPS/major mode display.

5.4 BFS GPC NOT ENGAGED/ENGAGED

Following the BFS IPL or transition from HALT to STANDBY or RUN, the BFS GPC will enter BFS OPS 0. If the BFS is not engaged, it will monitor the FC data buses to determine whether or not the PASS is in a state which supports the active PASS/BFS interface; i.e., in OPS 1, 3, or 6. If the PASS is in one of these states, the BFS will begin tracking (or maintaining a kind of sync with) the PASS based upon receipt of the 25 Hz high frequency executive (HFE) transaction and the PASS transfer data. If the PASS was not in OPS 1, 3, or 6 the BFS will ignore the PASS and enter the DISENGAGED-STAND ALONE mode in which no FC data bus inputs are considered valid.

5.4.1 Transitions Between the STAND-ALONE and PASS TRACKING States Not Engaged. If the BFS GPC is in the DISENGAGED-STAND ALONE state, it will require either a BFS I/O RESET EXEC input, a transition to OPS 101 or 301, or a movement of the BFS GPC MODE switch to HALT and back to STANDBY or RUN to force it to attempt to track the PASS. It should be noted that a transition from HALT to STBY or RUN significantly impacts software processing as it forces BFS OPS 0 (stops GNC processing in particular), whereas an I/O RESET EXEC input does not force OPS 0. An I/O reset of this type is done automatically by the BFS system software following a BFS keyboard entry for an OPS transition to OPS 1 or 3 (OPS 101 PRO or OPS 301 PRO). The BFS GPC will enter the STAND ALONE state when the PASS transitions to an OPS which the BFS cannot support (such as the OPS 1 to OPS 2 PASS GPC transition). If the BFS GPC is engaged and then disengaged (using the BFC DISENGAGE switch, for example), it will enter this STAND ALONE state. Also, if the BFS GPC is tracking the PASS and a GMT update of over 5 msec is made to the PASS, the BFS will enter the DISENGAGED-STAND ALONE state. For whatever the reason, whenever the BFS GPC stops tracking the PASS it will generate four fault messages indicating that the BFS is not listening to any PASS BCE chain inputs (e.g., BCE/STRG 1 (2, 3, 4) PASS). In addition, the BFC light (panels F2 and F4) will flash.

5.4.2 BFS Listening to PASS DK Buses Not Engaged. The BFS GPC will listen on all DK buses including those controlled by the PASS. On the PASS DK buses, the BFS will process only certain specified item entries on the HORIZ SIT, ENTRY TRAJ X (MM304), and XXXXX MNVR XXXXX displays, and manual major mode transition requests within an OPS. Also, GPC/CRT XY EXEC entries are recognized by the BFS. This capability eliminates the necessity to enter these items through both the PASS and BFS keyboards to the appropriate displays. Table 5-2 lists the items on the three displays which the BFS will receive by DK LISTEN.

5.4.3 BFS GPC Selective Listen Mode FC Data Buses Not Engaged. As previously mentioned, the BFS GPC receives data from the PASS-controlled FC data buses by operating a SELECTIVE TRANSACTION LISTEN mode. In OPS 1, 3, and 6 the PASS commander of a FC data bus begins its I/O sequence by sending a LISTEN command (used only by the BFS GPC) which identifies the particular I/O sequence and bus terminal unit (BTU) address flight aft (FA) or flight forward (FF) multiplexer/demultiplexer (MDM), Master events controller (MEC), engine interface unit (EIU), and data display unit (DDU). The BFS recognizes this LISTEN command and prepares itself to receive the subsequent data response. The selective transaction listen mode allows the BFS GPC to receive uplink commands and MTU updates as well as avionics sensor and status information. The BFS GPC does not, however, monitor the PASS GPC outputs to those BTU's mentioned above.

TABLE 5-2

PASS DISPLAYS MONITORED BY BFS

DISPLAY	KEYBOARD INPUTS	REMARKS
HORIZONTAL SITUATION	Items 3-5 Items 6-7 Item 8 Item 9	Runway select Glide slope select XEP SW select Altimeter data
XXX MNVR YYY	Items 1-4 Items 6-8 Item 9 Items 10-21 Item 22 Item 23 Items 24-26 Items 28-33 Item 35	Engine burn select Gimbal trim select Vehicle weight PEG 4/7 targeting data Load targeting data Start CRT timer Entry interface attitude OMS gimbal drive select Abort target
ENTRY TRAJ X	Item 1	Bias

5.4.4 PASS/BFS Transfer Data Not Engaged. During the OPS 1, 3, and 6 mission phases, the PASS GPC's will send certain status and computational information to the BFS GPC over FC data buses 5, 6, 7, and 8, including MDM/BCE element bypass data, string and PL port mode indicators, PASS major mode information, and an indicator which tells where the PASS is in its processing sequence (minor cycle sequencing). The minor cycle sequencing and string mode data are used to establish PASS tracking by the BFS. The above mentioned data is transferred at 25 Hz. Also transmitted in this transfer data are the state vector with a time tag, the IMU REFSMAT, the PASS time-to-launch reference, and VREL at ME OUT. This data is transferred at 1.04 Hz. The BFS GPC uses the PASS state vector to update its own state vector only after it has been moded from OPS 0 to OPS 301 and begins tracking the PASS. It uses the PASS state vector one time only. After that the BFS computes its own state vector and ignores the PASS state vector unless requested to on the HORIZ SIT display. The IMU REFSMAT is snapshot and utilized by the BFS on the transition from OPS 0 to MM301. The relative velocity at main engine out is snapshot by the BFS upon indication of main engine OUT. This PASS/BFS transfer data should be identical over all four FC data buses (FC5-FC8). The BFS GPC checks to ensure that this information is identical. If a discrepancy is found, a class 3 fault message is generated (BCE STRG X PASS) and the lowest numbered two identical FC inputs will be used. This BFS GPC will ignore, until reinitialized, those strings over which the differing data was transmitted. This means that if the BFS GPC detects that identical data is transferred over FC 5, 6, and 7 but (twice in a row) the transfer data over FC 8 is different, the BFS GPC will ignore string 4; i.e., both FC 4 and 8. If no two inputs are the same, the BFS GPC enters the DISENGAGED-STAND ALONE state. In either case, an appropriate class 3 fault message will be generated. (I/O ERROR or BCE/STRG).

5.4.5 One-Shot Transfers Not Engaged. In order to transfer certain data (launch polynomial, inertial measurement unit (IMU) calibration data, accelerometer data, etc.) into the BFS GPC during the launch countdown (prior to PASS moding to OPS 1), a one-shot transfer capability will be included in the PASS GNC OPS 9 software in the general test support (GTS) SPEC display. The BFS GPC must be in OPS 0 and in the DISENGAGED-STAND ALONE state for this to be possible. An Item number (24) exists on the BFS MEMORY display which, when initiated, will cause the BFS to set up to receive the data. An asterisk will appear next to ITEM 24. An Item number (29) exists on the PASS GTS display (SPEC 100) to initiate the transfer. If the transaction is successful, the asterisk on the BFS MEMORY display will disappear. If it is not successful, the one-shot transfer can be repeated, if necessary.

5.4.6 BFS/I/O Management

5.4.6.1 Data Bus Control Summary. The BFS GPC will not access the inter-computer communication (ICC) or, after IPL, the mass memory (MM) data buses. The BFS GPC will begin commanding on the PL data buses when it is in RUN or ENGAGED. Pre-engaged, the BFS will not command any FC data bus and will listen on the FC data buses only if it is tracking PASS (OPS 1, 3, or 6). When engaged, the BFS will command on the FC data buses and gain control of the vehicle. The BFS GPC may be assigned one forward CRT preengage and two forward CRT's postengage via the BFC/CRT DISPLAY and SELECT switches. Also, the GPC/CRT key may be used to assign or deassign the BFS from any DK bus as long as it does not deassign in conflict with the BFC CRT select. This capability provides a backup method for assigning the forward CRT's to the BFS if the BFC CRT SELECT switch develops a problem. Each GPC has a dedicated IP bus through which it receives OI data and transmits its downlist. When the BFS GPC is initialized, it does not have command of the LDB's. Control may be assigned to the BFS GPC via a keyboard entry to the BFS MEMORY display (Items 25 or 26). It is the user's responsibility to ensure that the PASS is no longer commanding on those data buses.

5.4.6.2 BFS I/O Error Processing. As is the case in the PASS, errors detected on outputs will be recorded in an I/O error log but cause no special downmoding or annunciation. The BFS tracks PASS transfer data (25 times-per-second) and also performs its own I/O error processing based solely on its own inputs.

For data access on the FC data buses and PL data buses, two consecutive errors on a particular transaction involving a BCE element (other than on an MDM return word) will result in a BCE element bypass. In this case, the element will no longer be accessed for data and a Class 3 alarm and fault message will be generated. The fault message will be of the same format as those generated by the PASS (BCE STRG X ABCD where X = 1,2,3,4 and ABCD indicates the failed element). Also, two consecutive errors with the MDM return word on a transaction will result in the BFS ignoring that MDM and generating an appropriate class 3 fault message of the I/O ERROR ABC variety. Also, an M will appear on the BFS GNC SYS SUMM 1 display beside the fault MDM (FF, FA, PL) just like in the PASS. It should be noted that this means that an MDM or certain line replaceable unit (LRU) failures will result in double annunciation by the PASS and BFS in the pre-engage state. After the first error is detected on a DK bus, or the second consecutive error detected on the instrumentation/pulse-code alarm and I/O ERROR

ABC fault message (where ABC indicates the faulty bus), the BFS GPC continues to use the bus. In these cases, the data bus is not downmoded.

Pre-engage, if the BFS GPC fails to correctly receive the PASS transfer data or the HFE transaction listen commands two consecutive times over a string, then the BFS GPC will downmode the involved string (HALT I/O on that string). This downmoding remains in effect until the BFS is reinitialized using its MODE switch, or until an I/O RESET is made (automatically upon OPS transition, or BFS engagement, or manually upon BFS keyboard entry). Also, the Class 3 fault message BCE STRG X PASS will be generated where X indicates on which string the problem was detected.

5.4.7 I/O RESET Response. Following an I/O RESET EXEC command to a BFS keyboard, the BFS restores data buses and BCE elements to their nominal configuration for the current mission phase and state (engaged or not). Because no downmoding occurs on the IP or DK buses, only the FC and PL buses are affected by an I/O RESET.

If the BFS is engaged when the I/O RESET is commanded, both the FC and PL buses are configured in the command mode, and BCE elements are restored as appropriate for the current mission phase.

If the BFS is not engaged, and an I/O RESET is commanded, the FC buses are placed in the listen mode and the BFS attempts to synchronize with the PASS. If the BFS succeeds in establishing sync with the PASS, the FC BCE elements are configured to the state indicated in the PASS transfer data. If the BFS is not successful, the BFS enters the DISENGAGED-STAND ALONE state and disables the FC data buses. In either case, the BFS configures the PL buses in the command mode if the BFS is in RUN and BCE elements are restored.

5.4.8 Timekeeping. The BSS software maintains the current value of GMT and MET for use by applications programs as well as for its own use. These values are internally updated 25 times-per-second, (once per minor cycle). Once per major cycle (1.04 times per second) a comparison is made between the internally computed time and an MTU source, if available (through the BFS listen mode on the FC data buses, when the BFS is not engaged but tracking the PASS, or through its normal I/O on the FC data buses when it is engaged). The BFS checks the MTU responses for BITE. If at least two of the MTU sources pass the BITE test, the BFS simply uses a mid-value selection to pick its time source. If only one time source passes the BITE fault test, it is used as a time source. In either case, the BFS uses this good source to update its internal clock. If no good source is found, the BFS uses internal time.

When the BFS GPC is initialized (moded from HALT to STANDBY or RUN), it checks for an MTU source. If one is available, it sets its GMT/MET to the lowest numbered available MTU accumulator GMT/MET (if valid). If no valid MTU source is available, the BFS GPC defaults its time values to day one for GMT and its MET to zero. The BFS will again update its internal clock to the MTU time upon the OPS transition to OPS 3.

The current BFS mission time in MET will be in the top line in the upper right-hand corner of all BFS driven CRT's. The CRT timer may be initiated to count-down of the loaded time of ignition (TIG) through a crew input to the

current XXXXX MNVR XXXXX display through a BFS keyboard, or through the BFS listening to PASS controlled DK buses. The current CRT timer time appears in the second line in the upper right-hand corner of all BFS CRT displays.

5.4.9 Uplink. Uplink to the BFS GPC is similar to uplink to the PASS GPC's. Only a subset of the PASS uplink commands will be used for the BFS. For example, no DEU Equivalent commands can be sent from the ground to the BFS. The ground can only uplink to the BFS GPC when the BFS GPC is listening on strings 1 or 3, since the network signal processor (NSP) 1 is on FF1 and NSP 2 is on FF3. The BFS, if not engaged, must be in the selective listen mode on the FC data buses in order to receive uplink, and thus the PASS must be in OPS 1, or 6. If the BFS entered the DISENGAGED-STAND ALONE state, it would stop listening on the FC data buses and thus would not be capable of uplink. If the BFS is engaged, it will be capable of responding to uplink commands since it controls the FC data buses.

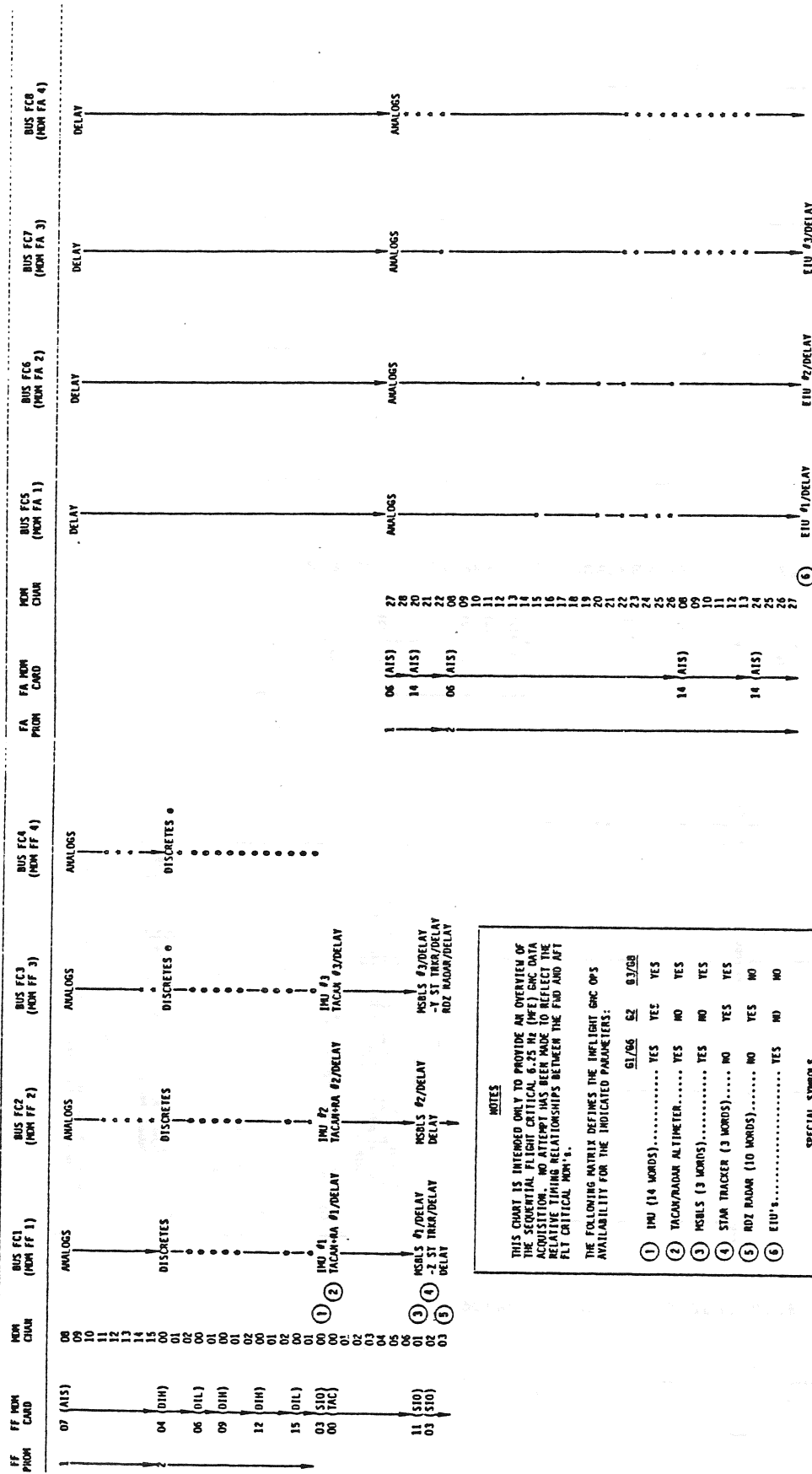
5.4.10 Downlist. The BFS GPC collects and sends its downlist to the pulse-code modulation master unit (PCMMU) 24 times-per-major cycle. This downlist data is stored in the PCMMU's toggle buffer 5 for incorporation into the downlink during the OPS 1, 3, and 6 mission phases. There are controls on the BFS MEMORY display to dump BFS main memory.

APPENDIX A
MDM TABLES

MFE INPUT TRANSACTION OVERVIEW (BCE STRING "A" OR "C")

REV DATE: 3/22/83

PAGE 1



NOTES

THIS CHART IS INTENDED ONLY TO PROVIDE AN OVERVIEW OF THE SEQUENCE OF INPUTS TO THE MFE. IT DOES NOT REFLECT THE ACQUISITION AND DELIVERY TIMES WHICH WOULD BE REQUIRED TO REFLECT THE RELATIVE TIMING RELATIONSHIPS BETWEEN THE PMO AND APT FLT CRITICAL MON'S.

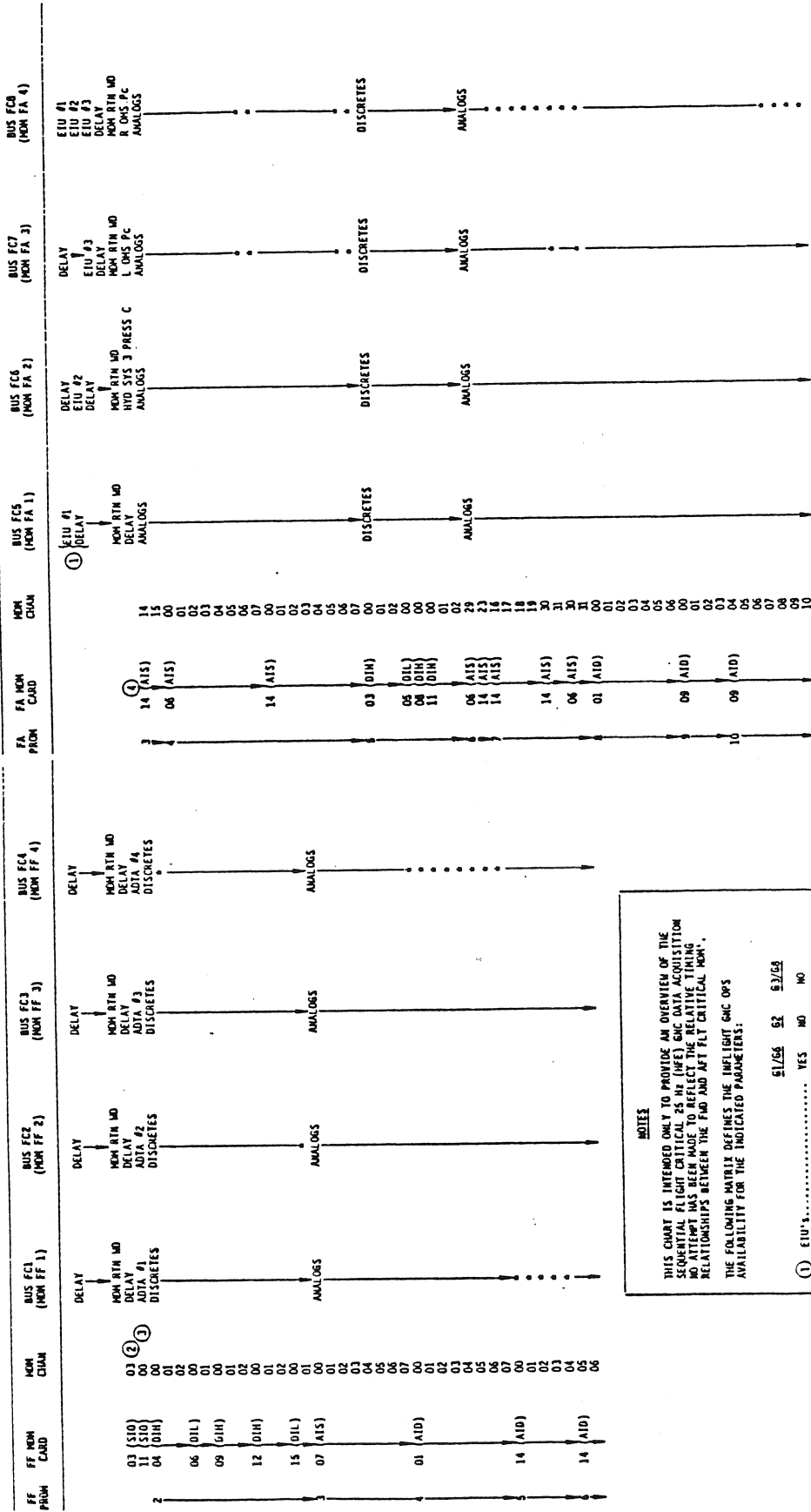
THE FOLLOWING MATRIX DEFINES THE INFLIGHT GNC OPS AVAILABILITY FOR THE INDICATED PARAMETERS:

	51/56	52	53/58
① IMU (14 WORDS).....	YES	YES	YES
② TACAN/RANDM ALTIMETER.....	YES	NO	YES
③ MSBLS (3 WORDS).....	YES	NO	YES
④ STAN TRACKER (3 WORDS).....	NO	YES	YES
⑤ RDZ RANDM (10 WORDS).....	NO	YES	NO
⑥ EIU'S.....	YES	NO	NO

SPECIAL SYMBOLS

- ... DUMMY INPUT CHD (CHANNEL NOT HARDWIRED BUT "DATA" READ TO SIMPLIFY THE I/O TRANSACTION PROFILE)
- ... VALID DATA DURING THE MFE INPUT TRANSACTION (6:25 Hz) BUT DATA NOT ACTUALLY UTILIZED BY THE GNC APPLICATIONS SOFTWARE

HFE INPUT TRANSACTION OVERVIEW (BCE STRING "B" or "D")



NOTES

THIS CHART IS INTENDED ONLY TO PROVIDE AN OVERVIEW OF THE CHANNELS THAT ARE USED FOR HFE DATA ACQUISITION. NO ATTEMPT HAS BEEN MADE TO REFLECT THE RELATIVE TIMING RELATIONSHIPS BETWEEN THE PWD AND APT FLT CRITICAL MOM.

THE FOLLOWING MATRIX DEFINES THE IMFLIGHT GMC OPS AVAILABILITY FOR THE INDICATED PARAMETERS:

①	ETU'S	SL/GR	GR	SL/GR
②	PAYLOAD SENSOR	YES	NO	NO
③	AUTA (6 WORDS)	YES	NO	YES
④	HYD SYS 3 PRESS C	MOM FA 2, CARD 14 (AIS), CHAN 28	MOM FA 3, CARD 06 (AIS), CHAN 18	MOM FA 4, CARD 06 (AIS), CHAN 18

SPECIAL SYMBOLS

--- DUMMY INPUT CH0 (CHANNEL NOT IMPLEMENTED BUT 'DATA' READ TO SIMPLIFY THE I/O TRANSACTION PROFILE)

INPUT CARD CHANNELIZATION (BCE STRING "A")

MDM FF 1 - FF 4

NOTE: PARAMETERS WITH * ARE NOT USED AS PART OF THE INPUT

FROM CARD	CHUM	BIT	MDM FF 1	MDM FF 2	MDM FF 3	MDM FF 4	COMMENT
-----------	------	-----	----------	----------	----------	----------	---------

2	06 (DIL)	00	0 RJDF 1 JET F1F CHAMBER PRESS IND	0 RJDF 2 JET F4R CHAMBER PRESS IND	0 RJDF 2 JET F3F CHAMBER PRESS IND	0 RJDF 2 JET F3F CHAMBER PRESS IND	
		01	1 F1L CHAMBER PRESS IND	1 F2R CHAMBER PRESS IND	1 F3L CHAMBER PRESS IND	1 F3L CHAMBER PRESS IND	
		02	2 F1D CHAMBER PRESS IND	2 F2D CHAMBER PRESS IND	2 F3R CHAMBER PRESS IND	2 F3D CHAMBER PRESS IND	
		03	3 LH DDU PWR SPLY A GOOD	3 LH DDU PWR SPLY A GOOD	3 FSR CHAMBER PRESS IND	3 F3D CHAMBER PRESS IND	
		04	4 C GOOD	4 C GOOD	4 POS 1 OUTPUT - C	4 POS 1 OUTPUT - C	
		05	5 C GOOD	5 C GOOD	5 POS 2 OUTPUT - C	5 POS 2 OUTPUT - C	
		06	6 FMD THC POS 1 OUTPUT - A	6 FMD THC POS 1 OUTPUT - B	6 MEG 1 OUTPUT - C	6 MEG 1 OUTPUT - C	
		07	7 MEG 1 OUTPUT - A	7 MEG 1 OUTPUT - B	7 POS 1 OUTPUT - C	7 POS 1 OUTPUT - C	
		08	8 MEG 2 OUTPUT - A	8 MEG 2 OUTPUT - B	8 POS 2 OUTPUT - C	8 POS 2 OUTPUT - C	
		09	9 MEG 2 OUTPUT - A	9 MEG 2 OUTPUT - B	9 POS 1 OUTPUT - C	9 POS 1 OUTPUT - C	
		10	10 MEG 2 OUTPUT - A	10 MEG 2 OUTPUT - B	10 POS 2 OUTPUT - C	10 POS 2 OUTPUT - C	
		11	11 POS 1 OUTPUT - A	11 POS 1 OUTPUT - B	11 MEG 1 OUTPUT - C	11 MEG 1 OUTPUT - C	
		12	12 POS 2 OUTPUT - A	12 POS 2 OUTPUT - B	12 MEG 2 OUTPUT - C	12 MEG 2 OUTPUT - C	
		13	13 MEG 1 OUTPUT - A	13 MEG 1 OUTPUT - B	13 LH SRTC TAKEOVER - A	13 LH SRTC TAKEOVER - C	
		14	14 MEG 2 OUTPUT - A	14 MEG 2 OUTPUT - B	14 LH SRTC TAKEOVER - B	14 LH SRTC TAKEOVER - C	
		15	15 LH SRTC TAKEOVER - A	15 LH SRTC TAKEOVER - B	15 LH SRTC TAKEOVER - B	15 LH SRTC TAKEOVER - C	
		01	0 LH RHC + PITCH TRIM - A	0 LH RHC + PITCH TRIM - B	0 LH RHC + PITCH TRIM - B	0 LH RHC + PITCH TRIM - B	
		02	1 - PITCH TRIM - A	1 - PITCH TRIM - B	1 - PITCH TRIM - B	1 - PITCH TRIM - B	
		03	2 - ROLL TRIM - A	2 - ROLL TRIM - B	2 - ROLL TRIM - B	2 - ROLL TRIM - B	
		04	3 - ROLL TRIM - A	3 - ROLL TRIM - B	3 - ROLL TRIM - B	3 - ROLL TRIM - B	
		05	4 - ROLL TRIM - A	4 - ROLL TRIM - B	4 - ROLL TRIM - B	4 - ROLL TRIM - B	
		06	5 SBB SEPARATION AUTO A CHO	5 SBB SEPARATION AUTO A CHO	5 SBB SEPARATION AUTO C CHO	5 SBB SEPARATION AUTO B CHO	
		07	6 SBB SEPN MANUAL/AUTO ENABLE A CHO	6 SBB SEPN MANUAL/AUTO ENABLE B CHO	6 SBB SEPN MANUAL/AUTO ENABLE C CHO	6 SBB SEPN MANUAL/AUTO ENABLE B CHO	
		08	7 SBB SEPARATION INITIATE A CHO	7 SBB SEPARATION INITIATE B CHO	7 SBB SEPARATION INITIATE C CHO	7 SBB SEPARATION INITIATE B CHO	
		09	8	8	8	8	
		10	9	9	9	9	
		11	10	10	10	10	
		12	11	11	11	11	
		13	12	12	12	12	
		14	13	13	13	13	
		15	14	14	14	14	
		00	15	15	15	15	

09	(DIL)	00	0 RJDF 1 JET F1F DRIVER	0 RJDF 1 JET F2F DRIVER	0 RJDF 2 JET F4R DRIVER	0 RJDF 2 JET F3F DRIVER	
		01	1 F1L DRIVER	1 F2R DRIVER	1 F2R DRIVER	1 F3L DRIVER	
		02	2 F1D DRIVER	2 F2D DRIVER	2 F3R DRIVER	2 F3D DRIVER	
		03	3 FMD DAP SELECT A - A	3 FMD DAP SELECT A - B	3 FMD DAP SELECT A - A	3 FMD DAP SELECT A - B	
		04	4 FMD DAP SELECT B - A	4 FMD DAP SELECT B - B	4 FMD DAP SELECT B - A	4 FMD DAP SELECT B - B	
		05	5 FMD DAP SELECT C - A	5 FMD DAP SELECT C - B	5 FMD DAP SELECT C - A	5 FMD DAP SELECT C - B	
		06	6 FMD DAP SELECT D - A	6 FMD DAP SELECT D - B	6 FMD DAP SELECT D - A	6 FMD DAP SELECT D - B	
		07	7 FMD DAP AUTO A	7 FMD DAP AUTO B	7 FMD DAP AUTO A	7 FMD DAP AUTO B	
		08	8 FMD DAP AUTO B	8 FMD DAP AUTO A	8 FMD DAP AUTO B	8 FMD DAP AUTO A	
		09	9 MAN A	9 MAN B	9 MAN A	9 MAN B	
		10	10 AFT DAP AUTO C	10 AFT DAP AUTO C	10 AFT DAP AUTO C	10 AFT DAP AUTO C	
		11	11 MAN C	11 MAN C	11 MAN C	11 MAN C	
		12	12 GAIN PITCH HI FWD - A	12 GAIN PITCH HI FWD - B	12 GAIN PITCH HI FWD - C	12 GAIN PITCH HI FWD - C	
		13	13 HIW FB A	13 HIW FB B	13 HIW FB - C	13 HIW FB - C	
		14	14 GAIN ROLL/YAW HI FWD - A	14 GAIN ROLL/YAW HI FWD - B	14 GAIN ROLL/YAW HI FWD - C	14 GAIN ROLL/YAW HI FWD - C	
		15	15 LO FWD - A	15 LO FWD - B	15 LO FWD - C	15 LO FWD - C	
		01	0 SCIL - MSP POWER 1 (OM)	0 MSP ME-2 SHUTDOWN CHO A	0 MSP ME-2 SHUTDOWN CHO B	0 MSP ME-2 SHUTDOWN CHO B	
		02	1 SENSE SH -2 COM A	1 SENSE SH -2 COM B	1 SENSE SH -2 COM C	1 SENSE SH -2 COM C	
		03	2 -1 COM A	2 -1 COM B	2 ENTRY ROLL MODE L GAIN - C	2 ENTRY ROLL MODE L GAIN - C	
		04	3 ENTRY ROLL MODE L GAIN - A	3 ENTRY ROLL MODE L GAIN - B	3 ENTRY ROLL MODE L GAIN - C	3 ENTRY ROLL MODE L GAIN - D	
		05	4 FMD ROTATION ROLL DISC RATE A	4 FMD ROTATION ROLL DISC RATE B	4 FMD ROTATION ROLL DISC RATE A	4 FMD ROTATION ROLL DISC RATE B	
		06	5 ACCEL A	5 ACCEL B	5 ACCEL A	5 ACCEL B	
		07	6 PITCH DISC RATE A	6 PITCH DISC RATE B	6 PITCH DISC RATE A	6 PITCH DISC RATE B	
		08	7 ACCEL A	7 ACCEL B	7 ACCEL A	7 ACCEL B	
		09	8 PULSE A	8 PULSE B	8 ACCEL A	8 ACCEL B	
		10	9 YAW DISC RATE A	9 YAW DISC RATE B	9 YAW DISC RATE A	9 YAW DISC RATE B	
		11	10 ACCEL A	10 ACCEL B	10 ACCEL A	10 ACCEL B	
		12	11 PULSE A	11 PULSE B	11 ACCEL A	11 ACCEL B	
		13	12 FMD RCS JETS NORM A	12 FMD RCS JETS NORM B	12 FMD RCS JETS NORM A	12 FMD RCS JETS NORM B	
		14	13 VERNIER A	13 VERNIER B	13 VERNIER A	13 VERNIER B	
		15	14 FMD TRANSLATION X NORM A	14 FMD TRANSLATION X NORM B	14 FMD TRANSLATION X NORM A	14 FMD TRANSLATION X NORM B	
		00	15	15	15	15	

00	(DIL)	00	0 RJDF 1 JET F1F DRIVER	0 RJDF 1 JET F2F DRIVER	0 RJDF 2 JET F4R DRIVER	0 RJDF 2 JET F3F DRIVER	
		01	1 F1L DRIVER	1 F2R DRIVER	1 F2R DRIVER	1 F3L DRIVER	
		02	2 F1D DRIVER	2 F2D DRIVER	2 F3R DRIVER	2 F3D DRIVER	
		03	3 FMD DAP SELECT A - A	3 FMD DAP SELECT A - B	3 FMD DAP SELECT A - A	3 FMD DAP SELECT A - B	
		04	4 FMD DAP SELECT B - A	4 FMD DAP SELECT B - B	4 FMD DAP SELECT B - A	4 FMD DAP SELECT B - B	
		05	5 FMD DAP SELECT C - A	5 FMD DAP SELECT C - B	5 FMD DAP SELECT C - A	5 FMD DAP SELECT C - B	
		06	6 FMD DAP SELECT D - A	6 FMD DAP SELECT D - B	6 FMD DAP SELECT D - A	6 FMD DAP SELECT D - B	
		07	7 FMD DAP AUTO A	7 FMD DAP AUTO B	7 FMD DAP AUTO A	7 FMD DAP AUTO B	
		08	8 FMD DAP AUTO B	8 FMD DAP AUTO A	8 FMD DAP AUTO B	8 FMD DAP AUTO A	
		09	9 MAN A	9 MAN B	9 MAN A	9 MAN B	
		10	10 AFT DAP AUTO C	10 AFT DAP AUTO C	10 AFT DAP AUTO C	10 AFT DAP AUTO C	
		11	11 MAN C	11 MAN C	11 MAN C	11 MAN C	
		12	12 GAIN PITCH HI FWD - A	12 GAIN PITCH HI FWD - B	12 GAIN PITCH HI FWD - C	12 GAIN PITCH HI FWD - C	
		13	13 HIW FB A	13 HIW FB B	13 HIW FB - C	13 HIW FB - C	
		14	14 GAIN ROLL/YAW HI FWD - A	14 GAIN ROLL/YAW HI FWD - B	14 GAIN ROLL/YAW HI FWD - C	14 GAIN ROLL/YAW HI FWD - C	
		15	15 LO FWD - A	15 LO FWD - B	15 LO FWD - C	15 LO FWD - C	
		01	0 SCIL - MSP POWER 1 (OM)	0 MSP ME-2 SHUTDOWN CHO A	0 MSP ME-2 SHUTDOWN CHO B	0 MSP ME-2 SHUTDOWN CHO B	
		02	1 SENSE SH -2 COM A	1 SENSE SH -2 COM B	1 SENSE SH -2 COM C	1 SENSE SH -2 COM C	
		03	2 -1 COM A	2 -1 COM B	2 ENTRY ROLL MODE L GAIN - C	2 ENTRY ROLL MODE L GAIN - C	
		04	3 ENTRY ROLL MODE L GAIN - A	3 ENTRY ROLL MODE L GAIN - B	3 ENTRY ROLL MODE L GAIN - C	3 ENTRY ROLL MODE L GAIN - D	
		05	4 FMD ROTATION ROLL DISC RATE A	4 FMD ROTATION ROLL DISC RATE B	4 FMD ROTATION ROLL DISC RATE A	4 FMD ROTATION ROLL DISC RATE B	
		06	5 ACCEL A	5 ACCEL B	5 ACCEL A	5 ACCEL B	
		07	6 PITCH DISC RATE A	6 PITCH DISC RATE B	6 PITCH DISC RATE A	6 PITCH DISC RATE B	
		08	7 ACCEL A	7 ACCEL B	7 ACCEL A	7 ACCEL B	
		09	8 PULSE A	8 PULSE B	8 ACCEL A	8 ACCEL B	
		10	9 YAW DISC RATE A	9 YAW DISC RATE B	9 YAW DISC RATE A	9 YAW DISC RATE B	
		11	10 ACCEL A	10 ACCEL B	10 ACCEL A	10 ACCEL B	
		12	11 PULSE A	11 PULSE B	11 ACCEL A	11 ACCEL B	
		13	12 FMD RCS JETS NORM A	12 FMD RCS JETS NORM B	12 FMD RCS JETS NORM A	12 FMD RCS JETS NORM B	
		14	13 VERNIER A	13 VERNIER B	13 VERNIER A	13 VERNIER B	
		15	14 FMD TRANSLATION X NORM A	14 FMD TRANSLATION X NORM B	14 FMD TRANSLATION X NORM A	14 FMD TRANSLATION X NORM B	
		00	15	15	15	15	

2 15 (01) 00

INPUT CARD CHANNELIZATION (BCE STRING "A")

MDM FF 1 - FF 4

REV DATE: 12/04/81

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FOR ALL PART OF THE INPUT

FROM CARD	CARD	BIT	MDM FF 1	BIT	MDM FF 2	BIT	MDM FF 3	BIT	MDM FF 4	COMMENTS
2 15 (01) 00		0	IN OP	0	IN OP	0	IN OP	0		
		1	IN OP	1	IN OP	1	IN OP	1		
		2	IN OP	2	IN OP	2	IN OP	2		
		3	IN OP	3	IN OP	3	IN OP	3		
		4	IN OP	4	IN OP	4	IN OP	4		
		5	IN OP	5	IN OP	5	IN OP	5		
		6	IN OP	6	IN OP	6	IN OP	6		
		7	IN OP	7	IN OP	7	IN OP	7		
		8	IN OP	8	IN OP	8	IN OP	8		
		9	IN OP	9	IN OP	9	IN OP	9		
		10	IN OP	10	IN OP	10	IN OP	10		
		11	IN OP	11	IN OP	11	IN OP	11		
		12	IN OP	12	IN OP	12	IN OP	12		
		13	IN OP	13	IN OP	13	IN OP	13		
		14	IN OP	14	IN OP	14	IN OP	14		
		15	IN OP	15	IN OP	15	IN OP	15		
		16	IN OP	16	IN OP	16	IN OP	16		
		17	IN OP	17	IN OP	17	IN OP	17		
		18	IN OP	18	IN OP	18	IN OP	18		
		19	IN OP	19	IN OP	19	IN OP	19		
		20	IN OP	20	IN OP	20	IN OP	20		
		21	IN OP	21	IN OP	21	IN OP	21		
		22	IN OP	22	IN OP	22	IN OP	22		
		23	IN OP	23	IN OP	23	IN OP	23		
		24	IN OP	24	IN OP	24	IN OP	24		
		25	IN OP	25	IN OP	25	IN OP	25		
		26	IN OP	26	IN OP	26	IN OP	26		
		27	IN OP	27	IN OP	27	IN OP	27		
		28	IN OP	28	IN OP	28	IN OP	28		
		29	IN OP	29	IN OP	29	IN OP	29		
		30	IN OP	30	IN OP	30	IN OP	30		
		31	IN OP	31	IN OP	31	IN OP	31		

MDM FF1-FF4 INPUT CARD CHANNELIZATION (BCE STRING "B")

REF DATE: 07/20/62

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FROM CARD	CHRG	BIT	FROM FF 1	BIT	FROM FF 2	BIT	FROM FF 3	BIT	FROM FF 4	COMMENTS
2	04	(DINH)	00							
			0	FCS NON CHRG 2 RESET/OVERRIDE A (1)	0	FCS NON CHRG 2 RESET/OVERRIDE A (1)	0	FCS NON CHRG 2 RESET/OVERRIDE A (1)	0	
			1	ENTIRE MOLL. MODE SEL - LEFT (1)	1	ENTIRE MOLL. MODE SEL - LEFT (1)	1	ENTIRE MOLL. MODE SEL - LEFT (1)	1	
			2	LN BODY FLAP UP - A (1)	2	LN BODY FLAP UP - A (1)	2	LN BODY FLAP UP - A (1)	2	
			3	DOWN A (1)	3	DOWN A (1)	3	DOWN A (1)	3	
			4	MPS RE-3 SHUTDOWN CHG 1	4	MPS RE-3 SHUTDOWN CHG 1	4	MPS RE-3 SHUTDOWN CHG 1	4	
			5	MPS RE-3 SHUTDOWN CHG 2	5	MPS RE-3 SHUTDOWN CHG 2	5	MPS RE-3 SHUTDOWN CHG 2	5	
			6	RUP 2 TRICKE CLR CONTINUITY 3 (1)	6	RUP 2 TRICKE CLR CONTINUITY 3 (1)	6	RUP 2 TRICKE CLR CONTINUITY 3 (1)	6	
			7	RCS FWD FWD MWP 15LN REV - 1 (1)	7	RCS FWD FWD MWP 15LN REV - 1 (1)	7	RCS FWD FWD MWP 15LN REV - 1 (1)	7	
			8	CL (1)	8	CL (1)	8	CL (1)	8	
			9	THANK 15LN REV - 1/2 OP (1)	9	THANK 15LN REV - 1/2 OP (1)	9	THANK 15LN REV - 1/2 OP (1)	9	
			10	CL (1)	10	CL (1)	10	CL (1)	10	
			11	MPS PRESS REV - A OP (1)	11	MPS PRESS REV - A OP (1)	11	MPS PRESS REV - A OP (1)	11	
			12	CL (1)	12	CL (1)	12	CL (1)	12	
			13	LN AIR DATA SOURCE SEL - LEFT	13	LN AIR DATA SOURCE SEL - LEFT	13	LN AIR DATA SOURCE SEL - LEFT	13	
			14	RIGHT	14	RIGHT	14	RIGHT	14	
			15	RIGHT	15	RIGHT	15	RIGHT	15	
			01	LN ADJ ATTITUDE SEL - INERTIAL	01	LN ADJ ATTITUDE SEL - INERTIAL	01	LN ADJ ATTITUDE SEL - INERTIAL	01	
			02	LN REFERENCE	02	LN REFERENCE	02	LN REFERENCE	02	
			03	LN RATE SCALE - HIGH	03	LN RATE SCALE - HIGH	03	LN RATE SCALE - HIGH	03	
			04	LN MEDIUM	04	LN MEDIUM	04	LN MEDIUM	04	
			05	LN LOW	05	LN LOW	05	LN LOW	05	
			06	LN ERROR SCALE - HIGH	06	LN ERROR SCALE - HIGH	06	LN ERROR SCALE - HIGH	06	
			07	LN MEDIUM	07	LN MEDIUM	07	LN MEDIUM	07	
			08	LN LOW	08	LN LOW	08	LN LOW	08	
			09	FCS LN PITCH GAIN ENABLE A (1)	09	FCS LN PITCH GAIN ENABLE A (1)	09	FCS LN PITCH GAIN ENABLE A (1)	09	
			10	CL (1)	10	CL (1)	10	CL (1)	10	
			11	R-Y GAIN ENABLE A (1)	11	R-Y GAIN ENABLE A (1)	11	R-Y GAIN ENABLE A (1)	11	
			12	CL (1)	12	CL (1)	12	CL (1)	12	
			13	R-Y GAIN ENABLE B (1)	13	R-Y GAIN ENABLE B (1)	13	R-Y GAIN ENABLE B (1)	13	
			14	CL (1)	14	CL (1)	14	CL (1)	14	
			15	LN BODY FLAP AUTO/MANUAL A (1)	15	LN BODY FLAP AUTO/MANUAL A (1)	15	LN BODY FLAP AUTO/MANUAL A (1)	15	
			02	LN SPB M/T/ROT AUTO/MAN B (1)	02	LN SPB M/T/ROT AUTO/MAN B (1)	02	LN SPB M/T/ROT AUTO/MAN B (1)	02	
			03	STAR TRK -Z BOOR CLOSER (1)	03	STAR TRK -Z BOOR CLOSER (1)	03	STAR TRK -Z BOOR CLOSER (1)	03	
			04	CL (1)	04	CL (1)	04	CL (1)	04	
			05	LN SPB M/T/ROT AUTO/MAN C (1)	05	LN SPB M/T/ROT AUTO/MAN C (1)	05	LN SPB M/T/ROT AUTO/MAN C (1)	05	
			06	STAR TRK -Z BOOR CLOSER (1)	06	STAR TRK -Z BOOR CLOSER (1)	06	STAR TRK -Z BOOR CLOSER (1)	06	
			07	CL (1)	07	CL (1)	07	CL (1)	07	
			08	R P/W WERTS 1 & 2 CLOSER 1	08	R P/W WERTS 1 & 2 CLOSER 1	08	R P/W WERTS 1 & 2 CLOSER 1	08	
			09	OPN 1	09	OPN 1	09	OPN 1	09	
			10	R P/W WERT 3 CLOSER 1	10	R P/W WERT 3 CLOSER 1	10	R P/W WERT 3 CLOSER 1	10	
			11	OPN 1	11	OPN 1	11	OPN 1	11	
			12	L P/W WERTS 4 & 7 CLOSER 1	12	L P/W WERTS 4 & 7 CLOSER 1	12	L P/W WERTS 4 & 7 CLOSER 1	12	
			13	OPN 1	13	OPN 1	13	OPN 1	13	
			14	R P/W WERT 5 CLOSER 1	14	R P/W WERT 5 CLOSER 1	14	R P/W WERT 5 CLOSER 1	14	
			15	OPN 1	15	OPN 1	15	OPN 1	15	

SM FUNC: RUP TRICKE CURRENT TEST LOSS, OPS B
 ALL PASS OPS: RCS SET MWD DOES NOT
 MWD STATUS DECLARED CLOSED - JETS NOT
 RUN ON APPROPRIATE MWD - PASS OPS 1, 4:
 OPS 1 - PASS OPS 2 - MWD STATUS
 LAST VALUE - OPEN OPERATOR AVAILABLE TO
 SELECT/SELECT JETS, OPS: RCS SET
 MWD STATUS
 LAST VALUE, NO OPEN OPERATOR

(c) DCCO CRT: P/Z, MWS 1ND LOSS OPS 2 & OPS 3

MDM FF1-FF4 INPUT CARD CHANNELIZATION (BCE STRING "B")

REQ DATE: 07/20/62

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NON	COND	BIT	NON FF 1	BIT	NON FF 2	BIT	NON FF 3	BIT	NON FF 4	COMMENTS
2	ON (BLL) 00		0 BUMP 1 JET P/F CHAMBER PRESS IND (1)		0 BUMP 1 JET P/F CHAMBER PRESS IND (1)		0 BUMP 2 JET P/F CHAMBER PRESS IND (1)		0 BUMP 2 JET P/F CHAMBER PRESS IND (1)	
			1 JET CHAMBER PRESS IND (1)		1 JET CHAMBER PRESS IND (1)		1 JET CHAMBER PRESS IND (1)		1 JET CHAMBER PRESS IND (1)	
			2 FIB CHAMBER PRESS IND (1)		2 FIB CHAMBER PRESS IND (1)		2 FIB CHAMBER PRESS IND (1)		2 FIB CHAMBER PRESS IND (1)	
			3 FIB CHAMBER PRESS IND (1)		3 FIB CHAMBER PRESS IND (1)		3 FIB CHAMBER PRESS IND (1)		3 FIB CHAMBER PRESS IND (1)	
			4 LH DDW PWR SP/L 8 6000 (1)		4 LH DDW PWR SP/L 8 6000 (1)		4 LH DDW PWR SP/L 8 6000 (1)		4 LH DDW PWR SP/L 8 6000 (1)	
			5 C 6000 (1)		5 C 6000 (1)		5 C 6000 (1)		5 C 6000 (1)	
			6 FIB TMC POS 1 OUTPUT - A (1)		6 FIB TMC POS 1 OUTPUT - A (1)		6 FIB TMC POS 1 OUTPUT - C (1)		6 FIB TMC POS 1 OUTPUT - C (1)	
			7 POS 2 OUTPUT - A (1)		7 POS 2 OUTPUT - A (1)		7 POS 2 OUTPUT - C (1)		7 POS 2 OUTPUT - C (1)	
			8 POS 3 OUTPUT - A (1)		8 POS 3 OUTPUT - A (1)		8 POS 3 OUTPUT - C (1)		8 POS 3 OUTPUT - C (1)	
			9 POS 4 OUTPUT - A (1)		9 POS 4 OUTPUT - A (1)		9 POS 4 OUTPUT - C (1)		9 POS 4 OUTPUT - C (1)	
			10 ME 1 OUTPUT - A (1)		10 ME 1 OUTPUT - A (1)		10 ME 1 OUTPUT - C (1)		10 ME 1 OUTPUT - C (1)	
			11 ME 2 OUTPUT - A (1)		11 ME 2 OUTPUT - A (1)		11 ME 2 OUTPUT - C (1)		11 ME 2 OUTPUT - C (1)	
			12 ME 3 OUTPUT - A (1)		12 ME 3 OUTPUT - A (1)		12 ME 3 OUTPUT - C (1)		12 ME 3 OUTPUT - C (1)	
			13 LH SATE TAKEOVER - A (1)		13 LH SATE TAKEOVER - A (1)		13 LH SATE TAKEOVER - C (1)		13 LH SATE TAKEOVER - C (1)	
			14		14		14		14	
			15		15		15		15	
01			0 LH INC - PITCH TRIN - A (1)		0 LH INC - PITCH TRIN - B (1)		0 LH INC - PITCH TRIN - B (1)		0 LH INC - PITCH TRIN - B (1)	
			1 PITCH TRIN - A (1)		1 PITCH TRIN - B (1)		1 PITCH TRIN - B (1)		1 PITCH TRIN - B (1)	
			2 BOLL TRIN - A (1)		2 BOLL TRIN - B (1)		2 BOLL TRIN - B (1)		2 BOLL TRIN - B (1)	
			3		3		3		3	
			4 SB SEPARATION AUTO A DO		4 SB SEPARATION AUTO B DO		4 SB SEPARATION INITIATE C DO		4 SB SEPARATION AUTO B DO	
			5 SB SEPARATION INITIATE A DO		5 SB SEPARATION INITIATE B DO		5 SB SEPARATION INITIATE C DO		5 SB SEPARATION INITIATE B DO	
			6		6		6		6	
			7		7		7		7	
			8		8		8		8	
			9		9		9		9	
			10		10		10		10	
			11		11		11		11	
			12		12		12		12	
			13		13		13		13	
			14		14		14		14	
			15		15		15		15	
00 (01H) 00			0 BUMP 1 JET P/F DRIVER (1)		0 BUMP 1 JET P/F DRIVER (1)		0 BUMP 2 JET P/F DRIVER (1)		0 BUMP 2 JET P/F DRIVER (1)	
			1 P/F DRIVER (1)		1 P/F DRIVER (1)		1 P/F DRIVER (1)		1 P/F DRIVER (1)	
			2 P/F DRIVER (1)		2 P/F DRIVER (1)		2 P/F DRIVER (1)		2 P/F DRIVER (1)	
			3 P/F DRIVER (1)		3 P/F DRIVER (1)		3 P/F DRIVER (1)		3 P/F DRIVER (1)	
			4 FIB DMP SELECT A - A (1)		4 FIB DMP SELECT A - B (1)		4 FIB DMP SELECT A - C (1)		4 FIB DMP SELECT A - C (1)	
			5 A - B (1)		5 A - B (1)		5 A - B (1)		5 A - B (1)	
			6 FIB DMP SELECT B - C (1)		6 FIB DMP SELECT B - C (1)		6 FIB DMP SELECT B - C (1)		6 FIB DMP SELECT B - C (1)	
			7 B - C (1)		7 B - C (1)		7 B - C (1)		7 B - C (1)	
			8 FIB DMP AUTO A (1)		8 FIB DMP AUTO A (1)		8 FIB DMP AUTO A (1)		8 FIB DMP AUTO A (1)	
			9 A (1)		9 A (1)		9 A (1)		9 A (1)	
			10 FIB DMP AUTO B (1)		10 FIB DMP AUTO B (1)		10 FIB DMP AUTO B (1)		10 FIB DMP AUTO B (1)	
			11 B (1)		11 B (1)		11 B (1)		11 B (1)	
			12 GATE PITCH HI FIB - A (1)		12 GATE PITCH HI FIB - B (1)		12 GATE PITCH HI FIB - C (1)		12 GATE PITCH HI FIB - C (1)	
			13 A (1)		13 A (1)		13 A (1)		13 A (1)	
			14 GATE PITCH/TAH HI FIB - A (1)		14 GATE PITCH/TAH HI FIB - B (1)		14 GATE PITCH/TAH HI FIB - C (1)		14 GATE PITCH/TAH HI FIB - C (1)	
			15 A (1)		15 A (1)		15 A (1)		15 A (1)	
01			0 SC/L - M2P POWER 1 (ON)		0 SC/L - M2P POWER 1 (ON)		0 M2S M2-2 SHUTDOWN DO B		0 M2S M2-2 SHUTDOWN DO B	
			1		1		1 SERSE M2 - 2 COM B (1)		1 SERSE M2 - 2 COM C (1)	
			2 ENTRY BOLL MODE (GATE - A (1)		2 ENTRY BOLL MODE (GATE - B (1)		2 ENTRY BOLL MODE (GATE - C (1)		2 ENTRY BOLL MODE (GATE - D (1)	
			3 B (1)		3 B (1)		3 B (1)		3 B (1)	
			4 FIB ROTATION BOLL ACCEL RATE A (1)		4 FIB ROTATION BOLL ACCEL RATE B (1)		4 FIB ROTATION BOLL DISC RATE A (1)		4 FIB ROTATION BOLL DISC RATE B (1)	
			5 B (1)		5 B (1)		5 B (1)		5 B (1)	
			6 PITCH RATE A (1)		6 PITCH RATE B (1)		6 PITCH RATE C (1)		6 PITCH RATE D (1)	
			7 B (1)		7 B (1)		7 B (1)		7 B (1)	
			8 PULSE		8 PULSE		8 PULSE		8 PULSE	
			9 YAM DISC RATE A (1)		9 YAM DISC RATE B (1)		9 YAM DISC RATE C (1)		9 YAM DISC RATE D (1)	
			10 B (1)		10 B (1)		10 B (1)		10 B (1)	
			11 PULSE		11 PULSE		11 PULSE		11 PULSE	
			12 YAM BOLL RATE A (1)		12 YAM BOLL RATE B (1)		12 YAM BOLL RATE C (1)		12 YAM BOLL RATE D (1)	
			13 B (1)		13 B (1)		13 B (1)		13 B (1)	
			14 FIB MCS JETS WORK A (1)		14 FIB MCS JETS WORK B (1)		14 FIB MCS JETS WORK B (1)		14 FIB MCS JETS WORK B (1)	
			15 B (1)		15 B (1)		15 B (1)		15 B (1)	
			16 FIB TRANSLATION B WORK A (1)		16 FIB TRANSLATION B WORK B (1)		16 FIB TRANSLATION B WORK B (1)		16 FIB TRANSLATION B WORK B (1)	

MDM FF1-FF4 INPUT CARD CHANNELIZATION (BCE STRING "B")

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MDM CARD	CHRG	BIT	NON FF 1	NON FF 2	NON FF 3	NON FF 4	COMMENTS
2	00	01	0	0	0	0	
			1	1	1	1	
			2	2	2	2	
			3	3	3	3	
			4	4	4	4	
			5	5	5	5	
			6	6	6	6	
			7	7	7	7	
			8	8	8	8	
			9	9	9	9	
			10	10	10	10	
			11	11	11	11	
			12	12	12	12	
			13	13	13	13	
			14	14	14	14	
			15	15	15	15	
			16	16	16	16	
			17	17	17	17	
			18	18	18	18	
			19	19	19	19	
			20	20	20	20	
			21	21	21	21	
			22	22	22	22	
			23	23	23	23	
			24	24	24	24	
			25	25	25	25	
			26	26	26	26	
			27	27	27	27	
			28	28	28	28	
			29	29	29	29	
			30	30	30	30	
			31	31	31	31	
			32	32	32	32	
			33	33	33	33	
			34	34	34	34	
			35	35	35	35	
			36	36	36	36	
			37	37	37	37	
			38	38	38	38	
			39	39	39	39	
			40	40	40	40	
			41	41	41	41	
			42	42	42	42	
			43	43	43	43	
			44	44	44	44	
			45	45	45	45	
			46	46	46	46	
			47	47	47	47	
			48	48	48	48	
			49	49	49	49	
			50	50	50	50	
			51	51	51	51	
			52	52	52	52	
			53	53	53	53	
			54	54	54	54	
			55	55	55	55	
			56	56	56	56	
			57	57	57	57	
			58	58	58	58	
			59	59	59	59	
			60	60	60	60	
			61	61	61	61	
			62	62	62	62	

(a) SYN FUNC: TACAN AUTO STATION SELECT, OPS 2 ON SELECT, OPS 3 ON OPS 2 POST POWER ON TACAN MUST BE AUTO SELECTED, W/S IDENTICAL

(b) CHEN CRT: OPS B ONLY

(c) SYN FUNC: ALL PASS OPS: RCS JET RW DOES NOT RUN APPROXIMATE 300 PASSES OPS 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100

(a) SYN FUNC: WITH REF PRE LOSS, ALL OPS

INPUT CARD CHANNELIZATION (BCE STRING "B")

MDM FF1-FF4

DETAILS: PARAMETERS WITH * ARE NOT USED AS PART OF THE INPUT

PACK	CHAN	CHAN	BIT	NON FF 1	NON FF 2	NON FF 3	NON FF 4	COMMENTS
2	15	(011)	00	0 IMJ - 1 IN OPERATE MODE PRESSURE GOOD PLATFORM TEMP READY CAPRI TEMP ALRTY SAFE 1 IMJ GOOD (1) 2 MT INC WEG 1 OUTPUT - A (1) 3 WEG 2 OUTPUT - A (1) 4 POS 1 OUTPUT - A (1) 5 POS 2 OUTPUT - A (1) 6 WEG 1 OUTPUT - A (1) 7 WEG 2 OUTPUT - A (1) 8 IMJ STIC TAGOVER - A (1)	0 IMJ - 3 IN OPERATE MODE PRESSURE GOOD PLATFORM TEMP READY CAPRI TEMP ALRTY SAFE 1 IMJ GOOD (1) 2 MT INC WEG 1 OUTPUT - C (1) 3 WEG 2 OUTPUT - C (1) 4 POS 1 OUTPUT - C (1) 5 POS 2 OUTPUT - C (1) 6 WEG 1 OUTPUT - C (1) 7 WEG 2 OUTPUT - C (1) 8 IMJ STIC TAGOVER - B (1)	0 IMJ - 3 IN OPERATE MODE PRESSURE GOOD PLATFORM TEMP READY CAPRI TEMP ALRTY SAFE 1 IMJ GOOD (1) 2 MT INC WEG 1 OUTPUT - C (1) 3 WEG 2 OUTPUT - C (1) 4 POS 1 OUTPUT - C (1) 5 POS 2 OUTPUT - C (1) 6 WEG 1 OUTPUT - C (1) 7 WEG 2 OUTPUT - C (1) 8 IMJ STIC TAGOVER - B (1)	0 IMJ - 3 IN OPERATE MODE PRESSURE GOOD PLATFORM TEMP READY CAPRI TEMP ALRTY SAFE 1 IMJ GOOD (1) 2 MT INC WEG 1 OUTPUT - C (1) 3 WEG 2 OUTPUT - C (1) 4 POS 1 OUTPUT - C (1) 5 POS 2 OUTPUT - C (1) 6 WEG 1 OUTPUT - C (1) 7 WEG 2 OUTPUT - C (1) 8 IMJ STIC TAGOVER - B (1)	
3	07	(015)	00	0 DASHY INPUT 1 DASHY INPUT 2 DASHY INPUT 3 DASHY INPUT 4 DASHY INPUT 5 DASHY INPUT 6 ET SEP INK ENABLE A 7 ET SEP INITIATE A 8 ET SEP AUTO A 9 MPS FALLOUT INHIBIT CND A 10 AUTO SELECT CND A	0 DASHY INPUT 1 DASHY INPUT 2 DASHY INPUT 3 DASHY INPUT 4 DASHY INPUT 5 DASHY INPUT 6 ET SEPARATION INHIBIT CND C 7 INITIATE C CND 8 AUTO C CND 9 MPS FALLOUT INHIBIT CND C 10 AUTO SELECT CND C	0 IMJ INC * PITCH TRIM - A (1) 1 PITCH TRIM - A (1) 2 ROLL TRIM - A (1) 3 ROLL TRIM - A (1) 4 ET SEP INK ENABLE B 5 INITIATE B 6 AUTO B 7 MPS FALLOUT INHIBIT CND B 8 AUTO SELECT CND B	0 IMJ INC * PITCH TRIM - B (1) 1 PITCH TRIM - B (1) 2 ROLL TRIM - B (1) 3 ROLL TRIM - B (1) 4 ET SEP INK ENABLE B 5 INITIATE B 6 AUTO B 7 MPS FALLOUT INHIBIT CND B 8 AUTO SELECT CND B	(A) CREW CRT: OPS B ONLY (A)
4	08	(018)	01	0 MCS - FWD DE THRUST INJ TEMP - F10 (1) 1 F10 (1) 2 F10 (1) 3 F10 (1) 4 F10 (1) 5 F10 (1) 6 F10 (1) 7 F10 (1)	0 MCS - FWD DE THRUST INJ TEMP - F20 (1) 1 F20 (1) 2 F20 (1) 3 F20 (1) 4 F20 (1) 5 F20 (1) 6 F20 (1) 7 F20 (1)	0 MCS - FWD DE THRUST INJ TEMP - F30 (1) 1 F30 (1) 2 F30 (1) 3 F30 (1) 4 F30 (1) 5 F30 (1) 6 F30 (1) 7 F30 (1)	0 MCS - FWD DE THRUST INJ TEMP - F40 (1) 1 F40 (1) 2 F40 (1) 3 F40 (1) 4 F40 (1) 5 F40 (1) 6 F40 (1) 7 F40 (1)	(A) S/W FUNC: NO JET LEAK DETECTION, ALL PASS OPS (A)
5	14	(019)	01	0 LH INC ROLL CND - A (1) 1 PITCH CND - A (1) 2 TAU CND - A (1) 3 LEFT MODER PEAK CND - A (1) 4 LH SATE CND - A (1) 5 LH INC ROLL CND - A (1) 6 PITCH CND - A (1) 7 TAU CND - A (1)	0 LH INC ROLL CND - B (1) 1 PITCH CND - B (1) 2 TAU CND - B (1) 3 LEFT MODER PEAK CND - B (1) 4 LH SATE CND - B (1) 5 LH INC ROLL CND - B (1) 6 PITCH CND - B (1) 7 TAU CND - B (1)	0 LH INC ROLL CND - C (1) 1 PITCH CND - C (1) 2 TAU CND - C (1) 3 LEFT MODER PEAK CND - C (1) 4 LH SATE CND - C (1) 5 LH INC ROLL CND - C (1) 6 PITCH CND - C (1) 7 TAU CND - C (1)	0 LH INC ROLL CND - C (1) 1 PITCH CND - C (1) 2 TAU CND - C (1) 3 LEFT MODER PEAK CND - C (1) 4 LH SATE CND - C (1) 5 LH INC ROLL CND - C (1) 6 PITCH CND - C (1) 7 TAU CND - C (1)	(A)
6	14	(018)	06	0 ACCEL ASSY 1 LAT ACCEL (1) 1 ACCEL (1) 2 ACCEL (1) 3 ACCEL (1)	0 ACCEL ASSY 2 LAT ACCEL (1) 1 ACCEL (1) 2 ACCEL (1) 3 ACCEL (1)	0 ACCEL ASSY 3 LAT ACCEL (1) 1 ACCEL (1) 2 ACCEL (1) 3 ACCEL (1)	0 ACCEL ASSY 4 LAT ACCEL (1) 1 ACCEL (1) 2 ACCEL (1) 3 ACCEL (1)	(A)

REV DATE: 12/04/81

MDM FF 1 - FF 4 (BCE STRING "SERIAL DEVICES")

NOTE: PARAMETERS WITH * ARE NOT USED AS PART OF THE INPUT

FROM	CARD	CHAN	BIT	MDM FF 1	BIT	MDM FF 2	BIT	MDM FF 3	BIT	MDM FF 4
11	(S10)	00		ADTA 1		ADTA 3		ADTA 3		ADTA 4
00	(TAC)	00-07		TACAN 1		TACAN 3		TACAN 3		
11	(S10)	01		MSBLS 1		MSBLS 3		MSBLS 3		
03	(S10)	00		IPI 1		IPI 3		IPI 3		
03	(S10)	01		MTU ACCUM 1		MTU ACCUM 3		MTU ACCUM 3		
03	(S10)	02		STU 1		STU 2		STU 2		
11	(S10)	03		NSP 1		NSP 2		NSP 2		

MDM PL 1 (2) INPUT CHANNELIZATION (BCE BYP "PL")

MODEL PARAMETERS WITH ANE NOT USED AS PART OF THE INPUT

REV DATE: 01/20/82

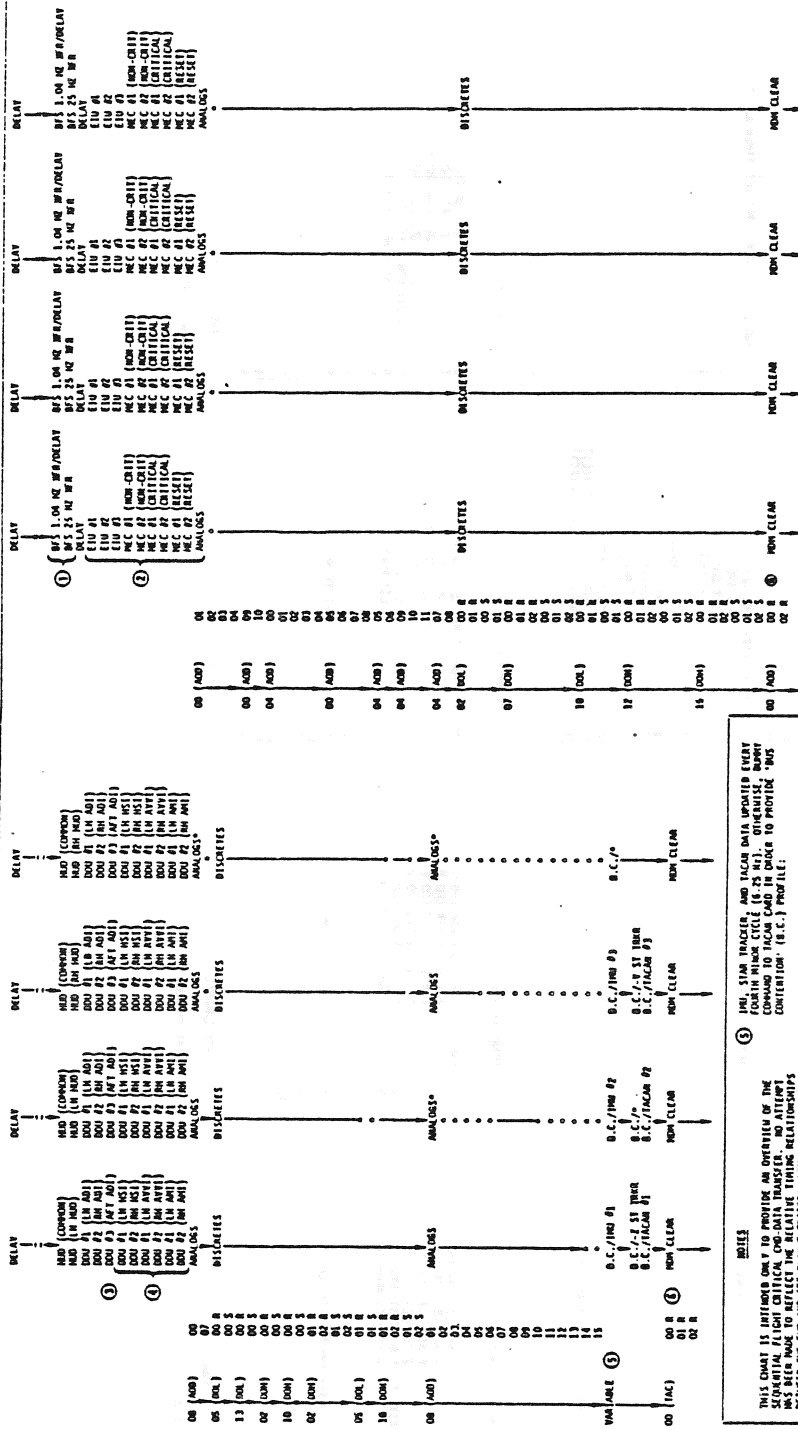
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FROM	COMP	CHAN	BIT	FROM PL 1	BIT	FROM PL 2	BIT	COMMENTS
01	(014)	00	0	0	0	0	0	(a) EACH CRT: NO DEMAND INDICATIONS FOR APPROPRIATE
			1	1	1	1	1	
			2	2	2	2	2	
			3	3	3	3	3	
			4	4	4	4	4	
			5	5	5	5	5	
			6	6	6	6	6	
			7	7	7	7	7	
			8	8	8	8	8	
			9	9	9	9	9	
			10	10	10	10	10	
			11	11	11	11	11	
			12	12	12	12	12	
			13	13	13	13	13	
			14	14	14	14	14	
			15	15	15	15	15	
01	(014)	00	0	0	0	0	0	(a)
			1	1	1	1	1	
			2	2	2	2	2	
			3	3	3	3	3	
			4	4	4	4	4	
			5	5	5	5	5	
			6	6	6	6	6	
			7	7	7	7	7	
			8	8	8	8	8	
			9	9	9	9	9	
			10	10	10	10	10	
			11	11	11	11	11	
			12	12	12	12	12	
			13	13	13	13	13	
			14	14	14	14	14	
			15	15	15	15	15	
01	(014)	00	0	0	0	0	0	(a)
			1	1	1	1	1	
			2	2	2	2	2	
			3	3	3	3	3	
			4	4	4	4	4	
			5	5	5	5	5	
			6	6	6	6	6	
			7	7	7	7	7	
			8	8	8	8	8	
			9	9	9	9	9	
			10	10	10	10	10	
			11	11	11	11	11	
			12	12	12	12	12	
			13	13	13	13	13	
			14	14	14	14	14	
			15	15	15	15	15	
01	(014)	00	0	0	0	0	0	(a)
			1	1	1	1	1	
			2	2	2	2	2	
			3	3	3	3	3	
			4	4	4	4	4	
			5	5	5	5	5	
			6	6	6	6	6	
			7	7	7	7	7	
			8	8	8	8	8	
			9	9	9	9	9	
			10	10	10	10	10	
			11	11	11	11	11	
			12	12	12	12	12	
			13	13	13	13	13	
			14	14	14	14	14	
			15	15	15	15	15	
01	(014)	00	0	0	0	0	0	(a)
			1	1	1	1	1	
			2	2	2	2	2	
			3	3	3	3	3	
			4	4	4	4	4	
			5	5	5	5	5	
			6	6	6	6	6	
			7	7	7	7	7	
			8	8	8	8	8	
			9	9	9	9	9	
			10	10	10	10	10	
			11	11	11	11	11	
			12	12	12	12	12	
			13	13	13	13	13	
			14	14	14	14	14	
			15	15	15	15	15	

(b) 3/4 FUNC: NO AUTO FC PURGE, OPS 2

HFE OUTPUT TRANSACTION OVERVIEW

REV DATE: 1/27/81



① THE "NON CLEAR" BINARY COMMANDS TO FACAM CARD (TS NON-C) OR ADD CARD (TA NON-C) HAVE ABSOLUTELY NO IMPACT ON A NORMALLY FUNCTIONING NON-C. HOWEVER, IF THE NON-C IS INITIATED WHILE THE FACAM CARD IS IN A STATE OF FAILURE, THE COMMAND WILL TAKE EFFECT. THE COMMANDS WILL TAKE EFFECT ONLY IF THE SPECIFIED CHANNELS TO BE RESET TO ZERO VDC ON ALL OF THE DISCRETE OUTPUT CARDS.

SPECIAL SYMBOLS

0 -- DISCRETE OUTPUT CARD "RESET" 000

1 -- DISCRETE OUTPUT CARD "SET" 000

• -- BINARY OUTPUT 000 (CHANNEL NOT MAINTAINED BY DATA TRANSFER) TO SUPPORT THE TPO TRANSACTION PRIORITY

② THE STAR TRACKER AND FACAM DATA UPDATED EVERY FOURTH FRAME CYCLE (8.75 Hz). OTHERWISE, BINARY COMMANDS WILL TAKE EFFECT TO PROVIDE "BUS CONVENTION" (B.C.) PROFILE:

SCAD	CHAM	FL	FSH
03 (S10)	00	100 (2 WORDS)	100 (2 WORDS)
00 (TAC)	00	ST TRKR (1 WORD)	TACAM
00 (TAC)	00	TACAM	TACAM
00 (TAC)	00	00	00
00 (TAC)	00	00	00
00 (TAC)	00	00	00

NOTE THAT FACAM CARD IS REGENERATED SUCH THAT THE CONTENTS OF CHANNELS 00, 01, 02 ARE NOT ALTERED BY THE BUS CONVENTION BINARY COMMANDS.

③ THIS CHART IS INTENDED ONLY TO PROVIDE AN OVERVIEW OF THE SEQUENTIAL FLIGHT CRITICAL ON-DATA TRANSFER. NO ATTEMPT HAS BEEN MADE TO REFLECT THE RELATIVE TIMING RELATIONSHIPS BETWEEN THE P-0 AND APT FLIGHT CRITICAL DATA.

THE FOLLOWING MATRIX REFLECTS THE IMPLICIT GAC OPS AVAILABILITY FOR THE INDICATED PARAMETERS:

①	BFS AFTER	01/02	02	03/08	YES	NO	YES	NO
②	EW's	01/02	02	03/08	YES	NO	YES	NO
③	MCC's (NON-CRIT)	01/02	02	03/08	YES	NO	YES	NO
④	MCC's (CRITICAL)	01/02	02	03/08	YES	NO	YES	NO
⑤	MCC's (RESET)	01/02	02	03/08	YES	NO	YES	NO
⑥	DOO #2 (APT ADT)	01/02	02	03/08	NO	YES	YES	NO
⑦	DOO's (MST, APPL, AMT)	01/02	02	03/08	YES	NO	YES	NO

MDM FF 1 - FF 4
OUTPUT CARD CHANNELIZATION

REV.

CARD	CHW	BIT	MON FF 1	BIT	MON FF 2	BIT	MON FF 3	BIT	MON FF 4	COMMENTS
05 (DOL)	00	0	RJDF 18: F RCS JET FIF CHO A	0	RJDF 1A: F RCS JET FZF CHO A	0	RJDF 28: F RCS JET FAR CHO A	0	RJDF 2A: F RCS JET F3F CHO A	
		1	F RCS JET FIF CHO A	1	F RCS JET FZF CHO A	1	F RCS JET FAR CHO A	1	F RCS JET F3F CHO A	
		2	F RCS JET F1U CHO A	2	F RCS JET F2A CHO B	2	F RCS JET F4D CHO B	2	F RCS JET F3U CHO B	
		3	F RCS JET F1D CHO A	3	F RCS JET F2D CHO B	3	F RCS JET F4F CHO B	3	F RCS JET F3D CHO B	
		4	AA #1: LATERAL BIITE CHO	4	AA #2: LATERAL BIITE CHO	4	AA #3: LATERAL BIITE CHO	4	AA #4: LATERAL BIITE CHO	
		5	NORMAL BIITE CHO	5	NORMAL BIITE CHO	5	NORMAL BIITE CHO	5	NORMAL BIITE CHO	
		6		6		6		6		
		7		7		7		7		
		8		8		8		8		
		9		9		9		9		
		10		10		10		10		
		11		11		11		11		
		12		12		12		12		
		13		13		13		13		
		14		14		14		14		
15		15		15		15				
01	01	0	FMO EVENT TIMER: ABORT TIMER-RESET	0	SPARE CHANNEL	0	CMW MATRIX: "RCS JET"	0	FMO EVENT TIMER: LIFT OFF TIMER-RESET	
		1		1		1	"OMS TVC"	1		
		2		2		2	"LEFT OMS"	2		
		3		3		3	"RIGHT OMS"	3		
		4		4		4	"RCS CHANNEL"	4		
		5		5		5	"FCS SATURATION"	5		
		6		6		6	"HIGH/AFT RHIC"	6		
		7		7		7	"LEFT RHIC"	7		
		8		8		8	"AIR DATA"	8		
		9		9		9	"RGA/ACCEL"	9		
		10		10		10	"RIGHT RCS" (LEAK DETECT)	10		
		11		11		11	"FMO RCS" (LEAK DETECT)	11		
		12		12		12		12		
		13		13		13		13		
		14		14		14		14		
15		15		15		15				
13 (DOL)	00	0	SPARE CHANNEL	0	SPARE CHANNEL	0	SPARE CHANNEL	0	SPARE CHANNEL	
		1		1		1		1		
		2		2		2		2		
		3		3		3		3		
		4		4		4		4		
		5		5		5		5		
		6		6		6		6		
		7		7		7		7		
		8		8		8		8		
		9		9		9		9		
		10		10		10		10		
		11		11		11		11		
		12		12		12		12		
		13		13		13		13		
		14		14		14		14		
15		15		15		15				
01	01	0	RJDF 18: F RCS JET FIF CHO B	0	RJDF 1A: F RCS JET FZF CHO B	0	RJDF 28: F RCS JET FAR CHO B	0	RJDF 2A: F RCS JET F3F CHO B	
		1	F RCS JET FIF CHO B	1	F RCS JET FZF CHO B	1	F RCS JET FAR CHO B	1	F RCS JET F3F CHO B	
		2	F RCS JET F1U CHO B	2	F RCS JET F2A CHO B	2	F RCS JET F4D CHO B	2	F RCS JET F3U CHO B	
		3	F RCS JET F1D CHO B	3	F RCS JET F2D CHO B	3	F RCS JET F4F CHO B	3	F RCS JET F3D CHO B	
		4	ADTA #1: LOW TEST MODE CHO	4	ADTA #2: LOW TEST MODE CHO	4	ADTA #3: LOW TEST MODE CHO	4	ADTA #4: LOW TEST MODE CHO	
		5	HIGH TEST MODE CHO	5	HIGH TEST MODE CHO	5	HIGH TEST MODE CHO	5	HIGH TEST MODE CHO	
		6		6		6		6		
		7		7		7		7		
		8		8		8		8		
		9		9		9		9		
		10		10		10		10		
		11		11		11		11		
		12		12		12		12		
		13		13		13		13		
		14		14		14		14		
15		15		15		15				
02	02	0	SPARE CHANNEL	0	SPARE CHANNEL	0	SPARE CHANNEL	0	SPARE CHANNEL	
		1		1		1		1		
		2		2		2		2		
		3		3		3		3		
		4		4		4		4		
		5		5		5		5		
		6		6		6		6		
		7		7		7		7		
		8		8		8		8		
		9		9		9		9		
		10		10		10		10		
		11		11		11		11		
		12		12		12		12		
		13		13		13		13		
		14		14		14		14		
15		15		15		15				
01	01	0	IMU #1: IMU OPERATE MODE CHO	0	IMU #2: IMU OPERATE MODE CHO	0	IMU #3: IMU OPERATE MODE CHO	0	IMU #4: IMU OPERATE MODE CHO	
		1	SPT: DATA VALID CHO ("OP" FLAG)	1		1		1		
		2		2		2		2		
		3		3		3		3		
		4		4		4		4		
		5		5		5		5		
		6		6		6		6		
		7		7		7		7		
		8		8		8		8		
		9		9		9		9		
		10		10		10		10		
		11		11		11		11		
		12		12		12		12		
		13		13		13		13		
		14		14		14		14		
15		15		15		15				
02	02	0	SPARE CHANNEL	0	SPARE CHANNEL	0	SPARE CHANNEL	0	SPARE CHANNEL	
		1		1		1		1		
		2		2		2		2		
		3		3		3		3		
		4		4		4		4		
		5		5		5		5		
		6		6		6		6		
		7		7		7		7		
		8		8		8		8		
		9		9		9		9		
		10		10		10		10		
		11		11		11		11		
		12		12		12		12		
		13		13		13		13		
		14		14		14		14		
15		15		15		15				

MDM FF 1 - FF 4
OUTPUT CARD CHANNELIZATION

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CARD	CHAN	BIT	MDM FF 1	BIT	MDM FF 2	BIT	MDM FF 3	BIT	MDM FF 4	COMMENTS
02	00	0	RH VERTS 1/2: MOTOR 1/CLOSE B (CL/18)	0	LH VERTS 1/2: MOTOR 2/CLOSE B (CL/28)	0	LH VERT 3: MOTOR 1/OPEN B (OP/18)	0	RH VERT 3: MOTOR 2/OPEN B (OP/28)	
		1	MOTOR 1/PURGE B (PG/18)	1	MOTOR 2/OPEN B (OP/28)	1	LH VERTS 1/2: MOTOR 1/OPEN B (OP/18)	1	RH VERTS 1/2: MOTOR 2/OPEN B (OP/28)	
		2	MOTOR 1/PURGE B (PG/18)	2	MOTOR 2/PURGE B (PG/28)	2	LH VERTS 1/2: MOTOR 1/PURGE B (PG/18)	2	MOTOR 2/PURGE B (PG/28)	
		3	F RCS: MANF 1 ISOL VLV GPC CL A (OR)	3	F RCS: MANF 2 ISOL VLV GPC CL A (OR)	3	F RCS: MANF 3 ISOL VLV GPC CL A (OR)	3	F RCS: MANF 4 ISOL VLV GPC CL A (OR)	
		4	OX TK ISOL VLV 3/4/5 GPC CL B	4	OX TK ISOL VLV 3/4/5 GPC CL B	4	OX TK ISOL VLV 3/4/5 GPC CL B	4	OX TK ISOL VLV 3/4/5 GPC CL B	
		5	OX TK ISOL VLV 3/4/5 GPC CL B	5	OX TK ISOL VLV 3/4/5 GPC CL B	5	OX TK ISOL VLV 3/4/5 GPC CL B	5	OX TK ISOL VLV 3/4/5 GPC CL B	
		6	TANK ISOL VLV 3/4/5 GPC CL A	6	TANK ISOL VLV 3/4/5 GPC CL A	6	TANK ISOL VLV 3/4/5 GPC CL A	6	TANK ISOL VLV 3/4/5 GPC CL A	
		7	MOSE WHEEL STEERING: GND SPEED ENABLE	7	MOSE WHEEL STEERING: GND SPEED ENABLE	7	MOSE WHEEL STEERING: GND SPEED ENABLE	7	MOSE WHEEL STEERING: GND SPEED ENABLE	
		8		8		8		8		
		9		9		9		9		
		10		10		10		10		
		11		11		11		11		
		12		12		12		12		
		13		13		13		13		
		14		14		14		14		
		15		15		15		15		
01	0	F7 LIGHT: C MPS AMBER STATUS	0	F7 LIGHT: L MPS AMBER STATUS	0	F7 LIGHT: R MPS AMBER STATUS	0	F7 LIGHT: R MPS AMBER STATUS	0	
	1	F2 LIGHT: LH EVENT SEQ "G"	1	F2 LIGHT: LH EVENT SEQ "G"	1	F2 LIGHT: RH EVENT SEQ "G"	1	F2 LIGHT: RH EVENT SEQ "G"	1	
	2	LH EVENT SEQ "COMF16"	2	LH EVENT SEQ "COMF16"	2	RH EVENT SEQ "COMF16"	2	RH EVENT SEQ "COMF16"	2	
	3	LH EVENT SEQ "PREFLAME"	3	LH EVENT SEQ "PREFLAME"	3	RH EVENT SEQ "PREFLAME"	3	RH EVENT SEQ "PREFLAME"	3	
	4	LH EVENT SEQ "SEAN"	4	LH EVENT SEQ "SEAN"	4	RH EVENT SEQ "SEAN"	4	RH EVENT SEQ "SEAN"	4	
	5	LH EVENT SEQ "MAN"	5	LH EVENT SEQ "MAN"	5	RH EVENT SEQ "MAN"	5	RH EVENT SEQ "MAN"	5	
	6		6		6		6		6	LH VERT 5: MOTOR 2/CLOSE B (CL/28)
	7	F6 LIGHT A: RCS CHD "ROLL LEFT"	7	F6 LIGHT A: RCS CHD "ROLL LEFT"	7	F6 LIGHT B: RCS CHD "ROLL LEFT"	7	F6 LIGHT B: RCS CHD "ROLL LEFT"	7	
	8	RCS CHD "ROLL RIGHT"	8	RCS CHD "ROLL RIGHT"	8	RCS CHD "YAW LEFT"	8	RCS CHD "YAW LEFT"	8	
	9	RCS CHD "YAW LEFT"	9	RCS CHD "YAW LEFT"	9	RCS CHD "YAW RIGHT"	9	RCS CHD "YAW RIGHT"	9	
	10	RCS CHD "YAW RIGHT"	10	RCS CHD "YAW RIGHT"	10	RCS CHD "PITCH UP"	10	RCS CHD "PITCH UP"	10	
	11	RCS CHD "PITCH UP"	11	RCS CHD "PITCH UP"	11	RCS CHD "PITCH DOWN"	11	RCS CHD "PITCH DOWN"	11	
	12	RCS CHD "PITCH DOWN"	12	RCS CHD "PITCH DOWN"	12		12		12	
	13	C3 LIGHT: FWD DAP CONTROL "AUTO"	13	FWD DAP SELECT "A"	13		13		13	
	14	FWD DAP SELECT "A"	14	FWD DAP SELECT "A"	14		14		14	
	15	FWD DAP RCS JETS "MORH"	15	FWD DAP RCS JETS "MORH"	15		15		15	
02	0	L OMS TVC: PRI ENABLE 1 ("ACTIVE")	0	L OMS TVC: SEC ENABLE 1 ("STBY")	0	L OMS TVC: SEC ENABLE 2 ("STBY")	0	R OMS TVC: SEC ENABLE 1 ("STBY")	0	R OMS TVC: PRI ENABLE 1 ("ACTIVE")
	1	PRI ENABLE 1 ("ACTIVE")	1	SEC ENABLE 1 ("STBY")	1	SEC ENABLE 2 ("STBY")	1	SEC ENABLE 1 ("STBY")	1	PRI ENABLE 2 ("ACTIVE")
	2	FWD DAP CONTROL "MAN"	2	FWD DAP CONTROL "MAN"	2	FWD DAP SELECT "B"	2	FWD DAP CONTROL "MAN"	2	PRI ENABLE 2 ("ACTIVE")
	3	FWD DAP SELECT "B"	3	FWD DAP SELECT "B"	3		3	FWD DAP SELECT "B"	3	
	4	FWD DAP RCS JETS "VERH"	4	FWD DAP RCS JETS "VERH"	4		4	FWD DAP SELECT "B"	4	
	5		5		5		5	FWD DAP RCS JETS "VERH"	5	
	6	RH VERTS 4/7: MOTOR 2/OPEN B (OP/28)	6	LH VERT 3: MOTOR 1/CLOSE B (CL/18)	6	LH VERTS 4/7: MOTOR 1/CLOSE B (CL/18)	6	LH VERT 3: MOTOR 1/CLOSE B (CL/18)	6	MOTOR 2/CLOSE B (CL/28)
	7	RH VERT 3: MOTOR 1/CLOSE B (CL/18)	7	LH VERTS 4/7: MOTOR 2/OPEN B (OP/28)	7	LH VERTS 4/7: MOTOR 2/OPEN B (OP/28)	7	LH VERTS 4/7: MOTOR 1/CLOSE B (CL/18)	7	MOTOR 2/CLOSE B (CL/28)
	8	MOTOR 1/CLOSE B (CL/18)	8	LH VERTS 4/7: MOTOR 2/OPEN B (OP/28)	8	LH VERTS 4/7: MOTOR 2/OPEN B (OP/28)	8	LH VERTS 4/7: MOTOR 1/CLOSE B (CL/18)	8	MOTOR 1/CLOSE B (CL/18)
	9	MOTOR 1/CLOSE B (CL/18)	9	LH VERT 6: MOTOR 1/OPEN B (OP/18)	9	LH VERTS 4/7: MOTOR 2/OPEN B (OP/28)	9	LH VERTS 4/7: MOTOR 1/CLOSE B (CL/18)	9	MOTOR 1/OPEN B (OP/18)
	10	LH VERT 6: MOTOR 1/OPEN B (OP/18)	10	MOTOR 2/OPEN B (OP/28)	10	MOTOR 2/OPEN B (OP/28)	10	LH VERTS 4/7: MOTOR 1/CLOSE B (CL/18)	10	MOTOR 2/OPEN B (OP/28)
	11	MOTOR 2/OPEN B (OP/28)	11	MOTOR 2/OPEN B (OP/28)	11	MOTOR 2/OPEN B (OP/28)	11	LH VERTS 4/7: MOTOR 1/CLOSE B (CL/18)	11	MOTOR 2/OPEN B (OP/28)
	12	MOTOR 2/OPEN B (OP/28)	12	MOTOR 2/PAG-1 B (P1/18)	12	MOTOR 2/PAG-1 B (P1/18)	12	LH VERTS 4/7: MOTOR 1/CLOSE B (CL/18)	12	MOTOR 2/PAG-1 B (P1/18)
	13	MOTOR 2/PAG-1 B (P1/18)	13	MOTOR 2/PAG-2 B (P2/18)	13	MOTOR 2/PAG-2 B (P2/18)	13	LH VERTS 4/7: MOTOR 1/CLOSE B (CL/18)	13	MOTOR 2/PAG-2 B (P2/18)
	14	MOTOR 2/PAG-2 B (P2/18)	14	MOTOR 1/OPEN B (OP/18)	14	MOTOR 1/OPEN B (OP/18)	14	LH VERTS 4/7: MOTOR 1/CLOSE B (CL/18)	14	MOTOR 1/OPEN B (OP/18)
	15	MOTOR 1/OPEN B (OP/18)	15	MOTOR 2/OPEN B (OP/28)	15	MOTOR 2/OPEN B (OP/28)	15	LH VERTS 4/7: MOTOR 1/CLOSE B (CL/18)	15	MOTOR 2/OPEN B (OP/28)

REV.

MDM FF 1 - FF 4
OUTPUT CARD CHANNELIZATION

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CARD	CHAN	BIT	MDM FF 1	BIT	MDM FF 2	BIT	MDM FF 3	BIT	MDM FF 4	COMMENTS
10	(004)	00	0 RH VENTS 1/2: MOTOR 1/CLOSE A (CL/1A) MOTOR 1/OPEN A (OP/1A) MOTOR 1/PURGE A (PG/1A)	0 LH VENTS 1/2: MOTOR 2/CLOSE A (CL/2A) MOTOR 2/OPEN A (OP/2A) MOTOR 2/PURGE A (PG/2A)	0 LH VENTS 1/2: MOTOR 1/CLOSE A (CL/1A) MOTOR 1/OPEN A (OP/1A)	0 RH VENTS 1/2: MOTOR 2/CLOSE A (CL/2A) MOTOR 2/OPEN A (OP/2A)	0 RH VENTS 1/2: MOTOR 2/CLOSE A (CL/2A) MOTOR 2/OPEN A (OP/2A)	0 RH VENTS 1/2: MOTOR 2/CLOSE A (CL/2A) MOTOR 2/OPEN A (OP/2A)	0 RH VENTS 1/2: MOTOR 2/CLOSE A (CL/2A) MOTOR 2/OPEN A (OP/2A)	
		1	F2 LIGHT: LH FCS BODY FLAP "MAN"	F2 LIGHT: LH FCS BODY FLAP "MAN"	F4 LIGHT: RH FCS BODY FLAP "AUTO"	F4 LIGHT: RH FCS BODY FLAP "AUTO"	F4 LIGHT: RH FCS BODY FLAP "AUTO"	F4 LIGHT: RH FCS BODY FLAP "AUTO"	F4 LIGHT: RH FCS BODY FLAP "MAN"	
		2	LH FCS SPEED BRK "AUTO"	LH FCS SPEED BRK "MAN"	RH FCS SPEED BRK "AUTO"	RH FCS SPEED BRK "MAN"	RH FCS SPEED BRK "AUTO"	RH FCS SPEED BRK "MAN"	RH FCS SPEED BRK "MAN"	
		3	LH FCS PITCH "AUTO"	LH FCS PITCH "MAN"	RH FCS PITCH "AUTO"	RH FCS PITCH "MAN"	RH FCS PITCH "AUTO"	RH FCS PITCH "MAN"	RH FCS PITCH "MAN"	
		4	LH FCS ROLL "MAN"	LH FCS ROLL "CSS"	RH FCS ROLL "MAN"	RH FCS ROLL "CSS"	RH FCS ROLL "MAN"	RH FCS ROLL "CSS"	RH FCS ROLL "MAN"	
		5	LH FCS ROLL/YAW "CSS"	LH FCS ROLL/YAW "CSS"	RH FCS ROLL/YAW "MAN"	RH FCS ROLL/YAW "CSS"	RH FCS ROLL/YAW "MAN"	RH FCS ROLL/YAW "CSS"	RH FCS ROLL/YAW "CSS"	
		6	F RCS: FU TK 150L VLV 3/4/5 GPC OP	F RCS: FU TK 150L VLV 3/4/5 GPC CL B	F RCS: FU TK 150L VLV 1/2 GPC OP	F RCS: FU TK 150L VLV 1/2 GPC CL B	F RCS: FU TK 150L VLV 1/2 GPC OP	F RCS: FU TK 150L VLV 1/2 GPC CL B	F RCS: MANF 2 150L VLV GPC CL B (OR)	
		7	HE PRESS VLV A GPC OP	HE PRESS VLV A GPC CL	HE PRESS VLV B GPC OP	HE PRESS VLV B GPC CL	HE PRESS VLV B GPC OP	HE PRESS VLV B GPC CL	HE PRESS VLV B GPC CL	
		8	MANF 4 150L VLV GPC CL B (OR)	MANF 4 150L VLV GPC CL B (OR)	MANF 5 150L VLV GPC OP	MANF 5 150L VLV GPC CL B (OR)	MANF 5 150L VLV GPC OP	MANF 5 150L VLV GPC CL B (OR)	MANF 5 150L VLV GPC CL B (OR)	
		9	F7 LIGHT: C WPS RED STATUS	F7 LIGHT: L WPS RED STATUS	F7 LIGHT: B WPS RED STATUS	F7 LIGHT: B WPS RED STATUS	F7 LIGHT: B WPS RED STATUS	F7 LIGHT: B WPS RED STATUS	F7 LIGHT: B WPS RED STATUS	
		10	C3 LIGHT: FWD MAN ROT ROLL "DISC RT"	C3 LIGHT: FWD MAN ROT ROLL "ACCEL"	A6 LIGHT: AFT MAN ROT ROLL "DISC RT"	A6 LIGHT: AFT MAN ROT ROLL "ACCEL"	A6 LIGHT: AFT MAN ROT ROLL "DISC RT"	A6 LIGHT: AFT MAN ROT ROLL "ACCEL"	A6 LIGHT: AFT MAN ROT ROLL "DISC RT"	
		11	FWD MAN ROT ROLL "ACCEL"	FWD MAN ROT ROLL "PULSE"	AFT MAN ROT ROLL "DISC RT"	AFT MAN ROT ROLL "PULSE"	AFT MAN ROT ROLL "DISC RT"	AFT MAN ROT ROLL "PULSE"	AFT MAN ROT ROLL "DISC RT"	
		12	FWD MAN ROT PITCH "DISC RT"	FWD MAN ROT PITCH "ACCEL"	AFT MAN ROT PITCH "DISC RT"	AFT MAN ROT PITCH "ACCEL"	AFT MAN ROT PITCH "DISC RT"	AFT MAN ROT PITCH "ACCEL"	AFT MAN ROT PITCH "DISC RT"	
		13	FWD MAN ROT PITCH "ACCEL"	FWD MAN ROT PITCH "PULSE"	AFT MAN ROT PITCH "DISC RT"	AFT MAN ROT PITCH "PULSE"	AFT MAN ROT PITCH "DISC RT"	AFT MAN ROT PITCH "PULSE"	AFT MAN ROT PITCH "DISC RT"	
		14	FWD MAN ROT YAW "DISC RT"	FWD MAN ROT YAW "ACCEL"	AFT MAN ROT YAW "DISC RT"	AFT MAN ROT YAW "ACCEL"	AFT MAN ROT YAW "DISC RT"	AFT MAN ROT YAW "ACCEL"	AFT MAN ROT YAW "DISC RT"	
		15	FWD MAN ROT YAW "ACCEL"	FWD MAN ROT YAW "PULSE"	AFT MAN ROT YAW "DISC RT"	AFT MAN ROT YAW "PULSE"	AFT MAN ROT YAW "DISC RT"	AFT MAN ROT YAW "PULSE"	AFT MAN ROT YAW "DISC RT"	
		16	FWD MAN TRANS X "WORN"	FWD MAN TRANS X "PULSE"	AFT MAN TRANS X "WORN"	AFT MAN TRANS X "PULSE"	AFT MAN TRANS X "WORN"	AFT MAN TRANS X "PULSE"	AFT MAN TRANS X "WORN"	
		17	FWD MAN TRANS Y "WORN"	FWD MAN TRANS Y "PULSE"	AFT MAN TRANS Y "WORN"	AFT MAN TRANS Y "PULSE"	AFT MAN TRANS Y "WORN"	AFT MAN TRANS Y "PULSE"	AFT MAN TRANS Y "WORN"	
		18	FWD MAN TRANS Z "WORN"	FWD MAN TRANS Z "PULSE"	AFT MAN TRANS Z "WORN"	AFT MAN TRANS Z "PULSE"	AFT MAN TRANS Z "WORN"	AFT MAN TRANS Z "PULSE"	AFT MAN TRANS Z "WORN"	
		19	FWD MAN TRANS Y "LOW Z"	FWD MAN TRANS Y "LOW Z"	AFT MAN TRANS Y "LOW Z"	AFT MAN TRANS Y "LOW Z"	AFT MAN TRANS Y "LOW Z"	AFT MAN TRANS Y "LOW Z"	AFT MAN TRANS Y "LOW Z"	
		20	C3 LIGHT: FWD MAN TRANS Z "WORN"	C3 LIGHT: FWD MAN TRANS Z "PULSE"	A6 LIGHT: AFT MAN TRANS Z "WORN"	A6 LIGHT: AFT MAN TRANS Z "PULSE"	A6 LIGHT: AFT MAN TRANS Z "WORN"	A6 LIGHT: AFT MAN TRANS Z "PULSE"	A6 LIGHT: AFT MAN TRANS Z "WORN"	
		21	FWD MAN TRANS Z "PULSE"	FWD MAN TRANS Z "HIGH"	AFT MAN TRANS Z "HIGH"	AFT MAN TRANS Z "HIGH"	AFT MAN TRANS Z "HIGH"	AFT MAN TRANS Z "HIGH"	AFT MAN TRANS Z "HIGH"	
		22	CMW MATRIX: "BACKUP C/W ALARM" (OR)	CMW MATRIX: "BACKUP C/W ALARM" (OR)	CMW MATRIX: "BACKUP C/W ALARM" (OR)	CMW MATRIX: "BACKUP C/W ALARM" (OR)	CMW MATRIX: "BACKUP C/W ALARM" (OR)	CMW MATRIX: "BACKUP C/W ALARM" (OR)	CMW MATRIX: "BACKUP C/W ALARM" (OR)	
		23	SM ALERT: TONE A CND 1 (OR)	SM ALERT: TONE A CND 2 (OR)	SM ALERT: TONE A CND 3 (OR)	SM ALERT: TONE A CND 4 (OR)	SM ALERT: TONE A CND 5 (OR)	SM ALERT: TONE A CND 6 (OR)	SM ALERT: TONE A CND 7 (OR)	
		24	RH VENTS 4/7: MOTOR 2/CLOSE A (CL/2A)	RH VENTS 4/7: MOTOR 2/CLOSE A (CL/2A)	LH VENT 3: MOTOR 1/CLOSE A (CL/1A)	LH VENT 3: MOTOR 1/PURGE A (PG/1A)	LH VENT 3: MOTOR 1/CLOSE A (CL/1A)	LH VENT 3: MOTOR 1/PURGE A (PG/1A)	RH VENT 3: MOTOR 2/CLOSE A (CL/2A)	
		25	RH VENT 3: MOTOR 2/OPEN A (OP/2A)	RH VENT 3: MOTOR 2/OPEN A (OP/2A)	LH VENT 4/7: MOTOR 2/CLOSE A (CL/2A)	LH VENT 4/7: MOTOR 2/OPEN A (OP/2A)	LH VENT 4/7: MOTOR 2/CLOSE A (CL/2A)	LH VENT 4/7: MOTOR 2/OPEN A (OP/2A)	RH VENT 4/7: MOTOR 1/OPEN A (OP/1A)	
		26	RH VENT 6: MOTOR 1/OPEN A (OP/1A)	RH VENT 6: MOTOR 2/OPEN A (OP/2A)	RH VENT 6: MOTOR 2/CLOSE A (CL/2A)	RH VENT 6: MOTOR 1/OPEN A (OP/1A)	RH VENT 6: MOTOR 2/CLOSE A (CL/2A)	RH VENT 6: MOTOR 1/OPEN A (OP/1A)	RH VENT 6: MOTOR 2/OPEN A (OP/2A)	
		27	MOTOR 1/PRG-1 A (P1/1A)	MOTOR 2/PRG-1 A (P2/1A)	MOTOR 1/PRG-1 A (P1/1A)	MOTOR 2/PRG-1 A (P2/1A)	MOTOR 1/PRG-1 A (P1/1A)	MOTOR 2/PRG-1 A (P2/1A)	MOTOR 1/PRG-1 A (P1/1A)	
		28	MOTOR 1/PRG-2 A (P2/1A)	MOTOR 2/PRG-2 A (P2/2A)	MOTOR 1/PRG-2 A (P2/1A)	MOTOR 2/PRG-2 A (P2/2A)	MOTOR 1/PRG-2 A (P2/1A)	MOTOR 2/PRG-2 A (P2/2A)	MOTOR 1/PRG-2 A (P2/1A)	
		29	RH VENT 5: MOTOR 3/CLOSE A (CL/3A)	RH VENT 5: MOTOR 2/CLOSE A (CL/2A)	RH VENT 5: MOTOR 1/CLOSE A (CL/1A)	RH VENT 5: MOTOR 3/CLOSE A (CL/3A)	RH VENT 5: MOTOR 2/CLOSE A (CL/2A)	RH VENT 5: MOTOR 1/CLOSE A (CL/1A)	RH VENT 5: MOTOR 3/CLOSE A (CL/3A)	
		30	MOTOR 1/OPEN A (OP/1A)	MOTOR 2/OPEN A (OP/2A)	MOTOR 1/OPEN A (OP/1A)	MOTOR 2/OPEN A (OP/2A)	MOTOR 1/OPEN A (OP/1A)	MOTOR 2/OPEN A (OP/2A)	MOTOR 1/OPEN A (OP/1A)	

MDM FF 1-FF 4
OUTPUT CARD CHANNELIZATION

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CARD	CHAM	BIT	MM FF 1	BIT	MM FF 2	BIT	MM FF 3	BIT	MM FF 4	COMMENTS
00 (IAC)	06	TACAM #1: AUTO CNTL WORD	TACAM #2: AUTO CNTL WORD	TACAM #3: AUTO CNTL WORD						CARD NOT USED
		0-1 X/Y MODE (STATION SELECT)	0-1 X/Y MODE (STATION SELECT)	0-1 X/Y MODE (STATION SELECT)						
		2 AIR-TO-AIR SELECT (NOT USED)	2 AIR-TO-AIR SELECT (NOT USED)	2 AIR-TO-AIR SELECT (NOT USED)						
		3 XMIT/RCV OR REV MODE SELECT	3 XMIT/RCV OR REV MODE SELECT	3 XMIT/RCV OR REV MODE SELECT						
		4 CHANNEL ID SELECT BITS	4 CHANNEL ID SELECT BITS	4 CHANNEL ID SELECT BITS						
		5 TACAM BITE-TEST CHD	5 TACAM BITE-TEST CHD	5 TACAM BITE-TEST CHD						
		6 TACAM BITE-TEST CHD	6 TACAM BITE-TEST CHD	6 TACAM BITE-TEST CHD						
		7-14 TACAM BITE-TEST CHD	7-14 TACAM BITE-TEST CHD	7-14 TACAM BITE-TEST CHD						
		15 TACAM BITE-TEST CHD	15 TACAM BITE-TEST CHD	15 TACAM BITE-TEST CHD						
07	TACAM #1/A: AUTO ANT CNTL WORD	TACAM #2/A: AUTO ANT CNTL WORD								CARD NOT USED
	0-3 INHIBIT TACAM ANTENNA-SELECT	0-3 INHIBIT TACAM ANTENNA-SELECT								
	4 UPPER/LOWER ANTENNA SELECT	4 UPPER/LOWER ANTENNA SELECT								
	5 RADAR ALTIMETER BITE-TEST CHD	5 RADAR ALTIMETER BITE-TEST CHD								
	6 RADAR ALTIMETER BITE-TEST CHD	6 RADAR ALTIMETER BITE-TEST CHD								
	7-15		7-15	7-15						
03 (SIO)	00	IMU #1: SERIAL CNTL WORD #1	IMU #2: SERIAL CNTL WORD #1	IMU #3: SERIAL CNTL WORD #1						CARD NOT USED
		0-4 X TORQUE CHD	0-4 X TORQUE CHD	0-4 X TORQUE CHD						
		5-9 Y TORQUE CHD	5-9 Y TORQUE CHD	5-9 Y TORQUE CHD						
		10-14 Z TORQUE CHD	10-14 Z TORQUE CHD	10-14 Z TORQUE CHD						
		15	15	15						
		IMU #1: SERIAL CNTL WORD #2	IMU #2: SERIAL CNTL WORD #2	IMU #3: SERIAL CNTL WORD #2						
		0 CAPRI SCALE FACTOR SELECT	0 CAPRI SCALE FACTOR SELECT	0 CAPRI SCALE FACTOR SELECT						
		1 SLEW +1 CHD	1 SLEW +1 CHD	1 SLEW +1 CHD						
		2 SLEW -1 CHD	2 SLEW -1 CHD	2 SLEW -1 CHD						
		3 SLEW +Y CHD	3 SLEW +Y CHD	3 SLEW +Y CHD						
		4 SLEW -Y CHD	4 SLEW -Y CHD	4 SLEW -Y CHD						
		5 SLEW +Z CHD	5 SLEW +Z CHD	5 SLEW +Z CHD						
		6 SLEW -Z CHD	6 SLEW -Z CHD	6 SLEW -Z CHD						
		7-15	7-15	7-15						
01	MTU UPDATE CHAN #1: SERIAL WORD #1	MTU UPDATE CHAN #2: SERIAL WORD #1	MTU UPDATE CHAN #3: SERIAL WORD #1							CARD NOT USED
	0-2 "DAYS" UPDATE BITS	0-2 "DAYS" UPDATE BITS	0-2 "DAYS" UPDATE BITS							
	3-15 "HRS" UPDATE BITS	3-15 "HRS" UPDATE BITS	3-15 "HRS" UPDATE BITS							
	10-15 "MIN" UPDATE BITS	10-15 "MIN" UPDATE BITS	10-15 "MIN" UPDATE BITS							
	MTU UPDATE CHAN #1: SERIAL WORD #2	MTU UPDATE CHAN #2: SERIAL WORD #2	MTU UPDATE CHAN #3: SERIAL WORD #2							
	0-6 "MIN" UPDATE BITS	0-6 "MIN" UPDATE BITS	0-6 "MIN" UPDATE BITS							
	7-13 "SEC" UPDATE BITS	7-13 "SEC" UPDATE BITS	7-13 "SEC" UPDATE BITS							
	14,15	14,15	14,15							
	MTU UPDATE CHAN #1: SERIAL WORD #3	MTU UPDATE CHAN #2: SERIAL WORD #3	MTU UPDATE CHAN #3: SERIAL WORD #3							
	0-2 "HILLT-SEC" UPDATE BITS	0-2 "HILLT-SEC" UPDATE BITS	0-2 "HILLT-SEC" UPDATE BITS							
	3-15 "HILLT-SEC" UPDATE BITS	3-15 "HILLT-SEC" UPDATE BITS	3-15 "HILLT-SEC" UPDATE BITS							
	MTU UPDATE CHAN #1: SERIAL WORD #4	MTU UPDATE CHAN #2: SERIAL WORD #4	MTU UPDATE CHAN #3: SERIAL WORD #4							
	0-3 UPDATE MODE CNTL (GMT VS MET)	0-3 UPDATE MODE CNTL (GMT VS MET)	0-3 UPDATE MODE CNTL (GMT VS MET)							
	4-10 COINCIDENCE TIME (MIN)	4-10 COINCIDENCE TIME (MIN)	4-10 COINCIDENCE TIME (MIN)							
	11-15	11-15	11-15							
02	-Z STAR TRACKER: SERIAL CHD WORD	-Y STAR TRACKER: SERIAL CHD WORD								CARD NOT USED
	0 OFFSET-MODE CHD	0 OFFSET-MODE CHD								
	1 SELF-TEST CHD	1 SELF-TEST CHD								
	2 BREAK-TRACK CHD	2 BREAK-TRACK CHD								
	3 SHUTTER-OPEN CHD	3 SHUTTER-OPEN CHD								
	4 BRIGHTNESS-THRESHOLD SELECT	4 BRIGHTNESS-THRESHOLD SELECT								
	5 HORIZONTAL OFFSET-CHD BITS	5 HORIZONTAL OFFSET-CHD BITS								
	6-10 HORIZONTAL OFFSET-CHD BITS	6-10 HORIZONTAL OFFSET-CHD BITS								
	11-15 VERTICAL OFFSET-CHD BITS	11-15 VERTICAL OFFSET-CHD BITS								
03	SPARE CHANNEL	SPARE CHANNEL	SPARE CHANNEL							CARD NOT USED

MDM FF 1 - FF 4 OUTPUT CARD CHANNELIZATION

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REV.

CARD	CHAN	BIT	MDM FF 1	BIT	MDM FF 2	BIT	MDM FF 3	BIT	MDM FF 4	COMMENTS
08 (ADD)	00		F7 TAPE MTR: MPS PRESS "C" MPS PC"		F7 TAPE MTR: MPS PRESS "L" MPS PC"		F7 TAPE MTR: MPS PRESS "M" MPS PC"		CARD NOT USED	
	01		03 PAPRTY QTY MTR: F ACS DTID		SPARE CHANNEL		03 PAPRTY QTY MTR: F ACS FUEL			
	02		L ACS DTID		SPARE CHANNEL		L ACS FUEL			
	03		R ACS DTID		SPARE CHANNEL		R ACS FUEL			
	04		L ACS LOWEST		SPARE CHANNEL		R ACS LOWEST			
	05		R ACS LOWEST		SPARE CHANNEL					
	06		OMS KIT FU TANK		SPARE CHANNEL		03 PAPRTY QTY MTR: OMS KIT FU TANK			
	07		OMS KIT FU TANK		SPARE CHANNEL					
	08		SPI: SPEED BRK "COMMAND"		MOSE WHEEL STEERING CMD		SPARE CHANNEL			
	09		"RUDDER" POSITION		SPI: "BODY FLAP" POSITION		SPARE CHANNEL			
	10		"SPEEDBRAKE" POSITION		SPARE CHANNEL		SPARE CHANNEL			
	11		"ELEVONS" L INBD POSITION		SPARE CHANNEL		SPARE CHANNEL			
	12		"ELEVONS" L OTBD POSITION		SPARE CHANNEL		SPARE CHANNEL			
	13		"ELEVONS" R INBD POSITION		SPARE CHANNEL		SPARE CHANNEL			
	14		"ELEVONS" R OTBD POSITION		SPARE CHANNEL		SPARE CHANNEL			
	15		SPARE CHANNEL		SPARE CHANNEL		SPARE CHANNEL			
11 (S10)	01		M.S #1: SERIAL TEST WORD		M.S #2: SERIAL TEST WORD		M.S #3: SERIAL TEST WORD		SPARE CHANNEL	
			0 BITE TEST CMD		0 BITE TEST CMD		0 BITE TEST CMD			
			1-15		1-15		1-15			

MDM FA1-FA4 OUTPUT CARD CHANNELIZATION

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REV.	CARD	CHAN	BIT	MDM FA 1	MDM FA 2	MDM FA 3	MDM FA 4	BIT	COMMENTS
00	(ADD)	00		RESERVED ("MOM CLEAR" LOGIC)	RESERVED ("MOM CLEAR" LOGIC)	RESERVED ("MOM CLEAR" LOGIC)	RESERVED ("MOM CLEAR" LOGIC)		
01		01		SRB TVC: LH ROCK ACTUATOR A CMO	SRB TVC: LH ROCK ACTUATOR B CMO	SRB TVC: RH ROCK ACTUATOR C CMO	SRB TVC: RH ROCK ACTUATOR D CMO		
02		02		RH TILT ACTUATOR A CMO	RH TILT ACTUATOR B CMO	RH TILT ACTUATOR C CMO	RH TILT ACTUATOR D CMO		
03		03		R YAW ACTUATOR A CMO	R YAW ACTUATOR B CMO	R YAW ACTUATOR C CMO	R YAW ACTUATOR D CMO		
04		04		R PITCH ACTUATOR A CMO	R PITCH ACTUATOR B CMO	R PITCH ACTUATOR C CMO	R PITCH ACTUATOR D CMO		
05		05		ASA #1: L INBD ELEVON ACTUATOR A CMO	ASA #2: L INBD ELEVON ACTUATOR B CMO	ASA #3: L INBD ELEVON ACTUATOR C CMO	ASA #4: L INBD ELEVON ACTUATOR D CMO		
06		06		L OTRD ELEVON ACTUATOR A CMO	L OTRD ELEVON ACTUATOR B CMO	L OTRD ELEVON ACTUATOR C CMO	L OTRD ELEVON ACTUATOR D CMO		
07		07		SPEED BRAKE ACTUATOR A CMO	SPEED BRAKE ACTUATOR B CMO	SPEED BRAKE ACTUATOR C CMO	SPEED BRAKE ACTUATOR D CMO		
08		08		RUDDER ACTUATOR A CMO	RUDDER ACTUATOR B CMO	RUDDER ACTUATOR C CMO	RUDDER ACTUATOR D CMO		
09		09		MPS TVC: L YAW ACTUATOR A CMO	MPS TVC: L YAW ACTUATOR B CMO	MPS TVC: L YAW ACTUATOR C CMO	MPS TVC: L YAW ACTUATOR D CMO		
10		10		LH TILT ACTUATOR A CMO	LH TILT ACTUATOR B CMO	LH TILT ACTUATOR C CMO	LH TILT ACTUATOR D CMO		
11		11		SPARE CHANNEL	SPARE CHANNEL	SPARE CHANNEL	SPARE CHANNEL		
12		12		SPARE CHANNEL	SPARE CHANNEL	SPARE CHANNEL	SPARE CHANNEL		
13		13		SPARE CHANNEL	SPARE CHANNEL	SPARE CHANNEL	SPARE CHANNEL		
14		14		SPARE CHANNEL	SPARE CHANNEL	SPARE CHANNEL	SPARE CHANNEL		
15		15		SPARE CHANNEL	SPARE CHANNEL	SPARE CHANNEL	SPARE CHANNEL		
04	(ADD)	00		SRB TVC: LH ROCK ACTUATOR A CMO	SRB TVC: LH ROCK ACTUATOR B CMO	SRB TVC: LH ROCK ACTUATOR C CMO	SRB TVC: LH ROCK ACTUATOR D CMO		
01		01		RH TILT ACTUATOR A CMO	RH TILT ACTUATOR B CMO	RH TILT ACTUATOR C CMO	RH TILT ACTUATOR D CMO		
02		02		R YAW ACTUATOR A CMO	R YAW ACTUATOR B CMO	R YAW ACTUATOR C CMO	R YAW ACTUATOR D CMO		
03		03		R PITCH ACTUATOR A CMO	R PITCH ACTUATOR B CMO	R PITCH ACTUATOR C CMO	R PITCH ACTUATOR D CMO		
04		04		ASA #1: L INBD ELEVON ACTUATOR A CMO	ASA #2: L INBD ELEVON ACTUATOR B CMO	ASA #3: L INBD ELEVON ACTUATOR C CMO	ASA #4: L INBD ELEVON ACTUATOR D CMO		
05		05		L OTRD ELEVON ACTUATOR A CMO	L OTRD ELEVON ACTUATOR B CMO	L OTRD ELEVON ACTUATOR C CMO	L OTRD ELEVON ACTUATOR D CMO		
06		06		SPEED BRAKE ACTUATOR A CMO	SPEED BRAKE ACTUATOR B CMO	SPEED BRAKE ACTUATOR C CMO	SPEED BRAKE ACTUATOR D CMO		
07		07		RUDDER ACTUATOR A CMO	RUDDER ACTUATOR B CMO	RUDDER ACTUATOR C CMO	RUDDER ACTUATOR D CMO		
08		08		MPS TVC: L PRI Y ACTR CMO ("ACTIVE")	MPS TVC: L SEC Y ACTR CMO ("STBY")	MPS TVC: L SEC Y ACTR CMO ("STBY")	MPS TVC: L SEC Y ACTR CMO ("ACTIVE")		
09		09		RGA #1: BITE ROLL TORQUE CMO	RGA #2: BITE ROLL TORQUE CMO	RGA #3: BITE ROLL TORQUE CMO	RGA #4: BITE ROLL TORQUE CMO		
10		10		BITE PITCH TORQUE CMO	BITE PITCH TORQUE CMO	BITE PITCH TORQUE CMO	BITE PITCH TORQUE CMO		
11		11		BITE YAW TORQUE CMO	BITE YAW TORQUE CMO	BITE YAW TORQUE CMO	BITE YAW TORQUE CMO		
12		12		SPARE CHANNEL	SPARE CHANNEL	SPARE CHANNEL	SPARE CHANNEL		
13		13		SPARE CHANNEL	SPARE CHANNEL	SPARE CHANNEL	SPARE CHANNEL		
14		14		SPARE CHANNEL	SPARE CHANNEL	SPARE CHANNEL	SPARE CHANNEL		
15		15		SPARE CHANNEL	SPARE CHANNEL	SPARE CHANNEL	SPARE CHANNEL		
02	(DEL)	00		RJDA 1B: L RCS JET L1A CMO A	RJDA 2B: L RCS JET L3A CMO A	RJDA 1A: L RCS JET L2L CMO A	RJDA 2A: L RCS JET L4L CMO A		
01		01		L RCS JET L1L CMO A	L RCS JET L3L CMO A	L RCS JET L2L CMO A	L RCS JET L4L CMO A		
02		02		R RCS JET L1R CMO A	R RCS JET L3R CMO A	R RCS JET L2R CMO A	R RCS JET L4R CMO A		
03		03		R RCS JET R1A CMO A	R RCS JET R3A CMO A	R RCS JET R2A CMO A	R RCS JET R4A CMO A		
04		04		R RCS JET R1B CMO A	R RCS JET R3B CMO A	R RCS JET R2B CMO A	R RCS JET R4B CMO A		
05		05		R RCS JET R1U CMO A	R RCS JET R3U CMO A	R RCS JET R2U CMO A	R RCS JET R4U CMO A		
06		06		R RCS JET L50 CMO A	R RCS JET R50 CMO A	R RCS JET R50 CMO A	R RCS JET R40 CMO A		
07		07		R RCS JET L50 CMO A	R RCS JET R50 CMO A	R RCS JET R50 CMO A	R RCS JET R40 CMO A		
08		08		MPS TVC: L CTR PITCH ACTUATOR A BYPASS	MPS TVC: CTR PITCH ACTUATOR B BYPASS	MPS TVC: CTR PITCH ACTUATOR C BYPASS	MPS TVC: CTR PITCH ACTUATOR D BYPASS		
09		09		L YAW ACTUATOR A BYPASS	L YAW ACTUATOR B BYPASS	L YAW ACTUATOR C BYPASS	L YAW ACTUATOR D BYPASS		
10		10		CTR PITCH ACTUATOR A RESET	CTR PITCH ACTUATOR B RESET	CTR PITCH ACTUATOR C RESET	CTR PITCH ACTUATOR D RESET		
11		11		L PITCH ACTUATOR A RESET	L PITCH ACTUATOR B RESET	L PITCH ACTUATOR C RESET	L PITCH ACTUATOR D RESET		
12		12		L YAW ACTUATOR A RESET	L YAW ACTUATOR B RESET	L YAW ACTUATOR C RESET	L YAW ACTUATOR D RESET		
13		13		RH ROCK ACTUATOR A BYPASS	RH ROCK ACTUATOR B BYPASS	RH ROCK ACTUATOR C BYPASS	RH ROCK ACTUATOR D BYPASS		
14		14		LH TILT ACTUATOR A BYPASS	LH TILT ACTUATOR B BYPASS	LH TILT ACTUATOR C BYPASS	LH TILT ACTUATOR D BYPASS		
15		15							

MDM FA1-FA4 OUTPUT CARD CHANNELIZATION

DATE: 12/04/81

REV.	CARD	CHAN	BIT	MDM FA 1	MDM FA 2	BIT	MDM FA 3	BIT	MDM FA 4	COMMENTS	
02	(DOL)	01	0	SRB TVC: RH ROCK ACTUATOR A RESET	SRB TVC: RH ROCK ACTUATOR B RESET	0	SRB TVC: RH ROCK ACTUATOR C RESET	0	SRB TVC: RH ROCK ACTUATOR D RESET		
			1	LH TILT ACTUATOR A RESET	LH TILT ACTUATOR B RESET	1	LH TILT ACTUATOR C RESET	1	LH TILT ACTUATOR D RESET		
			2	ASA #1: LH INBD ELEVON ACTUATOR BYPASS	ASA #2: LH INBD ELEVON ACTUATOR BYPASS	2	ASA #3: LH INBD ELEVON ACTUATOR BYPASS	2	ASA #4: LH INBD ELEVON ACTUATOR BYPASS		
			3	L OTBD ELEVON ACTUATOR BYPASS	L OTBD ELEVON ACTUATOR BYPASS	3	L OTBD ELEVON ACTUATOR BYPASS	3	L OTBD ELEVON ACTUATOR BYPASS		
			4	R INBD ELEVON ACTUATOR BYPASS	R INBD ELEVON ACTUATOR BYPASS	4	R INBD ELEVON ACTUATOR BYPASS	4	R INBD ELEVON ACTUATOR BYPASS		
			5	R OTBD ELEVON ACTUATOR BYPASS	R OTBD ELEVON ACTUATOR BYPASS	5	R OTBD ELEVON ACTUATOR BYPASS	5	R OTBD ELEVON ACTUATOR BYPASS		
			6	SPEED BRAKE ACTUATOR BYPASS	SPEED BRAKE ACTUATOR BYPASS	6	SPEED BRAKE ACTUATOR BYPASS	6	SPEED BRAKE ACTUATOR BYPASS		
			7	RUDDER ACTUATOR BYPASS	RUDDER ACTUATOR BYPASS	7	RUDDER ACTUATOR BYPASS	7	RUDDER ACTUATOR BYPASS		
			8	L INBD ELEVON ACTUATOR RESET	L INBD ELEVON ACTUATOR RESET	8	L INBD ELEVON ACTUATOR RESET	8	L INBD ELEVON ACTUATOR RESET		
			9	L OTBD ELEVON ACTUATOR RESET	L OTBD ELEVON ACTUATOR RESET	9	L OTBD ELEVON ACTUATOR RESET	9	L OTBD ELEVON ACTUATOR RESET		
			10	R INBD ELEVON ACTUATOR RESET	R INBD ELEVON ACTUATOR RESET	10	R INBD ELEVON ACTUATOR RESET	10	R INBD ELEVON ACTUATOR RESET		
			11	R OTBD ELEVON ACTUATOR RESET	R OTBD ELEVON ACTUATOR RESET	11	R OTBD ELEVON ACTUATOR RESET	11	R OTBD ELEVON ACTUATOR RESET		
			12	SPEED BRAKE ACTUATOR RESET	SPEED BRAKE ACTUATOR RESET	12	SPEED BRAKE ACTUATOR RESET	12	SPEED BRAKE ACTUATOR RESET		
			13	RUDDER ACTUATOR RESET	RUDDER ACTUATOR RESET	13	RUDDER ACTUATOR RESET	13	RUDDER ACTUATOR RESET		
			14	BODY FLAP ACTUATOR UP CHD	BODY FLAP ACTUATOR UP CHD	14	BODY FLAP ACTUATOR UP CHD	14	BODY FLAP ACTUATOR UP CHD		
			15	BODY FLAP ACTUATOR DOWN CHD	BODY FLAP ACTUATOR DOWN CHD	15	BODY FLAP ACTUATOR DOWN CHD	15	BODY FLAP ACTUATOR DOWN CHD		
02				SPARE CHANNEL					SPARE CHANNEL		
10	(DOL)	00	0	RJDA 1B: L RCS JET L1A CHD B	RJDA 2B: L RCS JET L1B CHD B	0	RJDA 1A: L RCS JET L2L CHD B	0	RJDA 2A: L RCS JET L4L CHD B		
			1	L RCS JET L1L CHD B	L RCS JET L1L CHD B	1	L RCS JET L2L CHD B	1	L RCS JET L4L CHD B		
			2	R RCS JET L1A CHD B	R RCS JET L1A CHD B	2	L RCS JET L2L CHD B	2	L RCS JET L4L CHD B		
			3	R RCS JET L1L CHD B	R RCS JET L1L CHD B	3	R RCS JET L2L CHD B	3	R RCS JET L4L CHD B		
			4	R RCS JET R1A CHD B	R RCS JET R1A CHD B	4	R RCS JET R2L CHD B	4	R RCS JET R4L CHD B		
			5	R RCS JET R1L CHD B	R RCS JET R1L CHD B	5	R RCS JET R2L CHD B	5	R RCS JET R4L CHD B		
			6	R RCS JET R1U CHD B	R RCS JET R1U CHD B	6	R RCS JET R2U CHD B	6	R RCS JET R4U CHD B		
			7	R RCS JET R1D CHD B	R RCS JET R1D CHD B	7	R RCS JET R2D CHD B	7	R RCS JET R4D CHD B		
			8	VERM JET L5L CHD B	VERM JET L5L CHD B	8	VERM JET R5L CHD B	8	VERM JET R5L CHD B		
			9	MPS TVC: CTR YAW ACTUATOR A BYPASS	MPS TVC: CTR YAW ACTUATOR B BYPASS	9	MPS TVC: CTR YAW ACTUATOR C BYPASS	9	MPS TVC: CTR YAW ACTUATOR D BYPASS		
			10	R PITCH ACTUATOR A BYPASS	R PITCH ACTUATOR B BYPASS	10	R PITCH ACTUATOR C BYPASS	10	R PITCH ACTUATOR D BYPASS		
			11	R YAW ACTUATOR A BYPASS	R YAW ACTUATOR B BYPASS	11	R YAW ACTUATOR C BYPASS	11	R YAW ACTUATOR D BYPASS		
			12	R PITCH ACTUATOR A RESET	R PITCH ACTUATOR B RESET	12	R PITCH ACTUATOR C RESET	12	R PITCH ACTUATOR D RESET		
			13	R YAW ACTUATOR A RESET	R YAW ACTUATOR B RESET	13	R YAW ACTUATOR C RESET	13	R YAW ACTUATOR D RESET		
			14	SRB TVC: RH TILT ACTUATOR A BYPASS	SRB TVC: RH TILT ACTUATOR B BYPASS	14	SRB TVC: RH TILT ACTUATOR C BYPASS	14	SRB TVC: RH TILT ACTUATOR D BYPASS		
			15	LH ROCK ACTUATOR A BYPASS	LH ROCK ACTUATOR B BYPASS	15	LH ROCK ACTUATOR C BYPASS	15	LH ROCK ACTUATOR D BYPASS		
01			0	SRB TVC: RH TILT ACTUATOR A RESET	SRB TVC: RH TILT ACTUATOR B RESET	0	SRB TVC: RH TILT ACTUATOR C RESET	0	SRB TVC: RH TILT ACTUATOR D RESET		
			1	LH ROCK ACTUATOR A RESET	LH ROCK ACTUATOR B RESET	1	LH ROCK ACTUATOR C RESET	1	LH ROCK ACTUATOR D RESET		
			2	ASA #1: BODY FLAP ACTUATOR ENABLE CHD	ASA #2: BODY FLAP ACTUATOR ENABLE CHD	2	ASA #3: BODY FLAP ACTUATOR ENABLE CHD	2	ASA #4: BODY FLAP ACTUATOR ENABLE CHD		
			3			3		3			
			4			4		4			
			5			5		5			
			6			6		6			
			7			7		7			
			8			8		8			
			9			9		9			
			10			10		10			
			11			11		11			
			12			12		12			
			13			13		13			
			14			14		14			
			15			15		15			
02				SPARE CHANNEL					SPARE CHANNEL		

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CARD	CHAN	BIT	MDM FA 1	MDM FA 2	MDM FA 3	MDM FA 4	BIT	COMMENTS
07 (001)	00	0	L RCS: MANS 3 ISOL VLV GPC CL A (OR)	L RCS: MANS 4 ISOL VLV GPC CL A (OR)	L RCS: MANS 4 ISOL VLV GPC CL A (OR)	L RCS: MANS 2 ISOL VLV GPC CL A (OR)	0	L RCS: MANS 2 ISOL VLV GPC CL A (OR)
		1	ET DOOR: FMD C/L LH MOTOR 2/LOCK A	ET DOOR: FMD C/L LH MOTOR 2/LOCK A	ET DOOR: FMD C/L LH MOTOR 2/LOCK A	ET DOOR: FMD C/L LH MOTOR 2/LOCK A	1	ET DOOR: FMD C/L LH MOTOR 2/LOCK A
		2	L LH DOOR MOTOR 1/LATCH A	L LH DOOR MOTOR 1/LATCH B	L LH DOOR MOTOR 1/LATCH A	L LH DOOR MOTOR 1/LATCH A	2	L LH DOOR MOTOR 1/LATCH A
		3	L LH DOOR MOTOR 1/CLOSE A	R LH DOOR MOTOR 2/CLOSE	L LH DOOR MOTOR 1/LATCH A	L LH DOOR MOTOR 1/LATCH A	3	L LH DOOR MOTOR 1/CLOSE A
		4	LH VENTS B/9: MOTOR 2/CLOSE A (CL/7A)	RH VENTS B/9: MOTOR 2/CLOSE A (CL/7A)	RH VENTS B/9: MOTOR 2/CLOSE A (CL/7A)	RH VENTS B/9: MOTOR 2/CLOSE A (CL/7A)	4	LH VENTS B/9: MOTOR 2/CLOSE A (CL/7A)
		5	MOTOR 1/PURGE A (PG/7A)	MOTOR 2/PURGE A (PG/2A)	MOTOR 1/PURGE A (PG/7A)	MOTOR 1/PURGE A (PG/7A)	5	MOTOR 2/PURGE A (PG/2A)
		6	C MPS: LOZ PREVALVE GPC CL B	C MPS: LOZ PREVALVE GPC CL C	C MPS: LOZ PREVALVE GPC CL A	C MPS: LOZ PREVALVE GPC CL A	6	C MPS: LOZ PREVALVE GPC CL B
		7	LH2 PREVALVE GPC CL B	LH2 PREVALVE GPC CL C	LH2 PREVALVE GPC CL A	LH2 PREVALVE GPC CL A	7	LH2 PREVALVE GPC CL B
		8	LH2 PREVALVE GPC CL B	LH2 PREVALVE GPC CL C	LH2 PREVALVE GPC CL A	LH2 PREVALVE GPC CL A	8	LH2 PREVALVE GPC CL B
		9	LH2 PREVALVE GPC CL B	LH2 PREVALVE GPC CL C	LH2 PREVALVE GPC CL A	LH2 PREVALVE GPC CL A	9	LH2 PREVALVE GPC CL B
		10	MPS: REPLACE LH2 TK PRESS XOOK CHO	MPS: REPLACE LH2 TK PRESS XOOK CHO	MPS: REPLACE LH2 TK PRESS XOOK CHO	MPS: REPLACE LH2 TK PRESS XOOK CHO	10	MPS: REPLACE LH2 TK PRESS XOOK CHO
		11	LH2 FEED-DISCONNECT VLV CL C	LH2 FEED-DISCONNECT VLV CL C	LH2 FEED-DISCONNECT VLV CL A	LH2 FEED-DISCONNECT VLV CL A	11	LH2 FEED-DISCONNECT VLV CL C
		12	LH2 FEED-DISCONNECT VLV CL C	LH2 FEED-DISCONNECT VLV CL C	LH2 FEED-DISCONNECT VLV CL A	LH2 FEED-DISCONNECT VLV CL A	12	LH2 FEED-DISCONNECT VLV CL C
		13	C MPS: MAINSTAGE A (THH PREVALVE CL)	C MPS: MAINSTAGE B (THH PREVALVE CL)	LH2 FEED-DISCONNECT VLV CL A	LH2 FEED-DISCONNECT VLV CL A	13	C MPS: MAINSTAGE A (THH PREVALVE CL)
		14	MPS: LH2 MANS PRESS VLV 2 GPC OP	MPS: LH2 MANS PRESS VLV 2 GPC OP	LH2 FEED-DISCONNECT VLV CL A	LH2 FEED-DISCONNECT VLV CL A	14	MPS: LH2 MANS PRESS VLV 2 GPC OP
15					15			
01	01	0	R OMS ENGINE: CTRL VLV 1 COIL 2 IGN	R OMS ENGINE: CTRL VLV 2 COIL 2 IGN	R OMS ENGINE: CTRL VLV 3 COIL 1 IGN	R OMS ENGINE: CTRL VLV 2 COIL 1 IGN	0	R OMS ENGINE: CTRL VLV 2 COIL 1 IGN
		1	L OMS: VAPOR ISOL VLV 1 GPC OP 2	L OMS: VAPOR ISOL VLV 2 GPC OP	L OMS: VAPOR ISOL VLV 1 GPC OP	L OMS: VAPOR ISOL VLV 2 GPC OP	1	L OMS: VAPOR ISOL VLV 1 GPC OP
		2	FU TK ISOL VLV A GPC CL 2	FU TK ISOL VLV A GPC CL 2	FU TK ISOL VLV A GPC CL 2	FU TK ISOL VLV A GPC CL 2	2	FU TK ISOL VLV A GPC CL 2
		3	FU TK ISOL VLV A GPC CL 2	FU TK ISOL VLV A GPC CL 2	FU TK ISOL VLV A GPC CL 2	FU TK ISOL VLV A GPC CL 2	3	FU TK ISOL VLV A GPC CL 2
		4	OX TK ISOL VLV A GPC CL 2	OX TK ISOL VLV A GPC CL 2	OX TK ISOL VLV A GPC CL 2	OX TK ISOL VLV A GPC CL 2	4	OX TK ISOL VLV A GPC CL 2
		5	OX TK ISOL VLV A GPC CL 2	OX TK ISOL VLV A GPC CL 2	OX TK ISOL VLV A GPC CL 2	OX TK ISOL VLV A GPC CL 2	5	OX TK ISOL VLV A GPC CL 2
		6	OX TK ISOL VLV A GPC CL 2	OX TK ISOL VLV A GPC CL 2	OX TK ISOL VLV A GPC CL 2	OX TK ISOL VLV A GPC CL 2	6	OX TK ISOL VLV A GPC CL 2
		7	FU FED VLV A GPC CL 2	FU FED VLV A GPC CL 2	FU FED VLV A GPC CL 2	FU FED VLV A GPC CL 2	7	FU FED VLV A GPC CL 2
		8	FU FED VLV A GPC CL 2	FU FED VLV A GPC CL 2	FU FED VLV A GPC CL 2	FU FED VLV A GPC CL 2	8	FU FED VLV A GPC CL 2
		9	FU FED VLV A GPC CL 2	FU FED VLV A GPC CL 2	FU FED VLV A GPC CL 2	FU FED VLV A GPC CL 2	9	FU FED VLV A GPC CL 2
		10	FU FED VLV A GPC CL 2	FU FED VLV A GPC CL 2	FU FED VLV A GPC CL 2	FU FED VLV A GPC CL 2	10	FU FED VLV A GPC CL 2
		11	OX FED VLV A GPC CL 2	OX FED VLV A GPC CL 2	OX FED VLV A GPC CL 2	OX FED VLV A GPC CL 2	11	OX FED VLV A GPC CL 2
		12	OX FED VLV A GPC CL 2	OX FED VLV A GPC CL 2	OX FED VLV A GPC CL 2	OX FED VLV A GPC CL 2	12	OX FED VLV A GPC CL 2
		13	OX FED VLV A GPC CL 2	OX FED VLV A GPC CL 2	OX FED VLV A GPC CL 2	OX FED VLV A GPC CL 2	13	OX FED VLV A GPC CL 2
		14	OX FED VLV A GPC CL 2	OX FED VLV A GPC CL 2	OX FED VLV A GPC CL 2	OX FED VLV A GPC CL 2	14	OX FED VLV A GPC CL 2
15					15			
02	02	0	L RCS: XFD VLV 3/4/5 GPC CL A	L RCS: XFD VLV 3/4/5 GPC CL B	L RCS: XFD VLV 3/4/5 GPC CL B	L RCS: XFD VLV 3/4/5 GPC CL A	0	L RCS: XFD VLV 3/4/5 GPC CL A
		1	XFD VLV 3/4/5 GPC CL A	XFD VLV 3/4/5 GPC CL B	XFD VLV 3/4/5 GPC CL B	XFD VLV 3/4/5 GPC CL A	1	XFD VLV 3/4/5 GPC CL A
		2	FU TK ISOL VLV 1/2 GPC CL B	FU TK ISOL VLV 3/4/5 GPC CL B	FU TK ISOL VLV 3/4/5 GPC CL B	FU TK ISOL VLV 3/4/5 GPC CL B	2	FU TK ISOL VLV 1/2 GPC CL B
		3	FU TK ISOL VLV 1/2 GPC CL B	FU TK ISOL VLV 3/4/5 GPC CL B	FU TK ISOL VLV 3/4/5 GPC CL B	FU TK ISOL VLV 3/4/5 GPC CL B	3	FU TK ISOL VLV 1/2 GPC CL B
		4	OX TK ISOL VLV 1/2 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	4	OX TK ISOL VLV 1/2 GPC CL B
		5	OX TK ISOL VLV 1/2 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	5	OX TK ISOL VLV 1/2 GPC CL B
		6	OX TK ISOL VLV 1/2 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	6	OX TK ISOL VLV 1/2 GPC CL B
		7	OX TK ISOL VLV 1/2 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	7	OX TK ISOL VLV 1/2 GPC CL B
		8	OX TK ISOL VLV 1/2 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	8	OX TK ISOL VLV 1/2 GPC CL B
		9	OX TK ISOL VLV 1/2 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	9	OX TK ISOL VLV 1/2 GPC CL B
		10	OX TK ISOL VLV 1/2 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	10	OX TK ISOL VLV 1/2 GPC CL B
		11	OX TK ISOL VLV 1/2 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	11	OX TK ISOL VLV 1/2 GPC CL B
		12	OX TK ISOL VLV 1/2 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	12	OX TK ISOL VLV 1/2 GPC CL B
		13	OX TK ISOL VLV 1/2 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	13	OX TK ISOL VLV 1/2 GPC CL B
		14	OX TK ISOL VLV 1/2 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	OX TK ISOL VLV 3/4/5 GPC CL B	14	OX TK ISOL VLV 1/2 GPC CL B
15					15			

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REV.	CHAM	BIT	MDM FA 1	MDM FA 2	BIT	MDM FA 3	BIT	MDM FA 4	COMMENTS
12 (DWH)	00	0	MPS: LOZ POGO RECIRC VLV 1 CL A	MPS: LOZ POGO RECIRC VLV 2 CL A	0	MPS: LOZ POGO RECIRC VLV 1 CL B	0	MPS: LOZ POGO RECIRC VLV 2 CL B	
		1	SIGNAL CONDOR PWR 1 ON CMO	LOZ OVRBD BLEED VLV GPC CL C	1	LOZ OVRBD BLEED VLV GPC CL B	1	LOZ OVRBD BLEED VLV GPC CL B	
		2	LH2 RTLS IMBD DAMP VLV OP C	LH2 RTLS IMBD DAMP VLV GPC OP	2	LH2 RTLS IMBD DAMP VLV OP A	2	SIGNAL CONDOR PWR 3 ON CMO	
		3	LH2 RTLS OTBD DRAIN VLV OP C	LH2 OTBD FILL/DRAIN VLV GPC CL	3	LH2 RTLS OTBD DAMP VLV OP A	3	LH2 RTLS IMBD DAMP VLV OP B	
		4	LOZ RTLS OTBD DRAIN VLV OP C	LH2 OTBD FILL/DRAIN VLV GPC CL	4	LH2 RTLS OTBD DAMP VLV OP A	4	LH2 RTLS OTBD DAMP VLV OP B	
		5	LH2 RTLS IMBD DRAIN VLV OP C	MPS: LOZ IMBD FILL/DRAIN VLV GPC CL	5	MPS: LOZ IMBD DAMP VLV OP A	5	MPS: HE SUPPLY BLOWDOWN VLV 2 OP	
		6	LH2 RTLS IMBD DRAIN VLV OP C	R MPS: LOZ PREVALVE GPC OP A	6	HE SUPPLY BLOWDOWN VLV 1 OP A	6	R MPS: LOZ PREVALVE GPC OP B	
		7	R MPS: LOZ PREVALVE GPC OP C	LH2 PREVALVE GPC CL A	7	R MPS: LOZ PREVALVE GPC OP A	7	R MPS: LOZ PREVALVE GPC CL B	
		8	LH2 PREVALVE GPC OP C	LH2 PREVALVE GPC CL A	8	LH2 PREVALVE GPC OP A	8	LH2 PREVALVE GPC CL B	
		9	LH2 PREVALVE GPC OP C	LH2 PREVALVE GPC CL A	9	LH2 PREVALVE GPC OP A	9	LH2 PREVALVE GPC CL B	
		10	LH2 PREVALVE GPC CL C	LH2 PREVALVE GPC CL A	10	LH2 PREVALVE GPC CL A	10	REPLACE LOZ TK PRESS ZICOR CMO	
		11	LH2 PREVALVE GPC CL C	LH2 PREVALVE GPC CL A	11	LH2 PREVALVE GPC CL A	11	REPLACE LOZ TK PRESS ZICOR CMO	
		12	MPS: HE SUPPLY BLOWDOWN VLV 1 OP C	MPS: LOZ RTLS MANF REPRESS VLV 2 OP C	12	MPS: LOZ FOLM RELIEF ISOL VLV CL C	12	MPS: LOZ RTLS MANF REPRESS VLV 1 OP C	
		13	MPS: HE SUPPLY BLOWDOWN VLV 1 OP C	MPS: LOZ RTLS MANF REPRESS VLV 2 OP C	13	LH2 RTLS MANF REPRESS VLV 2 OP C	13	MPS: LOZ RTLS MANF REPRESS VLV 1 OP C	
		14	R MPS: MAINSTAGE B (1MM PREVALVE CL)	L MPS: PNEU HE CROSSOVER VLV GPC OP	14	LH2 RTLS MANF REPRESS VLV 2 OP C	14	R MPS: MAINSTAGE A (1MM PREVALVE CL)	
		15	R MPS: MAINSTAGE B (1MM PREVALVE CL)	L MPS: PNEU HE CROSSOVER VLV GPC OP	15	LH2 RTLS MANF REPRESS VLV 2 OP C	15	R MPS: MAINSTAGE A (1MM PREVALVE CL)	
01		0			0		0		
		1			1		1		
		2			2		2		
		3	L OMS ENGINE: PURGE VLV 1 OP	L OMS ENGINE: PURGE VLV 2 OP	3		3	R OMS ENGINE: PURGE VLV 2 OP	
		4			4		4		
		5			5		5		
		6			6		6		
		7			7		7		
		8			8		8		
		9	C MPS: HE SUPPLY ISOL VLV A GPC OP	C MPS: HE SUPPLY ISOL VLV B GPC OP A	9	C MPS: HE SUPPLY ISOL VLV B GPC OP B	9	MPS: PNEU HE SUPPLY ISOL VLV 2 GPC OP	
		10	L MPS: HE SUPPLY ISOL VLV B GPC OP B	L MPS: HE SUPPLY ISOL VLV A GPC OP	10	L MPS: HE SUPPLY ISOL VLV B GPC OP B	10	L MPS: HE SUPPLY ISOL VLV B GPC OP A	
		11	R MPS: HE SUPPLY ISOL VLV B GPC OP A	R MPS: HE SUPPLY ISOL VLV B GPC OP B	11	R MPS: HE SUPPLY ISOL VLV A GPC OP	11	R MPS: HE SUPPLY ISOL VLV B GPC OP A	
		12	C MPS: HE INTCONM INLET VLV GPC OP A	L MPS: HE INTCONM INLET VLV GPC OP A	12	R MPS: HE SUPPLY ISOL VLV A GPC OP	12	L MPS: HE SUPPLY ISOL VLV B GPC OP A	
		13	R MPS: HE INTCONM INLET VLV GPC OP A	L MPS: HE INTCONM INLET VLV GPC OP A	13	L MPS: HE INTCONM INLET VLV GPC OP A	13	R MPS: HE INTCONM INLET VLV GPC OP A	
		14	R MPS: HE INTCONM INLET VLV GPC OP B	C MPS: HE INTCONM INLET VLV GPC OP B	14	L MPS: HE INTCONM INLET VLV GPC OP B	14	R MPS: HE INTCONM INLET VLV GPC OP	
		15	MPS: PNEU HE SUPPLY ISOL VLV 1 GPC OP	C MPS: HE INTCONM INLET VLV GPC OP B	15	L MPS: HE INTCONM INLET VLV GPC OP B	15	R MPS: HE INTCONM INLET VLV GPC OP	
02		0			0		0		
		1	L OMS ENGINE: PURGE VLV 1 OP	L OMS ENGINE: PURGE VLV 2 OP	1		1		
		2			2		2		
		3			3		3		
		4			4		4		
		5			5		5		
		6			6		6		
		7			7		7		
		8			8		8		
		9			9		9		
		10			10		10		
		11			11		11		
		12			12		12		
		13			13		13		
		14			14		14		
		15			15		15		

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COMMENTS

MDM FA 1

MDM FA 2

MDM FA 3

MDM FA 4

BIT

BIT

BIT

15 (00H)	00	01	02
0	ET DOOR: FMD C/L LCH MOTOR 2/STON B	0	ET DOOR: FMD C/L LCH MOTOR 2/STON B
1	R RCS: MAMF 4 ISOL VLV GPC CL A (OR)	1	R RCS: MAMF 4 ISOL VLV GPC CL A (OR)
2	ET DOOR: R UMB DOOR MOTOR 2/LATCH B	2	ET DOOR: R UMB DOOR MOTOR 2/LATCH B
3	LH VENTS B/9: MOTOR 2/CLOSE B (CL/28)	3	LH VENTS B/9: MOTOR 2/CLOSE B (CL/28)
4	MOTOR 1/OPEN B (OP/18)	4	MOTOR 1/OPEN B (OP/18)
5	MOTOR 2/PURGE B (PG/28)	5	MOTOR 2/PURGE B (PG/28)
6	MPS: LOZ FDM RELIEF ISOL VLV CL A	6	MPS: LOZ FDM RELIEF ISOL VLV CL A
7	L MPS: LOZ PREVALVE GPC OP B	7	L MPS: LOZ PREVALVE GPC OP B
8	LH2 PREVALVE GPC CL A	8	LH2 PREVALVE GPC CL A
9	LH2 PREVALVE GPC CL A	9	LH2 PREVALVE GPC CL A
10	MPS: LOZ IMBD FILL/DRAIN VLV GPC CL	10	MPS: LOZ IMBD FILL/DRAIN VLV GPC CL
11	LH2 PREVALVE GPC CL A	11	LH2 PREVALVE GPC CL A
12	LOZ FEED-DISCONNECT VLV OP C	12	LOZ FEED-DISCONNECT VLV OP C
13	L MPS: MAINSTAGE B (JHM PREVALVE CL)	13	L MPS: MAINSTAGE B (JHM PREVALVE CL)
14	MPS: LOZ RITLS MAMF REPRESS VLV 2 OP B	14	MPS: LOZ RITLS MAMF REPRESS VLV 2 OP B
15		15	
01	0	0	0
1	L OMS ENGINE: CNTL VLV 1 COIL 2 IGM	1	L OMS ENGINE: CNTL VLV 2 COIL 1 IGM
2	L OMS: HE PRESS ISOL VLV A GPC OP	2	R OMS: HE PRESS ISOL VLV B GPC OP
3	L OMS: TANK ISOL VLV B GPC OP 1	3	FU TK ISOL VLV B GPC OP 2
4	L OMS: TANK ISOL VLV B GPC OP 1	4	FU TK ISOL VLV B GPC CL 2
5	ET/ORBITER SEP CARRIERS HEATER-ON CMD	5	DE TR ISOL VLV B GPC OP 2
6		6	DE TR ISOL VLV B GPC CL 2
7		7	FU XFD VLV B GPC OP 2
8		8	FU XFD VLV B GPC CL 2
9		9	FU XFD VLV B GPC CL 2
10		10	FU XFD VLV B GPC CL 2
11	L OMS: XFD VLV B GPC OP 1	11	L OMS: XFD VLV B GPC OP 2
12	XFD VLV B GPC CL 1	12	OX XFD VLV B GPC CL 2
13	R OMS: XFD VLV B GPC OP 1	13	OX XFD VLV B GPC OP 2
14	XFD VLV B GPC CL 1	14	OX XFD VLV B GPC CL 2
15		15	
02	0	0	0
1	R RCS: OX XFD VLV 3/4/5 GPC CL B	1	R RCS: XFD VLV 3/4/5 GPC CL A
2	OX XFD VLV 3/4/5 GPC OP B	2	XFD VLV 3/4/5 GPC CL A
3	FU TK ISOL VLV 3/4/5 GPC CL B	3	FU TK ISOL VLV 3/4/5 GPC CL B
4	TANK ISOL VLV 3/4/5 GPC OP A	4	FU TK ISOL VLV 3/4/5 A GPC CL
5	TANK ISOL VLV 3/4/5 GPC CL A	5	OX TK ISOL VLV 3/4/5 A GPC CL
6	MAMF 1 ISOL VLV GPC OP	6	OX TK ISOL VLV 3/4/5 A GPC OP
7	ET DOOR: FMD C/L LCH MOTOR 2/LOCK B	7	MAMF 2 ISOL VLV GPC OP
8	L RCS: MAMF 3 ISOL VLV GPC CL B (OR)	8	ET DOOR: FMD C/L LCH MOTOR 2/LOCK B
9	R RCS: HE PRESS VLV B GPC OP	9	L RCS: MAMF 1 ISOL VLV GPC CL B (OR)
10	MAMF 3 ISOL VLV GPC CL	10	HE PRESS VLV B GPC OP
11	ET DOOR: CLOSE/LATCH RELAY DRVR ARM 1	11	MAMF 5 ISOL VLV GPC OP
12		12	ET DOOR: CLOSE/LATCH RELAY DRVR ARM 2
13		13	
14		14	
15		15	

MDM PL 1 & PL 2
OUTPUT CARD CHANNELIZATION

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CARD	CHAN	BIT	MDM PL 1	MDM PL 2	CARD	CHAN	BIT	MDM PL 1	MDM PL 2	BIT	SPARE CHANNEL
00	00	0	P/L RCDM: PRI CHO BIT 1		10	00	0	OPS RCDM #1: PRI CHO BIT 1		0	OPS RCDM #2: PRI CHO BIT 1
		1	PRI CHO BIT 2				1	PRI CHO BIT 2		1	PRI CHO BIT 2
		2	PRI CHO BIT 3				2	PRI CHO BIT 3		2	PRI CHO BIT 3
		3	PRI CHO BIT 4				3	PRI CHO BIT 4		3	PRI CHO BIT 4
		4	PRI CHO BIT 5				4	PRI CHO BIT 5		4	PRI CHO BIT 5
		5	PRI CHO BIT 6				5	PRI CHO BIT 6		5	PRI CHO BIT 6
		6	PRI CHO BIT 7				6	PRI CHO BIT 7		6	PRI CHO BIT 7
		7	PRI CHO BIT 8				7	PRI CHO BIT 8		7	PRI CHO BIT 8
		8	PRI CHO BIT 9				8	PRI CHO BIT 9		8	PRI CHO BIT 9
		9	PRI CHO BIT 10				9	PRI CHO BIT 10		9	PRI CHO BIT 10
		10	PRI CHO BIT 11				10	PRI CHO BIT 11		10	PRI CHO BIT 11
		11	PRI CHO BIT 12				11	PRI CHO BIT 12		11	PRI CHO BIT 12
		12	PRI CHO BIT 13				12	PRI CHO BIT 13		12	PRI CHO BIT 13
		13	PRI CHO BIT 14				13	PRI CHO BIT 14		13	PRI CHO BIT 14
		14	PRI CHO BIT 15				14	PRI CHO BIT 15		14	PRI CHO BIT 15
		15	PRI CHO BIT 16				15	PRI CHO BIT 16		15	PRI CHO BIT 16
			SPARE CHANNEL					SPARE CHANNEL			SPARE CHANNEL
			SPARE CHANNEL					SPARE CHANNEL			SPARE CHANNEL
01	01										OPS RCDM CNTL: SEC CHO AUTO SEQ 1
											SEC CHO AUTO SEQ 2
											CIM MATRIX: "PAYLOAD WARNING"
02	02										

MDM PL1 & PL2 OUTPUT CARD CHANNELIZATION

REV.

CARD	CHAN	BIT	MDM PL 1	MDM PL 2	MDM PL 1	MDM PL 2	BIT	MDM PL 1	MDM PL 2
02	(DOH)	00	0	14 (DOH)	00	0	0	L PBD: DOOR DRIVE MOTOR 2/OPEN	L PBD: DOOR DRIVE MOTOR 1/OPEN
			1			1	1	DOOR DRIVE MOTOR 2/CLOSE	DOOR DRIVE MOTOR 1/CLOSE
			2			2	2	FWD BID LCH MOTOR 2/RELEASE	FWD BID LCH MOTOR 1/RELEASE
			3			3	3	AFT BID LCH MOTOR 2/LATCH	AFT BID LCH MOTOR 1/LATCH
			4			4	4	FWD BID LCH MOTOR 1/RELEASE	FWD BID LCH MOTOR 2/RELEASE
			5			5	5	AFT BID LCH MOTOR 1/LATCH	AFT BID LCH MOTOR 2/LATCH
			6			6	6	PBD ENABLE CHD 1A (ACT ARM 1-MTRS)	PBD ENABLE CHD 2B (ACT ARM 2-MTRS)
			7			7	7	PBD ENABLE CHD 3A (ACT ARM 2-MTRS)	PBD ENABLE CHD 4B (ACT ARM 1-MTRS)
			8			8	8	PBD ENABLE CHD 4A (ACT ARM 1-MTRS)	PBD ENABLE CHD 5B (ACT ARM 2-MTRS)
			9			9	9	APU/HTD: P11 A CTRLS GPC - ON	APU/HTD: HVD SYS 1 CIRC PUMP ON SEL B
			10			10	10	FLASH EVAP: P11 A CTRLS GPC - ON	HVD SYS 2 CIRC PUMP ON SEL C
			11			11	11	M3 BLB: P11 A CTRLS GPC - ON	HVD SYS 3 CIRC PUMP ON SEL A
			12			12	12	CMX MATRIX: "BACKUP C/M ALARM" (OR)	HVD SYS 1 CIRC PUMP ON SEL C
			13			13	13	SM ALERT: TONE B CHD 2 (OR)	FREON LOOP #2: PUMP B GPC - ON
			14			14	14	SM ALERT: TONE B CHD 2 (OR)	
			15			15	15	F6 LIGHT A: "ABORT" ADVISORY	
			01		01	0	0	S-BAND FM: HENT ANT LOWER SEL 2	FUEL CELL #2: PURGE VALVES OPEN CHD A
			1			1	1	S-BAND FM: HENT ANT UPPER SEL 2	PURGE VALVES OPEN CHD B
			2			2	2	S-BAND FM: QUAD ANT UPPER LEFT SEL 1	
			3			3	3	S-BAND FM: QUAD ANT UPPER RIGHT SEL 1	
			4			4	4	QUAD ANT LOWER LEFT SEL 2	
			5			5	5	QUAD ANT LOWER RIGHT SEL 2	
			6			6	6	QUAD ANT FWD RIGHT SEL 2	
			7			7	7	QUAD ANT AFT RIGHT SEL 2	
			8			8	8		
			9			9	9		
			10			10	10		
			11			11	11		
			12			12	12		
			13			13	13		
			14			14	14		
			15			15	15		
			02		02	0	0	SPARE CHANNEL	PBD ENABLE CHD 6B (ACT ARM 12-MTRS)
			1			1	1		
			2			2	2	MDS WB/ACT PCH ON	
			3			3	3	PCH ON	
			4			4	4	RDR PLBK REV RELWIND ON	
			5			5	5	FWD ON	
			6			6	6	PBD ENABLE CHD 1B (ACT ARM 1-MTRS)	
			7			7	7		
			8			8	8		
			9			9	9		
			10			10	10		
			11			11	11		
			12			12	12		
			13			13	13		
			14			14	14		
			15			15	15		

MDM PL 1	MDM PL 2	MDM PL 1	MDM PL 2
0	0	0	0
1	1	1	1
2	2	2	2
3	3	3	3
4	4	4	4
5	5	5	5
6	6	6	6
7	7	7	7
8	8	8	8
9	9	9	9
10	10	10	10
11	11	11	11
12	12	12	12
13	13	13	13
14	14	14	14
15	15	15	15

MDM PL 1	MDM PL 2	MDM PL 1	MDM PL 2
0	0	0	0
1	1	1	1
2	2	2	2
3	3	3	3
4	4	4	4
5	5	5	5
6	6	6	6
7	7	7	7
8	8	8	8
9	9	9	9
10	10	10	10
11	11	11	11
12	12	12	12
13	13	13	13
14	14	14	14
15	15	15	15

MDM PL 1	MDM PL 2	MDM PL 1	MDM PL 2
0	0	0	0
1	1	1	1
2	2	2	2
3	3	3	3
4	4	4	4
5	5	5	5
6	6	6	6
7	7	7	7
8	8	8	8
9	9	9	9
10	10	10	10
11	11	11	11
12	12	12	12
13	13	13	13
14	14	14	14
15	15	15	15

MDM/TAB: PL/R/068

DATE: 07/20/82

MDM PL 1 & PL 2
OUTPUT CARD CHANNELIZATION

REV.

CARD	CHAN	BIT	MDM PL 1	MDM PL 2	CARD	CHAN	BIT	MDM PL 1	MDM PL 2
07 (DCH)	00	0	R13 TB FLAG: PL BAY DOOR "UP" CHO 1	R13 TB FLAG: PL BAY DOOR "UP" CHO 2	12 (ADD)	00			
		1	PL BAY DOOR "CL" CHO 1	PL BAY DOOR "CL" CHO 2		01			
		2	PL BAY DOOR "L" CHO 1	PL BAY DOOR "L" CHO 2		02			
		3	PL BAY DOOR "R" CHO 1	PL BAY DOOR "R" CHO 2		03			
		4	C/L LCH 1-4 MOTOR 1/LATCH	C/L LCH 1-4 MOTOR 2/LATCH		04			
		5	C/L LCH 5-8 MOTOR 1/RELEASE	C/L LCH 5-8 MOTOR 2/RELEASE		05			
		6	C/L LCH 9-12 MOTOR 1/LATCH	C/L LCH 9-12 MOTOR 2/LATCH		06			
		7	C/L LCH 13-16 MOTOR 1/RELEASE	C/L LCH 13-16 MOTOR 2/RELEASE		07			
		8	C/L LCH 17-20 MOTOR 1/LATCH	C/L LCH 17-20 MOTOR 2/LATCH		08			
		9	C/L LCH 21-24 MOTOR 1/RELEASE	C/L LCH 21-24 MOTOR 2/RELEASE		09			
		10	H2O LOOP #1: PUMP A CNTL GPC ENABLE	H2O LOOP #1: PUMP A CNTL GPC - ON CHO C		10			
		11	H2O LOOP #2: PUMP B CNTL GPC ENABLE	H2O LOOP #2: PUMP B CNTL GPC - ON CHO C		11			
		12	ACTIP: PUMP B-LW CHO (AERIO COEFF 10 PHG)	ACTIP: PUMP B-LW CHO (AERIO COEFF 10 PHG)		12			
		13	ACTIP: CAL MODE CHO	ACTIP: CAL MODE CHO		13			
		14				14			
		15				15			
01	01	0	FUEL CELL #1: PURGE VALVES OPEN CHO A	FUEL CELL #1: PURGE VALVES OPEN CHO A		00			
		1	SUMS: INSTRUMENTATION ON	SUMS: INSTRUMENTATION ON		01			
		2	TOR PUMP ON	TOR PUMP ON		02			
		3	MAINTENANCE PUMP ON	MAINTENANCE PUMP ON		03			
		4	FIM MODE AUTO CAL	FIM MODE AUTO CAL		04			
		5	MAOS CHO TRK SEQ 1 ON (RCOR PASS 3)	MAOS CHO TRK SEQ 1 ON (RCOR PASS 3)		05			
		6				06			
		7				07			
		8				08			
		9				09			
		10				10			
		11				11			
		12				12			
		13				13			
		14				14			
		15				15			
02	02	0	FUEL CELL #1: PURGE VALVES OPEN CHO B	FUEL CELL #1: PURGE VALVES OPEN CHO B		00			
		1	SUMS: INSTRUMENTATION ON	SUMS: INSTRUMENTATION ON		01			
		2	TOR PUMP ON	TOR PUMP ON		02			
		3	MAINTENANCE PUMP ON	MAINTENANCE PUMP ON		03			
		4	FIM MODE AUTO CAL	FIM MODE AUTO CAL		04			
		5	MAOS CHO TRK SEQ 1 ON (RCOR PASS 3)	MAOS CHO TRK SEQ 1 ON (RCOR PASS 3)		05			
		6				06			
		7				07			
		8				08			
		9				09			
		10				10			
		11				11			
		12				12			
		13				13			
		14				14			
		15				15			
		0	FUEL CELL #2: PURGE VALVES OPEN CHO A	FUEL CELL #2: PURGE VALVES OPEN CHO A		00			
		1	SUMS: INSTRUMENTATION ON	SUMS: INSTRUMENTATION ON		01			
		2	TOR PUMP ON	TOR PUMP ON		02			
		3	MAINTENANCE PUMP ON	MAINTENANCE PUMP ON		03			
		4	FIM MODE AUTO CAL	FIM MODE AUTO CAL		04			
		5	MAOS CHO TRK SEQ 1 ON (RCOR PASS 3)	MAOS CHO TRK SEQ 1 ON (RCOR PASS 3)		05			
		6				06			
		7				07			
		8				08			
		9				09			
		10				10			
		11				11			
		12				12			
		13				13			
		14				14			
		15				15			
		0	FUEL CELL #3: PURGE VALVES OPEN CHO B	FUEL CELL #3: PURGE VALVES OPEN CHO B		00			
		1	SUMS: INSTRUMENTATION ON	SUMS: INSTRUMENTATION ON		01			
		2	TOR PUMP ON	TOR PUMP ON		02			
		3	MAINTENANCE PUMP ON	MAINTENANCE PUMP ON		03			
		4	FIM MODE AUTO CAL	FIM MODE AUTO CAL		04			
		5	MAOS CHO TRK SEQ 1 ON (RCOR PASS 3)	MAOS CHO TRK SEQ 1 ON (RCOR PASS 3)		05			
		6				06			
		7				07			
		8				08			
		9				09			
		10				10			
		11				11			
		12				12			
		13				13			
		14				14			
		15				15			
		0	DECODER A SELECT	DECODER A SELECT		00			
		1	UPLINK CHO BIT A0	UPLINK CHO BIT A0		01			
		2	UPLINK CHO BIT A1	UPLINK CHO BIT A1		02			
		3	UPLINK CHO BIT A2	UPLINK CHO BIT A2		03			
		4	UPLINK CHO BIT A3	UPLINK CHO BIT A3		04			
		5	UPLINK CHO BIT A4	UPLINK CHO BIT A4		05			
		6	UPLINK CHO BIT A5	UPLINK CHO BIT A5		06			
		7	UPLINK CHO BIT A6	UPLINK CHO BIT A6		07			
		8	UPLINK CHO BIT A7	UPLINK CHO BIT A7		08			
		9	UPLINK CHO BIT A8	UPLINK CHO BIT A8		09			
		10	UPLINK CHO BIT A9	UPLINK CHO BIT A9		10			
		11	UPLINK CHO BIT B0	UPLINK CHO BIT B0		11			
		12	UPLINK CHO BIT B1	UPLINK CHO BIT B1		12			
		13	UPLINK CHO BIT B2	UPLINK CHO BIT B2		13			
		14	UPLINK CHO BIT B3	UPLINK CHO BIT B3		14			
		15	UPLINK CHO BIT B4	UPLINK CHO BIT B4		15			
		0	DECODER B SELECT	DECODER B SELECT		00			
		1	UPLINK CHO BIT B5	UPLINK CHO BIT B5		01			
		2	UPLINK CHO BIT B6	UPLINK CHO BIT B6		02			
		3	UPLINK CHO BIT B7	UPLINK CHO BIT B7		03			
		4	UPLINK CHO BIT B8	UPLINK CHO BIT B8		04			
		5	UPLINK CHO BIT B9	UPLINK CHO BIT B9		05			
		6	UPLINK CHO BIT C0	UPLINK CHO BIT C0		06			
		7	UPLINK CHO BIT C1	UPLINK CHO BIT C1		07			
		8	UPLINK CHO BIT C2	UPLINK CHO BIT C2		08			
		9	UPLINK CHO BIT C3	UPLINK CHO BIT C3		09			
		10	UPLINK CHO BIT C4	UPLINK CHO BIT C4		10			
		11	UPLINK CHO BIT C5	UPLINK CHO BIT C5		11			
		12	UPLINK CHO BIT C6	UPLINK CHO BIT C6		12			
		13	UPLINK CHO BIT C7	UPLINK CHO BIT C7		13			
		14	UPLINK CHO BIT C8	UPLINK CHO BIT C8		14			
		15	UPLINK CHO BIT C9	UPLINK CHO BIT C9		15			

F8 TAPE MTR "APU": APU #1 FUEL QTY
 APU #2 FUEL QTY
 APU #3 FUEL QTY
 HYD #1 H2O BLR QTY
 HYD #2 H2O BLR QTY
 HYD #3 H2O BLR QTY

SPARE CHANNEL
 SPARE CHANNEL
 SPARE CHANNEL
 SPARE CHANNEL
 SPARE CHANNEL
 SPARE CHANNEL
 SPARE CHANNEL
 SPARE CHANNEL
 SPARE CHANNEL

CARD NOT USED

APPENDIX B
OI PCM DOWNLINK FORMATS

TABLE B-1 DOWNLINK FORMATS

FORMAT	FLIGHT			DATA RATE	USAGES AND GPC TOGGLE BUFFER ACCESSED
	5	6	7		
102	X	X	X	LOW	ASCENT AND ABORT-TOGGLE BUFFERS ONE AND FIVE
103	X	X	X	LOW	ON-ORBIT-TOGGLE BUFFERS ONE AND TWO
104	X	X	X	LOW	ENTRY C/O-TOGGLE BUFFERS ONE AND TWO
105	X	X	X	LOW	ENTRY-TOGGLE BUFFERS ONE AND FIVE
106	X	X	X	LOW	GPC/MASS MEMORY UTILITY AND CHECKOUT FORMAT- TOGGLE BUFFERS ONE, TWO, AND FOUR
107	X			LOW	ON-ORBIT PAYLOAD SUPPORT FORMATS - EACH FORMAT ACCOMMODATES THREE 1.6 KBPS PDI WINDOWS, BUT A DIFFERENT COMPLEMENT OF PDI DECOM/TOGGLE BUFFERS- TOGGLE BUFFERS ONE AND TWO
108	X			LOW	
109	X			LOW	
110	X			LOW	
111		X		LOW	ON-ORBIT PAYLOAD SUPPORT-TWO 1.6 KBPS PAYLOAD WINDOWS-TOGGLE BUFFERS ONE AND TWO
114			X	LOW	ON-ORBIT PAYLOAD SUPPORT-TWO 1.6 KBPS PAYLOAD WINDOWS-TOGGLE BUFFERS ONE AND TWO
115			X	LOW	
116			X	LOW	ON-ORBIT FORMAT-TOGGLE BUFFERS ONE AND TWO
129	X	X	X	HIGH	FIXED FORMAT FOR PRIMARLY PRELAUNCH & ASCENT SUPPORT-TOGGLE BUFFERS ONE AND FIVE
140	X			HIGH	DFI PCM
141			X	LOW	MADS 32 KBPS RECORDED PCM FORMAT
142			X	HIGH	MADS 64 KBPS RECORDED PCM FORMAT
145	X	X	X	HIGH	LEFT SRB
146	X	X	X	HIGH	RIGHT SRB
150	X		X	HIGH	ET DFI
160	X	X	X	HIGH	PRELAUNCH FORMAT-TOGGLE BUFFERS ONE AND FOUR
161	X	X	X	HIGH	ON-ORBIT SUPPORT-TOGGLE BUFFERS ONE AND TWO

TABLE B-1 DOWNLINK FORMATS (Continued)

FORMAT	FLIGHT			DATA RATE	USAGES AND GPC TOGGLE BUFFER ACCESSED
	5	6	7		
162	X	X	X	HIGH	FCS C/O SUPPORT-TOGGLE BUFFERS ONE AND TWO
163	X	X	X	HIGH	GENERAL SYS AND GPC/MM DATA SUPPORT-TOGGLE BUFFERS ONE, TWO, AND FOUR
164	X	X	X	HIGH	ENTRY SUPPORT-TOGGLE BUFFERS ONE AND FIVE
165	X			HIGH	ON-ORBIT PAYLOAD SUPPORT-THREE 1.6 KBPS
168	X			HIGH	PDI WINDOWS-TOGGLE BUFFERS ONE AND TWO
169		X		HIGH	ASCENT PAYLOAD SUPPORT-ONE 1.6 KBPS PDI
173		X		HIGH	WINDOW-TOGGLE BUFFER ONE AND TWO
171	X	X	X	HIGH	KSC PRELAUNCH C/O FORMAT
172	X	X	X	HIGH	KSC C/O FORMAT-TOGGLE BUFFERS ONE AND TWO
174		X		HIGH	ORBIT PAYLOAD SUPPORT-TWO PDI WINDOWS
175		X		HIGH	(1.6 KBPS AND 17.6 KBPS)-TOGGLE BUFFERS ONE AND TWO
176		X		HIGH	KSC CHECKOUT FORMAT-TWO PDI WINDOWS (1.6 KBPS AND 17.6 KBPS)-TOGGLE BUFFERS ONE AND TWO
178			X	HIGH	ON-ORBIT PAYLOAD SUPPORT-TWO PDI WINDOWS
179			X	HIGH	(1.6 KBPS AND 9.6 KBPS)-TOGGLE BUFFERS ONE AND TWO
180			X	HIGH	KSC CHECKOUT FORMAT. RECONFIGURATION ON FLIGHT BASIS-TOGGLE BUFFERS AND PDI WINDOW WILL BE AS REQUIRED TO SUPPORT C/O
252		X		HIGH	SAIL, MCC/TDC INTERFACE TEST, AND PREFLIGHT IUS COMMUNICATIONS TEST FORMAT-TWO PDI WINDOWS (67.2 KBPS AND 19.2 KBPS)-TOGGLE BUFFER TWO

APPENDIX C
DPS ELECTRICAL BUS LOSS MATRIX

BOX \ BUS	GPC 1			GPC 2			GPC 3			GPC 4			GPC 5			CB	GPC STAT	CICU
	CPU 1			CPU 2			CPU 3			CPU 4			CPU 5					
	RPC A	B	C	RPC A	B	C	RPC A	B	C	RPC A	B	C	RPC A	B	C			
V MN A	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
FPC 1																		
MPC 1																		
APC 1																		
APC 4																		
O14, B																		
V MN B	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
FPC 2																		
APC 2																		
APC 5																		
O15, B																		
V MN C	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
FPC 3																		
MPC 3																		
APC 3																		
APC 6																		
V CAB PL 2																		
V ESS 1BC O13, A	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
V ESS 2CA O13, C	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
V ESS 3AB O13, E	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
V CNTL AB1																		
AB2																		
AB3																		
V CNTL BC1																		
BC2																		
BC3																		
V CNTL CA1																		
CA2																		
CA3																		

☒ = TELEMETRY INDICATION

DPS Electrical Bus Loss Matrix.

BOX BUS	TIME						DBIA'S		MEC'S			BFC'S									AV BAY'S				
	TIMERS						PL TIMING BUFFER																		
	FWD EVENT	AFT EVENT	FWD MISSION	AFT MISSION	CB A	CB B	MTU	RPC A	RPC B	MEC 1	MEC 2	RPC A	RPC B	RPC C	BFC 1-A	BFC 1-B	BFC 2-A	BFC 2-B	BFC 3-A	RA A	RA B	RA C	FAN A 1	FAN A 2	FAN A 3
V MN A	X	X					X	X	X		X	X		X	X	X	X	X	X	X	X	X	X	X	X
FPC 1																									
MPC 1																									
APC 1																									
APC 4																									
O14, B	X	X																							
V MN B	X		X				X	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X	X	
FPC 2																									
APC 2																									
APC 5																									
O15, B	X		X																						
V MN C									X		X	X		X	X	X	X	X	X	X	X	X	X	X	
FPC 3																									
MPC 3																									
APC 3																									
APC 6									X		X	X		X	X	X	X	X	X	X	X	X	X	X	
V CAB PL 2							X																		
V ESS 1BC																									
O13, A							X																		
V ESS 2CA																									
O13, C							X																		
V ESS 3AB																									
O13, E																									
V CNTL AB1							X	X	X	X	X	X													
AB2																									
AB3																									
V CNTL BC1							X	X	X	X	X	X													
BC2																									
BC3																									
V CNTL CA1																									
CA2																									
CA3																									

DPS Electrical Bus Loss Matrix.

BOX \ BUS	MCDS				FF MDM'S				FA MDM'S				PL MDM'S			MMU'S													
	DEU'S				DU'S																								
	DEU 1	2	3	4	DU 1	2	3	4	RPC A	B	RPC B	C	RPC A	C	RPC A	B	RPC B	C	RPC A	B	C	PL 1	PL 2	PL 3*	MM 1	MM 2			
V MN A	X				X				X				X				X				X				X			X	
FPC 1	X				X				X				X				X				X				X			X	
MPC 1																													
APC 1																													
APC 4																													
O14, B																													
V MN B		X				X				X				X				X				X				X			X
FPC 2		X				X				X				X				X				X				X			X
APC 2																													
APC 5																													
O15, B																													
V MN C		X	X			X	X			X	X			X	X			X	X			X	X			X	X		X
FPC 3		X	X			X	X			X	X			X	X			X	X			X	X			X	X		X
MPC 3																													
APC 3																													
APC 6																													
V CAB PL 2																													
V ESS 1BC																													
O13, A																													
V ESS 2CA																													
O13, C																													
V ESS 3AB																													
O13, E																													
V CNTL AB1	X			X	X			X	X			X	X			X	X			X	X			X	X			X	
AB2																													
AB3																													
V CNTL BC1		X				X				X				X				X				X				X			X
BC2		X				X				X				X				X				X				X			X
BC3																													
V CNTL CA1		X				X				X				X				X				X				X			X
CA2		X				X				X				X				X				X				X			X
CA3																													

☒ = TELEMETRY INDICATION * = NOT APPLICABLE

DPS Electrical Bus Loss Matrix.

MNA Equipment lost	Comments
<p>FPC1</p> <div style="border: 2px solid black; padding: 5px; margin: 5px 0;"> <p><u>TLM</u> RPC A: GPC's 1-5</p> <p><u>No TLM</u> MMU I DEU 1, DU 1</p> </div> <p>1/2 [FF1, FF3, PL1] AV BAY 1 FAN A AV BAY 3 FAN B</p> <p>MPC1 →NO IMPACT←</p> <p>APC1 1/2 [MEC 1]</p> <p>APC4 1/2 [FA1, FA3, FA4]</p> <p>O14 AFT EVENT TIMER (PNL A4) FWD MISSION TIMER (PNL 03)</p> <p>AC1 (φA) NUMERIC LIGHTING: (φB) RH KYBD ALL MISSION AND EVENT TIMERS</p>	<p><u>Will lose:</u> <u>If:</u></p> <p>MMU 2 CNTL AB2+</p> <p>CRT 2 CNTL BC2+</p> <p> 3 CA1+</p> <p> 4 CA2+</p> <p>FF 1 CNTL AB3+</p> <p> 3 CA3+</p> <p>PL 1 CNTL AB3+</p> <p>FA 1 CNTL AB2+</p> <p> 3 CA2+</p> <p> 4 CA3+</p> <p>PNL L4:R CB 126</p>

<u>MNB</u> Equipment lost	Comments
<p>FPC2</p> <div style="border: 2px solid black; padding: 5px; margin-bottom: 10px;"> <p><u>TLM</u> RPC B: GPC's 1-5</p> <p><u>No TLM</u> MMU 2 DEU 2, DU 2</p> </div> <p>1/2 [FF1, FF2, FF4] 1/2 [PL1, PL2] AV BAY 1, FAN B AV BAY 2, FAN A</p> <p>FLC2 NSP 1</p> <p>MPC2 →NO IMPACT←</p> <p>APC2 1/2 [MEC 1, MEC 2]</p> <p>APC5 1/2 [FA1, FA2]</p> <p>O15 FWD EVENT TIMER (PNL 03) AFT MISSION TIMER (PNL A4)</p>	<p><u>Will lose:</u> <u>If:</u></p> <p>MMU 1 CNTL AB1↓</p> <p>CRT 1 CNTL AB1↓ 3 CA1↓ 4 CA2↓</p> <p>FF 1 CNTL AB2↓ 2 BC3↓ 4 BC3↓</p> <p>FA 1 CNTL AB1↓ 2 BC2↓</p> <p>PL 1 CNTL AB1↓ 2 BC3↓</p> <p>NSP 2 CNTL BC2↓</p>

MNC Equipment lost	Comments
<p>FPC3</p> <div style="border: 2px solid black; padding: 5px; margin: 5px 0;"> <p>TLM RPC C: GPC's 1-5</p> <p>No TLM DEU 3, DU 3 DEU 4, DU 4</p> </div> <p>1/2 [FF2, FF3, FF4, PL2] AV BAY 2, FAN B AV BAY 3, FAN A</p> <p>FLC3 NSP 2</p> <p>MPC3 →NO IMPACT←</p> <p>APC3 1/2 [MEC 2]</p> <p>APC6 1/2 [FA2, FA3, FA4]</p> <p>O16 ORBITER TIMING BUFFER AFT MISSION TIMER (PNL A4)</p> <p>AC3 (φB) NUMERIC LIGHTING: LH KYBD MS KYBD</p>	<p><u>Will lose:</u> <u>If:</u></p> <p>CRT 1 CNTL AB1+ 2 BC2+</p> <p>FF 2 CNTL BC2+ 3 CA2+ 4 BC1+</p> <p>NSP 1 CNTL BC1+</p> <p>FA 2 CNTL BC1+ 3 CA1+ 4 CA1+</p> <p>PL 2 CNTL BC1+</p> <p>TIME STOPS UPDATING</p> <p>PNL L4:R CB 125 PNL L4:Q CB 106</p>

<u>ESS</u> Equipment lost	Comments
<p><u>ESS 1BC</u> <u>No TLM</u></p> <p>DA1 C/W SYS A PWR SUPPLY: ● ALL ANNUN LTS (PNL F7) ● PRI C/W LIMIT SENSING ● UPPER BULBS MA LTS</p> <div style="border: 1px solid black; padding: 5px; margin: 5px 0;"> <p>TLM GPC 1,4 HALT GPC 1,4 TERM (SW POS)</p> </div> <p>FD</p> <p>013 MTU OSC 1 (6 WATT HTR, PWR SUPPLY #1) LOC: ROW A, CB4</p>	<p><u>Caution:</u> Do not power down GPC 1 or 4</p> <p>Backup sw pos results in I/O TERM B.</p> <p>Loss of HISAM dump cap</p> <p>Loss of MTU pwr supply #1, will cause an MTU BITE, but will not immediately cause an auto OSC switch</p>
<p><u>ESS 2CA</u> <u>No TLM</u></p> <p>DA2 C/W SYS B PWR SUPPLY: ● B/U C/W ALARM ANNUN LIGHT CANNOT BE RESET ● LOWER BULBS MA LTS</p> <div style="border: 1px solid black; padding: 5px; margin: 5px 0;"> <p>TLM GPC 2,5 HALT GPC 2,5 TERM (SW POS)</p> </div> <p>FD</p> <p>013 MTU OSC 2 (6 WATT HTR, PWR SUPPLY #2) LOC: ROW C, CB12</p>	<p><u>Caution:</u> Do not power down GPC 2 or 5</p> <p>Backup sw pos results in I/O TERM B.</p> <p>Loss of HISAM dump cap</p> <p>Loss of MTU pwr supply #2, will cause an MTU BITE, but will not immediately cause an auto OSC switch</p>
<p><u>ESS 3AB</u> <u>TLM</u></p> <div style="border: 1px solid black; padding: 5px; margin: 5px 0;"> <p>GPC 3 HALT GPC 3 TERM (SW POS)</p> <p>NO TLM NO BFS ENGAGE CAP</p> </div> <p>FD</p> <p>013 CICU ● CAM (PNL O1) ● GPC STATUS CB LOC: ROW E, CB18</p>	<p><u>Caution:</u> Do not power down GPC 3</p> <p>Backup sw pos results in I/O TERM B.</p> <p>Loss of HISAM dump cap</p> <p>Cannot select any GPC as backup</p> <p>No CAM</p> <p>Loss of OI TLM H/W fail indications</p>

<u>CNTL</u>		
<u>Bus</u> ↓	<u>TLM</u>	<u>No TLM</u>
AB1	DEU 1, DU 1 1/2 [FA1:RPC A] MMU 1 TLM INDICATION FOR HISAM DUMP	1/2 [PL1:RPC A]
AB2	1/2 [FF1:RPC A] MMU 2	1/2 [FA2:RPC B] 1/2 [FA1:RPC B]
AB3	1/2 [PL1:RPC B]	1/2 [FF1:RPC B] Loss of: <ul style="list-style-type: none"> ● CDR's RHC BFS ENG CAP ● GPC's 1,2,4 - no BFS ENG discrettes
BC1	1/2 [FA2:RPC B] 1/2 [PL2:RPC B] 1/2 [FF4:RPC B]	
BC2	DEU 2, DU 2 1/2 [FF2:RPC B]	1/2 [FA2:RPC C]
BC3		1/2 [FF2:RPC C] 1/2 [FF4:RPC C] 1/2 [PL2:RPC C]
CA1	DEU 3, DU 3	1/2 [FA3:RPC A] 1/2 [FA4:RPC A] Loss of: <ul style="list-style-type: none"> ● PLT's RHC BFS ENG CAP ● GPC's 3,5 - no BFS ENG discrettes
CA2	DEU 4, DU 4 1/2 [FA3:RPC C]	1/2 [FF3:RPC A]
CA3	1/2 [FF3:RPC C] 1/2 [FA4:RPC C]	

APPENDIX D
MASS MEMORY DESCRIPTIONS

MASS MEMORY TAPE DESCRIPTION

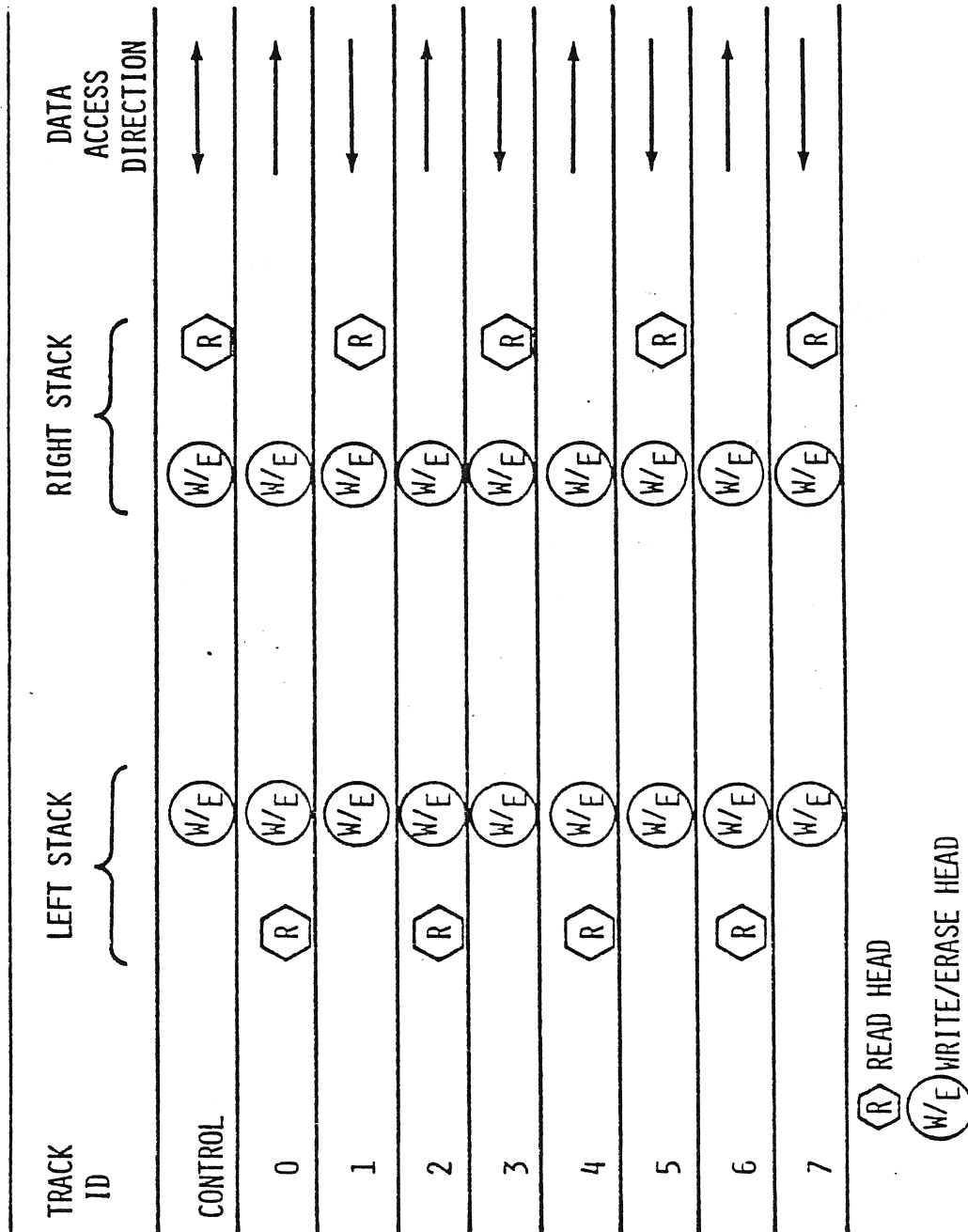
- 602 FEET LONG, 1/2 INCH WIDE, 1.13 MIL THICK MAGNETIC TAPE
 - 8 DATA TRACKS AND 1 CONTROL TRACK ARRANGED LONGITUDINALLY
 - 8 DATA FILES ARRANGED Laterally SEPARATED BY PROTECTIVE GAPS
 - 8 SUBFILES/FILE/TRACK
 - 32 BLOCKS OF DATA WORDS/SUBFILE SEPARATED BY PROTECTIVE GAPS
 - 512 SEVENTEEN-BIT WORDS/BLOCK: 16 BITS OF DATA + 1 BIT FOR PARITY
 - READ OR WRITE 1 SUBFILE OF 1 TRACK = 2.82 SECONDS
 - READ OR WRITE 1 FILE OF 1 TRACK = 8.59 SECONDS
 - READ OR WRITE 212,992 DATA WORDS (1 MAIN MEMORY) = 14-15 SECONDS
-

MASS MEMORY TAPE HEAD DESCRIPTION

-
- 2 WRITE/ERASE HEADS PER TRACK
 - DATA RECORDED ON 1 TRACK AT A TIME IN ONE DIRECTION ONLY
 - DIRECTION DATA IS RECORDED ALTERNATES FROM 1 TRACK TO THE NEXT
 - FOR EXAMPLE, THE TAPE MOVES TO THE LEFT WITH RESPECT TO THE HEADS TO WRITE ON (OR READ FROM) TRACK 3
 - THE (W/E) HEAD IN THE RIGHT STACK ERASES DATA FROM TRACK 3 WHILE THE (W/E) HEAD IN THE LEFT STACK WRITES DATA ONTO TRACK 3

 - 1 READ HEAD/TRACK - THE (R) HEAD FOR TRACK 3 IN THE RIGHT STACK READS DATA FROM TRACK 3
-

MASS MEMORY TAPE HEAD ORGANIZATION



D-5. MASS MEMORY TAPE HEAD ORGANIZATION

MASS MEMORY BITE STATUS DATA

BIT #	STATUS REGISTER A	STATUS REGISTER B
1	● POWER 24 VDC FOR 250 SEC	● WORDS/BLOCK = 512 FOR WRITE
2	● LAST REQUESTED FILE = LAST REQUESTED TAPE POSITION	● DROPOUT DURING DATA READ
3	● INVALID TAPE POSITION REQUESTED	● WORDS/BLOCK = 512 FOR READ
4	● WRITE COMMANDED ON PROTECTED TRACK	● DATA READ PARITY ERROR
5	● MIA DETECTED ERRORS ON COMMAND WORD	● INVALID MANCHESTER II FORMAT ON COMMAND DATA FOR WRITE
6	● SPARE	● GPC COMMAND RECEIVED WHEN NOT READY
7	● SPARE	● OPERATION COMPLETE WITHOUT LAST BLOCK
8	● SPARE	● REQUESTED ADDRESS NOT IN FILE SEARCHED
9	● SPARE	● MALFUNCTION IN MOTOR OR HEAD OPERATION
10	● SPARE	● BEGINNING OF TAPE SENSED
11	● SPARE	● END OF TAPE SENSED
12	● SPARE	● OPERATION ABORTED: POWER SUPPLY OR MOTOR PROBLEM
13	● SPARE	● MIA: WRONG NUMBER OF BITS IN COMMAND DATA
14	● SPARE	● MIA: PARITY ERROR ON COMMAND DATA
15	● SPARE	● INVALID "101" CHECK BITS ON COMMAND
16	● SPARE	● COMMAND SYNC IN BLOCK OF DATA
		● BITS 13, 14, OR 15 ARE SET

APPENDIX E
HARDWARE DATA SHEET

APPENDIX E
HARDWARE DATA SHEET

HARDWARE	CONTRACTOR	DIMENSIONS (INCHES)	WEIGHT (LBS.)	POWER INPUT (VDC)	NOMINAL POWER USAGE (WATTS)	OTHER CHARACTERISTICS
CPU	IBM	10X7.5X20	60	28	320-50% DUTY CYCLE IN RUN 300-HALT, STBY	163, 840 18-BIT WORD RAM
IOP	IBM	10X7.5X20	60	28	340-50% DUTY CYCLE IN RUN 300-HALT, STBY	49,152 18-BIT WORD RAM
MMU	ODETICS	10X7.5X15	25	28	53 - TAPE MOVING 20 - STANDBY	8,388, 608 17-BIT WORD MAGNETIC TAPE STORAGE
MDM	SPERRY- RAND	10X7X13	38	28	60 - 80	512 16-BIT WORD ROM
DEU	IBM	10X7.5X20	38.5	28	207	8192 17-BIT WORD RAM
DU	NORDEN	10X7X16	26.2	28	90 - ON 20 - STBY	5" X 7" CRT: 51 CHARACTERS X 26 LINES
KBU	IBM	6.5X4.5X7	3	5 VAC	8/KBU	32 DUAL-LAMP KEYS
DBIA	SINGER	7X3X8.5	7.5	28	22/CHANNEL	2 CHANNELS/DBIA (GSE, SRB)
BFC	AUTONETICS	7X3.5X15	8	28	12/MODULE	2 MODULES/BFC; 1 MODULE/GPC

APPENDIX F
SYSTEM FAULT MESSAGES

CRT ID	FAULT MESSAGE		PASS	BFS	A L R M C L	SOFTWARE DRIVEN CAUTION & WARNING LIGHT	CONDITIONS
	MAJOR FIELD	MINOR FIELD	OPS AVAIL	OPS AVAIL			
	B C E P L		Yes	No	3		o PL 1/2 BYPASS
	B C E S T R G 1	A	Yes	Yes	3		o FF1 INPUT PROM SEQ 1, 2 BYPASS
		ADTA	Yes	Yes	3		o FF1 ADTA BYPASS
		B	Yes	Yes	3		o FF1 INPUT PROM SEQ 2, 6 BYPASS
		C	Yes	Yes	3		o FA1 INPUT PROM SEQ 1, 2 BYPASS
		D	Yes	Yes	3		o FA1 INPUT PROM SEQ 3, 10 BYPASS
		IMU	Yes	Yes	3		o FF1 IMU BYPASS
		MLS	Yes	No	3		o FF1 MSBLS BYPASS
		MTU	Yes	Yes	3		o FF1 MTU BYPASS
		NSP	Yes	Yes	3		o FF1 NSP DISCRETES
		STKR	Yes	No	3		o FF1 STU BYPASS
		TAC	Yes	Yes	3		o FF1 TACAN/RA BYPASS
	PASS	No	Yes	3		o FAIL SYNC ON FF1/FA1	
	B C E S T R G 2	A	Yes	Yes	3		o FF2 INPUT PROM SEQ 1, 2 BYPASS
		ADTA	Yes	Yes	3		o FF2 ADTA BYPASS
		B	Yes	Yes	3		o FF2 INPUT PROM SEQ 2,6 BYPASS
		C	Yes	Yes	3		o FA2 INPUT PROM SEQ 1,2 BYPASS
		D	Yes	Yes	3		o FA2 INPUT PROM SEQ 3, 10 BYPASS
		IMU	Yes	Yes	3		o FF2 IMU BYPASS
		MLS	Yes	No	3		o FF2 MSBLS BYPASS
		MTU	Yes	Yes	3		o FF2 MTU BYPASS
		TAC	Yes	Yes	3		o FF2 TACAN/RA BYPASS
		PASS	No	Yes	3		o FAIL SYNC ON FF2/FA2
		B C E S T R G 3	A	Yes	Yes	3	
	ADTA		Yes	Yes	3		o FF3 ADTA BYPASS
	B		Yes	Yes	3		o FF3 INPUT PROM SEQ 2, 6 BYPASS
	C		Yes	Yes	3		o FA3 INPUT PROM SEQ 1, 2 BYPASS
	D		Yes	Yes	3		o FA3 INPUT PROM SEQ 3, 10 BYPASS
	IMU		Yes	Yes	3		o FF3 IMU BYPASS
	MLS		Yes	No	3		o FF3 MSBLS BYPASS
	MTU		Yes	Yes	3		o FF3 MTU BYPASS
	NSP		Yes	Yes	3		o FF3 NSP DISCRETES
	STKR		Yes	No	3		o FF3 STU BYPASS
	TAC		Yes	No	3		o FF3 TACAN/RA BYPASS
	PASS	No	Yes	3		o FAIL SYNC ON FF3/FA3	

CRT ID	FAULT MESSAGE		PASS OPS AVAIL	BFS OPS AVAIL	ALRM CL	SOFTWARE DRIVEN CAUTION & WARNING LIGHT	CONDITIONS
	MAJOR FIELD	MINOR FIELD					
	BCE STRG 4	A	Yes	Yes	3		o FF4 INPUT PROM SEQS 1, 2 BYPASS
		ADTA	Yes	Yes	3		o FF4 ADTA BYPASS
		B	Yes	Yes	3		o FF4 INPUT PROM SEQS 2, 6 BYPASS
		C	Yes	Yes	3		o FA4 INPUT PROM SEQS 1, 2 BYPASS
		D	Yes	Yes	3		o FA4 INPUT PROM SEQS 3, 10 BYPASS
		PASS	No	Yes	3		o FAIL SYNC ON FF4/FA4
	CRT BITE	1	Yes	Yes	3		o DEU1 BITE INDICATION
		2	Yes	Yes	3		o DEU2 BITE INDICATION
		3	Yes	Yes	3		o DEU3 BITE INDICATION
		4	Yes	Yes	3		o DEU4 BITE INDICATION
	GPC	BITE	Yes	Yes	3		o FORCE CLOSE ANY PROCESS
		CONF	Yes	No	3		o NOT ALL TARGET GPC'S IN RUN MODE o NO TARGET GPC IN RUN MODE
		SUM	No	Yes	3		o BFS GPC CHECKSUM ON PROTECTED FAIL
		1	Yes	No	2	* BACKUP C/W	o GPC1 FAIL IND
		2	Yes	No	2	* BACKUP C/W	o GPC2 FAIL IND
		3	Yes	No	2	* BACKUP C/W	o GPC3 FAIL IND
		4	Yes	No	2	* BACKUP C/W	o GPC4 FAIL IND
		5	Yes	No	2	* BACKUP C/W	o GPC5 FAIL IND
	I/O ERROR	CRTI	Yes	Yes	3		o I/O ERROR IN DEU1 INITIALIZATION o ERROR IN DEU1 MSG I/O OR CHECKSUM + o I/O ERROR IN DEU1 CRITICAL FORMAT LOAD

* A GPC FAIL will also result in the annunciation of a GPC status Matrix light and the C&W 'GPC' light.

+ Supported in PASS only.

CRT ID	FAULT MESSAGE		PASS OPS AVAIL	BFS OPS AVAIL	ALRM CLK	SOFTWARE DRIVEN CAUTION & WARNING LIGHT	CONDITIONS
MAJOR FIELD	MINOR FIELD						
I / O ERROR	C R T 2	Yes	Yes	3		<ul style="list-style-type: none"> o I/O ERROR IN DEU2 INITIALIZATION o ERROR IN DEU2 MSG I/O OR CHECKSUM + o I/O ERROR IN DEU2 CRITICAL FORMAT LOAD 	
	C R T 3	Yes	Yes	3		<ul style="list-style-type: none"> o I/O ERROR IN DEU3 INITIALIZATION o ERROR IN DEU3 MSG I/O OR CHECKSUM + o I/O ERROR IN DEU3 CRITICAL FORMAT LOAD 	
	C R T 4	Yes	Yes	3		<ul style="list-style-type: none"> o I/O ERROR IN DEU4 INITIALIZATION o ERROR IN DEU4 MSG I/O OR CHECKSUM + o I/O ERROR IN DEU4 CRITICAL FORMAT LOAD 	
	F A 1	Yes	Yes	3		<ul style="list-style-type: none"> o I/O ERROR ON FA1/P1 o I/O ERROR ON FA1/P2 	
	F A 2	Yes	Yes			<ul style="list-style-type: none"> o I/O ERROR ON FA2/P1 o I/O ERROR ON FA2/P2 	
	F A 3	Yes	Yes	3		<ul style="list-style-type: none"> o I/O ERROR ON FA3/P1 o I/O ERROR ON FA3/P2 	
	F A 4	Yes	Yes	3		<ul style="list-style-type: none"> o I/O ERROR ON FA4/P1 o I/O ERROR ON FA4/P2 	
	F F 1	Yes	Yes	3		<ul style="list-style-type: none"> o I/O ERROR ON FF1/P1 o I/O ERROR ON FF1/P2 	
	F F 2	Yes	Yes	3		<ul style="list-style-type: none"> o I/O ERROR ON FF2/P1 o I/O ERROR ON FF2/P2 	
	F F 3	Yes	Yes	3		<ul style="list-style-type: none"> o I/O ERROR ON FF3/P1 o I/O ERROR ON FF3/P2 	
	F F 4	Yes	Yes	3		<ul style="list-style-type: none"> o I/O ERROR ON FF4/P1 o I/O ERROR ON FF4/P2 	
	L A 1	No	Yes	3		<ul style="list-style-type: none"> o I/O ERROR ON LA1/P1 o I/O ERROR ON LA1/P2 	
	L F 1	No	Yes	3		<ul style="list-style-type: none"> o I/O ERROR ON LF1/P1 o I/O ERROR ON LF1/P2 	

+ Supported in PASS only.

CRT ID	FAULT MESSAGE		PASS	BFS	A L R M C L	SOFTWARE DRIVEN CAUTION & WARNING LIGHT	CONDITIONS
	MAJOR FIELD	MINOR FIELD	OPS AVAIL	OPS AVAIL			
	I / O E R R O R	MMU	Yes	No	3		<ul style="list-style-type: none"> o CHECKSUM ERROR OR I/O ERROR ON MMU TRANSACTION o FORMAT NOT FOUND IN BUFFER FOLLOWING RETRIEVAL FROM MMU o DATA XFER ON CHECKSUM ERROR ON GPC-GPC OVERLAY VIA MM OR LDB
		PCM	Yes	Yes	3		<ul style="list-style-type: none"> o I/O ERROR ON PCMMU
		PL1	Yes	Yes	3		<ul style="list-style-type: none"> o I/O ERROR ON PF1/PI o I/O ERROR ON PF1/P2
		PL2	Yes	Yes	3		<ul style="list-style-type: none"> o I/O ERROR ON PF2/PI o I/O ERROR ON PF2/P2
	ILLEGAL ENTRY		Yes	Yes	5		<ul style="list-style-type: none"> o OPS UNDEFINED OR OPS NOT RESIDENT AND NOT OVERLAY INITIATOR o OPS REQUEST CONTAINING INVALID MODE NUMBER o PRO NOT COMPATIBLE WITH CURRENT FORMAT OR STEP IN CONTROL SEGMENT o REQUESTED OPS NOT A LEGAL TRANSITION * o NO TARGET GPC IN CONFIG TABLE WHEN OPS SELECTED * o REQUEST REDUNDANT OPERATION OF SIMPLEX OPS * o REQUEST MEMORY RECONF WHEN GPCs NOT IN OPS OO RUN * o ATTEMPT TO ASSIGN PRIME GPC WHEN SELECTED GPC IS NOT PART OF AN RS o REQUEST FOR DEU INIT WHEN GPC NOT IN OPS OO OR PL OPS 9 * o NORMAL GMT UPDATE GREATER THAN 15 MS

* Supported in PASS only.

CRT ID	FAULT MESSAGE		PASS	BFS	A L R M C L	SOFTWARE DRIVEN CAUTION & WARNING LIGHT	CONDITIONS
	MAJOR FIELD	MINOR FIELD	OPS AVAIL	OPS AVAIL			
			Yes	Yes	5	*	<ul style="list-style-type: none"> o GMT OR MET DELTA UPDATE NOT ENTERED AND UPDATE REQUESTED o EXTERNAL DATA OUT OF LIMITS o INVALID ITEM NO. FOR DATA LOAD o ATTEMPT TO LOAD DATA VIA DISPLAY o INSUFFICIENT DIGITS ENTERED FOR ENG UNITS o ADD ID ON ODD WORD BOUNDARY WHEN 32 BIT FLOATING POINT OPTION IS SELECTED o SEQ READ REQ WITH NO ADD ID o EXEC LOAD WITH NO DATA o ATTEMPT TO WRITE INTO PROTECTED MEMORY WHEN MODE IS NOT CODE o SCALE CODE WITH BB 10 or A#1, 2 o EXEC LOAD WITH NO ADD ID o ADDRESS EXCEEDS MEMORY SIZE o DL DUMP ITEM EXEC IN MCI o NO DUMP ADDRESS SPECIFIED o SELECTION OF DISPLAY NOT ASSOCIATED WITH CURRENT OPS o SPEC NOT ALLOWED IN CURRENT OPS * o TWO ACTIVE NON-RESIDENT FORMATS WHEN ANOTHER REQUESTED * o REQUEST SPEC WHEN TWO ARE ACTIVE o GPC DETECTED INPUT MSG SYNTAX ERROR

ILLEGAL ENTRY

* Supported in PASS only.

CRT ID	FAULT MESSAGE		PASS	BFS	A L R M C L	SOFTWARE DRIVEN CAUTION & WARNING LIGHT	CONDITIONS
	MAJOR FIELD	MINOR FIELD	OPS AVAIL	OPS AVAIL			
	ILLEGAL ENTRY		Yes	Yes	5		<ul style="list-style-type: none"> o EXEC NOT COMPATIBLE WITH CURRENT FORMAT OR STEP IN CONTROL SEGMENT o EXEC, OR ITEM WHEN NEW FORMAT IS BEING RETRIEVED o INPUTS OTHER THAN MSG RESET, CLEAR, FAULT OR ACK IN MIDST OF OPS TRANSACTION o GPC/CRT KEY ENTRY WITH CRT # 1-4, GPC # 0-5
	MM OFF / BSY		Yes	No	3		<ul style="list-style-type: none"> o OPS NOT IN ACTIVE GPC AND MMU OFF/BUSY o REQUESTED MMU TRANSACTION WHEN MMU IS OFF/BUSY
	TIME	MTU	Yes	No	3		o AUTOMATIC TIME SOURCE CHANGE
		TONE	Yes	No	3		o TIME MGT TIME TONE

* Supported in PASS only.

APPENDIX G
LEGAL OPS/MODE TRANSITIONS

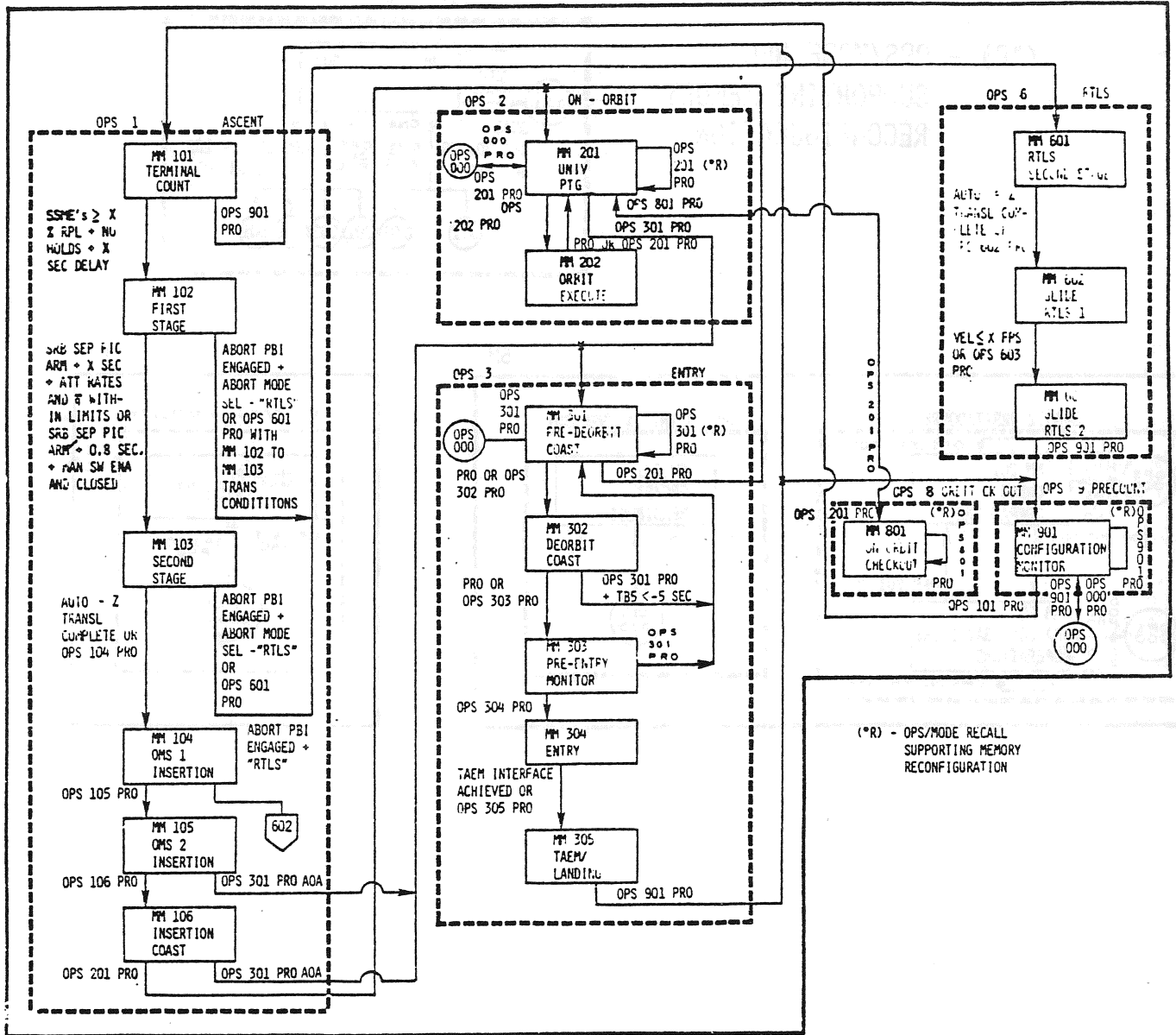


Figure G-2. Legal OPS/Mode Transitions (Sheet 1 of 2)

(*R) - OPS/MODE RECALL
SUPPORTING MEMORY
RECONFIGURATION

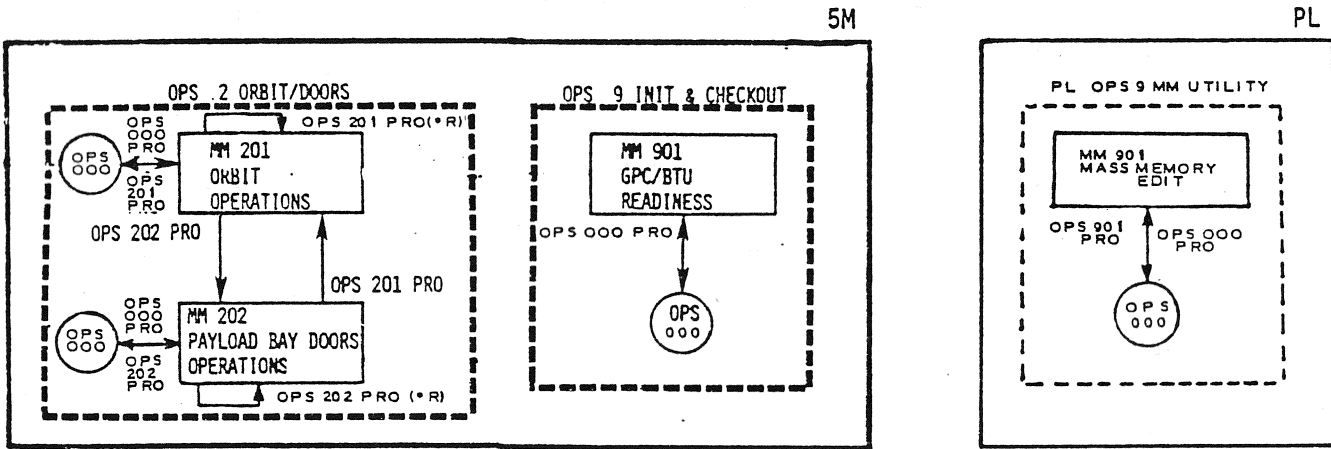
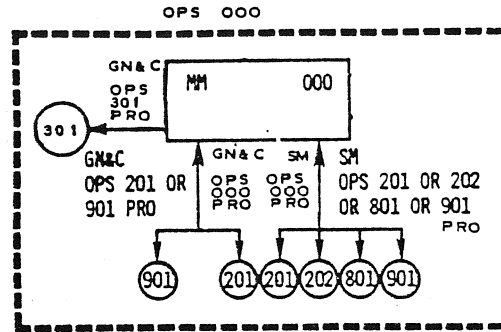


Figure G-3. Legal OPS/Mode Transitions (Sheet 2 of 2)

APPENDIX H
ACRONYMS AND ABBREVIATIONS

ACRONYMS AND ABBREVIATIONS

A	Amps
AA	Accelerometer Assembly
ACCEL	Accelerometer
ACK	Acknowledge
ACT	Activated
ACTR	Actuator
ACUM	Accumulator
A/D	Analog-to-Digital
ADD	Address
ADI	Attitude Director Indicator
ADTA	Air Data Transducer Assembly
ADU	Annunciator Display Unit
AID	Analog Input, Differential
AIS	Analog Input, Single-Ended
AMI	Alpha Mach Indicator
AOA	Abort Once Around
AOD	Analog Output, Differential
APC	Aft Power Controller
APU	Auxiliary Power Unit
ARS	Atmosphere Revitalization System
ASA	Aerosurface Amplifier
ASSY	Assembly
ATO	Abort to Orbit
ATT	Attitude
ATVCD	Ascent Thrust Vector Control Driver
AVVI	Altitude/Vertical Velocity Indicator
BCE	Bus Control Element
BFC	Backup Flight Controller
BFS	Backup Flight System
BITE	Built-in Test Equipment
BOS	Backup Operating System
BRNG	Bearing
BSY	Busy
BTU	Bus Terminal Unit
B/V	Bleed Valve
CAM	Computer Annunciation Matrix
C&D	Controls and Displays
C&W, C/W	Caution and Warning
CDR	Commander
CICU	Computer Interface Conditioning Unit
CL	Closed
CMC	Command Module Computer
CMD	Command
CMPT	Computer
CNTL, CNTRL	Control
COMM	Communications
COMP	Comparison, Computation
CON	Contact
COND	Conditioner
CONFIG	Configuration

ACRONYMS AND ABBREVIATIONS (CONT'D)

CPDS	Comuter Program Development Specification
CPU	Central Processing Unit
CRT	Cathode Ray Tube
CS	Common Set
CSM	Computer Status Matrix
CSTA	Crew Software Training Aid
DBIA	Data Bus Isolation Amplifier
DDS	Detailed Design Specification
DDU	Display Driver Unit
DES	Deselect
DEU	Display Electronics Unit
D/H	Discrete Input High
D/L	Discrete Input Low
DISC	Disconnect
DISP	Display Function
DK	Display/Keyboard
D/L	Downlist, Downlink
DOH	Discrete Output High
DOL	Discrete Output Low
DPLR	Doppler
DPS	Data Processing Subsystem
DU	Display Unit
ECLSS	Environmental Control Life Support Subsystem
EIU	Engine Interface Unit
EMER	Emergency
EMI	Electromagnetic Interference
ENA	Enable
ENG	Engine
EPDC	Electrical Power Distribution and Control Subsystem
EPGS	Electrical Power Generating Subsystem
EPS	Electrical Power System
ERR	Error
ESS	Essential
ET	External Tank
EXEC	Execute
FA	Flight Critical Aft
FAULT SUMM	Fault Summary
FC	Flight Critical
FCOS	Flight Computer Operating System
FCS	Flight Control Subsystem
FDA	Fault Detection and Annunciation
FDBK	Feedback
FDLN	Feedline
FDS	Functional Design Specification
FF	Flight Critical Forward
FL	Filter
FML	Fault Message Line
FPC	Forward Power Controller

ACRONYMS AND ABBREVIATIONS (CONT'D)

FS	Fail-to-Sync
FSSR	Functional Subsystem Software Requirements
FU	Fuel
FWD	Forward
GCIL	Ground Control Interface Logic
GMT	Greenwich Mean Time
GNC	Guidance, Navigation and Flight Control
GPC	General Purpose Computer
GR	Gear
GSE	Ground Support Equipment
HDR	High Data Rate
He	Helium
HFE	High Frequency Executive
HSI	Horizontal Situation Indicator
HSR	Hardware Status Register
HT	Halt
H/W	Hardware
HYD	Hydraulics
Hz	Hertz
I	Initialization
IC, ICC	Inter-Computer Communication
ID	Identification
I/F	Interface
IGN	Ignition
IMU	Inertial Measurement Unit
INBD	Inboard
IND	Indication
INH	Inhibit
INIT	Initiation
I/O	Input/Output
IOP	Input/Output Processor
IP	Instrumentation/PCMMU
IPL	Initial Program Load
IPR	Input Problem Report
ISOL	Isolation
KB, KBU	Keyboard Unit
KBS, KBPS	Kilobits per Second
KYBD	Keyboard
LA	Launch Aft
LAT	Lateral
LB	Launch/Boost, Pound
LCH	Latch
LDB	Launch Data Bus
LDG	Landing
LDR	Low Data Rate
LF	Launch Forward

ACRONYMS AND ABBREVIATIONS (CONT'D)

LH	Left Hand
LH2	Liquid Hydrogen
LL	Launch (SRB) Left
LOX, L02	Liquid Oxygen
LR	Launch (SRB) Right
LRU	Line Replaceable Unit
LTCH	Latch
LVL	Level
LVLH	Local Vertical Local Horizontal
M	Motor
MAJ FUNC	Major Function
MAN	Manual
MANF	Manifold
MC	Memory Configuration
MCA	Motor Control Assembly
MCC	Mission Control Center
MCDS	Multifunction CRT Display System
MCIU	Manipulator Controller Interface Unit
MDM	Multiplexer/Demultiplexer
ME	Main Engine
MEC	Master Events Controller
MED	Medium
MET	Mission Elapsed Time
MF	Major Function
MFE	Mid Frequency Executive
MFO	Major Function overlay
MHz	Megahertz
MIA	Multiplexer Interface Adapter
MLS,MSBLS	Microwave Scanning Beam Landing System
MM, MMU	Mass Memory Unit
MN	Main
MON	Monitor
MPS	Main Propulsion System
MS	Mission Specialist
MSEC	Millisecond
MSG	Message
MTU	Master Timing Unit
NAV	Navigation
NLG	Nose Landing Gear
NOM	Network Output Multiplexer
NORM	Normal
NRZ	Nonreturn-to-Zero
NSP	Network Signal Processor
N/W	Nosewheel
OF	Operational Forward
OFT	Orbiter Flight Test
OI	Operational Instrumentation
OMS	Orbiter Maneuvering System

ACRONYMS AND ABBREVIATIONS (CONT'D)

OP	Open
OPS	Operational Sequence, Operations
ORB	Orbiter
OSC	Oscillator
OTP	Operational Test Program
OUTBD	Outboard
OWDE	One-way Doppler Extractor
OX	Oxidizer
P	Primary, Pitch
PASS	Primary Avionics Software System
PBI	Pushbutton Indicator
PBK	Payload Bay Kit
PCM	Pulse-Code Modulation
PCMMU	PCM Master Unit
PDI	Payload Data Interleaver
PET	Phase Elapsed Time
PF	Payload Forward MDM
PFS	Primary Flight System
PIC	Pyro-Initiator Capacitor
PL	Payload
PLB	Payload Bay
PLS	Payload Systems
PLT	Pilot
PNL	Panel
POSN	Position
PRFLT	Preflight
PRI	Primary
PRO	Proceed
PROM	Programmable Read Only Memory
PRT	Port
PT	Prime GPC GMT
PUR	Purge
PWR	Power
QTY	Quantity
R	Roll, Read
RA	Radar Altimeter
RAM	Random Access Memory
RCS	Reaction Control System
RCVR	Receiver
RD	Redundant Set
RDR	Radar
RDY	Ready
RECIRC	Recirculation
REFSMMAT	Reference Stable Member Matrix
RG, RGA	Rate Gyro Assembly
RH	Right Hand
RHC	Rotational Hand Controller
RJCS	Reaction Jet Control System

ACRONYMS AND ABBREVIATIONS (CONT'D)

RJDA	Reaction Jet Driver Aft
RJDF	Reaction Jet Driver Forward
RLF	Relief
RM	Redundancy Management
RN	Run
ROM	Read Only Memory
RPC	Remote Power Controller
RPTA	Rudder Pedal Transducer Assembly
RS	Redundant Set
RST	Reset
RT	Right
RTC	Real-Time Computer
RTLS	Return to Landing Site
S	Secondary
SASTP	Stand-alone Self-test Program
SBTC	Speed Brake Thrust Controller
SCU	Sequence Control Unit
SDPC	Shuttle Data Processing Complex
SEC	Second, Secondary
SEL	Select
SEQ	Sequence, Sequential
SEV	Status, Error, and Validity
SF	Selection Filter
SHT DN	Shut Down
SIO	Serial Input/Output
SIP	Systems Interface Processing Software
SM	Systems Management
SMRD	Spin Motor Run Detector
SNSR	Sensor
SPEC	Specialist Function
SPI	Surface Position Indicator
SPL	Scratch Pad Line
SPLY	Supply
SRB	Solid Rocket Booster SRB
SRT	Special Rated Thrust
SS	Space Shuttle
S/S	Samples per second
ST	Star Tracker
STAT	Status
STBY, SB	Standby
STDN	Space Tracking and Data Network
STP	Self-Test Program
STRG	String
STS	Shuttle Transportation System
STU	Star Tracker Unit
STWD	Stowed
SVC	Supervisor Call
S/W	Software

ACRONYMS AND ABBREVIATIONS (CONT'D)

SYNC	Synchronization
SYS	System
SYS SUMM	Systems Summary
TACAN	Tactical Air Navigation
TAEM	Terminal Area Energy Management
TB	Talkback
TBD	To Be Determined
TBS	To Be Supplied
TDRS	Telemetry Data Relay Satellite
TEMP	Temperature
THC	Translational Hand Controller
THROT	Throttle
TIG	Time of Ignition
TLM	Telemetry
TMP	Time Management Processor
TNK, TK	Tank
T/RA	Tacan/Radar Altimeter
TRKR	Tracker
UI	User Interface
UMB	Umbilical
VAC	Volts Alternating Current
VAR	Variable
VDC	Volts Direct Current
VLV	Valve
VU	Vehicle Utility
WD, WDS	Word(s)
WSTF	White Sands Test Facility
WONG	Weight on Nose Gear
WOW	Weight on Wheels
WT	Watchdog Timer
XDCR	Transducer
XFEED	Crossfeed
XMTR	Transmitter
XPNDR	Transponder
XTRTR	Extractor
Y	Yaw
μ sec	Microsecond
msec	Millisecond

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ALPHABETICAL INDEX

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