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1. SCOPE

1.1 Scope. This specification establishes the performance, design, development, and verification requirements for the general purpose computer, referred to herein as GPC, or computer, or the equipment for the Space Shuttle Orbiter, or AP-101S. This machine is a dual CPU architecture (Shuttle and MIL-STD-1750A) single ATR LRU with 262,144 words of main memory with the Shuttle Input-Output Processor (IOP) and power supply.

2. APPLICABLE DOCUMENTS

2.1 Applicability. The following documents of the exact issue shown form a part of this specification to the extent specified herein. In the event of a conflict between documents referenced herein and the contents of this specification, the contents of this specification shall take precedence.

SPECIFICATIONS

Military

MIL-M-7793(1) Meter, Time Totalizing
31 December 1969

National Aeronautics and Space Administration/Johnson Space Center (NASA/JSC)

SP-T-0023B Environmental Acceptance Testing
September 1974

Rockwell International/Space Division

MC999-0096D Materials and Processes Control and
30 August 1974 Verification System for Space Shuttle
Amendment E-01 Program: Suppliers and Subcontractors
22 January 1975
Amendment E-14
8 November 1982

MF0004-002B Electrical Design Requirements for
28 June 1974 Electrical Equipment Utilized on the
Amendment C-01 Space Shuttle Vehicle
20 March 1975
Amendment C-02
4 November 1975
Amendment C-03
2 July 1976
Amendment C-04
14 April 1971
Amendment C-05
12 June 1978
Amendment C-06
25 May 1979

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MF0004-009
 5 November 1973
 Amendment A-01
 12 March 1974
 Amendment A-02
 27 March 1974
 Amendment A-03
 7 January 1975
 Amendment A-04
 20 February 1975

Equipment Cooling Requirements,
 Electrical/Electronic

MC615-0002A
 14 January 1974

Computer Manufacturer Supplied Support
 Software I/O Specification

MF0004-400
 30 August 1977
 Amendment C34
 4 November 1982

Electrical, Electronic, and Electro-
 mechanical - Orbiter Project Parts List

MC615-0010
 2 November 1974
 Amendment A-03
 26 November 1974

Adapter, Interface, IOP Multiplexer

MF0004-036
 22 November 1974

Data Bus System, Space Shuttle

STANDARDS

Federal

FED-STD-101G(2)
 8 October 1982

Preservation, Packaging, and Packing
 Materials: Test Procedures

Military

MIL-STD-810C(4) (Notice 1)
 7 April 1981

Environmental Test Methods

MIL-STD-1472A
 15 May 1970

Human Engineering Design Criteria for
 Military Systems, Equipment, and
 Facilities

MIL-STD-794E(1)
 16 July 1982

Parts and Equipment, Procedures for
 Packaging and Packing of

MIL-STD-129H
 30 September 1982

Marking for Shipment and Storage

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MIL-STD-130F(3)
21 May 1982

Identification Marking of U.S. Military
Property

MIL-STD-454C
15 October 1970

Standard General Requirements for
Electronic Equipment

MIL-STD-143B
12 November 1969

Standards and Specifications, Order of
Precedence for the Selection of

MIL-STD-12D(1)
29 May 1981

Abbreviations for Use on Drawings and
in Technical-Type Publications

MIL-STD-280A
7 July 1969

Definitions of Item Level, Item Inter-
changeability, Models, and Related Items

OTHER PUBLICATIONS

Handbooks

NEB 6000.1(1C)
June 1976

Requirements for Packaging, Handling
and Transportation for Aeronautical
and Space Systems Equipment and
Associated Components

DOD H 4-1
Latest Revision

Federal Supply Code of Manufacturers
Name to Code

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3. REQUIREMENTS

3.1 Item Definition. The General Purpose Computer (GPC) shall provide the capability for the following data processing for the orbiter: computation for the guidance, navigation and control subsystem, payload control for the manipulators, payload management, and system performance monitoring for the Shuttle orbiter.

3.1.1 Block Diagram. The computer shall consist of three major processing elements and functions:

- a. Central Processor Unit (CPU)
- b. Input/Output Processor (IOP)
- c. Main Memory

The AP101S block diagram is shown in Figure 1.

All functions shall have access to the main memory.

The interfaces between the GPC and the avionics system are shown in Figure 2. The GPC will interface with orbiter avionics through Multiplexer Interface Adapters which will supply operational commands via a serial data stream. Discrete dc voltage control signals will be routed in both directions between the computers and between the computer and the mass memories and control panels. 28 volt main dc power will be provided from redundant orbiter distribution buses. Two dedicated connectors will provide access to test points for use in ground checkout operation (AGE connector).

3.1.2 Interface Definition. The functional and physical interface requirements between the GPC and the orbiter avionics systems are defined in the following paragraphs. The interface definition establishes the functional and physical characteristics at the interface. The interfaces require control since a change of characteristics on one side of the interface could require a design change on the other side.

3.1.2.1 Electrical Power Characteristics. The computer shall contain a power supply that converts input dc power to required internal operating voltages. Operation of the power supply shall be coordinated and sequence-controlled during computer turn-on and turn-off and input power interruptions and transients to assure a predictable initial operating state and continuity of operation and to minimize data loss. Application and removal of input power and power interruptions shall be sensed, power-off and power-on interrupt signals generated, and internal protective operations conducted as required to provide the response specified. The computer shall also contain batteries which shall be used to retain the contents of memory whenever primary power is removed.

3.1.2.1.1 Input Power. The computer shall operate from a single power input which will supply 28 vdc (nominal). The current demand within steady-state limits of the input voltages shall be limited to 20 amperes. Provisions shall be made within the computer for isolation of power sources in accordance with that requirements of Specification MF0004-002.

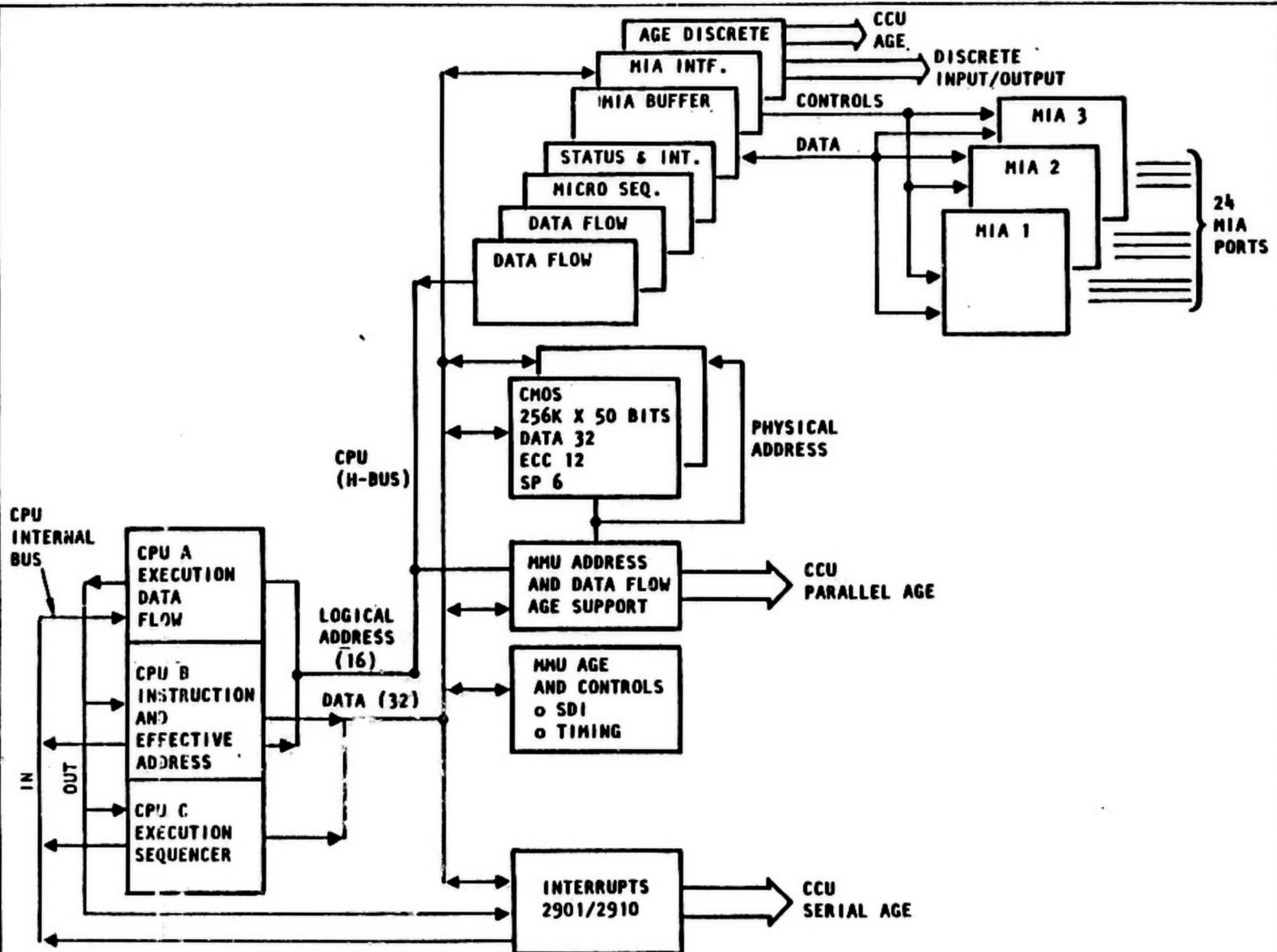


Figure 1. AP-101S Block Diagram

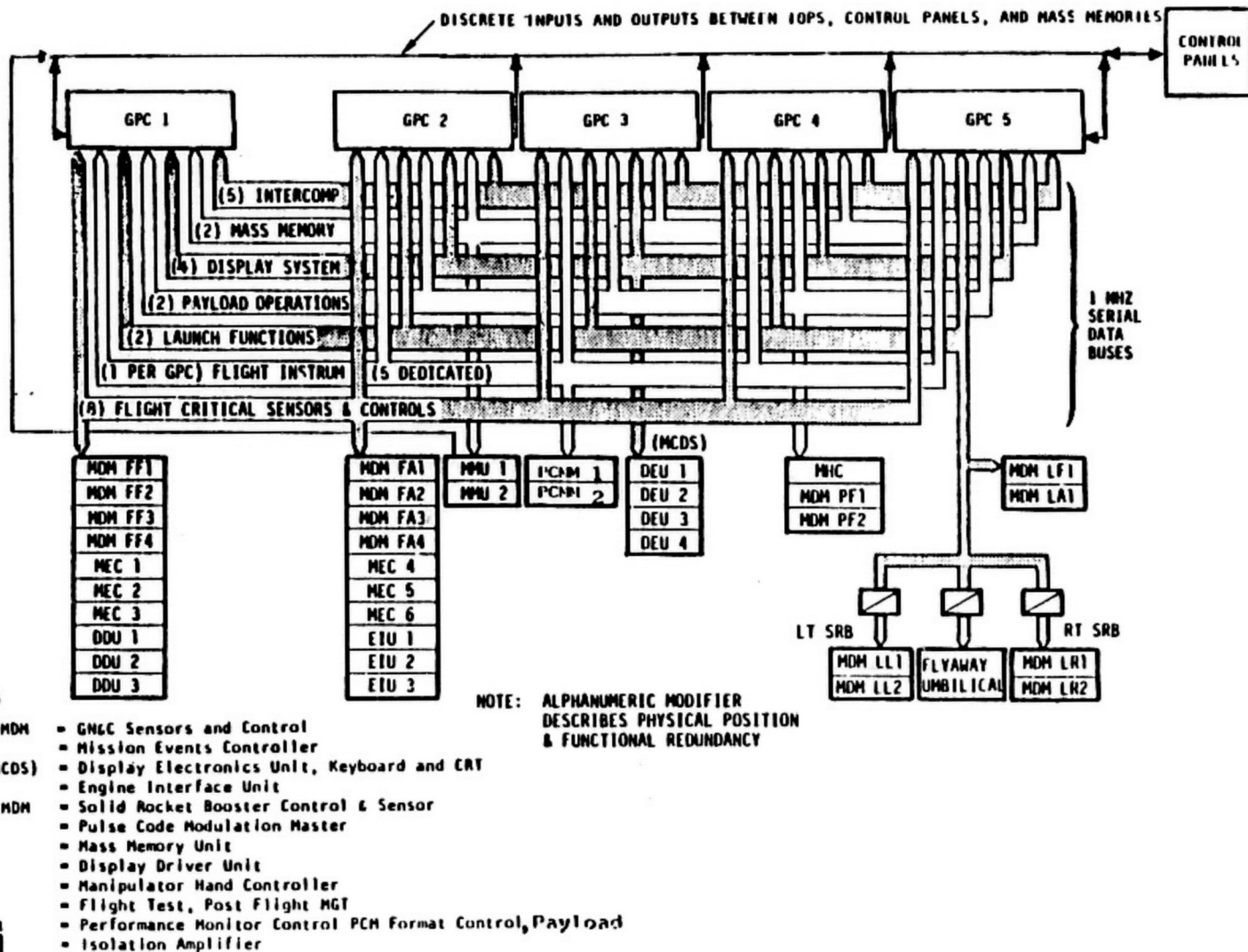


Figure 2. Multicomputer System Block Diagram

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3.1.2.1.1.1 Power Demand Goal. With the GPC equipped with 262,144 full words of memory and a duty cycle of 10 channels transmitting at a 15 percent duty cycle and 14 channels receiving, the input power demand shall be as follows:

- a. Maximum steady state current demand of 20A at 28 Vdc nominal input.
- b. Maximum steady state power demand of 550 watts at 24 Vdc input.

3.1.2.1.1.1.1 Deleted.

3.1.2.1.1.2 Power Characteristics. The computer shall perform as specified herein with input power meeting the requirements of Specification MF0004-002 for Category B equipment.

3.1.2.1.2 Capacity. All power supplies shall provide a reserve power capacity of at least 20 percent when operated at an input voltage not less than 24 VDC. One hundred percent power capacity is based upon the provisions of this specification.

3.1.2.1.3 Power-On Sequence. Application of input power to the computer shall be sensed and shall initiate an orderly startup and initialization sequence containing, but not limited to, the following steps:

- a. Sense input power application.
- b. Initiate master power reset signal. This event shall precede application of any internal supply voltages. This signal shall remain on continuously until turned off (Step f): Memory shall not be addressed, nor shall any I/O operations be conducted (discrete outputs shall be forced to the logic 0 state, except that the station ID source discrete output shall always be set to 1), while the master/power reset signal is on.
- c. Accomplish coordinated turn-on of CPU internal power supply.
- d. Reset interrupt status and disallow further interrupts until Step f.
- e. Microcode shall initialize registers and counters. The program counter shall be preset to address a predetermined memory location so that program execution will start with the first instruction in this location.
- f. Within 100 milliseconds after sensed input power application, generate a power-on interrupt signal and turn off the master power reset signal.
- g. Commence program execution at the location predetermined in step e. At this point, the discrete outputs are released from the condition of step b.

The master power reset signal (single-ended discrete) shall be made available at the computer interface for external uses.

3.1.2.1.4 Power-Off Sequence. Removal of input power from the computer shall be sensed and shall initiate an orderly shutdown sequence containing, but not limited to, the following steps:

- a. When the filtered 28-volt voltage decreases to a level of 17.5 Vdc, issue a Power-Off Interrupt (POI) signal.

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- b. Upon receipt of POI, the CPU shall complete any in-process instruction, putaway the general registers and Program Status Word (PSW), and terminate all IOP data bus transmission and reception.
- c. Accomplish coordinated turn-off of power supplies. The differential discrete output signals shall transition to the requirements specified in paragraph 3.1.2.3.1.4.6. Once shutdown is begun (issuance of POI), the sequence shall continue to completion regardless of subsequent input power status.
- 3.1.2.1.5 Power Interruption. The GPC shall meet all functional performance requirements with input power loss of up to 400 microseconds.
- 3.1.2.1.6 Normal Power Transients. Input power transients within the limits defined in Specification MF0004-002, Figure 11, for Category B equipment shall not cause computer malfunction.
- 3.1.2.1.7 Abnormal Power Transients. Input power transients with the limits defined in Specification MF0004-002, Figure 2, shall neither cause equipment damage nor spurious behavior, and the contents of memory shall not be affected. For undervoltage transients which exceed normal limits as defined in paragraphs 3.1.2.1.5 and 3.1.2.1.6, above, execution of a shutdown/restart sequence is permissible, provided all the sequence steps in paragraphs 3.1.2.1.4 and 3.1.2.1.3 are executed.
- 3.1.2.1.8 Grounding and Isolation. Provisions for equipment grounding for isolation of circuitry from ground, power returns, and shields, under normal and failure conditions, shall conform to the applicable requirements of Specification MF0004-002.
- 3.1.2.1.9 Electrical Bonding. Equipment chassis, cases, and enclosures shall incorporate electrical bonding provisions which meet the requirements of Specification MF0004-002.
- 3.1.2.1.10 Power Reapplication. Should input power be lost or an abnormal undervoltage transient occur for periods up to 400 microseconds, reapplication of input power shall inhibit a computer shutdown from being initiated, provided power is continuous once reapplied. Should power be discontinuous or subject to further abnormal undervoltage transients when reapplied, the computer shall initiate shutdown as defined in paragraph 3.1.2.1.4.
- 3.1.2.1.11 Battery Power. The battery pack used for memory retention in the event of primary power loss shall consist of rechargeable cells and have a nominal rating of 2 ampere hours at 3.6 Vdc. The battery pack shall be GPC front accessible for installation/removal with the GPC installed in its designated location.
- 3.1.2.2 Mechanical Interface.
- 3.1.2.2.1 Mounting. The mounting provisions of the GPC shall be as shown in Figure 3.

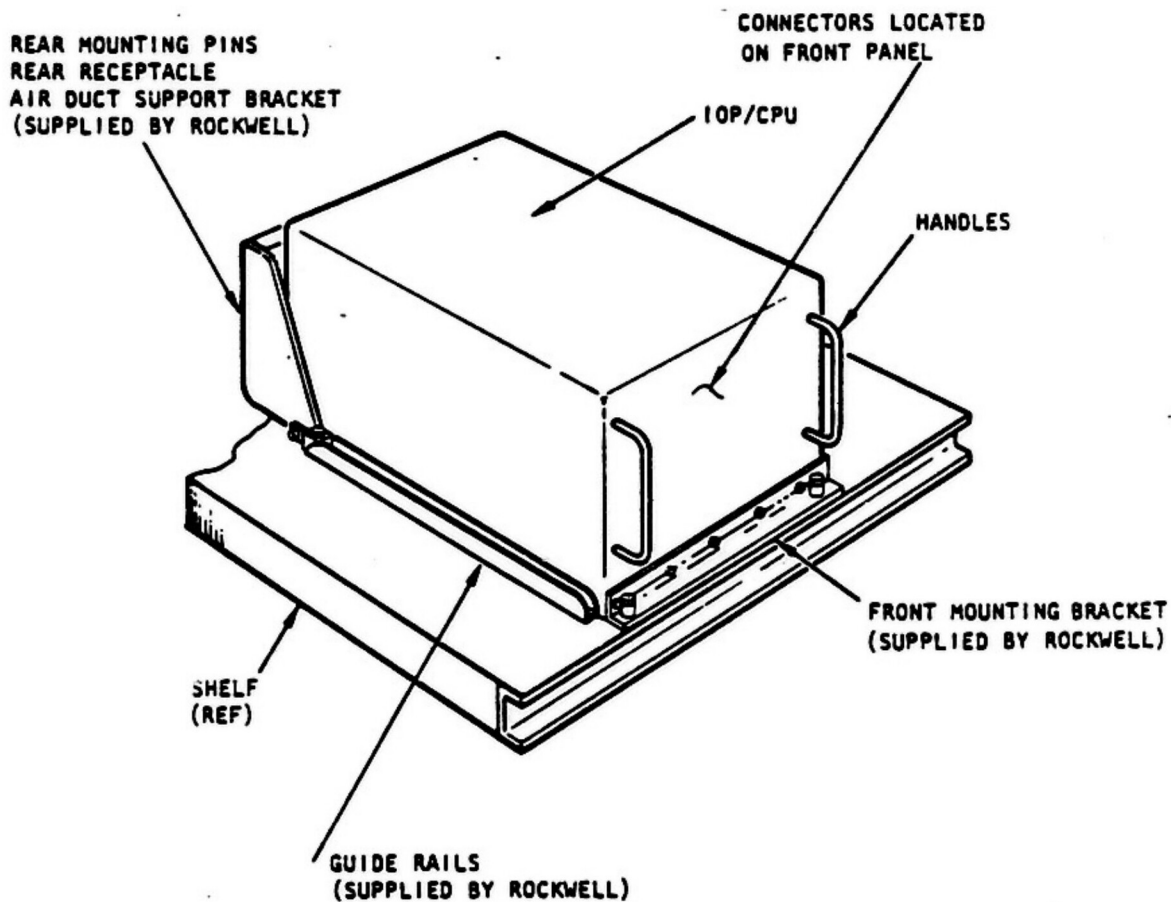


Figure 3. General Purpose Computer GPC Mounting Configuration

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3.1.2.2.2 Connector Location and Pin Function Assignments. Figure 4 specifies the electrical connector locations. Table I is a detailed connector and pin function listing. The connectors shall be of the type listed in Table I.

3.1.2.2.3 Cooling. The GPC shall be designed for forced-air cooling. The characteristics of GPC cooling shall be as specified in paragraph 3.2.7. The CPU structure shall comply with the requirements of MF0004-009.

3.1.2.3 Signal Interface Definition. The CPU LRU shall interface with the orbiter avionics system as shown in Figure 2. The individual signals at the CPU interface to other subsystem interfaces are shown in Table I.

3.1.2.3.1 Discrete Signal Characteristics. The interface requirements for all signals between elements of the GPC as well as those operating or terminating in the LRU of the GPC and interfacing with other LRU's of the orbiter avionics system are described below.

3.1.2.3.1.1 Discrete Wires/Cables. Other LRU's of the avionics systems that use differential drivers and receivers to the GPC will be connected via twisted shielded balanced pair or complementary cables. The cables will have a nominal line-to-line distributed capacitance of less than 30 picofarads per foot. The line-to-shield capacitance will be less than 50 picofarads per foot. Cables will be up to and including 100 feet in length including up to six stubs. Cables will be a minimum of 50 ohms impedance line to line.

3.1.2.3.1.2 Connectors. All cable connectors shall be low impedance. The shield will be connected to the LRU cases at each end with a Glen Air tag ring or equivalent. Ten percent spare pins shall be provided on each connector except as specified.

3.1.2.3.1.3 Complementary Discrete Input Signals.

3.1.2.3.1.3.1 Line Receivers. The line receivers shall be of the complementary type. The line receiver shall receive complementary digital data from the transmission lines using a plus 5-volt supply and a plus 12-volt supply.

3.1.2.3.1.3.1.1 Logic Voltage Levels. The logical one (+) state shall be defined as follows: The true side shall be plus 0.4 Vdc maximum minus 1.0 Vdc minimum. The complementary side shall be plus 12.4 Vdc maximum, plus 9.5 Vdc minimum; the true and complementary sides are reversed for the logical zero state.

3.1.2.3.1.3.1.2 Static Input Current Characteristics. The true and complementary sides of the input shall source up to 3.8 milliamps maximum when held at a down level (-5.0 Vdc minimum) and 0.4 milliamps minimum when held at an up level (9.4 Vdc maximum). The true and complementary sides of the input shall sink 5 microamps maximum at voltages above 12.0 Vdc (17.0 Vdc maximum).

3.1.2.3.1.3.1.3 Receiver Input Impedance. The line receiver input dynamic impedance at 5 megahertz shall be greater than 100 ohms. Line to line or line to ground.

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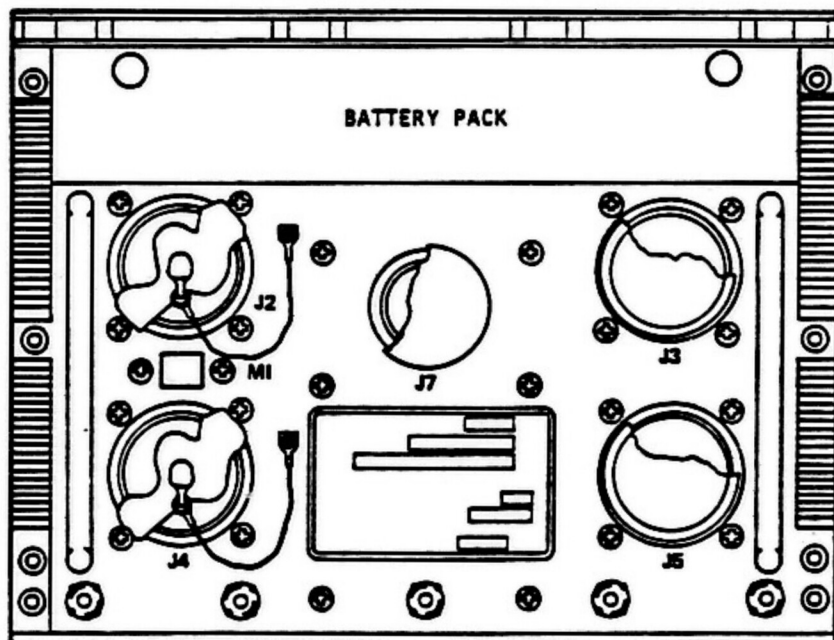


Figure 4. General Purpose Computer Connector Configuration

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Table I. Connector/Signal List

GPC Connector J2 - Connector Part No. MS27497T24F35PA

| GPC J2 Pin No. | Signal Name | GPC J2 Pin No. | Signal Name |
|-------------------|---|-------------------|---|
| 1 | SPARE | 42 | +L AGE DATA B20 |
| 2 | SPARE | 43 | RETURN (pins 31, 32, 44, 54, 55) |
| 3 | +AGE CHAN MODE WRITE | 44 | -AGE DMA PROC 2 |
| 4 | +L AGE DATA B00 | 45 | +L AGE DATA B51 |
| 5 | +L AGE DATA B01 | 46 | +L AGE DATA B52 |
| 6 | +L AGE DATA B02 | 47 | +L AGE DATA B53 |
| 7 | SPARE | 48 | RETURN (pin 36) |
| 8 | +L AGE DATA B08 | 49 | -L AGE CP2 |
| 9 | RETURN (pins 3, 18, 10, 17) | 50 | RETURN (pin 49) |
| 10 | -AGE CHAN MODE INSTR | 51 | +L AGE DATA B21 |
| 11 | +L AGE DATA B03 | 52 | +L AGE DATA B22 |
| 12 | RETURN (pins 4, 5, 6, 11, 13, 19, 20, 21) | 53 | +L AGE DATA B23 |
| 13 | +L AGE DATA B04 | 54 | -AGE DMA PROC 3 |
| 14 | SPARE | 55 | -AGE DMA PROC 4 |
| 15 | +L AGE DATA B09 | 56 | -AGE PROC 0 |
| 16 | +L AGE DATA B10 | 57 | RETURN (pins 56, 58, 68, 69, 70) |
| 17 | -AGE CHAN MODE HW | 58 | -AGE PROC 1 |
| 18 | -AGE CHAN MODE DMA | 59 | +L AGE DATA B24 |
| 19 | +L AGE DATA B05 | 60 | +L AGE DATA B25 |
| 20 | +L AGE DATA B06 | 61 | +L AGE DATA B26 |
| 21 | +L AGE DATA B07 | 62 | +L AGE DATA B32 |
| 22 | SPARE | 63 | +L AGE DATA B33 |
| 23 | SPARE | 64 | +L AGE DATA B34 |
| 24 | +L AGE DATA B48 | 65 | +L AGE DATA B40 |
| 25 | +L AGE DATA B11 | 66 | +L AGE DATA B41 |
| 26 | RETURN (pins 8, 15, 16, 25, 27, 37, 38, 39) | 67 | +L AGE DATA B42 |
| 27 | +L AGE DATA B12 | 68 | -AGE PROC 2 |
| 28 | +L AGE DATA B16 | 69 | -AGE PROC 3 |
| 29 | +L AGE DATA B17 | 70 | -AGE PROC 4 |
| 30 | +L AGE DATA B18 | 71 | +L AGE DATA B27 |
| 31 | -AGE DMA PROC 0 | 72 | RETURN (pins 59, 60, 61, 71, 73, 82, 83, 84) |
| 32 | -AGE DMA PROC 1 | 73 | +L AGE DATA B28 |
| 33 | +L AGE DATA B49 | 74 | +L AGE DATA B35 |
| 34 | RETURN (pins 24, 33, 35, 45, 46, 47) | 75 | RETURN (pins 62, 63, 64, 74, 76, 85, 86, 87) |
| 35 | +L AGE DATA B50 | 76 | +L AGE DATA B36 |
| 36 | -AGE CP1 | 77 | +L AGE DATA B43 |
| 37 | +L AGE DATA B13 | 78 | RETURN (pins 65, 66, 67, 77, 79, 88, 89, 90) |
| 38 | +L AGE DATA B14 | 79 | +L AGE DATA B44 |
| 39 | +L AGE DATA B15 | 80 | +L AGE HS DATA BUS 28 |
| 40 | +L AGE DATA B19 | | |
| 41 | RETURN (pins 28, 29, 30, 40, 42, 51, 52, 53) | | |

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Table I. Connector/Signal List (Cont)

GPC Connector J2 - Connector Part No. MS27497T24F35PA

| GPC J2 Pin No. | Signal Name | GPC J2 Pin No. | Signal Name |
|-------------------|-------------------------------------|-------------------|-------------------------------------|
| 81 | +L AGE HS DATA BUS 29 | 106 | +L AGE HS DATA BUS 03 |
| 82 | +L AGE DATA B29 | 107 | +L AGE HS DATA BUS 08 |
| 83 | +L AGE DATA B30 | 108 | +L AGE HS DATA BUS 06 |
| 84 | +L AGE DATA B31 | 109 | +L AGE HS DATA BUS 07 |
| 85 | +L AGE DATA B37 | 110 | +L AGE HS DATA BUS 18 |
| 86 | +L AGE DATA B38 | 111 | RETURN (pins 100, 101, 110, 119) |
| 87 | +L AGE DATA B39 | 112 | +L AGE HS DATA BUS 24 |
| 88 | +L AGE DATA B45 | 113 | +L AGE HS DATA BUS 22 |
| 89 | +L AGE DATA B46 | 114 | +L AGE HS DATA BUS 23 |
| 90 | +L AGE DATA B47 | 115 | +L AGE HS DATA BUS 09 |
| 91 | +L AGE HS DATA BUS 30 | 116 | RETURN (pins 107, 115, 122, 123) |
| 92 | RETURN (pins 80, 81, 91, 93) | 117 | +L AGE HS DATA BUS 12 |
| 93 | +L AGE HS DATA BUS 31 | 118 | RETURN (pins 117, 124, 125, 126) |
| 94 | +L AGE HS DATA BUS 00 | 119 | +L AGE HS DATA BUS 19 |
| 95 | RETURN (pins 94, 96, 105, 106) | 120 | RETURN (pins 112, 121, 127, 128) |
| 96 | +L AGE HS DATA BUS 01 | 121 | +L AGE HS DATA BUS 25 |
| 97 | +L AGE HS DATA BUS 04 | 122 | +L AGE HS DATA BUS 10 |
| 98 | RETURN (pins 97, 99, 108, 109) | 123 | +L AGE HS DATA BUS 11 |
| 99 | +L AGE HS DATA BUS 05 | 124 | +L AGE HS DATA BUS 13 |
| 100 | +L AGE HS DATA BUS 16 | 125 | +L AGE HS DATA BUS 14 |
| 101 | +L AGE HS DATA BUS 17 | 126 | +L AGE HS DATA BUS 15 |
| 102 | +L AGE HS DATA BUS 20 | 127 | +L AGE HS DATA BUS 26 |
| 103 | RETURN (pins 102, 104, 113, 114) | 128 | +L AGE HS DATA BUS 27 |
| 104 | +L AGE HS DATA BUS 21 | | |
| 105 | +L AGE HS DATA BUS 02 | | |

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Table I. Connector/Signal List (Cont)

GPC Connector J3 - Connector Part No. MS27497T24F35P

| GPC J3 Pin No. | Signal Name | Function | GPC J3 Pin No. | Signal Name | Function |
|-------------------|----------------|------------------|-------------------|----------------|---------------------|
| 1 | DO14T | Discrete Out 14T | 45 | DO22T | Discrete Out 22T |
| 2 | DO14C | Discrete Out 14C | 46 | DO28T | Discrete Out 28T |
| 3 | DO15T | Discrete Out 15T | 47 | DO28C | Discrete Out 28C |
| 4 | DO16T | Discrete Out 16T | 48 | DO07C | Discrete Out 07C |
| 5 | DP17C | Discrete Out 17C | 49 | DO06T | Discrete Out 06T |
| 6 | DO18C | Discrete Out 18C | 50 | DO06C | Discrete Out 06C |
| 7 | DO19T | Discrete Out 19T | 51 | DO00T | Discrete Out 00T |
| 8 | DO12T | Discrete Out 12T | 52 | DO04C | Discrete Out 04C |
| 9 | DO15C | Discrete Out 15C | 53 | DO29C | Discrete Out 29C |
| 10 | DP16C | Discrete Out 16C | 54 | SPARE | SPARE 5C |
| 11 | DO17T | Discrete Out 17T | 55 | DO25C | Discrete Out 25C |
| 12 | DO18T | Discrete Out 18T | 56 | DO25T | Discrete Out 25T |
| 13 | DO19C | Discrete Out 19C | 57 | DO30C | GPC I.D. Source - C |
| 14 | DO21C | Discrete Out 21C | 58 | DO30T | GPC I.D. Source - T |
| 15 | DO10T | Discrete Out 10T | 59 | DO05T | Discrete Out 05T |
| 16 | DO12C | Discrete Out 12C | 60 | DO05C | Discrete Out 05C |
| 17 | DO13T | Discrete Out 13T | 61 | DO08C | Discrete Out 08C |
| 18 | DO01T | Discrete Out 01T | 62 | DO08T | Discrete Out 08T |
| 19 | DO03C | Discrete Out 03C | 63 | DO00C | Discrete Out 00C |
| 20 | DO27T | Discrete Out 27T | 64 | SPARE | Spare 7C |
| 21 | DO26T | Discrete Out 26T | 65 | SPARE | Spare 5T |
| 22 | DO21T | Discrete Out 21T | 66 | DI15T | Discrete In 15T |
| 23 | DO23C | Discrete Out 23C | 67 | DO31C | GPC-IPL-Indicator C |
| 24 | DO23T | Discrete Out 23T | 68 | DO31T | GPC-IPL-Indicator T |
| 25 | DO09T | Discrete Out 09T | 69 | DI17T | Discrete In 17T |
| 26 | DO10C | Discrete Out 10C | 70 | DI17C | Discrete In 17C |
| 27 | DO13C | Discrete Out 13C | 71 | SPARE | Spare 2C |
| 28 | DO02T | Discrete Out 02T | 72 | SPARE | Spare 1T |
| 29 | DO01C | Discrete Out 01C | 73 | SPARE | Spare 1C |
| 30 | DO03T | Discrete Out 03T | 74 | DI32T | Discrete In 32T |
| 31 | DO27C | Discrete Out 27C | 75 | DI32C | Discrete In 32C |
| 32 | DO26C | Discrete Out 26C | 76 | SPARE | Spare 7T |
| 33 | DO22C | Discrete Out 22C | 77 | DI15C | Discrete In 15C |
| 34 | DO24T | Discrete Out 24T | 78 | DI18C | Discrete In 18C |
| 35 | DO24C | Discrete Out 24C | 79 | DI18T | Discrete In 18T |
| 36 | DO07T | Discrete Out 07T | 80 | DI10T | Discrete In 20T |
| 37 | DO09C | Discrete Out 09C | 81 | DI19T | Discrete In 19T |
| 38 | DO11T | Discrete Out 11T | 82 | SPARE | Spare 2T |
| 39 | DO11C | Discrete Out 11C | 83 | DI39C | Discrete In 39C |
| 40 | DO02C | Discrete Out 02C | 84 | DI37C | Discrete In 37C |
| 41 | DO04T | Discrete Out 04T | 85 | DI37T | Discrete In 37T |
| 42 | DO29T | Discrete Out 29T | 86 | SPARE | Spare 3C |
| 43 | DO20C | Discrete Out 20C | 87 | SPARE | Spare 3T |
| 44 | DO20T | Discrete Out 20T | 88 | DI16C | Discrete In 16C |

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Table I. Connector/Signal List (Cont)

GPC Connector J3 - Connector Part No. MS27497T24F35P

| GPC J3 Pin No. | Signal Name | Function | GPC J3 Pin No. | Signal Name | Function |
|-------------------|----------------|--------------------------------|-------------------|----------------|------------------------------------|
| 89 | DI16T | Discrete In 16T | 109 | DI29C | Discrete In 29C |
| 90 | DI23T | Discrete In 23T | 110 | +5VDC | +5-Volt Source (control panels) |
| 91 | DI20C | Discrete In 20C | 111 | DI26T | Discrete In 26T |
| 92 | DI21T | Discrete In 21T | 112 | DI25C | Discrete In 25C |
| 93 | DI19C | Discrete In 19C | 113 | DI24T | Discrete In 24T |
| 94 | DI39T | Discrete In 39T | 114 | DI22T | Discrete In 22T |
| 95 | DI38T | Discrete In 38T | 115 | DI36C | Discrete In 36C |
| 96 | DI35T | Discrete In 35T | 116 | DI33T | Discrete In 33T |
| 97 | DI35C | Discrete In 35C | 117 | DI31C | Discrete In 31C |
| 98 | SPARE | Spare 6T | 118 | DI30T | Discrete In 30T |
| 99 | DI29T | Discrete In 29T | 119 | DI28C | Discrete In 28C |
| 100 | SIGRTN | Control Panel Signal Return | 120 | DI27T | Discrete In 27T |
| 101 | DI26C | Discrete In 26C | 121 | DI24C | Discrete In 24C |
| 102 | DI23C | Discrete In 23C | 122 | DI34T | Discrete In 34T |
| 103 | DI22C | Discrete In 22C | 123 | DI33C | Discrete In 33C |
| 104 | DI21C | Discrete In 21C | 124 | DI31T | Discrete In 31T |
| 105 | DI38C | Discrete In 38C | 125 | DI30C | Discrete In 30C |
| 106 | DI36T | Discrete In 36T | 126 | DI28T | Discrete In 28T |
| 107 | DI34C | Discrete In 34T | 127 | DI27C | Discrete In 27C |
| 108 | SPARE | Spare 6C | 128 | DI25T | Discrete In 25T |

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Table I. Connector/Signal List (Cont)

GPC Connector J4 - Connector Part No. MS27497T24F35PD

| GPC J4 Pin No. | Signal Name | GPC J4 Pin No. | Signal Name |
|-------------------|---|-------------------|----------------------------------|
| 1 | +L AGE Addr Exp 0 | 44 | -L AGE Scan Data In |
| 2 | +L AGE Addr Exp 1 | 45 | -L AGE Scan Out |
| 3 | +L AGE Addr Exp 2 | 46 | -L AGE Enable |
| 4 | +L AGE Address 00 | 47 | -L AGE RTCC DATA OUT |
| 5 | +L AGE Address 04 | 48 | +L AGE Use Branch Taken |
| 6 | +L AGE Address 05 | 49 | Return For J1-036, 037, 038, 048 |
| 7 | +L AGE Address 06 | 50 | -L AGE CPU Macro Stopped |
| 8 | +L AGE Addr Exp 3 | 51 | -L AGE CPU Halt |
| 9 | Return For J1-001, 002, 003, 008 | 52 | Return For J1-039, 040, 050, 051 |
| 10 | +L AGE Address 01 | 53 | -L AGE IO Chain Halted |
| 11 | +L AGE Address 02 | 54 | Return For J1-041, 042, 043, 053 |
| 12 | Return For J1-004, 010, 011, 020 | 55 | -L AGE Execute |
| 13 | +L AGE Address 07 | 56 | Return For J1-044, 045, 046, 055 |
| 14 | Return For J1-005, 006, 007, 013 | 57 | -L AGE RTCC Data In |
| 15 | +L AGE Address 08 | 58 | Return For J1-047, 057 |
| 16 | +L AGE Address 09 | 59 | -L AGE Busy |
| 17 | +L AGE Address 10 | 60 | Return For J1-059 |
| 18 | +L AGE Address 12 | 61 | -L AGE ADR Available |
| 19 | +L AGE Address 13 | 62 | Return For J1-061 |
| 20 | +L AGE Address 03 | 63 | +L AGE CSA Exp |
| 21 | -L AGE IU Ack | 64 | +L AGE PROM ADDR 01 |
| 22 | Return For J1-030, 031, 032, 021 | 65 | +L AGE PROM ADDR 02 |
| 23 | -L AGE AGE Ack | 66 | +L AGE PROM ADDR 04 |
| 24 | -L AGE Write | 67 | +L AGE PROM ADDR 05 |
| 25 | +L AGE Address 11 | 68 | +L AGE PROM ADDR 08 |
| 26 | Return For J1-015, 016, 017, 025 | 69 | +L AGE PROM ADDR 09 |
| 27 | +L AGE Address 14 | 70 | +L AGE PROM ADDR 10 |
| 28 | +L AGE Address 15 | 71 | -L AGE XIO Initiate |
| 29 | Return For J1-018, 019, 027, 028 | 72 | Return For J1-071 |
| 30 | -L AGE EA Ack | 73 | -L AGE MONO SEL |
| 31 | -L AGE EA Store Project Latched (software) | 74 | Return For J1-073 |
| 32 | -L AGE EU Ack | 75 | +L AGE Prom ADDR 03 |
| 33 | -L AGE FW | 76 | Return For J1-063, 064, 065, 075 |
| 34 | -L AGE IO ACK | 77 | +L AGE Prom Addr 06 |
| 35 | Return For J1-023, 024, 033, 034 | 78 | +L AGE Prom Addr 07 |
| 36 | -L AGE Purge Pipeline | 79 | Return For J1-066, 067, 077, 078 |
| 37 | +L AGE Update EX PC | 80 | +L AGE Prom Addr 11 |
| 38 | +L AGE Ex Inst Is 32 Bits | 81 | Return For J1-068, 069, 070, 080 |
| 39 | -L AGE CPU Is Stopped | 82 | -L AGE Master TO |
| 40 | +L AGE EA ENDOP | 83 | Return For J1-082 |
| 41 | -L AGE Force 1750 | 84 | -L AGE Continue |
| 42 | -L Use Logical Address | 85 | Return For J1-084 |
| 43 | -L AGE IO Chain Stop | 86 | -L AGE Reset |
| | | 87 | Return For J1-086 |
| | | 88 | -L AGE Attached |

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Table I. Connector/Signal List (Cont)

GPC Connector J4 - Connector Part No. MS27497T24F35PD

| GPC J4 Pin No. | Signal Name | GPC J4 Pin No. | Signal Name |
|-------------------|-----------------------|-------------------|---------------------------------------|
| 89 | Return For J1-088 | 103 | Return For J1-102 (Softwire From B08) |
| 90 | +L AGE CPU Micro Stop | 105 | -L AGE CS Clock |
| 91 | Return For J1-090 | 106 | Return For J1-105 (Softwire From B12) |
| 92 | -L AGE CPU Macro Stop | 107 | -L AGE CE Micro Stop |
| 93 | Return For J1-092 | 108 | Return For J1-107 (Softwire From B16) |
| 94 | -L AGE CPU Crash | 109 | AGE PS Test -5V |
| 95 | Return For J1-094 | 110 | AGE PS Test +28VDC |
| 96 | -L AGE Scan Clock | 111 | AGE PS Test +5VDC |
| 97 | Return For J1-096 | 112 | AGE PS Test +12V |
| 98 | -L AGE RTCC Clock | 113 | AGE PS Test +8V |
| 99 | Return For J1-098 | | |
| 100 | -L AGE CH Interrupt | | |
| 101 | Return For J1-100 | | |
| 102 | +L AGE Prom Addr 12 | | |

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Table I. Connector/Signal List (Cont)

GPC Connector J5 - Connector Part No. MS27497T24F35S

| GPC J5 Pin No. | Signal Name | Function | GPC J5 Pin No. | Signal Name | Function |
|-------------------|----------------|-----------------------|-------------------|----------------|-------------------------|
| 1 | DI00T | Halt Mode Cmd | 45 | DRO07C | GPC N+1 Fail Vote Out |
| 2 | DI00C | Halt Mode Cmd | 46 | DRO00T | GPC Fail Indicator |
| 3 | DI01T | Standby Mode Cmd | 47 | DRI04C | GPC N+2 Fail Vote In |
| 4 | DI01C | Standby Mode Cmd | 48 | ICB01T | Data Bus 01T |
| 5 | DI02T | Run Mode Cmd | 49 | ICB01C | Data Bus 01C |
| 6 | DI02C | Run Mode Cmd | 50 | SPARE | Spare |
| 7 | DI03T | GPC IPL Activate Cmd | 51 | ICB02T | Data Bus 02T |
| 8 | DI04T | MM1 IPL Select Cmd | 52 | ICB02C | Data Bus 02C |
| 9 | DI04C | MM1 IPL Select Cmd | 53 | ICB03T | Data Bus 03T |
| 10 | DI05T | MM2 IPL Select Cmd | 54 | ICB03C | Data Bus 03C |
| 11 | DI05C | MM2 IPL Select Cmd | 55 | SPARE | Spare |
| 12 | DI06T | MM1 Ready | 56 | ICB04T | Data Bus 04T |
| 13 | DI06C | MM1 Ready | 57 | ICB04C | Data Bus 04C |
| 14 | DI03C | GPC IPL Activate Cmd | 58 | DRO00C | GPC Fail Indicator |
| 15 | DI07T | MM2 Ready | 59 | ICB05T | Data Bus 05T |
| 16 | DI07C | MM2 Ready | 60 | ICB05C | Data Bus 05C |
| 17 | DI08T | Discrete In 08T | 61 | SPARE | Spare |
| 18 | DI08C | Discrete In 08C | 62 | ICB06T | Data Bus 06T |
| 19 | DI09T | Discrete In 09T | 63 | ICB06C | Data Bus 06C |
| 20 | DI09C | Discrete In 09C | 64 | ICB07T | Data Bus 07T |
| 21 | DI10T | Discrete In 10T | 65 | ICB07C | Data Bus 07C |
| 22 | DI10C | Discrete In 10C | 66 | SPARE | Spare |
| 23 | DI11T | Discrete In 11T | 67 | ICB08T | Data Bus 08T |
| 24 | DI11C | Discrete In 11C | 68 | ICB08C | Data Bus 08C |
| 25 | DI12T | I/O Terminate Cmd A | 69 | SPARE | Spare |
| 26 | DI12C | I/O Terminate Cmd A | 70 | SPARE | Spare |
| 27 | DI13T | I/O Terminate Cmd B | 71 | ICB09T | Data Bus 09T |
| 28 | DI13C | I/O Terminate Cmd B | 72 | ICB09C | Data Bus 09C |
| 29 | DI14T | Discrete In 14T | 73 | SPARE | Spare |
| 30 | DI14C | Discrete In 14C | 74 | ICB10T | Data Bus 10T (FC Bus 1) |
| 31 | DRI06T | GPC N+4 Fail Vote In | 75 | ICB10C | Data Bus 10C (FC Bus 1) |
| 32 | DRI06C | GPC N+4 Fail Vote In | 76 | ICB11T | Data Bus 11T (FC Bus 2) |
| 33 | DRI05T | GPC N+3 Fail Vote In | 77 | ICB11C | Data Bus 11C (FC Bus 2) |
| 34 | DRI05C | GPC N+3 Fail Vote In | 78 | SPARE | Spare |
| 35 | DRI04T | GPC N+2 Fail Vote In | 79 | ICB12T | Data Bus 12T (FC Bus 3) |
| 36 | DRI03T | GPC N+1 Fail Vote In | 80 | ICB12CD | Data Bus 12C (FC Bus 3) |
| 37 | DRI03C | GPC N+1 Fail Vote In | 81 | SPARE | Spare |
| 38 | DRO10T | GPC N+4 Fail Vote Out | 82 | ICB13T | Data Bus 13T (FC Bus 4) |
| 39 | DRO10C | GPC N+4 Fail Vote Out | 83 | ICB13C | Data Bus 13C (FC Bus 4) |
| 40 | DRO09T | GPC N+3 Fail Vote Out | 84 | SPARE | Spare |
| 41 | DRO09C | GPC N+3 Fail Vote Out | 85 | ICB14T | Data Bus 14T (FC Bus 5) |
| 42 | DRO08T | GPC N+2 Fail Vote Out | 86 | ICB14C | Data Bus 14C (FC Bus 5) |
| 43 | DRO08C | GPC N+2 Fail Vote Out | 87 | ICB15T | Data Bus 15T (FC Bus 6) |
| 44 | DRO07T | GPC N+1 Fail Vote Out | 88 | ICB15C | Data Bus 15C (FC Bus 6) |

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Table I. Connector/Signal List (Cont)

GPC Connector J5 - Connector Part No. MS27497T24F35S

| GPC J5 Pin No. | Signal Name | Function | GPC J5 Pin No. | Signal Name | Function |
|-------------------|----------------|-------------------------|-------------------|----------------|-------------------------|
| 89 | SPARE | Spare | 110 | ICB23T | Data Bus 23T (LB Bus 2) |
| 90 | ICB16T | Data Bus 16T (FC Bus 7) | 111 | ICB23C | Data Bus 23C (PL Bus 2) |
| 91 | ICB16C | Data Bus 16C (FC Bus 7) | 112 | SPARE | Spare |
| 92 | SPARE | Spare | 113 | ICB24T | Data Bus 24T |
| 93 | SPARE | Spare | 114 | ICB24C | Data Bus 24C |
| 94 | ICB17T | Data Bus 17T (FC Bus 8) | 115 | SPARE | Spare |
| 95 | ICB17C | Data Bus 17C (FC Bus 8) | 116 | SPARE | Spare |
| 96 | SPARE | Spare | 117 | SPARE | Spare |
| 97 | ICB18T | Data Bus 18T (MM Bus 1) | 118 | SPARE | Spare |
| 98 | ICB18C | Data Bus 18C (MM Bus 1) | 119 | SPARE | Spare |
| 99 | ICB19T | Data Bus 19T (MM Bus 2) | 120 | SPARE | Spare |
| 100 | ICB19C | Data Bus 19C (MM Bus 2) | 121 | SPARE | Spare |
| 101 | SPARE | Spare | 122 | SPARE | Spare |
| 102 | ICB20T | Data Bus 20T (PL Bus 1) | 123 | SPARE | Spare |
| 103 | ICB20C | Data Bus 20C (PL Bus 1) | 124 | SPARE | Spare |
| 104 | SPARE | Spare | 125 | SPARE | Spare |
| 105 | ICB21T | Data Bus 21T (PL Bus 2) | 126 | SPARE | Spare |
| 106 | ICB21C | Data Bus 21C (PL Bus 2) | 127 | SPARE | Spare |
| 107 | SPARE | Spare | 128 | SPARE | Spare |
| 108 | ICB22T | Data Bus 22T (LB Bus 1) | | | |
| 109 | ICB22C | Data Bus 22C (LB Bus 1) | | | |

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Table I. Connector/Signal List (Cont)

GPC Connector J7 - Connector Part No. MS3102R22-22P

| GPC J7 Pin No. | Signal Name | Function | GPC J7 Pin No. | Signal Name | Function |
|-------------------|----------------|---------------|-------------------|----------------|---------------|
| A | 28VP | +28 vdc Power | C | SGRND | Safety Ground |
| B | 28VH | 28 v Return | D | SNGRND | Signal Ground |

Connector Notes:

- J4 = Computer AGE connector
J2 IOP AGE connector
J3 Discrete Inputs and Outputs
J5 Discrete inputs/outputs, data bus, and RM discrete I/O
J7 Power
- C after signal name (i.e., XXP01C) is the complement side and T is the true side.
N after signal name indicates single-ended.

Special Notes:

GPC connector J5 data bus signal definition. When measuring the output at the J5 connector pins (for data bus outputs) the pin having a positive voltage during the first half of the sync field of a command word is designated high (true = T) and the other lead is designated low (complement = C).

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3.1.2.3.1.3.1.4 Differential Noise Voltage. The noise voltage experienced by the line receiver inputs shall be rejected when it is within the range of plus or minus 1.65 Vdc with 0 volt common-mode voltage and normal complimentary (one side grounded and the other side open) signal source. With 4.4 volts common-mode voltage, the differential noise rejection shall be plus or minus 1.25 Vdc complimentary (one side grounded and the other side open) signal source. The differential noise voltage is the voltage accumulated between signal lines and consists of ac and dc components superimposed on the signal waveform at any instant in time. The noise voltages are due to EMI, induced or conducted currents, or crosstalk. These voltages add algebraically in time at the receiver inputs and are in addition to the normal logic levels present.

3.1.2.3.1.3.1.5 Common Mode Voltage. The receiver shall detect logical zero and one-stage signals in the presence of superimposed common mode noise or interference signals up to plus or minus 5.25 volts peak with zero differential noise. Common mode voltage is defined as the difference between ground planes for the source and receiver.

3.1.2.3.1.3.1.6 Power Off/Open Connection Condition. When driver power is removed (power off) or the input to the receiver is open circuited, the output of the line receivers shall be in the logical zero state. The receivers shall meet the noise rejection requirements of paragraphs 3.1.2.3.1.3.1.4 and 3.1.2.3.1.3.1.5, except the differential rejection may degrade to plus or minus 1.25 Vdc. The line receivers shall not be electrically damaged when in the power-off state with a logical one or a logical zero applied to its input. Line receivers which are powered-off shall not load the input line to a greater extent than specified in 3.1.2.3.1.3.1.2 and shall not adversely affect input signal levels seen by other receivers on the same input line.

3.1.2.3.1.3.1.7 Short Circuit Protection. The receivers shall not be damaged when their inputs are shorted together or to signal ground for an indefinite period of time.

3.1.2.3.1.3.1.8 Input Protection. The line receiver shall not be permanently damaged when plus or minus 20 vdc referred to ground or 20 volts differential line to line is applied to its inputs.

3.1.2.3.1.4 Complementary Discrete Output Signals.

3.1.2.3.1.4.1 Line Drivers. The line drivers shall be of the complementary output type. The line driver shall transmit differential digital data over the transmission lines using a single plus five-volt supply.

3.1.2.3.1.4.2 Logical States. Voltage levels shall be determined by interfacing receiver(s). True side ON, complementary side OFF for logic 1 state, reversed for logic 0. ON means a low-impedance path is established to the GPC secondary power circuit common for positive sources. OFF means a low-impedance path is not established for positive sources.

3.1.2.3.1.4.3 Signal Rise and Fall Times. The line driver signal rise and fall times of the true and complementary outputs shall not exceed 600 nano-seconds with 30 picofarad load line-to-line, 100 picofarad line-to-ground and a 1 kilohm pullup resistor from each line to +12 Vdc.

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3.1.2.3.1.4.4 Line Driver Load. The driver shall be capable of sinking up to 30 milliamps and drop no more than +0.4 Vdc on either the true or complementary side for the ON condition and sinking 0.25 milliamps maximum at voltages up to +16.4 Vdc on either the true or complement side for the OFF condition. The driver fan out shall be a minimum of 6.5 equivalent loads under power-on conditions.

3.1.2.3.1.4.5 Data Skew. The line driver true and complementary output shall be within 300 nanoseconds of each other when measured at the 50-percentile points of each waveform with load as specified in paragraph 3.1.2.3.1.4.3.

3.1.2.3.1.4.6 Power-Off Condition. The output DC impedance of the line driver when power is removed shall not be less than 65.6 kilohms at +16.4 Vdc for the true or complement side.

3.1.2.3.1.4.7 Ringing. Overshoot and undershoot of the line driver output waveforms measured differentially shall be held to less than 20 percent of the nominal signal amplitudes under the load conditions specified in 3.1.2.3.1.4.3.

3.1.2.3.1.4.8 Short Circuit Protection. The line drivers shall not be damaged when their outputs are shorted to ground for an indefinite period of time.

3.1.2.3.1.5 Pull-Up Voltage Source. A voltage source connection shall be provided for sourcing input pull-ups of external receivers which interface with GPC discrete output drivers. This source shall be derived from internal power supplies and shall be referenced to secondary power/signal common. The source shall supply plus 5 Vdc nominal with no external load. Voltage supplied to an external load shall be no greater than plus 6.0 volts and not less than plus 4.0 volts under all combinations of power supply operating conditions and load currents within the load current range zero to 100 ma. The steady-state current demand on the source due to external loading will not exceed 50 ma in normal operation. The source shall be protected against external faults such that an external short circuit will not cause the plus 5-volt power supply to malfunction.

3.1.2.3.1.7 High Speed Output Drivers. The six output drivers referenced in paragraph 3.2.1.5.1.5 shall be capable of providing rise and fall times (10 percent to 90 percent points) of less than 26.5 microseconds while driving into 175 feet of cable having the characteristics of paragraph 3.1.2.3.1.1. The high-speed driver fanout shall be a maximum of 4.2 equivalent loads under power-on conditions.

3.1.2.4 Intra-LRU Discrete Circuits. Discrete circuits of the differential and single ended types shall be used for Intra-LRU discrete signals.

3.1.2.4.1 Deleted.

3.1.2.4.2 Single-ended Discrete Circuits (Intra-LRU).

3.1.2.4.2.1 Driver Circuit. The single-ended driver shall provide a discrete output signal having a logical one (1) state of 11.0 Vdc plus or minus 2.5 Vdc and a logical zero (0) state of 0.0 Vdc plus or minus 0.5 Vdc. The output shall be capable of supplying a minimum logical one state output current of 2 ma at a minimum level of 9.5 Vdc and shall be capable of sinking a minimum level of 9.5 Vdc and shall be capable of

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sinking a minimum current of 2 ma at a maximum level of 0.5 Vdc in the logical zero state. The reference return for the single-ended discrete output signal shall be the computer regulated dc signal ground. The driver-to-receiver signal return path between transmitting and receiving units shall be provided via the respective signal return connections to the system single-point ground.

3.1.2.4.3 Receiver Circuit. The receiver circuit for single-ended interface signals shall be an offset biased differential receiver. The reference input to the receiver circuit shall be 5.0 Vdc \pm 10 percent referenced to signal ground in the receiving unit. The receiver-to-driver signal return path between receiving and transmitting units shall be provided via the respective signal return connections to the system single-point ground. The receiver circuit shall be capable of withstanding a differential input signal magnitude or individual input-to-signal ground magnitudes of 20 Vdc. A differential input signal (input signal minus the local plus 5 Vdc reference voltage) of plus 0.5 Vdc to plus 15.5 Vdc shall be received as a logical one (1). A difference input signal of minus 0.5 Vdc to minus 5.5 Vdc shall be received as a logical zero (0). The maximum input currents shall be plus 1.9 ma and minus 1.9 ma at difference input signal levels of plus 8.0 Vdc and minus 5.5 Vdc, respectively.

3.1.2.5 Single Ended Discrete Drivers and Receivers.

3.1.2.5.1 Single Ended Driver. The GPC shall contain single-ended output drivers for interfacing with pilot panels and mass memory units.

3.1.2.5.2 Logical States. The single ended driver logical state shall be identical to 3.1.2.4.2.1.

3.1.2.5.3 Signal Rise and Fall Times. The line driver signal rise and fall times shall not exceed 1.0 μ sec.

3.1.2.5.4 Single Ended Receiver. The single ended receiver characteristics for interfacing with pilot panels and mass memory units shall be as specified in 3.1.2.4.3.

3.1.2.6 Multiplex Interface Adapter Requirements. The GPC multiplex interface adapter (MIA) shall:

- a. Function as the interface between the digital data bus and the GPC.
- b. Accept commands and data received on the data bus and route them to the GPC.
- c. Accept commands and data from the GPC and transmit them on the data bus.
- d. Provide for serial transmission of command and data over data bus channels.

3.1.2.6.1 MIA Definition. Each multiplex interface adapter shall consist of a pulse transformer, transmitter/receiver, encoder, decoder, integrated circuits and electronic components. The interface between the GPC and the above described MIA components shall be as specified in MC615-0010. There shall be two MIA's per carrier. The carrier shall be attached to a page frame by screws and nuts.

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3.1.2.6.2 MIA Interface Characteristics. The GPC electrical characteristics shall be compatible with the voltage, data rate, impedance, waveforms, and performance requirements of the data bus as specified in the multiplexer interface adapter specification MC615-0010.

3.1.3 Major Component Identification. The identification of the Baseline Computer Model shall be as follows:

| <u>Item</u> | <u>Buyer Control Number</u> | <u>Seller Part Number</u> | <u>Traceability Classification</u> |
|---------------------------------|-----------------------------|---------------------------|------------------------------------|
| Computer, General Purpose 03640 | MC615-0025-0200 | 6966000-2 | Serial |

3.1.4 Buyer Furnished Property. The MIA carrier as specified in MC615-0010 will be supplied by the buyer and shall be incorporated into the GPC.

3.2 Characteristics.

3.2.1 Performance. The computer shall perform the orbiter operational functions through a combination of automatic and flight crew commanded software sequences. Such sequences are to be stored in computer main memory. Control of the sequences and external subsystems is effected via command or data transfers controlled by the GPC.

3.2.1.1 Life Requirements. The GPC, excluding the battery pack, shall be designed to provide the most cost effective life capability, considering minimum maintenance and refurbishment as well as state-of-the-art hardware design. Battery life is defined in paragraph 3.1.2.1.11.

3.2.1.1.1 Operating Life. The GPC shall be capable of performing all operations specified herein for a minimum of 40,000 hours.

3.2.1.1.2 Useful Life. The GPC shall have a minimum useful life of 40,000 hours, which is greater than 100 orbital missions in a ten-year period from date of delivery. The average orbital mission will be seven days; however, the design shall not preclude the capability to extend the orbital staytime up to 30 days. Preventive maintenance, servicing, repair, and replacement of parts shall be consistent with the seller's trade-off results, as agreed to by the buyer.

3.2.1.1.3 Shelf Life. The GPC shall be capable of operating in accordance with the requirements specified herein any time within a period of ten years from date of delivery when exposed to the applicable environments of 3.2.5.

3.2.1.1.4 Reliability Goal. As a goal, the GPC shall be capable of reliability growth to greater than 6,000 hours MTBF under operational conditions.

3.2.1.2 Major Functions. The computer shall consist of the CPU, IOP, and memory major functions.

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3.2.1.2.1 Central Processing Unit (CPU). The CPU shall provide the central computational capability of the computer. It shall also effect, but not be limited to, the following:

- a. Program controlled input and output (PCI/PCO)
- b. Interrupt control and handling
- c. Clock synchronization and control
- d. Instruction set execution
- e. Intercomputer synchronization

3.2.1.2.2 Input/Output Processor (IOP) Function. The IOP shall provide central control and interface linkage between the memory and external avionics subsystems via one megahertz serial interface buses. It shall also effect, but not be limited to, the following:

- a. Direct memory access (DMA) to the memory on a cycle steal basis with the CPU and in a burst DMA mode
- b. Discrete input and output capability
- c. Data processing system redundancy management
- d. Interface control of buyer supplied MIA carrier

3.2.1.2.3 Self-Test. The computer shall provide for the self-detection of malfunctions in the CPU, memory, and IOP. The design of the processors shall include sufficient hardware capability in the form of built-in test equipment (BITE) to provide for rapid (on-line) fault information. The hardware BITE shall be such that with the aid of the proper self-test programs (STP), maximum fault coverage will exist. Use of microcode and special hardware to enhance fault detection shall be considered.

3.2.1.2.3.1 Fault Detection Capability. BITE and self-test modules shall detect and indicate faults such that failures or out-of-tolerance conditions in the computer will be detected. The computer, as defined here and shown in Figure 1, includes 262,144 words of memory, the CPU, the IOP, and the power supplies. All detected errors shall provide a positive indication that can be directly read by resident software.

3.2.1.2.3.2 Self-Test Programs. The self-test is capable of being executed independent of external or peripheral equipment.

3.2.1.2.3.3 Self-Test Microprograms. Micro-routines which perform tests of GPC logic and internal data paths shall be implemented to be callable by use of the special machine instruction, DIAGNOSE, in the CPU, and @ STP and # STP in the IOP. (Reference Tables VIII and X.) It shall be possible to execute CPU and IOP self-test micro-routines independently and concurrently. Test results shall be accessible to software. DIAGNOSE shall be a privileged CPU instruction which may be executed only in the supervisor state.

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3.2.1.3 Central Processing Unit (CPU) Design and Functions.

3.2.1.3.1 Performance. The CPU shall provide the capability of at least 1,000,000 full-word operations per second in fixed point. This figure of merit is derived by utilizing the average execution time for a mix of four SRS full-word adds to one SRS full-word multiply.

3.2.1.3.2 Data Words. The data words shall have the following characteristics:

- a. Fixed point word size
 - (1) Half-word - 15 bits minimum and sign
 - (2) Full-word - 31 bits minimum and sign

- b. Floating point word size

The CPU shall have full- and double-word capability in floating point. The characteristic exponent shall have a minimum of 8 bits. The mantissa shall have as a minimum 24 bits in full-word and 56 bits in double-word.

3.2.1.3.3 Instruction Words. The CPU shall be capable of executing an instruction word on either a half- or full-word mode for the fixed point operations as shown in Table IIA, CPU Instruction Set, and Table II B, MIL-STD-1750A Instruction Set.

3.2.1.3.4 Addressability. The computer shall be capable of addressing 524,288 half-words or 262,144 full-words.

3.2.1.3.5 Instruction Set. The instruction set shall include, but not be limited to, those instructions listed in Table IIA and IIB.

3.2.1.3.6 Interrupt Structure. The interrupt structure (Table III) shall consist of 60 interrupts organized into priority levels of five classes. The five classes of interrupts shall be as follows:

- a. Power
- b. Machine Check
- c. Program
- d. Supervisor Call
- e. External

Machine check and power interrupts, when they occur, shall not allow other interrupts to be taken. Interrupt structure and priorities shall be provided according to Table III.

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Table IIA. CPU Instruction Set

| <u>Fixed Point Operations</u> | <u>Format</u> |
|--|---------------|
| Add (AR) | RR |
| Add (A) | SRS |
| Add (A) | RS |
| Add Halfword (AHR) | RR |
| Add Halfword (AH) | SRS |
| Add Halfword (AH) | RS |
| Add Halfword Immediate (AHI) | RI |
| Add to Storage | RS |
| Compare (CR) | RR |
| Compare (C) | SRS |
| Compare (C) | RS |
| Compare Between Limits (CBL) | RR |
| Compare Halfword (CH) | SRS |
| Compare Halfword (CH) | RS |
| Compare Halfword Immediate (CHI) | RI |
| Compare Immediate With Storage (CIST) | SI |
| Divide (DR) | RR |
| Divide (D) | RS |
| Exchange Upper and Lower Halfwords (XUL) | RR |
| Insert Address Low (IAL) | SRS |
| Insert Address Low (IAL) | RS |
| Insert Halfword Low (IHL) | RS |
| Load (LR) | RR |
| Load (L) | SRS |
| Load (L) | RS |
| Load Address (LA) | SRS |
| Load Address (LA) | RS |
| Load Arithmetic Complement Halfword (LACR) | RR |
| Load Fixed Immediate (LFXI) | RR |
| Load Halfword (LH) | SRS |
| Load Halfword (LH) | RS |
| Load Multiple (LM) | RS |
| Modify Storage Halfword (MSTH) | SI |
| Multiply (MR) | RR |
| Multiply (M) | SRS |
| Multiply (M) | RS |
| Multiply Halfword (MH) | SRS |
| Multiply Halfword (MHR) | RR |
| Multiply Halfword (MH) | RS |
| Multiply Halfword Immediate (MHI) | RI |

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Table IIA. CPU Instruction Set (Cont)

| <u>Fixed Point Operations</u> | <u>Format</u> |
|-------------------------------|---------------|
| Store (ST) | SRS |
| Store (ST) | RS |
| Store Halfword (STH) | SRS |
| Store Halfword (STH) | RS |
| Store Multiple (STM) | RS |
| Subtract (SR) | RR |
| Subtract (S) | SRS |
| Subtract (S) | RS |
| Subtract From Storage (SST) | RS |
| Subtract Halfword (SHR) | RR |
| Subtract Halfword (SH) | SRS |
| Subtract Halfword (SH) | RS |
| Tally Down (TD) | SRS |
| Tally Down (TD) | RS |

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Table IIA. CPU Instruction Set (Cont)

| <u>Branch Operations</u> | <u>Format</u> |
|---|---------------|
| Branch and Index (BIX) | RS |
| Branch and Link (BALR) | RR |
| Branch and Link (BAL) | RS |
| Branch on Condition (BCR) | RR |
| Branch on Condition (BC) | RS |
| Branch on Condition Backward (BCB) | SRS |
| Branch on Condition Extended (BCRE) | RR |
| Branch on Condition Forward (BCF) | SRS |
| Branch on Count (BCTR) | RR |
| Branch on Count (BCT) | RS |
| Branch on Count Backward (BCTB) | SRS |
| Branch on Overflow and Carry (BVCR) | RR |
| Branch on Overflow and Carry (BVC) | RS |
| Branch on Overflow and Carry Forward (BVCF) | SRS |

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Table IIA. CPU Instruction Set (Cont)

| <u>Shift Operations</u> | <u>Format</u> |
|--------------------------------------|---------------|
| Normalize and Count (NCTR) | RR |
| Shift Left Double Arithmetic (SRDA) | SRS |
| Shift Left Double Logical (SLDL) | SRS |
| Shift Left Logical (SLL) | SRS |
| Shift Right and Rotate (SRR) | SRS |
| Shift Right Double and Rotate (SRDR) | SRS |
| Shift Right Double Logical (SRDL) | SRS |
| Shift Right Arithmetic (SRA) | SRS |
| Shift Right Logical (SRL) | SRS |

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Table IIA. CPU Instruction Set (Cont)

| <u>Logical Operations</u> | <u>Format</u> |
|--|---------------|
| And (NR) | RR |
| And (N) | SRS |
| And (N) | RS |
| And Halfword Immediate (NHI) | RI |
| And Immediate With Storage (NIST) | SI |
| And To Storage (NST) | RS |
| Exclusive Or (XR) | RR |
| Exclusive Or (X) | SRS |
| Exclusive Or (X) | RS |
| Exclusive Or Halfword Immediate (XHI) | RI |
| Exclusive Or Immediate With Storage (XIST) | SI |
| Exclusive Or To Storage (XST) | RS |
| Or (OR) | RR |
| Or (O) | SRS |
| Or (O) | RS |
| Or Halfword Immediate (OHI) | RI |
| Or To Storage (OST) | RS |
| Search Under Mask (SUM) | RR |
| Set Bits (SB) | SI |
| Set Halfword (SHV) | SRS |
| Set Halfword (SHW) | RS |
| Test Bits (TB) | SI |
| Test Halfword (TH) | SRS |
| Test Halfword (TB) | RS |
| Test Register Bits (TRB) | RI |
| Zero Bits (ZB) | SI |
| Zero Halfword (ZH) | SRS |
| Zero Halfword (ZH) | RS |
| Zero Register Bits (ZRB) | RI |

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Table IIA. CPU Instruction Set (Cont)

| <u>Floating Point Operations</u> | <u>Format</u> |
|---|---------------|
| Add (Long Operands) (AEDR) | RR |
| Add (Long Operands) (AED) | RS |
| Add (Short Operands) (AER) | RR |
| Add (Short Operands) (AE) | SRS |
| Add (Short Operands) (AE) | RS |
| Compare (Short Operands) (CER) | RR |
| Compare (Short Operands) (CE) | SRS, RS |
| Convert to Fixed Point (CVFX) | RR |
| Convert to Floating Point (CVFL) | RR |
| Divide (Long Operands) (DEDR) | RR |
| Divide (Long Operands) (DED) | RS |
| Divide (Short Operands) (DER) | RR |
| Divide (Short Operands) (DE) | RS |
| Load (Long Operands) (LED) | RS |
| Load (Short Operands) (LER) | RR |
| Load (Short Operands) (LE) | SRS |
| Load (Short Operands) (LE) | RS |
| Load Complement (Short Operands) (LECR) | RR |
| Load Fixed Register (LFXR) | RR |
| Load Floating Immediate (LFLI) | RR |
| Load Floating Register (LFLR) | RR |
| Mid Value Select (Short Operands) (MVS) | RS |
| Multiply (Long Operands) (MEDR) | RR |
| Multiply (Long Operands) (MED) | RS |
| Multiply (Short Operands) (MER) | RR |
| Multiply (Short Operands) (ME) | SRS, RS |
| Subtract (Long Operands) (SEDR) | RR |
| Subtract (Long Operands) (SED) | RS |
| Subtract (Short Operands) (SER) | RR |
| Subtract (Short Operands) (SE) | SRS |
| Subtract (Short Operands) (SE) | RS |
| Store (Long Operands) (STED) | RS |
| Store (Short Operands) (STE) | SRS |
| Store (Short Operands) (STE) | RS |

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Table IIA. CPU Instruction Set (Cont)

| <u>Special Operations</u> | <u>Format</u> |
|--|---------------|
| Diagnose (P) (DIAG) | RS |
| Insert Storage Protect Bits (P) (ISPB) | RS |
| Load DSE Multiple (LDM) | RS |
| Load Extended Address (LXA) | RR, RS |
| Load Program Status Word (P) (LPS) | RS |
| Move Halfword Operands (MVH) | RR |
| Set Program Mask (SPM) | RR |
| Set System Mask (P) (SSM) | RS |
| Stack Call (SCALL) | RS |
| Stack Return (SRTN) | RR |
| Store DSE Multiple (STDM) | RS |
| Store Extended Address (STXA) | RR, RS |
| Supervisor Call (SVC) | RS |
| Test and Set (TS) | RS |
| Test and Set Bits (TSB) | SI |

| <u>I/O Operations</u> | <u>Format</u> |
|---|---------------|
| <i>Program</i> Program Controlled Input/Output Instruction (PCIO) | RR |

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Table IIA. CPU Instruction Set (Cont)

Internal Control Register Operations (ICR)

| <u>Designate</u> | <u>Function</u> | <u>Read/ Write</u> | <u>MMP Code</u> | <u>IIO Code</u> | <u>Format</u> |
|------------------|---|------------------------|---------------------|---------------------|---------------|
| TI(02) | Load Counter 0 | W | 8801 | - | RR |
| TI(02) | Start Counter 0 | W | 8802 | - | RR |
| TI(02) | Stop Counter 0 | W | 8803 | - | RR |
| TI(02) | Load Counter 1 | W | 8804 | - | RR |
| TI(02) | Start Counter 1 | W | 880A | - | RR |
| TI(02) | Stop Counter 1 | W | 880B | - | RR |
| TI(02) | Read Counters | R | 0802 | - | RR |
| TI(02) | Read Counters | R | 0803 | - | RR |
| Age and CPU | Read Age | R | 04XX | - | RR |
| Age and CPU | Load Age | W | 86XX | - | RR |
| Age and CPU | Direct Age | W | 84XX | - | RR |
| Age and CPU | Age Mode Control | W | 87XX | - | RR |
| MMU | Load DSE Register | W | - | 9404 | RR |
| MMU | Read DSE Register | R | - | 9405 | RR |
| MMU | Read Even Physical ADOR Reg 00-15 | R | - | 1400 | RR |
| MMU | Read Logical ADOR Reg 00-15 | R | - | 1405 | RR |
| MMU | Read BSR/DSR/BSV/DSV | R | - | 1406 | RR |
| MMU | Read and Clear MFER (Do Not Clear Code Parity) | R | 1408 | - | RR |
| MMU | Read MMU Store Protect Reg 00-10 | R | - | 1409 | RR |
| MMU | Read MMU Mode Reg 00-07 | R | - | 1408 | RR |
| MMU | Read MMU Misc Reg 00-08 | R | 140A | - | RR |
| MMU | Read EOAC ADOR Reg 00-13 | R | 140F | - | RR |
| MMU | Load MMU SP Reg 00-02 (CPU) | W | - | 9400 | RR |
| MMU | Load All EDAC Diagnostic Latches | W | - | 9403 | RR |
| MMU and IRPT | Load BSR/OSR | W | - | 9009 | RR |
| MMU | Load MMU Mode Reg 00-07 | W | - | 9407 | RR |
| MMU | Set 1750 Block Protect and E/W Override | W | - | 940A | RR |
| MMU | Clear 1750 Block Protect and E/W Override | W | - | 940B | RR |
| MMU | Hoop to MMU | W | - | 940I | RR |
| MMU | Load BSV/OSV | W | - | 9406 | RR |
| MMU | Read MFER and Clear Code Parity Error | R | 140C | - | RR |
| MMU | Clear Soft Error Counter | W | 140E | - | RR |

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Table IIA. CPU Instruction Set (Cont)

Internal Control Register Operations (ICR)

| <u>Designate</u> | <u>Function</u> | <u>Read/ Write</u> | <u>MMP Code</u> | <u>IIO Code</u> | <u>Format</u> |
|------------------|--------------------------------------|------------------------|---------------------|---------------------|---------------|
| IRPT | Set Program Mask | W | - | - /9017 | RR |
| IRPT | CPU EA Fault (Machine Check) Command | W | - | 9000/9001 | RR |
| IRPT | CPU Illegal Operation Command | W | - | 9002/9003 | RR |
| IRPT | CPU Privileged Instruction Command | W | - | 9004/9005 | RR |
| IRPT | CPU FP Divide by Zero Command | W | - | - /9006 | RR |
| IRPT | CPU Significance Command | W | - | - /9007 | RR |
| IRPT | CPU Convert Overflow Command | W | - | - /9008 | RR |
| IRPT and MMU | Load PSW Segment 16-31 | W | - | - /9009 | RR |
| IRPT | Load PSW Segment 32-47 | W | - | - /900A | RR |
| IRPT | Set All MMP Pending Interrupts | W | - | - /900B | RR |
| IRPT | Reset All MMP Pending Interrupts | W | - | - /900C | RR |
| IRPT | DMA Store Protect | W | - | - /900D | RR |
| IRPT | Reset Complete | W | - | 900E/900F | RR |
| IRPT | Supervisor Call | W | - | 9010/ - | RR |
| IRPT | Start 2901/2910 Self Test | W | - | 9011/9011 | RR |
| IRPT | Start Bad Parity Test | W | - | 9011/9011 | RR |
| IRPT | Start Capture Reg Test | W | - | 9011/9011 | RR |
| IRPT | Start Priority PLA Test | W | - | 9011/9011 | RR |
| IRPT | Start Command PLA Test | W | - | 9011/9011 | RR |
| IRPT | Start Arithmetic Interrupt Test | W | - | 9012/9012 | RR |
| IRPT | Set/Reset Diagnose Mode | W | - | 9013/9013 | RR |
| IRPT | Start Interrupt Priority Test | W | - | 9014/9014 | RR |
| IRPT | Start EA Scan | W | - | 9015/9015 | RR |
| IRPT | Write 1750 Fault Reg (Byte Field) | W | - | 9016/9016 | RR |
| IRPT | Echo HBus | R | - | 1000/1000 | RR |
| IRPT | Read Diagnose | R | - | 1001/1001 | RR |
| IRPT | Read ISW | R | - | 9018/9018 | RR |
| IRPT | Read Local Store Reg | R | - | 1002/1002 | |
| PCI | Program-Controlled Input | R | A000 | - | RR |
| PCO | Program-Controlled Output | W | A400 | - | RR |

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Table IIB. MIL-STD-1750A Instruction Set

Instruction Codings

| <u>OPCODE</u> | <u>OCX</u> | <u>Instruction</u> | <u>Mnemonic</u> | <u>Address Mode</u> |
|---------------|------------|--|-----------------|---------------------|
| 0000 0000 | | Single Precision Load | LB | B (BR=12) |
| 0000 0001 | | Single Precision Load | LB | B (BR=13) |
| 0000 0010 | | Single Precision Load | LB | B (BR=14) |
| 0000 0011 | | Single Precision Load | LB | B (BR=15) |
| 0000 0100 | | Double Precision Load | DLB | B (BR=12) |
| 0000 0101 | | Double Precision Load | DLB | B (BR=13) |
| 0000 0110 | | Double Precision Load | DLB | B (BR=14) |
| 0000 0111 | | Double Precision Load | DLB | B (BR=15) |
| 0000 1000 | | Single Precision Store | STB | B (BR=12) |
| 0000 1001 | | Single Precision Store | STB | B (BR=13) |
| 0000 1010 | | Single Precision Store | STB | B (BR=14) |
| 0000 1011 | | Single Precision Store | STB | B (BR=15) |
| 0000 1100 | | Double Precision Store | DSTB | B (BR=12) |
| 0000 1101 | | Double Precision Store | DSTB | B (BR=13) |
| 0000 1110 | | Double Precision Store | DSTB | B (BR=14) |
| 0000 1111 | | Double Precision Store | DSTB | B (BR=15) |
| 0001 0000 | | Single Precision Integer Add | AB | B (BR=12) |
| 0001 0001 | | Single Precision Integer Add | AB | B (BR=13) |
| 0001 0010 | | Single Precision Integer Add | AB | B (BR=14) |
| 0001 0011 | | Single Precision Integer Add | AB | B (BR=15) |
| 0001 0100 | | Single Precision Integer Subtract | SBB | B (BR=12) |
| 0001 0101 | | Single Precision Integer Subtract | SBB | B (BR=13) |
| 0001 0110 | | Single Precision Integer Subtract | SBB | B (BR=14) |
| 0001 0111 | | Single Precision Integer Subtract | SBB | B (BR=15) |
| 0001 1000 | | Single Precision Multiply With 32-Bit Product | MB | B (BR=12) |
| 0001 1001 | | Single Precision Multiply With 32-Bit Product | MB | B (BR=13) |
| 0001 1010 | | Single Precision Multiply With 32-Bit Product | MB | B (BR=14) |
| 0001 1011 | | Single Precision Multiply With 32-Bit Product | MB | B (BR=15) |
| 0001 1100 | | Single Precision Integer Divide With 32-Bit Dividend | DB | B (BR=12) |
| 0001 1101 | | Single Precision Integer Divide With 32-Bit Dividend | DB | B (BR=13) |
| 0001 1110 | | Single Precision Integer Divide With 32-Bit Dividend | DB | B (BR=14) |
| 0001 1111 | | Single Precision Integer Divide With 32-Bit Dividend | DB | B (BR=15) |

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Table IIB. MIL-STD-1750A Instruction Set (Cont)

Instruction Codings

| <u>OPCODE</u> | <u>OCX</u> | <u>Instruction</u> | <u>Mnemonic</u> | <u>Address Mode</u> |
|---------------|------------|--------------------------|-----------------|---------------------|
| 0010 0000 | | Floating Point Add | FAB | B (BR=12) |
| 0010 0001 | | Floating Point Add | FAP | B (BR=13) |
| 0010 0010 | | Floating Point Add | FAB | B (BR=14) |
| 0010 0011 | | Floating Point Add | FAB | B (BR=15) |
| 0010 0100 | | Floating Point Subtract | FSB | B (BR=12) |
| 0010 0101 | | Floating Point Subtract | FSB | B (BR=13) |
| 0010 0110 | | Floating Point Subtract | FSB | B (BR=14) |
| 0010 0111 | | Floating Point Subtract | FSB | B (BR=15) |
| 0010 1000 | | Floating Point Multiply | FMB | B (BR=12) |
| 0010 1001 | | Floating Point Multiply | FMB | B (BR=13) |
| 0010 1010 | | Floating Point Multiply | FMB | B (BR=14) |
| 0010 1011 | | Floating Point Multiply | FMB | B (BR=15) |
| 0010 1100 | | Floating Point Divide | FDB | B (BR=12) |
| 0010 1101 | | Floating Point Divide | FDB | B (BR=13) |
| 0010 1110 | | Floating Point Divide | FDB | B (BR=14) |
| 0010 1111 | | Floating Point Divide | FDB | B (BR=15) |
| 0010 0000 | | Inclusive Logical or | ORB | B (BR=12) |
| 0011 0001 | | Inclusive Logical or | ORB | B (BR=13) |
| 0011 0010 | | Inclusive Logical or | ORB | B (BR=14) |
| 0011 0011 | | Inclusive Logical or | ORB | B (BR=15) |
| 0011 0100 | | Logical and | ANDB | B (BR=12) |
| 0011 0101 | | Logical and | ANDB | B (BR=13) |
| 0011 0110 | | Logical and | ANDB | B (BR=14) |
| 0011 0111 | | Logical and | ANDB | B (BR=15) |
| 0011 1000 | | Single Precision Compare | CB | B (BR=12) |
| 0011 1001 | | Single Precision Compare | CB | B (BR=13) |
| 0011 1010 | | Single Precision Compare | CB | B (BR=14) |
| 0011 1011 | | Single Precision Compare | CB | B (BR=15) |
| 0011 1100 | | Floating Point Compare | FCB | B (BR=12) |
| 0011 1101 | | Floating Point Compare | FCB | B (BR=13) |
| 0011 1110 | | Floating Point Compare | FCB | B (BR=14) |
| 0011 1111 | | Floating Point Compare | FCB | B (BR=15) |
| 0100 000 | 0000 | Single Precision Load | LBX | BX (BR=12) |
| 0100 0001 | 0000 | Single Precision Load | LBX | BX (BR=13) |
| 0100 0010 | 0000 | Single Precision Load | LBX | BX (BR=14) |
| 0100 0011 | 0000 | Single Precision Load | LBX | BX (BR=15) |
| 0100 0000 | 0001 | Double Precision Load | DLBX | BX (BR=12) |
| 0100 0001 | 0001 | Double Precision Load | DLBX | BX (BR=13) |
| 0100 0010 | 0001 | Double Precision Load | DLBX | BX (BR=14) |
| 0100 0011 | 0001 | Double Precision Load | DLBX | BX (BR=15) |
| 0100 0000 | 0010 | Single Precision Store | STBX | BX (BR=12) |
| 0100 0001 | 0010 | Single Precision Store | STBX | BX (BR=13) |
| 0100 0010 | 0010 | Single Precision Store | STBX | BX (BR=14) |
| 0100 0011 | 0010 | Single Precision Store | STBX | BX (BR=15) |
| 0100 0000 | 0011 | Double Precision Store | DSTX | BX (BR=12) |

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Table IIB. MIL-STD-1750A Instruction Set (Cont)

Instruction Coding

| <u>OPCODE</u> | <u>OCX</u> | <u>Instruction</u> | <u>Mnemonic</u> | <u>Address Mode</u> |
|---------------|------------|--|-----------------|---------------------|
| 0100 0001 | 0011 | Double Precision Store | DSTX | BX (BR=13) |
| 0100 0010 | 0011 | Double Precision Store | DSTX | BX (BR=14) |
| 0100 0011 | 0011 | Double Precision Store | DSTX | BX (BR=15) |
| 0100 0000 | 0100 | Single Precision Integer Add | ABX | BX (BR=12) |
| 0100 0001 | 0100 | Single Precision Integer Add | ABX | BX (BR=13) |
| 0100 0010 | 0100 | Single Precision Integer Add | ABX | BX (BR=14) |
| 0100 0011 | 0100 | Single Precision Integer Add | ABX | BX (BR=15) |
| 0100 0000 | 0101 | Single Precision Integer Subtract | SBBX | BX (BR=12) |
| 0100 0001 | 0101 | Single Precision Integer Subtract | SBBX | BX (BR=13) |
| 0100 0010 | 0101 | Single Precision Integer Subtract | SBBX | BX (BR=14) |
| 0100 0011 | 0101 | Single Precision Integer Subtract | SBBX | BX (BR=15) |
| 0100 0000 | 0110 | Single Precision Integer Multiply With 32-Bit Product | MBX | BX (BR=12) |
| 0100 0001 | 0110 | Single Precision Integer Multiply With 32-Bit Product | MBX | BX (BR=13) |
| 0100 0010 | 0110 | Single Precision Integer Multiply With 32-Bit Product | MBX | BX (BR=14) |
| 0100 0011 | 0110 | Single Precision Integer Multiply With 32-Bit Product | MBX | BX (BR=15) |
| 0100 0000 | 0111 | Single Precision Integer Divide With 32-Bit Dividend | DBX | BX (BR=12) |
| 0100 0001 | 0111 | Single Precision Integer Divide With 32-Bit Dividend | DBX | BX (BR=13) |
| 0100 0010 | 0111 | Single Precision Integer Divide With 32-Bit Dividend | DBX | BX (BR=14) |
| 0100 0011 | 0111 | Single Precision Integer Divide With 32-Bit Dividend | DBX | BX (BR=15) |
| 0100 0000 | 1000 | Floating Point Add | FABX | BX (BR=12) |
| 0100 0001 | 1000 | Floating Point Add | FABX | BX (BR=13) |
| 0100 0010 | 1000 | Floating Point Add | FABX | BX (BR=14) |
| 0100 0011 | 1000 | Floating Point Add | FABX | BX (BR=15) |
| 0100 0000 | 1001 | Floating Point Subtract | FSBX | BX (BR=12) |
| 0100 0001 | 1001 | Floating Point Subtract | FSBX | BX (BR=13) |
| 0100 0010 | 1001 | Floating Point Subtract | FSBX | BX (BR=14) |
| 0100 0011 | 1001 | Floating Point Subtract | FSBX | BX (BR=15) |
| 0100 0000 | 1010 | Floating Point Multiply | FMBX | BX (BR=12) |
| 0100 0001 | 1010 | Floating Point Multiply | FMBX | BX (BR=13) |
| 0100 0010 | 1010 | Floating Point Multiply | FMBX | BX (BR=14) |
| 0100 0011 | 1010 | Floating Point Multiply | FMBX | BX (BR=15) |
| 0100 0000 | 1011 | Floating Point Divide | FDBX | BX (BR=12) |
| 0100 0001 | 1011 | Floating Point Divide | FDBX | BX (BR=13) |
| 0100 0010 | 1011 | Floating Point Divide | FDBX | BX (BR=14) |

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Table IIB. MIL-STD-1750A Instruction Set (Cont)

Instruction Codings

| <u>OPCODE</u> | <u>OCX</u> | <u>Instruction</u> | <u>Mnemonic</u> | <u>Address Mode</u> |
|---------------|------------|---|-----------------|---------------------|
| 0100 0011 | 1011 | Floating Point Divide | FDBX | BX (BR-15) |
| 0100 0000 | 1100 | Single Precision Compare | CBX | BX (BR-12) |
| 0100 0001 | 1100 | Single Precision Compare | CBX | BX (BR-13) |
| 0100 0010 | 1100 | Single Precision Compare | CBX | BX (BR-14) |
| 0100 0011 | 1100 | Single Precision Compare | CBX | BX (BR-15) |
| 0100 0000 | 1101 | Floating Point Compare | FCBX | BX (BR-12) |
| 0100 0001 | 1101 | Floating Point Compare | FCBX | BX (BR-13) |
| 0100 0010 | 1101 | Floating Point Compare | FCBX | BX (BR-14) |
| 0100 0011 | 1101 | Floating Point Compare | FCBX | BX (BR-15) |
| 0100 0000 | 1110 | Logical and | ANDX | BX (BR-12) |
| 0100 0001 | 1110 | Logical and | ANDX | BX (BR-13) |
| 0100 0010 | 1110 | Logical and | ANDX | BX (BR-14) |
| 0100 0011 | 1110 | Logical and | ANDX | BX (BR-15) |
| 0100 0000 | 1111 | Inclusive Logical or | ORBX | BX (BR-12) |
| 0100 0001 | 1111 | Inclusive Logical or | ORBX | BX (BR-13) |
| 0100 0010 | 1111 | Inclusive Logical or | ORBX | BX (BR-14) |
| 0100 0011 | 1111 | Inclusive Logical or | ORBX | BX (BR-15) |
| 0100 1000 | | Execute Input/Output | XIO | IM, IMX |
| 0100 1001 | | Vectored Input/Output | VIO | IM, IMX |
| 0100 1010 | 0001 | Single Precision Integer Add | AIM | IM |
| 0100 1010 | 0010 | Single Precision Integer Subtract | SIM | IM |
| 0100 1010 | 0011 | Single Precision Integer Multiply With 32-Bit Product | MIM | IM |
| 0100 1010 | 0100 | Single Precision Integer Multiply With 16-Bit Product | MSIM | IM |
| 0100 1010 | 0101 | Single Precision Integer Divide With 32-Bit Dividend | DIM | IM |
| 0100 1010 | 0110 | Single Precision Integer Divide With 16-Bit Dividend | DVIM | IM |
| 0100 1010 | 0111 | Logical and | ANDM | IM |
| 0100 1010 | 1001 | Inclusive Logical or | ORIM | IM |
| 0100 1010 | 1001 | Exclusive Logical or | XORM | IM |
| 0100 1010 | 1010 | Single Precision Compare | CIM | IM |
| 0100 1010 | 1011 | Logical and | NIM | IM |
| 0101 0000 | | Set Bit | SB | D, DX |
| 0101 0001 | | Set Bit | SBR | R |
| 0101 0010 | | Set Bit | SBI | I, IX |
| 0101 0011 | | Reset Bit | RB | D, DX |
| 0101 0100 | | Reset Bit | RBR | R |
| 0101 0101 | | Reset Bit | RBI | I, IX |
| 0101 0110 | | Test Bit | TB | D, DX |
| 0101 0111 | | Test Bit | TBR | R |
| 0101 1000 | | Test Bit | TBI | I, IX |
| 0101 1001 | | Test and Set Bit | TSB | D, DX |
| 0101 1010 | | Set Variable Bit in Register | SVBR | R |

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Table IIB. MIL-STD-1750A Instruction Set (Cont)

Instruction Codings

| <u>OPCODE</u> | <u>OCX</u> | <u>Instruction</u> | <u>Mnemonic</u> | <u>Address Mode</u> |
|---------------|------------|--|-----------------|---------------------|
| 0101 1100 | | Reset Variable Bit in Register | RVBR | R |
| 0101 1110 | | Test Variable Bit in Register | TVBR | R |
| 0110 0000 | | Shift Left Logical | SLL | R |
| 0110 0001 | | Shift Right Logical | SRL | R |
| 0110 0010 | | Shift Right Arithmetic | SRA | R |
| 0110 011 | | Shift Left Cyclic | SLC | R |
| 0110 0101 | | Double Shift Left Logical | DSLL | R |
| 0110 0110 | | Double Shift Right Logical | DSRL | R |
| 0110 0111 | | Double Shift Right Arithmetic | DSRA | R |
| 0110 1000 | | Double Shift Left Cyclic | DSLCL | R |
| 0110 1010 | | Shift Left Logical, Count in Register | SLR | R |
| 0110 1011 | | Shift Arithmetic, Count in Register | SAR | R |
| 0110 1100 | | Shift Cyclic, Count in Register | SCR | R |
| 0110 1101 | | Double Shift Logical, Count in Register | DSLRL | R |
| 0110 1110 | | Double Shift Arithmetic, Count in Register | DSAR | R |
| 0110 1111 | | Double Shift Cyclic, Count in Register | DSCR | R |
| 0111 0000 | | Jump on Condition | JC | D, DX |
| 0111 0001 | | Jump on Condition | JCI | I, IX |
| 0111 0010 | | Jump to Subroutine | JS | D, DX |
| 0111 0011 | | Subtract One and Jump | SOJ | D, DX |
| 0111 0100 | | Branch Unconditionally | BR | ICR |
| 0111 0101 | | Branch if Equal to (Zero) | BEZ | ICR |
| 0111 0110 | | Branch if Less Than (Zero) | BLT | ICR |
| 0111 0111 | | Branch to Execute | BEX | S |
| 0111 1000 | | Branch if Less Than or Equal to (Zero) | BLE | ICR |
| 0111 1001 | | Branch if Greater Than (Zero) | BGT | ICR |
| 0111 1010 | | Branch if Not Equal to (Zero) | BNZ | ICR |
| 0111 1011 | | Branch if Greater Than or Equal to (Zero) | BGE | ICR |
| 0111 1100 | | Load Status | LSTI | D, DX |
| 0111 1101 | | Load Status | LST | D, DX |
| 0111 1110 | | Stack IC and Jump to Subroutine | SJS | D, DX |
| 0111 1111 | | Unstack IC and Return From Subroutine | URS | S |
| 1000 0000 | | Single Precision Load | L | C, DX |
| 1000 0001 | | Single Precision Load | LR | R |
| 1000 0010 | | Single Precision Load | LISP | ISP |

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Table IIB. MIL-STD-1750A Instruction Set (Cont)

Instruction Codings

| <u>OPCODE</u> | <u>OCX</u> | <u>Instruction</u> | <u>Mnemonic</u> | <u>Address Mode</u> |
|---------------|------------|--|-----------------|---------------------|
| 1000 0011 | | Single Precision Load | LISN | ISN |
| 1000 0100 | | Single Precision Load | LI | I, IX |
| 1000 0101 | | Single Precision Load | LIM | IM, IMX |
| 1000 0110 | | Double Precision Load | DL | D, DX |
| 1000 0111 | | Double Precision Load | DLR | R |
| 1000 1000 | | Double Precision Load | DLI | I, IX |
| 1000 1001 | | Load Multiple Registers | LM | D, DX |
| 1000 1010 | | Extended Precision Floating Point Load | EFL | D, DX |
| 1000 1011 | | Load From Upper Byte | LUB | D, DX |
| 1000 1100 | | Load From Lower Byte | LLB | D, DX |
| 1000 1101 | | Load From Upper Byte | LUBI | I, IX |
| 1000 1110 | | Load From Lower Byte | LLBI | I, IX |
| 1000 1111 | | Pop Multiple Registers Off the Stack | POPM | S |
| 1001 0000 | | Single Precision Store | ST | D, DX |
| 1001 0001 | | Store a Non-Negative Constant | STC | D, DX |
| 1001 0010 | | Store a Non-Negative Constant | STCI | I, IX |
| 1001 0011 | | Move Multiple Words Memory-to- Memory | MOV | S |
| 1001 0100 | | Store Precision Store | STI | I, IX |
| 1001 0110 | | Double Precision Store | DST | D, DX |
| 1001 0111 | | Store Register Through Mask | SRM | D, DX |
| 1001 1000 | | Double Precision Store | DSTI | I, IX |
| 1001 1001 | | Store Multiple Registers | STM | D, DX |
| 1001 1010 | | Extended Precision Floating Point Store | EFST | D, DX |
| 1001 1011 | | Store Into Upper Byte | STUB | D, DX |
| 1001 1100 | | Store Into Lower Byte | STLB | D, DX |
| 1001 1101 | | Store Into Upper Byte | SUBI | I, IX |
| 1001 1110 | | Store Into Lower Byte | SLBI | I, IX |
| 1001 1111 | | Push Multiple Registers Onto the Stack | PSHM | S |
| 1010 0000 | | Single Precision Integer Add | A | D, DX |
| 1010 0001 | | Single Precision Integer Add | AR | R |
| 1010 0010 | | Single Precision Integer Add | AISP | ISP |
| 1010 0011 | | Increment Memory by a Positive Integer | INCM | D, DX |
| 1010 0100 | | Single Precision Absolute Value of Register | ABS | D, DX |
| 1010 0101 | | Double Precision Absolute Value of Register | DABS | R |
| 1010 0110 | | Double Precision Integer Add | DA | D, DX |
| 1010 0111 | | Double Precision Integer Add | DAR | R |
| 1010 1000 | | Floating Point Add | FA | D, DX |
| 1010 1001 | | Floating Point Add | FAR | R |

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Table IIB. MIL-STD-1750A Instruction Set (Cont)

Instruction Codings

| <u>OPCODE</u> | <u>OCX</u> | <u>Instruction</u> | <u>Mnemonic</u> | <u>Address Mode</u> |
|---------------|------------|--|-----------------|---------------------|
| 1010 1010 | | Extended Precision Floating Point Add | EPA | D, DX |
| 1010 1011 | | Extended Precision Floating Point Add | EFAR | R |
| 1010 1100 | | Floating Point Absolute Value of Register | FABS | R |
| 1011 0000 | | Single Precision Integer Subtract | S | D, DX |
| 1011 0001 | | Single Precision Integer Subtract | SR | R |
| 1011 0010 | | Single Precision Integer Subtract | SISP | ISP |
| 1011 0011 | | Decrement Memory by a Positive Integer | DECM | D, DX |
| 1011 0100 | | Single Precision Negate Register | NEG | R |
| 1011 0101 | | Double Precision Negate Register | DNEG | R |
| 1011 0110 | | Double Precision Integer Subtract | DS | D, DX |
| 1011 0111 | | Double Precision Integer Subtract | DSR | R |
| 1011 1000 | | Floating Point Subtract | FS | D, DX |
| 1011 1001 | | Floating Point Subtract | FSR | R |
| 1011 1010 | | Extended Precision Floating Point Subtract | EFS | D, DX |
| 1011 1011 | | Extended Precision Floating Point Subtract | EFPSR | R |
| 1011 1100 | | Floating Point Negate Register | FNEG | R |
| 1100 0000 | | Single Precision Integer Multiply With 16-Bit Product | MS | D, DX |
| 1100 0001 | | Single Precision Integer Multiply With 16-Bit Product | MSR | R |
| 1100 0010 | | Single Precision Integer Multiply With 16-Bit Product | MISP | ISP |
| 1100 0011 | | Single Precision Integer Multiply With 16-Bit Product | MISN | ISN |
| 1100 0100 | | Single Precision Integer Multiply With 32-Bit Product | M | D, DX |
| 1100 0101 | | Single Precision Integer Multiply With 32-Bit Product | MR | R |
| 1100 0110 | | Single Precision Integer Multiply Multiply | LM | D, DX |
| 1100 0111 | | Double Precision Integer Multiply | DMR | R |
| 1100 1000 | | Floating Point Multiply | FM | D, DX |

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Table IIB. MIL-STD-1750A Instruction Set (Cont)

Instruction Codings

| <u>OPCODE</u> | <u>OCX</u> | <u>Instruction</u> | <u>Mnemonic</u> | <u>Address Mode</u> |
|---------------|------------|---|-----------------|---------------------|
| 1100 1001 | | Floating Point Multiply | FMR | R |
| 1100 1010 | | Extended Precision Floating Point Multiply | EFM | D, DX |
| 1100 1011 | | Extended Precision Floating Point Multiply | EFMR | R |
| 1101 0000 | | Single Precision Integer Divide With 16-Bit Dividend | DV | D, DX |
| 1101 0001 | | Single Precision Integer Divide With 16-Bit Dividend | DVR | R |
| 1101 0010 | | Single Precision Integer Divide With 16-Bit Dividend | DISP | ISP |
| 1101 0011 | | Single Precision Integer Divide With 16-Bit Dividend | DISN | ISN |
| 1101 0100 | | Single Precision Integer Divide With 32-Bit Integer | D | D, DX |
| 1101 0101 | | Single Precision Integer Divide With 32-Bit Integer | DR | R |
| 1101 0110 | | Double Precision Integer Divide | DD | D, DX |
| 1101 0111 | | Double Precision Integer Divide | DDR | D7 |
| 1101 1000 | | Floating Point Divide | FD | D, DX |
| 1101 1001 | | Floating Point Divide | FDR | R |
| 1101 1010 | | Extended Precision Floating Point Divide | EPD | D, DX |
| 1101 1011 | | Extended Precision Floating Point Divide | EPDR | R |
| 1110 0000 | | Inclusive Logical or | OR | D, DX |
| 1110 0001 | | Inclusive Logical or | ORR | R |
| 1110 0010 | | Logical and | AND | D, DX |
| 1110 0011 | | Logical and | ANDR | R |
| 1110 0100 | | Exclusive Logical or | XOR | D, DX |
| 1110 0101 | | Exclusive Logical or | XORR | R |
| 1110 0110 | | Logical NAND | N | D, DX |
| 1110 0111 | | Logical NAND | NR | R |
| 1110 1000 | | Convert Floating Point to 16-Bit Integer | EIX | R |
| 1110 1001 | | Convert 16-Bit Integer to Floating Point | FLT | R |
| 1110 1010 | | Convert Extended Precision Floating Point to 32-Bit Integer | EFIX | R |
| 1110 1011 | | Convert 32-bit Integer to Extended Precision Floating Point | EFLT | R |
| 1110 1100 | | Exchange Bytes in Registers | XBR | S |

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Table IIB. MIL-STD-1750A Instruction Set (Cont)

Instruction Codings

| <u>OPCODE</u> | <u>OCX</u> | <u>Instruction</u> | <u>Mnemonic</u> | <u>Address Mode</u> |
|---------------|------------|--|-----------------|---------------------|
| 1110 1101 | | Exchange Words in Registers | XWR | R |
| 1111 0000 | | Single Precision Compare | C | D, DX |
| 1111 0001 | | Single Precision Compare | CR | R |
| 1111 0010 | | Single Precision Compare | CISP | ISP |
| 1111 0011 | | Single Precision Compare | CISN | ISN |
| 1111 0100 | | Compare Between Limits | CBL | F4 |
| 1111 0110 | | Double Precision Compare | DC | D, DX |
| 1111 0111 | | Double Precision Compare | DCR | R |
| 1111 1000 | | Floating Point Compare | FC | D, DX |
| 1111 1001 | | Floating Point Compare | FCR | R |
| 1111 1010 | | Extended Precision Floating Point Compare | EFC | D, DX |
| 1111 1011 | | Extended Precision Floating Point Compare | EFCR | R |
| 1111 1111 | | No Operation/Break Point | NOP/BPT | S |

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Table III. Interrupt Structure and Priorities

| Interrupt Source | Interrupt Number | Interrupt Priority | Class |
|-------------------------------------|------------------|--------------------|----------------------|
| Power-on | 0 | 1A* | Power |
| System reset | 1 | 1B** | Power |
| Power-off (POID) | 2 | 2 | Power |
| GPC storage error | 3 | 3 | Machine check |
| CPU address specification | 7 | 7 | Program exception |
| CPU store protect violation | 8 | 8 | Program exception |
| CPU ROS parity | 9 | 9 | Machine check |
| Instruction monitor | 10 | 10 | Program exception |
| Illegal operation | 11 | 11** | Program exception |
| Privileged instruction | 12 | 11** | Program exception |
| Fixed-point overflow | 13 | 11** | Program exception |
| Significance | 14 | 11** | Program exception |
| Exponent underflow (floating-point) | 15 | 11** | Program exception |
| Overflow (convert) | 16 | 11** | Program exception |
| Exponent overflow (floating-point) | 17 | 11** | Program exception |
| Divide (floating-point) | 18 | 11** | Program exception |
| Executive (supervisor call) | 19 | 12 | Supervisor call |
| Initiate putaway | 20 | 13 | Power |
| Real-Time clock No. 1 | 21 | 14 | CPU external Level 1 |
| Real-Time clock No. 2 | 22 | 15 | CPU external Level 1 |
| Watchdog timer timeout | 23 | 16A | IOP external Level 1 |
| IOP voter | 24 | 16B | IOP external Level 1 |
| C/M idle | 25 | 16C | IOP external Level 1 |
| IOP ROS parity | 26 | 16D | IOP external Level 1 |
| IOP fault | 27 | 16E | IOP external Level 1 |
| Spare | 28 | 16F | IOP external Level 1 |
| Queue overflow | 33 | 17E | IOP external Level 2 |
| DMA time-out | 34 | 17F | IOP external Level 2 |
| DMA address specification | 35 | 17G | CPU external Level 2 |
| DMA store protect violation | 36 | 17H | CPU external Level 2 |
| AGE interrupt | 39 | 17K | CPU external Level 2 |
| IOP programmable (1-12) | 41-52 | 18A-18L | IOP external Level 3 |
| Spare (4) | 53-56 | 19A-19D | IOP external Level 4 |
| Spare (4) | 57-60 | 20A-20D | IOP external Level 5 |

NOTES:

*Priority determined by hardware

**Mutually exclusive

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Each interrupt shall be individually maskable except for power on/off, machine check, supervisor call, and program interrupts. Power on/off, supervisor call, and program interrupts shall not be maskable except for fixed point overflow, exponent underflow, and significance. Machine check interrupts shall be maskable by class only. If program class interrupt conditions occur while masked, they shall be ignored and shall not remain pending. If any other interrupt condition occurs while masked, it shall remain pending. Machine check and instruction monitor interrupts do not remain pending.

Simultaneous interrupt requests shall be honored by the CPU according to the following priority:

- (1) Power on/off
- (2) Machine check
- (3) Program/supervisor call
- (4) External class (IOP class)

Interrupt handling shall consist of storing the current program status work (PSW) in its "old" position in mainstore and making the PSW at the "new" position the current PSW. The PSW shall hold all necessary status information on the system existing at the time of interruption.

When more than one unmasked interrupt requests service, the action shall consist of storing the old PSW and fetching the new PSW belonging to the interruption which is taken first. This new PSW shall subsequently be stored without any instruction execution and the next interruption PSW shall be fetched. This process shall continue until no more interruptions are to be serviced. When the last interruption request has been serviced, instruction execution shall be resumed using the PSW last fetched. Machine check and power interrupts, when they occur, shall not allow other interrupts to be taken. IOP interrupts shall be maskable by level only.

3.2.1.3.7 CPU Program Control I/O Mode. The CPU shall be capable of transferring one full word per single instruction between the CPU general registers and the IOP, or the IOP and the CPU general registers. This mode shall be initiated and controlled by the CPU.

3.2.1.3.8 CPU/DMA Mode. The CPU shall provide the capability for enabling or disabling the DMA mode under hardware control. DMA operations are specified in paragraph 3.2.1.5.2.3.

3.2.1.3.9 Clock (Internal Master). An internal master clock oscillator and associated circuitry shall supply precision timing signals for all logic circuits within the CPU. The accuracy of the oscillator shall be 0.001 percent. Accuracy is herein defined as the initial allowable offset from the nominal with the LRU at the standard test conditions specified in 4.1.2.1. The master clock oscillator and associated circuitry shall have a long term stability of at least 50 parts in 10^6 and a short term stability of at least 50 parts in 10^6 within the operating environment specified. Stability is herein defined as the allowable variation from the nominal. Long term stability is defined as 7 days and short term as 15 minutes. The turn on time of the oscillator shall not exceed 100 milliseconds from the time master power reset is released after the application of primary power.

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3.2.3.10 Real-Time Clocks. The CPU shall have two program settable real-time clock registers capable of being decremented from internal clock oscillator. When the count in the registers passes through zero, an interrupt shall be generated whose priorities are as specified in paragraph 3.2.1.2.6. Both counters shall have a resolution of at least 1 microsecond. The counter shall have 32 bit capacity. The clock registers shall be capable of being sampled by the CPU without interfering with the register counting function. The clock registers shall not be set during the power-on sequence. The clocks shall continue to count after pass in through their limits. The clocks shall be read via a privileged READ COUNTER instruction and shall be loadable via a privileged WRITE COUNTER instruction.

3.2.1.4 Memory.

3.2.1.4.1 Memory Capacity. The computer shall contain a minimum of 262,144 full-words of main memory. Half and full-word accessibility of the memory is required. Internal means for error correction and cosmic ray scrubbing is required.

3.2.1.4.2 Memory Functions. The memory shall function in the following modes:

- a. Active - Memory powered up and operating
- b. Standby - Memory and CPU powered up and not operating
- c. Scrub Only - Memory powered up, CPU powered down
- d. Memory Retention - Memory powered off, batteries supplying power, no scrubbing.

3.2.1.4.3 Memory Speed. The cycle time for a read-compute-write operation (to and from local store) shall not exceed 250 ns during instruction execution/effective address computation. The time required for storing data into semiconductor memory shall not exceed 750 ns from the time the address is available.

3.2.1.4.5 Memory Technology. The GPC shall have a CMOS solid state memory with battery back up power for maintaining nonvolatility of memory contents for short durations of power down or interrupts.

3.2.1.4.6 Memory Data Protection. The contents of memory shall not be altered due to primary power interruptions or fluctuations as defined in paragraph 3.1.2.1. A scrubbing technique shall be used to reduce the exposure of uncorrectable soft errors due to cosmic rays during orbital operation. The scrub rate is 1.7 seconds. The error correction code used shall correct all single errors and shall detect and report all double errors to the CPU as a machine check interrupt.

3.2.1.4.7 Deleted.

3.2.1.4.8 Memory Load. Capability to load the memory shall be provided. Mechanization occurs via computer hardware and microprogram store.

The bootstrap microprogram shall be capable of the following:

- a. Sending a program load command to an external storage device via a selected serial channel
- b. Specifying a designated program source address
- c. Capability to enable storage protection logic during loading

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3.2.1.4.9 Memory Storage Protection. The computer shall provide a means of selectively preventing writing into any half-word of memory. Each half-word of memory shall contain three voted storage protection bits. Capability shall be provided for setting and resetting these three protection bits either by individual half-word or by blocks of words under software control. An illegal attempt to gain access to protected storage shall cause an interrupt.

3.2.1.5 Input/Output Processor (IOP) Design and Functions. The input/output processor (IOP) will interface with avionics subsystems as shown in Figure 2. (Figure 2 is for reference only). The IOP shall be designed to perform the functions listed herein.

3.2.1.5.1 Operation and Definition.

3.2.1.5.1.1 Data Transfers. Data transfers shall occur one at a time and concurrently. The IOP shall be capable of performing 24 concurrent operations over different one megahertz data buses in any combination of transmitting and receiving.

3.2.1.5.1.2 Concurrency Mechanization. Concurrency mechanization shall allow for concurrent operations whose time skew is less than 28 microseconds. Time skew is defined as the time between the first multiplexed interface adapter (MIA) transmitting and the twenty-fourth MIA transmitting, or between the first MIA receiving and the twenty-fourth MIA receiving.

3.2.1.5.1.3 IOP/Memory Transfers. The IOP shall communicate with the computer main memory in both the normal DMA and burst DMA modes; the DMA modes shall be enabled by the CPU before the IOP can access memory. The normal DMA shall function on a cycle steal basis in conjunction with CPU memory requests. The IOP shall enter the burst mode when the number of requests pending is equal to eight (8) or more. The IOP shall exit the Burst mode when the Queue is seven less and at the end of 64 consecutive memory cycle times. This access shall be limited to 64 consecutive memory accesses as described in paragraph 3.2.1.5.2.3.

3.2.1.5.1.3.1 Memory Storage Protect. This feature shall be restricted to the boot-strap load mode. Control shall be initiated by the IOP to enable storage protection in the CPU to allow for the setting or resetting of memory storage protect bits associated with DMA data stored into the main memory for a program loading mode. Indication of the storage protect bit associated with a DMA data half-word being read from main memory shall be provided to allow verification of a program load. On DMA full-words being read, one store protect indication is given if either half-word is protected. Memory protect bits shall be assigned for each halfword of data, including error correction code. The CPU shall control this function via the "insert storage protect bits" instruction (privileged) as shown in Table II.

3.2.1.5.1.4 IOP Control. The IOP shall be under CPU control for initiation of input/output requests and shall be under its own internal control for initiating and controlling data acquisition sequences and for the output of commands for data input and output to and from subsystems. In the listen mode data transfer shall be initiated as specified in paragraphs 3.2.1.5.5.1.2 and 3.2.1.5.5.1.2.1.

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3.2.1.5.1.5 Discrete Drivers and Receivers. The discrete drivers and receivers shall be identical to the drivers and receivers specified in paragraph 3.1.2.3.1. Thirty-one (31) discrete outputs shall be provided which the CPU has the capability of independently setting/resetting under software control. Six of these discrete drivers (D.O. 18, 20, 22, 24, 26, and 28) shall meet the requirements of paragraph 3.1.2.3.1.7. One discrete output shall be provided which is always set to the "one" state. Five additional discrete outputs shall be provided for RM and shall function as specified in paragraph 3.2.1.8.3.

Forty-four (44) discrete input receivers shall be provided which the CPU can independently read under software control. Four of these discrete inputs shall be used for the RM as specified in paragraph 3.2.1.8.3. Three of these discrete inputs shall be used for IPL as specified in paragraph 3.2.1.12. Two of these discrete inputs shall directly disable respectively one group of four data buses and two groups of four data buses. Three of these discrettes shall be used for GPC station identification.

3.2.1.5.1.6 Deleted.

3.2.1.5.1.7 Deleted.

3.2.1.5.1.8 General IOP Design Requirements.

- a. The primary IOP design goal shall be to minimize computer control requirements and conserve computer processing time.
- b. The IOP shall be capable of performing cyclic input/output functions. Each cycle will be initiated by CPU command. The IOP shall execute the micro-programmed instruction sequences for each command cycle.
- c. Each IOP port (bus interface) shall be designed to operate independently of other IOP ports. Each port shall be designed to synchronize IOP operations with the "traffic" on the bus. Instructions for processing bus traffic shall be initiated by the associated computer (if in the command mode) or by a recognized bus command from an alternate source (if in the listen mode).
- d. The IOP will implement flexible design features where possible to avoid restrictions that would affect reserve growth capabilities.

3.2.1.5.2 Operational Modes. The IOP operational modes shall be under stored main memory computer program control. Computer programs will have the facility for supervising (i.e., start, stop, sense status, etc.,) the operation. Information transmission shall be controlled by the IOP once the operation has been initiated by the CPU. The IOP shall be capable of up to 24 concurrent, independent data transmissions and receptions on any combination of data bus channels. The IOP shall be capable of the following modes of operation:

3.2.1.5.2.1 Command Mode. In the command mode, the BCE shall control its associated MIA for the issuance of commands to the interfacing avionics subsystem. The command mode shall function as specified in paragraph 3.2.1.5.5.1.1.

3.2.1.5.2.2 Listening Mode. Each IOP channel that has its transmitter disabled and receiver enabled shall be capable of detecting a "command sync" pattern on the associated data bus. If a "common IOP address" is recognized in a "command sync" word,

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the "program memory address" shall be derived from the word format and placed in the BCE program counter. This register shall be derived from the word format and placed in the main memory for BCE instructions which shall describe the processing sequence for the anticipated "data sync" message words. Once initialized, data transfer is initiated by an external device. The listen mode shall function as specified in paragraph 3.2.1.5.5.1.2.

3.2.1.5.2.3 Direct Memory Access (DMA) Operations With Main Memory.

3.2.1.5.2.3.1 Normal DMA Mode. Direct memory access I/O operations shall provide the capability to transfer one or more full words between the main memory and the IOP. A main memory cycle request from the IOP shall have priority over all other normal memory cycle requests, once DMA has been enabled by the CPU. If continuous memory cycle requests occur, the DMA shall not be capable of monopolizing memory access; rather, the DMA operation shall be interleaved with other CPU memory requests as they occur. Normal DMA requests shall not interfere with existing memory cycles but shall be honored at the completion of the existing memory cycle. Normal DMA I/O operations shall be capable of providing a transfer rate of 625,000 full words per second.

3.2.1.5.2.3.2 Deleted.

3.2.1.5.2.3.3 Deleted.

3.2.1.5.2.3.4 Deleted.

3.2.1.5.2.3.5 Error Correction Code Generation and Error Detection. The GPC shall have as a minimum, a single error correction, and a double error detection capability. This bit shall be reset after being interrogated. Any error which cannot be corrected by the EDC mechanization shall trap the address and provide an interrupt to the program.

The GPC shall have provision for counting all soft errors that were corrected during memory scrub. The counter shall be read/reset by MMU XIO command.

3.2.1.5.3 Control/Monitor. The control/monitor (C/M) shall perform the following functions:

- a. Handle master and power on reset functions
- b. Issue C/M idle
- c. Read discrete inputs
- d. Enable or inhibit discrete outputs
- e. Enable/disable MLA transmitters
- f. Enable/disable MLA receivers

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- g. Halt BCE's
- h. Interrupt control
- i. Handle PCO-PCI interface
- j. Status reset
- k. Processor control and status

3.2.1.5.3.1 PCO/PCI Interface. The C/M interface with the CPU shall provide for the following:

- a. The C/M shall.

Decode PCI and PCO instructions

Send BCE number, MSC number, and commands to the appropriate control logic

Accept completion acknowledgements

- b. On PCO's, the IOP interface logic shall load the data into appropriate IOP te registers
- c. On PCI's, the IOP interface logic shall place the contents of the appropriate IOP buffer on the computer data lines and start the interface.

3.2.1.5.3.2 C/M Interrupts. The C/M interrupts shall consist of but not be limited to the IOP external interrupts listed in paragraph 3.2.1.3.6 and Table III, Levels 16 through 20.

3.2.1.5.3.3 CPU-Issued Reset Commands. The control monitor shall contain the reset logic and issue reset signals to all IOP elements as required. Table IV is list of the reset logic.

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Table IV. Control Monitor Reset Logic

| Function | Power Reset or Halt | | PCO Master Reset Command | IOP Fail Reset | Remarks |
|---------------------------|---------------------|----------------------|--------------------------|----------------|---|
| | ON | OFF | | | |
| Status 1 (Go/No Go) | Reset | Reset | Reset | No Change | Reset = Go |
| Status 4 (Busy/Wait) | Reset | Reset | Reset | Reset | Reset = Wait |
| Status 5 (Halt/No Halt) | Reset | Reset | Reset | Reset | Reset = Halt MSC/BCE |
| Transmitter Enable | Reset | Reset | Reset | | Reset = Disable |
| Receiver Enable | Reset | Reset | Reset | Reset | Reset = Disable |
| Channel | Reset | Reset | No Change | No Change | |
| Fail Vote Register | Reset | Reset | Reset | Reset | Reset = No Fail |
| Voter Test Register | Reset | Reset | Reset | Reset | Reset = OP data |
| Discrete Outputs | Reset | Reset | Reset | Reset | Reset = Inactive |
| Fail Latch | Reset | No Reset on CPU P.D. | No Change | No Change | Reset = No Fail |
| Time Out Latch | Reset | No Reset on CPU P.D. | No Change | No Change | Reset = Reset by watchdog timer |
| Watchdog Timer | Reset | No Change | Reset | Reset | Reset = Zero timer and inhibit counting |
| <u>Interrupt Register</u> | | | | | |
| ROS Parity Error | Reset | Reset | Reset | No Change | Set = Interrupt pending |
| C/M Idle | Set | Set | Set | Set | Set = Interrupt pending |
| IOP Fail Latch | Reset | No Reset on CPU P.D. | No Change | No Change | Set = Interrupt pending |

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Table IV. Control Monitor Reset Logic (Cont)

| Function | Power Reset or Halt | | PCO Master Reset Command | IOP Fail Reset | Remarks |
|---------------|---------------------|----------------------|--------------------------|----------------|-------------------------|
| | ON | OFF | | | |
| Timeout Latch | Reset | No Reset on CPU P.D. | No Change | No Change | Set = Interrupt pending |
| IOP Fault | Reset | Reset | Reset | No Change | Set = Interrupt pending |
| All Others | Reset | Reset | Reset | Reset | Set = Interrupt pending |

Note: Power reset ON-OFF is CPC power reset.

IOP Fail Reset: Stop voter, watchdog timer, ROS parity, and IOP fault.

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3.2.1.5.3.3.1 IOP Master Reset. A CPU-issued PCO master reset command shall be interpreted by the C/M to force the MSC and BCE to the wait state. The contents of the MSC and BCE registers shall be retained for CPU monitor functions. This halt mode shall be an immediate halt of BCE and MSC functions, independent of concurrent instruction executions. This command shall not override MSC and BCE errors which persist, but shall immediately inhibit all MIA transmitters and receivers and reset all discrete outputs except the computer fail discrete output as indicated in 3.2.1.8.4.

3.2.1.5.3.3.2 IOP Status Reset. A CPU-issued PCO status reset command shall be interpreted by the C/M to reset all status word error indicators except those in local store. This command shall not override MSC and BCE errors which persist.

3.2.1.5.3.5 Other Discrete Signals. The C/M shall act as a possible relay (with the exception of discrete outputs following a power-on, internally detected fault, or master reset from the CPU) for other special discrete signals. Enabling and inhibiting capabilities for all discrete outputs shall be provided by the C/M.

3.2.1.5.3.6 CPU-Issued PCO Commands. The CPU-issued PCO commands shall include as a minimum those instructions listed in Table V.

3.2.1.5.3.7 CPU-Issued PCI Monitor Requests. The CPU monitor requests shall be acknowledged by the C/M. The CPU-issued PCI monitor requests shall include as a minimum those shown in Table VI.

3.2.1.5.4 Master Sequence Controller (MSC). The CPU via program control output (PCO) shall activate the MSC to perform cyclic interleaved input/output requests. Once activated, the MSC shall provide, via its own instruction set execution, the particular I/O sequence. The major functions of the MSC shall be as follows:

- a. Execute programs located in main memory
- b. Schedule and initiate bus control element (BCE) programs
- c. Monitor the status of BCE's and aid in error handling
- d. Detect I/O completions
- e. Perform redundancy management processing functions
- f. Communicate with the CPU through IOP interrupts

3.2.1.5.4.1 MSC Operation. The MSC shall operate in one of three states:

- a. Wait state
- b. Busy state
- c. Halt state

In the Halt state, the MSC shall not perform any operations or execute programs. In the Busy state, the MSC shall execute programs located in main store. In the Wait state, the MSC shall wait for a command to execute a program.

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Table V. CPU-Issued PCO Commands

| PCO Command | Description |
|------------------------|--|
| 1. Load Local Store | This command shall be used to selectively load any word into the IOP local store, including the BCE base registers and all program counters. |
| 2. Disable Transmitter | This command shall be used to disable BCE transmitters selectively. A bit position will be assigned to each BCE. Each bit position shall be interpreted as 1 = disable, 0 = no change. |
| 3. Enable Transmitter | This command shall be used to enable BCE transmitters selectively. A bit position will be assigned to each BCE. Each bit position shall be interpreted as 1 = enable, 0 = no change. |
| 4. Disable Receiver | This command shall be used to disable BCE receivers selectively. A bit position will be assigned to each BCE. Each bit position shall be interpreted as 1 = disable, 0 = no change. |
| 5. Enable Receiver | This command shall be used to enable BCE receivers selectively. A bit position will be assigned to each BCE. Each bit position shall be interpreted as 1 = enable, 0 = no change. |
| 6. Halt Processors | This command shall be used to halt IOP processors selectively. A bit position will be assigned to each BCE and to the MSC. Each bit position shall be interpreted as 1 = halt, 0 = no change. The selected processors shall enter the halt mode. |
| 7. Enable Processors | This command shall be used to enable IOP processors selectively. A bit position will be assigned to each BCE and to the MSC. Each bit position shall be interpreted as 1 = enable processor, 0 = no change. |
| 8. Set Discrete Out | This command shall be used to set discrete outs. A bit position shall be assigned to each discrete. Each bit position shall be interpreted as 1 = set discrete, 0 = no change. |
| 9. Reset Discrete Out | This command shall be used to reset discrete outs. A bit position shall be assigned to each discrete. Each bit position shall be interpreted as 1 = reset discrete, 0 = no change. |
| 10. Spare | |

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Table V. CPU-Issued PCO Commands (Cont)

| PCO Command | Description |
|--|---|
| 11. Load Watchdog Timer | This command shall be used to load the watchdog timer (part of Redundancy Management) with the contents of the low order 12 bits of the data word. |
| 12. Load Voter Test | This command shall be used to load voter test register with one bit of the displacement field. |
| 13. Master Reset | This command shall be used to force the MSC and each BCE to idle mode. The contents of the respective program counters shall be retained for CPU monitoring. |
| 14. MSC Start | This command shall be used to cause the MSC to commence executing the instruction sequence starting at the addressed processors program counter setting. |
| 15. Reset Status Bit 1 (Go/No Go Bit) | This command shall be used to selectively reset the MSC and BCE status register. A bit position shall be assigned for each status register. Each bit position shall be interpreted as 1 = reset; 0 = no change. |
| 16. Enable DMA Burst Mode | This command enable the burst DMA mode to the IOP. |
| 17. Disable DMA Burst Mode | This command shall disable the burst DMA mode. |
| 18. Test Watchdog Timer | This command shall be used to test the watchdog timer. |

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Table VI. CPU-Issued PCI Monitor Requests (Cont)

| PCO Command | Description |
|---|---|
| 10. Read Receiver Enable (Status Bit 3) | This request shall be acknowledged by loading the designated 32-bit CPU register with the contents of the receiver enable register. |
| 11. Read Status Bit 5 (HALT) | This request shall be acknowledged by loading the designated 32-bit CPU register with status bit-5. Stat 5 is an indication of the BCE and MSC Halt register. There shall be one bit for each BCE and one bit for the MSC (Bit 1 = BCE 1, Bit 24 = BCE 24, Bit 25 = MSC) "1" = halt, "0" = Not in halt. |

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3.2.1.5.4.1.1 MSC Wait State. The MSC shall enter a quiescent (wait) state under the following conditions:

- a. A Wait instruction (#WAT) is executed.
- b. An illegal op code instruction is detected.
- c. A full-word (long) instruction is requested starting on an odd half-word boundary.
- d. The MSC also enters the wait state when it is halted by a PCO command.

The IOP shall provide a positive MSC Wait state indication via a status register to the computer. The status register shall contain the results of error and status functions of the MSC as specified in Table VII. The MSC shall acknowledge the "MSC start" PCO command while in the Wait state and shall not interfere with any PCO/PCI operation. When the MSC enters the Wait state from a #WAT instruction, it shall leave its program counter pointing to the next instruction. When the MSC enters the wait state due to an illegal op code or boundary alignment error, its program counter shall point to the instruction causing the error.

3.2.1.5.4.1.2 MSC Halt State. The MSC shall enter the Halt state under the following conditions:

- a. Power-on reset
- b. Power-down signal
- c. Master reset discrete from the CPU
- d. A halt processor command from the CPU
- e. Setting of the RM fail latch by either the RM logic or IOP detected errors.

The MSC shall enter the Wait state if it is in the Halt state when:

- a. The master reset discrete is reset
- b. The power-up sequence has been completed
- c. The fail latch is reset
- d. The CPU has issued an "enable processors" PCO with a 1 in bit zero.

A CPU issued MASTER RESET command shall be initiated before any other command acknowledgement when the halt mode is entered due to power changes or IOP detected errors. Upon exiting the Halt state, the MSC program execution bit and the status register shall be cleared.

3.2.1.5.4.2 MSC Busy State. The MSC shall enter the Busy state conditions:

When the CPU issues a PCO command. The Busy state is entered from the Wait state only.

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The MSC program counter shall be initialized under computer control. The program counter shall direct the MSC to the program memory instruction sequence to be executed. The MSC instruction sequence shall initialize bus control elements to perform for computer-requested data-bus input/output operations.

3.2.1.5.4.3 MSC Interruption. The MSC shall be capable of being interrupted by using the external call instructions (@ SEC, @ REC) listed in Table VIII.

3.2.1.5.4.4 MSC Index Register (X). The 18-bit index register shall be used to generate main memory addresses. In addition, it shall act as a holding register for signed two's complement, 18-bit integers.

3.2.1.5.4.5 MSC Program Counter (PC). The 18-bit PC shall contain the address of the next instructions to fetch for MSC execution. Following a fetch of an MSC instruction, the program counter shall be incremented by the specified counts.

3.2.1.5.4.6 MSC Instruction Register (IR). The 32-bit IR shall be loaded with the data (instruction) addressed by the PC. The MSC instructions to be executed are shown in Figure 7 and described in Table VII.

3.2.1.5.4.7 MSC Accumulator Register (ACC). The 32-bit ACC shall be utilized as the primary full-word holding register for most of the MSC instructions during execution. MSC instructions are available to load, modify, test, and store this register. The ACC shall also contain bit masks for status and polling applications.

3.2.1.5.4.8 Busy Signals. Busy signals shall be available to the MSC to reflect the current utilization status of all 24 BCE's. A busy BCE is defined as one outputting data, inputting data, or executing BCE instructions other than the wait instructions.

3.2.1.5.4.9 MSC Status Register (SR). The 18-bit SR shall be utilized to store the current status of the MSC. (See Table VII).

3.2.1.5.4.10 MSC Architecture Notation.

- a. R is a register or function of registers.
- b. "R" - refers to R itself.
- c. "(R)" - refers to the memory location addressed by the value of R.
- d. Stat 4 is a register loadable by the MSC that has one bit for each BCE and on bit for the MSC (1 = BCE or MSC is executing a program, 0 = BCE or MSC is in Wait state).

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Table VII. MSC Status Register
Status Register Bit Positions

| | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|---|
| S | S | S | S | S | S | S | S | S | S | S | S | I | L | L | B | I | E | B |
| P | P | P | P | P | P | P | P | T | P | P | O | P | B | B | A | | | / |
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | |

- 0 thru 7 - SP-SPARE - Reserved for future use.
- 8 - ST - Self-test error. A MSC self-test instruction detected an MSC fault.
- 9 and 10 - SP-SPARE - Reserved for future use.
- 11 - SIO - SIO error: An SIO (start I/O) instruction attempted to start a busy BCE 0 = good, 1 = SIO error.
- 12 - LBP - LBP error: An LBP (load program counter) instruction attempted to load a busy BCE. 0 = good, 1 = LBP error.
- 13 - LBB - LBB error: The LBB (load base register) instruction attempted to load a busy BCE, 0 = good, 1 = LBB error.
- 14 - BA - Boundary alignment: The MSC encountered a long format instruction on an odd half-word boundary. 0 = good, 1 = error.
- 15 - I - Illegal opcode: The MSC encountered an illegal instruction in the execution of a program. 0 = legal instruction, 1 = illegal instruction.
- 16 - E - Program exception: A copy of bit 0 of the program exception register. If one set (1) an error was detected during MSC program execution. Bits 8 through 15 given the exact errors detected.
- 17 - B/W - Busy/Wait: A copy of the Busy/Wait (bit 0) register. 0 = wait, 1 = busy.

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Table VIII. MSC Instruction Set

| Opcode I OPX | Instruction | Mnemonic | Format | Notes Reference Paragraph 3.2.1.5.4.12 |
|---------------------------------------|--------------------------|------------|------------------|---|
| Long Format Instructions | | | | |
| 1111 010 | Load BCE Base | @ LBB | BCE, Label (X) | 1,10,11,12 |
| 1111 011 | Load BCE PC | @ LBP | BCE, Label (X) | 1,10,11,12 |
| 1111 000 | Branch Unconditional | @ BU | Label (X) | 1,10,12 |
| 1111 001 | Subroutine Call | @ Call | Delta, Label (X) | 1,10,12,13 |
| 1111 110 | Compare | @ C | Label (X) | 1,10,13 |
| 1111 111 | Test Under Mask | @ TMI,@ TM | Label (X) | 1,10,14 |
| Load Accumulator Instructions | | | | |
| 1111 000 | Load ACC Full-word | @ LF | Label (X) | 1,10,12,15 |
| 1111 000 | Load ACC With Half-word | @ LH | Label (X) | 1,10,12,16 |
| Store Accumulator Instructions | | | | |
| 1111 101 | Store ACC Full | @ STF | Label (X) | 2,10,12,15 |
| 1111 101 | Store ACC Half | @ STH | Label (X) | 2,10,12,16 |
| Short Format Instructions | | | | |
| 0000-1 | Wait | @ WST | | |
| 0001 | Self Test | @ STP | | |
| 1100 | Delay | @ DLY | Count (X) | 1,3 |
| 0011 | Interrupt GPC | @ INT | Intlist (X) | 1,4 |
| 0100 | Load ACC | @ L | Label (X) | 1,2 |
| 0101 | Add to ACC | @ A | Label (X) | 1,2 |
| 0110 | And to ACC | @ N | Label (X) | 1,2 |
| 0111 | XOR to ACC | @ X | Label (X) | 1,2 |
| 1000 | Store ACC | @ ST | Label (X) | 1,2 |
| 1001 | Tally and Skip Zero | @ TSZ | Label (X) | 1,2 |
| 1101-000 | Repeat Until All Waiting | @ RAW | Count (X) | 1,5 |
| 1101-001 | Repeat Until Any Waiting | @ RNW | Count (X) | 1,5 |
| 1101-100 | Repeat Until All Indica. | @ RAI | Count (X) | 1,5 |
| 1101-101 | Repeat Until All Indica. | @ RNI | Count (X) | 1,5 |
| Conditional Branches | | | | |
| 00100 | Branch on ACC | @ BC | Cond, Label | 6,7 |
| 00101 | Branch on Index | @ BXC | Cond, Label | 6,7 |

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Table VIII. MSC Instruction Set (Cont)

| Opcode I OPX | Instruction | Mnemonic | Format | Notes Reference Paragraph 3.2.1.5.4.12 |
|-----------------------------------|---------------------------------|----------|---------------|---|
| Register Operations | | | | |
| 1110 0000 | Load AC With An IOP Stat Reg | @ LAR | Register | 8 |
| 1110 0111 | Reset BCE Indicator | @ RBI | BCE | 11,18 |
| 1110 0001 | Set Fail Discretes | @ SFD | | |
| 1110 0010 | Reset Fail Discretes | @ RFD | | |
| 1110 0011 | Load ACC with MSC Status | @ LMS | | |
| 1110 0100 | Start BCE's | @ SIO | | |
| 1110 0101 | Exchange ACC and /X | @ XAX | | |
| Register Immediates | | | | |
| 1110 1000 | Normalize and Inc. X | @ NIX | Immediate | 9 |
| 1110 1001 | Tally ACC to X | @ TAX | Immediate | 9 |
| 1110 1010 | Tally X | @ TXI | Immediate | 9 |
| 1110 1011 | Load X Immediate | @ LXI | Immediate | 9 |
| 1110 1100 | Tally X to ACC | @ TXA | Immediate | 9 |
| 1110 1110 | Sub ACC From IMM | @ SAI | Immediate | 9 |
| 1110 1111 | Load ACC Immediate | @ LI | Immediate | 9 |
| MSC Interrupt Instructions | | | | |
| 11100110 | Sample for Ext Call | @ SEC | External Call | |
| 1010 | Return from Ext Call | @ REC | External Call | |

Table VIII. MSC Instruction Set

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles |
|-------------------------------|----------|--------|---|-------------------------------|
| 1. Load a BCE Base Register | @ LBB | Long | <p>Load the selected BCE base register with the contents of the 18-bit address field. If the BCE number field is zero, the specified BCE is that indicated by the lower 5 bits of the MSC accumulator. If the BCE specified by bits 8-12 (or the MSC accumulator, if the BCE number field is zero) is <u>not</u> busy, then the 18-bit effective value and the address field is loaded into the BCE base register. If the BCE is busy, bit 13 in the MSC status register is set. In both cases, the MSC program counter is incremented by 2, and the next sequential instruction is executed.</p> <p><u>I M Effective Value Instruction Format</u></p> <p>0 0 Address @ LBB,BCE, Address 0 1 (Address) @ LBB @ BCE, Address 1 0 Address + X @ LBB,BCE, Address(1) 1 1 (Address +X) @ LBB,BCE, Address(1)</p> | 4 |
| 2. Load a BCE Program Counter | @ LBP | Long | <p>Load the addressed BCE program counter (Field BCE number bits 8-12 specify a BCE processor) with the contents of the address field. If the BCE number field is zero, the specified BCE is that indicated by the lower 5 bits of the MSC accumulator (bits 27 to 31). If the BCE specified by bits 8 through 12 is not busy, then the 18-bit effective value is stored in the specified BCE's program counter. No action is initiated and the next MSC instruction is executed. If the specified BCE is busy, bit 12 of the MSC status register is set. The effective value is compared according to the following table:</p> | 4 |

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Table VIII. MSC Instruction Set (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles |
|--------------------------------------|----------|--------|---|-------------------------------|
| 2. Load a BCE Program Counter (Cont) | | | <p><u>I M Effective Value Instruction Format</u></p> <p>0 0 Address @ LBP BCE, Address</p> <p>0 1 (Address) @ LBP @ BCE, Address</p> <p>1 0 Address + X @ LBP BCE, Address(1)</p> <p>(Address + X) @ LBP @BCE, Address(1)</p> | |
| 3. Branch Unconditional | @ BU | Long | <p>The MSC program counter is loaded with the lower 18 bits of the effective value. A branch to either an even or odd half-word is permitted.</p> <p><u>I M Effective Value Instruction Format</u></p> <p>0 0 Address @ BU Address</p> <p>0 1 (Address) @ BU @ Address</p> <p>1 0 Address + X @ BU Address (1)</p> <p>1 1 (Address + X) @ BU @ Address (1)</p> | 2 |
| 4. Test Under Mask | @ TM | Long | <p>The effective value is logically "anded" with the accumulator. If the result is not zero, then the program counter is incremented by 3 (skip the next halfword). If the MSC accumulator "and" the effective value equal zero, then the program counter is incremented by two (execute the next instruction). The original accumulator contents are not changed by this instruction.</p> <p><u>I M Effective Value Instruction Format</u></p> <p>0 0 Address* @ TM Value</p> <p>0 1 (Address*) @ TMI Address</p> <p>1 0 Address + X* @ TMI Value (1)</p> <p>1 1 (Address + X*) @ TM Address (1)</p> <p>*This 18-bit quantity is treated as a two's complement number, and is right justified with 14 leading "1's" to fill 32 bits.</p> | 6 |

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Table VIII. MSC Instruction Set (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles | | | | | | | | | | | | | | | | | | |
|-------------------|-------------------------------------|------------------------|---|-------------------------------|-------------------------------------|------------------------|----|----|-----|----|----|-----|----|----|-----|----|---|-----|----|---|-----|---|
| 5. Exclusive "or" | @ X | Short | <p>Exclusive "or" the contents of the MSC accumulator and the contents of the full word operand addressed by the effective address. The result is place in the MSC accumulator. The program counter is incremented by 1.</p> <p><u>I</u> <u>Effective Address</u> <u>Instruction Format</u> 0 PC + Displacement @ X Data 1 PC + Displacement + X @ X Data (1)</p> <p>PC refers to the updated program counter value (i.e., the address of the next instruction) bit 5 is the sign of the two's complement displacement field. The range of the displacement is -1024 to +1023 halfwords. X is the index register.</p> | 6 | | | | | | | | | | | | | | | | | | |
| 6. Interrupt CPU | @ INT | Short | <p>This instruction causes up to 12 interrupts to the CPU to be set. Each bit in the least significant 12 bits of the effective interrupt list (EIL) corresponds to one of the 12 IOP program interrupts. Bit zero is defined as the most significant bit of the effective interrupt list (EIL), and bit 17 as the least significant bit. The table below lists the correspondence between EIL and the IOP program interrupts. Any combination between zero and 12 of these interrupts may be set simultaneously.</p> <table border="1"> <thead> <tr> <th><u>EIL Bit</u></th> <th><u>IOP Program Interrupt Number</u></th> <th><u>Interrupt Level</u></th> </tr> </thead> <tbody> <tr> <td>17</td> <td>12</td> <td>18A</td> </tr> <tr> <td>16</td> <td>11</td> <td>18A</td> </tr> <tr> <td>15</td> <td>10</td> <td>18A</td> </tr> <tr> <td>14</td> <td>9</td> <td>18A</td> </tr> <tr> <td>13</td> <td>8</td> <td>18A</td> </tr> </tbody> </table> | <u>EIL Bit</u> | <u>IOP Program Interrupt Number</u> | <u>Interrupt Level</u> | 17 | 12 | 18A | 16 | 11 | 18A | 15 | 10 | 18A | 14 | 9 | 18A | 13 | 8 | 18A | 4 |
| <u>EIL Bit</u> | <u>IOP Program Interrupt Number</u> | <u>Interrupt Level</u> | | | | | | | | | | | | | | | | | | | | |
| 17 | 12 | 18A | | | | | | | | | | | | | | | | | | | | |
| 16 | 11 | 18A | | | | | | | | | | | | | | | | | | | | |
| 15 | 10 | 18A | | | | | | | | | | | | | | | | | | | | |
| 14 | 9 | 18A | | | | | | | | | | | | | | | | | | | | |
| 13 | 8 | 18A | | | | | | | | | | | | | | | | | | | | |

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Table VIII. MSC Instruction Set (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------------|-----------------------------|---------------------------|--|-------------------------------|-----------------------------|---------------------------|----|--------------|-----------------|----|------------------|-----------------|-----------|---|-----|---|---|-----|---|---|-----|---|---|-----|---|---|-----|---|------------|--|---|------------|--|---|------------|--|---|------------|--|---|------------|--|---|------------|--|--|
| 6. Interrupt CPU (Cont) | | | <p style="text-align: center;">IOP Program Interrupt</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left;"><u>Bit</u></th> <th style="text-align: left;"><u>Number</u></th> <th style="text-align: left;"><u>Interrupt Level</u></th> </tr> </thead> <tbody> <tr><td>12</td><td>7</td><td>18A</td></tr> <tr><td>11</td><td>6</td><td>18A</td></tr> <tr><td>10</td><td>5</td><td>18A</td></tr> <tr><td>9</td><td>4</td><td>18A</td></tr> <tr><td>8</td><td>3</td><td>18L</td></tr> <tr><td>7</td><td>2</td><td>18L</td></tr> <tr><td>6</td><td>1</td><td>18L</td></tr> <tr><td>5</td><td>Unassigned</td><td></td></tr> <tr><td>4</td><td>Unassigned</td><td></td></tr> <tr><td>3</td><td>Unassigned</td><td></td></tr> <tr><td>2</td><td>Unassigned</td><td></td></tr> <tr><td>1</td><td>Unassigned</td><td></td></tr> <tr><td>0</td><td>Unassigned</td><td></td></tr> </tbody> </table> | <u>Bit</u> | <u>Number</u> | <u>Interrupt Level</u> | 12 | 7 | 18A | 11 | 6 | 18A | 10 | 5 | 18A | 9 | 4 | 18A | 8 | 3 | 18L | 7 | 2 | 18L | 6 | 1 | 18L | 5 | Unassigned | | 4 | Unassigned | | 3 | Unassigned | | 2 | Unassigned | | 1 | Unassigned | | 0 | Unassigned | | |
| <u>Bit</u> | <u>Number</u> | <u>Interrupt Level</u> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 12 | 7 | 18A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 11 | 6 | 18A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10 | 5 | 18A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 9 | 4 | 18A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | 3 | 18L | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | 2 | 18L | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | 1 | 18L | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | Unassigned | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | Unassigned | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | Unassigned | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | Unassigned | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | Unassigned | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | Unassigned | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7. Delay | @ DLY | Short | <p>This instruction performs no operation other than delaying the execution of the next instruction (skip to next instruction). The time period delayed is indicated by the effective count (EC).</p> <p>Delay field resolution is 2.0 microseconds (i.e., wait effective displacement microseconds before continuing). The maximum delay is 0.548 seconds. At the end of this delay, the program counter is incremented by one, and the next instruction is executed. The displacement is a positive number in the range of 0 to + 2047. X refers to the index register.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left;"><u>I</u></th> <th style="text-align: left;"><u>Effective Count (EC)</u></th> <th style="text-align: left;"><u>Instruction Format</u></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Displacement</td> <td>@ DLY Count (1)</td> </tr> <tr> <td>1</td> <td>Displacement + X</td> <td>@ DLY Count (1)</td> </tr> </tbody> </table> | <u>I</u> | <u>Effective Count (EC)</u> | <u>Instruction Format</u> | 0 | Displacement | @ DLY Count (1) | 1 | Displacement + X | @ DLY Count (1) | See Text. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <u>I</u> | <u>Effective Count (EC)</u> | <u>Instruction Format</u> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | Displacement | @ DLY Count (1) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | Displacement + X | @ DLY Count (1) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

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Table VIII. MSC Instruction Set (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles |
|---------------|----------|--------|--|-------------------------------|
| 8. Wait | @ WAT | Short | This instruction causes the MSC to enter the <u>Wait</u> state. No more instructions are executed. The MSC program counter is updated to "point" to the next instruction. No other MSC register is changed except bit 0 of stat 4 which is set to zero, and bit 17 of the MSC status register which is set to zero. | N/A |
| 9. Store | @ ST | Short | This instruction shall store a copy of the contents of the accumulator in the memory location whose address is specified by EA. The accumulator is unchanged. The PC is incremented by one. Refer to instruction 11 for the definition of PC, Bit 5 and X. | 3 |
| 10. Self-Test | @ STP | Short | <p>This instruction initiates execution of a special micro program to perform self tests on the hardware supporting the MSC. These tests include checks of:</p> <ul style="list-style-type: none"> a. MSC local store registers b. MSC data flow operations c. Ability of MSC to read and write from memory d. Redundancy management fail discretes e. IOP ROS parity circuit <p>If any faults are detected, the MSC program exception bit is set to 0, and the MSC status register bit 8 is set to 1 (self-test failure). If any case, after completion of these tests, the MSC updates its PC by one and continues with the next instruction.</p> | TRD |

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Table VIII. MSC Instruction Set (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles | | | | | | | | | | |
|---|---------------------|--------|--|-------------------------------|---------------------|----|-------------------|----|--------------------|----|----------------|----|--------------------|---|
| 11. Load | @ L | Short | <p>The full-word operand addressed by EA is loaded into the accumulator. The program counter is incremented by one.</p> <p><u>I</u> <u>Effective Address (EA)</u> <u>Format</u></p> <p>0 PC + Displacement @L Data</p> <p>1 PC + Displacement + X @L Data (I)</p> <p>PC refers to the updated program counter (address of next instruction). Bit 5 is the sign of the two's complement displacement field. The range of the displacement is -1024 to +1023 half-words. X is the index register.</p> | 4 | | | | | | | | | | |
| 12. Load Accumulator With an IOP Status Register (Register operation) | @ LAR | Short | <p>The MSC accumulator is loaded (under program control) with a specified IOP status register. The Register field defines which IOP register is to be loaded.</p> <table border="0"> <thead> <tr> <th><u>Register Field</u></th> <th><u>IOP Register</u></th> </tr> </thead> <tbody> <tr> <td>00</td> <td>Stat 1 (Go/No Go)</td> </tr> <tr> <td>01</td> <td>BCE-MSD indicators</td> </tr> <tr> <td>10</td> <td>Fail Discretes</td> </tr> <tr> <td>11</td> <td>Stat 4 (Busy/Wait)</td> </tr> </tbody> </table> | <u>Register Field</u> | <u>IOP Register</u> | 00 | Stat 1 (Go/No Go) | 01 | BCE-MSD indicators | 10 | Fail Discretes | 11 | Stat 4 (Busy/Wait) | 3 |
| <u>Register Field</u> | <u>IOP Register</u> | | | | | | | | | | | | | |
| 00 | Stat 1 (Go/No Go) | | | | | | | | | | | | | |
| 01 | BCE-MSD indicators | | | | | | | | | | | | | |
| 10 | Fail Discretes | | | | | | | | | | | | | |
| 11 | Stat 4 (Busy/Wait) | | | | | | | | | | | | | |
| 13. Start BCE's (Register) | @ SIO | Short | <p>This instruction starts execution of BCE's by "or-ing" the accumulator with the busy/wait register (stat 4). A one in bit position of the MSC accumulator will place BCE (i) in a busy state. If any of the BCE's designated by the accumulator are already busy (i.e., the BCE bit in the busy/wait register is already set) bit 11 of the MSC status register is set and the MSC program exception bit is set.</p> | 8 | | | | | | | | | | |

Table VIII. MSC Instruction Set (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles | | | | | | | | | | | | | | | | | | | | |
|-------------------------|----------------|----------------|--|-------------------------------|-----------|---------------|---------------|------------|------------|---------|----------------|----------------|---|-----------|------------------|---|---|-------------|--------------------|---|---|---------------|----------------------|---|
| 14. Tally and Skip Zero | @ TSZ | Short | <p>The full-word addressed by EA is incremented by one and rewritten into memory at the same location (EA). If the incremented value is zero, the next instruction is skipped (program counter incremented by two). Otherwise, the program counter is incremented by one.</p> <table border="0"> <thead> <tr> <th><u>I</u></th> <th><u>EA</u></th> <th><u>Format</u></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>PC + Displ</td> <td>@ TSZ Data</td> </tr> <tr> <td>1</td> <td>PC + Displ + X</td> <td>@ TSZ Data (1)</td> </tr> </tbody> </table> <p>PC refers to the updated program counter. Bit 5 same as Instruction 11. X is index register.</p> | <u>I</u> | <u>EA</u> | <u>Format</u> | 0 | PC + Displ | @ TSZ Data | 1 | PC + Displ + X | @ TSZ Data (1) | 7 | | | | | | | | | | | |
| <u>I</u> | <u>EA</u> | <u>Format</u> | | | | | | | | | | | | | | | | | | | | | | |
| 0 | PC + Displ | @ TSZ Data | | | | | | | | | | | | | | | | | | | | | | |
| 1 | PC + Displ + X | @ TSZ Data (1) | | | | | | | | | | | | | | | | | | | | | | |
| 15. Subroutine Call | @ Call | Long | <p>This instruction implements a subroutine call. The current value of the MSC program counter plus the five-bit positive integer delta (Bits 8-12) is stored in the full-word specified by the former lower 18 bits of E.V. This quantity is zero padded on the left to fill the entire fullword. The MSC program counter is then loaded with the sum of the former lower 18 bits of E.V. "and" two.</p> <table border="0"> <thead> <tr> <th><u>I</u></th> <th><u>M</u></th> <th><u>E.V.</u></th> <th><u>Format</u></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Address</td> <td>@ Call Address</td> </tr> <tr> <td>0</td> <td>1</td> <td>(Address)</td> <td>@ Call @ Address</td> </tr> <tr> <td>1</td> <td>0</td> <td>Address + X</td> <td>@ Call Address (1)</td> </tr> <tr> <td>1</td> <td>1</td> <td>(Address + X)</td> <td>@ Call @ Address (1)</td> </tr> </tbody> </table> | <u>I</u> | <u>M</u> | <u>E.V.</u> | <u>Format</u> | 0 | 0 | Address | @ Call Address | 0 | 1 | (Address) | @ Call @ Address | 1 | 0 | Address + X | @ Call Address (1) | 1 | 1 | (Address + X) | @ Call @ Address (1) | 4 |
| <u>I</u> | <u>M</u> | <u>E.V.</u> | <u>Format</u> | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | Address | @ Call Address | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | (Address) | @ Call @ Address | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | Address + X | @ Call Address (1) | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | (Address + X) | @ Call @ Address (1) | | | | | | | | | | | | | | | | | | | | | |

Table VIII. MSC Instruction Set (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles |
|--------------------------------|----------|--------|--|-------------------------------|
| 16. Logical and to Accumulator | @ N | Short | <p>Logically "and" the contents of the MSC accumulator and the contents of the full word operand addressed by the effective address. The result is placed in the MSC accumulator, and the program counter is incremented by one.</p> <p><u>I</u> <u>Effective Address (EA)</u> <u>Format</u></p> <p>0 PC + Displacement @ N Data</p> <p>1 PC + Displacement + X @ N Data (1)</p> <p>Refer to Instruction 11 for the definition of PC, Bit 5 and X.</p> | 6 |
| 17. Add to Accumulator | @ A | Short | <p>This instruction shall add the contents of the accumulator to the full word operand addressed by EA. The result is placed in the accumulator. The program counter is incremented by one.</p> <p><u>I</u> <u>Effective Address</u> <u>Format</u></p> <p>0 PC + Displacement @ A Data</p> <p>1 PC + Displacement + X @ A Data (1)</p> <p>Refer to Instruction 16 for the definition of PC, Bit 5, and X.</p> | 6 |

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Table VIII. MSC Instruction Set (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles |
|-------------------------------------|----------|--------|---|-------------------------------|
| 18. Store Accumulator Full-word | @ STF | Long | This instruction shall store the MSC accumulator in the memory location whose address is defined by I below. In a full-word store (T=0), the least significant bit of the effective address is ignored and the entire accumulator is stored in the addressed full-word. <u>I</u> <u>Effective Value EV</u> <u>Format</u> 0 Address @ STF Address 1 Address + X @ STF Address (1) | 4 |
| 19. Store Accumulator Half-word | @ STH | Long | Same as Instruction 18 except for a half-word (T=1). | 4 |
| 20. Load Accumulator With Full-word | @ LF | Long | This instruction shall load the accumulator with a full-word from the memory location whose address is by the effective value (i.e., Bit 12 (T) = 0). The least significant bit of the effective address is ignored. <u>I</u> <u>Effective Value EV</u> <u>Format</u> 0 Address @ LF Address 1 Address + X @ LF Address (1) | 4 |
| 21. Load Accumulator with Half-word | @ LH | Long | Same as Instruction 20 except bit 12 (T) = 1. | 6 |

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Table VIII. MSC Instruction Set (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles |
|------------------------------|----------|--------|--|-------------------------------|
| 22. Sample for External Call | @ SEC | Short | <p>This instruction shall be used to cause a CPU interrupt of the MSC. @ SEC shall sample register C6 of the MSC local store. If the contents of the MSC register C6 is zero, the MSC shall continue with the next instruction. The @ SEC is a NO operation in this case. If, however, the MSC finds a non-zero in C6, it executes an @ SEC; the MSC takes the contents as a main memory address and stores the following in the 4 full-words addressed by C6:</p> <ol style="list-style-type: none"> a. The current value of the PC +delta +1 shall be stored in main memory whose address is the contents of register C6+6. b. The accumulator shall be stored in main memory at the location specified at the contents of register C6+2. c. The index register shall be stored in the main memory location specified by C6+4. d. The status register shall be stored in the main memory at location C6. The status word and the Go/No-Go bit shall then be reset. e. The contents of the MSC register C6+6 shall then be loaded into the program counter, register C6 shall be reset and the instruction executed. | 2 |

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Table VIII. MSC Instruction Set (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles |
|--|----------|--------|--|-------------------------------|
| 23. Return from External Call | @ REC | Short | <p>This instruction shall be used to:</p> <ol style="list-style-type: none"> Load the accumulator with the contents of the main memory location whose address is the current value of the PC + displacement + 3. Load the MSC index register with the contents of the main memory location whose address is the current value of the PC + displacement + 5. Load the MSC status register with the contents of the main memory location whose address is the current value of the PC + displacement + 1, and then set the MSC Go/No-Go bit to correspond to the value of this bit in the status register. Load the program counter with the contents of the main memory location whose address is the current value of the PC + displacement + 7. | 9 |
| 24. Repeat Until all BCE's are Waiting | @ RAW | Short | <p>This instruction shall cause a delay in MSC program execution until all of a set of specified BCE's have set their busy/wait status bits to 0, "wait" (condition A) or until a maximum wait time has been reached.</p> <p>If condition (A) is reached before the time-out, the MSC skips the next half-word instruction and resumes program execution. If the maximum wait time, (as specified by the maximum repeat count) is reached first, the MSC begins execution of the next half-word instruction.</p> | 13 |

Table VIII. MSC Instruction Set (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles | | | | | | | | | |
|---|-----------------------------|----------------------|--|-------------------------------|-----------------------------|----------------------|---|-------|-------------|---|-----------|-----------------|--|
| 24. Repeat Until BCE's are Waiting (Cont) | | | <p>The maximum wait time has a basic resolution of 33.0 microseconds and is derived from the maximum repeat count. In the nonindex mode, the maximum count of 255 corresponds to a wait time of 8415 microseconds. In the index mode, the maximum count of 262143 corresponds to 8.65 seconds.</p> <p>At the time this instruction is executed, the MSC accumulator is presumed to contain a bit mask specifying which BCE's are to be involved in the test of the desired repeat condition. A 1 in bit <i>i</i> of the accumulator specifies that the status of BCE (<i>i</i>) is to be included in the test: a 0 indicates that BCE (<i>i</i>) can be ignored.</p> <p>The condition "are all specified BCE's WAITING" is tested by logically "and-ing" the MSC accumulator with STAT 4 (the busy/wait register), and testing for all zeros. A 1 in bit <i>i</i> of Stat 4 indicates the BCE (<i>i</i>) is busy; a 0 indicates that it is not. Consequently, if the result of this "and" operation is all zeros, then all the specified BCE's will be in the desired state.</p> <table> <thead> <tr> <th><u>I</u></th> <th><u>Maximum Repeat Count</u></th> <th><u>Instr. Format</u></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Count</td> <td>@ RAW Count</td> </tr> <tr> <td>1</td> <td>X + Count</td> <td>@ RAW Count (1)</td> </tr> </tbody> </table> | <u>I</u> | <u>Maximum Repeat Count</u> | <u>Instr. Format</u> | 0 | Count | @ RAW Count | 1 | X + Count | @ RAW Count (1) | |
| <u>I</u> | <u>Maximum Repeat Count</u> | <u>Instr. Format</u> | | | | | | | | | | | |
| 0 | Count | @ RAW Count | | | | | | | | | | | |
| 1 | X + Count | @ RAW Count (1) | | | | | | | | | | | |

Table VIII. MSC Instruction Set (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles |
|--|----------|--------|--|-------------------------------|
| 25. Repeat Until any BCE's are Waiting | @ RNW | Short | <p>This instruction shall cause a delay in the MSC program until either any of a set of specified BCE's have set their busy/wait status bits to "Wait" (Condition A) or, until a maximum wait time has been reached. If condition (A) is reached before the time-out, the MSC shall skip the next half-word instruction and resume program execution. If the maximum wait time, as specified by the maximum repeat count, is reached first, the MSC begins execution of the next half-word instruction.</p> <p>The condition "<u>are any specified BCE's waiting</u>" is tested by logically "and-ing" the MSC accumulator with the complement of STAT 4 (the busy/wait register) and testing for nonzeros. A 1 bit <i>i</i> of Stat 4 indicates the BCE (<i>i</i>) is busy; a 0 indicates that it is not busy. Consequently, if the result of the above operation is a nonzero value, then at least one BCE from the set is not busy, and the condition is fulfilled.</p> <p>The maximum wait time has a basic resolution of 33 microseconds and is derived from the maximum repeat count. In non-index mode, the maximum repeat count of 255 corresponds to a maximum wait time of 8415 microseconds. In index mode, the maximum possible count of 262143 corresponds to 8.65 seconds.</p> | 13 |

Table VIII. MSC Instruction Set (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles | | | | | | | | | |
|----------------------------------|-----------------------------|---------------------|---|-------------------------------|-----------------------------|---------------------|---|-------|-------------|---|-----------|-----------------|----|
| 26. Repeat until all BCE are Set | @ RAI | Short | <p>This instruction waits a maximum count (Bits 8 through 15) until all of a specified set of BCE's set their BCE MSC indicators. The maximum wait time has a basic resolution of 33 microseconds and is derived from the maximum repeat count. In non-index mode, the maximum repeat count of 255 corresponds to a maximum possible count of 262143 corresponds to 8.65 seconds.</p> <p>At the time this instruction is executed, the MSC accumulator is presumed to contain a bit mask specifying which BCE's are to be involved in the test for the desired repeat condition. A 1 in bits i of the accumulator specifies that the status of BCE (i) is to be included in the test; a 0 indicates that BCE (i) can be ignored.</p> <table> <thead> <tr> <th><u>I</u></th> <th><u>Maximum Repeat Count</u></th> <th><u>Inscr Format</u></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Count</td> <td>@ RAI Count</td> </tr> <tr> <td>1</td> <td>X + Count</td> <td>@ RAI Count (1)</td> </tr> </tbody> </table> <p>The condition "are all specified BCE indicator bits set" is tested by logically "and-ing" the MSC accumulator with the complement of the BCE-MSI indicator register. If the result is all zeros, the desired condition has been reached.</p> | <u>I</u> | <u>Maximum Repeat Count</u> | <u>Inscr Format</u> | 0 | Count | @ RAI Count | 1 | X + Count | @ RAI Count (1) | 13 |
| <u>I</u> | <u>Maximum Repeat Count</u> | <u>Inscr Format</u> | | | | | | | | | | | |
| 0 | Count | @ RAI Count | | | | | | | | | | | |
| 1 | X + Count | @ RAI Count (1) | | | | | | | | | | | |

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Table VIII. MSC Instruction Set (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles |
|--|--------------|--------------|--|-------------------------------|
| <p>27. Repeat until any BCE Indicators are Set</p> | <p>@ RNI</p> | <p>Short</p> | <p>This instruction causes a delay in MSC program execution until any of a set of specified BCE's have set their BCE-MSc indicator bits to 1, Condition A, or until a maximum wait time has been reached.</p> <p>If Condition A is reached before the timeout, MSC skips the next half-word instruction and resumes program execution. If the maximum wait time, as specified by the maximum repeat, is reached first, the MSC begins execution of the next half-word instruction.</p> <p>The condition "are any of the specified BCE indicators set" is tested by logically "and-ing" the MSC accumulator with the BCE-MSc indicator register. If the result is nonzero, the desired condition has been reached.</p> <p>The maximum wait time has a basic resolution of 33 microseconds and is derived from the maximum repeat count. In nonindex mode, the maximum repeat count of 255 corresponds to a maximum wait time of 8415 microseconds. In index mode, the maximum possible count of 262143 corresponds to 8.65 seconds.</p> <p>At the time this instruction is executed, the MSC accumulator is presumed to contain a bit mask specifying which BCE's are to be involved in the test for the desired repeat condition. A 1 in bit i of the accumulator specifies that the status of BCE (i) is to be included in the test; a 0 indicates that BCE (i) can be ignored.</p> | <p>13</p> |

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Table VIII. MSC Instruction Set (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles | | | | | | | | | | | | | | | | | | |
|--|-----------------------|--------|---|-------------------------------|-------------|-----------|-----------------------|-----------|---------|-----------|---------|-----------|---------|-----------|---------|-----------|---------|-----------|---------|-----------|----------------------|---|
| 27. Repeat until any BCE Indicators are set (Cont) | | | <p style="text-align: center;"><u>I</u> <u>Maximum Repeat Count</u> <u>Instr Format</u></p> <p>0 Count @ RNI Count</p> <p>1 X + Count @ RNI Count (1)</p> | | | | | | | | | | | | | | | | | | | |
| 28. Branch on accumulator (conditional branch) | @ BC | Short | <p>This instruction shall select the accumulator register to be tested. If any of the three conditions specified by the condition code field are true, the 8-bit 2's complement signed displacement field is added to MSC program counter. This displacement has a range from -128 to +127 half-word locations. Branches may be made to even or odd half-word locations. The three bits of the condition code field specify the following tests:</p> <p style="margin-left: 40px;">Bit 5 - Register = 0</p> <p style="margin-left: 40px;">Bit 6 - Register < 0</p> <p style="margin-left: 40px;">Bit 7 - Register > 0</p> <p>The following table summarizes all 8 combinations and the resulting tests.</p> <table style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th style="text-align: center;"><u>Condition Code</u></th> <th style="text-align: center;"><u>Test</u></th> </tr> </thead> <tbody> <tr><td style="text-align: center;">0 - 0 0 0</td><td style="text-align: center;">FALSE = DO NOT BRANCH</td></tr> <tr><td style="text-align: center;">1 - 0 0 1</td><td style="text-align: center;">ACC > 0</td></tr> <tr><td style="text-align: center;">2 - 0 1 0</td><td style="text-align: center;">ACC < 0</td></tr> <tr><td style="text-align: center;">3 - 0 1 1</td><td style="text-align: center;">ACC ≠ 0</td></tr> <tr><td style="text-align: center;">4 - 1 0 0</td><td style="text-align: center;">ACC = 0</td></tr> <tr><td style="text-align: center;">5 - 1 0 1</td><td style="text-align: center;">ACC ≥ 0</td></tr> <tr><td style="text-align: center;">6 - 1 1 0</td><td style="text-align: center;">ACC ≤ 0</td></tr> <tr><td style="text-align: center;">7 - 1 1 1</td><td style="text-align: center;">TRUE = ALWAYS BRANCH</td></tr> </tbody> </table> | <u>Condition Code</u> | <u>Test</u> | 0 - 0 0 0 | FALSE = DO NOT BRANCH | 1 - 0 0 1 | ACC > 0 | 2 - 0 1 0 | ACC < 0 | 3 - 0 1 1 | ACC ≠ 0 | 4 - 1 0 0 | ACC = 0 | 5 - 1 0 1 | ACC ≥ 0 | 6 - 1 1 0 | ACC ≤ 0 | 7 - 1 1 1 | TRUE = ALWAYS BRANCH | 3 |
| <u>Condition Code</u> | <u>Test</u> | | | | | | | | | | | | | | | | | | | | | |
| 0 - 0 0 0 | FALSE = DO NOT BRANCH | | | | | | | | | | | | | | | | | | | | | |
| 1 - 0 0 1 | ACC > 0 | | | | | | | | | | | | | | | | | | | | | |
| 2 - 0 1 0 | ACC < 0 | | | | | | | | | | | | | | | | | | | | | |
| 3 - 0 1 1 | ACC ≠ 0 | | | | | | | | | | | | | | | | | | | | | |
| 4 - 1 0 0 | ACC = 0 | | | | | | | | | | | | | | | | | | | | | |
| 5 - 1 0 1 | ACC ≥ 0 | | | | | | | | | | | | | | | | | | | | | |
| 6 - 1 1 0 | ACC ≤ 0 | | | | | | | | | | | | | | | | | | | | | |
| 7 - 1 1 1 | TRUE = ALWAYS BRANCH | | | | | | | | | | | | | | | | | | | | | |

Table VIII. MSC Instruction Set (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--|-----------------------|--------------|--|-------------------------------|---|--------------|-------|---|--------------|-------|---|--------------|-----------------------|-------------|-----------|-----------------------|-----------|-------|-----------|-------|-----------|-------|-----------|-------|-----------|-------|-----------|-------|-----------|----------------------|--|
| 29. Branch on index (conditional branch) | @ BXC | Short | <p>This instruction shall select the index register (sign extended to 32 bits) to be tested. If any of the three conditions specified by the condition code field are true in regard to the index register, the 8-bit 2's complement signed displacement is added to the MSC program counter. The displacement has a range from -128 to +127 half-word locations. Branches may be made to even or odd half-word locations. The three bits of the condition code field specify the following tests:</p> <table> <tr> <td>Bit 5</td> <td>-</td> <td>Register = 0</td> </tr> <tr> <td>Bit 6</td> <td>-</td> <td>Register < 0</td> </tr> <tr> <td>Bit 7</td> <td>-</td> <td>Register > 0</td> </tr> </table> <p>The following table summarizes all 8 combinations and the resulting tests.</p> <table> <thead> <tr> <th><u>Condition Code</u></th> <th><u>Test</u></th> </tr> </thead> <tbody> <tr> <td>0 - 0 0 0</td> <td>FALSE - DO NOT BRANCH</td> </tr> <tr> <td>1 - 0 0 1</td> <td>R > 0</td> </tr> <tr> <td>2 - 0 1 0</td> <td>R < 0</td> </tr> <tr> <td>3 - 0 1 1</td> <td>R ≠ 0</td> </tr> <tr> <td>4 - 1 0 0</td> <td>R = 0</td> </tr> <tr> <td>5 - 1 0 0</td> <td>R ≥ 0</td> </tr> <tr> <td>6 - 1 1 0</td> <td>R ≤ 0</td> </tr> <tr> <td>7 - 1 1 1</td> <td>TRUE - ALWAYS BRANCH</td> </tr> </tbody> </table> | Bit 5 | - | Register = 0 | Bit 6 | - | Register < 0 | Bit 7 | - | Register > 0 | <u>Condition Code</u> | <u>Test</u> | 0 - 0 0 0 | FALSE - DO NOT BRANCH | 1 - 0 0 1 | R > 0 | 2 - 0 1 0 | R < 0 | 3 - 0 1 1 | R ≠ 0 | 4 - 1 0 0 | R = 0 | 5 - 1 0 0 | R ≥ 0 | 6 - 1 1 0 | R ≤ 0 | 7 - 1 1 1 | TRUE - ALWAYS BRANCH | |
| Bit 5 | - | Register = 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Bit 6 | - | Register < 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Bit 7 | - | Register > 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <u>Condition Code</u> | <u>Test</u> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 - 0 0 0 | FALSE - DO NOT BRANCH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 - 0 0 1 | R > 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 - 0 1 0 | R < 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 - 0 1 1 | R ≠ 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 - 1 0 0 | R = 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 - 1 0 0 | R ≥ 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 - 1 1 0 | R ≤ 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7 - 1 1 1 | TRUE - ALWAYS BRANCH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Table VIII. MSC Instruction Set (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles |
|---|-------------|--------|--|-------------------------------|
| 30. Compare | @ C @ CI | Long | <p>The 32-bit effective value is arithmetically compared to the accumulator. The program counter is incremented by:</p> <p style="text-align: center;">+ 2 If A > E.V. + 3 If A < E.V. + 4 If A = E.V.</p> <p style="text-align: center;"><u>I</u> <u>M</u> <u>Effective Value E.V.</u> <u>Instruction Format</u></p> <p>0 0 Address* @ CI Value 0 1 (Address*) @ C Address 1 0 Address + X* @ CI Value (1) 1 1 (Address + X*) @ C Address (1)</p> <p>This 18-bit quantity is treated as a two's complement number, and the most-significant bit is sign extended 14 places to the left to fill 32 bits.</p> | 6 |
| 31. Load accumulator with MSC status (register operation) | @ LMS | Short | This instruction shall allow the MSC ACC to be loaded under program control, with the 18-bit MSC status word. The format of this status word as it is loaded into the ACC is defined in Table VII. | 4 |

Table VIII. MSC Instruction Set (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles |
|--|----------|--------|---|-------------------------------|
| 32. Set fail discretes (register operation) | @ SFD | Short | This instruction shall allow the MSC accumulator bits 0, 1, 2, 3, and 4 to be logically "ORed" with the fail discrete register. A one in bit <i>i</i> of the accumulator (<i>i</i> = 1, 2, 3, 4) will set the equivalent fail discrete bit. A zero indicates no change. Setting bit zero inhibits the four fail discretes. | 3 |
| 33. Reset fail discretes (register operation) | @ RFD | Short | This instruction allows the fail discretes to be selectively reset. A one in the MSC accumulator bit <i>i</i> (<i>i</i> = 0, 1, 2, 3, 4) will cause bit <i>i</i> in the fail discrete register to be reset. A zero causes no change. Resetting bits zero allows the four discretes to be active | 3 |
| 34. Exchange accumulator and X (register operation) and index register | @ XAX | Short | This instruction shall allow a swap between the MSC accumulator and the index register (X). The lower 18 bits of the accumulator shall go into X and X is sign extended to fill the accumulator. | 8 |
| 35. Load X immediate index register (X) | @ LXI | Short | This instruction allows the data in IMM (sign extend to 18 bits) to be loaded into the index register. Note: The immediate field (IMM) is a 2's complement number, between -128 and +127, and forms a 32-bit constant by sign extending bit 8. The program counter is incremented by one. | 3 |

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Table VIII. MSC Instruction Set (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles |
|---|----------|--------|--|-------------------------------|
| 36. Tally index register (X) | @ TXI | Short | The TXI instruction allows the index register plus IMM to be loaded back into X. If the X is ≤ 0 the next half-word instruction is skipped. (Program counter incremented by 2). Otherwise, the next half-word instruction is executed (program counter incremented by 1). The immediate field is identical to LXI | 4 |
| 37. Tally accumulator to index register | @ TAX | Short | The lower 18 bits of the sum of the ACC and the IMM field are stored in the index register (X). An IMM value of 0 permits X to be loaded directly from the ACC. Immediate field see LXI. | 9 |
| 38. Tally index register (X) to accumulator | @ TXA | Short | This instruction allows X plus IMM to be stored in the accumulator (sign extended 32 bits) if IMM = 0 this instruction allows the sign extended index register to be stored in the accumulator. X is treated as an 18 bit 2's complement number with the sign in its most significant bit. The MSC program counter is incremented by one. The immediate field is defined in LXI. | 3 |
| 39. Tally accumulator immediate | @ TI | Short | This instruction allows the accumulator plus IMM (sign extended to 32 bits) to be loaded into the MSC accumulator. The program counter is incremented by one. The immediate field is as noted in LXI. | 5 |

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Table VIII. MSC Instruction Set (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles |
|---|----------|--------|--|-------------------------------|
| 40. Subtract the accumulator from immediate field | @ SAI | Short | This instruction allows the contents of the accumulator to be subtracted from IMM (sign extended to 32 bits) and loaded into the accumulator. If IMM = 0, a 2's complement of the accumulator is performed. If IMM = 1, a 1's complement of the accumulator is performed (each bit is inverted). The PC is incremented by one. See LXI for immediate field definition. | 7 |
| 41. Load | @ LI | Short | This instruction shall allow the contents of the immediate field (IMM sign extended to 32 bits) to be loaded into the MSC accumulator. The PC is incremented by one. See LXI for immediate field definition. | 3 |
| 42. Normalize and increment the index register | @ NIX | Short | The NIX instruction shifts the ACC left until either the ACC sign bit (bit 0) is one, or the ACC equals zero. Each time the ACC is shifted, the signed immediate value is added to the index register X. The shift and increment operation is done before either test. If the ACC reaches zero, the index register is cleared. | 5 |
| 43. Reset BCE indicator | @ RBI | Short | This instruction resets the specified BCE's BCE/MSB indicator bit to zero. For BCE i, this is bit i of the BCE/MSB indicator register. If the BCE specified in the instruction word is zero, the lower 5 bits of the MSC accumulator (bits 27-31) indicate the desired BCE. After resetting the specified indicator bit, the MSC increments its program counter by 1 and continues with the next sequential instruction. | 4 |

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There are two other MSC visible registers.

- (1) Error STAT (1 bit/processor) Go/No Go (0 - processor has detected error, 1 - no error).
- (2) BCE to MSC indicators (1 bit/BCE). Each BCE can set/clear its own bit under BCE program control.

All addresses are 18 bits long and refer to half-words in main memory. When used to reference a full-word, the least-significant bit of the address is ignored.

3.2.1.5.4.11 MSC Instruction Set. The instruction set is listed in Table VIII. Long instructions shall be located on even main-memory boundaries.

3.2.1.5.4.12 MSC Instruction Formats. Figures 5, 6, and 7 show the MSC instruction word formats. MSC instruction addressing shall be relative to the MSC program counter. The MSC program counter shall be incremented by the specified counts after each instruction execution. MSC instructions shall be in short (16-bit) or long (32-bit) formats. The MSC instruction list is associated with BCE control functions. They shall include the ability to detect BCE status before commanding new or continuing current input/output sequences. The execution times in Table VIII are in terms of the number of MSC microcycles for the minimum instruction option excluding any delays due to memory accessing. The minimum time per MSC microcycle is 2 microseconds.

- Notes:
1. (X) specifies indexing mode bit 4 (0) - No index, (1) - index.
 2. Label is translated into updated PC relative address, -1024 to +1023.
 3. Count has range 0 to 2047 (11 bits).
 4. INT LIST is an 11-bit interrupt designator.
 5. Count has range 0 to 255.
 6. COND has value from 0 to 7 to specify branch condition.
 7. Label is translated into updated PC relative address, -128 to +127.
 8. REG has value 0-7.
 9. IMM (Immediate) has value -128 to +127 (8 bit).
 10. Following OP code mnemonic by @ specifies M=1, direct addressing.
 11. BCE is BCE number -0 to 24.
 12. Label is absolute 18-bit address.
 13. Delta is positive constant between 0 and 31.
 14. Label can be 18-bit immediate or 18-bit address if direct specified.
 15. Bit 12 = 0 (T).
 16. Bit 12 = 1 (T).
 17. Short Format 1.
 18. Short Format 2.
 19. Long Format.

3.2.1.5.5 Bus Control Element. The bus control element (BCE) shall provide for control of data buses, and in conjunction with other IOP elements shall provide the following capabilities:

- a. Execute BCE programs from main memory.
- b. Control the associated MIA.

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- c. Compare and detect interfacing subsystem addresses.
- d. Serve as intermediate I/O data and command execution center between the control element (MSC) and MIA.
- e. Command and/or listen mode mechanization.
- f. Allow for BITE status information accumulation and access for itself and associated MIA.

Assuming that a software-controlled power-up sequence has been executed, a BCE operating in the command mode shall begin execution following an SIO instruction, provided the transmitter and receiver has been enabled, which shall send the PC ready signal to the BCE. The BCE shall sense this condition, fetch instructions from memory, decode the instructions, and take necessary action as a function of the opcode. The BCE shall continue to fetch instructions from memory for execution until a BCE wait instruction is executed. Once started by the MSC, the BCE shall run as an independent execution center.

3.2.1.5.5.1 Functional Modes. BCE's shall operate in two functional modes: (command mode, listen mode), and three functional states (halt, wait, and busy).

3.2.1.5.5.1.1 Command Mode. In the command mode, the BCE shall control its associated MIA for the issuance of commands to the interfacing avionics subsystems. The BCE shall acquire the data to be input to the memory, buffer it, and transfer it to the memory. For output data to interfacing avionics subsystems, the BCE shall acquire memory data, buffer it, and transfer the data to the MIA for transmission to the subsystem.

3.2.1.5.5.1.2 Listen Mode. In the listen mode, the BCE shall control its associated MIA, but only to the extent of processing data to be input to memory (as specified in paragraph 3.2.1.5.5.1.1). The actual command to the interfacing avionics subsystem requesting the input data will be provided by another computer on the data bus with its BCE operating in the command mode. A BCE in the listen mode receives an instruction from the other computer in the command mode. The instruction contains an index to the BCE program counter setting. The listen mode shall not require bit or word synchronization between the command (other) computer BCE and the listening computer BCE. The listen mode mechanization shall be a function of software execution and hardware in the BCE.

Assuming that a software-controlled power-up sequence has been executed and the BCE has executed a WAIT FOR INDEX instruction, a BCE operating in the listen mode shall await an indication from its MIA that a word has been received (provided it has previously been set in a listen mode). When a word is available, the BCE transfers the word from the MIA. The BCE decodes the word to determine if it has the common IOP address and a valid command sync signal. The command shall contain an 8-bit index which shall point to a table of listen mode program counters. The table of program counters is located in main memory at a starting address specified by the listen BCE program counter plus the contents of an n bit displacement field in the wait for index instruction. In addition to the index, the listen command shall contain a 5-bit interfacing avionics unit address (terminal address of the unit sending data). The wait for index instruction will extract this address to be used as an address compare value on the

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received data. The instruction shall indicate to the BCE the data processing requirements when it is received from the interfacing avionics subsystem under MSC control. Instruction execution shall continue until the BCE executes either a WAIT or WAIT FOR INDEX instruction.

In the first case, the BCE awaits a signal from the MSC; in the second case, the BCE monitors its MLA for another listen command.

3.2.1.5.5.1.2.1 Listen Mode Summary. A BCE shall respond to listen commands whenever the following conditions are met:

- a. The BCE executes a WAIT FOR INDEX instruction.
- b. The BCE's MLA receiver is enabled (transmitter disabled).
- c. Another IOP's issues a common IOP command.

3.2.1.5.5.1.3 General BCE Operation. During normal operation, a BCE shall be in one of three states: Halt, Wait, and Busy. In the Halt state, the BCE shall be physically restrained from performing any operations; in the Wait state, the BCE shall wait for an MSC command to execute a program; in the Busy state; the BCE shall execute BCE programs from main store. The function of each state shall be as follows:

3.2.1.5.5.1.3.1 BCE Halt State. When in the Halt state, the BCE shall:

- a. Allow the external world (control panels) to reset BCE operation to a known condition.
- b. Upon the detection of IOP faults, the Halt state shall isolate the BCE and prevent it from performing potentially erroneous operations.
- c. Allow the IOP to reset BCE operation to a known condition.

Entry and exit from the Halt state shall be controlled by the value of a single "BCE Halt" status bit which is part of the IOP halt register. There is one bit for each BCE. As long as this bit is set, the BCE program counter is forced to point to a microinstruction that performs no operation other than to clear the BCE busy/wait bit. The halt bit may be set at any time, and effectively terminates BCE operations.

The signals that set a BCE halt bit shall include:

- a. Master reset discrete from the CPU.
- b. Power-up/down signal.
- c. Setting of the fail latch for this GPC by either the Redundancy Management voting logic or IOP detected errors.
- d. A HALT PROCESSOR PCO from the CPU.

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The first three signal classes shall halt all BCE's.

Exit from this state to the Wait state shall occur only under the following conditions:

- a. Master reset discrete is reset.
- b. Power-up sequence is complete.
- c. Fail latch is reset,

and either an IPL signal or a CPU ENABLE PROCESSORS PCO set to 1 is present. Existence of the IPL signal shall cause the microcode supporting the BCE to perform an IPL sequence before entering the Wait state.

Upon any exit from the Halt state, the BCE program exception bit and the BCE status register shall be cleared.

3.2.1.5.5.1.3.2 BCE Wait State. In the Wait state, a BCE shall be ready to perform a BCE program. The BCE shall enter the Wait state upon exit from the Halt state, as described in 3.2.1.5.5.1.3.1 or by a transition from the Busy state. A BCE shall perform this transition to Wait from the Busy state when any of the following occurs:

- a. A WAIT instruction is executed.
- b. An instruction with an illegal opcode is encountered.
- c. A valid long format instruction is found starting on an odd half-word boundary.
- d. An error occurs, or a halt processor command is issued by the CPU.

In conditions b, c, and d above, a BCE shall perform the following operations before entering the Wait state:

- a. The BCE sets its bit in the program exception register (Stat 1) to 0.
- b. The BCE records the cause of the error in its own BCE register.
- c. The BCE leaves the program counter pointing to the instruction.

A BCE starts execution when it recognizes that the MSC has set its own busy/wait bit to 1 (for BCE i, this is bit i of the busy/wait register--Stat 4). This occurs when the MSC executes a Start I/O instruction with a 1 in bit i of the accumulator. The first BCE instruction in this case is found at the main memory word addressed by the contents of the BCE's program counter. This program counter may have been updated by an MSC load BCE program counter instruction or by a PCO from the CPU to write into the appropriate local store location.

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3.2.1.5.5.1.3.3 BCE Busy State. The Busy state shall be an indication of BCE program execution. When in the Busy state, the BCE shall be in the process of executing a program from main store. A value of 1 in the 0 bit position of the IOP Busy/Wait Register shall indicate this condition.

The Busy state shall be entered only from the Wait state, as described in 3.2.1.5.5.1.3.2. When the transition from wait on Busy occurs, the BCE shall use the value in its program counter to fetch the first instruction from memory and start executing it. The BCE shall continue executing instructions until either a wait instruction or invalid instructions are encountered. In either case, the BCE shall transition back to the Wait state. While the BCE is in the Busy state, it shall not interfere with CPU PC's. While in the Busy state, a BCE may also be in any combination of command/listen modes described in 3.2.1.5.5.1.

3.2.1.5.5.2 BCE Program Counter. The 18-bit program counter (PC) shall contain the memory address location of the next BCE instruction. BCE instructions are executed sequentially unless a BCE branch instruction is encountered.

3.2.1.5.5.3 BCE Instruction Register (IR). The IR shall contain the instruction to be executed by the BCE functions. The IR shall operate with other registers and control logic for the performance of BCE functions.

3.2.1.5.5.4 BCE Base Register (BR). The 18-bit BR shall contain the main memory address where input and output data is located.

3.2.1.5.5.5 BCE Timeout Register (TO). The 18-bit timeout register shall contain the maximum time that a BCE will wait for the first data word to arrive in the receive state.

3.2.1.5.5.6 BCE Status Register (SR). The BCE status register shall contain the results of error and status functions of the BCE and associated MIA's. (Refer to Table IX.)

3.2.1.5.5.7 BCE/MIA Control Logic. The BCE shall provide the necessary control logic and circuitry for controlling its associated MIA.

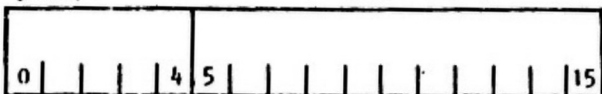
3.2.1.5.5.8 BCE Instructions. All BCE macro instructions shall be accessed from memory via the DMA interface. BCE data access shall be relative to the BCE base register and the instruction displacement field. BCE instructions shall be either short (16-bit), long (32-bit) or extended (64 or 96 bit) Min/Mout instructions. All data transfers shall start on even half-word boundaries. Long and extended instructions shall be located on even main memory addresses. The BCE instruction list shall be sufficient to interface with the serial data bus. BCE instructions shall include but not be restricted to the types specified in Table X. The BCE instruction list

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shall be sufficient to interface with the serial data bus. BCE instructions shall include but not be restricted to the types specified in Table X. The BCE instruction word format are shown in Figures 8 and 9. The execution times in Table X are in terms of number of BCE microcycles for the minimum instruction option excluding any delays due to memory accessing. The minimum time per BCE instruction per channel is 16.5 microseconds.

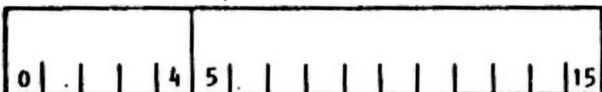
WAIT (#WAT)
 OPCODE
 5 BITS

UNUSED



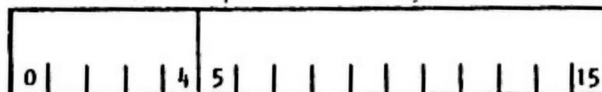
SET INDICATOR BIT (#SIB)
 OPCODE
 5 BITS

UNUSED



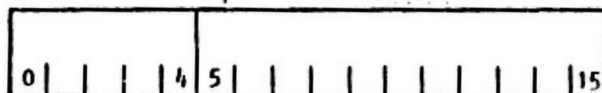
RESET INDICATOR BIT (#RIB)
 OPCODE
 5 BITS

UNUSED



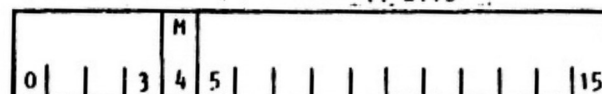
SELF TEST PROGRAM (#STP)
 OPCODE
 5 BITS

UNUSED



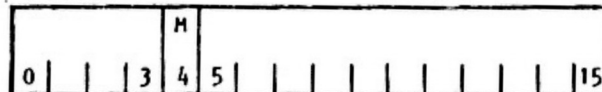
STORE STATUS AND CLEAR (#SSC)
 OPCODE
 4 BITS

DISPLACEMENT
 11 BITS



STORE STATUS (#SST)
 OPCODE
 4 BITS

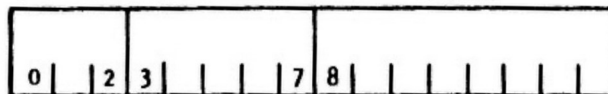
DISPLACEMENT
 11 BITS



RECEIVE DATA WORDS (#RDS)
 OPCODE
 3 BITS

COUNT
 5 BITS

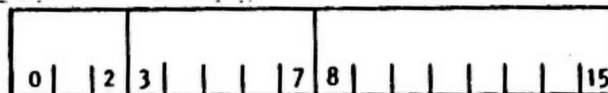
DISPLACEMENT
 8 BITS



TRANSMIT DATA WORDS (#TDS)
 OPCODE
 3 BITS

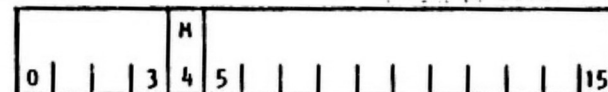
COUNT
 5 BITS

DISPLACEMENT
 8 BITS



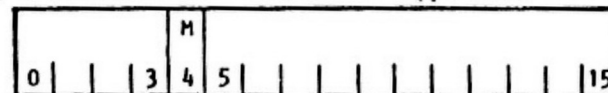
LOAD TIMEOUT REGISTER (#LTO1), (#LTO)
 OPCODE
 4 BITS

COUNT/DISPLACEMENT
 11 BITS



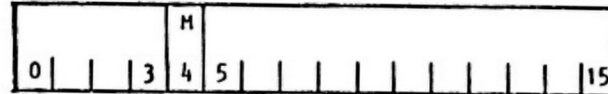
DELAY TIMEOUT (#DLY1)
 OPCODE
 4 BITS

COUNT/ADDRESS
 11 BITS



DELAY ADDRESS (#DYL)
 OPCODE
 4 BITS

COUNT/ADDRESS
 11 BITS



WAIT FOR INDEX (#WIX)
 OPCODE
 5 BITS

DISPLACEMENT
 11 BITS

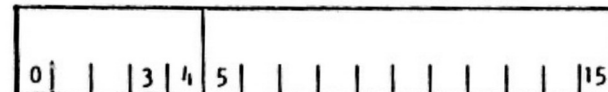


Figure 8. Short BCE Instruction Formats

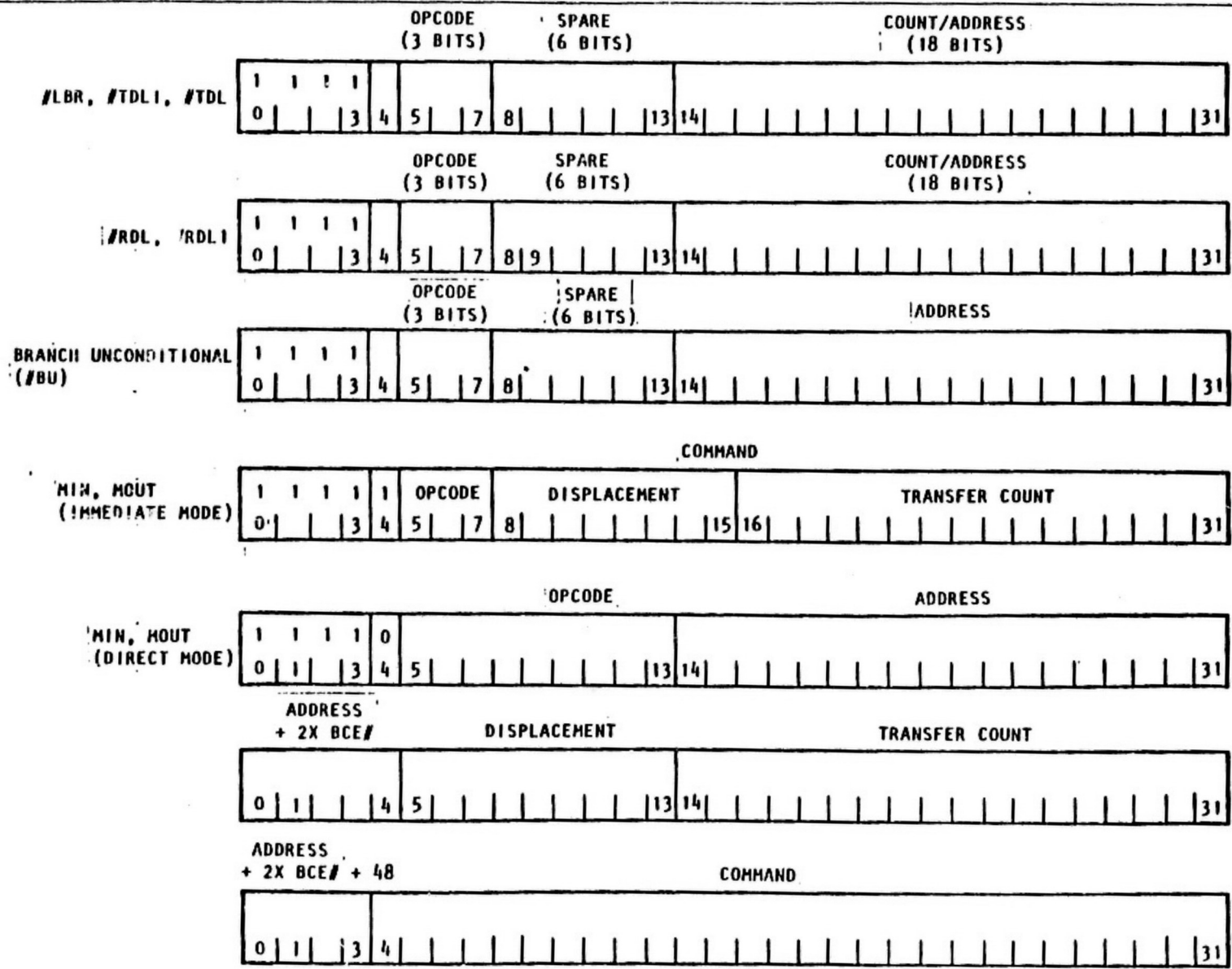
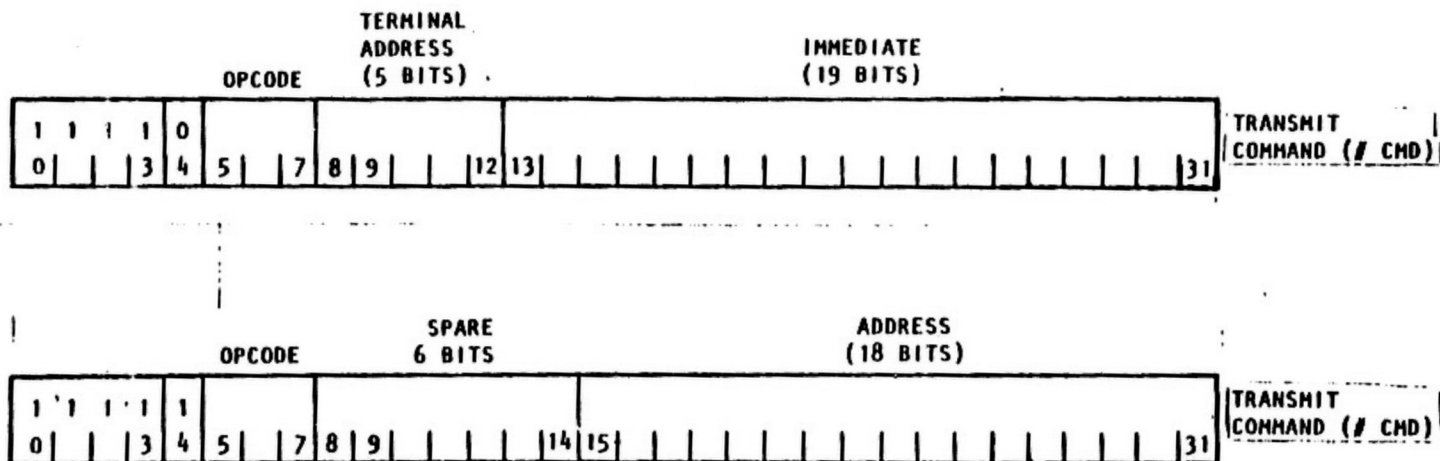


Figure 9. Long BCE Instruction Formats (Sheet 1 of 2)



NOTES FOR MIN/HOUT

- STARTING BUFFER ADDRESS = BASE + DISPLACEMENT
(FOR HOUT, ADDRESS IS TREATED AS A FULLWORD).
- TRANSFER COUNT = NUMERICALLY, 1 LESS THAN THE NUMBER OF BUS WORDS
(EACH 1/2 OF A MEMORY WORD) TO BE TRANSFERRED.
- COMMAND = COMMAND THAT IS SENT FIRST TO THE SUBSYSTEM TO
INITIATE MESSAGE TRANSFER.
- TA = TERMINAL ADDRESS USED BOTH FOR COMMAND AND DATA.
- 03 = OPTION BIT (DIRECT ADDRESSING MODE WITH INDEX
BY BCE NUMBER)

Figure 9. Long BCE Instruction Formats (Sheet 2 of 2)

Table IX. BCE Status Word Format

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|--------|---|---|---|---|---------------------|---|----|----|----|----|----|--------|-------|----|----|----|----|------------------|--------|-------------|-------------|-------------|-------------|-------------|--------|----|----|----|
| | | | T H | P | S | E | V | Terminal Address | | | | | | | S E | ----- | | | | | T G A P | S T | X M T | B T O | I T O | T T O | B T O | M A | I | | |
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |

BCE Status Word Format and Bit Position Bit 0 = MSB

Bit

- 0-2 - Unused - Reserved for future use.
- 3 - TH - Terminal Mismatch: While executing any receive data instruction, a mismatch between the input data words terminal address and the terminal address expected by the BCE was detected. The input data word's terminal address was simultaneously loaded into bits 8 to 12 of this status word.
- 4 - P - Parity: While executing any receive data instruction, an input word with bad parity, invalid Manchester, or bit count error was detected.
- 5-7 - SEV - This three bit field is the logical "or" of the SEV bits, acquired during any receive data instruction, of all input words that were detected to have errors. The S and V bits are inverted prior to the "or" operation.
- 8-12 - Terminal Address - This 5-bit field is the logical "or" of the received terminal's address of all input words that were detected to have errors during execution of any receive data instruction.
- 13 - Unused - Reserved for future use.
- 14 - Unused - Reserved for future use.
- 15 - SE - Sync error: While executing any receive data instruction, an input word with command sync was received.
- 16-20 - Unused - Reserved for future use.
- 21 - TGA² - Transmit gap: While executing any transmit data instruction, the gap time between the command word and first data word or between succeeding data words exceeded 6 μsec between words.
- 22 - ST - Self-test error. A BCE self-test instruction has detected a fault in this BCE.
- 23 - XMT - Transmitter disabled: At some point in the execution of any transmit command/data instruction, the MIA associated with the BCE had its transmitter disabled.
- 24 - Unused - Reserved for future use.

Table X. BCE Instructions

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles |
|-------------------|----------|--------|--|--|
| 1. Message output | #MOUT | Long | <p>Mout consists of a full-word instruction. The first word consists of the main store full-word address and the transfer count. The second word is the command word. The command word is used to send 24-bit commands to an interfacing terminal on the serial bus connection to the current BCE's MIA. (The half-word addressing bit, bit 31, is ignored.) The command word formats are extended (96 bit) and are described in paragraph 3.2.1.5.5.8. The actual transmission of the command is conditional on the BCE's associated MIA being in the command mode (both transmitter and receiver enabled).</p> <p>This instruction directs the bus control element (BCE) to transmit a number of data words (determined by the COUNT) to an interfacing terminal. The location of the first full-word is the sum of the BCE base requester and the displacement field. This may be any full-word location. Succeeding output quantities comes from succeeding full-words in memory. Each full-word is assembled by the BCE into word formats (see paragraph 3.2.1.5.5.8) and transferred to the MIA for transmission. (The MIA adds sync and parity bits.)</p> <p>The terminal address is a copy of the current contents of the terminal number register (TNR), which in turn was loaded during the transmission of the command word. The value in the TNR is thus the present terminal to which this BCE has transmitted a command.</p> | 5 plus 2 times the number of data outputs |

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Table X. BCE Instructions (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles |
|--------------------------|----------|--------|--|---------------------------------------|
| 1. Message output (Cont) | | | <p>If at any time during execution of this instruction the MIA associated with the executing BCE does not have its transmitter enabled, bit 23 of the BCE's status register is set, the Go/No-Go bit for this BCE is set to No-Go and the rest of the instruction is shipped. Completion of data transmission is followed by incrementation of the BCE's program counter by two, and execution of the next instruction.</p> | |
| 2. Message input | #MIN | Long | <p>The @MIN instruction requires two full-words (extended 64 or 96 bit instruction). This instruction results in the transmission of a command (when the BCE is in the command mode) to a subsystem followed by a receive data setup. The first data word to be received is destined for the memory half-word whose address is the sum of the base register plus the 8-bit displacement field.</p> <p>Starting buffer address=base + displacement.</p> <p>The displacement is an integer in the range of 0 to 255, and is right justified when it is added to the 18 bit base register. The LSB of this address is the halfword address. The transfer count field indicates the number of words to be received, assembled into full-words, and stored in memory. Numerically the transfer count is one less than the actual number of words to be received. A count of zero corresponds to one word and 65,535 corresponds to 65,536 data words. Since each memory full-word is constructed from two 16-bit data bus words, up to 32,000 full-words of memory can be loaded with a single MIN instruction.</p> | 5 plus 2 times number of data outputs |

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Table X. BCE Instructions (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles |
|---------------------------|---------------|--------|--|-------------------------------|
| 3. Load base register | #LBR | Long | <p>The 18-bit effective address field is loaded into the current BCE base register. The associated program counter is incremented by two.</p> <p><u>M Effective Address Instruction Format</u></p> <p>0 Address #LBR Address 1 (Address + 2 x BCE#) #LBR @ Address</p> | 1 |
| 4. Load time-out register | #LT01 #LT0 | Short | <p>This instruction loads the current BCE's maximum time-out register (MTR) with the effective count. These bits represent the maximum time that the BCE will wait for the first response word to arrive from a previously commanded terminal. The resolution of the MTR is 16.5 microseconds. Upon completion of this instruction, the BCE increments its program counter by one and executes the next instruction.</p> <p><u>M Effective Count Instruction Format</u></p> <p>0 Time-out #LT01 Count 1 (PC + displacement + 2 x BCE#) #LT0 Address</p> <p>Time-out: Any value between 0 and 2047 (0 to 33.78 milliseconds).</p> <p>PC+ disp: The lower 18 bits of the full-word addressed by PC (updates + address). This allows any count between 0 and 262143 (0 to 4.325 seconds).111</p> | 2 |

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Table X. BCE Instructions (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles |
|---------------------------|----------|--------|--|-------------------------------|
| 5. Wait | #WAT | Short | This instruction shall cause the BCE to enter the Wait state. The BCE's busy/wait bit in Stat 4 is set to 0 (wait). The PC is incremented by one and no further instructions are executed. The BCE is reset to the busy state either by the HSC or upon receiving a listen command, depending on the BCC's present mode. After execution of a WAIT instruction the BCE program counter points to the next sequential instruction. | |
| 6. Self-Test | #STP | Short | This instruction shall initiate execution of a special MICRO Program to perform self-tests on the hardware supporting the BCE that is executing this instruction. | TBS |
| 7. Store status and clear | #SSC | Short | <p>This instruction shall store the BCE's status register in the full-word location addressed by the effective address field. The least significant bit of EA is ignored. After initiating the store operation, the BCE shall clear its status register and set its Go/No-Go bit (Stat 1) to one (GO condition). The BCE shall increment its PC by one and continue with execution of the next instruction in the sequence.</p> <p><u>M</u> <u>Effective Address EA</u> <u>Instruction Format</u></p> <p>0 PC + Displacement #SSC Address 1 PC + Displacement #SSC Address (1) +2 (BCE No.)*</p> <p>*PC is the updated BCE program counter (i.e., the address of the next sequential instruction).</p> | 4 |

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Table X. BCE Instructions (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles |
|----------------------------|----------|--------|--|-------------------------------|
| 8. Store Status | #SST | Short | Same as instruction (#SSC) except that after initiating the store operation, the status registers are not cleared. | 3 |
| 9. Set indicator bit | #SIB | Short | The BCE to MSC indicator bit associated with the BCE that is executing this instruction is set to one. This bit will not change to zero until a reset indicator bit (#RIB) instruction is executed by this BCE. After this bit is set, the BCE's PC is incremented by one, and BCE program execution continues. | 2 |
| 10. Reset indicator bit | #RIB | Short | The BCE to MSC indicator bit associated with the BCE that is executing this instruction is reset to zero. This bit will not change to one until a set indicator bit instruction (#SIB) is executed. After this bit is reset, the PC is incremented by one and program execution continues. | 2 |
| 11. Branch unconditionally | #BU | Long | The 18-bit effective address is stored into the current BCE program counter. The next instruction is found at this designated location, which may be on a full- or half-word boundary. <u>M</u> <u>Effective Address EA</u> <u>Instruction Format</u> 0 Address #BU Address 1 (Address + 2 x BCE#) #BU@ Address | 3 |
| 12. Wait for index | #WIX | Short | This instruction is used primarily for listen mode and is distinct from #WAT instruction. When the index arrives in the command word from another computer it is added to the | N/A |

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Table X. BCE Instructions (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles |
|---------------------------|----------|--------|---|--|
| 12. Wait for index (Cont) | | | PC and displacement field for memory access (i.e., PC + 1 + 1 + displacement + index). This is an 18-bit address which indicates the starting main memory address of the table of program counters. #WIX does not rest (and ignores) busy/wait bit unless the transmitter is enabled. The wait for index loop for a common IOF address does not affect the BCE's terminal address register. | |
| 13. Receive data words | #RDS | Short | <p>This instruction directs the BCE to accept a number of input words from its MIA, to do various checks on these words, and to assemble them into 32-bit memory full-words and transfer them to memory. The input word format as received by the MIA is described in 3.2.1.5.6. Execution of this instruction is as follows:</p> <p>(When the BCE is in command mode)</p> <ol style="list-style-type: none"> 1. The input transfer count is extracted from the instruction. This count represents one less than the number of input words to be accepted, and these represent the number of 16-bit main memory half-words accepted. 2. The main memory address for the first input word is computed from the sum of the present contents of the current BCE's base register and the displacement field (Bits 8-15). This displacement may have any value in the range of 0 to 255. The first address is the main memory location for the first data word and may be odd or even. | 4 plus 2 times the number of data inputs |

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Table X. BCE Instructions (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles |
|-------------------------------|----------|--------|--|-------------------------------|
| 13. Receive data words (Cont) | | | <p>3. A WAIT FOR INPUT timer is initialized to the value stored in the maximum time-out register (10). This time is related to the latency of the interfacing subsystem and is on the order of 5 to 20 microseconds.</p> <p>4. The BCE waits for the first input word to arrive from the subsystem through the BCE's MIA. While it is waiting, the BCE decrements its timer at 16.5 microsecond intervals. If the timer reaches zero the BCE will set the time-out bit (bit 25) in its status register, set its exception bit (Stat 1) to 1, and begin executing the next instruction.</p> <p>5. If the BCE receives an input word before its initial time-out, it performs the following input word tests.</p> <ul style="list-style-type: none"> a. Does the input word's terminal address match the number stored in the BCE's terminal address register (TAR). b. Did the MIA detect a parity error. c. Are any SEV bits set indicating subsystem errors. d. Was the sync a data sync and not a command sync. e. If the first input is a command, it is ignored. The input times out and the BCE waits for the next data input. | |

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Table X. BCE Instructions (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles |
|-------------------------------|----------|--------|---|-------------------------------|
| 13. Receive data words (Cont) | | | <p>Detection of any of these errors results in the following error patterns being logically "or ed" with the BCE's status register bits 0 through 15.</p> <hr/> <p style="text-align: center;"> T Terminal 0 0 0 M P S E V Address SE </p> <hr/> <p style="text-align: center;"> 0 2 3 4 5 6 7 8 - - - - 12 13 14 15 </p> <p>Where: TM = 1 if there was a mismatch between the received address and terminal address (see status word for BCE)</p> <p style="margin-left: 40px;">P = 1 if parity error detected</p> <p style="margin-left: 40px;">SEV = the input SEV bits with S and V inverted. Thus, a valid SEV pattern - 101 - forms 000 in the above pattern.</p> <p>Received Terminal Address = The actual interface unit address from the input</p> <p style="margin-left: 40px;">S = 1 if input had command sync.</p> <p>The data transfer is lost, and the BCE enters the Wait state. If none of the above problems exist, the 16 bits of data are stripped from the 24 data bits. If the buffer address computer in Step 2 is odd or a 1-word transfer is desired, this 16-bit half-word is written into memory. Otherwise, it is saved until the next half-word arrives.</p> | |

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Table X. BCE Instructions (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles |
|-------------------------------|----------|--------|--|-------------------------------|
| 13. Receive data words (Cont) | | | <p>The BCE handles each succeeding word in the same manner analogous to that described above. For each input after the first, the BCE will wait at least 6 microseconds after receipt of the last bit of the previous word before declaring an error. If a timeout occurs, bit 26 of the BCE status register is set, the BCE program counter is updated and execution of the next sequential BCE instruction begun. Upon receipt of an input transfer, the BCE decrements its input word count and performs the tests described above. If the previously received 16 bits have not been sent to memory then the next 16 bits are assembled with the previous 16 bits to form a 32-bit full-word for storage in main memory at the buffer address which was updated by 2. This process continues until all words requested are received. The last word received will always be written in main memory even if there is no previously unassembled word. The sequence ends when the transfer count (word count) reaches zero and the last word is stored, upon which the BCE increments its program counter by 1 and executes the next sequential instruction. If an #RDS is started in the listen mode, it will first wait for a command having the same address as that in its terminal match register (TMR) before performing the above operation.</p> | |

Table X. BCE Instructions (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles |
|------------------------|---------------|--------|---|---|
| 14. Receive Data words | #RDLI #RDL | Long | <p>This instruction is executed in a fashion similar to #RDS (number 14) with the following exceptions:</p> <ol style="list-style-type: none"> 1. The displacement from the base is zero. The base must then point to the beginning of the buffer. 2. The input word count ranges from 0 to 262, 143 half-words and may be specified by bits 14-31 of #RDLI or by bits 14-31 of the main memory full-word addressed by bits 14-31 of #RDLI. In the second case, the least significant bit of the address (the half-word selected) is ignored. In either case, the effective word count is one less than the number of words received. 3. Upon instruction completion, the PC is incremented by 2. 4. Time-outs on input data are handled differently than #RDS, due to interblock gaps of data blocks from memory ground computer and the PCM master. Data requests from these units may be in 512 word blocks. A time-out on the first word is still treated as such (see #RDS), but on time-outs on succeeding words, a check is made of the remaining transfer count before declaring a time-out. If the remaining count modulo 512 (block size) is zero, this timeout is treated as the beginning of an interblock gap. Under this condition, the timer is reset to the value located in the maximum timeout register (MTO), and the input wait loop is reentered. A time-out after | <p>#RDLI = 3 + 2 times number of data inputs. #RDL = 4 + 2 times number of data inputs.</p> |

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Table X. BCE Instructions (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles |
|-------------------------------|----------|--------|--|---|
| 14. Receive data words (Cont) | | | <p>4. (Cont)</p> <p>this point is treated as a real time-out error, and the instruction is terminated with bit 27 of the status register set.</p> | |
| 15. Transmit data | #TDS | Short | <p>This instruction shall direct the BCE to transmit a number of 16-bit data words through the BCE's MIA to an interfacing terminal. The main memory location of the first half-word is the sum of the BCE base register and the displacement field. This may be any half-word location. Succeeding output quantities come from succeeding half-words in memory. Each halfword is assembled by the BCE into the format indicated in 3.2.1.4.6 and transferred to the MIA for transmission. The MIA adds data sync and generates parity.</p> <p>The terminal address field is a copy of the contents of the terminal address register of the BCE executing this #TDS. Completion of data transmission is followed by incrementation of the program counter by one and execution of the next instruction.</p> <p>If at any time during execution of this instruction, the BCE is not able to maintain the interword gap time on the bus to less than 10 microseconds (20 μs) then bit 21 of the BCE status register is set, the BCE's program exception bit (Stat 1) is set, the present instruction is terminated, and the next instruction initiated. The cause of gap time excess may be due to:</p> | 2 plus 2 times the number of data outputs |

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Table X. BCE Instructions (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles |
|--------------------------|---------------|--------|--|--|
| 15. Transmit data (Cont) | | | a. Instruction error on hangup at the DMA Channel. b. Memory contention that prevented a data read from being completed in time. | |
| 16. Transmit data | #TDLI #TDL | Long | Execution of this instruction is the same as #TDS (15 above) except: <ol style="list-style-type: none"> 1. The displacement from the base is zero. The base must then point to the beginning of the buffer. 2. The count of input words to be transmitted ranges from 0 to 262, 143 half-words, and may be specified by either bits 14-31 of #TDLI or by bits 14-31 of the main memory full-word addressed by bits 14-31 of #TDL. For #TDL the LSB of the address (the half-word selected) is ignored. 3. Upon completion of #TDLI or #TDL, the PC is incremented by two (2). | #TDL = 4 + 2 no. of data outputs. #TDLI = 2 + 2 no. of data outputs |
| 17. Transmit command | #CMDI #CMD | Long | This instruction is used to send 24 bit commands to a sub-system on the serial bus connected to the current BCE's PHIA. In the immediate mode (#CMDI), the command is found immediately in bits 8 through 31 of the instruction. In direct mode (#CMD), the command is the lower 24 bits of the main store full-word computed from the address field (bits 14 through 31) of the instruction. (The half-word addressing bit, bit 31, is ignored.) | #CMDI = 1 #CMD = 2 |

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Table X. BCE Instructions (Cont)

| Instruction | Mnemonic | Format | Description | Minimum Number of Microcycles | | | | | | | | | |
|------------------------------|--------------------------|--------------------|--|-------------------------------|------------------|--------------------|---|---------|---------------|---|--------------------------|--------------|---------|
| 17. Transmit command (Cont) | | | <p>The actual transmission of the command is conditional on the BCE's associated PMIA's transmitter being enabled and the PMIA not being busy. If either condition is false, the command is not sent, but no error condition is set.</p> <p>After execution of this instruction, the BCE's program counter is incremented by 2, and the next sequential instruction is executed.</p> | | | | | | | | | | |
| 18. Delay timeout: immediate | #DLYI | Short | <p>This instruction simply delays the execution of the next instruction. The time period delayed is the function of the effective count, with a resolution of 16.5 microseconds per count. At the end of this delay the program counter is incremented by one, and the next instruction is executed.</p> <p>Each count of one represents a delay of 16.5 microseconds, the execution time of a BCE micro instruction. Each count of 2 represents a delay of 33 microseconds, the minimum time for a word transmission over a serial data bus.</p> | #DLYI = 2 | | | | | | | | | |
| 19. | #DLY | | <table border="0" style="width: 100%;"> <tr> <td style="text-align: center;"><u>M</u></td> <td style="text-align: center;"><u>Effective</u></td> <td style="text-align: center;"><u>Instruction</u></td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">Timeout</td> <td style="text-align: center;">#DLYI Timeout</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">(PC + DISP)²</td> <td style="text-align: center;">#DLY Address</td> </tr> </table> <p>For the #DLY instruction, the address of the word containing the delay includes the number of the BCE executing the instruction. This allows many BCE's to execute the same program while still retaining the capability to delay for different periods. Note that twice the BCE number is a fullword index.</p> | <u>M</u> | <u>Effective</u> | <u>Instruction</u> | 0 | Timeout | #DLYI Timeout | 1 | (PC + DISP) ² | #DLY Address | DLY = 4 |
| <u>M</u> | <u>Effective</u> | <u>Instruction</u> | | | | | | | | | | | |
| 0 | Timeout | #DLYI Timeout | | | | | | | | | | | |
| 1 | (PC + DISP) ² | #DLY Address | | | | | | | | | | | |

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3.2.1.5.6 Multiplex Interface Adapter (MIA). The MIA provides the communication path between the IOP and the interfacing subsystems as shown in Figure 1. For purposes of the IOP design, the MIA is described in the following paragraphs. The MIA shall be buyer furnished.

3.2.1.5.6.1 Interface Definitions. The electrical interface between the GPC and the MDMA shall be by a fifty (50) pin connector. The pin portion of the connector (IBM P/N 6135907-1) shall be provided by the GPC and the socket portion of the connector (SKD P/N A520A620) shall be provided by the MDMA. The functional and physical interface requirements for the MIA are defined in MC615-0010. The MIA interface connector signal and pin assignment list is given in Table XI.

3.2.1.5.6.1.1 MIA. The MIA shall provide the performance characteristics defined in MC615-0010.

3.2.1.5.6.2 Electrical Power. The electrical power to the MIA shall be as defined in MC615-0010.

3.2.1.5.6.3 Data Bus Interface. The MIA is composed of buyer-furnished devices which will interface with the MIA multiplexing channels. The devices consist of carrier assemblies with two MIA's per carrier.

3.2.1.5.6.3.1 Data Bus Characteristics. The electrical characteristics of the MIA channel shall be as specified in MC615-0010.

3.2.1.5.7 Data Bus. The GPC design shall incorporate a MIA as defined in MC615-0010.

3.2.1.5.7.1 MIA/GPC Interface.

3.2.1.5.7.1.1 Electrical Design. The GPC design shall be compatible with the MIA/Host interface and timing defined in MC615-0010.

3.2.1.5.8 Heat Dissipation. The GPC design shall provide for MIA heat dissipation as defined in MC615-0010.

3.2.1.5.9 Mechanical Design. The MIA shall be installed in accordance with the mounting provisions as defined in MC615-0010. The MIA shall not be subjected to vibration levels in excess of the criteria defined in MC615-0010.

3.2.1.5.10 Data Bus Interconnection. Unless otherwise approved by the buyer, the interface cable from the GPC LRU output connector J5 to the data bus coupler pin connections shall be two-conductor, twisted, shielded, jacketed cable having a distributed capacitance of less than 22 pf per foot and an impedance of 70 ohms plus or minus 10 percent.

3.2.1.5.11 Data Bus Transfer Methods.

3.2.1.5.11.1 Modulation. The modulation shall be in accordance with MC615-0010.

3.2.1.5.11.2 Data Code. The data code shall be in accordance with MC615-0010.

3.2.1.5.11.3 Data Rate. The data rate shall be in accordance with MC615-0010.

3.2.1.5.11.4 Message. The message shall be in accordance with MC615-0010.

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Table XI. IBM MDMLA Interface Connector Signal List

| MDMLA Connector - IBM Part No. 6135907-1 | | |
|--|----------------|-------------------------------|
| Pin No. | Mnemonic | Name |
| -1 | BUSY (B) | MIA Busy Not |
| -2 | ME (B) | MIA ERROR (Valid Word Not) |
| -3 | RCS (B) | Received Command Sync |
| -4 | SDI (B) | Receive Data (Serial Data In) |
| -5 | +5 Vdc (Logic) | |
| -6 | Power RTN | |
| -7 | +5 Vdc (Logic) | |
| -8 | Power RTN | |
| -9 | | |
| -10 | ITC | Power Supply Clamp |
| -11 | | |
| -12 | | |
| -13 | Power RTN | |
| -14 | -12 Vdc | |
| -15 | Power RTN | |
| -16 | 12 Vdc | |
| -17 | Power RTN | |
| -18 | +12 Vdc | |
| -19 | Power RTN | |
| -20 | +12 Vdc | |
| -21 | Power RTN | |
| -22 | | |
| -23 | EOW (A) | MIA End of Word Not |
| -24 | BUSY (A) | MIA Busy Not |
| -25 | Chassis GND | |
| -26 | 16 MHz | 16 MHz Clock |
| -27 | EOW (B) | MIA End of Word Not |
| -28 | TXCS (B) | Transmit Command Sync |
| -29 | TXE (B) | XMIT ENABLE |
| -30 | LDR (B) | Load Data Register |
| -31 | REG CLK (B) | Register Clock |
| -32 | SDO (B) | XMIT Data (Serial Data Out) |
| -33 | TXE (A) | XMIT ENABLE |
| -34 | SDI (A) | Receive Data (Serial Data In) |
| -35 | LDR (A) | Load Data Register |
| -36 | REG CLK (A) | Register Clock |
| -37 | SDO (A) | XMIT Data (Serial Data Out) |
| -38 | RCVE (A) | Receive ENABLE |
| -39 | RCVE (B) | Receive ENABLE |
| -40 | BST | Reser. |

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Table XI. IBM MDMA Interface Connector Signal List (Cont)

| MDMA Connector - IBM Part No. 6135907-1 | | |
|---|-------------|-------------------------------------|
| Pin No. | Mnemonic | Name |
| -41 | BUS L (A) | Serial Data Bus Low |
| -42 | BUS H (A) | Serial Data Bus High |
| -43 | BUS C (A) | Serial Data Bus Common (XFM SHIELD) |
| -44 | BUS C (B) | Serial Data Bus Common (XFM SHIELD) |
| -45 | BUS L (B) | Serial Data Bus Low |
| -46 | BUS H (B) | Serial Data Bus High |
| -47 | RCS (A) | Received Command Sync |
| -48 | TXCS (A) | Transmit Command Sync |
| -49 | ME (A) | MIA ERROR (Valid Word Not) |
| -50 | Chassis GND | |

NOTES: Subscript (A) designates signals to left MIA.
Subscript (B) designates signals to right MIA.

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- 3.2.1.5.11.5 Command Word Sync. The command word sync shall be in accordance with MC615-0010.
- 3.2.1.5.11.6 Data Word Sync. The data word sync shall be in accordance with MC615-0010.
- 3.2.1.5.11.7 Transmission Line. The transmission line shall be in accordance with MC615-0010.
- 3.2.1.5.12 Output Circuit Characteristics.
- 3.2.1.5.12.1 Output Circuit Voltage. The output circuit voltage shall be in accordance with MC615-0010.
- 3.2.1.5.12.2 Output Waveform. The output waveform shall be in accordance with MC615-0010.
- 3.2.1.5.12.3 Transmitter Output Noise. The transmitter output noise shall be no greater than 75 MV P-P.
- 3.2.1.5.12.4 Transmitter Off Impedance. The transmitter off impedance shall be a minimum of 6,000 ohms in parallel with 150 picofarads line-to-line from 330 KHz to 1.5 MHz.
- 3.2.1.5.12.5 Output Waveform Distortion. The output waveform distortion shall be in accordance with MC615-0010.
- 3.2.1.5.13 Input Circuit Characteristics.
- 3.2.1.5.13.1 Input Circuit Common Mode Rejection. The input circuit characteristics shall be in accordance with MC615-0010.
- 3.2.1.5.13.2 Input Circuit Impedance. The input circuit impedance shall be a minimum of 6,000 ohms in parallel with 150 picofarads line-to-line from 330 KHz to 1.5 MHz.
- 3.2.1.5.14 DMIA Signal Characteristics Measurement. The DMIA signal output and input characteristics shall be measured at the GPC connector pins noted in Table I GPC connector J5.
- 3.2.1.6 Command and Data Word Formats.
- 3.2.1.6.1 Data Form. Digital data shall be transmitted in binary form compatible with the message and word formats defined in this specification. Any unused bit positions in a word shall be transmitted as logic zeros.
- 3.2.1.6.2 Command Word. A command word shall consist of a command sync waveform, DMIA address, control field, and parity bit (Figure 10).
- 3.2.1.6.2.1 Sync. The command sync waveform shall be as defined in MC615-0010. The width shall be three bit times, with the waveform being positive for the first one and one-half bit times and then negative for the following one and one-half bit times. Note that if the next bit following the sync is a logical zero, the last half of the sync waveform will have an apparent width of two clock periods because of the Manchester encoding.

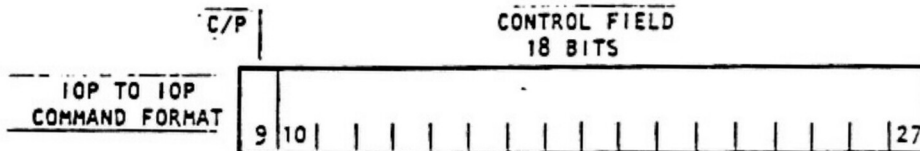
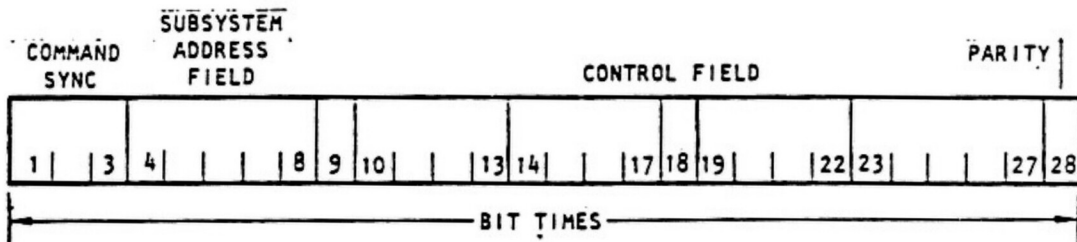
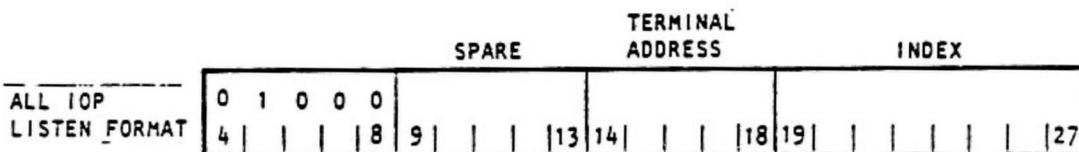
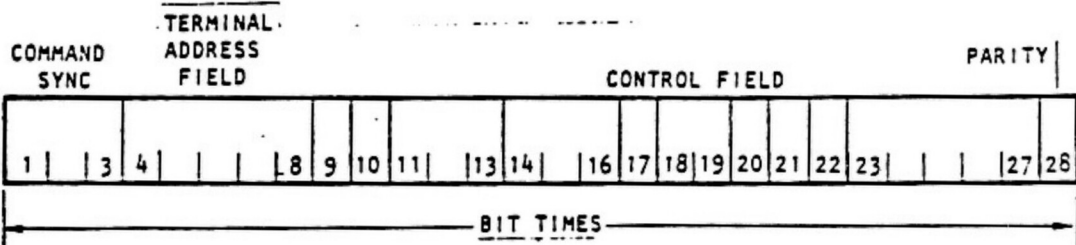


Figure 10. IOP Command Word Formats

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3.2.1.6.2.2 Address. The next five bits following the sync shall be the address of the interfacing subsystem to receive the command. This permits a maximum of 32 DMIA's to be attached to any one data bus, although the maximum is limited to 20 for system considerations. An 01000 code shall indicate a decimal address of 8, which shall be the common IOP address. An all "0's" code shall be a nonvalid DMIA address. The most significant bit of the address shall be transmitted first.

3.2.1.6.2.3 Control Field. Interfacing subsystems that make use of the 19 bits of the control field (following the address field) shall be used as described in Specification MF0004-036. IOP to IOP data transfers use the command word formats shown in Table XII and Figure 10.

Table XII. Command Word Format for the IOP to IOP Data Transfers

| Item | Position | Description |
|------|--------------|--|
| a | 1 through 3 | <u>Command Sync</u> : Three bit nonvalid Manchester code defined in 3.2.1.6.2. |
| b | 4 through 8 | <u>IOP Address</u> : This 5-bit code designates which IOP is to receive the command word and/or data words. Each IOP has a common IOP address which is 01000 and a unique IOP address (station I. D.). |
| c | 9 through 27 | <u>Control Field</u> : A 19-bit program counter setting or index pointer field. |
| d | 28 | <u>Parity</u> : This bit shall be used to indicate odd parity on the entire 24-bit command word. |

3.2.1.6.2.4 Parity. Bit 28 in each command word shall be used for parity over the preceding 24 bits. The parity bit shall be assigned a value, so that the total number "ones" in the word is odd (odd parity).

3.2.1.6.3 Deleted.

3.2.1.6.3.1 Interword Gap Times.

3.2.1.6.3.1.1 IOP-to-Subsystem Transfers. The IOP under CPU control shall issue a single command for data acquisition (input to IOP) or shall issue a command followed by the specified number of data words (output from IOP). The command and data words shall be transmitted in a continuous fashion with an interword gap time of 5.5 plus or minus 0.5 microseconds. These gap times are for command words followed by data and between consecutive data words.

3.2.1.6.3.1.2 Subsystem-to-IOP Transfers. The IOP shall issue a transmit command to the subsystem. The subsystem shall, after command verification, transmit data words back to the IOP from 5 to 25 microseconds after receipt of the last bit of the command word, except for subsystems with long latency times (response time) such as the mass memories and the launch bus (ground equipment, SRB's). In these cases, the subsystem shall transmit data to the IOP within 5 microseconds minimum and 4.1 seconds maximum.

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For block transfers of data consisting of consecutive 512 (16-bit) word blocks, the interblock gap time shall be 5 microseconds minimum and 0.6 seconds maximum. The data words shall be transmitted in a continuous fashion with an interword gap time of from 5 to 7.125 microseconds.

3.2.1.6.3.1.3 IOP-to-IOP Transfers. The IOP shall issue a command to another IOP, followed by data. The command and data words shall be transmitted in a continuous fashion with an interword gap time of 5.5 plus or minus 0.5 microseconds. These gap times are for command words followed by data and between consecutive data words.

3.2.1.6.4 IOP Output Data Word. The IOP data word transmitted to interfacing subsystems shall consist of a data sync waveform, data bits, a check pattern (101), and a parity bit. (See Figure 11 and Table XIII.)

Table XIII. IOP to Interfacing Subsystem Data Word Format

| Item | Position | Description |
|------|---------------|---|
| a | 1 through 3 | <u>Data Sync Field</u> : Three-bit nonvalid Manchester code defined in paragraph 3.2.1.6.4.1. |
| b | 4 through 8 | <u>Terminal Address</u> : This 5-bit code designates which subsystem is to receive data. |
| c | 9 through 24 | <u>Data Field</u> : Sixteen-bit data in binary form. Bit 9 is the most significant bit (MSB). Bit 24 is the least significant bit (LSB). |
| d | 25 through 27 | <u>Check Pattern</u> : This pattern shall be a 3-bit check pattern and shall always be a 101 pattern. (This code is used as an additional error check on transmitted data.) This pattern will be decoded by the interfacing terminal. |
| e | 28 | <u>Parity</u> : This bit shall be used to indicate odd parity on the entire 24-bit data word, excluding sync. |

3.2.1.6.4.1 Sync. The data sync waveform shall be defined in MC615-0010. The width shall be three bit times, with the waveform being negative for the first one and one-half bit times, and then positive for the following one and one-half times. Note that if the bits preceding and following the sync are logic ones, then the apparent width of the sync waveform will be increased to four bit times.

3.2.1.6.4.2 Terminal Address. The next five bits following the sync field shall be the address of the receiving terminal.

DATA WORD FROM IOP TO INTERFACING TERMINAL

| DATA SYNC | TERMINAL ADDRESS | DATA FIELD - 16 BITS | 101 CHECK PATTERN |
|-----------|------------------|----------------------|------------------------|
| 1 3 | 4 8 9 | | 24 25 26 27 28 |
| | | | 1 0 1 P |

DATA WORD FROM INTERFACING TERMINAL TO IOP

| DATA SYNC | TERMINAL ADDRESS | DATA FIELD - 16 BITS | 101 CHECK PATTERN |
|-----------|------------------|----------------------|------------------------|
| 1 3 | 4 8 9 | | 24 25 26 27 28 |
| | | | S E V P |

STATUS WORD FROM INTERFACING TERMINALS TO IOP

| DATA SYNC | TERMINAL ADDRESS | STATUS FIELD | 101 CHECK PATTERN |
|-----------|------------------|--------------|------------------------|
| 1 3 | 4 8 9 | | 24 25 26 27 28 |
| | | | 1 0 1 P |

Figure 11. Interfacing DPS Terminal Data

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3.2.1.6.4.3 Data. The 16 data bits following the address field shall be utilized by the interfacing subsystem. The bit positions shall be as defined in paragraph 3.2.1.6.7.

3.2.1.6.4.4 Check Pattern. Three bits of a coded check pattern shall follow the data field. The check pattern shall be 101 as shown in Figure 11.

3.2.1.6.4.5 Parity. Bit 28 in each data word shall be used for odd parity over the preceding 24 bits. The parity bit shall be assigned a value so that the total number of "ones" in the 24-bit field is odd.

3.2.1.6.5 IOP Input Data Word. The IOP input data word (transmitted to the IOP from subsystems) shall consist of data sync, data bits, an error pattern, and a parity bit.

3.2.1.6.5.1 Sync. The sync waveform shall be as specified in paragraph 3.2.1.6.4.1.

3.2.1.6.5.2 Terminal Address. The next five bits following the sync field shall be the address of the terminal (interfacing subsystem) that is transmitting data to the IOP.

3.2.1.6.5.3 Data. The 16 bits following the address field shall consist of data requested by the IOP. The bit position shall be as defined in paragraph 3.2.1.6.7.

3.2.1.6.5.4 Subsystem Error Pattern. The next three bits (25, 26, and 27) shall be used for subsystem error indications (refer to Table XIV). The error pattern shall be 101 for a no-error condition.

3.2.1.6.5.5 Parity. The last bit in the word indicate odd parity on the preceding 24 bits.

3.2.1.6.6 IOP Input Status Word. A status word shall consist of a data sync waveform, subsystem address, status field, flag bits, and a parity bit (Figure 11).

3.2.1.6.6.1 Sync. The sync waveform shall be as specified in paragraph 3.2.1.6.4.1.

3.2.1.6.6.2 Subsystem Address. The 5-bit address field (following the data sync) shall contain the address of the subsystem sending the status word.

3.2.1.6.6.3 Status Field. The 16-bits (Bits 9 through 24) following the address field shall be utilized for providing status information on the interfacing subsystem.

3.2.1.6.6.4 SEV Error Pattern. Bits 25, 26, and 27, which represent the SEV bits as specified in paragraph 3.2.1.6.5.4, shall be set in a 101 pattern that represents a no-error condition. SEV errors are indicated in data words only, not status words.

3.2.1.6.6.5 Parity. The last bit in the word shall be used for parity over the preceding 24 bits. Odd parity shall be as defined in paragraph 3.2.1.6.4.5.

3.2.1.6.6.6 Bit Position. The most significant bit of a data word shall be transmitted first. The number of bits required to define a quantity shall be 16 bits and shall be consistent with the resolution or accuracy required. In the event double precision quantities (information accuracy or resolution requiring more than 16 data bits) are transmitted, the most significant half shall be transmitted first, followed by the least significant half.

Table XIV. Data Word From Subsystem to IOP (Response Data Word)

| Item | Position | Description |
|------|--------------|--|
| a | 1 through 3 | <u>Data Sync Field:</u> Three-bit nonvalid manchester code as defined in paragraph 3.2.1.6.4.1. |
| b | 4 through 8 | <u>Terminal Address:</u> This 5-bit code is the address of the terminal that is transmitting data to the IOP. |
| c | 9 through 24 | <u>Data Field:</u> Sixteen bits of subsystem data are binary form. Bit 9 is the most significant bit. Bit 24 is the least significant bit. |
| d | 25 | <u>S (Power Transient) Flag:</u> This bit will indicate to the IOP that a power transient has occurred in the subsystem since the last command. A logical one shall indicate no power transient. A logical zero shall indicate a power transient occurred. |
| e | 26 | <u>E (Error) Flag:</u> This bit indicates a parity error has occurred in the subsystem (i.e., a parity error on an MDM serial channel) from an interfacing subsystem. Logical one indicates a parity error. Logical zero, no error. |
| f | 27 | <u>V (Validity) Flag:</u> This bit indicates validity of the subsystem. This bit is set to a logical zero to indicate that the subsystem is unable to transfer data. A logical one indicates valid data. A logical zero, nonvalid data. |
| g | 28 | <u>Parity:</u> This bit indicates odd parity on the entire 24-bit data word (excluding sync). |

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Table XV. Status Word Format Description From Subsystem to IOP

| Item | Position | Description |
|------|--------------|---|
| a | 1 through 3 | <u>Sync Field</u> : Three-bit nonvalid Manchester code. (See paragraph 3.2.1.6.4.1). |
| b | 4 through 8 | <u>Terminal Address</u> : A 5-bit code which shall indicate the address of the terminal which is transmitting the data. |
| c | 9 through 24 | <u>Status Field</u> : This 16-bit field indicates the status of the interfacing terminal. Typical examples of status might be: <ol style="list-style-type: none"> 1. MDM instruction counter in error 2. Illegal command 3. Circuit module errors 4. Serial channel errors 5. Analog channel errors 6. Discrete channel errors 7. Internal power supply status |
| d | 25 | 1 fixed pattern (S)* |
| e | 26 | 0 fixed pattern (E)* |
| f | 27 | 1 fixed pattern (V)* |
| | | *Bits 25, 26, and 27 shall indicate a no-error condition. |
| g | 28 | <u>P (Parity)</u> : This bit indicates odd parity on the 24-bit status word, excluding sync. |

3.2.1.7 Error Handling, Status Monitoring, and Control. The IOP shall provide the error handling, status monitoring, and error control actions for errors detected in the IOP. This capability shall be provided to respond to errors generated by all functional elements of the IOP.

3.2.1.7.1 Data Input Error Handling. The IOP shall detect errors on input data on a message level. Message level detection is defined to mean that the error status word shall distinguish which types of errors occurred during a message reception (transmission of data to this IOP from an interfacing terminal or other IOP). The IOP shall not store erroneous data in main memory nor shall the IOP store valid data received in an incorrect memory location.

3.2.1.7.1.1 Missing Word Error. Whenever a missing word error (gaps in excess of 38 microseconds) is detected (except for the first word of a message) on a word for word basis in a message, the current instruction being executed shall be terminated. The time-out bit (Bit 26, TO) in the BCE status register shall be set, the BCE shall enter the wait state, and status Bit 1 of the BCE (NO-GO bit) shall be set to zero.

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3.2.1.7.1.2 Data Receive Failure. Failure of the first data word to arrive after an IOP command for data within the time specified in paragraph 3.2.1.6.3.1 shall cause the BCE initial time-out (ITO) bit to be set. The current instruction shall be terminated, the BCE shall enter the wait state, and the NO-GO bit (status Bit 1) of the BCE shall be set.

3.2.1.7.1.3 Bit Count, Parity or Manchester Errors. These errors are DMIA detected. When a word is received having bad parity, invalid manchester coding, or less than 25 bits (excluding sync character), the NO-GO bit (Status Bit 1) shall be set and the "P" bit in the status register shall be set. The BCE shall then enter the "Wait State."

3.2.1.7.1.4 Deleted.

3.2.1.7.1.5 SEV Bit Errors. If the SEV bit pattern in the received data word was not a 101 pattern, the respective S, E, or V bit shall be set in the BCE status register. The No-Go bit (status Bit 1) shall be set and the BCE shall enter the wait state.

3.2.1.7.1.6 Terminal Mismatch. Error handling for terminal mismatch (i.e., the designated terminal address requested by the IOP for data does not compare with the received data terminal address) is identical to that for SEV bit errors (paragraph 3.2.1.7.1.5 except the TM bit is set in the BCE status word.

3.2.1.7.1.7 Incorrect Sync. While executing a receive data instruction, an input data word with command sync was received. The SE bit in the BCE status register shall be set. Other actions shall be identical to paragraph 3.2.1.7.1.5.

3.2.1.7.1.8 Data Input Error Summary. Table XVI is a summary of input error actions.

3.2.1.7.2 Command/Data Output Error Handling. The IOP shall detect errors on data or command outputs. The following errors shall be detected as a minimum.

3.2.1.7.2.1 Interword Gap Time. When the interword gap time exceeds six microseconds due to memory contention, the BCE shall set the NO-GO bit (status bit 1 in the BCE status register), and the TO bit in the BCE status word. The transmit data instruction shall be terminated, and the BCE shall enter wait state.

3.2.1.7.2.2 Disabled Transmitter on Transmit Data Instruction. When the IOP tries to output a command or data word to a disabled DMIA transmitter, the BCE shall set the NO-GO bit and the XMT bit in the BCE status word. The current instruction shall be terminated, and the BCE shall enter the wait state.

3.2.1.7.2.3 Data Output Error Summary. Table XVII is a summary of output error action.

3.2.1.7.3 Internal IOP Error Handling. The IOP shall detect internal fault conditions within each functional element of the IOP. As a minimum, the following errors shall be detected and the corrective actions indicated shall be implemented.

3.2.1.7.3.1 Illegal Op Code. Whenever an illegal op code is detected by the MSC or a BCE, the MSC or the BCE shall enter the wait state. The MSC or BCE shall set the NO-GO (status 1) bit in the MSC or BCE status register; and, if an MSC detected error, the MSC shall set the I bit (Bit 29) in the MSC status register. If it is a BCE detected illegal op code, the BCE shall set the I bit (Bit 29) of the respective BCE status register.

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Table XVI. Summary of BCE Error Modes

| Error Type | Detected By | Action |
|--|---------------------------------|---|
| 1. Missing Word | BCE (Look Ahead) | Set NO-GO bit Set Status Bit 26 Terminate Instruction Enter Wait state |
| 2. First Data Receive Failure | BCE Device Response Time-out | Set NO-GO bit Set Status Bit 25 Terminate instruction |
| 3. Bad Parity Invalid Manchester Bit Count Error | MIA | Set NO-GO bit Set Status Bit 4 Terminate instruction Enter Wait state |
| 4. SEV | BCE | Set NO-GO bit Set Status Bits 5, 6, or 7 Terminate instruction Enter Wait state |
| 5. Terminal Mismatch | BCE | Set NO-GO bit Set Status Bit 3 Terminate instruction Enter Wait state |
| 6. Command Sync Data Transmission After First Word | BCE | Set NO-GO bit Set Status Bit Terminate instruction Enter Wait state |

3.2.1.7.3.2 ECC Errors. The ECC scheme is to correct all single errors and detect all double errors. An ECC error is any uncorrectable error that is detected.

3.2.1.7.3.2.1 ECC Error - Instruction. When the CPU detects an ECC error on a DMA instruction read, the CC shall force an illegal op code to the MSC or BCE which shall then execute the illegal op code as specified in paragraph 3.2.1.7.3.1. The CPU shall issue an interrupt to indicate that an ECC error was detected.

3.2.1.7.3.2.2 ECC Error - Data. When the CPU detects an ECC error on a DMA data read, the CC shall inhibit data transfers to local store. The IOP shall continue operations, the BCE shall time-out or hang up, and the MSC shall loop indefinitely. The CPU shall issue an interrupt to indicate that an ECC error was detected.

3.2.1.7.3.2.4 Micro-Store Parity Error. Micro-stores (read only store (ROS)) parity errors shall be detected by ROS decode logic. When a parity error is detected, the IOP shall issue an interrupt to the CPU (Interrupt Number 26 from Table III). The IOP shall enter the reset mode to give positive response to the CPU of the IOP reset condition. The IOP shall also set the control monitor interrupt (Interrupt Number 25 from Table III).

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Table XVII. Summary of BCE Error Modes

| Error Type | Detected By | Action |
|---|------------------------|--|
| 1. Illegal op code | BCE or MSC | BCE or MSC sets NO-GO bit BCE or MSC sets Status Bit 29 Enter Wait state |
| 2. Boundary alignment error | BCE or MSC | Set NO-GO bit Set Status Bit 28 Enter Wait State |
| 3. MSC attempt to load or start a busy BCE | MSC | Set Status Bit 25 (Start I/O) Set Status Bit 26 (Load PC) Set Status Bit 27 (Load Base Register) Begin next instruction |
| 4. DMA cycle time-out | Channel controller | Interrupt CPU Clear DMA channel |
| 5. Queue overflow | Channel controller | Interrupt CPU |
| 6. Voter fail latch | R/M logic | Interrupt CPU, IOP resets and sets C/M interrupt if termination control is ON. |
| 7. ROS parity | ROS decode logic | Interrupt CPU and IOP resets |
| 8. Clock failure | Timing detect logic | Interrupt CPU and IOP resets |
| 9. Watch-dog timer time-out | R/M logic | Interrupt CPU and IOP resets and sets C/M interrupt if termination control is ON. |
| 10. Failure in data flow, local store, channel controller, MIA buffer, or MIA | Self-test instructions | Sets NO-GO bit in the appropriate processor and enters the Wait state |
| 11. ECC Error DMA instructions read | Channel controller | Channel controller forces illegal op code; processor executes illegal op code sequence. |
| 12. ECC error on DMA data read | Channel controller | Abort transfer, processor times-out or hangs up |
| 13. Disabled transmitter on transmit data | BCE | BCE sets NO-GO bit BCE sets Status Bit 23 Terminate instruction Enter Wait state |
| 14. Output interword gap > 6 μ sec due to memory contention | BCE | BCE sets NO-GO bit BCE sets Status Bit 21 Terminate instruction |

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3.2.1.7.3.3 Clock Failure. Clock failure is determined by the IOP timing error detection logic. When a clock failure is detected, the IOP shall issue an interrupt to the CPU (Interrupt Number 27 from Table III) and shall reset. The reset action shall set Interrupt Number 25 (C/M idle) to give a positive indication to the CPU of the IOP reset mode.

3.2.1.7.3.4 Watchdog Timer. When the R/M watchdog timer times-out, the IOP shall issue an interrupt to the CPU (Interrupt Number 23 from Table III) and the IOP shall reset if the termination control latch is ON and shall also issue Interrupt Number 25 (C/M idle) to the CPU to give a positive response to the CPU of the IOP reset condition. Watchdog timer errors are detected by the redundancy management logic.

3.2.1.7.3.5 R/M Voter Failure Latch. The R/M logic shall detect voter failure errors and issue an interrupt to the CPU (Interrupt Number 24 from Table III). The IOP shall also issue Interrupt 25 to the CPU for positive indication of the IOP reset condition if the termination control latch is ON.

3.2.1.7.3.6 Boundary Alignment. When decoding odd boundary instructions (op codes of 1,111 branches to the boundary alignment routine) the BCE or MSC shall enter the wait state upon detecting this type of error. The BCE or MSC program counter shall point to the offending instruction. The BCE or MSC shall set the NO-GO bit (Stat 1) and shall set the status bit in the respective MSC or BCE status word. (Bit 28, BA for BCE, and Bit 28 BA for MSC.)

3.2.1.7.3.7 Load BCE. Whenever the MSC attempts to load a "Busy" BCE with a base register setting, program counter setting, or a start I/O instruction, the MSC shall detect this error condition. The MSC shall take the following action upon detecting these errors:

- a. Set the NO-GO bit (Stat 1) and set the appropriate status bit.
- b. Do not load the BCE with the setting or instruction.
- c. And continue with the execution of the next sequential MSC instruction.

3.2.1.7.3.8 Burst DMA Excess. The IOP enters the burst DMA mode when the number of requests pending is eight or more. The IOP shall stay in this mode until the number of requests in the QUEUE is less than eight.

3.2.1.7.3.9 DMA Timeout. When in the DMA mode, the IOP hangs-up, i.e., the CPU is inadvertently locked out, the channel controller shall issue an interrupt to the CPU (Interrupt Number 34 from Table III). When this error occurs, the IOP shall clear the channel and continue normal operations.

3.2.1.7.3.10 Queue Overflow. When the queue overflows, i.e., more requests pending than specified, the channel controller shall issue an interrupt to the CPU (Interrupt Number 33 from Table III). The IOP, after having issued this interrupt, shall continue normal operations.

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3.2.1.7.3.11 Other Errors. Errors involved with the data flow logic, local store, channel controller, MIA buffer, or the MIA itself, shall be detected by the IOP selftest instructions. Whenever one of these errors are detected, the IOP shall:

- a. Set the NO-GO bit (Stat 1 of Table IV in the appropriate BCE or MSC).
- b. Enter the MSC or BCE Wait state.

3.2.1.7.3.12 Internal IOP Error Summary. Table XVII is a summary of internal error actions.

3.2.1.7.4 Status Monitoring. The IOP shall provide for the BCE and MSC an error status word of at least 32 bits. This status word shall be used to indicate input/output data errors. The status word shall provide sufficient distinguishable states to uniquely identify any or all of the errors specified in 3.2.1.7. The SEV error pattern in the status word shall be the logic OR of all the data words received in the input message. The IOP shall be capable of storing the status word into main memory at the end of the input message. The BCE shall provide the capability to signal the MSC when the errors occur during the receipt of an input data message.

3.2.1.8 Redundancy Management.

3.2.1.8.1 Redundancy and Fail-Soft Operation. The orbiter avionics system design includes redundant computer elements and subsystems for fail-operational/fail-safe (FO/FS) requirements. The GPC design shall allow no single failure that results in the transmission of information on more than one interfacing subsystem channel. To satisfy flight safety requirements, the GPC shall be fail-soft with respect to data transfers on the serial digital multiplexed channels. Fail-soft is defined as the method whereby the GPC shall not interfere with the ability of other GPC's to communicate over any one, any group, or all of the serial digital multiplexed channels. Fail-soft performance shall be provided under any single GPC failure or whenever the input power is out of those limits required for full GPC performance or any combination of single failures, and input power fault conditions. It shall be a GPC design goal to ensure that it will exhibit fail-soft operation for multiple-failure cases. The GPC shall automatically inhibit transmission (not reception) on the serial digital multiplexed channel whenever hardware BITE indicates a failure condition that affects more than one channel.

3.2.1.8.2 General System Redundancy Description. The Space Shuttle vehicle will include redundant computer stations and system elements for FO/FS flight safety considerations. Each system-critical data bus will interface with each computer. The bus interface network shall provide each computer with the capability to service normal and backup system control and monitor functions. Control of redundant subsystem elements will normally be distributed among the computer stations. A dedicated-hierarchical assignment will be determined by the computer configuration management software. To facilitate the computer voting algorithms (for failure detection and other considerations) and minimize configuration management response time, each IOP shall control communications on selected data buses and monitor communications on other buses (where the other buses have a different control source). For system essential power conservation cases and for FO/FS considerations, each computer shall be capable of control for all interfacing buses.

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3.2.1.8.2.1 Normal Operations. To satisfy normal operations, the data bus network can be considered as a group of physically and functionally independent sets of buses. Each set of buses will interface with redundant system elements. For a given bus in the set, only one computer shall issue commands. The same computer shall be receptive (via listen mode) to received commands and to data traffic on other buses in the set.

3.2.1.8.2.2 Concurrent Operations. Some system functions will require a concurrency of command-response operations between the computer members of a redundant set. Concurrency within the digital software requirements will be maintained by cooperative mutual synchronization between each computer station. Intercomputer synchronization requirements will not be within the requirements for processing data bus traffic; i.e., interbus data bit or data word synchronization shall not be an IOP requisite. The redundant subsystem responses are not synchronized. The processing of all data bus traffic shall be synchronized with the messages on each individual data bus. In particular, listen mode data bus traffic will be processed independently of other operations.

3.2.1.8.3 Redundancy Management Implementation (RM). The IOP shall include hardware elements to support the redundancy management functions of the computer fault detection, isolation and reconfiguration. The elements shall consist of the master sequence controller, the failure vote transmission logic, the failure determination logic, the transmission termination logic, RM self-test, and the RM discrete receivers and drivers.

3.2.1.8.3.1 RM Functions. The redundancy management functions shall include the following:

- a. GPC fault detection: Compare data received from other computers with its own computer data.
- b. GPC fault isolation: (1) send failure vote indication to other computers, based on the results of the compare process, (2) indicate failures, (3) inhibit IOP transmission of data, (4) inhibit discrete outputs, and (5) inhibit own voting participation.
- c. GPC reconfiguration: Reenable IOP transmission.
- d. Watchdog timer: set to a value for timing out IOP functions.

3.2.1.8.3.1.1 Master Sequence Controller (MSC). Computer fault detection is accomplished by bite hardware and such software techniques as data comparison between computers, its error analysis, and ability to synchronize GPC's. Failure opinions among GPC's shall be communicated to the crew panels by failure vote discrettes. Failure votes shall be stored in a failure vote register under MSC control.

3.2.1.8.3.1.2 Failure Vote Transmission Logic. The contents of the failure vote register shall be transmitted over IOP dedicated discrettes. The failure-vote register-set votes shall be transmitted when a computer is determined as failed. The failure vote register shall be reset by the master power reset signal, specified in 3.2.1.5.3.3.1.

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3.2.1.8.3.1.3 Failure Determination Logic. The failure determination logic shall consist of a voter, watchdog timer, and a fail latch.

3.2.1.8.3.1.4 Voter. The voter shall provide a voter-failed signal whenever at least two of the failure-vote discrete signals are received as logical ones. The hardware logic shall not be dependent on the computer station location.

3.2.1.8.3.1.5 Fail Latch, Time-out Latch, and Computer Fail Discrete. The fail latch contained in the IOP shall be set whenever the voted-failed signal is present. The time-out latch shall be set whenever the watchdog timer time-out signal is present. Both latches shall be reset by the master power reset command. In case of conflict between set and reset conditions, the set conditions shall have priority. The fail latch output or the timer latch output shall be transmitted as a dedicated computer fail discrete from the IOP. The computer fail discrete shall be a logical one whenever the fail latch or the time-out latch are set.

3.2.1.8.3.1.6 Watchdog Timer. A watchdog timer shall provide a time-out signal to set a time-out latch whenever the loaded time is elapsed. The timer shall be loaded and read under PCO/PCI control. The timer shall have a resolution of at least one millisecond. The interval to be measured shall be at least one second.

3.2.1.8.5 RM Self-Test. Sufficient status signals, reconfiguration, PCI control, and test commands loadable under PCO control shall be included in the RM hardware to control and detect failures in the failure vote transmission, failure determination, and transmission termination logic to a probability of 0.99 or better. The test commands shall be used to inhibit the reception of failure votes, the transmission of failure votes, and the computer fail discrettes. Table XVIII is a list of RM status register bit positions and descriptions.

Table XVIII. RM Status Register

| Bit | Description |
|-----------------------------------|-----------------------------|
| 1. Voter/fail latch logic failure | 0 = No fault, 1 = Fault |
| 2. Failure Vote A | 0 = No failure, 1 = Failure |
| 3. Failure Vote B | 0 = No failure, 1 = Failure |
| 4. Failure Vote C | 0 = No failure, 1 = Failure |
| 5. Failure Vote D | 0 = No failure, 1 = Failure |

3.2.1.8.6 RM Discrete Receivers and Drivers. The RM hardware logic shall have the capability to receive four dedicated discrettes and drive five dedicated discrettes. The discrete interface shall be implemented as differential drivers and receivers as specified in paragraph 3.1.2.3.

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3.2.1.9 Computer/Bench Test Equipment Interface. The characteristics of this interface shall be established by the seller.

3.2.1.10 Support Software. The software requirements are defined in MC615-0002.

3.2.1.11 Bench Test Equipment Interface. For performance of ground tests and interfaces, the computer shall be provided with the capability of interfacing with a system monitoring console. Via a unique BTE (bench test equipment) or AGE connector, all computer voltages shall be capable of being externally monitored. All lines shall be properly buffered. Capability shall effect the following functions:

3.2.1.11.1 Memory Load and Verify. Memory load and verify all or any part of memory. The loading operation shall utilize a prewired bootstrap subroutine such that multiple entry keyboard program loading shall not be necessary. Capability for reading out any specific word or all contents of memory shall be provided.

3.2.1.11.2 Single Step MACRO Operation. The computer shall be capable of stopping at end of present instruction and executing one instruction at a time. It must then be capable of resuming normal operation. (Restart.)

3.2.1.11.3 CPU or IOP Wait State. (Stop) the CPU or IOP shall each be capable of being independently placed in an external pause at the conclusion of a specified complete MACRO instruction.

3.2.1.11.4 Memory Dump. Main memory may be dumped in whole or in part over the AGE connector. Capability shall exist to override error correction so that the dump data will show any memory error conditions.

3.2.1.11.5 Registers, PSW, Timers, Etc. Capability shall exist to read and load the various hardware registers.

3.2.1.11.6 Control Store Dump. Capability shall exist to dump in whole or partially the contents of the read only control store memories within the CPU and IOP.

3.2.1.11.7 Single Step - MICRO Operation. The CPU or IOP shall each be capable of being independently stopped at the end of the present MICRO instruction for the purpose of executing one MICRO instruction at a time.

3.2.1.11.8 CPU and IOP Reset. Resets for both CPU and IOP shall be provided.

3.2.1.11.9 Address Lines. Address lines for main memory and CPU and IOP control memories shall be available for the purposes of address comparisons.

3.2.1.11.10 Data Lines. A set of data lines commensurate with the data item being addressed in 3.2.1.11.9 shall be available. Control store data shall not be dynamically available.

3.2.1.11.11 Dynamic Data Extraction. The data item present on the lines in 3.2.1.11.10 may be read in real time along with its address as specified in 3.2.1.11.9.

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3.2.1.11.12 Error Status Conditions. Various error conditions shall be available as they occur for both hard and soft errors as detected by hardware and/or microcode in the CPU and IOP.

3.2.1.11.13 Status Indications. Various hardware and software status indications shall be available from the CPU and IOP. These indicators shall include at least the following:

- Stopped/running conditions
- Pipe Line status.

3.2.1.11.14 Forced Execution of Micro Operations. This item is for potential diagnostic purposes and details are TBD. the general requirement is to be able to load the internal CPU and IOP micro control registers and force the execution of these micro instructions one at a time (single stepped).

3.2.1.11.15 TBD.

3.2.1.12 Initial Program Loading (IPL). When the GPC is installed in the avionic system the methods of loading programs are: (1) mass memory readout and (2) via the launch bus by ground support equipment.

3.2.1.12.1 IOP Control. The IOP shall provide for control of IPL from the selected external source to the GPC main memory. This control shall be via IPL microcode instructions and discrettes assigned for this function. The discrete interface control shall be:

- a. GPC-IPL discrete: Switch input from the pilot's panel when activated in the presence of "HALT" shall initiate IPL.
- b. Halt discrete input: When true, this discrete shall cause an IOP reset and shall cause the CPU to enter the system reset mode. The IOP reset shall cause the actions in 3.2.1.5.3.3 to be completed.
- c. Standby discrete input: When true, this discrete shall cause the IOP to enter the standby mode.
- d. Run discrete input: When true, the discrete shall cause the IOP to enter the run mode.
- e. IPL indicator: The IOP shall issue an IPL indication when the IOP is in the IPL mode.
- f. Mass Memory I ready - Discrete input to each IOP to determine the availability of the Mass Memory. This discrete will be used by the IOP logic to gain access to the Mass Memory when it becomes available. If more than one block of program/data is being loaded during IPL, the blocks will be chained and the Mass Memory will keep the "Mass Memory Ready" discrete active and will not relinquish control until the complete load module is transferred into the Computer Memory. This discrete will also be readable by the Computer software to determine Mass Memory availability for normal operational use.

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g. Mass Memory 2 ready - Same as "Mass Memory 1 ready" above; but for Mass Memory 2.

3.2.1.12.2 IPL Ground Rules.

- a. At least one mass memory will be operational before a computer is selected for IPL.
- b. One computer will be IPL'd at a time.
- c. Once the defined program load has been completed, verification of data shall be by check sum.
- d. Before loading the computer memory, the entire memory will be conditioned with a SVC (Supervisor Call) code to provide a trip if program execution deviates from expected flow.
- e. All data read from the mass memory will be storage protected, computer storage shall be loaded beginning at memory location zero.
- f. The computer will operate required bus interfaces for loading as in the normal operational mode except that the computer will control storage protection of data being transferred into memory over the DMA channel.
- g. Any IPL error shall leave the IPL indicator set. The indicator shall be resettable only by recycling power.
- h. The IPL load module shall be variable from 2 to 72 blocks of 512 halfwords under control of a constant to be supplied as part of the load module.

3.2.1.12.3 IPL Initial Conditions. The following conditions shall be initiated prior to loading a computer memory:

- a. GPC must be previously powered-on.
- b. GPC shall be in the Halt state by a discrete input from the crew panel.
- c. The IPL mode shall be set and latched by an IPL discrete input from a momentary (crew panel) switch.
- d. IPL discrete output indicator shall be in the true state.
- e. The DMA store protect control shall be ON.
- f. At least one mass memory (MM) IPL select discrete input shall be TRUE.
- g. The selected mass memory ready signal shall be in the True state (ON).

3.2.1.12.4 IPL Mechanization. The GPC IPL mechanization shall include as a minimum the following:

- a. Initiated from crew panel.
- b. IOP control uses MM1 or MM2 as the IPL source.
- c. All data shall be store protected.

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d. IPL load module size shall be 18,432 fullwords maximum.

e. Mass memories shall be dedicated to:

(1) BCE 18 for MM1

(2) BCE 19 for MM2

3.2.2 Physical Characteristics. The GPC shall have the following physical characteristics.

3.2.2.1 Envelope. The envelope of the GPC shall not exceed the dimensions of one ATR envelope as shown in Figure 12 Connectors shall be on the face indicated by Figure 4.

3.2.2.2 Mounting. The mounting provisions of the GPC shall be as shown in Figure 3.

3.2.2.3 Weight. The weight of the GPC LRU including all control elements, modules, and power supplies shall not exceed 70 pounds.

3.2.2.4 Volume. The computer volume with 262,144 full words of memory shall not exceed one LRU. The LRU case packaging shall conform to one standard ATR size.

3.2.2.5 Center of Gravity and Moments of Inertia. The center of gravity (CG) shall be determined in three axis from a defined reference datum. The moments of inertia shall be calculated about the CG of the GPC.

3.2.3 Reliability. The following reliability requirements shall be included in the design of the GPC.

3.2.3.1 Fasteners. Threaded ports and fasteners shall be positively locked to prevent loosening during service.

3.2.3.2 Circuit Protection. GPC circuit protection shall be provided in accordance with Specification MF0004-002.

3.2.3.3 Parts Selection. Electrical, electronic, and electromechanical piece parts in new and modified portions of the computer design are to be selected and applied in accordance with the Orbiter Project Parts List (OPPL), MF0004-400. Off-the shelf (OTS) elements of the computer design are to be identified by the seller, and necessary specific exemptions from OPPL requirements for OTS elements will be authorized by the buyer after review of seller's EEE parts selection, application, and experience. Non-exempted OTS elements of the design are to meet the same requirements as new and modified portions of the design.

3.2.4 Maintainability.

3.2.4.1 Design Allocations. The design shall satisfy the following maintainability allocations:

a. The GPC shall have the capability in conjunction with ground support equipment (GSE), if applicable, to isolate any discrepancy to the malfunctioning LRU or onboard verification of LRU functional performance after installation within five minutes.

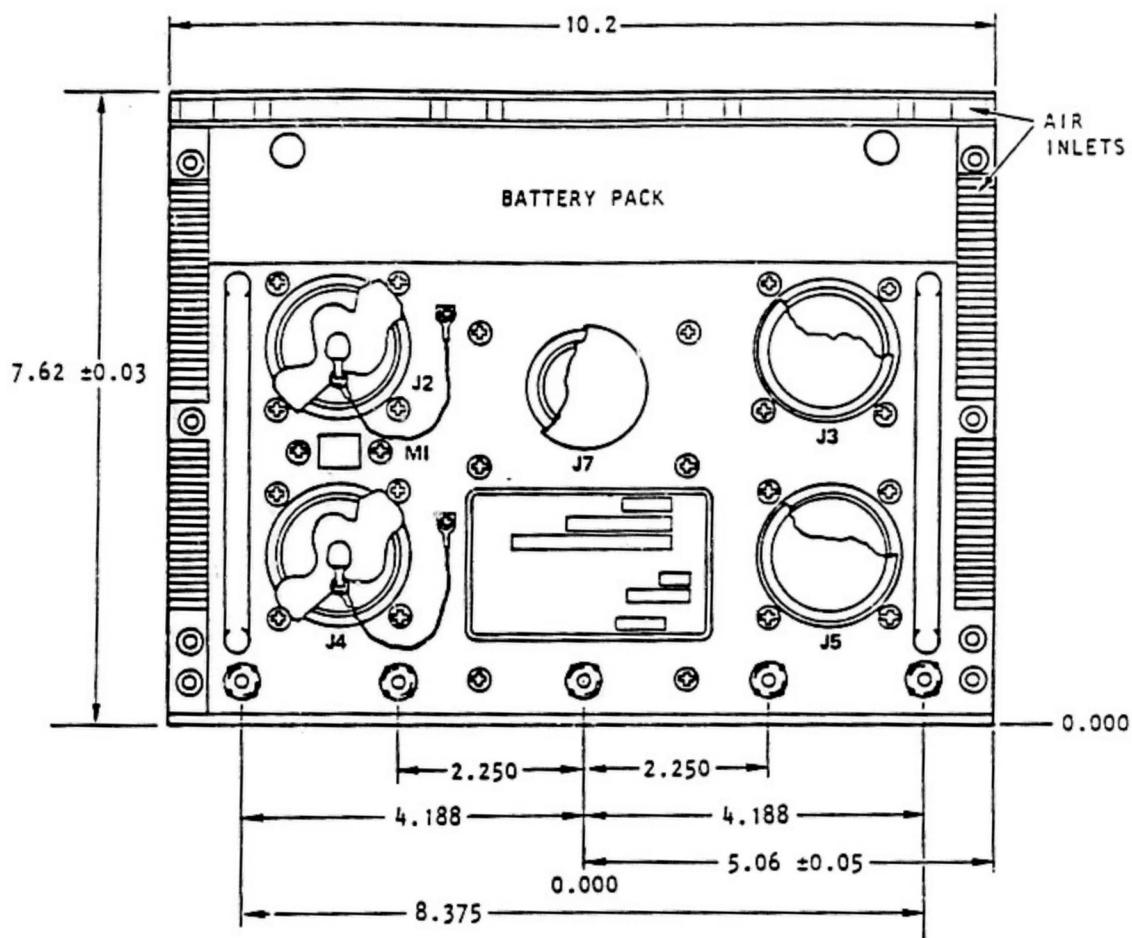


Figure 12. General Purpose Computer Configuration
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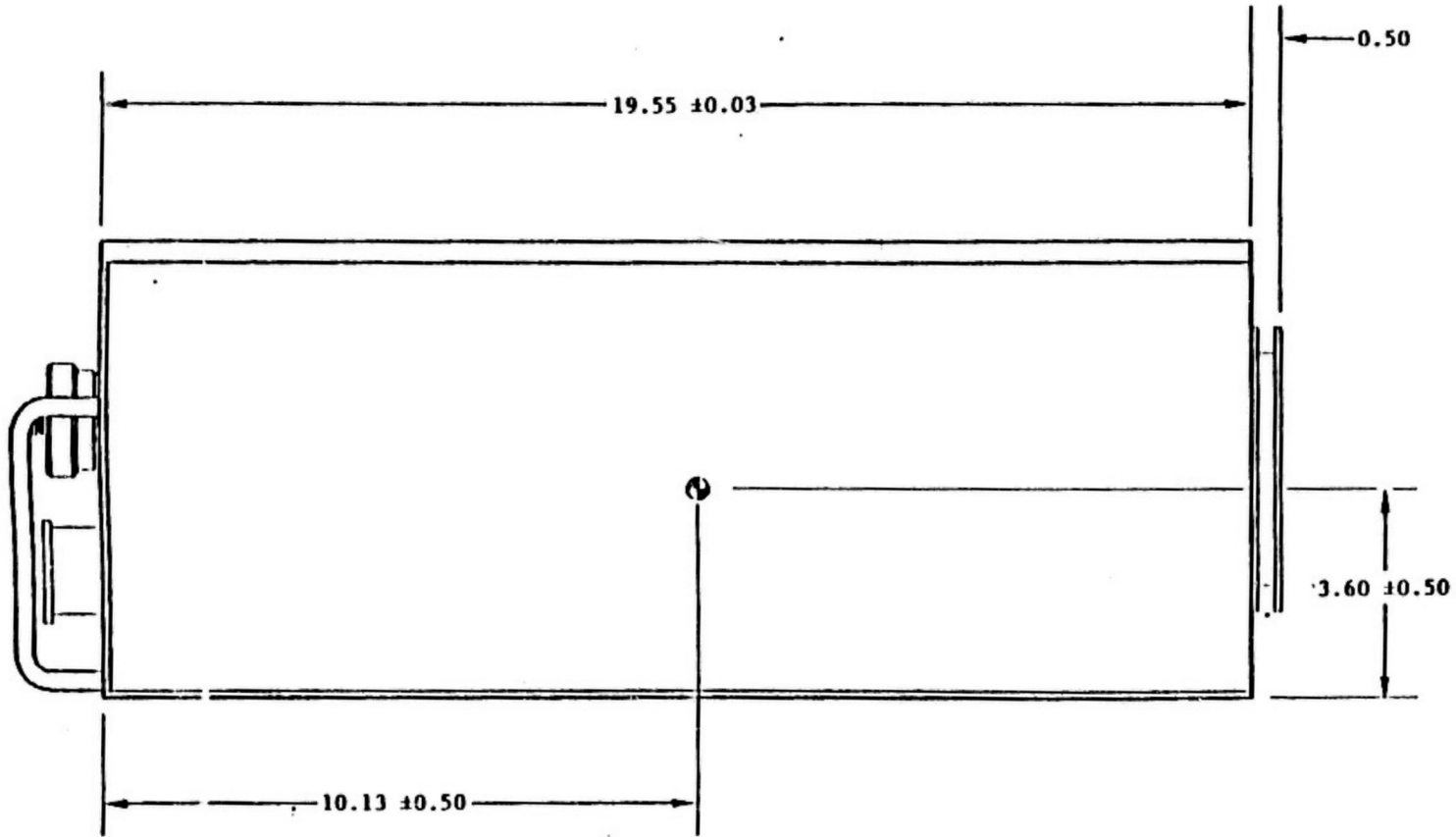


Figure 12. General Purpose Computer Configuration
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- b. Scheduled maintenance required for equipment shall be limited to replacement of time/cycle sensitive equipment.
- c. The GPC shall be designed to allow failed subassemblies to be replaced in 0.3 hours or less after failure identification.
- d. The GPC shall be designed to allow bench verification of the GPC interfaces and internal functions within 0.5 hours using suitable support equipment in the maintenance area.
- 3.2.4.2 Design Features. The design shall incorporate the following maintainability features.
- 3.2.4.2.1 Maintenance.
- a. The GPC shall not require scheduled maintenance except as noted in 3.2.4.1(b).
- b. The GPC shall be designed to preclude the use of special tools and equipment for site maintenance and repairs. Special tools, if required, and approved by the buyer, shall be designed to withstand the intended use throughout the life of the equipment.
- c. The GPC shall be designed to satisfy the requirements of an LRU.
- d. LRU's shall be designed so that routine corrective maintenance can be accomplished by the replacement of Shop Replaceable Units (SRU's).
- e. SRU's shall be designed so that maintenance actions not requiring extensive refabrication, refurbishment, or overhaul can be accomplished at the shop level of maintenance. Corrective maintenance of SRU's shall be accomplished by the replacement of minor subassemblies or piece parts. SRU's shall be designed to preclude the loss or dropping of hardware which could cause internal damage or affect the LRU's serviceability or increase maintenance time.
- f. Scheduled maintenance of the GPC when in its installed configuration shall be limited to the maintenance and repair areas.
- g. The necessity for any maintenance servicing or checkout tasks, other than built-in test capability, to be accomplished during flight is prohibited.
- h. Items requiring forming (rolling) or welding of attaching surfaces at disassembly points shall be designed so that removal of material upon disassembly during repair, overhaul, or modification does not destroy or render unusable any repairable subassemblies or components of the item.
- i. Suitable warnings shall be provided on instruction plates or service placards if hazardous conditions exist when maintenance is performed.
- j. The GPC design shall not require preinstallation acceptance checkout prior to use.
- k. The GPC shall be designed so as to preclude the need for on-line support equipment.

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1. Maintenance Materials. No materials or procedures shall be required for maintenance activities at any assembly level of equipment that will result in requirements for highly specialized skills, sophisticated manipulative techniques, or extended maintenance task times.
- m. Scheduled Overhaul. The computer shall not require scheduled overhaul with the exception of battery replacement.
- n. Calibration/Adjustment. Adjustment or calibration of the computer shall not be permitted at the LRU level. Adjustments shall be permitted at the SRU level as a result of SRU repair actions.
- o. Diagnostic/Modularity Capability. The computer shall be logically and electrically designed with modular features integrated with BITE to facilitate the location and replacement of malfunctioning modules through ground diagnostic programming.
- p. Time Totalizing Meter. Each GPC shall be provided with a time totalizing meter mounted on the front. The meter shall conform to MIL-M-7793. The glass shall be shatterproof.

3.2.4.2.2 Installation.

- a. The equipment design shall physically prevent the incorrect installation of modules and submodules. Clearly visible color coding and labeling in close proximity to maintenance disconnect points shall be used to facilitate removal and replacement of any subassembly level of equipment.
- b. Components shall be mounted in a manner to avoid blind adjustments.
- c. Mechanical retention devices for equipment/components shall not require safety wiring.
- d. If a GPC is mounted and secured by bolts where the component must be held in place until the bolts are engaged, pilot keyhole mounting or similar installation aid shall be provided.
- e. Threaded fasteners used for securing a single component, where practical, shall be the same type, size, and tensile strength.
- f. Assembly/subassembly installations shall be designed such that accessibility to threaded fasteners may be accomplished without the use of universal joints, angular extensions, handle extensions, or combinations thereof, in conjunction with torque tools.
- g. Captive fasteners shall be utilized to hold LRU's.

3.2.4.2.3 Accessibility.

- a. Electrical connectors shall be accessible without disassembly or removal of functional equipment or components.

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- b. Servicing and test points shall be clearly marked and shall be accessible without requiring removal of access plates or covers except service caps. Calibration controls shall be accessible and clearly marked for major functions.
- c. All fasteners on a single access cover shall be of the same length, diameter, and type.

3.2.4.2.4 Replacement.

- a. Mounting provisions shall permit SRU removal (except for page cable assemblies) and replacement without disconnecting any equivalent level SRU in the line replaceable unit. If removal of a LRU structural element is required for access, such removal shall not affect electrical or mechanical alignment, nor shall the mechanical strength of the unit be impaired to the point that bending of the unit, its assemblies, electrical harnesses, or plumbing attachments will occur during normal bench handling of the unit.
- b. Attach fittings for components routinely removed shall be operable without hand tools and shall be accessible without requiring removal of access panels or covers.

3.2.4.2.5 Handling.

- a. Handling provisions shall be provided on LRU's in accordance with MIL-STD-1472, except for the LRU handle.

3.2.4.2.6 Miscellaneous.

3.2.4.2.6.1 Design Allocations.

- a. The computer shall be designed to allow bench verification of the module interfaces and control logic functions within 30 minutes, using suitable test equipment.
- b. The computer shall be designed to allow failed subassemblies or modules to be replaced within 0.3 hours or less after failure detection and LRU removal.

3.2.4.3 Self Test Provisions.

3.2.4.3.1 LRU Peculiar Requirements. Provisions shall be incorporated to detect and report failure of redundant capability. This level of failure detection is required for both automatic reconfiguration and for those cases where reconfiguration is under external control.

- a. Means of indicating the validity of data received via the serial digital data bus interface shall be provided.
- b. Capability to provide status of redundant functional paths in the installed flight configuration shall be provided.
- c. Provisions to enable loop test verification utilizing the integrated avionics system shall be incorporated in the GPC.

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- d. The GPC shall provide failure detection of peculiar failure modes.
- e. Means of indicating operating modes (operational, acquisition, self-test, and stand-by) shall be provided.
- f. The GPC shall include the capability to accomplish diagnostic or self-test verification of stored logic.

3.2.4.3.2 Implementation. Built-in-test may be implemented utilizing an appropriate mixture of Built-In-Test-Equipment (BITE), self-test circuitry, or by providing adequate test points at the electrical interface. It may be designed for automatic continuous, or iterative operation. However, it shall be designed to operate in all modes and conditions in both flight and ground operation. The type of implementation shall be selected in accordance with the following restraints:

- a. Continuous testing or monitoring shall be used only when it can be performed simultaneously with operational use and where such testing does not degrade operational performance.
- b. Iterative testing not under computer control shall not interfere with equipment's operational performance.
- c. Any technique that requires external control or evaluation shall require buyer approval prior to implementation.

3.2.4.3.3 Test Circuitry Failure. Failure of the test circuitry shall be fail-safe and shall not induce failures in other portions of the LRU, or in another LRU.

3.2.5 Environments.

3.2.5.1 Operational. The GPC shall be capable of meeting the operating performance requirements specified herein during and after exposure to any feasible combination of the following conditions:

- a. Temperature
 - Minimum: Minus 20°F (compliance with operational performance requirements at plus 35°F and above)
 - Maximum: Plus 120°F
- b. Pressure
 - Minimum: 12.3 psia, continuous, 8 psia for 2 hours
 - Maximum: 18.0 psia
- c. Humidity
 - Minimum: 8 percent relative
 - Maximum: 100 percent relative
- d. Salt fog
 - Exposure to 1 percent salt solution by weight
- e. Deleted

f. Random Vibration

- | | | |
|--|----------------|---|
| (1) Qualification - acceptance vibration (acceleration spectral density) | 20 - 80 Hz | Increasing at plus 3 dB/octave to 0.067 g ² /Hz at 80 Hz |
| | 80 - 350 Hz | Constant at 0.067 g ² /Hz |
| | 350 - 2,000 Hz | Decreasing at minus 3 dB/octave from 0.067 g ² /Hz at 350 Hz |

Duration:

- (1) 5 times AVT time
(2) 20 times AVT time (goal)

(2) Flight (Interior)

- | | |
|------------------|--|
| 20 - 150 Hz | Increasing at 6 dB/octave to 0.03 g ² /Hz at 150 Hz |
| 150 - 1,000 Hz | Constant at 0.03 g ² /Hz |
| 1,000 - 2,000 Hz | Decreasing at 6 dB/octave from 0.03 g ² /Hz at 1,000 Hz |
- Time Duration: 48 minutes per axis

g. Acceleration

Plus and minus 5 g's in all major axes

h. Shock

(1) Landing

Rectangular pulses of the following peak accelerations, time durations, and number of applications in the vertical (up) direction during landing:

| <u>Acceleration</u> (g peak) | <u>Duration</u> (ms) | <u>Applications</u> |
|---------------------------------|-------------------------|---------------------|
| 0.23 | 170 | 22 |
| 0.28 | 280 | 37 |
| 0.35 | 330 | 32 |
| 0.43 | 360 | 20 |
| 0.56 | 350 | 9 |
| 0.72 | 320 | 4 |
| 1.50 | 260 | 4 |

(2) Transient

5 to 35 Hz; plus and minus 0.25 g peak in one sweep from 3 to 35 Hz at one octave/minute.

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3.2.5.2 Nonoperational. The GPC shall be capable of meeting the operating performance requirements specified herein after exposure to the following conditions:

- a. Temperature
 - Minimum: Minus 65°F
 - Maximum: Plus 120°F with extremes of 150°F for 6 hours per day
- b. Pressure
 - Minimum: 3.28 psia
 - Maximum: 30.0 psia
- c. Shock
 - (1) Bench handling
 - As specified in MIL-STD-810, Method 516.1, Procedure V
 - (2) Basic design
 - 20g terminal sawtooth shock pulse of 11 ms duration in each direction of three orthogonal axes (both directions)
 - (3) Crash safety
 - 40g terminal sawtooth shock pulse of 11 ms duration in each of three orthogonal axes (both directions). Equipment and its mounting attachments shall not break loose, create a hazard to personnel, or prevent egress from a crashed vehicle. Operating performance is not required after this test.
- d. Ozone
 - 3 to 6 parts per hundred million (pphm). Total oxidant concentration may reach 60 pphm for 1 to 3 hours in any 24-hour period.
- f. Fungus
 - As specified in MC999-0096

3.2.5.3 Transportation and Storage. The GPC shall be protected from the environments specified in paragraph 5.2.3 by adequate packaging or protective processes unless the design to vehicle flight requirements precludes the need.

3.2.6 Transportability. The GPC shall be designed so as to be capable of being handled and transported to using facilities without damage or degradation, utilizing available methods of transport with the item prepared for shipment in accordance with Section 5 requirements. The equipment design shall be compatible with the planned packaging and transportation system to the extent that loads induced in the equipment during transportation will not produce stresses, internal loads or deflections resulting in damage to the equipment.

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3.2.6.1 Integral Protective Capability. The equipment design shall incorporate one or more of the following provisions for protection of components which are highly vulnerable to damage during transport and associated handling:

- a. Provide attach points for installation of temporary protective device (covers, reinforcing structure, desiccant cartridge, air breather/filter, heater, etc.)
- b. Make provisions for removal of sensitive component(s) for separate shipment.
- c. Provide built-in protective device (e.g., cover, caging of free-moving components, desiccant chamber, heater, etc.)

3.2.7 Thermal Design Requirements. The thermal design requirements shall be in accordance with MF0004-009, except that inlet air shall be 100°F and exhaust air temperature shall be 133°F.

3.2.7.1 Cooling System Configuration. Each computer shall be cooled as shown in Figure 13.

3.2.7.2 Cooling Air Pressure Loss. The cooling air pressure loss for a given LRU shall be the difference between the total pressure of the coolant entering and outlet pressure of the air leaving. The unit total pressure loss for each of two specified conditions is as shown in the table below. The total pressure loss of like delivered units shall not vary more than 10 percent from a nominal design value to be agreed upon by the seller and buyer.

Cooling Air Pressure Loss Table

| Condition | A (Ground) | B (In Flight) |
|--|-------------|---------------|
| Maximum allowable computer total pressure loss (in. of H ₂ O) | 1.3 | 1.3 |
| Surrounding air pressure (psia) | 18 (+0, -2) | 14.7 |
| Inlet air temperature (°F) | 100 | 100 |
| Exhaust Maximum air temperature (°F) | 133 | 133 |

3.2.7.3 Cooling Air Flow. During flight and ground operations, at ambient pressures of 12.3 to 18.0 psia, the GPC shall have a minimum gas coolant flow rate of 4.0 lbs/min.

3.3 Design and Construction. The computer design shall make maximum use of modular plug assemblies. Commonality of modular functions shall be stressed to reduce the requirement for spares allocation of circuit boards due to uniqueness. The computer case shall be of minimum weight consistent with supporting modules and subassemblies for the specified environment. Wherever practical, the computer design shall include modules, subassemblies, and components of proven design. Workmanship shall be in accordance with MIL-STD-454, Requirement 9.

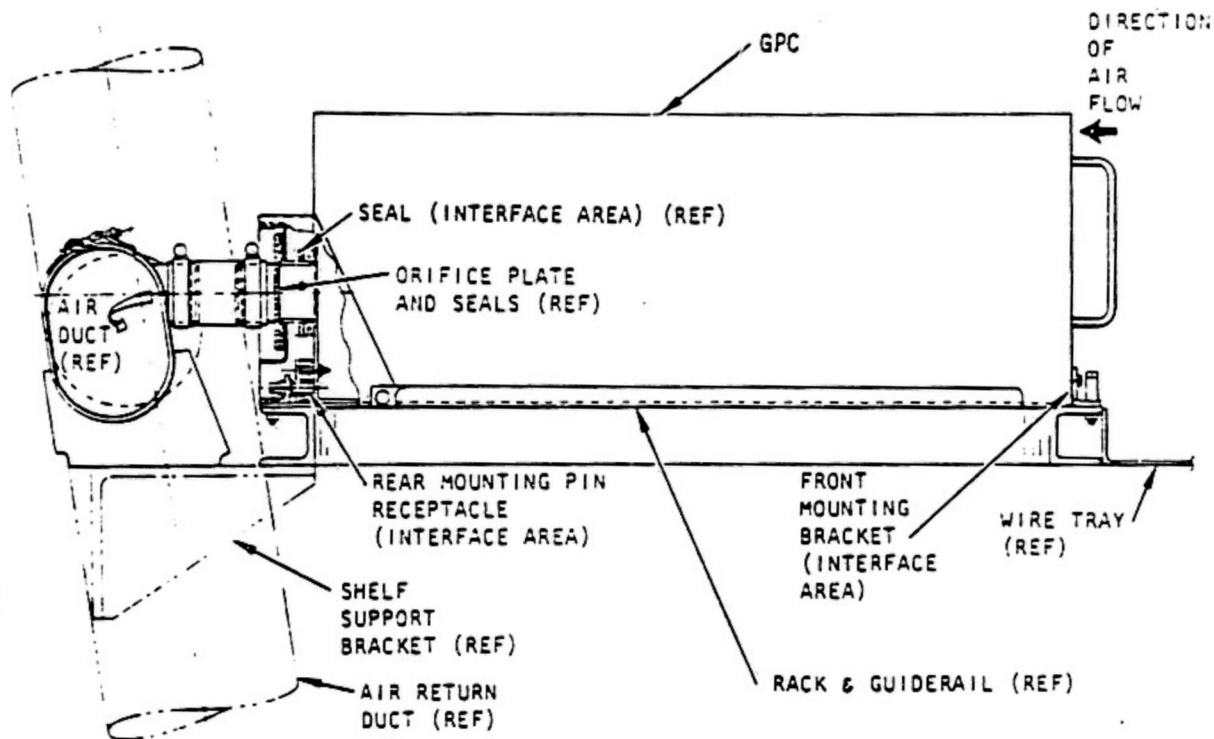


Figure 13. General Purpose Computer Cooling System Configuration

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3.3.1 Materials, Processes, and Parts.

3.3.1.1 Materials and Processes. Materials and processes for the GPC shall be in accordance with MC999-0096 to the extent specified in the requirements table of the purchase order.

3.3.1.2 Parts Standardization. Parts utilization shall be based upon: (1) selection of qualified parts, (2) proper derating and application, and (3) minimizing the number of part types. Parts used in design and fabrication shall be selected from MF0004-400.

3.3.1.3 Cleanliness. The GPC shall be cleaned to the cleanliness requirements of MC999-0096 (visibly clean).

3.3.1.4 Vibration Isolators. The computer LRU's shall be rigidly mounted without benefit of vibration isolators.

3.3.2 Selection of Specifications and Standards. Specifications and standards for use in the design and construction of the GPC, other than those specified herein, shall be selected in the order of precedence in accordance with MIL-STD-143, except that NASA documents, when suitable for the purpose shall take precedence.

3.3.3 Electromagnetic Compatibility and Electrical Design.

3.3.3.1 Electromagnetic Compatibility (EMC). The GPC shall meet the electromagnetic interference and compatibility requirements of MF0004-002 for Class ID requirements.

3.3.3.2 Electrical Design Requirements. Electrical design requirements for the GPC shall be in accordance with MF0004-002 to the extent specified in the requirements table of the purchase order.

3.3.3.2.1 Deleted.

3.3.3.2.2 Metals and Metal Couples, Restriction on Use. Metal joints which require electrical bonding shall be precise, dry, and conducting. Nonconducting corrosion inhibitors may be added after joint assembly. Conducting metal joints shall be required for electrical circuit fault-current return, electrostatic corona prevention, and structural shielding from lightning-strike induction and avionic interference.

3.3.4 Identification and Marking.

3.3.4.1 Identification of Parts. Each part fabricated shall be identified with a part number. The same specification or part number shall be used to identify all like materials, processes, and parts. Seller shall assign a new part number to the part when authorized changes make the superseded part not interchangeable with respect to interface, reliability, safety, logistics, traceability, or performance. The part identification shall include the manufacturer's identification code per DOD Handbook H 4-1, and be lot numbered or serial numbered when required.

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3.3.4.2 Identification of All Development/Qualification Test Specimens. Test specimens shall be permanently and obviously identified prior to testing with the words "ENG TEST ONLY" in addition to the identification required by the drawing/specification to preclude their use on production items. The letters shall be indelible and provide a distinctive and vivid contrast with the color of the test specimen. The lettering size and identification location shall be clearly visible to casual observation. Materials used for the identification shall be compatible with the test specimen in its operating environment. When the size or configuration of the test specimen is such that the identification cannot appear on the specimen other suitable means such as metal tags shall be used.

3.3.4.3 Nameplates. Nameplates shall be marked in accordance with MIL-STD-130 and shall include (as applicable) item name; buyer's control number; manufacturer; date of manufacture; and manufacturers serial number, part number, lot number, and code identification number. Abbreviations, in accordance with MIL-STD-12, may be used.

3.3.5 Traceability. Traceability shall be provided by assigning traceability identification to end items or major components as identified in 3.1.3. Each component, part, and subassembly comprising or contained within the end item or major component shall be classified and processed as exempt or traceable, in accordance with the criteria contained herein.

3.3.5.1 Traceability Classification. Each component, subassembly, and part within the end item shall be evaluated and receive a traceability classification. Seller and subordinate supplier engineering documentation (e.g., drawings and specifications) shall specify the traceability classification for each part, component, and subassembly as classified by the seller.

3.3.5.1.1 Serial Traceability (T_C). Serial traceability requires the assignment of a unique serialized identifier and processing of each part, subassembly, major component, or end item identified (T_S) as a separate item, and maintaining historical records pertaining to that item alone. The historical records in turn will provide the capability for backward traceability to the identification of its procurement, fabrication, inspection, processing, test, and operating records and any other pertinent data deemed necessary by the seller. The capability shall also provide for backward traceability to the procurement document(s) and receiving record(s) of part(s), components, and subassemblies within the end item designated as traceable (exempt items excluded).

3.3.5.1.1.1 Serial Traceability Criteria. Sub-tier items comprising or contained within the end item which satisfy any of the following criteria shall be traceable by serialization:

- a. Limited life.
- b. Contains traceable subordinate items, assemblies, or parts.

3.3.5.1.2 Lot Traceability (T_T). Lot traceability requires lot serial numbering of sub-tier items produced by the lot, batch, mix, heat, or melt in a given time sequence and the maintaining of historical data equally pertinent to all items in the lot. Separate lot numbers shall be assigned when planned differences between individual items in the lot occur due to changes in materials (substitution) or processes which effect form, fit, or function. The "given time sequence" includes identification of work on the production order for a specific part number, from initiation of work through completion of the last operation.

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3.3.5.1.2.1 Lot Traceability Criteria. Sub-tier items which satisfy the following criteria shall be lot traceable:

- All functional electrical, electronic, and electromechanical (EEE) parts in accordance with MF0004-400
- Parts with materials identified by the seller as critical, except for resistors, capacitors, and connectors/test point blocks
- Parts identified by the seller as controlled by unique manufacturing process(es)

3.3.5.1.3 Exempt From Traceability (E). This classification identifies those items which are exempt from traceability requirements. All items which have not been classified and identified as T_S or T_L shall be exempt (E) from traceability.

3.3.5.2 Traceability Identification. Each item identified as traceable (T_S, T_L) shall have a traceability identifier consisting of the manufacturer's code identification number as listed in DOD Handbook H 4-1 and a serial, lot, or member number as illustrated below. The serial, lot, or member number shall be assigned by the manufacturer and shall not exceed 10 characters (alpha-numeric, dashes, etc.).

| Digit | Mfr's Code No. | | | | | Mfr Assigned Traceable No. | | | | | | | | | |
|---------------------------------|----------------|---|---|---|---|----------------------------|---|---|---|----|----|----|----|----|----|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| Mfr's Code and Traceability No. | 0 | 3 | 9 | E | X | A | M | P | L | E | | | | | |

3.3.6 Interchangeability. The GPC and the items identified in 3.1.3, shall be interchangeable in accordance with the definition of MIL-STD-280. Interchangeability shall be a design feature for all removable items/subassemblies/parts designated as LRU's or SRU's. When removable items/subassemblies contain controls, wiring, hydraulic lines, etc., interchangeability shall be provided at the attachments of these items to their next assembly, as well as for structural attachments of the assembly.

3.3.6.1 Design Tolerances. Provisions shall be made for design tolerances such that items having the dimensions and characteristics permitted by the item specification or drawing are interchangeable without selection or departure from the specified equipment performance.

3.3.6.2 Use of Standard Parts. When standard parts (refer to 3.3.1.2) are not available and permission is granted for use of a nonstandard part due to unavailability of the standard part, the equipment shall be designed so that the nonstandard part can be replaced by the standard part. Appropriate space, mounting holes, and other necessary provisions shall be provided for this purpose.

3.3.7 Safety. The design and operation shall comply with the following safety requirements:

- The design shall insure that transient effects to the computer cannot introduce erroneous signals which are hazardous during critical operations.
- The computer shall not generate electrical current or radio frequency transients that could cause failure or malfunction of other equipment unless the computer is properly shielded.

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- c. The physical form or shape, as designed and built, shall minimize sharp points, corners, edges, etc., which present a hazard to operations personnel or to their personal clothing or equipment. When such features are required for mission accomplishment, then suitable guards shall be provided for ground or flight handling operations.

3.3.8 Human Performance/Human Engineering. The design shall consider the capabilities and limitations of the human operator wherever a man-machine interface exists, including torques, forces, and other functional design characteristics of controls, displays, and work stations. The principal design guide for the man-machine interface shall be MIL-STD-1472. Handling provisions shall be in accordance with 3.2.4.2.5.

3.3.9 Mechanical Design Requirements.

3.3.9.1 Provisions for LRU Alignment. LRU's requiring a particular alignment in the spacecraft shall incorporate special alignment means appropriate to the accuracy of the alignment required.

The design of mechanical systems involving linkages or other devices that require accurate alignment by adjustment shall include provisions for alignment and recheck of alignment without removal of components of the system and without removal of other equipment.

3.3.10 Other Requirements.

- a. Electrical and Electronic Piece-Parts - Closure Construction. Electrical and electronic piece-parts with all-welded closure construction shall be used in preference to piece parts with other types of closure construction. Other types of construction may be used if adequate program controls are imposed to assure that internal contamination cannot cause part degradation and/or failure under a zero-gravity environment.
- b. Wire Bundles - Protective Coating. Where protective coating or sheathing is added to wire bundles, ability to withstand anticipated handling and operating deformations without wire damage shall be demonstrated by appropriate test programs. Adequacy of materials applied to wire bundles will be demonstrated during development testing and by various installation-level tests. Verification tests of specially-designed and procured cables will include tests to demonstrate the adequacy of the cover.

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4. QUALITY ASSURANCE PROVISIONS

4.1 General Requirements

4.1.1 General Verification Guidelines and Criteria. The seller shall use the following general requirements in developing a verification program.

- a. Each performance and design requirement specified in Sections 3 and 5 of this specification shall be verified by test, assessment, or analysis in support of certification of the design for operational use.
- b. Verification of maintainability, accessibility, and ease of operation shall be demonstrated.
- c. Each measured parameter for testing shall have a specified tolerance band of acceptability bracketing the nominal value.
- d. As a general guideline, off-limit testing will not be conducted. However, off-limit testing will be considered:
 - (1) When design margins are relatively small with respect to off-nominal abort conditions.
 - (2) When uncertainty exists in the definition of the design criteria.

Testing of this nature must have prior approval of the buyer and must have considered preservation of at least one specimen of certification hardware for later testing.

- e. Acceptance test procedures, equipment and test levels shall be verified during development testing.
- f. Certification shall be structured to verify the full range of the design requirements under specified environments.
- g. Whenever practical and technically sound, accelerated life test techniques shall be utilized.
- h. Testing shall be conducted at the most cost effective level of assembly.
- i. All qualification test specimens shall be processed through specified acceptance testing prior to qualification test.

4.1.2 Test Conditions.

4.1.2.1 Standard Test Conditions. Environmental standard test conditions for tests required by this specification shall be: an atmospheric pressure of 28.5 plus 2 or minus 4.5 inches of mercury (Hg), a temperature of 73 plus or minus 18°F and a relative humidity of 50 plus or minus 30 percent.

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4.1.2.1.1 Coldplate or Forced Air Cooled Equipment. When operation of the unit under test is required during environmental exposure, coolant in accordance with specification requirements shall be supplied. During tests in which the ambient temperature is other than standard room ambient, the coolant temperature shall be at design extremes and "in-phase" with the test chamber temperature. If the use of coolant will have no effect upon test results for a particular environment, the requirement to use cooling shall be at the discretion of the seller.

4.1.2.2 Test Tolerances. Test tolerances shall be used as specified in MIL-STD-810, or FED-STD-101 as applicable, except as follows:

4.1.2.2.1 Random Vibration. Test tolerances and procedures shall be in compliance with SP-T-0023.

Analog vibration spectral density analysis criteria: Analysis sample time (T) shall equal or exceed 50/BW, where BW is the effective bandwidth of the filter utilized. For swept filter analysis, analyzer filter scan rate (SR) shall (1) not exceed BW/T Hz/second when averaging is obtained using linear integration with an integration time of T; or (2) shall be BW/4RC when averaging is obtained by smoothing with an equivalent resistance capacitance (RC) low pass filter using a time constant $RC \geq T/2$.

4.1.2.2.2 Shock.

| | |
|----------------------------|--|
| (Acceleration versus time) | Peak amplitude: Plus or minus 10 percent |
| | Pulse duration: Plus or minus 10 percent |

4.1.2.2.3 Acceleration.

Specified acceleration: Plus 10 percent,
Minus 0 percent

4.1.2.2.4 Exposure Time.

Duration specified for vibration or acceleration environments:

Plus 10 percent, Minus 0 percent

4.1.2.2.5 Measuring Instrumentation. Allowable error shall not exceed one-tenth of the tolerance specified for the parameter to be measured.

4.1.3 Test Responsibility and Location. The seller shall be responsible for implementing the quality assurance requirements specified herein. Except as otherwise noted, the seller may use his own facilities or any commercial laboratory acceptable to the buyer.

4.2 Quality Conformance. The following sections define the tests, analyses, simulations, and assessments necessary to verify that the requirements of Sections 3 and 5 of this specification are met.

4.2.1 Development. The seller shall perform development engineering evaluation of hardware, software, manufacturing processes, and techniques for the purpose of acquiring engineering data; identifying sensitive parameters; evaluating the development

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configuration; providing the necessary confidence that the hardware will meet the specification product. Development objectives shall encompass the following as a minimum:

- a. Design and performance capability, including redundancy.
- b. Ability to meet specified requirements with adequate design margin.
- c. Integration of each component and subsystem with other components, subsystems, facilities, support equipment, etc.
- d. Establishment of process, procedures, equipment, and test levels for manufacturing acceptance testing, maintenance, checkout, and operational phases of the program.
- e. Identification of significant failure modes and effects.
- f. Determination of the effect of various combinations of tolerance and drift of design parameters.
- g. Determination of the effect of combinations and sequences of environments and varying stress levels.
- h. Identification of safety hazards, parameters, requirements, and procedures.

4.2.1.1 Operating Limit on Temperature Controlled Equipment. For flight equipment whose operating temperature is normally controlled by heating or cooling equipment, and whose temperature is monitored in flight, the test program and appropriate analyses shall define:

- a. The maximum and minimum temperatures expected in normal operations.
- b. The maximum and minimum temperature at which equipment may be expected to fail to function until temperature is restored to normal range.

4.2.2 Acceptance. Acceptance tests and inspections shall be performed on all computers to be employed in qualification test programs and on all computers delivered to the buyer. These acceptance tests and inspections shall be performed to demonstrate that specified requirements have been met. Final acceptance tests and inspections shall be performed in a manner and under conditions which simulate end-use to the highest degree practicable without damage to the GPC. All final acceptance tests and inspections determined to be necessary to demonstrate end item compliance to contract, drawing and specification requirements shall be listed in Table XIX.

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Table XIX. Acceptance Requirements

| Inspection and Test | Paragraphs Listed in Recommended Sequence |
|----------------------------|---|
| Examination of Product | 4.2.2.1 |
| Insulation Resistance Test | 4.2.2.6 |
| Dielectric Strength Test | 4.2.2.7 |
| Acceptance Vibration Test | 4.2.2.3 |
| Acceptance Thermal Test | 4.2.2.4 |
| Performance | 4.2.2.2 |
| Power Variation Test | 4.2.2.5 |

Note: Functional performance and/or continuity tests of 4.2.2 shall be conducted on each GPC to the greatest degree practicable before, during, and after acceptance vibration tests and acceptance thermal test. When complete functional verification cannot be accomplished during the acceptance test with environments because of limited test time, the most critical functions that demonstrate equipment performance shall be tested and all other functional circuits monitored.

4.2.2.1 Examination of Product. Each GPC shall be carefully examined to determine conformance to the requirements of this specification. Particular attention shall be given to weight, workmanship, finish, dimensions, construction, cleanliness, identification, marking traceability level, and that certified materials and processes have been used.

4.2.2.2 Functional and Performance Tests. Functional and performance tests shall be conducted on all deliverable equipment to establish compliance with the requirements of Section 3. Tolerance bands or pass-fail performance criteria, based on performance design requirements, shall be established for each parameter. They will include the following as a minimum:

a. Power Requirements.

- (1) Isolation of primary power and ground
- (2) Power-on/off sequence
- (3) Power interruption

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- b. Built-in Test (BIT).
- c. Control Processing Unit (CPU).
- (1) Proper operation of computer instructions
 - (2) Proper operation of CPU registers, clock, and interrupts
- d. Memory.
- (1) Main store areas addressed correctly
 - (2) Ability to modify memory storage protect bits under program control
 - (3) Proper operation of parity interrupt and memory storage protection interrupt
- e. Intra Element Input/Output (CPU/IOP).
- (1) Verify operation of discrete inputs/outputs
 - (2) Ability to exercise address lines and to command data output line
 - (3) Ability to process external interrupts and to override DMA operation
- f. Input/Output Processor (IOP).
- (1) Verify operation of MSC, BCE, CPU interrupt mechanizations generated by IOP including discrete output and input mechanizations.
 - (2) Verify entire MSC and BCE instruction set, intercomputer operations, and DMA.
 - (3) Verify IOP discrete inputs and output (including RM).
- g. Multiplex Interface Adapter (DMIA).
- (1) Verify command and data word sync recognition
 - (2) Demonstrate return word capability

4.2.2.3 Acceptance Vibration Test. The GPC shall be subjected to random vibration, in each of three orthogonal axes, in accordance with the spectral density envelope specified below. The vibration duration shall be adequate to perform selected functional performance tests, but shall not be less than 30 seconds nor greater than 5 minutes per axis. Should retest be required, the total accumulative vibration test time in any axis shall not exceed the qualified time for AVT in that axis (reference 4.2.4.1.3.1) without prior buyer approval. Tolerances, procedures and tests shall be conducted before and after the vibration test. Selected performance tests (TBS) shall be conducted during vibration, with all other circuits monitored.

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Acceleration Spectral Density

- 20 to 80 Hz - Increasing at plus 3 dB/octave to 0.04 g²/Hz at 80 Hz
- 80 to 350 Hz - Constant at 0.04 g²/Hz
- 350 to 2,000 Hz - Decreasing at minus 3 dB/octave, from 0.04 g²/Hz at 350 Hz

4.2.2.4 Acceptance Thermal Tests (ATT). The GPC shall be thermal cycled from 70°F to plus 100°F, to 0°F, to plus 35°F, to plus 100°F, and to 70°F with continuity monitored throughout. The thermal rate of change shall not exceed 4°F per minute, nor be less than 1°F per minute. Dwell at each temperature limit shall be a minimum of 60 minutes after thermal stabilization of the test article. Selected performance tests shall be conducted on all items during each thermal extreme except that the GPC will not be operated at temperatures below plus 35°F. The performance test at each high temperature extreme shall include operation at the maximum heat dissipating mode for a duration consistent with the design capability and sufficient to verify acceptance performance.

4.2.2.5 Power Variation and Usage Tests. Tests shall be conducted to determine if the equipment performs satisfactorily under power input conditions specified in 3.1.2.1.

4.2.2.6 Insulation Resistance Test. Insulation resistance test shall be in accordance with MF0004-002, except that the test shall be made at less than 50 volts.

4.2.2.7 Dielectric Strength Test. 800 Vdc shall be used to check for short circuits and insulation breakdown on multilayer interconnection boards (MIB's). Page connectors shall be qualified to 450 Vac and LRU connectors shall be qualified to 1,300 Vac.

4.2.3 Assessment. Verification by assessment methods shall be used to verify design features. These methods employ the orderly review and evaluation of design (documentation) or visual inspection techniques (e.g., mock-up forms, fit checks, maintainability access, tolerances, safety wiring and placards).

4.2.3.1 Reliability. Verification of the applicable reliability requirements of 3.2.3, which cannot be verified by test or analysis, shall be by assessment.

4.2.3.2 Maintainability. Compliance with the maintainability requirements of 3.2.4, which cannot be verified by analysis, shall be by assessment of engineering data.

4.2.3.3 Materials and Processes. Conformance of the GPC with materials and processes in accordance with 3.3.1.1, which cannot be verified by test or analysis, shall be verified by assessment of design drawings and process specifications.

4.2.3.4 Parts Standardization. Conformance of the GPC with standard parts in accordance with 3.3.1.2 shall be verified by assessment of design drawings.

4.2.3.5 Selection of Specification and Standards. Verification that selection of specifications and standards are in accordance with 3.3.2 shall be verified by assessment of design drawings and specifications.

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4.2.3.6 Electrical Design Requirements. Verification that the GPC conforms to the electrical design requirements of 3.3.3.2, which cannot be verified by analysis or test, shall be verified by assessment of design drawings.

4.2.3.7 Interchangeability and Replaceability. Verification that the GPC design conforms to the interchangeability and replaceability requirements of 3.3.6 shall be verified by assessment of design documentation.

4.2.3.8 Design Tolerances. Verification that the GPC conforms to the design tolerances required in 3.3.6.1 shall be verified by assessment of the design documentation.

4.2.3.9 Use of Standard Items. Verification that standard items will be used in the GPC when available in accordance with 3.3.6.2 shall be verified by assessment of design drawings.

4.2.3.10 Human Performance/Human Engineering. Verification that the GPC conforms to the human performance/human engineering requirements of 3.3.8 shall be verified by assessment of the design drawings.

4.2.4 Certification. The seller shall certify the requirements of Section 3 and 5 by the methods specified below.

4.2.4.1 Qualification Tests. Qualification testing performed to satisfy the requirements specified in the performance and design verification matrix (Table XXI) shall be in conformance with the requirements of this paragraph. Qualification test specimens shall be subjected to the tests specified in Table XX in the sequence below.

Table XX. Required Tests

| Test | Paragraph |
|-----------------------|------------|
| Acceptance Test (REF) | 4.2.2 |
| Power Test | 4.2.4.1.6 |
| EMC | 4.2.4.1.8 |
| Cabin Atmosphere | 4.2.4.1.12 |
| Thermal Cycle | 4.2.4.1.10 |
| Vibration | 4.2.4.1.3 |
| Acceleration | 4.2.4.1.4 |
| Thermal-Vacuum | 4.2.4.1.9 |
| Life | 4.2.4.1.11 |
| Shock | 4.2.4.1.5 |

4.2.4.1.1 Test Hardware. Qualification test hardware shall be of the same configuration as flight hardware.

4.2.4.1.2 Performance Requirements. The GPC shall be subjected to complete performance tests before and after each environment test and to selected functional and performance tests during each environmental exposure. Where complete performance verification cannot be accomplished during the environmental exposure because of limited test

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time, the most critical functions shall have priority. Tolerance bands or pass-fail performance criteria, based on performance design requirements, shall be established for each parameter. Parameter shifts during or after each environment shall not exceed the absolute value of the allowable difference between the acceptance and qualification test limits for each parameter.

4.2.4.1.3 Vibration.

4.2.4.1.3.1 Qualification - Acceptance Vibration Test (OAVT). The GPC shall be subjected to the random vibration specified in 3.2.5.1.f(1), for the duration specified, in each of three orthogonal axes. Vibration tolerances, test criteria, and procedures shall be in accordance with SP-T-0023. Performance verification tests shall be identical to those conducted during AVT (reference 4.2.2.3). Duration (2) shall not begin until the GPC has successfully completed the post duration (1) performance verification test specified above.

4.2.4.1.3.2 Flight Vibration. The GPC shall be subjected to the random vibration specified in 3.2.5.1.f(2), for the duration specified, in each of three orthogonal axes. Vibration tolerances, criteria, and test procedures shall be in accordance with SP-T-0023. Performance tests shall be in accordance with 4.2.4.1.2.

4.2.4.1.4 Acceleration. The GPC shall be subjected to the acceleration specified by 3.2.5.1g for a minimum of five minutes in each direction along each of three orthogonal axes. If any axis(es) is (are) considered significant, with respect to acceleration effects, it (they) shall be considered when establishing the orthogonal axes system.

4.2.4.1.5 Shock.

- a. Bench Handling. The GPC shall be subjected to bench handling shock as specified in Procedure V, Method 516.1 of MIL-STD-810.
- b. Landing. The landing shock shall be verified by analysis.
- c. Design. The GPC shall be subjected to design shock as specified in 3.2.5.2h(2) in accordance with MIL-STD-810, Method 516.1, Procedure I.
- d. Crash Safety. The GPC or the chassis of the GPC with a dummy load simulating the mass and distribution of the remaining elements of the GPC shall be attached by its normal mounting attachments and subjected to sawtooth shock as specified in Procedure III, Method 516.1 of MIL-STD-810. Crash safety may be verified by analysis.

4.2.4.1.6 Power Tests. Tests shall be performed to assure that the GPC meets performance requirements of Section 3.2.1 and the power consumption requirements of 3.3.3.2.1 with input power meeting the requirements of 3.1.2.1, including both normal and emergency transient conditions, as well as steady-state maximum and minimum limits.

4.2.4.1.7 Deleted.

4.2.4.1.8 Electromagnetic Compatibility Tests. EMC requirements, which cannot be verified by analysis, shall be verified by the minimum susceptibility and emission test developed in accordance with MF0004-002.

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4.2.4.1.9 Thermal-Vacuum Test. The GPC shall be placed in a thermal-vacuum chamber, with the air temperature in the chamber maintained at 80°F throughout the test. The pressure shall be reduced from room ambient to 8 psia at a rate of change of 0.15 psia/minute. Pressure shall be maintained at 8 psia for 165 minutes and then returned to room ambient at a rate of change of 9.0 psia/minute. The GPC shall be operating throughout the entire test, with performance tests conducted during the 8-psia stabilized condition.

The inlet air temperature shall be maintained at 80°F with a density consistent with the 8-psia requirements, and the air temperature rise across the GPC shall not exceed 45°F.

4.2.4.1.10 Thermal Cycle Test. The GPC shall be mounted on a surface to simulate usage conditions and thermally cycled 5 times from 70°F to the maximum design temperature (plus 120°F), to the minimum design temperature (minus 20°F), to plus 35°F, to the maximum design temperature (plus 120°F), and to 70°F. The thermal rate of change shall not exceed 4°F per minute nor be less than 1°F per minute. Dwell at each thermal extreme shall not be less than 60 minutes after thermal stabilization of the test article. Selected performance tests shall be conducted at each thermal extreme except that the GPC will not be operated at temperatures below plus 35°F. Performance at the high temperature shall include operation at the maximum heat dissipating mode for a duration consistent with the design capability and sufficient to verify acceptable performance. Performance at the low temperature extreme shall include operation at the minimum heat dissipating mode for a duration sufficient to verify acceptable performance. (See 4.1.2.1.1 for applicable equipment cooling requirements.)

4.2.4.1.11 Operating Life Test. On-off cycles and operating time accumulated on a single specimen during other qualification tests may be applied toward these requirements.

- a. Cyclic: The GPC shall be operated for 1,000 on-off cycles.
- b. Forward: The GPC shall be operated for 750 hours.
- c. The remaining hours of 3.2.1.1.1 life requirements shall be satisfied by analysis.

4.2.4.1.12 Cabin Atmosphere. The GPC shall be subjected to a salt fog test in accordance with MIL-STD-810, Method 509, Procedure I, for a duration of one hour. Immediate upon conclusion of the salt fog exposure, without cleaning, the GPC shall be placed in a humidity chamber and thermally cycled between 60 and 120°F for a total of four cycles at a relative humidity of 85 percent. The unit shall remain at each temperature extreme during each cycle for a period sufficient to achieve thermal stabilization plus the time required to conduct performance testing or six hours, whichever is longer. The GPC shall be performance tested at each temperature extreme for each cycle following thermal stabilization and all circuits shall be monitored during the temperature change period between thermal extremes. The test duration shall be 120 hours.

4.2.4.1.13 Package Qualification Tests. Certification of package performance shall be accomplished by analysis whenever possible. When certification cannot be accomplished by analysis, a buyer approved simulated dummy load shall be installed in its package and both subjected to the applicable FED-STD-101 test to verify conformance to 5.2.3. Development assigned hardware may be used for testing in lieu of a dummy load.

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4.2.4.1.14 Temperature Altitude, and Cooling Air Tests.

4.2.4.1.14.1 General. Unless otherwise specified in the individual test procedures, the equipment shall be placed in a test chamber in the as-installed condition. The term "as installed" shall be interpreted as including the applicable cooling provisions, as well as any features of the orbiter installation that bear on equipment thermal environment. At least the following data, as applicable, shall be recorded for each item of equipment during the temperature, altitude, and cooling air tests:

- a. Operating surface or reference temperature of the critical components and piece-parts.
- b. Cooling air flow rate, supply temperature, and exit temperature.
- c. Cooling air total pressure loss.
- d. Electrical heat dissipation.
- e. Functional parameters of Section 3.

4.2.4.2 Certification by Analysis. The following requirements shall be verified by analysis.

4.2.4.2.1 Shelf/Operating Life. Compliance with shelf/operating life requirements of Section 3 shall be verified by analysis of the applicable documentation and test data.

4.2.4.2.2 Reliability. Compliance with the reliability requirements of 3.2.3 shall be verified by analysis and evaluation of design drawings and test data, as applicable.

4.2.4.2.3 Maintainability. Compliance with the maintainability requirements of 3.2.4, which cannot be verified by assessment, shall be verified by analysis of the engineering data.

4.2.4.2.4 Ozone. Compliance with the ozone requirements under 3.2.5 shall be verified by analysis of design drawings and test data.

4.2.4.2.5 Fungus. Compliance with the fungus requirements under 3.2.5 shall be verified by analysis of design drawings and test data.

4.2.4.2.6 Materials and Processes. Compliance with the materials and processes requirements of 3.3.1.1, which cannot be verified by assessment or test, shall be verified by analysis of design drawings and material test data.

4.2.4.2.7 Electromagnetic Compatibility. Compliance with the EMC requirements of 3.3.3.1, which cannot be verified by test, shall be verified by analysis of design drawings and test data.

4.2.4.2.8 Electrical Design Requirements. Compliance with the electrical design requirements under 3.3.3.2, which cannot be verified by test or assessment, shall be verified by analysis of design drawings and engineering data.

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4.2.4.2.9 Safety. Compliance with the safety requirements of 3.3.7 shall be verified by analysis and evaluation of design drawings and test data, as applicable.

4.2.4.2.10 Transient Shock. Compliance with the transient shock requirements of 3.2.5.1h(2) shall be verified by test or analysis.

4.2.4.2.11 Certification by Other Test Data. Test data generated from articles previously certified may be used as a certification method when it can be shown that the article is similar or identical to the article being certified. Features to be considered shall include design, performance, environmental duration and limits, manufacturing process, and quality control. Special effort shall be made to avoid duplication of previous tests from this or similar programs. Where certification by testing is required, data from other than qualification tests may be used to satisfy the requirements under the following conditions:

| | |
|---|---|
| Predeclaration | The intent to use the test for certification is declared prior to test conduct. |
| Configuration | Production configuration or approval (where allowed) for differences. |
| Facilities | Certified |
| Inspection | Required |
| Test requirement/ procedure/pass-fail criteria | Formally approved by buyer |
| Acceptance | Required |
| Functional Test pre-, post-, and during environment | Required (except for nonoperating tests such as packaging tests). |
| Documentation | Configuration description, failure reports, and test results. |

4.2.4.2.12 Mature Hardware (Off-the-Shelf).

- a. Evaluate and document equipment capability utilizing a comparison matrix which includes considerations such as configuration, performance and environment versus specified requirements.
- b. Where the environmental levels are more stringent than previous qualification levels, analyse or test to verify that the item can withstand the higher level design requirements.
- c. For items that require minor modifications or have not been qualified to all environments, only the design modifications for the additional environments need to be certified, if cumulative and interaction effects do not exist. If cumulative and interaction effects do exist, complete qualification testing is required.

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4.2.5 Verification Requirements Matrices. The sellers verification program shall satisfy the performance and design verification requirements specified in Table XXI. Where a verification method is not indicated, the seller shall propose a suitable approach to requirement verification. Where a verification method is indicated, the seller may recommend an alternate approach.

Table XXI. Performance and Design Verification Matrix

VERIFICATION METHOD

- 1. Analysis
- 2. Assessment
 - a. Inspection
 - b. Review of Design

- 3. Test
 - a. Development
 - b. Qualification
 - c. Acceptance
 - d. Vehicle Acceptance
 - e. Pre-Flight Checkout
 - f. Horizontal Flight
 - g. Vertical Flight
 - h. Major Ground Test

Seller-Conducted

Buyer-Conducted

N/A - Not Applicable

| Section 3 and 5 Requirement No. | Verification Method | | | | | | | | | | | Section 4 Requirement No. | |
|---------------------------------|---------------------|---|---|---|---|---|---|---|---|---|---|---------------------------|------------------------------|
| | N/A | 1 | 2 | | 3 | | | | | | | | |
| | | | a | b | a | b | c | d | e | f | g | | h |
| 3. | X | | | | | | | | | | | | |
| 3.1 | X | | | | | | | | | | | | |
| 3.1.1 | | | | X | | | | | | | | | 4.2.3 |
| 3.1.2 | X | | | | | | | | | | | | |
| 3.1.2.1 | X | | | | | | | | | | | | |
| 3.1.2.1.1 | | | | | X | X | X | | | | | | 4.2.2.2 |
| 3.1.2.1.1.1 | | | | | X | X | X | | | | | | 4.2.2.2, 4.2.4.1.10 |
| 3.1.2.1.1.1.1 | | | | | | | X | | | | | | 4.2.4.2 |
| 3.1.2.1.1.2 | | X | | X | | X | | | | | | | 4.2.4.2, 4.2.3, 4.2.4.1.6 |
| 3.1.2.1.2 | | X | | | X | | | | | | | | 4.2.4.2, 4.2.4.2.11 |
| 3.1.2.1.3 | | | | X | | X | X | | | | | | 4.2.3, 4.2.2.2 |
| 3.1.2.1.4 | | | | X | | X | X | | | | | | 4.2.3, 4.2.2.2 |
| 3.1.2.1.5 | | | | X | | X | X | | | | | | 4.2.3, 4.2.2.2 |
| 3.1.2.1.6 | | X | | X | | X | | | | | | | 4.2.4.2, 4.2.3, 4.2.4.1.6 |
| 3.1.2.1.7 | | X | | X | | X | | | | | | | 4.2.4.2, 4.2.3, 4.2.4.1.6 |
| 3.1.2.1.8 | | X | | X | | X | X | | | | | | 4.2.4.2, 4.2.3, 4.2.2.2 |
| 3.1.2.1.9 | | | | | | X | X | | | | | | 4.2.2.2 |
| 3.1.2.1.10 | | X | | X | | X | X | | | | | | 4.2.3, 4.2.4.2, 4.2.2.2 |
| 3.1.2.1.11 | | X | | | | | | | | | | | |
| 3.1.2.2 | X | | | | | | | | | | | | |
| 3.1.2.2.1 | | | | X | | X | | | | | | | 4.2.3 |
| 3.1.2.2.2 | | | X | X | | X | X | | | | | | 4.2.2.1, 4.2.3, 4.2.2.2 |

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Table XXI. Performance and Design Verification Matrix (Cont)

VERIFICATION METHOD

- 1. Analysis
- 2. Assessment
 - a. Inspection
 - b. Review of Design

- 3. Test
 - a. Development
 - b. Qualification
 - c. Acceptance
 - d. Vehicle Acceptance
 - e. Pre-Flight Checkout
 - f. Horizontal Flight
 - g. Vertical Flight
 - h. Major Ground Test

Seller-Conducted

Buyer-Conducted

N/A - Not Applicable

| Section 3 and 5 Requirement No. | Verification Method | | | | | | | | | | | Section 4 Requirement No. | | |
|---------------------------------|---------------------|---|---|---|---|---|---|---|---|---|---|---------------------------|---|-------------------------------|
| | N/A | 1 | 2 | | 3 | | | | | | | | | |
| | | | a | b | a | b | c | d | e | f | g | | h | |
| 3.1.2.2.3 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.4.1.10 4.2.3 |
| 3.1.2.3 | | | | X | | | | | | | | | | |
| 3.1.2.3.1 | X | | | | | | | | | | | | | |
| 3.1.2.3.1.1 | X | | | | | | | | | | | | | |
| 3.1.2.3.1.2 | | | | | | X | | | | | | | | 4.2.3 |
| 3.1.2.3.1.3 | X | | | | | | | | | | | | | |
| 3.1.2.3.1.3.1 | | X | | X | | | | | | | | | | 4.2.4.2, 4.2.3 |
| 3.1.2.3.1.3.1.1 | | X | | X | | X | X | | | | | | | 4.2.4.2, 4.2.3, 4.2.2.2 |
| 3.1.2.3.1.3.1.2 | | X | | X | X | | | | | | | | | 4.2.4.2, 4.2.3, 4.2.4.2.11 |
| 3.1.2.3.1.3.1.3 | | X | | X | X | | | | | | | | | 4.2.4.2, 4.2.3, 4.2.4.2.11 |
| 3.1.2.3.1.3.1.4 | | X | | X | | X | | | | | | | | 4.2.4.2, 4.2.3, 4.2.2.2 |
| 3.1.2.3.1.3.1.5 | | X | | X | | X | | | | | | | | 4.2.4.2, 4.2.3, 4.2.2.2 |
| 3.1.2.3.1.3.1.6 | | X | | X | X | | | | | | | | | 4.2.4.2, 4.2.3, 4.2.4.2.11 |
| 3.1.2.3.1.3.1.7 | | X | | X | X | | | | | | | | | 4.2.4.2, 4.2.3, 4.2.4.2.11 |
| 3.1.2.3.1.3.1.8 | | X | | X | X | | | | | | | | | 4.2.4.2, 4.2.3, 4.2.4.2.11 |
| 3.1.2.3.1.4 | X | | | | | | | | | | | | | |
| 3.1.2.3.1.4.1 | | X | | X | | | | | | | | | | 4.2.4.2, 4.2.3 |
| 3.1.2.3.1.4.2 | | X | | X | | | | | | | | | | 4.2.4.2, 4.2.3, 4.2.2.2 |

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Table XXI. Performance and Design Verification Matrix (Cont)

VERIFICATION METHOD

- 1. Analysis
- 2. Assessment
 - a. Inspection
 - b. Review of Design

- 3. Test
 - a. Development
 - b. Qualification
 - c. Acceptance
 - d. Vehicle Acceptance
 - e. Pre-Flight Checkout
 - f. Horizontal Flight
 - g. Vertical Flight
 - h. Major Ground Test

Seller-Conducted

Buyer-Conducted

N/A - Not Applicable

| Section 3 and 5 Requirement No. | Verification Method | | | | | | | | | | | Section 4 Requirement No. | | |
|---------------------------------|---------------------|---|---|---|---|---|---|---|---|---|---|---------------------------|---|---|
| | N/A | 1 | 2 | | 3 | | | | | | | | | |
| | | | a | b | a | b | c | d | e | f | g | | h | |
| 3.1.2.3.1.4.3 | | X | | X | X | | | | | | | | | 4.2.4.2, 4.2.3, 4.2.4.2.11 |
| 3.1.2.3.1.4.4 | | X | | X | X | | | | | | | | | 4.2.4.2, 4.2.3, 4.2.4.2.11 |
| 3.1.2.3.1.4.5 | | X | | X | X | | | | | | | | | 4.2.4.2, 4.2.3, 4.2.4.2.11 |
| 3.1.2.3.1.4.6 | | X | | X | X | | | | | | | | | 4.2.4.2, 4.2.3, 4.2.4.2.11 |
| 3.1.2.3.1.4.7 | | X | | X | X | | | | | | | | | 4.2.4.2, 4.2.3, 4.2.4.2.11 |
| 3.1.2.3.1.4.8 | | X | | X | X | | | | | | | | | 4.2.4.2, 4.2.3, 4.2.4.2.11 |
| 3.1.2.3.1.5 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2 |
| 3.1.2.3.1.6 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2 |
| 3.1.2.4 | X | | | | | | | | | | | | | |
| 3.1.2.4.2 | X | | | | | | | | | | | | | |
| 3.1.2.4.2.1 | | X | | | X | | | | | | | | | 4.2.4.2, 4.2.4.2.11 |
| 3.1.2.4.3 | X | | | | | | | | | | | | | |
| 3.1.2.5 | X | | | | | | | | | | | | | |
| 3.1.2.5.1 | X | | | | | | | | | | | | | |
| 3.1.2.5.2 | X | | | | | | | | | | | | | |
| 3.1.2.5.3 | X | | | | | | | | | | | | | |
| 3.1.2.5.4 | X | | | | | | | | | | | | | |
| 3.1.2.6 | X | | | | | | | | | | | | | |
| 3.1.2.6.1 | | | X | X | | X | X | | | | | | | 4.2.3, 4.2.2.1 |
| 3.1.2.6.2 | | | | X | | X | X | | | | | | | 3.2.5.11, 3.2.5.12, 3.2.5.13 (ref only) |

Table XXI. Performance and Design Verification Matrix (Cont)

VERIFICATION METHOD

- 1. Analysis
- 2. Assessment
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 - b. Qualification
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 - e. Pre-Flight Checkout
 - f. Horizontal Flight
 - g. Vertical Flight
 - h. Major Ground Test

Seller-Conducted

Buyer-Conducted

N/A - Not Applicable

| Section 3 and 5 Requirement No. | Verification Method | | | | | | | | | | | Section 4 Requirement No. | | |
|------------------------------------|---------------------|---|---|---|---|---|---|---|---|---|---|------------------------------|---|---------------------------------------|
| | N/A | 1 | 2 | | 3 | | | | | | | | | |
| | | | a | b | a | b | c | d | e | f | g | | h | |
| 3.1.3 | | | X | X | | X | X | | | | | | | 4.2.2.1, 4.2.3 |
| 3.1.4 | | | X | X | | | | | | | | | | 4.2.2.1, 4.2.3 |
| 3.2 | X | | | | | | | | | | | | | |
| 3.2.1 | X | | | | | | | | | | | | | |
| 3.2.1.1 | X | | | | | | | | | | | | | |
| 3.2.1.1.1 | | X | | | | | | | | | | | | 4.2.4.2 |
| 3.2.1.1.2 | | X | | | | | | | | | | | | 4.2.4.2 |
| 3.2.1.1.3 | | X | | | | | | | | | | | | 4.2.4.2 |
| 3.2.1.1.4 | | X | | X | | | | | | | | | | |
| 3.2.1.2 | X | | | | | | | | | | | | | |
| 3.2.1.2.1 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2 |
| 3.2.1.2.2 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2 |
| 3.2.1.2.3 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2 |
| 3.2.1.2.3.1 | | X | | X | | | | | | | | | | 4.2.4.2, 4.2.3 |
| 3.2.1.2.3.2 | | | | X | | | | | | | | | | 4.2.3 |
| 3.2.1.2.3.3 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2 |
| 3.2.1.3 | X | | | | | | | | | | | | | |
| 3.2.1.3.1 | | X | | X | | | | | | | | | | 4.2.4.2, 4.2.4.1.10, 4.2.4.2.11 |
| 3.2.1.3.2 | | | | X | | | | | | | | | | 4.2.3 |
| 3.2.1.3.3 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.3.4 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.3.5 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.3.6 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |

Table XXI. Performance and Design Verification Matrix (Cont)

VERIFICATION METHOD

- 1. Analysis
- 2. Assessment
 - a. Inspection
 - b. Review of Design

- 3. Test
 - a. Development
 - b. Qualification
 - c. Acceptance
 - d. Vehicle Acceptance
 - e. Pre-Flight Checkout
 - f. Horizontal Flight
 - g. Vertical Flight
 - h. Major Ground Test

Seller-Conducted

Buyer-Conducted

N/A - Not Applicable

| Section 3 and 5 Requirement No. | Verification Method | | | | | | | | | | | Section 4 Requirement No. | | |
|---------------------------------|---------------------|---|---|---|---|---|---|---|---|---|---|---------------------------|---|----------------------------|
| | N/A | 1 | 2 | | 3 | | | | | | | | | |
| | | | a | b | a | b | c | d | e | f | g | | h | |
| 3.2.1.3.7 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.3.8 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.3.9 | | X | | X | | X | X | | | | | | | 4.2.2.2, 4.2.3, 4.2.4.2 |
| 3.2.1.3.10 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.4 | X | | | | | | | | | | | | | |
| 3.2.1.4.1 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.1, 4.2.4.1 |
| 3.2.1.4.2 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.4.3 | | | | X | X | | | | | | | | | 4.2.3, 4.2.4.2.11 |
| 3.2.1.4.5 | | | | X | X | | | | | | | | | 4.2.3 |
| 3.2.1.4.6 | | | | X | | X | X | | | | | | | 4.2.2.2, 4.2.3 |
| 3.2.1.4.8 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2 |
| 3.2.1.4.9 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5 | X | | | | | | | | | | | | | |
| 3.2.1.5.1 | X | | | | | | | | | | | | | |
| 3.2.1.5.1.1 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.1.2 | | | | X | X | | | | | | | | | 4.2.3, 4.2.4.2.11 |
| 3.2.1.5.1.3 | | | | X | X | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.2.11 |
| 3.2.1.5.1.3.1 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.1.4 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |

| | | | | | | | |
|----------------------|-----------------|--|--|--|--|--|-------------|
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Table XXI. Performance and Design Verification Matrix (Cont)

VERIFICATION METHOD

- 1. Analysis
- 2. Assessment
 - a. Inspection
 - b. Review of Design

- 3. Test
 - a. Development
 - b. Qualification
 - c. Acceptance
 - d. Vehicle Acceptance
 - e. Pre-Flight Checkout
 - f. Horizontal Flight
 - g. Vertical Flight
 - h. Major Ground Test

Seller-Conducted

Buyer-Conducted

N/A - Not Applicable

| Section 3 and 5 Requirement No. | Verification Method | | | | | | | | | | | Section 4 Requirement No. | | |
|---------------------------------|---------------------|---|---|---|---|---|---|---|---|---|---|---------------------------|---|-------------------------------------|
| | N/A | 1 | 2 | | 3 | | | | | | | | | |
| | | | a | b | a | b | c | d | e | f | g | | h | |
| 3.2.1.5.1.5 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.1.7 | | | | X | | | | | | | | | | 4.2.3 |
| 3.2.1.5.1.8 | X | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.2 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.2.1 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.2.2 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.2.3 | X | | | X | X | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1, 4.2.4.2.11 |
| 3.2.1.5.2.3.1 | | | | X | X | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.2.3.5 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.3 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.3.1 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.3.2 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.3.3 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.3.3.1 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.3.3.2 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.3.4 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |

Table XXI. Performance and Design Verification Matrix (Cont)

VERIFICATION METHOD

- 1. Analysis
- 2. Assessment
 - a. Inspection
 - b. Review of Design

- 3. Test
 - a. Development
 - b. Qualification
 - c. Acceptance
 - d. Vehicle Acceptance
 - e. Pre-Flight Checkout
 - f. Horizontal Flight
 - g. Vertical Flight
 - h. Major Ground Test

Seller-Conducted

Buyer-Conducted

N/A - Not Applicable

| Section 3 and 5 Requirement No. | Verification Method | | | | | | | | | | | Section 4 Requirement No. | | |
|------------------------------------|---------------------|---|---|---|---|---|---|---|---|---|---|------------------------------|---|----------------------------|
| | N/A | 1 | 2 | | 3 | | | | | | h | | | |
| | | | a | b | a | b | c | d | e | f | | | g | |
| 3.2.1.5.3.5 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.3.6 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.3.7 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.4 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.4.1 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.4.1.1 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.4.1.2 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.4.2 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.4.3 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.4.4 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.4.5 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.4.6 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.4.7 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.4.8 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.4.9 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |

Table XXI. Performance and Design Verification Matrix (Cont)

VERIFICATION METHOD

- 1. Analysis
- 2. Assessment
 - a. Inspection
 - b. Review of Design

- 3. Test
 - a. Development
 - b. Qualification
 - c. Acceptance
 - d. Vehicle Acceptance
 - e. Pre-Flight Checkout
 - f. Horizontal Flight
 - g. Vertical Flight
 - h. Major Ground Test

Seller-Conducted

Buyer-Conducted

N/A - Not Applicable

| Section 3 and 5 Requirement No. | N/A | Verification Method | | | | | | | | | | Section 4 Requirement No. | | |
|---------------------------------|-----|---------------------|---|---|---|---|---|---|---|---|---|---------------------------|---|-------------------------|
| | | 1 | 2 | | 3 | | | | | | h | | | |
| | | | a | b | a | b | c | d | e | f | | | g | |
| 3.2.1.5.4.10 | X | | | | | | | | | | | | | |
| 3.2.1.5.4.11 | | | X | | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.4.12 | | | X | | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.5 | | | X | | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.5.1 | | | X | | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.5.1.1 | | | X | | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.5.1.2 | | | X | | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.5.1.2.1 | | | X | | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.5.1.3 | | | X | | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.5.1.3.1 | | | X | | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.5.1.3.2 | | | X | | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.5.1.3.2.1 | | | X | | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.5.1.3.3 | | | X | | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.5.2 | | | X | | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.5.3 | | | X | | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |

Table XXI. Performance and Design Verification Matrix (Cont)

VERIFICATION METHOD

- 1. Analysis
- 2. Assessment
 - a. Inspection
 - b. Review of Design

- 3. Test
 - a. Development
 - b. Qualification
 - c. Acceptance
 - d. Vehicle Acceptance
 - e. Pre-Flight Checkout
 - f. Horizontal Flight
 - g. Vertical Flight
 - h. Major Ground Test

Seller-Conducted

Buyer-Conducted

N/A - Not Applicable

| Section 3 and 5 Requirement No. | Verification Method | | | | | | | | | | | Section 4 Requirement No. | |
|---------------------------------|---------------------|---|---|---|---|---|---|---|---|---|---|---------------------------|---|
| | N/A | 1 | 2 | | 3 | | | | | | h | | |
| | | | a | b | a | b | c | d | e | f | | | g |
| 3.2.1.5.5.4 | | | | X | | X | X | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.5.5 | | | | X | | X | X | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.5.6 | | | | X | | X | X | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.5.7 | | | | X | | X | X | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.5.8 | | | | X | | X | X | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.5.6 | X | | | | | | | | | | | | |
| 3.2.1.5.6.1 | X | | | | | | | | | | | | |
| 3.2.1.5.6.1.1 | | | | X | | X | X | | | | | | 3.2.1.5.11, 3.2.1.5.12, 3.2.1.5.13 (ref only) |
| 3.2.1.5.6.2 | | | | X | X | | | | | | | | 4.2.3, 4.2.4.2.11 |
| 3.2.1.5.6.3 | X | | | | | | | | | | | | |
| 3.2.1.5.6.3.1 | | | | X | | X | X | | | | | | 3.2.1.5.11, 3.2.1.5.12, 3.2.1.5.13 (ref only) |
| 3.2.1.5.7 | | | | X | | | | | | | | | 4.2.3 |
| 3.2.1.5.7.1 | X | | | | | | | | | | | | |
| 3.2.1.5.7.1.1 | | | | X | X | | | | | | | | 4.2.3, 4.2.4.2.11 |
| 3.2.1.5.8 | | X | | | X | | | | | | | | 4.2.3, 4.2.4.2, 4.2.4.2.11, 4.2.4.1.10 |

| | | | | | | | |
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Table XXI. Performance and Design Verification Matrix (Cont)

VERIFICATION METHOD

- | | | | |
|---------------------|------------------------|------------------|------------------|
| 1. Analysis | 3. Test | a. Development | Seller-Conducted |
| 2. Assessment | | b. Qualification | |
| a. Inspection | | c. Acceptance | |
| b. Review of Design | d. Vehicle Acceptance | Buyer-Conducted | |
| | e. Pre-Flight Checkout | | |
| | f. Horizontal Flight | | |
| | g. Vertical Flight | | |
| | h. Major Ground Test | | |
- N/A - Not Applicable

| Section 3 and 5 Requirement No. | Verification Method | | | | | | | | | | | Section 4 Requirement No. | | |
|---------------------------------|---------------------|---|---|---|---|---|---|---|---|---|---|---------------------------|---|----------------------------|
| | N/A | 1 | 2 | | 3 | | | | | | | | | |
| | | | a | b | a | b | c | d | e | f | g | | h | |
| 3.2.1.5.9 | | X | X | X | | X | | | | | | | | 4.2.3, 4.2.2.1, 4.2.4.1.3 |
| 3.2.1.5.10 | X | | | | | | | | | | | | | |
| 3.2.1.5.11 | X | | | | | | | | | | | | | |
| 3.2.1.5.11.1 | | | | X | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.2.11 |
| 3.2.1.5.11.2 | | | | X | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.2.11 |
| 3.2.1.5.11.3 | | | | X | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.2.11 |
| 3.2.1.5.11.4 | X | | | | | | | | | | | | | |
| 3.2.1.5.11.5 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2 |
| 3.2.1.5.11.6 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2 |
| 3.2.1.5.11.7 | X | | | | | | | | | | | | | |
| 3.2.1.5.12 | X | | | | | | | | | | | | | |
| 3.2.1.5.12.1 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2 |
| 3.2.1.5.12.2 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2 |
| 3.2.1.5.12.3 | | | | X | | X | | | | | | | | 4.2.3, 4.2.4.1.2 |
| 3.2.1.5.12.4 | | | | X | X | | | | | | | | | 4.2.3, 4.2.4.2.11 |
| 3.2.1.5.12.5 | | | | X | | X | | | | | | | | 4.2.3, 4.2.4.1.2 |
| 3.2.1.5.13 | X | | | | | | | | | | | | | |
| 3.2.1.5.13.1 | | | | X | X | | | | | | | | | |
| 3.2.1.5.13.2 | | | | X | X | | | | | | | | | 4.2.3, 4.2.4.2.11 |
| 3.2.1.5.14 | | | | X | X | X | X | | | | | | | 4.2.3, 4.2.2.2 |
| 3.2.1.6 | X | | | | | | | | | | | | | |
| 3.2.1.6.1 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.6.2 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2 |
| 3.2.1.6.2.1 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2 |

Table XXI. Performance and Design Verification Matrix (Cont)

VERIFICATION METHOD

- 1. Analysis
- 2. Assessment
 - a. Inspection
 - b. Review of Design

- 3. Test
 - a. Development
 - b. Qualification
 - c. Acceptance
 - d. Vehicle Acceptance
 - e. Pre-Flight Checkout
 - f. Horizontal Flight
 - g. Vertical Flight
 - h. Major Ground Test

Seller-Conducted

Buyer-Conducted

N/A - Not Applicable

| Section 3 and 5 Requirement No. | Verification Method | | | | | | | | | | | Section 4 Requirement No. | | |
|---------------------------------|---------------------|---|---|---|---|---|---|---|---|---|---|---------------------------|---|-------------------------------------|
| | N/A | 1 | 2 | | 3 | | | | | | | | | |
| | | | a | b | a | b | c | d | e | f | g | | h | |
| 3.2.1.6.2.2 | X | | | | | | | | | | | | | |
| 3.2.1.6.2.3 | X | | | | | | | | | | | | | |
| 3.2.1.6.2.4 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.6.3 | X | | | | | | | | | | | | | |
| 3.2.1.6.3.1 | X | | | | | | | | | | | | | |
| 3.2.1.6.3.1.1 | | | | X | X | X | X | | | | | | | 4.2.3, 4.2.4.2.11, 4.2.2.2, 4.2.4.1 |
| 3.2.1.6.3.1.2 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.6.3.1.3 | X | | | | | | | | | | | | | |
| 3.2.1.6.4 | X | | | | | | | | | | | | | |
| 3.2.1.6.4.1 | X | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2 |
| 3.2.1.6.4.2 | X | | | | | | | | | | | | | |
| 3.2.1.6.4.3 | X | | | | | | | | | | | | | |
| 3.2.1.6.4.4 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.6.4.5 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.6.5 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2 |
| 3.2.1.6.5.1 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2 |
| 3.2.1.6.5.2 | X | | | | | | | | | | | | | |
| 3.2.1.6.5.3 | X | | | | | | | | | | | | | |
| 3.2.1.6.5.4 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2 |
| 3.2.1.6.5.5 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2 |
| 3.2.1.6.6 | X | | | | | | | | | | | | | |
| 3.2.1.6.6.1 | X | | | | | | | | | | | | | |

Table XXI. Performance and Design Verification Matrix (Cont)

VERIFICATION METHOD

- 1. Analysis
- 2. Assessment
 - a. Inspection
 - b. Review of Design

- 3. Test
 - a. Development
 - b. Qualification
 - c. Acceptance
 - d. Vehicle Acceptance
 - e. Pre-Flight Checkout
 - f. Horizontal Flight
 - g. Vertical Flight
 - h. Major Ground Test

Seller-Conducted

Buyer-Conducted

N/A - Not Applicable

| Section 3 and 5 Requirement No. | Verification Method | | | | | | | | | | | Section 4 Requirement No. | | |
|------------------------------------|---------------------|---|---|---|---|---|---|---|---|---|---|------------------------------|---|----------------------------|
| | N/A | 1 | 2 | | 3 | | | | | | h | | | |
| | | | a | b | a | b | c | d | e | f | | | g | |
| 3.2.1.6.6.2 | X | | | | | | | | | | | | | |
| 3.2.1.6.6.3 | X | | | | | | | | | | | | | |
| 3.2.1.6.6.4 | X | | | | | | | | | | | | | |
| 3.2.1.6.6.5 | X | | | | | | | | | | | | | |
| 3.2.1.5.5.6 | X | | | | | | | | | | | | | |
| 3.2.1.7 | X | | | | | | | | | | | | | |
| 3.2.1.7.1 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.7.1.1 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.7.1.2 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.7.1.3 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.7.1.5 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.7.1.6 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.7.1.7 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.7.1.8 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.7.2 | X | | | | | | | | | | | | | |
| 3.2.1.7.2.1 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.7.2.2 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.7.2.3 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |

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Table XXI. Performance and Design Verification Matrix (Cont)

VERIFICATION METHOD

- 1. Analysis
- 2. Assessment
 - a. Inspection
 - b. Review of Design

- 3. Test
 - a. Development
 - b. Qualification
 - c. Acceptance
 - d. Vehicle Acceptance
 - e. Pre-Flight Checkout
 - f. Horizontal Flight
 - g. Vertical Flight
 - h. Major Ground Test

Seller-Conducted

Buyer-Conducted

N/A - Not Applicable

| Section 3 and 5 Requirement No. | Verification Method | | | | | | | | | | | Section 4 Requirement No. | | | |
|---------------------------------|---------------------|---|---|---|---|---|---|---|---|---|---|---------------------------|---|--|-------------------------------------|
| | N/A | 1 | 2 | | 3 | | | | | | | | | | |
| | | | a | b | a | b | c | d | e | f | g | | h | | |
| 3.2.1.7.3 | X | | | | | | | | | | | | | | |
| 3.2.1.7.3.1 | | | | X | | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.7.3.2 | X | | | | | | | | | | | | | | |
| 3.2.1.7.3.2.1 | | | | X | | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.7.3.2.2 | | | | X | | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.7.3.2.4 | | | | X | | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.7.3.3 | | | | X | | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.7.3.4 | | | | X | | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.7.3.5 | | | | X | | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.7.3.6 | | | | X | | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.7.3.7 | | | | X | | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.7.3.8 | | | | | X | X | X | | | | | | | | 4.2.3, 4.2.4.1, 4.2.2.2, 4.2.4.2.11 |
| 3.2.1.7.3.9 | | | | | | X | X | | | | | | | | 4.2.3, 4.2.4.1, 4.2.2.2 |
| 3.2.1.7.3.10 | | | | | | X | X | | | | | | | | 4.2.3, 4.2.4.1, 4.2.2.2 |
| 3.2.1.7.3.11 | | | | X | | X | X | | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |

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Table XXI. Performance and Design Verification Matrix (Cont)

VERIFICATION METHOD

- 1. Analysis
- 2. Assessment
 - a. Inspection
 - b. Review of Design

- 3. Test
 - a. Development
 - b. Qualification
 - c. Acceptance
 - d. Vehicle Acceptance
 - e. Pre-Flight Checkout
 - f. Horizontal Flight
 - g. Vertical Flight
 - b. Major Ground Test

Seller-Conducted

Buyer-Conducted

N/A - Not Applicable

| Section 3 and 5 Requirement No. | Verification Method | | | | | | | | | | | Section 4 Requirement No. | |
|---------------------------------|---------------------|---|---|---|---|---|---|---|---|---|---|---------------------------|-------------------------|
| | N/A | 1 | 2 | | 3 | | | | | | h | | |
| | | | a | b | a | b | c | d | e | f | | | g |
| 3.2.1.7.3.12 | | | | X | | X | X | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.7.6 | | | | X | | X | X | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.8 | X | | | | | | | | | | | | |
| 3.2.1.8.1 | X | | | | | | | | | | | | |
| 3.2.1.8.2 | X | | | | | | | | | | | | |
| 3.2.1.8.2.1 | X | | | | | | | | | | | | |
| 3.2.1.8.2.2 | X | | | | | | | | | | | | |
| 3.2.1.8.3 | X | | | | | | | | | | | | |
| 3.2.1.8.3.1 | | | | X | | X | X | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.8.3.1.1 | | | | X | | X | X | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.8.3.1.2 | | | | X | | X | X | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.8.3.1.3 | | | | X | | X | X | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.8.3.1.5 | | | | X | | X | X | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.8.3.1.6 | | | | X | | X | X | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.8.5 | | | | X | | X | X | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.8.6 | | | | X | | X | X | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1 |
| 3.2.1.9 | | | | X | | | | | | | | | 4.2.3 |
| 3.2.1.10 | X | | | | | | | | | | | | |
| 3.2.1.11 | | | | X | | X | X | | | | | | 4.2.3, 4.2.2.2 |

Table XXI. Performance and Design Verification Matrix (Cont)

VERIFICATION METHOD

1. Analysis

2. Assessment

a. Inspection

b. Review of Design

3. Test

a. Development

b. Qualification

c. Acceptance

d. Vehicle Acceptance

e. Pre-Flight Checkout

f. Horizontal Flight

g. Vertical Flight

h. Major Ground Test

Seller-Conducted

Buyer-Conducted

N/A - Not Applicable

| Section 3 and 5 Requirement No. | Verification Method | | | | | | | | | | | Section 4 Requirement No. | | |
|---------------------------------|---------------------|---|---|---|---|---|---|---|---|---|---|---------------------------|---|-------------------------------|
| | N/A | 1 | 2 | | 3 | | | | | | | | | |
| | | | a | b | a | b | c | d | e | f | g | | h | |
| 3.2.1.11.1 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2 |
| 3.2.1.11.2 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2 |
| 3.2.1.11.3 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2 |
| 3.2.1.12 | X | | | | | | | | | | | | | |
| 3.2.1.12.1 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1.10 |
| 3.2.1.12.2 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1.10 |
| 3.2.1.12.3 | | | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1.10 |
| 3.2.1.12.4 | | X | | X | | X | X | | | | | | | 4.2.3, 4.2.2.2, 4.2.4.1.10 |
| 3.2.2 | X | | | | | | | | | | | | | |
| 3.2.2.1 | | | | X | X | X | X | | | | | | | 4.2.3, 4.2.2.1 |
| 3.2.2.2 | | | | X | X | X | X | | | | | | | 4.2.3, 4.2.2.1 |
| 3.2.2.3 | | | | | | X | X | | | | | | | 4.2.2.1 |
| 3.2.2.4 | | | | | X | | | | | | | | | 4.2.3 |
| 3.2.2.5 | | X | | | | X | | | | | | | | 4.2.4.2 |
| 3.2.3 | X | | | | | | | | | | | | | |
| 3.2.3.1 | | | | X | | | | | | | | | | 4.2.2.1 |
| 3.2.3.2 | | | | | X | | | | | | | | | 4.2.3 |
| 3.2.3.3 | | | | | X | | | | | | | | | 4.2.3 |
| 3.2.4 | X | | | | | | | | | | | | | |
| 3.2.4.1 | | X | | | X | | | | | | | | | 4.2.4.2, 4.2.3 |
| 3.2.4.2 | X | | | | | | | | | | | | | |
| 3.2.4.2.1 | | | | X | X | | | | | | | | | 4.2.2.1, 4.2.3 |
| 3.2.4.2.2 | | | | X | X | | | | | | | | | 4.2.2.1, 4.2.3 |
| 3.2.4.2.3 | | | | X | X | | | | | | | | | 4.2.2.1, 4.2.3 |
| 3.2.4.2.4 | | | | X | X | | | | | | | | | 4.2.2.2.1, 4.2.3 |

Table XXI. Performance and Design Verification Matrix (Cont)

VERIFICATION METHOD

- 1. Analysis
- 2. Assessment
 - a. Inspection
 - b. Review of Design

- 3. Test
 - a. Development
 - b. Qualification
 - c. Acceptance
 - d. Vehicle Acceptance
 - e. Pre-Flight Checkout
 - f. Horizontal Flight
 - g. Vertical Flight
 - h. Major Ground Test

Seller-Conducted

Buyer-Conducted

N/A - Not Applicable

| Section 3 and 5 Requirement No. | Verification Method | | | | | | | | | | | Section 4 Requirement No. | |
|------------------------------------|---------------------|---|---|---|---|---|---|---|---|---|---|------------------------------|--------------------------|
| | N/A | 1 | 2 | | 3 | | | | | | h | | |
| | | | a | b | a | b | c | d | e | f | | | g |
| 3.2.4.2.5 | | | X | X | | | | | | | | | 4.2.2.2.1, 4.2.3 |
| 3.2.4.5.6 | X | | | | | | | | | | | | |
| 3.2.4.5.6.1 | | X | | X | | | | | | | | | 4.2.4.2, 4.2.3 |
| 3.2.4.3 | X | | | | | | | | | | | | |
| 3.2.4.3.1 | | | | X | | | | | | | | | 4.2.3 |
| 3.2.4.3.2 | | | | X | | | | | | | | | 4.2.3 |
| 3.2.4.3.3 | | | | X | | | | | | | | | 4.2.3 |
| 3.2.5 | X | | | | | | | | | | | | |
| 3.2.5.1 | X | | | | | | | | | | | | |
| 3.2.5.1a | | | | | | X | | | | | | | 4.2.4.1.10, 4.2.4.1.2 |
| 3.2.5.1b | | | | | | X | | | | | | | 4.2.4.1.9 4.2.4.1.2 |
| 3.2.5.1c | | X | | | | X | | | | | | | 4.2.4.1.12, 4.2.4.2 |
| 3.2.5.1d | | X | | | | X | | | | | | | 4.2.4.2.12, 4.2.4.2 |
| 3.2.5.1f | X | | | | | | | | | | | | |
| 3.2.5.1f(1) | | | | | | X | | | | | | | 4.2.4.1.3, 4.2.4.1.2 |
| 3.2.5.1f(2) | | | | | | X | | | | | | | 4.2.4.1.3, 4.2.4.1.2 |
| 3.2.5.1g | | X | | | | X | | | | | | | 4.2.4.1.4, 4.2.4 |
| 3.2.5.1h(1) | | X | | | | X | | | | | | | 4.2.4.1.5b, 4.2.4.2 |
| 3.2.5.1h(2) | | X | | | | X | | | | | | | 4.2.4.1.10, 4.2.4.2 |

Table XXI. Performance and Design Verification Matrix (Cont)

VERIFICATION METHOD

- 1. Analysis
- 2. Assessment
 - a. Inspection
 - b. Review of Design

- 3. Test
 - a. Development
 - b. Qualification
 - c. Acceptance
 - d. Vehicle Acceptance
 - e. Pre-Flight Checkout
 - f. Horizontal Flight
 - g. Vertical Flight
 - h. Major Ground Test

Seller-Conducted
Buyer-Conducted

N/A - Not Applicable

| Section 3 and 5 Requirement No. | Verification Method | | | | | | | | | | | Section 4 Requirement No. | | | |
|---------------------------------|---------------------|---|---|---|---|---|---|---|---|---|---|---------------------------|---|--|-----------------|
| | N/A | 1 | 2 | | 3 | | | | | | | | | | |
| | | | a | b | a | b | c | d | e | f | g | | h | | |
| 3.2.5.2 | X | | | | | | X | | | | | | | | 4.2.2 |
| 3.2.5.2a | | | | | | | X | | | | | | | | 4.2.2 |
| 3.2.5.2b | | | | | | | X | | | | | | | | |
| 3.2.5.2c | X | | | | | | X | | | | | | | | 4.2.4.2, |
| 3.2.5.2c(1) | | X | | | | | X | | | | | | | | 4.2.4.1.5a |
| 3.2.5.2c(2) | | | | | | | X | | | | | | | | 4.2.4.2, |
| 3.2.5.2c(3) | | X | | | | | X | | | | | | | | 4.2.4.1.5c |
| 3.2.5.2d | | X | | | | | X | | | | | | | | 4.2.4.2, |
| 3.2.5.2e | | X | | | | | X | | | | | | | | 4.2.4.1.5d |
| 3.2.5.2f | | X | | | | | X | | | | | | | | 4.2.4.2.4 |
| 3.2.5.3 | | X | | | | | X | | | | | | | | 4.2.4.2.5 |
| 3.2.6 | | X | | | | | X | | | | | | | | 4.2.4.1.13 |
| 3.2.6.1 | X | | | | | | X | | | | | | | | 4.2.4.1.13 |
| 3.2.7 | | X | | X | | | X | | | | | | | | 4.2.4.2, 4.2.3, |
| 3.2.7.1 | | | X | X | | | X | | | | | | | | 4.2.4.1.10 |
| 3.2.7.2 | | | | | | | X | X | | | | | | | 4.2.2.1, 4.2.3 |
| 3.2.7.3 | | X | | | | | X | | | | | | | | 4.2.2 |
| 3.3 | | | | | | | X | | | | | | | | 4.2.4.1.10, |
| 3.3.1 | X | | | | X | | | | | | | | | | 4.2.4.2 |
| 3.3.1.1 | | | X | X | | | | | | | | | | | 4.2.3 |
| 3.3.1.2 | | | X | X | | | | | | | | | | | 4.2.3 |
| 3.3.1.3 | | | X | X | | | X | | | | | | | | 4.2.2.1, 4.2.3 |
| 3.3.1.4 | | | | X | | | | | | | | | | | 4.2.3 |
| 3.3.2 | | | | X | | | | | | | | | | | 4.2.3 |
| 3.3.3 | X | | | | | | | | | | | | | | 4.2.3 |

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Table XXI. Performance and Design Verification Matrix (Cont)

VERIFICATION METHOD

1. Analysis
2. Assessment

- a. Inspection
- b. Review of Design ;

3. Test

- a. Development
- b. Qualification
- c. Acceptance
- d. Vehicle Acceptance
- e. Pre-Flight Checkout
- f. Horizontal Flight
- g. Vertical Flight
- h. Major Ground Test

Seller-Conducted

Buyer-Conducted

N/A - Not Applicable

| Section 3 and 5 Requirement No. | Verification Method | | | | | | | | | | | Section 4 Requirement No. | |
|------------------------------------|---------------------|---|---|---|---|---|---|---|---|---|---|------------------------------|------------------------------|
| | N/A | 1 | 2 | | 3 | | | | | | | | |
| | | | a | b | a | b | c | d | e | f | g | | h |
| 3.3.3.1 | | | | X | | X | | | | | | | 4.2.3, 4.2.4.1.8 |
| 3.3.3.2 | | | | X | | | | | | | | | 4.2.3 |
| 3.3.3.2.1 | | | | | | X | X | | | | | | 4.2.2 |
| 3.3.3.2.2 | | | | X | | | | | | | | | 4.2.3 |
| 3.3.4 | X | | | | | | | | | | | | |
| 3.3.4.1 | | | | X | | | | | | | | | 4.2.3 |
| 3.3.4.2 | | | X | | | X | | | | | | | 4.2.2.1 |
| 3.3.4.3 | | | X | | | X | X | | | | | | 4.2.2.1 |
| 3.3.5 | | | | X | | | | | | | | | 4.2.3 |
| 3.3.5.1 | | | | X | | | | | | | | | 4.2.3 |
| 3.3.5.1.1 | | | | X | | | | | | | | | 4.2.3 |
| 3.3.5.1.1.1 | | | | X | | | | | | | | | 4.2.3 |
| 3.3.5.1.2 | | | | X | | | | | | | | | 4.2.3 |
| 3.3.5.1.2.1 | | | | X | | | | | | | | | 4.2.3 |
| 3.3.5.1.3 | | | | X | | | | | | | | | 4.2.3 |
| 3.3.5.2 | | | | X | | | | | | | | | 4.2.3 |
| 3.3.6 | | | | X | | | | | | | | | 4.2.3 |
| 3.3.6.1 | | | | X | | | | | | | | | 4.2.3 |
| 3.3.6.2 | | | | X | | | | | | | | | 4.2.3 |
| 3.3.7 | | | X | X | | X | | | | | | | 4.2.2.1, 4.2.3, 4.2.4.2.7 |
| 3.3.8 | | | X | X | | | | | | | | | 4.2.2.1, 4.2.3 |
| 3.3.9 | X | | | | | | | | | | | | |
| 3.3.9.1 | X | | | | | | | | | | | | |
| 3.3.10 | X | | | | | | | | | | | | |
| 5. | X | | | | | | | | | | | | |
| 5.1 | X | | | | | | | | | | | | |
| 5.2 | | | | X | | | | | | | | | 4.2.3 |

Table XXI. Performance and Design Verification Matrix (Cont)

VERIFICATION METHOD

- | | | | |
|----------------------|------------------------|------------------|------------------|
| 1. Analysis | 3. Test | a. Development | Seller-Conducted |
| 2. Assessment | | b. Qualification | |
| a. Inspection | | c. Acceptance | |
| b. Review of Design | d. Vehicle Acceptance | Buyer-Conducted | |
| N/A - Not Applicable | e. Pre-Flight Checkout | | |
| | f. Horizontal Flight | | |
| | g. Vertical Flight | | |
| | h. Major Ground Test | | |

| Section 3 and 5 Requirement No. | Verification Method | | | | | | | | | | | Section 4 Requirement No. | |
|------------------------------------|---------------------|---|---|---|---|---|---|---|---|---|---|------------------------------|----------------|
| | N/A | 1 | 2 | | 3 | | | | | | h | | |
| | | | a | b | a | b | c | d | e | f | | | g |
| 5.2.1 | | | | X | | | | | | | | | 4.2.3 |
| 5.2.2 | | | | X | | | | | | | | | 4.2.3 |
| 5.2.3 | X | | | | | | | | | | | | |
| 5.2.3a | | X | | | | X | | | | | | | 4.2.4.1.13 |
| 5.2.3b | | X | | | | X | | | | | | | 4.2.4.1.13 |
| 5.2.3c | | X | | | | X | | | | | | | 4.2.4.1.13 |
| 5.2.3d | | X | | | | X | | | | | | | 4.2.4.1.13 |
| 5.2.3e | | X | | | | X | | | | | | | 4.2.4.1.13 |
| 5.2.3f | | X | | | | X | | | | | | | 4.2.4.1.13 |
| 5.2.3g | | X | | | | X | | | | | | | 4.2.4.1.13 |
| 5.2.3h | | X | | | | X | | | | | | | 4.2.4.1.13 |
| 5.2.3i | | X | | | | X | | | | | | | 4.2.4.1.13 |
| 5.2.3j | | X | | | | X | | | | | | | 4.2.4.1.13 |
| 5.2.3k | | X | | | | X | | | | | | | 4.2.4.1.13 |
| 5.2.3l | | X | | | | X | | | | | | | 4.2.4.1.13 |
| 5.2.4 | X | | | | | | | | | | | | |
| 5.2.5 | | | X | | | | X | | | | | | 4.2.2.1 |
| 5.2.6 | X | | | | | | | | | | | | |
| 5.2.7 | X | | | | | | | | | | | | |
| 5.2.8 | | | X | X | | | X | | | | | | 4.2.2.1, 4.2.3 |

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5. PREPARATION FOR DELIVERY

5.1 General Requirements. The requirements specified herein govern the preparation for shipment and the transport of the GPC to all Buyer and Government facilities. The methods of preservation, packaging and packing utilized for shipment together with necessary special control during transportation shall adequately protect the GPC from damage or degradation of performance due to the natural and induced environments encountered during transportation and subsequent storage as specified herein.

5.2 Detailed Requirements. Packaging, handling, and transportation shall be in accordance with applicable requirements and guidelines of MHB6000.1(1A) as supplemented by the following subparagraphs.

5.2.1 Preservation and Packaging. Preservation and packaging shall be in accordance with the requirements of Level B of MIL-STD-794.

5.2.2 Packaging. Packing shall be in accordance with the requirements of Level B of MIL-STD-794.

5.2.3 Design Requirements (Structural). Preservation, packaging, and packing shall be designed to withstand the rough handling package requirements of MIL-STD-794 as defined in FED-STD-101 (without damage or degradation to the useful life performance, and reliability of the contained item without damage to the preservation, packaging, and packing which would affect their utility) in accordance with the following:

a. Rough Handling

Gross Weight and Dimensions

Less than 200 pounds and not exceeding 60 inches on any edge or diameter.

FED-STD-101 Method

5007 Procedure E Free Fall Corner Drop (Level A)
 5007 Procedure B Free Fall Flat Drop (Level A)
 5016 Superimposed Load (with damage, Level A)
 5019 Vibration (Repetitive shock)
 5020 Sinusoidal Vibration

b. Pressure

(1) Transportation: Air 3.28 to 15.23 psia
 Ground 9.76 to 15.23 psia

(2) Storage: 12.4 to 15.23 psia

c. Temperature

(1) Transportation: Air Minimum; Minus 25°F
 Maximum; Plus 150°F for 6 hours

Ground Minimum; Minus 20°F
 Maximum; Plus 150°F for 6 hours

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(2) Storage: Uncontrolled . . Minimum; Minus 20°F
Maximum; Plus 150°F for 6 hours

Controlled . . Nominal; Plus 60 to
Plus 80°F

*Minimum; Plus 25°F
*Maximum; Plus 115°F

*Duration 4 hours maximum

d. Humidity Air 0 to 100 percent relative
Ground 8 to 100 percent relative

e. Salt Spray 1.0 percent by weight salt solution for
30 days.

f. Sand and Dust

*Sand Particle Diameter: 0.0031 to 0.039 inches
Suspended Sand: 1.2 pounds per cubic foot
**Dust Particle Diameter: 0.0000039 to 0.0031 inches
Suspended Dust: 3.7 x 10 pounds per cubic foot
Sand and Dust Particle Hardness: 7 to 8 MOH Scale
Wind Speed: 33 feet per second

*90 percent or more between 0.0037 and 0.012 inches.

**90 percent or more between 0.0000039 and 0.000079 inches.

g. Fungus As specified in MIL-STD-454.

h. Ozone 3 to 6 parts per hundred million
(ppm). Total oxidant concentrations
may reach 60 ppm for 1 to 3 hours in
any 24 hour period.

i. Rain Maximum of 19 inches during any 24 hour
period, including short period extremes
of 4 inches per hour.

j. Rail Maximum Diameter: 2 inches
Fall Velocity: 100 feet/second
Railstone Density: 50 lb/cu ft
Wind Speed: 33 ft/sec
Hardness, MOH Scale: 2 to 4
Duration: 15 minutes max

k. Snow 10.2 pounds per square foot.

l. Solar Radiation 363 BTU/ft²/hour for 6 hours per
day for two weeks./

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5.2.4 Reusable Containers. Where analysis in accordance with NHB6000.1(1A) indicates a requirement for reusable containers, maximum practical utilization shall be made of standard off-the-shelf, low cost, metal or plastic containers.

5.2.5 Temporarily Installed Hardware Identification. All temporarily installed devices such as caps, plugs, covers, support bracketry, protective plates, etc., shall be cerise red in color or shall have attached cerise red colored streamers to ensure that they are easily identified under casual observation. Reusable protective devices shall be labeled "REUSABLE ITEM, DO NOT DESTROY, RETAIN FOR REUSE."

5.2.6 Packaging and Labeling of Ordnance. Deleted.

- k. Snow 10.2 pounds per square root.
- l. Solar Radiation 363 BTU/ft²/hour for 6 hours per day for two weeks.

5.2.4 Reusable Containers. Where analysis in accordance with NHB6000.1(1A) indicates a requirement for reusable containers, maximum practical utilization shall be made of standard off-the-shelf, low cost, metal or plastic containers.

5.2.5 Temporarily Installed Hardware Identification. All temporarily installed devices such as caps, plugs, covers, support bracketry, protective plates, etc., shall be cerise red in color or shall have attached cerise red colored streamers to ensure that they are easily identified under casual observation. Reusable protective devices shall be labeled "REUSABLE ITEM, DO NOT DESTROY, RETAIN FOR REUSE."

5.2.6 Packaging and Labeling of Ordnance. Deleted.

5.2.7 Pre-Production Packaging Qualification Tests. Testing to verify the functional capability of the package or transport methods/equipment shall be accomplished as required by Section 4 of this specification.

5.2.8 Marking for Shipment. Interior and exterior containers shall be marked and labeled in accordance with MIL-STD-129 including precautionary markings necessary to ensure safety of personnel and facilities and to ensure safe handling, transport, and storage. For hazardous materials, markings shall also comply with applicable requirements governing packaging and labeling of hazardous materials. Packages with reuse capability shall be identified with the words "REUSABLE CONTAINER - DO NOT DESTROY RETAIN FOR REUSE." NASA Critical Item Labels (Form 1368 series) shall be applied in accordance with NHB6000.1(1A). Identification information on interior and exterior containers shall be in the following format and shall include:

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BUYER CONTROL NUMBER _____

ITEM NAME _____

FSN/NATO STOCK NUMBER _____ (WHEN APPLICABLE)

MANUFACTURER'S TYPE OR PART NUMBER _____

QUANTITY IN PACKAGE _____ TRACEABILITY IDENTIFICATION _____

AGE CONTROL MARKING _____

CLEANING MARKING _____ (NOT APPLICABLE)

SERIAL NUMBER _____

MANUFACTURER _____

BUYER PURCHASE ORDER NUMBER _____

DATE OF PACKAGING _____

LEVELS OF PACKAGING AND PACKING _____

MANUFACTURER'S PACKAGE PART NUMBER _____ (NOT REQUIRED FOR OFF-THE-SHELF CONTAINERS)

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6. NOTES

6.1 Definitions.

6.1.1 Acceptance Tests. Inspection and tests to determine that a part, component, subsystem or system is capable of meeting design and performance requirements specified herein.

6.1.2 Assessment. A verification method employing inspection and review of design techniques to verify design features not covered by verification test and analysis such as finishes, tolerances, bonding, identification traceability, safety wiring, warning and servicing labels, Bill of Materials, etc.

6.1.3 Classification.

Type. This term denotes differences in like items or processes as to design, model, shapes, etc., and is designated by upper case Roman numerals (e.g., Type I, Type II).

Class. This term denotes differences in performance or physical characteristics and is designated by Arabic numerals (e.g., Class 1, Class 2).

Grade. This term denotes differences in quality of an item and is designated by capital letters (e.g., Grade A, Grade B).

6.1.4 Certification. Certification consists of qualification testing, major ground test, and other tests and analysis required to determine that the design hardware from the component through the subsystem level meets requirements.

- a. Qualification Test. Those tests conducted as part of the certification program to demonstrate that design requirements can be realized under specified conditions.
- b. Certification by Analysis. Certification by analysis allows the use of appropriate engineering analysis including simulation to provide fulfillment of certification objectives. Certification analysis will normally be conducted due to one or both of the following factors.

(1) The inability to simulate flight conditions in an effective ground test.

(2) Qualification testing would not be practical.

Analysis may be used where it can be shown that the article is similar or identical in design, manufacturing processes, and quality control to another article that has been previously certified to equivalent or more stringent criteria.

6.1.5 Development Tests. These tests performed with minimum rigors and controls to verify a design approach.

6.1.6 Fail Operational. The ability to sustain a failure and retain safe, full operational capability (mission continuation).

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6.1.7 Fail Safe. The ability to detect a failure and retain safe operational capability (successfully terminate the mission).

6.1.8 Failure. The inability of a system, subsystem, component, or part to perform its required function within specified limits, under specified conditions for a specified duration.

6.1.9 Line Replaceable Unit (LRU). A combination of components, units, parts, assemblies, subassemblies, etc., that are contained in one package or are so arranged that together the combination is common to one mounting; and in addition, provides a complete function(s) to the larger entity within which it operates. In order to aid in the further definition on an individual basis, the following list of characteristics which can be attributed to a line replaceable unit are provided.

- a. It can be verified as ready for installation in an off-vehicle environment.
- b. After installation readiness verification, it can be installed in any vehicle or GSE and item without regard to serial number.
- c. The installation does not require manufacturing type tooling of dimensional or other similar nature.
- d. It does not require engineering support during the installation or removal.
- e. It does not require more time or involve more spares costs or other resources than is next assembly for installation or removal.

6.1.10 Shop Replaceable Unit (SRU). A SRU is an integral subassembly of a LRU consisting of units and parts or a combination of parts so arranged that together the combination is common to one mounting; and in addition, provides a complete function to the larger entity within which it operates.

6.1.11 Scheduled Maintenance. The action performed in an attempt to retain an item in a specified condition by providing systematic inspection, detection, and servicing for the prevention of incipient failure.

6.1.12 Operating Cycles. The cumulative number of times an item completes a sequence of activation and return to its initial state; e.g., a switched-on/switched-off sequence, a valve-opened/valve-closed sequence, a tank pressurized/depressurized, or Dewar cryogenic exposure/drain.

6.1.13 Operating Life. The specified operating time/cycles which an item can accrue before replacement or refurbishment without risk of degradation or performance beyond acceptable limits.

6.1.14 Preflight Checkout. Verifies that the flight hardware functions within prescribed limits when the subsystem are operated alone, or together as an integrated vehicle.

6.1.15 Structural Safe-Life. A design approach under which structural failure will not occur because of undetected flaws and/or fatigue damage during the specified service life of the article; also, the period of time for which the integrity of the structure can be ensured in the expected operating environments.

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6.1.16 Shelf Life. That period of time during which an item can remain in storage without having its operability affected. Preventive maintenance, servicing, and replacement of age-sensitive material parts shall be permitted on a scheduled basis during the storage period.

6.1.17 Single Failure Point. A hardware failure which, by itself, could result in a safety hazard or serious impairment (or loss) of functional capability.

6.1.18 Single Failure Point Summary (SFPS). Summary listing of those single failure points identified in the failure mode and effects analysis.

6.1.19 Useful Life. The item's total life span including operating life and storage with normal preventive maintenance, servicing, repair, and replacement of parts before item is considered unacceptable for further usage. This life span may be equal to (throw-away), or greater than (repair, refurbishable) the value specified for "operating life."

6.1.20 Verification. The process of planning and implementing a program that determines that the item meets all design, performance, and safety requirements. The verification process includes certification, development testing, acceptance testing, assessment, flight demonstration, preflight checkout, and analysis necessary to support the total verification plan.

6.1.21 Torr. The Torr is defined as 1/760 of a standard atmosphere or 1,013,250/760 dynes per square centimeter. This is equivalent to defining the Torr as 1333.22 microbars, and differs by only one part in seven million from the International Standard millimeter of mercury.

6.1.22 Sheltered. A warehouse type facility, enclosed, and providing protection against environmental conditions.

6.1.23 Unsheltered. An open area unprotected against environmental conditions.

6.1.24 Page Cable Assembly. A logic page containing an integral cable to an LRU external connector.

6.1.25 Cable Core. Cable core is that group of conductors and associated shields which terminate at one equipment interface connector exclusive of any overall shield.

6.1.26 Built-In Test (BIT). Is defined as additional circuitry implemented in the basic design of an LRU or system for the purpose of failure detection and/or reporting operational and/or health status of the LRU. Built-in test is defined to include: built-in test equipment (BITE), self-test, and test points.

- a. Built-In Test Equipment (BITE). That circuitry provided to perform continuous monitoring of specific parameters, groups of parameters or functions of the LRU to provide a GO/NO-GO indication. This type of built-in test capability represent those implementational at techniques which are autonomous in nature, provide continuous real-time monitoring, but do not interrupt normal operation of the LRU.
- b. Self-Test. That circuitry contained in the LRU which provide the means to simulate operation of a LRU for the purpose of functional verification. This type of built-in test capability is non-autonomous in nature in that it may require an external initiation and does interrupt the normal operation of the LRU.

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- c. **Test Points.** Those measurements of LRU parameters which are provided at the electrical interface of the LRU to enable determination of the relative health or operational status of the individual unit.
- d. **Unaugmented Test.** Is defined as a test that does not require the use of the computer in a mode other than the normal operational mission of data reception/command generation.
- e. **Probability of Failure Calculation.** An acceptable way to calculate the probability of failure detection for a LRU is:

1. **Failure Rate of Undetected Item Parts.**

Total failure rate of items that effect LRU ability to meet CEI performance requirements.

For this calculation one can assume the input data to the LRU are correct and the output faults are due only to the sending LRU.

6.1.27 **Miscellaneous.**

- a. **Bond.** A controlled connection resulting in a defined low-impedance dc and RF path.
- b. **Checkout.** Checkout is a test conducted on an item to determine its condition or operable status.
- c. **Failure Criteria.** Variations of operational and performance characteristics which are outside of the limits permitted by the detail equipment specification deem the equipment failed. Deterioration and material failure of any part of material which could in any manner prevent the equipment from meeting operational, performance, and reliability requirements during service life shall provide reason to consider the equipment as having failed.
- d. **Minimum Cooling Airflow.** The minimum cooling airflow is the rate required to prevent the temperature of all critical components within a given unit from exceeding safe levels.
- e. **Module.** A module is a removable plug-in part of an equipment.
- f. **Processor State.** Volatile registers which define the current status and exchange sequence of a program.
- g. **Power Common.** This conductor is used for a current-carrying return path for more than one power source or load.
- h. **Power Reference Tie.** This conductor between power circuits is used to establish a voltage relationship (not primarily a current-carrying conductor).
- i. **Power Return.** This conductor is used for current-carrying return path for one load.
- j. **Shield Reference Tie.** A conductor from a shield to any other points is a shield reference tie.

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- k. **Signal Return.** This conductor is used for a signal-carrying path for one load.
- l. **Structure Tie.** A conductor between structural members is a structure tie.
- m. **Full Duplex.** Full-duplex operation is the method wherein a common transmitter-receiver unit can send and receive information simultaneously over the same channel.
- n. **Half Duplex.** Half-duplex operation is the method wherein a common transmitter-receiver unit can send and receive information on the same channel, but not simultaneously.
- o. **Cyclic.** The sequential process whereby one item is followed by another in a serial fashion is described as cyclic.
- p. **Dummy Load.** For the purpose of shock tests, a dummy load is a duplication of the shape, size, rigidity, mounting methods, weight, mass distribution and center-of-gravity of the qualification unit. There is no requirement that it be a functioning device.

6.2 **Abbreviations and Acronyms.** Abbreviations and acronyms used in this specification are defined as follows:

| | |
|-----------------|--|
| Al | Aluminum |
| amp | Ampere |
| ATT | Acceptance thermal tests |
| AVT | Acceptance vibration tests |
| AGE | Aerospace ground equipment |
| BCE | Bus control element |
| BITE | Built-in test equipment |
| BTE | Bench test equipment |
| Btu | British thermal unit |
| BW | Bandwidth |
| BPCS | Backup flight control system |
| CG | Center of Gravity |
| COS/MOS | Complementary symmetry/metal oxide semiconductor |
| cm ³ | Cubic centimeter |
| CPU | Central processor unit |
| Cu | Copper |
| CW | Continuous wave |
| DA | Double amplitude |
| DACBU | Data acquisition and control buffer unit |
| db | Decibel |
| dc | Direct current |
| DEU | Display electronics unit |
| DMA | Direct memory access |
| ECC | Error Correction Code |
| EEE | Electronic/electrical/electromechanical |
| EIU | Engine interface unit |
| EMC | Electromagnetic compatibility |

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| | |
|-----------------------------------|--|
| F | Fahrenheit |
| ft | Foot or feet |
| ft² | Square foot or feet |
| ft³ | Cubic feet |
| FSN | Federal stock number |
| FCOS | Flight control operating system |
| GPC | General purpose computer |
| GSE | Ground support equipment |
| He | Helium |
| Hg | Mercury |
| hr | Hour |
| Hz | Hertz (cycles per second) |
| ICC | Intercomputer communication channel |
| IOP | Input/output processor |
| k | Kilohm |
| kHz | Kilohertz (kilocycles per second) |
| Km | Kilometers |
| lb | Pound |
| LRU | Line replaceable unit |
| ma | Milliamper |
| MDM | Multiplexer/demultiplexer |
| mg | Milligram |
| MHz | MegaHertz (megacycles per second) |
| ml | Milliliter |
| mm | Millimeter |
| MM | Mass memory |
| MCH | Monomethylhydrazine |
| MOS | Metal oxide semiconductor |
| ms | Millisecond |
| MSC | Master sequence controller |
| MSFC | Marshall Space Flight Center |
| MTBF | Mean time between failures |
| mv | Millivolt |
| MTTR | Mean time to repair |
| MUX | Multiply |
| NASA | National Aeronautics and Space Administration |
| NATO | North Atlantic Treaty Organization |
| NDE | Non-destructive evaluation |
| N₂ | Nitrogen |
| N₂O₄ | Nitrogen Tetroxide |
| Ni | Nickel |
| nsec | Nanosecond |
| NVR | Non-volatile residue |
| O₂ | Oxygen |
| OI | Operational instrumentation |

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|------|--|
| Pb | Lead |
| PCI | Program control unit |
| pcw | Pulse continuous wave |
| PCO | Program control output |
| PMIA | Parallel multiplexer interface adapter |
| ppm | Parts per million |
| PROM | Programmable read only memory |
| psi | Pounds per square inch |
| psia | Pounds per square inch absolute |
| psid | Pounds per square inch differential |
| psig | Pounds per square inch gauge |
| phm | Parts per hundred million |
| | |
| Q | Magnification factor |
| | |
| RAM | Random access memory |
| RC | Resistance capacitance |
| rf | Radio frequency |
| rms | Root mean square |
| ROS | Read only store |
| ROM | Read only memory |
| | |
| SD | Space Division |
| sec | second |
| SRU | Shop replaceable unit |
| std | Standard |
| STP | Self-test programs |
| | |
| TBS | To be supplied by seller |
| TF | Trichlorotrifluorethane |
| | |
| usec | Microseconds |
| | |
| vdc | Volts direct current |
| V/m | Volts per meter |

| | | | | | | | |
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APPENDIX I

10. PROTOTYPE MODEL

10.1 Scope. This appendix establishes the performance, design, development, and verification requirements for the prototype configuration of the GPC, orbiter.

10.1.1 Classification. All requirements of the basic specification shall apply.

10.2 Applicable Documents

10.2.1 Applicability. The documents listed in Section 2 of the basic specification shall apply.

10.3 Requirements. The requirements of Section 3. of the basic specification shall apply, except as follows:

a. Deviations in components or process requirements may be granted upon request from the seller.

10.3.1 Item Identification. The identification of the prototype model shall be as follows:

| <u>Nomenclature and Mfr Code Ident. No.</u> | <u>Buyer Control No.</u> | <u>Seller Part No.</u> | <u>Traceability Classification</u> |
|---|--------------------------|----------------------------|--|
| GPC | MC615-0025-2000 | 6966000-1 | Serial |

10.4 Quality Assurance Provisions. The provisions of Section 4 of this specification are waived. The supplier shall submit an acceptance test procedure for the buyer's approval and shall conduct acceptance tests in accordance with the approved procedure.

10.5 Preparation for Delivery. The requirements of this section of the basic specification shall apply.

10.6 Notes. The requirements of Section 6. of this specification shall apply.

SHUTTLE

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| PREPARED BY G.F. McMullen <i>5/14</i> D/292-440 <i>5237</i> | CODE IDENT. NO. 03953 <i>6</i> | DOCUMENT NUMBER MC615-0025 | REV A | SEQ 01 |
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| Rockwell International | | AUTHORITY G. O. 40977 | | |
| AMENDMENT | | DATE 4-16-85 | PAGE OF | 1 16 |
| COMPUTER, GENERAL PURPOSE ORBITER | | SUBJECT CHANGE <i>79</i> | | |

This amendment forms a part of MC615-0025, new, dated September 19, 1984.

Page 3

WAS: MF0004-400
30 August 1977
Amendment CO4
4 November 1982

IS: MF0004-400C
18 June 1984
Amendment D-01
14 December 1984

WAS: MC615-0010
2 November 1974
Amendment A-03
26 November 1974

Adapter, Interface, IOP Multiplexer

IS: MC615-0010B
13 August 1975
Amendment C-01
18 June 1980
Amendment C-02
24 September 1984
Amendment C-03
3 April 1985

Adapter, Interface, Serial Multiplexer

ADD: MT0802-106
16 December 1984

Quality Assurance requirements for subcontractors
of electrical, electronic, and electromechanical
parts for the Shuttle program

Page 25, Paragraph 3.1.3

WAS: "Item"

IS: Nomenclature and Mfr.
Code Ident. No.

Computer, General
Purpose. 03640

EOCN ABM949

1985 APR 22 AM 10:38

RELEASED

CODE IDENT. NO. 03953

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Page 192, Paragraph 10.3.1

WAS: Nomenclature and Mfr.
Code Ident. No.

GPC

IS: Nomenclature and Mfr.
Code Ident. No.

Computer, General
Purpose. 03640

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ADD: 11. Appendix II pre-production configuration

ADD: Page 193

APPENDIX II

11. PRE-PRODUCTION CONFIGURATION

11.1 SCOPE

The pre-production GPC's are to be manufactured utilizing a combination of qualified parts and parts that do not meet the requirements of the Quality Assurance Requirements Specification, MT0802-106 or Amendment D-01 of the Electrical, Electronic, and Electromechanical Orbiter Parts List (OPPL), MF0004-400C.

These parts are "equivalent parts" that have not been subjected to the additional requirements imposed by Amendment D-01 and MT0802-106.

The pre-production GPC's are to be restricted to nonflight use and are to be identified with the following part number:

Rockwell Part No.IBM Part No.

MC615-0025-3000

6966000-2

In order to minimize the use of "equivalent parts," qualified parts shall be used whenever possible.

With the exceptions noted above the requirements of the basic specification shall apply.

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Page 47, Paragraph 3.2.1.3.9

Delete the last two sentences and add:

The frequency of the oscillator shall have an accuracy of plus or minus .001 percent at the standard temperature condition specified in Paragraph 4.1.2.1. The frequency shall be stable within .001 percent from 30 minutes to 7 days under the ambient temperatures specified in Paragraph 4.1.2.1, but the frequency accuracy of plus or minus .0045 percent is permitted for the first 30 minutes of operation within the operating environment specified. The turn-on time of the oscillator shall not exceed 100 milliseconds from the time master power reset is released after application of primary power.

Page 12

Replace Figure 4 with the enclosed figure

Page 7

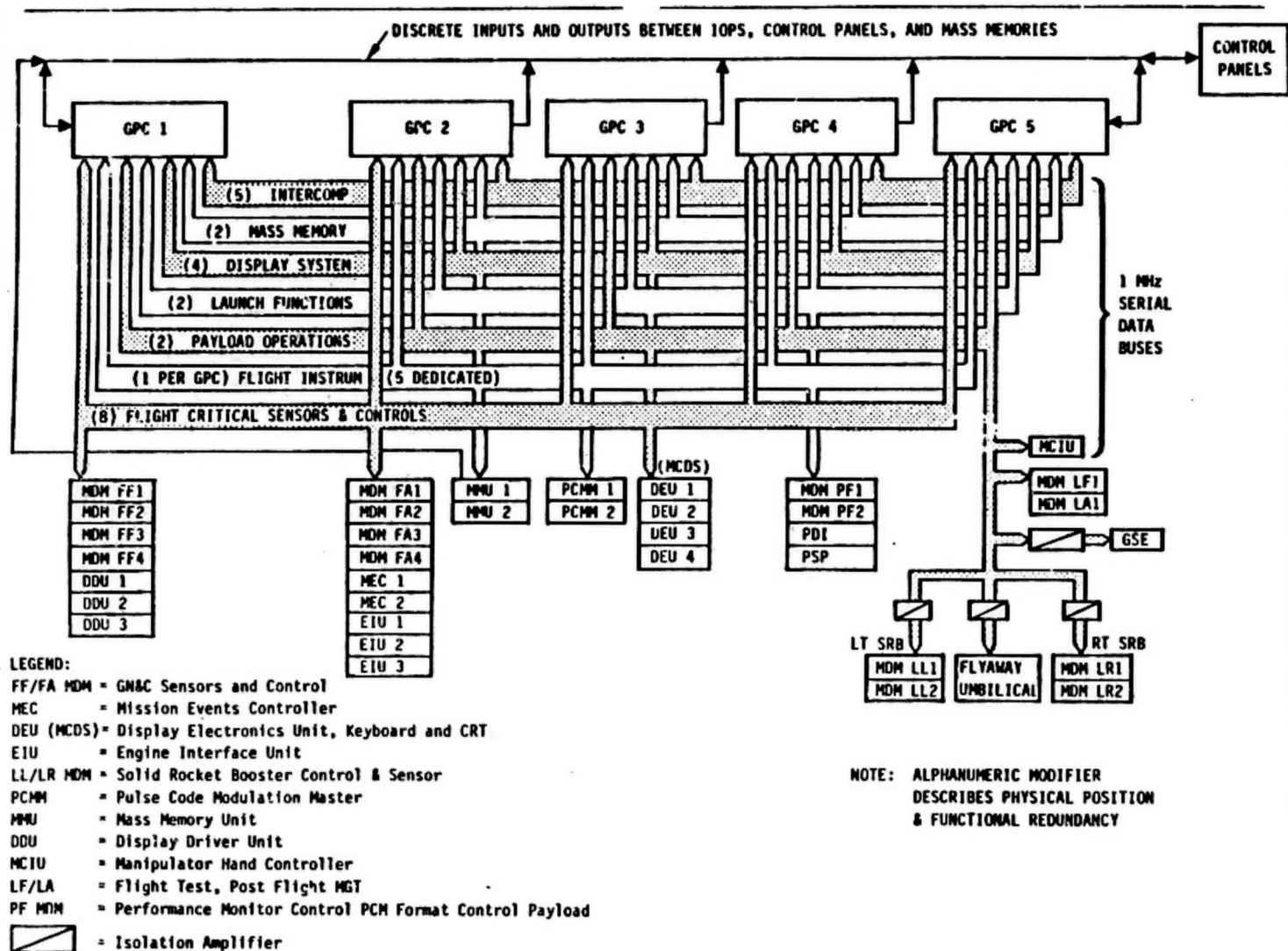
Replace Figure 2 with the enclosed figure

Page 13, Table I

| | | |
|------|-------------------|------------------|
| WAS: | GPC J2 Pin No. | Signal Name |
| | 1 2 | Spare Spare |
| IS: | GPC J2 Pin No. | Signal Name |
| | 1 2 | -L AD POR GND |

Page 15, Table I

| | | | |
|------|-------------------|----------------|--------------------------|
| WAS: | GPC J3 Pin No. | Signal Name | Function |
| | 86 87 | Spare Spare | Spare 3C Space 3T |
| IS: | GPC J3 Pin No. | Signal Name | Function |
| | 86 87 | | Overtemp 1 Overtemp 2 |



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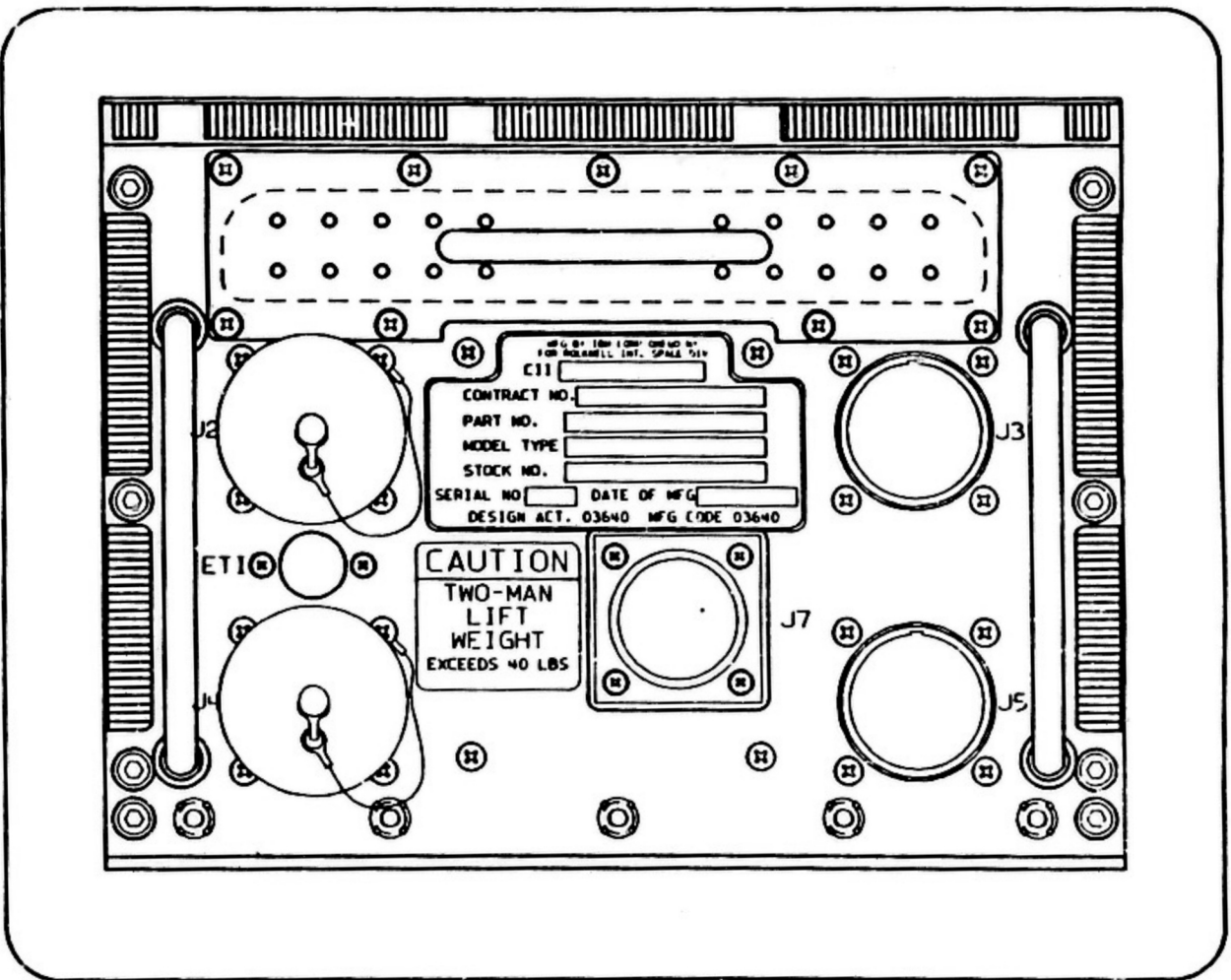


Figure 4. General Purpose Computer Connector Configuration

CODE IDENT. NO. 03953

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WAS:

| GPC J3 Pin No. | Signal Name | Function |
|-------------------|----------------|-----------------|
| 107 | D134C | Discrete in 34T |

IS:

| GPC J3 Pin No. | Signal Name | Function |
|-------------------|----------------|-----------------|
| 107 | D134C | Discrete in 34C |

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| GPC J4 Pin No. | Signal Name |
|-------------------|---|
| 9 | WAS: J1-001 IS: J4-001 |
| 12 | WAS: J1-004 IS: J4-004 |
| 14 | WAS: J1-005 IS: J4-005 |
| 22 | WAS: J1-030 IS: J4-030 |
| 26 | WAS: J1-015 IS: J4-015 |
| 29 | WAS: J1-018 IS: J4-018 |
| 31 | WAS: -L AGE EA store project latched (Softwire) IS: -L AGE read store protect (Softwire) |
| 35 | WAS: J1-023 IS: J4-023 |
| 49 | WAS: J1-036 IS: J4-036 |
| 52 | WAS: J1-039 IS: J4-039 |
| 54 | WAS: J1-041 IS: J4-041 |
| 56 | WAS: J1-044 IS: J4-044 |
| 58 | WAS: J1-047 IS: J4-047 |
| 60 | WAS: J1-059 IS: J4-059 |
| 62 | WAS: J1-061 IS: J4-061 |
| 72 | WAS: J1-071 IS: J4-071 |

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| | | | | | | | |
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Page 17 (Cont)

| GPC J4 Pin No. | Signal Name |
|-------------------|---------------------------|
| 74 | WAS: J1-073 IS: J4-073 |
| 76 | WAS: J1-063 IS: J4-063 |
| 79 | WAS: J1-066 IS: J4-066 |
| 81 | WAS: J1-068 IS: J4-068 |
| 83 | WAS: J1-082 IS: J4-082 |
| 85 | WAS: J1-084 IS: J4-084 |
| 87 | WAS: J1-086 IS: J4-086 |

Page 18

| GPC J4 Pin No. | Signal Name |
|-------------------|---|
| 89 | WAS: J1-088 IS: J4-088 |
| 90 | WAS: +L AGE IS: -L AGE |
| 91 | WAS: J1-090 IS: J4-090 |
| 93 | WAS: J1-092 IS: J4-092 |
| 95 | WAS: J1-094 IS: J4-094 |
| 97 | WAS: J1-096 IS: J4-096 |
| 99 | WAS: J1-098 IS: J4-098 |
| 101 | WAS: J1-100 IS: J4-100 |
| 103 | WAS: Return for J1-102 (Software from B08) IS: Return for J4-102 |
| ADD: 104 | SPARE |
| 106 | WAS: Return for J1-105 (Software from B12) IS: Return for J4-105 |
| 108 | WAS: Return for J1-107 (Software from B16) IS: Return for J4-107 |

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| | | | | | | | | |
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Page 35, Table IIA, under "Function"

Line 16

WAS: ADOR
IS: ADDR

Line 18

DELETE: "(Do not clear code parity)"

Line 22

WAS: Read EOAC ADOR REG 00-13
IS: Read EDAC ADDR REG 00-15

Line 25

WAS: BSR/OSR
IS: BSR/DSR

Line 29

WAS: Hoop
IS: Loop

Line 30

WAS: BSV/OSV
IS: BSV/DSV

Line 31:

WAS: Read MFER and clear code parity error
IS: Read and clear MFER

Page 46

Replace Table III with new Table III enclosed.

Page 47, Line 14

WAS: Work
IS: Word

Page 48, Line 8

WAS: Pass ing
IS: Passing

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Table III. Interrupt Structure and Priorities

| Interrupt Priority | Class | Old PSM | New PSM | Not Maskable | PSW Mask Bit | Pending | Int. Code | Interrupt Accept Time | CPU/IOP/AGE Generated | Interrupt |
|--------------------|-------|----------------------|---------|-------------------|--------------|---------|-----------|-----------------------|-----------------------|---|
| 00 | POWER | 0010 | -- | X | -- | -- | N/A | ENDOP | CPU | Power Off ^{****} (Microcode Put Away) |
| 01 | POWER | -- | 0004 | 2 nd | -- | -- | N/A | MCYCLE | CPU | Power On |
| 02 | POWER | -- | 0014 | 2 nd | -- | -- | N/A | MCYCLE | CPU | System Reset |
| 03 | POWER | -- | -- | -- | -- | -- | N/A | -- | -- | N/A to Shuttle ISA |
| 04 | NC | 0040 ^{****} | 0044 | -- | 45 | No | 0008 | MCYCLE | CPU | EA Fault |
| 05 | NC | 0040 | 0044 | -- | 45 | No | 0005 | MCYCLE | CP1 | CPU Microstore Parity |
| 06 | NC | 0040 | 0044 | -- | 45 | No | 0006 | ENDOP | CPU | Interrupt Page Fault |
| 07 | NC | 0040 | 0044 | -- | 45 | No | 0002 | Forced ENDOP | IOP | DMA Memory Multi-bit Error |
| 10 | NC | 0040 ^{****} | 0044 | X | -- | -- | 0001 | Forced ENDOP | CPU | CPU Memory Multi-bit Error |
| 11 | NC | -- | -- | -- | -- | -- | 0004 | MCYCLE | CPU | Spare |
| 12 | NC | 0040 ^{****} | 0044 | X | -- | -- | 0007 | MCYCLE | CPU | ENDOP Timeout |
| 13 | NC | -- | -- | -- | -- | -- | -- | -- | -- | Spare |
| 14 | NC | 0040 ^{****} | 0044 | X | -- | No | 0009 | MCYCLE | CPU | CPU Cannot Continue |
| 15 | NC | -- | -- | -- | -- | -- | -- | -- | -- | Reserved |
| 16 | NC | -- | -- | X | -- | -- | -- | ENDOP | AGE | AGE Breakpoint (Teaser Service) |
| 30 | NC | -- | -- | -- | -- | -- | -- | -- | -- | N/A to Shuttle ISA |
| 36 | NC | -- | -- | -- | -- | -- | -- | -- | -- | IU Memory Error ^{*****} |
| 37 | NC | -- | -- | -- | -- | -- | -- | -- | -- | EU Memory Error ^{*****} |
| 17 | PE | 0070 | 0074 | -- | 36 | No | N/A | ENDOP | CPU | CPU Breakpoint (Instruction Monitor) |
| 20 | PE | 0048 | 004C | -- | 20 | Note 1 | 0004 | ENDOP | CPU | Fixed Point Overflow |
| 21 | PE | 0048 | 004C | X | -- | No | 0008 | Forced ENDOP | CPU | Floating Point Overflow (Exponent) |
| 22 | PE | 0048 | 004C | -- | 22 | No | 0009 | Forced ENDOP | CPU | Floating Point Underflow |
| 23 | PE | -- | -- | -- | -- | -- | -- | -- | -- | Spare |
| C1 | PE | 0048 | 004C | X | -- | No | 0000 | MCYCLE | CPU | Illegal Instruction |
| C2 | PE | 0048 | 004C | X ^{****} | -- | No | 0001 | -- | CPU | Privileged Instruction (Maskable Only in Problem State, PSM 47=1) |
| C3 | PE | 0048 | 004C | X | -- | No | 000C | Forced ENDOP | CPU | Divided by Zero (Flt. Pt.) |
| C4 | PE | 0048 | 004C | -- | 23 | No | 0005 | Forced ENDOP | CPU | Significance |
| C5 | PE | 0048 | 004C | X | -- | No | 000A | ENDOP | CPU | Convert Overflow |
| C6 | PE | 0048 | 004C | X | -- | No | 0003 | Forced ENDOP | CPU | Spare |
| P0 | SC | 0058 | 005C | X | -- | No | (Inst) | ENDOP | CPU | Supervisor Call |
| 31 | PE | -- | -- | -- | -- | -- | -- | -- | -- | Spare |
| 32 | PE | -- | -- | -- | -- | -- | -- | -- | -- | N/A to Shuttle ISA |
| 33 | PE | 0048 | 004C | -- | -- | -- | 0007 | Forced ENDOP | CPU | Store Protect Violation |
| 34 | PE | -- | -- | -- | -- | -- | -- | -- | CPU | Interrupt Page Fault |
| 35 | PE | -- | -- | -- | -- | -- | -- | -- | -- | N/A to Shuttle ISA |
| 40-43 | SYS | -- | -- | -- | -- | -- | -- | -- | -- | N/A to Shuttle ISA |
| 44 | SYS | -- | -- | -- | -- | -- | -- | -- | -- | Spare |
| 45 | SYS | 0060 | 0064 | -- | 32 | Yes | -- | ENDOP | CPU | Interval Timer No. 1 |
| 46 | SYS | 0068 | 006C | -- | 33 | Yes | -- | ENDOP | CPU | Interval Timer No. 2 |
| 47 | SYS | -- | -- | -- | -- | -- | -- | -- | -- | N/A to Shuttle ISA |
| 50 | SYS | 0078 | 007C | -- | 35 | Yes | 0004 | ENDOP | IOP | External 0 (IOP Voter, IOP Reg. A) |
| 50 | SYS | 0078 | 007C | -- | 35 | Yes | 0004 | ENDOP | IOP | External 0 (C/N Idle, IOP Reg. A) |
| 50 | SYS | 0078 | 007C | -- | 35 | Yes | 0004 | ENDOP | IOP | External 0 (IOP BUS Parity, IOP Reg. A) |
| 50 | SYS | 0078 | 007C | -- | 35 | Yes | 0004 | ENDOP | IOP | External 0 (IOP Fault, IOP Reg. A) |
| 50 | SYS | 0078 | 007C | -- | 35 | Yes | 0004 | ENDOP | IOP | External 0 (Watchdog Timer, IOP Reg. A) |
| 51 | SYS | 0080 | 0084 | -- | 36 | Yes | 0000 | ENDOP | IOP | PCI/PCO Channel Parity Error (IOP Reg. B) - GB Only |
| 51 | SYS | 0080 | 0084 | -- | 36 | Yes | 0000 | ENDOP | IOP | DMA Instruction Read Parity Error (IOP Reg. B), GB Only |
| 51 | SYS | 0080 | 0084 | -- | 36 | Yes | 0000 | ENDOP | IOP | DMA Data Read Parity Error (IOP Reg. B), GB Only |
| 51 | SYS | 0080 | 0084 | -- | 36 | Yes | 0000 | ENDOP | IOP | Bad DMA Word Count Excess (IOP Reg. B), GB Only |
| 51 | SYS | 0080 | 0084 | -- | 36 | Yes | 0000 | ENDOP | IOP | Q Overflow (IOP Reg. B) |
| 51 | SYS | 0080 | 0084 | -- | 36 | Yes | 0000 | ENDOP | IOP | DMA Timeout (IOP Reg. B) |
| 51 | SYS | 0080 | 0084 | -- | 36 | Yes | 0000 | ENDOP | IOP | DMA Store Protect Violation (IOP Reg. B) |
| 52 | SYS | 0088 | 008C | -- | 37 | Yes | -- | ENDOP | IOP | IOP Programmed Interrupts (1-12) |
| 53 | SYS | 0090 | 0094 | -- | 38 | Yes | -- | ENDOP | IOP | Spare External 1 |
| 54 | SYS | 0098 | 009C | -- | 39 | Yes | -- | ENDOP | IOP | Spare External 4 |
| 55 | SYS | -- | -- | -- | -- | -- | -- | -- | CPU | Spare |
| 56 | SYS | -- | -- | -- | -- | -- | -- | -- | CPU | Spare |
| 57 | SYS | 0080 | 0084 | -- | 36 | Yes | 0008 | ENDOP | AGE | Shuttle AGE Interrupt |

* CPU must not be in the halt mode
 ** CPU must be in halt mode
 *** PSM can vary, maybe updated
 **** PC or unupdated PC
 ***** Only occurs when in problem state
 ***** Valid only during execution of Eragnis instruction
 ***** If power off during long instruction, IC may be backed up
 (INST) Code comes from SVC instruction

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Page 49

Line 30

WAS: A program

IS: an

Line 32

WAS: Loading

IS: IPL

Page 52, b.

WAS: IOpte registers

IS: IOP registers

Page 60, Paragraph 3.2.1.5.4.1.2, c.

Delete entire sentence

Page 61, Line 11

WAS: instructions

IS: instruction

Page 90, Line 13

WAS: instruction is executed.

IS: instruction is executed or the BCE detects an error condition.

CHANGE: "d" to "c"

Page 91, Line 31

Delete entire sentence.

Page 92, Line 5

Delete entire sentence.

Page 93

Line 3

WAS: 0 bit position

IS: appropriate bit position

Line 9

WAS: instruction or invalid instructions are encountered

IS: instruction, invalid instruction, or BCE detected error is encountered

Paragraph 3.2.1.5.5.8 BCE Instructions

Delete 4th sentence.

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Page 18 (Cont)

| GPC J4 Pin No. | Signal Name |
|-------------------|---|
| 109 | WAS: AGE PS Test -5V IS: AGE PS Test +5V DC Memory |
| 111 | WAS: AGE PS Test +5VDC IS: AGE PS Test +5VDC CPU |
| 112 | WAS: AGE PS Test +12V IS: AGE PS Test +12VDC |
| 113 | WAS: AGE PS Test +8V IS: AGE PS Test -12 VDC |
| ADD: 114 | BATTERY 1 AGE |
| 115 | BATTERY 2 AGE |
| 116 | RETURN FOR J4-114, 115 |
| 117 | SPARE |
| 118 | SPARE |
| 119 | SPARE |
| 120 | SPARE |
| 121 | SPARE |
| 122 | SPARE |
| 123 | SPARE |
| 124 | SPARE |
| 125 | SPARE |
| 126 | SPARE |
| 127 | SPARE |
| 128 | SPARE |

Page 25

Paragraph 3.1.3

WAS: Seller
Part Number
6966000-2

IS: Seller
Part Number
6966000-3

Paragraph 3.2.1.1

WAS: Life Requirements. The GPC, excluding battery pack, shall be designed to provide the most cost effective life capability, considering minimum maintenance and refurbishment as well as state-of-the-art hardware design. Battery life is defined in Paragraph 3.1.2.1.11.

IS: Life Requirements. The GPC shall be designed to provide the most cost effective life capability, considering minimum maintenance as well as state-of-the-art hardware design.

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Page 98

BIT
23

WAS: - XMT
IS: XMT/MIA BUSY

Add after last word of sentence: or MIA busy.

Page 99

BIT
28

WAS: . . . instruction of an odd . . .
IS: . . . instruction on an ODD . . .

Page 101

Instruction

Description

1

Line 5

DELETE and ADD: enters the wait state.

Delete the last sentence.

Page 103

Instruction

Description

5

The fourth sentence should be changed to read: The BCE is reset to the busy state by the MSC.

Page 106

Instruction

Description

13

4- WAS: and begin executing the next instruction

IS: and enters the wait state

Page 107

Instruction

Description

13

Line 18

WAS: S=1

IS: SE=1

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| | | | | | | | |
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Page 108

Instruction

13

Description

Third sentence

CHANGE TO READ: If a timeout occurs, Bit 26 of the BCE status register is set, and the BCE goes to the wait state.

Page 110

Instruction

15

Description

Third paragraph

WAS: and the next instruction initiated.
IS: and the BCE goes to the wait state.

Page 123, Paragraph 3.2.1.7.1.1

WAS: mission word error

IS: missing word error

Page 124

Paragraph 3.2.1.7.1.2, Line 4

WAS: (status Bit 1)

IS: (Status Reg 1)

Paragraph 3.2.1.7.1.3, Line 3

WAS: (Status BIT 1)

IS: (Status REG 1)

Paragraph 3.2.1.7.1.5, Line 3

WAS: (status Bit 1)

IS: (Status Reg 1)

Paragraph 3.2.1.7.2.1

CHANGE TO READ: When the interword gap time exceeds six microseconds, the BCE shall set the NO-GO BIT (Status REG BIT 1) and BIT 21 in the BCE status register. The transmit data instruction shall be terminated, and the BCE shall enter the wait state.

Paragraph 3.2.1.7.2.2, Line 2

After "transmitter," add "or if MIA busy,"

Paragraph 3.2.1.7.3.1, second sentence

CHANGE TO READ: The MSC or BCE shall set the NO-GO BIT (Status REG 1) and, if an MSC detected error, the MSC shall set the I BIT (BIT 15) in the MSC status register.

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Page 125, Table XVI

ACTION

Line 14: After "6, or 7" add "(as appropriate)"

Line 22: After "STATUS BIT" add 15

Paragraph 3.2.1.7.3.2.1, Line 4

WAS: issue an interrupt

IS: issue a machine check interrupt

Paragraph 3.2.1.7.3.2.2, Line 4

WAS: issue an interrupt

IS: issue a machine check interrupt

Page 126, Table XVII

ACTION

Line 2

WAS: 29

IS: 15

Line 5

WAS: 28

IS: 14

Line 7

WAS: 25

IS: 11

Line 8

WAS: 26

IS: 12

Line 9

WAS: 27

IS: 13

Page 127, Paragraph 3.2.1.7.3.6

BIT 28 (2 places) should be BIT 14

Page 128, Paragraph 3.2.1.7.4, Line 2

WAS: 32

IS: 18

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Page 132

DELETE: "3.2.1.11.15 TBD."

Paragraph 3.2.1.12

CHANGE TO READ: When the GPC is installed in the avionic system the method of loading the program is mass memory read.

Page 135

Replace Figure 12, Sheet 1 with new Figure 12 enclosed.

PAGE 137, Figure 12, Sheet 3

ADD: missing dimension line and arrow to the 0.875 dimension.

Page 138, Paragraph 3.2.4.2.1 a.

WAS: oted
IS: noted

Page 139, Paragraph 3.2.4.2.2 a.

Delete last sentence.

Page 142, h. Shock

Under the applications column the last number

WAS: 4
IS: 1

Page 154, c.

WAS: control processing unit (CPU)
IS: central processing unit (CPU)

Page 156, Paragraph 4.2.4.1.1 Test Hardware

WAS: Qualification test hardware shall be of the same configuration as the flight hardware.

IS: A pre-production configuration GPC (P/N MC 615-0025-3000) shall be used for qualification test.

Page 157, Paragraph 4.2.4.1.6 Power Tests

Delete "and the power consumption requirements of 3.3.3.2.1" from the sentence.

Page 183

Delete lines 10 through 21.

| | |
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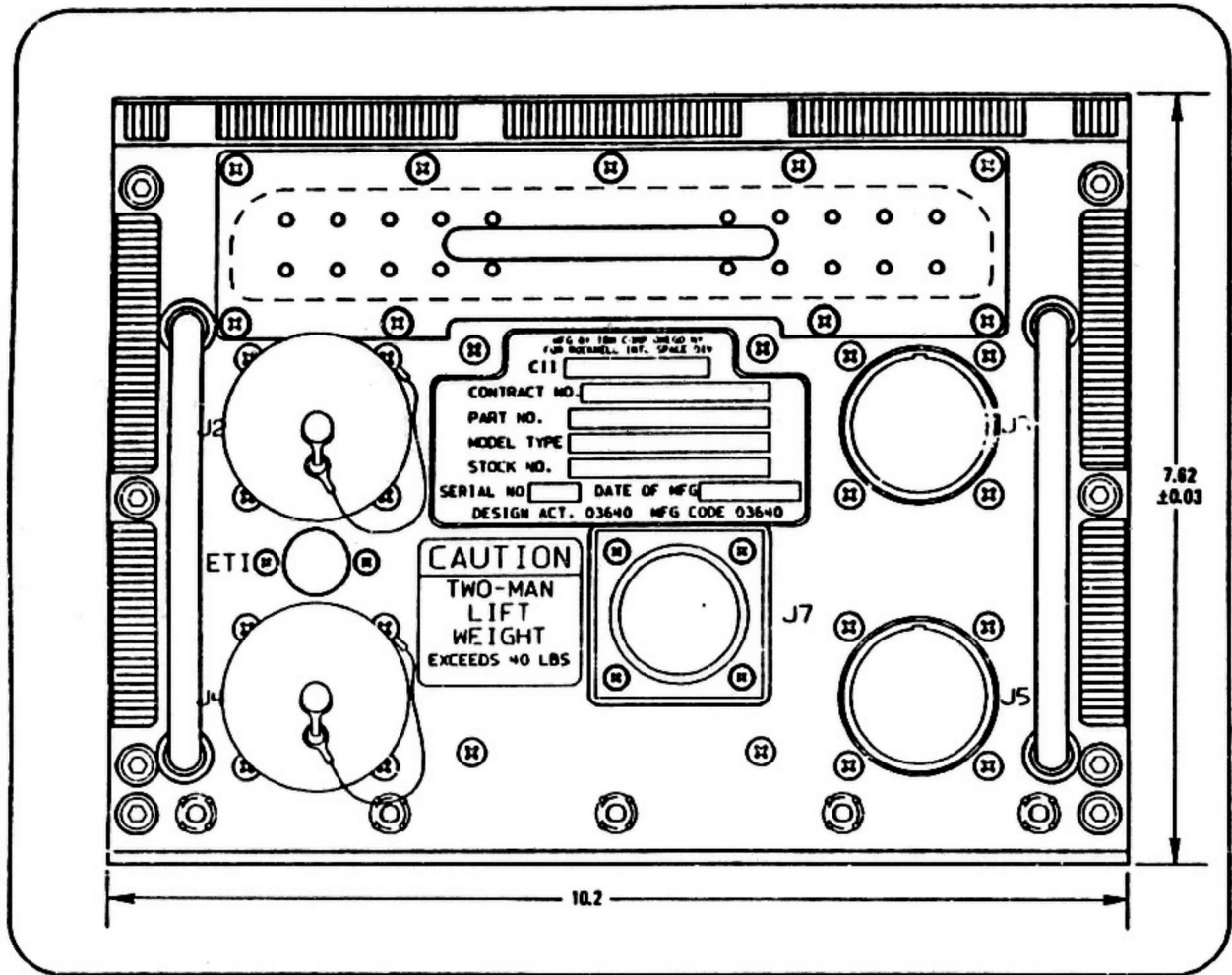




Figure 12. General Purpose Computer Configuration
(Sheet 1 of 3)

| | | | | | |
|---|--|-------------------|-------------------------------|---|-----------|
| PREPARED BY G.F. McMullen FB14 D/292-440 X5237 | CODE IDENT. NO. 03953 ⁶³ | | DOCUMENT NUMBER MC615-0025 | REV A | SEQ 02 |
| |  Rockwell International | | DOCUMENT TYPE PROCUREMENT | | |
| | AMENDMENT COMPUTER GENERAL PURPOSE ORBITER | | AUTHORITY G.O. 40977 | | |
| | APPROVALS <i>[Signatures]</i> 10/14/85 10-14-85 10-17-85 | | DATE 07/24/85 | PAGE OF | 1 14 |
| | | SUBJECT CHANGE | |  | |

This amendment forms a part of MC615-0025, new dated September 19, 1984

Page V.

- add: 12. Appendix III Battery Backup Unit (Production configuration)
- 13. Appendix IV Battery Backup Unit (Pre-Production Configuration)
- 14. Appendix V Battery Backup Unit (Prototype Configuration)

Page 3

add: MIL-STD-202F Test Methods for electronic and electrical component parts
 April 1980

Page 141

3.2.5.1 b.

was: b. Pressure Minimum: 12.3 psia, continuous,
 8 psia for 2 hours

Maximum: 18.0 psia

is: b. Pressure (1) Minimum: 12.3 psia, continuous,
 8 psia for 2 hours

Maximum: 18.0 psia

(2)

10.2 psia in a 35% oxygen environment
 for 165 hours

OFFICIALLY
 RELEASED
 1985 OCT 28 AM 10:55

Page 142

add: i. Lightning In accordance with Paragraph 4.2.4.1.7

ABV 304

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SEQ

PAGE

Page 156

Table XX

Change to read:

| Test | Paragraph |
|-----------------------|------------|
| Acceptance Test (REF) | 4.2.2 |
| Power Test | 4.2.4.1.6 |
| Lightning | 4.2.4.1.7 |
| EMC | 4.2.4.1.8 |
| Cabin Atmosphere | 4.2.4.1.12 |
| Thermal Cycle | 4.2.4.1.10 |
| Vibration | 4.2.4.1.3 |
| Acceleration | 4.2.4.1.4 |
| Thermal-Vacuum | 4.2.4.1.9 |
| Life | 4.2.4.1.11 |
| Shock | 4.2.4.1.5 |

Page 157

4.2.4.1.7

was: Deleted

is: Lightning

The GPC shall be designed to withstand a lightning pulse voltage transient without sustaining damage, malfunction, or upset. The test waveform shall have a 0.6 ± 0.3 microsecond risetime and a pulse width of at least 10 microseconds. The test signal peak amplitudes, with respect to a zero current or voltage baseline, are specified in paragraphs 4.2.4.1.7.1, 4.2.4.1.7.2, 4.2.4.1.7.3, and 4.2.4.1.7.4. When both voltage and current transient peaks are specified, whichever is encountered first, when increasing the threat level, satisfies the requirement.

4.2.4.1.7.1

Receiver Circuits

The Receiver circuits shall be designed to perform without damage, malfunction or upset when +27 volts or +2.2 milliamps and -14 volts or -4.2 milliamps is applied as a common mode transient from pin to chassis.

| | | | |
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4.2.4.1.7.2

Driver Circuits

the Driver circuits shall be designed to perform without damage, malfunction or upset when +17 volts or +10 milliamps and -0.2 volts or -30 milliamps is applied as a common mode transient from pin to chassis in either output operating state.

4.2.4.1.7.3

28 VDC Power Circuits

The 28 VDC power circuits shall be designed to perform without damage, malfunction or upset when +91 volts or +10 amps and -18 volts or -6 amps is applied as a common mode transient from pin to chassis.

4.2.4.1.7.4

Data Bus Circuits

The data bus interfaces shall be designed to perform without damage, malfunction or upset when ± 18 volts is applied in common mode from transients to common ground (logic, chassis, power).

Page 160

Add:

4.2.4.2.13

Pressure

Compliance with the pressure requirements of 3.2.5.1b(2) shall be verified by analysis of design and engineering data.

Page 25

Paragraph 3.1.3

Was: Seller
Part Number

6966000-3

Is: Seller
Part Number

6966000-20

| | | | |
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Page 177

Change to read as follows:

| Section 3 and 5 Requirement No. | Verification Method | | | | | | | | | | | Section 4 Requirement No. | | | |
|------------------------------------|---------------------|---|---|---|---|---|---|---|---|---|---|------------------------------|---|--|--------------------------|
| | N/A | 1 | 2 | | 3 | | | | | | | | | | |
| | | | a | b | a | b | c | d | e | f | g | | h | | |
| 3.2.4.2.5 | | | X | X | | | | | | | | | | | 4.2.2.2.1, 4.2.3 |
| 3.2.4.5.6 | X | | | | | | | | | | | | | | |
| 3.2.4.5.6.1 | | X | | X | | | | | | | | | | | 4.2.4.2, 4.2.3 |
| 3.2.4.3 | X | | | | | | | | | | | | | | |
| 3.2.4.3.1 | | | | X | | | | | | | | | | | 4.2.3 |
| 3.2.4.3.2 | | | | X | | | | | | | | | | | 4.2.3 |
| 3.2.4.3.3 | | | | X | | | | | | | | | | | 4.2.3 |
| 3.2.5 | X | | | | | | | | | | | | | | |
| 3.2.5.1 | X | | | | | | | | | | | | | | |
| 3.2.5.1a | | | | | | X | | | | | | | | | 4.2.4.1.10, 4.2.4.1.2 |
| 3.2.5.1b(1) | | | | | | X | | | | | | | | | 4.2.4.1.9 |
| 3.2.5.1b(2) | | X | | | | | | | | | | | | | 4.2.4.1.2 |
| 3.2.5.1c | | X | | | | X | | | | | | | | | 4.2.4.1.12, 4.2.4.2 |
| 3.2.5.1d | | X | | | | X | | | | | | | | | 4.2.4.2.12, 4.2.4.2 |
| 3.2.5.1f | X | | | | | | | | | | | | | | |
| 3.2.5.1f(1) | | | | | | X | | | | | | | | | 4.2.4.1.3, 4.2.4.1.2 |
| 3.2.5.1f(2) | | | | | | X | | | | | | | | | 4.2.4.1.3, 4.2.4.1.2 |
| 3.2.5.1g | | X | | | | X | | | | | | | | | 4.2.4.1.4, 4.2.4 |
| 3.2.5.1h(1) | | X | | | | X | | | | | | | | | 4.2.4.1.5B, 4.2.4.2 |
| 3.2.5.1h(2) | | X | | | | X | | | | | | | | | 4.2.4.1.10, |
| 3.2.5.1i | | X | | | | X | | | | | | | | | 4.2.4.1.7, 4.2.4.2 |

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Amendment A-01

Page 9 Table III

Add to bottom of page:

"Note 1: Status held active in PSW 19."

Page 116

Add:

- 3.2.1.5.15 Battery Backup Unit (BBU)
The BBU provides backup power to the GPC memory in order to retain the memory contents in the event of a primary power interruption. For purposes of the GPC design, the BBU is defined in the following paragraphs.
- 3.2.1.5.15.1 Interface Definitions
The electrical interface between the GPC CMOS memory array, the memory power supply and the BBU shall be by a twenty five pin connector. The socket portion of the connector shall be provided on the BBU and the pin portion of the connector shall be provided on the GPC. The functional and physical interface requirements for the BBU are defined in Appendix III.
- 3.2.1.5.15.2 Performance Characteristics
The BBU shall provide the performance characteristics defined in Appendix III.
- 3.2.1.5.15.3 Physical Characteristics
The BBU shall have the physical characteristics defined in Appendix III.

Appendix III

12. Battery Backup Unit (Production Configuration).
- 12.1 Scope
This appendix establishes the performance, design, development, and verification requirements for the Battery Backup Unit (BBU).
- 12.1.1 Classification
The requirements of the basic specification shall apply
- 12.2 Applicable Documents

| | | | |
|-----------------|-----|-----|-------|
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| DOCUMENT NUMBER | REV | SEQ | _____ |

12.2.1 Applicability

The documents listed in section 2 of the basic specification shall apply

12.2.2 Item Identification. The identification of the BBU shall be as follows:

| <u>Nomenclature and Mfr Code Ident No.</u> | <u>Seller Part No.</u> | <u>Traceability Classification</u> |
|---|----------------------------|--|
| Battery Rechargeable: 3.6 volts Nickel-Cadmium | 6966081-20 | Serial |

12.3 Requirements

The requirements of Section 3 of the basic specification shall apply unless otherwise specified herein.

12.3.1 Materials

The materials utilized in the manufacturing of the BBU shall provide protection against corrosion. Materials, including the contents of the device or its marking, shall not liberate or generate toxic or corrosive fumes in the specified environments. The BBU package shall be made from materials which are protected from corrosive chemicals such as the electrolyte of Nickel Cadmium batteries.

12.3.2 Finish

The BBU shall employ a finish which protects against electrolytic corrosion between the BBU and the structure. The structure material is 6061-T6 Aluminum alloy with chemical film MIL-C-5541 Class 3.

12.3.3 Batteries

The BBU shall use Ni-Cad batteries

12.4 Design and Construction1.2.4.1 Configuration

The overall dimensions and mounting provisions shall be as shown in Figure 1.

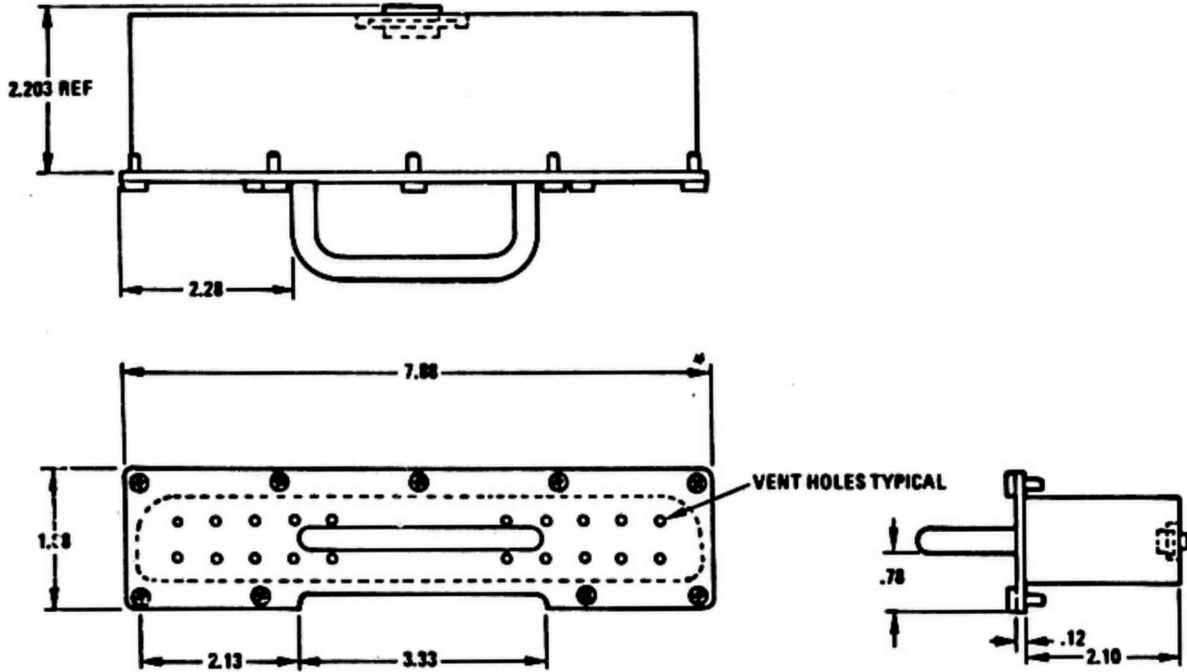


Figure 1. Battery Backup Unit

| | |
|-----------------|------------|
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- 12.5 Maintainability
The battery module shall be designed to meet all performance requirements specified herein. This device shall be repairable. Depleted/defective cells or current protective components shall be replaceable.
- 12.6 Thermal
The BBU shall be designed for natural cooling (i.e. free convection and radiation) to a still air temperature environment defined in 12.9.1. All external surfaces of the item excluding the front panel shall be finished to enhance radiation cooling. The surface(s) shown in Figure 1 shall provide adequate conduction cooling of the item to meet the environmental conditions of 12.9. The item shall be constructed so that any output pin may be shorted to ground without stressing the battery unit components.
- 12.7 Performance requirements
The battery module shall operate per the performance requirements throughout the environmental conditions indicated in section 12.8 and 12.9 of this specification. Development testing shall be performed at temperatures as defined in paragraph 12.9.1 and Qualification testing shall be conducted with the conditions as specified in Section 12.9. Prior to acceptance, each unit shall be tested for the electrical characteristics defined in the Applicable functional test specifications.
- 12.7.1 Battery module interface characteristics.
The BBU interface described herein provides an interface between the battery and the CMOS memory array, and the memory power supply. The BBU interface is defined in Table I.
- 12.7.1.1 Interface Requirements
The interface connector pin assignments are shown in Table I.

| | | | |
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|-------------------------------|----------|-----------|-------------|

Table I**Battery Backup Unit Interface**

| <u>Pin No.</u> | <u>Signal Name</u> | <u>Pin No.</u> | <u>Signal Name</u> |
|----------------|----------------------|----------------|------------------------|
| 1 | WRAPA2 (1) (BATTERY) | 14 | |
| 2 | WRAPA1 (1) | 15 | TS1 TEST POINT |
| 3 | BP VBATT (A) | 16 | |
| 4 | | 17 | RETURN |
| 5 | SAFETY GROUND (3) | 18 | RETURN |
| 6 | RETURN | 19 | +10 BATTERY CHARGE 2 |
| 7 | | 20 | +10 BATTERY CHARGE 1 |
| 8 | MEMORY +5VDC (A) | 21 | MEMORY +5VDC (B) |
| 9 | +L BATTERY 1 GO | 22 | +L CHARGER 1 GO |
| 10 | BATTERY 1 AGE | 23 | BATTERY 2 AGE |
| 11 | BP VBATT (B) | 24 | TS2 TEST POINT |
| 12 | WRAPB1 (2) | 25 | WRAPB2 (2) (BATTERY 2) |
| 13 | | | |

NOTES:

- (1) TIE POINTS TOGETHER EXTERNAL TO CONNECTOR FOR TEST PURPOSES ONLY
- (2) TIE POINTS TOGETHER EXTERNAL TO CONNECTOR FOR TEST PURPOSES ONLY
- (3) PIN 5 AND PINS (6, 17 AND 18) MUST BE ELECTRICALLY ISOLATED IN THE BATTERY BACKUP UNIT.
- (4) PIN 6, 17, 18 ARE NOT TIED INTERNAL TO THE BATTERY BACKUP UNIT.
- (5) CONNECTOR PART NO. 102A622-1 (BBU), 102A599-1 (GPC)

12.8 Acceptance

Acceptance tests and inspections shall be performed on all BBU's to be employed in qualification test programs and on all BBU's delivered to the buyer. These acceptance tests and inspections shall be performed to demonstrate that specified requirements have been met. Final acceptance tests and inspections shall be performed in a manner, and under conditions, which simulate end-use to the highest degree practicable without damage to the BBU.

12.8.1 Examination of Product

Each BBU shall be carefully examined to determine conformance to the requirements of this specification. Particular attention shall be given to weight, workmanship, finish, dimensions, construction, cleanliness, identification, marking traceability level, and that certified materials and processes have been used.

12.8.2 Functional and Performance Tests

Functional and performance tests shall be conducted on all deliverable equipment to establish compliance with the requirements of the suppliers Factory Acceptance Test (FAT) and Customer Acceptance Test (CAT). Tolerance bands or pass fail performance criteria, based on performance design requirements, shall be established for each parameter.

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12.8.3 Thermal Cycle (Non-Operational)

Each BBU shall be subjected to ten thermal cycles. Each cycle shall consist of a thermal transition from -40°F to +150°F. Stabilization at each temperature shall be 30 minutes. The thermal transition time between each temperature extreme shall not exceed 5 minutes. The BBU shall not be electrically operated during this test.

12.8.4 Acceptance Vibration

The BBU shall be subjected to random vibration in each of the three orthogonal axes. The vibration testing shall be conducted in accordance with MIL-STD-202F, Method 214, Test condition IG. The vibration duration shall be no less than 30 seconds per axis. The total accumulative vibration time in any axis shall not exceed 5 minutes without prior buyer approval. The functional characteristics of the BBU shall be monitored throughout the test.

12.8.5 Acceptance Thermal

The thermal profile shall be as specified in 4.2.2.4 of the basic specification. The functional characteristic of the BBU shall be monitored throughout the test.

12.9 Qualification Test

The BBU shall meet the performance requirements during and after any combination of testing as defined in paragraphs 12.9.1 through 12.9.7. Prior to the Qualification tests specified in paragraphs 12.9.1 through 12.9.7, the operation of the BBU shall be verified per the applicable functional test specification. If the BBU is not operated during a specified environmental test, the functional test will be conducted at the conclusion of the specified environment.

12.9.1 Temperature

The operating temperature range of the BBU shall be as follows:

Charging: +35°F to +130°F

Discharging: 0°F to + 120°F (1)

Storage: -40°F to +120°F (1)

(1) Transients to +150°F for 6 hours per day

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12.9.2 Vibration

The BBU SHALL be designed to operate during a Random Vibration test per MIL-STD-202F, Method 214. Test condition "IG" for a duration of 15 minutes. The BBU shall be mounted using the mounting provisions provided in figure 1 with the vibration fixture mating connector held rigidly.

12.9.3 Shock

The BBU shall be designed to operate during the shock pulses per MIL-STD-202F, Method 213, Test Condition "A" (50g's, 11 MS, half sine). The BBU shall be mounted using the mounting provisions provided in figure 1 with the fixture mating connector held rigidly.

12.9.4 Pressure

The BBU shall be designed to operate during and after exposure to the following pressure conditions:

Operational

1. Minimum: 12.3 psia continuous
or 8 psia for 2 hours

Maximum: 18 psia.

2. 10.2 psia, at 35% O₂ for 165 hours.

Nonoperational

1. Minimum: 3.28 psia

Maximum: 30.0 psia

12.9.5 Moisture Resistance

The BBU shall be designed to operate with full specified performance when subjected to the tests described by MIL-STD-202F, Method 106E except that no vibration shall be employed.

12.9.6 Fungus

The BBU shall be designed to operate with full specified performance when subjected to the fungus growth test described by MIL-STD-810C, Method 508.1.

12.9.7 Salt Atmosphere

The BBU shall be designed to operate with full specified performance when subjected to the salt spray environment described by MIL-STD-202F, Method 101D, Test Condition "B" (48 hours exposure).

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PAGE

12.10

Marking

Items shall be permanently and legibly marked in accordance with MIL-STD-202 Method 215. The following shall be included.

- A. Supplier identification number
- B. IBM part number

Serial numbers shall be consecutive from 1 without redundant numbering.

- C. Battery rechargeable: 3.6 volts
Nickel-Cadmium (Front of Unit)
- D. Date code of Battery Mfg. (Year-Week) (Front of Unit)
- E. Warning Label as required. Place Warning on front of Battery Module to be visible when Module is plugged into box.

APPENDIX IV

13. Battery Back up Unit (Pre-Production Configuration)

13.1 Scope

This appendix establishes the design and performance requirements for the pre-production configuration of the BBU. The pre-production BBU's are to be restricted to nonflight use.

The pre-production BBU's are to be manufactured utilizing a combination of qualified parts and parts that do not meet the requirements of the quality assurance specification MT802-106, or amendment D-01 of the Electrical, Electronic, and Electromechanical Orbiter Parts List (OPPL), MF0004-400C.

These parts are "equivalent parts" that have not been subjected to the additional requirements imposed by amendment D-01 and MT802-106.

In order to minimize the use of "equivalent parts", qualified parts shall be used whenever possible.

13.1.1 Classification

All requirements of the basic specification shall apply.

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13.2 Applicable Documents**13.2.1** Applicability

The documents listed in Section 2 of the basic specification shall apply.

13.3 Requirements

The requirements of Appendix III shall apply.

13.3.1 Item Identification

The identification of the pre-production BBU shall be as follows:



| <u>Nomenclature and Mfr. Code Ident. No.</u> | <u>Seller Part No.</u> | <u>Traceability Classification</u> |
|---|----------------------------|--|
| Battery Rechargeable: 3.6 volts Nickel-Cadmium | 6966081-1 | Serial |

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DOCUMENT NUMBERA
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PAGE

APPENDIX V

14. Battery Backup Unit (Prototype Configuration)
- 14.1 Scope
This appendix established the design and performance requirements for the prototype configuration of the BBU.
- 14.1.1 Classification
All requirements of the basic specification shall apply.
- 14.2 Applicable Documents
- 14.2.1 Applicability
The documents listed in section 2 of the basic specification shall apply.
- 14.3 Requirements
The requirements of Appendix III shall apply, except as follows:
- a. Deviations in components or process requirements may be granted upon request from the seller.
- 14.3.1 Item Identification
The identification of the prototype model shall be as follows:
- | <u>Nomenclature and Mfr.
Code Ident. No.</u> | <u>Seller
Part No.</u> | <u>Traceability
Classification</u> |
|---|----------------------------|--|
| Battery Rechargeable: 3.6 volts Nickel-cadmium | 6966081-99 | Serial |
- 14.4 Quality Assurance Provisions
The provisions of Section 4 of this specification are waived. The supplier shall submit an acceptance test procedure for the buyer's approval and shall conduct acceptance tests in accordance with the approved procedure.

| | | | |
|---|---|---|---------------|
| PREPARED BY G. F. McMullen D/292-440, FB14, 2593 | CODE IDENT. NO. 03953  Rockwell International AMENDMENT Computer, General Purpose Orbiter  | DOCUMENT NUMBER MC615-0025 | REV B1 A 0 |
| APPROVALS <i>R. C. [Signature]</i> 7/19/86 | | DOCUMENT TYPE Procurement | |
| <i>[Signature]</i> 7/19/86 <i>T. C. [Signature]</i> 7-10-85 | | AUTHORITY G.O. 40977 DATE 7-8-86 | |
| | | SUBJECT Change PAGE 1 OF 1 | |

This amendment forms a part of MC615-0025, New, dated September 19, 1984.

Page 2

WAS: MC999-0096D
 30 August 1974
 Amendment E-01
 22 January 1975
 Amendment E-14
 8 November 1982

IS: MC999-0096D
 Amendment E-01
 through
 Amendment E-14

Page 3

WAS: MF0004-400C
 18 June 1984
 Amendment D-01
 14 December 1984

IS: MF0004-400C
 18 June 1984
 Amendment D-01
 14 December 1984
 Amendment D-02
 17 October 1985

WAS: MT0802-106
 16 December 1984

IS: MT0802-106A
 22 October 1985

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|---|--|
| PREPARED BY G. F. McMullen D/292-440, FBI4, 5237 | |
| APPROVALS <i>[Signature]</i> 6/10/87 <i>[Signature]</i> 6/12/87 <i>T.C. Toyo</i> 6-11-87 | |
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CODE IDENT. NO. 03953

58



Rockwell International

AMENDMENT

COMPUTER, GENERAL PURPOSE
ORBITER

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|-----------------|------|-----|
| DOCUMENT NUMBER | REV | SEQ |
| MC615-0025 | A | 04 |
| DOCUMENT TYPE | | |
| PROCUREMENT | | |
| AUTHORITY | | |
| G.O. 40977 | | |
| DATE | PAGE | |
| 6-3-87 | 1 | |
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| | 2 | |
| SUBJECT | | |
| CHANGE | | |

This amendment forms a part of MC615-0025, New dated September 19, 1984.

Amendment A02 Page 10

12.8.4 Acceptance Vibration

Change to read:

"The BBU shall be designed to satisfy the vibration requirements specified in Paragraph 4.2.2.3 of this specification."

Amendment A02 Page 11

12.9.2 Vibration

Change to read:

The BBU shall be designed to satisfy the vibration requirements specified in Paragraph 4.2.4.1.3 of this specification. The BBU shall be mounted using the mounting provisions provided in Figure 1 with the vibration fixture mating connector held rigidly.

Amendment A01 Page 2

11.1 Scope

Add between the first and second paragraphs:

"The following paragraphs of the basic specification do not apply to the pre-production units.

- 4.1.2.2.1 Random Vibration
- 4.2.2.3 Acceptance Vibration Test
- 4.2.2.4 Acceptance Thermal Test (ATT)"

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MC615-0025

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PAGE 2

DOCUMENT NUMBER

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Page 47

3.2.1.3.9 Clock (Internal Master)

Change to read:

Internal Master Clock Oscillators and associated circuitry shall supply precision timing signals for all logic circuits within the GPC. The absolute accuracy of the oscillators shall not exceed +87 ppm from the nominal oscillator frequency.

The accuracy specification shall be met within 100m sec from the time the master power reset is released for the life duration of the GPC as specified in paragraph 3.2.1.1.


Accuracy is herein defined as the maximum allowable fractional peak frequency offset from the nominal oscillator frequency.

The accuracy specification shall be all inclusive, covering all applicable operational environmental effects, primary power supply variations, power cycling, aging and other applicable variables.

The turn-on time of the oscillators shall not exceed 100 ms from the time the master power reset is released after the application of primary power.

| | |
|---|--|
| PREPARED BY G. F. McMullen D/292-440, FB14, 2-5237 | |
| APPROVALS <i>[Signature]</i> 11/9/87 <i>[Signature]</i> <i>T.K. Togo</i> 11-17-87 | |


CODE IDENT. NO. 03953 53



Rockwell International

AMENDMENT

Computer, General Purpose Orbiter



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|-----------------|------|-----|
| DOCUMENT NUMBER | REV | SEQ |
| MC615-0025 | A | 05 |
| DOCUMENT TYPE | | |
| Procurement | | |
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| DATE | PAGE | OF |
| 11-9-87 | 1 | 1 |
| SUBJECT | | |
| Change | | |

This amendment forms a part of MC615-0025, New, Dated September 19, 1984

Page 193 Appendix II

11.1 Scope


| | | |
|------|-------------------------|--------------------|
| WAS: | <u>Rockwell Part No</u> | <u>IBM Part No</u> |
| | MC615-0025-3000 | 6966000-2 |
| IS: | <u>Rockwell Part No</u> | <u>IBM Part No</u> |
| | MC615-0025-3000 | 6966000-2 |
| | MC615-0025-3001 | 6966000-3 |

GPL Part Number MC615-0025-3001 is the result of a block change consisting of the incorporation of the following EDCP's:

| <u>EDCP#</u> | <u>CHANGE DESCRIPTION</u> |
|--------------|---|
| 87-1015-38 | Corrects GPC IPL delay. |
| 87-1015-39 | Corrects failure of CC page when extended. |
| 87-1015-44 | Corrects EDC disable condition. |
| 87-1015-45 | Corrects bouncing halt and standby discrete inputs. |
| 87-1015-46 | Corrects IOP hang by changing timing/hardware. |
| 87-1015-47 | Reduces execution time of DSE (LXA) instruction. |
| 87-1015-48 | Deletes unwanted additional cycle on all X10's. |
| 87-1015-49 | Changes Microcode to prevent unpredictable GPC response to unsolicited MDM data. |
| 87-1015-50 | Adds tighter tolerance capacitor to correct variance in pre-prod power-off putaway times. |
| 87-1015-51 | Corrects TDx, RDS, RDL, RDLI, MIN & MINL Microcode deficiencies. |
| 87-1015-53 | Adds capacitor to 12 volt converter in order to reduce ripple. |
| 87-1015-54 | Corrects timing race condition on MC page. |

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RELEASE

EDCP # 001757

| | | | | |
|---|---|-------------------------------|------------|-----------|
| PREPARED BY G.F. McMULLEN D/292-440 (FB14) | CODE IDENT. NO. 03953 | DOCUMENT NUMBER MC615-0025 | REV A | SEQ 06 |
| APPROVALS <i>W.D. Haines 6/24/89</i> |  Rockwell International AMENDMENT COMPUTER, GENERAL PURPOSE ORBITER | DOCUMENT TYPE PROCUREMENT | | |
| <i>J.D. Hovey 6/21/89</i> | | AUTHORITY G.O. 40977 | | |
| <i>D.K. F. Hovell 6/24/89</i> | | DATE June 20, 1989 | PAGE OF | 1 2 |
| <i>B. Van Valkenburg 6/23/89</i> | | SUBJECT CHANGE | | |

THIS AMENDMENT FORMS A PART OF MC615-0025, NEW, DATED SEPTEMBER 19, 1984

PAGE 193 APPENDIX II

WAS: ROCKWELL PART NO. IBM PART NO.
MC615-0025-3000 6966000-2

IS: ROCKWELL PART NO. IBM PART NO.
MC615-0025-3000 6966000-2
MC615-0025-3001 6966000-3
MC615-0025-3002 6966000-4
MC615-0025-3003 6966000-5

PAGE 25 PARA. 3.1.3

WAS: BUYER SELLER
CONTROL NO. PART NO.
MC615-0025-0200 6966000-20

IS: BUYER SELLER
CONTROL NO. PART NO.
MC615-0025-0200 6966000-20
MC615-0025-0201 6966000-21

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GPC PART NUMBER MC615-0025-3002 IS A RESULT OF A BLOCK CHANGE CONSISTING OF THE INCORPORATION OF THE FOLLOWING EDCPs:

| <u>EDCP #</u> | <u>CHANGE DESCRIPTION</u> |
|---------------|--|
| 88-101S-058 | CORRECTS TEMPERATURE RELATED PARITY ERRORS |
| 88-101S-059 | CORRECTS THE ERRONEOUS CLEARING OF THE XIO CONTROL REGISTER |
| 88-101S-060 | CORRECTS EDAC ADDRESS FAILURES |
| 88-101S-062 | CORRECTS A POWER DOWN PUTAWAY ANOMALY |
| 88-101S-064 | CORRECTS ANOMALIES THAT OCCUR DURING EXTENDER PAGE TESTING |
| 88-101S-065 | CORRECTS A CONDITION WHEREBY DMA AND QUEUE PARITY ERRORS OCCUR DURING LOW TEMP TESTING |
| 88-101S-066 | BREAKS UP THE CLOCK NET TO CORRECT TIMING FAILURES DURING EXTENDER PAGE TESTING |


EOCN' 026672

GPC PART NUMBERS MC615-0025-3003 AND MC615-0025-0201 ARE THE RESULT OF THE INCORPORATION OF THE FOLLOWING EDGP'S:

| <u>EDCP #</u> | <u>CHANGE DESCRIPTION</u> |
|---------------|--|
| 88-101S-074 | CORRECTS A CONDITION WHEREBY THE GPC DOES NOT GO TO THE "WAIT" STATE UPON RECEIPT OF A MACHINE CHECK INTERRUPT |
| 88-101S-076 | INCORPORATES A CHANGE TO ALLOW THE COUNTER ON THE INTERRUPT PAGE TO START WHEN POWERING DOWN IN THE "HALT" MODE |
| 88-101S-077 | CORRECTS THE -12V SUPPLY LOW VOLTAGE CONDITION THAT OCCURS WHEN TRANSMITTING ON MULTIPLE MIA CHANNELS SIMULTANEOUSLY |
| 88-101S-078 | CORRECTS A CONDITION WHEREBY THE UNPOWERED CPU LOGIC PULLS THE DIAGNOSTIC LINES LOW LEAVING THEM IN AN UNPREDICTABLE STATE |

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SHUTTLE

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|--|---|--|-------------------------------|
| PREPARED BY G. F. McMullen D/292-440 (FB14) | CODE IDENT. NO. 03953 | DOCUMENT NUMBER MC615-0025 | REV A SEQ 07 |
| APPROVALS <i>[Signature]</i> 10/27/89 |  Rockwell International AMENDMENT COMPUTER, GENERAL PURPOSE ORBITER | DOCUMENT TYPE PROCUREMENT | |
| <i>[Signature]</i> 12/1/89 | | AUTHORITY MCR 10757 R10 G.O. 40977 | |
| <i>[Signature]</i> 12/1/89 | | DATE 10-17-89 | PAGE 1 OF 1 |
| <i>[Signature]</i> 12/2/89 | | SUBJECT CHANGE | |

This Amendment forms a part of MC615-0025, new, dated September 19, 1984.

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| | | |
|-------------|--------------------------|---------------------|
| WAS: | <u>ROCKWELL PART NO.</u> | <u>IBM PART NO.</u> |
| | MC615-0025-3000 | 6966000-2 |
| | MC615-0025-3001 | 6966000-3 |
| | MC615-0025-3002 | 6966000-4 |
| | MC615-0025-3003 | 6966000-5 |

| | | |
|------------|--------------------------|---------------------|
| IS: | <u>ROCKWELL PART NO.</u> | <u>IBM PART NO.</u> |
| | MC615-0025-3000 | 6966000-2 |
| | MC615-0025-3001 | 6966000-3 |
| | MC615-0025-3002 | 6966000-4 |
| | MC615-0025-3003 | 6966000-5 |
| | MC615-0025-3004 | 6966000-6 |
| | MC615-0025-4000 | 6966000-200 |

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| | | |
|-------------|--------------------------|------------------------|
| WAS: | <u>BUYER CONTROL NO.</u> | <u>SELLER PART NO.</u> |
| | MC615-0025-0200 | 6966000-20 |
| | MC615-0025-0201 | 6966000-21 |

| | | |
|------------|--------------------------|---------------------|
| IS: | <u>ROCKWELL PART NO.</u> | <u>IBM PART NO.</u> |
| | MC615-0025-0200 | 6966000-20 |
| | MC615-0025-0201 | 6966000-21 |
| | MC615-0025-0202 | 6966000-22 |

GPC Part Numbers MC615-0025-0202 and MC615-0025-3004 are the result of Incorporation of EDCP #89-101S-086.


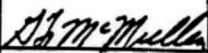


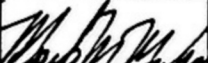
GPC Part Number MC615-0025-2000 is assigned to those units that are downgraded to "Non-Flight" status.

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SHUTTLE

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|---|--|---|-----------------|
| PREPARED BY R. A. Bugge D/292-440 (FB14) | CODE IDENT. NO. 03958  Rockwell International AMENDMENT COMPUTER, GENERAL PURPOSE ORBITER | DOCUMENT NUMBER MC615-0025 | REV A SEQ 08 |
| APPROVALS  | | DOCUMENT TYPE PROCUREMENT | |
|  3/21/91 | | AUTHORITY MCR 16991 Basic & RI G.O. 40977 | |
|  4/1/91 | | DATE 3-20-91 | PAGE 1 OF 1 |
|  4/1/91 | | SUBJECT CHANGE | |

This amendment forms a part of MC615-0025, New, dated September 19, 1984.

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| WAS: <u>ROCKWELL PART NO.</u> | <u>IBM PART NO.</u> |
|-------------------------------|---------------------|
| MC615-0025-0200 | 6966000-20 |
| MC615-0025-0201 | 6966000-21 |
| MC615-0025-0202 | 6966000-22 |

GPC Part Numbers MC615-0025-0202 and MC615-0025-3004 are the result of incorporation of EDCP #89-101S-086.

GPC Part Number MC615-0025-4000 is assigned to those units that are downgraded to "Non-Flight" status.

| IS: <u>ROCKWELL PART NO.</u> | <u>IBM PART NO.</u> |
|------------------------------|---------------------|
| MC615-0025-0200 | 6966000-20 |
| MC615-0025-0201 | 6966000-21 |
| MC615-0025-0202 | 6966000-22 |


GPC part numbers MC615-0025-0202 and MC615-0025-3004 are the result of the incorporation of the following EDCP's:

| <u>EDCP #</u> | <u>CHANGE DESCRIPTION</u> |
|---------------|--|
| 89-101S-086 | Replaces PROMs containing "Mid Value Select" micro-code which would sometimes cause the GPC to calculate incorrect results |
| 90-101S-092 | Corrects a condition whereby IOP parity errors occur due to timing margins that change when a particular manufacturer's integrated circuit is used |
| 91-101S-094 | Corrects a condition whereby an erroneous IOP write to memory can be caused by a Power On Reset |

GPC Part Number MC615-0025-4000 is assigned to those units that are downgraded to "Non-Flight" status.

EOCN # 053978

89-101S-086
 90-101S-092
 91-101S-094
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|--|--|---|------------------|-----------------|------------------|
| PREPARED BY R. A. Bugge D/292-440 (FR14) APPROVALS <i>Ab M. Mulla 8/27/91</i> <i>J. Alan 8/27/91</i> <i>M. Davila 8/27/91</i> | CODE IDENT. NO. 03953  Rockwell International AMENDMENT COMPUTER, GENERAL PURPOSE ORBITER | SHUTTLE DOCUMENT NUMBER MC615-0025 | | REV A | SEQ 09 |
| | | DOCUMENT TYPE PROCUREMENT | | | |
| | | AUTHORITY MCR 16991 R2 G.O. 40977 | | | |
| | | DATE 8-16-91 | PAGE 1 | OF 1 | |
| | | SUBJECT CHANGE | | | |

This amendment forms a part of MC615-0025, New, dated September 19, 1984.

Page 25 Para. 3.1.3

ADD:

ROCKWELL PART NO.

IBM PART NO.

MC615-0025-0203

6966000-23

GPC part numbers MC615-0025-0203 and MC615-0025-3005 are the result of the incorporation of the following EDCP's:

EDCP #

CHANGE DESCRIPTION

91-101S-095

corrects condition whereby adverse tolerance build-up in power supply diode mounting block hardware could allow screws to short against GPC top cover

91-101S-096

corrects component/vendor dependency condition whereby the use of one vendor's parts caused the GPC to go to "sleep" immediately on power-up in "Halt."

16 22 58 050

20 01 MY 82 90V 1688

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