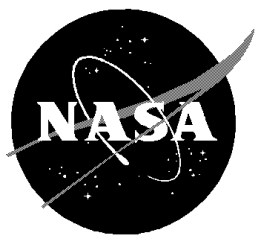


# **Instrumentation and Communications Officer (INCO) Systems Briefs**

---

Systems Division  
Communications Systems Branch

Revision G  
March 1, 2006



National Aeronautics and  
Space Administration

Lyndon B. Johnson Space Center  
Houston, Texas

Mission Operations Directorate

Instrumentation and Communications Officer (INCO)  
Systems Briefs

Revision G

March 1, 2006

Prepared by

*Original approval obtained*

---

Eric Wingrove  
Communications Systems Group

Approved by

*Original approval obtained*

---

John McKinnie  
Group Lead/Communications Systems Group

*Original approval obtained*

---

Ray B. Lachney  
Chief, Communications Systems Branch

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION  
LYNDON B. JOHNSON SPACE CENTER  
HOUSTON, TEXAS



## CONTENTS

| Section |   | Page |
|---------|---|------|
| 1       | ONBOARD COMMAND SYSTEM.....   | 1-1  |
| 2       | GROUND COMMAND SYSTEM DESCRIPTION.....  | 2-1  |
| 3       | S-BAND PHASE MODULATION SYSTEM.....   | 3-1  |
| 4       | S-BAND TRANSPONDER.....   | 4-1  |
| 5       | S-BAND PREAMPLIFIER.....  | 5-1  |
| 6       | S-BAND POWER AMPLIFIER.....   | 6-1  |
| 7       | S-BAND ANTENNA SYSTEM.....  | 7-1  |
| 8       | S-BAND FREQUENCY MODULATION SYSTEM.....   | 8-1  |
| 9       | KU-BAND RADAR/COMMUNICATIONS SYSTEM.....  | 9-1  |
| 10      | SOFTWARE DESCRIPTION FOR THE KU-BAND<br>INTEGRATED RADAR AND COMMUNICATIONS<br>EQUIPMENT ELECTRONIC ASSEMBLY..... | 10-1 |
| 11      | GROUND COMMAND INTERFACE LOGIC CONTROLLER.....  | 11-1 |
| 12      | NETWORK SIGNAL PROCESSOR.....   | 12-1 |
| 13      | COMSEC.....   | 13-1 |
| 14      | ANTENNA MANAGEMENT.....   | 14-1 |
| 15      | AUDIO DISTRIBUTION SYSTEM.....  | 15-1 |
| 16      | OPERATIONAL WIRELESS CREW<br>COMMUNICATIONS SYSTEM.....   | 16-1 |
| 17      | ULTRAHIGH FREQUENCY SYSTEM.....   | 17-1 |
| 18      | RESERVED  |      |
| 19      | SPACE-TO-SPACE COMMUNICATIONS SYSTEM.....   | 19-1 |
| 20      | COMMUNICATIONS AND INSTRUMENTATION SYSTEM<br>WATER AND AIR-COOLED EQUIPMENT.....                                  | 20-1 |
| 21      | RESERVED  |      |
| 22      | RESERVED  |      |

| <b>Section</b> | <b>Page</b>  |
|----------------|--|
| <b>23</b>      | RESERVED   |
| <b>24</b>      | RESERVED   |
| <b>25</b>      | RESERVED   |
| <b>26</b>      | <b>ORBITER OPERATIONAL INSTRUMENTATION OVERVIEW ..... 26-1</b>               |
| <b>27</b>      | <b>OI DEDICATED SIGNAL CONDITIONERS..... 27-1</b>                            |
| <b>28</b>      | <b>MULTIPLEXER/DEMULTIPLEXER..... 28-1</b>                                   |
| <b>29</b>      | <b>PULSE CODE MODULATION MASTER UNIT ..... 29-1</b>                          |
| <b>30</b>      | <b>SM INPUT/OUTPUT AND ERROR PROCESSING<br/>SOFTWARE FOR PCMMU..... 30-1</b> |
| <b>31</b>      | <b>PAYLOAD INTERROGATOR..... 31-1</b>  |
| <b>32</b>      | <b>PAYLOAD SIGNAL PROCESSOR ..... 32-1</b>                                   |
| <b>33</b>      | <b>PAYLOAD DATA INTERLEAVER..... 33-1</b>                                    |
| <b>34</b>      | RESERVED   |
| <b>35</b>      | <b>MODULAR AUXILLARY DATA SYSTEM..... 35-1</b>                               |
| <b>36</b>      | RESERVED   |
| <b>37</b>      | RESERVED   |
| <b>38</b>      | <b>ORBITER INTERFACE UNIT ..... 38-1</b>                                     |
| <b>39</b>      | RESERVED   |
| <b>40</b>      | <b>MODULAR MEMORY UNIT/SOLID STATE RECORDER ..... 40-1</b>                   |
| <b>41</b>      | RESERVED   |
| <b>42</b>      | RESERVED   |
| <b>43</b>      | RESERVED   |
| <b>44</b>      | RESERVED   |
| <b>45</b>      | RESERVED   |
| <b>46</b>      | RESERVED   |
| <b>47</b>      | <b>GROUND NETWORK..... 47-1</b>  |
| <b>48</b>      | <b>TRACKING AND DATA RELAY SATELLITE SYSTEM ..... 48-1</b>                   |

| <b>Section</b> |  | <b>Page</b> |
|----------------|--|-------------|
| <b>49</b>      | <b>TELEMETRY PROCESSING IN THE MCC.....</b>      | <b>49-1</b> |
| <b>50</b>      | RESERVED   |             |
| <b>51</b>      | RESERVED   |             |
| <b>52</b>      | RESERVED   |             |
| <b>53</b>      | RESERVED   |             |
| <b>54</b>      | RESERVED   |             |
| <b>55</b>      | RESERVED   |             |
| <b>56</b>      | RESERVED   |             |
| <b>57</b>      | RESERVED   |             |
| <b>58</b>      | RESERVED   |             |
| <b>59</b>      | RESERVED   |             |
| <b>60</b>      | RESERVED   |             |
| <b>61</b>      | RESERVED   |             |
| <b>62</b>      | RESERVED   |             |
| <b>63</b>      | RESERVED   |             |
| <b>64</b>      | RESERVED   |             |
| <b>65</b>      | RESERVED   |             |
| <b>66</b>      | RESERVED   |             |
| <b>67</b>      | RESERVED   |             |
| <b>68</b>      | RESERVED   |             |
| <b>69</b>      | RESERVED   |             |
| <b>70</b>      | <b>CLOSED CIRCUIT TELEVISION .....</b>           | <b>70-1</b> |
| <b>71</b>      | <b>SOLID STATE COLOR TELEVISION CAMERA .....</b> | <b>71-1</b> |
| <b>72</b>      | <b>WIRELESS VIDEO SYSTEM.....</b>                | <b>72-1</b> |
| <b>73</b>      | <b>SHUTTLE IN-CABIN VIDEO EQUIPMENT .....</b>    | <b>73-1</b> |
| <b>74</b>      | <b>COLOR TELEVISION MONITOR.....</b>             | <b>74-1</b> |

| <b>Section</b> |   | <b>Page</b> |
|----------------|---|-------------|
| <b>75</b>      | <b>SEQUENTIAL STILL VIDEO .....</b>                                     | <b>75-1</b> |
| <b>76</b>      | <b>DIGITAL TELEVISION .....</b>   | <b>76-1</b> |
| <b>77</b>      | <b>ORBITER BOOM SENSOR SYSTEM .....</b>                                 | <b>77-1</b> |
| <b>78</b>      | <b>ENHANCED LAUNCH VEHICLE IMAGING SYSTEM .....</b>                     | <b>78-1</b> |
| <b>79</b>      | RESERVED  |             |
| <b>80</b>      | RESERVED  |             |
| <b>81</b>      | <b>SOLID ROCKET BOOSTER/EXTERNAL TANK<br/>RANGE SAFETY SYSTEM .....</b> | <b>81-1</b> |

**List of Originators**

| <b>SB</b> | <b>Title</b>   | <b>Originator</b> |
|-----------|--|-------------------|
| 1         | Onboard Command System   | S. Sides          |
| 2         | Ground Command System Description  | S. Sides          |
| 3         | S-Band Phase Modulation System   | D. Brown          |
| 4         | S-Band Transponder   | D. Brown          |
| 5         | S-Band Preamplifier  | D. Brown          |
| 6         | S-Band Power Amplifier   | L. Hoppe          |
| 7         | S-Band Antenna System  | L. Hoppe          |
| 8         | S-Band Frequency Modulation System   | D. Miller         |
| 9         | Ku-Band Radar/Communications System  | J. Fanelli        |
| 10        | Software Description for the Ku-Band Integrated Radar and Communications Equipment Electronic Assembly | J. Fanelli        |
| 11        | Ground Command Interface Logic Controller  | D. Brown          |
| 12        | Network Signal Processor   | J. Fanelli        |
| 13        | COMSEC   | S. Sides          |
| 14        | Antenna Management   | S. Sides          |
| 15        | Audio Distribution System  | D. Branham        |
| 16        | Operational Wireless Crew Communications System  | L. Hoppe          |
| 17        | Ultrahigh Frequency System   | J. Scott          |
| 18        |  |                   |
| 19        | Space-to-Space Communications System   | D. Branham        |
| 20        | Communications and Instrumentation System Water and Air-Cooled Equipment                               | J. King           |
| 21        |  |                   |
| 22        |  |                   |
| 23        |  |                   |
| 24        |  |                   |
| 25        |  |                   |
| 26        | Orbiter Operational Instrumentation Overview   | D. Miller         |
| 27        | OI Dedicated Signal Conditioners   | D. Miller         |
| 28        | Multiplexer/Demultiplexer  | D. Miller         |
| 29        | Pulse Code Modulation Master Unit  | D. Miller         |
| 30        | SM Input/Output and Error Processing Software for PCMMU  | S. Sides          |

| <b>SB</b> | <b>Title</b>                             | <b>Originator</b> |
|-----------|--|-------------------|
| 31        | Payload Interrogator                     | D. Miller         |
| 32        | Payload Signal Processor                 | J. Fanelli        |
| 33        | Payload Data Interleaver                 | J. Fanelli        |
| 34        |  |                   |
| 35        | Modular Auxiliary Data System            | D. Miller         |
| 36        |  |                   |
| 37        |  |                   |
| 38        | Orbiter Interface Unit                   | D. Branham        |
| 39        |  |                   |
| 40        | Modular Memory Unit/Solid State Recorder | J. Joy            |
| 41        |  |                   |
| 42        |  |                   |
| 43        |  |                   |
| 44        |  |                   |
| 45        |  |                   |
| 46        |  |                   |
| 47        | Ground Network                           | J. McKinnie       |
| 48        | Tracking and Data Relay Satellite System | J. McKinnie       |
| 49        | Telemetry Processing in the MOC          | D. Miller         |
| 50        |  |                   |
| 51        |  |                   |
| 52        |  |                   |
| 53        |  |                   |
| 54        |  |                   |
| 55        |  |                   |
| 56        |  |                   |
| 57        |  |                   |
| 58        |  |                   |
| 59        |  |                   |
| 60        |  |                   |
| 61        |  |                   |
| 62        |  |                   |
| 63        |  |                   |

| <b>SB</b> | <b>Title</b>   | <b>Originator</b> |
|-----------|--|-------------------|
| 64        |  |                   |
| 65        |  |                   |
| 66        |  |                   |
| 67        |  |                   |
| 68        |  |                   |
| 69        |  |                   |
| 70        | Closed Circuit Television                              | J. McKinnie       |
| 71        | Solid State Color Television Camera                    | J. McKinnie       |
| 72        | Wireless Video System                                  | D. Bickham        |
| 73        | Shuttle In-Cabin Video Equipment                       | D. Branham        |
| 74        | Color Television Monitor                               | L. Hoppe          |
| 75        | Sequential Still Video                                 | D. Gresham        |
| 76        | Digital Television                                     | D. Branham        |
| 77        | Orbiter Boom Sensor System                             | E. Wingrove       |
| 78        |  |                   |
| 79        |  |                   |
| 80        |  |                   |
| 81        | Solid Rocket Booster/External Tank Range Safety System | G. Horlacher      |

## SECTION 1 - ONBOARD COMMAND SYSTEM

### CONTENTS

| Section | Page   |
|---------|--|
| 1.1     | INTRODUCTION..... 1-1  |
| 1.2     | SYSTEMS OVERVIEW..... 1-1  |
| 1.2.1   | Command Type Overview..... 1-2                                     |
| 1.2.2   | Command Validation Overview..... 1-2                               |
| 1.3     | COMMAND DATA STRUCTURE..... 1-2                                    |
| 1.3.1   | Command Header Information..... 1-2                                |
| 1.3.2   | Real-Time Commands..... 1-8  |
| 1.3.3   | Command Loads..... 1-12  |
| 1.4     | COMMAND PROCESSING..... 1-12                                       |
| 1.4.1   | NSP Processing..... 1-12   |
| 1.4.2   | NSP to GPC Interface..... 1-13                                     |
| 1.4.3   | GPC Processing..... 1-19   |
| 1.5     | INCO COMMAND TYPES..... 1-25                                       |
| 1.5.1   | Table Maintenance Block Update..... 1-25                           |
| 1.5.2   | Stored Program Command..... 1-26                                   |
| 1.5.3   | Time Executed Command..... 1-27                                    |
| 1.5.4   | Telemetry Format Load/Decomutator Format Load..... 1-28            |
| 1.5.5   | Payload Throughput Loads..... 1-30                                 |
| 1.5.6   | PSP Rejection Indicators from Uplinked Commands..... 1-31          |
| 1.6     | ON-BOARD COMMANDING..... 1-33                                      |
| 1.6.1   | Uplink Activity Indicator..... 1-33                                |
| 1.6.2   | Real-Time Commands via the DPS Utility Spec..... 1-33              |
| 1.6.3   | Crew Command Inhibits..... 1-35                                    |
| 1.7     | UPLINK ERROR CONDITIONS AND REPONSES..... 1-35                     |
| 1.7.1   | I/O Error FF3 [FF1]..... 1-35                                      |
| 1.7.2   | PASS/BFS Sync Is Lost..... 1-35                                    |
| 1.7.3   | BFS Not Tracking String 3 [1]..... 1-35                            |
| 1.7.4   | GNC-SM Loss of Common Set Sync..... 1-35                           |
| 1.7.5   | Bus Control Element (BCE) String 3 [1] - NSP..... 1-36             |
| 1.7.6   | On-Orbit SM GPC Fails..... 1-36                                    |
| 1.8     | COMMAND SYSTEM IDIOSYNCRASIES..... 1-36                            |
| 1.8.1   | Two-Stage Word-by-Word Problems..... 1-36                          |
| 1.8.2   | DEU Equivalent Commands (DR 36329)..... 1-37                       |
| 1.8.3   | Uplink Error Processing (DR 37553)..... 1-37                       |
| 1.8.4   | TM - SPEC vs. Uplink Interaction (DR 37572)..... 1-38              |
| 1.8.5   | Uplink to RS OPS-000 (DR 43987)..... 1-38                          |
| 1.8.6   | Ku Band/ PTC Overwritten (DR 55064)..... 1-38                      |
| 1.8.7   | Concatenation of Multiple PTCs (DR 55783)..... 1-38                |
| 1.8.8   | Multiple RTCIO on FC Buses may Jitter HFE I/O (DR 56157)..... 1-38 |



| Section |   | Page |
|---------|---|------|
| 1.8.9   | PSP Load In G9 Incorrectly Rejected (DR 111692) ..... | 1-39 |
| 1.8.10  | MDM Channel Address Anomaly (DR B03934) .....         | 1-39 |
| 1.8.11  | BFS Uplink Command Processor (DR B08063).....         | 1-39 |
| 1.9     | REFERENCES.....                                       | 1-39 |

## TABLES

### Table

|      |   |      |
|------|---|------|
| 1-1  | Orbiter Vehicle Codes .....                             | 1-3  |
| 1-2  | Major Function and GPC Codes .....                      | 1-3  |
| 1-3  | Op Codes .....  | 1-4  |
| 1-4  | First Word/Last Word Indications .....                  | 1-7  |
| 1-5  | MDM Codes .....   | 1-10 |
| 1-6  | NSP Power Discrettes.....                               | 1-15 |
| 1-7  | Uplink Block Discrettes.....                            | 1-16 |
| 1-8  | GPC Uplink Validity Bit Definition .....                | 1-20 |
| 1-9  | Definition of GPC Bits in the NSP Validity Word .....   | 1-20 |
| 1-10 | Definition of GPC Bits in the NSP Validity Word 2 ..... | 1-22 |
| 1-11 | Two-Stage Buffer Telemetry .....                        | 1-24 |
| 1-12 | TFL/DFL item entries .....                              | 1-29 |
| 1-13 | PSP Command Reject Flags.....                           | 1-32 |

## FIGURES

### Figure

|      |                                      |      |
|------|--------------------------------------|------|
| 1-1  | Command System Overview.....         | 1-1  |
| 1-2  | Command Header .....                 | 1-3  |
| 1-3  | RTC Routing Bits .....               | 1-9  |
| 1-4  | Example of an RTC.....               | 1-11 |
| 1-5  | Example of Reset/Set Mask Data ..... | 1-11 |
| 1-6  | Command Data Route .....             | 1-15 |
| 1-7  | NSP/GPC Interface .....              | 1-17 |
| 1-8  | NSP Serial I/O Structure .....       | 1-17 |
| 1-9  | NSP Validity Word.....               | 1-18 |
| 1-10 | NSP Val Word 2 .....                 | 1-19 |
| 1-11 | DPS Utility SPEC Display.....        | 1-34 |

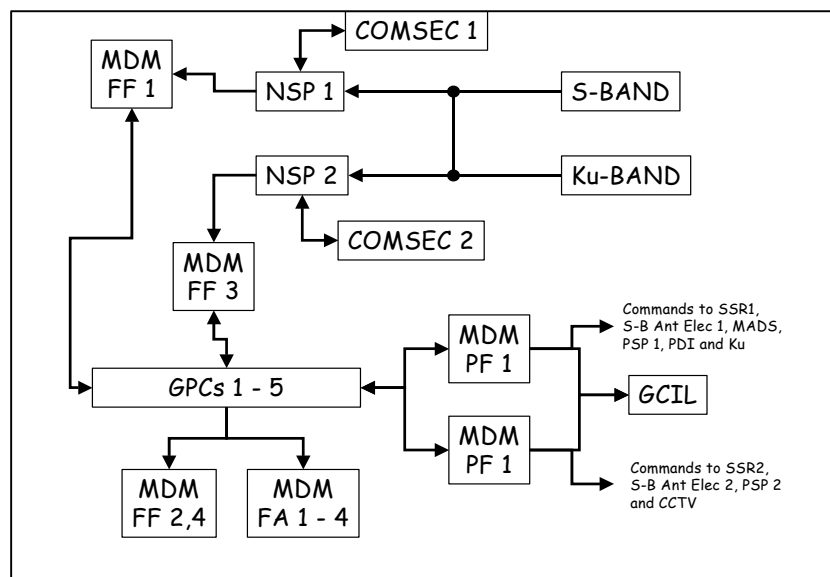
## SECTION 1 ON BOARD COMMAND SYSTEM

### 1.1 INTRODUCTION

The command system on the orbiter is primarily used to control the operations of sub-systems and to make changes to flight software parameters. This systems brief will describe: (1) how the sub-systems involved in processing the commands interface to one another, (2) how the commands are validated, (3) how the commands are distributed to the sub systems or the flight software applications, (4) some safeguards that should be used to prevent erroneous commanding and (5) some idiosyncrasies of the on-board command system. Uplink of commands from the Mission Control Center (MCC) is described in INCO Systems Brief Section 2 Ground Command System Description.

### 1.2 SYSTEMS OVERVIEW

The orbiter Network Signal Processor (NSP) selects either the S-Band or the Ku-Band system 128 kbps multiplexed uplink. The uplinked data is sent to the Network Signal processor, which passes the data on to the Communications Security (COMSEC) line replaceable unit (LRU) if the uplink is encrypted. The COMSEC will decrypt the uplink data, time authenticate the command portion, multiplex it with the audio channels, and transfer it back to the NSP. Once the NSP has validated the command data, it will send the data via a flight critical Multiplexer/Demultiplexer (MDM) to a general purpose computer (GPC). The GPC will process the contents of the command data, looking for valid command structures and data types. After the GPC has confirmed that the command data is valid, it forwards the data to either a flight critical MDM, a payload MDM, or a flight software application. Figure 1-1 depicts these interfaces.



**Figure 1-1. Command System Overview**

### 1.2.1 Command Type Overview

There are several types of commands that can be uplinked to the orbiter. The various types of commands have different functions on board. The predominant type of command is the Real-Time Command (RTC). These commands are primarily used to change the operation of an onboard LRU. For example, INCO sends commands that control when the FM system is on or off. The other primary types of commands are called Loads. These commands are used to change the state of flight software, which may eventually change the state of some LRU. Each type of command will be covered in more detail later in this systems brief.

### 1.2.2 Command Validation Overview

In order to ensure the data integrity of the commands that are sent to the orbiter, there are several operations that must occur in the MCC to validate the command data. The MCC will add a time stamp, BCH encode, add parity bits, and then encrypt the whole uplink to the orbiter. The time stamp is used to ensure the command originated from the MCC less than 19 sec apart from the on-board time. The parity bits are used by the NSP and the COMSEC to validate that the command data did not get corrupted during uplink. The encryption guarantees that the command data could not be tampered with during uplink. See the NSP and COMSEC Systems Briefs for details on these validation techniques.

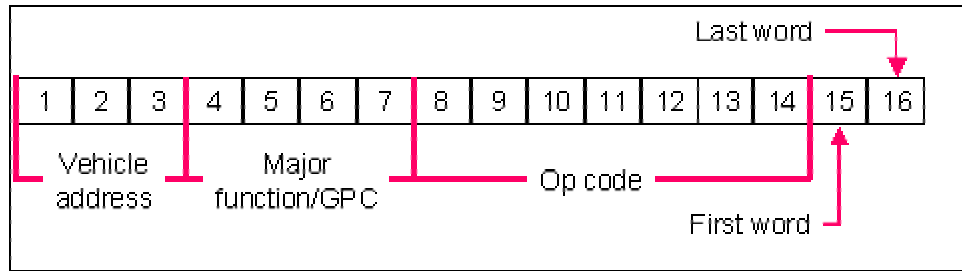
## 1.3 COMMAND DATA STRUCTURE

Commands are made up of one or more 48 bit command data words. These command data words must be correctly implemented for the command to successfully execute onboard. Each type of command is defined in the Downlist/Uplink Computer Program Development Specification (CPDS) for the Primary Avionics Software System (PASS) and the Program Requirements Document (PRD) for the Backup Flight Software (BFS).

In all cases, the first 16 bits of the 48 bit command data word consist of: a vehicle address (i.e., orbiter tail number), a GPC major function (i.e., GNC, SM, BFS and PL), an operations code and a first word/last word indicator. The 32 bits of actual command data that will affect an LRU or flight software follow the first 16 bits. Each command uplinked could have up to 33 of these command data words.

### 1.3.1 Command Header Information

The command header information is contained in the first 16 bits of each command. Figure 1-2 shows how the bits in the command header are organized.



**Figure 1-2. Command Header**

**1.3.1.1 Vehicle Address**

Each orbiter has a 3 bit address programmed within its five GPCs. This address uniquely identifies the orbiter to which the command is intended. If this value is not correct, the GPC will reject the command with a vehicle address error indication. This concept was implemented so that the MCC could support multiple orbiter activities at one time. The following table is the list of vehicle addresses.

**Table 1-1. Orbiter Vehicle Codes**

| <u>Code</u> | <u>Vehicle</u> | <u>Name</u> |
|-------------|----------------|-------------|
| 011         | 103            | Discovery   |
| 100         | 104            | Atlantis    |
| 101         | 105            | Endeavor    |

**All other values are illegal**

**1.3.1.2 Major Function (MF)/GPC Number**

Each command must be addressed to either a major function (i.e., flight software configuration) or a particular GPC. The GPC flight software checks for this condition. The following table is the list of codes for the major functions and the GPC numbers.

**Table 1-2. Major Function and GPC Codes**

| <u>Code</u> | <u>GPC</u> | <u>Code</u> | <u>MF</u> |
|-------------|------------|-------------|-----------|
| 0001        | 1          | 0111        | GNC       |
| 0010        | 2          | 1000        | SM        |
| 0011        | 3          | 1001        | PL        |
| 0100        | 4          | 1010        | BFS       |
| 0101        | 5          |             |           |
| 0110        | ALL        |             |           |

**1011 to 1111 are illegal codes**

1.3.1.3 Operation Code

The seven bit Operation Code, or Op Code, is used to define what type of command is contained in the command words. The flight software specifies what these Op Codes are and how the command data is organized within the command words. Some Op Codes are not valid in all flight software configurations (a.k.a. Ops modes). Table 1-3 provides GPC OI-30 Op Codes which list command types and software configurations.

Table 1-3. Op Codes

| Op Code | Command Type                    | Memory Config (Ops Mode) |    |    |    |    |   |    |    |    |    |    |
|---------|---------------------------------|--------------------------|----|----|----|----|---|----|----|----|----|----|
|         |                                 | G1                       | G6 | G2 | G3 | S2 | 0 | P9 | G8 | G9 | B1 | B3 |
| 0000001 | G-MEM Contiguous                |                          |    | ●  |    | ●  | ● | ●  | ●  | ●  | ●  | ●  |
| 0000010 | G-MEM Scatter                   |                          |    | ●  |    | ●  | ● | ●  | ●  | ●  | ●  | ●  |
| 0000011 | MDM Multiple                    | ●                        | ●  | ●  | ●  | ●  | ● | ●  | ●  | ●  | ●  | ●  |
| 0000100 | MDM SPC MULT                    |                          |    |    |    | ●  |   |    |    |    | ●  | ●  |
| 0000101 | Equiv DEU                       | ●                        | ●  | ●  | ●  | ●  | ● | ●  | ●  | ●  |    |    |
| 0000110 | MMU Patch SM Interface          |                          |    |    |    | ●  |   | ●  |    |    |    |    |
| 0000111 | Ku Band / S Band Antenna Cntl   |                          |    |    |    | ●  |   |    |    |    |    |    |
| 0001000 | IMU Refsmmat                    |                          |    | ●  | ●  |    |   |    |    |    |    | ●  |
| 0001001 | Orbiter State Vector            | ●                        | ●  | ●  | ●  |    |   |    | ●  |    | ●  | ●  |
| 0001010 | Rend Veh State Vector           |                          |    | ●  |    |    |   |    |    |    |    |    |
| 0001011 | Wind Table                      |                          |    |    |    |    |   |    |    | ●  |    |    |
| 0001100 | Guidance Polynomial             |                          |    |    |    |    |   |    |    | ●  |    |    |
| 0001110 | Throt-Vel & Tref-Adjust         |                          |    |    |    |    |   |    |    | ●  |    |    |
| 0001111 | Launch Targeting                | ●                        | ●  |    |    |    |   |    |    |    | ●  |    |
| 0010000 | On-Orbit Guidance Targets PEG 7 |                          |    | ●  |    |    |   |    |    |    |    |    |
| 0010001 | Deorbit Guidance PEG 7          |                          |    | ●  | ●  |    |   |    |    |    |    | ●  |
| 0010010 | IMU Gyro Bias                   | ●                        |    | ●  | ●  |    |   |    |    |    |    | ●  |
| 0010011 | IMU Accelerometer Bias          |                          |    | ●  | ●  |    |   |    |    |    |    | ●  |
| 0010100 | Deorbit Guidance PEG 4          |                          |    | ●  | ●  |    |   |    |    |    |    | ●  |
| 0010101 | Deorbit Landing Site Parameters | ●                        | ●  |    | ●  |    |   |    |    |    | ●  | ●  |

Table 1-3. Op Codes (continued)

| Op Code | Command Type   | Memory Config (Ops Mode) |    |    |    |    |   |    |    |    |    |    |
|---------|--|--------------------------|----|----|----|----|---|----|----|----|----|----|
|         |  | G1                       | G6 | G2 | G3 | S2 | 0 | P9 | G8 | G9 | B1 | B3 |
| 0010110 | TDRS State Vector                                    |                          |    |    |    | ●  |   |    |    |    | ●  | ●  |
| 0010111 | Ku Band Antenna Bias Matrix                          |                          |    |    |    | ●  |   |    |    |    |    |    |
| 0011000 | ADI Inertial Quaternion                              |                          | ●  | ●  |    |    |   |    | ●  |    |    | ●  |
| 0011001 | OMS Targeting  | ●                        | ●  |    |    |    |   |    |    |    | ●  |    |
| 0011010 | Payload Data Load                                    |                          |    |    |    | ●  |   |    |    |    |    |    |
| 0011011 | PSP Configuration Message                            |                          |    |    |    | ●  |   |    |    |    |    |    |
| 0011100 | Vehicle Inertia Matrix                               |                          |    | ●  |    |    |   |    |    |    |    |    |
| 0011101 | ADI Reference Quaternion                             |                          |    | ●  | ●  |    |   |    |    | ●  | ●  | ●  |
| 0011110 | ADI Bias LVLH Quat                                   |                          |    | ●  | ●  |    |   |    |    | ●  | ●  | ●  |
| 0011111 | Deorbit TACAN Para                                   | ●                        | ●  |    | ●  |    |   |    |    |    | ●  | ●  |
| 0100000 | Delta Nav  | ●                        | ●  |    | ●  |    |   |    |    |    | ●  | ●  |
| 0100001 | Table Maintenance Block Update                       |                          |    |    |    | ●  |   |    |    |    | ●  | ●  |
| 0100010 | MSBLS Parameters Load                                | ●                        | ●  |    | ●  |    |   |    |    |    |    |    |
| 0100101 | OMS Assist, Abort Dump Timers, Masses and Velocities |                          |    |    |    |    |   |    |    | ●  |    |    |
| 0100110 | IMU Accelerometer Scale Factor                       |                          |    | ●  | ●  |    |   |    |    |    |    | ●  |
| 0100111 | Throttle Levels                                      |                          |    |    |    |    |   |    |    | ●  |    |    |
| 0101000 | Guidance Polynomial PHI I                            |                          |    |    |    |    |   |    |    | ●  |    |    |
| 0101001 | Vent/RCS Body Force Vector                           |                          |    | ●  |    |    |   |    |    |    |    |    |
| 0101010 | Drag Model Scale Factors Load                        |                          |    | ●  |    |    |   |    | ●  |    |    |    |
| 0101011 | Covariance Matrix Parameters Load                    |                          |    | ●  |    |    |   |    |    |    |    |    |
| 0101100 | MDM BITE Data Read                                   | ●                        | ●  | ●  | ●  | ●  | ● | ●  | ●  | ●  |    |    |
| 0101101 | Insertion Guidance Target PEG 4                      | ●                        | ●  |    |    |    |   |    |    |    | ●  |    |

Table 1-3. Op Codes (continued)

| Op Code | Command Type                        | Memory Config (Ops Mode) |    |    |    |    |   |    |    |    |    |    |
|---------|-------------------------------------|--------------------------|----|----|----|----|---|----|----|----|----|----|
|         |                                     | G1                       | G6 | G2 | G3 | S2 | 0 | P9 | G8 | G9 | B1 | B3 |
| 0101110 | Time Executed SIO (TEC)             |                          |    |    |    | ●  |   |    |    |    |    |    |
| 0101111 | Star Catalog Update Load            |                          |    | ●  |    |    |   |    |    |    |    |    |
| 0110000 | Orbiter Rate Gyro Bias Update       |                          |    |    | ●  |    |   |    |    |    |    | ●  |
| 0110001 | Accelerometer Assembly Bias Update  |                          |    |    | ●  |    |   |    |    |    |    | ●  |
| 0110010 | RCS Quantity Monitoring             |                          |    | ●  |    |    |   |    |    | ●  |    |    |
| 0110011 | Notch Filter/Mass Properties Update |                          |    | ●  |    |    |   |    |    |    |    |    |
| 0110100 | RMS End Effector ID Data Load       |                          |    |    |    | ●  |   |    |    |    |    |    |
| 0110101 | RMS Payload ID Data Load            |                          |    |    |    | ●  |   |    |    |    |    |    |
| 0110110 | TFL and DFL and PSP I/O Enable      |                          |    |    |    | ●  |   |    |    |    |    |    |
| 0110111 | Variable D/L Select                 | ●                        | ●  | ●  | ●  | ●  | ● | ●  | ●  | ●  | ●  | ●  |
| 0111000 | Time Execute Command Clear          |                          |    |    |    | ●  |   |    |    |    |    |    |
| 0111001 | RMS Autosequence Header Data Load   |                          |    |    |    | ●  |   |    |    |    |    |    |
| 0111010 | RMS Autosequence Point Data Load    |                          |    |    |    | ●  |   |    |    |    |    |    |
| 0111011 | RNP Matrix Time Parameter Load      |                          |    | ●  | ●  |    |   |    |    |    |    |    |
| 0111100 | Scaling Corf Set & Data Type Update |                          |    |    |    | ●  |   |    |    |    |    |    |
| 0111101 | Payload Throughput                  |                          |    |    |    | ●  |   |    |    |    |    |    |
| 0111110 | Payload MDM SPC Mult                |                          |    |    |    | ●  |   |    |    |    |    |    |
| 0111111 | GPS SOP Time Adjustment Load        | ●                        | ●  | ●  | ●  |    |   |    |    | ●  | ●  | ●  |
| 1000001 | 2-Stage Buffer Clear                | ●                        | ●  | ●  | ●  | ●  | ● | ●  | ●  | ●  | ●  | ●  |
| 1000010 | SPC Buffer Clear                    |                          |    |    |    | ●  |   |    |    |    | ●  | ●  |
| 1000011 | 2-Stage Buffer Execute              | ●                        | ●  | ●  | ●  | ●  | ● | ●  | ●  | ●  | ●  | ●  |
| 1000100 | Word By Word Correction             | ●                        | ●  | ●  | ●  | ●  | ● | ●  | ●  | ●  |    |    |
| 1000101 | MDM Single                          | ●                        | ●  | ●  | ●  | ●  | ● | ●  | ●  | ●  | ●  | ●  |

*Table 1-3. Op Codes (concluded)*

| Op Code | Command Type   | Memory Config (Ops Mode) |    |    |    |    |   |    |    |    |    |    |
|---------|--|--------------------------|----|----|----|----|---|----|----|----|----|----|
|         |  | G1                       | G6 | G2 | G3 | S2 | 0 | P9 | G8 | G9 | B1 | B3 |
| 1000110 | UL Activity Off                                      | ●                        | ●  | ●  | ●  | ●  | ● | ●  | ●  | ●  | ●  | ●  |
| 1000111 | UL Activity On                                       | ●                        | ●  | ●  | ●  | ●  | ● | ●  | ●  | ●  | ●  | ●  |
| 1001000 | Memory Overlay Uplink                                | ●                        | ●  | ●  | ●  | ●  | ● | ●  | ●  | ●  | ●  | ●  |
| 1001001 | Payload SPC Buffer Clear                             |                          |    |    |    | ●  |   |    |    |    |    |    |
| 1001010 | Uplink Command Counter Reset                         | ●                        | ●  | ●  | ●  | ●  | ● | ●  | ●  | ●  | ●  | ●  |
| 1001011 | PTC Buffer Clear                                     |                          |    |    |    | ●  |   |    |    |    |    |    |
| 1100000 | Ascent Pseudo and ATO MECO Targets Load              |                          |    |    |    |    |   |    |    | ●  |    |    |
| 1100001 | GPCF Command   |                          |    |    |    | ●  |   |    |    |    |    |    |
| 1100010 | RTLS Guidance Parameters Load                        |                          |    |    |    |    |   |    |    | ●  |    |    |
| 1100011 | Variable Intact Abort Throttle Limit Velocities Load |                          |    |    |    |    |   |    |    | ●  |    |    |

**1.3.1.4 First Word/Last Word Indicator**

The last two bits in the 16 bit command header are the first word/ last word indicator. As described in paragraph 1.3, each command uplinked could contain multiple 48 bit command words. The last two bits are used by the GPCs to determine if the 48 bit command word is the first word, last word, or “in the middle”. They are also used to indicate if the 48-bit command word is a complete command. Table 1-4 describes the combinations for first word/last word indications.

*Table 1-4. First Word/Last Word Indications*

| Bits      |           | <u>Combination Meaning</u>   |
|-----------|-----------|--|
| <u>15</u> | <u>16</u> |  |
| 1         | 0         | First command word in the load                                     |
| 0         | 1         | Last command word in the load                                      |
| 1         | 1         | Single command word load   |
| 0         | 0         | Intermediate command words in loads greater than two command words |



### 1.3.1.5 Command Data Word

Bits 17 through 38 represent the portion of the command that will perform a configuration change to the flight software or directly to an LRU. These bits vary depending on the Op Code of the command. If a command is made up of multiple command words then each command word will contain the command header and last 32 bits of command data. If a command does not need all 32 bits of the last command data word, then the command processing on the ground will fill the remainder of the command with zeros.

### 1.3.2 Real-Time Commands

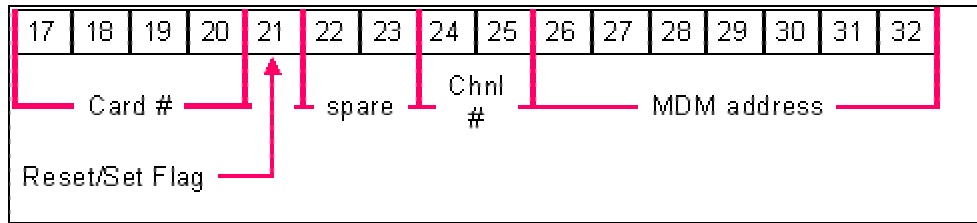
Real-Time Commands (RTC) are designed to directly configure MDM output drivers. INCO is the primary user of this type of command although there are other systems that can be manipulated via RTCs. For a complete listing of the RTCs that are available for each mission, refer to either the Shuttle Data Tape file 5 or the generic command server RTC inventory display in the MCC.

#### 1.3.2.1 RTC Command Data Structure

An RTC usually consists of two 48-bit words, one with a reset mask and one with a set mask. Although these are usually thought of as one command, it is important to remember that the command system treats these as **two separate commands**. It is possible for half of the RTC to be rejected because of errors, and the other half to be executed. This has been experienced in flight and can result in unexpected command response (e.g., recorder going to run instead of standby). The number of single word RTCs is limited (i.e., U/L activity on/off, SPC and TEC buffer clears, 2-STG buffer exec). Since the first 16 bits of each command word has already been defined above, this section will only cover the reset and set masks for an RTC.

There are two major components of an RTC included in the last 32 bits of the command word. Bits 17 through 32 define which MDM card and channel to send the mask data (bits 33 through 48).

Bits 17 through 20 define the module address (MOD ADDR) which is the card on the MDM that is connected to the commanded LRU. Bit 21 indicates whether the command is a reset or a set command. Bits 22 and 23 are not used. Bits 24 and 25 are the channel selection on the MDM card that is specified in the MOD ADDR above. Lastly, bits 26 through 32 are the address of the MDM connected to the commanded LRU. Figure 1-3 graphically represents these bits.



**Figure 1-3. RTC Routing Bits**

### 1.3.2.2 Module Address

The module address, represented in binary in bits 17 through 20, is the card number in the MDM which is addressed in bits 26 through 32. As an example card 15 in the MDM would be represented by 1111 in these bits. An MDM has 16 cards, 0-15.

### 1.3.2.3 Reset/Set

The reset/set bit 21 is used to determine if the command is a reset or a set command for the channel on the MDM card. If this bit is set low, '0', then the command is a reset command. Conversely, if it's high, '1', the command is a set command. Bits 22 and 23 are spares, which are not used for this type of command.

### 1.3.2.4 Discrete Channel Select

The discrete channel select bits 24 and 25 are used to pick between the various channels on the MDM card. There are up to four channels (0-3) defined on an MDM card.

### 1.3.2.5 MDM Number

Bits 26 through 32 indicate which MDM is addressed for the command. Bit 32 is the least significant bit. Table 1-5 is a summary of the 7 bit representation of Orbiter MDMs.

**Table 1-5. MDM Codes**

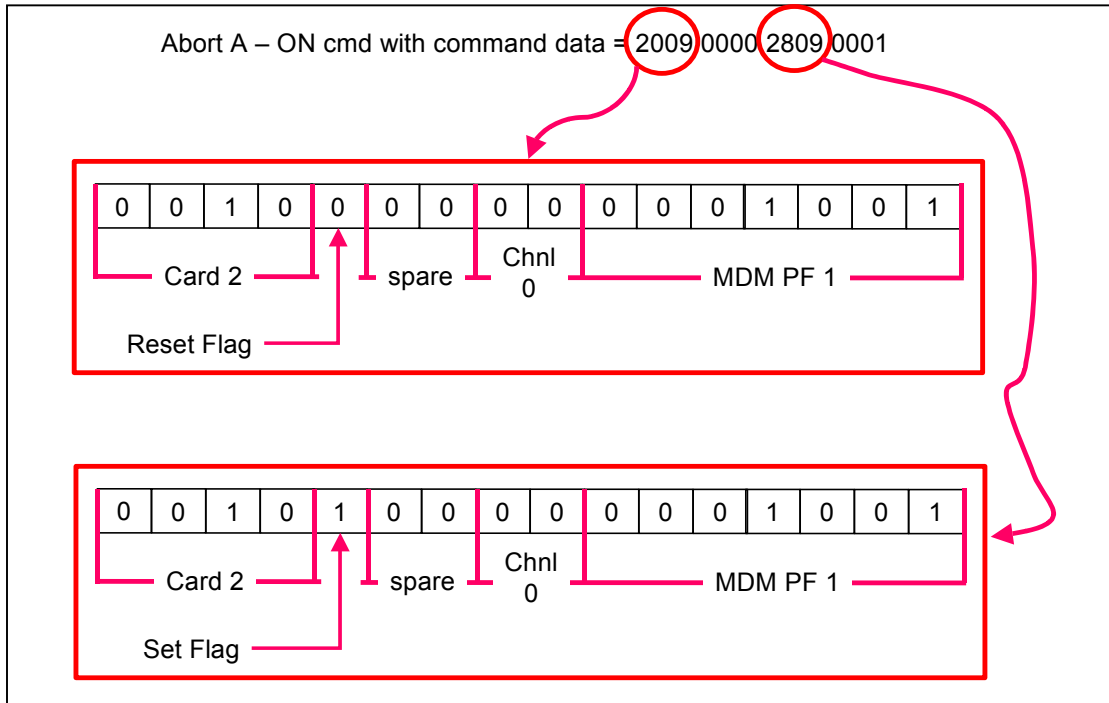
| <b>MDM Number</b> | <b>MDM Name</b> |
|-------------------|-----------------|
| 0000001           | FF1             |
| 0000010           | FF2             |
| 0000011           | FF3             |
| 0000100           | FF4             |
| 0000101           | FA1             |
| 0000110           | FA2             |
| 0000111           | FA3             |
| 0001000           | FA4             |
| 0001001           | PF1             |
| 0001010           | PF2             |
| 0001011           | LF1             |
| 0001100           | LA1             |
| 0010010           | LM1             |

### **1.3.2.6 Mask**

Bits 33 through 48 of each RTC are used to set each of the bits on the specified MDM card and channel. In a reset command, the MDM will process the mask bits by interpreting any high bits, '1', as a request to drive the equivalent bit on the channel to low '0'. Any bits in the mask that are '0' will make no change to the equivalent bits on the channel. In a set command, any bits in the mask that are set high, '1', will drive the equivalent bits in the channel to high '1'. Just as with the reset command, any bits in the mask that are '0' will make no change to the equivalent bits on the channel.

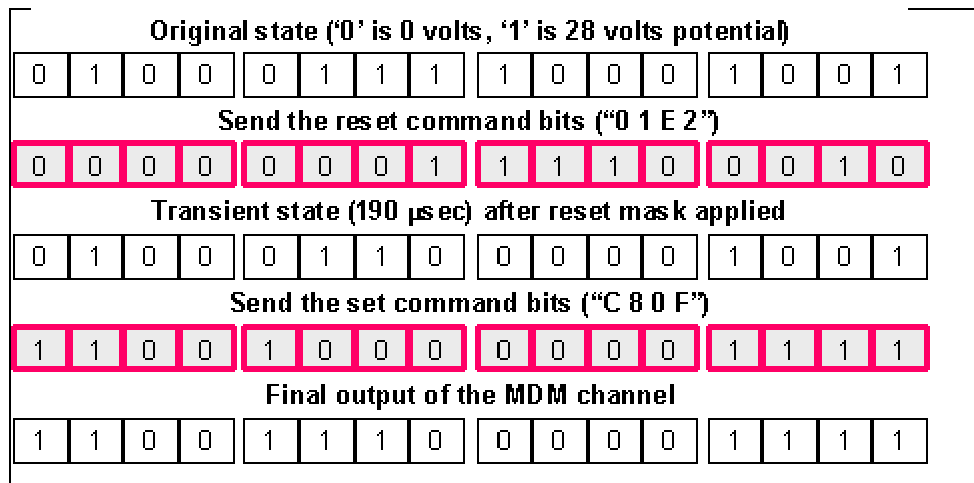
### **1.3.2.7 An Example of an RTC**

To help in the understanding of the contents of an RTC, one command from the generic command server (GCS) was selected. This command is the Abort A On command which turns on a small light in front of the Commanders seat on the flight deck. Figure 1-4 details each bit in the command address.



**Figure 1-4. Example of an RTC**

For the mask part of each command, the process is different. Figure 1-5 is an example of how the reset and set masks affect the actual bits on the 16-bit channel of a card on an MDM. For better demonstration purposes, the mask is different from that shown in Figure 1-4.



**Figure 1-5. Example of Reset/Set Mask Data**

### 1.3.3 Command Loads

A command load is considered to be a command that is processed as a two-stage command. Two-stage commanding is the process by which the command is uplinked to the GPCs. The GPC stores the command data, and sends a copy of it back to the ground. The generic command server (GCS) compares the uplinked command data to the downlinked command data. If the uplinked command is the same as the downlinked command, the GCS will send another command to the GPC to cause it to execute the previously stored command load. Details of the two-stage process are discussed later in the Command Processing section.

There are currently 64 different types of command loads. Although the INCO console position is responsible for the uplink of all the command loads, only those command loads that INCO regularly uses are discussed in this systems brief. Section 6.3 of the Downlist/Uplink Computer Program Development Specification (CPDS) contains the descriptions of all the command loads available for the GNC and SM major functions. Section 3.6.3 of the Program Requirements Design MG038101-30 (PRD) contains the descriptions of the command loads available for the BFS major function.

## 1.4 COMMAND PROCESSING

Each command that is uplinked to the shuttle is processed the same way. First the NSP will receive the command from the uplink source, either the S Band or Ku band system. Next, the NSP will pass the command to the COMSEC for decryption. After the command is decrypted, the NSP will validate the command by comparing the parity bits. Once the NSP has validated the command, it is sent over to a GPC for final command processing and validation before it is sent to the LRU or flight software element. The following sections detail each of the preceding steps.

### 1.4.1 NSP Processing

When the NSP receives the uplink source, it will bit synchronize the data and pass it on to the COMSEC to be processed (if the forward link is encrypted). The COMSEC will then return the decrypted uplink to the NSP. Next, the NSP will separate the uplink voice channels (A/G 1 and 2) and the command channel in the uplink data. The NSP uses the Bose-Chaudhuri-Hocquenghem (BCH) algorithm to determine if the command data uplinked has any bit errors. If it does, the NSP will change the vehicle address in the first 16 bits of the 48-bit command word to "0000". After all this has happened, the NSP sends the processed command data to the GPC for final processing and implementation. The "zeroed out" vehicle address is the only way the GPC will know there was a command bit error detected by the NSP.

#### 1.4.1.1 Bose-Chaudhuri-Hocquenghem (BCH) algorithm

BCH is a method of determining if the 48 bits of command data have been corrupted during uplink. The MCC command server will pass the 48 bits of command data through this algorithm and generate 77 bits of parity. The 48 bits of command and the

77 bits of parity are combined and sent as the uplink command data. The NSP and the COMSEC will separate the original 48 bit command word from the uplinked 77 bit BCH encoded command word. Next both the NSP and COMSEC will generate its own 77 bit BCH code and compare the uplinked 77 bits against the 77 bits that were generated. If the 77 bits are the same the command data is considered to be error free and the command continues through the process of being verified. For a more detailed discussion about BCH see section 13, COMSEC in the INCO Systems Briefs document.

#### **1.4.1.2 COMSEC Processing**

The COMSEC receives the uplink from the NSP. It will decrypt the uplink before it starts to determine if the command data is valid. The COMSEC uses the same BCH algorithm to determine if there are errors in the command data but since the uplinked data was encrypted and time tagged, the process is slightly different than in the NSP. The COMSEC will get the current IRIG-B time from the Master Timing Unit (MTU). This time tag will be used to filter out the time tag in the uplinked command data (called time authentication). After this filtering is done, the COMSEC will complete the BCH test. If the command data passes this test, the data is sent on to the NSP for more processing. If the command data does not pass this test the original command data with time tag is filtered through a second time tag that is 10 seconds older than the first pass. The BCH process is repeated. If the command data passes during the second try, it is passed on to the NSP for further processing. If the command data does not pass the second time through the BCH/time authenticate test, the first 16 bits of the 48-bit command word are "zeroed out". This will guarantee that the command will fail the BCH check in the NSP, which will also make the command fail validity checks in the GPC.

#### **1.4.1.3 NSP Validation Process**

Once the command data and voice channels are returned to the NSP from the COMSEC, the voice channels are stripped off the uplink data so that the command data can be BCH tested again. If the data passes this BCH check it is placed into one of two 10 command word buffers. These buffers are polled by the GPC every 190  $\mu$ sec. The command word buffers are toggled each time the GPC reads one of them so that a new set of command words can be loading while the old set is being read by the GPC. The NSP will verify that each of the 10 - 48 bit command words are non-zero. This information is placed in the NSP validity word, which is sent to the GPC along with the 10-command word buffer.

#### **1.4.2 NSP to GPC Interface**

Once the NSP has processed the command data, it allows this command data to be retrieved by the GPCs. This process is accomplished differently depending on the type of flight software that is active in the GPCs. In order to process command, the GPCs must know which NSP is currently powered, the status of the uplink block switch on panel C3, and whether the command has been validated by the NSP. Only one NSP may be powered on at a time. The following paragraphs explain the different ways that

commands are distributed to the major functions and the processes of statusing the interfaces and the commands along the way.

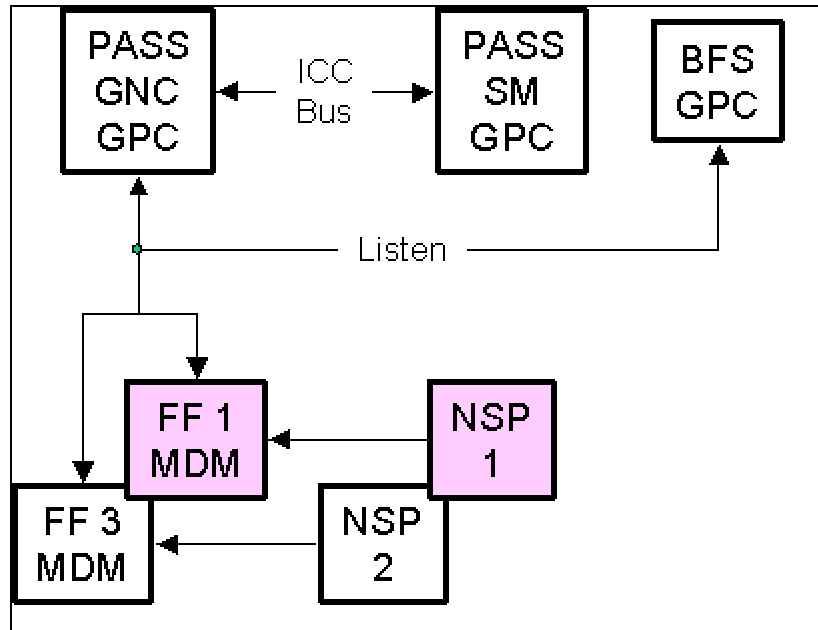
#### **1.4.2.1 BFS Command Path**

BFS acquires commands in two different ways. The BFS computer operates in the “Run” mode the majority of the time. While in this mode the BFS listens to all the Flight Critical strings, PASS input commands, and response words to ensure that the BFS does not directly interact with PASS.

This is done to protect against a BFS failure that could affect the PASS. If the crew has to engage the BFS GPC the PASS computers relinquish control over the FF MDMs, and BFS acquires command data by directly polling the NSPs via the MDMs.

For the BFS to receive data, the BFS “tracks” input/output on the orbiter data buses that are controlled by PASS. By “listening” to these transactions, BFS can “hear” any uplink commands as they are transmitted from the NSP to the PASS GNC GPCs. The PASS GNC GPCs reject the commands with the BFS address; the BFS accepts them and executes them.

This mode of operation causes two major constraints on uplink commanding to BFS pre-engage. First, BFS must be tracking PASS on the proper flight-critical strings. BFS downlists its status as to whether or not it is tracking PASS on flight-critical strings. These data are displayed on several INCO displays, including the INCO ASC/ENT Management and ASC/ENT INST Management. The second major constraint is that the BFS can only track PASS when the PASS GNC computers are in OPS 1 (ascent), OPS 6 (RTLs), or OPS 3 (deorbit/entry). It is impossible to uplink to BFS in other OPS pre-engage. Figure 1-6 shows these relationships.



**Figure 1-6. Command Data Route**

#### 1.4.2.2 SM Command Path

Commands enter the SM major function in a very different way from PASS GNC or BFS major function. Commands are routed to the SM computer via the PASS GNC computer. The GNC major function polls the NSP and collects the uplink command words. If the command destination is the SM major function, the GNC GPC will place the command data on an Inter-Computer Communication (ICC) data bus that links all GPCs. The SM computer retrieves the command data from the GNC major function and processes it accordingly.

#### 1.4.2.3 Power Discrete

When an NSP is powered on, its power discrete is set in the forward load controller assembly (FLC). NSP 1 gets powered through forward FLC 2 while NSP 2 gets powered from forward FLC 3. The FLCs send a signal to flight critical MDMs, which pass the information on to the GNC and/or BFS GPCs. Table 1-6 shows these relationships.

**Table 1-6. NSP Power Discrettes**

| NSP | Power Source | Power Controller | MDM  | Card | Channel |
|-----|--------------|------------------|------|------|---------|
| 1   | Main B       | F LC 2           | FF 1 | 9    | 1       |
| 2   | Main C       | F LC 3           | FF 3 | 2    | 1       |



The systems software in the GPC, maintains the status of which NSP serial data path is currently active (being polled) and which NSP is currently bypassed. When the current NSP has its serial I/O bypassed by the GPC (FDA message “BCE STRG 3(1) NSP”), the GPCs will look to the power discretetes to determine which NSP is powered on. The NSP power discrete that is ON (+28 volts) will be used as the “Current NSP” in the next computer cycle, while the other NSP will be considered the “Alternate NSP”. This process of re-establishing serial I/O polling is called “Upmoding”. This re-starts polling the current NSP without requiring the crew to execute a GNC I/O reset following an GNC Ops transition or an MDM port mode on flight critical strings 1 or 3. INCO Systems Brief 12 describes the NSP upmoding logic as it relates to the power discretetes in more detail.

#### 1.4.2.4 Uplink Block Switch

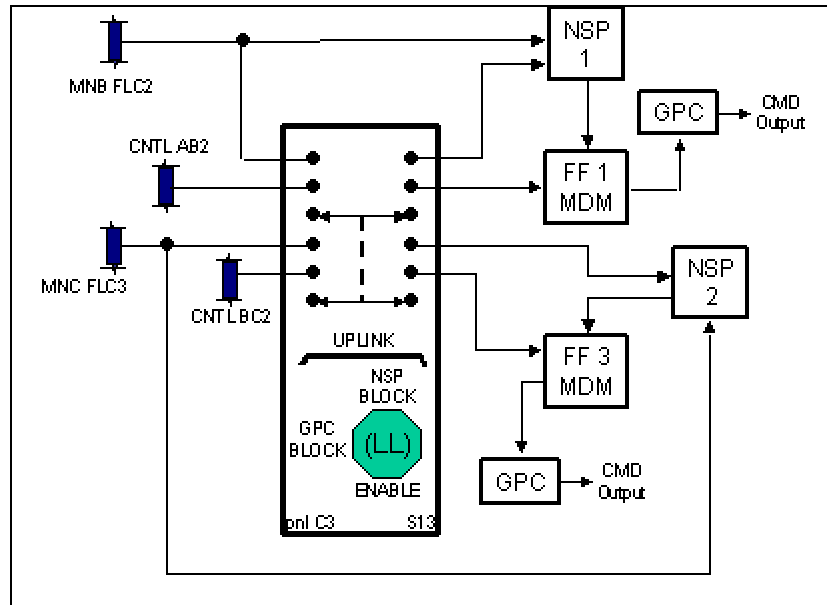
The crew can prevent uplink command processing by using, the Uplink Block switch. This switch has three positions. The bottom position is “ENABLE”. This switch position is not electrically connected to anything, thus allowing the uplink commands to be processed nominally . The middle position of the switch is “GPC BLOCK” which is used to tell the GPC software to not allow commands to be processed and executed. There are 2 discretetes that are added together to determine if the GPC is to not process commands. The first discrete, called “Discrete A” or “GPC UPLINK BLOCK CMD-FF1” is passed through MDM FF1 while “Discrete B” goes through MDM FF3. Both discretetes must be high (+28 volts) before the GPCs will stop processing commands.

**Table 1-7. Uplink Block Discretetes**

| NSP | Nomenclature             | MSID      | MDM  | Card | Channel |
|-----|--------------------------|-----------|------|------|---------|
| 1   | GPC Uplink Block CMD-FF1 | V72K8225X | FF 1 | 4    | 0       |
| 2   | GPC Uplink Block CMD-FF3 | V72K8226X | FF 3 | 4    | 0       |

The top position is “NSP BLOCK”. This switch position is connected directly to the NSP to inhibit all command output and set the “Data Inhibit” bit (PASS V92X6082X, BFS V98X0232X) in the NSP status word. It prevents the GPCs from processing any command data and generates a “BCE STRG X NSP” message. The only way to re-establish the command interface after this has happened is to put the switch back in ENABLE and have the crew perform a “GNC I/O RESET”. Figure 1-7 graphically shows these relationships.

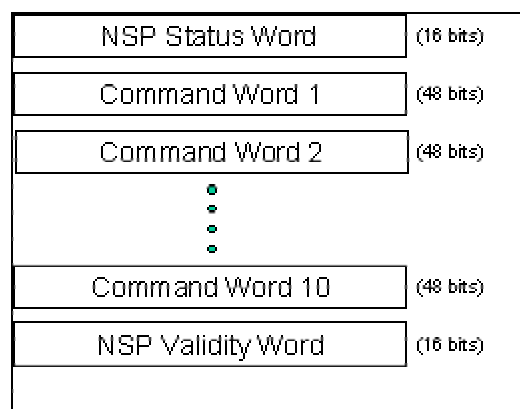
The crew does not normally use the “NSP Block” switch position since it causes an error message. There is more discussion about this topic in INCO Systems Brief 12.



**Figure 1-7. NSP/GPC Interface**

**1.4.2.5 Transaction Data**

Once I/O is established between the NSP and the GPCs via the associated flight critical MDM, data transactions occur every 190  $\mu$ sec. These transactions transfer the status of the NSP, the command data from one of the two NSP command buffers and the indication as to which command buffers are non-zero. This information is vital to the GPC software so that the command data can be processed correctly. Each part of this transaction is discussed in the paragraphs to follow. Figure 1-8 shows the structure of the NSP serial I/O to the GPCs.



**Figure 1-8. NSP Serial I/O Structure**

### 1.4.2.5.1 NSP Status Word

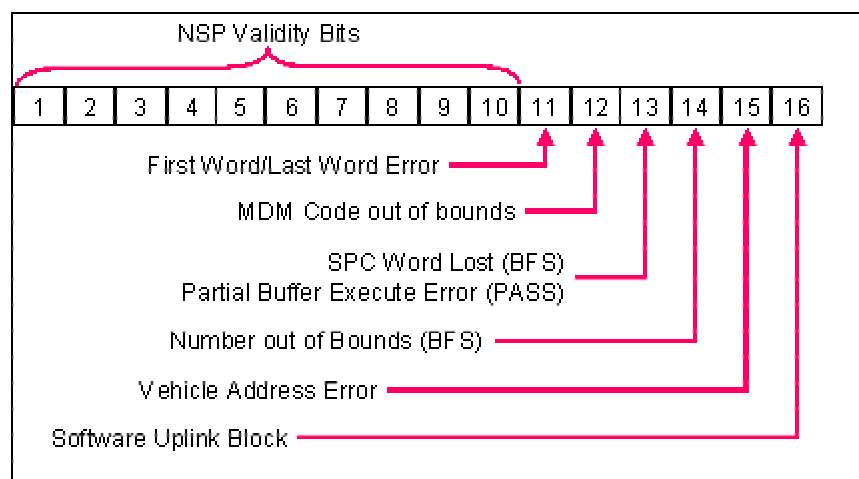
The NSP status word has two bits, which are very important to the GPC flight software. The Data Ready bit (PASS V92X6081X and BFS V98X0231X = 1), which is the first bit of the 16, indicates that at least one of the following 10 command words passed the BCH validity test in the NSP and has a nonzero vehicle address. When the Data Ready bit is set, the flight software in the GPCs examines the ten 48-bit command words and NSP validity word. The Data Inhibit bit (PASS V92X6082X and BFS V98X0230X = 1), which is the second bit of the 16, is set by the NSP when the crew “Uplink” switch on panel C3 is put in “NSP BLOCK”. Discussion of the rest of the NSP status word can be found in INCO Systems Brief 12.

### 1.4.2.5.2 NSP CMD Buffers

All ten of the 48-bit command words in the buffer are transferred to the flight software each transaction cycle. This process must be faster than the NSP can fill the command buffers so that no commands are lost. This results in the maximum command rate of 200  $\mu$ sec.

### 1.4.2.5.3 NSP Validity Word

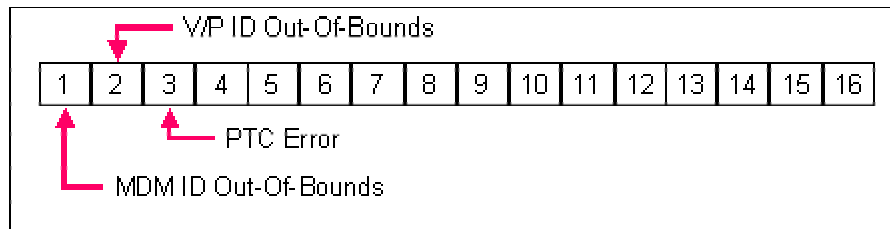
The NSP validity word is 16 bits long (V92M6078PX - GNC, V92M6078PY - SM, V92M6078PZ - Ops 0. V98M0250P - BFS). The first ten bits are set by the NSP, while the last six bits are set by the GPCs. Each of the ten bits set by the NSP corresponds to one of the ten 48-bit command words in the transaction. The NSP identifies nonzero 48-bit command words by a “1” in the appropriate bit in the NSP validity word. Even if a command word is identified by a “1” in the NSP validity, it does not necessarily mean that it is a valid command. It only means that it passed the BCH check and has a nonzero vehicle address. The last six bits are discussed in the GPC Validation Process section of this Systems Brief. Figure 1-9 shows the bits in the NSP validity word along with their function.



**Figure 1-9. NSP Validity Word**

#### 1.4.2.5.4 NSP Validity Word 2

The second NSP validity word (V92M2922P) is an extension of the NSP validity function, which consists entirely of error indicators. Only the first three bits in this 16-bit word are used currently. The details of the first 2 bits are covered in the GPC validation section and the last bit is covered in the Payload Through Put section. Figure 1-10 shows the bits in NSP Val Word 2.



**Figure 1-10. NSP Val Word 2**

### 1.4.3 GPC Processing

After the NSP has completed processing the command data, it places the data into the command buffer from which the GPC will poll the data for its command processing. The GPC flight software will perform a number of checks on the command data. These checks are done to ensure that the information in the command data word is properly assembled and correctly routed. Each major function (GNC, SM, BFS, PL and Ops 0) will downlist its command processing status independently.

The first step after the NSP has made the command data available is for the GPC Flight Computer Operating System (FCOS) to transfer the command data to the vehicle address/Op Code decoder module. This module will validate the command header information and determine how to route the command data inside the GPC software. The following paragraphs discuss the command validation process along with the downlisted indications of command errors, two-stage and single stage command processing, and special processing done for payload related commands.

#### 1.4.3.1 GPC Validation Process

The GPC validation process includes checks on the command header data (first 16 bits of the command word) as well as the information provided by the NSP in the NSP validation word and NSP status word. Each of these validation processes can generate an error condition. These error conditions are explained in Table 1-8 below. If the command is confirmed to be for the major function checking it and the vehicle address is valid, then the commands are forwarded to other command processes.

**Table 1-8. GPC Uplink Validity Bit Definition**

| Name                                  | Bit #     | MSID   | Meaning   |
|---------------------------------------|-----------|--|---|
| GPC Validity Bits                     | Bits 1-10 | V92X6112X - V92X6121X or V98X0201X - V98X0210X | If bit is on, it means that the corresponding command word in the 10-word buffer contained a command word with a nonzero vehicle address.   |
| GPC/Major Function Check              | 11        | V92X6125X or V98X0211X                         | This bit is set when the GPC/MAJOR FUNCTION code in a command word was not a legal code.  |
| Process Skip Flag                     | 12        | V92X6126X or V98X0212X                         | This bit is reset whenever a load has completed processing. It is set when FCOS/BSS determines that a load has not completed processing in an uplink cycle (because of GPC overload or delay in uplink processing caused by GPC errors).  |
| SPC Buffer Full                       | 13        | V92X6128X or V98X0213X                         | Set whenever 25 SPCs are in the buffer (full). Reset whenever an SPC times out or the buffer is cleared.  |
| Illegal Op Code/ Memory Configuration | 14        | V92X6132X or V98X0214X                         | Each uplink is checked prior to processing to verify it is a legal command in the computer processing the load. If it is not a legal command, this bit is set.  |
| Two Stage Error                       | 15        | V92X6134X or V98X0215X                         | If two different OP codes are observed in between a command load with a first word bit set on and a command word with the last word bit set on, this bit will be set and the load rejected. This bit will also be set if more than 33 command data words of uplink are attempted in a single load (67 half words). This is also set if a command word with a zero vehicle address is found as an intermediate word in a two-stage load. |

**Table 1-9. Definition of GPC Bits in the NSP Validity Word**

| Name                       | Bit # | Checked By | MSID                   | Meaning   |
|----------------------------|-------|------------|------------------------|---|
| First Word/Last Word Error | 11    | PASS & BFS | V92X5995X or V98X4270X | Load rejected and this bit set<br>A. If first command word of a load does not have first word bit set on<br>B. If a command load is in progress and command word with a first word bit set on is received prior to a word with the last word bit set on (i.e., start of a new command load prior to end of a previous load) |
| MDM Code Out of Bounds     | 12    | PASS & BFS | V92X5996X or V98X4271X | This bit is set when an Illegal MDM number is found in an RTC or MRTC.  |
| SPC Word Lost              | 13    | BFS only   | V98X4272X              | This bit is set when an attempt is made to load more than 25 SPCs.  |

**Table 1-9. Definition of GPC Bits in the NSP Validity Word (continued)**

| Name                   | Bit # | Checked By | MSID      | Meaning  |
|------------------------|-------|------------|-----------|--|
| Execute Partial Buffer | 13    | PASS only  | V92X5998X | This bit is set when an attempt has been made to execute a two-stage buffer that does not contain a complete load (word with last word bit set on has not been received).  |
| Number Out of Bounds   | 14    | BFS only   | V98X4273X | <p>The following conditions will cause a "Number Out of Bounds" error in the BFS.</p> <ul style="list-style-type: none"> <li>A. An MDM SINGLE, MDM MULTIPLE, or SPC MULTIPLE command load contains an MDM number that is zero or greater than 14.</li> <li>B. The number of command groups in an MDM MULTIPLE or SPC MULTIPLE command load is zero or greater than 10.</li> <li>C. The number of words to be written in a G-MEM CONTIGUOUS command load is zero or greater than 64.</li> <li>D. The starting address of a G-MEM command load, plus the number of words to be written, minus 1, is greater than 33FFF (hex).</li> <li>E. The number of address and word pairs in a G-MEM SCATTER command load is zero or greater than 32.</li> <li>F. A G-MEM SCATTER command load contains a memory address that is greater than 33FFF (hex).</li> <li>G. The number of data sets in a TABLE MAINTENANCE BLOCK UPDATE command load is zero or greater than 10.</li> <li>H. There is an illegal data set type in a TMBU command load.</li> <li>I. There is an illegal parameter interpretation in a TMBU command load.</li> <li>J. A displacement in a TMBU command load exceeds the length of the table for which its data set is intended or causes a full word parameter to be written to an odd address.</li> <li>K. A parameter value in a TMBU command load exceeds the limits specified for its interpretation.</li> </ul> |
|                        |       |            |           | L. The landing site table slot in a DE-ORBIT LANDING SITE PARAMETERS command load is less than 19 or greater than 21   |

**Table 1-9. Definition of GPC Bits in the NSP Validity Word (concluded)**

| Name                         | Bit # | Checked By     | MSID                   | Meaning   |
|------------------------------|-------|----------------|------------------------|---|
|                              |       |                |                        | M. The TACAN table slot ID in a DE-ORBIT TACAN PARAMETERS command load is less than 51 or greater than 60   |
| PTC First Word/Last Word Err | 14    | PASS (SM only) | V92X0308XY             | This bit is set if the first word/last word flags do not agree in the Payload Through Put (PTC) buffer.   |
| Vehicle Address Error        | 15    | PASS & BFS     | V92X5997X or V98X4274X | Vehicle ID in uplink load was not zero and did not agree with I-loaded vehicle ID<br>If uplink load fails BCH code check at NSP, then NSP sets vehicle address to zero. A vehicle address error can then be caused by an RF link dropout causing BCH errors |
| Software Uplink Block        | 16    | PASS & BFS     | V92X6000X              | If the C3 uplink control switch is in GPC block, this bit is set and the GPC rejects all commands although it continues input/output with the NSP   |

**Table 1-10. Definition of GPC Bits in the NSP Validity Word 2**

| Name                      | Bit # | Checked By     | MSID      | Meaning  |
|---------------------------|-------|----------------|-----------|--|
| MDM ID Out of Bounds Flag | 1     | PASS only      | V91X2888X | When an MDM BITE data read command is formatted for output, the MDM address is checked for validity. If the MDM address is not valid, the command will not be processed and this bit is set.                             |
| V/P ID Out of Bounds Flag | 2     | PASS only      | V91X2889X | When an MDM BITE data read command is formatted for output, the variable parameter (V/P) downlist slot is checked for validity. If the V/P slot is not valid the command will not be processed and this bit will be set. |
| PTC Error                 | 3     | PASS (SM only) | V92X1346X | If a PTC command attempting to load more than 67 buffer locations is detected, the load is not transferred to the Payload Through Put application and this bit is set.   |

### 1.4.3.2 Single Stage Commanding

Single stage commands are considered to be real-time commands that are direct outputs to MDMs, command some payload capability (payload throughput commands), or manipulate command applications in the major functions (i.e., buffer execute, buffer clear, command word modify as in word-by-word initiate, SPC clear, TEC clear). This buffer is only 10 commands long by 48 bits per command just like the NSP command buffer.

### **1.4.3.3 Two Stage Commanding**

The two-stage command process is primarily used for commands which have a major impact to the orbiter and must be carefully controlled and monitored. The two-stage process consists of a comparison of the command data words in the GCS, followed by an execute command from the ground to execute the command data words that were stored in the flight software two-stage buffer.

The command data words are first uplinked to the GPC. The GPC software stores the command data words in a two-stage buffer and then a copy to the ground. On the ground, the GCS software compares the uplinked words against the downlisted words. If they are the same, the GCS will uplink a buffer execute command. If the GCS is in automatic mode, this process will be done automatically by the GCS software. If the GCS is configured for manual mode, it will wait for the uplinking console to send the Buffer Execute command. If there is a miscompare between the uplinked and downlinked command data words, the GCS will not send or allow the flight controller to send a Buffer Execute command. In this case an error is generated on the ground (See Ground Command Processing Systems Brief for more details on the two stage process). To clear the onboard two-stage buffer, the uplinking console sends a Buffer Clear command.

#### **1.4.3.3.1 Two Stage Buffer Telemetry**

The two-stage buffer is separate from the single stage buffer. It contains 33, 48 bit command words instead of 10, 48 bit command data words. These command data words are downlinked as 67, 16-bit words. The command header is stripped off all the command data words with the exception of the first one to save space in the downlink. The command data is downlinked to the ground for comparison with the uplinked command words. Each of the major functions in the flight software has a two-stage buffer. The flight controller uplinking a command must be careful to be sure they are commanding to an active major function or they will get a rejection error in the GCS. The following is the table of MSIDs for each of the major functions.



**Table 1-11. Two-Stage Buffer Telemetry**

|             |          | <b>PASS</b> |            |            |
|-------------|----------|-------------|------------|------------|
| <b>BITS</b> | <b>1</b> | <b>16</b>   | <b>32</b>  | <b>48</b>  |
|             | CW 1     | V92U6140C?  | V92U6141C? | V92U6142C? |
|             | CW 2     |             | V92U6143C? | V92U6144C? |
|             | •        |             | •          | •          |
|             | •        |             | •          | •          |
|             | •        |             | •          | •          |
|             | CW 32    |             | V92U6203C? | V92U6204C? |
|             | CW 33    |             | V92U6205C? | V92U6206C? |

NOTE: '?' is replaced by an 'X' for GNC, 'Y' for SM and 'Z' for Ops 0/PL Major functions. MSIDs are continuous from V92U6140 to V92U6206.

| <b>BITS</b> | <b>1</b> | <b>16</b> | <b>32</b> | <b>48</b> |
|-------------|----------|-----------|-----------|-----------|
|             |          |           |           |           |
|             |          |           |           |           |
|             |          |           |           |           |
|             |          |           |           |           |
|             |          |           |           |           |

1.BFS

| <b>BITS</b> | <b>1</b> | <b>16</b> | <b>32</b> | <b>48</b> |
|-------------|----------|-----------|-----------|-----------|
|             | CW 1     | V98U0021C | V98U0022C | V98U0023C |
|             | CW 2     |           | V98U0024C | V98U0025C |
|             | •        |           | •         | •         |
|             | •        |           | •         | •         |
|             | •        |           | •         | •         |
|             | CW 32    |           | V98U0084C | V98U0085C |
|             | CW 33    |           | V98U0086C | V92U0087C |

NOTE: MSIDs are continuous from V98U0021C to V98U0087C.

### 1.4.3.3.2 Two Stage Error Correction

There are two types of two-stage processing errors. The first type occurs when the command uplinked is sent to a major function that does not have a downlist at the moment of uplink. This type of two-stage error is a telemetry reject (TMRJ). The flight controller can uplink a single-stage command to clear the two-stage buffer for this error if the major function is active but just not sending down telemetry in the downlink format that is active. If the major function is not active then no command was processed so there is no command data on-board. The flight controller would simply clear the GCS two-stage process (see the Ground Command Systems Brief for details) with a command terminate command.

The second type of two-stage processing error is a data reject (DREJ). This means the major function is down linking the two-stage buffer data but there was some miscompare between the uplinked data and the down listed data. In the case of a DREJ, the recommended course of action is to clear the two stage buffer and try to re-uplink the command

#### **1.4.3.4 GPC to Software Applications**

All GPC major functions work the same way when it comes to commands intended for an application. When an application Op Code is executed via a two-stage command, the two-stage processor sets the appropriate applications flag. When the Applications Uplink Processor (AUP) sees this flag, it begins to transfer the contents of the two-stage buffer (TSB) to the applications uplink buffer. Once the transfer is complete, the AUP will clear the TSB. This process occurs in under a second.

### **1.5 INCO COMMAND TYPES**

There are many different command types available in the various GPC major functions (see Table 1-3 Op Codes). This section will only discuss those command types that INCO uses.

#### **1.5.1 Table Maintenance Block Update**

Table Maintenance Block Update (TMBU) commands are primarily used to change software limits, enable/inhibit Fault Detection and Annunciation (FDA) messages or change constants in either the SM or BFS flight software.

The TMBU commands contain from 1 to 10 data sets. Each data set contains a data set ID corresponding to the item number of the limit or constant value to be changed, the parameter ID of the value, and the value. The TMBU will be rejected if the load is received while the Table Maintenance (TM) SPEC 60 is active) or if the load contains an illegal number of data sets.

The number of the last data set rejected is downlinked (V92J0660C - TMBU Load Reject Indicator, in the SM only). BFS rejection of a TMBU is indicated by bit 14 (V98X4273X - Number Out of Bounds) being set in the NSP validity word and is described in Table 1-9 above.

If a data set in the TMBU sent to the SM GPC is rejected (V92J0660C = 1 through 10), the possible problems are:

- A. Class 2 limit change is requested and no class 2 limit set is defined for FDA parameter.
- B. Class 0, 3, 4 limit change is requested and no class 0, 3, 4 limits are defined for FDA parameter.
- C. Class 0, 3, 4 limit change is requested and specified limit set does not exist.

- D. Requested change is a high limit and changed parameter is a discrete.
- E. FDA does not process parameter of a limit change.
- F. Analog or engineering units (EU) limit value exceeds allowable range.
- G. Parameter of a constant change is not a constant parameter.

If V92J0660C = 11, the possible problems are

- A. TM spec is active when the load reaches the application.
- B. The number of data sets is less than 1 or greater than 10.

If V92J0660C = 0 then the TMBU was processed properly in the SM GPC.

If SPEC 60 is not active and a TMBU load is received, a discrete parameter is enabled to indicate that TMBU load processing is in progress (V92J0661C - TMBU Load in Progress Flag). The SM processes the entire load within 10 seconds of the time it is received from the uplink software. If TM SPEC 60 is called up while a TMBU uplink is in progress, the load processing continues and all TM SPEC item entries are rejected. The INCO Management display includes an indication that SPEC 60 is active when variable parameter number 4 for the SM is set.

### 1.5.2 Stored Program Command

The Stored Program Command (SPC) allows a RTC to be stored onboard the orbiter to be executed at a specified time. The SPC buffer stores up to 150 sixteen-bit words, which equates to 25 SPCs. This buffer resides in the BFS, PL (not used) and SM software but not in the GNC. The SPC buffer accepts SPC commands from the two-stage processor, which inserts them in unused slots, and then positions the command pointer to the oldest command in the SPC buffer. The TSB EXECUTE command, when received, causes the two-stage processor to begin the preceding process. The SPC processor executes the command data within  $\pm 2$  seconds of the execution time, as specified in SPC. If the time has expired (equal to or less than the current GMT), command is executed immediately once entered in the SPC buffer, commands are time-ordered (based on the execution time associated with each command) by positioning the command pointer to the oldest command.

Once an SPC execution time has expired, the slot is available for storage of another command. The number of active SPCs is maintained and downlisted by the software (MSID V92U6105C for SM and V98J4403C for BFS). The two-stage processor rejects the entire SPC command if there is not enough room in the buffer for the additional SPCs. This rejection is indicated by bit 13 (V92X6128X for GNC or V98X0213X for BFS - SPC Buffer Full) in the GPC Command Validity Word being set. Additionally, bit 13 (V98X4272X - SPC Word Lost) is set in the BFS NSP Validity word (Table 1-9) if an attempt is made to load more than 25 SPCs into the BFS SPC buffer.

### 1.5.2.1 Impacts of Ops Transitions on SPCs

Going through OPS 0, deletes all the SPCs in the SM SPC buffer. This is true for either a keyboard PRO to OPS 0 or repositioning of the GPC mode switch to STANDBY. If SM is transitioned from SM 2 to SM 4 without explicitly going to OPS 0 (OPS 0 PRO) or from SM 4 to SM 2 without explicit OPS 0, then SPCs are retained.

The SPC buffer is cleared upon Initial Program Load (IPL) initialization and on any HALT to STBY/RUN transition to OPS 0, for the BFS. The BFS TSC buffer is also cleared at the same time. If BFS is explicitly moded to OPS 0 (via OPS 0 PRO), SPCs are retained and executed in OPS 0. BFS maintains SPCs during an OPS 1 to OPS 3 or 6 transition.

### 1.5.3 Time Executed Command

Time Executed Commands (TECs) are commands that are equivalent to SPCs in processing except that they will reconfigure a load to be executed at a specified time.. TECs are supported only by the SM major function. When the SM is initialized from mass memory, the TEC buffer is initialized to zero. Additionally, the TEC buffer is reset to zero at OPS transitions. Up to 25 commands can be stored in the TEC buffer at one time. The number of commands in the TEC buffer (V92J1126C - TECs In Storage) and a status indicating a full buffer (V92X1125X - TEC Storage Full) are downlisted from the SM. The SM application is not required to be aware of the data content format internal to those 16-bit words. A TEC buffer clear command exists which will, when received, cause the TEC buffer to be reset to all zeros.

Each command contains the GMT of execution, followed by control and data words. Each part of the TEC is checked for legal values as specified in the Downlink/Uplink Computer Program Development Specifications (CPDS). The SM rejects the command (V92X1124X - Uplink Invalid Request), if any of the fields are invalid. The rejection is downlinked to the ground and displayed onboard. When the next valid TEC is received, the rejection flag is cleared. Once a successful TEC is received, it is placed in the buffer and waits to be executed at the GMT transmitted in the command. The TEC executes within 2 seconds of the GMT in the command unless the SM interface is busy. Once the SM interface is freed up, the TEC is transmitted for execution. If the TEC has an execution time in the past, it executes the command within 2 seconds of receiving it in the SM software.

TECs used to control the antenna management software in the SM computer can command the following capabilities:

- Antenna Radar Range Estimate Auto
- Antenna Radar Range Estimate Minimum
- Ku-Band Antenna Interface Enable
- S-band Auto Antenna Pointing Enable and Inhibit
- TDRS Mode Override
- S-Band Site Select Auto
- S-Band Site Select Next

Ku-Band Channel 1 Spread Spectrum Toggle On/Off  
Ku-Band Channel 1 Self-Test Toggle On/Off  
Ku-Band Channel 1 Forward Link Mode 1 or 2  
Ku-Band Radar Threshold Toggle Variable/Fixed  
Ku-Band Obscuration Override Toggle Off/On  
Ku-Band TWTA Toggle Off/On  
Ku-Band Mask Select  
Ku-Band Modulation On  
Ku-Band Modulation Auto  
Ku-Band Primary Acquisition Mode On/Off  
Ku-Band Inertial Stabilization On/Off  
Auto H/O S-Band to Ku-Band Enable/Inhibit  
Auto H/O Ku-Band to S-Band Enable/Inhibit  
S-Band and Ku-Band TDRS Select TGT-A Prime  
S-Band and Ku-Band TDRS Select TGT-B Prime  
Ku RF Protect Zones 1, 2, 3 and 4 Enable/Inhibit  
TDRS State Vectors 1, 2, 3, 4, 5 and 6 to TGT-A  
TDRS State Vectors 1, 2, 3, 4, 5 and 6 to TGT-B  
TDRS State Vectors 1, 2, 3, 4, 5 and 6 Enable/Inhibit

If the TEC is directed to a payload, it is output from the SM within 2 seconds after the GMT time of execution has occurred and sent to the PSP. If another load transfer to the PSP is in progress when the time of execution occurs, the TEC load is held and output to the PSP after transmission of the current load is completed. If the time of execution occurs when communication with the PSP is disabled, the TEC is rejected (V92X1124X - Uplink Invalid Request).

#### **1.5.4 Telemetry Format Load/Decomutator Format Load**

The Telemetry Format Load/Decom Format Load (TFL/DFL) Op Code is used to request the SM GPC to load the Pulse Code Modulation Master Unit (PCMMU) or Payload Data Interleaver (PDI) with data formatting tables from the Mass Memory Unit (MMU). The command structure includes all the steps (same as item entries the crew would make) for loading a new format ID into either the PCMMU or the PDI. Table 1-12 lists the item entries used to load a TFL or DFL.

**Table 1-12. TFL/DFL item entries**

|                | Description of function  |
|----------------|--|
| 01             | Selects the fixed High Data Rate (HDR) downlink formatter (TFL = 129)  |
| 02             | Selects the programmable HDR downlink formatter. (A TFL must have been loaded into the programmable (soft) formatter before this option should be used)            |
| 03             | Selects a TFL to be loaded into the Low Data Rate (LDR) or HDR formatter. Valid LDR formats are 102 and 103. Valid HDR formats are 128-254                         |
| 04             | Loads the selected TFL into the formatter  |
| 05             | PCMMU I/O reset, resets the bypassed data read tables in the SM GPC so that SM software can start processing data again.   |
| 06, 07         | PSP 1(2) I/O reset, resets the interface between the SM GPC and the PSP.   |
| 08             | PDI I/O reset, re-establishes communications between the SM and the PDI  |
| 09             | Selects the desired PDI decom to be loaded (format, source or both). This function displays a decom number (1 - 4 for decoms and 5 for Fetch Pointer Memory (FPM)) |
| 10             | Selects the format to be loaded into the selected decom. Valid DFLs are 00 - 31. Valid FPMs are 501-525  |
| 11             | Loads the previously selected DFL/FPM  |
| 12             | Selects the input source for the previously selected decom. Valid range is 0 - 6   |
| 13             | Loads the previously selected input source into the previously selected decom  |
| 14, 15, 16, 17 | Toggles the Fault Detection Annunciation (FDA) enable/disable bit for PDI decoms 1, 2, 3, 4  |

MSID V92J0054C is the TFL/DFL load reject indicator. The load reject indicator is a decimal integer used to indicate which data set in the load was rejected. Because the TFL/DFL process checks data sets as it executes them, if an intermediate data set has an error, the sets before it are executed before the error is located. Once the error is detected, the load is rejected from further processing. The TFL/DFL reject indicator can be set for any of the following reasons:

- A. If SPEC 62 is displayed on a crew MDU when the uplink load is initiated, then the uplink load is rejected and the indicator is set to decimal 11.
- B. If a TFL or DFL load is requested in the uplink and the mass memory is busy, the SM common buffer is busy, or a TFL or DFL is currently being executed, the load is rejected and the indicator is set to the number of the data set that was executing when the error was detected.

- C. If the TFL or DFL requested in the load is not in the mass memory directory of TFLs and DFLs contained on the mass memory, then the load is rejected and the load reject indicator is set to the data set that contained the illegal ID.
- D. If the number of data sets (actions) in the load is outside the legal range (0-10), the load is rejected and the load reject indicator is set to decimal 11.
- E. If a function ID in a load is invalid (less than 1 or greater than 17), the load is rejected and the load reject indicator is set to the number of the data set that contained the error.
- F. If a function is addressing a decom (decom format load or source select) and the decom identification number is illegal (less than 1 or greater than 5), the load is rejected and the load reject indicator is set to the number of the data set containing the error.
- G. If the function is attaching a source to a PDI decom and the source is invalid (less than 0 or greater than 6), the load is rejected and the load reject indicator is set to the number of the data set containing the error.
- H. If a TFL or DFL fails to complete successfully because of problems in the Line Replaceable Unit (LRU), data buses, or GPC, the load processing stops and the load reject indicator is set to the data set being executed when the error occurred. The success of the load is determined by a checksum test on a readout of loaded format in the LRU.

### 1.5.5 Payload Throughput Loads

The primary path for processing payload systems commands is the payload throughput application in the SM major function. When a Payload Throughput Command (PTC) Op Code is received, the SM GPC passes the command data to the Payload Throughput Buffer. When the last word of the load is stored in the TSB, the command is pushed out of the buffer and on to the system being commanded. No validation other than standard two-stage buffer loading validation is performed on the PTC data content before the data is transferred to the specific Payload (P/L) destination. The GPC is not required to downlist the PTC data. If the last word is lost because of errors or the incorrect number of words in the load, the load is stopped in the Payload Throughput Buffer (PTB). The load remains in the PTB until a PTC BUFFER CLEAR command is transmitted.

#### 1.5.5.1 PTC Software Rejection Indicators

There are three possible error indications generated from the payload throughput process.

##### First Word/Last Word (FW/LW) Error (V92X0308XY)

This MSID indicates that a PTC command was received but the first command word or the last command word sequence was incorrect. Bit 14 in the SM major function version of the NSP VAL word will be set if the PTC buffer receives a new command

while it is processing the previous command or if the first word or last word indicators contained in each command word (48 bits long) was set in the wrong sequence.

1 = FW/LW error detected

0 = FW/LW accepted

Checksum Error (V92X1141XY)

This MSID indicates that the PTC checksum calculated by the SM does not compare to the checksum value sent as part of the PTC.

1 = Checksum error

0 = Checksum valid

PTC Error (V92X1346XY)

This MSID indicates that the PTC buffer was full when a new command was received. When this happens, bit 3 of NSP VAL word 2 is set.

1 = PTC buffer full

0 = PTC accepted

The only way to view the contents of the PTC buffer is to have DPS designate variable parameter slots, usually allocated to slots 8, 9, and 10. The INCO PTC buffer displays the contents of those slots and the three error flags.

### **1.5.6 PSP Rejection Indicators from Uplinked Commands**

The Payload Signal Processor (PSP) is used to process commands for Orbiter payloads (See INCO Systems Brief 32). Generally these commands are PTCs but there are other ways to command to the payloads that are not PTCs. INCO can send commands to configure the PSP which can cause some of these reject flags. The crew can command via a Payloads SPEC display. INCO can store commands in the TEC buffer, which will go through or to the PSP. The next time a valid command is passed through the PSP, the affected rejection flag is reset. The following table documents the PSP rejection flags that relate to the command processes.



**Table 1-13. PSP Command Reject Flags**

| Name                   | MSID      | Meaning  |
|------------------------|-----------|--|
| PSP Load Reject        | V92X1102X | This bit is set when either a reinitialize command fails or a command that has no data words is set to the PSP.  |
| PSP TEC Reject         | V92X1120X | This bit is set if a TEC to a payload is executed but the PSP cannot process it.   |
| PSP Sequence Reject    | V92X1121X | This bit is only used prelaunch by Test and Checkout System (TCS) software. It is set if the TCS cannot command through the PSP.   |
| Uplink Invalid Request | V92X1124X | <p>The following conditions can be set this bit:</p> <ul style="list-style-type: none"> <li>A. Invalid checksum for PL throughput command to any destination (PSP or SSI).</li> <li>B. PTC intended for the PSP has an invalid number of data words (&gt;64) or an invalid configuration ID (&gt;5).</li> <li>C. PTC to an SSI and the number of words is invalid (&gt;32) or the SSI ID is of invalid range (&gt;7) or not identified for a particular flight.</li> <li>D. PTC sent to an SSI and previous requests to output are not complete. The incomplete requests could have originated from uplink, cargo control specifications (CC SPEC) or TECs.</li> <li>E. PTC with a destination code set to something other than PSP or SSI.</li> <li>F. A PSP OP code in a PTC load with an invalid PSP configuration message ID (&lt;1 or &gt;10).</li> <li>G. TEC with a destination of PSP and the PSP configuration ID is not valid (&lt;1 or &gt;10) or the number of words is invalid (&gt;64).</li> <li>H. TEC with a destination of an SSI and the SSI ID is not valid (&lt;1 or &gt;8), the SSI ID is not valid for the flight, or the number of words is invalid (&lt;1 or &gt;32).</li> </ul> |
|                        |           | <ul style="list-style-type: none"> <li>I. Uplink with SM major function ID but contains an Op Code that is not valid in the SM. This condition would also set the illegal OP code/major function bit in the GPC validity word for the SM computer.</li> </ul>  |

**Table 1-13. PSP Command Reject Flags (concluded)**

| <b>Name</b>          | <b>MSID</b> | <b>Meaning</b>  |
|----------------------|-------------|---|
| PSP Uplink Reject    | V92X1127X   | This bit is set when either an invalid PSP configuration message is sent or if the PTC checksum or syntax checks fail.                    |
| PSP CC SPEC Reject   | V92X1140X   | This bit is set if the crew attempts to command to a PSP from a SPEC when there are no active PSPs.                                       |
| PSP Port Mode Reject | V92X1140X   | This bit is set if the output port (PI or UMB) is not correctly set up after the GCIL command is issued from the SM or G9 major function. |

## **1.6 ON-BOARD COMMANDING**

The crew has the capability to issue Real-Time Commands and in some cases, execute the same operations as uplink loads but this capability is limited. Most of what the crew does is item entries from their displays. The crew does have insight to tell when the ground is sending two stage commands to the orbiter. They also have the capability to inhibit the grounds commands from changing anything on the orbiter. The following sections discuss these capabilities.

### **1.6.1 Uplink Activity Indicator**

The crew can tell when the ground is commanding by checking any of their PASS displays for the uplink activity on flag. This flag is turned on each time the ground uplinks a two-stage command to a PASS major function. The flag will go off as soon as the two-stage command is processed or cleared from the two-stage buffer. The flag is located on the top right area of each GNC or SM display. The ground can turn this indication on by uplinking the “Uplink Activity ON” command. To turn the indicator off, the ground must uplink an “Uplink Activity OFF” command. The BFS does not have this capability.

### **1.6.2 Real-Time Commands via the DPS Utility Spec**

The crew has the capability to send any RTC ( Reset/Set pairs). . They must enter the hexadecimal bit pattern to build the commands on the DPS Utility SPEC (SPEC 001), which is a PASS (GNC & SM) major function only display. The crew cannot send RTCs directly to the BFS major function.

The RTC capability is very valuable for issuing contingency commands to subsystem equipment. If regular requirements exist to control a subsystem via the PL MDMs, it is better to implement this function by an explicit SPEC item entry. Item entries are better because the RTC process requires many manual entries and is prone to error.

In order to use the RTC capability, the DPS UTILITY SPEC (SPEC 001) must be called up on the computer major function that is controlling the MDM for which the command is intended. For example, if a command to a payload MDM is desired and the PL MDMs are being controlled by the SM major function, then the SPEC 001 must be called up on a MDU assigned to the SM major function. RTCs are not exchanged between major functions; so it is important for the user to call up the SPEC under the correct major function. See Figure 1-11 for the DPS UTILITY (SPEC 001) display.

```

XXXX/XXX/XXX      DPS UTILITY      XX X  DDD/HH:MM:SS
                                   DDD/HH:MM:SS

MMU ASSIGN
  1  2
GN&C 1X 2X      PORT ASSIGN
SM 3X 4X        PRI SEC
PL 5X 6X        STRING 1 15X 16X
OPS 0 7X 8X     2 17X 18X
                3 19X 20X
                4 21X 22X
                PL 1/2 23X 24X

MMU STATUS
  1 XXX
  2 XXX
                VAR PARM ID LIST
                25 XXXX
MMU SOURCE/BUS  26 XXXX
GPC/MMU 9X      27 XXXX
MMU/MMU 10X     28 XXXX
GPC/LDB 11X     29 XXXX
                30 XXXX
CKPT RETRV ENA 12X 31 XXXX
                32 XXXX
RTC             33 XXXX
  13 XXXX XXXX 34 XXXX
  CMD 14

                G3 ARCHIVE
                LOAD 48X
                RETRIEVE 49X

                GROUND OPS
                GSE POLL ENA 50X
                SM GSE INH 51X
                SM C/O ENA 52X
                GN&C C/O ENA 53X
                BFC C/O ENA 54X
                ALT PL9 TB 55X

                                   (XX)

                MESSAGE LINE
                SCRATCH PAD LINE
    
```

**Figure 1-11. DPS Utility SPEC Display**

RTC capability does not allow for implementation of command loads such as state vectors. Commands, such as state vectors, can only be entered from the crew keyboard by GPC memory patches. RTC capability only implements the capability to directly address parallel output cards from MDMs.

In order to implement an RTC via SPEC 001, it is important to know these four steps:

- A. Enter the hex for the reset mask (ITEM 13 + XXXXXXXX EXEC)
- B. Execute the reset mask (ITEM 14 EXEC)
- C. Enter the hex for set mask (ITEM 13 + XXXXXXXX EXEC)
- D. Execute the set mask (ITEM 14)

where XXXX XXXX is the hex pattern for the Set or Reset mask. To review the contents of an RTC, go to the earlier section in this brief which discusses this function.

Prior to executing a Set or Reset mask, crew must observe SPEC 001 to verify that the correct mask has been loaded in the computer. Once the ITEM 13 + XXXX XXXX is executed, SPEC 001 displays the accepted XXXX XXXX pattern.

### 1.6.3 Crew Command Inhibits

If the crew does not want commands to be processed on board they have a couple of options available to them. They can block commanding with the Uplink block switch on panel C3 (see [1.4.2.4](#) which discusses this). If they have the SM major function running in a GPC they can simply enter an ITEM 37 EXEC on SPEC 001 from their Integrated Display Processor (IDP) to prevent commands from being processed.

## 1.7 UPLINK ERROR CONDITIONS AND REPONSES

The following conditions break the uplink command path to the Payload MDMs. The responses are assuming NSP 2 is selected prime with NSP 1 as backup (“[ ]” represents the affected LRU if NSP 1 is prime).

### 1.7.1 I/O Error FF3 [FF1]

Uplink data is lost because the FF 3 [FF1] MDM is not accessed by the GPCs. Uplink is not available until either an I/O reset restores the data path to FF 3 [FF1] or (if that action does not recover the MDM) string 3 [string 1 (FF1/FA1)] has I/O established with another GPC.

### 1.7.2 PASS/BFS Sync Is Lost

When this condition exists, the PASS acquired uplink data from FF 3 [FF 1] is not “listened to” by BFS. PASS (GNC) uplink is still available. An I/O RESET to the BFS can be used to reestablish sync. If sync is not recoverable, the BFS may be switched to “standby” so that the payload MDMs can be commanded via the PASS/GNC GPCs.

### 1.7.3 BFS Not Tracking String 3 [1]

When this condition occurs, the same problem as detailed above exists except only one Flight-Critical (FC) string is involved. To recover command, swap to NSP 1 [2] via a Panel/ Command on panel C3.

### 1.7.4 GNC-SM Loss of Common Set Sync

This condition precludes SM from receiving uplink data from the GNC on the ICC buses. Recovery is a difficult procedure. The SM Major Function (MF) must be reestablished from the beginning (usually in another GPC) to reacquire common set sync. During this period, the payload buses must be handed over (known as a restrung) to the GNC GPC(s) for payload MDM commanding. GNC uplink loads are not affected. There is no more automatic antenna pointing so either the crew will be selecting manual antennas or INCO will attempt to command antennas. TECs and/or SPCs will be lost; once the DM major function has be recovered, any TECs and/or SPCs will have to be re-uplinked.

### 1.7.5 Bus Control Element (BCE) String 3 [1] - NSP

Uplink is totally lost while this condition persists. The GPC does not access the NSP SIO channel because of some detected errors. Communication may be regained by use of the I/O reset to GNC. If this action does not clear the problem, NSP 1 [2] must be selected by the crew via the Panel/ Command switch on panel C3..

**Note:** If the problem was internal to the MDM SIO, a faint possibility exists that power cycling of the MDM could recover use of the NSP SIO.

### 1.7.6 On-Orbit SM GPC Fails

The automatic uplink enable/inhibit for on-orbit OPS is initialized to the enable state (ITEM 36 on DPS Utility SPEC 1) at transition to OPS 2. The crew, per their checklist, executes the DPS Utility item 35 entry to select the auto mode. If SM fails after this point, the state of the uplink control is a function of Acquisition of Signal/Loss of Signal (AOS/LOS) period. If the SM GPC failure occurs in an LOS period, the uplink is inhibited because the site-in-view flag is no longer set. The MCC (INCO) ensures that ENABLE ITEM 36 is EXECUTED on the DPS UTILITY SPEC 001 at the next AOS. Until the SM is up again, the uplink has to be controlled via the UPLINK BLOCK switch on panel C3 . If the SM GPC failure occurs in an AOS period, the uplink software is enabled because the site-in-view flag was set. The same procedure as detailed above is used until the SM GPC is recovered.

Uplink control ITEM 36 for enable is selected during deorbit prep since the site-in-view flag is forced to the zero state at SM transition to OPS 00.

## 1.8 COMMAND SYSTEM IDIOSYNCRASIES

The command system has several problems that are documented in Operational Notes and Waivers. These idiosyncrasies are discussed in the following sections along with their associated Discrepancy Report (DR) numbers, if one was created for the problem.

### 1.8.1 Two-Stage Word-by-Word Problems

If a two-stage command is uplinked and the first 16-bit command header word does not get to or is corrupted in the two-stage buffer, a word-by-word command has the capability to update the first buffer location, but the two-stage processing flags are not affected. If this command load is subsequently executed, the PRIMARY uplink software permanently locks up until the system is re-IPL'd. The Mission Control Center (MCC) does not allow uplink of a word-by-word command if the first 16-bit word in the two-stage buffer does not match the uplinked value.

If the error occurred in the last word, it is impossible to correct using a word-by-word command because it is impossible to set the last word flag by word-by-word correction. In this case, a buffer execute command results in rejection of the load and an execute partial buffer telemetry flag being set.

BFS two-stage word-by-word correction is no longer implemented.

### **1.8.2 DEU Equivalent Commands (DR 36329)**

If a DEU Equivalent command is sent to a GPC that is not communicating with the DEU specified in the command, the GPC will process the command, which might lead to undesirable results. DEU Equivalent commands can be issued to a DEU that is powered off. If that DEU is isolated (assigned to GPC 0), any DEU commands that request a new display will not be completed. DEU commands sent to an isolated DEU cannot be dependent on the SPEC display output. The workaround is the user's certainty that the GPC receiving the commands is communicating with the specified DEU. They should also be aware of the status of powered off DEUs. No display related keys should be sent to an isolated DEU.

### **1.8.3 Uplink Error Processing (DR 37553)**

The uplink software detects certain error conditions that result in no indication to the ground that an error occurred or that the command did not execute. A list of those error conditions follows:

- A. A two-stage execute command without the correct FEF0 bit pattern (bits 17-32) is ignored by the uplink software.
- B. An attempt to perform a word-by-word correction of a two-stage buffer position greater than 66 is ignored.
- C. After a valid execution of the two-stage for an application, the two-stage buffer is protected until the appropriate application reads the buffer and makes it available for subsequent uplinks. During the time the buffer is protected, an attempt to re-execute the buffer, clear the buffer, or perform a word-by-word correction of the buffer is ignored.
- D. If an Ops overlay command is attempted with a first/last command word indicator of binary 11, the uplink software ignores the command.
- E. The range of the DEU ID (bits 22-24) and the number of keystrokes (bits 43-48) are checked by the uplink software. If the DEU ID is out of range (0 or greater than 4) or the number of keystrokes is out of range (0 or greater than 30), the DEU equivalent command is ignored.
- F. If there are less than 0 or more than 10 RTCs in an MDM multiple command (MRTC), the command is ignored. No indication is sent to the ground that an error was detected or that the command did not execute.

#### **1.8.4 TM - SPEC vs. Uplink Interaction (DR 37572)**

The table maintenance (TM) display (SPEC 60) and the TMBU via uplink have interlocks defined to prevent interference in each other's updates. The effect of these interlocks is as follows:

- A. If SPEC 60 is active, TMBU loads are rejected, even if SPEC 60 is not on the screen (i.e., overlaid with a display).
- B. If a TMBU load is in progress and SPEC 60 is called, the SPEC comes up, but all keyboard entries are rejected (ILLEGAL ENTRY) until the TMBU load is completed. A TMBU in progress condition can be recognized by a flashing "UPLINK" at the top-center of the SPEC 60 display.

#### **1.8.5 Uplink to RS OPS-000 (DR 43987)**

In the event of an Ops transition failure that causes a default to OPS 0, the only uplink MF/GPC ID option that is valid in the software for such a configuration is the ALL GPC option. This ALL GPC option will pass the MF/GPC ID test for both the primary and backup systems and require additional care to ensure PASS/BFS uplink compatibility, consequently it is safer to re-establish a nominal DPS configuration.

#### **1.8.6 Ku Band/ PTC Overwritten (DR 55064)**

The Ku band/Payload Throughput Commands will be cyclically overwritten if the special processes out is enabled (as indicated by a "blank" next to ITEM 15 on SPEC 64). Execute an ITEM 15 on SPEC 64 prior to sending a Ku band/Payload Throughput Command but be aware that this will inhibit all special processes outputs.

#### **1.8.7 Concatenation of Multiple PTCs (DR 55783)**

Uplink processing of a PTC in which the last 48-bit command word is in error results in the PTC not being passed to the SM uplink processor. Any subsequent PTC uplinked before the PTC buffer is cleared will have its first command word rejected (PTC First/Last word error). Valid intermediate/last command words will be placed in the PTC buffer after the previously uplinked concatenated PTC is passed to the SM uplink processor. The SM uplink processor then rejects the concatenated PTC caused by the PTC first/last word error.

#### **1.8.8 Multiple RTCIO on FC Buses may Jitter HFE I/O (DR 56157)**

Whenever multiple real-time command I/O (RTCIO) requests for the flight critical (FC) buses are made in flight ops, the possibility exists of jittering the start of HFE (high frequency executable) I/O. This is due to the high amount of FC bus contention in these ops. The possibility increases with the number of requests and with increased bus contention due to I/O error processing.

### 1.8.9 PSP Load In G9 Incorrectly Rejected (DR 111692)

The “U/L” symbol is correctly displayed when an uplink PSP command fails, however it is incorrectly displayed when a test and checkout systems (TCS) PSP command is rejected when the PSP is processing another command.

### 1.8.10 MDM Channel Address Anomaly (DR B03934)

BFS uplink software does not check the bits in “Channel Address” fields that are described as “spare” by the requirements specifying the format for MDM Single, MDM Multiple and MDM SPC Multiple command loads. If these spare bits are not set to zero, an MDM BITE status will be set upon execution and the command will have no effect. This condition will be undetectable in the case of MDM single stage commands. MDM multiple and SPC multiple commands with this problem will be available for review through the TSC buffer.

### 1.8.11 BFS Uplink Command Processor (DR B08063)

If an off-nominal two-stage command load is detected by uplink, the TSC ERROR flag is set in the GPC validity word. Once such a condition has been detected, any subsequent “TSC Execute” single stage commands or additional TSC command loads will be rejected until a “TSC Clear” single stage command has been processed.

## 1.9 REFERENCES

- A. Space Shuttle Computer Program Development Specification (CPDS), SS-P-0002-140-OI30, CPN 1, SS Downlist/Uplink Software Requirements. Aug 15, 2003
- B. CPDS, SS-P-0002-580-OI-30, CPN 2, Functional Level Requirements, Systems Management. Feb 27, 2003
- C. Program Notes and Waivers Database (formerly JSC-19320) located at <http://usa1.unitedspacealliance.com/apps/usahou/orgs/6340/pnws/index.cfm>, Last updated Nov. 2003
- D. Backup Flight System (BFS) Systems Management/Special Processing and Payloads Program Requirements Document (PRD), MG038119-30. January 25, 2001
- E. BFS Backup Systems Services PRD, MG038101-30, June 11, 2001
- F. Systems Management Level C Flight Software Requirements, JSC-19590-116, Nov. 2003
- G. SS CPDS SS Systems Level A Software Requirements, SS-P-0002-170, CPN 2, March 12, 2004



THIS PAGE INTENTIONALLY BLANK

## SECTION 2 – GROUND COMMAND SYSTEM DESCRIPTION

### TABLE OF CONTENTS

| Section |   | Page |
|---------|---|------|
| 2.1     | GENERAL .....   | 2-1  |
| 2.2     | GROUND COMMAND SYSTEM OVERVIEW .....                  | 2-1  |
| 2.2.1   | MCC Commands to Orbiter Systems .....                 | 2-1  |
| 2.2.2   | Ku-Band Command Link .....                            | 2-3  |
| 2.2.3   | Remote POCC Commands (via GSFC, JPL, STC, etc.) ..... | 2-3  |
| 2.2.4   | MCC-to-GN Command Link.....                           | 2-3  |
| 2.2.5   | MCC/STC/RTS Command Link.....                         | 2-4  |
| 2.2.6   | MCC/Space Network/SSO Command Link.....               | 2-5  |
| 2.3     | MCC UPLINK COMMAND SYSTEMS.....                       | 2-6  |
| 2.4     | MCC CONSOLES - COMMAND CONFIGURATION FUNCTIONS.....   | 2-9  |
| 2.4.1   | CCM Enable/Disable Button .....                       | 2-9  |
| 2.4.2   | MCC SAFE/OPER Indicator .....                         | 2-10 |
| 2.4.3   | Position Enable/Disable Indicator.....                | 2-10 |
| 2.4.4   | LOAD/RTC Mode Control Button.....                     | 2-10 |
| 2.4.5   | Auto Execute/Manual Execute Modes.....                | 2-10 |
| 2.4.6   | Single-Stage/Two-Stage Modes .....                    | 2-11 |
| 2.4.7   | Auto Retransmission (POCC).....                       | 2-11 |
| 2.4.8   | Major Function ID Button .....                        | 2-11 |
| 2.4.9   | GPC 1-5 and GPC ALL ID Button.....                    | 2-11 |
| 2.4.10  | TEC Buffer Clear Execute Button .....                 | 2-12 |
| 2.4.11  | MDM Address Select Button.....                        | 2-12 |
| 2.4.12  | Display Electronic Unit Address Select Button .....   | 2-12 |
| 2.4.13  | DSM Clear Button.....                                 | 2-13 |
| 2.4.14  | CMD Initiate Button.....                              | 2-13 |
| 2.4.15  | TSB Clear Button.....                                 | 2-13 |
| 2.4.16  | W-x-W Initiate Button .....                           | 2-13 |
| 2.4.17  | Compare Initiate Button.....                          | 2-13 |
| 2.4.18  | Command Terminate Button .....                        | 2-14 |
| 2.4.19  | SPC Buffer Clear Button.....                          | 2-14 |
| 2.4.20  | TSB Execute Button .....                              | 2-14 |
| 2.4.21  | DSM Numerical Buttons (10).....                       | 2-14 |
| 2.5     | MCM.....  | 2-15 |
| 2.6     | SAFEGUARDS TO PREVENT INADVERTENT COMMANDING.....     | 2-16 |
| 2.7     | COMMAND SYSTEM IDIOSYNCRASIES.....                    | 2-16 |
| 2.8     | REFERENCES .....                                      | 2-17 |

## FIGURES

| Figure |                                    | Page |
|--------|------------------------------------|------|
| 2-1    | Command path through the MCC ..... | 2-2  |
| 2-2    | Basic ground network.....          | 2-4  |
| 2-4    | Basic TDRS network .....           | 2-5  |
| 2-6    | Uplink Verify display .....        | 2-6  |
| 2-8    | GCS DSM panel.....                 | 2-9  |
| 2-10   | MCM panel.....                     | 2-15 |

## SECTION 2 GROUND COMMAND SYSTEM DESCRIPTION

### 2.1 GENERAL

The following discussions and descriptions of the Mission Control Center (MCC) command systems are based on MCC Generic Command Subsystems Requirements (JSC-37534) and the MCC Level B and C Requirements for Shuttle (Vol. 1, Book 4, SFOC-FL1278). The displays and functions are subject to change. A description of the orbiter command system can be found in the INCO Systems Briefs, Section 1.

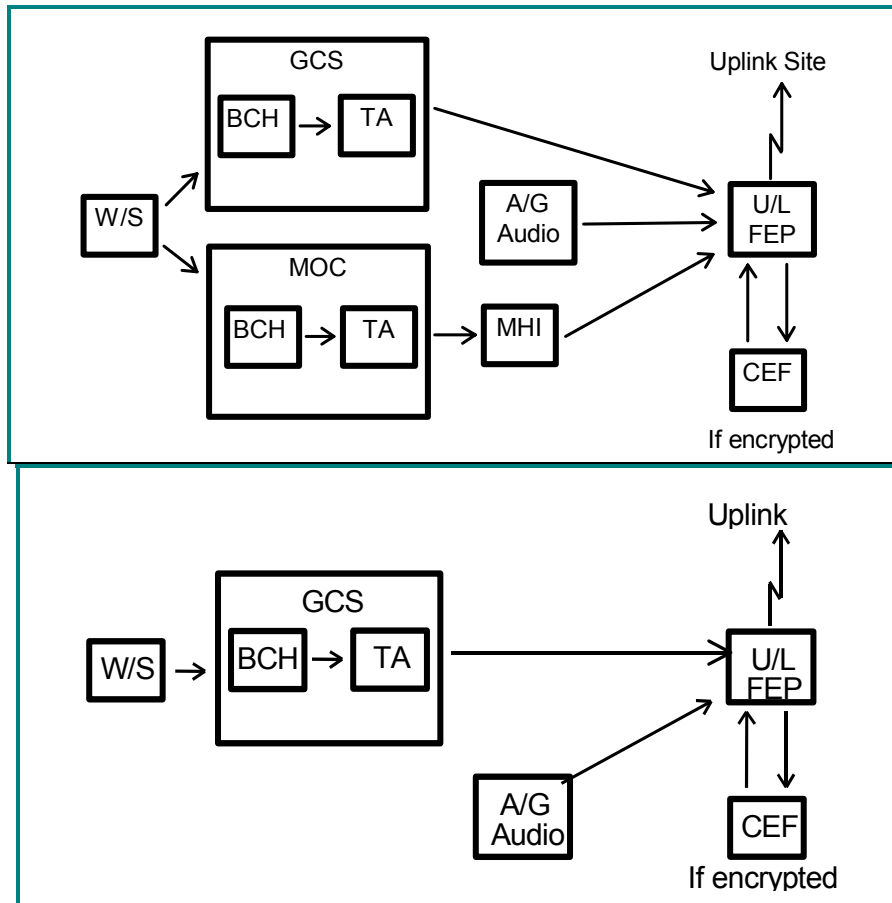
### 2.2 GROUND COMMAND SYSTEM OVERVIEW

The ground command systems are used whenever control of the orbiter or payload systems is required. The ground system will establish communications with the orbiter and the command system via either the S-band or Ku-band path. The ground communicates to the orbiter through the Tracking and Data Relay Satellite (TDRS) System or one of the available ground sites located around the world. The TDRSS network (S-band and Ku-band support) is controlled at White Sands Ground Station (WSGT) and Second TDRS Ground Terminal (STGT) with a remote site at Guam Remote Ground Terminal (GRGT). GRGT is controlled from WSGT. The NASA ground sites (S-band only) are controlled from Goddard Space Flight Center (GSFC) while the Air Force sites (also S-band only) are controlled from the Satellite Test Center (STC) Remote Tracking Station (RTS).

Commands routed to the orbiter command system through one of the above links originate from various Remote Payload Operations Control Centers (POCCs) and JSC MCC command-capable positions. The following discussion details the various paths that commands can take entering the MCC and passing to the uplinking site.

#### 2.2.1 MCC Commands to Orbiter Systems

Orbiter commands are initiated in the MCC by consoles that are configured with a hardware command panel or are running one of the command initiation displays. The console outputs a directive to GCS that verifies that the flight control position is a valid command initiator and that the command received is valid for uplink. The GCS then computes 77 error protection bits that are added to each of the 48 Command Data Words (CDWs) to be uplinked for a total of 128 bits of data. This process is known as Bose, Chaudhuri, and Hocquenghem (BCH) encoding. Once the CDWs are encoded they are exclusive OR'd with 128 bit time word, if necessary. This process is known as Time Authentication (TA). TA is only required on the uplink if the onboard system is set to receive an encrypted command link. After all the augmentation process is completed the command data from the command server are transferred directly to the Uplink Front-End Processor (U/L FEP) for shipment to the assigned uplink point (TDRSS or ground site). Figure 2-1 is the command path through the MCC.



**Figure 2-1. Command path through the MCC**

The U/L FEP Time Division Multiplexes (TDM) commands with digitized Air-to-Ground (A/G) voice and/or Orbital Communications Adapter (OCA) messages. The U/L FEP then outputs the data at a rate of 32 kbs or 72 kbs (S-band) and 72 kbs or 216 kbs (Ku-band) simultaneously to the NASA Communications Network (NASCOM) 2000 via the Consolidated Data Select Switch (CDSS). If the uplink is encrypted, controlled by the COMMAND console position, the U/L FEP will send the uplink data stream to the COMSEC Equipment Facility (CEF). The CEF will return the encrypted data stream to the U/L FEP for shipment to the uplink point.

Onboard, the data stream is routed through the NSP, which, if the onboard systems are set for encrypted uplink, will send the data to the COMSEC decryptor. The attached time word is compared with the GMT from the orbiter Master Timing Unit (MTU). If the ground attached timetag and the GMT from the MTU are not within 10 seconds of each other, the time is not stripped from the command data, and the command is BCH-rejected by the NSP. The primary purpose for this procedure is to further protect the uplink. TA prevents anyone from intercepting, recording an encrypted command, uplinking it at a later time and getting it to execute an onboard function. TA has no effect on A/G voice; the commands may be rejected, but voice continues to be processed.

In all cases the MCC, the ground networks, and the orbiter communications systems must be configured to operate in the same mode and data rate at the same time to establish a complete command loop between the MCC and the orbiter. The MCC must be configured to support the correct flight and vehicle, and the ground networks must be scheduled and told the proper configuration to match the orbiter. Coordination of the onboard and ground systems to maintain communication is the responsibility of INCO and COMMAND. COMMAND is responsible for the configuration and operation of the MCC to shuttle orbiter command system, under the direction of INCO and the Ground Controller (GC). COMMAND is responsible for the reconfiguration and scheduling of the TDRSS service to fulfill telemetry, command, and tracking data requirements. COMMAND monitors the status of the command link and command-related hardware and software and also coordinates troubleshooting of the ground command system and the associated networks.

### **2.2.2 Ku-Band Command Link**

128-kbs commands are routed from the POCC to the MCC via the Internet Protocol (IP) system. The commands are then routed through the CDSS. No validation is performed on the 128-kbs commands. In the U/L FEP, the 128-kbs commands are interleaved with 8-kbs orbiter/payload commands, 64-kbs digital voice (two channels), and 16 kbs sync to make the 216 kbs Ku-band high data rate forward link.

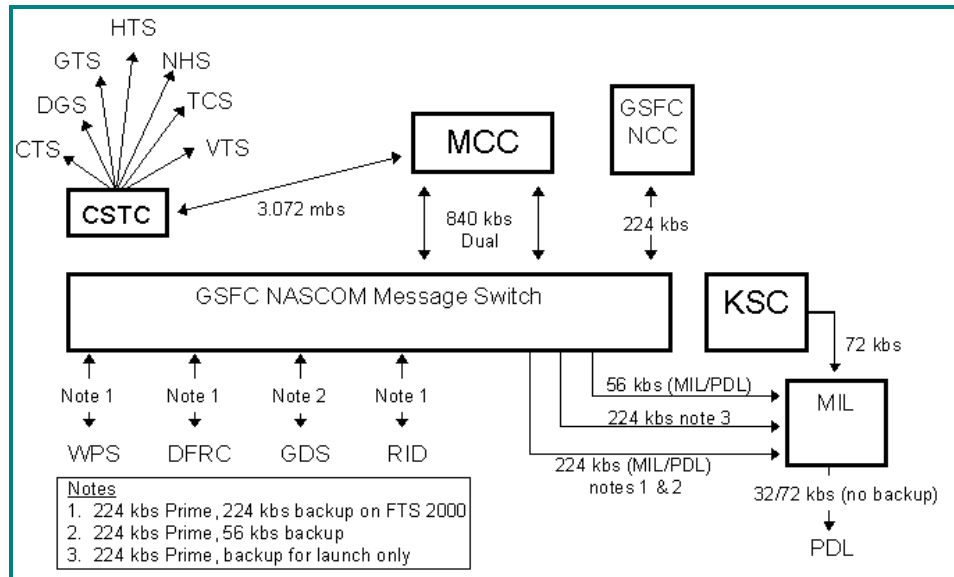
### **2.2.3 Remote POCC Commands (via GSFC, JPL, STC, etc.)**

Normal payload commanding from a remote POCC is received at Johnson Space Center (JSC) via the IP system, processed, and routed through CDSS to the Ground to Ground FEP where it is demultiplexed, and routed to the GCS command application for verification, authorization validation, hazardous command check, and proper destination screening checks. If all checks are properly passed, the GCS reformats the POCC command for orbiter uplink and outputs the payload-addressed command into the normal orbiter command data stream.

### **2.2.4 MCC-to-GN Command Link**

When the uplink data stream is routed to a ground site (GN mode), the U/L FEP output is routed to two redundant data blockers and then to two redundant JSC-GSFC NASCOM-2000 Communications Network interfaces. The best of the two links is selected for use, and the second link is designated as backup. From the NASCOM-2000 interfaces, the command data is manually circuit-switched to route the data over NASCOM-2000 communication lines to the appropriate GN site. The GN site accepts the forward link command data and then uplinks the commands via S-band equipment to the orbiter. Figure 2-2 shows the basic GN.

In the GN throughput mode, uplink composite data from the MCC to the orbiter via the GN sites are output from the U/L FEP at 32 kbs for low data rate and 72 kbs for high data rate. The 8 kbs (6.4 kbs command + 1.6 kbs sync and station ID) of command data are time division multiplexed with one digital voice channel of 24 kbs for low data rate and two digital voice channels of 32 kbs each for high data rate.



**Figure 2-2. Basic ground network**

The communication links between GSFC and the GN sites have bandwidth and line data rate limitations that constrain uplink operations. MILA/PDL, WLPS, and DFRC each have a 224-kbs command line. A constraint in the GN throughput mode is that neither A/G voice nor command modulation originating at the GN can be applied to the uplink S-band Radio Frequency (RF) carrier. This means that all commanding and S-band A/G voice must originate from the MCC U/L FEP with no emergency uplink capability at the GN sites. The non-throughput mode for uplink has been removed from all GN sites.

Refer to the STS NOSP/STDN 601 for current network capabilities and more details on the various modes.

### 2.2.5 MCC/STC/RTS Command Link

Commands from the MCC to the orbiter via the RTS are routed through the Satellite Test Center in Sunnyvale, California. This is a bent-pipe link that operates only in throughput mode. The MCC/STC/RTS command link can be either clear or encrypted. The output from the U/L FEP, digital time division multiplexed data and voice, is routed by the CDSS to the JSC-STC IP system (via GSFC). An alternate path is from GSFC to STC via JPL. The STC Conversion Devices receives the command data from the IP system, then routes it to the STC external switching system. The command stream is then routed to the T1 or Defense Communication Satellite Control Facility Interface (Defense Satellite Information System (DSIS)). DSIS is the prime STC to RTS communication link. From the DSIS equipment at the RTS, the commands are routed to the station data processing computer and then to S-band equipment for uplink to the orbiter. Uplink command echoes are nominally routed from the RTS S-band RF equipment back through DSIS to the STC and then to the JSC U/L FEP decom.

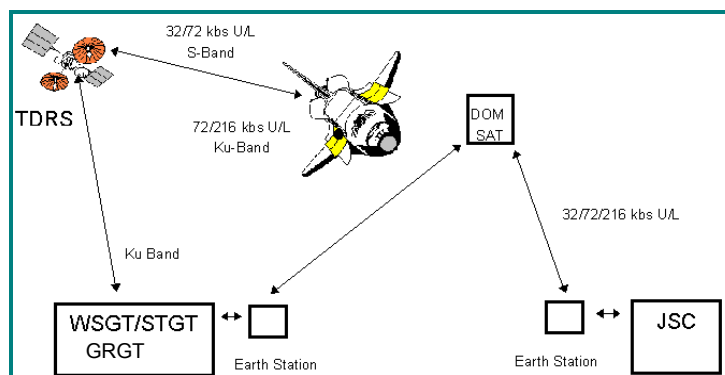
All Air Force RTSs interface with JSC via the Consolidated Space Test Center (CSTC), call sign DICE, located in Sunnyvale, California at Onazuka Air Force Base. The sites all have the same command link data rate capabilities. The following is a list of the Air Force sites:

| Site | Call sign | Capabilities                           |
|------|-----------|--|
| CTS  | PIKE      | One communication link (called a side) |
| DGS  | REEF      | Two sides; both sides have SSP uplink  |
| GTS  | GUAM      | Two sides; only side B has SSP uplink  |
| HTS  | HULA      | Two sides; only side B has SSP uplink  |
| NHS  | BOSS      | Two sides; only side B has SSP uplink  |
| TCS  | LION      | Two sides; both have SSP uplink        |
| TVC  | BEACH     | One side                               |
| VTS  | COOK      | Two sides; only side B has SSP uplink  |

STC has the capability to command payloads (e.g., the Inertial Upper Stage (IUS)) in the orbiter payload bay directly via S-band uplink through the RTS. These commands originate at the STC, bypassing the MCC and the orbiter command system.

### 2.2.6 MCC/Space Network/SSO Command Link

The MCC-to-orbiter command link via WSGT/TDRS/Space Network (SN) also operates in a bent-pipe configuration that functions solely in the throughput mode. The SN operates similar to the MCC/GSFC/GN link in the throughput mode and the MCC/STC/RTS throughput link. Composite command data from the MCC to the orbiter via the TDRS can be uplinked at three data rates. Uplink to the orbiter S-band system via the TDRS network (Figure 2-3) can be at 32 kbs for low data rate and 72 kbs for high data rate. Uplink via TDRS to the orbiter Ku-band system can be at either 72 kbs or 216 kbs if the orbiter is on orbit, the Ku-band antenna is deployed and activated in the communication mode, and there is a line of sight between the Ku-band antenna and TDRS. The link selected for NSP input is shown on the INCO management display as SOURCE S or Ku. Refer to the TDRS Network Operations Support Plan, TNOSP/STDN 602.

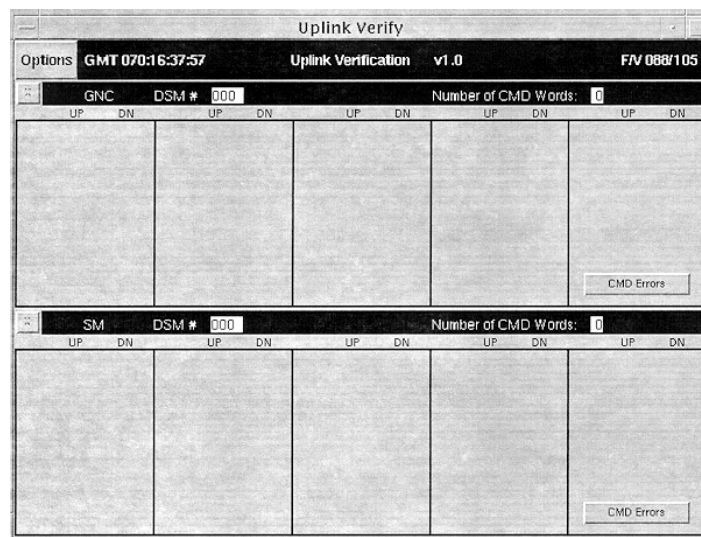


**Figure 2-3. Basic TDRS network**



### 2.3 MCC UPLINK COMMAND SYSTEMS

- A. All commands are assigned DSM numbers for identification and for software accountability. RTCs use a four-digit code, and command loads use a five-digit code. DSM number assignments are under control of Configuration Management and are unique to the JSC command system.
- B. Most command loads are treated as TSCs. An exception to this is a TPC. All RTCs can be sent as SSCs or TSCs.
- C. All TSCs are processed the same as far as auto comparisons and verification indications are concerned. The only user options in two-stage processing are the manual compare/execute mode and the auto compare/execute mode selectable on the command-capable consoles. In the auto compare/execute mode, the ground software compares the transmitted command with the return telemetry of the TSB contents. If the transmitted command and the return readout of the TSB compare, the ground software automatically transmits the TSB EXECUTE command in the auto compare/execute mode. If the command was part of a multicommand (chained) load, the ground software uplinks the next command in the chain and continues this process until completion of all of the commands in the chain. This automatic process stops if a miscompare exists. In the manual execute mode, the operator must transmit the TSB EXECUTE command after a visual compare using the Uplink Verify display (Figure 2-4). The display points out any miscompares between the uplink side and the downlink side by highlighting the line in red.



**Figure 2-4. Uplink Verify display**

There are two types of miscompares possible, as follows:

1. TM RJ - Indicates a failure of the compare routine caused by telemetry dropouts or an absence of telemetry from that GPC MF; e.g., SM downlist. Sending a COMPARE INITIATE from the console after there is a good

telemetry downlink or after the downlist is restored may be all that is required to get a compare and a buffer execute. This function can be performed anytime without doing any harm and can save time rather than doing a Word-by-Word (W-x-W) INITIATE or performing a TSB CLEAR and then reuplinking the command. Telemetry reject is defined as follows:

- a. Two-stage uplink command-initiated and downlink telemetry data are not available or suspect as invalid for comparison.
- b. Compare or W-x-W initiate when downlink telemetry data are not available
- c. Two-stage buffer execute when downlink telemetry data are not available
- d. Two-stage buffer clear when downlink telemetry data are not available

**CAUTION**

**DO NOT EXECUTE A TWO-STAGE COMMAND WITH A TELEMETRY REJECT WITHOUT EXPLICIT FLIGHT DIRECTOR APPROVAL (Flight Rule A11.1.1-22)**

Telemetry reject indicates the contents of the two-stage buffer cannot be verified either good or bad via downlink telemetry. Lack of verification can result from downlink telemetry dropouts, loss of signal, or absence of downlist data from the GPC for such reasons as an incompatible Telemetry Format Load (TFL), e.g., no SM downlist in format 129. Execution of a two-stage buffer without telemetry, "two-stage commanding in the blind," will only be performed for extenuating circumstances. An extenuating circumstance is defined as a case when the chance of possibly executing a bad two-stage command is judged by the Flight Director to be of less risk than not uplinking the command at all. This call is entirely at the discretion of the Flight Director.

2. DATA RJ - Indicates a failure of the compare routine because the uplinked command did not compare with the downlinked command. This is an indication of a data content error in the two-stage buffer. A data reject will most likely result from a noisy or weak forward link while the command is in transmission. It will not result from downlink telemetry dropouts, but in some cases it could be caused by noise hits on the return link. That is why in some cases, a COMPARE INITIATE to force the command system to run the compare routine again is all that is required. If the data reject is sustained after the COMPARE INITIATE, either depress the two-stage buffer clear button or depress the W-x-W initiate button (See the CAUTION on W-x-W). Data reject is defined as follows:
- a. Two-stage uplink command initiate and one or more 16-bit words failed to compare.
  - b. Compare or W-x-W initiate and one or more 16-bit words failed to compare.
  - c. Initiating two-stage buffer clear and one or more words in the onboard downlink buffer failed to clear (reset to zero).
  - d. Initiating two-stage buffer execute and one or more words in the onboard downlink buffer failed to clear (reset to zero).

**CAUTION**

**NEVER EXECUTE A TWO-STAGE COMMAND WITH A DATA REJECT!**

Execution of a bad two-stage command, which is indicated by a data reject, could have severe and unknown consequences including a worst case of loss of crew and/or orbiter. However, if a two-stage command gets a COMPARE and the interactive TWO-STAGE BUFFER EXECUTE command gets a data reject, it is permissible to retransmit BUFFER EXECUTE. The interactive command is a single word RTC that only executes the buffer; it cannot affect the content of the two-stage command resident in the buffer. Standard procedure on a data reject is to clear the buffer and reuplink the command.

- D. The Two-Stage Lockout (TSLO) process is a guard against another command console position commanding to, clearing, or executing an active TSB. TSLO becomes active when a command position initiates a TSC. When a TSC is initiated, the ground software does not allow another command access to the same TSB with a TSC, thus locking it out. If a console operator attempts to access an active TSB, the ground software rejects the input from that console and displays this information on the command track display as TSLO. TSLO processing is not active for TPC single-stage loads. However, this does not mean that someone

uplinking a TPC will not receive a TSLO if the two-stage processor is active. It means that a single-stage TPC in progress does not cause another position to get a TSLO. If a POCC transmits a TPC while the two-stage processor is active, it will receive a Ground Data Reject (GDR) and the following message, "Received POCC input while U/L active (TSLO)."

## 2.4 MCC CONSOLES - COMMAND CONFIGURATION FUNCTIONS

This section provides a functional description of each command configuration utilized to generate and uplink command data by INCO, COMM SUPPORT, DATACOMM, or INSTRUMENTATION. Two primary applications are used to configure and send commands from the MCC. The hardware panel and the software panel are basically identical in functionality; so a discussion of each of the buttons on both panels follows.

### 2.4.1 CCM Enable/Disable Button

The CCM ENABLE/DISABLE button is used to control command initiation from the console. The hardware panel does not have this button. A display associated with the hardware panel has the enable/disable function. The reason the hardware panel does not have this button is to protect the tool from being used while the console is paused. If there was an enable/disable button on the hardware panel, then a user could press it and send commands while the rest of the console was paused. The software panel, on the other hand, has this button on its display. When either the hardware panel display or the software panel buttons are pressed, the ability to uplink commands will be toggled (ENABLED (green) to DISABLED (red)). There is an extra level of disable on the hardware panel. When the hardware panel display button is disabled, the hardware panel does not allow output from the console to the command server at all. This is not true for the software panel. When the software panel CCM button is pressed it only disables output for that position at the command server. Figure 2-5 is the GCS DSM panel.



Figure 2-5. GCS DSM panel

### 2.4.2 MCC SAFE/OPER Indicator

This indicates the state of the MCC command software. MCC safe indicates that the software system is not configured to uplink commands. MCC operate indicates that the MCC command software is properly configured to uplink commands (armed).

The MCC should be safed by COMMAND whenever no commanding is required to prevent erroneous commands from being sent to the orbiter. Operationally, COMMAND only safes/arms the command system when instructed to do so by the Flight Director (via GC).

### 2.4.3 Position Enable/Disable Indicator

The COMMAND controller can enable or disable a console/position from access to the uplink part of the command server. The position enable/disable function should be used if console maintenance is in progress. During LOS periods or times when the console will be unattended, the CCM Enable/Disable button should be used to prevent bad commands from being sent from the panels.

### 2.4.4 LOAD/RTC Mode Control Button

This LOAD/RTC mode button controls the types of execute requests that are made from the panel. The load mode position allows the operator to select a five-digit number from the panel. The RTC mode position allows the operator to select a four-digit RTC number from the panel.

### 2.4.5 Auto Execute/Manual Execute Modes

This button selects the execute mode in which TSCs are to be uplinked.

TSCs transmitted in the auto execute mode or manual execute mode are verified by the ground system automatically by comparing the transmitted command data and the downlisted telemetry of the contents of the TSB. If the auto execute mode is selected and the uplink and downlink compare, the ground command application software in the command server automatically transmits the TSB EXECUTE command. If manual execute mode is selected, the operator must transmit the BUFFER EXECUTE command by depressing the TSB EXECUTE button. The operator should always verify a good compare of the uplinked command and the downlink of the TSB contents before a manual execute.

When a multicommand (chained) load is transmitted in the auto execute mode, it will be automatically compared. If the compare is valid, the BUFFER EXECUTE command is automatically transmitted. When the BUFFER EXECUTE command is verified, the next command in the chain is automatically uplinked, and the sequence continued until all the commands in the chain are transmitted. In the manual execute mode, the operator must transmit another command, such as TWO-STAGE BUFFER EXECUTE or TWO-STAGE BUFFER CLEAR, to complete/continue the sequence.

The two-stage uplink buffer/downlink Telemetry (TLM) verification time delay is fixed at 3 seconds at the initialization of the command server. This means that a 3-second time delay between the two-stage uplink initiate and downlink TLM verification is established before a count of five compare cycles starts. This time delay is variable from 1 to 9 seconds. INCO can request COMMAND to adjust the delay time if required. Refer to MOH, Vol. III, SOP 6.2 for details and procedures.

#### **2.4.6 Single-Stage/Two-Stage Modes**

This button identifies to the ground software the mode in which the command is to be uplinked, single-stage or two-stage. The ground software attaches the applicable OP code identifier to the uplinked command. The OP code identifier routes the command to either the SSB or TSB, as applicable.

This mode is applicable to any command that is prestored as a single-stage command. Commands that are stored as loads are generally configured for two-stage uplink. This button does not affect those commands. This button should normally be left in the single-stage position until the operator desires to uplink an RTC two-stage.

#### **2.4.7 Auto Retransmission (POCC)**

There is no button available on any of the INCO command panels for this capability since it is only used by Payloads to support retransmission of POCC commands. The following discussion is included here for completeness. While in two-stage mode, automatic retransmission is valid for either the manual or auto execute mode. When the automatic retransmission mode has been selected for a POCC command uplink, the software automatically retransmits the entire command a maximum of three times if the downlink verification indicates a non-compare; i.e., data reject. A TWO-STAGE BUFFER CLEAR command is automatically uplinked after each non-compare prior to retransmission. This PBI is only valid for POCC commands.

#### **2.4.8 Major Function ID Button**

This button toggles through the available major functions. The major functions selectable by INCO/RFCOMM/DATACOMM/INST are: SM, GNC, BFS and P/L. The P/L MF is not an MF normally selected by INCO/COMM/ INST, even though it is on the standard panel. P/L is used only for MMU read/write commands that must be done while in P/L 9.

#### **2.4.9 GPC 1-5 and GPC ALL ID Button**

This button toggles through the available GPC selections. The GPCs selectable by the INCO/RFCOMM/DATACOMM/INST are GPCs 1, 2, 3, 4, or 5. The GPC ALL position transmits all commands to all active GPCs. To use these GPC select functions, the operator must use the manual compare routine. GPC ALL is the only method of commanding to a redundant set. GPC must be used when commanding to a computer in OPS 0 since there is no MF in OPS 0.

**CAUTION****SELECTION OF A SINGLE GPC NUMBER CAN RESULT IN A REDUNDANT SET SPLIT**

Selection of a single GPC is ILLEGAL if it is a member of a redundant set. The onboard uplink software tests GPC number codes versus redundant set status. Coordinate with Data Processing System (DPS) or Avionics flight controller prior to uplink to a single GPC number. Reference the NSTS Downlink/Uplink CPDS.

Selection of a single GPC number and GPC ALL is ILLEGAL for two-stage OPERATIONAL CODES (OP CODES) greater than 05 DECIMAL (0000101 BINARY), except for OP CODE 55 DECIMAL (0110111 BINARY). The execute for these codes is also ILLEGAL. Reference the NSTS Downlink/Uplink CPDS.

**2.4.10 TEC Buffer Clear Execute Button**

The TEC buffer clear button is illuminated when the console is enabled. The TEC buffer clear button initiates a command which clears the TEC buffer in the SM major function.

**2.4.11 MDM Address Select Button**

This button selects either the prime or secondary RTC data set field in the command server RTC inventory. Each RTC/DSM has two data fields. Procedurally, MDM PF1 data are located in the MDM 1 field, and MDM PF2 data are located in the MDM 2 field. If no data are stored in the MDM 2 location, the MDM 1 data field is used for both MDM 1 and MDM 2. Presently, only the orbiter Ground Control Interface Logic (GCIL) commands have two data sets. The GCIL commands have location 1 loaded with the MDM PF1 address and location 2, with the MDM PF2 address. All other RTCs have data stored only in the MDM 1 location.

**2.4.12 Display Electronic Unit Address Select Button**

This button selects the Display Electronic Unit (DEU) address ID of the DEU that is being commanded through. This addressing information is required in the uplink command format for all DEU equivalent loads. The ground is prohibited procedurally from uplinking DEU equivalents that would cause OPS transitions or major mode changes. DEU equivalent loads always require crew coordination. Refer to FCOH, Vol. 1, Section 3.

The DEU equivalent command capability allows the MCC to emulate any DEU command available to the crew via the DEU. The DEU equivalent load is fixed length, consisting of six 48-bit command words. They are valid to the GNC, SM, and OPS 0. There is no DEU equivalent command capability to the BFS or P/L. Serious errors can result from incorrect DEU uplink configuration or procedures. Reference the INCO Onboard Command System Brief for idiosyncrasies concerning DEU equivalents.

### 2.4.13 DSM Clear Button

The function of this button is to clear selected DSM numbers that appear in the DSM number window on the panel. The hardware panel uses this button to indicate a problem with the command that is selected. This button blinks if the command is safed or does not exist in the command server. The software panel does not have the same feature. Safed commands show up as red characters for the DSM number and title while no-existent commands show up as red characters for the DSM number with no title.

### 2.4.14 CMD Initiate Button

This button is illuminated if the console is command-uplink-enabled. The depression of the CMD INIT button is used to initiate loads or RTCs that have been "dialed in." If the console is not uplink-enabled, the button is grayed out. Pressing it does not initiate a command uplink.

### 2.4.15 TSB Clear Button

The TSB clear button is illuminated when the console is command-uplink-enabled. The TSB clear button initiates a command to the orbiter vehicle that clears the contents of the TSB of the addressed onboard computer. Another command console cannot clear an active TSB or command to it unless the console that initiated the TSC executes the TSB, clears the TSB, or does a command terminate.

### 2.4.16 W-x-W Initiate Button

This button is illuminated if the console is command-uplink-enabled, if a TSC has been transmitted, if command word number 1 is good, and if a miscompare is in the TSB. The depression of this illuminated button retransmits those words that did not compare. The retransmission corrects only the words that had a miscompare, beginning with the first word with a miscompare, rather than the entire command. This function is not valid for the interactive commands for buffer clear or buffer execute that did not compare. The operator may repeat as many W-x-W corrections as necessary to obtain a valid compare. If there are many miscompares, W-x-W can be more time consuming than doing a TSB clear and replinking the entire command. However, if there are a lot of dropouts in the data, the W-x-W may be preferable because it might increase the chances of getting the entire load onboard. The miscompares can be identified by viewing the uplink verify display. Ground software is incapable of generating a W-x-W command for TPCs or any command to the BFS major function.

### 2.4.17 Compare Initiate Button

This button is illuminated when the console is command-uplink-enabled. If the W-x-W INITIATE button is illuminated, the depression of this button from the same console reinitiates only the ground software comparison routine. If there was a miscompare because of a dropout in the downlink telemetry and the red compare is successful, the load may be executed either automatically or manually. Neither the command nor any



of the words in the command will be retransmitted as a result of depressing the compare initiate button. This function is only valid from the console that initiated the command.

#### 2.4.18 Command Terminate Button

The command terminate button is illuminated when the console is command-uplink-enabled. The command terminate button only terminates the ground two-stage processing and terminates any ground processing associated with a TSC initiated from the same console; i.e., auto compare. Command terminate will stop an auto execute from being transmitted if it is initiated before the ground TSB compare routine is complete.

#### **CAUTION**

#### **DO NOT DEPRESS COMMAND TERMINATE UNTIL THE ORBITER TWO-STAGE BUFFER IS VERIFIED CLEAR**

The COMMAND TERMINATE PBI should not be depressed until the TWO-STAGE BUFFER is verified clear because it releases the command system two-stage process. Another console could then inadvertently execute a bad command. If COMMAND TERMINATE is used to stop execution of a command in progress, it should be followed immediately by a TWO-STAGE BUFFER CLEAR.

#### 2.4.19 SPC Buffer Clear Button

The SPC buffer clear button is illuminated when the console is command-uplink-enabled. The SPC buffer clear button initiates a command that clears the orbiter SPC buffer of the major function that is addressed (SM or BFS). This command clears out all commands in the buffer that are awaiting execution, resets the buffer to all zeros, and requests that the command server clear the ground displays that show what commands are stored onboard (GCS - command buffers).

#### 2.4.20 TSB Execute Button

The TSB execute button is illuminated when the console is command-uplink-enabled. The TSB button initiates a command that transmits the contents of the orbiter TSB to the vehicle system addressed by the TSC.

#### 2.4.21 DSM Numerical Buttons (10)

These buttons (0 through 9) are used to dial up the required DSM numbers for either the RTC or load desired. The readout of this code appears in the DSM window upon depressing these buttons. On the software panel the title is also displayed.

## 2.5 MCM

The MCM (Figure 2-6) is a panel with the capability of eight field select buttons that can select between two fields on each button. Each field provides 24 buttons to be used for either RTC or load transmission. Therefore, this panel provides a total of 360 RTCs or loads. Generally, load fields are broken up into predefined load types, and RTC fields are separated into categories related to subsystems. However, loads and RTCs can be combined on the same field. These functions are permission defined.



**Figure 2-6. MCM panel**

In order to transmit commands from this panel, the following configuration must exist:

- A. Console is position-enabled.
- B. CCM is in the enable mode.
- C. Proper field on the MCM is selected.
- D. Desired button is depressed.

The RTC mode on the DSM panel does not have to be selected to transmit an RTC from the MCM nor does the load mode on the DSM panel have to be selected to transmit a load from the MCM.

If two-stage is selected on the DSM panel, an RTC transmitted from the MCM is uplinked two-stage; but, if single-stage is selected on the DSM panel, a load transmitted from the MCM is still uplinked two-stage. The single-stage/two-stage button on the DSM panel is usually left in single-stage so that RTCs can be sent single-stage from the MCM.

## 2.6 SAFEGUARDS TO PREVENT INADVERTENT COMMANDING

Extreme care should be given to prevent inadvertent uplinking of commands. The following precautions can be used to reduce the chance of inadvertent commanding:

- A. Request COMMAND to safe MCC commanding if no commands should be uplinked from MCC.
- B. Request COMMAND to disable the console for commanding if no commands are to be transmitted from that console for an extended period of time.
- C. Disable console commanding by depressing CCM ENABLE/DISABLE button on the DSM panel when not actively involved in commanding or uplink activity is not imminent.
- D. If a console is to be left unattended for a short time, CCM DISABLE the console. If the console is to be left unattended for an extended period or maintenance work is to be informed on the console, request COMMAND to disable the console and verify the console is disabled.
- E. If two flight controllers share a common command panel, these controllers should use extreme care to verify the other operator has not changed the configuration prior to sending each command. These controllers will advise each other when changing the Major Function (MF) or the Multiple Command Module (MCM) field selects.
- F. Clear all buildable loads, such as State Vectors, P/L Data Loads, SPCs and TMBUs, if those commands are no longer needed for uplink. State Vectors or other critical commands stored in the command server but not currently needed for uplink must be SAFED to prevent unauthorized or inadvertent uplink. Inadvertent uplink could result from confusion or a DSM number incorrectly dialed by a flight controller. COMMAND performs all safing and unsafing at the request of the flight controllers.
- G. Be careful of objects above the command panels that could fall on the panel and inadvertently send a command.

## 2.7 COMMAND SYSTEM IDIOSYNCRASIES

Some of the command idiosyncrasies are listed in the Onboard Command System brief, SB 1. Command operators should refer to these notes, the OI Program Notes (see references), and INCO Console Handbook Procedures for more specific information on commanding, such as building and storing commands, executing commands, safing, command restrictions, etc. Command operators should review all DRs, program notes, operational notes and waivers, and command system idiosyncrasies on the appropriate software load prior to each Shuttle mission.

## 2.8 REFERENCES

A list of references used in research for this brief and a partial list of documents that can provide additional or detailed information on the STS Command System follows.

1. Command Guidelines for STS Customers, JSC-19943.
2. Mission Control Center Generic Command Subsystem Requirements, JSC-37534.
3. MCC Level B and C Requirements for Shuttle, Vol. 1, Book 4, SFOC-FL1278
4. Flight Control Modules Workbook, Ground Systems User Tool, UT CMD 2102.
5. Flight Control Operations Handbook (FCOH), JSC-12808, Vol. I, Sec. 3, Command.
6. Ground Data Flow Textbook, Network Overview 202.
7. INCO/COMM Console Handbook, SCP 3.110, Command
8. INCO/COMM System Brief, Vol. I, SB 1, Onboard Command System.
9. MCC Operations Handbook (MOH), Vol. II, Section 1, Command.
10. MCC Operations Handbook (MOH), Vol. III, Section 6, Command.
11. MCC Operations Handbook (MOH), Vol. IV, Section 1, Command Anomalies.
12. Network Operations Support Plan for the Space Transportation System (NOSP), STDN No. 601/STS.
13. Shuttle Orbiter Computer Program Development Specification (CPDS), SS-P-0002-140, Vol. I, Book 4, Downlist/Uplink Software Requirements.
14. Shuttle Orbiter Computer Program Development Specification (CPDS), SS-P-0002-1701, Level A Software Requirements.
15. Shuttle Orbiter Computer Program Development Specification (CPDS), Vol. V, book 1, OFT Functional (Level B) Requirements, GNC.
16. Shuttle Orbiter Computer Program Development Specification (CPDS), SS-P-0002-530, Vol. V, Book 3, SM Functional Level Requirements.
17. Shuttle Orbiter Computer Program Development Specification (CPDS), SS-P-0002-540, Vol. V, Book 4, SM Detail Level Requirements.
18. Shuttle Orbiter Computer Program Development Specification (CPDS), SS-P-0002-580G, Vol. V, Book 8, SM Level B Software Requirements.
19. TDRS Network Operations Support Plan for the Space Transportation System (TNOSP), STDN no. 602/STS.

THIS PAGE INTENTIONALLY BLANK

## SECTION 3 – S-BAND PHASE MODULATION SYSTEM

### CONTENTS

| Section |  | Page |
|---------|--|------|
| 3.1     | GENERAL .....                                    | 3-1  |
| 3.2     | SYSTEM CAPABILITIES.....                         | 3-1  |
| 3.2.1   | Major Components .....                           | 3-1  |
| 3.2.2   | S-Band PM Frequencies.....                       | 3-2  |
| 3.2.3   | Data Rates and Formats.....                      | 3-3  |
| 3.2.4   | S-Band Modes and Modulation Techniques.....      | 3-5  |
| 3.2.5   | Mode Controls .....                              | 3-9  |
| 3.2.6   | S-Band System Command Control.....               | 3-12 |
| 3.2.7   | S-Band PM Switched Beam Antenna System .....     | 3-13 |
| 3.2.8   | Circuit Margins.....                             | 3-19 |
| 3.3     | SYSTEM OPERATING CONSTRAINTS .....               | 3-19 |
| 3.3.1   | Equipment Warmup.....                            | 3-20 |
| 3.3.2   | System Switching Transients.....                 | 3-21 |
| 3.3.3   | RF Hot Switching .....                           | 3-21 |
| 3.3.4   | S-Band PM System Acquisition Time .....          | 3-22 |
| 3.3.5   | Problems Modes or Commands .....                 | 3-23 |
| 3.4     | SYSTEM MONITORING.....                           | 3-24 |
| 3.4.1   | Special TM Computations.....                     | 3-24 |
| 3.5     | SYSTEMS MANAGEMENT (SM) .....                    | 3-26 |
| 3.6     | S-BAND EQUIPMENT (LRU) NOTES .....               | 3-26 |
| 3.6.1   | S-Band Transponder .....                         | 3-26 |
| 3.6.2   | Network Signal Processor .....                   | 3-30 |
| 3.6.3   | NSP COMSEC.....                                  | 3-35 |
| 3.7     | S-BAND PM SYSTEM COMMAND LIST.....               | 3-35 |
| 3.7.1   | Miscellaneous MRTC's .....                       | 3-35 |
| 3.7.2   | S-Band Transponder LRU .....                     | 3-37 |
| 3.7.3   | S-Band Preamplifier .....                        | 3-39 |
| 3.7.4   | S-Band Power Amplifier.....                      | 3-40 |
| 3.7.5   | S-Band Network Signal Processor.....             | 3-40 |
| 3.8     | S-BAND PM TELEMETRY LIST.....                    | 3-42 |
| 3.8.1   | Antenna Switch and Switch Beam Electronics ..... | 3-42 |
| 3.8.2   | Switch Beam Antenna .....                        | 3-42 |
| 3.8.3   | Transponder .....                                | 3-43 |
| 3.8.4   | Preamplifier .....                               | 3-44 |
| 3.8.5   | Power Amplifier Configuration .....              | 3-44 |
| 3.8.6   | NSP Configuration.....                           | 3-45 |
| 3.8.7   | NSP/COMSEC Configuration .....                   | 3-50 |
| 3.8.8   | COMSEC Equipment.....                            | 3-51 |

| <b>Section</b> |                                   | <b>Page</b> |
|----------------|-----------------------------------|-------------|
| 3.9            | SM 076 COMM DISPLAY .....         | 3-55        |
| 3.9.1          | SM 076 Display Text .....         | 3-57        |
| 3.9.2          | Logic Type/MSID.....              | 3-58        |
| 3.10           | SM 2011 ANTENNA DISPLAY.....      | 3-60        |
| 3.10.1         | Item Entries.....                 | 3-62        |
| 3.10.2         | SM 2011 Antenna Display Text..... | 3-63        |

## TABLES

| Table |   | Page |
|-------|---|------|
| 3-1   | S-Band PM Frequencies.....                  | 3-2  |
| 3-2   | S-Band PM forward link modes .....          | 3-6  |
| 3-3   | S-Band PM return link modes.....            | 3-7  |
| 3-4   | Ranging modulation sequence .....           | 3-8  |
| 3-5   | S-band mode controls .....                  | 3-10 |
| 3-6   | GCIL only command fail states.....          | 3-12 |
| 3-7   | S-Band PM GCIL Mode (SALVO) commands .....  | 3-14 |
| 3-8   | S-Band PM system circuit margins .....      | 3-19 |
| 3-9   | Preamp dc power (watts).....                | 3-20 |
| 3-10  | Mode parity check.....                      | 3-50 |
| 3-11  | COMSEC quiescent states of status TLM ..... | 3-54 |
| 3-12  | SM 076 COMM display text .....              | 3-57 |
| 3-13  | SM 2011 antenna display text .....          | 3-63 |

## FIGURES

| Figure |   |      |
|--------|---|------|
| 3-1    | S-Band PM controls.....                               | 3-11 |
| 3-2    | S-Band PM quad (SW beam) antenna location.....        | 3-15 |
| 3-3    | Antenna pattern $\theta/\phi$ coordinate system ..... | 3-16 |
| 3-4    | Switch beam antenna composite 2106.4 MHz .....        | 3-17 |
| 3-5    | Switch beam antenna composite 2287.5 MHz .....        | 3-17 |
| 3-6    | Switch beam antenna composite 2041.9 MHz .....        | 3-18 |
| 3-7    | Switch beam antenna composite 2217.5 MHz .....        | 3-18 |
| 3-8    | Receiver RF acquisition algorithm .....               | 3-28 |
| 3-9    | Spread spectrum processor acquisition algorithm.....  | 3-31 |
| 3-10   | NSP SIO data flow.....                                | 3-33 |
| 3-11   | NSP output message format .....                       | 3-34 |
| 3-12   | SPEC 76.....  | 3-56 |
| 3-13   | SPEC 2011.....  | 3-60 |



THIS PAGE INTENTIONALLY BLANK

## SECTION 3 S-BAND PHASE MODULATION SYSTEM

### 3.1 GENERAL

The S-band Phase Modulation (PM) system provides forward link voice, command, and ranging, and return link voice, telemetry, and ranging between the Space Shuttle Orbiter (SSO) and the ground station or Tracking and Data Relay Satellite (TDRS).

The system has three basic modes for communication between the SSO and flight controllers. The TDRS mode is provided to give increased coverage through the use of two geosynchronous TDRSs. The Spaceflight Tracking and Data Network (STDN) mode provides communications through the STDN sites, and the Space-To-Ground Link System (SGLS) mode provides communications with the Air Force Satellite Control Facility (AFSCF).

### 3.2 SYSTEM CAPABILITIES

This section provides data and information relative to the operational capabilities of the system, such as modes, data rates, circuit margins, controls, antenna coverage, and equipment.

#### 3.2.1 Major Components

The electronic units are called Line Replaceable Units (LRUs) and are replaced in the SSO at the box level. The following LRUs make up the S-band PM system:

- Four quad switch beam antennas
- Antenna switch electronics 1 and 2 (1 LRU)
- Switchbeam control assembly 1 and 2 (1 LRU)
- Preamplifier 1 and 2 (1 LRU)
- Power amplifier 1 and 2 (1 LRU)
- Transponders 1 and 2 (2 LRUs)
- Network signal processor 1 and 2 (2 LRUs)
- COMSEC 1 and 2 (2 LRUs)
- Ground control interface logic (1 LRU)

**3.2.2 S-Band PM Frequencies**

Table 3-1 presents the transponder operating frequencies.

**Table 3-1. S-Band PM Frequencies**

| Mode | Freq | RCV (MHz) | XMIT/RCV ratio | XMIT (MHz) |
|------|------|-----------|----------------|------------|
| SGLS | Low  | 1775.733  | 256/205        | 2217.5     |
|      | High | 1831.787  | 256/205        | 2287.5     |
| STDN | Low  | 2041.947  | 240/221        | 2217.5     |
|      | High | 2106.406  | 240/221        | 2287.5     |
| TDRS | Low  | 2041.947  | 240/221        | 2217.5     |
|      | High | 2106.406  | 240/221        | 2287.5     |

Receive frequency times XMIT/RCV ratio equals transmit frequency in coherent mode. Transmit frequency shown is for noncoherent mode and center frequency in coherent mode.

### 3.2.3 Data Rates and Formats

#### 3.2.3.1 Forward Link

a. NSP Inputs

S-band 32/72 (uncoded)/96/216 kbps (coded)  
 Ku-band 32/72 kbps (uncoded)  
 GSE 32/72 (uncoded)/96/216 kbps (coded)

b. 48-bit command format built in command server before Bose, Chaudhuri, and Hocquenghen (BCH) encoding

VVV = 3-bit Vehicle Address  
 MMMM = 4-bit Major Function designator  
 OOOOOOO = 7-bit OP Code  
 F = 1-bit First Word designator  
 L = 1-bit Last Word designator

|     |      |         |   |   |                     |
|-----|------|---------|---|---|---------------------|
| VVV | MMMM | OOOOOOO | F | L | 32-bit command data |
|-----|------|---------|---|---|---------------------|

c. Next step in command server: BCH encoded command

FFF = 3 fill data bits

|     |                |                    |
|-----|----------------|--------------------|
| FFF | 48-bit command | 77 BCH parity bits |
|-----|----------------|--------------------|

128 bit command frame = 4 words X 32 bit words

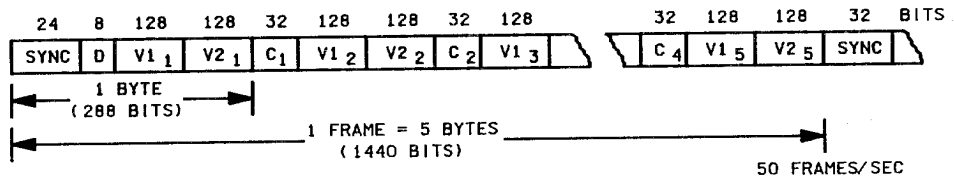
d. Time authentication (TA) completes command server processing

128 bits representing current GMT, rounded down to last 10 second mark, are exclusive OR'ed with the 128 ffbits BCH encoded command frame. Example of exclusive OR TA (16-bit):

|                     |             |
|---------------------|-------------|
| 1000 0110 1011 1101 | CMD DATA    |
| 1101 1000 1110 0001 | GMT DATA    |
| 0101 1110 0101 1100 | CMD WITH TA |

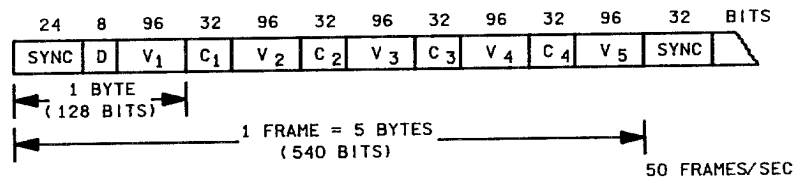
e. Uncoded data multiplexed in the Uplink front-end processor (FEP)

HIGH DATA RATE = TWO VOICE CHANNELS (2 X 32 KBPS) + COMMAND CHANNEL (8 KBPS) = 72 KBPS



|                   |   |                  |
|-------------------|---|------------------|
| STATION ID (D)    | = 8 BITS/BYTE                                   | = 0.4 KBPS       |
| FRAME SYNC (SYNC) | = 24 BITS/BYTE X 1 BYTE/FRAME X 50 FRAMES/SEC   | = 1.2 KBPS       |
| VOICE NO. 1 (V1)  | = 128 BITS/BYTE X 5 BYTES/FRAME X 50 FRAMES/SEC | = 32.0 KBPS      |
| VOICE NO. 2 (V2)  | = 128 BITS/BYTE X 5 BYTES/FRAME X 50 FRAMES/SEC | = 32.0 KBPS      |
| COMMAND (C)       | = 32 BITS/BYTE X 4 BYTES/FRAME X 50 FRAMES/SEC  | = 6.4 KBPS       |
|                   |   | <u>72.0 KBPS</u> |

LOW DATA RATE = 1 VOICE CHANNEL (24 KBPS) + COMMAND CHANNEL (8 KBPS) = 32 KBPS

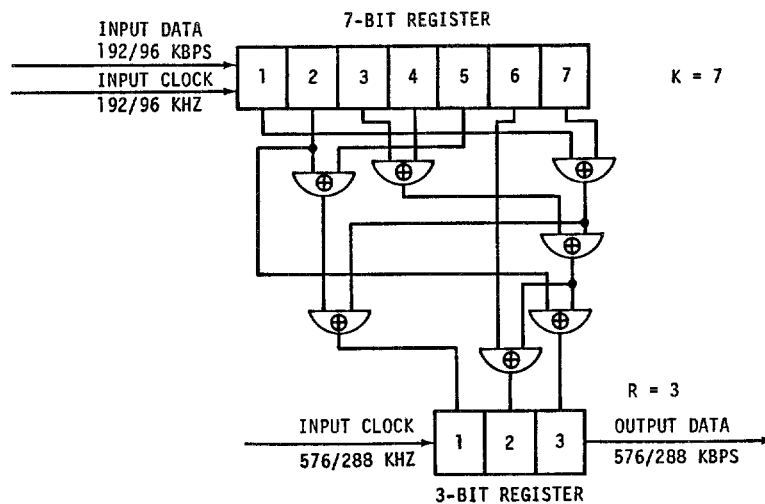


|                   |  |                  |
|-------------------|--|------------------|
| STATION ID (D)    | = 8 BITS/BYTE                                  | = 0.4 KBPS       |
| FRAME SYNC (SYNC) | = 24 BITS/BYTE X 1 BYTE/FRAME X 50 FRAMES/SEC  | = 1.2 KBPS       |
| VOICE (V)         | = 96 BITS/BYTE X 5 BYTES/FRAME X 50 FRAMES/SEC | = 24.0 KBPS      |
| COMMAND (C)       | = 32 BITS/BYTE X 4 BYTES/FRAME X 50 FRAMES/SEC | = 6.4 KBPS       |
|                   |  | <u>32.0 KBPS</u> |

If no command is available for uplink from the server, the FEP will substitute unauthenticated fill data for the 128 bit command frame. Encryption occurs after TA but before convolutional encoding. For encryption bypass mode, TA must be disabled in the server.

f. Convolutional Encoding applied at the site if required

3 X Uncoded Data Rate

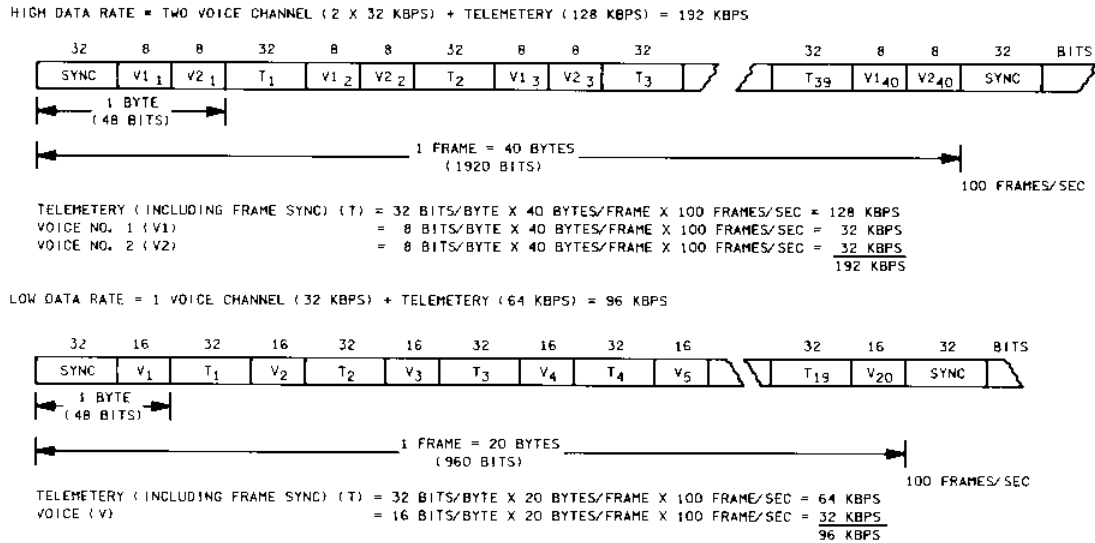


3.2.3.2 Return Link

a. NSP Outputs

S-band 96/192 (uncoded)/288/576 kbps (coded)  
 Ku-band 96/192 kbps (uncoded)/288/576 kbps (coded)  
 GSE 96/192 (uncoded)/288/576 kbps (coded)  
 Recorder 96/192 kbps (DOD)  
 192 (data + voice)/128 kbps (data only)

b. Uncoded data



3704. ART, 2

c. Convolutional encoded data

3 X uncoded data rate

3.2.4 S-Band Modes and Modulation Techniques

Table 3-2 and Table 3-3 present the S-band PM forward and return link modes, the information on each channel, and the modulation technique used, including the type, modulation index, data rate, data format, and subcarriers.

The ranging channel is always enabled in the standard 447X STDN and SGLS SALVO commands, but due to lack of supporting equipment at “most” ground sites the Ranging Off command is additionally sent to improve the forward and reverse link data circuit margin by approximately 3.7 dB. Currently, only MILA supports the Ranging Subcarrier.

**Table 3-2. S-Band PM forward link modes**

| Forward link mode no.  |                      | 00<br>OFF   | 01<br>①   | 02<br>①<br>( 24 L ) | 03<br>①<br>( 24 L )                | 04<br>( 25 L )                     | 05<br>( 25 H )                            |   |  |
|--|----------------------|-------------|---|---------------------|------------------------------------|------------------------------------|---|---|--|
| PM<br>forward<br>modes   | STDN<br>SGLS         | Channel     | No<br>carrier   | Carrier<br>only     | Carrier<br>1 voice<br>CMD<br>(LDR) | Carrier<br>2 voice<br>CMD<br>(HDR) | Carrier<br>1 voice<br>CMD<br>RNG<br>(LDR) | Carrier<br>2 voice<br>CMD<br>RNG<br>(HDR) |  |
|  | TDRS                 | Mode<br>no. | F00   | F01                 | F02                                | F03                                |   |   |  |
|  |                      | Channel     | No<br>carrier   | Carrier<br>only     | Carrier<br>1 voice<br>CMD<br>(LDR) | Carrier<br>2 voice<br>CMD<br>(HDR) |   |   |  |
| PM<br>FWD<br>link<br>modulation  | STDN<br>SGLS         | ②<br>③      | PSK (1.57 rad) B1φ-L 32 KBPS LDR OR 72 KBPS HDR TDM ONLY<br>PM (1.1 rad) B1φ-L 32 KBPS LDR OR 72 KBPS HDR TDM WITH TONE RNG<br>PM/PM (1.0 rad) RNG 1.7 MHz SC with (0.6 rad) 500-kHz, 20-kHz, 4-kHz, 800-Hz, 160-Hz, 40-Hz, and 10-Hz tones |                     |                                    |                                    |   |   |  |
|  | TDRS<br>(SPD<br>SPC) |             | PSK (1.57 rad) B1φ-L 96 kbps LDR coded or 216 kbps HDR coded<br>PN code: Rate = 11.232 Mbps, Length = 2047 Bits NRZ-L<br>Coding: Sub bits (V) = 3, constraint length (K) = 7  |                     |                                    |                                    |   |   |  |
| ① The Ranging Subcarrier is removed from forward link<br>② PM (1.3 rad) for launch phase HDR with coding<br>③ Only one minor tone XMIT with major tone (500 kHz) for major tone phase delay resolution |                      |             |   |                     |                                    |                                    |   |   |  |

**Table 3-3. S-Band PM return link modes**

| Return link mode no.   |              |             | 00  | 01<br>①         | 02<br>①                            | 03<br>①                            | 04  | 05  |  |
|--|--------------|-------------|---|-----------------|------------------------------------|------------------------------------|---|---|--|
| PM<br>return<br>link<br>modes  | STDN<br>SGLS | Channel     | No<br>carrier   | Carrier<br>only | Carrier<br>1 voice<br>TLM<br>(LDR) | Carrier<br>2 voice<br>TLM<br>(HDR) | Carrier<br>1 voice<br>TLM<br>RNG<br>(LDR) | Carrier<br>2 voice<br>TLM<br>RNG<br>(HDR) |  |
|  | TDRS         | Mode<br>no. | R00   | R01             | R02                                | R03                                |   |   |  |
|  |              | Channel     | No<br>carrier   | Carrier<br>only | Carrier<br>1 voice<br>TLM<br>(LDR) | Carrier<br>2 voice<br>TLM<br>(HDR) |   |   |  |
| PM<br>return<br>link<br>modulation   | STDN<br>SGLS | ②           | PM (0.55 rad) B $\phi$ -L 96 kbps LDR or 192 kbps HDR TDM<br>PM (0.55 rad) B $\phi$ -L 96 kbps LDR or 192 kbps HDR TDM with tone rng<br>PM/PM RNG (0.9 rad) 1.7 MHz SC with (0.6 rad) 500-kHz, 20-kHz, 4-kHz,<br>800-Hz, 160-Hz, 40-Hz, and 10-Hz tones |                 |                                    |                                    |   |   |  |
|  | TDRS         | P<br>S<br>K | (1.57 rad) B $\phi$ -L 288 kbps LDR coded or 576 kbps HDR coded   |                 |                                    |                                    |   |   |  |
| ① Ranging in SSO cannot be disabled in STDN/SGLS modes. Modulation is removed from forward link in these modes |              |             |   |                 |                                    |                                    |   |   |  |
| ② Only one minor tone transmitted with major tone (500 kHz) for major tone phase delay resolution              |              |             |   |                 |                                    |                                    |   |   |  |



The ranging tones are transmitted to the SSO via a 1.7 MHz subcarrier. The major tone (500-kHz) phase modulates the subcarrier continuously during ranging operations with a modulation index of  $0.3 \pm 0.03$  radians. During range ambiguity resolution, the minor tone complement additionally phase modulates ( $0.3 \pm 0.03$  radians) the subcarrier.

Table 3-4 presents the ranging modulation sequence.

**Table 3-4. Ranging modulation sequence**

| Seq step   | Tones phase modulated on 1.7-MHz subcarrier  | Seq step | Tones phase modulated on 1.7-MHz subcarrier  |
|--|--|----------|--|
| 1  | 500 kHz major tone   | 6        | 500 kHz major tone<br>4 kHz minor tone   |
| 2  | 500 kHz major tone<br>100 kHz major tone   |          | (The 4-kHz minor tone is modulated by a 160-Hz tone using Double Sideband Suppressed Carrier (DSBSC) modulation) |
| 3  | 500 kHz major tone<br>20 kHz minor tone  | 7        | 500 kHz major tone<br>4 kHz minor tone   |
| 4  | 500 kHz major tone<br>4 kHz minor tone   |          | (The 4-kHz minor tone is modulated by a 40-Hz tone using DSBSC modulation)                                       |
| 5  | 500 kHz major tone<br>4 kHz minor tone   | 8        | 500 kHz major tone<br>4 kHz minor tone   |
|  | (The 4-kHz minor tone is modulated by an 800-Hz tone using Upper Single Sideband Suppressed Carrier (USSBSC)) modulation with the lower sideband filtered so that it is 20 dB down.) |          | (The 4-kHz minor tone is modulated by a 10-Hz tone using DSBSC modulation)                                       |
|  |  | 9        | 500 kHz major tone   |
| Reference: ICD 2-0D004, JSC/GSFC Space Shuttle RF Communications and Tracking. |  |          |  |

### 3.2.5 Mode Controls

Table 3-5 presents all S-band Radio Frequency (RF) and Network Signal Processor (NSP) controls for the S-band PM modes shown.

Switch positions shown in brackets designate the backup or alternate switch position which may be used. Switches are identified by their Switch Number (SXX) on the indicated panel. Ground Control Interface Logic (GCIL) functions are identified by GCIL in brackets (GCIL) in the switch no./GCIL row. Figure 3-1 shows the orbiter control switches for the S-band PM system.

Table 3-5. S-band mode controls

| SWITCH/<br>CMD TITLE    | S-BAND PM   |                         |                       |                       |                 |                 |                       | NETWORK SIG PROC   |                    |                    |                    |                         |                               |                          |                           |
|-------------------------|---|-------------------------|-----------------------|-----------------------|-----------------|-----------------|-----------------------|--------------------|--------------------|--------------------|--------------------|-------------------------|-------------------------------|--------------------------|---------------------------|
|                         | MODE  | R/L DATA<br>ENABLE<br>③ | RANGING<br>③          | SPREAD<br>SPECTRUM    | PM<br>FREQ      | XPNDR           | FAIL<br>SAFE          | DATA RATE          |                    | CODING             |                    | ENCRYPTION              |                               | NSP1<br>T-ZERO<br>UMB ON | NSP 2<br>T-ZERO<br>UMB ON |
|                         |   |                         |                       |                       |                 |                 |                       | XMIT               | RCV                | XMIT               | RCV                | MODE                    | SELECT                        |                          |                           |
| SWITCH/CMD<br>POSITIONS | SGLS<br>STDN LO<br>STDN HI<br>TDRS DATA<br>TDRS RNG | ENABLE<br><br>DISABLE   | ENABLE<br><br>DISABLE | ENABLE<br><br>DISABLE | HIGH<br><br>LOW | XPND<br><br>RCV | ENABLE<br><br>DISABLE | HIGH<br><br>LOW    | HIGH<br><br>LOW    | ON<br><br>OFF      | ON<br><br>OFF      | ALL<br><br>SELECT       | T/R<br><br>RCV<br><br>BY PASS | ON<br><br>OFF            | ON<br><br>OFF             |
| PNL (SWNO./GCIL)        | A1L(S6)   | A1L(S6)                 | A1L(S6)               | (GCIL)                | (GCIL)          | (GCIL)          | (GCIL)                | A1L(S18)           | A1L(S19)           | A1L(S21)           | A1L(S22)           | A1L(S25)                | A1L(S26)                      | (MDM)                    | (MDM)                     |
| M SGLS                  | SGLS  | ENABLE                  | ENABLE                | DISABLE<br>④          | HIGH<br>(LOW)   | XPND            | DISABLE               | HIGH               | HIGH               | OFF                | OFF                | AS<br>REQ<br>FOR<br>FLT | AS<br>REQ<br>FOR<br>FLT       | OFF                      | OFF                       |
| O STDN LO               | STND LO   | ENABLE                  | ENABLE<br>③           | DISABLE<br>④          | HIGH<br>(LOW)   | XPND            | DISABLE               | HIGH               | HIGH               | OFF                | OFF                |                         |                               | OFF                      | OFF                       |
| D STDN HI               | STND HI   | ENABLE                  | ENABLE<br>③           | DISABLE<br>④          | HIGH<br>(LOW)   | XPND            | DISABLE               | HIGH               | HIGH               | OFF                | OFF                |                         |                               | OFF                      | OFF                       |
| E TDRS DATA             | TDRS<br>DATA  | ENABLE                  | DISABLE<br>③          | ENABLE                | HIGH<br>(LOW)   | XPND            | DISABLE               | LOW                | LOW                | ON                 | ON                 |                         |                               | OFF                      | OFF                       |
| TDRS RNG                | TDRS<br>DATA  | ENABLE                  | ENABLE                | ENABLE                | HIGH<br>(LOW)   | XPND            | DISABLE               | LOW                | LOW                | ON                 | ON                 |                         |                               |                          |                           |
| GSE                     | N/A   | N/A                     | N/A                   | N/A                   | N/A             | N/A             | N/A                   | HIGH<br>(LOW)      | HIGH<br>(LOW)      | (ON)<br>OFF        | (ON)<br>OFF        |                         |                               |                          |                           |
| ②<br>GCIL FAIL          | SWITCH<br>POSITION                                  | SWITCH<br>POSITION      | SWITCH<br>POSITION    | ENABLE                | HIGH            | XPND            | DISABLE               | SWITCH<br>POSITION | SWITCH<br>POSITION | SWITCH<br>POSITION | SWITCH<br>POSITION | N/A                     | N/A                           | N/A                      | N/A                       |

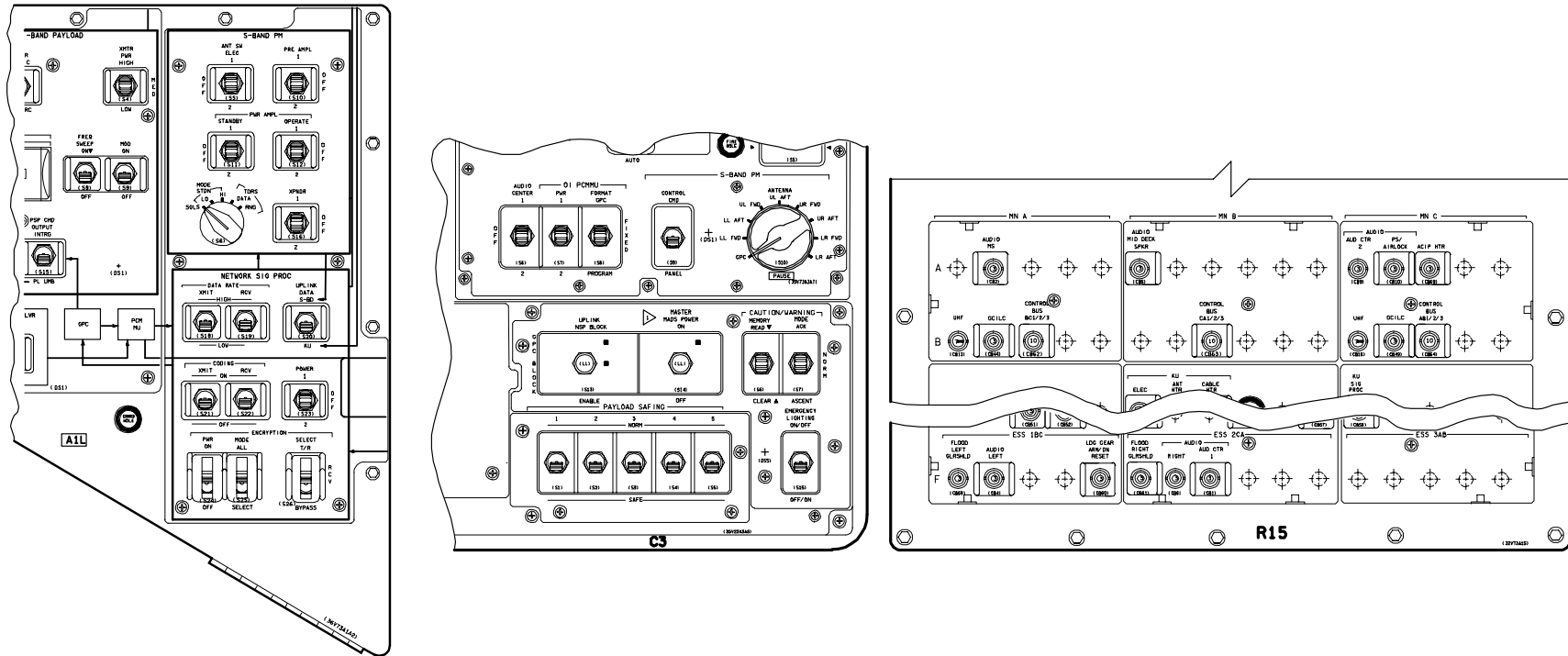


Figure 3-1. S-Band PM controls

### 3.2.6 S-Band System Command Control

Section 3.7 lists the S-band PM system commands. The list is broken up into sections according to the primary LRU affected; however, other LRUs may be cued by the same command. For example, command of S-BD XPNDR 1 - ON powers transponder 1, and cues NSPs 1 and 2, PA 1 and PA 2, and the antenna switch that XPNDR 1 is ON.

#### 3.2.6.1 Redundant LRU Mode Selection

A single GCIL Real-Time Command (RTC) will enable both GCIL mode drivers of NSPs 1 and 2 and XPNDRs 1 and 2, so that switching between LRUs 1 and 2 will not require configuration of the mode commands after the switchover has been made.

#### 3.2.6.2 GCIL-Only Command Fail States

GCIL-only command functions are those LRU control functions which do not have an associate panel switch, are not affected by the S-band PM control-CMD/panel switch, and have a predetermined fail-to state if the GCIL should fail or lose all power (revert to panel mode).

Table 3-6 presents the GCIL-only functions that affect the S-band PM system.

**Table 3-6. GCIL only command fail states**

| Function        | Fail state     |
|-----------------|----------------|
| Spread spectrum | Enable ①       |
| PM XPNDR freq   | High           |
| PM XPNDR mode   | Transpond      |
| Preamplifiers   | 1 & 2 ON       |
| Ku/S fail safe  | Disable (S-BD) |

- ① STDN and SGLS modes inhibit spread spectrum in transponder, even though it is enabled by GCIL.

#### 3.2.6.3 S-Band PM Control-CMD/Panel Switch

The S-band PM control-CMD/panel switch selects either the command mode or panel mode of the S-band PM GCIL driver logic. These drivers are designated by PM in the lower part of the GCIL driver symbol on the Space Shuttle Systems Handbook (SSSH) schematics. Note that the GCIL-only drivers have an N designation and are not affected by this switch.

- A. Panel mode: When panel mode is selected, the GCIL panel drivers will be activated or remain off according to whether the function is selected or not, respectively, by the associated crew panel control switch.

The GCIL will revert to panel mode automatically when it senses both power sources are below 22 V dc for > 400 μsec.

- B. Command mode: In command mode, the LRUs are controlled by ground command or crew keyboard entry. When the S-band PM control-CMD/panel switch is changed from panel to command, those GCIL driver functions which are on will remain on, since the GCIL logic senses that the panel driver was on, and therefore, the command driver is desired to be on. This is so there will not be a change in the LRU controls during the switchover.

#### **3.2.6.4 S-Band PM GCIL MODE (SALVO) Commands**

Table 3-7 lists the GCIL MODE (SALVO) commands executed by one RTC. When the GCIL decoder receives the single GCIL MODE (SALVO) RTC, multiple commands listed will be executed. The individual RTCs (DSMs 44XX) are shown in parentheses for reference.

Note: The return link data enable and ranging control functions are part of the S-band salvos (TDRS DATA/STDN LO/STDN HI/SGLS).

#### **3.2.7 S-Band PM Switched Beam Antenna System**

Four S-band quad antenna locations (Figure 3-2) are spaced around the forward fuselage in an approximately symmetrical manner.

Each switch beam antenna uses two closely spaced radiating elements. The elements are phase switchable to direct the beam forward or aft. The radiating elements are broadbanded crossed dipoles that are fed to provide right-hand circularization.

Four antennas, one each UL, UR, LL, and LR, were tested with the upper right and lower right orbiter mockups. Composite coverage plots of the antenna system are shown in Figure 3-4 to Figure 3-7. Figure 3-2 defines the antenna pattern theta/phi coordinate system.

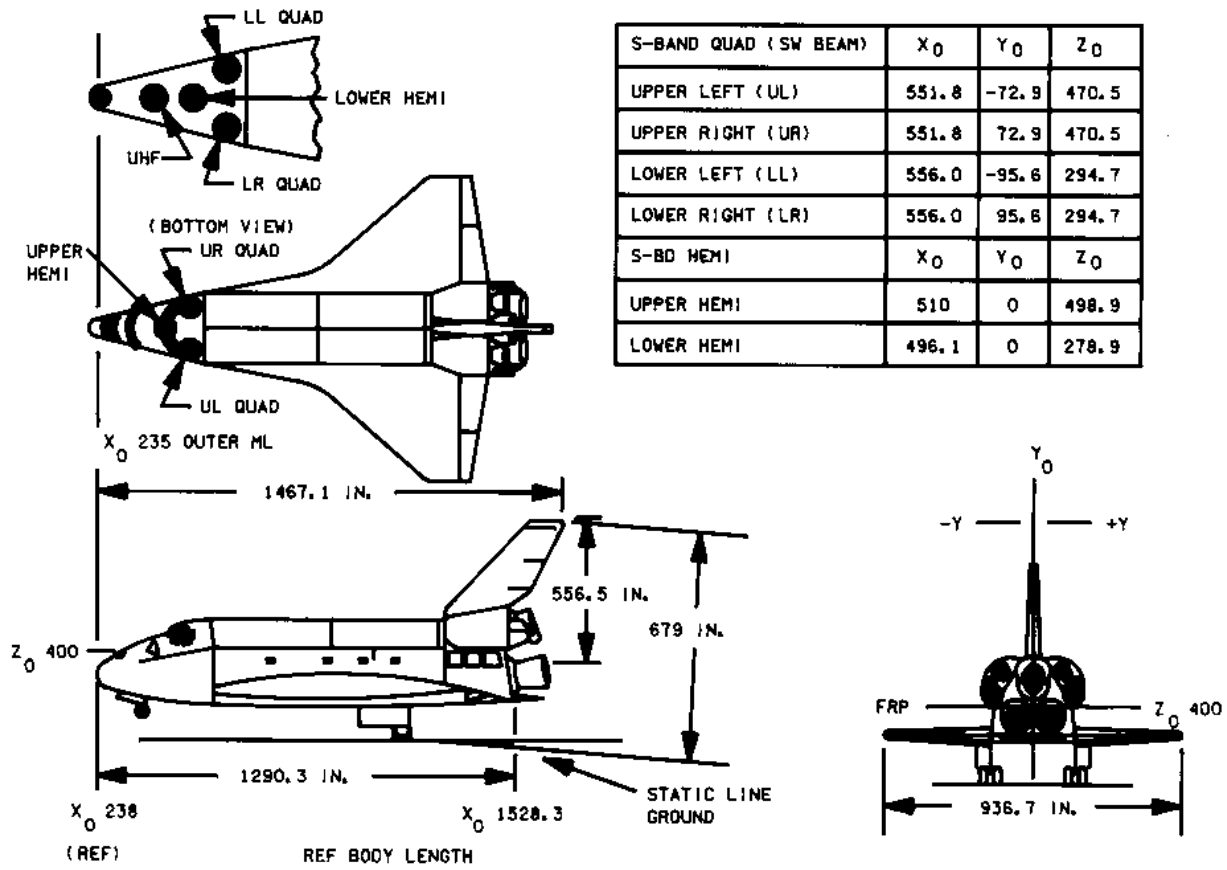
**Table 3-7. S-Band PM GCIL Mode (SALVO) commands**

|        |                       |        |                          |
|--------|-----------------------|--------|--------------------------|
| 4470   | TDRS Mode (Salvo)     | 4473   | SGLS Mode (Salvo)        |
| (4786) | S-Bd Mode - TDRS      | (4789) | S-Bd Mode - SGLS         |
| (4781) | XPNDR Direct - OFF    | (4781) | XPNDR Direct - ON        |
| (4758) | Uplink - LDR          | (4759) | Uplink - HDR             |
| (4763) | Dnlink - LDR          | (4764) | Dnlink - HDR             |
| (4770) | Uplink Coding - ON    | (4771) | Uplink Coding - OFF      |
| (4772) | Dnlink Coding - ON    | (4773) | Dnlink Coding - OFF      |
| (4768) | Data Source - S       | (4768) | Data Source - S          |
| (4790) | Spd Spm - ON          | (4746) | RNG Disable - OFF        |
| (4741) | S-Bd XPNDR Mode - T/R | (4741) | S-Bd XPNDR Mode - T/R    |
| (4735) | R/L Data XMIT - ON    | (4735) | R/L Data XMIT - ON       |
| (4745) | RNG Disable - ON      |        |                          |
| 4471   | STDN Low Mode (Salvo) | 4474   | TDRS S-Band Carrier Only |
| (4787) | S-Bd Mode STDN LO     | (4786) | S-Bd Mode - TDRS         |
| (4781) | XPNDR Direct - ON     | (4790) | SPD SPM - ON             |
| (4759) | Uplink - HDR          | (4741) | S-Bd XPNDR Mode - T/R    |
| (4764) | Dnlink - HDR          | (4768) | Data Source - S          |
| (4771) | Uplink Coding - OFF   | (4745) | RNG Disable - ON         |
| (4773) | Dnlink Coding - OFF   | (4758) | Uplink - LDR             |
| (4768) | Data Source - S       | (4770) | Uplink Coding - OFF      |
| (4746) | RNG Disable - OFF     | (4735) | R/L Data XMIT - OFF      |
| (4735) | R/L Data XMIT - ON    |        |                          |
| (4741) | S-Bd XPNDR Mode - T/R |        |                          |
| 4472   | STDN HI Mode(Salvo)   | 4475   | S-Band to Ku-Band        |
| (4788) | S-Bd Mode STDN HI     | (4767) | Data Source - Ku         |
| (4781) | XPNDR Direct - OFF    | (4759) | Uplink - HDR             |
| (4759) | Uplink - HDR          | (4764) | Dnlink - HDR             |
| (4764) | Dnlink - HDR          | (4771) | Uplink Coding - OFF      |
| (4771) | Uplink Coding - OFF   | (4773) | Dnlink Coding - OFF      |
| (4773) | Dnlink Coding - OFF   | (4755) | S-Bd PA 1/2 OPR - OFF    |
| (4768) | Data Source - S       | (4743) | S-Bd XPNDR Mode - RCV    |
| (4746) | RNG Disable - OFF     | (4745) | RNG Disable - ON         |
| (4741) | S-Bd XPNDR Mode - T/R |        |                          |
| (4735) | R/L Data XMIT - ON    |        |                          |

<sup>a</sup>Spread spectrum is inhibited in transponder in this mode.

Notes:

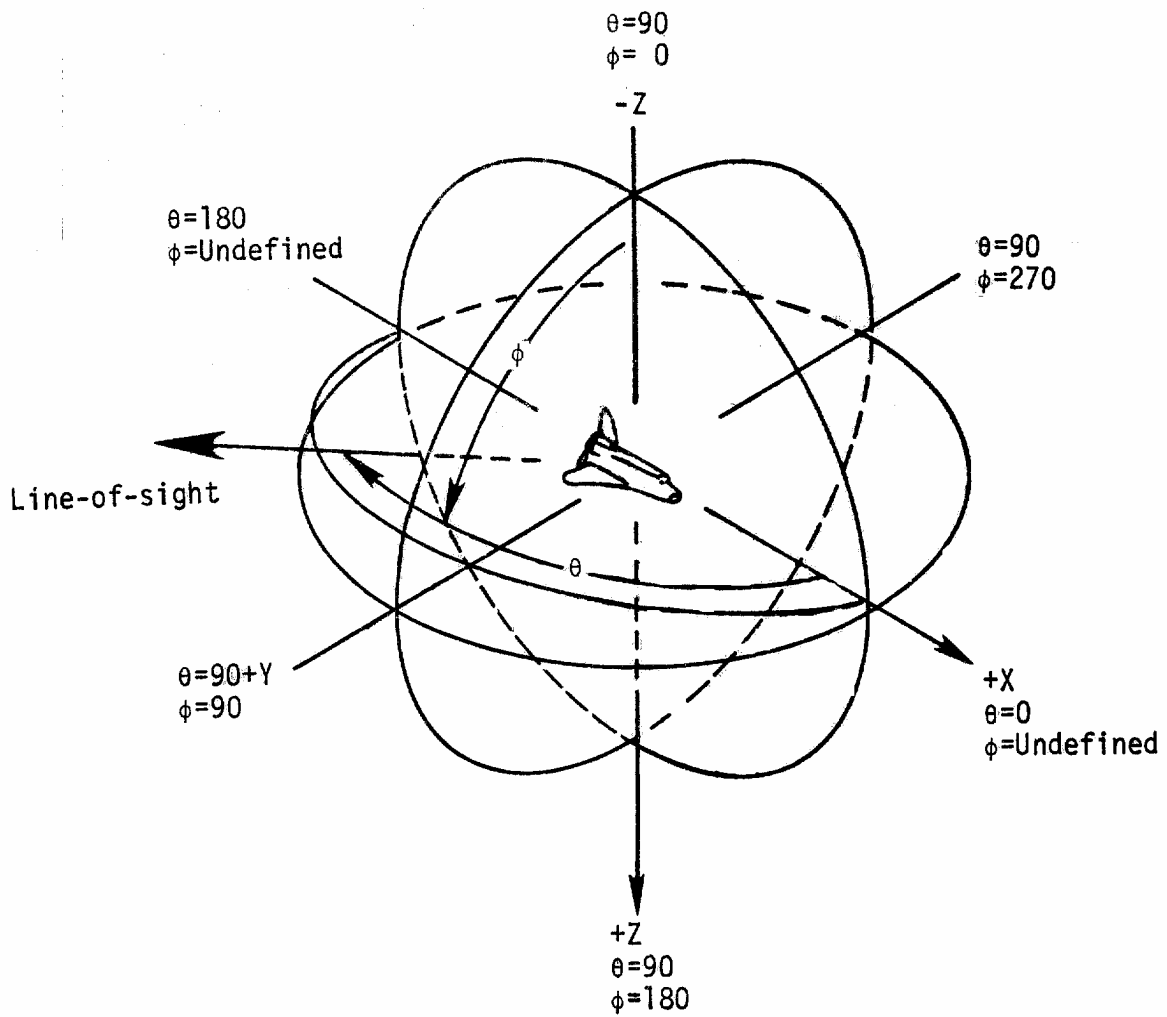
1. Individual RTC (DSMs) are shown in parentheses.
2. RNG DISABLE - ON = RNG OFF.



3198. ART. 2

Figure 3-2. S-Band PM quad (SW beam) antenna location

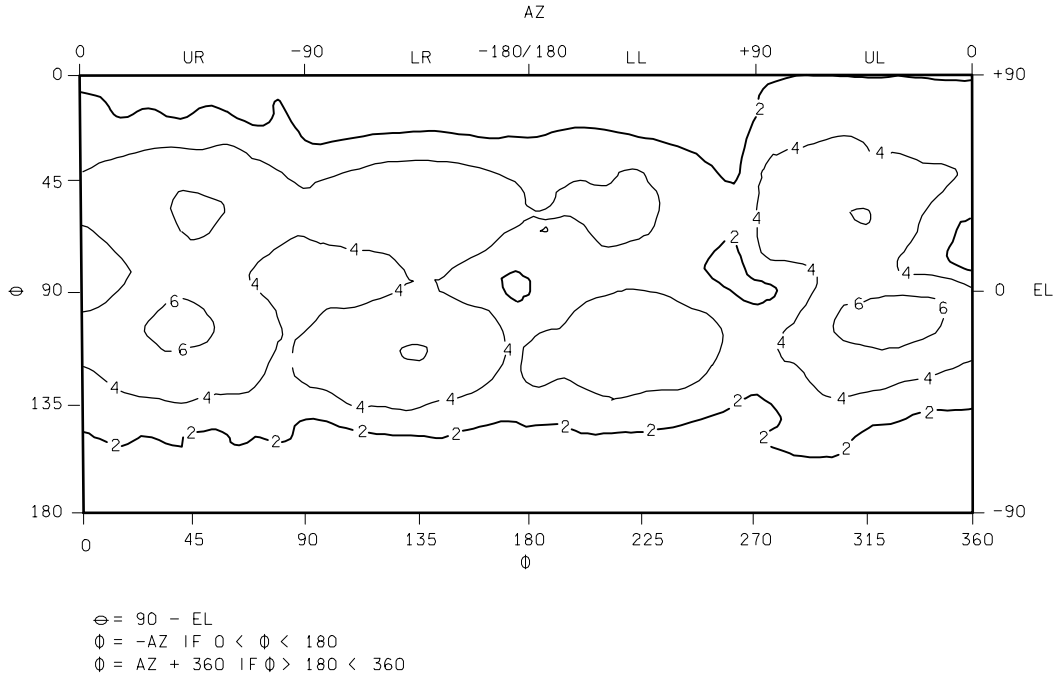




$\phi$  Measured from  $-Z$  body axis positively about  $X$  body axis to vector projection in  $Y-Z$  plane.

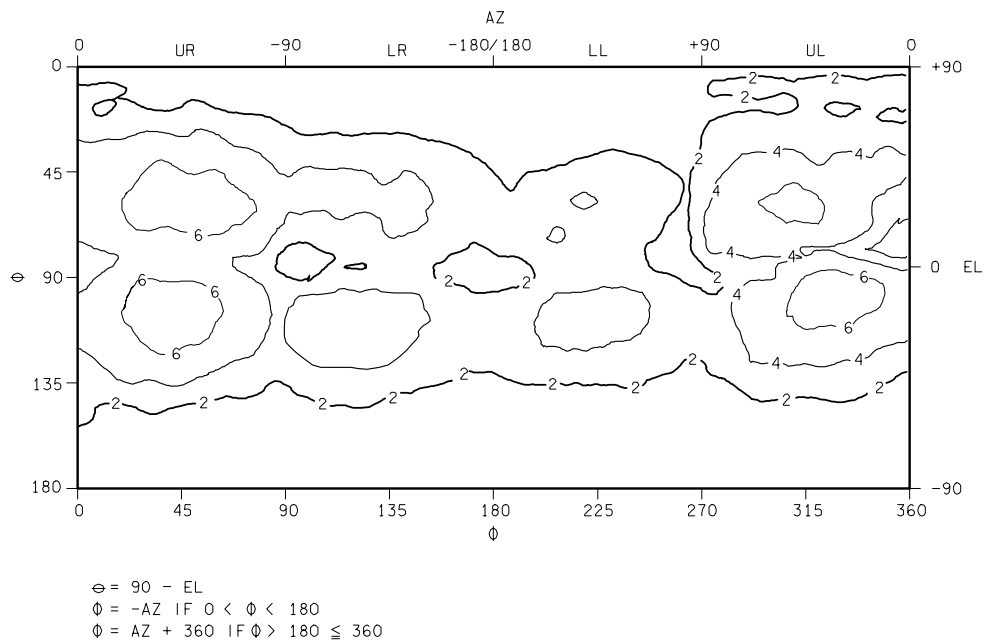
$\theta$  Smallest angle measured from  $+X$  body axis to vector.

**Figure 3-3. Antenna pattern  $\theta/\phi$  coordinate system**



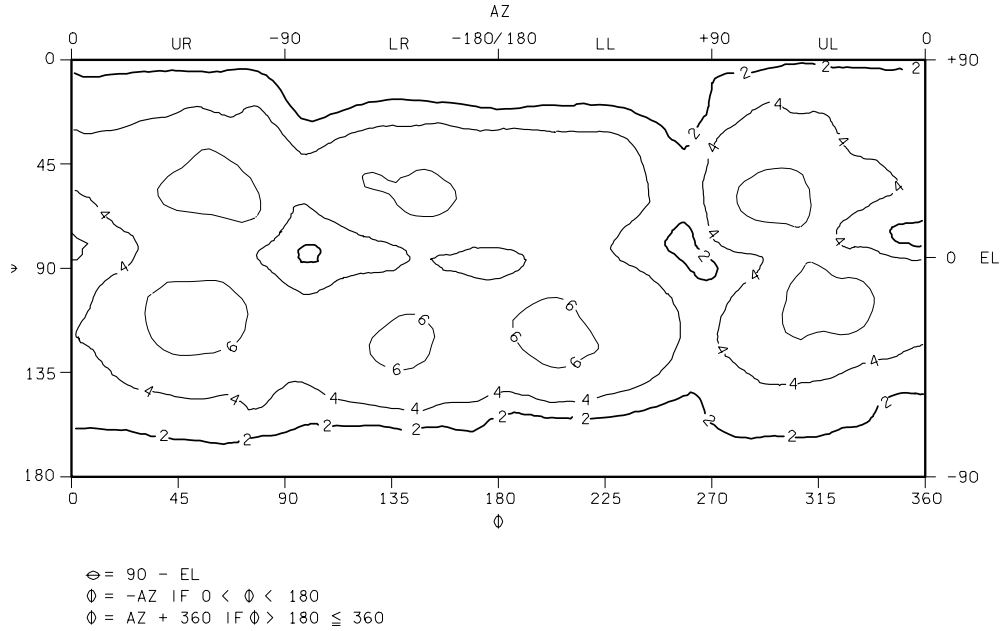
3199. ART; 4

**Figure 3-4. Switch beam antenna composite 2106.4 MHz**



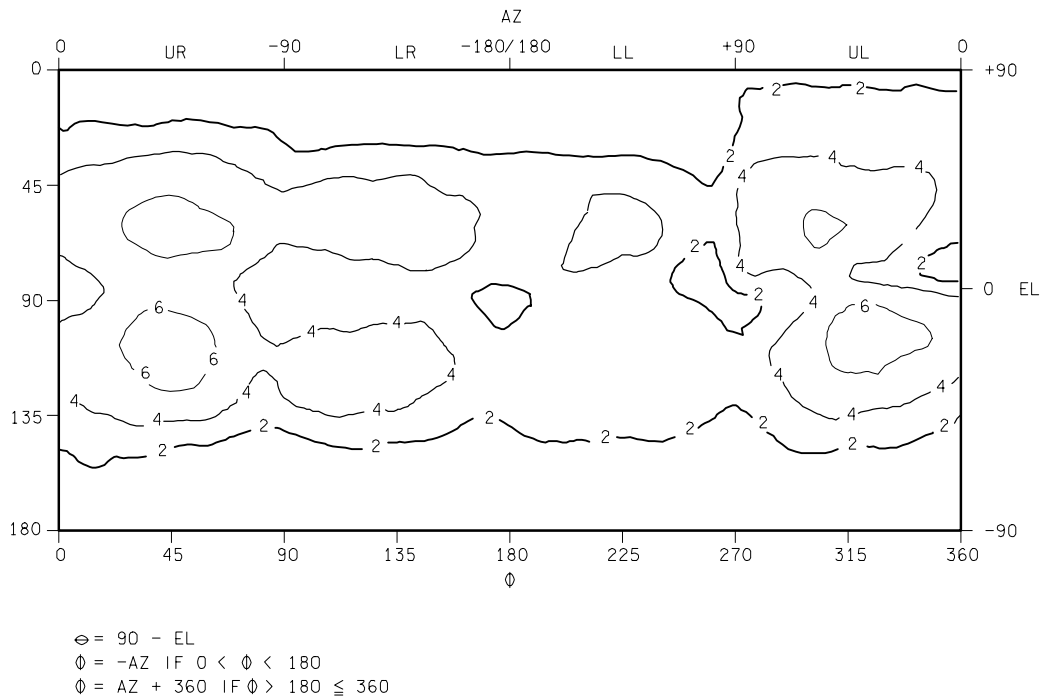
3202. ART; 3

**Figure 3-5. Switch beam antenna composite 2287.5 MHz**



3200. ART, 4

**Figure 3-6. Switch beam antenna composite 2041.9 MHz**



3201. ART, 4

**Figure 3-7. Switch beam antenna composite 2217.5 MHz**

**3.2.8 Circuit Margins**

Table 3-8 is a summary of the S-band PM system circuit margins. Data will be added to the table as it becomes available.

**Table 3-8. S-Band PM system circuit margins**

| FORWARD LINK         | STDN HIGH          |                    | STDN LOW           |                    | SGLS (AFSCF) |         | TDRS 4 |
|----------------------|--------------------|--------------------|--------------------|--------------------|--------------|---------|--------|
|                      | 30' 1              | 14' 2<br>(DUAL)    | 30' 1              | 14' 2<br>(DUAL)    | 46' 1        | 60' 3   |        |
| LDR (32 kbps)        | 54.4 dB            | 54.6 dB            | 49.4 dB            | 49.4 dB            | 43.9 dB      | 39.1 dB | 3.4 dB |
| HDR (72 kbps)        | 50.9 dB            | 50.9 dB            | 44.9 dB            | 43.2 dB            | 40.4 dB      | 38.2 dB | -1 dB  |
| LDR (32 kbps)<br>RNG | 51.1 dB<br>75.6 dB | 51.1 dB<br>75.6 dB | 45.1 dB<br>69.6 dB | 45.1 dB<br>69.6 dB | N/A          | N/A     | N/A    |
| HDR (72 kbps)<br>RNG | 47.6 dB<br>75.6 dB | 47.6 dB<br>75.6 dB | 41.6 dB<br>69.6 dB | 41.6 dB<br>69.6 dB | N/A          | N/A     | N/A    |

| RETURN LINK           | STDN HIGH          |                    | STDN LOW           |                    | SGLS (AFSCF) |         | TDRS 4 |
|-----------------------|--------------------|--------------------|--------------------|--------------------|--------------|---------|--------|
|                       | 30'                | 14'<br>DUAL        | 30'                | 14'<br>DUAL        | 46'          | 60' 3   |        |
| LDR (96 kbps)         | 34.6 dB            | 19.4 dB            | 12.9 dB            | -2.3 dB            | 20.6 dB      | 19.4 dB | 4.5 dB |
| HDR (192 kbps)        | 31.6 dB            | 16.4 dB            | 15.9 dB            | .7 dB              | 17.6 dB      | 16.4 dB | 1.5 dB |
| LDR (96 kbps)<br>RNG  | 32.2 dB<br>71.6 dB | 17.0 dB<br>55.9 dB | 16.5 dB<br>55.9 dB | 1.3 dB<br>40.7 dB  |              |         |        |
| HDR (192 kbps)<br>RNG | 29.2 dB<br>71.6 dB | 14.0 dB<br>42.4 dB | 13.5 dB<br>55.9 dB | -1.7 dB<br>40.7 dB |              |         |        |

NOTES: 1 2 kW TRANSMIT (ADD 7 dB FOR 10 kW TRANSMIT)  
 2 14' STDN SITES  
 QUI (DUAL) - REFERENCE  
 NFS (SINGLE) - ADD + 1.8 dB D/L AND - 18 dB U/L  
 PDL (SINGLE) - ADD + 1.8 dB D/L AND - 18 dB U/L  
 3 60' SGLS SITE  
 IOS  
 4 CODES MODE

Source: Space Shuttle Communications and Tracking RF Link Circuit Margin Summary. EH2-M/79 - 039 (April 1979)

**3.3 SYSTEM OPERATING CONSTRAINTS**

This section contains operating constraints, such as warmup times, mode switching, thermal, Radio Frequency Interface (RFI), RF hot switching, and acquisition times. Included are automatic fail-over modes of the system.

**3.3.1 Equipment Warmup**

**3.3.1.1 S-Band Antenna Switch Warmup**

No warmup required.

**3.3.1.2 S-Band Switch Beam Electronics**

No warmup required.

**3.3.1.3 S-Band Power Amplifier Warmup**

The power amplifier has an internal timer (to allow the Traveling Wave Tube (TWT) filament to warm up) that must time out (140 sec) before high voltage is applied to the TWT and RF amplification takes place. A total of 4 minutes is required to stabilize.

The standby mode is provided so that one power amplifier can be operating and the second power amplifier put in the standby mode. Note that both power amplifiers may be put in the standby mode via ground command. Crew switches only allow one at a time in standby.

**3.3.1.4 S-Band Preamplicifier Warmup**

The preamplifier requires a warmup period of 4 to 18 minutes to stabilize. In 4 minutes the gain is 22 dB, and full gain can be expected at 18 minutes. Two separate heaters are required to stabilize the RF, circulator assembly impedance ( $90^{\circ} \pm 25^{\circ} \text{ F}$ ), and gun diode oscillator frequency ( $175^{\circ} \pm 1^{\circ} \text{ F}$ ), respectively. Full gain is achieved in less than 10 seconds if the heaters have been operating for at least 18 minutes.

Power requirements are shown in Table 3-9.

**Table 3-9. Preamp dc power (watts)**

| Time   | One On            |        | One STBY          | Total |
|--------|-------------------|--------|-------------------|-------|
|        | HTR               | PREAMP |                   |       |
| T = 0  | 23.5              | 13     | 23.5              | 60    |
| 10 min | 13.5 <sup>a</sup> | 13     | 13.5 <sup>a</sup> | 40    |

<sup>a</sup>Varies from 8 to 19 W, depending on baseplate temperature.

Note that both preamplifier heater pairs are turned on by a single command that may be used as a standby mode. The HEATER ON command is not required for the operating preamplifier because the heater is powered when the preamplifier is selected.

**3.3.1.5 S-Band Transponder Warmup**

The warmup time is 30 seconds to meet specification. No warmup time is required to reach operation.

### 3.3.1.6 NSP Warmup

No warmup required.

### 3.3.2 System Switching Transients

Antenna switching dropout time ~1 ms to 5 ms (no loss of lock).

Prime mode switching dropout time ~100 ms for XPNDR and 200 ms for PWR AMP.

Coherent-to-noncoherent VCXO dropout time ~5 ms to 10 ms.

XPNDR normally maintains RCVR lock during antenna switching.

### 3.3.3 RF Hot Switching

RF hot switching is defined as making or breaking an RF path while an RF signal is present on the RF path; e.g., switching a coax switch.

Note: No constraint is placed on changing modes or switching LRUs while operating the S-band PM system, providing all logic in the GCIL and LRUs is operational.

#### 3.3.3.1 Antenna Switch Coax Switching

Coax switches in the antenna switch are break-before-make, with a switching time of 25 msec and an RF hot switching capability of 175 W continuous. Life tests have been performed to 250,000 cycles. Expected maximum RF power level is 147 W.

#### 3.3.3.2 Preamplicifier Coax Switching

Coax switches S1 and S2 are in the receive RF path and therefore switch a low-level RF signal. Coax switch S3, however, switches the power amplifier transmit signal whenever the transponder frequency mode is changed or the power amplifiers are switched.

When the frequency mode of the transponder is changed, the transmit RF signal out of the transponder is inhibited for 30 to 100 msec to allow the transponder transmitter coax switch to switch. This loss of RF is sensed by the power amplifier RF threshold circuit, which removes the TWT high voltage within 6 msec and drops the power amplifier RF output to preamplicifier coax switch S3 in time for the coax switch to switch at a safe RF level.

#### 3.3.3.3 Power Amplifier

When switching from one power amplifier to another, assuming both were in the standby mode or one operating and one in standby, a 1-second delay of the normal command select line inhibits the new selected power amplifier from RF amplification, so the coax relay S3 in the preamplicifier can switch before the RF signal is applied to the coax switch.

The RF level will reach full power within 1.5 to 2.5 seconds (1-second delay included) of the NORMAL ON select signal.

Note: Preamplifier 1 or 2 must be selected before the power amplifier is allowed to come on after a 1-second delay. The GCIL/PREAMP SELECT switch provides this interlock function.

#### **3.3.3.4 Transponder**

The RF signal to the final RF power amplifier stage of the transmitter is inhibited for 30 to 100 msec whenever the frequency high, frequency low, STDN low, STDN high, TDRS, or SGLS mode of the transponder is changed. This removes RF power from the transmitter KI coax switch.

### **3.3.4 S-Band PM System Acquisition Time**

Several circuits must be satisfied before data are available to the forward link and return link user. These circuits in the SSO are the transponder Spread Spectrum Processor (SSP) and phase lock channel, and the NSP bit sync and frame sync circuits, and convolutional decoder.

#### **3.3.4.1 Forward Link Circuits**

##### **A. Transponder SSP**

The SSP must be locked (Pseudonoise (PN) code acquisition) in TDRS mode before phase lock channel can be locked. This time can vary depending on the data rate, PN code Doppler, and signal level. Time to acquire the forward link at expected signal level is 5 to 10 seconds with Doppler compensation. Acquisition may not occur at all if Doppler is greater than 40 kHz and not compensated.

See Section 3.6.1.2 for the SSP acquisition algorithm.

##### **B. Transponder phase lock channel**

The Ground Spacecraft Tracking and Data Network (GSTDN) uplink acquisition time of the phase lock channel varies with temperature and signal level. Nominal time is less than 3 seconds with carrier only. Sweep is +150 kHz at 40 kHz/sec rate (sawtooth) starting at -75 kHz and retracking at +75 kHz. GSTDN downlink acquisition time is <1.5 seconds. Two-way lock is <7.3 seconds (Electronics Systems Test Laboratory (ESTL) data).

See Section 3.6.1.1 for the transponder loop filter and sweep circuit operation (receiver acquisition algorithm).

##### **C. NSP bit sync and frame sync lock**

Bit sync acquisition time is a function of Signal-to-Noise (S/N) ratio. In uncoded mode acquisition, time is less than 3 seconds (S/N 0 dB), and in coded mode, it is less 5 seconds (S/N 3 dB).

Frame sync lock will occur within two frame periods, which would make the worst case time less than 60 msec, providing the proper signal level is available for Bit Error Rate (BER) of  $10^{-3}$  in selected mode.

D. Convolutional decoder

In coded mode, data are output within 0.1 second from the convolutional decoder.

### 3.3.4.2 Return Link Functions

During transponder no-lock and acquisition periods of the forward link, the transponder frequency is fixed and derived from the auxiliary oscillator. Upon receiver lock on the carrier, the transponder frequency source is switched to the voltage-controlled oscillator, and is a fixed ratio of the forward link frequency (see Section 3.2.1).

### 3.3.4.3 TDRS Ground Station Acquisition Time

Acquisition time will be 0.11 to 0.51 second through the data demodulator.

### 3.3.4.4 STDN/SGLS Ground Station Acquisition Time

Data through the RF circuits and the bit sync should be obtained in less than 5 seconds. The receiver will be Doppler compensated so that the return link signal frequency will be within the acquisition bandwidth of the ground receiver when the SSO transponder switches to the receiver Voltage-Controlled Crystal Oscillator (VCXO).

### 3.3.5 Problems Modes or Commands

#### 3.3.5.1 Antenna Switch

The antenna switch should not be allowed to switch faster than 4 cps.

#### 3.3.5.2 Loss of S-BD U/L Voice and CMD Problem

The modification to the S-band transponder to provide TDRS ranging (no capability due to circuit margin) added a GCIL/PNL control function to disable D/L data. This modification can result in a loss of U/L.

A. Problem

If GCIL CMD S-band mode-TDRS RNG has been sent and NSPs are subsequently switched, the transponders will be configured to route U/L data to the unselected NSP and a loss of U/L will occur on S-band.

B. Procedure

If NSPs are to be switched

- Send DSM 4744 S-BD R/L data - ENA
- Switch NSPs



- Send 4737 S-BD mode - TDRS RNG (R/L data-off)

This sequence reconfigures the transponder to operator with the selected NSP.

### 3.3.5.3 Pulse-Code Modulation Fail (NSP Internal) Mode

In the absence of the Pulse-Code Modulation Master Unit (PCMMU) 64-kbps or 128-kbps telemetry, 1.152-MHz clock, or 100 PPS sync signal, the return link data buffers will go into an internal mode of operation, providing frame sync bits and dummy Telemetry (TLM) data blocks of 32 bits of alternating 1's and 0's. The Time Division Multiplexer (TDM) signal in the internal mode allows one or two voice channels to operate in a normal manner with 32-bit bytes of dummy TLM data.

Loss of only the PCMMU 1.152 MHz clock will not cause loss of Pulse-Code Modulation (PCM) and voice to the recorder; however, loss of the PCMMU 128-kbps PCM will cause loss of voice, as well as TLM, since the data sent to the recorders will not have a sync pattern to record and the voice data cannot be recovered. In DOD mode (encryption select-all), the OPS recorder data are obtained from the return link data buffers which provide a dummy PCM sync pattern.

## 3.4 SYSTEM MONITORING

Section 3.9 lists all the telemetry associated with the S-band system.

### 3.4.1 Special TM Computations

“M” parameters are used in ODRC; substitute “W” for “M” for workstation comps.

#### M06I0200R XPNDR MODE

| <u>V74X</u> | <u>TDRS</u> | <u>STDN LO</u> | <u>STDN HI</u> | <u>SGLS</u> |
|-------------|-------------|----------------|----------------|-------------|
| 4786E (TD)  | 1           | 0              | 0              | 0           |
| 4787E (SL)  | 0           | 1              | 0              | 0           |
| 4788E (SH)  | 0           | 0              | 1              | 0           |
| 4789E (SG)  | 0           | 0              | 0              | 1           |

#### M09I0200R PWR AMPL 1

| <u>V74X</u>  | <u>ON</u> | <u>INVL</u> | <u>STBY</u> | <u>OFF</u> |
|--------------|-----------|-------------|-------------|------------|
| 4784E (ON)   | 1         | 1           | 0           | 0          |
| 4747E (STBY) | 1         | 0           | 1           | 0          |

#### M10I0200R PWR AMPL 2

| <u>V74X</u> | <u>ON</u> | <u>INVL</u> | <u>STBY</u> | <u>OFF</u> |
|-------------|-----------|-------------|-------------|------------|
| 4785E       | 1         | 1           | 0           | 0          |
| 4749E       | 1         | 0           | 1           | 0          |

M01I0201F ANT MODE SEL MAN

| <u>V74S</u> | <u>MAN</u> | <u>MAN</u> |
|-------------|------------|------------|
| 6503E       | 1          | 0          |
| 6504E       | 0          | 1          |

M02I0201E ANT MODE SEL GPC

| <u>V74S</u> | <u>GPC</u> |
|-------------|------------|
| 6503E       | 0          |
| 6504E       | 0          |

M05I0200R ANTENNA SELECT (PM)

| RL<br>Source<br>(Antenna Text)                          | S-Band SWITCH BEAM ANT SEL           |                                      |                                      |                                      |
|---|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|
|   | UL                                   | UR                                   | LL                                   | LR                                   |
| GCIL - XPNDR 1<br>DIRECT V74X4780X<br>(SGLS/STDN LO)    | V74X7084X<br>S4B<br>S1B<br>V74X7072X | V74X7084X<br>S4B<br>S1A<br>V74X7070X | V74X7082X<br>S4A<br>S3A<br>V74X7078X | V74X7082X<br>S4A<br>S3B<br>V74X7080X |
| GCIL - XPNDR 2<br>DIRECT V74X4781X<br>(SGLS/STDN LO)    | V74X7076X<br>S2B<br>S1A<br>V74X7070X | V74X7076X<br>S2B<br>S1B<br>V74X7072X | V74X7074X<br>S2A<br>S3B<br>V74X7080X | V74X7074X<br>S2A<br>S3A<br>V74X7078X |
| GCIL - PREAMPL<br>HIGH FREQ X74X4779X<br>(TDRS/STDN HI) | V74X7082X<br>S4A<br>S1B<br>V74X7072X | V74X7082X<br>S4A<br>S1A<br>V74X7070X | V74X7084X<br>S4B<br>S3A<br>V74X7078X | V74X7084X<br>S4B<br>S3B<br>V74X7084X |
| GCIL - PREAMPL<br>LOW FREQ V74X4778X<br>(TDRS/STDN HI)  | V74X7074X<br>S2A<br>S1A<br>V74X7070X | V74X7074X<br>S2A<br>S1B<br>V74X7072X | V74X7076X<br>S2B<br>S3B<br>V74X7078X | V74X7076X<br>S2B<br>S3A<br>V74X7078X |

M02I0603R SWITCH BEAM ANTENNA/BEAM SELECT

| V74X-                  | ULF | ULA | URF | URA   | LLF | LLA | LRF | LRA |
|------------------------|-----|-----|-----|-------|-----|-----|-----|-----|
| 7090X                  | 1   | 0   | X   | X     | X   | X   | X   | X   |
| 91X                    | 0   | 1   | X   | X     | X   | X   | X   | X   |
| 92X                    | X   | X   | 1   | 0     | X   | X   | X   | X   |
| 93X                    | X   | X   | 0   | 1     | X   | X   | X   | X   |
| 94X                    | X   | X   | X   | X     | 1   | 0   | X   | X   |
| 95X                    | X   | X   | X   | X     | 0   | 1   | X   | X   |
| 96X                    | X   | X   | X   | X     | X   | X   | 1   | 0   |
| 97X                    | X   | X   | X   | X     | X   | X   | 0   | 1   |
| M05I<br>0200R          | UL  | UL  | UR  | UR    | LL  | LL  | LR  | LR  |
| ERROR IN M05I0200R     |     |     |     | = ER1 |     |     |     |     |
| ALL OTHER COMBINATIONS |     |     |     | = ER2 |     |     |     |     |

**3.5 SYSTEMS MANAGEMENT (SM)**

S-band system 1 (2) will be commanded on and operating and system 2 (1) selected on the panel switches. This configuration allows the redundant system to be activated by the crew (PNL C3; S-band PM CNTL-PNL) or automatically by the command interface logic LRU (GCIL) should GCIL power fail.

**3.6 S-BAND EQUIPMENT (LRU) NOTES**

This section contains certain data, descriptions, and operation of S-band system LRUs that are of particular interest to understanding the operation and interfaces of the LRUs in the system. This information is intended to give additional information that is not apparent or presented on the SSSH schematics.

**3.6.1 S-Band Transponder**

**3.6.1.1 Transponder Loop Filter and Sweep Circuit Operation**

The loop filter and sweep circuit is shown as a single block on SSSHB drawing 16.2-1. The loop filter serves to sweep the VCXO frequency during acquisition, and then to switch to a narrow phase lock-loop bandwidth after acquisition. The tracking phase error signal is formed as the product of the I and Q channels, and a coherent amplitude estimate is formed by the difference of the squared outputs of the I and Q arms ( $I^2 - Q^2$ ).

The amplitude estimate from the coherent amplitude detector is filtered by a two-pole variable bandwidth low-pass filter prior threshold detection by the phase lock-loop lock detector (comparator).

Note: The lock detector (comparator) has two threshold voltages ( $V$  and  $1/2 V$ ). When the voltage out of the ( $I^2 - Q^2$ ) compatible amplitude detector reaches threshold, phase lock is assumed to be achieved, the transmitter is switched to coherent mode (VCXO) and the threshold to the comparator is lowered. This change in threshold requires a lower out-of-lock voltage to be sensed than an in-lock voltage. A 50 to 90 msec delay (wait) occurs before the transmitter is switched to noncoherent oscillator mode when lock is lost.

Figure 3-8 presents the receiver acquisition algorithm.

The following four equations control the operation of the transponder loop filter and sweep circuit:

$$\begin{aligned} A &= PL + \underline{CP} + (\underline{SP} \cdot \underline{SD} \cdot TD) && \text{sweep control} \\ B &= PL + \underline{CP} + (\underline{SP} \cdot \underline{SD} \cdot TD) \\ I &= J = SP + SD + \overline{TD} && \text{(VCO control)} \\ G &= H = PL && \text{(bandwidth control)} \end{aligned}$$

To understand these equations, it is necessary to define each logic term and the conditions that cause each term to take a high "1" or low "0" state.

Functions A, B, I, J, G, and H are control inputs to the loop filter and sweep circuit. Note that they actively control the sweep circuit when the equation output is low "0."



PL - (Phase lock) Costas loop lock

“1” = Lock

“0” = No lock

CP - (Sweep limit) sweep voltage is at the low end of its range

“1” = Low end of range

“0” = In sweep range

SP - (Spread spectrum phase lock)

“1” = In lock

“0” = Out of lock

SD - (Spread spectrum disable)

“1” = Disable selected

“0” = Enable selected

TD - (TDRS Mode) TDRS mode selected

“1” = TDRS mode selected

“0” = STDN or SGLS mode selected

“A” and “B” functions control the receiver sweep voltage. “A” going low causes the sweep voltage to go rapidly to the high end of the sweep range. “B” going low causes the sweep voltage to decay in a ramp-down fashion. “CP” signal indicates the sweep voltage has reached the end of the sweep cycle and is ready to start over. Examine equations “A” and “B,” and it will be apparent that the  $\overline{\text{CP}}$  and “CP” control these functions in a toggle fashion.

The last term in function “A” and “B,” (SP · SD · TD) when high (“1”), says that in the TDRS mode, if the spread spectrum mode is not disabled and the spectrum circuit is not locked (“0”), the sweep voltage is not applied to the sweep circuit until the SSP is locked (“0”). The sweep voltage is then enabled until the Phase Lock (PL) term becomes (“1”), indicating phase lock is achieved and the sweep voltage is not longer required.

The “I” and “J” functions when low (“0”) hold the VCO control voltage stable (to zero) until the SSP is locked, or the SSP is disable din the TDRS mode.

$$I = J = SP + SD + \overline{TD}$$

The “G” and “H” functions switch the loop filter bandwidth from 600 Hz to 200 Hz when phase locked (PL = “1”). Note also that functions “A” and “B” go high (“1”) when PL is high (“1”). This removes the sweep voltage when in the STDN or SGLS mode.

$$G = H = PL$$

### 3.6.1.2 SSP Acquisition Algorithm

The S-band PM receiver in the TDRS/spread spectrum mode uses an SSP to despread the RF signal. The processor operates as a noncoherent carrier detector and code phase tracking loop. This circuit is simply shown as an SSP block on the SSSHB

drawing 16.2-1. Inside the SSP, the Intermediate Frequency (IF) signal input is split into three channels:

- A. Punctual channel - provides the despread output.
- B. Acquisition channel - initially detects proper code alignment.
- C. Tracking channel - tracks code variation when code is acquired.

When the internal generated code is aligned in phase with the PN code modulation, an increase in signal ( $E_o$ ) occurs which is sensed by a threshold detector, and if  $E_o$  is greater than the threshold ( $V_{acq}$ ), the SSP VCXO in the track channel is ungrounded and the threshold detector threshold is set to  $V_{trk}$ . If correlation is maintained for the 12.6 msec dwell time, correlation is assumed.

Five sequential noncorrelations are required to start the acquisition logic searching again.

The data high control switches the track channel and the acquisition channel band pass filters for high data rate operation.

Figure 3-9 presents the detail SSP acquisition algorithm.

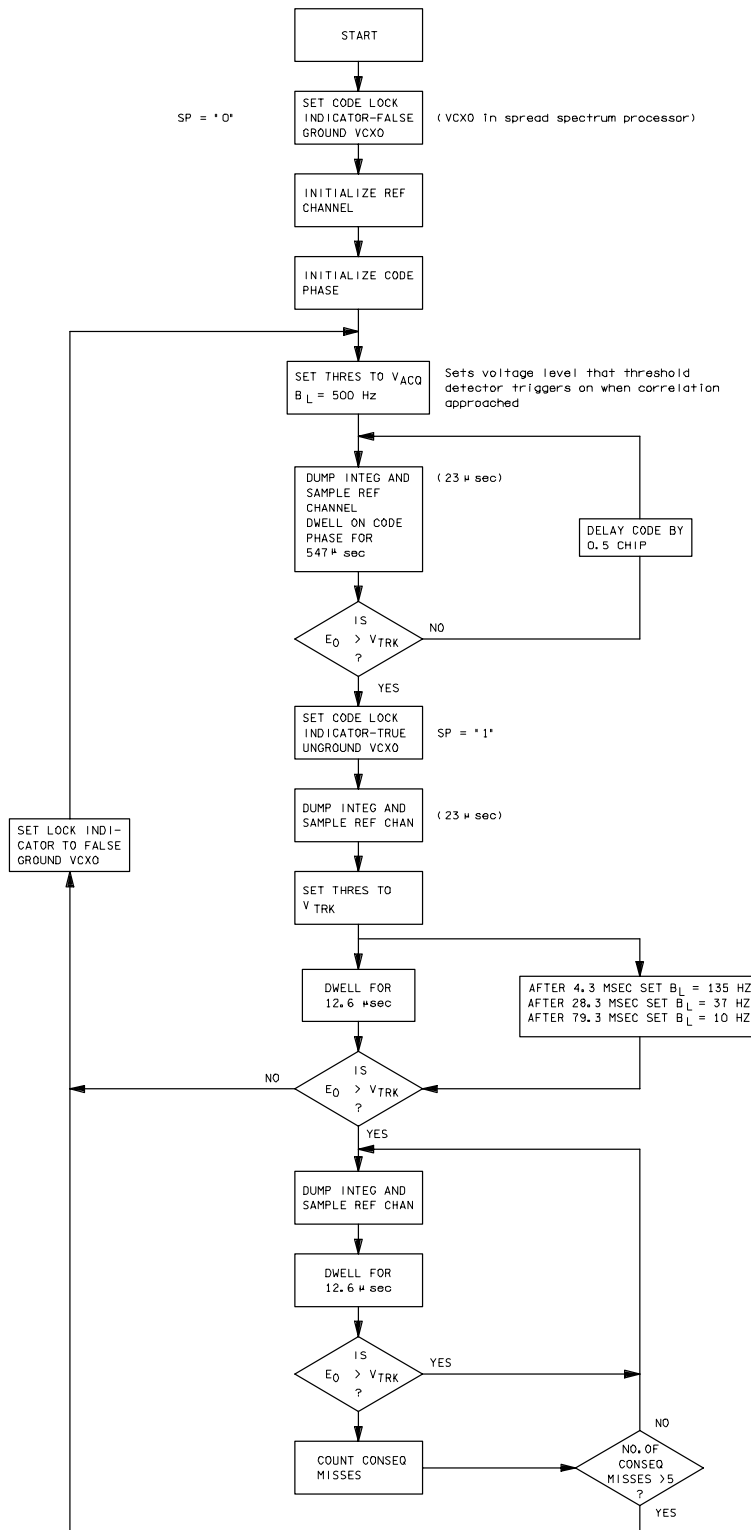
### **3.6.2 Network Signal Processor**

#### **3.6.2.1 Serial I/O Data Channel**

NSP Polling is controlled by the Guidance, Navigation, and Control (GNC) GPC or Backup Flight System (BFS) GPC. During ascent and entry, uplink software will track the BFS engage/disengage discrettes to determine GNC or BFS control.

Polling is every 165 msec (maximum rate for NSP) to ensure that each buffer of the command double buffer (A or B) will be polled at least once every 10 forward link PCM frame times. Each frame contains one 128-bit command, which is decoded into a 48-bit command and loaded into the command double buffer. The fill time of the buffer is 200 msec (1 CMD/frame) (10 CMDS) (50 frames/sec).

When polled, all 32 words are output (the first word is the Built-In Test Equipment (BITE) status word; the second through thirty-first words are command words, and the thirty-second word is the command validity word).



3724, ART 2

Figure 3-9. Spread spectrum processor acquisition algorithm



The 32 words output are from the command buffer not being filled by the forward link commands.

The BITE status and command status words provided are those associated with the command words transmitted. Status data are continuously loaded when data ready is LOW and then held when data ready is HIGH until the NSP is polled.

When data ready is ("0") because of:

- A. No bracketed data status (loss of NSP frame sync during receipt of command)
- B. The same buffer is polled more than once prior to it being refilled. Data ready bit is cleared after the first poll
- C. The buffer is polled within 20 msec prior to the buffer switch time

The NSP will transmit the valid BITE status word, even though data ready = "0", followed with 31 words of zeros (containing only a single "1" for each word for odd parity).

The 20-msec inhibit polling time is a design implementation to ensure no buffer mixing in a single transmission.

The data ready bit is set to a "1" at the end of the buffer fill time if at least one command word has passed the BCH decoder and valid vehicle address check.

### **3.6.2.2 NSP-MDM Data Flow**

Figure 3-10 shows the NSP SIO data flow within the NSP to the MDM interface. Figure 3-11 shows the NSP output message format.

### **3.6.2.3 NSP Internal Mode**

In the absence of the 64-kbps or 128-kbps telemetry, 1.152 MHz, or 100 PPS sync signal, the NSP shall go into an internal mode of operation, providing the frame sync bits and dummy TLM data blocks of 32 bits of alternating 1's and 0's. The TDM signal in internal mode allows the one- or two-voice channels to operate normally.

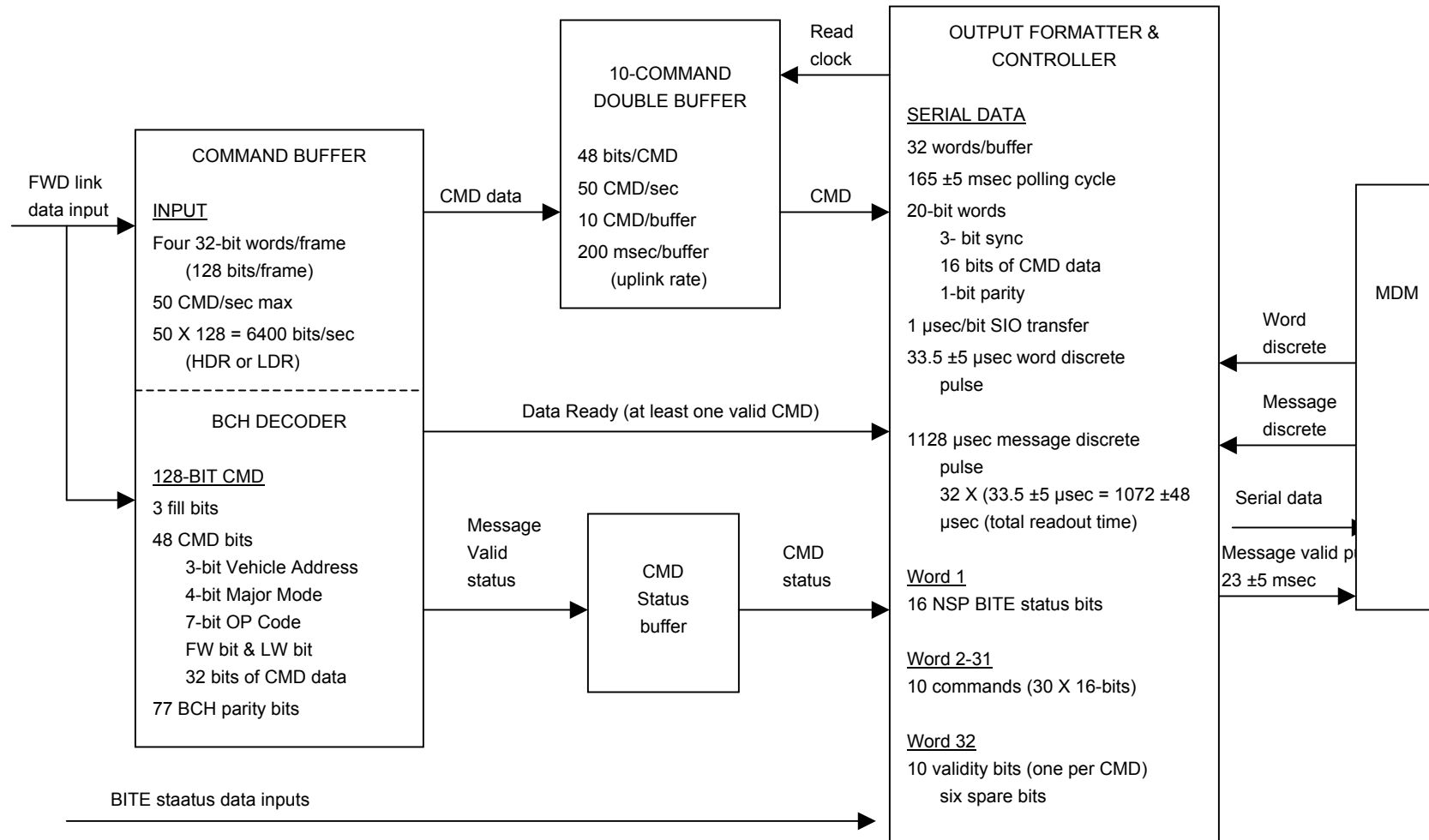
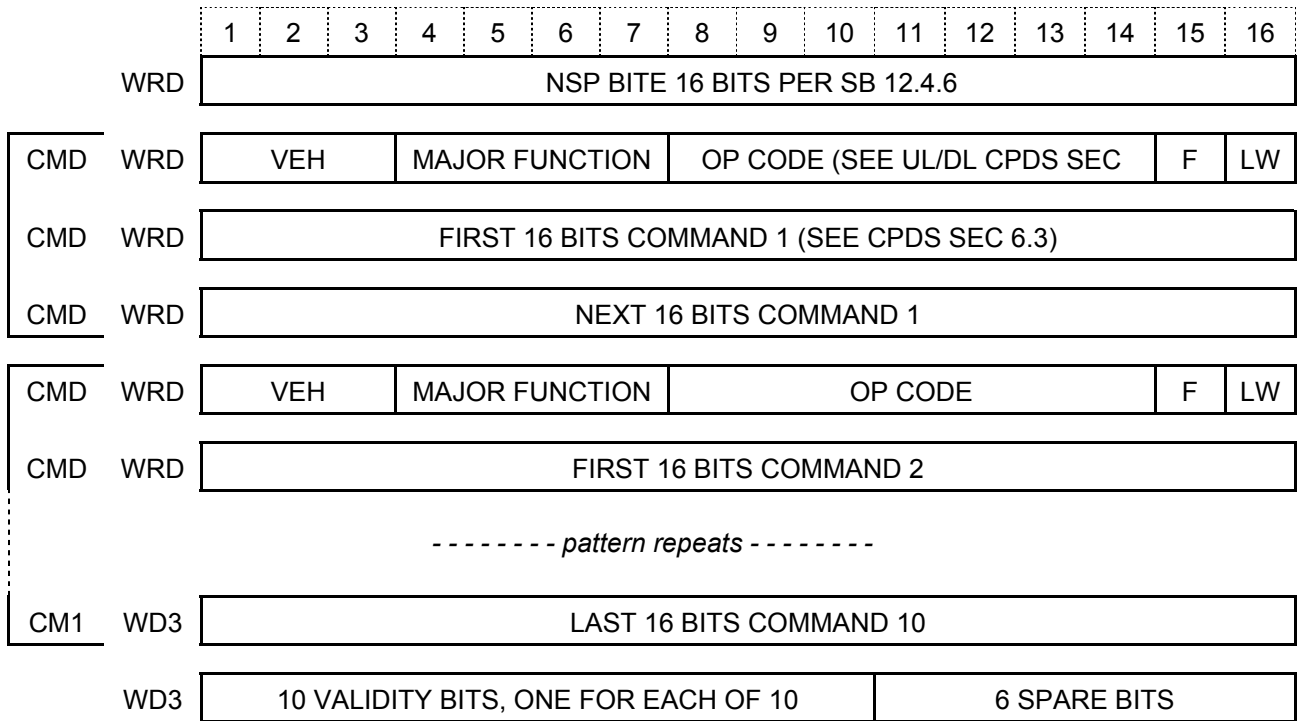


Figure 3-10. NSP SIO data flow



**Figure 3-11. NSP output message format**

### 3.6.3 NSP COMSEC

#### Operational Instructions

- A. Loss of power will zeroize the crypto variable memory. Only clear data available.
- B. If alarm condition occurs, cycle the operate control by cycling the associated NSP power.

### 3.7 S-BAND PM SYSTEM COMMAND LIST

#### 3.7.1 Miscellaneous MRTC's

| DSM   | ① | Title                | RTCs                          |
|-------|---|----------------------|-------------------------------|
| 4476  | M | S-BD STRING 1 SELECT | 4760 4730 4709 4722 4754 4752 |
| 4477  | M | S-BD STRING 2 SELECT | 4762 4732 4711 4724 4756 4750 |
| 4769* | M | TDRS SBD HDR MRTC    | 4470 4759 4764 4766           |
| 4640* | M | TDRS SBD HDR MRTC    | 4470 4759 4764 4766           |

\* DSM 4769 up to STS-114 only. DSM changes to 4640 for STS-115 and subs.

Antenna Switch/Switch Beam Elec/Antenna LRUs

| DSM                    | ① | Stimulus number | Title                        | MDM        | CMD reset            | HEX set              |
|------------------------|---|-----------------|------------------------------|------------|----------------------|----------------------|
| 4709                   | F | V74K3037U       | S-BD ANT ELEC SW - 1         | PF1<br>PF2 | 710901FF<br>710A01FF | 7909001F<br>790A001F |
| 4710                   | F | V74K3052U       | ANT ELEC SW - OFF            | PF1<br>PF2 | 710901FF<br>710A01FF | 7909002A<br>790A002A |
| 4711                   | F | V74K3036U       | S-BD ANT ELEC SW - 2         | PF1<br>PF2 | 710901FF<br>710A01FF | 7909001E<br>790A001E |
| 4676                   | F | V74K7120U       | SBD QUAD SEL 1-UL/FWD        | PF1        | 20893F00             | 28892200             |
| 4677                   | F | V74K7121U       | SBD QUAD SEL 1-UL/AFT        | PF1        | 20893F00             | 28892100             |
| 4678                   | F | V74K7122U       | SBD QUAD SEL 1-UR/FWD        | PF1        | 20893F00             | 28891200             |
| 4679                   | F | V74K7123U       | SBD QUAD SEL 1-UR/AFT        | PF1        | 20893F00             | 28891100             |
| 4680                   | F | V74K7124U       | SBD QUAD SEL 1-LL/FWD        | PF1        | 20893F00             | 28890A00             |
| 4681                   | F | V74K7125U       | SBD QUAD SEL 1-LL/AFT        | PF1        | 20893F00             | 28890900             |
| 4682                   | F | V74K7126U       | SBD QUAD SEL 1-LR/FWD        | PF1        | 20893F00             | 28890600             |
| 4683                   | F | V74K7127U       | SBD QUAD SEL 1-LR/AFT        | PF1        | 20893F00             | 28890500             |
| 4692                   | F | V74K7220U       | SBD QUAD SEL 2-UL/FWD        | PF2        | 208A3F00             | 288A2200             |
| 4693                   | F | V74K7221U       | SBD QUAD SEL 2-UL/AFT        | PF2        | 208A3F00             | 288A2100             |
| 4694                   | F | V74K7222U       | SBD QUAD SEL 2-UR/FWD        | PF2        | 208A3F00             | 288A1200             |
| 4695                   | F | V74K7223U       | SBD QUAD SEL 2-UR/AFT        | PF2        | 208A3F00             | 288A1100             |
| 4696                   | F | V74K7224U       | SBD QUAD SEL 2-LL/FWD        | PF2        | 208A3F00             | 288A0A00             |
| 4697                   | F | V74K7225U       | SBD QUAD SEL 2-LL/AFT        | PF2        | 208A3F00             | 288A0900             |
| 4698                   | F | V74K7226U       | SBD QUAD SEL 2-LR/FWD        | PF2        | 208A3F00             | 288A0600             |
| 4699                   | F | V74K7227U       | SBD QUAD SEL 2-LR/AFT        | PF2        | 208A3F00             | 299A0500             |
| ① Type: F = single RTC |   |                 |                              |            |                      |                      |
| 4668                   | M |                 | <u>S-BD ANT UL-FWD/UPPER</u> |            |                      |                      |
| 4684                   | F | V74K7130U       | SBD ANT 1-UL/FWD/UP          | PF1        | 2089FF00             | 28896200             |
| 4700                   | F | V74K7230U       | SBD ANT 2-UL/FWD/UP          | PF2        | 208AFF00             | 288A6200             |
| 4669                   | M |                 | <u>S-BD ANT UL-AFT/UPPER</u> |            |                      |                      |
| 4685                   | F | V74K7131U       | SBD ANT 1-UL/AFT/UP          | PF1        | 2089FF00             | 28896100             |
| 4701                   | F | V74K7231U       | SBD ANT 2-UL/AFT/UP          | PF2        | 208AFF00             | 288A6100             |
| 4670                   | M |                 | <u>S-BD ANT UR-FWD/UPPER</u> |            |                      |                      |
| 4686                   | F | V74K7132U       | SBD ANT 1-UR/FWD/UP          | PF1        | 2089FF00             | 28895200             |
| 4702                   | F | V74K7232U       | SBD ANT 2-UR/FWD/UP          | PF2        | 208AFF00             | 288A5200             |
| 4671                   | M |                 | <u>S-BD ANT UR-AFT/UPPER</u> |            |                      |                      |
| 4687                   | F | V74K7133U       | SBD ANT 1-UR/AFT/UP          | PF1        | 2089FF00             | 28895100             |
| 4703                   | F | V74K7233U       | SBD ANT 2-UR/AFT/UP          | PF2        | 208AFF00             | 288A5100             |

| DSM  | ① | Stimulus number | Title                        | MDM | CMD reset | HEX set  |
|------|---|-----------------|------------------------------|-----|-----------|----------|
| 4672 | M |                 | <u>S-BD ANT LL-FWD/LOWER</u> |     |           |          |
| 4688 | F | V74K7134U       | SBD ANT 1-LL/FWD/LO          | PF1 | 1089FF00  | 28898A00 |
| 4704 | F | V74K7234U       | <u>SBD ANT 2-LL/FWD/O</u>    | PF2 | 208AFF00  | 288A8A00 |
| 4673 | M |                 | S-BD ANT LL-AFT/LOWER        |     |           |          |
| 4689 | F | V74K7135U       | SBD ANT 1-LL/AFT/LO          | PF1 | 2089FF00  | 28898900 |
| 4705 | F | V74K7235U       | SBD ANT 2-LL/AFT/LO          | PF2 | 208AFF00  | 288A8900 |
| 4674 | M |                 | <u>S-BD ANT LR-FWD/LOWER</u> |     |           |          |
| 4690 | F | V74K7136U       | SBD ANT 1-LR/FWD/LO          | PF1 | 2089FF00  | 28898600 |
| 4706 | F | V74K7236U       | SBD ANT 2-LR/FWD/LO          | PF2 | 208AFF00  | 288A8600 |
| 4675 | M |                 | <u>S-BD ANT LR-AFT/LOWER</u> |     |           |          |
| 4691 | F | V74K7137U       | SBD ANT 1-LR/AFT/LO          | PF1 | 2089FF00  | 28898500 |
| 4707 | F | V74K7237U       | SBD ANT 2-LR/AFT/LO          | PF2 | 208AFF00  | 288A8500 |

① Type: F = single RTC M = multiword RTC

### 3.7.2 S-Band Transponder LRU

| DSM   | ① | Stimulus number | Title  | MDM        | CMD reset            | HEX set              |
|---|---|-----------------|--|------------|----------------------|----------------------|
| 4730  | F | V74K3076U       | S-BD XPNDR 1 - ON                              | PF1<br>PF2 | 710901FF<br>710A01FF | 7909003E<br>790A003E |
| 4731  | F | V74K3077U       | S-BD XPNDR 1/2 - OFF                           | PF1<br>PF2 | 710901FF<br>710A01FF | 7909003F<br>790A003F |
| 4732  | F | V74K3100U       | S-BD XPNDR 2 - ON                              | PF1<br>PF2 | 710901FF<br>710A01FF | 79090040<br>790A0040 |
| 4733  | F | V74K3101U       | S-BD MODE - TDRS*<br>XPNDR - TDRS MODE*        | PF1<br>PF2 | 710901FF<br>710A01FF | 79090041<br>790A0041 |
| ① Type: F = single RTC * Upper title is pre-STIS-115, lower title is STIS-115 and subs. |   |                 |  |            |                      |                      |
| 4734  | F | V74K3102U       | S-BD MODE - STDN HI*<br>XPNDR - STDN HI MODE*  | PF1<br>PF2 | 710901FF<br>710A01FF | 79090042<br>790A0042 |
| 4735  | F | V74K3103U       | S-BD MODE - STDN LO*<br>XPNDR - STDN LO MODE*  | PF1<br>PF2 | 710901FF<br>710A01FF | 79090043<br>790A0043 |
| 4736  | F | V74K3104U       | S-BD MODE - SGLS*<br>XPNDR - SGLS MODE*        | PF1<br>PF2 | 710901FF<br>710A01FF | 79090044<br>790A0044 |
| 4737  | F | V74K3107U       | S-BD MODE - TDRS RNG*<br>TDRS RANGING (NO OD)* | PF1<br>PF2 | 710901FF<br>710A01FF | 79090047<br>790A0047 |
| 4738  | F | V74K3105U       | SPD SPM - ON                                   | PF1<br>PF2 | 710901FF<br>710A01FF | 79090045<br>790A0045 |
| 4739  | F | V74K3106U       | SPD SPM - OFF                                  | PF1<br>PF2 | 710901FF<br>710A01FF | 79090046<br>790A0046 |
| 4740  | F | V74K3111U       | FREQ - LOW                                     | PF1        | 710901FF             | 79090049             |

| DSM  | ① | Stimulus number | Title                     | MDM | CMD reset | HEX set  |
|--|---|-----------------|---------------------------|-----|-----------|----------|
|  |   |                 |                           |     | 710A01FF  | 790A0049 |
| 4741   | F | V74K3112U       | FREQ - HI                 | PF1 | 710901FF  | 7909004A |
|  |   |                 |                           | PF2 | 710A01FF  | 790A004A |
| 4742   | F | V74K3113U       | S-BD XPNDR MODE- T/R      | PF1 | 710901FF  | 7909004B |
|  |   |                 |                           | PF2 | 710A01FF  | 790A004B |
| 4743   | F | V74K3114U       | S-BD XPNDR MODE- RCV*     | PF1 | 710901FF  | 7909004C |
|  |   |                 | XPNDR RCV ONLY*           | PF2 | 710A01FF  | 790A004C |
| 4470   | S | V74K3361U       | TDRS S-BAND MODE*         | PF1 | 710901FF  | 790900F1 |
|  |   |                 | TDRS MODE (SALVO)*        | PF2 | 710A01FF  | 790A00F1 |
| 4471   | S | V74K3362U       | STDN LOW S-BAND MODE*     | PF1 | 710901FF  | 790900F2 |
|  |   |                 | STDN LO MODE (SALVO)*     | PF2 | 710A01FF  | 790A00F2 |
| 4472   | S | V74K3363U       | STDN HI S-BAND MODE*      | PF1 | 710901FF  | 790900F3 |
|  |   |                 | STDN HI MODE (SALVO)*     | PF2 | 710A01FF  | 790A00F3 |
| 4473   | S | V74K3364U       | SGLS S-BAND MODE*         | PF1 | 710901FF  | 790900F4 |
|  |   |                 | SGLS MODE (SALVO)*        | PF2 | 710A01FF  | 790A00F4 |
| 4474   | S | V74K3366U       | TDRS S-BD CAR MODE        | PF1 | 710901FF  | 790900F6 |
|  |   |                 |                           | PF2 | 710A01FF  | 790A00F6 |
| 4475   | S | V74K3365U       | S-BAND TO KU-BAND         | PF1 | 710901FF  | 790900F5 |
|  |   |                 |                           | PF2 | 710A01FF  | 790A00F5 |
| 4765   | F | V74K3126U       | XPNDR U/L FLTR-NAR        | PF1 | 710901FF  | 79090056 |
|  |   |                 |                           | PF2 | 710A01FF  | 790A0056 |
| 4766   | F | V74K3125U       | XPNDR U/L FLTR-WIDE       | PF1 | 710901FF  | 79090055 |
|  |   |                 |                           | PF2 | 710A01FF  | 790A0055 |
| 4744   | F | V74K3110U       | S-BD R/L DATA - ENA       | PF1 | 710901FF  | 79090048 |
|  |   |                 |                           | PF2 | 710A01FF  | 790A0048 |
| 4745   | F | V74K3170U       | RANGING OFF               | PF1 | 710901FF  | 79090078 |
|  |   |                 |                           | PF2 | 710A01FF  | 790A0078 |
| ① Type: F = single RTC S = salvo RTC                           |   |                 |                           |     |           |          |
| * Upper title is pre-STS-115, lower title is STS-115 and subs. |   |                 |                           |     |           |          |
| 4746   | F | V74K3167U       | RANGING ON                | PF1 | 710901FF  | 79090077 |
|  |   |                 |                           | PF2 | 710A01FF  | 790A0077 |
| 4747   | M |                 | <u>TDRS TRACKING MRTC</u> |     |           |          |
| 4737   | F | V74K3107U       | S-BD MODE - TDRS RNG      | PF1 | 710901FF  | 79090047 |
|  |   |                 |                           | PF2 | 710A01FF  | 790A0047 |
| 4742   | F | V74K3113U       | S-BD XPNDR MODE-T/R       | PF1 | 710901FF  | 7909004B |
|  |   |                 |                           | PF2 | 710A01FF  | 790A004B |
| 4759   | F | V74K3176U       | NSP UPLINK HDR            | PF1 | 710901FF  | 7909007E |
|  |   |                 |                           | PF2 | 710A01FF  | 790A007E |
| 4766   | F | V74K3125U       | XPNDR U/L FLTR-WIDE       | PF1 | 710901FF  | 79090055 |
|  |   |                 |                           | PF2 | 710A01FF  | 790A0055 |

| DSM  | ① | Stimulus number | Title            | MDM | CMD reset | HEX set  |
|------|---|-----------------|------------------|-----|-----------|----------|
| 4470 | S | V74K3361U       | TDRS S-BAND MODE | PF1 | 710901FF  | 790900F1 |
|      |   |                 |                  | PF2 | 710A01FF  | 790A00F1 |
| 4764 | F | V74K3132U       | DNLINK-HDR       | PF1 | 710901F   | 79090053 |
|      |   |                 |                  | PF2 | 710A01FF  | 790A0053 |

### 3.7.3 S-Band Preampfier

| DSM  | ① | Stimulus number | Title                | MDM | CMD reset | HEX set  |
|------|---|-----------------|----------------------|-----|-----------|----------|
| 4722 | F | V74K3071U       | PREAMP 1 - ON        | PF1 | 710901FF  | 79090039 |
|      |   |                 |                      | PF2 | 810A01FF  | 790A0039 |
| 4723 | F | V74K3072U       | PREAMP 1/2 - OFF     | PF1 | 710901FF  | 7909003A |
|      |   |                 |                      | PF2 | 710A01FF  | 790A003A |
| 4724 | F | V74K3073U       | PREAMP 2 - ON        | PF1 | 710901FF  | 7909003B |
|      |   |                 |                      | PF2 | 710A01FF  | 790A003B |
| 4725 | F | V74K3075U       | PREAMP HEATERS - OFF | PF1 | 710901FF  | 7909003D |
| 4726 | F | V74K3074U       | PREAMP HEATERS - ON  | PF1 | 710901FF  | 7909003C |
|      |   |                 |                      | PF2 | 710A01FF  | 790A003C |

① Type: F = single RTC

S = salvo RTC

M = multiword RTC



### 3.7.4 S-Band Power Amplifier

| DSM  | ① | Stimulus number | Title                | MDM               | CMD reset                        | HEX set                          |
|------|---|-----------------|----------------------|-------------------|----------------------------------|----------------------------------|
| 4750 | F | V74K3066U       | S-BD PA STBY - 1     | PF1<br>PF2        | 710901FF<br>710A01FF             | 79090036<br>790A0036             |
| 4751 | F | V74K3067U       | S-BD PA STBY -FF     | PF1<br>PF2        | 710901FF<br>710A01FF             | 79090037<br>790A0037             |
| 4752 | F | V74K3070U       | S-BD PA STBY - 2     | PF1<br>PF2        | 710901FF<br>710Z01FF             | 79090038<br>790A0038             |
| 4754 | F | V74K3063U       | S-BD PA OPR - 1 ON   | PF1<br>PF2        | 710901FF<br>710A01FF             | 79090033<br>790A0033             |
| 4755 | F | V74K3064U       | S-BD PA OPF -1/2 OFF | PF2<br>PF1<br>PF2 | 710A01FF<br>710901FF<br>710A01FF | 790A003D<br>79090034<br>790A0034 |
| 4756 | F | V74K3065U       | S-BD PA OPR - 2 ON   | PF1<br>PF2        | 710901FF<br>710A01FF             | 79090035<br>790A0035             |

### 3.7.5 S-Band Network Signal Processor

| DSM  | ① | Stimulus number | Title              | MDM        | CMD reset            | HEX set              |
|------|---|-----------------|--------------------|------------|----------------------|----------------------|
| 4758 | F | V74K3177U       | NSP UPLINK LDR     | PF1<br>PF2 | 710901FF<br>710A01FF | 7909007F<br>790A007F |
| 4759 | F | V74K3176U       | NSP UPLINK HDR     | PF1<br>PF2 | 710901FF<br>710A01FF | 7909007E<br>790A007E |
| 4760 | F | V74K3120U       | NSP 1 - ON         | PF1<br>PF2 | 710901FF<br>710A01FF | 79090050<br>790A0050 |
| 4761 | F | V74K3121U       | NSP 1/2 - OFF      | PF1<br>PF2 | 710901FF<br>710A01FF | 79090051<br>790A0051 |
| 4762 | F | V74K3122U       | NSP 2 - ON         | PF1<br>PF2 | 710901FF<br>710A01FF | 79090052<br>790A0052 |
| 4763 | F | V74K3124U       | DNLINK - LDR       | PF1<br>PF2 | 710901FF<br>710A01FF | 79090054<br>790A0054 |
| 4764 | F | V74K3123U       | DNLINK - HDR       | PF1<br>PF2 | 710901FF<br>710A01FF | 79090053<br>790A0053 |
| 4767 | F | V74K3127U       | DATA SOURCE - KU   | PF1<br>PF2 | 710901FF<br>710A01FF | 79090057<br>790A0057 |
| 4768 | F | V74K3130U       | DATA SOURCE - S    | PF1<br>PF2 | 710901FF<br>710A01FF | 79090058<br>790A0058 |
| 4770 | F | V74K3131U       | UPLINK CODING - ON | PF1<br>PF2 | 710901FF<br>710A01FF | 79090059<br>790A0059 |

① Type: F = single RTC

M = multiword RTC

| DSM  | ① | Stimulus number | Title                | MDM        | CMD reset            | HEX set              |
|------|---|-----------------|----------------------|------------|----------------------|----------------------|
| 4771 | F | V74K3132U       | UPLINK CODING - OFF  | PF1<br>PF2 | 710901FF<br>710A01FF | 7909005A<br>790A005A |
| 4772 | F | V74K3133U       | DNLINK CODING - ON   | PF1<br>PF2 | 710901FF<br>710A01FF | 7909005B<br>790A005B |
| 4773 | F | V74K3134U       | DNLINK CODING - OFF  | PF1<br>PF2 | 710901FF<br>710A01FF | 7909005C<br>790A005C |
| 4774 | F | V74K3136U       | RCDR VOICE 1/2 - ON  | PF1<br>PF2 | 710901FF<br>710A01FF | 7909005E<br>790A005E |
| 4775 | F | V74K3135U       | RCDR VOICE 1/2 - OFF | PF1<br>PF2 | 710901FF<br>710A01FF | 7909005D<br>790A005D |
| 4776 | F | V74K5079U       | NSP 1 TO RF - ON     | LF1        | 000B0200             | 080B0000             |
| 4777 | F | V74K5080U       | NSP 2 TO UMB - ON    | LF1        | 000B0000             | 080B0200             |
| 4778 | F | V74K5082U       | NSP 2 TO RF - ON     | LF1        | 200B0200             | 280B0000             |
| 4779 | F | V74K5081U       | NSP 2 TO UMB - ON    | LF1        | 200B0000             | 280B0200             |

① Type: F = single RTC

M = multiword RTC

### 3.8 S-BAND PM TELEMETRY LIST

#### 3.8.1 Antenna Switch and Switch Beam Electronics

V74X4782E S-BAND ANT SW ASSY PWR ON - 1  
V74X4783E S-BAND ANT SW ASSY PWR ON - 2

A logic "1" indicates power applied to the indicated ANT SW ASSY electronics.

V74X6491E S-BAND SW BEAM CNTL ASSY ON - 1  
V74X6492E S-BAND SW BEAM CNTL ASSY ON - 2

A logic "1" indicates power applied to the indicated SWITCH BEAM CNTL ASSY

V74X7214E PM ANT SEL 1/2 - GPC  
V74S7215E PM ANT SEL 1/2 - UL FWD  
V74S7216E PM ANT SEL 1/2 - UR FWD  
V74S7217E PM ANT SEL 1/2 - LL FWD  
V74S7218E PM ANT SEL 1/2 - LR FWD  
V74S7315E PM ANT SEL 1/2 - UL AFT  
V74S7316E PM ANT SEL 1/2 - UR AFT  
V74S7317E PM ANT SEL 1/2 - LL AFT

These TLM points indicate the position of the crew antenna select switch. All TLM points low ("0") indicate loss of power or PM ANT SEL 1/2 - LR AFT.

V74X4780E XPNDR 1 Direct  
V74X4781E XPNDR 2 Direct  
V74X4778E Preamp Low Freq (ANT sw)

A logic "1" indicates the mode specified.

V74X7070E S-band Quad Ant Sel S1A ON  
V74X7074E S-band Quad Ant Sel S2A ON  
V74X7078E S-band Quad Ant Sel S3A ON  
V74X7082E S-band Quad Ant Sel S4A ON  
V74X7072E S-band Quad Ant Sel S1B ON  
V74X7076E S-band Quad Ant Sel S2B ON  
V74X7080E S-band Quad Ant Sel S3B ON  
V74X7084E S-band Quad Ant Sel S4B ON

A logic "1" indicates the position of the S-band antenna switch coax switches.

#### 3.8.2 Switch Beam Antenna

V74X7090E S-BD QUAD ANT UPPER LEFT FWD  
V74X7091E S-BD QUAD ANT UPPER LEFT AFT  
V74X7092E S-BD QUAD ANT UPPER RIGHT FWD  
V74X7093E S-BD QUAD ANT UPPER RIGHT AFT

|           |                               |
|-----------|-------------------------------|
| V74X7094E | S-BD QUAD ANT LOWER LEFT FWD  |
| V74X7095E | S-BD QUAD ANT LOWER LEFT AFT  |
| V74X7096E | S-BD QUAD ANT LOWER RIGHT FWD |
| V74X7097E | S-BD QUAD ANT LOWER RIGHT AFT |

A logic "1" indicates the coax switch position in the switch beam antennas.

### 3.8.3 Transponder

|           |                             |
|-----------|-----------------------------|
| V74X4791E | S-BD XPNDR RNG - OFF        |
| V74X4789E | S-BD PM XPNDR SGLS mode     |
| V74X4788E | S-BD PM XPNDR STDN HI mode  |
| V74X4787E | S-BD PM XPNDR STDN LOW mode |
| V74X4786E | S-BD PM XPNDR TDRS mode     |

A logic "1" indicates the mode selected/commanded. If TDRS RNG mode is selected, V74X4791E will indicate a "0" (range is ENABLED).

|           |                             |
|-----------|-----------------------------|
| V74X4792E | S-BD XPNDR Freq Lo (preamp) |
| V74X4793E | S-BD XPNDR Freq Hi (preamp) |

A logic "1" indicates the frequency mode selected by GCIL command. GCIL fail state is "FREQ HI."

|           |                              |
|-----------|------------------------------|
| V74X4790E | S-BD XPNDR SPD Spectrum DSBL |
|-----------|------------------------------|

A logic "0" when spread spectrum mode selected by GCIL command. GCIL fail state is "0" (enabled).

|           |                        |
|-----------|------------------------|
| V74X4735E | S-BD PM XPNDR R/L data |
|-----------|------------------------|

A logic "1" indicates the XPNDR return link data are ON.

|           |                             |
|-----------|-----------------------------|
| V74X4741E | S-BD PM XPNDR T/R mode      |
| V74X4743E | S-BD PM XPNDR RCV only mode |

A logic "1" indicates the mode selected. GCIL fail state is "XPNDR T/R MODE."

|           |                    |
|-----------|--------------------|
| V74X4745E | S-BD PM XPNDR 1 ON |
| V74X4746E | S-BD PM XPNDR 2 ON |

A logic "1" indicates which transponder is selected.

|           |                         |
|-----------|-------------------------|
| V74X9151E | S-band XPNDR Coherent 1 |
| V74X9152E | S-band XPNDR Coherent 2 |

A logic "1" indicates the transponder has switched to the coherent mode (see receiver acquisition algorithm, Figure 3-8).

|           |                           |
|-----------|---------------------------|
| V74X4090E | S-band XPNDR Phase Lock 1 |
| V74X4091E | S-band XPNDR Phase Lock 2 |

A logic "1" indicates the transponder is phase locked (see receiver acquisition algorithm, Figure 3-8).

V74B4086A S-band Loop Stress 1  
V74B4087A S-band Loop Stress 2

An analog parameter (-90 to +90 kHz) indicating the frequency offset of the receiver VCXO.

V74E4080A S-band PM XPNDR 1 AGC S/S  
V74E4081A S-band PM XPNDR 2 AGC S/S

An analog parameter (-142 to -30 dBm) indicating the received signal strength by combining the receiver coherent and noncoherent Automatic Gain Control (AGC) voltages.

V74E4088A S-Bd XPNDR RF Pwr Out 1  
V74E4089A S-Bd XPNDR RF Pwr Out 2

An analog parameter (0 to 5 W) indicating transponder RF output power in the SGLC and STDN LO mode.

### 3.8.4 Preamplifier

The preamplifier does not have any telemetry which will directly provide information on its performance; however, the transponder AGC, when compared to expected RF levels, will indicate any loss of gain the preamplifier may have. The preamplifier gain is 23 - 25 dB.

V74X4776E Preamp 1 ON  
V74X4777E Preamp 2 ON

A logical "1" indicates which preamplifier is selected.

V74X4707E Preamp 1 Heater ON  
V74X4708E Preamp 2 Heater ON

A logical "1" indicates both preamp heaters are on. GCIL fail state is both heaters on.

### 3.8.5 Power Amplifier Configuration

V74X4784E Pwr Amp 1 Operate  
V74X4785E Pwr Amp 2 Operate

A logic "1" indicates which power amplifier is selected to operate.

V74X4747E Pwr Amp 1 Standby  
V74X4749E Pwr Amp 2 Standby

A logic "1" indicates which power amplifier is in standby mode.

V74E4512A S-band Pwr Amp RF Out 1  
V74E4513A S-band Pwr Amp RF Out 2

These are analog signals (0 to 150 W) which indicate the RF power output of the power amplifier. Nominal value is 147 W.

V74E4540A          Pwr Amp Reflected Pwr 1  
V74E4541A          Pwr Amp Reflected Pwr 2

These are analog signals (0 to 200 W) which indicate the amount of RF that is reflected back into the power amplifier if there is a mismatch in the power amplifier output circuit.

V74T4514A          S-band Pwr Amp 1 Temperature  
V74T4515A          S-band Pwr Amp 2 Temperature

These are analog signals (+32° to +226° F) which monitor the power amplifier collector temperature.

### 3.8.6 NSP Configuration

V74X4760E          NSP Power 1 ON  
NOT ON OI BUT ON GPC DOWNLIST  
V74X4761E          NSP Power 2 ON

A logic "1" indicates which NSP is selected.

V74X4795E          NSP Uplink Data Source S-band  
V74X4758E          NSP Uplink Data Ku-band  
V74X4753E          NSP Data Rate Xmit High  
V74X4754E          NSP Data Rate Xmit Low  
V74X4794E          NSP Data Rate RCV High  
V74X4756E          NSP Data Rate RCV Low  
V74X4797E          NSP Coding Xmit ON  
V74X4751E          NSP Coding Xmit OFF  
V74X4796E          NSP Coding RCV ON  
V74X4752E          NSP Coding RCV OFF  
V74X4798E          NSP RCDR Voice Chan 1/2 OFF  
V74X4799E          NSP RCDR Voice Chan 1/2 ON

A logic "1" indicates which function is selected.

V74X5188E          NSP Bit Sync Lock 1  
V74X5189E          NSP Bit Sync Lock 2

A logic "1" indicates lock if the bit sync lock detector reaches threshold after integrating for 214 symbol times (760 ms). The lock detector threshold changes for each mode (DOD or NASA, decoding on or off).

V74V9201A          NSP Bit Error Rate 1  
V74V9202A          NSP Bit Error Rate 2

These parameters work only in TDRS mode. In STDN and SGLS modes, a high reading will occur because the convolutional decoder is seeing only 1/3 of the data necessary for a correct reading.

V74X5176E        NSP Frame Sync Lock 1  
V74X5177E        NSP Frame Sync Lock 2

A logic "1" indicates lock when two consecutive frame sync patterns are verified (<3 errors) and remains a "1" until three frame sync patterns (>3 errors) fail the pattern check.

V74X5180E        NSP MSG Valid 1  
V74X5181E        NSP MSG Valid 2

A logic "1" indicates that a 128-bit BCH coded command has passed the BCH parity check (77 parity bits), has a valid (nonzero) vehicle address, and frame sync lock was in lock before and after receipt of the command.

V74X5184        NSP 1 BITE fail  
V74X5185        NSP 2 BITE fail

A logic zero indicates proper operation of the forward link voice (AG1 and AG2) buffers, the return link voice (AG1 and AG2) buffers, and that there has not been an NSP 10 V dc supply undervoltage condition. Failure of any one of these functions for 0.5 sec will cause the parameters to indicate FAIL.

### NSP Output Message Format

#### Word 1

Bit 1 - Data Ready  
Bit 2 - Data Inhibit ("Block All")  
Bits 3-16 - Bite Status bits

#### Word 2-31

16-bit words - 10, 48-bit commands

#### Word 32

Bit 1    CMD 1 Status through  
Bit 10    CMD 10 Status

NSP output message status

NSP output message status is contained in word 1 of the message as follows:

V92X6081X Data Ready Stat B1 RDY = ("1") NO = ("0")

NSP SIO Word 1 Bit 1 parameter

RDY indicates one command word in the 10 command double buffer has passed:

- BCH DECODER CHECK
- VALID VEHICLE ADDRESS CHECK (any nonzero address)
- BUFFER FILL TIME COMPLETE

NO indicates no commands received or no valid commands received

V92X6082X NSP CMD PATH B2 BLK = ("1") CMD = ("0")

NSP SIO Word 1 Bit 2 parameter

BLK indicates panel C3, UPLINK BLOCK switch in the NSP BLOCK position and only word 1, the status word, is transmitted.

CMD indicates panel C3, UPLINK BLOCK switch in the GPC BLOCK or ENABLE position, or power to the switch was lost.

V92X6083X Bit SYNC Lock B3 LOSS = ("1") BIT = ("0")

NSP SIO Word 1 Bit 3 parameter

BIT indicates the NSP bit sync threshold detector threshold has been exceeded and bit sync is in lock.

LOSS indicates the NSP bit sync is out of lock due to one or more instances of bit sync loss.

V92X6084X Frame SYNC Lock B4 LOSS = ("1") FRM = ("0")

NSP SIO Word 1 Bit 4 parameter

FRM indicates the NSP frame sync lock logic has detected two consecutive frame sync correlations with three or less frame sync errors.

LOSS indicates the NSP frame sync lock logic has detected three consecutive frame sync correlation failures and NSP forward link data processing is inhibited.

V92X6085X Bracket Data B5 LOSS = ("1") BRKT = ("0")

NSP SIO Word 1 Bit 5 parameter

BRKT indicates the NSP sync lock logic has indicated lock and has received two consecutive valid frame sync correlations, and data bracketed by the sync correlations is valid.



LOSS indicates one or more sync correlation failures have occurred and NSP command and Doppler data processing is inhibited.

V92X6086X DEMUX Check B6 FAIL = ("1") NORM = ("0")

NSP SIO Word 1 Bit 6 parameter (see V92X6096X NSP status B16)

FAIL indicates a data overflow or underflow condition has been detected in one or both forward link voice buffers due to a timing or data transmission error.

NORM indicates both forward link buffers are operating properly in high data rate (HDR) or Low Data Rate (LDR), or no signal is present.

V92X6087X MUX Check B7 FAIL = ("1") NORM = ("0")

NSP SIO Word 1 Bit 7 parameter (see V92X6096X NSP status B16)

FAIL indicates a data overflow condition has been detected in one or both return link voice buffers due to a timing or data transmission error.

NORM indicates all other conditions.

V92X6088X Internal Mode B8 INTL = ("1") EXTL = ("0")

NSP SIO Word 1 Bit 8 parameter (see V92X6096X NSP status B16)

INTL indicates the NSP has detected a failure of the PCMMU sync word in three successive frames, or failure of the 100 PPS sync signal or 1.152-MHz clock. The NSP in internal mode provides the data stream with a sync pattern and alternating 1's and 0's in the TLM data (PCMMU) blocks. Voice data are available in this mode.

EXTL indicates normal operation of the NSP.

V92X6089X SEC PWR Check B9 FAIL = ("1") NORM = ("0")

NSP SIO Word 1 Bit 9 parameter

FAIL indicates a momentary loss of the NSP 10-V regulator output and NSP data at the time of the undervoltage will be in error.

NORM indicates the 10-V regulator is operating properly.

V92X6090X RCD Mode Mux B10 FAIL = ("1") NORM = ("0")

NSP SIO Word 1 Bit 10 parameter

FAIL indicates one or more errors have been detected in bits 6 ("0") and 7 ("1") of the record mode frame sync pattern. Check is only done in the record data/voice mode.

NORM indicates all other conditions.

V92X6091X Bit SYNC QUAL B11 FAIL = ("1") NORM = ("0")

NSP SIO Word 1 Bit 11 parameter

FAIL indicates the data level is below threshold level. Threshold levels are set at a given signal to noise ratio dependent on the mode selected as follows: LOCK - 5 dB, NASA CODED - 3 dB, DOD CODED 0 dB, NASA UNCODED + 4 dB, and DOD UNCODED + 7 dB. Minimum bit error for lock is 10<sup>-2</sup>.

NORM indicates signal above mode threshold and bit sync is in lock.

V92X6092X BCH VAL B12 VAL = ("1") NO = ("0")

NSP SIO Word 1 Bit 12 parameter

VAL indicates at least one correct decoded message has occurred since the last MDM polling. Messages are checked for BCH code and nonzero vehicle address.

NO indicates no command words pass the BCH combined parity check and the vehicle address is zero.

V92X6093X BCH INVL B13 INVL = ("1") NO = ("0")

NSP SIO Word 1 Bit 13 parameter

INVL indicates at least one incorrect decoded message has occurred since the last MDM polling.

NO indicates no commands were sent or all commands passed the BCH check.

V92X6094X Mode Parity Even B14 EVEN = ("1") BLANK = ("0")

NSP SIO Word 1 Bit 14 parameter

EVEN indicates the mode logic equation is a logic "1".

$(PS \oplus ENCODING) \oplus (DECODING \oplus DOD) \oplus (RCV HI) = ("1")$

See Table 3-10 for possible combinations.

V92X6095X Mode Parity Odd B15 ODD = ("1") BLANK = ("0")

NSP SIO Word 1 Bit 15 parameter

This parameter is the logic inversion of V92X6094X "MODE PARITY EVEN."

**Table 3-10. Mode parity check**

| Mode      | PS | ENC | DEC | DOD | HI | Parity (V92X6094X)<br>BIT 14 |
|-----------|----|-----|-----|-----|----|------------------------------|
| TDRS      | 0  | 1   | 1   | 0   | 0  | 0 (Odd)                      |
| STDN - LO | 0  | 0   | 0   | 0   | 1  | 1 (Even)                     |
| STDN - HI | 0  | 0   | 0   | 0   | 1  | 1 (Even)                     |
| SGLS (1)  | 0  | 0   | 0   | 1   | 1  | 0 (Odd)                      |
| SGLS (2)  | 1  | 0   | 0   | 1   | 1  | 1 (Even)                     |
| SGLS (3)  | 0  | 0   | 0   | 1   | 0  | 1 (Even)                     |
| SGLS (4)  | 1  | 0   | 0   | 1   | 0  | 0 (Odd)                      |
| SGLS (5)  | 0  | 0   | 0   | 0   | 1  | 1 (Even)                     |
| SGLS (6)  | 0  | 0   | 0   | 0   | 0  | 0 (Odd)                      |

V92X6096X NSP Status B16 FAIL = ("1") GOOD = ("0")

NSP SIO Word 1 Bit 16 parameter

GOOD indicates proper operation of the forward link voice buffers (AG1 and AG2) and the return link voice buffers (AG1 and AG2), and that there has not been an NSP 10-V dc supply undervoltage condition. Failure of any one of these functions for 0.5 sec or more will cause the parameter to indicate FAIL.

### 3.8.7 NSP/COMSEC Configuration

|           |                      |
|-----------|----------------------|
| V76X3065E | COMSEC 1 RPC A - ON  |
| V76X3066E | COMSEC 1 RPC B - ON  |
| V76X3067E | COMSEC 2 RPC A - ON  |
| V76X3068E | COMSEC 2 RPC B - ON  |
| V74X5390E | NSP 1 RCV ENCRYPTED  |
| V74X5391E | NSP 1 XMIT ENCRYPTED |
| V74X5392E | NSP 1 RCD ENCRYPTED  |
| V74X5590E | NSP 2 RCV ENCRYPTED  |
| V74X5591E | NSP 2 XMIT ENCRYPTED |
| V74X5592E | NSP 2 RCD ENCRYPTED  |

A logic 1 indicates the function is selected.

V74S5005 ENCRYPT COMSEC 1

A logic 1 indicates COMSEC 1 and COMSEC 2 are power selected.

V74S5007E COMSEC 1 ZEROIZE

A logic 1 indicates COMSEC 1 and COMSEC 2 are selected to be zeroized. (See byte TM).

### 3.8.8 COMSEC Equipment

The functions monitored are as follows.

| Status measurement              | Polarity                    | PCM sampling rate |
|---------------------------------|-----------------------------|-------------------|
| No. 1 - Alarm condition         | One = Alarm                 | 1/S               |
| No. 2 - Transmit - full operate | One = Full operate          | 1/S               |
| No. 3 - Receive - full operate  | One = Full operate          | 1/S               |
| No. 4 - CVM zeroized            | One = Zeroized condition    | 1/S               |
| No. 5 - Master BITE             | One = Equipment operating   | 1/S               |
| No. 6 - Frame sync              | One = In sync               | 10/S              |
| No. 7 - Authenticate            | One = Command authenticated | 50/S              |

Note: In standby mode, the status circuits are not powered except for the crypto variable memory. In the unpowered state status, outputs could be either high (1) or low (0) logic levels. Cycling power to STANDBY and back to operate will update status variables.

Power failure of the KGX-60 will force all status bits to "0".

When the KGX-60 is turned ON (power applied), the bits should read 0001000. When the unit has been filled and is in standby, the bits should read 0110100. When the unit is operating the bits should read 0110111. When idle patterns are sent without authentication time, the NSP will indicate a nonvalid message and BCH errors in the NSP status word. The same happens when convolutional decoder passes errors. The COMSEC 1 (COMSEC 2) status bits from the KGX-60 are defined as follows.

V74X5017E (5018E)

Status 1 is the Alarm Condition indicator. Should a problem exist in either transmit or receive or both, a "1" (high) indicates the KGX-60 is not operating properly (failure of the unit or failure of the memory). A "0" (low) is correct operation. The unit must be in full operate mode to detect an alarm.

V74X5013E (5014E)

Status 2 is the Transmit Full Operate indicator. If a "1", the unit is in transmit or downlink state and fully operable. This is proper operation. A "0" indicates failure of the transmit mode. Other indicators as discussed herein are required to establish the exact problem within the unit.

V74X50015E (5016E)

Status 3 is the Receive Full Operate indicator. If a "1", the unit is in receive or uplink state and fully operable. This is proper operation. A "0" indicates failure of the receive mode. Other indicators, as discussed herein, are required to establish the problem.

If status 3 (RCV FULL OPR) is a "1" and status 2 (XMIT FULL OPR) is a "0", status 4 (CVM ZEROIZED) may indicate a "1". This states the transmit key has been zeroized or the key was not loaded properly. The opposite applies for status 2 being a "1" and status 3 a "0".

V74X5011E (5012E)

Status 4 is the CVM Zeroized indicator. If a "1", the unit's crypto variable memory has been zeroized or erased and the unit is not operable. If a "0", the KGX-60 is operating properly with the proper key in the memory. This is proper operational condition.

Status 4 (CVM ZEROIZED) does not indicate which key is zeroized; only that one or more keys is zeroized.

V74X5003E (5004E)

Status 5 is the Master BITE indicator. If a "1", the unit is operating properly. This is proper operation. A "0" indicates failure of an SRU within the LRU. This status must be compared to the power ON 28 V dc to be valid. The same statement applies to all "0" indicators.

V74X5019E (5020E)

Status 6 is the Frame Sync indicator. If a "1," the data prior to authentication have been frame synchronized. It has the same meaning as the NSP. A "1" is proper operation. A "0" indicates no frame synchronization.

V74X5001E (5002E)

Status 7 is the Command Authenticated indicator. If a "1", all commands are authenticated. This is normal operation when commands are present. A "0" indicates an individual command has not been authenticated. This is normal when fill data is being uplinked instead of commands. Authentication is verified by the BCH validity check in the COMSEC. The message valid status of the NSP and the command authenticate of the KGX-60 operate identically. Both stay high except when a command is not authenticated or a message is not valid, then the indicator goes low.

Any error in the BCH code will cause the 48 bit command to be zeroed by the COMSEC and b passed on to the NSP. The NSP will indicate BCH not valid.

A loss of input clock from the NSP can hold status bits 6 (FRM SYNC) and 7 (CMD AUTH) as "1" or as a "1" and "0" respectively (last memory state prior to failure). True meaning can be determined from NSP FRAME SYNC data. The clock updates both status bits 6 and 7.

Failure or loss of the MTU time word signal is indicated by status bit 7 (CMD AUTH) being a "0" and NSP message valid a "0" over a period of time with time coded commands being uplinked.

Status 7 (CMD AUTH) can be a "1" and NSP message valid a "0". The KGX-60 checks for command authentication and BCH parity. The NSP checks for BCH parity and nonzero vehicle address.

Special cases to be observed and the proper meanings are as follows:

If status 3 (RCV FULL OPR) is a "1" and status 2 (XMIT FULL OPR) is a "0", status 4 (CVM ZEROIZED) may indicate a "1". This indicates the transmit key has been zeroized or the key was not loaded properly. The opposite applies for status 2 being a "1" and status 3 a "0".

Status 4 (CVM ZEROIZED) does not indicate which key (XMIT/RCV) is zeroized; only that one or both keys are zeroized.

When the KGX-60 is turned ON (power applied and in standby), the bits (B1-B7) read 00000000. When the unit has been filled and is in operate, the bits read 0110100.

When idle patterns are sent without TA, the COMSEC will not authenticate the commands, and the NSP will indicate a nonvalid message and BCH errors in the NSP status word. The same occurs when the bit sync or convolutional decoder passes errors.

**Table 3-11. COMSEC quiescent states of status TLM**

| Status       | Bit | Power       | Key loaded |         |                 |
|--------------|-----|-------------|------------|---------|-----------------|
|              |     | (off or on) | Stby       | Operate | Uplink/<br>mode |
| ALARM        | 1   | 0           | 0          | 0       | 0               |
| XMIT         | 2   | 0           | 0          | 1       | 1               |
| RCV          | 3   | 0           | 0          | 1       | 1               |
| CVM ZERO     | 4   | 0           | 0          | 0       | 0               |
| BITE         | 5   | 0           | 0          | 1       | 1               |
| FRM SYNC     | 6   | 0           | 0          | 0       | 1               |
| AUTHENTICATE | 7   | 0           | 0          | 0       | 0 ①             |

① Pulse to "1" indicate command authenticated.

### 3.8.8.1 ESTL Test Results

Electronic Systems Test Laboratory Test Report, SD-274.

- A. With power off at the KGX-60, all status signals are low.
- B. Loss of clock or loss of clock and data into the KGX-60 decryptor causes the KGX-60 FRAME SYNC indication to maintain the status indicated the last time the clock was present.
- C. Loss of data only into the KGX-60 decryptor causes the KGX-60 FRAME SYNC indication and the AUTHENTICATE indication to go low.
- D. Selection of wrong data rate on the KGX-60 will cause the KGX-60 FRAME SYNC indication and the AUTHENTICATE indication to go low. The KGX-60 will pass data to the SSO NSP and the NSP will show good frame sync, but it is not commandable.
- E. Selection of STANDBY on the KGX-60 causes all status indications to go low.
- F. Selection of ZEROIZE on the KGX-60 causes all status indications to go low except CVM ZEROIZED, which goes high.
- G. Improper time (on the forward link data) causes the AUTHENTICATE indication to go low. NSP frame sync is high, but the NSP is not commandable.
- H. Loss of clock into the SSO NSP will cause the NSP FRAME SYNC indication to maintain the status shown the last time clock was present.
  - Power OFF to the KGX-60, removal of clock to the KGX-60 decryptor, selection of STANDBY at the KGX-60, and KGX-60 ZEROIZE all cause loss of clock to the SSO NSP.

### 3.8.8.2 Alarm Meaning

Ref: RSOC task order memo TM 3R1-87-043, July 2, 1987

Unless a specific failure occurs that would cause the MASTER BITE, TRANSMIT FULL OPERATE, or RECEIVE FULL OPERATE status signal to stay high independent of the condition of the box, all status signals (with the possible exception of ZEROIZE) will go low whenever ALARM goes high. Therefore, it is unlikely that you will ever encounter a condition where ALARM is high and either TRANSMIT FULL OPERATE or RECEIVE FULL OPERATE is also high.

### 3.9 SM 076 COMM DISPLAY

This display provides the crew with means of monitoring the actual configuration and condition of the communication system during on-orbit phases. In general, this display will not be viewed at all times; however, an SCM or fault summary message may direct the crew to this display to ascertain the status of the communication system. Figure 3-12 is the communications display format.

An "M" for missing data will be driven in the status column for all parameters listed below. The status column for all parameters processed for out-of-limit conditions will be as described in the applicable paragraphs.



| XXXX/XXX/076   |        | COMMUNICATIONS |        | XX X             | DDD/HH:MM:SS | DDD/HH:MM:SS |
|----------------|--------|----------------|--------|------------------|--------------|--------------|
| S - BAND PM    |        |                | XXXXXS |                  | KU - BAND    |              |
| FREQ           | XXS    | 1              | 2      | PA TEMP          | ±XXXXS       |              |
| ANT ELEC       | XXS    | XXS            | XXS    | GIMBAL TEMP A    | ±XXXXS       |              |
| XPNDR          | XXS    | XXS            | XXS    | B                | ±XXXXS       |              |
| PREAMP         | XXS    | XXS            | XXS    | GYRO TEMP        | ±XXXXS       |              |
| PWR AMPL       |        |                |        | PWR OUT          | XXS          |              |
| OPER           | XXS    | XXS            | XXS    | FRM SYNC         | XXXXS        |              |
| STBY           | XXXXXS | XXXXXS         | XXXXXS | MODE             | XXXXXS       |              |
| PWR OUT        | XXXXS  | XXXXS          | XXXXS  | FAIL SAFE        | XXXXS        |              |
| TEMP           | XXXXS  | XXXXS          | XXXXS  | AUTO K TO S      | XXX          |              |
| NSP            | 1      | 2              |        | AUTO S TO K      | XXX          |              |
| BIT SYNC       | XXXXS  | XXXXS          | XXXXS  | SSOR             | 1            | 2            |
| FRM SYNC       | XXXXS  | XXXXS          | XXXXS  | FRM SYNC         | XXXXS        | XXXXS        |
| BITE           | XXXXXS | XXXXXS         | XXXXXS | PROC STAT        | XXXXS        | XXXXS        |
| COMSEC BITE    | XXXXXS | XXXXXS         | XXXXXS | PWR LEVEL        | ±XX.XS       |              |
|                |        |                |        | STATUS           | X.XS         |              |
| UL DATA SOURCE |        | XXS            |        | GCIL CONFIG      | XXXXS        |              |
| DATA RATE XMIT |        | XXS            |        | CCTV CAMR OVRTMP | XXXXS        |              |
|                | RCV    | XXS            |        |                  |              |              |
| CODING XMIT    |        | XXXXS          |        |                  |              |              |
|                | RCV    | XXXXS          |        |                  |              |              |

( XX )

Figure 3-12. SPEC 76

3.9.1 SM 076 Display Text

Table 3-12 SM 076 display text shows the possible text for each variable and each status (S) field.

Table 3-12. SM 076 COMM display text

| CRT NAME  | UNITS   | DISPLAYED RANGE   | STATUS INDICATORS                    |                  |                  |                  |        |
|---|---|---|--------------------------------------|------------------|------------------|------------------|--------|
|   |   |   | M                                    | H                | L                | ↑                | ↓      |
| S-BAND PM: [1]<br>FREQ<br>ANT ELEC 1,2<br>XPNDR 1,2<br>PREAMP 1,2<br>PWR AMPL OPER 1,2<br>STBY 1,2<br>OUT 1,2<br>TEMP 1,2                     | text<br>text<br>text<br>text<br>text<br>text<br>watts<br>degF         | See Remarks<br>'LO' or 'HI'<br>'blank' or 'ON'<br>'blank' or 'ON'<br>'blank' or 'ON'<br>'blank' or 'ON'<br>'blank' or 'STBY'<br>0 to 150<br>32 to 266   | M<br>M<br>M<br>M<br>M<br>M<br>M<br>M | H<br>H           | L<br>L           | ↑<br>↑           | ↓<br>↓ |
| NSP: BIT SYNC 1,2<br>FRM SYNC 1,2<br>BITE 1,2<br>COMSEC BITE 1,2<br>UL DATA SOURCE [1]<br>DATA RATE XMIT [1]<br>RCV [1]<br>CODING XMIT<br>RCV | text<br>text<br>text<br>text<br>text<br>text<br>text<br>text          | 'YES' or 'NO'<br>'YES' or 'NO'<br>'GOOD' or 'FAIL'<br>'GOOD' or 'FAIL'<br>'S' or 'KU'<br>'LO' or 'HI'<br>'LO' or 'HI'<br>'OFF' or 'ON'<br>'OFF' or 'ON' | M<br>M<br>M<br>M<br>M<br>M<br>M<br>M |                  |                  |                  |        |
| KU-BAND: PA TEMP<br>GMBL TEMP A,B<br>GYRO TEMP<br>PWR OUT<br>FRM SYNC<br>MODE<br>FAIL SAFE<br>AUTO K TO S<br>AUTO S TO K                      | degF<br>degF<br>degF<br>watts<br>text<br>text<br>text<br>text<br>text | -75 to +300<br>-75 to +300<br>-75 to +300<br>0 to 30<br>'YES' or 'NO'<br>'RDR' or 'COMM'<br>'ENA' or 'INH'<br>'ENA' or 'INH'<br>'ENA' or 'INH'          | M<br>M<br>M<br>M<br>M<br>M<br>M<br>M | H<br>H<br>H<br>H | L<br>L<br>L<br>L | ↑<br>↑<br>↑<br>↑ | ↓<br>↓ |
| SSOR<br>FRM SYNC 1,2<br>PROC STAT 1,2<br>PWR LEVEL<br>STATUS  | text<br>text<br>dBm<br>amps   | 'YES' or 'NO'<br>'OK' or 'BAD'<br>+15 to +45<br>0 to +15  | M<br>M<br>M<br>M                     | H<br>H           | L<br>L           |                  |        |
| GCIL CONFIG [2]   | text  | 'PNL' or 'CMD'  | M                                    |                  |                  |                  | ↓      |
| CCTV CAMR OVRTMP  | text  | 'YES' or 'NO'   | M                                    |                  |                  |                  | ↓      |

- ① When both OPER and STBY are the same, OPER takes precedence. PWR AMPL 1 and 2 in STBY or OFF are legal. A blank for both OPER and STBY indicates a malfunction.
- ② GCIL CONFIG is a bilevel measurement indicating that the GCIL has reverted to the panel control for the S-band, Ku-band, and TV configuration functions (“PNL” displayed). Multiple GCIL power supply failures, multiple electrical bus transients, and initial GCIL power-up will result in “PNL” being displayed. GCIL command control may or may not still be available. “CMD” shall be displayed as long as no failures have occurred and GCIL control operations are nominal.

### 3.9.2 Logic Type/MSID

SM 076 COMM display logic listed in

Table 3-12 in the “Logic type/MSID” column.

#### A. S-band PM transponder configuration logic

The following logic is required to generate and display alphanumeric text that indicates the GCIL S-band PM transponder configuration.

| GCIL S-BAND PM<br>XPNDR 1 (ON)<br>V74X4745E | GCIL S-BAND PM<br>XPNDR 2 (ON)<br>V74X4746E | Configuration<br>text output |
|---|---|------------------------------|
| 1   | 0   | 1                            |
| 0   | 1   | 2                            |
| 0   | 0   | OFF                          |
| 1   | 1   | (blank)                      |

#### B. Multiple discrete input comm fault logic

The comm fault bits of these input parameters shall be OR’ed to display a single “M” in the parameter status field.

#### C. S-band PM preamp configuration logic

The following logic is required to generate and display the alphanumeric text that indicates the current GCIL S-band preamplifier configuration.

| GCIL S-BAND<br>PREAMP 1 ON<br>V74X4776E | GCIL S-BAND<br>PREAMP 2 ON<br>V74X4777E | Configuration<br>text output |
|---|---|------------------------------|
| 1                                       | 0                                       | 1                            |
| 0                                       | 1                                       | 2                            |
| 0                                       | 0                                       | OFF                          |
| 1                                       | 1                                       | (blank)                      |

D. S-band PM PWR AMP OPER/STBY configuration logic

The following logic is required to generate and display alphanumeric text that indicates the present configuration of the GCIL S-band amplifiers.

| GCIL S-BAND<br>PM-PWR AMPL<br>1-STBY<br>V74X4747E | GCIL S-BAND<br>PM-PWR AMPL<br>2-STBY<br>V74X4749E | GCIL S-BAND<br>POWER AMPL 1<br>OPERATE<br>V74X4784E | GCIL S-BAND<br>POWER AMPL 2<br>OPERATE<br>V74X4785E | Configuration<br>text output |                   |
|---|---|---|---|------------------------------|-------------------|
|   |   |   |   | Operate<br>(OPER)            | Standby<br>(STBY) |
| 1   | 0   | 1   | 0   | 1                            | OFF               |
| 1   | 0   | 1   | 1   | 1                            | OFF               |
| 1   | 1   | 1   | 0   | 1                            | 2                 |
| 0   | 1   | 0   | 1   | 2                            | OFF               |
| 0   | 1   | 1   | 1   | 2                            | OFF               |
| 1   | 1   | 0   | 1   | 2                            | 1                 |
| 1   | 0   | 0   | 0   | OFF                          | 1                 |
| 0   | 1   | 0   | 0   | OFF                          | 2                 |
| 0   | 0   | 0   | 0   | OFF                          | OFF               |
| 0   | 0   | 1   | 1   | (blank)                      | OFF               |
| 1   | 1   | 0   | 0   | OFF                          | 1/2               |
| 1   | 1   | 1   | 1   | (blank)                      | 1/2               |

### 3.10 SM 2011 ANTENNA DISPLAY

This OPS function display provides control of the GPC automatic Antenna Management (AM) sequence for the S-band and Ku-band antenna systems. Only the S-band portion will be covered. In addition, provisions are made for monitoring the antenna systems and their associated electronics. Figure 3-13 is the antenna display format.

- A. The crewmember will use this display for initial configuration of the automatic antenna management software and control of the antenna management function for the S-band systems. The crewmember may be directed to view the antenna display to exercise control functions or simply to monitor antenna management parameters.
- B. S-band data are formatted below and to the right of the orbiter blockage pattern and look angle plot.

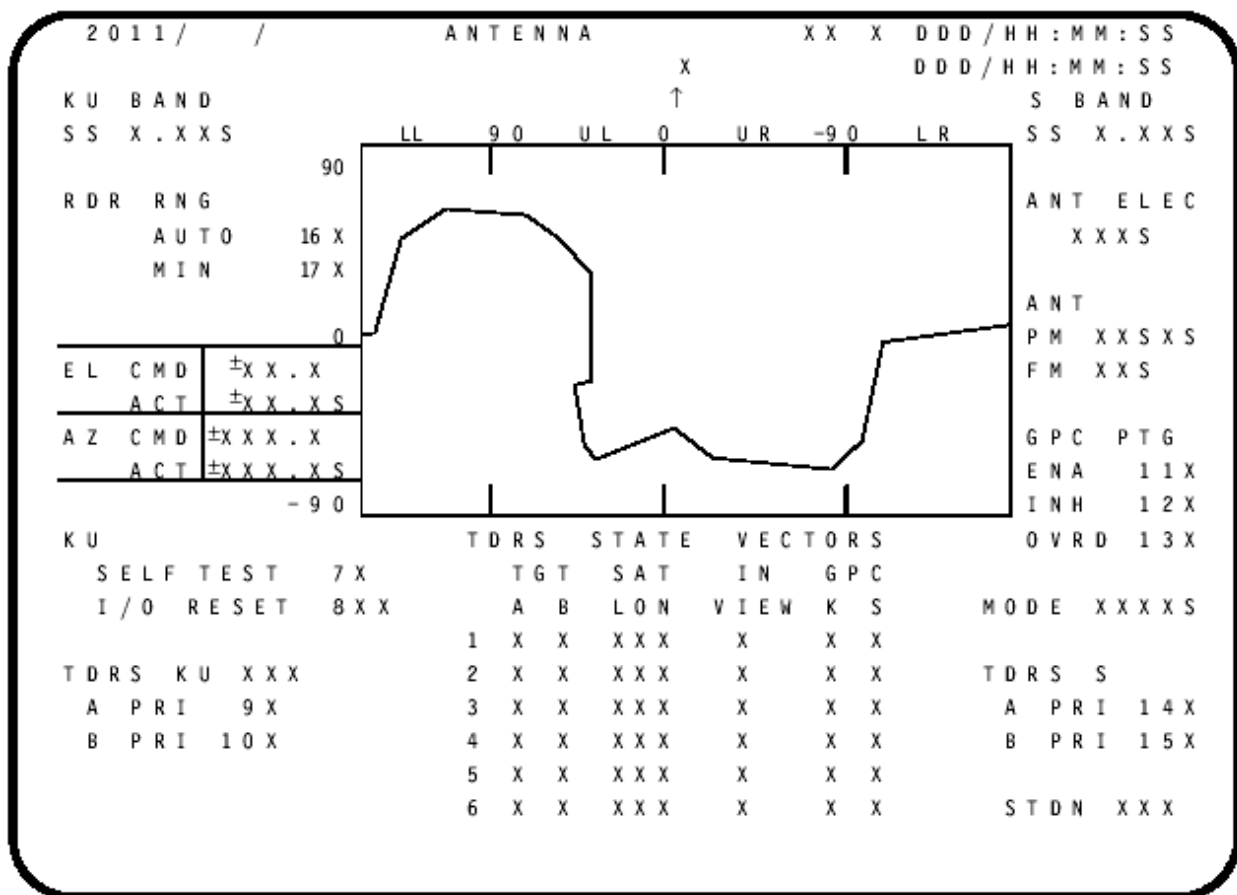


Figure 3-13. SPEC 2011

The S-band system is monitored by a set of measurements defined in the following paragraphs. (Note: In cases where GPC is selecting antennas for the S-band system, the output antenna command is compared with actual selected antennas. If the two do not

compare after three tries, an error message will be generated and annunciated to the crew.)

- A. SIG STR is an analog measurement given in volts dc that represents the uplink received signal strength of the active S-band antenna. The curve used by the SM is as follows:  $SIG STR = 2.5 + 0.005 (PCM CNTS)$
- B. ANT ELEC are discrete measurements that indicate which antenna switch assembly has had power applied to it. The remote text to be displayed is "1", "2", "OFF", or blank.
- C. ANT QUAD and HEMI are discrete measurements that indicate which S-band switch beam QUAD antenna and which S-band HEMI antenna are currently selected by the AM processor, the crew manual antenna switch, or ground uplink command.

The S-band switch beam QUAD antenna status indication is divided into two remote text fields, each having a parameter status and separated by a blank space. The first is a two-character field which will identify the S-band switch beam quadrant antenna; Upper Right (UR), Upper Left (UL), Lower Right (LR), and Lower Left (LL). The parameter status column for this field will be driven with an "M" for missing data or blank. The second is a three-character field which identifies Forward (FWD) or Aft (AFT) direction of antenna switch beam. The parameter status column for this field will be driven with a down arrow (↓) for a miscompare between what is selected and what is commanded, an "M" for missing data, or is blank. If the discretes for both miscompare and missing data are both set, then both the "M" and (↓) will be displayed overlaid simultaneously (↓).

The S-band HEMI antenna status indications is a two-character remote text field which will identify Upper (UP) or Lower (LO) antenna. The parameter status column for this field will be driven with a down arrow (↓) for a miscompare between what is selected and what is commanded, an "M" for missing data, or is blank. If the discretes for both miscompare and missing data are both set, then both the "M" and (↓) will be displayed simultaneously (↓).

- D. MODEs are discrete measurements that indicate the current mode of the active S-band system: TDRS, S-HI (STDN HI), S-LO (STDN LO), or SGLS (DOD SPACE Ground Link System/Station). Results of these discretes are displayed in alphanumeric text.
- E. STDN are discrete measurements that indicate which STDN/SGLS SITE is presently utilized by the AM sequence for automatic S-band antenna pointing. These data are displayed in alphanumeric text.
- F. TDRS indicates which TDRS vector, west or east, is presently being processed and outputting antenna selection information to the S-band antenna. The selected TDRS is displayed in alphanumeric text.

### 3.10.1 Item Entries

The S-band antennas are controlled by use of item entries as defined in the following paragraphs (as referenced by DPS Dictionary):

- |                   |   |
|-------------------|---|
| ITEMS 1 through 6 | TDRS TGT SELECT A or B – used to assign any of the 6 TDRS state vectors, to targets A or B. An '*' is displayed in the 'A' column adjacent to the TDRS state vector slot number (1–6), if that TDRS state vector slot is selected as the 'A' target. An '*' is displayed in the 'B' column adjacent to the TDRS state vector slot number (1–6), if that TDRS state vector slot is selected as the 'B' target. Only one TDRS state vector slot can be assigned to target 'A' or 'B' at a time. The same TDRS state vector slot can be assigned to both 'A' and 'B'.  |
| ITEMS 16 and 17   | RDR RNG – used to control the range estimate output (AUTO or MIN) to the Ku-band Rendezvous Radar/COMM A system. An '*' is displayed next to the selected item. Initialization is in AUTO.  |
| ITEM 7            | SELF-TEST – used to select or terminate the radar self-test function. An '*' appears next to item 7 when the self-test is selected. After the 3-minute test is completed, item 7 must be reexecuted to deselect the self-test function and blank the test results (displayed on the Range meter on panel A2).   |
| ITEM 8            | I/O RESET KU – used to initiate communication between SM GPC and the Ku-band system. An '*' is displayed next to the item whenever the interface is enabled, otherwise an 'M' is displayed. When the SM is initialized, the interface is enabled.   |
| ITEMS 9 and 10    | TDRS KU PRI A/B – item 9 allows the SM Antenna Management (AM) software to select TDRS target 'A' for primary pointing of the Ku-band Comm antenna, if it is in view. If target 'A' is not in view but target 'B' is in view, the target 'B' TDRS satellite will be utilized for pointing. If neither target 'A' nor 'B' is in view, the lowest numbered TDRS state vector slot in view will be utilized for pointing (as denoted by the '*' located in the 'IN VIEW' column of the TDRS STATE VECTORS table). Item 10 allows AM to select TDRS target 'B' for primary pointing if it is in view. If target 'B' is not in view but target 'A' is in view, the target 'A' TDRS satellite will be utilized for pointing. If neither is in view the lowest numbered slot in view will be used for pointing. An '*' is displayed next to the selected item entry. Initialization is in TDRS Ku A PRI. |
| ITEMS 11 and 12   | GPC ANT CMD ENA/INH – used to enable or inhibit AM selection of S-band antennas. An '*' is displayed next to the selected function. ENA is selected at SM initialization.   |
| ITEMS 13          | OVRD – used to force AM to TDRS mode and remain there. This will allow AM to select the best S-Band antenna to TDRS even if there is a status problem preventing AM from knowing what is the correct mode. An '*' is displayed next to the item when it is enabled. The display is initialized with item 13 inhibited.  |
| ITEM 14 and 15    | TDRS S-Band PRI A/B – works the same as the Ku-band PRI A/B function but for the S-Band antennas.   |

**3.10.2 SM 2011 Antenna Display Text**

Table 3-13 SM 2011 antenna display text shows the possible text for each variable and status (S) field.

**Table 3-13. SM 2011 antenna display text**

| CRT NAME   | UNITS                                       | DISPLAYED RANGE                               | STATUS INDICATORS  |                       |   |   |   |        |
|--|---|---|--|-----------------------|---|---|---|--------|
|  |   |   | M  | H                     | L | ↑ | ↓ |        |
| KU BAND: SS<br>ANT EL CMD<br>ACT<br>AZ CMD<br>ACT<br>TDRS Ku | [1]<br><br><br><br>[2]                      | volts<br>deg<br>deg<br>deg<br>deg<br>text     | 0 to 5<br>-99.9 to +99.9<br>-99.9 to +99.9<br>-999.9 to +999.9<br>-999.9 to +999.9<br>'TGT' or blank | M<br><br>M<br><br>M   |   |   |   |        |
| S BAND: SS<br>ANT ELEC<br>PM<br>FM<br>MODE<br>STDN           | [1]<br><br><br>[3] [4]<br>[4]<br>[5]<br>[6] | volts<br>text<br>text<br>text<br>text<br>text | 0 to +5<br>1,2, 'OFF', blank<br>See Remarks<br>'UP' or 'LO'<br>See Remarks<br>See Remarks            | M<br>M<br>M<br>M<br>M |   |   |   | ↓<br>↓ |
| TDRS STATE VECTORS<br>SAT LON 1<br>2<br>3<br>4<br>5<br>6     |   | deg<br>deg<br>deg<br>deg<br>deg<br>deg        | 0 to 360<br>0 to 360<br>0 to 360<br>0 to 360<br>0 to 360<br>0 to 360                                 |                       |   |   |   |        |
| Pictorial Section  | [7]   | text  | See Remarks  |                       |   |   |   |        |

**3.10.2.1 Logic Type/MSID**

These logic types are keyed to the SM 2011 antenna display text,

Table 3-12, in the "Logic type/MSID" column.

**A. Current selected TDRS for Ku-band**

The following logic is required to generate the appropriate RTXT for the current Ku-band TDRS:

| Inputs to IU                                     | State | Text output |
|--|-------|-------------|
| Current selected TDRS<br>for Ku-band (V92J1052C) | 00    | (Blank)     |
|  | 01    | West        |
|  | 10    | East        |



B. Current selected TDRS for S-band

The following logic is required to generate the appropriate RTXT for the selected S-band TDRS. This logic is applicable if the current mode is TDRS.

| Inputs to IU                                    | State | Text output |
|---|-------|-------------|
| Current selected TDRS<br>for S-band (V92J1055C) | 00    | (Blank)     |
|   | 01    | West        |
|   | 10    | East        |

C. Current STDN/SGLS site

A three-letter site designator will be displayed in accordance with antenna management special processing. The following are typical designators and will be controlled by table maintenance.

| Site ID No. | Text output | Site ID No. | Text output |
|-------------|-------------|-------------|-------------|
| 0           | (Blank)     | 8           | GWM         |
| 1           | IOS         | 9           | DKR         |
| 2           | MAD         | 10          | ACN         |
| 3           | GDS         | 11          | AGO         |
| 4           | VDB         | 12          | ORR         |
| 5           | BDA         | 13          | PDL         |
| 6           | MIL         | 14          | BUC         |
| 7           | HAW         | 15          | TUL         |
|             |             | 16          | SPR         |

For further reference, the ground station location tables are defined in the Level C Systems Management FSSR (STS81-0027), Section 6.3.

D. S-band switch beam QUAD and HEMI antenna selected

The following output parameters generated by the SM sequence will enable UI to display the appropriate text in accordance with selection of a switch beam QUAD and HEMI antenna.

| Inputs to IU                        | Logic | Text output |
|-------------------------------------|-------|-------------|
| S-band quad ant sel=<br>(V92J1057C) | 001   | UR (QUAD)   |
|                                     | 010   | LR (QUAD)   |
|                                     | 011   | LL (QUAD)   |
|                                     | 100   | UL (QUAD)   |
| S-band SW beam sel=<br>(V92J1062C)  | 01    | FWD (QUAD)  |
|                                     | 10    | AFT (QUAD)  |
| S-band SW beam sel=<br>(V92J1056C)  | 01    | UP (HEMI)   |
|                                     | 10    | LO (HEMI)   |

Computations governing the selection of a switch beam QUAD and HEMI antenna are defined in the Level C, Systems Management FSSR (STS81-0027); Section 6.3.

E. TDRS LOS roll/pitch angles

The principal function of the plotting symbol is to provide a dynamic indicator for the roll/pitch line of sight look angle to a TDRS. The TDRS, east or west, will be represented by the symbol "E" or "W," respectively. A plotting symbol will appear on the display only if the TDRS is in view of the orbiter. The TDRS in view flag signal is V92X1061X for west and V92X1060X for east. The symbols are driven by the following parameter outputs computed by the AM sequence:

East - "E"

|           |                              |
|-----------|------------------------------|
| V92H1064C | EAST TDRS LOS ROLL ANGLE     |
| V92H1065C | EAST TDRS LOS PITCH ANGLE    |
| V92X1060X | EAST TDRS IN VIEW (Computed) |

West - "W"

|           |                              |
|-----------|------------------------------|
| V92H1066C | WEST TDRS LOS ROLL ANGLE     |
| V92H1067C | WEST TDRS LOS PITCH ANGLE    |
| V92X1061X | WEST TDRS IN VIEW (Computed) |

Conversion of the above roll and pitch angles into CRT addressable units is provided by SM Level C, Section 6.3.

F. Actual angles to TDRS

The actual pointing angle of an antenna will be denoted by the plotting symbol “□” (DUE symbol 1A). This symbol is driven by the following parameter outputs computed by the AM sequence:

Actual - “□”

|           |                                |
|-----------|--------------------------------|
| V74H2618J | Ku-BAND A CH1 ROLL WORD 3 W03  |
| V74H2619J | Ku-BAND A CH1 PITCH WORD 4 W04 |

Conversion of the above roll and pitch angles into CRT addressable units is provided by the Level C Systems Management FSSR (STS81-0027), Section 6.3.

G. Line of site angles to STDN site

The symbol “S” (DUE symbol 53) will represent the roll/pitch line-of-sight angle to an STDN site. This symbol will only appear on the display if the current STDN site is in view. The in view flag signal is V92J1054C when the value is a number other than 0. The symbol is driven by the following parameter outputs computed by the AM sequence.

LOS STDN - “S”

|           |                                       |
|-----------|---------------------------------------|
| V92H1069C | CURRENT SITE LOS ROLL ANGLE COMPUTED  |
| V92H1068C | CURRENT SITE LOS PITCH ANGLE COMPUTED |

Conversion of the above roll and pitch angles into CRT addressable units is provided by the Level C Systems Management FSSR (STS81-0027), Section 6.3.

H. GCIL S-band PM transponder mode comm fault status

The comm fault bits on these parameters shall be OR'd to display an “M” in the parameter status column.

|           |                                |
|-----------|--------------------------------|
| V74X4786E | GCIL-S-band PM XPNDR-TDRS MODE |
| V74X4787E | GCIL-S-band PM LOW XPNDR STDN  |
| V74X4788E | GCIL-S-band PM HI XPNDR STDN   |
| V74X4789E | GCIL-S-band PM XPNDR-SGLS MODE |

I. S-band PM transponder signal strength

The following logic is required to determine the transponder source for the S-band SIGNAL STR value to be displayed:

| Transponder source                        |                                      | GCIL S-band PM                            |                                      | S-BD PM XPNDR AGC SIG STRENGTH parameter to be displayed |
|---|--------------------------------------|---|--------------------------------------|--|
| X<br>P<br>N<br>D<br>4<br>N<br>O<br>5<br>1 | V<br>7<br>4<br>X<br>4<br>7<br>4<br>E | X<br>P<br>N<br>D<br>4<br>N<br>O<br>6<br>2 | V<br>7<br>4<br>X<br>4<br>7<br>4<br>E |  |
| 1   | 0                                    | V74E4080A                                 |                                      |  |
| 0   | 1                                    | V74E4081A                                 |                                      |  |
| 0   | 0                                    | Blank                                     |                                      |  |
| 1   | 1                                    | N/A                                       |                                      |  |

The comm fault bit of the SIG STRENGTH parameter to be displayed shall be used to display the “M” in the parameter status field.

J. GCIL S-band antenna electronics status

The following logic is required to generate the appropriate RTXT for the antenna electronics status.

| Antenna electronics logic                  |  |                    |
|--|--|--------------------|
| GCIL-S-BAND ANT SW ASSY PWR ON 1 V74X4782E | GCIL-S-BAND ANT SW ASSY PWR ON 2 V74X4783E | Status text output |
| 1  | 0  | 1                  |
| 0  | 1  | 2                  |
| 0  | 0  | OFF                |
| 1  | 1  | Blank              |

The comm fault bits on these parameters shall be OR'd to display a single “M” in the parameter status field.

THIS PAGE INTENTIONALLY BLANK

**SECTION 4 – S-BAND TRANSPONDER**  
**CONTENTS**

| <b>Section</b> |                                      | <b>Page</b> |
|----------------|--------------------------------------|-------------|
| 4.1            | GENERAL .....                        | 4-1         |
| 4.2            | INTERFACES .....                     | 4-2         |
| 4.3            | FUNCTIONAL DESCRIPTION .....         | 4-2         |
| 4.3.1          | Receiver.....                        | 4-3         |
| 4.3.2          | Transmitter .....                    | 4-19        |
| 4.3.3          | Control Logic.....                   | 4-24        |
| 4.3.4          | Dual S-Band Triplexer .....          | 4-26        |
| 4.3.5          | RF Coaxial Switches.....             | 4-27        |
| 4.4            | POWER CONSUMPTION .....              | 4-27        |
| 4.5            | WEIGHT .....                         | 4-27        |
| 4.6            | INSTALLATION .....                   | 4-28        |
| 4.7            | DESCRIPTION OF OPERATION .....       | 4-28        |
| 4.7.1          | Crew Controls .....                  | 4-29        |
| 4.7.2          | Crew Displays .....                  | 4-29        |
| 4.7.3          | Ground Commands .....                | 4-29        |
| 4.7.4          | Telemetry.....                       | 4-30        |
| 4.7.5          | Operational Instructions.....        | 4-30        |
| 4.8            | SPECIAL TELEMETRY COMPUTATIONS ..... | 4-30        |
| 4.9            | REFERENCES .....                     | 4-30        |
| 4.10           | SUMMARY DATA.....                    | 4-32        |
| 4.11           | OPERATIONAL NOTES.....               | 4-32        |

## TABLES

| Table |   | Page |
|-------|---|------|
| 4-1   | S-band PM frequencies .....             | 4-1  |
| 4-2   | Transponder modes and frequencies ..... | 4-29 |

## FIGURES

| Figure |   |      |
|--------|---|------|
| 4-1    | Transponder .....                                     | 4-2  |
| 4-2    | Receiver RF acquisition algorithm .....               | 4-6  |
| 4-3    | Spread spectrum processor.....                        | 4-14 |
| 4-4    | Spread spectrum processor acquisition algorithm ..... | 4-16 |
| 4-5    | Control logic.....                                    | 4-25 |
| 4-6    | Coax relay mechanical drawing .....                   | 4-28 |
| 4-7    | Summary data .....                                    | 4-32 |

## SECTION 4 S-BAND TRANSPONDER

### 4.1 GENERAL

The transponder is a multifrequency, multimode Line Replaceable Unit (LRU) capable of receiving and transmitting signals. It is compatible with the Space Ground Link System (SGLS) station, Spaceflight Tracking and Data Network (STDN), and Tracking and Data Relay Satellite (TDRS) operational modes and signal formats. A summary of transponder functions is given below:

- A. Provides two-way coherent communications with SGLS and STDN ground stations or TDRS satellites at the frequency and transpond ratio shown in Table 4-1.
- B. Receive only mode for SGLS, STDN, or TDRS signals.
- C. Despreads the spread spectrum code from the received TDRS signal.
- D. Demodulates Phase Shift Keyed (PSK) signals received from the TDRS or Phase Modulated (PM) signals received from SGLS or STDN.
- E. PM modulates the coherent S-band transmit carrier with wideband data and tone ranging signals in the STDN and SGLS mode. Modulation is PSK in the TDRS mode.
- F. Provides noncoherent data transmission in the absence of a received signal.

The transponder (receiver-transmitter) is the same for all three modes (TDRS, STDN, and SGLS). Frequency synthesis is used to achieve commonality of design for the transmitter drive and the first local oscillator. The TDRS Pseudonoise (PN) code is removed by the spread spectrum processor using a noncoherent code loop which gives fast code acquisition performance.

**Table 4-1. S-band PM frequencies**

| Mode | Frequency | RCV (MHz) | XMIT/RCV ratio | XMIT (MHz) |
|------|-----------|-----------|----------------|------------|
| SGLS | Low       | 1775.733  | 256/205        | 2217.5     |
|      | High      | 1831.787  | 256/205        | 2287.5     |
| STDN | Low       | 2041.947  | 240/221        | 2217.5     |
|      | High      | 2106.406  | 240/221        | 2287.5     |
| TDRS | Low       | 2041.947  | 240/221        | 2217.5     |
|      | High      | 2106.406  | 240/221        | 2287.5     |

<sup>a</sup>Receive frequency times XMIT/RCV ratio equals transmit frequency in the coherent mode. Transmit frequency shown is for noncoherent mode and center frequency in the coherent mode.



## 4.2 INTERFACES

Figure 4-1 shows the transponder interfaces. The controls and displays on panel A1L and the ground command interface logic (commands) for command-only functions are shown going to the transponder and the functional modules they control.

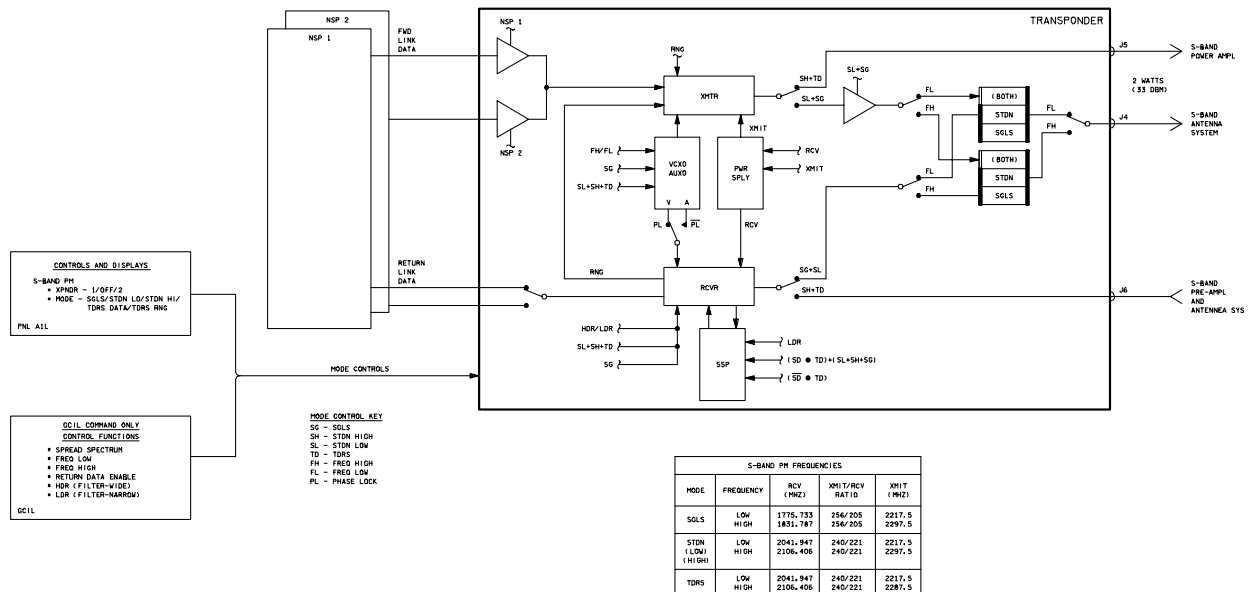


Figure 4-1. Transponder

## 4.3 FUNCTIONAL DESCRIPTION

The received signal, processed through the preamplifier LRU in the TDRS OR STDN HI modes or through the transponder triplexer receive filter (high or low) in the SGLS or STDN LOW direct link modes, is amplified by a low noise S-band preamplifier prior to downconversion to approximately 240 MHz.

A second coherent downconversion brings the signal to 31 MHz, where, in the TDRS mode, despreading is accomplished by the spread spectrum processor, which uses a noncoherent code search loop. The TDRS despread signal is routed to the Costas loop, which is used to derive phase tracking information. In the SGLS and STDN modes of operation, the Costas loop is also used to track the residual carrier. Demodulation of Network Signal Processor (NSP) command/voice data and ranging information is accomplished using an offline wideband phase detector, so that the phase lock loop detector predetection bandwidths can be optimized for tracking performance. Both tone ranging and data outputs from the receiver are noncoherently Automatic Gain Controlled (AGC) to maintain the downlink modulation index and data voltage respectively.

All frequencies are derived from two switchable Voltage Control Crystal Oscillator (VCXO) subassemblies and one reference crystal oscillator. The reference oscillator

operates at 31 MHz, and thus places the second Intermediate Frequency (IF) at 31 MHz. This is sufficiently high in frequency to provide good first IF image rejection and still allow the use of narrowband second IF filters. Channel selection is provided by changing the VCXO frequency. Each VCXO subassembly contains four VCXOs for two-channel operation in either SGLS or STDN/TDRS modes. The two noncoherent transmit frequencies are obtained from a four-channel VCXO (with grounded input) identical to the receiver VCXO. A simple unique multiplier configuration is used, employing phase-locked oscillators to accomplish the X25 (second LO) X14 or X15 (first LO) and X15 or X16 (transmitter drive) multiplication. By simply changing the divider feedback ratios, the multiplication factor can be changed. This technique provides the wide percentage bandwidth multiplication required for multimode operation, while yielding very low spurious products. The final first local oscillator multiplication ratio (X6 or X7) is selected as a function of mode.

The third mixer in the second LO chain offsets the second LO frequency using a 62-MHz reference signal, so that the second IF is fixed and does not vary as a function of received frequency. Therefore, the spread spectrum processor and the Costas detector preselection filters can be operated at very low Signal-To-Noise Ratios (SNRs) and at the same center frequency, regardless of input channel selection. The drive frequencies to the third mixer are at twice the first IF and twice the reference oscillator frequency. This eliminates the potential problem of generating a high-level signal at the third mixer exactly equal to the first IF frequency, which could result in a self-lock condition. An additional advantage is that by using an "offset" oscillator and thus placing the high gain second IF at a frequency noncoherently related to the S-band input signals, regeneration or self-lock problems are eliminated that can otherwise arise in systems where the second IF is at submultiple of the S-band input frequency.

Downlink STDN and SGLS linear modulation is accomplished at about 560 MHz and then multiplied by 4 to S-band. The original TDRS mode biphase modulator was eliminated in favor of linear modulation at 560 MHz ( $\pm >/8$ ) and multiplication to S-band (X4) in order to avoid undesired sidebands which would have caused payload receiver interference.

An S-band solid state power amplifier provides a low level (TDRS/STDN HIGH) or high level output (STDN LOW/SGLS), depending on mode selection.

The dual S-band triplexer combines two independent triplexers in a common housing. Each triplexer, one for the low frequency mode and one for the high frequency mode, is configured as a three-port network consisting of three narrowband bandpass filters, and a low pass filter.

#### 4.3.1 Receiver

The receiver searches for and acquires S-band residual carrier, PSK, or spread spectrum signals in any of four prime modes and any of four S-band frequencies.

Received S-band Radio Frequency (RF) signals are amplified via a low noise (4 dB NF) preamplifier and downconverter to a first IF frequency at  $25 f_0$  (216.5 to 238.3 MHz).

Downconverted first IF signals are routed to either of two selectable (via PIN diode switches) IF filters, one serving the SGLS input frequencies, and the other serving the STDN or TDRS input frequencies. First IF amplification and gain management are provided by two identical cascaded hybrid microcircuit AGC amplifiers. These amplifiers provide in excess of 58 dB of IF gain and more than 60 dB of AGC dynamic range. Post-AGC first IF filtering attenuates spurious responses and noise in the second IF image band prior to a second downconversion to 31 MHz. The composite first IF filters provide sufficient skirt rejection to place all specified interfering signal levels at least 20 dB below the IF noise at threshold. After the second downconversion, the IF band is limited to 28-MHz 3-dB bandwidth, amplified, and noncoherently controlled to a level of -19 dBm at the Spread Spectrum Processor (SSP) interface. The 28-MHz bandwidth second IF filter ensures greater than 22.5-MHz bandwidth is available for TDRS spread spectrum signals. The noncoherent AGC applied to the first IF gain control amplifiers and second IF AGC amplifier holds the total signal and noise power to the spread spectrum processor to  $-19 \pm 1.3$  dBm. Maintenance of this interface level is critical to the operation of the SSP. After the second IF signal has been noncoherently AGC'd, it is routed either to the SSP (TDRS spread spectrum mode), or routed directly to downstream IF processing circuitry (all other modes). For all modes other than TDRS spread spectrum, the IF signal bandwidth is narrowed to 12 MHz and coherently AGC'd prior to data demodulation. The IF signal spectrum used for phase tracking is further narrowed by a 1-MHz bandwidth predetection filter and amplified prior to detection by the Costas loop circuitry. The 1-MHz IF bandwidth has been determined to be optimum from the viewpoint of required phase detector dynamic range and acceptable data distortion. The loop phase detection and coherent amplitude detection circuitry are configured as a Costas I-Q detector. The I-Q detector arms contain selectable bandwidth low pass filters, providing single-pole 3-dB responses of 308 kHz for TDRS high data rate, or 134 kHz for all other modes. The tracking phase error signal is formed as the product of the I and Q channels, and a coherent amplitude estimate is formed by the difference of the squared outputs of the I and Q arms ( $I^2 - Q^2$ ). The arms of the Costas I-Q detectors and baseband multipliers are carefully balanced during production alignment to ensure optimum performance. The phase error signal is processed by the phase lock loop filter prior to controlling the VCXO. The loop filter serves to sweep the VCXO frequency during acquisition, and then to switch to a narrower phase lock loop bandwidth after acquisition.

The amplitude estimate from the Coherent Amplitude Detector (CAD) is filtered by a two-pole variable bandwidth low-pass filter prior to threshold detection by phase lock loop lock detector. The lock detector predetection noise bandwidth is 126 Hz prior to acquisition, and then switched to 15 Hz after acquisition. The lock detector employs two threshold voltages. Prior to acquisition, the threshold is set at 80 percent of the normal CAD output, and after acquisition, the threshold voltage is reduced to 40 percent of the CAD output to decrease the probability of false dismissal. The receiver signal search and acquisition procedure is controlled by the acquisition algorithm shown in Figure 4-2.

Local oscillator signals are formed by indirect frequency synthesis techniques. The indirect synthesis technique offers the advantages of variable multiplication ratios and

excellent spurious performance without the use of complex multipole L-C filters, as is the case with direct multipliers. The first LO signal is formed by an indirect frequency multiplier loop, which multiplies the VCXO frequency by either 14 (STDN or TDRS modes) or by 15 (SGLS mode). The two multiplier ratios are selected by changing the digital divider count modulus in the synthesizer loop. A final fixed multiplication (X6 for SGLS, X7 for STDN or TDRS) by a varactor diode multiplier produces the first LO signal.

The second LO signal is synthesized by multiplying the VCXO by 25 with an indirect loop ( $50 f_o$ ) mixing with twice the reference signal (62 MHz), and dividing the difference frequency by two ( $25 f_o - f_R$ ). The Doppler extractor RF signal at  $10 f_o$  is derived from a tap in the second LO indirect synthesizer loop and buffered to the output through a line driver and resistive pad.

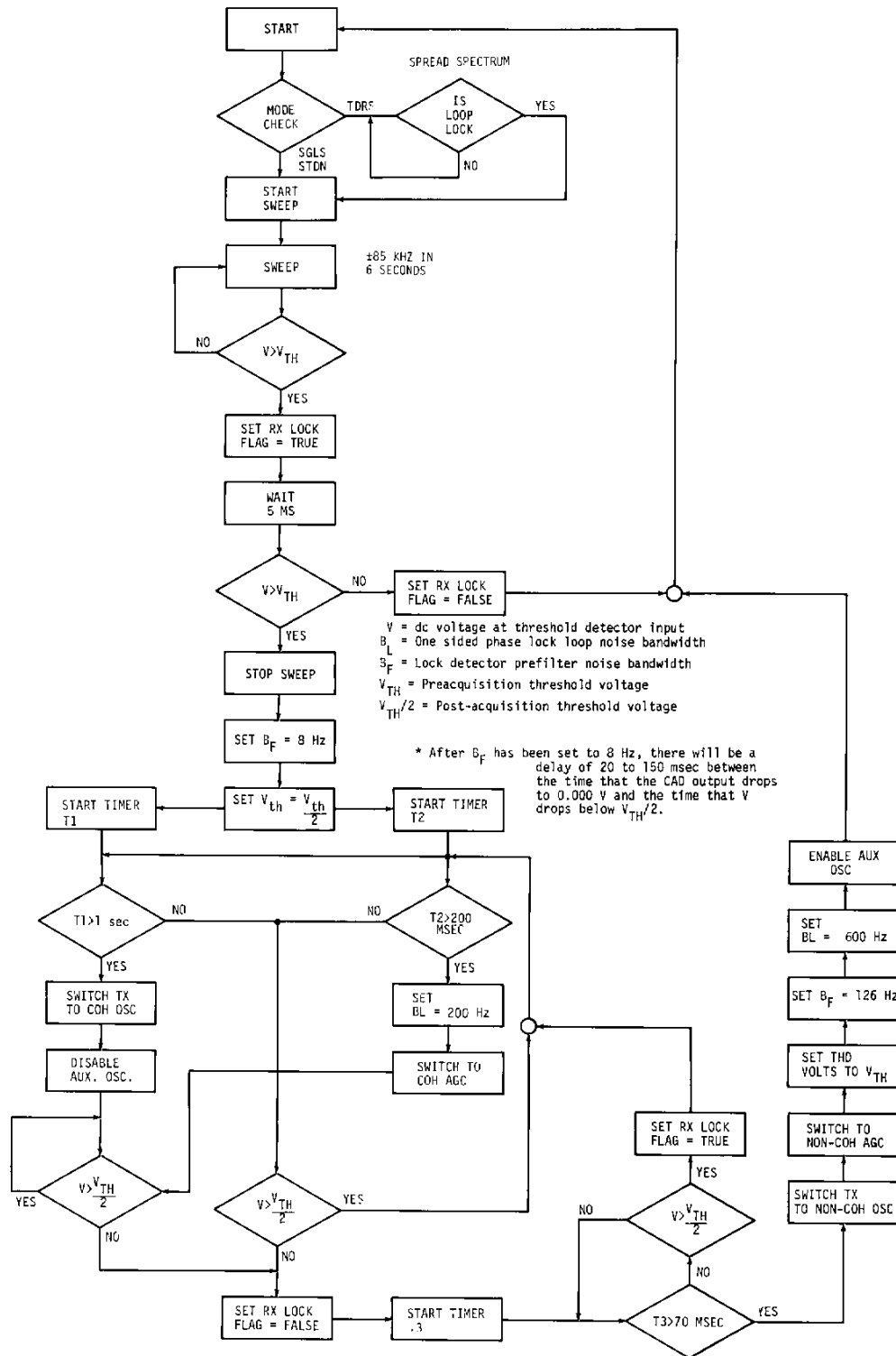


Figure 4-2. Receiver RF acquisition algorithm

#### 4.3.1.1 First Intermediate Frequency

The first IF operates at any one of four different nominal input frequencies. The S-band RF input is preamplified and converted to a first IF frequency in the preamplifier/downconverter. The major parameters for this stage are outlined below:

- Input frequency range 1770 to 2120 MHz
- IF output frequency range 210 to 275 MHz
- LO frequency range 1555 to 1875 MHz
- Conversion gain 22 to 28 dB
- Gain flatness <1 dB variation over any 60-MHz range
- Noise figure 4.0 dB
- Image rejection >20 dB at  $\geq 1641$  MHz

The LO drive is derived from multiplication of an input signal from the source module. In the SGLS mode of operation, the SG/enable command (ON) activates the X6 multiplier; in the STDN/TDRS mode, the SG/enable command (OFF) activates the X7 multiplier.

The multiplier circuits use varactor diodes to generate a frequency comb at multiples of the LO drive signal (300 MHz). The desired harmonic is selected via filtering on the multiplier substrate. Five-pole Tchebycheff filters are used to select the desired output frequency and to provide >50 dB of rejection to all other harmonics. A low loss multiplexer formed by the junction of quarter-wave lines separates the X6 circuit from the X7 network. This approach provides performance equivalent to PIN diode switches without their attendant insertion loss and dc power consumption.

The RF drive for the diode multipliers is supplied by the power amp and switch substrate. The LO drive signal from the source module is amplified to a level of +20 dBm and routed to either the X6 or X7 multiplier through PIN diode switches on the substrate.

The first LO signal output of the X6 and X7 substrate is passed through an isolator prior to driving the preamp/downconverter subassembly. The isolator prevents detuning and ensures stability of the multipliers after their initial alignment.

After downconversion to the first IF, the IF signal is processed by one of two selectable IF bandpass filters. The filters are designed so that one of the filters serves the SGLS prime mode (both frequency high and frequency low secondary modes share this filter), and the other filter serves for both STDN and TDRS requirements. The appropriate filter is selected on external command via PIN diode switches. Each filter is a five-pole Tchebycheff design with sufficient skirt rejection to the specified interfering signal bands to place interfering signals >20 dB below the noise in the filter bandwidth.

The mode bandpass filters are buffered from the AGC amplifiers with a 10-dB pad. The pad minimizes detuning of the bandpass filters over the AGC dynamic range.

Approximately two-thirds of the first IFs total 75-dB AGC dynamic range is supplied by the cascade of two identical IF amplifier microwave integrated circuits. The amplifier circuits contain integral PIN diode attenuators to provide >40 dB of gain control range per circuit. The major electrical characteristics are outlined below:

- Frequency range                      200 to 275 MHz
- Power gain                              29 to 31 dB
- Gain flatness                             $\pm 0.24$  dB
- Noise figure                             $\leq 4.0$  dB (max gain)
- 1 dB gain compression               $\geq 0$  dBm (output)
- Input/output voltage
- Standing wave ratio (VSWR)         $\leq 1.5:1$
- Gain control range                     $\geq 40$  dB

Conditioning circuits modify the AGC control signal from the NON-COH AGC board in order to balance the gain among the three AGC amplifiers.

The AGC network is followed by a five-pole bandpass filter, which, in addition to supplementing the interference rejection of the mode bandpass filters, also band limits the second IF image noise generated in the AGC amplifiers. The output of the post-AGC bandpass filter is buffered from a 2.0:1 input VSWR of the second mixer with a discrete amplifier.

The second mixer LO signal originates in the first IF by mixing of the 62 MHz from the second IF module and an appropriate third LO input signal from the source module. The two inputs are combined in the third mixer, filtered for spur rejection, frequency divided by two, filtered for more spur rejection, amplified, and then supplied to the second mixer.

The net result of the second downconversion is to provide a fixed 31-MHz IF signal under receiver phaselock conditions. The second mixer output is filtered for upper sideband rejection and then amplified by the final stage of the noncoherent AGC.

The noncoherent AGC receives the 31-MHz output of the second mixer, passes it through a 23-MHz bandwidth three-pole Bandpass Filter (BPF) to attenuate upper sideband signals and improve SNR, and couples it to an AGC amplifier. The AGC amplifier has a gain of 34 dB, open loop, and a bandwidth greater than 40 MHz. The output of the AGC amplifier is split into two paths. One path leads to the AGC Amplified Modulation (AM) detector. The output of the AM detector is a dc voltage proportional to

the RF signal and noise level. This voltage is filtered in the high gain AGC loop filter, an active low pass filter, and the dc voltage is fed to the second IF AGC amplifier and to the first IF PIN diode attenuators on the AGC network board. The noncoherent AGC loop bandwidth is nominally 7.5 Hz at receiver tracking threshold. The other path from the output of the AGC amplifier is the RF output of the first IF module and is made available to the second IF and detector module.

#### **4.3.1.2 Receiver Wideband Detector and Second IF**

##### **A. SSP interface and AGC**

The SSP interface and AGC provide the necessary interface between the second IF and the SSP, including facility to switch between spread and nonspread spectrum function. The AGC amplifier is controlled by a noncoherent detector prior to acquisition, and by the coherently generated AGC control voltage after acquisition (receiver locked). The minimum IF gain of this substrate with the AGC amplifier at maximum gain is 20 dB, and the 3-dB bandwidth is approximately 12 MHz. Two outputs are provided, one for the wideband detector and the other for the Costas demodulator.

##### **B. Wideband detector**

The wideband detector substrate coherently demodulates PSK or PM signals. The baseband output is filtered to remove RF signals (31 MHz and harmonics), and recovered data are routed to the NSP after further signal conditioning. Included is the facility to adjust the phase differential between the wideband detector and the tracking phase detector.

##### **C. 31-MHz BPF**

The 31-MHz BPF establishes the predetection bandwidth for the double balanced mixers on the phase detector and CAD. This filter narrows the IF bandwidth to 1.0 MHz and is a three-pole butterworth design.

##### **D. 31-MHz amplifier**

The output of the 31-MHz BPF is coupled to the 31-MHz amplifier. The 31-MHz amplifier has a gain of 27 dB and a 1-dB compression of +4 dBm.

##### **E. Phase detector and CAD**

The phase detector and CAD accept the output of the 31-MHz amplifier and split the signal between the phase detector and the CAD. The phase detector and CAD also receive quadrature-phased reference signals. The RF and reference signals are mixed to form I and Q baseband outputs to the Costas circuit. The phase detector and CAD circuit contain a temperature compensated phase shift to maintain low Bit Error Rate (BER) performance over temperature.



## F. Costas circuit

The Costas circuit Resistor Capacitor (RC) filters amplify and cross-multiply the quadrature I-Q signals to provide phase error information to the phase lock channel. The signals may have no modulation Continuous Wave (CW), PM, or PSK data. Signal strength information is provided by squaring and differencing each signal via analog multipliers. One of the multipliers is used to derive noncoherent AGC control voltage prior to receiver acquisition. The noncoherent AGC prevents saturation prior to acquisition. This voltage is filtered with a two-pole, 3.5-Hz active low pass filter and combined with the coherent AGC control voltage. The line from the noncoherent AGC circuit is opened after receiver acquisition on command from the control logic. Coherent AGC information is obtained by taking the difference of the two multipliers to form  $I^2 - Q^2$  amplitude estimate after receiver acquisition. This difference is proportional to the signal strength. The output of the difference circuit is then supplied to the acquisition bandwidth control. Facility is also provided to switch Costas arm filter bandwidth on command from the control logic. The two bandwidths available are 308 kHz (high data rate), and 134 kHz (low data rate), single-pole response.

## G. Reference oscillator source

The reference signals for all three detectors, Wideband (WB), CAD, and phase detector, are generated by the reference oscillator. This oscillator also generates the 62-MHz reference signal for the third mixer. All frequencies generated are coherent and have a stability of  $\pm 20$  ppm.

## H. 62-MHz BPF

The 62-MHz output of the reference source is filtered by the 62-MHz BPF board to reduce the second harmonic (124 MHz) to provide 40 dB of discrimination against 31-MHz spurious induced phase detector offsets.

**4.3.1.3 Frequency Source Module**

The frequency source module contains indirect frequency synthesis loops used to generate receiver LO signals and transmitter RF drive. The frequency source module performs the following functions:

- Provide inputs to the receiver LO chains with frequencies coherent with the receiver VCXO
- Provide noncoherent RF drive to the transmitter prior to receiver phase lock
- Provide coherent RF drive to the transmitter after receiver phase lock
- Provide a Doppler extractor RF output signal at 5X the receiver VCXO frequency ( $10 f_0$ ). (This capability is not used.)

The main source module design objectives were the following:

- Low output phase noise and spurious signals
- Multimode capability and moderate tuning bandwidths
- Coherent/noncoherent transmitter drive capability
- Moderately fast mode switching
- Low static phase error variation versus temperature
- Synthesizer loop response fast enough to avoid affecting the receiver long loop response

A. First LO loop

The first LO drive signal for the SGLS modes is generated by operating the first LO loop in an X15 mode, while the STDN/TDRS LO signal is formed by operating the loop in an X14 mode. The two multiplication ratios (X14 or X15) are achieved by changing, on command, the modulus of the high-speed digital dividers in the feedback leg of the loop. The digital divider output is phase detected against the receiver VCXO input via a high-speed phase/frequency detector integrated circuit. The phase detector output is filtered by the high gain active loop filter and used to control the loop Voltage Controlled Oscillator (VCO). The VCO operates directly at the output frequency.

The first LO loop produces any of four output frequencies, depending on the selected prime and frequency modes, ranging from 258.7 MHz to 268.1 MHz. Key parameters for this loop are presented below.

First LO Loop Parameter Summary

|                           |  |
|---------------------------|--|
| Loop bandwidth ( $B_L$ ): | $\leq 30$ kHz  |
| Loop damping factor:      | $0.707 \pm 20$ percent   |
| Loop acquisition time:    | $< 30$ msec  |
| Spurious outputs:         | $> 88$ dBd $\pm 45$ to $\pm 56$ MHz from carrier<br>$> 79$ dBd $\pm 56$ to $\pm 76$ MHz from carrier<br>$> 57$ dBd elsewhere |

B. Transmitter drive loop

The transmitter drive loop design is identical to the first LO loop, with the exception that the digital divider modulus is selectable as modulo 15 (STDN/TDRS) or modulo 16 (SGLS). This loop receives RF from the auxiliary (noncoherent) oscillator prior to receiver signal acquisition, and switches to the receiver VCXO after receiver acquisition for coherent turnaround operation. The transmitter drive loop produces two output frequencies, ranging from 277 MHz to 286 MHz. Key parameters for this loop are presented below.

Transmitter Drive Loop Parameter Summary

|                               |  |
|-------------------------------|--|
| Loop bandwidth ( $B_L$ ):     | $\leq 30$ kHz  |
| Loop damping factor:          | $0.707 \pm 20$ percent   |
| Loop acquisition time:        | $< 30$ msec  |
| Spurious outputs:             | $> 83$ dBd 0 to $\pm 34$ MHz offset<br>$> 43$ dBd $\pm 34$ to $\pm 47.5$ MHz offset<br>$> 83$ dBd $\pm 47.5$ to $+85$ MHz offset<br>$> 103$ dBd $-171$ to $-181$ MHz offset<br>$> 41$ dBd all others |
| Noise power spectral density: | $\leq -150$ dBm/Hz $\pm 47.5$ to $\pm 85$ MHz offset   |

C. Second LO loop

The second IF LO loop is similar to the first LO loop, with the exception of higher output frequencies (433 MHz to 476.5 MHz) and fixed modulus divider ratio ( $\div 25$ ). This loop uses the receiver VCXO for the input reference for all modes. The digital divider consists of a cascade of two  $\div 5$  high-speed programmable dividers. A tap is provided between the dividers to form the Doppler extractor output. The Doppler extractor RF signal is buffered from the digital divider circuits by a line driver and resistive pad. Key parameters for this loop are presented below.

Second LO Loop Parameter Summary

|                        |                        |
|------------------------|------------------------|
| Loop bandwidth:        | $< 30$ kHz             |
| Loop damping factor:   | $0.707 \pm 20$ percent |
| Loop acquisition time: | $< 30$ msec            |
| Spurious outputs       |                        |
| Harmonics:             | $> 20$ dBd             |
| Nonharmonics:          | $> 60$ dBd             |

D. Frequency source

The RF switch circuit contains the RF switch that selects either the auxiliary oscillator or coherent (receiver VCXO) oscillator for the transmitter loop. This switch is composed of series and shunt PIN diodes, and provides in excess of 75 dB of isolation between selected parts. This isolation is required in order to maintain the spurious level of the nonselected oscillator greater than 60 dB below the desired output at S-band.

E. VCXO and auxiliary oscillators

The receiver uses a four-channel voltage controlled temperature compensated crystal oscillator as the basic frequency determining element. The oscillator is configured as a single oscillator circuit, using switched crystals to implement the four discrete output frequencies. The output frequencies are at the 2f coherent submultiple of the input frequency, and were selected such that none of the harmonics of the VCXO can fall within any of the IF frequencies. An identical oscillator subassembly is used for noncoherent transmitter auxiliary signal generation during the time before receiver signal acquisition. The voltage control line for the auxiliary oscillator is grounded to force center frequency only operation.

**4.3.1.4 Spread Spectrum Processor**

When the receiver is operated in the TDRS spread spectrum mode, S-band signals spread by a PN code, 1023 bits long and at a rate of 11.232 Mcps are processed to remove the spreading code prior to data demodulation. The spreading code is removed from the signal by the receiver SSP module. This module operates at the receiver second IF frequency of 31 MHz.

The SSP (Figure 4-3) IF input is amplified and split into three channels: the punctual channel, which provides the despread output; the acquisition channel, which contains the circuitry necessary to initially detect proper code alignment; and the tracking channel, which compensates the SSP for code phase variations once the signal is acquired.

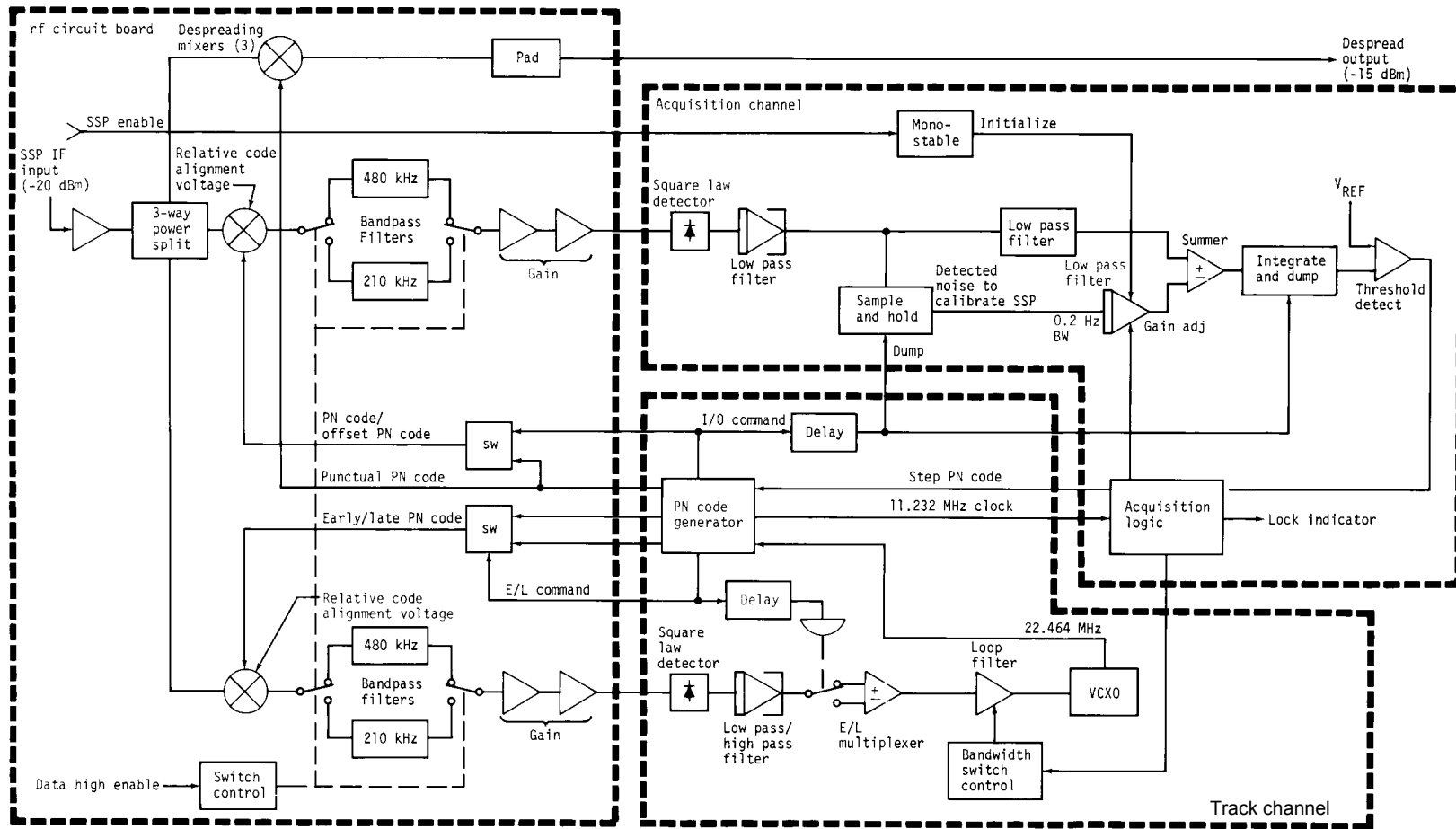


Figure 4-3. Spread spectrum processor

A. Acquisition logic

The acquisition logic section controls the operation of the SSP, stepping the local code phase until acquisition is attained (Figure 4-4).

Considering the RF circuitry in both the acquisition and track channels, both channels are identical through the square law detector diode.

Following the power splitter, each channel contains a despreading mixer. When the locally generated PN demodulated code is aligned in phase with that of the PN code modulation in the IF, an increase in power occurs within a band near the IF center frequency at the output of the mixer. The mixer and bandpass filters in the SSP use this phenomenon to produce an output voltage which is an indication of relative code alignment. The SSP must operate in a very poor SNR environment; therefore, the bandpass filters following the mixers must be optimized for the expected input signal. Two data rates are specified for the TDRS mode, high (216 kbps) and low (96 kbps). The bandpass crystal filters provide optimum performance for these data rates. Beyond the crystal filters, the signal is amplified and detected via a square law diode detector. The square law detector produces a triangular voltage correlation function when the code phases are aligned within one chip.

In the acquisition channel, the local PN is the punctual PN code modulo two, summed with a low duty cycle 10-chip offset code used for calibration.

After the detector diode, the acquisition channel signal is amplified and band-limited. The bandwidth is constrained so that noise present in the channel does not cause amplifier saturation. When the offset code is present at the mixer, no despreading occurs; thus, the output of the initial baseband amplifier is an indication of the detected noise level within the channel. A sample-and-hold circuit samples the detected noise level to calibrate the SSP. A very low cutoff frequency filter (0.2 Hz BW) follows the sample-and-hold circuit to gain a good estimate of the mean noise level within the channel. If during the time when the offset code is not present, the amplifier output is greater than the noise reference level, code phase alignment may have occurred. This is detected by taking the difference of the noise reference level (times a small gain) and the baseband amplifier level. Thus, if a correlation is present, the output of this amplifier will be negative; if no correlation is present, the output is positive. To enhance detection probability, an integrate-and-dump circuit follows the summer; the output of the inverting integrator will be positive at the end of the dwell period if correlation is true, and negative otherwise. The code phase dwell period during the acquisition phase is 547  $\mu$ sec, corresponding to three code intervals. The integrator output is compared to a positive reference voltage at the end of the dwell interval. A high level on this threshold detect signal indicates assumed correlation.

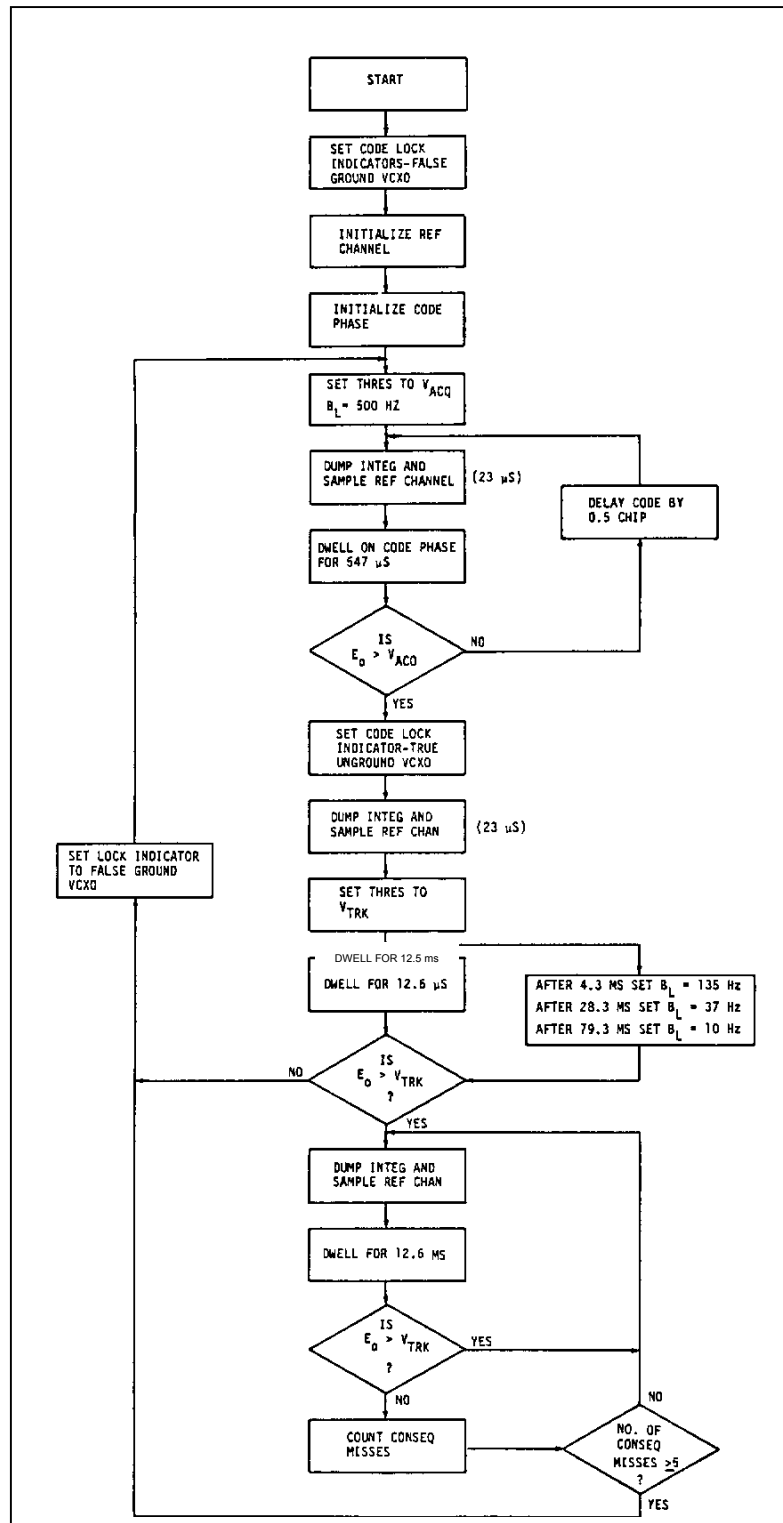


Figure 4-4. Spread spectrum processor acquisition algorithm

Upon detecting correlation, the acquisition logic circuitry inhibits the SSP local PN code phase from searching, increases the integration dwell time from 546 msec to 12.6 msec, and enables the track channel circuitry.

If, after the second 12.6-msec dwell interval, no correlation is detected, the acquisition logic assumes that the initial correlation was a false alarm and resumes searching for correct code phase using the 547- $\mu$ sec dwell interval. If, however, correlation is detected at the end of the second 12.6-msec dwell interval, the acquisition logic assumes that true correlation has occurred. Once two such successive indications of correlations have been detected, five sequential noncorrelations are required to start the acquisition logic searching. This process, called the acquisition algorithm, is presented in flow diagram form in Figure 4-4.

#### B. Track channel

Before a correlation is detected, the track channel is disabled by grounding the VCXO control voltage. Upon detection of correlation, the channel is enabled and moves the VCXO control voltage (and thereby the local code phase) to maintain code phase alignment. The track channel is configured as an Early/Late (E/L) delay lock tracking loop.

The track and acquisition channels use identical hardware through the square law detectors. In the track channel, the mixer PN input is switched between a half-chip early and a half-chip late PN code (as referred to the punctual PN code) at an 11-kHz rate. The same triangular correlation function applies instantaneously to each code phase. After the diode detector, an amplifier filter increases the signal amplitude and reduces the effective noise. This amplifier is ac coupled because all the information required to drive the code phase to zero error is contained in the polarity of the detected signal relative to the E/L switch signal. The amplifier output is then presented to a synchronous detector, whereupon it is multiplied by either a positive or negative gain of equal absolute value at the E/L switch rate. A correlation curve, the track s-curve, is thus produced, which generates a signal analogous to the phase detector error voltage of an analog phase lock loop.

Having this phase detector function, the remainder of the track channel, the loop filter, is designed exactly like an analog phase lock loop filter. Certain constraints upon the loop filter, however, have appeared both through theory and through breadboard test. First, a loop bandwidth of 10 Hz at acquisition threshold is required during the track mode to ensure sufficiently low phase jitter, so that the SSP will not degrade the transponder BER. On the other hand, the loop bandwidth must be sufficiently wide during the time immediately following initial acquisition, so that the loop filter can slew the VCXO to its proper frequency before the codes can drift far enough apart that correlation cannot be maintained. Both theory and practice indicate that this loop bandwidth must be approximately 500 Hz at the same Carrier/Noise Ratio ( $C/N_0$ ). Because of the wide disparity between these bandwidths, there is a very low probability of maintaining track if the bandwidths are switched in a single step.



The loop bandwidth is narrowed from the acquisition bandwidth of 500 Hz to the tracking bandwidth of 10 Hz steps of 4:1 in bandwidth. This is accomplished by successively switching loop filter components until the desired bandwidth is achieved. Transient free operation is ensured by switching precharged capacitors into the loop filter during the bandwidth transition.

#### 4.3.1.5 Baseband Signal Processing

Signal processors condition receiver demodulated data through two channels, the ranging channel, and the NSP channel. In the ranging channel, the demodulated signals from the second IF and detector module are filtered by a three-pole butterworth filter. The filter is designed to meet the following requirements:

##### Ranging Channel Filter Requirements

|                       |  |
|-----------------------|--|
| Center frequency:     | 1.7 MHz  |
| Filter passband:      | Flat within 0.3 dB from 1.5 to 1.9 MHz   |
| Skirt rejection:      | Upper 3 dBd frequency $\leq 3$ MHz<br>Lower 3 dBd frequency $\leq 800$ KHz<br>Upper 20 dBd frequency $\leq 5.2$ MHz<br>Lower 30 dBd frequency $\geq 300$ KHz |
| Time delay variation: | $\leq 20$ ns   |

The ranging channel output is buffered by an emitter follower and then sent to the transmitter baseband processing circuits.

The NSP baseband channel contains the circuitry necessary for band-limiting and amplitude leveling of the recovered NSP data. Demodulated data and noise from the second IF module are amplified and noncoherently amplitude controlled to maintain a differential interface level of 114 to 259 mV rms into a 71-ohm load. This channel is ac coupled with a lower cutoff frequency of  $\leq 1$  kHz and an upper cutoff frequency of 2.4 MHz. The NSP output is routed via relay contacts to the selected NSP (NSP 1 or NSP 2).

#### 4.3.1.6 Automatic Gain Control

Coherent AGC filtering is provided by an active low pass filter. The active filter operates on the CAD voltage from the second IF. The AGC delay voltage is fixed, and is set to yield a nominal CAD output of 100 mV dc. This delay voltage simultaneously sets the phase detector scale factor of 100 mV/radian in the second IF module.

Coherent AGC voltage, after filtering, is sent back to the second IF module AGC amplifiers for RF gain control. A sample of the coherent AGC control voltage is summed with a sample of the noncoherent AGC control voltage from the first IF to form the AGC signal strength telemetry output. The noncoherent AGC is dynamic for signal input levels

ranging from threshold to -90 dBm, and the coherent AGC is dynamic for signal levels from -90 dBm to -50 dBm.

#### 4.3.1.7 Receiver Interference

Receiver interference resulting from high level payload transmitter signals was a potential problem. If the third or fourth harmonics of the transponder receiver VCXO are allowed to occur as sidebands on the receiver first LO, payload transmitter signals removed from the network receiver center frequency by an equal amount could be mixed to exactly the network receiver first IF. This potential problem was eliminated by allocating rejection requirements to the triplexer receiver filter and the first LO filters, so that the interfering signal would fall well below the receiver threshold level. Use of an indirect phase-locked oscillator multiplier significantly helped reduce the presence of VCXO harmonic LO sidebands.

#### 4.3.2 Transmitter

The transmitter is designed to provide an S-band carrier modulated with NSP downlink data and range tones. The modulated carrier is either coherently or noncoherently related to the received uplink signal, depending on selected transmitter drive signal, and thus the receiver phase-lock status. Two output levels are provided, a high level (4.7 to 8.4 W) for STDN LOW and SGLS direct link operation and a low level (0.8 to 1.4 W) Traveling Wave Tube Amplifier (TWTA) drive signal for TDRS and STDN HI operation.

The modulator/multiplier provides an S-band output that is developed by direct multiplication (X8) of the input signal as received from the receiver frequency source module. The input frequency is switched between 277.19 MHz and 285.94 MHz. This input signal is established by either an auxiliary oscillator or a tracking loop that is phase-locked to the received signal. The resulting output frequencies (2217.52 or 2287.52 MHz) are phase modulated with NSP data in either the PSK mode (mod. index =  $\pi/2$  radians peak) or the linear PM mode (mod. index = 0.55 radians peak). Two differential input pairs are provided so that either NSP may provide data to the transmitter.

The turnaround ranging tone (1.7 MHz) may also be modulated (0.5 radian peak) in conjunction with the NSP data. The ranging tone signal, as received from the wideband detector, has a wide range of signal and noise levels, and therefore, this signal is conditioned in an AGC amplifier before it is applied to the linear modulator. TDRS biphasic modulation (PSK mode) is accomplished using the linear phase modulator ( $\pm\pi/8$  radians) and then multiplying by four.

The power amplifier chain receives the modulated carrier and provides the proper amplification, limiting, and switching necessary to provide either of two outputs. The TDRS and STDN HI nominal output level is +30.5 dBm (1.1 W). The common output (SGLS/STDN LO) nominal output level is +38 dBm (6.3 W).

#### 4.3.2.1 Modulator/Multiplier

The modulator/multiplier contains the circuitry necessary to develop an S-band carrier that is coherently related to the Very High Frequency (VHF) input signal. This carrier is then phase modulated with the NSP data and/or turnaround tone ranging signal.

The transmitter drive input is received from the frequency source module of the receiver at a level of +2.4 dBm. The input frequency of either 277.19 MHz or 285.94 MHz is developed in the frequency source module by having a tracking loop phase lock to either the received carrier or an auxiliary oscillator signal. The frequency variance of this input signal is less than 10 kHz (including Doppler).

This input signal is applied to the X2 multiplier, where it is transformed to an output frequency of either 554.38 or 571.88 MHz. The X2 is a single-stage transistorized amplifier in the common emitter configuration, biased to class B operation. It is sufficiently saturated to provide a 5-dB to 1-dB compression ratio between the input and output. The transistor stage is followed by a two-pole Tchebycheff filter with a 1-dB bandwidth of greater than 25 MHz. This filter selects the desired second harmonic while attenuating the adjacent harmonics by more than 35 dB. A pi-type resistive attenuator on the input provides assurance that satisfactory input impedances are achieved, and a similar attenuator on the output establishes the output level. The X2 output, at a level of +6 dBm, is sent to the linear phase modulator.

The linear phase modulator is a reflective coupler modulator utilizing a 180° hybrid power divider and a 90° transmission line on one of the coupled ports to simulate the required 90° hybrid power divider.

The 90° hybrid divides the input signal to its two output ports. A reactive load on each output port, which is created by a series-resonant tank circuit, creates a reflected signal with a phase shift that is controlled by the capacitance of the varactor diode. The 90° hybrid sums these two reflected signals out of phase at the input (cancellation) and in phase at the output; thus, the only signal attenuation is the typical 2-dB loss in the power divider (1 dB each direction) and the resistive losses inherent in the Qs of the series tanks.

This modulator has demonstrated the ability to provide very linear performance (typically <2 percent from the best fit straight line) over a 30° peak range. This is accomplished by shunting the series resonant circuit with an inductor, which tends to increase and linearize the phase angle component of the reflection coefficient of the circuit. The baseband signal (to be described later) modulates the RF carrier at a scale factor of about  $75^\circ/V$ . This signal drives the UHF buffer amplifier.

The UHF buffer amplifier is a single-stage amplifier. This stage provides about 6 dB of gain at 563 MHz with a 10:1 compression. It is almost identical to the X2 multiplier. Attenuators are placed on both the input and output of this amplifier, in order to provide the greatest flexibility of signal levels, while maintaining the desired compression. The total gain of this amplifier is 7 dB; therefore, the output signal, which is directed to the X4 multiplier, is at a level of +8 dBm.

The X4 multiplier is a single-stage transistorized multiplier using a transistor biased to class B operation. This common emitter stage provides about 1 dB of conversion loss, and also provides a 2-dB/1-dB compression. It utilizes a combination of discrete and microstrip components to establish the input and output matching circuits and the three-pole output filter. The filter is designed to provide at least 110 MHz of bandwidth at the 1-dB points, while providing more than 40 dB of rejection to the adjacent harmonics. A pi-type attenuator is included in the output of the filter, providing adjustment capability to the output signal.

The S-band amplifier is a single-stage common emitter amplifier. This amplifier provides about 4 dB of gain, while supplying at least a 1.3:1 compression at 2.25 GHz. A combination of discrete (chip) and microstrip components is applied to implement the amplifier, input and output matching circuits, and the three-pole filter on the output. The filter is designed to supply at least 110 MHz of bandwidth at the 1-dB point, while providing more than 40 dB of rejection to the adjacent harmonics. This amplifier receives about a 4.0-dBm input signal from the X4 multiplier, and provides a +4.8-dBm signal that is delivered to the isolator.

The S-band isolator is a ferrite terminated, circulator-type isolator.

The isolator output at a level of 4.4 dBm is made available to the power amplifier module.

The ranging amplifier and AGC contains the two ranging tone amplifiers, the AGC emitter follower transistor, the zero-bias high sensitivity AGC detector diode and its counterpart temperature diode, and the AGC operational amplifier.

The two amplifiers each provide about 25 dB of gain to the 1.7-MHz ranging tone input signal, which is received at a level as low as 1.8-mV rms. About 22 dB of AGC range is used in each amplifier to minimize the input signal that may vary as much as 43 dB. A diode limiter is installed between the amplifiers, so that if large signals are suddenly applied to the input, the output amplifier will not be excessively saturated before the AGC can take effect. The emitter follower buffers the AGC detector from the signal path. The AGC detector, amplifier, and temperature compensation network is very similar to that used in the first IF module noncoherent AGC of this transponder. The AGC threshold adjust is in the circuit in order to limit the maximum gain (approaching 100 dB for two Integrated Circuits (ICs)) when there is an absence of signal.

The two NSP line receivers provide the ability to receive the differential NSP data, and at the same time withstand large common mode voltages. The output is controlled by gating signals. The control inputs to these amplifiers are the NSP 1 and NSP 2 enable commands. In both PM (linear) and PSK (biphase) modes, the line receiver output drives a saturated transistor switch which controls the data signal amplitude to be applied to the summing amplifier. This data signal amplitude is accurately controlled by the MOD index control, thus controlling the modulation index of the linear phase modulator to a level of 0.55 radian peak at the transmitter output. The PSK enable command changes the data signal amplitude so that a modulation index of  $\pi/2$  radians peak

(biphase) is developed at the transmitter output when TDRS mode is commanded. The digital signal is then applied to one input of the summing amplifier. The switch controlled by the ranging disable command switches the turnaround ranging tone into the second input of the summing amplifier. The ranging tone is adjusted for 0.5 radian peak deviation. By using the ranging disable command, the ranging tone may be disabled to the modulator. The summing amplifier was selected because it provides a high gain bandwidth product, thus maximizing the isolation between its two input signals. The two sections of a second Field Effect Transistor (FET) switch change the gain of the summing amplifier and the modulator offset bias for high and low frequency RF carrier. The gain change compensates for high and low transmit frequency modulation sensitivity. The modulator offset bias brings the modulator to the center of its linear range. A temperature sensitive resistance is included here to reduce modulator temperature variations.

The output of this circuit is applied directly to the linear phase modulator, where the voltages control the varactor diodes in the resonant circuits.

#### **4.3.2.2 RF Amplifier Assembly**

The RF amplifier assembly provides power amplification and amplitude limiting of the phase-modulated S-band signal developed in the multiplier/modulator. This all solid-state RF power amplifier is composed of a cascade of five transistor stages, consisting of the preamp, driver, and power amp, providing a total gain in excess of 30 dB. The gain compression of the module has been demonstrated to be better than a 0.3-dB output variation for a 1-dB input variation, while the amplifier provides an output level of +30.5 dBm (1.1 W) in the TDRS mode and +38 dBm (6.3 W) in the common mode.

The TDRS/common output port switching is performed in the power amplifier module, utilizing commands received from the control logic. The RF disable command attenuates the output signal to less than 1 mW whenever the logic provides this command.

The input signal is received at a level of  $+4 \pm 2$  dBm, and is composed of a phase-modulated carrier at either 2217.52 or 2287.52 MHz. This input signal (from the modulator/multiplier) is presented to the preamplifier.

#### **4.3.2.3 Transmitter Preamplifier**

The preamplifier provides about 16 dB of RF gain at relatively low RF power levels. It amplifies the RF input signal to a level of +20 dBm, which is used to drive the following driver amplifier. The preamplifier, in conjunction with the inhibit control, provides for the gating of the amplifier output upon command (inhibit function). The preamplifier is a standard common emitter RF amplifier stage. The amplifier is designed as a wideband unit, so its alignment is not critical. The inhibit circuitry functions to provide a wide range variable resistance between the control terminal and the -14 V supply line. This reduces the available bias voltage to approximately 0.35 V during the RF output disable command interval, which is insufficient to permit stage amplification of low level signals. The output of this preamplifier is sent to the driver amplifier.

#### 4.3.2.4 Driver Amplifier

The driver amplifier increases the power level of the preamplifier output to a level of 31.3 dBm to drive the following power amplifier subassembly or the TDRS output; in which case, the driver amplifier output is switched directly out of the power amplifier (PA) module by a relay upon receipt of an external command. The driver amplifier also provides the amplitude limiting needed to suppress the amplitude excursions of the input signal.

The driver amplifier is a two-stage, common-base class C amplifier in cascade. The first stage uses a transistor which is capable of 1-W power dissipation. The second stage uses a transistor with a nominal power dissipation capability of 3 W.

The common/TDRS relay switches the driver amplifier power output between the power amplifier subassembly and the TDRS output port. Spare relay contacts are used to supply mode status to the switching pulsers.

A momentary pulse of 15 to 50 msec is received from the control logic to either of two control coils within the relay, which results in transfer to the opposite contacts where magnetic latching action causes it to remain until the other coil is pulsed. An RF output inhibit pulse removes RF power in 30 to 100 msec during the switching interval, permitting a desirable cold-switching condition. Diodes are provided to suppress the back Electromagnetic Force (EMF) generated by the relay coils, following removal of the operating pulse.

#### 4.3.2.5 Power Amplifier

The PA provides the final stage of power amplification when the common mode is selected. It provides a total output of up to 8.4 W.

The power amplifier contains a parallel pair of transistors biased to class C, common-base amplifier operation, a Wilkinson power divider/combiner pair, and a transmit level detector to be used for telemetry purposes.

The transistor paralleling technique employed is in common usage today, and is employed when the unit power output requirements exceed the capability of a single device.

The Transmitter Level Sensor (TLS) detector receives a sample of the PA output level from a backward wave coupler. This coupler design was selected to provide a reasonable directivity, so that mismatch energy will not produce an erroneous detector output.

The coaxial S-band isolators at the common and TDRS output ports of the PA serve to establish a definite, stable output impedance characteristic, and also protect the PA proper, should a gross load fault occur during operation.

The isolators use conventional, established ferrite techniques and packaging. A unique feature is a removable connector on both ports, which, in the case of the common output, facilitates an efficient physical integration with the PA proper.

The XMIT level sense amplifier functions to convert the voltage from the transmitter level RF detector in the power amplifier subassembly into a differential balanced voltage having a calibrated output between the levels of -5 V for no signal and +5 V for maximum output power.

The circuit selected uses two operational amplifiers interconnected to provide a balanced output.

The regulator reduces and regulates the  $+24.0 \pm 0.96$  bus voltage to +20.0 V to supply the driver and predriver stages. An improved RF output stability results from reduced line voltage variations. Also provided is circuitry for inhibiting the preamplifier during TDRS/COMMON relay switching or other independent events, thus preventing damage to the PA assembly or external relays.

RF power output reduction during the RF output disable command interval is accomplished by removing essentially all forward bias from the two class A preamplifier stages. Residual power output of the preamplifier is then insufficient to drive the following class C stages in the driver assembly. The preamplifier bias is referenced to the -14 V bus, and the control function is shifted to this level by employing an opto-isolator whose unique properties also provide a thresholding characteristic.

The photo transistor portion of the opto-isolator, a wide range variable resistance, is used to shunt the bias divider within the preamplifier. The opto-isolator Light Emitting Diode (LED) is driven with a signal received from a transistor, which is activated by the RF disable input signal which originates in the control logic.

### **4.3.3 Control Logic**

The control logic (Figure 4-5) contains the necessary circuitry for processing and internal distribution of input commands and control logic governing receiver signal acquisition. Prime mode switching dropout time is approximately 100 milliseconds. Coherent-to-noncoherent VCXO dropout time is 5 to 10 milliseconds.

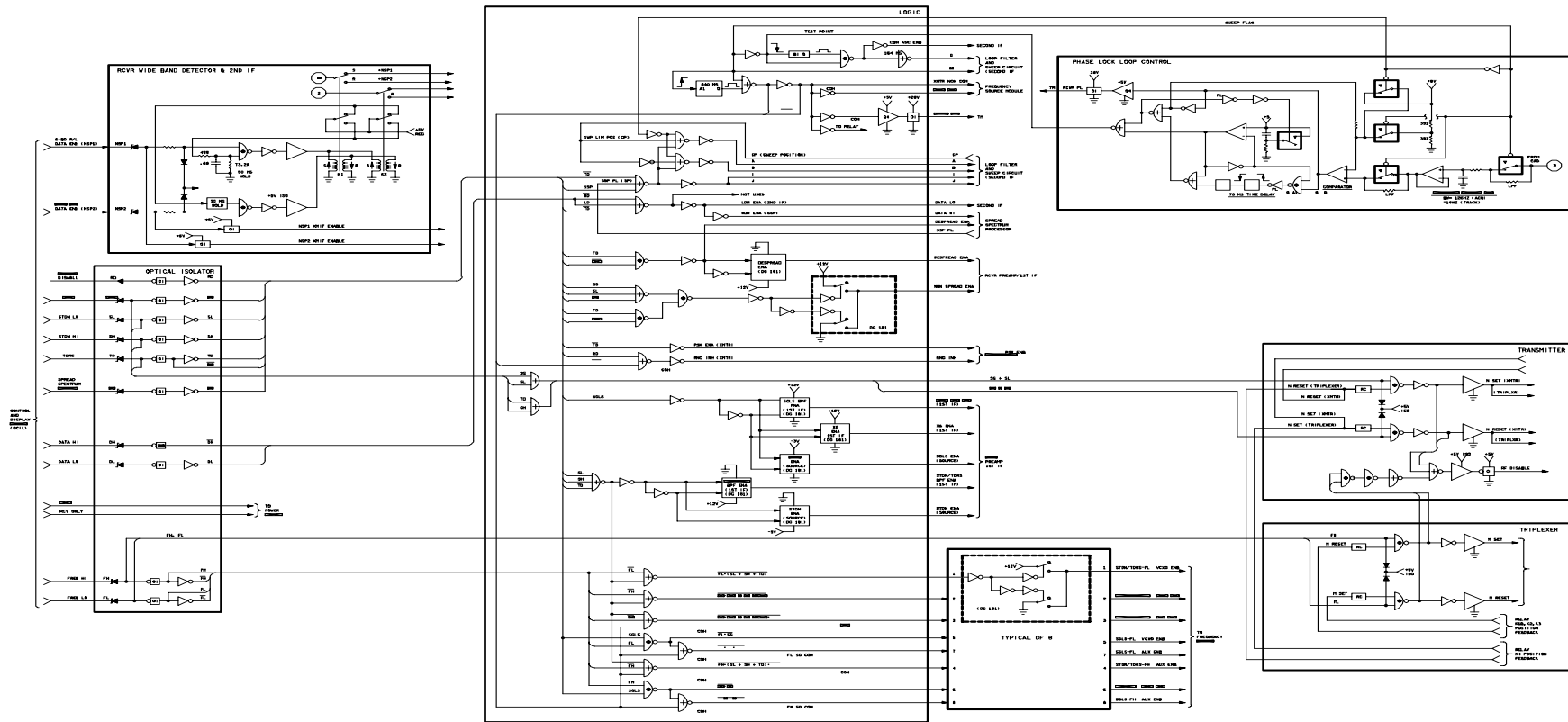


Figure 4-5. Control logic



#### 4.3.3.1 Input Command Processing

The command input signals are isolated from chassis and referenced to the 28-V prime power return. Internal mode and command signals, referenced to chassis, are coupled to the input commands via optically coupled isolator integrated circuits. The input commands are conditioned by series resistor-zener diode networks prior to the optical isolators to guarantee that command line voltages less than 1.8 V peak produce false level internal commands, and that command line voltages greater than 23.1 V produce true level internal commands. Isolation between input command lines and chassis is in excess of 2 M $\Omega$ . Internal commands are of three general types: high level discrettes, low level discrettes, and pulse commands. The high level discrettes switch between the +12 V (true) or -12 V (false) secondary supply voltages. These commands are used to control PIN diode switches in the preamp/first IF module and the second IF and detectors module. Pulse commands are used to control relay and RF coaxial switch positions. The pulse commands use monitor contact feedback from the relays and coaxial switches so that current delivered to the desired coil is maintained until verification of switch transfer is received via the monitor contacts. After switch transfer, coil current is switched off and the relays and RF coaxial switches are held in position by their latching mechanisms.

#### 4.3.3.2 Lock Detection

The receiver signal acquisition procedure is controlled by the acquisition algorithm given in Figure 4-2. The circuit contains both the threshold detectors and logic circuits that implement the algorithm. The receiver phase-lock detection threshold detector is fed by the CAD output from the second IF and detector module. This detector employs a predetection filter which has a two-pole 126-Hz noise bandwidth low pass response prior to signal acquisition, and a 16-Hz two-pole low pass response after acquisition. The switchable bandwidth lock detection filter optimizes detection probability during receiver sweep, and minimizes the false dismissal probability after lock. The threshold delay voltage is also controlled by the acquisition logic, and is set for 2 percent false alarm probability during acquisition, and reduced to half the acquisition value after lock.

A separate threshold detector is provided for the Doppler data good output flag. This threshold detector also operates on the CAD output voltage to determine Doppler data quality. A two-pole filter of 73.1-Hz maximum noise bandwidth serves for predetection filtering. The threshold voltage is set to 40 percent of nominal CAD output voltage. The combination of threshold voltage and predetection bandwidth yields a response time of  $4 \pm 1$  msec for the data good output.

#### 4.3.4 Dual S-Band Triplexer

The triplexer provides filtering for operation of the transponder in the SGLS and STDN LOW modes. RF coaxial switches S1 (K1B), S2 (K2), and S3 (K3) respond to the frequency low and frequency high commands to route the RF signals to the appropriate section of the triplexer. In the TDRS and STDN HI mode, the received signal bypasses

the triplexer and is routed to the receiver via RF switch S4 (K4) when it is commanded to the TDRS or STDN LOW position.

The dual S-band triplexer combines two independent triplexers in a common housing. Each triplexer, one designated low and the other designated high, is configured as a three-port network, consisting of three narrowband bandpass filters and a low pass filter. The optimum filter design, in terms of number of resonators, unloaded  $Q_u$  required, and size for the triplexer receiver branches was found to be a six-section 0.01-dB Tchebycheff, and for the transmit filters, a four-section 0.01-dB Tchebycheff. All filters are reactively coupled through adjacent sidewalls.

The bandpass filters are joined to a common port with small loss (approximately 0.15 dB) through a coupling network that makes use of the respective off-band impedance characteristics. Given the input impedance of each triplexed filter at its neighbor's operating frequency, a computer optimization routine was used to determine the optimum length of 50 ohms coaxial line required to couple the filters with minimum deleterious effect. Whereas the receive path rejection requirements are satisfied by the bandpass filter characteristic alone, the extended rejection requirement applied to the transmit paths requires the addition of a low pass filter. The low pass filter is a nine-pole 0.01-dB Tchebycheff design, which, in cascade with the transmit filter, will maintain a minimum of 30 dB rejection to the specified 6- to 10-GHz frequency range.

#### 4.3.5 RF Coaxial Switches

The RF coaxial switches S1 (K1B), S2 (K2), S3 (K3), and S4 (K4) are single-pole, double throw type switches. Performance characteristics are briefly summarized below:

- Insertion loss                                      0.2 dB maximum
- Power handling capability                      5 W CW
- Switching time                                      15 msec maximum
- Switch type    Latching, no hold-in current required

See Figure 4-6 coax relay mechanical drawing.

#### 4.4 POWER CONSUMPTION

| <u>Mode</u>       | <u>Power</u> |
|-------------------|--------------|
| SGLS or STDN LOW  | 58.5 W       |
| TDRS or STDN HIGH | 41.0 W       |
| RCV only          | 30.0 W       |

#### 4.5 WEIGHT

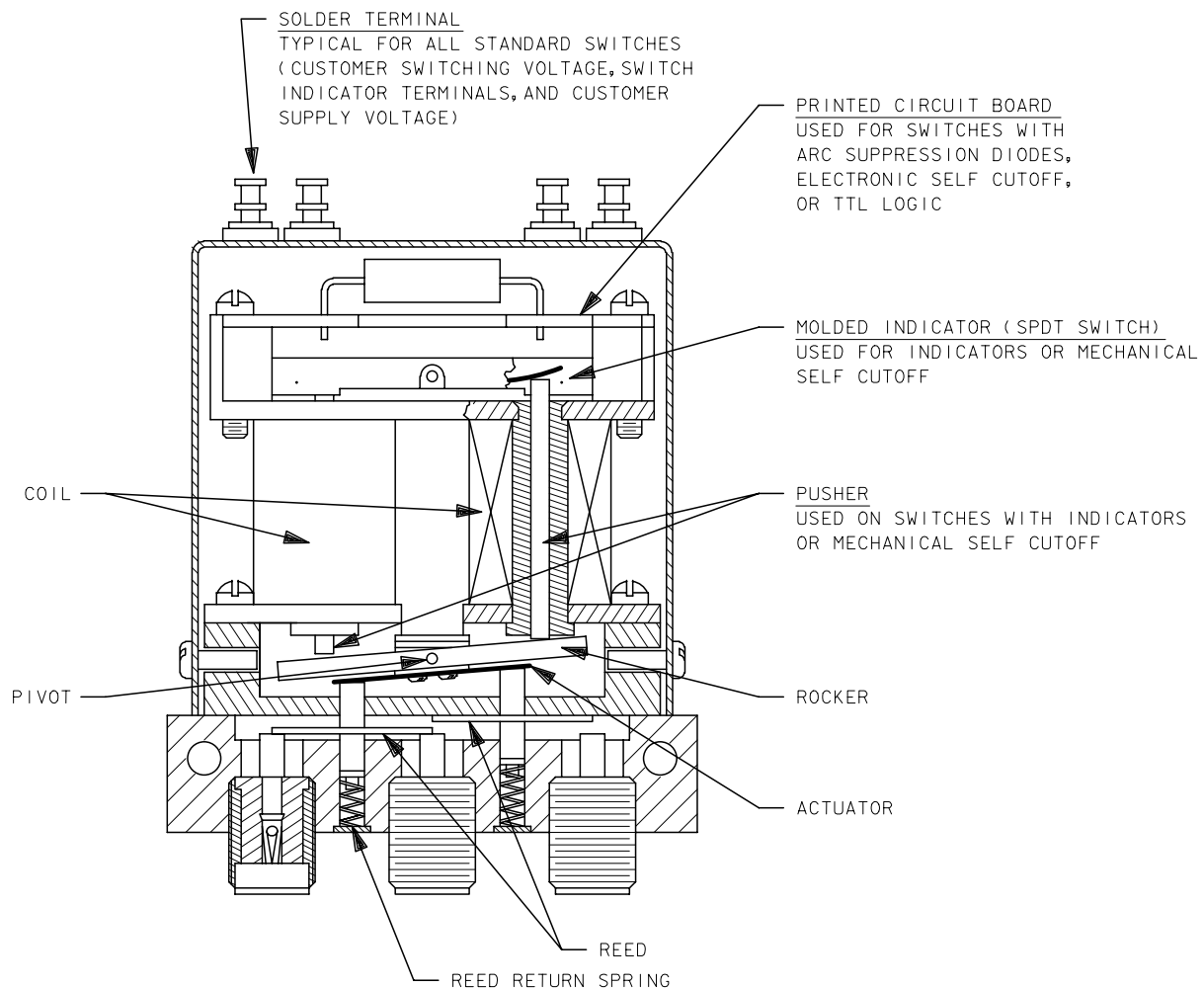
35.3 pounds

#### 4.6 INSTALLATION

Transponders 1 and 2 are mounted on dual coldplates in bay 3A. (See Section 18, COMMUNICATIONS AND INSTRUMENTATION SYSTEM WATER AND AIR COOLED EQUIPMENT.)

#### 4.7 DESCRIPTION OF OPERATION

Transponders 1 and 2 operate as a receiver/transmitter in S-band systems 1 and 2. Each transponder is a separate, redundant electronics unit which can operate in either string 1 or string 2. The modes and frequencies are shown in Table 4-2.



186110306. ART 1

**Figure 4-6. Coax relay mechanical drawing**

**Table 4-2. Transponder modes and frequencies**

| S-Band PM frequencies |           |           |                |            |
|-----------------------|-----------|-----------|----------------|------------|
| Mode                  | Frequency | PCV (MHz) | XMIT/PCV ratio | XMIT (MHz) |
| SGLS                  | Low       | 1775.733  | 256/205        | 2217.5     |
|                       | High      | 1831.787  | 256/205        | 2297.5     |
| STDN                  | Low       | 2041.947  | 240/221        | 2217.5     |
|                       | High      | 2106.406  | 240/221        | 2297.5     |
| TDRS                  | Low       | 2041.947  | 240/221        | 2217.5     |
|                       | High      | 2106.406  | 240/221        | 2297.5     |

#### 4.7.1 Crew Controls

(AIL)

S-Band PM

XPNDR - 1/OFF/2

Mode

- SGLS
- STDN LO
- STDN HI
- TDRS DATA
- TDRS RNG

Signal strength - S-Band PM/KU/S-Band P/L

#### 4.7.2 Crew Displays

(AIL)

Signal strength meter  
(range 0-5)

(F-9)

DC amps/signal strength  
(range 0-500)

Note: The meters display the signal strength of the operating transponder, which could be different from the one selected by the panel switch if selected differently by the GCIL.

(CRT) see Section 2, PM SYSTEM

#### 4.7.3 Ground Commands

See Section 2, PM SYSTEM, S-Band PM System CMD List.

#### 4.7.4 Telemetry

See Section 2, PM SYSTEM, S-Band PM Telemetry List.

#### 4.7.5 Operational Instructions

See Section 2, PM SYSTEM, S-Band Equipment (LRU) Notes.

### 4.8 SPECIAL TELEMETRY COMPUTATIONS

See Section 2, PM SYSTEM, Special TM Computations.

### 4.9 REFERENCES

#### Orbiter Schematic List

Schematic Diagram, C&T NETWORK S-BAND TRANSPONDER, VS70-740129, Rev B, 7-14-83, Rockwell International.

Schematic Diagram, C&T GCIL, VS70-240299, Rev E, 10-24-84, Rockwell International.

#### LRU Schematic List (TRW)

|  |                          |
|--|--------------------------|
| Triplexer assembly transponder PWR converter |                          |
| Input switch                                 | D292167                  |
| SGLS BPF                                     | D292029                  |
| STDN/TDRS BPF                                | D292096                  |
| Output switch                                | D292197                  |
| AGC network                                  | D292099                  |
| Post AGC BPF                                 | D292104                  |
| Second and third mixer                       | D292091                  |
| Noncoherent AGC                              | D292093                  |
| Power amp and switch                         | D292087                  |
| X6 and X7 multiplier                         | D292089                  |
| Interconnect diagram                         | D292111, Rev NC, 1-19-77 |
| SSPI and coherent AGC                        | D292117                  |
| 31 MHz BPF                                   | D292119                  |
| Phase detector and CAD                       | D292121                  |
| Reference source                             | D292123m                 |
| Wideband detector                            | D292107                  |
| 62 MHz BPF                                   | D292109                  |
| 31 MHz amplifier                             | D292595                  |
| Costas and phaselock                         | D292126, Rev B, 12-19-77 |
| Interconnect diagram - dual diplexer         | D293658, NC, 1-23-78     |
| Interconnect diagram - S-band transponder    | D292003, Rev B, 11-21-77 |
| Interconnect diagram - freq source           | D292131, Rev A, 7-26-77  |
| 300 MHz analog circuit                       | D292139                  |

|  |                         |
|--|-------------------------|
| 500 MHz analog circuit                         | D292142                 |
| Regulator and switch                           | D292145                 |
| 500 MHz digital circuit                        | D292148                 |
| 300 MHz digital - 15/16 circuit                | D292136                 |
| 300 MHz digital - 14/15 circuit                | D292635                 |
| Interconnect diagram spread spec<br>RF section | D292161, Rev A, 7-26-77 |
| Code acquisition and PN generator              | D292171                 |
| Tracking and acquisition channel               | D292174                 |
| Interconnect diagram                           | D292177                 |
| Interface and logic 1                          | D292181, Rev A, 1-23-78 |
| Interface and logic 2                          | D292199                 |
| CAD channel                                    | D292202                 |
| Wideband channel                               | D292188                 |
| X2 multiplier                                  | D292191                 |
| Interconnect diagram, modulator multiplier     | D292071                 |
| UHF buffer, linear phase mod, X4 multiplier    | D292061, Rev A 7-26-77  |
| Amplifier, buffer, S-band                      | D292067                 |
| Ranging tone amp and AGC                       | D292069                 |
| Modulator baseband                             | D292076                 |
| First IF                                       | D292079                 |
| Preamplifier                                   | D292081, Rev A, 7-8-77  |
| Driver   | D292050                 |
| Power amplifier                                | D292045                 |
| Power amplifier                                | D292047                 |
| TLS amplifier                                  | D292031                 |
| Control/regulator                              | D292059                 |
|  | D292056                 |

### Microfilm

Network Transponder CDR, TRW, October 10, 1977.

Network Transponder CDR Drawing Package, vol II, TRW October 10, 1977.

Network Transponder CDR Monthly Review, TRW, November 15, 1977.

Effects of Doppler on TDRSS Acquisition for the Space Shuttle Orbiter, Lockheed,  
June 1, 1981.

### ESTL Test Reports

System Verification Test Requirements and Status Reports for TDRS S-Band Relay  
Link, JSC-11757, Rev C, June 6, 1983.

Orbiter/TDRSS S-Band Forward Link TDM System Verification Test Report,  
JSC-16689, October 1980.

TDRSS/Orbiter SSA Forward Line RF Acquisition Test Report, JSC-16963,  
August 1981.

System Verification Tests Requirements and Report for DOD IUS - Orbiter Link, JSC-18163, March 22, 1982.

Orbiter/TDRSS - S-Band Return Link TDM System Performance Verification Test Report, JSC-18302, May 1982.

System Verification Test Requirements and Status Report for AFSCF Direct Link, Addendum 1, March 23, 1982, JSC-13022, Rev B.

System Verification Test Requirements and Status Report for GSTDN Direct Link, JSC-11300, Rev C, March 24, 1982.

System Verification Test Requirements and Status Reports for GSTDN/SLSS- Orbiter Interface, JSC-16506, Rev A, February 26, 1982.

Orbiter/AFSCF S-Band Direct Link System Verification Test Report, JSC-16680, May 1980.

### 4.10 SUMMARY DATA

See Figure 4-7.

### 4.11 OPERATIONAL NOTES

See Section 2, S-BAND PM SYS, System Operating Constraints.

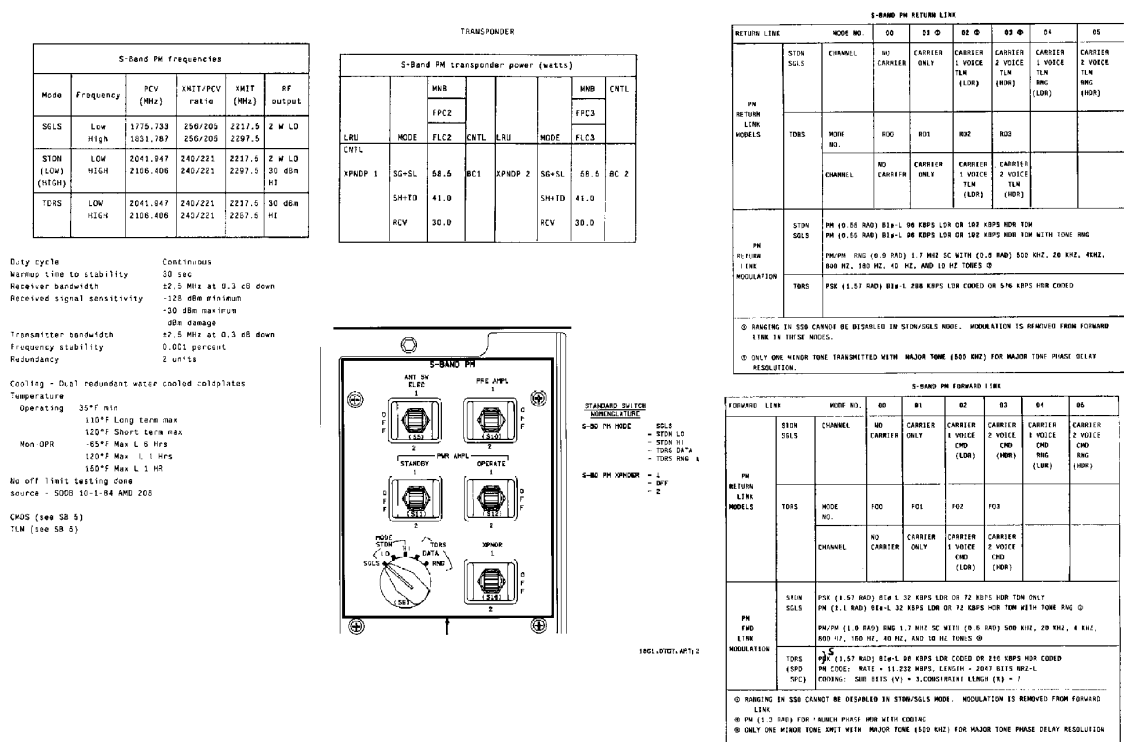


Figure 4-7. Summary data

**SECTION 5 – S-BAND PREAMPLIFIER**  
**CONTENTS**

| <b>Section</b> |   | <b>Page</b> |
|----------------|---|-------------|
| 5.1            | GENERAL DESCRIPTION .....                   | 5-1         |
| 5.2            | INTERFACES .....                            | 5-1         |
| 5.3            | DESCRIPTION .....                           | 5-1         |
| 5.3.1          | Major Components .....                      | 5-1         |
| 5.3.2          | Parametric Amplifier .....                  | 5-3         |
| 5.3.3          | Transistor Amplifier.....                   | 5-3         |
| 5.3.4          | Dual Diplexer .....                         | 5-3         |
| 5.3.5          | Preamp Heater Assemblies .....              | 5-5         |
| 5.3.6          | Preamp Power Converter and Regulators ..... | 5-5         |
| 5.3.7          | Control Logic.....                          | 5-6         |
| 5.3.8          | RF Coax Switches .....                      | 5-6         |
| 5.3.9          | Control Logic Driver Operation .....        | 5-8         |
| 5.3.10         | Power Relay Drivers .....                   | 5-8         |
| 5.3.11         | Electrical Power .....                      | 5-8         |
| 5.3.12         | Weight .....                                | 5-9         |
| 5.4            | INSTALLATION .....                          | 5-9         |
| 5.5            | DESCRIPTION OF OPERATION .....              | 5-9         |
| 5.5.1          | Crew Controls .....                         | 5-10        |
| 5.5.2          | Ground Commands .....                       | 5-10        |
| 5.5.3          | Telemetry.....                              | 5-10        |
| 5.5.4          | Operational Instructions.....               | 5-11        |
| 5.6            | REFERENCES .....                            | 5-12        |
| 5.7            | OPERATIONAL NOTES.....                      | 5-13        |



## TABLES

| Table |                             | Page |
|-------|-----------------------------|------|
| 5-1   | Preamplifier equipment..... | 5-2  |
| 5-2   | DC input power.....         | 5-9  |
| 5-3   | Preamp gain .....           | 5-11 |

## FIGURES

| Figure |                             |      |
|--------|-----------------------------|------|
| 5-1    | Preamplifier equipment..... | 5-2  |
| 5-2    | DC input power.....         | 5-9  |
| 5-3    | Preamp gain .....           | 5-11 |

## SECTION 5 S-BAND PREAMPLIFIER

### 5.1 GENERAL DESCRIPTION

The preamplifier assembly consists of redundant parametric amplifier modules with switching regulator/dc-to-dc converters, Radio Frequency (RF) dual diplexer, and RF coax switches and redundant control logic.

### 5.2 INTERFACES

Figure 5-1 shows the preamplifier equipment consisting of two redundant preamplifiers. Routing of the RF signals from the antenna system antenna switch to the operating preamplifier is determined by which transponder is selected and the frequency mode (high or low) of the transponder.

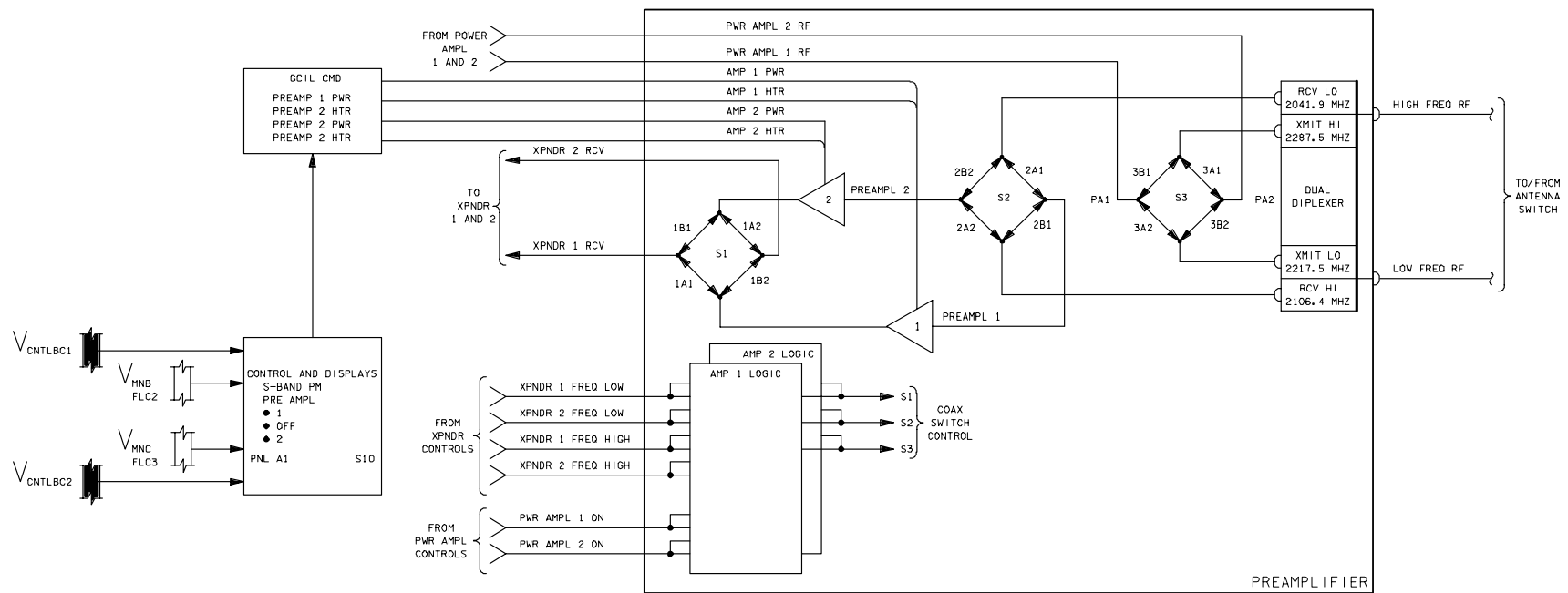
The dual (frequency) diplexer is located in the preamplifier to allow diplexing of the transmit and receive signals to a single antenna system. Routing of the transmit RF signal to the dual diplexer is determined by which power amplifier is selected.

### 5.3 DESCRIPTION

The preamplifier equipment contains two preamplifiers. Each preamplifier is a single-stage, broadband, low-noise parametric amplifier with a gain of 13.5 dB followed by a transistor amplifier with a gain of 11.5 dB, providing an overall gain of 25 dB.

#### 5.3.1 Major Components

- Parametric amplifier
  - Transistor amplifier
  - Dual diplexer
  - Heater assembly
  - Power converters and regulators
  - Control logics 1 and 2
  - Coax switches S1, S2, and S3
  - Controls (command and panel)
- } One each in PREAMPL 1 and 2



186110801.ART.3

Figure 5-1. Preamp equipment

### 5.3.2 Parametric Amplifier

The name parametric amplifier is derived from the operating principle of the amplifier. Signal amplification is obtained by varying one of the circuit parameters; the circuit parameter being the capacitance of a varactor diode which is varied by the pump signal (Gun Diode Oscillator (GDO)) voltage.

Amplification is obtained as follows: the voltage across the varactor ( $V = Q/C$ ), as a result of the input signal, is amplified when the varactor capacitance is decreased by the pump signal, the energy source. The pump frequency is much higher (50.7 GHz) than the signal frequency to provide low noise operation.

The mixing of the input signal and the pump signal generates a signal, called the idler signal, which is filtered out so that it will not appear on either the input or output.

The idler filter follows the varactor diode in the circuit. This filter is followed by a tuned capacitor tuned to the center frequency of the amplified signal.

The circulator assembly provides RF isolation of the input signal from the output signal.

### 5.3.3 Transistor Amplifier

The transistor amplifier consists of two single-ended transistor stages connected in cascade, followed by an integral pad at the output, whose attenuation is selected to adjust the gain to 12 to 13 dB.

The gain stability vs. temperature achieved is on the order of 0.1 to 0.25 dB peak-to-peak.

### 5.3.4 Dual Diplexer

The dual diplexer has two sections, one for the frequency low mode and one for the frequency high mode. Each section is used to diplex the transmit and receive signals so that a single antenna can be used for transmit and receive.

### 5.3.4.1 Transmit Bandwidth

Flat within 0.3 dB for  $\pm 2.5$  MHz (filter only)

Flat within 3 db for  $\pm 6$  MHz

Down 60 dB or more for  $2265.0 \text{ MHz} \leq f \leq 4435 \text{ Mhz}$   
Down 50 dB or more for  $2130 \text{ MHz} \leq f \leq 2150 \text{ Mhz}$   
Down 62 dB or more for  $200 \text{ MHz} \leq f \leq 2130 \text{ Mhz}$   
Down 50 dB or more for  $4435 \text{ MHz} \leq f \leq 4800 \text{ MHz}$

Down 15 dB or more  $4800 \text{ MHz} \leq f \leq 5300 \text{ Mhz}$   
Down 45 dB or more  $5300 \text{ MHz} \leq f \leq 5600 \text{ MHz}$   
Down 25 dB or more  $5600 \text{ MHz} \leq f \leq 6500 \text{ Mhz}$   
Down 50 dB or more  $6500 \text{ MHz} \leq f \leq 7100 \text{ MHz}$

2217.500 Mhz (FREQ LOW)

Harmonics: FREQ LOW times 2, times 3, times 4 down 57 dB or more, and for FREQ LOW times 6 at least 30 dB.

Down 60 dB or more for  $2370 \text{ MHz} \leq f \leq 4575 \text{ MHz}$   
Down 40 dB or more for  $2350 \text{ MHz} \leq f \leq 2370 \text{ MHz}$   
Down 62 dB or more for  $200 \text{ MHz} \leq f \leq 2240 \text{ MHz}$   
Down 50 dB or more for  $4575 \text{ MHz} \leq f \leq 4800 \text{ MHz}$

Down 15 dB or more  $4800 \text{ MHz} \leq f \leq 5300 \text{ Mhz}$   
Down 45 dB or more  $5300 \text{ MHz} \leq f \leq 5600 \text{ MHz}$   
Down 25 dB or more  $5600 \text{ MHz} \leq f \leq 6500 \text{ MHz}$   
Down 50 dB or more  $6500 \text{ MHz} \leq f \leq 7100 \text{ MHz}$

2287.500 MHz (FREQ HIGH)

Harmonics: FREQ HIGH times 2, times 3, times 4 down 57 dB or more, and for FREQ LOW times 6 at least 30 dB.

Down 115 dB or more at  $2041.9 \text{ MHz} \pm 12 \text{ MHz}$  for 2217.5 MHz (FREQ LOW)  
Down 115 dB or more at  $2106.4 \text{ MHz} \pm 12 \text{ MHz}$  for 2287.5 MHz (FREQ HIGH)

### 5.3.4.2 Transmit Insertion Loss

1.3 dB maximum from preamplifier power amplifier input to RF output.

### 5.3.4.3 Receive Bandwidth

0.3 dB or less for  $\pm 2.5$  MHz (filter only)

3 dB or less for  $\pm 12$  MHz

Down 70 dB or more for  $200 \text{ MHz} \leq f \leq 2049 \text{ MHz}$   
Down 65 dB or more for  $2049 \text{ MHz} \leq f \leq 2060 \text{ MHz}$   
Down 50 dB or more for  $2170 \text{ MHz} \leq f \leq 2200 \text{ MHz}$   
Down 70 dB or more for  $2200 \text{ MHz} \leq f \leq 4500 \text{ MHz}$   
Down 50 dB or more for  $4500 \text{ MHz} \leq f \leq 4600 \text{ MHz}$

2106.406 MHz (FREQ HIGH)

Down 20 dB or more  $4600 \text{ MHz} \leq f \leq 5300 \text{ MHz}$   
Down 50 dB or more  $5300 \text{ MHz} \leq f \leq 5500 \text{ MHz}$   
Down 6 dB or more  $5500 \text{ MHz} \leq f \leq 6200 \text{ MHz}$   
Down 50 dB or more  $6200 \text{ MHz} \leq f \leq 7100 \text{ MHz}$

Down 70 dB or more for  $200 \text{ MHz} \leq f \leq 1950 \text{ MHz}$   
Down 50 dB or more for  $1950 \text{ MHz} \leq f \leq 1970 \text{ MHz}$   
Down 65 dB or more for  $2088 \text{ MHz} \leq f \leq 2097 \text{ MHz}$   
Down 70 dB or more for  $2097 \text{ MHz} \leq f \leq 4300 \text{ MHz}$   
Down 50 dB or more for  $4320 \text{ MHz} \leq f \leq 4600 \text{ MHz}$

2041.947 MHz (FREQ LOW)

Down 20 dB or more  $4600 \text{ MHz} \leq f \leq 5300 \text{ MHz}$   
Down 50 dB or more  $5300 \text{ MHz} \leq f \leq 5500 \text{ MHz}$   
Down 6 dB or more  $5500 \text{ MHz} \leq f \leq 6200 \text{ MHz}$   
Down 50 dB or more  $6200 \text{ MHz} \leq f \leq 7100 \text{ MHz}$

Down 103 dB or more at  $2217.5 \text{ MHz} \pm 2.3 \text{ MHz}$  for 2041.947 MHz (FREQ LOW)  
Down 103 dB or more at  $2287.5 \text{ MHz} \pm 2.3 \text{ MHz}$  for 2106.406 MHz (FREQ HIGH)

### 5.3.5 Preamp Heater Assemblies

A heater and temperature controller maintains the GDO at a temperature of  $175 \pm 1^\circ \text{ F}$  to obtain a constant pump power level. A separate heater and temperature controller are used to stabilize the circulator ferrites at  $75 \pm 25^\circ \text{ F}$  to provide a constant source impedance to the parametric amplifier.

The temperature controllers are of the proportional control type with the heaters resistively sized to provide the proper amount of power to achieve the 10-minute warmup time.

### 5.3.6 Preamp Power Converter and Regulators

The dc/dc converter and regulators provide the GDO with a precision voltage reference, the varactor bias with a regulated negative output voltage at less than  $1 \mu \text{ amp}$ , and power to the output transistor amplifier.

The prime 28-V dc input is fed through an input filter to a preregulator, which regulates the input voltage to the master inverter to approximately 18 V dc. The master inverter operating at 25 kHz provides the square-wave base drive to the slave inverter, and a sync signal to the switching regulator. The switching regulator provides an 18-V dc regulated voltage to the slave inverter.

The 11.6-V dc output of the slave regulator is further regulated and overcurrent protected. This voltage is used to power the transistor amplifier and operate the varactor bias and GDO regulators.

### 5.3.7 Control Logic

Logics 1 and 2 provide redundant control to configure three coax switches in response to mode commands. Mode commands are fed into the logic through optical isolators. The logic circuit determines, from the command inputs, the desired positions of the RF switches. It compares the desired with the actual switch positions and, if a disparity exists, applies a pulse to the appropriate switch coil to update the configuration.

Table 5-1 presents the logic input equations to the logic 1 and 2 drivers and the associated relay coil driven by that logic, along with the coax switch RF path and preamp mode. The drivers are numbered 9 through 13 on each logic board. The brackets around the driver number and the relay coil denote logic 2 driven functions.

Table 5-2 shows how the preamp, power amp, transponder, and transponder frequency select functions affect the coax switch positions.

### 5.3.8 RF Coax Switches

All three RF coax switches, S1 through S3, are identical; however, S3 must handle more RF power since it is in the transmit link. The switches are capable of handling up to 175 watts RF nonswitching. During switching RF is removed from S3 by the preamp/power amp interlock on the power amp operate (normal) control. The power amp goes to the standby mode during preamp switching.

**Table 5-1. Preamp logic switching**

| Driver logic input                       | Driver logic 1 (2) | Relay coil | Coax sw path | Preamp mode                    |
|--|--------------------|------------|--------------|--------------------------------|
| XP1H + XP1L                              | 8<br>(9)           | 1A<br>(1B) | 1A1<br>1B1   | XPNDR 1 PRE 1<br>XPNDR 1 PRE 2 |
| XP2H + XP2L                              | 9<br>(8)           | 1B<br>(1A) | 1B2<br>1A2   | XPNDR 2 PRE 1<br>XPNDR 2 PRE 2 |
| XP1H + XP2H                              | 10<br>(10)         | 2A<br>(2B) | 2A2<br>2B1   | PRE 1 HIGH<br>PRE 2 HIGH       |
| XP1L + XP2L                              | 11<br>(11)         | 2B<br>(2A) | 2B2<br>2A1   | PRE 1 LOW<br>PRE 2 LOW         |
| PA1 (XP1H + XP2H) +<br>PA2 (XP1L + XP2L) | 12<br>(13)         | 3A<br>(3A) | 3A1<br>3A2   | PA1 HIGH<br>PA2 LOW            |
| PA1 (XP1L + XP2L) +<br>PA2 (XP1H + XP2H) | 13<br>(12)         | 3B<br>(3B) | 3B2<br>3B1   | PA1 LOW<br>PA2 HIGH            |

**Table 5-2. Preamplifier coax switch matrix**

| Preamp | Power amp       | XPNDR freq      | Coax sw path |               |                           | XPNDR freq               | Power amp | Preamp |
|--------|-----------------|-----------------|--------------|---------------|---------------------------|--------------------------|-----------|--------|
|        |                 |                 | S1 (xp-pre)  | S2 (freq/pre) | S3 <sup>a</sup> (freq/pa) |                          |           |        |
| 1      | 1               | 1-HI            | 1A1          | 2A2           | 3A1                       | <del>XPNDR 1 PRE 1</del> | 2         | 2      |
|        |                 | <del>1-LO</del> | 1A2          | 2A1           | 3A2                       | 2-LO                     |           |        |
|        |                 | 1-LO            | 1A1          | 2B2           | 3B2                       | <del>XPNDR 1 PRE 2</del> |           |        |
|        |                 | <del>1-HI</del> | 1A2          | 2B1           | 3B1                       | 2-HI                     |           |        |
|        | 2               | 2-HI            | 1B2          | 2A2           | 3B1                       | <del>XPNDR 2 PRE 1</del> | 2         |        |
|        |                 | <del>2-LO</del> | 1B1          | 2A1           | 3A2                       | 1-LO                     |           |        |
|        |                 | 2-LO            | 1B2          | 2B2           | 3A2                       | <del>XPNDR 2 PRE 2</del> |           |        |
|        |                 | <del>2-HI</del> | 1B1          | 2B1           | 3B1                       | 1-HI                     |           |        |
|        | 2               | 1-HI            | 1A1          | 2A2           | 3B1                       | <del>XPNDR 1 PRE 1</del> | 1         |        |
|        |                 | <del>1-LO</del> | 1A2          | 2A1           | 3B2                       | 2-LO                     |           |        |
|        |                 | 1-LO            | 1A1          | 2B2           | 3A2                       | <del>XPNDR 1 PRE 2</del> |           |        |
|        |                 | <del>1-HI</del> | 1A2          | 2B1           | 3A1                       | 2-HI                     |           |        |
| 1      | 2-HI            | 1B2             | 2A2          | 3A1           | <del>XPNDR 2 PRE 1</del>  | 1                        |           |        |
|        | <del>2-LO</del> | 1B1             | 2A1          | 3B2           | 1-LO                      |                          |           |        |
|        | 2-LO            | 1B2             | 2B2          | 3B2           | <del>XPNDR 2 PRE 2</del>  |                          |           |        |
|        | <del>2-HI</del> | 1B1             | 2B1          | 3A1           | 1-HI                      |                          |           |        |

<sup>a</sup> Switch S3 is not used in RCV-only modes.



### 5.3.9 Control Logic Driver Operation

The following is a description of the operation of a typical driver. If a disparity exists between the coax switch position and the desired position, the input to the NAND gate will be satisfied and the driver turned on. After approximately 75 msec, the cutoff Resistor Capacitor (RC) circuit, which has been maintaining the driver on, times out and the driver is turned off. Note that the talkback signal is lost the moment the coax switch has switched. Switching time is less than 50 msec.

The 0.1-msec delay circuit prevents the driver from coming on if the coax switch is already in the desired position when power is first applied to the preamp.

### 5.3.10 Power Relay Drivers

Relay drivers 1 and 2 are used to apply power to logics 1 and 2, depending on which preamp is selected. The relay driver is similar to the coax relay driver circuit.

### 5.3.11 Electrical Power

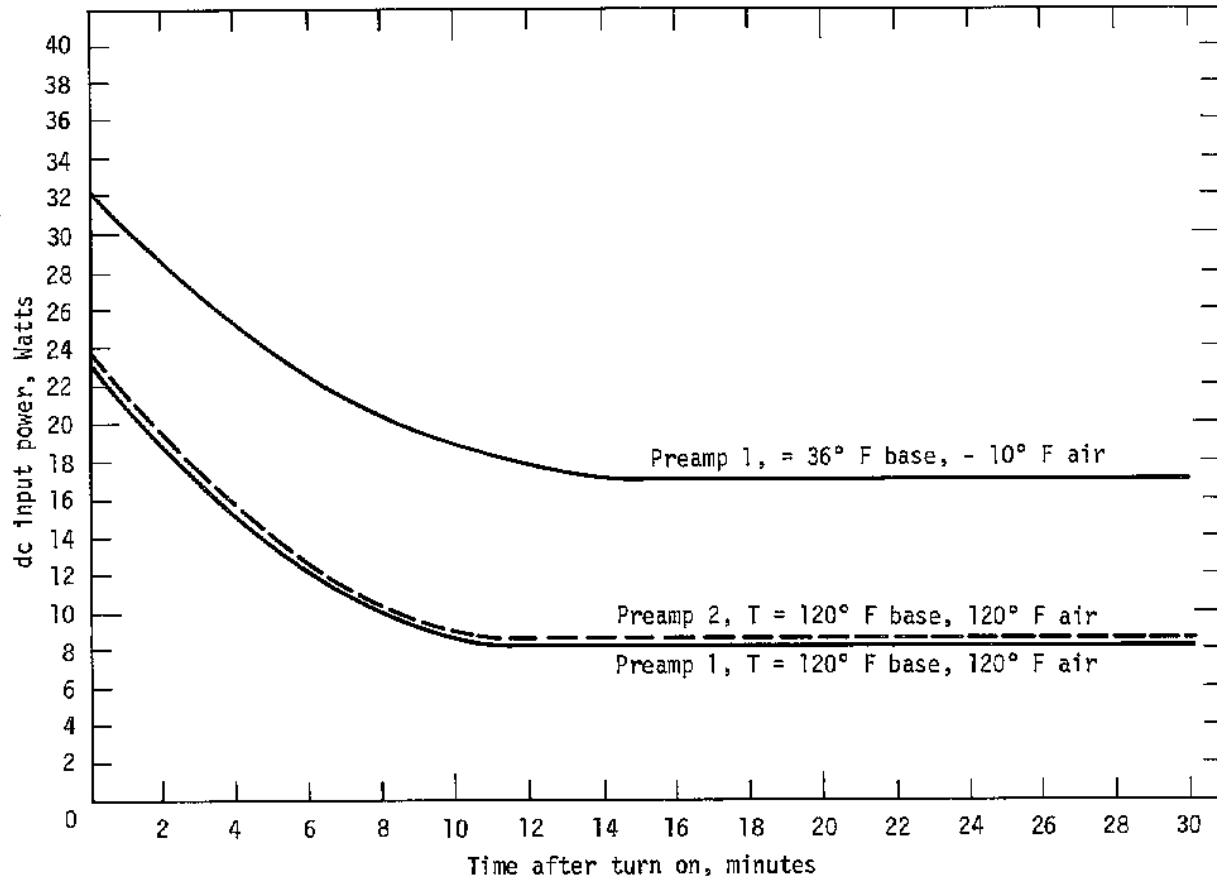
The dc input power vs. time curves for the engineering model at two different conditions is shown in Figure 5-2. Preamp dc power usage at T - 0 vs. 10 minutes is shown in Table 5-3.

**Table 5-3. Preamp dc power (watts)**

| Time   | One on            |        | One STBY          | Total |
|--------|-------------------|--------|-------------------|-------|
|        | HTR               | PREAMP |                   |       |
| T - 0  | 23.5              | 13     | 23.5              | 60    |
| 10 min | 13.5 <sup>a</sup> | 13     | 13.5 <sup>a</sup> | 40    |

<sup>a</sup> Varies from 8 to 19 W, depending on baseplate temperature.

Note that both preamplifier heater pairs are turned on by a single command which may be used as a standby mode. The HEATER ON command is not required for the operating preamplifier, since the heater is powered when the preamplifier is selected via a diode.



**Figure 5-2. DC input power**

**5.3.12 Weight**

25.6 pounds maximum

**5.4 INSTALLATION**

The preamplifier is mounted on bay 3A dual coldplates (ref. SB 20, COMMUNICATIONS AND INSTRUMENTATION SYSTEM WATER AND AIR-COOLED EQUIPMENT).

**5.5 DESCRIPTION OF OPERATION**

The preamplifier is used to amplify the received S-band signal from the antenna system and provide routing of the amplified transmit signal from the selected power amp. The preamplifier also provides diplexing of the transmit and receive signal to/from a single antenna system.

**5.5.1 Crew Controls**

Panel A1 switch S10  
 S-Band PM  
 PRE AMPL - 1/OFF/2

**5.5.2 Ground Commands**

| DSM    | Stimulus number | Title                | MDM | CMD reset | HEX set  |
|--------|-----------------|----------------------|-----|-----------|----------|
| 4722 F | V74K3071U       | PREAMP 1 - ON        | PF1 | 710901FF  | 79090039 |
|        |                 |                      | PF2 | 710A01FF  | 790A0039 |
| 4723 F | V74K3072U       | PREAMP 1/2 - OFF     | PF1 | 710901FF  | 7909003A |
|        |                 |                      | PF2 | 710A01FF  | 790A003A |
| 4724 F | V74K3073U       | PREAMP 2 - ON        | PF1 | 710901FF  | 7909003B |
|        |                 |                      | PF2 | 710A01FF  | 790A003B |
| 4725 F | V74K3075U       | PREAMP HEATERS - OFF | PF1 | 710901FF  | 7909003D |
|        |                 |                      | PF2 | 710A01FF  | 790A003D |
| 4726 F | V74K3074U       | PREAMP HEATERS - ON  | PF1 | 710901FF  | 7909003C |
|        |                 |                      | PF2 | 710A01FF  | 790A003C |

**5.5.3 Telemetry**

The preamplifier does not have any telemetry which will directly provide information on its performance; however, the transponder AGC, when compared to expected RF levels, will indicate any loss of gain the preamplifier may have. The preamplifier gain is 23 to 25 dB.

V74X4776E Preamp 1 ON

V74X4777E Preamp 2 ON

A logical "1" indicates which preamplifier is selected.

V74X4707E Preamp 1 heater ON

V74X4708 Preamp 2 heater ON

A logical "1" indicates both preamp heaters are on. Ground Control Interface Logic (GCIL) fail state is both heaters on.

### 5.5.4 Operational Instructions

#### 5.5.4.1 Warmup Characteristics

The preamplifier requires a warmup period of 4 to 18 minutes to stabilize if the heaters are initially off. In 4 minutes, the gain is 22 dB, and at 18 minutes, full gain can be expected. Two separate heaters are required to stabilize the RF, circulator assembly impedance ( $95^{\circ} \pm 25^{\circ} \text{ F}$ ), and the GDO frequency ( $175^{\circ} \pm 1^{\circ} \text{ F}$ ), respectively.

Full gain is achieved in less than 10 seconds if the heaters were on for at least 18 minutes prior to amplifier selection.

The gain characteristics vs. time after turnon for the engineering model is shown in Figure 5-3. The initial conditions are with the heater off.

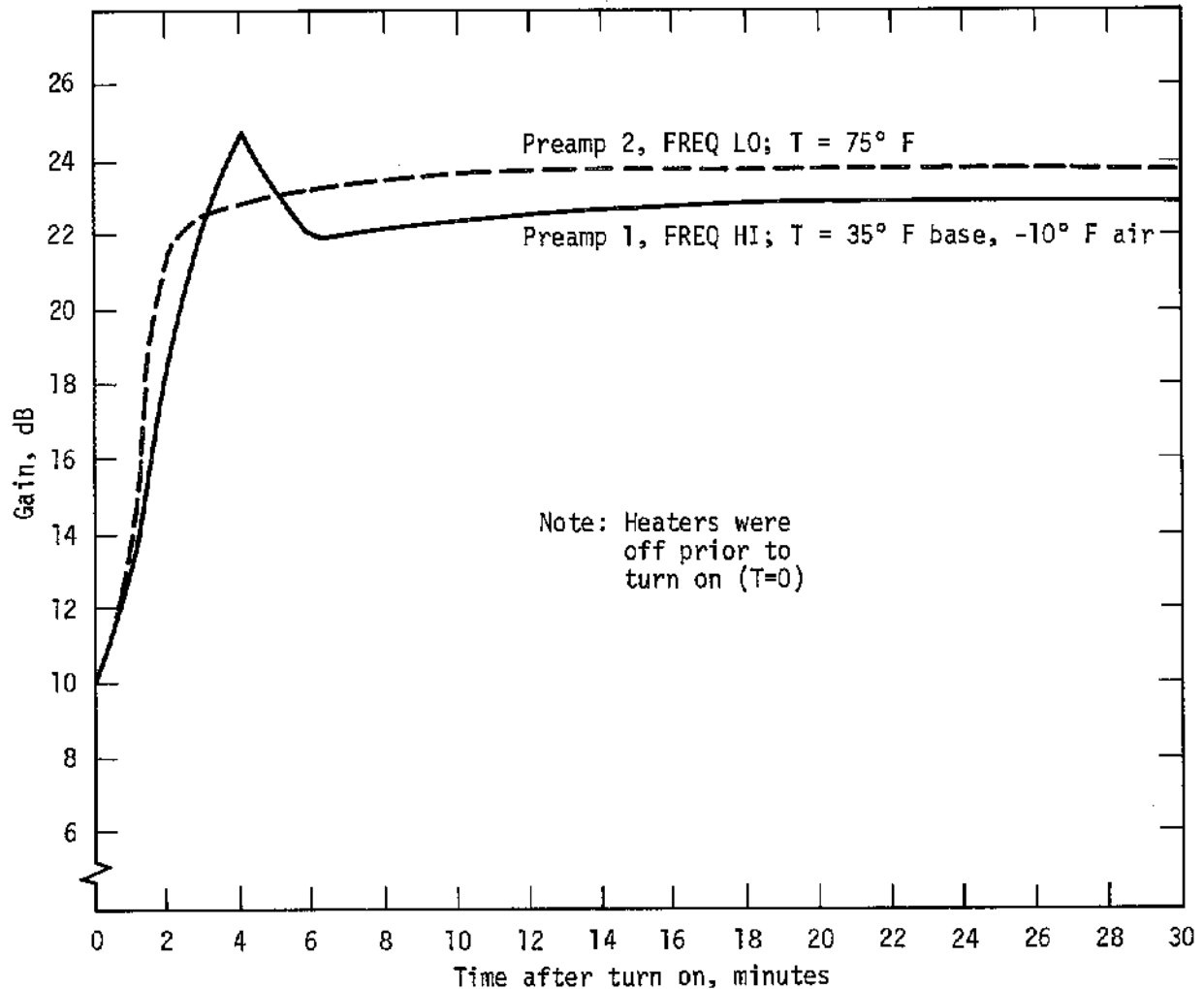


Figure 5-3. Preamp gain

### 5.5.4.2 Damaging Commands

Control circuit failure, such that preamps 1 and 2 are energized at the same time, will add additional heat, thermally stress parts, and induce failures.

Control circuit failure, such that transponders 1 and 2, frequency high and low, or power amps 1 and 2 are selected at the same time, would cause coax switches S1, S2, or S3 to cycle and reduce the life of the switches.

### 5.5.4.3 Dynamic Range

-55 dbm to -130 dbm with no damage for up to +3 dbm input.

## 5.6 REFERENCES

### A. Documentation

1. RI Schematic Diagram, COMM & Track Power Amp Subsystem, VS70-740139, Rev. D, 7-31-84
2. RI Specification Equipment, S-Band Network, MC478-0106 Rev. E
3. S-Band Preamplifier, CDR, Addendum, A.I.L. for T.R.W., September 15, 1977
4. S-Band Preamplifier, PDR, Addendum, A.I.L. for T.R.W., October 13, 1976
5. S-Band Preamplifier, PDR, vols I and II, September 1976

### B. A.I.L. LRU Schematics

1. S-BD PREAMP SCHEM DIAG, 557502D, August 1, 1977
2. ELECTRONIC SUPPORT, SCHEM DIAG, 557517C, August 1, 1977
3. TRANSISTOR AMPLIFIER, SCHEM DIAG, 557595B, April 20, 1977
4. PARAMETRIC AMPLIFIER, SCHEM DIAG, 557602A, April 20, 1977
5. TEMP CONTROL AND PARAMP REGULATORS, SCHEM DIAG, 557641B, April 20, 1977
6. DIPLEXER AND SWITCH, SCHEM DIAG, 557699NC, August 2, 1977
7. LOGIC MATRIX AND SWITCH DRIVER, SCHEM DIAG, 557852G, June 2, 1977
8. SWITCH REGULATOR AND DC-DC CONVERTER, SCHEM DIAG, 557862B, November 24, 1976

## 5.7 OPERATIONAL NOTES

- Heaters are normally commanded (GCIL only) on for the entire flight.
- When switching preamplifier, full stabilized gain can be expected in less than 10 seconds.

THIS PAGE INTENTIONALLY BLANK

## SECTION 6 – S-BAND POWER AMPLIFIER

### CONTENTS

| Section       |   | Page |
|---------------|---|------|
| 6.1           | GENERAL DESCRIPTION .....                         | 6-1  |
| 6.2           | DESCRIPTION .....                                 | 6-1  |
| 6.2.1         | Electrical .....                                  | 6-1  |
| 6.2.2         | Mechanical .....                                  | 6-7  |
| 6.3           | INSTALLATION .....                                | 6-10 |
| 6.4           | DESCRIPTION OF OPERATION .....                    | 6-10 |
| 6.4.1         | Controls .....                                    | 6-10 |
| 6.4.2         | Responses to Control Inputs .....                 | 6-11 |
| 6.4.3         | Temperature Monitor .....                         | 6-12 |
| 6.4.4         | Telemetry.....                                    | 6-14 |
| 6.5           | SPECIAL TM COMPUTATIONS .....                     | 6-14 |
| 6.6           | REFERENCES .....                                  | 6-14 |
| <br>          |   |      |
| <b>Figure</b> |   |      |
| 6-1           | S-Band PM power amplifier interface diagram ..... | 6-2  |
| 6-2           | Switchable automatic level control schematic..... | 6-4  |
| 6-3           | Dual isolator/power monitor schematic.....        | 6-6  |
| 6-4           | Chassis with RF chain installation .....          | 6-8  |
| 6-5           | Power supply .....                                | 6-9  |
| 6-6           | TWT and housing capsule.....                      | 6-10 |
| 6-7           | TWT collection temperature curves.....            | 6-13 |



THIS PAGE INTENTIONALLY BLANK

## SECTION 6 S-BAND POWER AMPLIFIER

### 6.1 GENERAL DESCRIPTION

The S-Band Power Amplifier (PA) Line Replaceable Unit (LRU) contains redundant power amplifiers for amplification of the S-band Phase Modulation (PM) signal from the transponder in the Space Tracking and Data Network (STDN) HI mode and the Tracking and Data Relay Satellite (TDRS) mode.

The Radio Frequency (RF) output is 144 to 151 W, requiring 329 to 340 W input power at 28 V dc. The high voltage is held off the Traveling Wave Tube (TWT) by a 140-second timer to allow the TWT filament to warm up when the OPERATE mode (normal command) is selected from a cold start. The STANDBY mode, requiring 22 W, is provided for "instant-on" operation from the STANDBY mode.

The power amplifier interfaces are shown in Figure 6-1. The interface with the preamplifier is to provide high and low frequency dual diplexer interconnect switching to the antenna system.

### 6.2 DESCRIPTION

The following paragraphs describe the power amplifier electrical and mechanical characteristics.

#### 6.2.1 Electrical

Switchable Automatic Level Control (6.2.1.1)

Control Logic (6.2.1.2)

Dual Power Monitor (6.2.1.3)

Low Voltage Power Supplies (6.2.1.4)

Pulse Width Monitor (6.2.1.5)

High Voltage Supply (6.2.1.6)

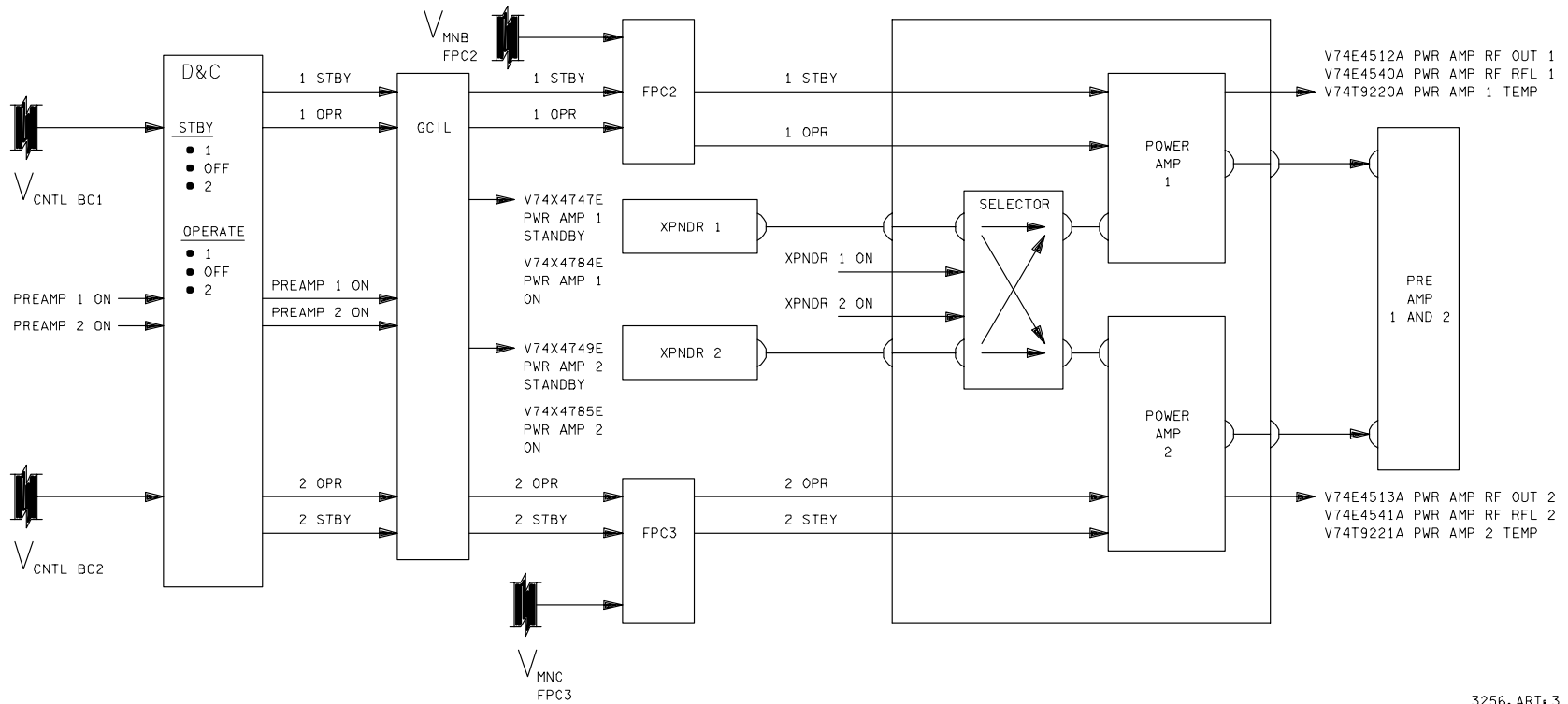
Traveling Wave Tube (6.2.1.7)

Dc Input Power (6.2.1.8)

RF Input and Output Power (6.2.1.9)

##### 6.2.1.1 Switchable Automatic Level Control

The Switchable Automatic Level Control (SALC) contains the RF diode selector switch for routing of the RF from the transponders to the selected power amplifier. Also, the SALC provides Positive-Intrinsic-Negative (PIN) diode attenuators to control the RF level into the TWT. The control loop contains an RF level detector whose output is fed back through an OP amp to control the bias on the PIN diode attenuator.



3256. ART 3

Figure 6-1. S-Band PM power amplifier interface diagram

A. PIN Diode Attenuators

The PIN diode attenuators maintain the TWT input within  $\pm 0.6$  dB, with an input RF range of 26.5 to 31.5 dBm. Control for the PIN diode attenuator comes from the rf level detectors through the automatic level control amplifier. This amplifier is biased, so that if the input drive drops below 24.5 dBm, the RF threshold relay is energized and the pulse width monitor circuit inhibits the TWT high voltage. The attenuator will provide maximum power transfer with no control input.

B. RF Diode Switch

The RF switch contains RF diodes which complete RF paths and terminate quarter wavelength RF paths to reflect an RF open circuit when bias is ON. The bias is "on" when alternate combinations of power amplifiers and transponders are selected; i.e., PA2/XPNDR 1 or PA1/XPNDR 2.

### 6.2.1.2 Control Logic

The logic performs two functions, control of the filament warmup cycle and primary 28-V dc voltage sensing.

A. Low Input Voltage Cutoff

The low voltage comparator senses the primary 28-V dc input power, and provides a reset to the 140-second timer when the input voltage drops below 24 V dc for 0.5 msec.

B. Filament Warmup Cycle

Primary power is applied to the PA in either the OPERATE mode or STANDBY mode. The OPERATE mode also provides the NORMAL ON command, which enables the HIGH VOLTAGE ON relay driver. After the 140-sec timer times out, the relay driver energizes RELAY K1, and the pulse width monitor circuit operates to put high voltage on the TWT.

The STANDBY mode provides power to the TWT filament and low voltage power supply, so that the PA can be put into the OPERATE mode when needed without the 140-second delay.

The 140-second timer consists of a divide by  $2^{23}$  counter clocked by the 30-MHz oscillator.

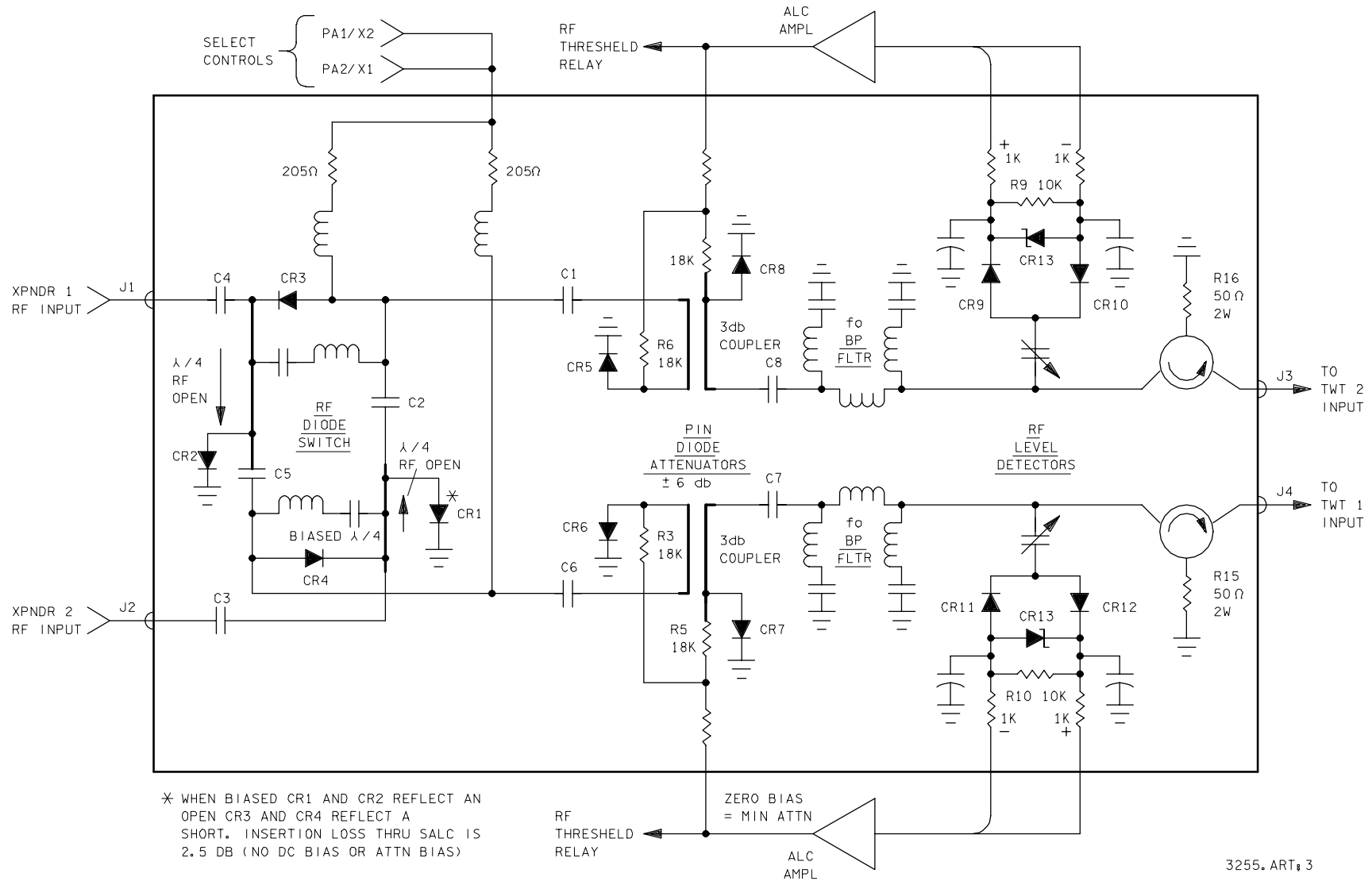


Figure 6-2. Switchable automatic level control schematic

### 6.2.1.3 Dual Power Monitor

The power monitor circuits use the 23-dB isolation and directivity of the circulators to provide the forward and reflected power telemetry signals. The power detectors incorporate low pass filters, so that they measure the true signal and do not respond to harmonics. The detector diodes are zener protected to inhibit potential problems with static discharge.

The isolator protects the TWT output from load variations and TWT output variations. A worst case change in the TWT will cause the output Voltage Standing Wave Ratio (VSWR) to vary from 1.1 to 1.13 as a result of the isolation.

No damage or performance loss will occur if the LRU output is shorted or open for a period of 30 minutes or less.

Figure 6-3 is a schematic of the dual isolation/power monitor, one for each power amplifier.

### 6.2.1.4 Low Voltage Power Supplies

The low voltage power supply consists of Low Voltage Converters (LVC) 1 and 2, and the 5-V dc and 18-V dc regulators.

LVC 1 is a dc-dc converter which provides 36 V ac for TWT heater filament, bias voltages for the current inverter, and power to telemetry circuits.

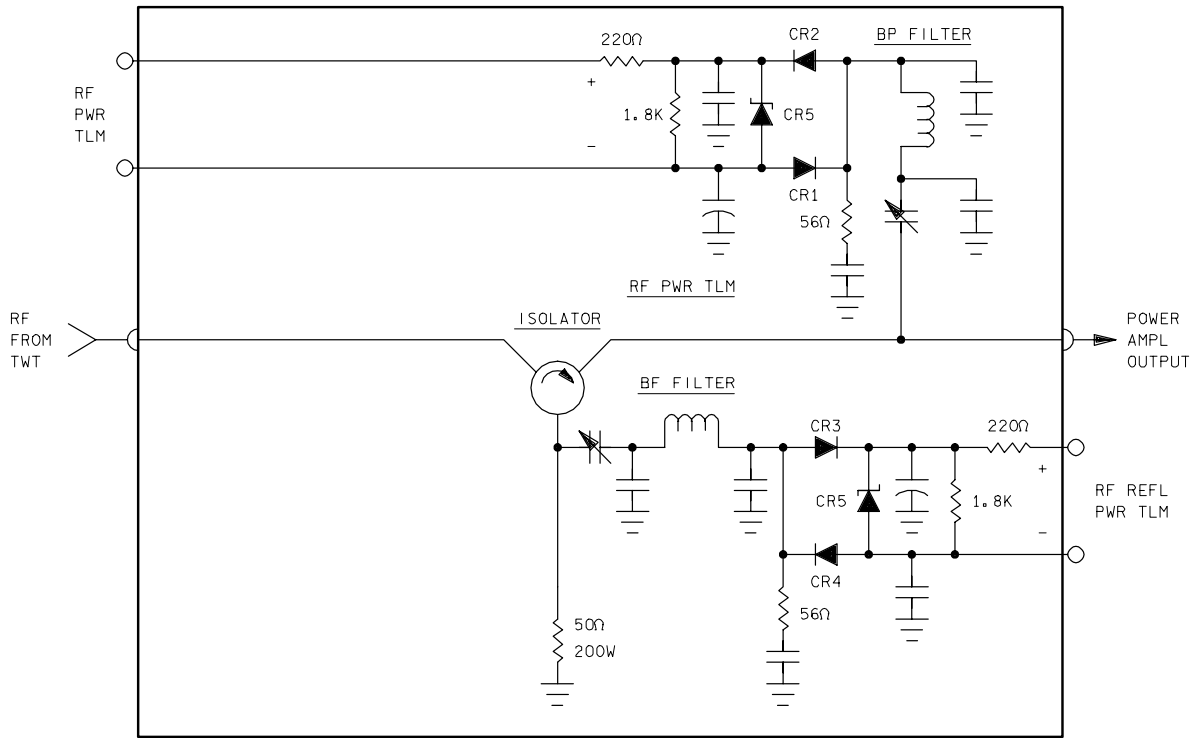
LVC 2 provides the normal bias to the buck regulator and power to the RF diode switch control circuit. The normal bias output is controlled by the NORMAL command via one of the K1 relay contacts.

### 6.2.1.5 Pulse Width Monitor

The Pulse Width Monitor (PWM) optimizes the duty ratio of the buck regulator. At startup of the current inverter and high voltage supply, the 21-V bus voltage from the buck regulator is "ramped up" to control in-rush current on the 28-V dc input line. Ac and dc voltages are monitored for voltage changes to provide transient response. The duty cycle of the buck regulator is determined by comparing the PWM reference (30 MHz OSC) sawtooth to an accumulated error voltage, and inhibiting the buck regulator basedrive when the reference is higher than the error voltage.

### 6.2.1.6 High Voltage Supply

Regulated 21 V dc drives the switching transistors of the high voltage supply current inverter. High voltage is gradually applied to the TWT after warmup and a NORMAL ON command.



3254. ART 3

**Figure 6-3. Dual isolator/power monitor schematic**

The helix-to-cathode potential is tightly regulated by the helix regulator. This voltage determines the speed of the electrons from the cathode down the center of the helix. Regulated anode-helix voltage is provided by the anode regulator.

#### **6.2.1.7 TWT**

The TWT consists of a heater, a slow-wave structure (helix), an electron beam traveling through the helix, a magnetic field to focus the electrons inside the helix, and two collectors to collect the electron beam.

The RF signal traveling at the speed of light is supplied at the heater end of the helix. However, the axial velocity of the traveling wave is a little less than the velocity of the electron beam accelerated by the anode-to-cathode potential. The electric field component of the RF interacts with the electron beam. This interaction will cause the electrons to bunch up and slow down. As the electron beam slows down, it gives up energy to the RF electric field on the helix. As the interaction continues down the helix, the electric field becomes stronger, and the interaction increases. This creates a growing RF wave, and amplification is obtained.

#### **6.2.1.8 DC Input Power**

Operate mode - 390 W  
Standby mode - 11 W

#### **6.2.1.9 RF Input and Output Power**

RF input - 26.0 to 34.5 dBm

Note: High voltage is removed when RF input falls below 24.5 dBm  
(0.355 W)

RF output (typical) - 144 to 151 W  
RF output varies with transmit frequency

#### **6.2.2 Mechanical**

Figure 6-4, Figure 6-5, and Figure 6-6 show the power amplifier chassis, power supply, and TWT, respectively.

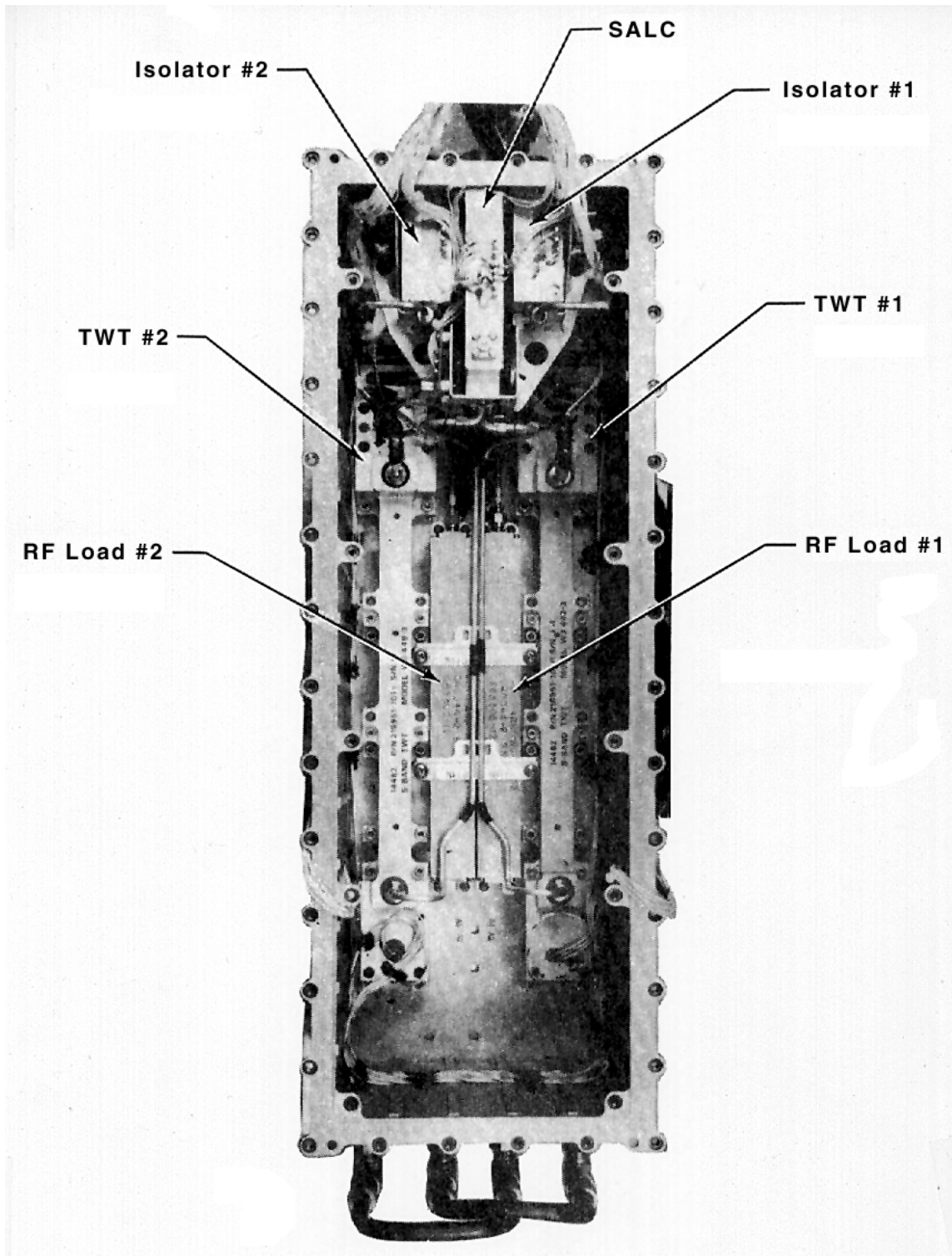
##### **6.2.2.1 Weight**

Less than 32.5 pounds.

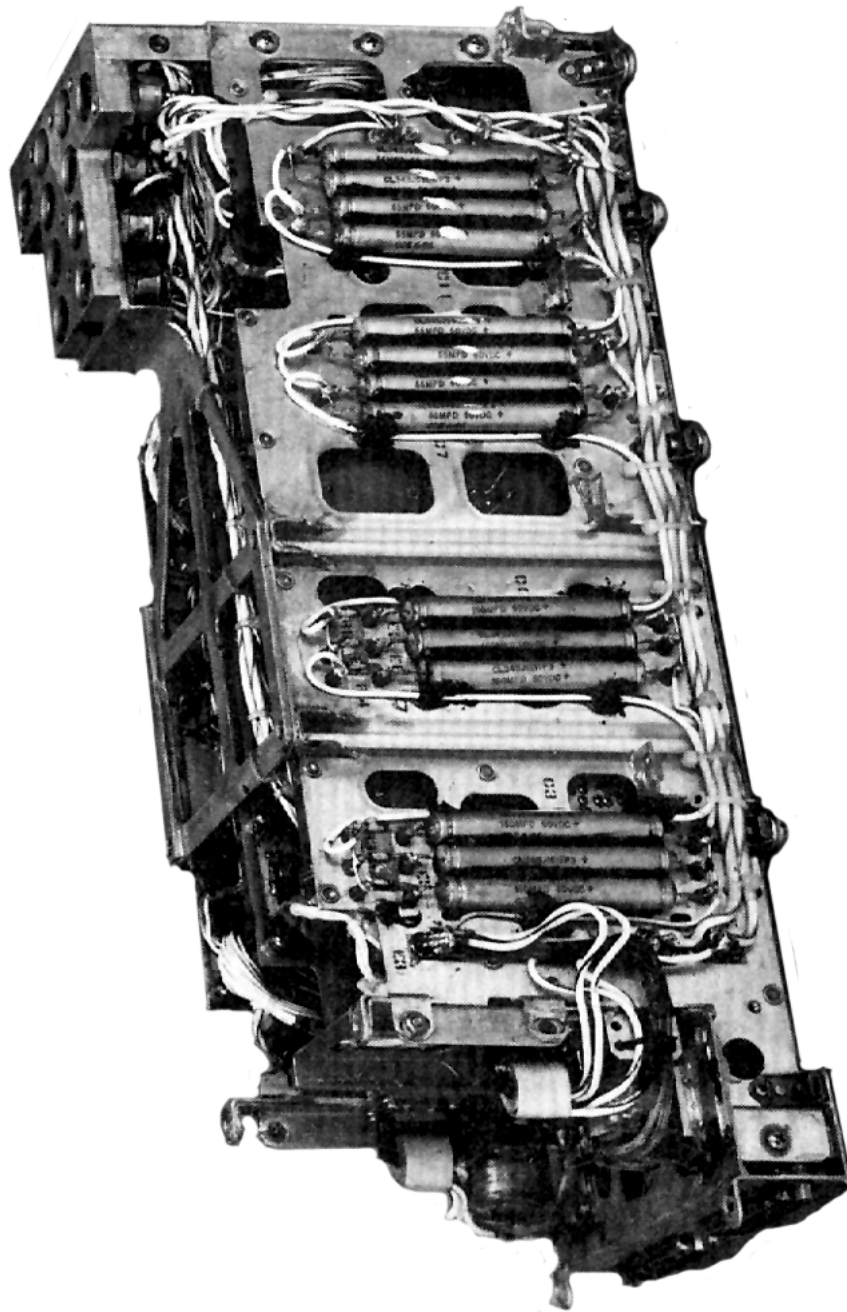
##### **6.2.2.2 Temperature Sensor**

The temperature sensor is mounted on the TWT collector housing.

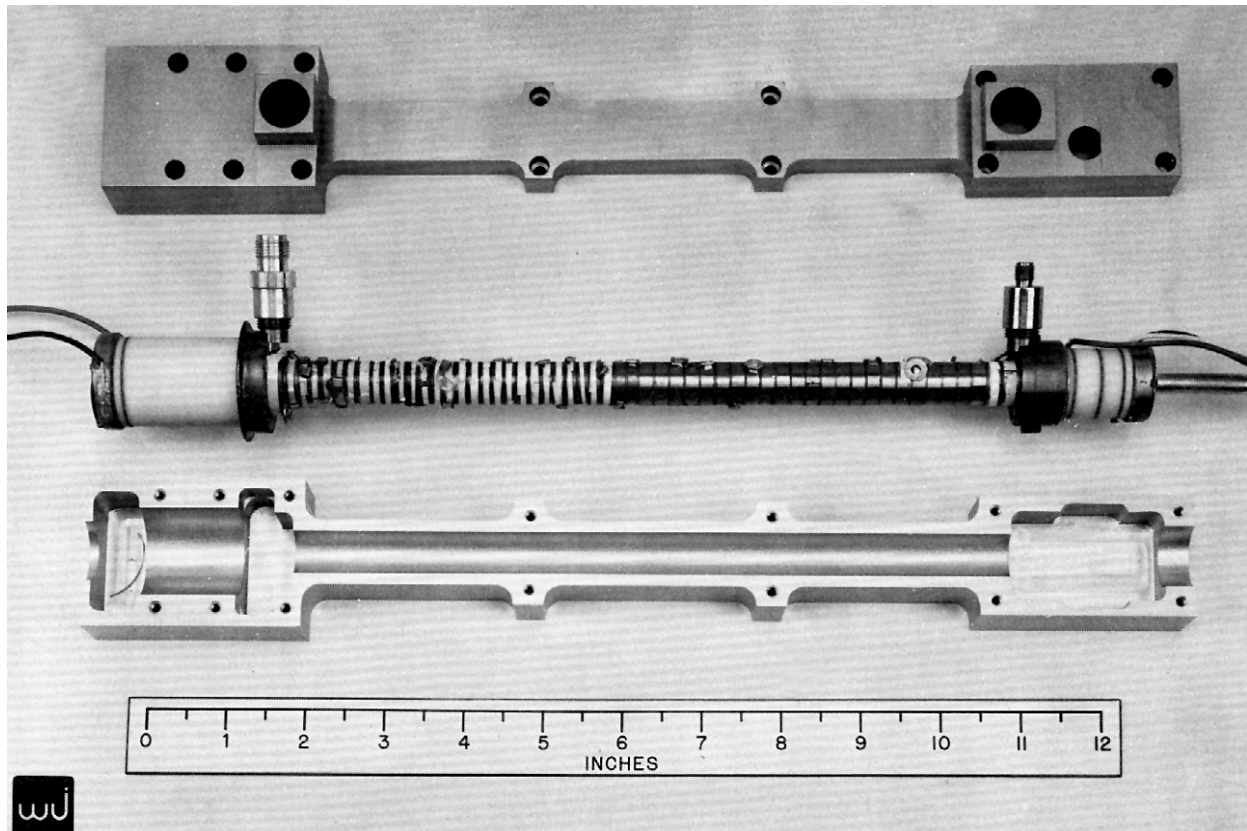




**Figure 6-4. Chassis with RF chain installation**



*Figure 6-5. Power supply*



**Figure 6-6. TWT and housing capsule**

### 6.3 INSTALLATION

Systems brief, COMMUNICATIONS AND INSTRUMENTATION SYSTEM WATER AND AIR COOLED EQUIPMENT, shows the location (bay 3A) and installation of the power amplifier.

The amplifier is on the primary and secondary water coolant loop.

### 6.4 DESCRIPTION OF OPERATION

The power amplifier is part of the S-band PM system and is used only in the STDN high and TDRS modes. A description of the system is contained in the S-band PM system brief.

#### 6.4.1 Controls

A. (PNL A1) S-band PM PWR AMP Switches

S11 Standby 1/OFF/2

S12 Operate 1/OFF/2

B. GCIL Commands

S-BD PA STBY - 1  
S-BD PA - 1/2 OFF  
S-BD PA STBY - 2

S-BD OPR 1  
S-BD OPR 1/2 OFF  
S-BD OPR 2

A 1-second delay power controller in the Operate 1 and Operate 2 control lines delays the operate mode (high voltage on) and thus power amplifier output until the coax switch S3 in the preamplifier has completed transfer; transfer will occur when changing frequency and power amplifiers.

Note that preamplifier 1 or 2 must be selected for the operate controls to be active.

C. Transponder Select Inputs

S-band transponders 1 and 2 select lines are input to the power amplifier for routing control of the active transponder to the selected power amplifier.

#### 6.4.2 Responses to Control Inputs

A. NORMAL ON command (no warmup)

Normal startup with NORMAL command preceded with short STANDBY situation. Timer is initiated at 24 V on bus B or C. Timeout is  $140 \pm 10$  seconds. The TWT is ramped on after timeout, following logic delays of up to 5 msec. RF output is less than 1 W in 20 msec, less than 30 W in 50 msec, and full power is obtained before 200 msec.

B. NORMAL OFF command

NORMAL command to OFF quenches RF (<1 W) in 20 msec.

C. NORMAL ON command (STANDBY ON)

NORMAL ON after timeout after a long (greater than 140 sec) STANDBY situation. TWT is actuated (after logic delays) immediately after NORMAL command.

D. Undervoltage turnoff

An undervoltage turnoff is turnoff due to line fault.

A line fault of more than 0.4 msec at 24 V or more than 0.6 msec at 32 V will turn LRU into STANDBY and restart 140-second timeout interval.

E. Transponder switchover (loss of RF input)

Whenever the TWT is energized and the RF input is removed, the RF output goes to zero.

After 6 msec without RF input, the TWT is completely deenergized. As the alternate transponder is selected, the High Voltage Control (HVC) is commanded within 6 msec to energize the TWT. Within an additional 50 msec, the TWT will provide 30 W (maximum) of RF output. Full power output will be obtained in 200 msec.

### 6.4.3 Temperature Monitor

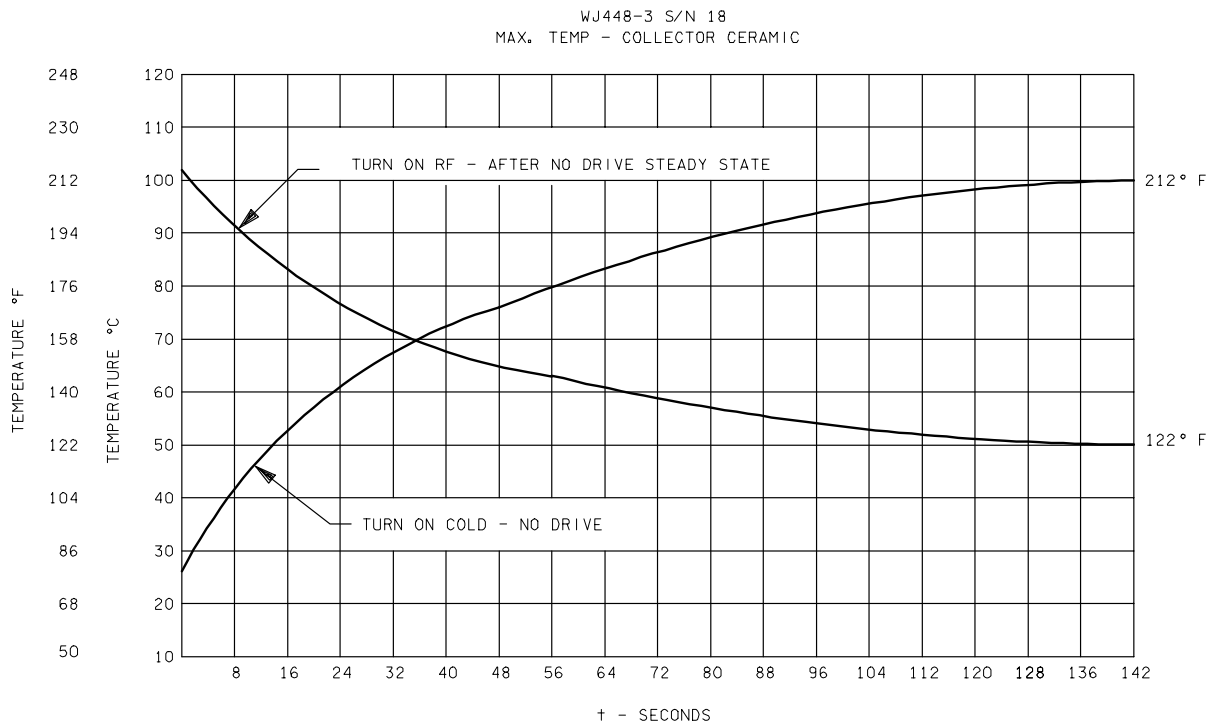
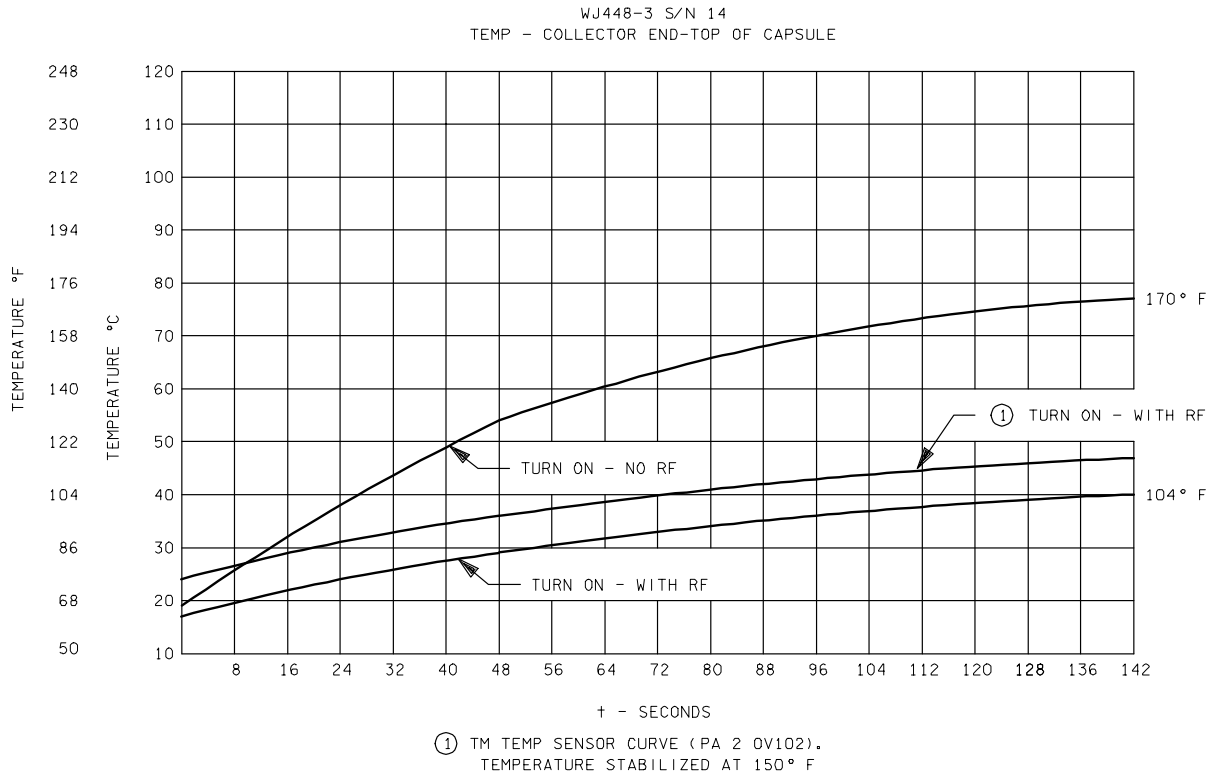
The temperature monitor sensor is located on the TWT mount at the end holding the TWT collector. Temperature curves showing the temperature profile of the collector for four different operating conditions are depicted in Figure 6-7.

The third curve on Figure 6-7 as plotted from OV-102 PA2 data (STS-9).

- Turn on - no RF input
- Turn on - with RF input
- Turn on RF after no RF input from a steady state temperature
- Turn on cold - no RF input

Note: These curves were not made with data from the TM temperature sensor but the temperature profile will be the same.





3258. ART 2

**Figure 6-7. TWT collection temperature curves**

#### **6.4.4 Telemetry**

The power amplifier telemetry is found in the S-band PM system brief.

#### **6.5 SPECIAL TM COMPUTATIONS**

None.

#### **6.6 REFERENCES**

- A. Critical Design Review, Watkins-Johnson, May 1977, Delta CDR, March 1978
- B. Schematic Diagram, C&T S-band Power Amplifier Subsystem, VS70-740139
- C. Schematic Diagram, SSSH, dwg 16.2 sheet 2 of 3
- D. Rockwell Spec, S-band Network Equipment, MC 478-0106

**SECTION 7 – S-BAND ANTENNA SYSTEM**  
**CONTENTS**

| <b>Section</b> | <b>Page</b>   |
|----------------|---|
| 7.1            | GENERAL ..... 7-1   |
| 7.2            | S-BAND SWITCH ASSEMBLY ..... 7-1  |
| 7.2.1          | Antenna Switch RF Assembly ..... 7-1  |
| 7.2.2          | RF Switch ..... 7-1   |
| 7.2.3          | RF Switch Pulser and Drivers ..... 7-2  |
| 7.2.4          | Logic Circuits ..... 7-7  |
| 7.2.5          | RF Characteristics ..... 7-8  |
| 7.3            | SWITCH BEAM CONTROL LRU ..... 7-8   |
| 7.3.1          | Input Forward/Aft GPC/Manual Beam Gates ..... 7-8   |
| 7.3.2          | FWD/AFT Beam Logic ..... 7-8  |
| 7.3.3          | Pulse/Driver Circuits ..... 7-9   |
| 7.4            | SWITCH BEAM ANTENNA FUNCTIONAL DESCRIPTION ..... 7-10   |
| 7.4.1          | Dipole Antenna ..... 7-13   |
| 7.4.2          | Stripline Hybrids ..... 7-16  |
| 7.4.3          | Coax Switch ..... 7-16  |
| 7.4.4          | Quad Antenna Performance Budget ..... 7-16  |
| 7.4.5          | Antenna Gain Coverage ..... 7-18  |
| 7.5            | S-BAND ANTENNA INSTALLATION ..... 7-20  |
| 7.6            | TELEMETRY ..... 7-25  |
| 7.7            | ANTENNA SYSTEM SPECIAL COMPUTATIONS ..... 7-26  |
| 7.7.1          | M02I0603R S-band Switch Beam Antenna Select FWD/AFT ..... 7-26  |
| 7.7.2          | M05I0200R Antenna Select (PM) Computation ..... 7-26  |
| 7.7.3          | M02G3210R S-band Quad Selected ..... 7-27   |
| 7.7.4          | M05I0201E, M06I0201E, M07I0201E, M08I0201E, ANT<br>SEL (PM) UR, LR, LL and UL Computations ..... 7-27 |
| 7.8            | REFERENCES ..... 7-31   |
| 7.9            | SUMMARY DATA ..... 7-31   |
| 7.10           | OPERATIONAL NOTES ..... 7-31  |



## TABLES

| Table |   | Page |
|-------|---|------|
| 7-1   | Antenna path matrix .....                       | 7-2  |
| 7-2   | Pulser output states .....                      | 7-7  |
| 7-3   | Stripline hybrid phase shift values .....       | 7-16 |
| 7-4   | Antenna performance budget .....                | 7-18 |
| 7-5   | Switch beam antenna percent coverage/gain ..... | 7-20 |
| 7-6   | S-BD switch beam antenna computation .....      | 7-29 |
| 7-7   | Antenna select (PM) computation .....           | 7-30 |

## FIGURES

| Figure |  |      |
|--------|--|------|
| 7-1    | S-band PM antenna system (switch beam) .....                     | 7-3  |
| 7-2    | RF switch .....  | 7-4  |
| 7-3    | Mechanical coax switch drawing for antenna switch assembly ..... | 7-5  |
| 7-4    | Antenna switch dual pulser .....                                 | 7-6  |
| 7-5    | Relay driver .....   | 7-9  |
| 7-6    | Switch beam antenna .....  | 7-11 |
| 7-7    | Switch beam antenna schematic .....                              | 7-12 |
| 7-8    | Dipole antenna .....   | 7-13 |
| 7-9    | Balun .....  | 7-14 |
| 7-10   | Stripline hybrids .....  | 7-15 |
| 7-11   | S-band switch beam antenna coax switch .....                     | 7-17 |
| 7-12   | Antenna mechanical offset .....                                  | 7-19 |
| 7-13   | Coverage zone for 2041.5 MHz operating frequency .....           | 7-21 |
| 7-14   | Coverage zone for 2106.4 MHz operating frequency .....           | 7-22 |
| 7-15   | Coverage zone for 2217.5 MHz operating frequency .....           | 7-23 |
| 7-16   | Coverage zone for 2287.5 MHz operating frequency .....           | 7-24 |
| 7-17   | S-band quad antenna installation .....                           | 7-26 |
| 7-18   | S-band antenna system coax cable schematic .....                 | 7-28 |
| 7-19   | S-band antenna system path diagram .....                         | 7-32 |

## SECTION 7 S-BAND ANTENNA SYSTEM

### 7.1 GENERAL

The S-band system is comprised of

- Four switched-beam antennas
- Beam control electronics
- Antenna switch electronics
- Interconnecting coax cables

The four switched-beam antennas are mounted equally spaced around the forward fuselage of the orbiter giving a quad type coverage gain for each of the antennas when selected by the antenna control electronics. The forward or aft coverage is controlled by the beam control electronics. Beam switching is accomplished by selecting the phased input to two crossed dipole antennas mounted in the antenna. Figure 7-1 is a block diagram of the switched-beam antenna system.

### 7.2 S-BAND SWITCH ASSEMBLY

The antenna switch consists of a Frequency Modulation (FM) Radio Frequency (RF) switch assembly, a Phase Modulation (PM) RF switch assembly, and separate redundant FM and PM control logic circuits, each with individual regulators powered by prime 28 V dc power.

Each of the five RF switches has redundant switch coils driven by separate logic and solid state Darlington drivers.

#### 7.2.1 Antenna Switch RF Assembly

The antenna switch RF assembly consists of one FM switch RF circuit and four PM switch RF circuits as shown in Figure 7-2. This assembly is mounted on the front connector face of the antenna switch LRU with the RF connectors on the front of the LRU as shown. The figure is shown looking from inside the LRU to the outside.

#### 7.2.2 RF Switch

The RF switch is of the reed type, with the reeds and contacts arranged as shown in Figure 7-3. The reeds are located with respect to the contacts, such that the actuation of the switch rocker arm by the switch coil will, for example, push the top reed down, making its contacts, and the associated underside reed on the same side of the rocker arm will be pushed down opening its contacts. The teeter-totter arrangement of the rocker arm between opposing switch coils provides the same type of reed-to-contact action, but in the opposite manner; i.e., the top reed opens and the underside reed closes.

The reeds are held in place by a permanent magnet when power is removed from the coil after the 100 msec coil drive pulse from the logic driver is removed. The “A” and “B” RF paths operate such that when one set of position contacts is open, the other set is closed. Antenna switching dropout time is ~1 msec to 5 msec.

Table 7-1 shows the switch configuration required to connect any one of the four RF ports to any one of the antennas.

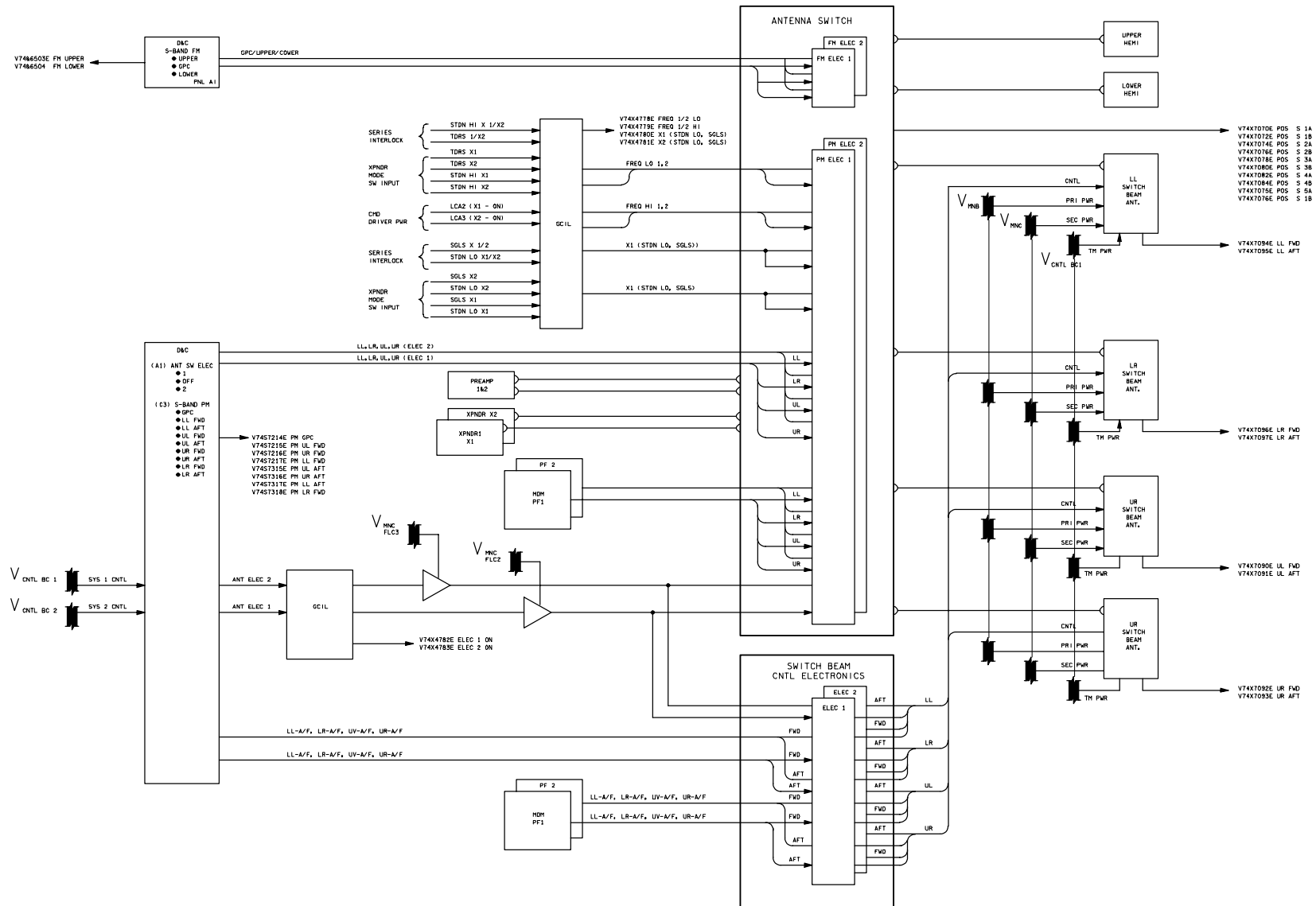
**Table 7-1. Antenna path matrix**

| RF port                             | Quad antenna |            |            |            |
|-------------------------------------|--------------|------------|------------|------------|
|                                     | UL           | UR         | LR         | LL         |
| XPNDR 1<br>DIRECT<br>(SGLS/STDN LO) | 4B2<br>1B2   | 4B2<br>1A1 | 4A2<br>3B1 | 4A2<br>3A2 |
| XPNDR 2<br>DIRECT<br>(SGLS/STDN LO) | 2B1<br>1A2   | 2B1<br>1B1 | 2A1<br>3A1 | 2A1<br>3B2 |
| FREQ<br>LOW<br>(TDRS/STDN HI)       | 2A2<br>1A2   | 2A2<br>1B1 | 2B2<br>3A1 | 2B2<br>3B2 |
| FREQ<br>HIGH<br>(TDRS/STDN HI)      | 4A1<br>1B2   | 4A1<br>1A1 | 4B1<br>3B1 | 4B1<br>3A2 |

### 7.2.3 RF Switch Pulser and Drivers

The control logic selects the switch coil pulsers which operate in a flip-flop manner, causing the pulser to output only when the state of the pulser is to be changed. The pulsers have a self-cutoff feature via a 100-msec time delay circuit. This delay circuit must discharge before the pulser state can be changed by a new input signal.

Redundancy is provided by having two sets of logic with separate and independent pulser/driver circuits, which, in turn, operate redundant switch coils.



0882, ART 4

Figure 7-1. S-band PM antenna system (switch beam)

The pulser shown in Figure 7-4 operates as follows: Starting with an assumed state No. 1 and the next input state change shown in Table 7-2.

Note that if the time delay circuit has not had time to decay or is charged and its nor gate input is selected again the time delay circuit will inhibit the switch driver input and thus the driver output and the proper antenna will not be selected. The decay time is less 100 msec.

- BOTTOM REEDS (SPRING LOADED CLOSED)
- TOP REEDS (SPRING LOADED OPEN)

NOTE: REEDS IN ANY COIL SET ARE EITHER OPEN OR CLOSED IN PAIRS.  
FOR EXAMPLE: WHEN "A" PAIR IS CLOSED "B" PAIR WILL BE OPEN.

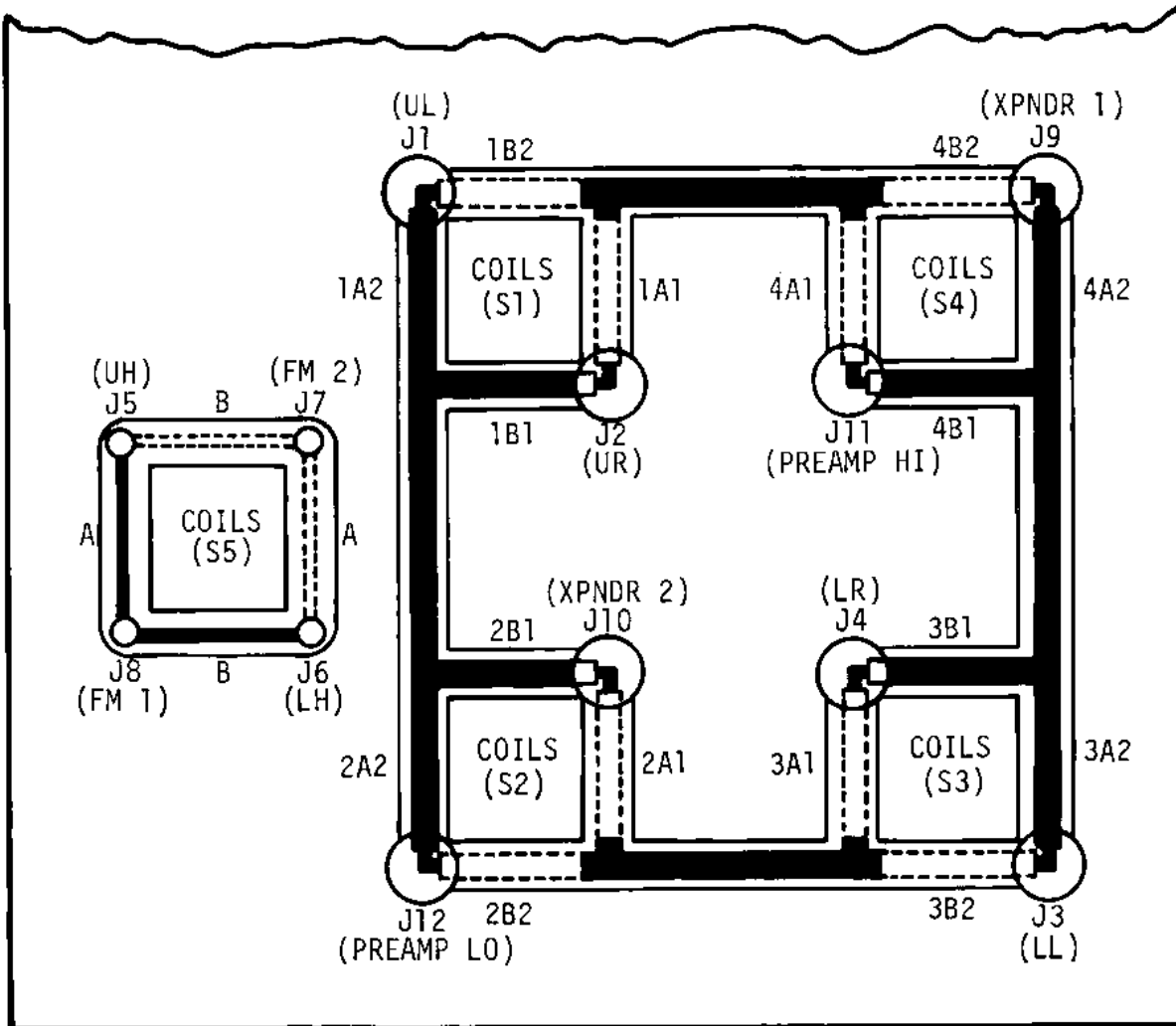
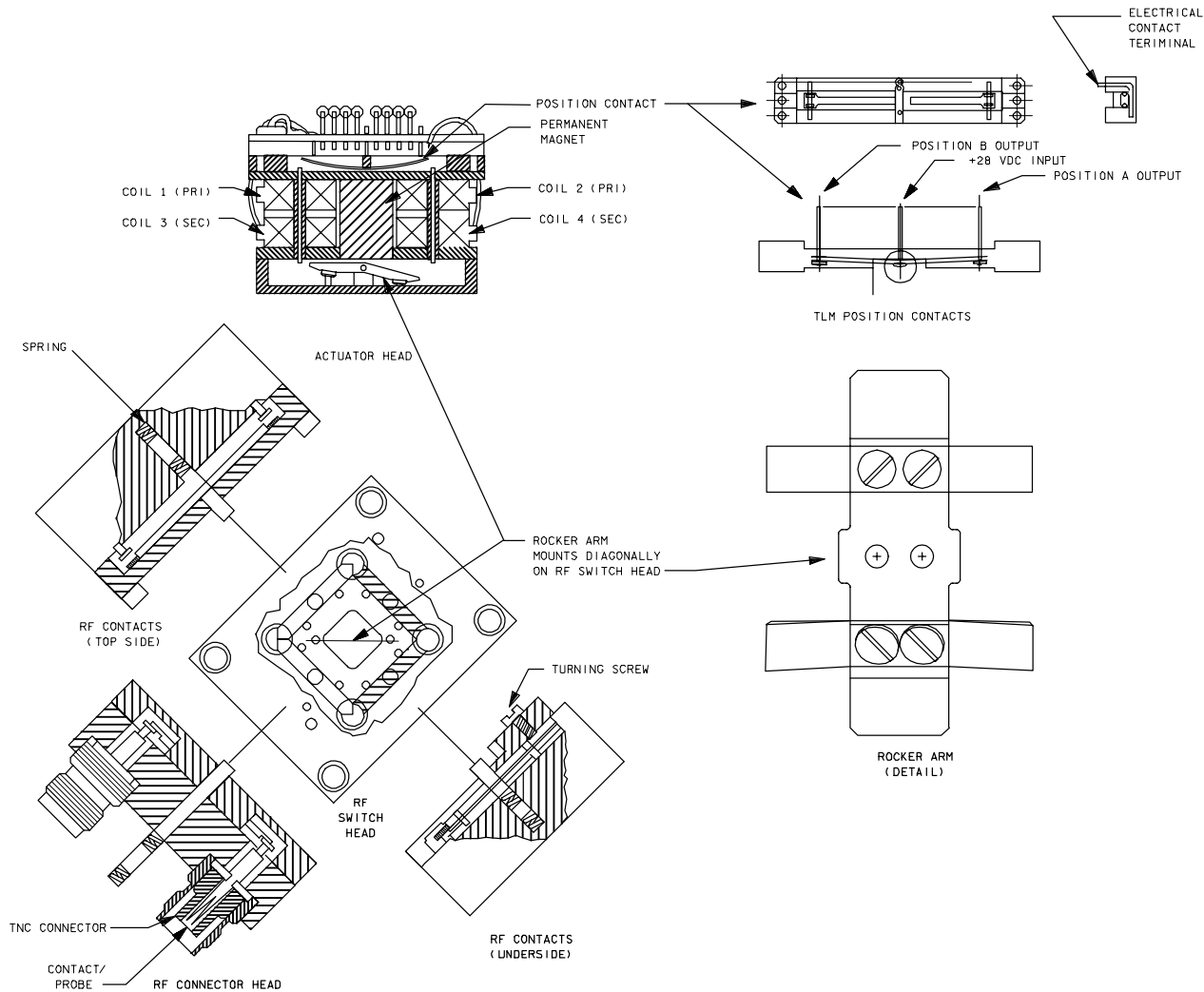


Figure 7-2. RF switch

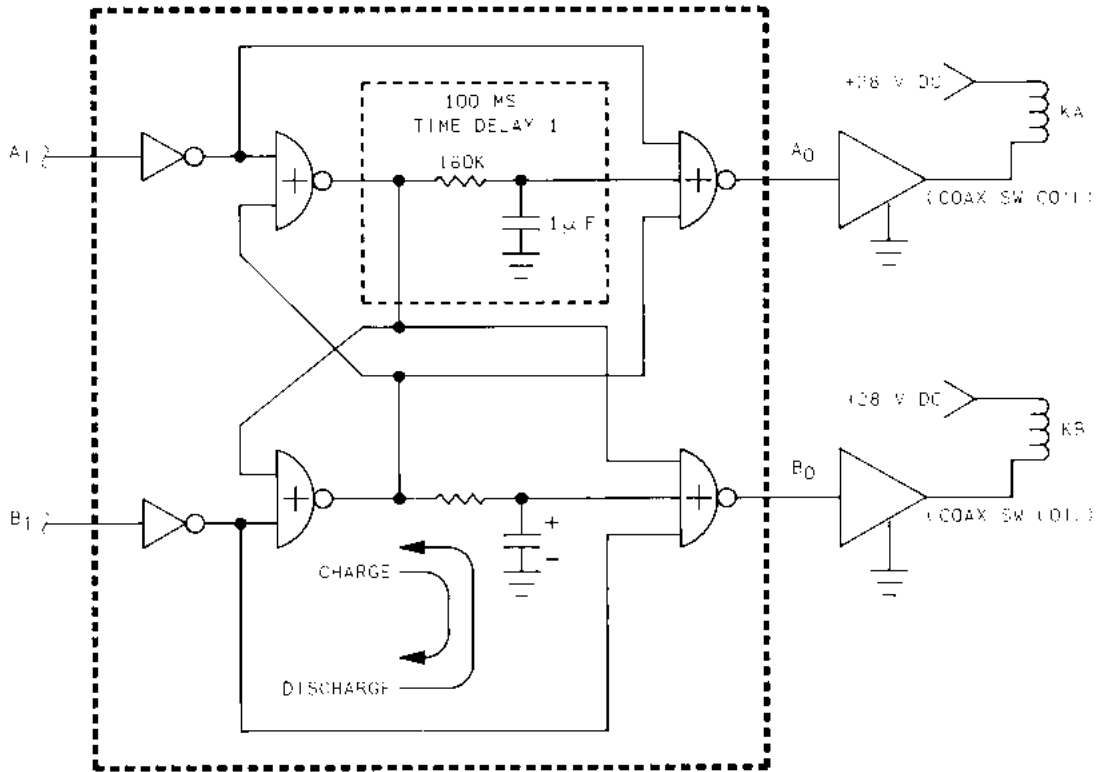


0889. ART, 2

Figure 7-3. Mechanical coax switch drawing for antenna switch assembly

NOTE

Therefore it is important that the GPC or D&C antenna select switch input does not select, deselect, and reselect the same pulser input faster than 100 msec.



0868, AR1:2

Figure 7-4. Antenna switch dual pulser

**Table 7-2. Pulser output states**

| STATE | INPUT (T)      |                | INPUT (T + 1)  |                | OUTPUT         |                | TIME DELAY |     |
|-------|----------------|----------------|----------------|----------------|----------------|----------------|------------|-----|
|       | A <sub>T</sub> | B <sub>T</sub> | A <sub>T</sub> | B <sub>T</sub> | A <sub>0</sub> | B <sub>0</sub> | A          | B   |
| 1     | 0              | 0              | 0              | 0              | 0              | 0              | DIS        | DIS |
| 2     | 0              | 0              |                | 0              |                | 0              |            | DIS |
| 3     | 1              | 0              | 1              | 0              | 0              | 0              | CHG        | DIS |
| 4     | 1              | 0              |                |                | 0              |                |            |     |
| 5     | 0              | 1              | 0              | 1              | 0              | 0              | DIS        | CHG |
| 6     | 0              | 1              |                | 1              | 0              | 0              | DIS        | CHG |
| 7     | 1              | 1              | 1              | 1              | 0              | 0              | DIS        | CHG |
| 8     | 1              | 1              |                |                | 0              | 0              | DIS        |     |
| 9     | 0              | 0              | 0              | 0              | 0              | 0              | DIS        | DIS |
| 10    | 0              | 0              |                |                | RACE           | RACE           |            |     |

O888. ART; 2

### 7.2.4 Logic Circuits

The logic input selector requires an enable signal from the panel control switch to accept the General Purpose Computer (GPC) ANTENNA SELECT commands; therefore, the manual antenna select controls override the AUTO SELECT commands.

The Frequency High (FH) and Frequency Low (FL) logic inputs derived from the TRANSPONDER FREQUENCY mode via the Ground Control Interface Logic (GCIL) drivers 14/8, 6/8, 14/7, and 6/7 override the transponder direct input controls, and therefore, the Tracking and Data Relay Satellite (TDRS) and Spaceflight Tracking and Data Network (STDN) HIGH modes, which require that the antenna switch pre-



amp ports be routed to the desired antenna, have priority over the STDN LOW and Space/Ground Link System (SGLS) ports via the logic.

The logic gates are simply a combination of dual-input nor gates driving quad-input nor gates. A typical pulser input equation from these gates is as follows.

$$(\overline{FL} + \overline{LL}) + (\overline{FH} + \overline{LR}) + (\overline{X1} + \overline{LR}) + (\overline{X2} + \overline{LL}) = 3B$$

which reduces to:

$$(FL \cdot LL) + (FH \cdot LR) + (X1 \cdot LR) + (X2 \cdot LL) = 3B$$

Therefore, driver 3B output is selected for low frequency and lower left antenna selected or high frequency and lower right antenna selected and so on for each of the other two terms of the equation.

### 7.2.5 RF Characteristics

RF isolation is 70 dB between ports and 90 dB between PM and FM sections.

Insertion loss is 0.45 dB (PM) and 0.16 dB (FM). Voltage Standing Wave Ratio (VSWR) is 1.3:1 (1750-2000 MHz) and 1.2:1 (2000 MHz - 2300 MHz).

## 7.3 SWITCH BEAM CONTROL LRU

The switch beam control LRU has redundant selectable electronics each composed of four input gates for manual/GPC, forward/aft antenna inputs, a forward/aft beam logic circuit, four pulse/driver circuits and power regulator/filter.

### 7.3.1 Input Forward/Aft GPC/Manual Beam Gates

These gates, composed of input overvoltage protected inverters and OR gates, select either the GPC/Multiplexer/Demultiplexer (MDM) input pair or the D&C panel C3 switch input pair and further select the individual antenna forward or aft inputs from the manual or GPC/MDM input selects.

Each gate output is connected to the FWD/AFT beam logic select circuit.

### 7.3.2 FWD/AFT Beam Logic

This logic circuit receives the input gate output signals and outputs the desired beam position only to the antenna selected by the antenna switch LRU.

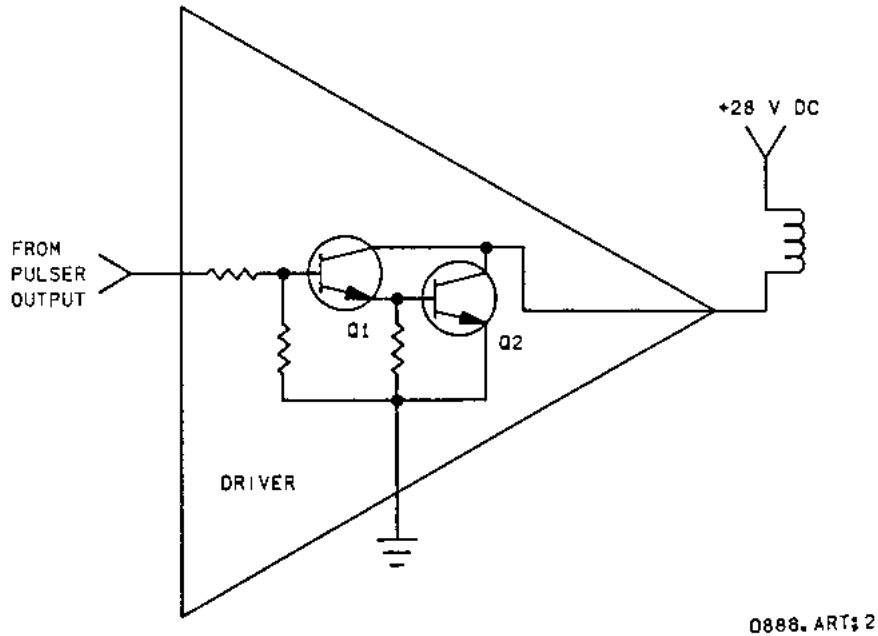
The logic consists of two OR gates and one AND gate for each output. For example the logic equation for the lower left forward beam under GPC control is:

$$LLF = (GPC \cdot F_G \cdot LL_G) + (\overline{GPC} \cdot F_G \cdot LL_G) = AI$$

Each forward/aft pair of outputs drive the pulser inputs. These pulsers and their driver outputs are the same as those in the antenna switch (ref. Section 7.2.2).

### 7.3.3 Pulse/Driver Circuits

The pulsers operate the same as those in the antenna switch LRU (ref. Section 7.2.2); each output operates a two-stage transistor driver which provides a ground to the +28-V dc powered redundant relay coils (Figure 7-5).



**Figure 7-5. Relay driver**

## 7.4 SWITCH BEAM ANTENNA FUNCTIONAL DESCRIPTION

The switch beam antenna consists of an antenna housing, mounting flange, antenna cavity, radome, two dipole antennas each with a balun, redundant driven coax switch with Telemetry (TLM) position contacts, three 3-dB hybrid couplers, one RF coax connector, and one dc signal/control connector as shown in Figure 7-6.

Figure 7-7 is the electrical schematic of the antenna.

The antennas are right-hand circularly polarized.

System parameters which affect the gain and beam directivity are as follows.

### Antenna

- Impedance match (VSWR)
- Dipole mutual coupling
- Cavity depth/size (IRIS)
- Radome material/thickness
- Mechanical tilt
- Mounting surface
- Axial ratio
- Cross polarization
- Balun spacing/loading
- Balun short position
- Dipole length
- Dipole position relative to aperature

### Stripline Hybrids

- Impedance match (VSWR)
- Coupling (~3 dB)
- Phase quadrature
- Isolation
- Termination load

### Coax Switch/RF Connectors

- Contact resistance
- Connector loss
- Coax loss

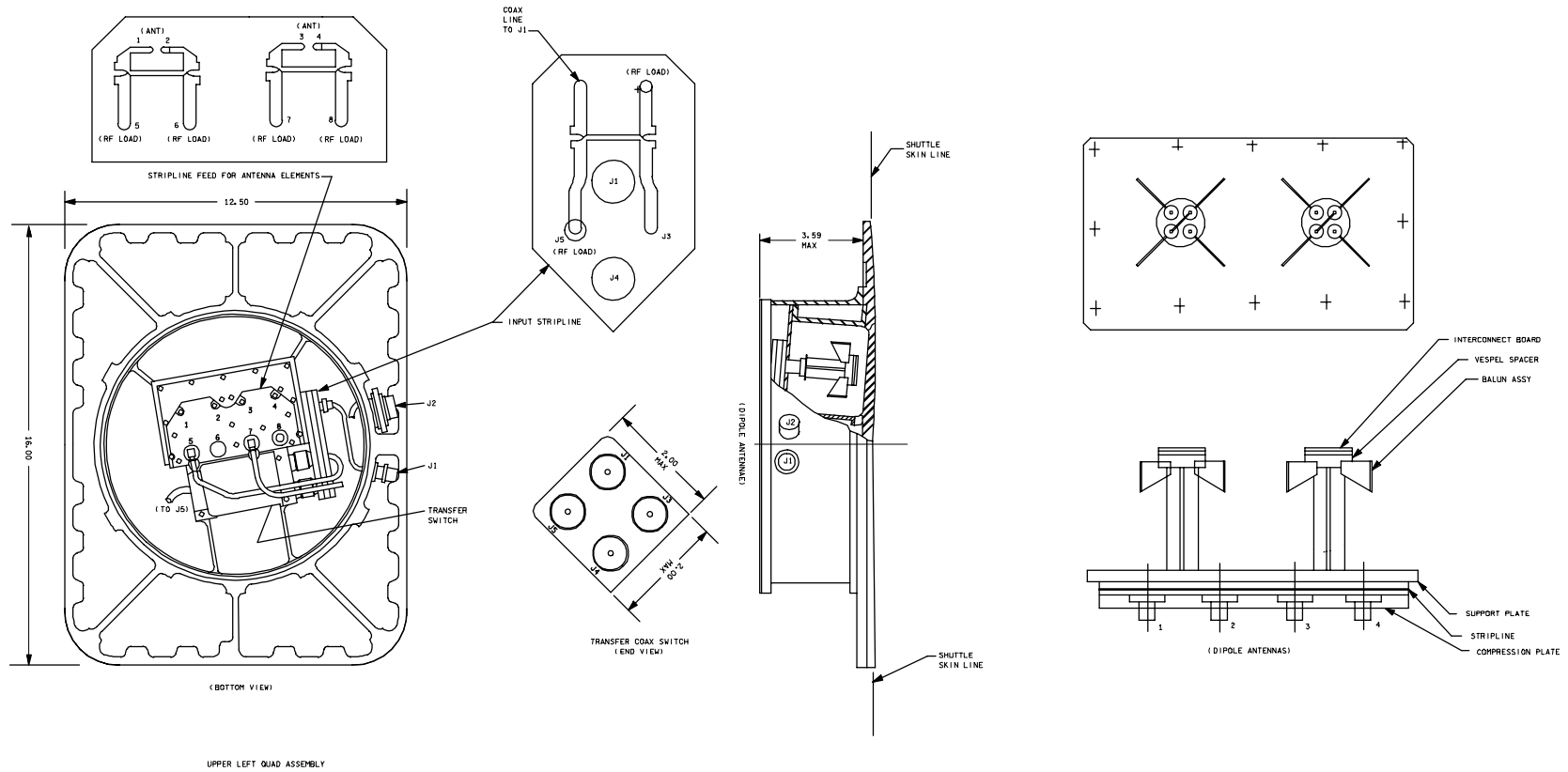
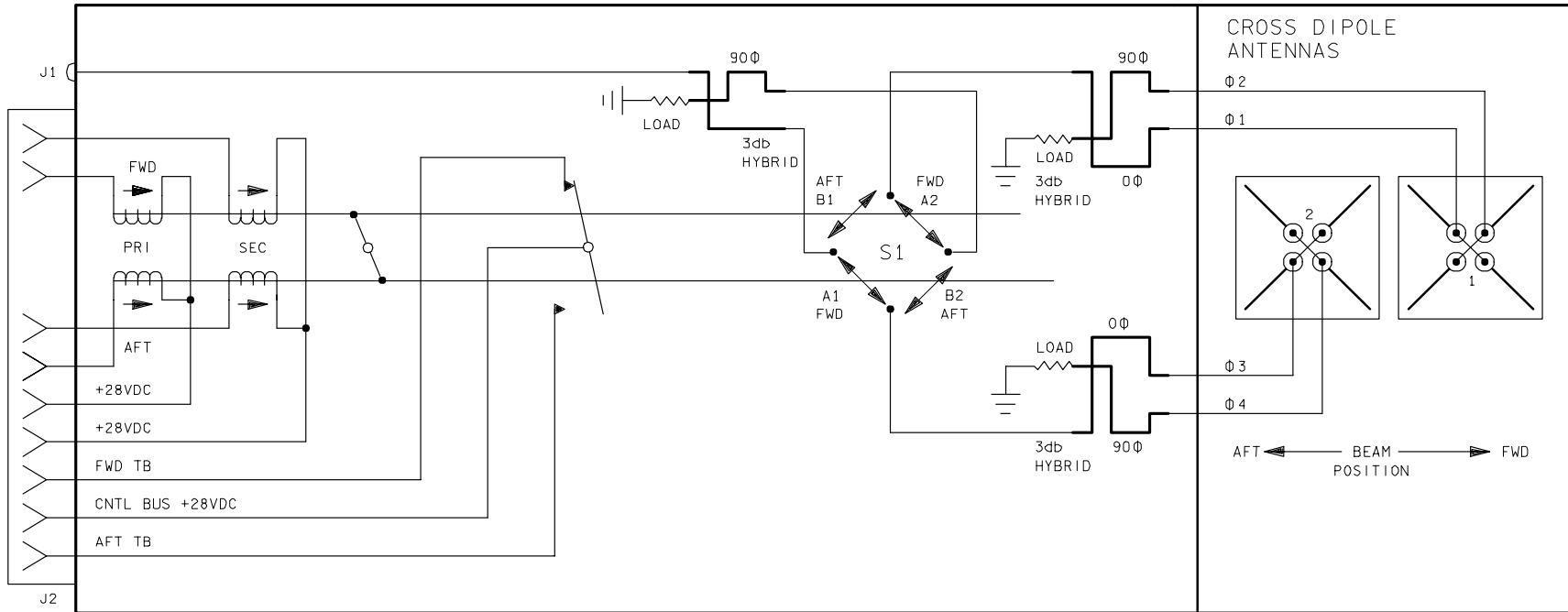


Figure 7-6. Switch beam antenna



0885. ART: 4

Figure 7-7. Switch beam antenna schematic

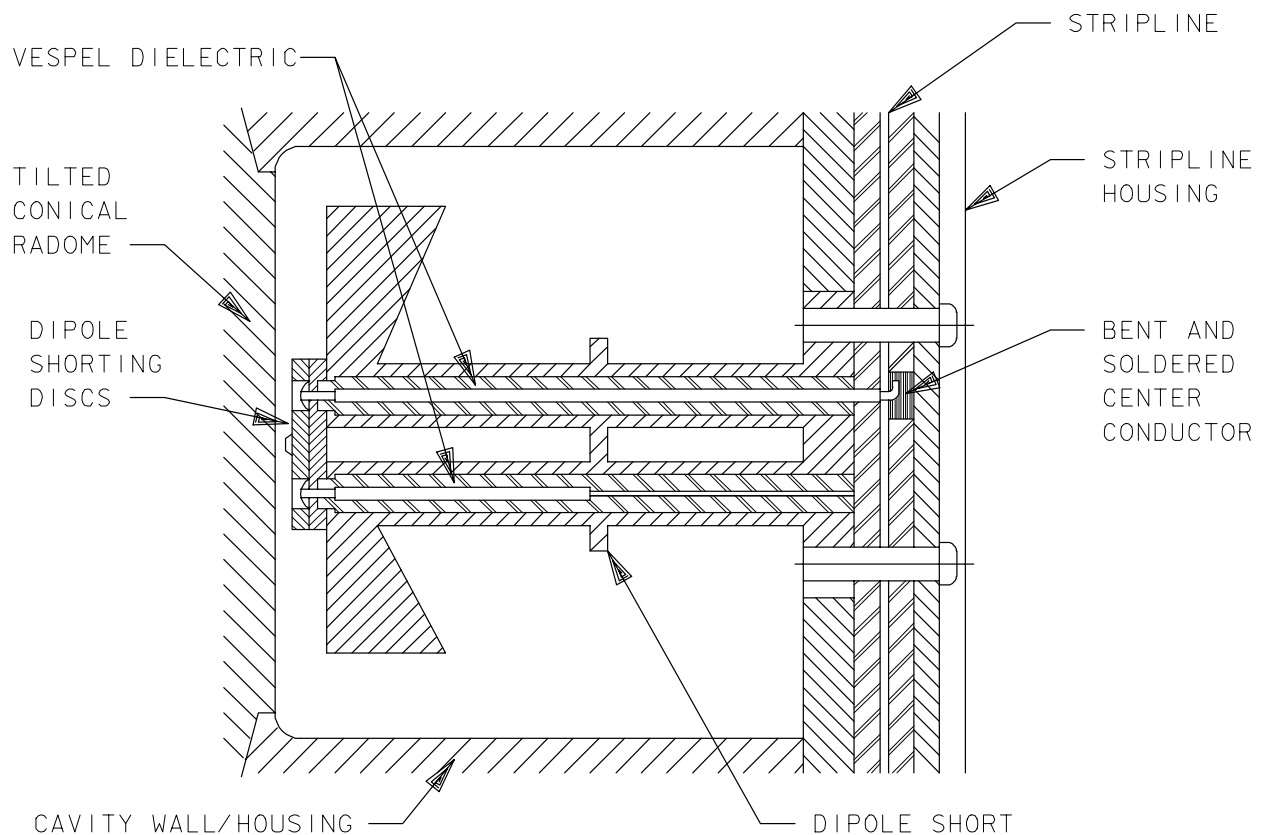
### 7.4.1 Dipole Antenna

The antenna is composed of two dipole elements, a dipole shorting disc, a balun with dipole short, and a stripline as shown in Figure 7-8, Figure 7-9 and Figure 7-10. This assembly is inserted into a can (cavity).

Two dipole antenna assemblies are used simultaneously with only the signal phase input changed to provide the forward and aft beam positions.

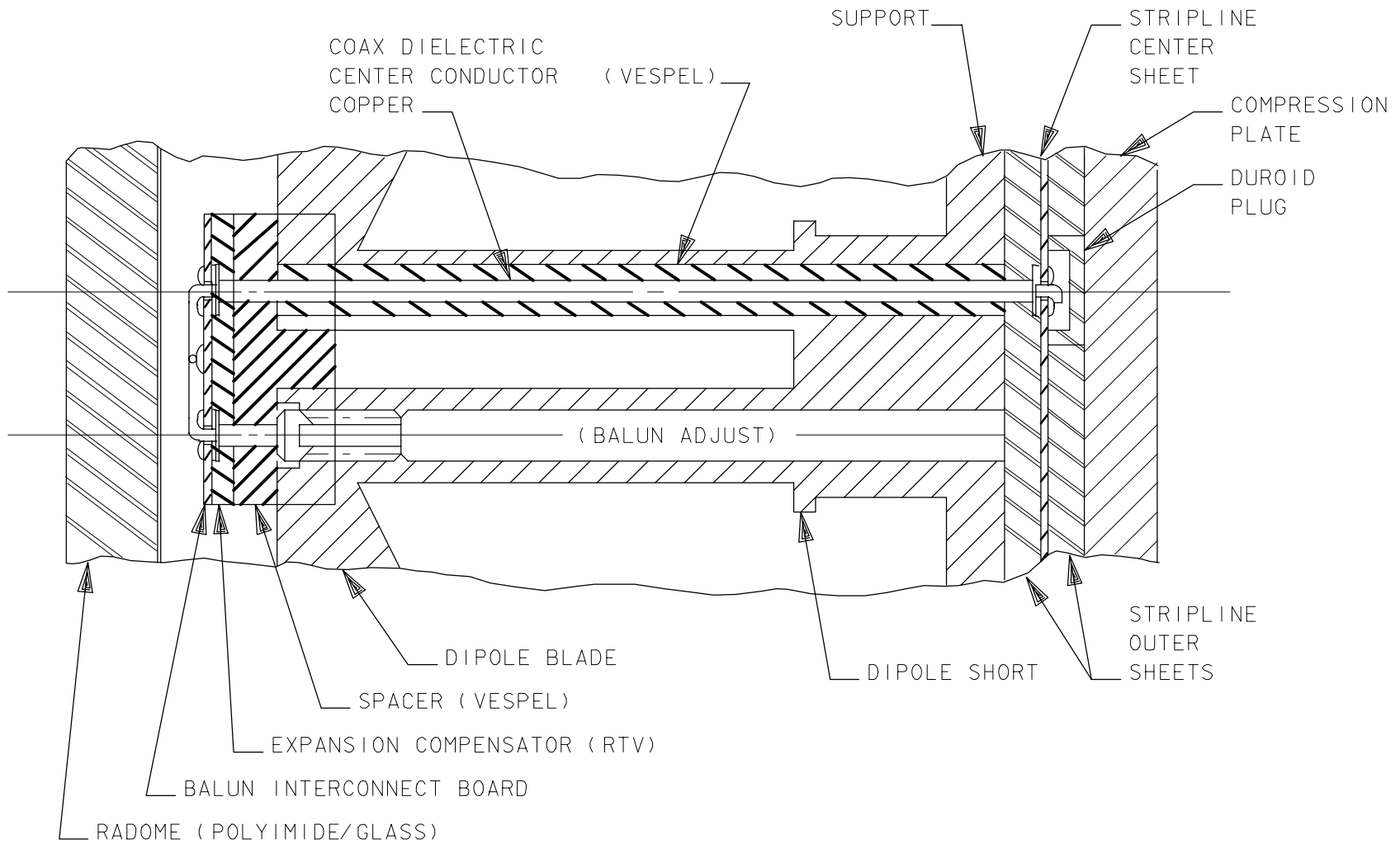
The two dipole elements are driven by a signal with one input 90° shifted from the other to provide the right-hand circular polarization.

The dipole short disc is used to connect the two branches of the balun. The balun serves as an impedance matching device over the designed operating frequency range.



0887. ART 1

**Figure 7-8. Dipole antenna**



0886. ART 3

Figure 7-9. Balun

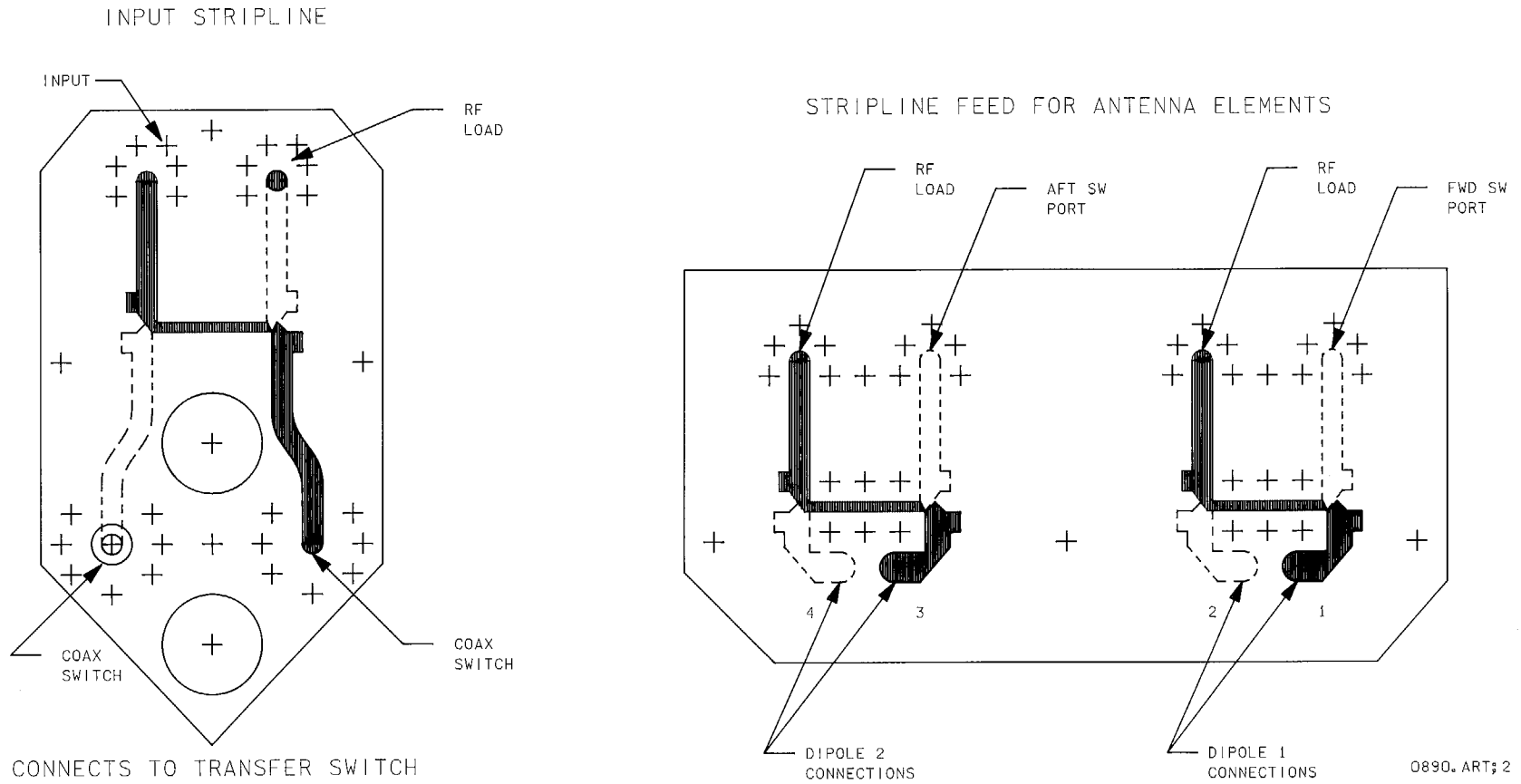


Figure 7-10. Stripline hybrids



**7.4.2 Stripline Hybrids**

The input stripline and stripline feeds for the antenna elements act as 3-dB couplers and 0- or 90-degree phase shifters to provide the two dipole antenna assemblies with the phased signal necessary to provide beam switching as shown in Table 7-3. Refer to Figure 7-7 for signal flow through hybrids and coax switch.

**Table 7-3. Stripline hybrid phase shift values**

| Dipole | Phase | Beam position |      |
|--------|-------|---------------|------|
|        |       | Aft           | Fwd  |
| 1      | Q1    | 0°            | 90°  |
| 2      | Q2    | 90°           | 180° |
|        | Q3    | 90°           | 0°   |
|        | Q4    | 180°          | 90°  |

Tuning (impedance matching) of the hybrids is accomplished by the physical shape and trace separation between the two traces. The TABS on the striplines are trimmed to provide capacitive and inductive fine tuning.

**7.4.3 Coax Switch**

The coax switch provides the switching path between the input stripline and the dipole antenna feed stripline (see Figure 7-11). It is a break-before-make switch with a switching time of less than 2.5 msec. The dc position monitor contacts provide telemetry for the coax switch position state.

**7.4.4 Quad Antenna Performance Budget**

Table 7-4 lists the typical performance budget parameters which comprise the net gain of the antenna.

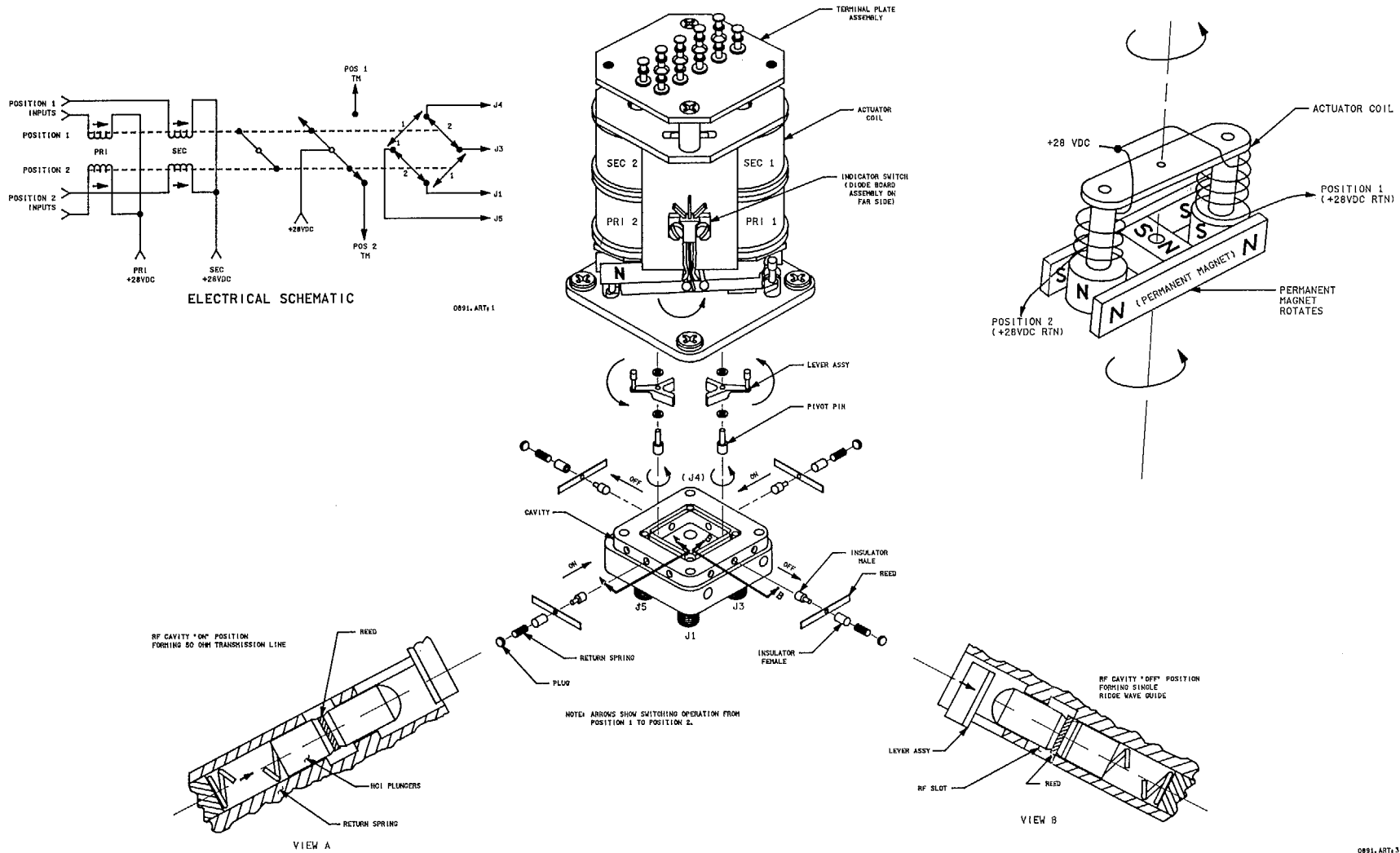


Figure 7-11. S-band switch beam antenna coax switch

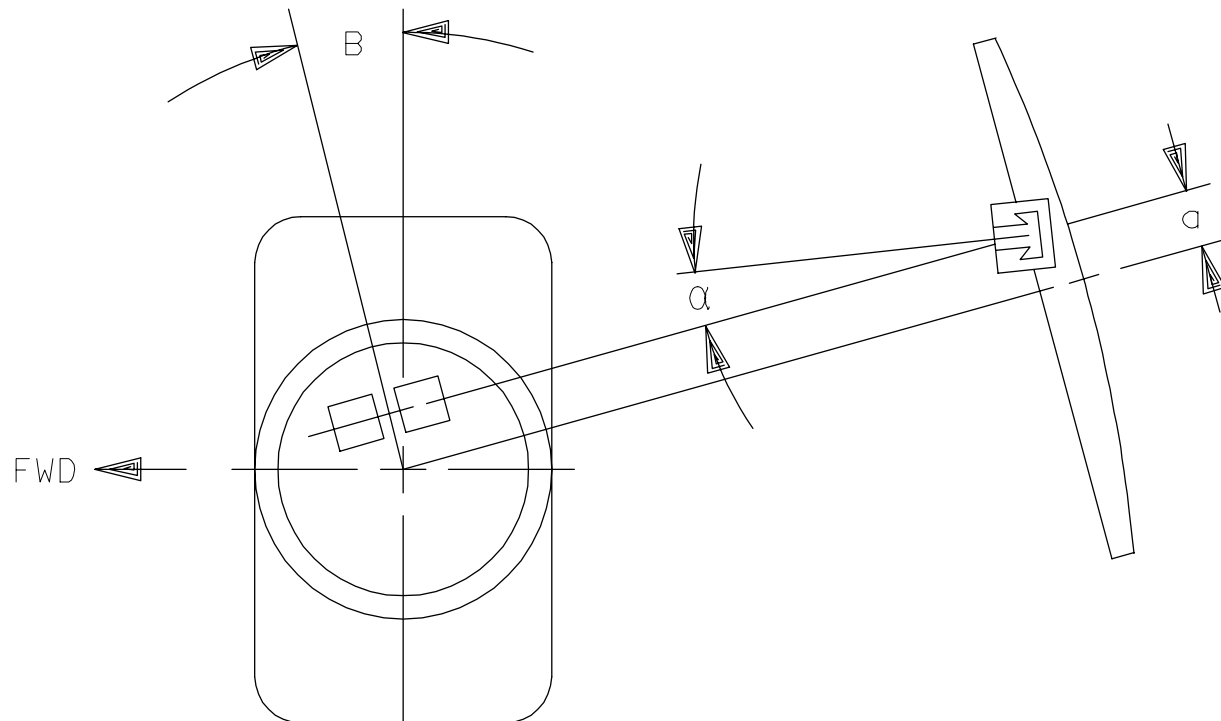
**Table 7-4. Antenna performance budget**

| Item   | Value(dB)    | Component performance  |
|--|--------------|--|
| Antenna directivity<br>(freq and ANT variations) | 7.15-8.35    | Roll > 100° (2dB) > 66° (4dB)<br>Pitch > 110 (2dB) > 83° (4dB)<br>Axial ratio ≤ 8 dB |
| Connector loss (4)                               | 0.12         |  |
| Stripline loss                                   | 0.2          |  |
| COAX loss  | 0.26         |  |
| Switch loss                                      | 0.10         |  |
| Coupler isolation                                | 0.4          | 24-30 dB   |
| Coupler VSWR                                     | 0.38         | 1.15:1.11 VSWR   |
| Dipole cavity/balum                              | 0.10         |  |
| Element VSWR                                     | 0.18         | 1.14:1.2 VSWR  |
| Radome   | 0.1          |  |
| TPS  | 0.21         |  |
| <hr/>  |              |  |
| Total losses                                     | 2.04 dB      |  |
| Net gain   | 5.11-6.31 dB |  |
| (Data derived from demonstration model)          |              |  |

#### 7.4.5 Antenna Gain Coverage

The antenna mechanical foresight is offset as shown in Figure 7-12 to compensate for the orbiter mounting surface contour and offset so that the pattern is nearly centered in the orbiter azimuth/elevation quadrant.

The individual quad antenna gain coverage varies with frequency and orbiter installation location. The four-antenna composite coverage for each frequency and the average of all four frequencies are shown in Table 7-5.



| ANTENNA   | CAVITY ORIENTATION |    |          |
|---|--------------------|----|----------|
|   | $\alpha$           | B  | a ( IN ) |
| UPPER LEFT  | 0°                 | 8° | 1.00"    |
| LOWER LEFT<br>( RIGHT SIDE ANTS ARE<br>MIRROR IMAGE ) | 2.5°               | 2° | 2.25"    |

**Figure 7-12. Antenna mechanical offset**

Figure 7-13 through Figure 7-16 show the composite gain coverage contours for the switch beam antenna system for the four S-band operating frequencies. Imposed on these contours is the individual antenna +4 decibels circular isotropic (dBci) contour to show the overlap/gap in the +4 dBci coverage. Gain is in reference to a perfect circular isotropic, radiation equally in all directions, antenna and is specified in dBci.

These contours do not contain obstruction and multipath effects. The data were taken using full-scale orbiter ground plane sections. Care should be used in using the contours for data near the nose and tail of the orbiter.

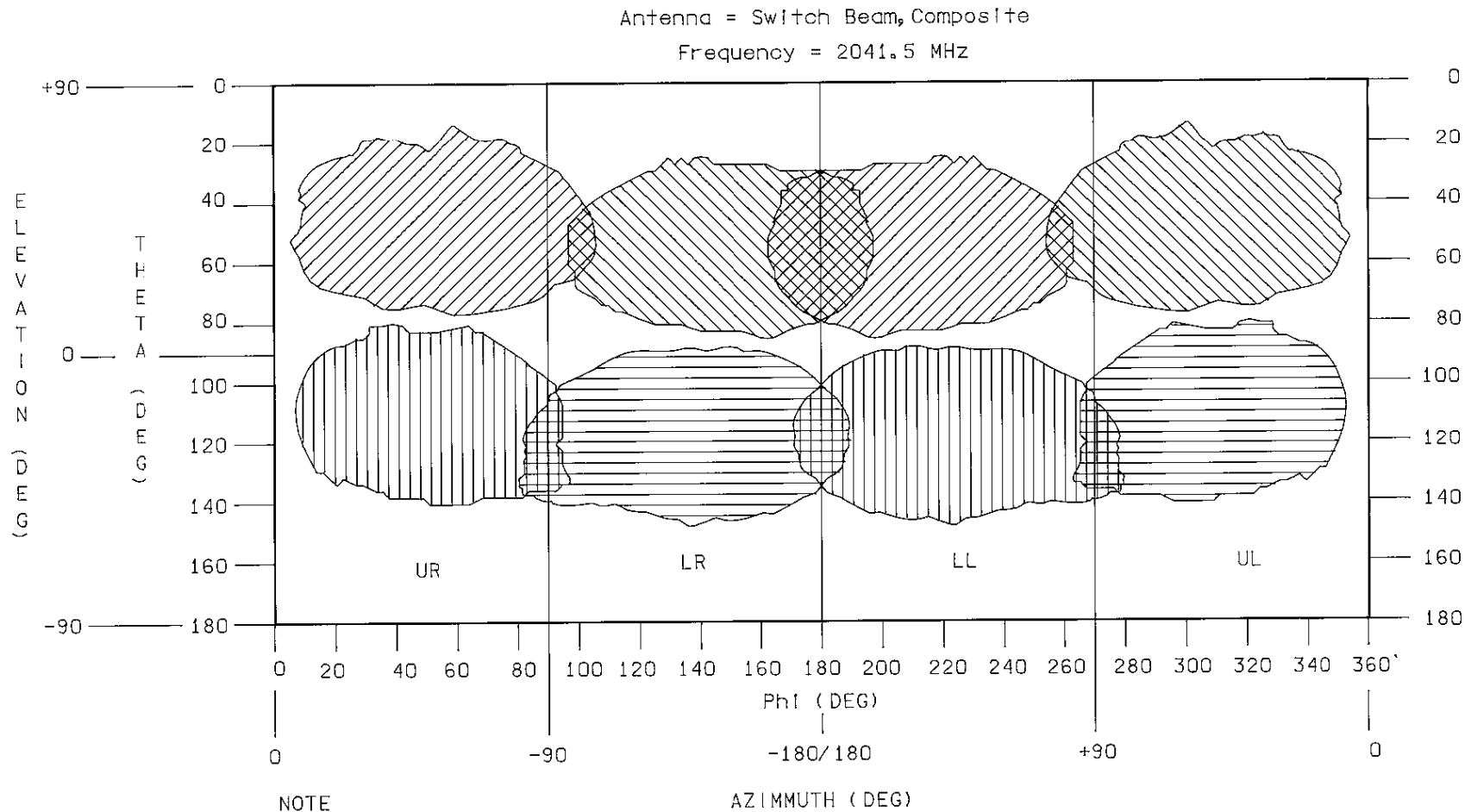
**Table 7-5. Switch beam antenna percent coverage/gain**

| Freq.<br>(Mhz) | Percent coverage    |       |                     |       |                     |       |
|----------------|---------------------|-------|---------------------|-------|---------------------|-------|
|                | +4 dBci             |       | +3 dBci             |       | +2 dBci             |       |
|                | Flight<br>(Typical) | Demo  | Flight<br>(Typical) | Demo  | Flight<br>(Typical) | Demo  |
| 2041           | 23.4                | 58.99 | 50.51               | 75.98 | 72.1                | 87.26 |
| 2106           | 42.7                | 60.26 | 65.06               | 76.68 | 78.0                | 85.80 |
| 2217           | 35.3                | 45.18 | 60.52               | 67.15 | 75.9                | 80.04 |
| 2287           | 21.6                | 43.02 | 44.66               | 64.27 | 67.3                | 76.98 |
| Average        | 30.8                | 51.9  | 55.2                | 71    | 73.3                | 82.5  |

**7.5 S-BAND ANTENNA INSTALLATION**

Figure 7-17 shows the installation of the four S-band quad antennas and the routing of the coax cables from the quads to the Xo 576 bulkhead. The two upper quad coax and two lower coax cables run through the Xo 576 bulkhead and down the bulkhead for the upper antennas and up the bulkhead for the lower antennas bulkhead to the two bay 3A cable brackets at shelf 2 and then to the S-band antenna switch.

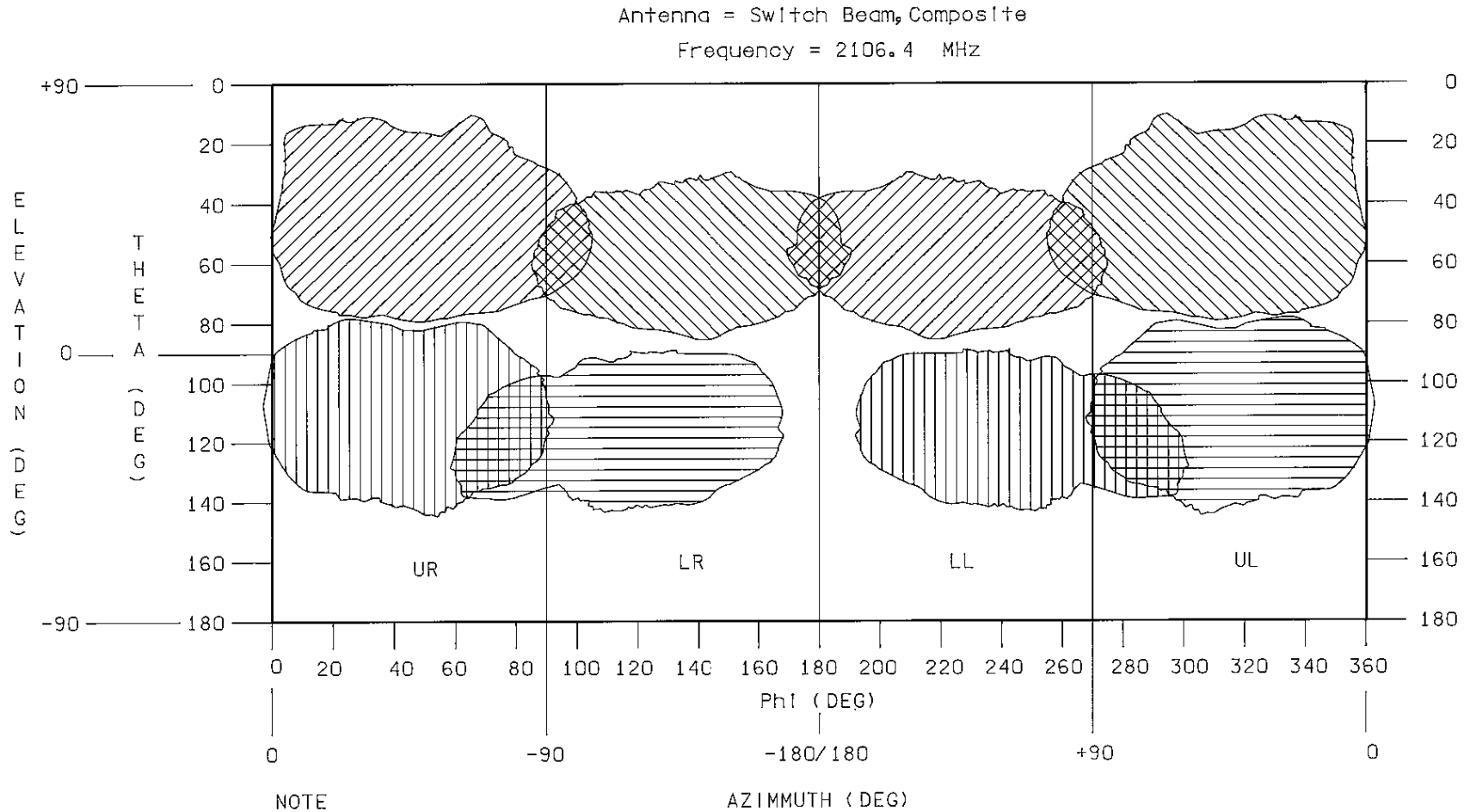
The detailed installation of the quad antennas is shown in Figure 7-18. Figure 7-19 shows the coax cables and connectors with their designation numbers.



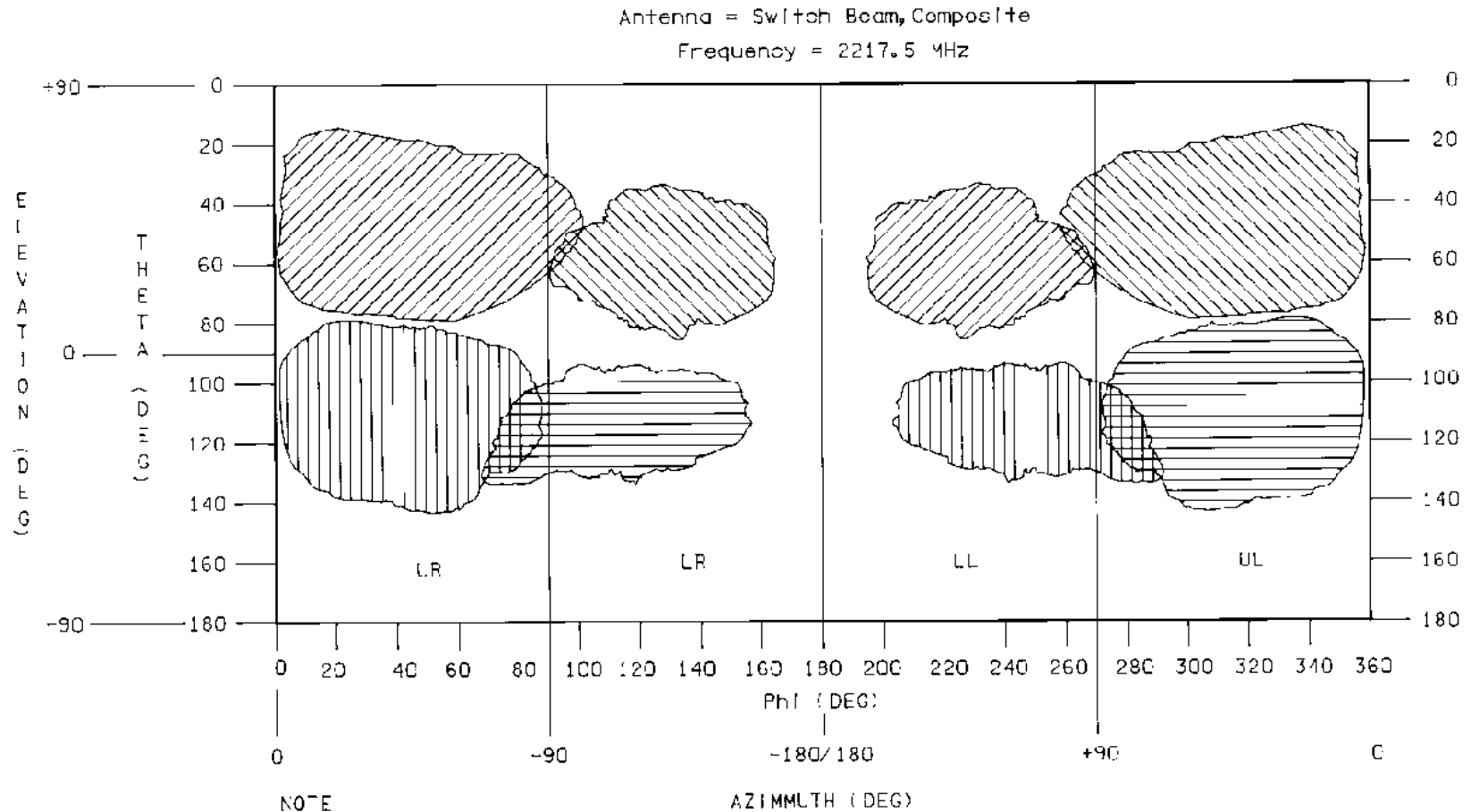
NOTE  
Shaded areas = Coverage sectors  
of greater than or equal to 4 dB gain

0893. ART; 2

**Figure 7-13. Coverage zone for 2041.5 MHz operating frequency**



**Figure 7-14. Coverage zone for 2106.4 MHz operating frequency**



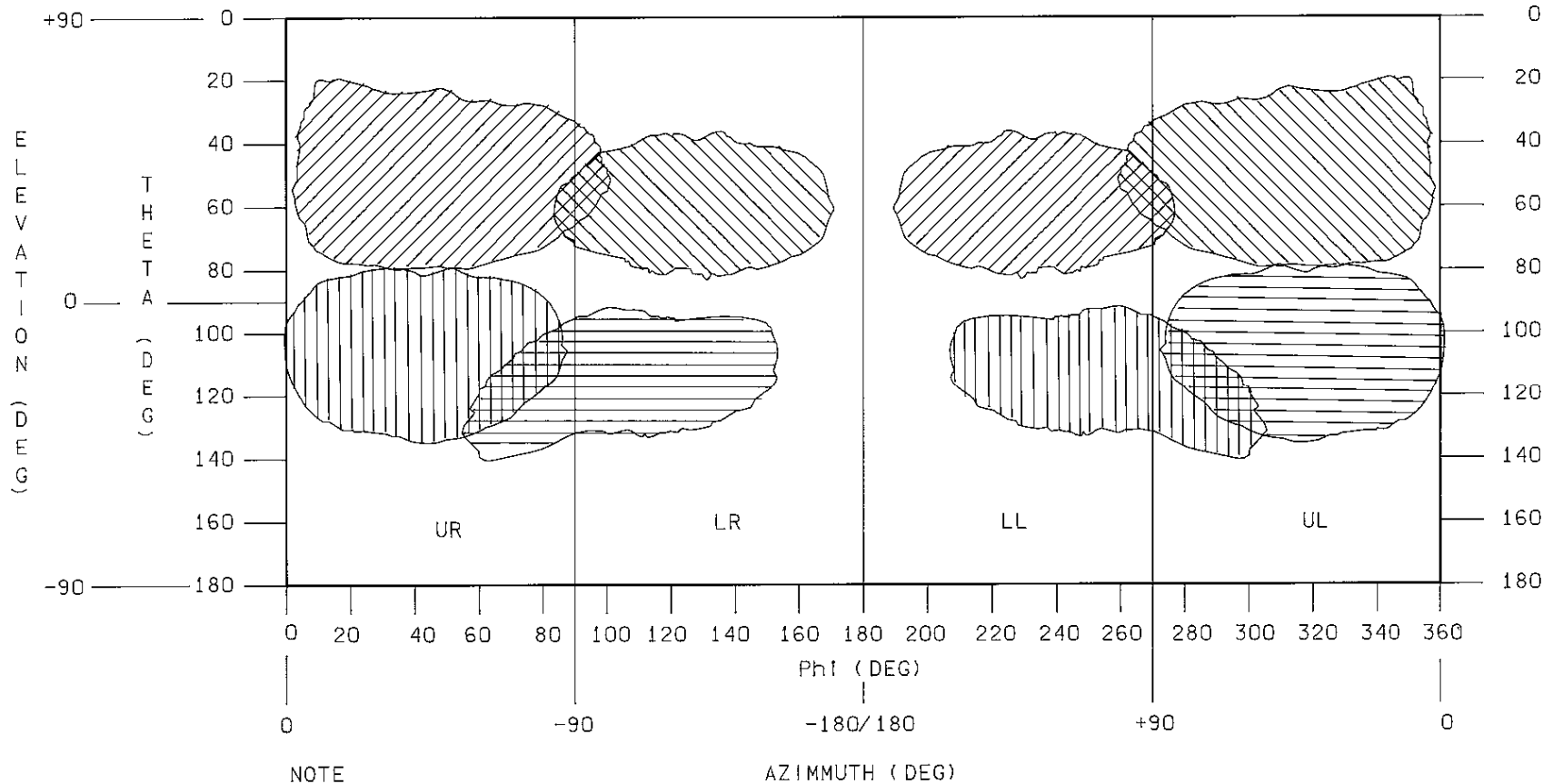
NOTE  
Shaded areas = Coverage sectors  
of greater than or equal to 4 dB gain

0893, ART: 2

**Figure 7-15. Coverage zone for 2217.5 MHz operating frequency**



Antenna = Switch Beam, Composite  
Frequency = 2287.5 MHz



NOTE  
Shaded areas = Coverage sectors  
of greater than or equal to 4 dB gain

0893. ART; 2

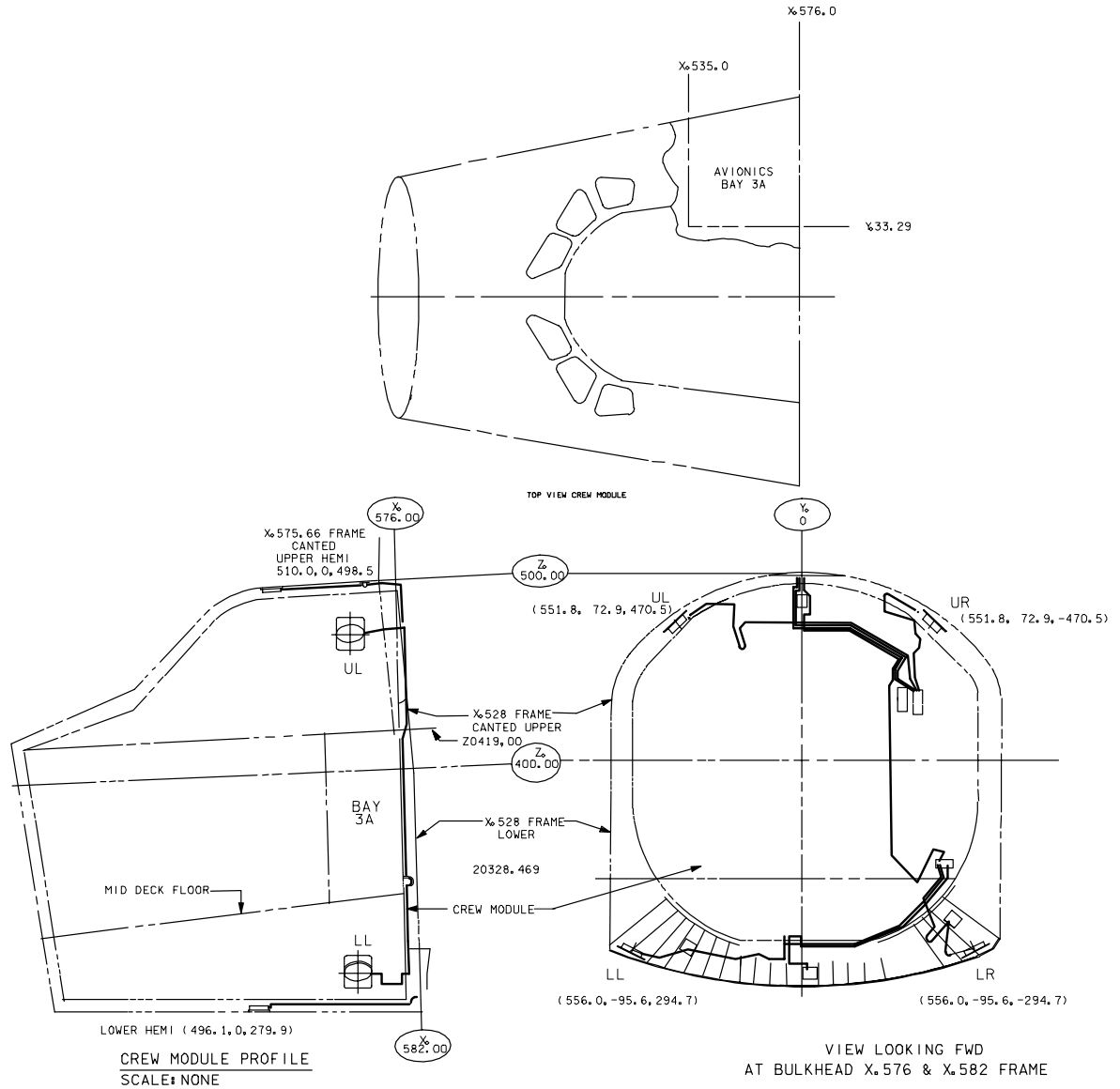
**Figure 7-16. Coverage zone for 2287.5 MHz operating frequency**

## 7.6 TELEMETRY

The following is a list of the antenna system telemetry.

|           |                               |
|-----------|-------------------------------|
| V74X4778E | S-BD ANT SW FREQ LOW          |
| V74X4779E | S-BD ANT SW FREQ HIGH         |
| V74X4782E | S-BD PM/FM ANT SW1 - ON       |
| V74X4783E | S-BD PM/FM ANT SW2 - ON       |
| V74X4780E | S-BD XPNDR 1 DIRECT           |
| V74X4781E | S-BD XPNDR 2 DIRECT           |
| V74X6491E | S-BD BEAM CNTL ASSY PWR ON 1  |
| V74X6492E | S-BD BEAM CNTL ASSY PWR ON 2  |
| V74S6503E | FM HEMI SEL - UPPER           |
| V74S6504E | FM HEMI SEL - LOWER           |
| V74S6550E | FM CONTROL COMMAND            |
| V74E6650A | FM 1 RF POWER OUT             |
| V74E6651A | FM 2 RF POWER OUT             |
| V74X6675E | FM ANT POS S5A                |
| V74X6676E | FM ANT POS S5B                |
| V74X7070E | PM QUAD ANT SEL S1A           |
| V74X7072E | PM QUAD ANT SEL S1B           |
| V74X7074E | PM QUAD ANT SEL S2A           |
| V74X7076E | PM QUAD ANT SEL S2B           |
| V74X7078E | PM QUAD ANT SEL S3A           |
| V74X7080E | PM QUAD ANT SEL S3B           |
| V74X7082E | PM QUAD ANT SEL S4A           |
| V74X7084E | PM QUAD ANT SEL S4B           |
| V74X7090E | S-BD QUAD ANT UPPER LEFT FWD  |
| V74X7091E | S-BD QUAD ANT UPPER LEFT AFT  |
| V74X7092E | S-BD QUAD ANT UPPER RIGHT FWD |
| V74X7093E | S-BD QUAD ANT UPPER RIGHT AFT |
| V74X7094E | S-BD QUAD ANT LOWER LEFT FWD  |
| V74X7095E | S-BD QUAD ANT LOWER LEFT AFT  |
| V74X7096E | S-BD QUAD ANT LOWER RIGHT FWD |
| V74X7097E | S-BD QUAD ANT LOWER RIGHT AFT |
| V74S7214E | S-BD QUAD ANT SEL 1/2-GPC     |
| V74S7215E | S-BD QUAD ANT SEL 1/2-UL FWD  |
| V74S7216E | S-BD QUAD ANT SEL 1/2-UR FWD  |
| V74S7217E | S-BD QUAD ANT SEL 1/2-LL FWD  |
| V74S7218E | S-BD QUAD ANT SEL 1/2-LR FWD  |
| V74S7315E | S-BD QUAD ANT SEL 1/2-UL AFT  |
| V74S7316E | S-BD QUAD ANT SEL 1/2-UR AFT  |
| V74S7317E | S-BD QUAD ANT SEL 1/2-LL AFT  |

A logic "1" indicates the function noted.



**Figure 7-17. S-band quad antenna installation**

## 7.7 ANTENNA SYSTEM SPECIAL COMPUTATIONS

### 7.7.1 M02I0603R S-band Switch Beam Antenna Select FWD/AFT

This special computation is a combination of M05I0200R “antenna select (PM)” computation and the TM talkbacks from the switch beam antennas (Table 7-6).

### 7.7.2 M05I0200R Antenna Select (PM) Computation

This computation is used for the fixed beam quad antennas and as a base for the switch beam antennas (Table 7-7).

**7.7.3 M02G3210R S-band Quad Selected**

This remote text output computation is driven by the GPC downlink TLM which is derived from the antenna position TLM and antenna switch TLM outputs. It is a software output.

| <u>Telemetry</u>             | Text    |
|------------------------------|---------|
| <u>V92J1057C</u>             |         |
| 001                          | UR      |
| 010                          | LR      |
| 100                          | UL      |
| 011                          | LL      |
| All other bit configurations | "BLANK" |

**7.7.4 M05I0201E, M06I0201E, M07I0201E, M08I0201E, ANT SEL (PM) UR, LR, LL and UL Computations**

These single events are based on M05I020R antenna select computation in Section 7.7.2.

|                  |                  |
|------------------|------------------|
| <u>M05I0200R</u> | <u>M05I0201E</u> |
| UR               | "1"              |
| ANY OTHER OUTPUT | "0"              |
|                  | <u>M06I0201E</u> |
| LR               | "1"              |
| ANY OTHER OUTPUT | "0"              |
|                  | <u>M07I0201E</u> |
| LL               | "1"              |
| ANY OTHER OUTPUT | "0"              |
|                  | <u>M08I0201E</u> |
| UL               | "1"              |
| ANY OTHER OUTPUT | "0"              |

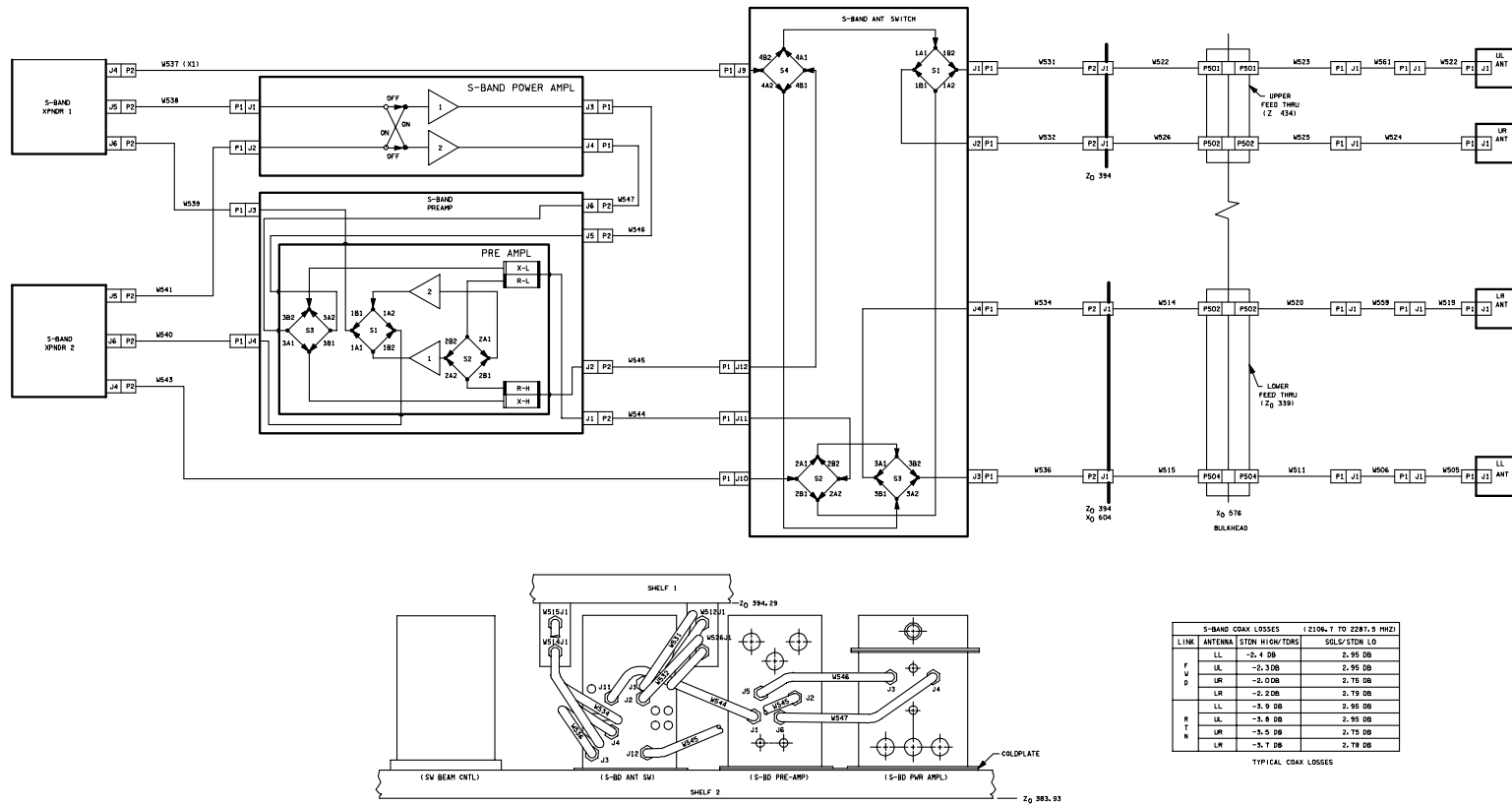


Figure 7-18. S-band antenna system coax cable schematic

0895 ANT 5

**Table 7-6. S-BD switch beam antenna computation**

| COMP/TLM No.                   |   | Output text |     |     |     |     |     |     |     |     |
|--------------------------------|---|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
| M02I0603R Remote text          |   | ULF         | ULA | URF | URA | LLF | LLA | LRF | LRA | ER1 |
| M05I0200R                      |   | UL          | UL  | UR  | UR  | LL  | LL  | LR  | LR  | ER  |
| I<br>N<br>P<br><br>U<br>T<br>S | V74X7090E<br>S-BD QUAD ULF<br>(M12I0603E) | 1           | 0   | X   | X   | X   | X   | X   | X   | X   |
|                                | V74X7091E<br>S-BD QUAD ULA<br>(M13I0603E) | 0           | 1   | X   | X   | X   | X   | X   | X   | X   |
|                                | V74X7092E<br>S-BD QUAD URF<br>(M14I0603E) | X           | X   | 1   | 0   | X   | X   | X   | X   | X   |
|                                | V74X7093E<br>S-BD QUAD URA<br>(M15I0603E) | X           | X   | 0   | 1   | X   | X   | X   | X   | X   |
|                                | V74X7094E<br>S-BD QUAD LLF<br>(M16I0603E) | X           | X   | X   | X   | 1   | 0   | X   | X   | X   |
|                                | V74X7095E<br>S-BD QUAD LLA<br>(M17I0603E) | X           | X   | X   | X   | 0   | 1   | X   | X   | X   |
|                                | V74X7096E<br>S-BD QUAD LRF<br>(M18I0603E) | X           | X   | X   | X   | X   | X   | 1   | 0   | X   |
|                                | V74X7097E<br>S-BD QUAD LRA<br>(M19I0603E) | X           | X   | X   | X   | X   | X   | 0   | 1   | X   |
|                                | All other combinations output ER2         |             |     |     |     |     |     |     |     |     |

Table 7-7. Antenna select (PM) computation

| COMP/TLM NO.               |                                  | Output text |      |      |      |  |
|----------------------------|----------------------------------|-------------|------|------|------|--|
| M05I0200R                  |                                  | UR          | LR   | LL   | UL   | EP   |
| I<br>N<br>P<br>U<br>T<br>S | V74X7070E<br>PM QUAD S1A         | 1010        | XXXX | XXXX | 0101 | ALL<br><br>O<br>T<br>H<br>E<br>R<br><br>C<br>O<br>M<br>B<br>I<br>N<br>A<br>T<br>I<br>O<br>N<br>S |
|                            | V74X7072E<br>PM QUAD S1B         | 0101        | XXXX | XXXX | 1010 |  |
|                            | V74X7074E<br>PM QUAD S2A         | X0X1        | X1X0 | X1X0 | X0X1 |  |
|                            | V74X7076E<br>PM QUAD S2B         | X1X0        | X0X1 | X0X1 | X1X0 |  |
|                            | V74X7078E<br>PM QUAD S3A         | XXXX        | 0101 | 1010 | XXXX |  |
|                            | V74X4780E<br>PM QUAD S3B         | XXXX        | 1010 | 0101 | XXXX |  |
|                            | V74X7082E<br>PM QUAD S4A         | 0X1X        | 1X0X | 1X0X | 0X1X |  |
|                            | V74X7084E<br>PM QUAD S4B         | 1X0X        | 0X1X | 0X1X | 1X0X |  |
|                            | V74X4780E<br>PM X1 DIRECT        | 1000        | 1000 | 1000 | 1000 |  |
|                            | V74X4781E<br>PM X2 DIRECT        | 0100        | 0100 | 0100 | 0100 |  |
|                            | V74X4779E<br>PM ANT SW FREQ LOW  | 0010        | 0010 | 0010 | 0010 |  |
|                            | V74X4778E<br>PM ANT SW FREQ HIGH | 0001        | 0001 | 0001 | 0001 |  |
| X = Do not care state      |                                  |             |      |      |      |  |

## 7.8 REFERENCES

- A. Installation - Crew Module, Semirigid coaxial cable, S-band, V070-743005C (OV102 and SUBS)
- B. Installation - Coaxial cables, S-band, lower equipment bay, cabin, VS70-TBD
- C. Interconnection Diagram - Coaxial cables and antenna equipment, S-band, VS70-974099
- D. Installation - Antennas and coaxial cables, S-band, V070-742005
- E. Schematic Diagram - S-band antenna switch subsystem, VS70-974099
- F. Microfilm
- G. Space Shuttle Antenna Program Review, September 13, 1979, Rockwell International.
  - First technical exchange meeting 10-28-79
  - Second technical exchange meeting 1-21-80
  - Third technical exchange meeting 3-10-80
  - Fourth technical exchange meeting 4-14-80
  - Fifth (PDR) technical exchange meeting 7-15-80
  - Seventh (PRE CDR) technical exchange meeting 1-27-81
  - Ninth technical exchange meeting 9-15-81

## 7.9 SUMMARY DATA

Figure 7-19 provides a RF path diagram from/to each XPNDR to each quad antenna. Each rectangle represents the four paths through each coax switch. Each path is given a number derived as follows:

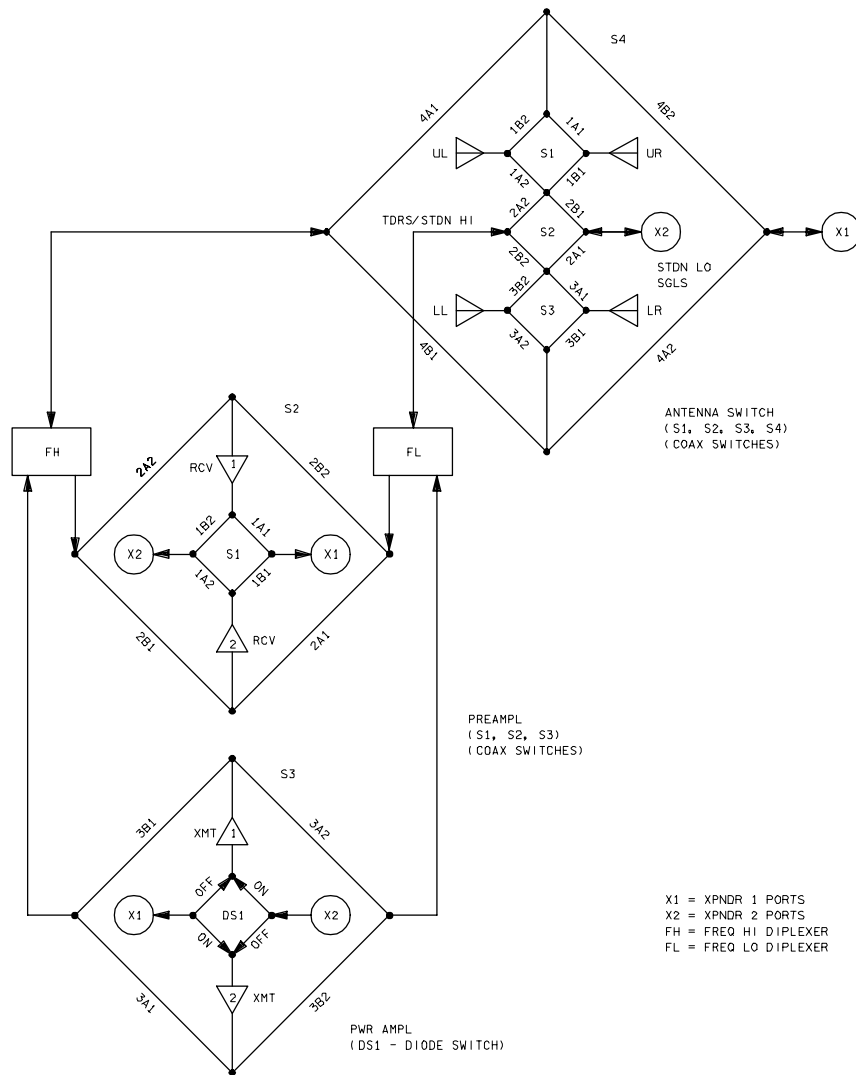
(SW no.) (A or B pair) (No. in pair)

The antenna switch has four coax switches and the preamp, three. The power ampl has one diode switch.

## 7.10 OPERATIONAL NOTES

(None)





ANTENNA SWITCH PATH MATRIX

| RF PORT                       | QUAD ANTENNA |            |            |            |
|-------------------------------|--------------|------------|------------|------------|
|                               | UL           | UR         | LR         | LL         |
| XPNDR 1 DIRECT (SGLS/STDN LO) | 4B2<br>1B2   | 4B2<br>1A1 | 4A2<br>3B1 | 4A2<br>3A2 |
| XPNDR 2 DIRECT (SGLS/STDN LO) | 2B1<br>1A2   | 2B1<br>1B1 | 2A1<br>3A1 | 2A1<br>3B2 |
| FREQ LOW (TDRS/STDN HI)       | 2A2<br>1A2   | 2A2<br>1B1 | 2B2<br>3A1 | 2B2<br>3B2 |
| FREQ HIGH (TDRS/STDN HI)      | 4A1<br>1B2   | 4A1<br>1A1 | 4B1<br>3B1 | 4B1<br>3A2 |

PATH TELEMETRY

V74X4778E S-BD ANT SW FREQ LOW  
V74X4779E S-BD ANT SW FREQ HIGH  
V74X4782E S-BD PM/FM ANT SW1-ON  
V74X4783E S-BD PM/FM ANT SW2-ON  
V74X4780E S-BD XPNDR 1 DIRECT  
V74X4781E S-BD XPNDR 2 DIRECT  
V74X6491E S-BD BEAM CNTL ASSY PWR ON 1  
V74X6492E S-BD BEAM CNTL ASSY PWR ON 2  
V74X7070E PM QUAD ANT SEL S1A  
V74X7072E PM QUAD ANT SEL S1B  
V74X7074E PM QUAD ANT SEL S2A  
V74X7076E PM QUAD ANT SEL S2B  
V74X7078E PM QUAD ANT SEL S3A  
V74X7080E PM QUAD ANT SEL S3B  
V74X7082E PM QUAD ANT SEL S4A  
V74X7084E PM QUAD ANT SEL S4B  
V74X7090E S-BD QUAD ANT UPPER LEFT FWD  
V74X7091E S-BD QUAD ANT UPPER LEFT AFT  
V74X7092E S-BD QUAD ANT UPPER RIGHT FWD  
V74X7093E S-BD QUAD ANT UPPER RIGHT AFT  
V74X7094E S-BD QUAD ANT LOWER LEFT FWD  
V74X7095E S-BD QUAD ANT LOWER LEFT AFT  
V74X7096E S-BD QUAD ANT LOWER RIGHT FWD  
V74X7097E S-BD QUAD ANT LOWER RIGHT AFT  
V74S7214E S-BD QUAD ANT SEL 1/2-GPC  
V74X7215E S-BD QUAD ANT SEL 1/2-UL FWD  
V74S7216E S-BD QUAD ANT SEL 1/2-UR FWD  
V74S7217E S-BD QUAD ANT SEL 1/2-LL FWD  
V74S7218E S-BD QUAD ANT SEL 1/2-LR FWD  
V74S7315E S-BD QUAD ANT SEL 1/2-UL AFT  
V74S7316E S-BD QUAD ANT SEL 1/2-UR AFT  
V74S7317E S-BD QUAD ANT SEL 1/2-LL AFT  
V74X4776E PREAMP 1 ON  
V74X4777E PREAMP 2 ON  
V74X4792E XPNDR/PREAMP FREQ LOW  
V74X4793E XPNDR/PREAMP FREQ HIGH  
V74X4784E POWER AMPL 1 ON  
V74X4785E POWER AMPL 2 ON  
V74X4789E S-BD PM XPNDR-SGLS  
V74X4788E S-BD PM XPNDR-STDN HI  
V74X4787E S-BD PM XPNDR-STDN LOW  
V74X4786E S-BD PM XPNDR-TDRS

A LOGIC '1' INDICATES THE FUNCTION NOTED

PREAMPLIFIER COAX SWITCH PATH MATRIX

| COAX SW PATH | PREAMP MODE                        |
|--------------|------------------------------------|
| 1A1<br>1B1   | XPNDR 1 PRE 1<br>XPNDR 1 PRE 2     |
| 1B2<br>1A2   | XPNDR 2 PRE 1<br>XPNDR 2 PRE 2     |
| 2A2<br>2B1   | PRE 1 FREQ HIGH<br>PRE 2 FREQ HIGH |
| 2B2<br>2A1   | PRE 1 FREQ LOW<br>PRE 2 FREQ LOW   |
| 3A1<br>3A2   | PA1 HIGH<br>PA2 LOW                |
| 3B2<br>3B1   | PA1 HIGH<br>PA2 LOW                |

X1 = XPNDR 1 PORTS  
X2 = XPNDR 2 PORTS  
FH = FREQ HI DIPLEXER  
FL = FREQ LO DIPLEXER

Figure 7-19. S-band antenna system path diagram

**SECTION 8 - S-BAND FREQUENCY MODULATION SYSTEM**  
**CONTENTS**

| <b>Section</b> |  | <b>Page</b> |
|----------------|--|-------------|
| 8.1            | S-band Wideband Frequency Modulation System..... | 8-1         |
| 8.1.1          | System Controls .....                            | 8-1         |
| 8.1.2          | Commands .....                                   | 8-4         |
| 8.1.3          | Telemetry.....                                   | 8-8         |
| 8.1.4          | Power .....                                      | 8-9         |
| 8.1.5          | Location/Cooling.....                            | 8-9         |
| 8.1.6          | Operation.....                                   | 8-9         |
| 8.2            | References .....                                 | 8-10        |
| 8.2.1          | Narrative .....                                  | 8-10        |
| 8.2.2          | Drawings.....                                    | 8-10        |
| 8.3            | FM System Flight Anomalies .....                 | 8-10        |

**TABLES**

| <b>Table</b> |  |     |
|--------------|--|-----|
| 8-1          | Input/output signal characteristics..... | 8-5 |
| 8-2          | MDM commands.....                        | 8-7 |

**FIGURES**

| <b>Figure</b> |   |     |
|---------------|---|-----|
| 8-1           | S-band FM system block diagram .....                | 8-2 |
| 8-2           | Panel A1 display and control S-band FM system ..... | 8-3 |

**THIS PAGE INTENTIONALLY BLANK**

## SECTION 8 S-BAND FREQUENCY MODULATION SYSTEM

### 8.1 S-BAND WIDEBAND FREQUENCY MODULATION SYSTEM

The S-band wideband Frequency Modulation (FM) system consists of redundant signal processor/transmitter combinations located in avionics bay 3A. TV, real-time payload or main engine data, or recorder dump data are downlinked to the Ground Spacecraft Tracking and Data Network (GSTDN) or Space Ground Link System (SGLS) on the 2250-MHz FM carrier. The solid state system 15-W output is selected via the FM transfer switch and routed to either the upper or lower hemi-antenna through the S-band antenna switch assembly. Figure 8-1 is a block diagram of the S-band FM system, showing internal and external interfaces.

#### 8.1.1 System Controls

(Refer to SSSH drawing 16.8.) All controls for the wideband FM system are located on panel A1, with the exception of the S-Band Phase Modulation (PM) control (command/panel) which controls the ANTENNA SWITCH ELECTRONICS switch and is located on panel C3. These switches are as follows:

##### A. S-Band FM - Panel A1 (Figure 8-2)

##### 1. CONTROL

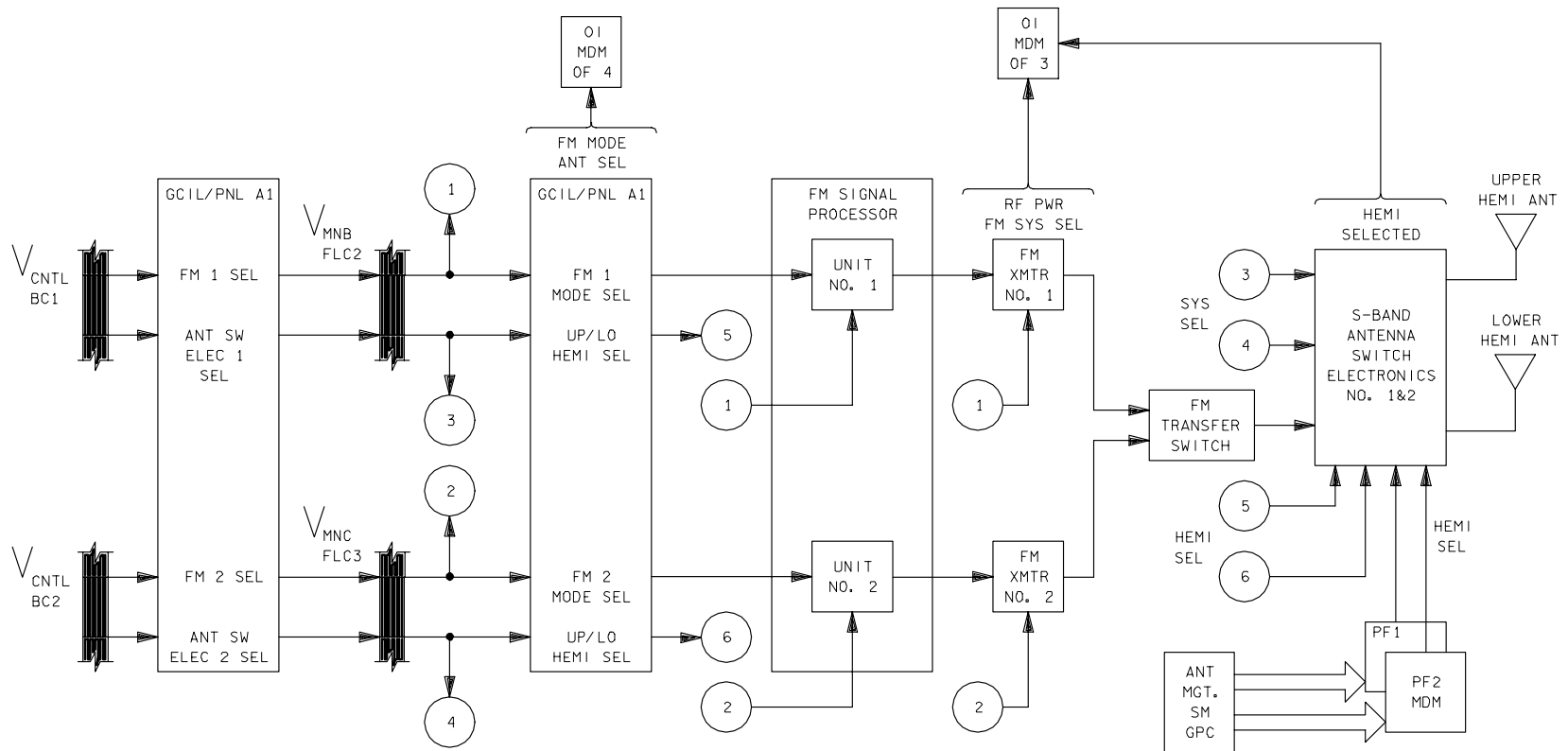
COMMAND/PANEL - Gives control of the system to either the ground/crew

##### 2. POWER

1/OFF/2 - Provides 28 V dc power to system 1/2 FM signal processor and FM transmitter or removes power from both systems

##### 3. ANT

XMTR UPPER-RCVR LOWER/GPC/XMTR LOWER-RCVR UPPER - Selects either upper/lower hemi-antenna or the General Purpose Computer (GPC) and lets the computer select either antenna



186111101. ART, 2

Figure 8-1. S-band FM system block diagram



**Figure 8-2. Panel A1 display and control S-band FM system**

4. DATA SOURCE (Table 8-1)

Rotary - Selects the source of modulation for the FM downlink

TV - TV from the video switching unit

PL ANLG - Analog data or mini-cam entry video from the payload distribution panel

PL DIGITAL - Digital data from the payload distribution panel

MMU 1 - Dump data from the Solid State Recorder #1

ME - Main engine data from the three Engine Interface Units (EIUs), and the 1024-kHz clock from the Master Timing Unit (MTU)

OFF - No modulation selected, transmit carrier only

MMU 2 - Dump data from the Solid State Recorder #2

DOD - Digital Department of Defense (DOD) data from the payload distribution panel

B. S-Band PM - Panel A1

ANT SW ELEC

1/OFF/2 - Provides 28 V dc power to electronics 1/2 to change antennas (both PM and FM). In OFF, the FM output remains connected to the last antenna selected, no matter what position the S-BAND FM ANT panel switch is in.

The S-band PM CONTROL - COMMAND/PANEL switch on panel C3 disables the ANT SW ELEC switch in COMMAND and enables it in the PANEL position.

All switch functions are commandable from the ground, except the CONTROL switches. Four commands are used for ground checkout only, and they are not commandable in flight. They can turn off either transmitter and select either signal processor output to the T-0 umbilical.

### **8.1.2 Commands**

Ground Control Interface Logic (GCIL) commands duplicate the communication mode functions of the crew controls. Table 8-2 is a listing of the commands (GCIL and PF MDM) available to the ground controller.

When the S-band FM ANT switch on panel A1 is in the GPC position, the Systems Management (SM) General Purpose Computer (GPC) (using the antenna management software) will select the hemi-antenna via Payload Forward 1 (PF1)/PF2 Multiplexer/ Demultiplexer (MDM) to the antenna switch electronics 1/2. The associated MDM discrete output "high" card/channel is card 2/channel 1 for either MDM.

*Table 8-1. Input/output signal characteristics*

| <u>FM Signal Processor</u> |  |                          |
|----------------------------|--|--------------------------|
| Input voltage              | 28 + 4 V dc  |                          |
| Input power                | 6.0 W (max) at 28 V dc                               |                          |
| Channel characteristics    | Input  | Output                   |
| <u>Television</u>          |  |                          |
| Impedance                  | 75 ohms  | 75 ohms                  |
| Bandwidth                  | 4.5 MHz  | 4.5 MHz                  |
| Signal level               | 0 to 1 V peak<br>(sync tip to white reference level) | 9.0 V p-p                |
| Signal bias                | sync tip at<br>0 V dc                                | sync tip at<br>-4.5 V dc |
| Coupling method            | ac differential                                      | Single ended             |
| Polarity                   | Positive going black to white                        |                          |
| <u>MMU (1 or 2)</u>        |  |                          |
| Impedance                  | 75 ohms  | 75 ohms                  |
| Signal format              | Biphase-L  |                          |
| Data rate                  | 25 kbps - 2048 kbps                                  |                          |
| <u>DOD</u>                 |  |                          |
| Impedance                  | 75 ohms  | 75 ohms                  |
| Signal format              | Manchester II, Biphase-L or NRZ-L                    |                          |
| Data rate                  | 250 bps to 256 Kbps                                  |                          |
| Signal level               | 1 + 0.5 V dc   | 1.27 V p-p               |
| Coupling method            | Balanced differential                                | Single ended             |



*Table 8-1. Input/output signal characteristics (concluded)*

| Channel characteristics          | Input  | Output                             |
|----------------------------------|--|------------------------------------|
| <u>P/L digital</u>               |  |                                    |
| Impedance                        | 75 ohms  | 75 ohms                            |
| Signal format                    | Manchester II  | Manchester II                      |
|                                  | Biphase-L or NRZ-L   | Biphase-L                          |
| Data rate                        | (Biphase-L) 200 bps to 2 Mbps<br>(NRZ-L) 200 bps to 5 Mbps | 200 bps to 5 Mbps                  |
| Signal level                     | 5 + 0.5 V dc   | 4 V p-p                            |
| Coupling method                  | Balanced differential                                      | Single ended                       |
| <u>P/L analog</u>                |  |                                    |
| Impedance                        | 75 ohms  | 75 ohms                            |
| Type data                        |  | Analog                             |
| Bandwidth                        |  | dc to 4 MHz                        |
| Signal level                     | 1 V p-p  | 4 V p-p                            |
| Coupling method                  | Balanced differential                                      | Single ended                       |
| <u>Main engine (3 channels)</u>  |  |                                    |
| Impedance                        | 75 ohms  | 75 ohms                            |
| Signal format                    | Manchester II<br>Biphase-L                                 | Frequency Division<br>Multiplexed  |
| Subcarrier frequencies           |  | 576, 768, and 1,024 kHz            |
| Subcarrier modulation            |  | Phase Shift Keyed                  |
| Data rate                        | 60 kbps  | Composite of summed<br>subcarriers |
| Signal level<br>(for each input) | 5 to 9 V p-p   | 1.27 V p-p for each<br>subcarrier  |
| Coupling method                  | Balanced differential                                      | Single ended                       |
| <u>FM transmitter</u>            |  |                                    |
| Input voltage                    | 28 ± 4 V dc  |                                    |
| Input power (dc)                 | 80 W (nominal)   |                                    |
| Input impedance                  | 75 ohms  |                                    |
| Output power (rf)                | 15 W (nominal)   |                                    |
| Output impedance                 | 50 ohms  |                                    |
| Output frequency                 | 2250 MHz   |                                    |

**Table 8-2. MDM commands**

| DSM  | OPS nomenclature     | MDM        | Reset                | Set                  |
|------|----------------------|------------|----------------------|----------------------|
| 4709 | S-BD ANT ELEC SW -1  | PF1<br>PF2 | 710901FF<br>710A01FF | 7909001F<br>790A001F |
| 4710 | ANT ELEC SW - OFF    | PF1<br>PF2 | 710901FF<br>710A01FF | 7909002A<br>790A002A |
| 4711 | S-BD ANT ELEC SW - 2 | PF1<br>PF2 | 710901FF<br>710A01FF | 7909001E<br>790A001E |
| 4712 | S-BD HEMI SEL 1 - UP | PF1        | 2089C000             | 28894000             |
| 4713 | S-BD HEMI SEL 1 - LO | PF1        | 2089C000             | 28898000             |
| 4714 | S-BD HEMI SEL 2 - UP | PF2        | 208AC000             | 288A4000             |
| 4715 | S-BD HEMI SEL 2 - LO | PF2        | 208AC000             | 288A8000             |
| 4727 | FM - MMU2            | PF1<br>PF2 | 710901FF<br>710A01FF | 79090069<br>790A0069 |
| 4728 | FM - MMU 1           | PF1<br>PF2 | 710901FF<br>710A01FF | 7909006B<br>790A006B |
| 4780 | FM SYSTEM 1 - ON     | PF1<br>PF2 | 710901FF<br>710A01FF | 79090065<br>790A0065 |
| 4781 | FM SYSTEM 1/2 - OFF  | PF1<br>PF2 | 710901FF<br>710A01FF | 79090066<br>790A0066 |
| 4782 | FM SYSTEM 2 - ON     | PF1<br>PF2 | 710901FF<br>710A01FF | 79090067<br>790A0067 |
| 4783 | FM - OFF             | PF1<br>PF2 | 710901FF<br>710A01FF | 79090068<br>790A0068 |
| 4785 | FM - MAIN ENG        | PF1<br>PF2 | 710901FF<br>710A01FF | 7909006A<br>790A006A |
| 4787 | FM - PL DIGI         | PF1<br>PF2 | 710901FF<br>710A01FF | 7909006C<br>790A006C |
| 4788 | FM - PL ANLG         | PF1<br>PF2 | 710901FF<br>710A01FF | 7909006D<br>790A006D |
| 4789 | FM -DOD              | PF1<br>PF2 | 710901FF<br>710A01FF | 7909006E<br>790A006E |
| 4790 | FM -TV               | PF1<br>PF2 | 710901FF<br>710A01FF | 7909006F<br>790A006F |

### 8.1.3 Telemetry

There are 15 Telemetry (TLM) measurements which can be monitored on the ground, 13 events and 2 analogs.

- FM ANT SEL L (V74S6506E) - This is an event that, when high, indicates the panel switch is in the LOWER position.
- FM ANT SEL U (V74S6505E) - This is an event that, when high, indicates the panel switch is in the UPPER position.
- ANT POS S5B (V74X6676E) - This is an event that, when high, indicates the FM system output is connected to the lower hemi-antenna.
- ANT POS S5A (V74X6675E) - This is an event that, when high, indicates the FM system output is connected to the upper hemi-antenna.
- DATA MODE - TV (V74X4806E) - This is an event that, when high, indicates the TV from the video switching unit is the data source for both signal processors.
- DATA MODE - PL ANLG (V74X4804E) - This is an event that, when high, indicates analog data or mini-cam entry video from the payload distribution panel is the data source for both signal processors.
- DATA MODE - PL DIGI (V74X4803E) - This is an event that, when high, indicates digital data from the payload distribution panel are the data source for both signal processors.
- DATA MODE - MMU 1 - (V74X3447E) - This is an event that, when high, indicates the Solid State Recorder #1 is the data source for both signal processors.
- DATA MODE - Main Engine - (V74X4801E) - This is an event that, when high, indicates digital data from the EIUs and the 1024-kHz clock from the MTU are the data sources for both signal processors.
- DATA MODE - MMU 2 - (V74X3446E) - This is an event that, when high, indicates the Solid State Recorder #2 is the data source for both signal processors.
- DATA MODE - DOD - (V74X4805E) - This is an event that, when high, indicates digital DOD data from the payload distribution panel are the data source for both signal processors.
- FM SYS 1 - ON (V74X6120E) - This is an event that, when high, indicates 28 V dc power is applied to FM transmitter 1.
- FM SYS 2 - ON (V74X6121E) - This is an event that, when high, indicates 28 V dc power is applied to FM transmitter 2.

- FM RF OUTPUT 1 (V74E6650A) - This is an analog measurement of the transmitter 1 Radio Frequency (RF) power output. The range of measured power is from 0 to 20 W. Nominal power output is about 15 W.
- FM RF OUTPUT 2 (V74E6651A) - This is an analog measurement of the transmitter 2 RF power output. The range of measured power is from 0 to 20 W. Nominal power output is about 15 W.

#### 8.1.4 Power

Twenty-eight V dc power is provided to the FM signal processor, FM transmitter, and the antenna switch electronics from the forward load control assemblies. The GCIL unit panel or command drivers use 28 V dc control bus power to turn the load control assembly 28 V dc output to the Line Replaceable Unit (LRU) on or off.

#### 8.1.5 Location/Cooling

The FM system equipment is located in the forward avionics equipment bay 3A. These LRUs are cooled as follows:

- |  |                          |
|--|--------------------------|
| • FM signal processor (dual-systems 1 and 2) | Air cooled               |
| • FM transmitter 1                           | Water cooled (coldplate) |
| • FM transmitter 2                           | Water cooled (coldplate) |
| • S-band FM 1/2 transfer switch              | Air cooled               |
| • S-band antenna switch assembly             | Air cooled               |

#### 8.1.6 Operation

(Refer to SSSH drawing 16.8.) When system 1 or 2 is selected, power is applied to both the signal processor and its associated transmitter. With no data source selected as an input to the signal processor, only the power supply and output amplifier are energized. When a particular data source is selected, the proper relays are closed to provide a path through the processor, and power is applied to the proper amplifiers. There are basically three data paths through the processor:

- Analog - TV or payload analog
- Digital - recorder dumps or payload digital
- Main engine low rate digital

The nominal Input/Output (I/O) signal characteristics are shown in Table 8-1.

During ground checkout, a parallel output to the Ground Support Equipment (GSE) can be enabled through the Launch Forward (LF 1) MDM. This control path is disabled during flight.

## 8.2 REFERENCES

### 8.2.1 Narrative

FM Signal Processor Critical Design Review, April 1978

FM Transmitter Critical Design Review, November 1977

S-Band FM System Specification, Rockwell, MC 478-0106D

### 8.2.2 Drawings

#### Rockwell

VS70-740269, S-Band FM Signal Processor Schematic (OV-103 and subs)

VS70-740279, S-Band FM Transmitter Schematic (OV-103 and subs)

#### FM Signal Processor (CONRAC)

7905345, Power Supply

7905348, Logic TV, ANLG & ME Output

7905351, Main Engine Processing

7905354, Interconnection Diagram

7905360, Digital Data Processing

#### FM Transmitter (Teledyne)

SK2008736, Modulator/Exciter

SK2008748, Power Supply

SK2008750, TLM Processor

SK2008763, RF Power Amplifier

SK2008925, Interconnection Diagram

## 8.3 FM SYSTEM FLIGHT ANOMALIES

This section summarizes anomalies that have occurred on the FM system during past missions.

- A. On STS-32, the FM 1 transmitter RF power output dropped to 0 watts during powered flight. FM system 1 was down for the rest of the mission. FM system 2 and Ku-band were used for recorder dumps. Postflight, the bad part could not be verified. Suspect parts were replaced, including the exciter module. FM 1 transmitter serial number was 304.

- B. On STS-58, Bermuda noted that there were some side bands with the center frequency of 2250 MHz. The frequencies were 2228 and 2272 MHz. This indicated that the FM 1 transmitter was near total failure. FM 1 transmitter RF Power Output degraded to 6.0 watts (spec of 10 watts). On the previous flight of this LRU (OV-102, STS-55), the output power was 15.5 watts. FM 1 transmitter serial number was 304. FM 1 transmitter was removed and replaced postflight. The problem was linked to cracked solder joints in the power amplifier board that could be seen only under a 20x microscope. The cracks are believed to be caused by poor solder joints exposed to movement resulting from supporting components expanding/contracting at different rates over the lifetime of the unit (built in 1979). This was not considered a generic problem since no other units had any history of cracked solder joints.
- C. On STS-65, the FM 1 transmitter RF power output fluctuated by a couple of watts during prelaunch and on orbit. The values ranged from 17 to 13.5 watts. FM system 2 was used for recorder dumps. FM 1 transmitter serial number was 302. FM 1 transmitter was removed and replaced postflight. The most probable cause was a fractured solder joint on the power amplifier board caused by improper soldering during a previous repair.

THIS PAGE INTENTIONALLY BLANK

## SECTION 9 – KU-BAND RADAR/COMMUNICATIONS SYSTEM

### CONTENTS

| Section | Page  |      |
|---------|---|------|
| 9.1     | GENERAL .....   | 9-1  |
| 9.1.1   | Line Replacement Units Overview .....                         | 9-1  |
| 9.1.2   | Communications Mode Overview.....                             | 9-2  |
| 9.1.3   | Radar Mode Overview .....                                     | 9-2  |
| 9.1.4   | Ku-Band Activation Overview.....                              | 9-3  |
| 9.1.5   | COMM Mode Operations Overview .....                           | 9-3  |
| 9.1.6   | Communication Mode Forward Link Path Overview .....           | 9-6  |
| 9.1.7   | Communication Mode Return Link Path Overview.....             | 9-7  |
| 9.1.8   | Radar Mode Operations Overview .....                          | 9-8  |
| 9.1.9   | Radar Mode RF Pulse Transmission and Reflection Overview..... | 9-8  |
| 9.1.10  | Interfaces Overview .....                                     | 9-9  |
| 9.1.11  | Communications Mode vs. Radar Mode .....                      | 9-12 |
| 9.2     | ELECTRONICS ASSEMBLY - 1 (EA-1).....                          | 9-12 |
| 9.2.1   | Reference Oscillator.....                                     | 9-13 |
| 9.2.2   | Automatic Gain Control .....                                  | 9-13 |
| 9.2.3   | Automatic Level Control .....                                 | 9-13 |
| 9.2.4   | COSTAS Demodulator .....                                      | 9-14 |
| 9.2.5   | COSTAS LOCK Detector .....                                    | 9-15 |
| 9.2.6   | Tau-Dither Acquisition and Tracking Loop .....                | 9-15 |
| 9.2.7   | Pseudorandom Noise Lock Detector.....                         | 9-16 |
| 9.2.8   | Comm/Radar Tracking Logic.....                                | 9-16 |
| 9.2.9   | a and b Gimbal Servo Circuits.....                            | 9-16 |
| 9.3     | COMMUNICATIONS SIGNAL PROCESSOR (SPA) .....                   | 9-17 |
| 9.3.1   | Bit Synchronizer and Ambiguity Resolver .....                 | 9-18 |
| 9.3.2   | Bit Detector .....  | 9-18 |
| 9.3.3   | Frame Synchronizer .....                                      | 9-18 |
| 9.3.4   | Frame Decommulator .....                                      | 9-19 |
| 9.3.5   | Data Source Selector .....                                    | 9-19 |
| 9.3.6   | Square Wave Oscillator.....                                   | 9-23 |
| 9.3.7   | FM High Data Rate Channel .....                               | 9-23 |
| 9.3.8   | PM HDR channel .....  | 9-23 |
| 9.3.9   | Convolutional encoder .....                                   | 9-23 |
| 9.3.10  | QPSK modulator .....  | 9-24 |
| 9.3.11  | SPA Internal Microprocessor.....                              | 9-26 |
| 9.4     | RADAR SIGNAL PROCESSOR (EA-2) .....                           | 9-26 |
| 9.4.1   | Analog Processor.....   | 9-28 |
| 9.4.2   | Digital preprocessor .....                                    | 9-28 |
| 9.4.3   | Filter processor .....  | 9-29 |
| 9.4.4   | Magnitude Detector.....                                       | 9-29 |
| 9.4.5   | Postdetection Integrator .....                                | 9-29 |



| Section | Page   |
|---------|--|
| 9.4.6   | Log Converter ..... 9-29                                 |
| 9.4.7   | Target Detect ..... 9-30                                 |
| 9.4.8   | Automatic Gain Control Processor ..... 9-30              |
| 9.4.9   | Discriminant Generator ..... 9-30                        |
| 9.4.10  | Angle Processor ..... 9-30                               |
| 9.4.11  | Range Processor ..... 9-31                               |
| 9.4.12  | Velocity Processor ..... 9-31                            |
| 9.4.13  | Low Voltage Power Supply ..... 9-31                      |
| 9.5     | RADAR OPERATIONS ..... 9-32                              |
| 9.5.1   | Ku-Band RF Output Power and Acquisition Range ..... 9-36 |
| 9.5.2   | Ku-band Radiated Field ..... 9-38                        |
| 9.5.3   | Operations in Ku-Band Radar Mode with ISS ..... 9-40     |
| 9.6     | MECHANICAL CONVERSIONS ..... 9-41                        |
| 9.6.1   | Azimuth-Elevation ..... 9-41                             |
| 9.6.2   | a-b Coordinate System ..... 9-41                         |
| 9.6.3   | Coordinate Conversion Equations ..... 9-41               |
| 9.7     | DEPLOYED ELECTRONICS ASSEMBLY (DEA) ..... 9-46           |
| 9.7.1   | Deployed Electronics Assembly Overview ..... 9-46        |
| 9.7.2   | Exciter In-Depth Detail ..... 9-48                       |
| 9.7.3   | Transmitter In-Depth Detail ..... 9-50                   |
| 9.7.4   | Receiver In-Depth Detail ..... 9-54                      |
| 9.7.5   | Microwave Assembly In-Depth Detail ..... 9-56            |
| 9.7.6   | Low voltage power supply In-Depth Detail ..... 9-57      |
| 9.8     | DEPLOYED MECHANICAL ASSEMBLY (DMA) ..... 9-58            |
| 9.8.1   | Dish Antenna Electronics ..... 9-58                      |
| 9.8.2   | Rate Sensor Assembly ..... 9-60                          |
| 9.8.3   | a/b Gimbal ..... 9-60                                    |
| 9.8.4   | Rotary Joint ..... 9-60                                  |
| 9.9     | EA-1 INTERFACES ..... 9-60                               |
| 9.9.1   | EA-1 Interfaces with the SM GPC ..... 9-61               |
| 9.9.2   | Crew Interfaces with EA-1 ..... 9-76                     |
| 9.9.3   | EA-1 to SPA Interface ..... 9-90                         |
| 9.9.4   | EA-1 to EA-2 Interface ..... 9-91                        |
| 9.9.5   | EA-1 to DA Interface ..... 9-97                          |
| 9.9.6   | EA-1 to Deployed Motor Interface ..... 9-100             |
| 9.10    | SPA TO DEA INTERFACE ..... 9-103                         |
| 9.11    | DEA TO EA-2 INTERFACE ..... 9-104                        |
| 9.12    | TELEMETRY ..... 9-106                                    |
| 9.12.1  | OI telemetry description ..... 9-106                     |
| 9.12.2  | GNC, SM and OI Telemetry for RNDZ Radar ..... 9-108      |
| 9.12.3  | SM Downlist Telemetry for Ku-Band ..... 9-109            |
| 9.13    | INSTALLATION/POWER/WEIGHT ..... 9-111                    |
| 9.13.1  | Location ..... 9-111                                     |

| Section | Page  |
|---------|---|
| 9.13.2  | Power/Weight/Cooling..... 9-112                                   |
| 9.14    | KU-BAND OPERATIONS EXAMPLES ..... 9-118                           |
| 9.14.1  | Power Up Ku-Band System (Example) ..... 9-118                     |
| 9.14.2  | Enable SM SIO Channel Through MDM PF1 (Example) ..... 9-118       |
| 9.14.3  | GPC Designate Mode commanding Modulation-On (Example) ..... 9-118 |
| 9.14.4  | Command TWT Off (Example)..... 9-118                              |
| 9.14.5  | Ku RF Protection Boxes (Example)..... 9-119                       |
| 9.14.6  | Configure Ku-Band System 3 Channel Downlink (Example)..... 9-119  |
| 9.14.7  | Auto-handovers between S-band and Ku-band (Example) ..... 9-119   |
| 9.14.8  | Beta gimbal limit protection (Example)..... 9-120                 |
| 9.15    | KU-BAND POWER MALFUNCTIONS ..... 9-121                            |
| 9.16    | REFERENCES..... 9-122   |
| 9.16.1  | Narrative..... 9-122  |
| 9.16.2  | Drawings ..... 9-122  |
| 9.17    | KU-BAND OPERATIONAL NOTES/ANOMALIES ..... 9-124                   |
| 9.17.1  | Anomalies ..... 9-124   |
| 9.17.2  | Signatures ..... 9-128  |

## TABLES

| Table |  | Page  |
|-------|--|-------|
| 9-1   | Return link modulation and carrier status .....                              | 9-5   |
| 9-2   | High/low data rate channel input signal characteristics .....                | 9-20  |
| 9-3   | Internal SPA Signals .....   | 9-26  |
| 9-4   | Frequency selection .....  | 9-27  |
| 9-5   | GPC mode operating data.....   | 9-35  |
| 9-6   | Ratio of power versus range .....  | 9-37  |
| 9-7   | Coordinate conversions .....   | 9-45  |
| 9-8   | Narrow Beam Antenna Characteristics .....                                    | 9-59  |
| 9-9   | Ku-band antenna Control Word 1.....  | 9-62  |
| 9-10  | Ku-band antenna Control Words 2 through 5.....                               | 9-63  |
| 9-11  | SM/GNC downlist telemetry - Status Word 1 .....                              | 9-68  |
| 9-12  | SM/GNC downlist telemetry - Status Word 2 .....                              | 9-69  |
| 9-13  | SM/GNC downlist telemetry - Status Words 3 to 10.....                        | 9-70  |
| 9-14  | GCIL commands .....  | 9-74  |
| 9-15  | (Serial I/O) EA-1 Control Word to SPA <u>and</u> SPA Status Word to EA-1 ... | 9-91  |
| 9-16  | Serial I/O EA-1 Control Word to EA-2 .....                                   | 9-94  |
| 9-17  | Serial I/O EA-2 Status Word to EA-1.....                                     | 9-95  |
| 9-18  | MSIDS and default values.....  | 9-120 |

## FIGURES

| Figure |   | Page  |
|--------|---|-------|
| 9-1    | Ku-band system block diagram.....                                 | 9-11  |
| 9-2    | Forward link 216-kbps data format .....                           | 9-20  |
| 9-3    | Convolutional encoder functional block diagram.....               | 9-25  |
| 9-4    | Pulsed continuous wave radar control signals .....                | 9-28  |
| 9-5    | Plot of the ratio range versus power .....                        | 9-39  |
| 9-6    | Ku-band peak field intensity versus range .....                   | 9-42  |
| 9-7    | Orbiter vehicle coordinate system and slewing directions .....    | 9-43  |
| 9-8    | Coordinate system.....  | 9-44  |
| 9-9    | Panel R14 Active Ku-Band Circuit Breakers.....                    | 9-78  |
| 9-10   | Panel A1U.....  | 9-79  |
| 9-11   | Panel A2 .....  | 9-83  |
| 9-12   | A1U Signal Strength Meter .....                                   | 9-84  |
| 9-13   | A1U EA-1 Talkbacks.....   | 9-84  |
| 9-14   | ANTENNA display .....   | 9-86  |
| 9-15   | SM SPEC 76 display .....  | 9-88  |
| 9-16   | REL NAV display .....   | 9-89  |
| 9-17   | EA-1/SPA signal interfaces.....                                   | 9-90  |
| 9-18   | EA-2/EA-1 interface .....   | 9-93  |
| 9-19   | EA-1/DA signal interface.....                                     | 9-98  |
| 9-20   | DEA/SPA signal interface .....                                    | 9-104 |
| 9-21   | EA-2/DEA interfaces.....  | 9-106 |
| 9-22   | Ku-band LRU locations, bay 3A.....                                | 9-113 |
| 9-23   | Ku-band LRU locations, bay 3B.....                                | 9-114 |
| 9-24   | Ku-band deployed assembly.....                                    | 9-115 |
| 9-25   | Ku-band location.....   | 9-116 |
| 9-26   | Ku-band deployed assembly power and temperature measurements .... | 9-117 |

**THIS PAGE INTENTIONALLY BLANK**

## SECTION 9 KU-BAND RADAR/COMMUNICATIONS SYSTEM

### 9.1 GENERAL

The KU system is a deployable dual mode system and functions as either a Communications (COMM Mode) device or as a Radar (RADAR Mode) sensor. COMM Mode is a continuous wave signal transmitter and receiver system and the RADAR Mode is a monopulse type RADAR with variable frequencies and pulse repetition rates.

The deployment and activation of the Ku System usually occurs 2 hours and 30 minutes after launch and stow usually occurs the day prior to the scheduled entry.

#### 9.1.1 Line Replacement Units Overview

The following is the list of the various Line Replaceable Units (LRUs) which make up the Ku-Band System. It contains both Internal LRUs (contained within the Shuttle Pressurized Cabin) and external LRUs (items contained within the forward starboard section of the Payload Bay).

There are three internal LRUs in Aviation Bay (AV BAY) 3 A and B.

- A. Electronics Assembly 1 (EA-1) provides the microprocessor control for the Ku system in both the COMM and RADAR Mode, the Average Gain Control (AGC) for the incoming signal, the Tau Dither Acquisition and Tracking Circuit for de-spreading the incoming data, and the COSTAS Demodulator/Lock Detector.
- B. The Signal Processor Assembly (SPA) is used for communications. This LRU selects the uplink mode and three downlink channels for the Ku Communications. The SPA also contains the Modulator switch and one Carrier control input.
- C. Electronics Assembly 2 (EA-2) is used for RADAR Signal processing. EA-2 controls the frequency and time of the outgoing monopulse signals and processes the incoming data pulse to establish RADAR lock to determine range/range rate, angle/angle rate data. This is accomplished using an Analog to Digital Processor.

There are several crew interface Ku-Band Displays and Switches on Panels A1U and A2.

The Ku-Band external components are contained within either the Deployed Electronics Assembly (DEA) or the Deployed Mechanical Assembly (DMA).

- A. The DEA houses the Exciter, Transmitter, Microwave Assembly and Receiver.
- B. The DMA contains the Alpha and Beta Gimbal Assemblies, Gyro Rate Sensor Assembly and the 36 inch parabolic dish (with associated Dish Antenna Electronics).

### 9.1.2 Communications Mode Overview

After deployment, power-on initialization, and Self-Test, command and control of the Ku system in Communication Mode is normally performed by INCO thru ground commands. In the communications mode, the KU-Band functions as a continuous wave transmitter/receiver.

1. The receiver operates as a Phase Shift Key (PSK) receiver. There are two possible subcarrier modes, Mode 1 and Mode 2. Mode 1, normally used, is the 216Kbps link composed of the 72Kbps (Command and Voice data, shipped to the NSP) component and a 128Kbps digital link that can be used for various payload purposes. Mode 2 has only the 72Kbps Command and Voice data subcarrier.
2. The transmitter is a non-coherent transmitter, that is, it has no dependence on the uplink frequency for transmission frequency. The transmitter can transmit in either the Frequency Modulated (FM) Mode or the Phase Modulated (PM) Mode. The FM Mode supports the 192 KBPS OD TLM link (channel 1), a low rate digital channel up to 4 Mbps (channel 2), and an analog channel capable of an analog TV transmission or high rate digital data up to 4 Mbps (channel 3). In the PM Mode, channel 1 and channel 2 capabilities remain the same but channel 3 becomes a digital channel capable of transmitting up to 48 Mbps.

### 9.1.3 Radar Mode Overview

The Crew normally uses panel switches, SPECs and Digital Displays to command and control the Ku-Band System in Radar Mode. In the RADAR mode, the Ku-Band functions as a monopulse transmitter/receiver. The Ku-Band can operate as either a passive system or active system. The active mode has never been used in flight. The passive mode uses target skin tracking of the returned transmitted Ku-band frequency to determine target location. The usable tracking range for the Ku-Band is from 150,000 ft to 100 ft.

1. At distances greater than 150K ft, the Ku-Band has a range ambiguity problem. It will report the system determined range at values at less than half of the true range. To prevent this false range solution, the Ku-Band activation into the RADAR mode is delayed until the target is within 135K ft.
2. Ku-Band is also inhibited at close distances, typically less than 500 ft, to prevent the introduction of tracking errors due to the phenomenon known as hunting. This is caused by the high signal return from a large RADAR cross section. The target does not appear as a single small point in space but as a large mass so the Ku-Band tracking functions hunt for the strongest signal.

#### 9.1.4 Ku-Band Activation Overview

Ku-Band activation is a crew function only. The ground can only monitor actions and provide assistance if called. The Ku-Band is deployed 146 degrees out of the payload bay with the electronic system unpowered and the 36 inch parabolic dish locked in place. The orbiter uses PL BAY MECH PWR to supply two 3 phase motors to deploy (and stow) the Ku-Band Deployed Assembly. Dual motor time for deployment is  $\approx$  23 seconds and single motor time is  $\approx$  46 seconds. Once deployed, the crew performs Ku-Band Activation and Initialization. Initialization, which includes EA-1 prom logic power-up, gimbal tests, gyro test, and TWT Heater warmup time takes approximately four minutes. Once initialization is complete, the crew can perform a Ku-Band Self-Test to check the functionality of some of the Ku-Band system LRUs; Self-Test takes approximately three minutes to complete. It is very important that the ground monitor this series of test and provide help if problems are encountered. The ground is also responsible to determine and calculate any ranging bias. This is reported to the Guidance Procedures Officer (GPO) and to the Flight Director.

#### 9.1.5 COMM Mode Operations Overview

When the Ku-Band system is placed in the COMM Mode of operations, the ground has the prime responsibility to monitor, control, and operate the system. The ground is responsible for keeping the on-board Ku-Band system and the Space Network (SN) TDRS system properly configured for uplink/downlink compatibility.

The Ku-Band has three ways to point the Azimuth and Elevation of the 36 inch Parabolic Dish in either COMM or RADAR Mode.

- A. The Crew can control the Ku-Band via Azimuth and Elevation Switches on Panel A1U.
- B. The SM GPC can point the Ku-Band Azimuth and Elevation angles using Orbiter - TDRSS pointing angles via PF1 MDM.
- C. EA-1 can track the uplink signal strength through four differential ports on the 36 inch Parabolic Dish and follow signal error generated by the differences.

The designers used these three ways to point the Parabolic Dish Antenna as inputs to four Antenna Steering Mode: MANUAL, AUTO, GPC and DESIG. The selection of the four Antenna Steering Modes can be commanded via GCIL or A1U Switch manipulation.

- A. The first Antenna Steering Mode discussed is the MANUAL mode. In this mode, the antenna can be pointed to Azimuth and Elevation angles via switches on panel PANEL A1U. It can be used to point the antenna for manual acquisition for various system failures. Normally, it is just used to slew the antenna to the "STOW position".



- B. The second Antenna Steering Mode discussed is AUTO Mode. In this mode, the Ku-Band can be first manually steered using the panel A1U Azimuth and Elevation switches. Once forward link is acquired, EA-1 will point the Parabolic Dish using its tracking function. If the forward link is lost, the antenna will remain in position until another mode is selected. In AUTO Mode, the Crew can hit the "SEARCH" momentary Switch to force EA-1 into its SEARCH routine to "look" for the forward link. Normally, AUTO Antenna Steering Mode is used while in RADAR Mode and the crew is maneuvering the vehicle.
- C. The third mode is the GPC or (GPC ACQ) Mode. GPC Antenna Steering mode is normally used in both COMM Mode and RADAR Mode. GPC Antenna Steering Mode uses both the PF1 MDM as an initial input of AZ and EL Angles to steer the 36 inch Parabolic Antenna and EA-1 track function. In GPC Mode, EA-1 uses PF1 MDM to point the Parabolic Dish Antenna to within .3 degrees of the intended AZ and EL. EA-1 will then ignore the PF1 AZ and EL inputs turning to Track Mode to control all Gimbal motor inputs. Once forward link has been detected EA-1 will track the forward link thru the differential ports using the generated signal error. If the acquisition is delayed by either a gap in forward link coverage or transitioning from blockage to an open look angle, the system will continue to search until the expiration of the search timer.
- D. The fourth Antenna Steering Mode is Designate (DESIG). DESIG mode forces EA-1 to use the SM GPC AZ and EL Pointing Angles to drive the Alpha and Beta Motors. Do NOT use DESIG mode in RADAR Mode; this will cause no Angle and Angle Rate information to be entered into the GNC GPC Kalman Filter.

EA-1 is programmed to allow the SPA to control the output Modulator Switch and Carrier Switches or override the DEA's Transmitter's Traveling Wave Tube (TWT) Carrier Out Switch. The SPA is designed to operate these two switches in either Primary or Alternate Acquisition Mode. Ku-Band operations always uses Alternate Acquisition Mode to allow the SPA to determine whether the Modulator and/or Carrier Switches are either on or off. In general, GPC Mode needs a forward link to turn on both the Carrier and Modulator switches; GPC DESIG mode will always have the Carrier switch on, and will normally turn on the modulator when an uplink signal is present. See Table 9-1.

**Table 9-1. Return link modulation and carrier status**

| Ku-Band Modulation - Automatic       |                                     |     |       |     |                            |     |       |     |
|--------------------------------------|-------------------------------------|-----|-------|-----|----------------------------|-----|-------|-----|
| SPA Carrier and Modulation Protocols |                                     |     |       |     |                            |     |       |     |
|                                      | Primary acquisition mode (Not Used) |     |       |     | Alternate acquisition mode |     |       |     |
|                                      | Not track                           |     | Track |     | Not track                  |     | Track |     |
| Antenna steering mode                | CARR                                | MOD | CARR  | MOD | CARR                       | MOD | CARR  | MOD |
| GPC                                  | ON                                  | OFF | ON    | ON  | OFF                        | OFF | ON    | ON  |
| GPC designate                        | ON                                  | OFF | ON    | ON  | ON                         | OFF | ON    | ON  |
| Auto track                           | ON                                  | OFF | ON    | ON  | OFF                        | OFF | ON    | ON  |
| Manual slew                          | ON                                  | OFF | ON    | ON  | ON                         | OFF | ON    | ON  |

PRIMARY ACQ mode is not used and is not planned to be used because TDRS cannot handle the increase in power as the Ku-band switches from wide beam to narrow beam.

In GPC and AUTO steering modes, the Ku-band radiates through the wide beam and receives through the narrow beam antenna until forward link "track," then transmit and receive through the narrow beam.

The ALTERNATE ACQ mode is how the Ku-band antenna is normally operated. In all steering modes using alternate acquisition, transmit and receive is done through the narrow beam antenna at all times.

Ku-Band Modulation - Automatic: (carrier and modulation) on/off status is a function of acquisition mode, tracking and modulation ON/OFF/AUTO controls (see Table 9-1).

Ku-Band Modulation - ON: TWT (carrier) and modulation is always on.

Ku-Band Modulation - OFF: TWT(carrier) and modulation is always off.

TRACK = COSTAS LOCK (carrier lock) and angle track in GPC and AUTO antenna modes.

In addition to the SPA's Alternate Acquisition mode controlling the DEA Transmitter's TWT switch. The prevention of Ku-Band from radiating specific physical regions (International Space Station, EVA Members, Payloads, the Shuttle) is a key area of Ku-Band operations. The underlying goal is to ensure EA-1 directly turns off (and back on) the TWT at critical times. There are several methods to allow EA-1 to turn off the TWT.

In Communications Mode, the Ground can command the SM to program EA-1 to directly control TWT off and on periods, by using “Beta plus Mask” or “Beta Only” RF Protocols. “Beta plus Mask” uses the following two protocols in parallel, i.e., if Alpha and Beta gimbal angles are below Shuttle Mask and below the Beta Angle an EA-1 will turn off the TWT-Off. If the ground commands “Beta Only”, EA-1 will turn off the TWT by using constraint (2) Beta only.

- A. The Shuttle Mask: The Original Designers created the Shuttle Mask contained within EA-1; this is a hardware PROM which contains a linear interpolation of the Shuttle with respect to the Ku-Band Deployed Position. In Radar Mode, if Alpha and Beta angles are “under” the Shuttle Mask, EA-1 will turn off the Carrier.
- B. Beta: This is a SM software loaded TMBU, stored within EA-1. Its value is continually compared with the Beta Gimbal Angle. If the Beta Value is smaller than actual Beta Gimbal Angle, EA-1 turns off the TWT.

A second way of having EA-1 control the DEA Carrier is RF Protect Boxes. In Communications Mode, up to four RF Protect Boxes can be loaded into SM Software to command the TWT-OFF command either on and off, forcing EA-1 to turn the TWT off or on. In General, ground commanding will load (via TMBUs) up to four sets of AZ and EL Angles within SM Software. The SM GPC, every 1.92 seconds, compares the Ku-Band AZ and EL angles and determines if this “point” is within one of the four enabled RF Protect Boxes. If the AZ and EL Angle is within one of these boxes, it commands EA-1 to turn off the TWT. There is a software anomaly written into this code. If the Ku-Band acquires within one of these RF Protect Boxes, it will radiate for 1.92 seconds (the time it takes for the SM GPC to get “feedback” determining that the AZ and EL are within an RF Protect Box). INCOs should use their predictive tools to determine when these events happen and manually command Ku-Band TWT to Off (and then back on) using Stored Program Commands.

Single Fault Analysis has determined that one hardware failure within Ku-Band could cause the Ku-Band to radiate the Orbiter Docking Station (ODS). The ODS has a pyro assembly with RF limitations. Even if it is protected by other methods, INCO will command the Ku-Band to STBY when pointing angles are within a 3° cone intersecting the ODS. The Ku Band can be commanded to ON 3° past the ODS exit cone.

#### **9.1.6 Communication Mode Forward Link Path Overview**

In Communications Mode, the Ku-band system receives the forward link signal from the TDRS and process it for use in the NSP and OCA/Payload systems. The Ku-Band forward link Carrier is normally a spread RF Signal with a frequency ~ 13.775 GHz signal (Doppler dependant). This forward Link signal is reflected off the parabolic dish and concentrated into the Dish Antenna Electronics entering a two-channel receiving system.

- A. The sum channel is processed to recover forward link modulation.
- B. The four difference channels are processed by alternating Summing and Subtracting then time division multiplexed to provide angle error information to EA-1.

Both channels enter the DEA, channeled along through the Microwave Assembly, downconverted in the Receiver to the first Intermediate Frequency (IF) of 647 MHz, then output to EA-1.

In EA-1, the sum channel is then downconverted to the second IF frequency of 21.88 MHz. After Automatic Gain Control (AGC) is used, it is applied to the Pseudorandom Noise (PN) despreader and COSTAS demodulator. The spreading signal is removed by the tau-dither circuit if in the spread spectrum mode. The COSTAS demodulator finds the exact uplink frequency to remove the uplink modulation (216 kbps). This baseband signal is then output to the Communications Signal Processor (SPA).

The baseband signal sent to the SPA is bit synchronized, frame synchronized, and demultiplexed. The 72 kbps data is sent directly to the NSP (notice Ku-Band uplink modulation is not convolutionally coded). The 128 kbps data is sent to the shuttles PDIP port (currently being used for Orbiter Communications Adaptor (OCA) or Payloads).

In EA-1 the difference channels are time division demultiplexed and amplitude modulated. Angle error information is demodulated from the 647 MHz track IF and summed to the antenna Gimbal Servo Circuits. This output is applied to a control function to signal Alpha and Beta Motor rates for closed loop tracking of the forward link signal.

### **9.1.7 Communication Mode Return Link Path Overview**

The return link transmits telemetry data to the ground via TDRS. Ku-Band SPA has three output channels. Channel 1 receives operational data at 192 kbps and Channel 2 digital data (up to 2 Mbps NRZ-L); these are phase multiplexed on an 8.5-MHz subcarrier. The 8.5 MHz subcarrier is used as a digital output directed to both a Frequency Modulator and Phase Modulator. Selection of Channel 3 determines which modulation output is actually sent to be applied to the Carrier.

If Payload MAX is selected, channel 3 data (up to 48 Mbps) enters the SPA and is Convolutionally Encoded. This digital Output is multiplexed in the I direction with the phase multiplexed 8.5-MHz subcarrier in the Q direction using an RF Coupler. This output is placed on an S-band carrier of 1.875 GHz.

If Payload MAX is not selected, Channel 3 will use the Frequency Modulation output. Any other HDR 500 bps - 4.5 MHz source (analog or digital) GCIL selected input, is

summed with the phase multiplexed 8.5-MHz subcarrier onto the Channel 1/2 data. This signal is frequency modulated onto the S-band carrier at 1.875 GHz.

After either the PM or FM output is selected, this “3 channel output” 1.875 GHz signal is routed to the EA-1 controlled Modulator On/Off Switch. If EA-1 commands the Modulator On, the 1.875 GHz signal leaves the SPA and is routed to the DEA’s Exiter.

Within the DEA’s Exiter, the “3 channel output” 1.875 GHz signal is upconverted to 15.003 GHz, passing unaffected through the Step Attenuator being routed to the Transmitter.

The “3-channel output” 15.003 GHz carrier signal will enter the Traveling Wave Tube (TWT) and will be amplified by ~43 dB to 60 W. This “3-channel output” 15.003 GHz amplified carrier signal is then routed to the DEA’s Microwave Assembly.

DEA’s Microwave Assembly will filtered and routed through two diplexers and a circulator to the Deployed Mechanical Assembly (DMA). The Modulated Carrier Signal is shipped through the DMA’s rotary joints to the sum feed of the antenna. This signal is then radiated to the TDRS and retransmitted to White Sands, New Mexico.

### **9.1.8 Radar Mode Operations Overview**

Radar Operations are performed by the crew. Ground operations are to monitor, observe and report. Once the crew transitions to the RADAR Mode and enables GNC pointing, it is the GPO’s responsibility to evaluate the data for incorporation into the NAV Base. Any observed irregularities should be reported to GPO and the Flight Director. Two critical points to be monitored are:

- A. When the Orbiter is maneuvering out of the target track attitude the KU-Band antenna must be placed in the AUTO Mode. This will prevent the antenna from entering a search mode if lock is lost. The search scan in the RADAR mode is 40°per sec and if allowed to encroach into the ALPHA stop zone may cause structural damage to the antenna. The rule is never allow the antenna to get to  $\pm 38^\circ$  in BETA angles.
- B. The other point of monitoring is the radiation requirements for payloads. This is based on a 20volt/m radiation level. The flight rule value for distance is 864 feet when the RADAR OUTPUT is switched to LO. The same can be accomplished if the TWT is commanded OFF from the ground (this will place the TWT in the Bypass mode).

### **9.1.9 Radar Mode RF Pulse Transmission and Reflection Overview**

When in Radar Mode, the radar is a low Pulse Repetition Frequency (PRF), pulsed Continuous Wave (CW), coherent Doppler radar. Two operating modes are available, passive (skintrack) and cooperative (target has a transponder). The passive mode is always used.

EA-2 controls all radar RF functions including:

- A. Signals to EA-1 to control gimbal motor rates
- B. Signals to DEA to control Exciter Output Frequency
- C. Signals to DEA to control Output RF Pulse Length
- D. Signals to DEA to control RF Pulse Power

In General, EA-1 sends EA-2 a “predicted range” to target. With this range, EA-2 will directly control RF Pulse Length (Longer Pulse, farther distance) and RF Pulse Power (More Power, farther distance). It controls the DEA to cycle through five different frequencies with different pulse repetition rates to try to “paint” a target with RF Energy. With a 49 MHz timer, each pulse is “shot” out of the DEA Exciter and “should” hit the target with a portion of the energy being reflected back into the Parabolic Dish. The Parabolic Dish receives this energy through a two-channel receiving system.

The sum channel

The four difference channels, which process the signals by alternating Summing and Subtracting then time division multiplexed to provide angle error information to EA-1 for Tracking error signals.

Both channels enter the DEA, channeled along through the Microwave Assembly, downconverted in the Receiver to the first Intermediate Frequency (IF) to ~ 647 MHz, then summed. Note this difference from Communications Mode, in Radar Mode the DEA will sum all four differential signals to the main sum signal and downconverts it to ~ 78 MHz (plus or minus Doppler) prior to being sent to EA-2.

EA-2 receives this “reflected” energy and downconverts it a third time to ~ 0MHz (+ or - Doppler). EA-2 will convert this energy to a digital signal to represent the RF Power Reflected, Frequency Received and “clock” the time the energy was received. EA-2 will then “shoot” the next RF Pulse, and repeat.

EA-2 uses this digital data and processes it with a collection of other received pulse information to derive Range, Range Rate, Azimuth, Azimuth Rate, Elevation and Elevation Rate.

EA-2 sends this information to EA-1. EA-1 sends this information to GNC GPC, SM GPC, and Panel A2 Digital Output displays.

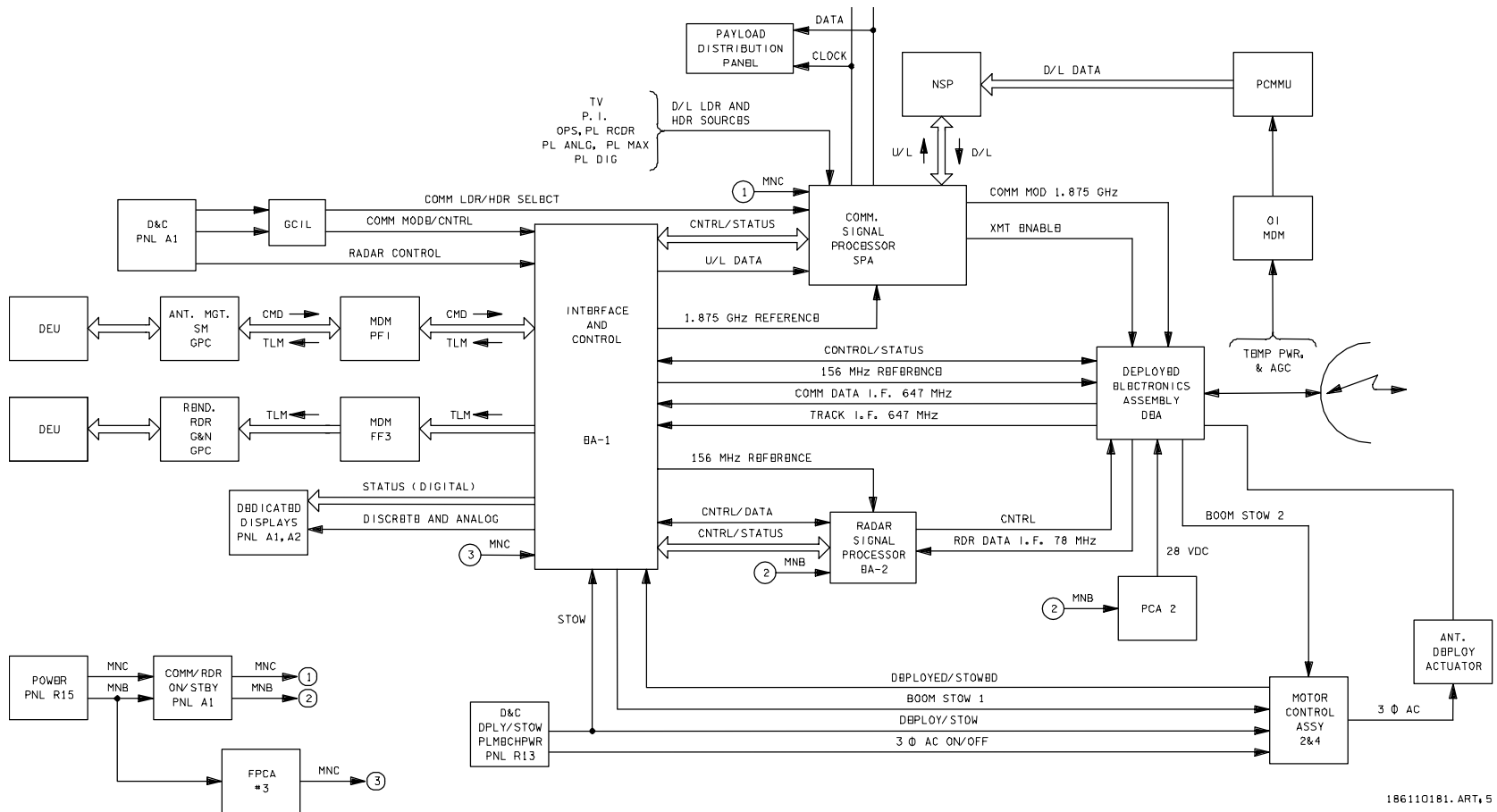
### 9.1.10 Interfaces Overview

Ku-Band is a complex system of LRUs. Each LRU performs a certain task with either control or routing key signals. Understanding how the Uplink, Downlink, Analog control, Digital control, and Discrete control flow between LRUs is very important.

It is this writer's opinion (not humble opinion) the understanding EA-1 (also known as the RADAR/COMM Interface and Control Unit) is key in understanding how the entire Ku-Band system works. EA-1 hardware/software sends "most" of the controlling discrettes/signals to many of the other systems LRUs. EA-1 interfaces with the following LRUs.

- A. SM General Purpose Computer (GPC) via the Payload Forward 1 (PF 1) Multiplexer/ Demultiplexer (MDM) receives configuration data from, and provides telemetry data to, the Antenna Management (AM) Software.
- B. Guidance, Navigation and Control GPC receives telemetry via the Flight Forward 3 (FF 3) MDM to perform rendezvous radar operations.
- C. Crew controls on panel A1U operate the system in either Radar or Communication mode.
- D. Ground Control Interface Logic (GCIL) commands allow the ground to operate the system in the Communication mode.
- E. Dedicated displays on panels A1U and A2 display measured system parameters; e.g., range, angle, signal strength, etc. System data are also displayed on the SM and GNC and SM Display Electronics Units (DEUs).
- F. Providing the SPA the forward link and Modulation Switch control.
- G. Controlling the DEA Carrier Switch Action.
- H. Providing DMA Alpha and Beta Gimbal motor rate controls.
- I. Interaction with EA-2 provides key Radar Information.
- J. The Deployed Motor Subassemblies inputs

A large subsection of this System Brief discusses each LRU to LRU signal interfaces.



186110181. ART. 5

Figure 9-1. Ku-band system block diagram



### 9.1.11 Communications Mode vs. Radar Mode

The Ku-band units that are functional and powered up in Communications mode are

- Interface and Control Unit (also referred to as Electronic Assembly No. 1 (EA-1))
- Deployed Assembly (includes the Deployed Mechanical Assembly (DMA) and DEA)
- Communications Signal Processor (also referred to as the Signal Processor Assembly (SPA))

The Ku-band units that are functional and powered up in Radar mode are

- Interface and Control Unit (EA-1)
- Deployed Assembly (DA)
- Radar Signal Processor (EA-2)

## 9.2 ELECTRONICS ASSEMBLY - 1 (EA-1)

Electronics Assembly - 1 (also known as the Interface and Control Unit) is the central processing LRU within the Ku-Band system itself. It provides the key interfaces to the other LRUs in the Ku-band system and information to the D&C and GPCs. It also provides control signals for proper configuration and operation of the system.

The control function is executed using a microprocessor that evaluates the various analog, discretized, serial Input/Output (I/O) signals and system status to configure the system for the proper operating modes.

The functions of the microprocessor are very important, controlling the input and output flow, logic states, and subroutines used. Due to the large amount of microprocessor information, System Brief 10 (SB10) will provide all the EA-1 software protocols.

A large portion of EA-1 circuitry is devoted to processing the forward link communications signal. In addition to amplifying and filtering, the signal is despread (remove the PN code) and demodulated (COSTAS demodulator removes the phase shift keyed 72/216-kbps data from the forward link signal) prior to sending it to the Communications Signal Processor for final data decommutation and distribution.

EA-1 also contains a very stable oscillator which is the frequency reference source for most of the circuits in the four Ku-band LRUs.

EA-1 also houses the alpha (a) and beta (b) gimbal servo circuits that control motor position. These gimbal servo circuits are only slightly different; the alpha circuit contains two more stages of gain adjustment and also includes Radio Frequency

Interference (RFI) reduction circuitry. The gimbal motor drive signals, which positions the antenna use various inputs, in general:

- A. When the system is in Search or Slew Mode is composed of a microprocessor commanded rate minus the rate sensor gyro signal (which is the actual antenna inertial rate).
- B. When the antenna is in Track Mode, the gimbal motor drive signal is composed of either the comm or radar angle error signal (D AZ/D EL) minus the rate sensor gyro signal.

### 9.2.1 Reference Oscillator

The fundamental oscillator frequency, 156.285 MHz, is generated by a seventh overtone crystal and is the reference frequency signal provided to the DEA exciter module and Radar Signal Processor.

A times four (x4) frequency signal (625.14 MHz), used as the second local oscillator frequency, is used in EA-1 to downconvert the 647 MHz data IF to the second IF of 21.88 MHz.

A x12 frequency signal (1875.42 MHz) is output to the Communications Signal Processor (SPA) where it is used to generate the Phase-Shift Keyed (PSK'd) S-band carrier signal for the Phase Modulation (PM) mode of operation.

### 9.2.2 Automatic Gain Control

The AGC circuit is used to generate a control signal derived from the RF noise spectrum associated with the second IF signal at 21.88 MHz. A 1-MHz bandpass filter is centered at the first null of the PN spectrum at 18.85 MHz. (The bit rate of the PN code is 3.028 Mbps, therefore, the first null will be at +3.028 MHz about the 21.88-MHz IF). The noise level is compared against a reference voltage, and the resultant signal is amplified and used to control the AGC attenuator to maintain the IF signal level constant over the expected 10-dB dynamic range of the IF input signal. This signal, after passing through the Automatic Level Control (ALC) attenuator, is divided by a series of power dividers and applied to the ALC circuit, the PN despreader (tau-dither loop) and PN lock detector, and the COSTAS demodulator and COSTAS lock detector for further processing.

### 9.2.3 Automatic Level Control

The ALC circuit operation is similar to that of the AGC, the major difference being the method used to derive the ALC control signal. It is derived from the outputs of two separate filters, a signal plus noise filter (2-MHz bandwidth) located at the center of the 21.88-MHz IF spectrum and a noise filter identical to the AGC filter (1 MHz) centered at the first PN null. The signal-plus-noise and noise signals are differenced, and this signal is compared against a reference level. This signal is amplified and then used to control the ALC attenuator to maintain the IF signal level constant over the operating

range. A second output is used to decrease the gain of the correlation detector in the tau-dither loop to minimize the possibility of false lock at strong signal levels. The third output of the ALC circuit is used to provide a measure of comm forward link signal strength. The signal strength measurement is compensated for the spread spectrum mode of operation because, in the spread mode, the signal-plus-noise filter truncates the RF spectrum in its 2-MHz bandwidth.

#### 9.2.4 COSTAS Demodulator

The COSTAS demodulator is the primary sensor used to acquire and track the forward link TDRS signal. The demodulator will acquire the following types of signals in approximately 350 ms:

- Unmodulated carrier
- Data modulated carrier (72/216 kbps)
- Spread spectrum modulated carrier (3.024-Mbps PN code)
- Spread spectrum and data modulated carrier

The 21.88-MHz IF signal is biphase modulated by the 5.92-kHz square wave dither signal in order for the COSTAS loop to track the unmodulated carrier (since the primary function of the loop is to track the "suppressed" carrier in frequency and phase and remove the modulation). The COSTAS loop can also acquire and lock onto the spread spectrum modulated carrier. In this case, there would be no data output since the signal is only modulated by the spreading PN code. In normal operating mode, the COSTAS loop locks up to the spread signal and the COSTAS lock detector causes the antenna scan to be terminated if searching. When the tau-dither loop locks up to the spread signal and despreads it, the COSTAS loop acquisition/track control logic enables the on-time PN code to biphase modulate the 21.88-MHz IF signal and despread it. The 5.92-kHz dither, although not required, still modulates the IF signal.

The COSTAS demodulator uses in-phase and quadrature-phase detectors (mixers) to acquire and track the "suppressed" carrier IF signal. During acquisition, the acquisition/track control logic issues a "sweep on" command to the loop filter and sweep circuit that sweeps the 21.88-MHz VCO + 175 kHz about its rest frequency. The phase shifter provides the 0° phase signal to the in-phase mixer and the 90° phase delayed signal to the quadrature-phase mixer. The VCO synchronizes its frequency with the IF signal and tracks it. The VCO control signal is derived from the Q-channel phase detector (mixer) output and is a measure of the IF signal average phase shift. The data (72/216 kbps) are removed from the Q-channel signal by inverting it and multiplexing it with the hard limited I-channel signal. The COSTAS LOCK detector will output a COSTAS LOCK signal to the acquisition/track control logic which will terminate the VCO sweep, disable the ac coupling, and decrease the Q-channel bandwidth. The VCO will then track the IF signal "suppressed" carrier. The dithered data in the I-channel are biphase modulated to remove the 5.92-kHz dither, then filtered, amplified, and output to

the comm signal processor. Another output is routed to the data detect circuit to determine whether data are present or not. An AGC circuit is used to set the gain of the I-channel amplifier to provide a constant input level to the hard limiter.

### 9.2.5 COSTAS LOCK Detector

The COSTAS LOCK detector is a circuit that determines when the COSTAS demodulator is in lock with the 21.88-MHz IF signal, outputs the COSTAS LOCK signal to the acquisition/track control logic, and enables the comm 0°/180° and D AZ/D EL signals for difference channel tracking of the forward link. The biphasic modulator spreads the IF signal with the locally generated on-time code for the condition where the forward link signal is not spread. This ensures that the signal into the detector is nearly the same, regardless of the type of signal received; i.e., unmodulated carrier or data modulated carrier. The spreading code is disabled if the signal is already spread. The spread IF signal is mixed with a 1.48-kHz dithered version of the COSTAS VCO 0° and -90° phase signals. This signal is filtered and limited to about 500 millivolts. The square law detector rectifies and outputs a signal which is proportional to the I<sup>2</sup>Q<sup>2</sup> signals in the COSTAS loop. When the COSTAS loop is near or is in lock, I<sup>2</sup>>>> Q<sup>2</sup> the low pass (5 Hz) output signal will exceed the referenced threshold and output a COSTAS LOCK signal to the tracking logic and to the data present AND gate.

### 9.2.6 Tau-Dither Acquisition and Tracking Loop

The tau-dither acquisition and tracking module, in conjunction with the PN lock detector, removes the PN code from the 21.88-MHz IF signal in the spread spectrum mode. The removal of the PN code requires a local replica of a code which is in synchronism with the received code. Therefore, the tau-dither loop/PN lock detector must search out the phase of the received PN code and then lock the local code generator to it. Once synchronism is established, the tau-dither loop must track the received code.

The 5.92-kHz dithered early code (1/2 bit advanced relative to the on-time code) and late code (1/2 bit delayed relative to the on-time code) are mixed with the 21.88-MHz IF spread signal. In the unspread mode, the COSTAS demodulator and lock detector would recover the data. The biphasic modulated signal is passed through the matched bandpass correlation filter. The correlated output is detected and the dither removed. These two signals, corresponding to the early and late code correlations, are differenced, filtered, and summed with the scan signal. After loop filtering, the phase error signal is applied to the 12.112-MHz VCO to adjust the 3.028-MHz output so that the gold code PN generator outputs the on-time code that is in phase synchronization with the received PN code.

In the acquisition phase, the scan circuit outputs a voltage that offsets the 12.112 MHz VCO frequency from its rest frequency and causes the locally generated PN code and the received code to slip past each other until synchronism (correlation) is achieved. When this occurs, the PN lock detector outputs the PN lock signal that decreases the loop filter bandwidth and removes the scan circuit offset voltage from the VCO. Then the phase error output of the summer will maintain PN code phase lock.

### 9.2.7 Pseudorandom Noise Lock Detector

The PN lock detector is similar in operation to the COSTAS LOCK detector, but instead of a phase correlation ( $I_2 \gg Q_2$ ), it looks for an on-time code correlation by comparing it to a late-late code (1-1/2 bits delayed relative to the on-time code). The on-time and late-late codes are dithered at a 739-Hz rate and mixed with the received PN code. The mixer output is match filtered and detected, then demultiplexed at the 739-Hz dither rate. This output signal is then low-pass filtered and compared to a reference threshold. During acquisition, both the on-time and late-late code correlations will be equal and the output signal will not exceed the reference threshold. But as the on-time code approaches, synchronization with the received PN code; i.e., higher correlation, the lowpass filter output level will increase. When it exceeds the reference threshold, the PN lock signal will be output to the scan circuit, bandwidth control, and data present logic.

### 9.2.8 Comm/Radar Tracking Logic

When the Ku-band system is in Track Mode, certain signals are required to enable the tracking logic to provide the proper angle error signals and lobing signals ( $0^\circ/180^\circ$  and AZ/EL) to the a and b gimbal servo circuits and to the receiver phase shifter (DEA) and the AZ/EL switch in the antenna electronics. In Comm Mode, the COSTAS lock signal enables the timing generator to output a 739-Hz square wave for the  $0^\circ/180^\circ$  lobing and a 369 Hz square wave for the AZ/EL lobing. In Radar Mode, the radar lobing enable (from the Radar Signal Processor) enables the Radar Signal Processor to output the  $0^\circ/180^\circ$  lobing signal, which will be a square wave in the frequency range 8 Hz to 206 Hz. Actual frequency is the PRF divided by 34 (PRF/34), and an AZ/EL lobing signal, which will be a square wave in the frequency range 4 Hz to 103 Hz. Actual frequency is the PRF divided by 68 (PRF/68).

In Radar Mode, the antenna angle error signals are multiplexed onto the difference channel signal, which is added to the sum channel and mixed with the radar second LO (573 MHz) to downconvert it to the radar second IF of 78 MHz. The  $0^\circ$  and  $180^\circ$  AZ and EL error signals are demultiplexed in the Radar Signal Processor and output to the a and b gimbal servo circuits.

In Comm Mode, the antenna angle error signals are similarly multiplexed onto the difference channel and added to the sum channel. However, this first IF signal (647 MHz) is then provided as the comm track IF signal to the Interface and Control Unit. There it is bandpass filtered, AGC'd, and detected to recover the angle error multiplexed signal. The angle error detector demultiplexes the  $0^\circ$  and  $180^\circ$  AZ and EL error signals and outputs them to the a and b gimbal servo circuits.

### 9.2.9 a and b Gimbal Servo Circuits

The only difference between the a and b gimbal servo circuits is that the a circuit has two additional stages of gain adjustment in the amplifier and shaper, and it includes an RFI reduction circuit. Therefore, the description is applicable to both gimbal circuits.

The output of the gimbal servo is an 8.3-KHz pulsewidth modulated direct current (dc) signal that will cause the antenna gimbal motor to turn in a positive or negative direction. Thus the drive 1 and drive 2 outputs are bipolar; i.e., + dc. The gimbal servo operates in two modes, point or track. In point mode, the servo comparator receives a commanded rate computed by the microprocessor as the difference in the designated angle and the actual angle or as a slew control input that is processed into a pseudo-designated angle and then differenced with the actual angle. This commanded rate is then algebraically added to the high input, which is the high rate (coarse) output of the gyro in the rate sensor assembly and is the actual antenna inertial angle rate. In track mode, the servo comparator receives actual antenna angle error signal and algebraically adds it to the low input, which is the low rate (fine) output of the gyro.

The amplifier and shaper circuit sets the required gain and shapes the comparator output signals into torque commands to achieve required servo loop performance and loop stability. The RFI adjuster circuit monitors the a and b torque commands and, in conjunction with the 8.3-kHz sawtooth signal, selectively inverts the phase of a sawtooth based on the polarity of the a and b torque commands to ensure that the loads placed on the power bus by the two motor drivers are always 180° out of phase. In this way, conducted interference from each driver tends to cancel the other.

The duty cycle modulator uses a dc-to-dc converter operating at 50 kHz and a duty cycle that switches the motor drive output polarity at an 8.3-kHz rate. At a 50 percent duty cycle, the output current (drive) would be zero. Duty cycles greater or less than 50 percent result in positive or negative dc, respectively. A sample of the output drive is compared to the commanded torque, and the difference is used to adjust the duty cycle from 0 to 100 percent in order to output the desired motor drive.

A tachometer circuit is used to monitor the antenna encoder outputs to determine the antenna angular rate. The motor drive output will be shut off if either gimbal angular rate exceeds 130 deg/s.

The timing generator (tau-dither circuit) also provides the signals required by the gyros in the rate sensor assembly: a two-phase square wave at 893 Hz for the spin motors and a 4.6-kHz sine wave signal for the primary gyro excitation.

### **9.3 COMMUNICATIONS SIGNAL PROCESSOR (SPA)**

The Communications Signal Processor receives the forward link data (72/216 kbps) from the Electronics Assembly - 1 (EA-1). In 72-kbps mode it throughputs the biphasic bit stream to the network signal processors. In 216-kbps mode it must bit synchronize, resolve the one-half bit phase ambiguity, frame synchronize and decommutate, and output the data to the network signal processors and the text and graphics and payload distribution systems. (Normally, we are in 216 kbps uplink mode)

The SPA assembles three channels of data from various orbiter sources and PSKs the operational data and the low rate data onto an 8.5-MHz subcarrier. This subcarrier is then combined with the high rate data onto a 1.875 GHz carrier by either of two

modulation methods. It is Quadrature Phase Shift Keyed (QPSK'd) with the payload max (Spacelab) data or frequency modulated with one of the other high data rate sources.

The SPA also contains an internal microprocessor with protocols for both Primary and Alternate acquisition mode. Again, only Alternate Acquisition mode is used to control the Modulator On/Off control and a Carrier On/Off signal to the DEA.

### 9.3.1 Bit Synchronizer and Ambiguity Resolver

The function of the bit synchronizer is to synchronize the locally generated 216 kHz clock with the forward link 216-kbps Biphase Level (Bif-L) bit stream and resolve the one-half bit phase ambiguity (is it a "one" or a "zero"?). The bit synchronizer uses a 6.912-MHz clock generated by differencing a 27.648-MHz VCO and a 20.736-MHz VCO. This method increases the effective linear pull-in range of a single VCO and maintains its frequency stability. The forward link timing module outputs the 6.912-MHz reference clock and a 2x bit rate clock (432 kHz) to the frame decommutator timing module. It also outputs an in-phase and inverted bit rate clock (216/216 kHz) to the ambiguity resolver. A 2x bit rate clock (432 kHz) is mixed with the forward link 216 kbps Bif-L data and the output is fed to the in-phase Integrate and Dump (I&D) circuit. The mixer converts the 216-kbps Bif-L data to a 432-kbps Non-Return-to-Zero Level (NRZ L) bit stream. The I&D control signal operates both I&D circuits so that they integrate their input data at the 432-kbps rate, thus sampling the 432-kbps data every bit and the 216 kbps every Bif-L bit. The in-phase I&D logic, by integrating at the 432 kbps rate, integrates over each bit transition. These will correspond to mid-bit and between-bit transitions of the Bif-L bit stream. It can then resolve the phase ambiguity of the 216-kbps Bif-L data stream and the ambiguity resolver will select either the 216 kHz or 216-kHz clock and output it to the bit detector. The output of the quadrature I&D is gated under control of the in-phase logic to provide the correct sense error signal to the loop filter to synchronize and lock the VCO to the 216-kbps data stream.

### 9.3.2 Bit Detector

After bit synchronization, the bit detector is used to convert the 216 kbps Bif-L data to 216 kbps NRZ-L. The bit detector mixes the 216-kHz clock from the ambiguity resolver with the 216-kbps Bif-L data and provides the output to an I&D circuit, which converts it to 216-kbps NRZ-L.

### 9.3.3 Frame Synchronizer

The purpose of the frame synchronizer is to detect the frame synchronization pattern (32 bits), lock up to it and maintain lock, and output the 216-kbps forward link data to the decommutator. Figure 9-2 shows the format of the 216-kbps Time Division Multiplexed (TDM) data. Each frame consists of 9 bytes, and each byte is 48 bits. There are 500 frames per second. The first 32 bits of each frame consist of a frame code (B7EB8CEC, hexadecimal) which is used to establish frame synchronization. The remaining 16 bits in byte 1, as well as the last 16 bits in every byte, are reserved for

operations data at a 72-kbps rate. The first 32 bits of the 8 remaining bytes in a frame are used for text and graphics/payload data at a 128-kbps rate.

The byte counter derives the byte clock (4.5 kHz) and the frame clock (500 Hz) from the 216 kHz clock from the ambiguity resolver. These clocks are divided by 2 and output to the four 256-bit shift registers. When the system is in lock, these signals alternately load the 128-kbps and 72-kbps data into the shift registers.

The correlation detector compares the 32 bits of sync data every bit time in search and passes the 216 kbps data or invert it, depending on whether it detects a positive correlation (30 bits agree with the local code) or negative correlation (no more than 2 bits agree with the local code). No correlation keeps the circuit in search mode. After one correlation, the detector goes into acquisition mode. After the second correlation, the frame synchronizer goes into lock mode and an event counter is set to zero. Once in lock mode, it takes three correlation misses to switch the synchronizer back to search mode.

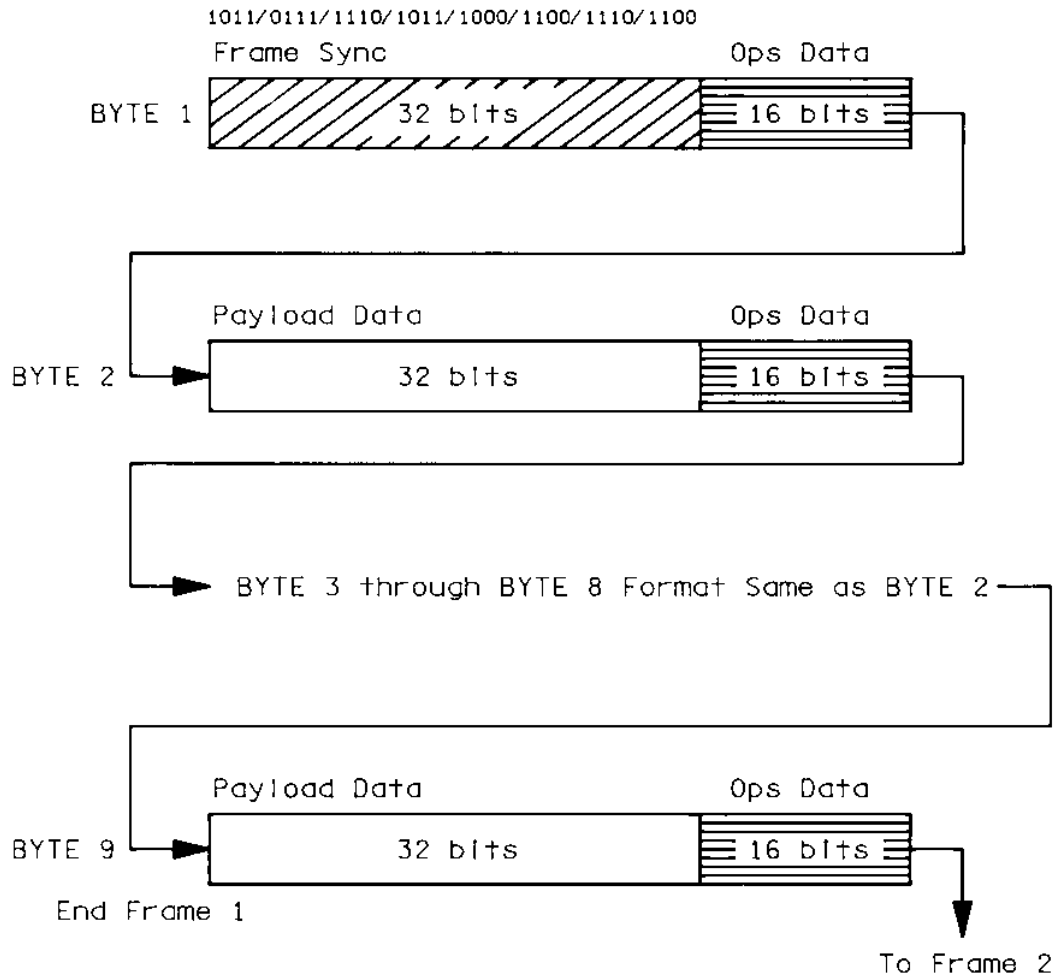
#### **9.3.4 Frame Decommutator**

The frame decommutator uses the 128-kHz and 72-kHz clocks to read the 128-kbps and 72 kbps data alternately from the 256-bit shift registers. The 128-kbps NRZ-L data are clocked out by the 128-kHz clock to the text and graphics/payload equipment. The 72 kbps NRZ-L data are converted to Bif-L using the 144-kHz clock to drive a Manchester encoder. The 72-kbps operational data are output to both NSPs.

#### **9.3.5 Data Source Selector**

The data source selector configures the three-channel return link and selects the modulation technique (Frequency Modulation (FM)/PM) in accordance with the GCIL select discrettes for the HDR and LDR channels and the forward load control assembly discrettes that select which NSP is powered up and will provide data to the OPS data channel. The HDR selection determines the modulation technique used for the return link. If PL max (2 to 50 Mbps) is selected, the modulation technique will be QPSK on the return link. For any other HDR selection, including the OFF position, the modulation technique will be FM on the return link. The characteristics of the various high and low data rate inputs of the signal processor are shown in Table 9-2.





TDM RATE = 216 KBPS  
PAYLOAD DATA RATE = 128 KBPS  
OPS DATA RATE = 72 KBPS  
SYNC DATA RATE = 16 KBPS

48 BITS = 1 BYTE  
9 BYTES = 1 FRAME  
500 FRAMES/SEC = 216 KBPS

**Figure 9-2. Forward link 216-kbps data format**

**Table 9-2. High/low data rate channel input signal characteristics**

| High data rate  |                         |
|-----------------|-------------------------|
| Payload maximum |                         |
| Data .....      | 2 to 50 Mbps (variable) |
| Clock .....     | 2 to 50 Mbps (variable) |
| Waveform        |                         |
| Data .....      | NRZ-L, -M, -S           |

**Table 9-2. High/low data rate channel input signal characteristics (continued)**

| <b>High data rate</b>       |  |
|-----------------------------|--|
| Clock .....                 | Square wave  |
| Signal amplitude            |  |
| Data .....                  | Logic 1 = 4.5 to 6.5 volts<br>Logic 0 = -0.5 to 0.5 volts  |
| Clock .....                 | Logic 1 = 3.7 to 6.5 volts<br>Logic 0 = -0.5 to 1.5 volts  |
| Load impedance              |  |
| Data/clock .....            | 50 ohms  |
| Source coupling             |  |
| Data/clock .....            | Single ended   |
| Asymmetry                   |  |
| Input                       |  |
| Data.....                   | Less than 16 percent at 50 Mbps, increasing linearly with decreasing data rate to 38 percent at 8.5 Mbps and lower rates |
| Clock .....                 | Less than 30 percent   |
| Output                      |  |
| Data/clock .....            | Degraded less than 10 percent  |
| Closed circuit TV           |  |
| Waveform.....               | EIA RS 330 figure 1  |
| Frame rate.....             | 29.97 per second   |
| Lines per frame .....       | 525  |
| Aspect ratio .....          | 4/3  |
| Horizontal scan rate .....  | 15,734.264 Hz  |
| Vertical scan rate .....    | Horizontal scan rate/262.5   |
| Bandwidth .....             | Dc to 6.95 MHz   |
| Signal level.....           | 1.0 volt peak-to-peak (from sync tip to reference white level). Sync tip is at 0 volts.                                  |
| Impedance .....             | 50 ohms  |
| Payload analog              |  |
| Waveform.....               | Analog or payload TV   |
| Signal level.....           | 1 volt peak-to-peak (line-to-line)   |
| Source/load coupling.....   | Balanced differential  |
| Source/load impedance ..... | 75 ohms  |

**Table 9-2. High/low data rate channel input signal characteristics (concluded)**

| <b>High data rate</b>       |  |
|-----------------------------|--|
| Bandwidth .....             | Dc to 6.95 MHz   |
| Payload interrogator        |  |
| Waveform .....              | 1.024 MHz or 1.7 MHz subcarrier modulated by PSK or FM                 |
| Signal level .....          | 6 volt peak-to-peak (line-to-line)                                     |
| Source/load coupling .....  | Balanced differential  |
| Source/load impedance ..... | 75 ohms  |
| Payload digital             |  |
| Data rate .....             | 16 kbps to 4 Mbps  |
| Waveform .....              | NRZ-L, -M, -S  |
| Signal level .....          | 1 volt peak-to-peak (line-to-dedicated return)                         |
| Source impedance .....      | 75 ohms (unbalanced)   |
| <b>Low data rate</b>        |  |
| MMU 1 or 2                  |  |
| Data rate .....             | 25.5 kbps to 1.024 Mbps  |
| Data type .....             | Biphase level (Bi $\phi$ -L)   |
| Signal level .....          | 2.5 to 9 volts peak-to-peak  |
| Source/load coupling .....  | Balanced differential  |
| Source/load impedance ..... | 75 ohms  |
| Payload interrogator        |  |
| Waveform .....              | 1.024 MHz or 1.7 MHz subcarrier modulated by PSK or FM                 |
| Signal level .....          | 6 volt peak-to-peak (line-to-line)                                     |
| Source/load coupling .....  | Balanced differential  |
| Source/load impedance ..... | 75 ohms  |
| Payload digital             |  |
| Data rate .....             | 16 kbps to 2 Mbps (NRZ-L, -M, -S) 16 kbps to 1.024 Mbps (Bi $\phi$ -L) |
| Data type .....             | NRZ-L, -M, -S or Bi $\phi$ -L  |
| Signal level .....          | 5 volts peak-to-peak (line-to-line)                                    |
| Source coupling .....       | Balanced differential  |
| Load impedance .....        | 75 ohms  |

### 9.3.6 Square Wave Oscillator

The operational data and the LDR source are multiplexed on the Quadrature (Q) and In-phase (I) components of the 8.5-MHz square wave. The power split is 80 percent on the I channel and 20 percent on the Q channel. The square wave oscillator outputs two phases ( $0^\circ$  and  $180^\circ$ ) of the 8.5-MHz signal. Both of these signals are run through delay lines to introduce a phase delay of  $63^\circ$ . These four phases of the 8.5-MHz square wave ( $0^\circ, -63^\circ, -180^\circ, -243^\circ$ ) are provided to the multiplexer that will output one of the four phases, depending on the state of the binary I and Q channel inputs. In the PM mode of operation, this QPSK signal is routed to the quadrature input of the QPSK modulator. In the FM mode of operation, the multiplexer QPSK output is amplified, and the 8.5-MHz signal is bandpass filtered to eliminate the higher harmonics and provided as one input to the linear summer.

### 9.3.7 FM High Data Rate Channel

One of four HDR signals can be selected as the HDR input to the FM channel. The signal is amplified and lowpass filtered and output to the summer where it is linearly summed with the 8.5-MHz sine wave containing the OPS and LDR information. The summer output is input to the FM VCO (1.875 GHz) and deviates it  $\pm 17$  MHz, ( $\pm 6$  MHz OPS/LDR and  $\pm 11$  MHz HDR). This signal is output to the communications upconverter in the DEA.

### 9.3.8 PM HDR channel

The 2- to 50-Mbps HDR input to the PM channel is routed through the asymmetry corrector to remove any asymmetry from the input clock signal. Asymmetry is defined as different pulsewidths for the positive and negative going pulses of the clock signal. The asymmetry corrector uses a phase locked loop operating at twice the input clock frequency. The input and output frequency divided by 2 are compared, and when the frequencies are in lock, a control signal proportional to the phase difference is used as an error signal to synchronize the input clock to the 2x clock output. This 2x clock is used as the output clock in the convolutional encoder.

### 9.3.9 Convolutional encoder

A block diagram of the convolutional encoder is shown in Figure 9-3. The convolutional encoder is used to encode the HDR channel at a rate  $1/2$  and constraint length 7, thus converting the 2 to 50 Mbps NRZ data into 4 to 100 Mbps encoded data. The data are clocked into a 31-bit shift register at the input clock rate. The output of two modulo 2 adders is serially loaded into two 5-bit shift registers. The input to the no. 2 shift register is inverted to ensure data transitions in the output data for the case of all zeros or all ones input data. Every five clock pulses of the 1x clock, the contents of both 5-bit shift registers are parallel transferred to the 10-bit shift register. The purpose of the delay line in the 2x clock line, which serially clocks the data out of the 10-bit shift register, is to synchronize the 2x clock frequency with the delay the data experiences in its path

through the 31- and 5-bit shift registers. These 4- to 100-Mbps encoded data are fed to the I input of the QPSK modulator.

### **9.3.10 QPSK modulator**

The purpose of the QPSK modulator is to biphase modulate two identical carriers (1.875 GHz) with two independent binary data streams, orthogonally combine the modulated carriers, and amplify them. The bit rates are widely different, and the power sharing is such that the HDR channel (I) contains 80 percent of the power and the OPS/LDR channel (Q) contains 20 percent. The 1.875-GHz reference carrier from the Interface and Control Unit is split through an equal phase power divider and fed to two doubly balanced mixers for Biphase Shift Key (BPSK) modulation by the I and Q channel data. The summation of the mixer outputs is implemented by using a 6-dB quadrature coupler that furnishes the orthogonality and power imbalance.

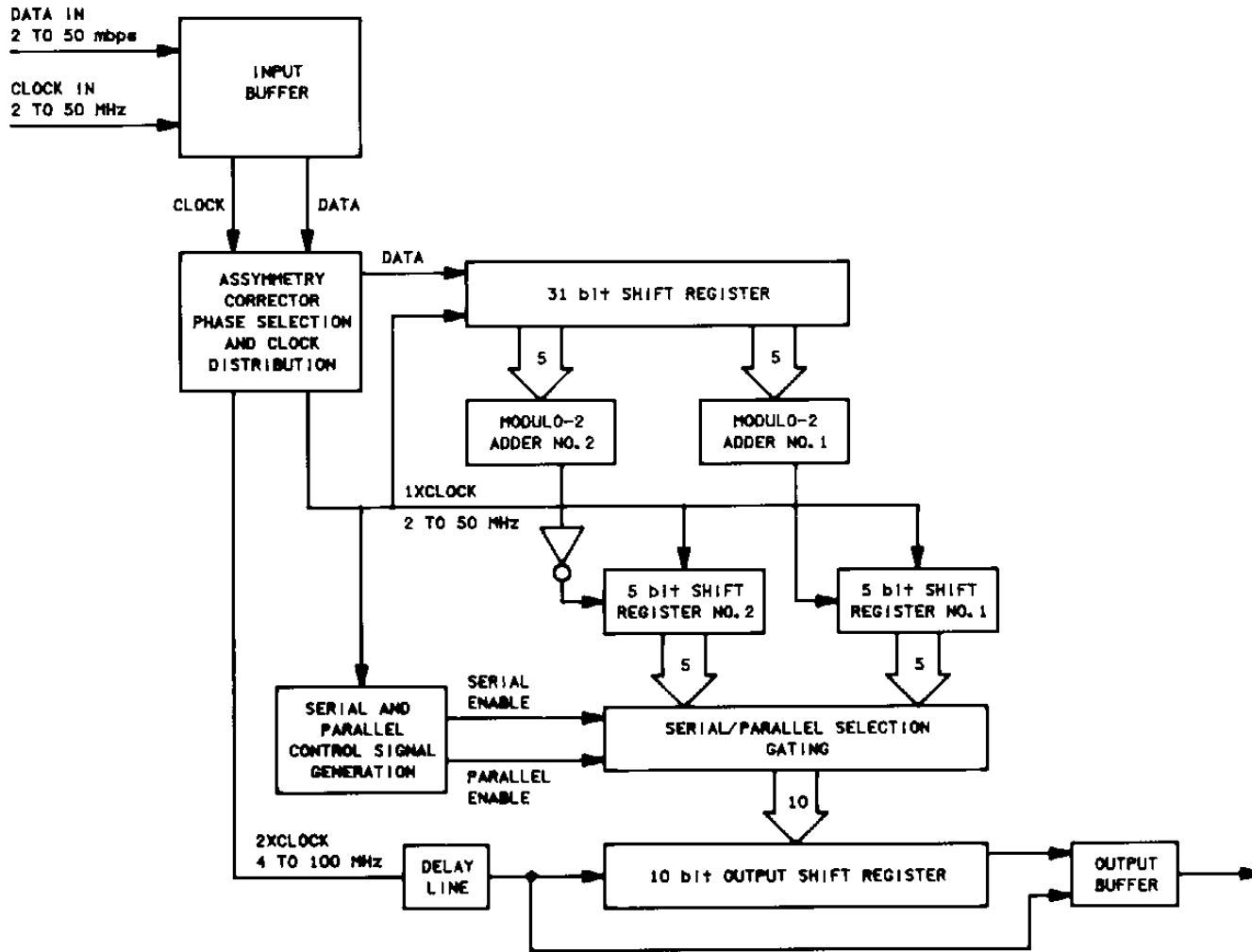


Figure 9-3. Convolutional encoder functional block diagram

### 9.3.11 SPA Internal Microprocessor

The Communications Signal Processor contains a small microprocessor to control all discrete and serial input/output signals to properly configure the SPA.

When initialized, the will SPA is configured for return link mode PL MAX with modulation ON and forward link mode 216-kbps with NSP 1 selected as the source. Immediately after initialization, the SPA is configured according to the discrete (HDR/LDR and NSP ON from LCA-2/3) and serial inputs. The microprocessor stores this configuration in memory and only changes it for allowable inputs. Allowable HDR/LDR inputs are one HIGH discrete for each data rate; therefore, configuration will not change for either all HIGH or all LOW inputs for either HDR or LDR.

Internal SPA signals are described as follows:

**Table 9-3. Internal SPA Signals**

|                   |  |
|-------------------|--|
| MODULATION ON/OFF | Applies/removes modulation from the 1.875 GHz carrier.   |
| MODE FM/PM        | Selects FM/PM mode of modulation, depending on the HDR selection. PL max selects PM mode, all others, including off, select FM mode. |
| MODE 72/216       | 72 select the throughput mode, and 216 select the path through the decommutator.   |
| FRAME SYNC        | Indicates that the frame synchronizer is locked up to the forward link 216-kbps data.  |

Signals Interfacing between EA-1 and the SPA are described in Section 9.9.4.

### 9.4 RADAR SIGNAL PROCESSOR (EA-2)

The Radar Signal Processor receives mode configuration data and provides status and control signals to EA-1. It also provides control signals and receives the 78-MHz radar second IF signal from the DEA. It processes this signal to detect, acquire, track, and extract data concerning the radar target.

The purpose of the Radar Signal Processor is to detect the presence of a target and then obtain continuous accurate estimates of the various target parameters, namely, range, range rate (velocity), azimuth and elevation angle errors, and angle rates. The target is detected when the radar is in search mode and accurate parameter estimates are derived in track mode.

The basic radar system obtains target information in an analog fashion; i.e., it derives the data from an individual pulse (as in the case of range) and from pulse to pulse (as in the case of range rate, angle rate, and angle error). The Ku-band radar system uses digital techniques to process the echo signals and forms statistical estimates of the target data (range, range rate, etc.) over numerous samples of many echo signals. In passive mode, frequency diversity is used to enhance target detection. Five different frequencies, spaced 52 MHz apart, are cycled to transmit 16 pulses at each frequency. One pulse repetition interval is idle to allow for frequency change.

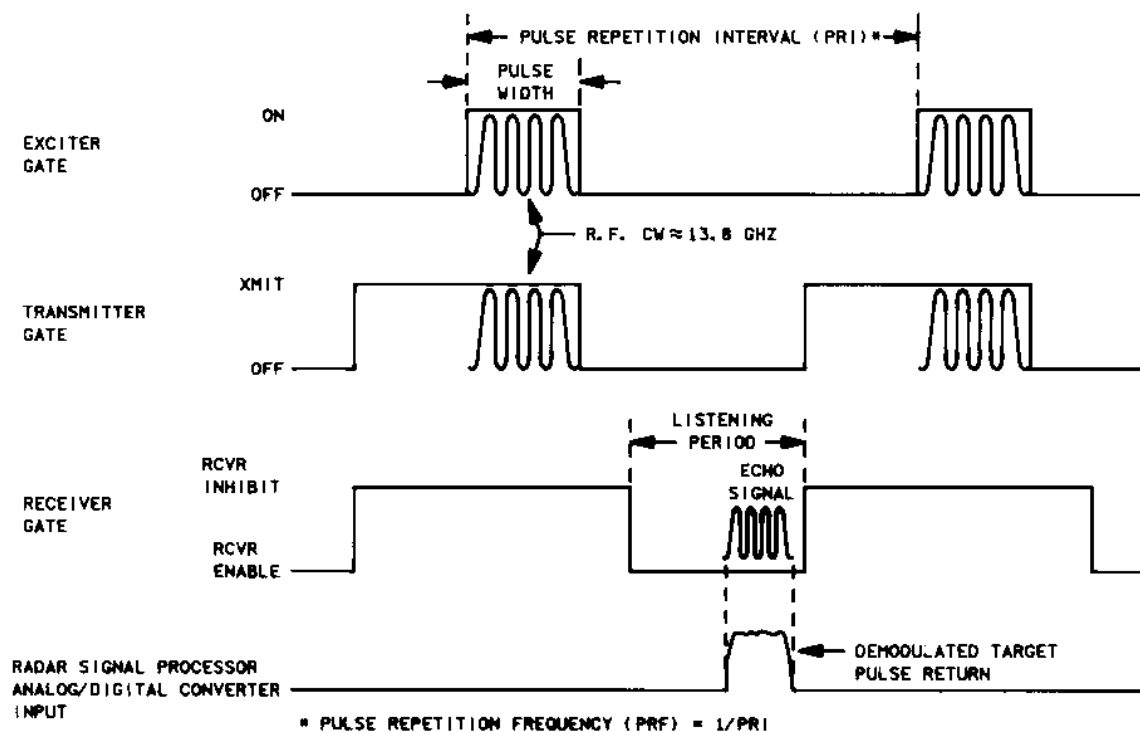
The mode interface and range correction logic and the DEA gates and processor timing modules output the transmit control signals to the DEA. A three-bit binary code is used to generate the five frequencies in the passive mode and the single frequency in the active mode. Table 9-4 shows the frequency channels selected in the exciter.

**Table 9-4. Frequency selection**

| Binary code |   |   | Channel select | Exciter output frequency - GHz | Radar mode used |
|-------------|---|---|----------------|--------------------------------|-----------------|
| A           | B | C | no.            |                                |                 |
| 1           | 0 | 0 | 1              | 13.779                         | Passive         |
| 0           | 1 | 0 | 2              | 13.831                         | Passive         |
| 1           | 1 | 0 | 3              | 13.883                         | Active/passive  |
| 0           | 0 | 1 | 4              | 13.935                         | Passive         |
| 1           | 0 | 1 | 5              | 13.987                         | Passive         |

The exciter, transmitter, and receiver gating signals are also output to the DEA to generate the transmitted pulses. Figure 9-4 shows the relationship between the gating signals.





**Figure 9-4. Pulsed continuous wave radar control signals**

In search mode, only the receiver sum channel is processed through the DEA receiver. In track mode, the antenna pointing error data (D AZ and D EL) are multiplexed on the receiver difference channel and added to the sum channel. This combined signal is mixed with the radar second LO (573 MHz) to obtain the radar second IF (78 MHz). After additional amplification and filtering, this signal is output to the Radar Signal Processor.

### 9.4.1 Analog Processor

The radar second IF received signal level is set by the AGC processor to maintain a constant level at the input to the Analog to Digital (A/D) converters. The 156-MHz reference frequency from the Interface and Control Unit is bandpass filtered and phase shifted to provide an in-phase and quadrature phase reference signal to the I and Q mixers. The baseband I and Q signals out of the mixers are lowpass filtered (14.5 MHz) to eliminate the unwanted sum product (156 MHz). Each output is filtered further by a 237 kHz lowpass filter in the low sample mode (482-kHz sample rate), or a 4 MHz lowpass filter in the high sample mode (8.2-MHz sample rate). The high sample mode is only used for ranges less than 0.42 n. mi. The I and Q signals are then A/D converted (4 bit) and sent to the preprocessor.

### 9.4.2 Digital preprocessor

In short range search mode (less than 0.42 n. mi.) the I and Q samples are individually summed and evaluated so that if the I or Q signal (or both) exceeds the Constant False

Alarm Ratio (CFAR) threshold, a single pulse hit is declared. At longer ranges, two overlapping range gates (when range is designated) or four butted range gates (when range is not designated) are used to sum and multiplex the I and Q data into 8-bit bytes which are output to the filter processor. In track mode, two butted range gates (an early gate and a late gate) are used to process the I and Q data.

#### 9.4.3 Filter processor

The filter processor receives the sequential I and Q data from the preprocessor, stores these data, filters them, and outputs them to the magnitude detector. In search mode, 16 Doppler filters, covering a range of velocities from 0 to 150 ft/s closing and 0 to 75 ft/s opening, are equally spaced over one pulse repetition interval. In track mode, the velocity processor will select five Doppler filters, spaced by the pulse repetition frequency over 32 (PRF/32), with the target Doppler normally positioned in the middle filter. The Doppler filters are used to enhance the signal-to-noise ratio in search mode and to determine the Doppler frequency, therefore, range rate, in track mode. The data out of all Doppler filters will be processed by the postdetection integrator and log converter for output to the target detector and AGC processor. However, only the outputs of three Doppler filters are processed by the discriminant generator; i.e., the filter whose center frequency is closest to the actual Doppler frequency and the filters on either side of it. These outputs are used to calculate initial estimates of range, range rate, and azimuth and elevation angles for the velocity, range, and angle processors in search mode and to update these estimates with the error signals in track mode.

#### 9.4.4 Magnitude Detector

The purpose of the magnitude detector is to determine the magnitude of the I, Q vector, that is,  $\text{magnitude} = (I^2 + Q^2)^{1/2}$ . An approximation of this relationship is used to determine the vector magnitude. The I, Q vector is rotated until it is aligned with the I axis. This is done by calculating the I, Q vector angle  $q = \text{Tan}^{-1} Q/I$ . Then the I, Q vector magnitude =  $I \cos q + Q \sin q$ . This is output in 8 bits to the postdetection integrator.

#### 9.4.5 Postdetection Integrator

The function of the postdetection integrator is to coherently accumulate the magnitude detector output data prior to further processing; i.e., range bin/early-late gate, Doppler filter number, time slot (AZ/EL) for each transmitted frequency. These data are then output to the log converter.

#### 9.4.6 Log Converter

The log converter converts the 16-bit input data to 8 bits (3-bit characteristic and 5-bit mantissa). The 16 bits are shifted up until the most significant bit is a 1; this determines the characteristic. Then the seven less significant bits are converted to the mantissa.

#### 9.4.7 Target Detect

The main function of the target detect circuit is to detect that a target signal is present. It does this by comparing each range bin, Doppler filter output to the mean signal level of all range bins and all Doppler filters. If it detects a target hit, it outputs which Doppler filter it is in to the velocity processor. A second function is to detect an antenna sidelobe hit. It does this by comparing the sum antenna data with data acquired through the wide-beam horn antenna. A third function is to detect a target hit in the "fixed threshold" mode. It compares the data to a preset threshold rather than the mean signal level to determine a target hit.

#### 9.4.8 Automatic Gain Control Processor

The function of the AGC processor is to maintain the radar signal level within the dynamic range of the A/D converter. It does this by measuring the signal to noise ratio, converting it to an analog voltage, and sending three attenuator control signals to the receiver in the DEA. The "XMIT LMTR" and "step if" controls introduce 30 dB of attenuation each in the receiver; the "linear" control introduces a variable attenuation of 0 to 40 dB in the receiver. When tracking a target, the TWT bypass control will reduce the transmitted power (about 40 dB) and, therefore, the received power at short range (about 640 feet). An additional 20 dB of attenuation is provided in the analog processor. A measure of the received signal strength is output to the Interface and Control Unit for onboard displays and downlink telemetry. It is the difference between the last noise AGC measured in search and the track AGC.

#### 9.4.9 Discriminant Generator

The purpose of the discriminant generator is to obtain an estimate of the error signal (including sign) of the radar parameters being measured; i.e., range, range rate (velocity), angles, and angle rates. This is accomplished by taking the difference of the logarithms of the outputs of the appropriate Doppler filters for a given parameter to form an estimate of that parameter. The range discriminant is generated by accumulating the early and late gate outputs for the center Doppler filter for the five frequencies. The angle discriminant is obtained in the same fashion as range; however, the D AZ and D EL signals will be combined separately. The range rate discriminant is generated by accumulating the early and late gate outputs for the adjacent Doppler filters (next higher/lower from the center) for the five frequencies.

#### 9.4.10 Angle Processor

The azimuth/elevation error estimates out of the discriminant generator are fed into the azimuth/elevation loop filters in the angle processor. The loop filters output two sets of estimates: the a/b error estimates, which are used to drive the antenna servos, and AZ/EL angle rate estimates, which are sent to the Interface and Control Unit for output to the crosspointer display (panel A2) and downlinked to the ground.

#### 9.4.11 Range Processor

The range processor contains a tracking circuit called the a/b tracker. Its function is to provide a smoothed estimate of the current range for onboard display and downlink. It also provides a predicted estimate of the next range for properly positioning the early and late range gates. The designated range, in GPC and GPC designate modes, is used to set the initial conditions.

#### 9.4.12 Velocity Processor

The velocity processor initially selects the Doppler filter containing the return signal and the two adjacent filters for generating the range rate discriminant. It also contains circuitry to resolve the ambiguous Doppler by comparison with a smoothed estimate of the range rate provided by the range processor. This smoothed estimate of range rate is also output to the onboard displays and downlinked. After resolving the range rate ambiguity, it predicts a new Doppler estimate which is used to select the Doppler filter containing the target return.

#### 9.4.13 Low Voltage Power Supply

There are four Low Voltage Power Supplies (LVPS) in the Ku-band system. These power supplies accept unregulated 28 V dc and condition it to furnish regulated voltage forms to the DEA, the Interface and Control Unit, and the radar and comm signal processors.

The steady-state dc input voltage is  $28 + 4$  V. Regulation of the output voltage is 5 percent of the nominal value. Maximum ripple voltage is within 1 percent of each voltage peak-to-peak. The four power supplies are similar, the main differences being variations in their output voltages and current.

##### A. Line filters

The line filter consists of a two-section L-C filter. This filter is required to keep 28-V bus noise and ripple out of the power supply and, conversely, to keep power supply generated noise and ripple from being put back on the 28-V power bus.

##### B. Undervoltage protection

The undervoltage protection circuit turns off the linear regulator and, hence, the power supply when the input voltage (28 V dc) drops below  $20 + 0.5$  V dc. It automatically turns the power supply back on when the input voltage returns to  $22 + 0.5$  V dc if the LVPS ON command is present.

##### C. Linear regulator

The linear regulator provides a constant voltage to the converter despite input line variation; the output voltage is approximately 21 V dc. The linear regulator consists of a series pass stage transistor controlled by a high gain feedback network by means of an

error amplifier and a temperature-compensated zener for reference voltage. The linear regulator does not sense the 21 V dc bus directly for regulation but senses the voltage developed from an auxiliary winding from the converter. This sensing arrangement provides better regulation for output voltage of the converter. The linear regulator has current limiting. If a short is present on the output of the regulator, either between the regulator and the converter or at the output of the converter, the +21 V dc begins to drop. When voltage drops below 20 V dc, the converter is turned off. When the short is removed, the converter remains off. To start the converter again, the ON command must be removed and reapplied.

#### D. Overvoltage protection

The overvoltage protection circuit turns off the converter if the 21 V dc bus increases to 24 V dc. If the overvoltage condition is cleared, the converter will remain off. To restart it, the ON command must be removed and reapplied. As an example of how this sequence could occur, assume that the pass stage of the linear regulator failed short-circuited. The converter then shuts off because of the resulting overvoltage. The output voltage is, therefore, prevented from applying an overvoltage condition to the loads.

#### E. Dc-dc converter

A dc-dc converter provides the various output voltages for the LVPS. Each output is obtained through a separate secondary winding of the converter transformer. The voltage is then rectified and filtered by an LC network. The converter is a standard two-transformer design with the output transformer nonsaturating. It runs at a frequency of approximately 20 kHz. It is started by a 100-ms start pulse that is provided only when the ON command is first applied or when the undervoltage protection circuit has recovered from a low line condition.

### 9.5 RADAR OPERATIONS

The basic oscillator frequency of the Radar Signal Processor is 49.17856 MHz. The period, which is designated  $\tau$  (tau), is equal to  $1/49.17856 = 20.334$  nanoseconds. The distance to a target and return during this time interval is

$$\begin{aligned} D &= c\tau = (9.843 \times 10^8) (20.334 \times 10^{-9}) \\ & \qquad c = 9.843 \times 10^8 \text{ ft/sec [ speed of light ]} \\ & \qquad \tau = 20.334 \times 10^{-9} \text{ sec} \\ &= 20 \text{ ft} \end{aligned}$$

Range to a target is then

$$R = D/2 = 20/2 = 10 \text{ ft}$$

The radar transmitted pulsewidth is a function of target range, antenna steering mode, radar mode (active/passive) and whether in search or track. The target return (echo signal) is sampled at a high rate (8.2 MHz) for ranges less than 2550 feet and at a low rate (482 kHz) for ranges greater than 2550 feet. These data are stored in range bins (storage buffers), the number and arrangement of which depend on range, antenna and radar modes, and whether in search or track.

The maximum unambiguous range which can be determined for the various PRFs is

- Radar passive

$$R_{3\text{KHz}} = c/2 (\text{PRF})$$

$$= 9.843 \times 10^8 / 2(3,000) \times 1/6063$$

$$= 27 \text{ n. mi.} \qquad 1 \text{ n. mi.} = 6063 \text{ ft}$$

$$R_{7\text{KHz}} = 11.6 \text{ n. mi.}$$

$$R_{15\text{KHz}} = 5.4 \text{ n. mi.}$$

- Radar cooperative

$$R_{268 \text{ Hz}} = 303 \text{ n. mi.}$$

A. Search mode

1. Transmitted pulses

The transmitted pulse template consists of 17 pulse repetition intervals. One pulse is transmitted during each of the first 16 intervals and the 17th interval is used to change frequency. This template is as follows:

|         |     |     |     |    |        |     |     |     |     |
|---------|-----|-----|-----|----|--------|-----|-----|-----|-----|
| PULSE # | 1   | 2   | 3   | 4  | 15     | 16  | 1   | 2   | 3   |
|         | --- | --- | --- | -/ | /- --- | --- | FC- | --- | --- |
| PRI     | 1   | 2   | 3   |    | 15     | 16  | 17  | 1   | 2   |

For AUTO TRACK and MANUAL SLEW antenna steering modes, the transmitted pulse template is as follows, with the 17th interval consisting of a frequency change and three pulses at a PRF of 15 kHz, (A = TWT bypass power, B = low power and C = medium power) for search ranges less than 1 mile. The remaining 16 intervals will consist of one pulse/interval at a PRF of 3 kHz and a power level as selected on the D&C panel and will be used to search out to the maximum range of 27 miles.

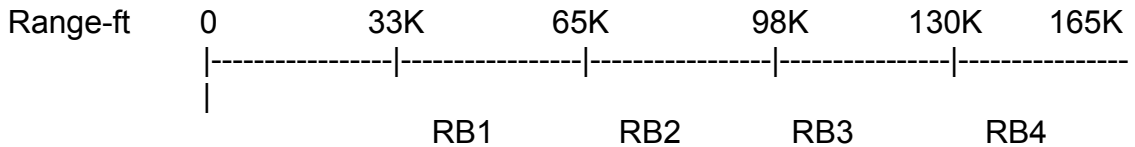
|                  |                    |        |        |        |                   |       |
|------------------|--------------------|--------|--------|--------|-------------------|-------|
| PULSE #          |                    | A      | B      | C      | 1                 | 2     |
|                  | --- FC ---         | -----  | -----  | -----  | -----             | ----- |
| TIME - $\mu$ sec | --- 132 ---        | - 66 - | - 66 - | - 66 - | ----- 330 -----   |       |
|                  | -----PRI # 17----- |        |        |        | -----PRI # 1----- |       |





4. Range bins - AUTO TRACK/MANUAL SLEW

The Radar Signal Processor forms four butted range bins to search over the entire 27-mile range interval when in radar passive mode and autotrack or manual antenna steering modes.



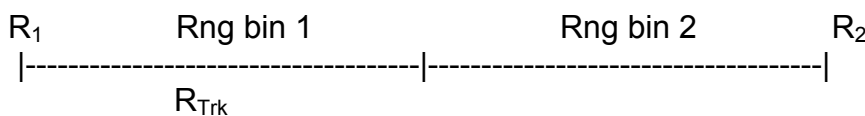
**Table 9-5. GPC mode operating data**

| Target range - ft | Range desig    | Power mode*     | PRF KHz | Search     |                       |                       |                  | Track       |                    |
|-------------------|----------------|-----------------|---------|------------|-----------------------|-----------------------|------------------|-------------|--------------------|
|                   |                |                 |         | PW**<br>μs | R <sub>1</sub><br>ft  | R <sub>2</sub><br>ft  | Rng bin width ft | PW***<br>μs | 2 rng bin width ft |
| - 2550            | -              | var             | 7       | 0.122      | 120                   | 5660                  | 4140             | 0.122       | 120                |
| 2560 - 3830       | 3840           | Low             | 7       | 4.15       | 2820                  | 6900                  | 3060             | 2.075       | 2040               |
| 3840 - 5750       | R <sub>D</sub> | Low             | 7       | 4.15       | R <sub>D</sub> -1020  | R <sub>D</sub> +3060  | 3060             | 2.075       | 2040               |
| 5760 - 6390       | 6400           | Me <sub>D</sub> | 7       | 8.3        | 4360                  | 12520                 | 6120             | 4.15        | 4080               |
| 6400 - 11510      | R <sub>D</sub> | Me <sub>D</sub> | 7       | 8.3        | R <sub>D</sub> -2040  | R <sub>D</sub> +6120  | 6120             | 4.15        | 4080               |
| 11520 - 13430     | 13440          | High            | 7       | 16.6       | 9360                  | 25680                 | 12240            | 8.3         | 8160               |
| 13440 - 23030     | R <sub>D</sub> | High            | 7       | 16.6       | R <sub>D</sub> -4080  | R <sub>D</sub> +12240 | 12240            | 8.3         | 8160               |
| 23040 - 25590     | 25600          | High            | 7       | 33.2       | 17440                 | 50080                 | 24480            | 16.6        | 16320              |
| 25600 - 43510     | R <sub>D</sub> | High            | 7       | 33.2       | R <sub>D</sub> -8160  | R <sub>D</sub> +24480 | 24480            | 16.6        | 16320              |
| 43520 - 49910     | 49920          | High            | 3       | 66.4       | 33600                 | 98880                 | 48960            | 33.2        | 32640              |
| 49920 -           | RD             | High            | 3       | 66.4       | R <sub>D</sub> -16320 | R <sub>D</sub> +48960 | 48960            | 33.2        | 32640              |

\*Power output switch on panel A1U will limit power if not in high.  
\*\*This is the radar pulsewidth during search.  
\*\*\*This is the radar pulsewidth during track.

B. Track mode

In track mode, for all antenna steering and radar modes, the Radar Signal Processor forms two butted range bins, each equal to the transmitted pulsewidth. The range bins will be adjusted to maintain the echo signal in the center of the butted range bins. The transmitted power level will be maintained at the panel switch level (high/medium/low) until the actual range is equal to or less than 640 feet, at which time bypass power will automatically be selected.



$R_{Trk}$  is the range from the range tracker and is normally positioned in range bin 1.



### 9.5.1 Ku-Band RF Output Power and Acquisition Range

For nominal Ku-band radar operation the LDEF should be acquired at 100K feet (16.5 n. mi.). During a rendezvous sim the RF output was reduced from a nominal telemetry indication of 27 to 11 W. The expected radar range can be calculated by using the Signal to Noise Ratio (SNR) equation below.

$$SNR = \frac{P_T G^2 \lambda^2 \delta}{(4\pi)^3 R^4 K_B L_T B} \cdot \frac{G}{T}$$

- P<sub>T</sub> = Transmitted power
- G = Antenna gain
- λ = Wavelength
- δ = Target size (radar cross section)
- R = Range to the target
- K<sub>B</sub> = Boltzman's constant
- L<sub>T</sub> = Ku-band system transmission loss
- B = Receiver bandwidth
- T = Receive system temperature

The equation can be simplified:

$$SNR = \frac{P_T}{R^4} \cdot K_c \quad \text{and} \quad K_c = \frac{G^2 \lambda^2 \delta}{(4\pi)^3 K_B L_T B T}$$

It can be seen that SNR varies directly as the Transmitted Power (PT) and inversely as the fourth power of the Range (R).

For the simulator problem the SNR must be the same, so the expected range for the reduced RF output power can be determined as follows:

$$\begin{aligned} SNR &= \frac{P_1}{R_1^4} \cdot K_c = \frac{P_2}{R_2^4} \cdot K_c \quad \text{and} \\ &= \frac{P_1}{R_1^4} = \frac{P_2}{R_2^4} \end{aligned}$$

Rearranging,

$$\frac{P_1}{P_2} = \frac{R_1^4}{R_2^4} = \frac{1}{(R_2 / R_1)^4} \quad \text{or} \quad R_2 = \sqrt[4]{\frac{R_1^4}{P_1 / P_2}}$$

New range (R2) is expressed is as a fraction of the old range (R1) and is shown in Table 9-6 and plotted in Figure 9-5.

Example: P1 = 27 W                      R1 = 100,000 ft  
           P2 = 11 W                      R2 = ?  
           P1/P2 = 27/11 = 2.45

From Figure 9-5, a P1/P2 power ratio of 2.45 corresponds to an R2/R1 range ratio of 0.8. Using the relationship:

$$\begin{aligned} R_2 &= 0.8R_1 \\ &= 0.8 (100,000) \\ &= 80,000 \text{ ft} \end{aligned}$$

and the expected acquisition range would be 80,000 feet. This can be verified using the ratio equation to find R<sub>2</sub>.

**Table 9-6. Ratio of power versus range**

| P <sub>1</sub> /P <sub>2</sub> | R <sub>2</sub> /R <sub>1</sub> |
|--------------------------------|--------------------------------|
| 1                              | 1                              |
| 1.05                           | 0.987877                       |
| 1.08                           | 0.980944                       |
| 1.15                           | 0.965663                       |
| 1.30                           | 0.936514                       |
| 1.50                           | 0.903602                       |
| 1.75                           | 0.869442                       |
| 2.0                            | 0.840896                       |
| 3.0                            | 0.759836                       |
| 4.0                            | 0.707107                       |
| 5.0                            | 0.66874                        |
| 6.0                            | 0.638943                       |
| 7.0                            | 0.614788                       |
| 8.0                            | 0.594604                       |
| 9.0                            | 0.57735                        |
| 10.0                           | 0.562341                       |
| 11.0                           | 0.5491                         |
| 12.0                           | 0.537285                       |
| 13.0                           | 0.52664                        |
| 14.0                           | 0.516973                       |
| 15.0                           | 0.508133                       |
| 16.0                           | 0.5000                         |
| 17.0                           | 0.492479                       |
| 18.0                           | 0.485492                       |

**Table 9-6. Ratio of power versus range (concluded)**

| <b>P<sub>1</sub>/P<sub>2</sub></b> | <b>R<sub>2</sub>/R<sub>1</sub></b> |
|------------------------------------|------------------------------------|
| 19.0                               | 0.478974                           |
| 20.0                               | 0.472871                           |
| 21.0                               | 0.467138                           |
| 22.0                               | 0.461737                           |
| 23.0                               | 0.456634                           |
| 24.0                               | 0.451801                           |
| 25.0                               | 0.447214                           |

### 9.5.2 Ku-band Radiated Field

The Ku-band radiated field has been analyzed and documented in Rockwell report STS 82-0473. This report concludes that the Ku-band antenna radiated field is the equivalent of a 20-dB Taylor aperture. The boresight radiation for this type of antenna is a maximum at 3 meters, falling to a minimum at 5 meters, then increasing to a maximum again at 9 meters, which occurs in the near field of the antenna. The boresight radiation that observes the 1/R<sup>2</sup> law in the far field (beyond 84 meters) closely approximates it in the range from 9 to 84 meters.

#### A. Flux density

The flux density is an indication of signal intensity and varies inversely as the range from the antenna squared.

$$W = PG / 4\pi R^2$$

where

W = Flux density (watts/meter<sup>2</sup>)

P = Transmitted power (watts)

G = Antenna gain (ratio)

R = Range (meters)

#### B. Field intensity

The field intensity is an indication of signal potential and varies inversely as the range.

$$E = (120\pi W)^{1/2}$$

where

E = Field intensity (volts/meter)

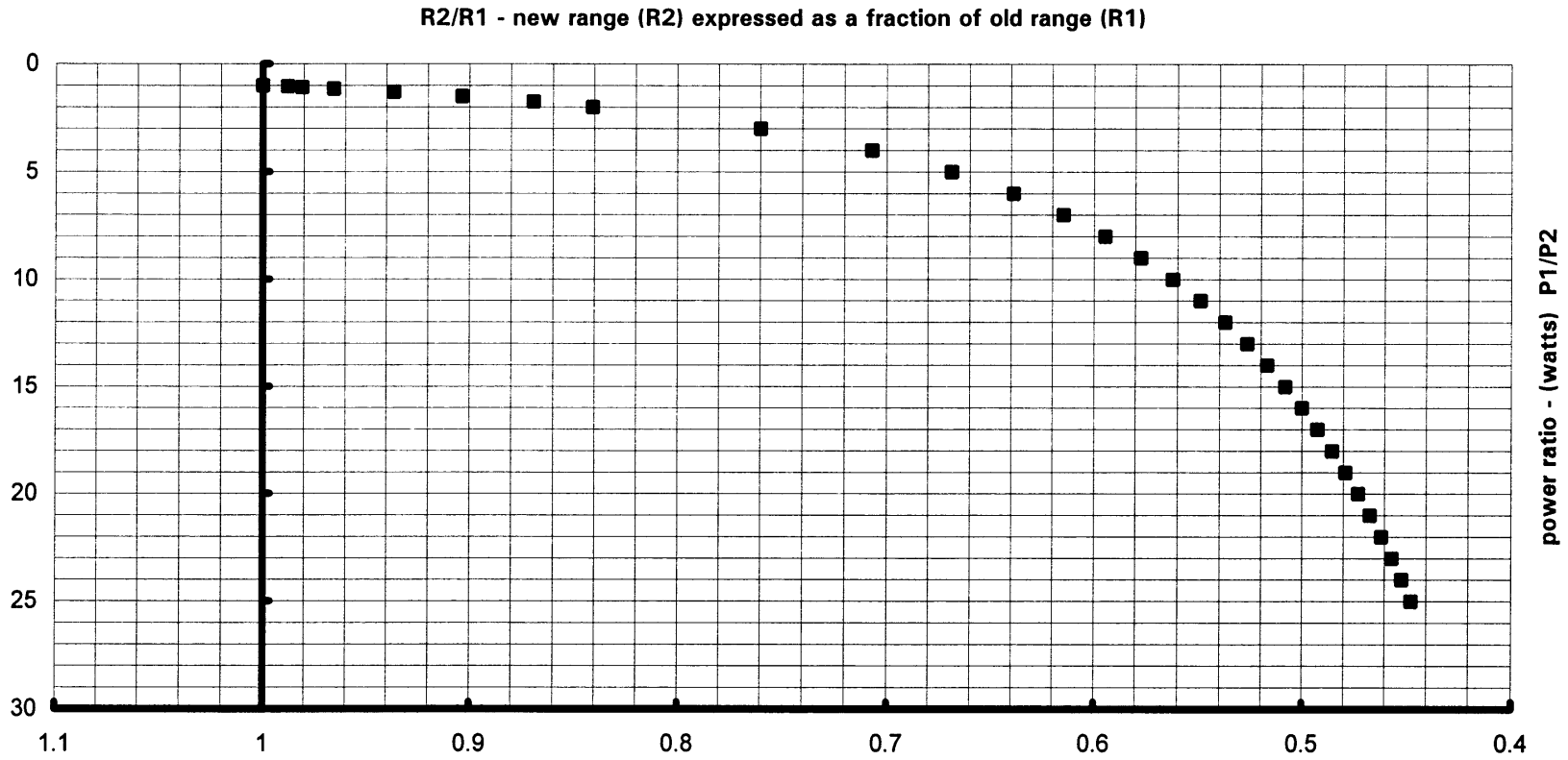


Figure 9-5. Plot of the ratio range versus power

C. Duty factor

The radar duty factor is equal to the pulse repetition frequency times the pulsewidth.

$$DF = PRF \cdot PW$$

where

PRF = Pulse repetition frequency (cycles/second)

PW = Pulsewidth (seconds)

D. Average power

The average power can be determined by multiplying the peak power by the radar duty factor.

$$P_{avg} = P_{pk} DF$$

where

Ppk = Peak transmitted power (watts)

DF = Duty factor (ratio)

E. Transmission characteristics

|                   | <b>Comm</b> | <b>Radar</b> |
|-------------------|-------------|--------------|
| Transmission loss | 2.95 dB     | 3.5 dB       |
| Antenna gain      | 39.4 dB     | 38.9 dB      |

| <b>RF output power</b> | <b>TWT/exciter* output, watts</b> | <b>Antenna input, watts</b> |
|------------------------|-----------------------------------|-----------------------------|
| Comm                   | 50.0                              | 25.41                       |
| Radar                  |                                   |                             |
| High                   | 50.0                              | 22.39                       |
| Medium                 | 3.15                              | 1.4                         |
| Low                    | 0.199                             | 0.09                        |
| Bypass*                | 0.0071                            | 0.0032                      |

Figure 9-6 is a plot of peak field intensity versus range for the comm and various radar modes. These curves were derived from the previously mentioned report and similar curves generated by A. Rueben's (JSC). The data on the curves can be verified using the nominal transmission characteristics in conjunction with the specific formulas for determining flux density and field intensity.

### 9.5.3 Operations in Ku-Band Radar Mode with ISS

From STS-108, a test was performed to determine the distance Ku-Band would "drop lock" in Radar mode Low Power operations while undocking with the ISS. The test

concluded with ISS in an STS-108 assembly stage, Shuttle Ku-Band Radar kept lock until 8000ft. (Notice, RF Power Level does not select the EA-2 Range Bins.)

As a **general rule** for Ku-Band Radar in Low Power, use the following equation to determine distance until the "Signal to Noise" ration < 3db.

SNR pd 99% = Ku-Band RF Out - Low Power attenuation + 10 log (Radar Cross Section ft<sup>2</sup>) dbm - 40 log (Range ft) dbm

3dbm = 175.45dbm - 24dbm + 10 log (2000ft<sup>2</sup>) dbm - 40 log (Range ft) dbm

-181 dbm = -40 log (Range ft) dbm

~ 34,000 ft = Range ft (to lock on ISS (STS-113 config)) in Low Power

## 9.6 MECHANICAL CONVERSIONS

### 9.6.1 Azimuth-Elevation

The +X axis is aligned with the orbiter vehicle longitudinal axis forward. The +Y axis is aligned nominally with the orbiter right wing so that the X-Y plane is parallel to the vehicle lateral plane. The +Z axis is directed downward to complete a right-handed set.

Orientation of the antenna Line of Sight (LOS) in the XYZ system is defined by an azimuth-elevation Euler angle sequence, starting with the LOS initially aligned with the Z axis. In this azimuth-elevation sequence, azimuth occurs first, followed by elevation. A positive azimuth angle moves the LOS toward the vehicle left wing. A positive elevation angle moves the LOS toward the vehicle nose. A given orientation of the LOS, to any direction within the sphere, is defined by an azimuth angle between +180° and an elevation angle between +90°. Slewing motions are shown in Figure 9-7.

### 9.6.2 a-b Coordinate System

The a-b coordinate system XAYAZA is defined in Figure 9-8. The azimuth-elevation (XYZ) coordinate system is also included for reference (Figure 9-8). The XAYAZA system is generated from the XoYoZo system by a single rotation through an angle of 67° about the -Z axis, so the XA - YA plane is parallel to the X-Y plane, and the -ZA axis is aligned with the -Z axis. The a-b coordinate system is a right-handed system, so positive a motion is toward the orbiter right wing and positive b motion is toward the payload bay. This is the same as the orbiter roll and pitch motion if the orbiter is yawed +67°.

### 9.6.3 Coordinate Conversion Equations

The coordinate transformation between the roll-pitch coordinate and a - b coordinate shall be as shown on Table 9-7.

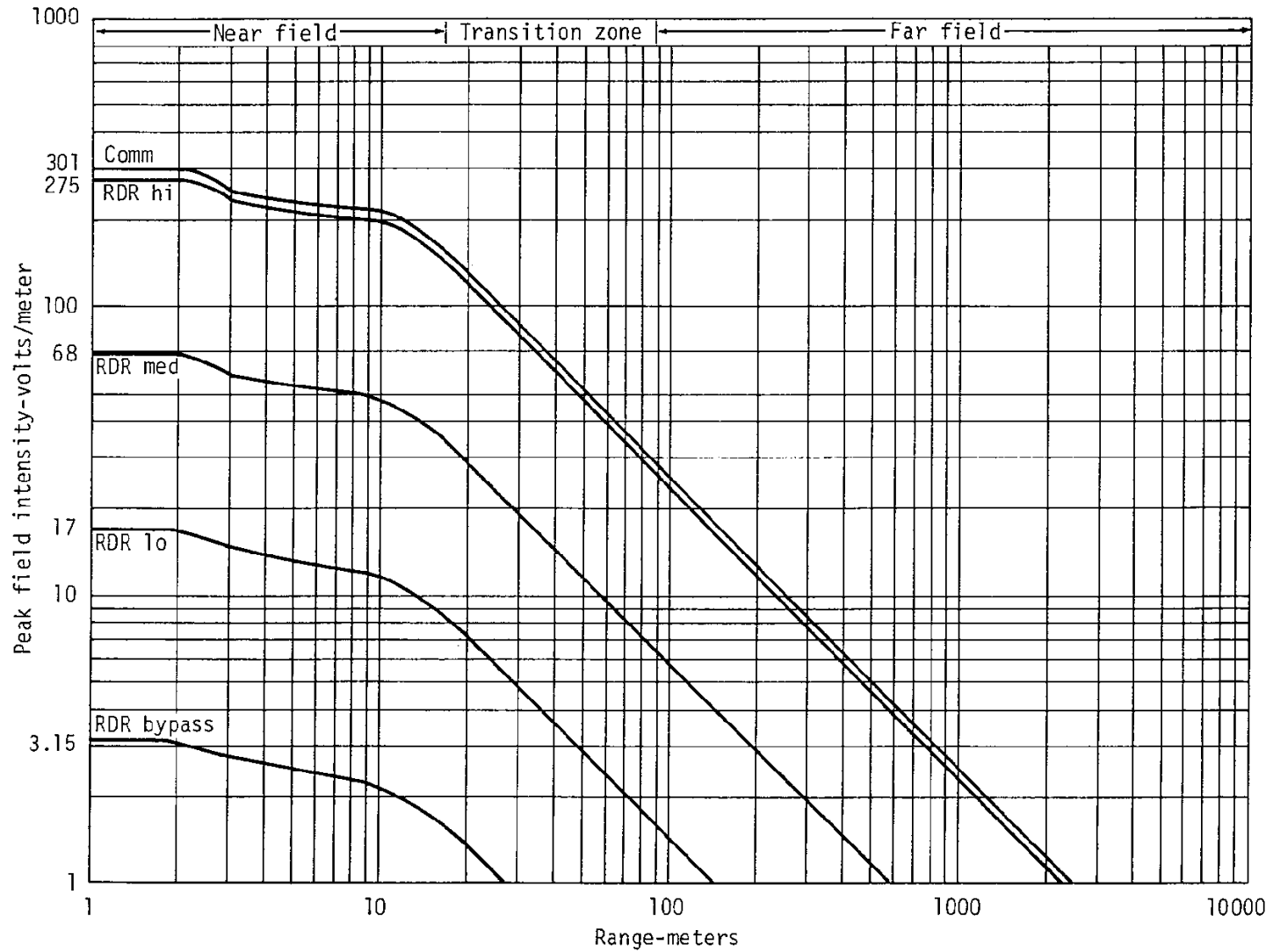
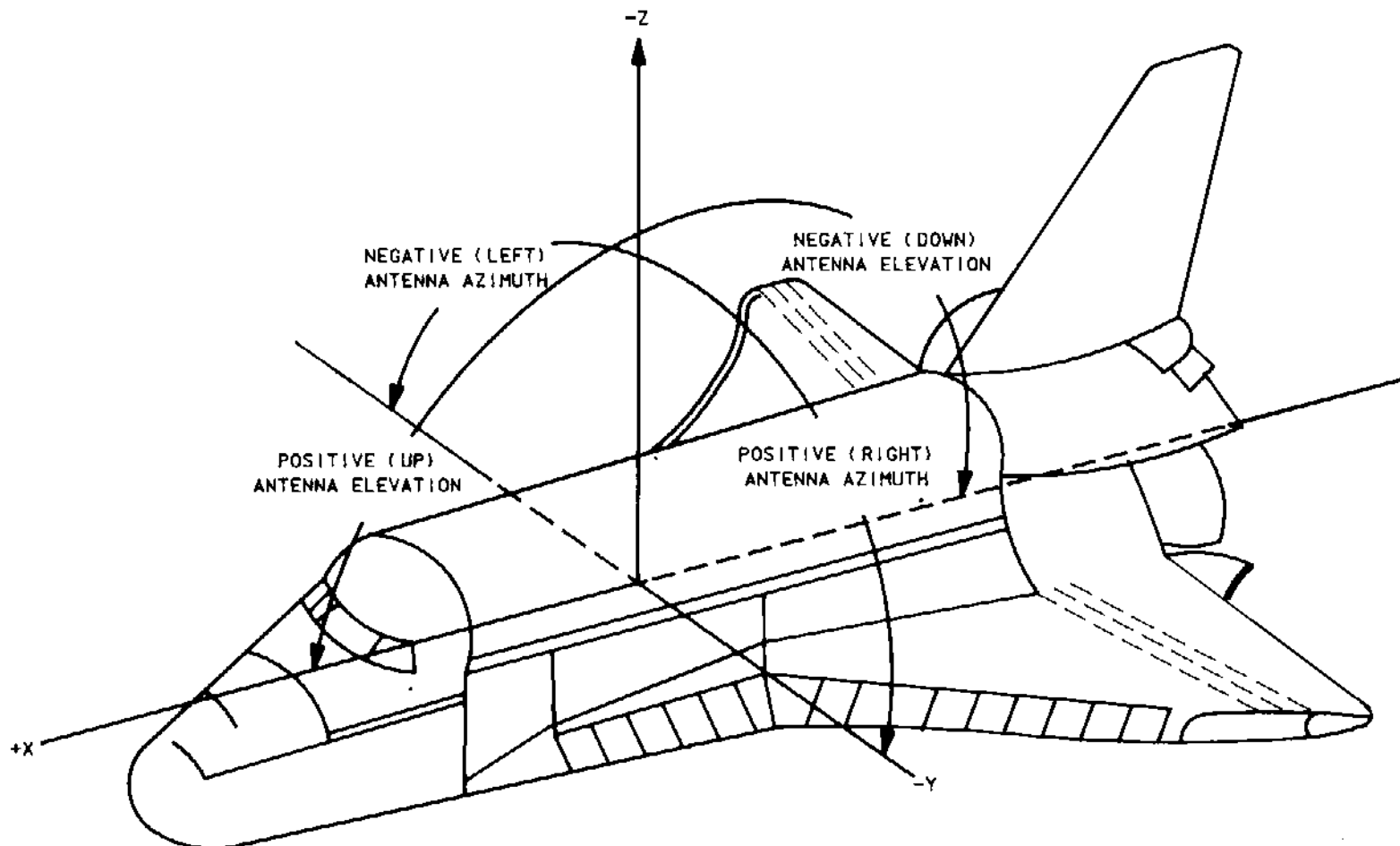


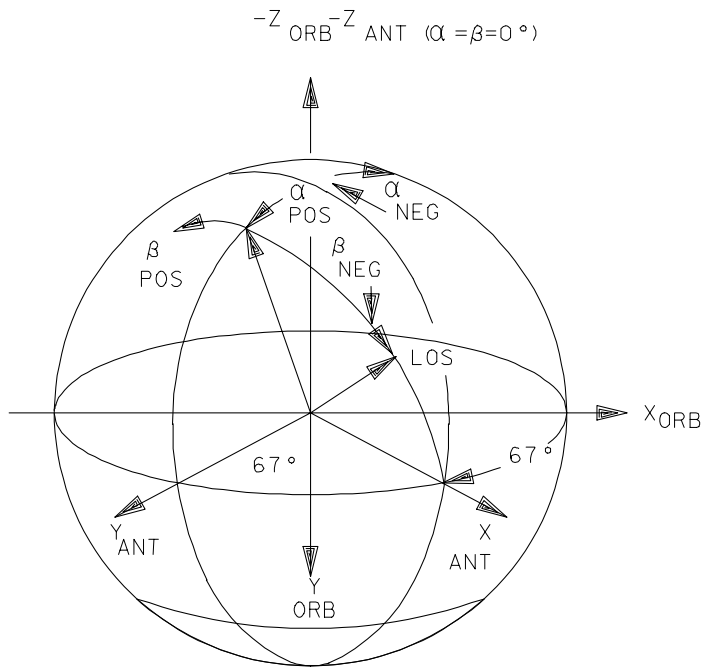
Figure 9-6. Ku-band peak field intensity versus range

NOTE  
ZERO ELEVATION AND ZERO AZIMUTH  
OCCUR ALONG THE -Z AXIS

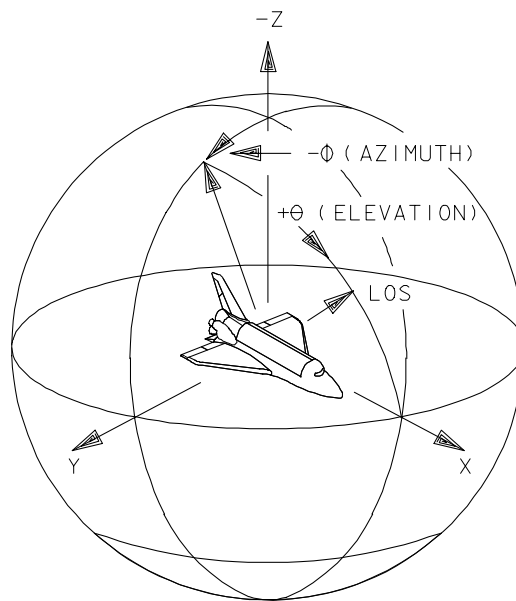


**Figure 9-7. Orbiter vehicle coordinate system and slewing directions**





(a.) ALPHA-BETA



(b.) AZIMUTH-ELEVATION

186111811.BPT; 2

**Figure 9-8. Coordinate system**

*Table 9-7. Coordinate conversions*

**Orbiter-to-gimbal angles**

$$\sin \beta = -\cos \psi \sin EL + \sin \psi \sin AZ \cos EL$$

$$\sin \alpha = \frac{-\cos \psi \sin AZ \cos EL - \sin \psi \sin EL}{\cos \beta}$$

**Gimbal-to-orbiter angles**

$$\sin EL = -\cos \psi \sin \beta - \sin \psi \sin \alpha \cos \beta$$

$$\sin AZ = \frac{-\cos \psi \sin \alpha \cos \beta + \sin \psi \sin \beta}{\cos EL}$$

**LOS rates for display**

$$\omega_A = \omega_\alpha (-\cos \Psi \cos \beta + \sin \Psi \sin \alpha \sin \beta) + \omega_\beta \sin \Psi \cos \alpha$$

$$\omega_E = -\omega_\alpha (\sin \Psi \cos \beta + \cos \Psi \sin \alpha \sin \beta) - \omega_\beta \cos \Psi \cos \alpha$$

**Definition of symbols**

$\alpha$  = Alpha gimbal angle

$\beta$  = Beta gimbal angle

$\Psi$  = 67° antenna boom offset in the orbiter yaw plane

EL = Elevation angle

AZ = Azimuth angle

$\omega_\alpha$  = Alpha line of sight angle rate

$\omega_\beta$  = Beta line of sight angle rate

$\omega_A$  = Azimuth line of sight angle rate

$\omega_E$  = Elevation line of sight angle rate

## 9.7 DEPLOYED ELECTRONICS ASSEMBLY (DEA)

The DEA houses the RF circuits of the system and provides for transmission and reception of RF signals in either Communications or Radar Mode and also provides circuitry for performing self-test in radar mode only. The major units in the DEA are

- Exciter
- Transmitter
- Microwave assembly
- Receiver
- Low voltage power supply

### 9.7.1 Deployed Electronics Assembly Overview

The DEA is mechanized to operate in either Comm or Radar Mode, and two radar submodes, active or passive. During Radar or Comm, upon receipt of the STANDBY or ON commands the DEA logic within the transmitter subassembly issues a Low Voltage Power Supply (LVPS) enable command to the LVPS, turning on all DEA dc power and enabling the LVPS fault sensing circuits. The transmitter logic also enables the transmitter high voltage, TWT filament, and TWT modulating anode power supplies and initiates a 3.5-minute TWT filament warmup period, during which the TWT modulating anode is inhibited.

#### 9.7.1.1 Exciter Overview

During Radar Mode, the 156-MHz reference signal, received from the EA-1, is power divided in the exciter subassembly and upconverted to the Ku-band first Local Oscillator (LO) signal by means of a harmonic phase comparator loop and Ku-band Gunn VCO. This first LO is mixed with the first IF offset frequency of 651 MHz to further upconvert it to the transmitter TWT drive signal. A sample of the first LO is also fed to the receiver subassembly for receive signal downconversion.

The TWT drive amplitude ripple and power levels are controlled, respectively, by a limiting amplifier and an absorptive modulator. The limiting amplifier provides amplitude gain compression on the order of 3, with a resulting output level of +7 dBm in full power mode. This output power level is controlled by means of the radar power low and medium signals to effect 12-dB and 24-dB reduced DEA power output levels from full power by reduction of the TWT drive level. An even lower reduced power output level mode, termed TWT bypass, is also available; as the name implies, this mode bypasses the transmitter TWT entirely and transmits the TWT drive signal. This mode is selected automatically when tracking a target at ranges less than 640 feet.

Frequency agility is provided for in Radar Mode by means of five discrete selectable channels between 13.779 and 13.987 GHz with channel separations of 52 MHz during

the passive target submode. With an active target, radar channel number 3 (13.883 GHz) is commanded only. With passive or active targets in radar mode, the TWT drive signal is pulsed at various PRFs and pulsewidths, depending on the Ku-band mode selected and the target range.

Derivation of the TWT drive signal during Comm Mode operation is identical to that of radar mode except that the radar channel 1 first LO is mixed with a modulated 1875 MHz comm S-band carrier signal to upconvert it to the TWT drive; a transmit frequency of 15.003 GHz results that is CW, as opposed to pulsed, and is always output at full power level.

### 9.7.1.2 Transmitter Overview

On receipt of Transmit Enable commands (XMIT ENA COMM A), the TWT modulating anode is enabled, provided that the 3.5-minute TWT filament timeout is complete and that no faults, such as TWT cathode overvoltage, body current, or high reflected power, exist. With the TWT modulating anode enabled and the transmitter on, the operate status signal is issued. The TWT amplifies the pulsed (radar) or CW (comm) TWT drive signal to provide an output of approximately 55 W in radar bandwidth and 60 W in comm.

### 9.7.1.3 Microwave Subassembly Overview

The TWT output is routed to the microwave subassembly, in which any harmonics outside the radar and comm bandwidths are filtered. This signal is then duplexed and routed via different paths, depending on whether the DEA is operating in Radar or Comm mode.

In Radar Mode the transmit RF signal is routed through a ferrite circulator switch that is commanded to the minimum attenuation state during the transmitted RF pulse interval and provides 80 dB of attenuation during receive time. This switch arrangement attenuates any noise emanating from the TWT that would degrade receiver sensitivity during receive listening time.

During TWT bypass mode, the circulator switch is switched to the high attenuation state, providing both a low attenuation path for the TWT bypass pulsed RF signal and, at the same time, the required 80-dB attenuation of the TWT noise output.

The transmit RF pulse is then routed via a second diplexer and circulator to the high gain sum antenna. The nominal output power level at this point is approximately +46 dBm in TWT full power mode and +6.6 dBm in TWT bypass mode.

In Comm Mode, the CW RF signal is routed via the first diplexer to a waveguide switch that routes the RF signal to either the DEA wide-beam horn antenna (primary acquisition mode) or through the second diplexer and circulator to the sum antenna (alternate acquisition mode). The output power level during comm operation is +47 dBm (50 W - SPEC value).

#### 9.7.1.4 Receiver Overview

The DEA is implemented as a dual-channel (sum and difference) receiver during Radar or Comm Modes. The sum and difference received RF signals from the DMA narrow-beam antenna are bandpass filtered before low noise amplification.

In Comm Mode the output of the sum first IF bandpass filter is amplified and sent to the EA-1 for processing during comm. The sum and difference first IFs are also summed and AGC amplified to form the comm track IF signal.

In Radar Mode the sum and difference channel first IF signals are summed together and amplified in the radar band first IF amplifier to form the Radar Track IF signal and, in addition, downconverted further to the radar second IF of 78 MHz and sent to EA-2.

#### 9.7.1.5 LVPS Overview

The Low Voltage Power Supply receives 28 volts power from Mid-Power Control Assembly No. 2 via MNB MPC 2.

The LVPS provides DC to DC Power Conversion for various voltages throughout the DEA.

#### 9.7.2 Exciter In-Depth Detail

The DEA exciter subassembly provides highly stable and spectrally pure low-level drive signals for the transmitter TWTA in each of the five radar frequency channels and the single channel in the comm mode of operation. In the TWTA bypass mode of radar operation, the exciter output is used as the transmitter signal. In addition, the exciter provides the first and second LO signals for use in the receiver mixer downconverters. The radar self-test function is also provided by the exciter subassembly.

The reference oscillator for the exciter is a highly stable 156.285-MHz, quartz crystal controlled oscillator that is located in the Interface and Control Unit. The radar second LO signal (573.05 MHz) is generated by frequency dividing ( $\div 3$ ) the buffered 156.285 MHz reference signal and frequency multiplying it ( $\times 11$ ) in a step recovery diode combine generator followed by a bandpass filter. To provide additional receiver protection from saturation during radar transmission, the second LO is blanked by the T/R gate.

The radar Transmit Oscillator (TO) offset signal (651.19 MHz), which is used as the IF drive to the radar mixer/upconverters, is synthesized by frequency dividing ( $\div 2$ ) the buffered reference oscillator signal, amplifying it, and mixing it with a sample of the 573.05-MHz second LO signal. The TO offset signal is blanked during the receiver listening time by turning off the divide-by-2 frequency divider.

A harmonic phase-locked loop generates five crystal-stabilized Ku-band operating frequencies from the single 156.285-MHz reference oscillator. These RF frequencies range from 13.128 to 13.336 GHz in steps of 52 MHz; they are selected one at a time

on command from the Radar Signal Processor to provide the first LO signals as well as RF drive to the radar and comm upconverters. In radar mode they are upconverted by the TO offset frequency (651.19 MHz) to provide the five radar transmit frequencies. In comm mode the lowest frequency channel (13.128 GHz) is selected and upconverted by the modulated comm signal (1.875 GHz carrier) to provide the 15.003-GHz drive to the TWTA.

The 156.285-MHz reference signal, amplified to +27 dBm, drives a step recovery diode combine frequency generator followed by a single-tuned cavity filter that selects the 83rd harmonic (12.972 GHz). The output of this times-83 frequency multiplier is mixed with a sample of the Gunn diode VCO (Gunn VCO), which produces an IF of 156 to 364 MHz at a signal level of -30 dBm. Wideband amplifiers raise this level sufficiently to drive a phase comparator with a reference input of 52 MHz obtained by dividing the 156.285-MHz reference frequency by three. Whenever the Gunn VCO tunes to a frequency for which the IF output from the Ku-band mixer equals any integral multiple of 52 MHz, the phase comparator output will be a "zero beat" that is used, through a suitable loop filter, to phase-lock the VCO.

It remains to select the desired operating frequency channel from among the several possibilities available. To make this selection, a sample of the IF signal from the Ku band mixer drives five simple LC filters, each of which is followed by an RF detector. The sweep and logic circuitry responds to the output from these detectors, as well as to a zero-beat detection circuit, and to an input code that specifies the desired frequency channel. The logic ENSures that the sweep circuit will be disabled and will permit phase-lock only when the Gunn VCO is phase-locked in the passband of the IF filter that corresponds to the selected Ku-band frequency channel. The output from the harmonic phase-locked loop is power divided to provide both the first LO signal and RF drive to either the radar or comm mixer/upconverter, depending on the position of the Single Pole Double Throw (SPDT) mode select switch. In radar mode, the RF drive to the upconverter is gated by the radar exciter gate on command from the Radar Signal Processor to form the desired pulsewidth and PRF.

Following upconversion in either radar or comm mode, the RF transmit signal is used to drive the limiting amplifier. This amplifier, which consists of four balanced stages, increases drive power to the TWTA and also serves as a limiter to reduce amplitude modulations on the drive signal to the transmitter.

In TWTA bypass mode, the SPDT switch following the limiting amplifier is used to route the drive signal around the TWTA to reduce radar transmitted power in short range operation. In addition, further control of transmitted power is provided by the absorptive modulator, which is controlled by the radar output panel switch in radar power low and medium modes, by reducing the TWTA drive power to effect a 12-dB and a 24-dB reduction in the DEA output level from full power.

Circuitry is also contained within the DEA exciter module for generation of a simulated radar target during the Ku-band system radar self-test. A sample of the radar

upconverter output is fed through a Single Pole Single Throw (SPST) switch and a variable attenuator to the self-test dipole located in the antenna reflector at one of four selectable power levels and pulsed by the Radar Signal Processor to simulate targets at various ranges.

### 9.7.3 Transmitter In-Depth Detail

The transmitter provides RF Pulse or CW RF amplification of the Ku-band signal in both Radar and Comm modes, respectively. The saturated output power is 50 W minimum, 60 W typical. Coincidental with the amplification function, the transmitter module also provides an analog signal that indicates the power radiated from either the widebeam or narrow-beam antenna. As a secondary function, the transmitter generates the control signal for the DEA waveguide switch and the DMA polarization switch.

Four distinct functional blocks make up the transmitter subassembly.

- Logic
- Filament/anode supply
- High Voltage Power Supply (HVPS)
- TWT (Hughes model 874H)

#### 9.7.3.1 Logic

The transmitter logic controls the “TWT Enable Sequence” and “TWT Disable Sequence” of the TWT modulating anode, controlling the TWT during power amplification and disabling it during waveguide transitions or HVPS malfunctions. This logic also provides the drive for the DEA waveguide and DMA polarization switches.

##### TWT Enable Sequence

On receipt of the STANDBY/ON commands, the logic enables the LVPS (LVPS ON). With application of power, the logic initiates a 3.5-minute TWT filament warmup time, during which high voltage to the TWT is inhibited. Concurrently, the prime power relay is energized to apply 28 V dc to the HVPS. A logic level COMM ON signal is also sent to the exciter subassembly.

When the 3.5-minute timeout has elapsed, high voltage may be applied to the TWT via RADAR ON or COMM ON commands; RF amplification is inhibited until the transmit enable commands are received. The logic determines the phasing of the converter transistors and provides a converter enable signal, applying high voltage to the TWT.

Operationally, the DEA must process two commands to “enable the TWT” to provide a Carrier Signal. The RADAR SELF TEST/TWT INH and XMIT ENA

COMM A allow the DEA Transmitter to apply 200 volts to the TWT anode, readying the TWT for RF amplification.

RADAR SELF TEST/TWT INH: EA-1 will send this command to directly control TWT off and on times using Obscuration, RF Protect Masks, and Beta Modes.

XMIT ENA COMM A: SPA will use this command to "control" TWT-OFF command to control the Carrier for Alternate Acquisition Mode.

Operate status is flagged at this time to indicate that the DEA is ready to transmit.

#### TWT Disable Sequence

The TWT cannot amplify during the presence of any of the following conditions:

1. Transmitter faults
2. Insufficient filament warmup
3. Waveguide switch transitions
4. High reflected power

An abnormality such as cathode over/undervoltage, high helix current, or high reflected power will prevent the TWT from transmitting. Cathode undervoltage and reflected power are nonlatching faults; the transmitter will operate without further stimuli if these faults disappear.

Cathode overvoltage and high helix current are latched faults; the transmitter will not operate without further stimuli even after these faults disappear. An automatic recycle function in the logic prevents the latched faults from shutting off the transmitter during short-term instabilities. Only after three latched faults have been sensed within a 3-second interval is the TWT prohibited from transmitting without external manipulation; i.e., recycling the ON command.

Occurrence of a current fault results in the latching open of the 28 V dc input relay. STANDBY and ON commands must be removed to check the validity of this fault.

The 3.5-minute timer inhibits application of high voltage to the TWT until the tube gun is sufficiently heated. Provision to withstand a 7-second loss of power without reinitialization of the timer is also included.

RF is pulsed OFF during the transition of either the DMA or DEA waveguide switches. Information regarding the position of each waveguide switch is sent via waveguide switch interlock inputs to prevent occurrence of high reflected power levels that could damage the TWT output isolation load. In addition, the RF is held off when the DEA and DMA switches are sensed to be in inconsistent positions. During most of the radar self-test, the transmitter is held OFF by a self-test



enable/TWT inhibit signal from the Interface and Control Unit to prevent the transmitted RF from masking the simulated target returns.

The logic processes the linear polarization and wide-beam select commands generating 100-ms pulse drive excitation for the DMA polarization rotary switch and DEA waveguide switch. Transitions for these signals occur at the rising and falling edges of the input command.

The power monitor detects the peak power radiated from either the wide-beam or the narrow-beam antenna. The RF-detected signal is sent from the DMA to the operational instrumentation system and processed to provide an analog dc signal with amplitude proportional to the peak power output.

### 9.7.3.2 Filament/Anode Supply

The filament/anode supply provides biasing for the TWT filament and anode. The filament voltage is -6.3 V dc with respect to the TWT cathode. The anode supply output is adjusted for each TWT. The voltage range is 0 to 300 V dc.

A linear regulator and dc-dc converter are used to achieve the filament and anode biases. The linear regulator provides regulated +21 V dc to the converter. Constant current limiting protects the filament from overloads; the current limit point is 2.0 A. Voltage feedback to the regulator is provided by a sense winding on the converter transformer. The converter switching rate (10 kHz) and phasing of the converter switches is controlled by the logic. The supply is enabled when DEA power is applied.

### 9.7.3.3 High Voltage Power Supply

The HVPS provides biasing for the TWT. The output requirements follow. All voltages are with respect to ground.

|                | <u>Element</u> | <u>Voltage (kV)</u> | <u>Current (mA)</u> |
|----------------|----------------|---------------------|---------------------|
| Nominal values | Cathode        | -7.0                | 2.0                 |
|                | Collector 1    | -4.6                | 33.0                |
|                | Collector 2    | -5.3                | 18.0                |
|                | Collector 3    | -6.6                | 8.0                 |

An input filter, pulsewidth modulated dc-dc converter, and high voltage cathode regulator are the major elements of the HVPS.

A single section L-C input filter provides the required ripple reduction on the 28 V dc bus. Current surge amplitude at turnon is limited by a 2-ohm resistor that is bypassed when the input capacitor has been charged. TWT biases are supplied by a pulsewidth

modulated dc-dc converter. Output voltage is sensed indirectly via a low voltage winding. An error signal derived from the sense voltage and a precision ramp generator controls the duty cycle of the converter. The converter phasing and frequency (10 kHz) are controlled by the logic. The power supply is enabled by command from the logic. The +28 V dc current drawn by the pulsewidth modulated converter is sensed. An overload results in a logic level signal being sent to the logic to remove power.

Eight transformer secondaries are connected in series to form the cathode supply voltage of -7.0 kV. The cathode output is series regulated to obtain the required noise performance. The collector secondaries are then added to the cathode voltage to obtain the required depression; i.e., for the collector 3 voltage, a 400-V supply is added to the cathode supply to achieve -6.6 kV, while for the collector 2 bias, a 1300-V supply is added to the collector 3 and cathode supplies to achieve 5.3 kV, and a 700-V supply is added to the collector 2 and cathode supplies to obtain -4.6 kV. The collector supplies are not postregulated as is the cathode supply.

The cathode voltage is sensed by a precision high voltage divider assembly. The sense voltage is the input to the cathode regulator. This same voltage is buffered to be used in the detection of the cathode over/undervoltage faults sent to the logic.

TWT helix current is sensed in the return of the cathode supply. A high current condition results in the removal of high voltage from the tube.

For optimization of TWT performance, cathode and anode voltage supplies are adjusted to the optimum voltage for each TWT. During transmitter module testing, cathode and anode voltage forms are adjusted to the TWT nameplate voltage by a change of the fixed resistors on the transmitter module. Adjustment of the modulating anode supply voltage changes the total beam current and TWT RF power output. Each tube, therefore, can be adjusted to provide 60 W of nominal power output.

#### **9.7.3.4 Traveling Wave Tube**

The TWT selected for the DEA transmitter is the Hughes model 874H. It provides 60 W of CW power in the 13.75- to 15.1-GHz frequency range, satisfying the requirements for both radar and comm bands. This tube is a Permanent Periodic Magnetic (PPM) focused helix TWT with three stages of depressed collectors that provide an overall efficiency of greater than 45 percent.

The 874H electron gun is designed to provide a 65-mA electron beam at -7.0 kV. A modulating anode is incorporated to switch the tube on and off. A helix supported by beryllium oxide rods is used for the RF circuit. A dual pitch helix was selected to provide optimum RF characteristics in both radar and comm bands with low distortion. A beam scraper is introduced between the electron gun and the input end of the circuit to provide protection for the first few turns of the helix. In case of power supply malfunction or gun arcs, the beam scraper (with a much higher thermal tolerance) will intercept the current and protect the helix. The magnetic circuit has a high focusing quality factor; the result is very low helix and body interception of the electron beam.

The magnetic material is samarium cobalt, which has the highest energy product of known magnetic materials. The collector is conduction cooled and comprises three separate stages, each operating at different potentials. The input connector is an SMA connector, while the output connector is waveguide.

The tube operates at a -7.0 kV cathode voltage with the three collector stages operating respectively at 65, 75, and 95 percent depression. A positive anode voltage of about 300 V sets the cathode current at approximately 65 mA.

RF power of 60 W over the band from 13.75 to 15.1 GHz with a gain of 43 dB has been achieved. Efficiency in excess of 45 percent has been attained on several tubes.

#### 9.7.4 Receiver In-Depth Detail

The DEA is implemented as a dual-channel (sum and difference) receiver during Radar or Comm Modes. Each channel can be separately controlled so that during search, the sum channel only is enabled. On target detection, the difference channel can be enabled so that a radar mainlobe/sidelobe discrimination can be performed to prevent sidelobe lockons. In track, the sum and difference channels are both enabled and summed in the receiver to form the angle error tracking signals.

The sum and difference received RF signals from the DMA narrow-beam antenna are bandpass filtered before low noise amplification. Each channel contains a solid-state T/R limiter to protect against high level incident power. Each is also actively gated (switched off) during TWT ON modes to prevent the Low Noise Amplifiers (LNAs) from oversaturation.

The LNAs are 0.5-micron devices with a typical noise figure of less than 5 dB and a gain of 23 dB. The RF outputs from the LNAs are mixed with the first LO from the exciter for downconversion to a first IF of 651 MHz in radar and 647 MHz in comm. A phase shifter in the difference channel of the first LO provides a 0°/180° lobing phase shift to form the +D AZ, +D EL angle tracking error signals and a 0°/45° phase shift for linearly (radar passive) or circularly (comm or radar active) polarized target returns.

Solid-state diode switches in each channel are selectively gated during radar search or track operation to prevent ringing of the first IF bandpass filters and second IF amplifier stage saturation caused by main bang leakage during the transmit pulse. In Comm Mode, the diode switches are unblanked (switched on - receiver enabled).

The first IF bandpass filter characteristics result in minimal phase distortion during comm mode and relatively steep skirts for adequate rejection of a spur at 13.725 GHz generated by other S-band equipment operating onboard the orbiter. The output of the sum first IF bandpass filter (comm data IF) is amplified and sent to the Interface and Control Unit for processing during comm. The sum and difference first IFs are also summed and AGC amplified to form the comm track IF signal, then downconverted further to the radar second IF of 78 MHz. Depending on the transmit pulsewidth, the

radar second IF bandwidth is selectable to form a matched filter for short pulse (0.122  $\mu$ s, bandwidth = 10 MHz) and long pulse (>2.07  $\mu$ s, bandwidth = 3 MHz) modes.

The receiver has a dynamic range of 120 dB that is AGC implemented via a 30-dB step in the transmitter microwave T/R limiter and a 30-dB step, 42-dB linear AGC amplifier in the receiver subassembly. In addition, the TWT bypass (44 dB) is also included in the overall AGC profile.

The RF LNA and the first mixer and IF amplifier are housed in a single hermetically sealed subassembly that is physically located in the transmitter microwave subassembly adjacent to the T/R limiter to reduce receive microwave losses. However, this assembly is functionally a part of the receiver, one such subassembly being used in each of the dual receive channels.

The RF LNA is a GaAs FET amplifier with three balanced stages. Following the LNA is a microstrip bandpass filter designed to pass the receive RF frequency band and provide more than 20 dB of rejection at the image band for purposes of image rejection. Following the bandpass filter is a single balanced mixer for downconversion to the first IF (651 MHz for radar mode and 647 MHz for comm mode). After downconversion, receive signals are amplified in the first IF amplifier, which is followed by a passive temperature compensation circuit for reduction of the gain variations of the subassembly overtemperature. The subassembly provides an RF-to-IF gain of 23 + 2 dB, over frequency and environment, with a maximum associated noise figure of 5 dB.

A 4-bit digital phase shifter is located in the line providing the LO drive to the difference channel first IF mixer. The phase shifter provides a 45° bit for realigning the phase of the dual channels when switching from linearly (radar passive) to circularly (radar active) polarized target returns. It also provides a 180° bit for the lobing phase shift.

Solid-state diode receiver inhibiting switches are located in both dual channels following the first IF amplifiers. These switches perform a number of functions.

- A. Gate the receiver off during radar transmission
- B. Enable the sum channel only during radar search
- C. Enable the difference channel only after radar target detection to perform a mainlobe/sidelobe discrimination test
- D. Enable both the sum and difference channels during track to form the angle tracking error signals

First IF bandpass filters are located in each receiver channel following the diode receiver inhibiting switches. These filters are needed for sufficient rejection of potential interference from the S-band communications transmitter onboard the orbiter, secondary image frequency (494.91 MHz) before the receiver second IF mixer, and interference at 1.875 GHz that occurs during comm mode.

The output from the sum channel first IF bandpass filter is amplified in the comm band first IF amplifier (gain = 56 dB nominal) and sent to EA-1 at a carrier frequency of 647 MHz for further processing during comm mode.

The sum and difference channel first IF signals are also summed together and amplified in the radar band first IF amplifier (gain = 60 dB nominal) to form the comm track IF signal and, in addition, downconverted further to the radar second IF of 78 MHz. The radar first IF amplifier provides a 30-dB step of AGC and a 42-dB range of linear AGC for extending the dynamic range of the receiver during radar operation. The radar second IF amplifier has a selectable bandpass that forms an approximately ideal matched filter for short pulse (0.122  $\mu$ s, bandwidth = 10 MHz) and long pulse (>2.07  $\mu$ s, bandwidth = 3 MHz) radar modes.

### 9.7.5 Microwave Assembly In-Depth Detail

The Microwave Subassembly separates radar band energy from comm band energy, isolates the radar receiver from the noise generated in the TWT during the interpulse period, and recombines the radar and comm energy into a single transmission line.

The Microwave Subassembly consists of a harmonic filter, a diplexer, ferrite and waveguide switches, directional couplers, bandpass filters, a ferrite circulator, Field Effect Transistor (FET) low noise amplifiers, and receiver protection devices.

The ferrite circulator provides a matched load impedance to the TWTA by absorbing any reflected energy. The harmonic filter reflects all harmonic energy generated in the TWTA to the circulator to be absorbed in the attached termination.

The diplexer separates the comm band energy from the radar band energy and recombines the two signals after the RF switch. The diplexer consists of two 3-dB short-slot couplers and two matched bandpass/band reject filters. Radar band energy is reflected from the filters to the ferrite switches while comm band energy is coupled through the device with minimum loss.

Four ferrite switches couple radar channel interpulse noise energy to absorptive terminations. The TWTA bypass RF signal is coupled through the fourth ferrite switch to the antenna. The drivers are integral to the devices.

A waveguide switch couples comm band energy either to the main sum antenna or to the wide-beam horn. The switch also couples the receive signal to the receiver difference channel. The actuator element employs a torque motor with the actuator and stator magnetically coupled to the rotor. The indicating circuits utilize microswitches.

Two waveguide directional couplers provide RF power samples for ground support equipment. A three-port ferrite circulator is used in the sum channel as a diplexer to time-share the narrow-beam antenna. An identical circulator (with the third port terminated) in the difference channel equalizes losses and ensures phase tracking of the two channels over the temperature range of operation.

The bandpass filters following the circulators couple the receive signals into the receiver with minimum insertion loss and reject the transmit comm band energy.

The receiver protector devices are passive T/R limiters, each consisting of dual diode stages. The diodes can be triggered passively but will normally be biased actively during radar operation to achieve faster switching times and greater isolation with attendant increased protection. The devices are also used as a single discrete step of RF AGC with a 30 dB precision attenuation level.

The low noise amplifiers are physically located in the microwave assembly to minimize RF losses.

### 9.7.6 Low voltage power supply In-Depth Detail

There are four LVPSs in the entire Ku-band system. These power supplies accept unregulated 28 V dc and condition it to furnish regulated voltage forms to the DEA, the Interface and Control Unit, and the radar and comm signal processors.

The steady-state dc input voltage is  $28 + 4$  V. Regulation of the output voltage is 5 percent of the nominal value. Maximum ripple voltage is within 1 percent of each voltage peak-to-peak. The four power supplies are similar, the main differences being variations in their output voltages and current.

The LVPS provides the following five different design criteria to provide the best stable power sources:

#### A. Line filters

The line filter consists of a two-section L-C filter. This filter is required to keep 28 V bus noise and ripple out of the power supply and, conversely, to keep power supply generated noise and ripple from being put back on the 28-V power bus.

#### B. Undervoltage protection

The undervoltage protection circuit turns off the linear regulator and, hence, the power supply when the input voltage (28 V dc) drops below  $20 + 0.5$  V dc. It automatically turns the power supply back on when the input voltage returns to  $22 + 0.5$  V dc if the LVPS ON command is present.

#### C. Linear regulator

The linear regulator provides a constant voltage to the converter despite input line variation; the output voltage is approximately 21 V dc. The linear regulator consists of a series pass stage transistor controlled by a high gain feedback network by means of an error amplifier and a temperature-compensated zener for reference voltage. The linear regulator does not sense the 21 V dc bus directly for regulation but senses the voltage developed from an auxiliary winding from the converter. This sensing arrangement provides better regulation for output voltage of the converter. The linear regulator has

current limiting. If a short is present on the output of the regulator, either between the regulator and the converter or at the output of the converter, the +21 V dc begins to drop. When voltage drops below 20 V dc, the converter is turned off. When the short is removed, the converter remains off. To start the converter again, the ON command must be removed and reapplied.

#### D. Overvoltage protection

The overvoltage protection circuit turns off the converter if the 21 V dc bus increases to 24 V dc. If the overvoltage condition is cleared, the converter will remain off. To restart it, the ON command must be removed and reapplied. As an example of how this sequence could occur, assume that the pass stage of the linear regulator failed short-circuited. The converter then shuts off because of the resulting overvoltage. The output voltage is, therefore, prevented from applying an overvoltage condition to the loads.

#### E. Dc-dc converter

A dc-dc converter provides the various output voltages for the LVPS. Each output is obtained through a separate secondary winding of the converter transformer. The voltage is then rectified and filtered by an LC network. The converter is a standard two-transformer design with the output transformer nonsaturating. It runs at a frequency of approximately 20 kHz. It is started by a 100-ms start pulse that is provided only when the ON command is first applied or when the undervoltage protection circuit has recovered from a low line condition.

### 9.8 DEPLOYED MECHANICAL ASSEMBLY (DMA)

The DMA is made up of five major components.

- Dish Antenna Electronics
- Rate sensor assembly
- Beta (b) gimbal
- Alpha (a) gimbal
- Rotary joint

#### 9.8.1 Dish Antenna Electronics

The main antenna, which is a 36-inch graphite, fiber-reinforced composite, parabolic reflector, is edge-mounted on the beta gimbal. One leg of the tripod-mounted antenna feed contains two waveguide paths to the antenna feed. One path is used with the narrow beam sum channel to provide a Transmit/Receive (T/R) signal path in the comm and radar modes. The second path, the difference channel, is only active when tracking a signal and is a receive-only channel in both comm and radar modes.

The four-slot antennas that are mounted in the four quadrants around the sum antenna provide the delta Azimuth (AZ) and delta Elevation (EL) error signals after processing by the monopulse comparator. The delta AZ/delta EL switch multiplexes these signals on the difference channel. The difference channel is linearly polarized, while the sum channel is Right-hand Circularly Polarized (RHCP) in comm and radar cooperative and linearly polarized in radar passive. The narrow-beam antenna characteristics are shown in Table 9-8.

**Table 9-8. Narrow Beam Antenna Characteristics**

| Antenna type diameter     | Prime fed parabola 36 in. |
|---------------------------|---------------------------|
| <b>Sum channel</b>        |                           |
| Parameter                 | Performance               |
| Frequency                 | 13.75 - 15.15 GHz         |
| Peak gain                 | 38.5 dB                   |
| 3 dB beamwidth            | 1.7°                      |
| Sidelobe/Backlobe level   | -20 dB / - 40 dB          |
| Polarization              | RHC/linear                |
| <b>Difference channel</b> |                           |
| Parameter                 | Performance               |
| Frequency                 | 13.75 - 14.0 GHz          |
| Polarization              | Linear                    |

A wide-beam linearly polarized horn antenna is also mounted on the beta gimbal. It was to be used in comm primary acquisition mode to aid TDRS acquisition of the orbiter return link. However, because of TDRS receiver limitations, the primary acquisition mode is not used. Therefore, the 20-dB gain horn is used only in radar mode to prevent antenna sidelobe lock on the radar target.

A waveguide switch is used to select input to the receiver difference channel, either delta AZ/delta EL error data when tracking or the sidelobe prevention circuit signal during acquisition in radar mode. The position of the switch is monitored by the transmitter logic circuitry in the DEA to disable the Traveling Wave Tube (TWT) RF output during waveguide switching and incorrect switch positioning; i.e., connecting the TWT output to the monopulse comparator.

A second waveguide switch is used to provide a measure of output power from the sum channel or difference channel. Of course, the difference channel output would be used in primary acquisition mode only, and this mode is not used operationally. Therefore, the switch is always in the sum channel position.

A third waveguide switch is used to select either linear or RHCP in the sum channel. EA-1 sends a control signal to the DEA to configure linear for radar passive and circular for comm or radar active modes.



### 9.8.2 Rate Sensor Assembly

The rate sensor assembly, which is also mounted on the beta gimbal, houses two rate gyroscopes and associated circuitry in a temperature stabilized enclosure. Each gyro provides an output proportional to the inertial antenna line-of-sight motion in its respective axis. A high output signal is selected when the antenna is in radar search or being slewed. The low output is selected during comm search or comm/radar track. These signals are used to modify the gimbal servomotor drive outputs during acquisition or track.

The Deployed Electronics Assembly (DEA) Low Voltage Power Supply provides the Rate Sensor Assembly Logic to precede the Gyro Error Signals. Failure of this DEA power supply will cause large erratic motion of both Alpha and Beta motors; if the Ku Band is not quickly turned off this failure may cause damage to the parabolic dish.

### 9.8.3 a/b Gimbal

The beta gimbal is mounted on the alpha gimbal housing, which, in turn, is mounted on the frame into which the DEA fits. Both dc gimbal motors are identical but the beta, or inner, gimbal is limited in its motion from  $-85^{\circ}$  to  $+75^{\circ}$ . The alpha, or outer, gimbal motion is from  $-206^{\circ}$  to  $+154^{\circ}$ . The antenna coordinate system 0,0 reference is up the minus Z body axis. Two drive signals (1 and 2) are provided from the gimbal servodrive circuits in the Interface and Control Unit and provide for positive or negative motion about the gimbal axis. An encoder disc is mounted on each motor shaft and provides motor position information. The digital output ( $0.088^{\circ}$  resolution) resets a storage buffer in the Interface and Control Unit every time a Master Index Pulse (MIP) is encountered. There is one MIP on each gimbal encoder.

### 9.8.4 Rotary Joint

The rotary joint provides a dual waveguide path through the alpha and beta gimbals for the sum and difference channels. Also, a ribbon cable is routed through the gimbal housings to provide a path for power and control signals.

## 9.9 EA-1 INTERFACES

Ku-Band is a complex system of LRUs. Each LRU performs a certain task with either control or routing key signals, understanding how the Uplink, Downlink, Analog control, Digital control, and Discrete control flow between LRUs is very important.

The understanding how EA-1 interacts with the other LRUs is key in understanding how the entire Ku-Band system works. EA-1 hardware/software sends "most" of the controlling discretess/signals to many of the other systems LRUs. Briefly, EA-1 interfaces with the following LRUs.

- SM General Purpose Computer (GPC) via the Payload Forward 1 (PF 1) Multiplexer/ Demultiplexer (MDM).

- Guidance, Navigation and Control GPC receives telemetry via the Flight Forward 3 (FF 3) MDM.
- Crew controls on Panel A1U operate the system in either Radar or Communication mode.
- Ground Control Interface Logic (GCIL) commands allow the ground to operate the system in the Communication mode.
- Dedicated displays on panels A1U and A2 display measured system parameters; e.g., range, angle, signal strength, etc. System data are also displayed on the SM and GNC and SM Display Electronics Units (DEUs).
- Providing the SPA the forward link and Modulation Switch control.
- Controlling the DEA TWTA Switch.
- Providing DMA Alpha and Beta Gimbal Motor Rate Controls.
- Interaction with EA-2 Providing key Radar Information.
- The Deployed Motor Subassemblies Inputs

#### **9.9.1 EA-1 Interfaces with the SM GPC**

The SM GPC interfaces with EA-1 by via PF1 MDM Card 8 Channel 2 via a Serial Input/Output Card. After the SPEC 2011 Item 8 this interface transmits back and forth:

The SM GPC sends five-16 bit words (Control Word) to the Ku-Band

The Ku-Band sends ten-16 bit words (Status Words) to the SM GPC

##### **9.9.1.1 SM GPC to EA-1 Control Words**

The SM GPC sends Ku-Band five-16 bit control words. These are all listed in Table 9-9 and Table 9-10. In General:

- INCO will write SM GPC loads to configure “most” of Control Word 1.
- The SM GPC, using Antenna Management software will derive AZ and EL, placed in Control Words 2 & 3.
- The SM GPC using GNC GPC Kalman Filter input, will ship Radar Range in Control Word 4 & 5.
- INCO will overwrite the Beta Angle RF Constraint in Control Word 5.

**Table 9-9. Ku-band antenna Control Word 1**

| Data bit | Word bit | Function                         | Logic state 1 |
|----------|----------|----------------------------------|---------------|
|          | 1-3      | SYNC                             | -             |
| 0        | 4        | SEARCH INITIATE (CR)             | When true*    |
| 1        | 5        | KU-BAND BRK TRK CMD TGL 1 (C)    | When true*    |
| 2        | 6        | KU-BAND BRK TRK CMD TGL 2 (C)    | When true*    |
| 3        | 7        | SPREAD SPECTRUM ON/OFF (C)       | Off           |
| 4        | 8        | Ku A/B SELECT (C)                | Ku B          |
| 5        | 9        | SELF TEST ON/OFF (R)             | On            |
| 6        | 10       | MODULATION CONTROL 1 (C)         | (See note)    |
| 7        | 11       | MODULATION CONTROL 2 (C)         | (See note)    |
| 8        | 12       | PRIMARY ACQ MODE ON/OFF (C)      | Off           |
| 9        | 13       | GPC DESIG INERT STAB ON/OFF      | Off           |
| 10       | 14       | FORWARD LINK MODE 1/2 216/72 (C) | Mode 1        |
| 11       | 15       | RADAR THRESHOLD VAR/FIX (R)      | Fix           |
| 12       | 16       | OBSCURATION INTLK OVERRIDE (CR)  | When true     |
| 13       | 17       | TWTA OFF (CR)                    | When true     |
| 14       | 18       | MASK SELECT BETA/BETA + MASK (C) | Beta          |
| 15       | 19       | SPARE                            | -             |
|          | 20       | PARITY                           | As applicable |

| Logic state |             | Modulation mode |
|-------------|-------------|-----------------|
| Word bit 10 | Word bit 11 |                 |
| 0           | 0           | Auto            |
| 0           | 1           | Off             |
| 1           | 1           | On              |
| 1           | 0           | Auto***         |

\*Momentary control functions, bit set on one MDM cycle and reset on following cycle.

\*\*Mutually exclusive.

\*\*\*Not normally selected.

C = Communications; R = Radar

Table 9-10. Ku-band antenna Control Words 2 through 5

| Bit      | Word 2<br>Radar/comm designated<br>azimuth angle, deg | Word 3<br>Radar/comm designated<br>elevation angle, deg | Word 4<br>Designated radar<br>range, ft | Word 5<br>Designated radar<br>range, ft |
|----------|---|---|---|---|
| 1        | Sync  | Sync  | Sync                                    | Sync                                    |
| 2        | Sync  | Sync  | Sync                                    | Sync                                    |
| 3        | Sync  | Sync  | Sync                                    | Sync                                    |
| 4        | +/-*  | +/-*  | 1,310,720                               | 20                                      |
| 5        | 180   | 90  | 655,360                                 | 10                                      |
| 6        | 90  | 45  | 327,680                                 | 0 not used                              |
| 7        | 45  | 22.5  | 163,840                                 | 0 not used                              |
| 8        | 22.5  | 11.25   | 81,920                                  | +/-*                                    |
| 9        | 11.25   | 5.625   | 40,960                                  | 90                                      |
| 10       | 5.625   | 2.8125  | 20,480                                  | 45                                      |
| 11       | 2.8125  | 1.40625   | 10,240                                  | 22.5                                    |
| 12       | 1.40625   | 0.703125  | 5,120                                   | 11.25                                   |
| 13       | 0.703125  | 0.3515625   | 2,560                                   | 5.625                                   |
| 14       | 0.3515625   | 0.17578125  | 1,280                                   | 2.8125                                  |
| 15       | 0.17578125  | 0.087890625   | 640                                     | 1.40625                                 |
| 16       | 0.087890625   | 0 not used  | 320                                     | 0.703125                                |
| 17       | 0 not used  | 0 not used  | 160                                     | 0.3515625                               |
| 18       | 0 not used  | 0 not used  | 80                                      | 0.17578125                              |
| 19       | 0 not used  | 0 not used  | 40                                      | 0.087890625                             |
| 20       | Parity  | Parity  | Parity                                  | Parity                                  |
| MSI<br>D | V74H2648J   | V74H2650J   | V74U2651J                               |   |
|          |   |   | BETA                                    |   |
|          |   |   | ANGLE=V74H2655J                         |   |

\*Minus (-) = Logic 1.

### 9.9.1.2 SM GPC Loads to EA-1

The following are a list of SM GPC loads to change the SM GPC Control Words 1-5. Some of these loads are available on SPEC 2011 Antenna to allow the crew access to “enter” these loads. Operationally, most of these loads are sent by INCO to configure the Ku-Band for Comm Mode.

|  |   |
|--|---|
| <p>KU RADAR RNG EST - AUTO<br/>(14005)</p> | <p>Enables the AM to output an estimated range (words 4 and 5) computed from the target state vector provided by the GNC GPC. Inhibited in comm mode.</p>   |
| <p>KU RADAR RNG EST - MIN<br/>(14006)</p>  | <p>Forces the AM to output zeros in designated azimuth and elevation angles (words 2 and 3) (antenna will point up the -Z axis; this is the normal rendezvous attitude and the origin of the antenna coordinate system AZ = 0° and EL = 0°) and output a designated range (words 4 and 5) of 2400 feet.</p>                     |
| <p>KU SERIAL I/O ENABLE<br/>(14007)</p>    | <p>Enables the serial input/output channel between the SM GPC and the Ku-band interface and control assembly via MDM PF1. This channel will be bypassed when the SM GPC is initialized because the Ku-band system is not normally powered up when the SM GPC is initialized on orbit.</p>                                       |
| <p>KU-A SPRD SPM - ON<br/>(14013)</p>      | <p>Resets data bit 3 word 1 - Enables the Ku-band interface and control assembly to operate in the spread spectrum mode on the forward link.</p>  |
| <p>KU-A SPRD SPM - ON<br/>(14013)</p>      | <p>Resets data bit 3 word 1 - Enables the Ku-band interface and control assembly to operate in the spread spectrum mode on the forward link.</p>  |
| <p>KU-A SPRD SPM - OFF<br/>(14014)</p>     | <p>Sets data bit 3 word 1 - Disables the spread spectrum mode of operation in the Ku-band interface and control assembly.</p>   |
| <p>KU-BD A/B SEL - A ON<br/>(14015)</p>    | <p>Resets data bit 4 word 1 - Forces the Ku-band communications signal processor to accept forward link data from the Ku-band A system. (Since the Ku-band B system was deleted, the Communications Signal Processor will always be initialized to the Ku-band A system. There is only one Ku-band antenna on the orbiter.)</p> |

---

|                                   |   |
|-----------------------------------|---|
| KU RDR SELF TEST ON<br>(14016)    | Sets data bit 5 word 1 - Forces the interface and control assembly to perform a self-test of the radar system. No effect in comm mode.  |
| KU RDR SELF TEST OFF<br>(14017)   | Resets data bit 5 word 1 - Terminates the self-test function whether or not the radar self-test is complete.  |
| KU-A MODLN CONT - AUTO<br>(14018) | Resets data bits 6 and 7 word 1 - Configures the return link carrier on/off and modulation on/off according to the state of the primary acquisition bit (data bit 8 word 1) and the antenna steering mode; i.e., GPC, GPC DESIG, AUTO TRACK, or MAN SLEW.                                 |
| KU-A MODLN CONT - ON<br>(14019)   | Sets data bits 6 and 7 word 1 - Configures modulation on, but the return link carrier on/off is determined by the state of the primary acquisition bit (data bit 8 word 1) and the antenna steering mode. See Table 9-9.  |
| KU-A MODLN CONT - OFF<br>(14020)  | Resets data bit 6 and sets data bit 7 word 1 - Configures modulation off, but the return link carrier on/off is determined by the state of the primary acquisition bit (data bit 8 word 1) and the antenna steering mode. See Table 9-9.  |
| KU PRI ACQ MODE - ON<br>(14021)   | Resets data bit 8 word 1 - Configures the system to radiate through the wide beam antenna and receive through the narrow beam antenna. When a TDRS signal is being tracked, transmit and receive through the narrow beam antenna. (Not used.) See Table 9-9.                              |
| KU PRI ACQ MODE - OFF<br>(14022)  | Sets data bit 8 word 1 - Configures the system in alternate acquisition mode; i.e., transmit and receive through the narrow beam antenna. Carrier on/off and modulation on/off are determined by data bits 7 and 8 and the antenna steering mode. (Normal operating mode.) See Table 9-9. |
| KU ANT INTL STAB - ON<br>(14023)  | Resets data bit 10 word 1 - Enables inertial pointing of the antenna in GPC designate antenna steering mode only.   |

---

|                                    |  |
|------------------------------------|--|
| KU ANT INTL STAB - OFF<br>(14024)  | Sets data bit 10 word 1 - Enables body referenced pointing of the antenna in GPC designate antenna steering mode only.   |
| KU FWD LK MODE 1 [216]<br>(14025)  | Sets data bit 11 word 1 - Configures the communications signal processor to receive and decommutate the 216-kbps forward link data. [ The 216-kbps forward link is the normal Ku-Band Uplink Mode ]                              |
| KU FWD LK MODE 2 [72]<br>(14026)   | Resets data bit 11 word 1 - Configures the communications signal processor to throughput the 72 kbps to the S-band network signal processor.   |
| KU RADAR RNG THLD - VAR<br>(14027) | Resets data bit 12 word 1 - Configures the radar receiver AGC as a function of the range to the target (normal operating mode).  |
| KU RADAR RNG THLD - FIX<br>(14028) | Sets data bit 12 word 1 - Configures the radar at a threshold to aid in detecting a target in clutter; i.e., a noisy environment, as with the Earth behind the target. (This function has not been implemented in the hardware.) |
| KU OBSC OVRD - OFF<br>(14029)      | Resets data bit 13 word 1 - Configures the system so that the TWT will be turned off whenever the antenna is pointing into the obscuration zone (normal mode).   |
| KU OBSC OVRD - ON<br>(14030)       | Sets data bit 13 word 1 - Configures the system so that the TWT will be enabled to transmit even if the antenna is pointed into the obscuration zone. This function is disabled in radar self-test mode.                         |
| KU TWTA - ON<br>(14031)            | Resets data bit 14 word 1 - Enables the TWT to transmit when not pointing into the obscuration zone (normal operating mode).   |
| KU TWTA - OFF<br>(14032)           | Sets data bit 14 word 1 - Prevents the TWT from transmitting.  |
| MASK SELECT - BETA<br>(14034)      | Sets data bit 15 word 1 - Selects the beta-only mode. In this mode the TWT will be shut off when the antenna beta angle is greater (positively) than the selected beta angle.  |

---

|  |  |
|--|--|
| MASK SELECT - BETAMASK<br>(14035)            | Resets data bit 15 word 1 - Selects the beta + mask mode. In this mode, the TWT will be shut off when the antenna beta angle is greater (positively) than the selected beta angle and the antenna line of sight is pointing within the Ku-band obscuration zone. |
| KU-BD RF ZONE 1 ENA<br>(14037)               | Enables RF Protect Box #1  |
| KU-BD RF ZONE 1 INH<br>(14038)               | Inhibits RF Protect Box #1   |
| AUTO KU-BD TO S-BD H/O<br>ENABLE<br>(14039)  | Enables the automatic handover from Ku-band to S-band when the Ku data present signal goes low (0) for 5 seconds.  |
| AUTO KU-BD TO S-BD H/O<br>INHIBIT<br>(14040) | Inhibits the handover from Ku-band to S-band.  |
| AUTO S-BD TO KU-BD H/O<br>ENABLE<br>(14041)  | Enables the Auto Handover from S-band to Ku-band when Ku data present signal is high (1), the Ku signal strength is greater than about -100 dB, and the Ku forward link has been stable for 15 seconds.  |
| AUTO S-BD TO KU-BD H/O<br>Inhibit<br>(14042) | Inhibits the automatic handover from S-band to Ku-band.  |
| KU-BD RF ZONE 2 ENA<br>(14043)               | Enables RF Protect Box #2  |
| KU-BD RF ZONE 2 INH<br>(14044)               | Inhibits RF Protect Box #2   |
| KU-BD RF ZONE 3 ENA<br>(14045)               | Enables RF Protect Box #3  |
| KU-BD RF ZONE 3 INH<br>(14046)               | Inhibits RF Protect Box #3   |
| KU-BD RF ZONE 4 ENA<br>(14047)               | Enables RF Protect Box #4  |



KU-BD RF ZONE 4 INH            Inhibits RF Protect Box #4  
(14048)

**9.9.1.3 EA-1 to SM GPC Status Words**

Ku-band comm/radar system status and data are telemetered to the ground in the SM downlist (via MDM PF1) and operational instrumentation (OI) downlink. The GNC GPC acquires Ku-band system status and data (via MDM FF3) when the rendezvous radar software is active. Selected data are displayed onboard to aid the crew in system operation, and certain radar status/data acquired by the rendezvous radar software are downlinked in the GNC downlist. Ten-16 bit Data Words are transmitted to both the SM and GNC GPCs via the PF1 and FF3 MDMs.

Use Table 9-11, Table 9-12 and Table 9-13 to find a “bit by bit” description of each of the 10 Data Words. Briefly, the Ten-16 bit Data Words sent to the SM GPC are composed of the following:

WORD

1. Ku-Band Configuration
2. Ku-Band Configuration
3. AZIMUTH ANGLE            V74H2618J
4. ELEVATION ANGLE        V74H2619J
5. RANGE RATE            V74R2621J
6. NOT DOWNLINKED
7. RANGE            V74U2623J
8. RANGE            V74U2623J (repeat of 7)
9. AZIMUTH ANGLE RATE        V74R2626J
10. ELEVATION ANGLE RATE    V74R2628J

**Table 9-11. SM/GNC downlist telemetry - Status Word 1**

| Bit | Function                                 | Logic state 1 | MSID (SM) | MSID (GNC) |
|-----|--|---------------|-----------|------------|
| 1-3 | SYNC                                     | -             | -         | -          |
| 4   | COMM A/RADAR MODE (CR)                   | Radar         | V74X2583J | V74X2883B  |
| 5   | ANTENNA STEERING AUTO MODE (CR)          | When true     | V74X2584J | V74X2884B  |
| 6   | ANTENNA STEERING GPC DESIGNATE MODE (CR) | When true     | V74X2585J | V74X2885B  |
| 7   | ANTENNA STEERING GPC ACQ MODE (CR)       | When true     | V74X2586J | V74X2886B  |

|    |                                 |               |           |           |
|----|---------------------------------|---------------|-----------|-----------|
| 8  | PARITY ERROR (CR)               | When true     | V74X2587J | V74X2887B |
| 9  | SYNC ERROR (CR)                 | When true     | V74X2588J | V74X2888B |
| 10 | VALIDITY ERROR (CR)             | When true     | V74X2589J | V74X2889B |
| 11 | RADAR ANGLE DATA GOOD (R)       | When true     | V74X2590J | V74X2890B |
| 12 | RADAR ANGLE RATE DATA GOOD (R)  | When true     | V74X2591J | V74X2891B |
| 13 | RADAR SELF-TEST IN PROGRESS (R) | When true     | V74X2592J | V74X2892B |
| 14 | Ku A/B SELECT (C)               | Ku B          | V74X2593J | V74X2893B |
| 15 | RADAR THRESHOLD VAR/FIX (R)     | Fix           | V74X2594J | V74X2894B |
| 16 | OBSCURATION OVERRIDE (CR)       | When true     | V74X2595J | V74X2895B |
| 17 | SPARE                           | -             |           | -         |
| 18 | SPARE                           | -             |           | -         |
| 19 | SPARE                           | -             |           | -         |
| 20 | PARITY                          | As applicable |           | -         |

C = Comm; R = Radar.

**Table 9-12. SM/GNC downlist telemetry - Status Word 2**

| Bit | Function                       | Logic state 1 | MSID (SM) | MSID (GNC) |
|-----|--------------------------------|---------------|-----------|------------|
| 1-3 | SYNC                           | -             |           |            |
| 4   | SEARCH (CR)                    | When true     | V74X2601J | V74X2901B  |
| 5   | DETECT (CR)                    | When true     | V74X2602J | V74X2902B  |
| 6   | TRACK (CR)                     | When true     | V74X2603J | V74X2903B  |
| 7   | OPERATE (CR)                   | When true     | V74X2604J | V74X2904B  |
| 8   | EA1 RADAR TEST STATUS (R)      | Pass          | V74X2605J | V74X2905B  |
| 9   | DA RADAR TEST (R)              | Pass          | V74X2606J | V74X2906B  |
| 10  | EA2 RADAR TEST STATUS (R)      | Pass          | V74X2607J | V74X2907B  |
| 11  | RADAR SYSTEM TEST STATUS (R)   | Pass          | V74X2608J | V74X2908B  |
| 12  | TDRS WEST SELECTED (C)         | When true     | V74X2609J | V74X2909B  |
| 13  | TDRS EAST SELECTED (C)         | When true     | V74X2610J | V74X2910B  |
| 14  | SPARE                          | -             |           | -          |
| 15  | FWD LINK DATA FRAME SYNC (C)   | When true     | V74X2612J | V74X2912B  |
| 16  | DATA PRESENT (C)               | When true     | V74X2613J | V74X2913B  |
| 17  | SCAN WARN LIMIT (CR)           | When true     | V74X2615J | V74X2914B  |
| 18  | RADAR RANGE DATA GOOD (R)      |               |           | V74X2915B  |
| 19  | RADAR RANGE RATE DATA GOOD (R) | When true     | V74X2616J | V74X2916B  |
| 20  | PARITY                         | As applicable |           |            |

C = Comm; R = Radar.

**Table 9-13. SM/GNC downlist telemetry - Status words 3 to 10**

| Bit no.   | Word 3<br>(1) (2) (3)<br>Radar/comm<br>azimuth angle<br>(deg) | Word 4<br>(1) (3)<br>Radar/comm<br>elevation angle<br>(deg) | Word 5<br>(1)<br>Radar range<br>rate wd1<br>(FPS) | Word 6<br>(1)<br>Radar range<br>rate wd2<br>(FPS) | Word 7<br>(1)<br>Radar range<br>wd1<br>(ft) | Word 8<br>(1)<br>Radar range<br>wd2<br>(ft) | Word 9<br>(1)<br>Azimuth angle<br>rate<br>(deg/s) | Word 10<br>(1)<br>Elevation angle<br>rate<br>(deg/s) |
|-----------|---|---|---|---|---|---|---|--|
| 1         | Sync  | Sync  | Sync  | Sync  | Sync  | Sync  | Sync  | Sync   |
| 2         | Sync  | Sync  | Sync  | Sync  | Sync  | Sync  | Sync  | Sync   |
| 3         | Sync  | Sync  | Sync  | Sync  | Sync  | Sync  | Sync  | Sync   |
| 4         | +/-(-2)   | +/-(-2)   | +/-(-2)   | 0 not used  | 1,310,720                                   | 20  | +/-(-2)   | +/-(-2)  |
| 5         | 180   | 90  | 819.2   | 0 not used  | 655,360                                     | 10  | 8.192   | 8.192  |
| 6         | 90  | 45  | 409.6   | 0 not used  | 327,680                                     | 5   | 4.096   | 4.096  |
| 7         | 45  | 22.5  | 204.8   | 0 not used  | 163,840                                     | 2.5   | 2.048   | 2.048  |
| 8         | 22.5  | 11.25   | 102.4   | 0 not used  | 81,920                                      | 1.25  | 1.024   | 1.024  |
| 9         | 11.25   | 5.625   | 51.2  | 0 not used  | 40,960                                      | 0.625                                       | 0.512   | 0.512  |
| 10        | 5.625   | 2.8125  | 25.6  | 0 not used  | 20,480                                      | 0.3125                                      | 0.256   | 0.256  |
| 11        | 2.8125  | 1.40625   | 12.8  | 0 not used  | 10,240                                      | 0 not used                                  | 0.128   | 0.128  |
| 12        | 1.40625   | 0.703125  | 6.4   | 0 not used  | 5,120                                       | 0 not used                                  | 0.064   | 0.064  |
| 13        | 0.703125  | 0.3515625   | 3.2   | 0 not used  | 2,560                                       | 0 not used                                  | 0.032   | 0.032  |
| 14        | 0.3515625   | 0.17578125  | 1.6   | 0 not used  | 1,280                                       | 0 not used                                  | 0.016   | 0.016  |
| 15        | 0.17578125  | 0.087890625   | 0.8   | 0 not used  | 640   | 0 not used                                  | 0.008   | 0.008  |
| 16        | 0.087890625   | 0.0   | 0.4   | 0 not used  | 320   | 0 not used                                  | 0.004   | 0.004  |
| 17        | 0.0   | 0.0   | 0.2   | 0 not used  | 160   | 0 not used                                  | 0.002   | 0.002  |
| 18        | 0.0   | 0.0   | 0.1   | 0 not used  | 80  | 0 not used                                  | 0.001   | 0.001  |
| 19        | 0.0   | 0.0   | 0.0   | 0 not used  | 40  | 0 not used                                  | 0.0   | 0.0  |
| 20        | Parity  | Parity  | Parity  | Parity  | Parity                                      | Parity                                      | Parity  | Parity   |
| MSID(SM)  | V74H2618J   | V74H2619J   | V74R2621J   | -   | V74U2623J                                   |   | V74R2626J   | V74R2628J  |
| MSID(GNC) | V74H2918B   | V74H2920B   | V74R2922B   | -   | V74H2924B                                   | V742925B                                    | V74R2926B   | V74R2928B  |

**9.9.1.3.1 Status Word 1 Description**

|   |  |
|---|--|
| Bit 4 (comm/radar) (O/1)<br>(V74X2583J)   | Indicates Ku-band system operating mode.   |
| Bits 5, 6, 7 (GPC, GPC DESIG,<br>AUTO TRACK)<br>(V74X2584J, V74X2585J,<br>V74X2586J)  | Indicates which antenna steering mode has been selected.   |
| Bits 8, 9, 10 (parity, sync,<br>validity error)<br>(V74X2587J, V74X2588J,<br>V74X2589J)   | Indicates a parity, sync, or validity error has been detected in the five data words from the SM GPC to the interface and control assembly over the channel 1 SIO. |
| Bits 11, 12 (radar angle, angle<br>rate data good)<br>(V74X2590J, V74X2591J)  | Indicates that angle and angle rate tracking circuits in the Radar Signal Processor are locked up and tracking the received radar signal.                          |
| Bit 13 (radar self test)<br>(V74X2592J)   | Indicates the radar self-test is in progress.  |
| Bit 14 (Ku A/B select)(O/1)<br>(V74X2593J)  | This is an echo of the Ku-band system selected in the Ku-band antenna control word.  |
| Bits 15, 16, 17, 18 (radar<br>threshold VAR/FIX,<br>obscuration override, TWT off,<br>Beta Mode)<br>(V74X2594J, V74X2595J,<br>V74K2644J, V74K2645J) | These are echoes of the state commanded or, in other words, stimuli in the Ku-band antenna control word.   |

**9.9.1.3.2 Status Word 2 Description**

|                               |  |
|-------------------------------|--|
| Bit 4 (search)<br>(V74X2601J) | Indicates that the Ku-band antenna is being driven in a spiral scan pattern. Interrupting the scan (antenna steering mode change or a detect) will abort the search scan and cause the signal to go low. |
| Bit 5 (detect)<br>(V74X2602J) | Indicates that the received signal has exceeded the detection threshold.   |

|  |   |
|--|---|
| Bit 6 (track)<br>(V74X2603J)   | In GPC and AUTOTRACK, indicates that the signal tracking servo circuits are closed, indicating angle tracking in comm mode and range, range rate, angle, and angle rate tracking in radar mode. In GPC DESIGNATE and MANUAL SLEW, this indicates signal detection in comm mode and range and range rate tracking in radar mode. |
| Bit 7 (operate)<br>(V74X2604J)   | Indicates that the Ku-band system is fully deployed, the TWT is warmed up, and no faults have been detected; therefore, high voltage is applied and the antenna has been initialized; i.e., encoder readout indicates azimuth and elevation angles.   |
| Bits 8, 9, 10 (radar self-test results, EA-1, DA, EA-2)<br>(V74X2605J, V74X2606J, V74X2607J) | Indicate that the interface and control assembly, deployed assembly, and Radar Signal Processor have passed/failed the radar self-test.   |
| Bit 11 (radar self-test system result)<br>(V74X2608J)  | This is an "AND" of bits 8, 9, and 10 and indicates that all three LRUs passed or one or more LRUs failed the radar self-test.  |
| Bits 12, 13 (TDRS west/east selected)<br>(V74X2609J/V74X2610J)                               | This indicates that TDRS west/east has been selected by the Interface and Control Unit internal logic.  |
| Bit 15 (forward link frame sync)<br>(V74X2612J)  | Indicates that the Communications Signal Processor has acquired the forward link and is locked up and tracking the frame sync pattern. This is functional only in 216-kbps (mode 1) forward link mode.  |
| Bit 16 (data present)<br>(V74X2613J)   | Indicates comm carrier detect (COSTAS LOCK), data detect (data on carrier), and, if operating in the spread spectrum mode, PN lock.   |
| Bit 17 (scan warning limit)<br>(V74X2614J)   | Indicates that the antenna is pointing into the obscuration zone (the area enclosed by the dashed line on the AM display).  |
| Bits 18, 19 (radar range, range rate data good)<br>(V74X2615J, V74X2616J)                    | Indicates that range and range rate tracking circuits in the Radar Signal Processor are locked up and tracking the received radar signal.   |

### 9.9.1.3.3 Data words 3 through 10 Description

Data words 3 and 4 are the actual antenna AZ and EL angles in either Comm or Radar Mode. Data words 5 through 10 provide measured range rate, range, and angle rate data in the radar mode. Data word 6 is all zeros.

In Comm Mode, Data words 5 through 10 will be all zeros. EA-1 to GCIL Interfaces

EA-1 is designed to receive GCIL (and Panel Switch) inputs thru a Discrete Input/Output card. GCIL commands duplicate the communication mode functions of the crew controls.

Table 9-14 is a listing of GCIL commands available to the ground controller.

|                                |  |
|--------------------------------|--|
| KU COMM A PWR - OFF<br>(4101)  | Removes the enabling signal (standby/on), thus removing power from the Ku-band system (Ku fault message to the crew).  |
| KU COMM A PWR - ON<br>(4102)   | Applies the enabling signal to the interface and control assembly that in turn, enables the Communications Signal Processor and the deployed assembly. Begins initializing the system and starts a 3.5-minute timer to allow the TWT to warm up.   |
| KU COMM A PWR - STBY<br>(4103) | Does the same thing as the "on" signal except it does not apply power to the antenna gimbals or comm signal processor and does not allow the TWT to radiate after the 3.5-minute warmup.   |
| KU A ANT - GPC<br>(4104)       | Selects GPC antenna steering mode. Initial antenna pointing angles are commanded by the SM GPC AM program. Antenna is inertially stabilized. Antenna angle search is initiated by the GPC if a signal is not detected within 20 seconds (variable) after the antenna is pointed to the commanded angles. When a signal is detected, automatic angle tracking will begin. |
| KU A ANT - GPC DESIG<br>(4105) | Antenna pointing angles are commanded by the SM GPC AM program. The antenna can be inertially or body stabilized as directed by a discrete command from the GPC. Angle search and track are inhibited in this mode.  |

**Table 9-14. GCIL commands**

| DSM    | OPS nomenclature     | MDM | Reset    | Set      |
|--------|----------------------|-----|----------|----------|
| 4101   | KU COMM A PWR - OFF  | PF1 | 710901FF | 79090003 |
|        |                      | PF2 | 710A01FF | 790A0003 |
| 4102   | KU COMM A PWR - ON   | PF1 | 710901FF | 79090001 |
|        |                      | PF2 | 710A01FF | 790A0001 |
| 4103   | KU COMM A PWR - STBY | PF1 | 710901FF | 79090002 |
|        |                      | PF2 | 710A01FF | 790A0002 |
| 4104   | KU A ANT - GPC       | PF1 | 710901FF | 79090007 |
|        |                      | PF2 | 710A01FF | 790A0007 |
| 4105   | KU A ANT - GPC DESIG | PF1 | 710901FF | 79090008 |
|        |                      | PF2 | 710A01FF | 790A0008 |
| 4106   | KU A ANT - AUTO      | PF1 | 710901FF | 7909001B |
|        |                      | PF2 | 710A01FF | 790A001B |
| 4107   | KU A ANT - MAN SLEW  | PF1 | 710901FF | 79090009 |
|        |                      | PF2 | 710A01FF | 790A0009 |
| 4121   | KU HDR - OFF         | PF1 | 710901FF | 79090010 |
|        |                      | PF2 | 710A01FF | 790A0010 |
| 4122   | KU HDR - PL MAX      | PF1 | 710901FF | 7909000F |
|        |                      | PF2 | 710A01FF | 790A000F |
| 4123   | KU HDR - PL INT      | PF1 | 710901FF | 79090014 |
|        |                      | PF2 | 710A01FF | 790A0014 |
| 4124   | KU HDR - PL ANLG     | PF1 | 710901FF | 79090012 |
|        |                      | PF2 | 710A01FF | 790A0012 |
| 4125   | KU HDR - PL DIGI     | PF1 | 710901FF | 79090013 |
|        |                      | PF2 | 710A01FF | 790A0013 |
| 4126   | KU HDR - TV          | PF1 | 710901FF | 79090011 |
|        |                      | PF2 | 710A01FF | 790A0011 |
| 4131   | KU LDR - OFF         | PF1 | 710901FF | 79090015 |
|        |                      | PF2 | 710A01FF | 790A0015 |
| 4136   | KU LDR - MMU1        | PF1 | 710901FF | 79090017 |
|        |                      | PF2 | 710A01FF | 790A0017 |
| 4133   | KU LDR - MMU2        | PF1 | 710901FF | 79090018 |
|        |                      | PF2 | 710A01FF | 790A0018 |
| 4134   | KU LDR - PL DIGI     | PF1 | 710901FF | 79090016 |
|        |                      | PF2 | 710A01FF | 790A0016 |
| 4135   | KU LDR - PL INT      | PF1 | 710901FF | 7909001D |
|        |                      | PF2 | 710A01FF | 790A001D |
| * 4140 | KU/S FAIL SAFE - ENA | PF1 | 710901FF | 79090019 |
|        |                      | PF2 | 710A01FF | 790A0019 |
| * 4141 | KU/S FAIL SAFE - DIS | PF1 | 710901FF | 7909001A |
|        |                      | PF2 | 710A01FF | 790A001A |

\* Operationally, GCIL Fail Safe Commands are not used, due to the advantage of the “S to Ku” and “Ku to S” Uplink Auto-handover SM Software

---

|                                |  |
|--------------------------------|--|
| KU A ANT - AUTO<br>(4106)      | Inertially stabilized antenna pointing. The ground cannot point the antenna in this mode; however, the slew switches are enabled as long as the antenna is not tracking. If a signal is detected, the antenna will lock up and track. Angle search can only be initiated by the panel switch in this mode. |
| KU A ANT - MAN SLEW<br>(4107)  | Body referenced antenna pointing is provided in this mode. Slew switches are enabled, but search and track functions are inhibited.  |
| KU HDR - OFF<br>(4121)         | No high data rate input is selected to the communications signal processor. The Ku-band system will be in FM mode.   |
| KU HDR - PL MAX<br>(4122)      | Selects high rate digital data from the payload distribution panel. The Ku-band system will be in PM mode.   |
| KU HDR - PL INT<br>(4123)      | Selects data output from the payload interrogator. The Ku-band system will be in FM mode.  |
| KU HDR - PL ANLG<br>(4124)     | Selects analog data from the payload distribution panel. The Ku-band system will be in FM mode.  |
| KU HDR - PL DIGI<br>(4125)     | Selects digital data from the payload distribution panel. The Ku-band system will be in FM mode.   |
| KU HDR - TV<br>(4126)          | Selects the CCTV output from the video switching unit. The Ku-band system will be in FM mode.  |
| KU LDR - OFF<br>(4131)         | No low data rate input is selected to the communications signal processor.   |
| KU LDR - MMU1<br>(4136)        | Selects Solid State Recorder 1.  |
| KU LDR - MMU2<br>(4137)        | Selects Solid State Recorder 2.  |
| KU LDR - PL DIGI<br>(4134)     | Selects low data rate digital data from the payload distribution panel.  |
| KU LDR - PL INT<br>(4135)      | Selects data output from the payload interrogator.   |
| KU/S FAIL SAFE - ENA<br>(4140) | (Not Used) Enables the Ku-band to S-band fail-over circuit in the GCIL. GCIL will execute:   |



KU/S fail safe - ENABLE

S-band control - COMMAND

NSP source - KU

Ku-band data - GOOD

Otherwise, the Ku-band comm system will fail to S-band approximately 13 seconds after data good goes low.

The GCIL circuit was implemented so that if power is removed from the driver (if COMM STBY or RADAR ON/STBY go high) the fail safe circuit will be disabled.

KU/S FAIL SAFE - DIS  
(4141)

(Not Used) Disables the fail to S-band circuit in the GCIL.

## 9.9.2 Crew Interfaces with EA-1

The Crew interfaces with Ku-Band EA-1 through Switch Manipulation, viewing Ku-Band telemetry through Digital Panels A2, SPEC 2011, SPEC 72, and analog telemetry through A1U.

### 9.9.2.1 Panel R14

Figure 9-9 displays Panel R14.

|                 |  |
|-----------------|--|
| cb 23 ELEC      | Provides main B 28 V dc power to the Ku-band power switch, the RDR/COMM, ON/STBY GCIL command drivers, the Radar Signal Processor, and DEA through midpower control assembly no. 2. Also provides main C 28 V dc power to the EA-1 through forward power control assembly no. 3. |
| cb 24 ANT HTR   | Provides main B 28 V dc power from mid-power control assembly no. 2 to heaters in the DEA (2), A gimbal, B gimbal, rate sensor assembly, and antenna feed.   |
| cb 25 CABLE HTR | Not used.  |
| cb 31 SIG PROC  | Provides main C 28 V dc power to the Ku-band power switch and SPA.   |

### 9.9.2.2 Panel A1U

Figure 9-10 displays Figure A1U.

- |                         |   |
|-------------------------|---|
| sw 1 S-BD PM/KU/S-BD PL | Selects which source of received signal (AGC) drives the signal strength meter; S-band PM transponder/Ku-band receiver (comm or radar)/S-band payload interrogator.   |
| sw 2 AZIMUTH SLEW       | Powered when the Ku-band power switch (S12) is ON. Enables antenna slewing (left/ right) in azimuth when in the MAN SLEW or AUTO TRACK position (when not angle tracking) of the antenna steering rotary switch (S7). |
| sw 3 ELEVATION SLEW     | Powered when the Ku-band power switch (S12) is ON. Enables antenna slewing (up/ down) in elevation when in the MAN SLEW or AUTO TRACK position (when not angle tracking) of the antenna steering rotary switch (S7)   |



**Figure 9-9. Panel R14 Active Ku-Band Circuit Breakers**



**Figure 9-10. Panel A1U**

sw 4 SLEW RATE

Powered when the Ku-band power switch (S12 is ON). Selects the azimuth and elevation slew rate, either FAST (20 deg/s) or SLOW (0.4 deg/s).

sw 6 CONTROL

In panel mode, all panel switches are enabled. In command mode, command drivers in the GCIL are enabled for the following functions in comm mode only; RADAR is not commandable.

Antenna steering (rotary)

sw 7 GPC/GPC DESIG/AUTO TRACK/MAN SLEW

Powered when the Ku-band power switch (S12) is ON. Selects one of four steering modes for antenna operation.

GPC - Initial antenna pointing angles are commanded by the SM GPC antenna management program. Antenna pointing is inertially stabilized. Antenna angle search is initiated by the GPC if a signal is not detected within 20 seconds (variable) after the antenna is pointed to the commanded angles. When a signal is detected, automatic angle tracking begins.

GPC DESIG - Antenna pointing angles are commanded by the SM GPC antenna management program. The antenna can be inertially or body stabilized as directed by a discrete command from the GPC. Angle search and track are inhibited in this mode.

AUTO TRACK - Inertially stabilized antenna pointing is provided when using the azimuth and elevation slew switches. Angle tracking will be enabled if a signal is detected while slewing at the slow rate but will be disabled when slewing at the high rate. Antenna search is initiated by the SEARCH switch (S8).

MAN SLEW - Body referenced antenna pointing is provided when using the azimuth and elevation slew switches. Angle search and track are inhibited in this mode.

sw 8 SEARCH

Powered when the Ku-band power switch (S12) is ON. Initiates a spiral scan search pattern about the antenna line of sight in auto track mode only.

sw 12 ON/STBY/OFF

In the ON position, provides main B power to the following.

- Panel A2 digital meter
- Azimuth, elevation, and rate slew switches
- Antenna steering mode switch (rotary)
- SEARCH switch
- MODE switch

In the STANDBY position, provides main B power to the MODE switch (S13) for radar/ comm standby (minimum power usage) operation.

In the OFF position, all power is removed from the Ku-band system. Deployed assembly heater power will remain ON as long as cb 24 on panel R15 is closed.

sw 13 RDR COOP/RDR  
PASSIVE/COMM

In either radar cooperative (transponder mode - not used) or passive (skintrack mode - normal radar mode) if the power switch is ON, provides main B power to the line-of-sight rates meter and the enabling discretes to the Interface and Control Unit, and for relay to the Radar Signal Processor, and the DEA. In the communications position, if the power switch is ON, provides main C power to the HIGH and LOW DATA RATE switches (S15 and S16) and main B power for the enabling discretes to the Interface and Control Unit, and for relay to the Communications Signal Processor, and the DEA.

sw 14 RADAR OUTPUT

In either radar mode if power switch is ON, selects the TWT amplifier output level.

HIGH - Maximum output power (approximately +45 dBm)

MED - Medium output power (approximately +33 dBm)

LOW - Low output power (approximately +21 dBm)

sw 15 HIGH DATA RATE

Selects one of five signal sources as the input to the Ku-band HDR channel (channel 3) as follows.

- TV - CCTV system
- PL DIGITAL - Digital data from the PL distribution panel
- PL ANALOG - Analog data from the PL distribution panel
- PL INTRG - Phase-modulated subcarrier(s) from the PL interrogator
- PL MAX - High rate digital data from the PL distribution panel
- OFF - No input selected

sw 16 LOW DATA RATE

Selects one of four signal sources as the input to the Ku-band LDR channel (channel 2) as follows.

- PL INTRG - Phase-modulated subcarrier(s) from the PL interrogator
- PL DIGITAL - Digital data from the PL distribution panel

- MMU 2 - Digital data from MMU 2
- MMU 1 - Digital data from MMU 1
- OFF - No input selected

### 9.9.2.3 Panel A2

Figure 9-11 displays Figure A2.

Switch 1 DIGI DISPLAY SELECT- Selects data input to the digital meters (M2).

R /  $\dot{R}$  - Selects range and range rate data (radar mode only).

EL/AZ - Selects line of sight pointing angles to TDRS/target in elevation and azimuth.

LAMP TEST - Selects a test mode for both digital displays which causes all numeric segments to be illuminated.

LED between the two R/R and EL/AZ digital Readouts - This LED will light when there is an internal failure within the A2 power or logic.

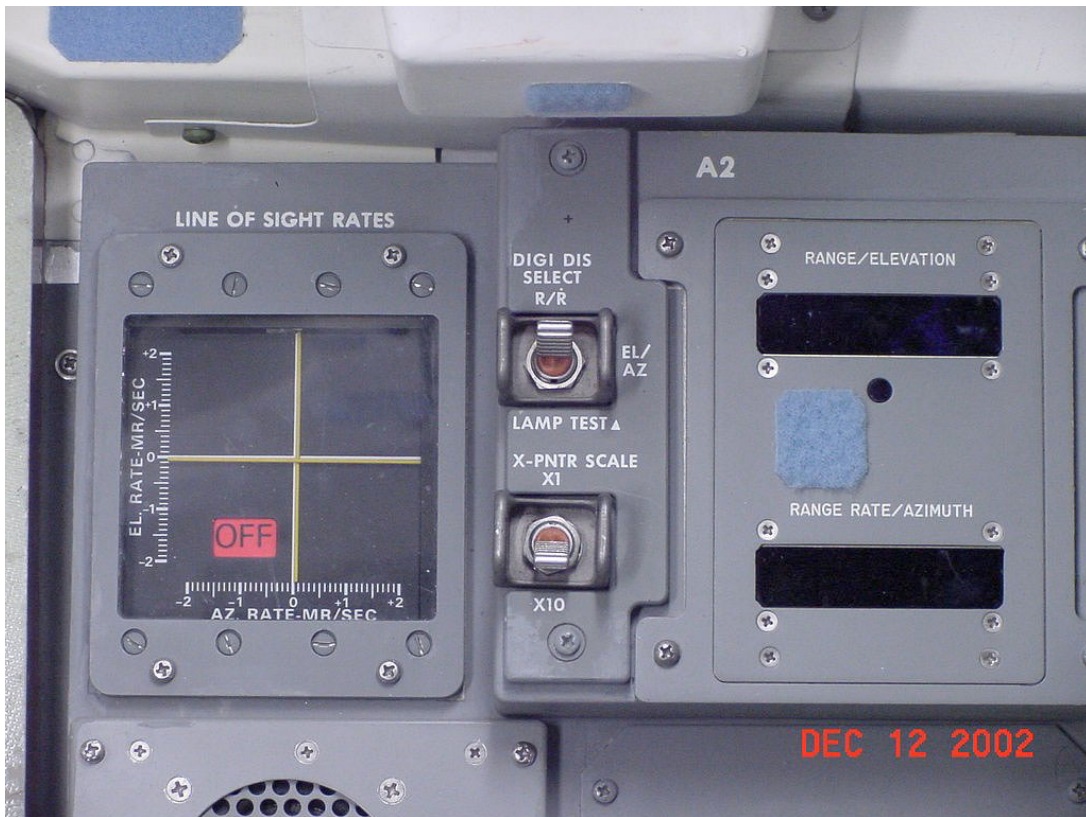
Switch 2 X-PNTR SCALE- Selects one of two elevation and azimuth inertial angle

| Parameter   | Units  | Measurement range | Decimal location | Minimum resolution | rates (milliradians/sec) as inputs to the crosspointer meter (M1). |
|---|--------|-------------------|------------------|--------------------|--|
| AZ  | Deg    | 0 - 204.7         | ±XXX.X           | 0.1°               | Selects a unity factor so the reads 0 to ±2 MR/SEC.                |
| EL  | Deg    | 0 - 102.3         | ±XXX.X           | 0.1°               |  |
| X1 - scale meter  | Kft    | R < 9.99          | X.XXO            | 10 ft              | Selects the scale so the meter 0 to ±20 MR/SEC.                    |
|   |        | 10 - 99.99        | XX.XX            | 10 ft              |  |
|   |        | 100 - 999.9       | XXX.X            | 100 ft             |  |
|   |        | 1000 < R          | XXXX.            | 1,000 ft           |  |
| Range* rate   | ft/sec | R < 999.9         | ±XXX.X           | 0.1 ft/sec         | Selects the scale so the meter 0 to ±20 MR/SEC.                    |
|   |        | 1000 < R          | ±XXXX.           | 1.0 ft/sec         |  |
| *Positive (+) indicates increasing range to the target.<br>Negative (-) indicates decreasing range to the target. |        |                   |                  |                    |  |

### LINE OF SIGHT RATES (M2)

Crosspointers indicate the relative motion between the orbiter and the radar target in milliradians/sec in elevation and azimuth.





**Figure 9-11. Panel A2**

**RANGE/ELEVATION**

Indicates range in thousands of feet (left justified with a floating decimal point) in radar mode if s1 is in R/Rdot position.

Indicates elevation angle in tenths of a degree in both radar and comm modes if s1 is in EL/AZ position.

**RANGE RATE/AZIMUTH**

Indicates range rate in tenths of a foot/sec for rates less than 1,000 ft/sec, and in feet/sec for rates greater than 1,000 ft/sec in radar mode if s1 is in R/Rdot position.

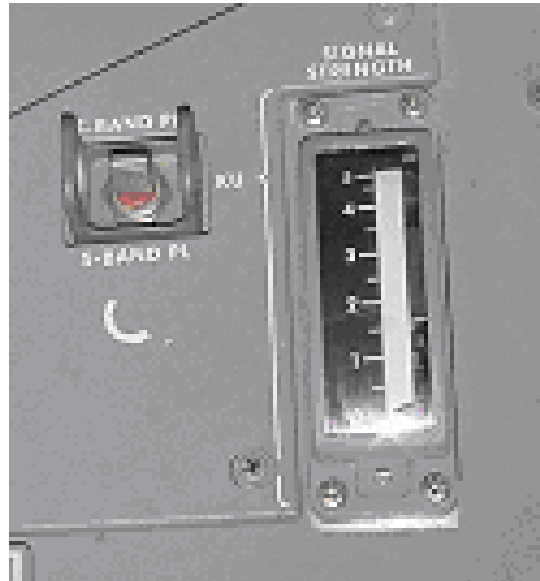
Indicates azimuth angle in tenths of a degree in both radar and comm modes if s1 is in EL/AZ position.



### 9.9.2.4 Panel A1

#### SIGNAL STRENGTH (M1)

Indicates the radar or communications received signal strength (0-5 V dc). Figure 9-12 display s1 in KU position Figure 9-12.



**Figure 9-12. A1U Signal Strength Meter**

#### Talk Backs (Figure 9-13)

EA-1 microprocessor outputs to the Discrete Input/Output card these indications to talkbacks. [Note, These talkbacks also indicate whether Self Test Passed or Failed].

#### SCAN WARN

Indicates that the antenna is pointing into the obscuration zone.

#### TRACK

Indicates EA-1 is "good" signal strength and uplink modulation.

#### SEARCH

Ku-Band is performing a search routine.



**Figure 9-13. A1U EA-1 Talkbacks**

### 9.9.2.5 SM SPEC 2011 Antenna

Figure 9-14 shows SPEC 2011 Antenna display.

|                    |   |
|--------------------|---|
| TDRS STATE VECTORS | Items 1-6 - The SM contains six TDRS vectors that can be assigned to the two available TDRS targets which are displayed on SPEC 201. Item x + A assigns the corresponding vector to target A. Item x + B assigns the corresponding vector to target B. (See SB 14, Antenna Management, for more details.) |
| RADAR RANGE        | Item 16 AUTO - Selects a search range determined by the SM GPC designated target range (normal operating mode).<br><br>Item 17 MIN - Selects a search range out to 2400 feet with azimuth and elevation angles equal to zero.   |
| SELF-TEST          | Item 7 - This is an enable/disable item that initiates a self-test in radar mode. Self-test is indicated by an asterisk (*). When item 7 is executed the second time (no asterisk), the radar self-test is terminated. Time to run self-test is 3 minutes. Normal operating mode is self-test off.        |
| I/O RESET KU       | Item 8 - Enables the serial input/output channel with the SM GPC through MDM PF1. The Ku-band system will normally be powered off when the SM GPC is initialized and, therefore, will be bypassed.  |



### 9.9.2.6 SM SPEC 076

Figure 9-15 shows SPEC 76.

|             |  |
|-------------|--|
| PA TEMP     | Indicates the temperature in the DEA in the vicinity of the TWT power amplifier. The same measurement is sent to the ground as "transmitter" temp. An SM alert occurs if the temperature exceeds 171° F. |
| GMBL TEMP   | Indicates the temperature of the A and B gimbal motors. An SM alert occurs if temperature A exceeds 150° F or if temperature B exceeds 166° F.   |
| GYRO TEMP   | Indicates the temperature of the A and B gyros in the rate sensor assembly. An SM alert occurs if the temperature exceeds 155° F.  |
| PWR OUT     | Indicates Ku-band RF output, nominally 20 W.   |
| FR SYNC     | Indicates that the Ku-band forward link is locked and the signal processor assembly is demultiplexing the 216-kbps data.   |
| MODE        | Indicates that the Ku-band is in either comm or radar mode.  |
| FAIL SAFE   | Indicates that the fail safe is enabled or inhibited. This function is not used.   |
| AUTO K TO S | Indicates that auto K to S handover is enabled or inhibited.   |
| AUTO S TO K | Indicates that auto S to K handover is enabled or inhibited.   |

| XXXX/XXX/076   |        | COMMUNICATIONS |        | XX X             | DDD/HH:MM:SS | DDD/HH:MM:SS |
|----------------|--------|----------------|--------|------------------|--------------|--------------|
| S - BAND PM    |        |                | XXXXXS |                  | KU - BAND    |              |
| FREQ           | XXS    | 1              | 2      | PA TEMP          | ±XXXXS       |              |
| ANT ELEC       | XXS    | XXS            | XXS    | GIMBAL TEMP A    | ±XXXXS       |              |
| XPNDR          | XXS    | XXS            | XXS    | B                | ±XXXXS       |              |
| PREAMP         | XXS    | XXS            | XXS    | GYRO TEMP        | ±XXXXS       |              |
| PWR AMPL       |        |                |        | PWR OUT          | XXS          |              |
| OPER           | XXS    | XXS            | XXS    | FRM SYNC         | XXXXS        |              |
| STBY           | XXXXXS | XXXXXS         | XXXXXS | MODE             | XXXXXS       |              |
| PWR OUT        | XXXXS  | XXXXS          | XXXXS  | FAIL SAFE        | XXXXS        |              |
| TEMP           | XXXXS  | XXXXS          | XXXXS  | AUTO K T O S     | XXX          |              |
| NSP            | 1      | 2              |        | AUTO S T O K     | XXX          |              |
| BIT SYNC       | XXXXS  | XXXXS          | XXXXS  | SSOR             | 1            | 2            |
| FRM SYNC       | XXXXS  | XXXXS          | XXXXS  | FRM SYNC         | XXXXS        | XXXXS        |
| BITE           | XXXXXS | XXXXXS         | XXXXXS | PROC STAT        | XXXXS        | XXXXS        |
| COMSEC BITE    | XXXXXS | XXXXXS         | XXXXXS | PWR LEVEL        | ±XX.XS       |              |
|                |        |                |        | STATUS           | X.XS         |              |
| UL DATA SOURCE |        | XXS            |        | GCIL CONFIG      | XXXXS        |              |
| DATA RATE XMIT |        | XXS            |        | CCTV CAMR OVRTMP | XXXXS        |              |
|                |        | XXS            |        |                  |              |              |
| CODING XMIT    |        | XXXXS          |        |                  |              |              |
|                |        | XXXXS          |        |                  |              |              |
|                |        | XXXXS          |        |                  |              |              |

Figure 9-15. SM SPEC 76 display

### 9.9.2.7 GNC Display SPEC 033

Figure 9-16 shows GNC SPEC 033.

RNDZ NAV ENA

Item 1 - This is an enable/disable item that controls the rendezvous navigation software in the Guidance and Navigation Computer (GNC) GPC.

KU ANT ENA

Item 2 - This is an enable/disable item that controls transfer of radar target position data from the GNC GPC to the SM GPC so that the AM program can compute estimated range and pointing angles to the target. (Item 1 must be active for this entry to be legal.) If disabled, the target defaults to TDRS.

RR XXXX

Indicates comm if Ku-band system is in comm mode; or in radar mode, STST if a self-test is in progress, and GPC, GDSG, ATRK, MSLW, antenna steering mode if it is not in self-test.

- RNG Indicates range to the target in thousands of feet.
- R Indicates opening (+) or closing (-) rate to the target in ft/sec.
- EL Indicates the elevation pointing angle to the target in degrees, + toward the nose, - toward the tail.
- AZ Indicates the azimuth pointing angle to the target in degrees, + toward the port wing, - toward the starboard wing.
- $\omega P$  Indicates the antenna line-of-sight elevation angle rate in milliradians/sec.
- $\omega R$  Indicates the antenna line-of-sight azimuth angle rate in milliradians/sec.

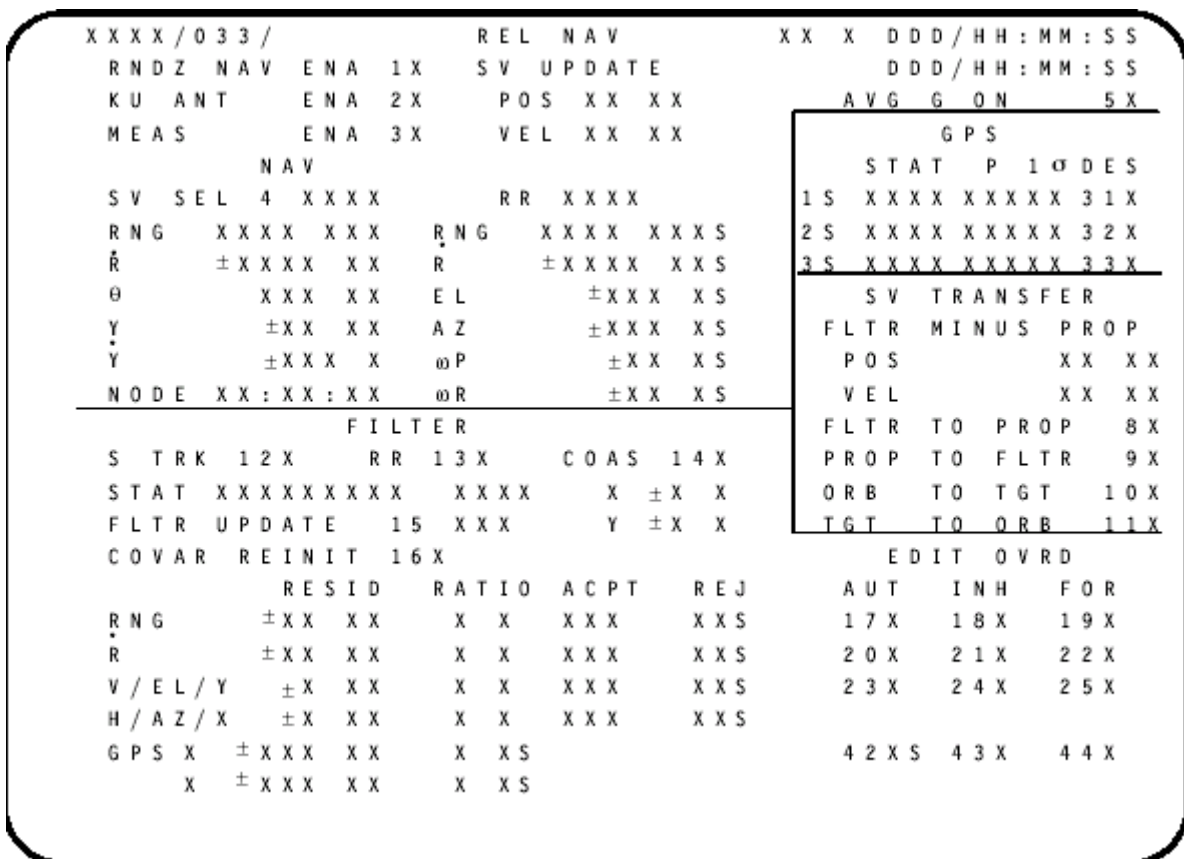
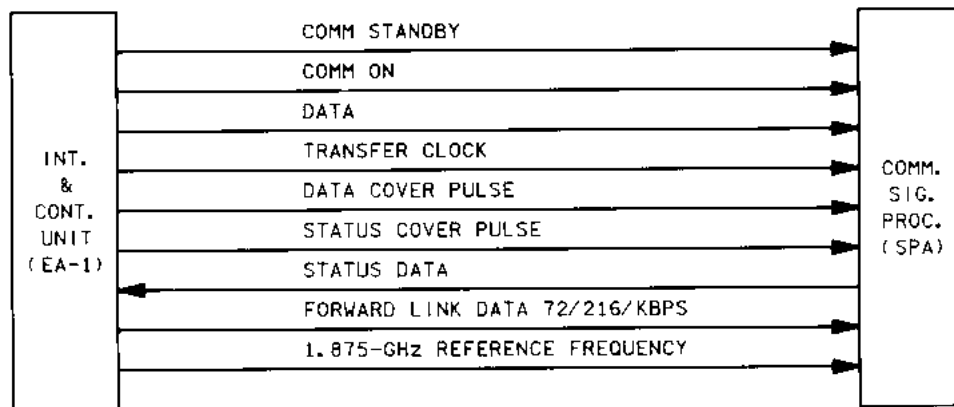


Figure 9-16. REL NAV display

### 9.9.3 EA-1 to SPA Interface

EA-1 to SPA Interface consist of several types of Discrete, Analog and Digital Serial I/O signals as shown in Figure 9-17. The serial I/O is a two-way channel: Control is sent from EA-1 to SPA, and status is sent from SPA to EA-1. The transfer clock (100 kbps) inputs/outputs data or status information in 8-bit bytes. The data cover pulse is high when data are sent from EA-1 to SPA. The status cover pulse is high when status information is sent from SPA to EA-1. The data transfer clock and the data/status cover pulse controls are contained in EA-1. A breakdown of the data/status serial I/O is shown in Table 9-15.

The SPA microprocessor is where the Primary and Alternate Mode protocols are “stored”. EA-1 will “tell” the SPA the Antenna Steering Mode (GPC, Manual, etc) and the Modulation Control (On, Off, Automatic); the SPA then directly controls MOD On/Off and TWT ENA COMM A (Carrier on/off).



**Figure 9-17. EA-1/SPA signal interfaces**

Signal definition is as follows.

|                |   |
|----------------|---|
| COMM STANDBY   | Communications Signal Processor is nonfunctional.   |
| COMM ON        | Communications Signal Processor is completely functional for selected high and low data rate modes.                                 |
| CONTROL WORD   | Serial I/O channel. Configuration and control data to the Communications Signal Processor (two 8-bit bytes).                        |
| TRANSFER CLOCK | 125-kHz clock in the Interface and Control Unit that clocks data or status information to/from the Communications Signal Processor. |

|                               |   |
|-------------------------------|---|
| DATA COVER PULSE              | When high, enables data to be shipped from the Interface and Control Unit to the Communications Signal Processor.               |
| STATUS COVER PULSE            | When high, enables status information to be shipped from the Communications Signal Processor to the Interface and Control Unit. |
| STATUS DATA                   | Serial I/O channel. Communications Signal Processor status information (one 8-bit byte).  |
| FORWARD LINK DATA             | Either 72-kbps or 216-kbps biphasic data from the Interface and Control Unit.   |
| 1.875-GHz REFERENCE FREQUENCY | This is the carrier used by the QPSK modulator to generate the return link carrier in PM mode.                                  |

**Table 9-15. (Serial I/O) EA-1 Control Word to SPA and SPA Status Word to EA-1**

| Control Word |     |                                 | Status Word |     |                              |
|--------------|-----|---------------------------------|-------------|-----|------------------------------|
| Byte         | Bit | Title                           | Byte        | Bit | Title                        |
| 1            | 1   | SPARE                           | 1           | 1   | SPARE                        |
|              | 2   | TDRS EAST SELECT                |             | 2   | SPARE                        |
|              | 3   | TDRS WEST SELECT                |             | 3   | SPARE                        |
|              | 4   | SPARE                           |             | 4   | FORWARD LINK DATA FRAME SYNC |
|              | 5   | Ku B/A SELECT                   |             | 5   | SPARE                        |
|              | 6   | SPARE                           |             | 6   | SPARE                        |
|              | 7   | MODULATION CONTROL 1 see note 1 |             | 7   | SPARE                        |
|              | 8   | MODULATION CONTROL 2            |             | 8   | SPARE                        |
| 2            | 1   | ENCODED MODE 1                  |             |     |                              |
|              | 2   | ENCODED MODE 2 see note 2       |             |     |                              |
|              | 3   | FORWARD LINK MODE 1/2 (216/72)  |             |     |                              |
|              | 4   | DATA PRESENT                    |             |     |                              |
|              | 5   | TRACK                           |             |     |                              |
|              | 6   | PRIMARY ACQUISITION MODE ON/OFF |             |     |                              |
|              | 7   | ID-BIT = "0"                    |             |     |                              |
|              | 8   | PERIOD = "1"                    |             |     |                              |

Note 1

|                    | Bits     |          |
|--------------------|----------|----------|
| Modulation control | <u>1</u> | <u>2</u> |
| AUTO               | 0        | 0        |
| OFF                | 0        | 1        |
| ON                 | 1        | 0        |
| AUTO               | 1        | 1        |

Note 2

|              | Bits     |          |
|--------------|----------|----------|
| Encoded mode | <u>1</u> | <u>2</u> |
| AUTO TRACK   | 0        | 0        |
| GPC          | 0        | 1        |
| MANUAL SLEW  | 1        | 1        |
| GPC DES      | 1        | 0        |

### 9.9.4 EA-1 to EA-2 Interface

Interface and Control Unit/Radar Signal Processor signal interfaces are shown in Figure 9-18. The Control Word from EA-1 to EA-2 contains five 8-bit bytes as shown in



Table 9-16. The Status Word from EA-2 to EA-1 contains eleven 8-bit bytes and is shown in Table 9-17.

Signal definition is as follows:

|                       |   |
|-----------------------|---|
| RADAR STANDBY         | Radar Signal Processor is nonfunctional.  |
| RADAR ON              | Radar Signal Processor is completely functional in the selected radar mode.   |
| RADAR POWER LOW       | The TWT output power is limited to 24 dB below the maximum TWT output.  |
| RADAR POWER MEDIUM    | The TWT output power is limited to 12 dB below the maximum TWT output.  |
| LOBING ENABLE         | Indicates the Radar Signal Processor has detected a target and this is the signal to enable antenna tracking (i.e., radar 0°/180° and $\Delta$ AZ/ $\Delta$ EL signals are provided to the Interface and Control Unit). |
| DATA                  | Serial I/O channel. Configuration and control data to the Radar Signal Processor (five 8-bit bytes).  |
| TRANSFER CLOCK        | 125 kHz clock in the Interface and Control Unit that clocks data or status information to/from the Radar Signal Processor.  |
| DATA COVER PULSE      | When high, enables data to be shipped from the Interface and Control Unit to the Radar Signal Processor.  |
| STATUS COVER PULSE    | When high, enables status information to be shipped from the Radar Signal Processor to the Interface and Control Unit.  |
| STATUS                | Serial I/O channel. Radar status information (11 8-bit bytes).  |
| RADAR SIGNAL STRENGTH | A measure of the radar received signal strength (AGC).  |
| ALPHA ERROR           | Measured alpha gimbal pointing angle error (derived from antenna lobing data).  |
| BETA ERROR            | Measured beta gimbal pointing angle error (derived from antenna lobing data).   |
| RDR LOBING AZ/EL      | Square wave at a frequency of PRF/68 (range - 4 Hz to 103 Hz).  |

|                    |  |
|--------------------|--|
| RDR LOBING 0°/180° | Square wave at a frequency of PRF/34 (range 8 Hz to 206 Hz).                               |
| 156 MHz REF FREQ   | This is the reference frequency used to mix the radar second IF down to a baseband signal. |

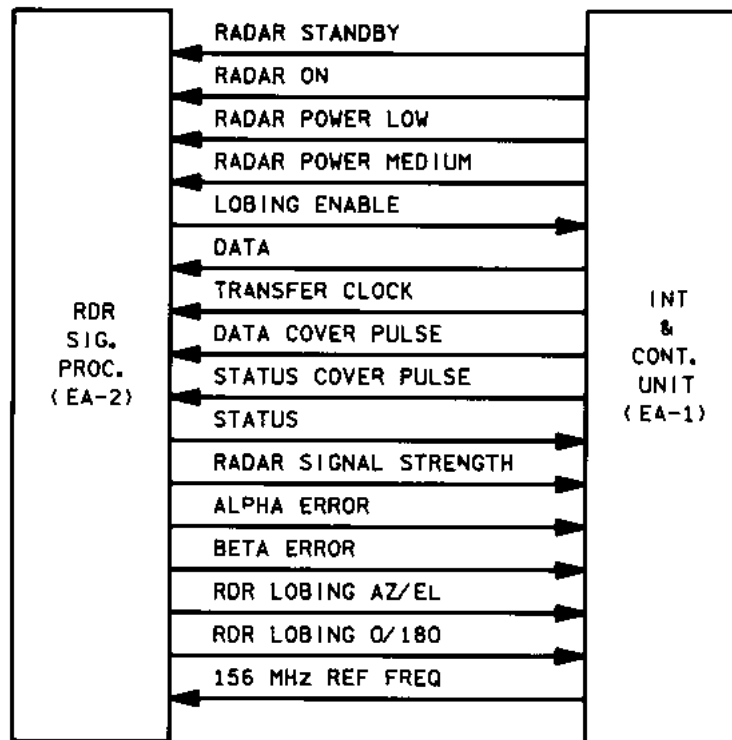


Figure 9-18. EA-2/EA-1 interface

**Table 9-16. Serial I/O EA-1 Control Word to EA-2**

| Data |     |                       |
|------|-----|-----------------------|
| Byte | Bit | Title                 |
| 1    | 1   | SPARE                 |
|      | 2   | ENCODED MODE BIT 1    |
|      | 3   | ENCODED MODE BIT 2    |
|      | 4   | ACQUISITION INHIBIT   |
|      | 5   | RADAR FIXED THRESHOLD |
|      | 6   | SELECT                |
|      | 7   | MAIN SCAN             |
|      | 8   | MINI SCAN             |
| 2    | 1   | PROVIDE TEST TARGET   |
|      | 2   | RADAR ACTIVE/PASSIVE  |
|      | 3   | SPARE                 |
|      | 4   | SPARE                 |
|      | 5   | SPARE                 |
|      | 6   | SPARE                 |
|      | 7   | SPARE                 |
|      | 8   | SPARE                 |

| Data (con't) |     |                 |
|--------------|-----|-----------------|
| Byte         | Bit | Bit value - ft. |
| 3            | 1   | 1,310,720       |
|              | 2   | 655,360         |
|              | 3   | 327,680         |
|              | 4   | 163,840         |
|              | 5   | 81,920          |
|              | 6   | 40,960          |
|              | 7   | 20,480          |
|              | 8   | 10,240          |
| 4            | 1   | 5,120           |
|              | 2   | 2,560           |
|              | 3   | 1,280           |
|              | 4   | 640             |
|              | 5   | 320             |
|              | 6   | 160             |
|              | 7   | 80              |
|              | 8   | 40              |
| 5            | 1   | 20              |
|              | 2   | 10              |
|              | 3   |                 |
|              | 4   |                 |
|              | 5   |                 |
|              | 6   |                 |
|              | 7   |                 |
|              | 8   |                 |

Note 1

|              | Bits     |          |
|--------------|----------|----------|
|              | <u>1</u> | <u>2</u> |
| Encoded mode | 1        | 2        |
| AUTO TRACK   | 0        | 0        |
| GPC          | 0        | 1        |
| MANUAL SLEW  | 1        | 0        |
| GPC DES      | 1        | 1        |

Table 9-17. Serial I/O EA-2 Status Word to EA-1

| Byte | Bit | Title                  | Byte | Bit | Radar range, ft | Byte | Bit | Radar range rate, ft/s | Byte | Bit | Radar alpha angle rate deg/s | Byte | Bit | Radar beta angle rate deg/s |
|------|-----|------------------------|------|-----|-----------------|------|-----|------------------------|------|-----|------------------------------|------|-----|-----------------------------|
| 1    | 1   | RADAR ANGLE RATE       | 3    | 1   | 1,310,720       | 6    | 1   | +1,638.4               | 8    | 1   | ±1.18                        | 10   | 1   | ±1.18                       |
|      |     | DATA GOOD              |      | 2   | 655,360         |      | 2   | 819.2                  |      | 2   | 0.59                         |      |     |                             |
|      | 2   | RADAR ANGLE            |      | 3   | 327,680         |      | 3   | 409.6                  |      | 3   | 0.295                        |      |     |                             |
|      |     | DATA GOOD              |      | 4   | 163,840         |      | 4   | 204.8                  |      | 4   | 0.1475                       |      |     |                             |
|      | 3   | SPARE                  |      | 5   | 81,920          |      | 5   | 102.4                  |      | 5   | 0.07375                      |      |     |                             |
|      |     |                        |      | 6   | 40,960          |      | 6   | 51.2                   |      | 6   | 0.03688                      |      |     |                             |
|      | 4   | SPARE                  |      | 7   | 20,480          |      | 7   | 25.6                   |      | 7   | 0.01844                      |      |     |                             |
|      | 5   | GENERATING TEST TARGET |      | 8   | 10,240          |      | 8   | 12.8                   |      | 8   | 0.00922                      |      |     |                             |
|      | 6   | OPERATE                | 4    | 1   | 5,120           | 7    | 1   | 6.4                    | 9    | 1   | 0.00461                      | 11   | 1   | 0.00461                     |
|      | 7   | RADAR RANGE            |      | 2   | 2,560           |      | 2   | 3.2                    |      | 2   | 0.00230                      |      |     |                             |
|      |     | DATA GOOD              |      | 3   | 1,280           |      | 3   | 1.6                    |      | 3   | 0.00115                      |      |     |                             |
|      | 8   | RADAR RANGE RATE       |      | 4   | 640             |      | 4   | 0.8                    |      | 4   | 0.000576                     |      |     |                             |
|      |     | DATA GOOD              |      | 5   | 320             |      | 5   | 0.4                    |      | 5   | 0                            |      |     |                             |
|      |     |                        |      | 6   | 160             |      | 6   | 0.2                    |      | 6   | 0                            |      |     |                             |
|      |     |                        |      | 7   | 80              |      | 7   | 0.1                    |      | 7   | 0                            |      |     |                             |
|      |     |                        |      | 8   | 40              |      | 8   | 0.05                   |      | 8   | 0                            |      |     |                             |
| 2    | 1   | MINISCAN 2             | 5    | 1   | 20              |      | 1   |                        |      | 1   |                              |      | 1   |                             |
|      | 2   | SIDELOBE               |      | 2   | 10              |      | 2   |                        |      | 2   |                              |      |     |                             |
|      | 3   | DETECT                 |      | 3   | 5               |      | 3   |                        |      | 3   |                              |      |     |                             |
|      | 4   | TRACK                  |      | 4   | 2.5             |      | 4   |                        |      | 4   |                              |      |     |                             |
|      | 5   | SPARE                  |      | 5   | 1.25            |      | 5   |                        |      | 5   |                              |      |     |                             |
|      | 6   | SPARE                  |      | 6   | 0.625           |      | 6   |                        |      | 6   |                              |      |     |                             |
|      | 7   | SPARE                  |      | 7   | 0.313           |      | 7   |                        |      | 7   |                              |      |     |                             |
|      | 8   | SPARE                  |      | 8   | 0               |      | 8   |                        |      | 8   |                              |      |     |                             |

| <b>Serial I/O EA-1 Control Word to EA-2</b> |         |                          |   |
|---|---------|--------------------------|---|
| Byte 1                                      | Bit     | Set = 1/<br>Reset = 0    |   |
| (Encoded mode bits 1,2)                     | 2 and 3 | 0,0<br>0,1<br>1,0<br>1,1 | Antenna steering mode is auto track.<br>Antenna steering mode is GPC.<br>Antenna steering mode is manual slew.<br>Antenna steering mode is GPC designate. |
| (Acquisition inhibit)                       | 4       | 1                        | Inhibits search and angle track in GPC designate and manual slew antenna steering modes.  |
| (Radar fixed threshold select)              | 5       | 1                        | Radar fixed threshold selected (to acquire a target in clutter; i.e., noise) variable threshold is the normal operating mode.                             |
| (Main scan)                                 | 6       | 1                        | The antenna is in search mode.  |
| (Mini scan)                                 | 7       | 1                        | Indicates a target was detected and lost and a search is being made about the point where the target was detected.  |
| (Provide test target)                       | 8       | 1                        | Indicates the radar is in self-test mode and a simulated target is requested to test the receiver/radar processor.  |
| Byte 2                                      | Bit     | Set = 1/<br>Reset = 0    |   |
| (Radar active/passive)                      | 1       | 1                        | Indicates radar cooperative mode is selected. Normal operating mode is passive.   |
| Bytes 3, 4, and 5                           |         | 1                        | This is the designated target range in feet.  |

| <b>Serial I/O EA-2 Status Word to EA-1</b>        |                |                       |   |
|---|----------------|-----------------------|---|
| Byte 1  | Bit            | Set = 1/<br>Reset = 0 |   |
| (Range, range rate, angle, angle rate, data good) | 1, 2, 7, and 8 | 1                     | These data good flags are timed out functions indicating that statistical conditions have been satisfied. |
| (Generating test target)                          | 5              | 1                     | Indicates the radar is generating a simulated target.   |
| (Operate)   | 6              | 1                     | Indicates the radar processor is powered up.  |

| Serial I/O EA-2 Status Word to EA-1 |     |                       |  |
|-------------------------------------|-----|-----------------------|--|
| Byte 2<br>(Mini scan 2)             | 1   | 1                     | Indicates the radar target was detected and lost and range is greater than 9.5 nautical miles and therefore a smaller conical minis can scan is required; i.e., less than 9°.  |
| (Sidelobe)                          | 2   | 1                     | Indicates a target has been detected in the antenna sidelobe; i.e., the system should reacquire automatically.   |
| (Detect)                            | 3   | 1                     | A target has been detected.  |
| Byte 2                              | Bit | Set = 1/<br>Reset = 0 |  |
| (Track)                             | 4   | 1                     | In GPC and auto track antenna steering modes, indicates that the range, range rate, angle, and angle rate data good flags are high. In GPC designate and manual slew antenna steering modes, indicates that the range and range rate data good flags are high. |
| Bytes 3, 4 and 5                    |     |                       | Measured target range in feet.   |
| Bytes 6 and 7                       |     |                       | Measured target range rate in feet/sec.  |
| Bytes 8 and 9                       |     |                       | Measured alpha inertial angle rate in degrees/sec.   |
| Bytes 10 and 11                     |     |                       | Measured beta inertial angle rate in degrees/sec.  |

### 9.9.5 EA-1 to DA Interface

Communications from EA-1 to DA are normally Analog Signals, vice digital communication as was previously described using Serial Cards.

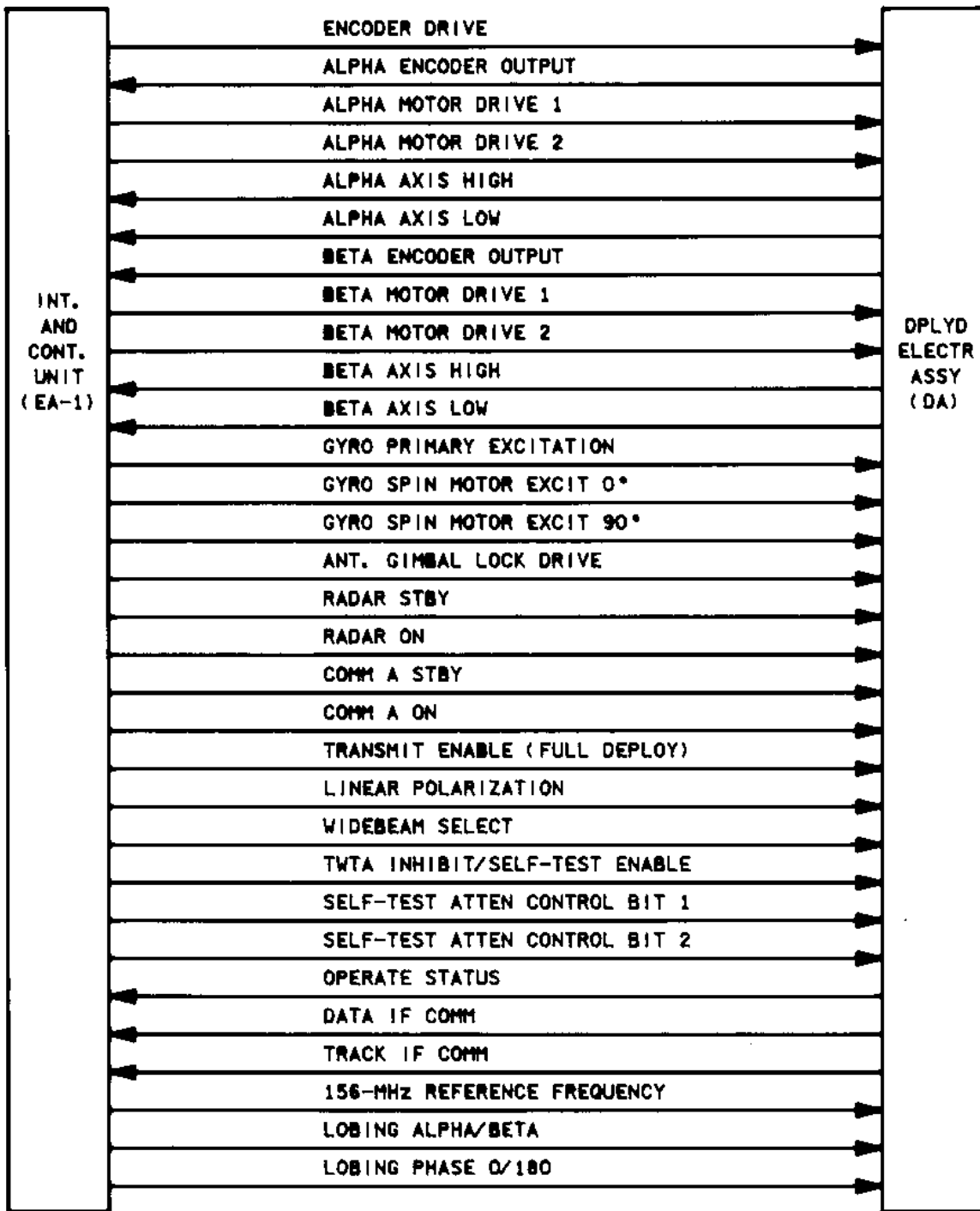


Figure 9-19. EA-1/DA signal interface

|   |   |
|---|---|
| EA-1 to/from DA Signal Interfaces are shown in Figure 9-19. |   |
| <b>Note: ← indicates DA to EA-1 Signal</b>                  |   |
| ENCODER DRIVE   | Provides excitation for antenna $\alpha$ and $\beta$ position encoders 5 V dc.  |
| ← ALPHA ENCODER OUTPUT                                      | Provides $\alpha$ gimbal position data.   |
| ALPHA MOTOR DRIVE 1 and 2                                   | Plus or minus 28 V dc 8.3-kHz signal to drive $\alpha$ gimbal to the commanded angle.                                 |
| ← ALPHA AXIS HIGH/LOW                                       | Provides antenna actual angular rate in the $\alpha$ axis, either a coarse/fine measurement.                          |
| ← BETA ENCODER OUTPUT                                       | Provides $\beta$ gimbal position data.  |
| BETA MOTOR DRIVE 1 and 2                                    | Plus or minus 28 V dc 8.3-kHz signal to drive $\beta$ gimbal to the commanded angle.                                  |
| ← BETA AXIS HIGH/LOW  | Provides antenna actual angular rate in the $\beta$ axis, either a coarse/fine measurement.                           |
| GYRO PRIMARY EXCITATION                                     | Provides primary power to the $\alpha$ and $\beta$ gyros in the rate sensor assembly for gyro angle rate data output. |
| GYRO SPIN MOTOR EXCITATION<br>0° and 90°                    | Two-phase drive for the gyro spin motors in the rate sensor assembly.   |
| ANTENNA GIMBAL LOCK DRIVE                                   | Provides plus or minus 14 V dc to the antenna gimbal lock circuit to lock/unlock the $\alpha$ and $\beta$ gimbals.    |
| RADAR STANDBY   | Activates the low voltage, high voltage, and anode/filament power supplies (RF output is inhibited).                  |
| RADAR ON  | Same as RADAR STANDBY except the radar exciter output is selected to drive the TWT (RF output is enabled).            |
| COMM A STANDBY  | Same as RADAR STANDBY.  |
| COMM A ON   | Same as RADAR ON except the comm exciter output is selected to drive the TWT (RF output is enabled).                  |
| TRANSMIT ENABLE<br>(full deploy)                            | Enables the TWT RF output (RF output is inhibited when not fully deployed).   |
| LINEAR POLARIZATION   | Selects LINEAR/CIRCULAR polarization for the sum transmit and receive channel.  |



|   |   |
|---|---|
| WIDEBEAM SELECT                           | Selects the wide-beam horn (1) or AZ/EL switch (0) as the input to the receiver difference channel.                       |
| TWT INHIBIT/SELF-TEST ENABLE              | Inhibits the TWT output and enables the exciter output to the self-test switch (DEA).                                     |
| SELF-TEST ATTENUATOR CONTROL BITS 1 and 2 | Controls the exciter power level to the self-test dipole.   |
| ← OPERATE STATUS                          | Indicates the TWT 3.5-minute timeout is complete, high voltage is on and the TWT is operating (RF power is being output). |
| ← DATA IF COMM                            | 647-MHz first comm data IF output to the Interface and Control Unit.  |
| ← TRACK IF COMM                           | 647-MHz first comm tracking IF output to the Interface and Control Unit.  |
| 156 MHz REFERENCE FREQUENCY               | A stable 156-MHz reference frequency for use in the exciter.  |
| LOBING ALPHA/BETA                         | Alternately selects the $\Delta$ AZ/ $\Delta$ EL signals out of the monopulse comparator for RF angle tracking.           |
| LOBING 0°/180°                            | Alternately selects 0°/180° phase shift in the receiver difference channel for RF angle tracking.                         |

### 9.9.6 EA-1 to Deployed Motor Interface

A safety feature was employed with the design of EA-1 to ensure that the Parabolic Dish was “locked” in the correct Stow position prior to either deploying or stowing the Ku-Band Deployed Assembly.

SSSH 14.7 Ku DPLY/STO/JETT is used as the reference as this section.

#### 9.9.6.1 Deployment

Prior to Deployment the Ku-Band Alpha and Beta Motors will be locked with two pins, ensuring the Dish will not move during the Ascent Phase.

During Ku-Band Deployment the crew will energize R13 Payload Bay Mach Par and Ku-Band Antenna to Deploy.

In General, the Ku-Band is verified at the Deployed Position [146 degrees out of the Payload Bay (deploy microswitches enabled)] via the MID MOTOR Controller send EA-1 a “Transmit Scan Enable”.

EA-1 can then be powered up and command the Antenna Gimbals to be unlocked during Initialization. Unlocking the two Antenna Gimbals causes “Boom Enable Stow II” to become inhibited.

|                                      |  |
|--------------------------------------|--|
| <b>EA-1 to Mid Motor Controllers</b> | <b>Mid Motor Controllers to EA-1</b>         |
|                                      | Transmit Scan Enable (Deployed $\mu$ switch) |
| <b>EA-1 to Antenna Gimbals</b>       | <b>Antenna Gimbals to EA-1</b>               |
| Unlock Command                       |  |
| <b>Antenna Gimbals to Macs</b>       | <b>Macs to Antenna Gimbals</b>               |
| Boom Enable Stow II <i>Inhibited</i> |  |

### 9.9.6.2 EA-1 Stow

Stowing the Ku-Band is operationally more dangerous than deployment; the dish must be locked into its stow position prior to the two ac stow motors being activated bringing the Ku-Band into the Payload Bay. The MMACS group primarily is responsible for this procedure, but INCO is routinely asked for help in troubleshooting due to the software interfaces with EA-1.

To nominally stow the Ku-Band, EA-1 receives a microswitch input which indicates the DA is completely deployed (“Transmit Scan Enable” input). The crew indicates the Stow Sequence by a switch on Panel R13 Ku Antenna - Stow (“Boom Stow Initiate” input). Boom Stow Initiate signal directly to Mid Motor Control Assemblies 2 & 4 (MMC 2&4), then this signal is routed back to EA-1.

Briefly, EA-1 will then command alpha and beta to the stow positions, send the “lock” command to both gimbal locks. Once locked, a feedback signal “Boom Stow Enable II” signal is sent from the Antenna Gimbals directly to the MMCs. EA-1 does not receive the “Boom Stow Enable II” feedback signal; EA-1 verifies that both the alpha and beta motors are locked is via the software procedure “Wiggle Test”. EA-1 commands both alpha and beta motors to move back and forth, if the 12-bit digital motor encoders signals detect no movement, EA-1 commands “Boom Stow Enable I”.

Once MMCs receive “Boom Stow Enable I”, “Boom Stow Enable II”, and R13 Ku-Antenna Stow signals, the MMCs energize the two 3 phase deploy/stow motors and stows the Ku-Band.

The Motors will be de-energized and movement will stop when the Stowed Microswitch is detected.

Note: If the Wiggle Test fails during this procedure: EA-1 is programmed to:

1. Retract the Locking Pins
2. Drive the Alpha and Beta Motors back to the Stow Position
3. Insert Locking Pins
4. Repeat Wiggle Test, if failed, repeat these four steps, ad infinitum or until it passes

| <b>EA-1 to MMCs</b> | <b>MMCs to EA-1</b>                          |
|---------------------|--|
|                     | Transmit Scan Enable (Deployed $\mu$ switch) |
|                     | Boom Stow Initiate (from Crew)               |
| Boom Stow Enable I  |  |

| <b>EA-1 to Antenna Gimbals</b> | <b>Antenna Gimbals to EA-1</b> |
|--------------------------------|--------------------------------|
| Lock Gimbal Motors             |                                |
|                                |                                |

| <b>Antenna Gimbals to MMCs</b> | <b>MMCs to Antenna Gimbals</b> |
|--------------------------------|--------------------------------|
| Boom Stow Enable II            |                                |

**9.9.6.3 Direct Stow**

If EA-1 fails and cannot be used for the Stow Procedure, the crew must manually position the Ku-Band Dish Antenna during EVA and using IFM breakout box power lock the two Gimbal Wedge Pins in place.

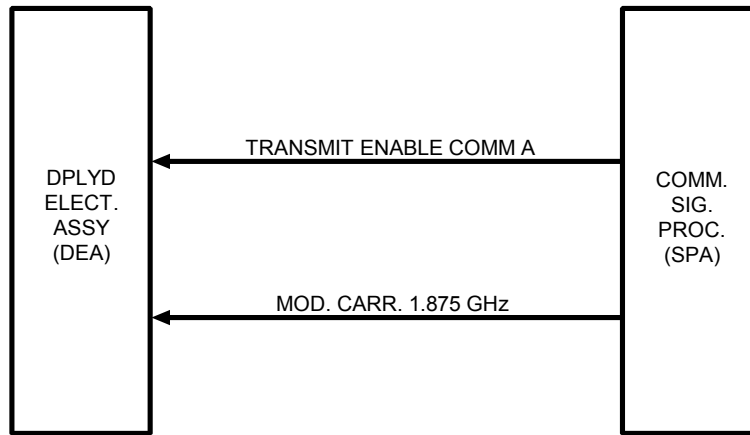
In General, once both Wedge pins are physically locked in place, the IV member can put R13 Ku-Band Antenna in Direct Stow (bypassing Boom Stow I and II) and forcing both MMCs to activate and move 146 degrees within the payload bay.

Again, The two AC motors will be de-energized and movement will stop when the Stowed Microswitch is hit.

**9.10 SPA TO DEA INTERFACE**

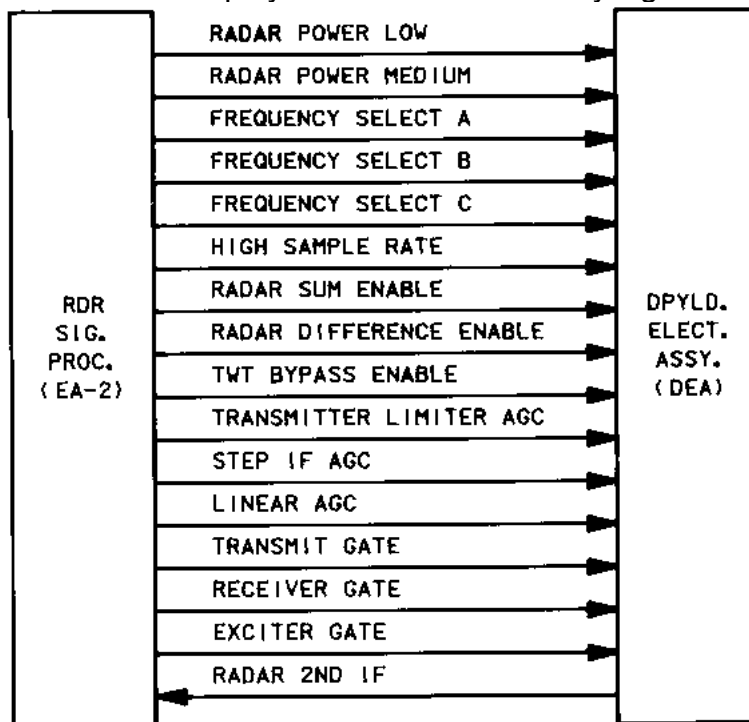
|   |   |
|---|---|
| Signals from the SPA to the DEA are shown in Figure 9-20 and described below. |   |
| TRANSMIT ENABLE COMM A  | Enables the 1.875-GHz output to drive the communications upconverter.<br><br>[This Signal allows the SPA to control the Carrier Switch in Alternate Acquisition Mode] |
| MODULATED CARRIER<br>1.875 GHz  | This is the Communications Signal Processor output carrier to the communications upconverter in the DEA.  |

Figure 9-20. DEA/SPA signal interface



9.11 DEA TO EA-2 INTERFACE

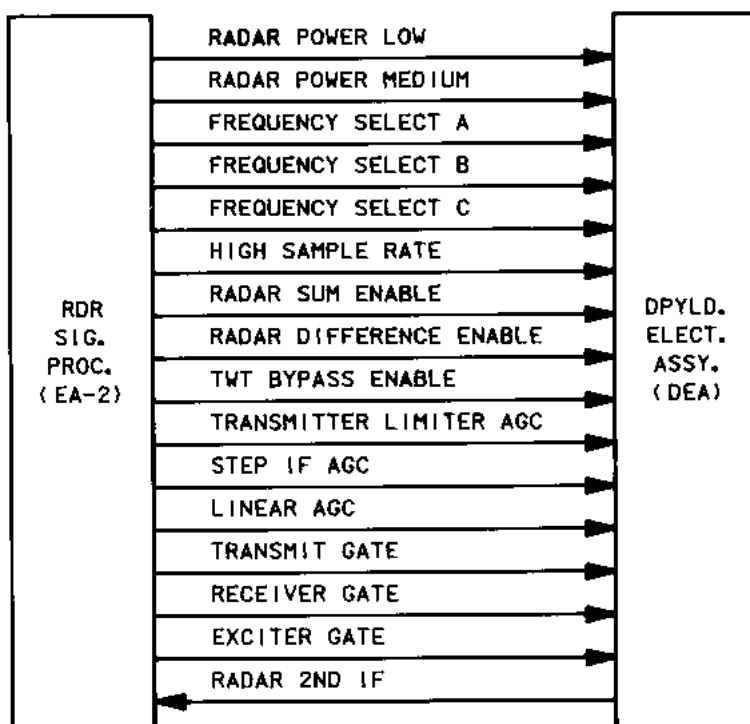
The Radar Signal Processor/deployed electronic assembly signal interface is shown in



Signal definition is as follows.

|  |   |
|--|---|
| EA-1 to/from DEA Signal Interfaces are shown in Figure 9-19. |   |
| <b>Note: ← indicates DA to EA-1 Signal</b>                   |   |
| RADAR POWER LOW  | The TWT output power is limited to 24 dB below the maximum TWT output.                                    |
| RADAR POWER MEDIUM   | The TWT output power is limited to 12 dB below the maximum TWT output.                                    |
| FREQUENCY SELECT A,B,C                                       | A 3-bit binary code used to select one of five frequencies in the radar mode.                             |
| HIGH SAMPLE RATE   | Selects a 10-MHz bandpass filter for the radar receiver second IF (78 MHz).                               |
| RADAR SUM ENABLE   | Enables the radar receiver sum channel.   |
| RADAR DIFFERENCE ENABLE                                      | Enables the radar receiver difference channel.  |
| TWT BYPASS ENABLE  | Connects the exciter output to the antenna sum channel.   |
| TRANSMITTER LIMITER AGC                                      | Inserts 30 dB of attenuation in the receiver sum and difference channels.                                 |
| STEP IF AGC  | Inserts 30 dB of attenuation in the radar first IF channel.   |
| LINEAR AGC   | Inserts a variable attenuation of 0 dB to 40 dB in the radar first IF channel.                            |
| TRANSMIT GATE  | Sets the ferrite switch to the minimum attenuation state; i.e., enables TWT RF output to the sum antenna. |
| RECEIVER GATE  | Disables the exciter second LO output and the receiver first IF sum and difference channels.              |
| EXCITER GATE   | Enables the exciter output to the radar up-converter.   |
| ← RADAR SECOND IF  | Radar second IF (78 MHz) output from the DEA receiver.  |

Figure 9-21. EA-2/DEA interfaces



## 9.12 TELEMETRY

They comprise the switch scan, analog, and GCIL, measurement, SM and GNC Downlist.

### 9.12.1 OI telemetry description

|  |   |
|--|---|
| (S) RDR COOPERATIVE<br>(V74S2419E)                       | If Ku-band system is powered on, indicates that radar cooperative (transponder) mode has been selected.   |
| (S) RDR PASSIVE<br>(V74S2420E)                           | If Ku-band system is powered on, indicates that radar passive (skintrack) mode has been selected.   |
| (S) Ku CONTROL PANEL/<br>COMMAND<br><br>(V74S2430E)(0,1) | All panel switches are enabled.<br><br>Command drivers in the GCIL are enabled for the following functions in comm mode only; RADAR is not commandable. |
| (S) RDR PWR OUT MEDIUM<br>(V74S2495E)                    | If Ku-band system is powered on in radar mode, indicates medium transmitted power has been selected.  |

|  |  |
|--|--|
| (S) RDR PWR OUT HIGH<br>(V74S2496E)          | If Ku-band system is powered on in radar mode, indicates high transmitted power has been selected. |
| (A) KU RCVD SIG. STR.<br>(V74E2508A)         | Indicates the radar or communications received signal strength in dBm.                             |
| (A) KU XMIT RF PWR<br>(V74E2511A)            | Indicates the radar or communications TWT RF output power in watts.                                |
| (A) KU TEMPERATURES<br>(V74T2497A)           | Temperature range -75° F to +300° F.<br>Transmitter - Sensor in the DEA located near the TWT.      |
| (V74T2961A)                                  | Receiver - Sensor in the DEA located near the receiver.  |
| (V74T2963A)                                  | Antenna feed - Sensor located on the feed assembly in the monopulse comparator.                    |
| (V74T2965A)                                  | A axis gimbal - Sensor located in the A gimbal housing near the motor.                             |
| (V74T2967A)                                  | Gyro - Sensor located in the rate sensor assembly (mounted on the B gimbal).                       |
| (V74T2969A)                                  | B axis gimbal - Sensor located in the B gimbal housing near the motor.                             |
| (G) KU COMM STANDBY<br>(V74X4807E)           | Indicates the GCIL has commanded the Ku system into the comm standby mode (minimum power usage).   |
| (G) KU/S FAIL SAFE (V74X4809E)               | Indicates the fail to S-band command has been received by the GCIL. (Not Used)                     |
| (G) KU ANT STEERING MAN<br>SLEW (V74X4810E)  | Indicates the GCIL has commanded the manual slew antenna steering mode.                            |
| (G) KU COMM ON (V74X4818E)                   | Indicates the GCIL has commanded the Ku system into comm on mode.                                  |
| (G) KU ANT STEERING GPC<br>(V74X4820E)       | Indicates the GCIL has commanded the GPC antenna steering mode.                                    |
| (G) KU ANT STEERING GPC<br>DESIG (V74X4822E) | Indicates the GCIL has commanded the GPC designate antenna steering mode.                          |
| (G) KU ANT STEERING AUTO<br>(V74X4824E)      | Indicates the GCIL has commanded the auto track antenna steering mode.                             |



|                       |   |
|-----------------------|---|
| (G) KU HDR/LDR SELECT | Indicates the GCIL has commanded the high data rate (one of five) and low data rate (one of four) sources for the return link modulation. |
|-----------------------|---|

|            |           |
|------------|-----------|
| HDR        |           |
| PL ANALOG  | V74X4828E |
| PL DIGITAL | V74X4829E |
| TV         | V74X4830E |
| PL MAX     | V74X4831E |
| PL INTERG  | V74X4832E |

|           |           |
|-----------|-----------|
| LDR       |           |
| PL INTERG | V74X4836E |
| MMU1      | V74X3448E |
| MMU2      | V74X3449E |
| PL DIGI   | V74X4839E |

### 9.12.2 GNC, SM and OI Telemetry for RNDZ Radar

|           |                                    |         |
|-----------|------------------------------------|---------|
| V90A0711C | DRAG ALT/RR R DOT MEAS RESIDUAL    | SPECIAL |
| V90H0221C | BARO ALT/RR RNG MEAS RESIDUAL      | SPECIAL |
| V90X4899X | SNAP RR RANGE DATA GOOD            | EVENT   |
| V90X4900X | SNAP RR RNG RATE DATA GOOD         | EVENT   |
| V90X4901X | SNAP RR ANGLES DATA GOOD           | EVENT   |
| V90U4893C | SNAP RR ROLL ANGLE MEAS            | DEG     |
| V90U4894C | SNAP RR PITCH ANGLE MEAS           | DEG     |
| V90U4895C | SNAP RR RANGE MEAS                 | FT      |
| V90U4896C | SNAP RR RANGE RATE MEAS            | FT/S    |
| V90X4866X | IND RR TO BE PROC BY FILTER        | EVENT   |
| V90J1361C | RNDZ NAV ANGLE AUT/INH/FOR FLAG    | ND      |
| V90J1362C | RNDZ NAV RR RNGE AUTO/INH/FOR FLAG | ND      |
| V90J1368C | RNDZ NAV RANGE RATE A/I/F FLAG     | ND      |
| V90J1400C | RR RNG MARKS ACCEPTED              | ND      |
| V90J1401C | RR R DOT MARKS ACCEPTED            | ND      |
| V90J1402C | H/X/AZ ANGULAR MARKS ACCEPTED      | ND      |
| V90J1403C | V/Y/EL ANGULAR MARKS ACCEPTED      | ND      |
| V90J1405C | RR RNG MARKS REJECTED              | ND      |
| V90J1406C | RR RDOT MARKS REJECTED             | ND      |
| V90J1407C | H/X/AZ ANGULAR MARKS REJECTED      | ND      |
| V90J1408C | V/Y/EL ANGULAR MARKS REJECTED      | ND      |
| V90J8881C | BARO ALT/RR RNG FILTER FLAG        | ND      |
| V90J8882C | DRAG ALT/RR R DOT FILTER FLAG      | ND      |
| V74E2508A | KU-BND A RDR/COMM RCVD SIG STR-AGC | DBM     |
| V74E2511A | KU-BAND COMM A/RADAR RF POWER      | W       |
| V74H2618J | KU-BAND A CH1 ROLL WORD 3 WD3      | DEG     |

|           |                                     |       |
|-----------|-------------------------------------|-------|
| V74H2619J | KU-BAND A CH1 PITCH WORD 4 WD4      | DEG   |
| V74H2648J | KU-BAND A CH1 DES ROLL WD WD2       | DEG   |
| V74H2650J | KU-BAND A CH1 DES PITCH WD WD3      | DEG   |
| V74M2582P | KU-A CH1 STATUS WORD 1 WD1          |       |
| V74M2600P | KU-A CH1 STATUS WORD 2 WD2          |       |
| V74M2622P | KU-A CH1 RDR RANGE                  |       |
| V74R2621J | KU-A CH 1 RANGE RATE BITS 01-16WD5  | FT/S  |
| V74R2626J | KU BAND A CH 1 ROLL RATE WD9        | DEG/S |
| V74R2628J | KU BAND A CH 1 PITCH RATE WD10      | DEG/S |
| V74S2419E | KU-BAND A RADAR COOPERATIVE         | EVENT |
| V74S2420E | KU-BAND A RADAR PASSIVE MODE        | EVENT |
| V74S2495E | KU-BAND A RADAR OUTPUT-MED          | EVENT |
| V74S2496E | KU-BAND A RADAR OUTPUT-HIGH         | EVENT |
| V74U2623J | KU-A CH 1 RDR RANGE BITS 01-23      | KFT   |
| V74X2583J | KU-A CH1 COMM A/RDR MODE(CR)WD1B00  | EVENT |
| V74X2584J | KU-A CH1 ANT STRG AUTO (CR) WD1B01  | EVENT |
| V74X2585J | KU-A CH1 ANT STRG GPC DES CRWD1B02  | EVENT |
| V74X2586J | KU-A CH1 ANT STRG GPC ACQ CRWD1B03  | EVENT |
| V74X2590J | KU-A CH1 RDR ANG DATA GD (R)WD1B07  | EVENT |
| V74X2591J | KU-A CH1 RDR ANG RT DG (R) WD1B08   | EVENT |
| V74X2592J | KU-A CH1 RDR STST IN PROG(R)WD1B09  | EVENT |
| V74X2594J | KU-A CH1 RDR THLD VAR/FIX(R)WD1B11  | EVENT |
| V74X2595J | KU-A CH1 OBSC INTLK OVRD(CR)WD1B12  | EVENT |
| V74X2601J | KU-A CH1 SEARCH (CR) WD2B00         | EVENT |
| V74X2602J | KU-A CH1 DETECT (CR) WD2B01         | EVENT |
| V74X2603J | KU-A CH1 TRACK (CR) WD2B02          | EVENT |
| V74X2614J | KU-A CH1 SCAN WARN LIMIT(CR) WD2B13 | EVENT |
| V74X2615J | KU-A CH1 RANGE DATA GOOD (R)WD2B14  | EVENT |
| V74X2616J | KU-A CH1 RANGE RATE GOOD (R)WD2B15  | EVENT |

### 9.12.3 SM Downlist Telemetry for Ku-Band

|           |                                    |  |
|-----------|------------------------------------|--|
| V74H2618J | KU-BAND A CH1 ROLL WORD 3 WD3      |  |
| V74H2619J | KU-BAND A CH1 PITCH WORD 4 WD4     |  |
| V74H2648J | KU-BAND A CH1 DES ROLL WD WD2      |  |
| V74H2650J | KU-BAND A CH1 DES PITCH WD WD3     |  |
| V74H2655J | KU-A CH1 BETA ANGLE(C)BIT05-16 WD5 |  |
| V74K0422J | KU-BD COMM BRK TRK CMD TGL1 WD1B01 |  |
| V74K0423J | KU-BD COMM BRK TRK CMD TGL2 WD1B02 |  |
| V74K2631J | KU-A CH1 SEARCH INIT (CR) WD1B00   |  |
| V74K2634J | KU-A CH1 SPRD SPCT ON/OFF(C)WD1B03 |  |
| V74K2635J | KU-A CH1 KU A/B SELECT (C) WD1B04  |  |
| V74K2636J | KU-A CH1 SELF TST ON/OFF (R)WD1B05 |  |
| V74K2637J | KU-A CH1 MODLN CONT B1 (C) WD1B06  |  |

|           |                                    |
|-----------|------------------------------------|
| V74K2638J | KU-A CH1 MODLN CONT B2 (C) WD1B07  |
| V74K2639J | KU-A CH1 PRI ACQ M ON/OFF(C)WD1B08 |
| V74K2640J | KU-A CH1 INTL STB ON/OFF(CR)WD1B09 |
| V74K2641J | KU-A CH1 FWD LK MODE 1/2 (C)WD1B10 |
| V74K2642J | KU-A CH1 RDR THLD VAR/FIX(R)WD1B11 |
| V74K2643J | KU-A CH1 OBSC INTLK OVRD(CR)WD1B12 |
| V74K2644J | KU-A CH1 TWTA OFF (CR) WD1B13      |
| V74K2645J | KU-A CH1 MASK SELECT(C) WD1B14     |
| V74M2582P | KU-A CH1 STATUS WORD 1 WD1         |
| V74M2600P | KU-A CH1 STATUS WORD 2 WD2         |
| V74M2622P | KU-A CH1 RDR RANGE                 |
| V74M2630P | KU-A CH1 GPC ACQ CONT WORD 1WD1    |
| V74M2653P | KU-A CH1 CONTROL WD4,5             |
| V74R2621J | KU-A CH 1 RANGE RATE BITS 01-16WD5 |
| V74R2626J | KU BAND A CH 1 ROLL RATE WD9       |
| V74R2628J | KU BAND A CH 1 PITCH RATE WD10     |
| V74U2623J | KU-A CH 1 RDR RANGE BITS 01-23     |
| V74U2651J | KU-A CH1 TGT RNG EST B01-18 WD4,5  |
| V74X0420J | KU-BD COMM BRK TRK TLM TGL1 WD2B08 |
| V74X0421J | KU-BD COMM BRK TRK TLM TGL2 WD2B09 |
| V74X2583J | KU-A CH1 COMM A/RDR MODE(CR)WD1B00 |
| V74X2584J | KU-A CH1 ANT STRG AUTO (CR) WD1B01 |
| V74X2585J | KU-A CH1 ANT STRG GPC DES CRWD1B02 |
| V74X2586J | KU-A CH1 ANT STRG GPC ACQ CRWD1B03 |
| V74X2587J | KU-A CH1 PARITY ERROR (CR) WD1B04  |
| V74X2588J | KU-A CH1 SYNC ERROR (CR) WD1B05    |
| V74X2589J | KU-A CH1 VALIDITY ERROR (CR)WD1B06 |
| V74X2590J | KU-A CH1 RDR ANG DATA GD (R)WD1B07 |
| V74X2591J | KU-A CH1 RDR ANG RT DG (R) WD1B08  |
| V74X2592J | KU-A CH1 RDR STST IN PROG(R)WD1B09 |
| V74X2593J | KU-A CH1 KU A/B SELECTED (C)WD1B10 |
| V74X2594J | KU-A CH1 RDR THLD VAR/FIX(R)WD1B11 |
| V74X2595J | KU-A CH1 OBSC INTLK OVRD(CR)WD1B12 |
| V74X2601J | KU-A CH1 SEARCH (CR) WD2B00        |
| V74X2602J | KU-A CH1 DETECT (CR) WD2B01        |
| V74X2603J | KU-A CH1 TRACK (CR) WD2B02         |
| V74X2604J | KU-A CH1 OPERATE (CR) WD2B03       |
| V74X2605J | KU-A CH1 EA1 RDR TST STAT(R)WD2B04 |
| V74X2606J | KU-A CH1 DA RDR TST STAT(R) WD2B05 |
| V74X2607J | KU-A CH1 EA2 RDR TST STAT(R)WD2B06 |
| V74X2608J | KU-A CH1 RDR SYS TST STAT(R)WD2B07 |

|           |                                    |
|-----------|------------------------------------|
| V74X2612J | KU-A CH1 FWD LK FR SYNC (C) WD2B11 |
| V74X2613J | KU-A CH1 DATA PRESENT (C) WD2B12   |
| V74X2614J | KU-A CH1 SCAN WARN LIMIT(CR)WD2B13 |
| V74X2615J | KU-A CH1 RANGE DATA GOOD (R)WD2B14 |
| V74X2616J | KU-A CH1 RANGE RATE GOOD (R)WD2B15 |
| V92H0545C | KU-BD RF PROTECT ZONE ROLL 1 (DL)  |
| V92H0546C | KU-BD RF PROTECT ZONE ROLL 2 (DL)  |
| V92H0547C | KU-BD RF PROTECT ZONE PITCH 1 (DL) |
| V92H0548C | KU-BD RF PROTECT ZONE PITCH 2 (DL) |
| V92J0899C | KU-BD RF PROTECTION ZONE ID        |
| V92X0104X | KU-BAND BETA STOP FLAG             |
| V92X0992X | KU-A VAR BETA MASK LIM STATUS      |
| V92X0993X | KU-BAND BETA LIMIT FLAG            |
| V92X5601X | KU-BD RF PROTECTION ANGLES REJECT  |
| V93X1082X | TDRS SV 1 GPC SELECT FOR KU-BAND   |
| V93X1083X | TDRS SV 2 GPC SELECT FOR KU-BAND   |
| V93X1084X | TDRS SV 3 GPC SELECT FOR KU-BAND   |
| V93X1085X | TDRS SV 4 GPC SELECT FOR KU-BAND   |
| V93X5606X | KU-BD RF PROTECTION ZONE 1 STATUS  |
| V93X5620X | ANTENNA-S BAND SITE SEL-AUTO       |
| V93X5621X | KU-BD RF PROTECTION ZONE 2 STATUS  |
| V93X5622X | ANTENNA-S BAND SITE SEL-NEXT       |
| V93X5623X | KU-BD RF PROTECTION ZONE 3 STATUS  |
| V93X5624X | KU-BD RF PROTECTION ZONE 4 STATUS  |
| V93X5625X | ANTENNA-AUTO S-BAND ANT SEL ENA    |
| V93X5626X | ANTENNA-AUTO S-BAND ANT SEL INH    |
| V93X5641X | ANTENNA-RADAR RANGE ESTIMATE-MIN   |
| V93X5642X | ANTENNA-RADAR RANGE ESTIMATE-AUTO  |
| V93X5647X | ANTENNA-TDRS MODE OVERRIDE CMD     |
| V93X5648X | ANTENNA KU-BAND TDRS SEL TGT-A PRI |
| V93X5649X | ANTENNA KU-BAND TDRS SEL TGT-B PRI |
| V93X6859X | KU ANTENNA ENA/INH CMD             |

### 9.13 INSTALLATION/POWER/WEIGHT

#### 9.13.1 Location

Avionics bay 3A (Figure 9-22)

- A. Interface and Control Unit (EA-1)
- B. Radar Signal Processor (EA-2)

Avionics bay 3B (Figure 9-23)

Communications Signal Processor (SPA)

Payload bay

DA - Figure 9-24, consisting of the DMA & DEA

The location of the ALPHA/BETA gimbal intersection in the orbiter coordinate system is shown in Figure 9-25 and is

| Stowed      | Deployed    | Center of DA rotation |
|-------------|-------------|-----------------------|
| X = 628.430 | X = 565.841 | X = 589.00            |
| Y = 85.800  | Y = 134.365 | Y = 99.60             |
| Z = 443.875 | Z = 443.875 | Z = 422.00            |

### 9.13.2 Power/Weight/Cooling

Power usage, weight, and cooling for the Ku-band system are as follows:

| Equipment    | Power, W |     |       |     | Weight, lb | Cooling           |
|--------------|----------|-----|-------|-----|------------|-------------------|
|              | Comm     |     | Radar |     |            |                   |
|              | STBY     | ON  | STBY  | ON  |            |                   |
| EA-1         | 150      | 150 | 150   | 150 | 45         | Water loop        |
| EA-2         | -        | -   | -     | 48  | 34         | Water loop        |
| SPA          | -        | 87  | -     | -   | 41         | Water loop        |
| DEA          | 112      | 290 | 112   | 244 | 83         | No active cooling |
| DMA          | -        | -   | -     | -   | 89         | No active cooling |
| Heaters      |          |     |       |     |            |                   |
| DEA-(2)      | 135      | 135 | 135   | 135 | -          |                   |
| DMA-(4)      | 170      | 170 | 170   | 170 | -          |                   |
| Total        |          |     |       |     |            |                   |
| Without htrs | 262      | 527 | 262   | 442 |            |                   |
| With htrs    | 567      | 832 | 567   | 747 |            |                   |

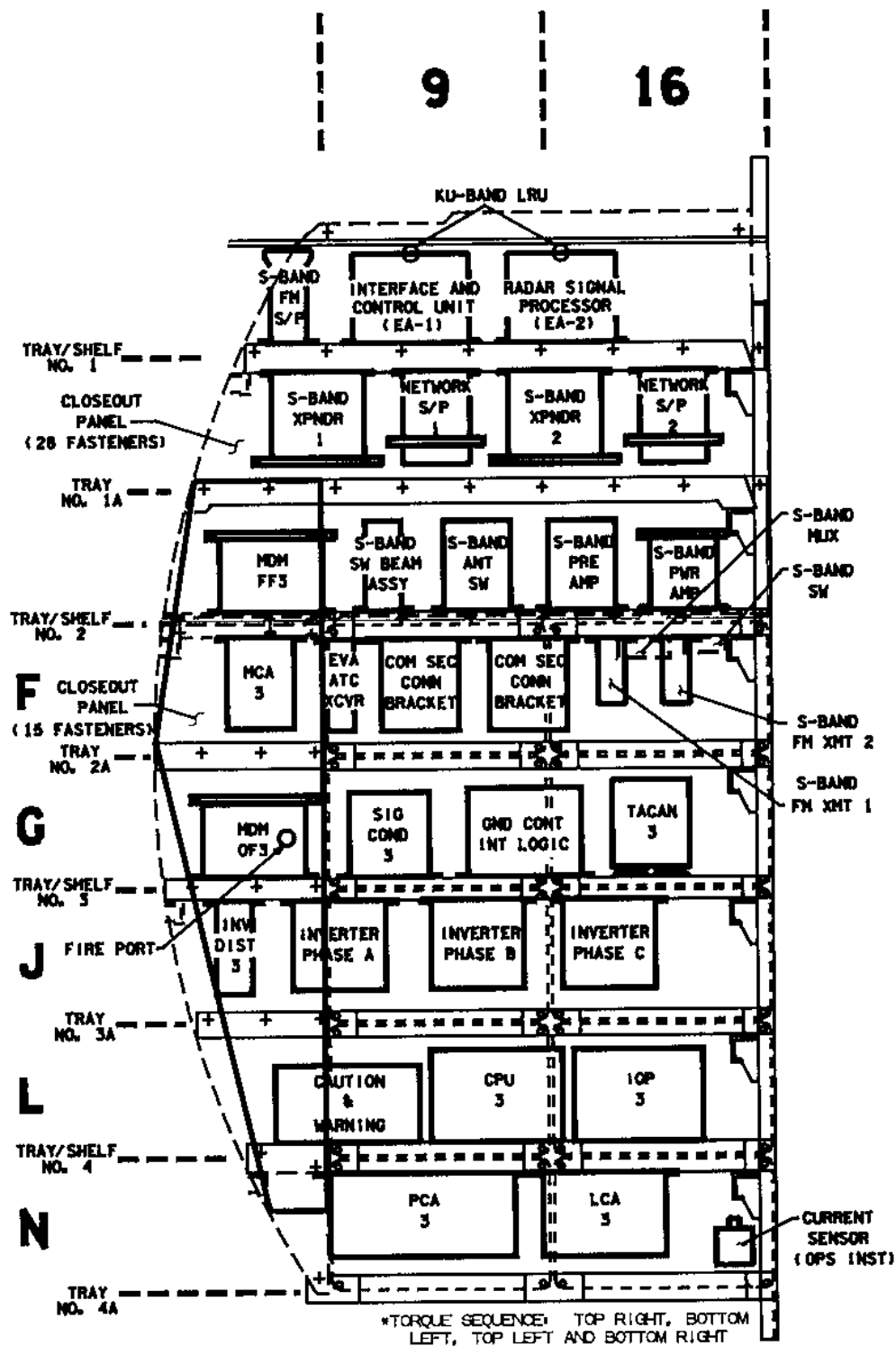
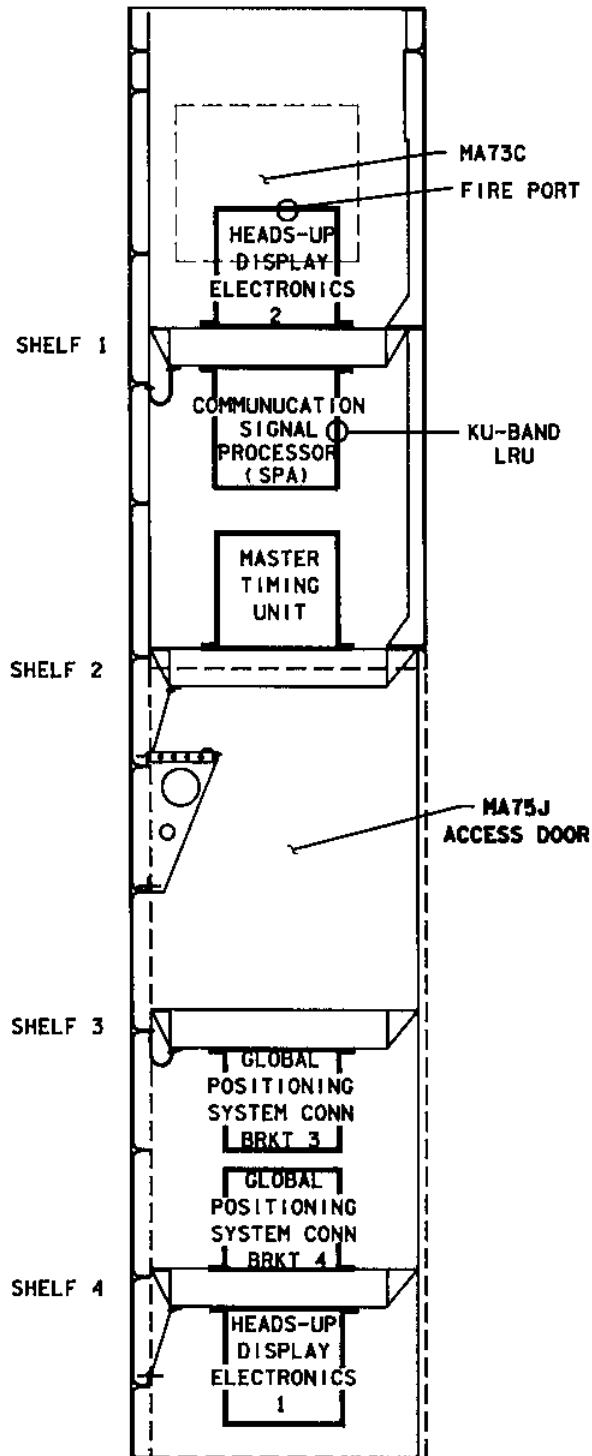


Figure 9-22. Ku-band LRU locations, bay 3A



10611012, ART. 4

Figure 9-23. Ku-band LRU locations, bay 3B

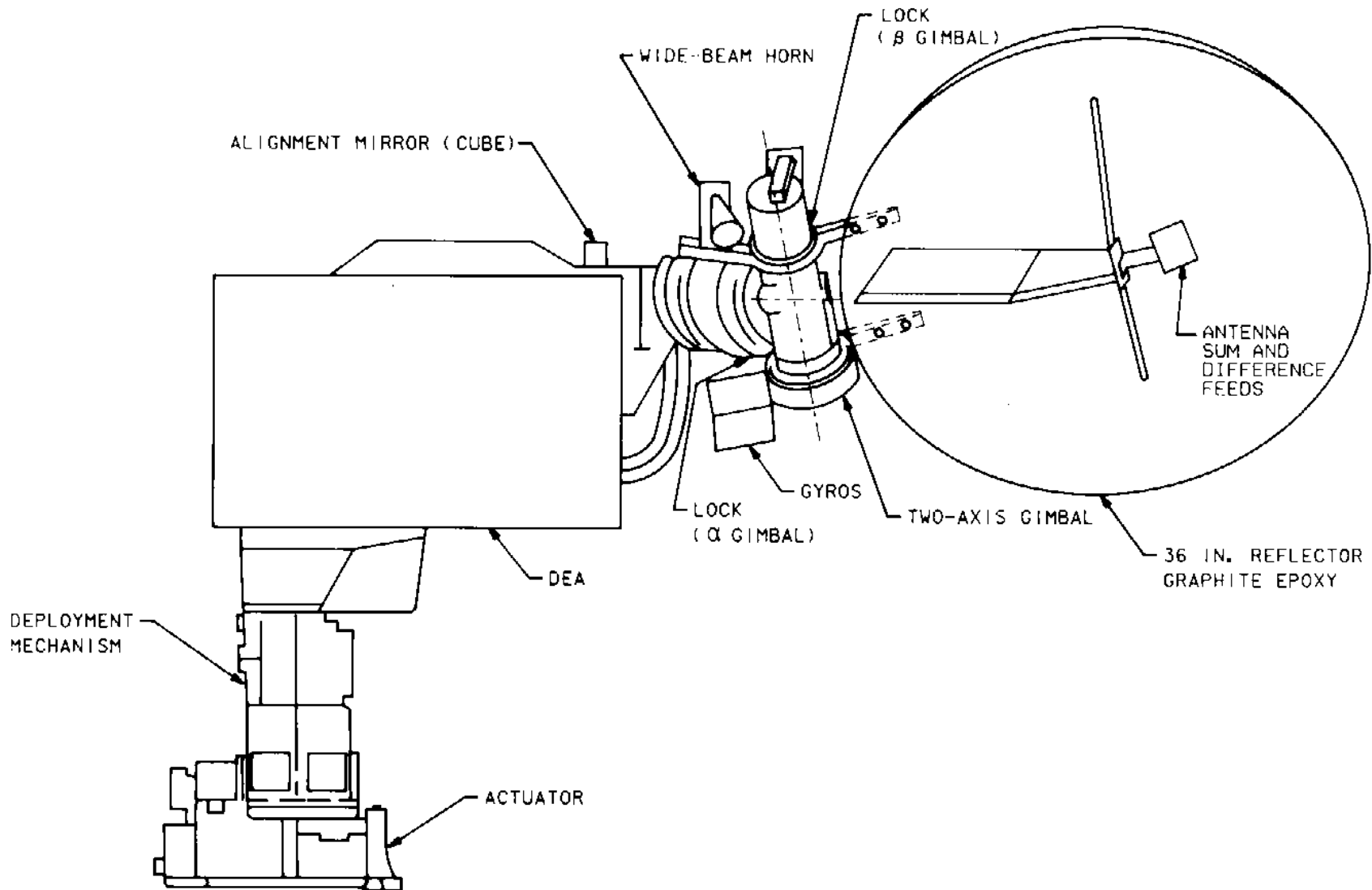
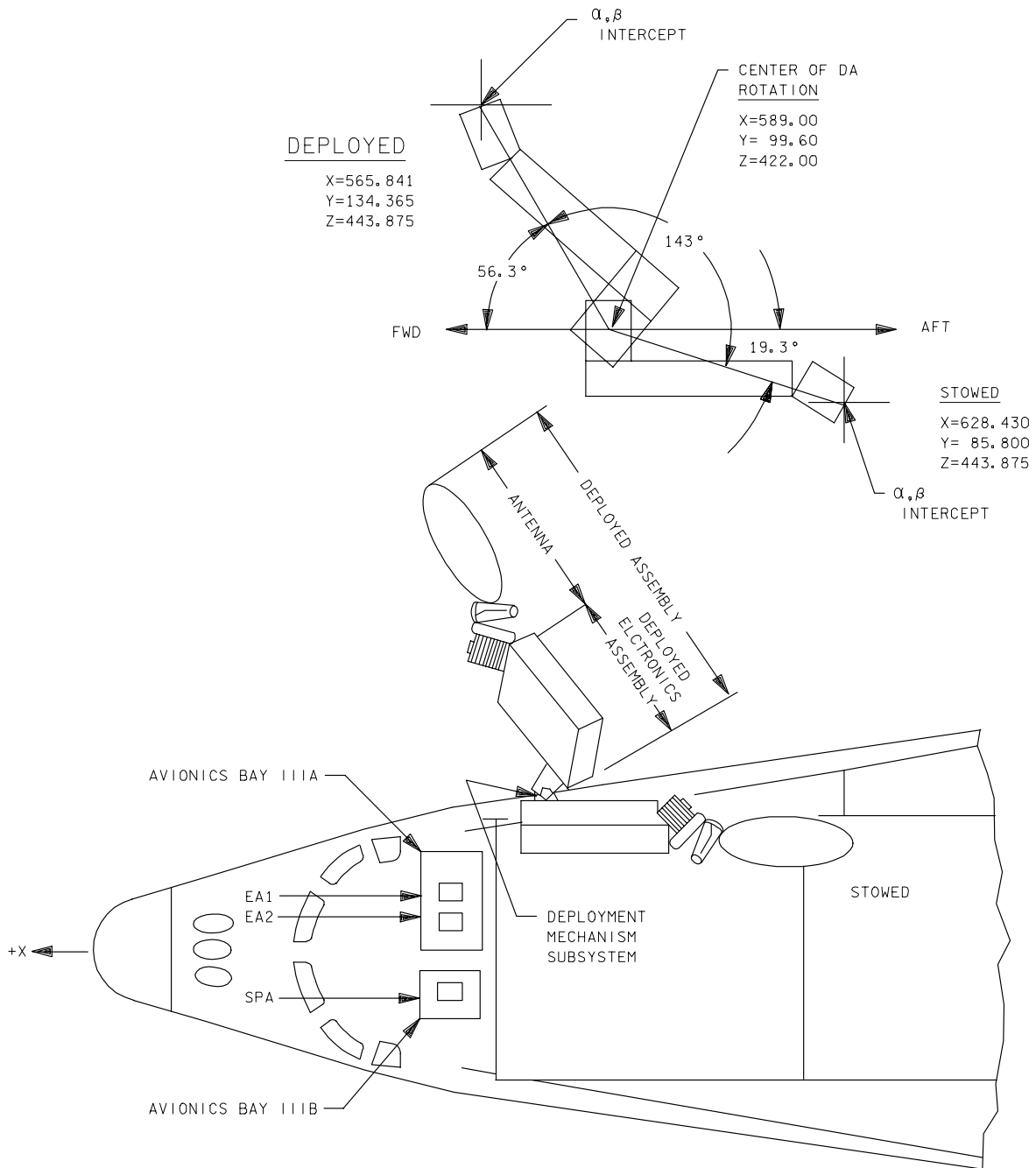


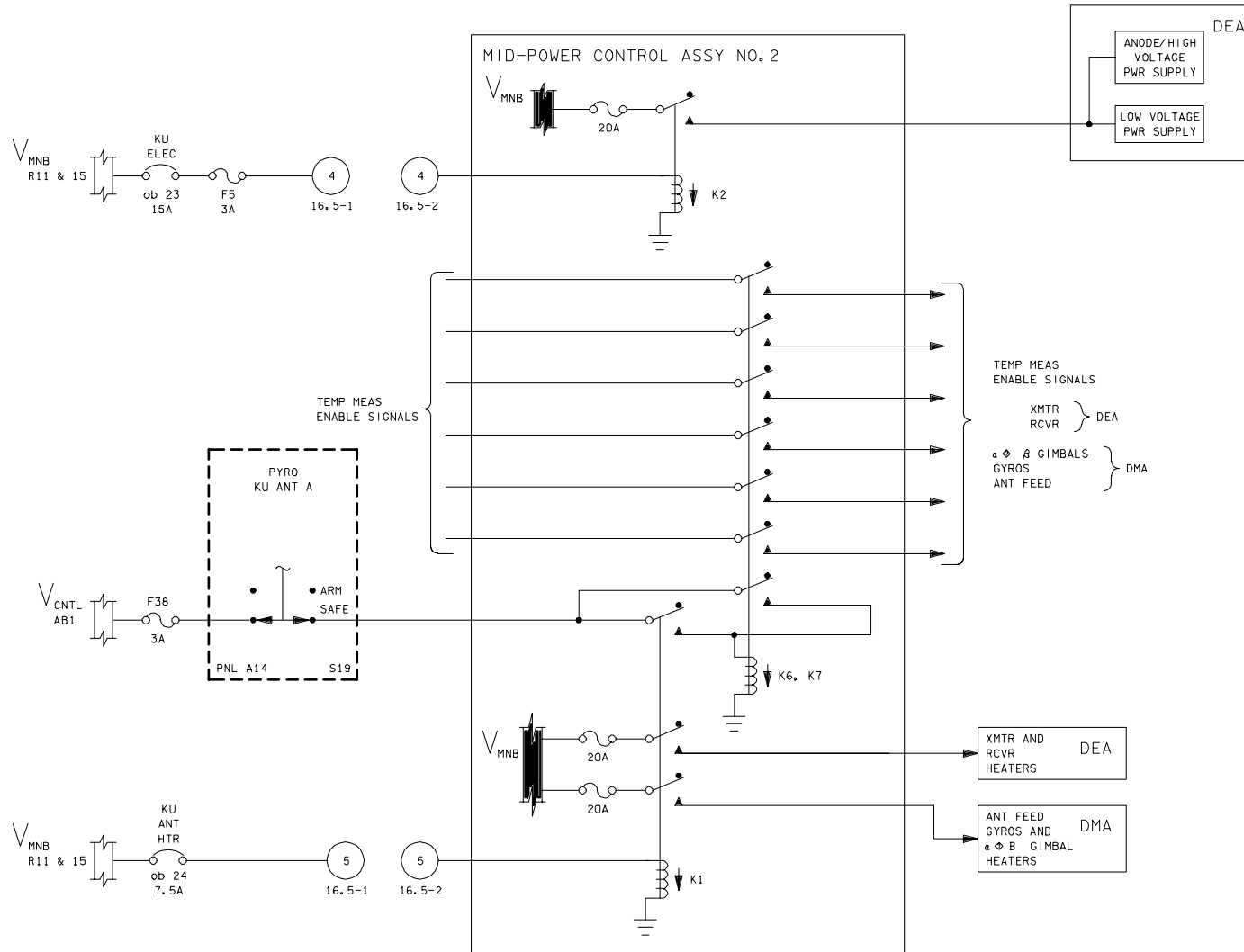
Figure 9-24. Ku-band deployed assembly





186111815. ART# 2

Figure 9-25. Ku-band location



186111827, ART, 2

Figure 9-26. Ku-band deployed assembly power and temperature measurements

## KU-BAND BETA GIMBAL MOTOR TEMPERATURE FOR STALL CONDITIONS

Hughes Aircraft Co. has a thermal program that can predict Ku-band temperature profiles for on-orbit operations and that they feel is in good agreement with flight data. The beta motor has a temperature sensor located in the vicinity of the encoder that is downlinked in telemetry, but the armature, which is the hottest area in the motor, does not have a temperature sensor. The temperature gradient from the armature to the temperature sensor is large, but Hughes Aircraft Co. has concluded that the telemetry can be used to infer the armature temperature.

### 9.14 KU-BAND OPERATIONS EXAMPLES

#### 9.14.1 Power Up Ku-Band System (Example)

When the system is powered up (ON/STBY), a timer is initiated to prevent RF radiation for 4 minutes (nominally 3.5 minutes). When the system is powered ON, the antenna will not initialize to 0° AZ, 0° EL until the gyros spin up (nominally 1 minute). The antenna will not initialize when the system is powered to STANDBY.

GCIL command

- 4102 COMM PWR - ON

or

- 4103 COMM PWR - STBY

#### 9.14.2 Enable SM SIO Channel Through MDM PF1 (Example)

Command load

14007 serial I/O enable

#### 9.14.3 GPC Designate Mode commanding Modulation-On (Example)

When operating without a TDRS forward link, GPC Designate mode be used and the return link Modulation must be commanded ON. *(Normally, KU-A MODLN CONT - AUTO is selected, allowing SPA to decide when to turn on the Modulation switch)*

- 14019 KU-A MODLN CONT - ON

#### 9.14.4 Command TWT Off (Example)

If Ku-band radiation is restricted because of payload constraints, the TWT can be commanded off; this will permit only forward link Ku Band communications. If the system is commanded to STANDBY, the antenna will normally remain fixed (with reference to the body axis). *(As inferred by previous text, Normally, the SPA will "decide" by Alternate Acquisition Mode Logic, when to turn the TWTswitch On and Off. MCC Commanding TWT- Off will command the EA-1 to always leave TWT switch Off.)*

Command load

- 14032 TWT - OFF

### 9.14.5 Ku RF Protection Boxes (Example)

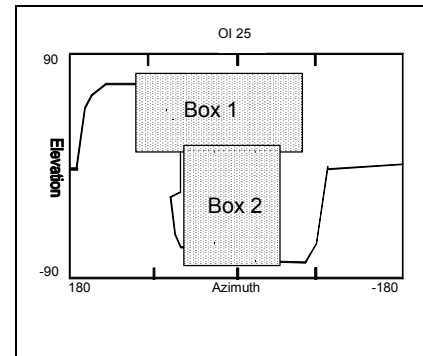
Enable Box 1 and 2

KU-BD RF ZONE 1 ENA  
(14037)

Enables RF  
Protect Box #1

KU-BD RF ZONE 2 ENA  
(14043)

Enables RF  
Protect Box #2



### 9.14.6 Configure Ku-Band System 3 Channel Downlink (Example)

GCIL command

- 4104 KU A ANT - GPC
- 4126 KU HDR - TV
- 4136 KU LDR - MMU1

### 9.14.7 Auto-handovers between S-band and Ku-band (Example)

The SM AM software will be able to automatically configure the forward link from the S-band system to the Ku-band system and back. The reason for this enhancement was to simplify the amount and type of commanding required to force the systems to hand over to and from each other. The SM AM will determine if the capability has been enabled before executing the auto handover. The crew cannot enable or disable this capability. When the SM is initialized the capability is disabled, but it can be enabled via command from the ground. If the S to K handover is enabled, the AM will look for a Ku forward link data present and signal strength greater than about  $-100$  dB. Once these conditions are satisfied, AM will wait 15 seconds to be sure that the link is stable, then it will send GCIL commands to configure the NSP (Source KU and Uplink Coding OFF) to use the Ku-band as the forward link for commands and voice. If the K to S handover is enabled, then the AM will look for Ku data present to be low (0) for 5 seconds. If this condition is met, AM will issue GCIL commands to configure the NSP (Source S-band and Uplink Coding ON) to use the S-band system as the forward link for commands and voice. If the Ku-band system is taken to RADAR or Standby, the auto-handover capability will send the TDRS Salvo GCIL command followed by GCIL commands for uplink high data rate, downlink high data rate, and transponder filter wide.

Some of the controlling conditions may be adjusted via SM TMBU. Table 9-18 lists the MSIDs and their default values.

**Table 9-18. MSIDs and default values**

| MSID      | Default value | TMBU | Nomenclature (name)            |
|-----------|---------------|------|--------------------------------|
| V93V1017C | 1.04 volts    | YES  | Auto Ku to S H/O Min AGC       |
| V93W1018C | 15 sec        | YES  | Auto S-BD to Ku-BD H/O Time    |
| V93W1019C | 5 sec         | YES  | Auto Ku-BD to S-BD H/O Time    |
| V93X1012X | 0             | NO   | Auto Ku-BD to S-BD H/O Enable  |
| V93X1013X | 1             | NO   | Auto Ku-BD to S-BD H/O Inhibit |
| V93X1015X | 0             | NO   | Auto S-BD to Ku-BD H/O Enable  |
| V93X1016X | 1             | NO   | Auto S-BD to Ku-BD H/O Inhibit |

Command load

Verify on INCO MGMT

- 14039 AUTO K to S H/O ENA      K-S AUTO H/O - ENA
- 14041 AUTO S to K H/O ENA      S-K AUTO H/O - ENA

#### 9.14.8 Beta gimbal limit protection (Example)

The SM software will protect an area near both beta ( $\beta$ ) gimbal limits to ensure that the antenna drive does not force the antenna against the hard stops for an excessive period of time, which could damage the gimbal motor. This problem has occurred on earlier flights. The area to be protected is called the forbidden zone. It is defined as:

- $\beta \geq 74.5^\circ$  for the positive beta stop
- $\beta \leq -83.5^\circ$  for the negative beta stop

These angles are the actual angles and not the designated (commanded) angles.

The software monitors the angles, and if the forbidden zone is entered, a counter (V92Q0103C) is started and a flag (V92X0104X, Ku-Band Beta Stop Flag) is set. The counter increments to 125 (1.92 seconds/count) or 240 seconds before the Ku-band system is commanded to standby mode via both PF1 and PF2 MDMs (GCIL command). This will prevent the antenna from moving any farther into the forbidden zone. If the forbidden zone is exited before the counter reaches 125, the counter is reset to 0 and the flag is turned off. When the Ku-band system is commanded to standby, the counter and flag are also reset to 0. Another flag (V92X0993X, Ku-band Beta Limit) will be turned on when the Ku system is commanded to standby so that the ground will understand why this action took place. Once the Ku-band system is commanded to standby, the software will monitor the designated beta angles to determine when the system will command a beta angle that is outside of the forbidden zones. The SM will command the system back on once the designated angles are outside the forbidden zones.

## 9.15 KU-BAND POWER MALFUNCTIONS

### A. Main B R14

Loss of control power to EA-1

Loss of GCIL Power to Ku-Band

Loss of Power to Deployed Electronics Assembly (DEA)

Loss of Power to EA-2

Loss of Ku-Band Heaters

Loss of A2 Meter

Actions: Use IFM K-25 to Re-energize EA-1 and stow, if EA-1 is cause of the short, use K-28 to Contingency Stow w/EVA

### B. Main B R14 loses power from Main B

Loss of control power to EA-1

Loss of GCIL Power to Ku-Band

Loss of Power to Deployed Electronics Assembly (DEA)

Loss of Power to EA-2

Loss of Ku-Band Heaters

Loss of A2 Meter

Actions: Use IFM K-25 to Re-energize EA-1 and stow

### C. Main C FPC 3 loses power from Main C

Loss of Power to EA-1

Actions: Use IFM K-25 to re-energize EA-1 and stow, if EA-1 is cause of the short, use K-28 to Contingency Stow w/EVA

### D. Main C R14

Loss of Power to the SPA

Actions: Use Ku-Band for Radar Mode

E. Main B MPC 2

Loss of Power to the DEA due to loss of Mid-Power Control Assembly No. 2 (MPCA2)

Actions: Write IFM to repower MPCA2

## 9.16 REFERENCES

### 9.16.1 Narrative

System Critical Design Review, June 1981.  
Electronic Assembly No. 1 Critical Design Review, August 1980.  
Signal Processor Assembly Critical Design Review, July 1980.  
Electronic Assembly No. 2 Critical Design Review, September 1980.  
Deployed Electronic Assembly Critical Design Review, April 1980.  
Deployed Mechanical Assembly Critical Design Review, May 1980.  
Radar System Critical Design Review, September 1980.  
Electronic Assembly No. 1 Flight Software Release XII, August 1984.  
Ku-Band COMM/Radar System Specification, Rockwell, MC409-0025.

### 9.16.2 Drawings

Rockwell

|             |   |
|-------------|---|
| VS70-740102 | Ku-Band COMM Schematic (OV102)                      |
| VS70-740109 | Ku-Band COMM Schematic (OV103 and SUBS)             |
| VS70-740292 | Ground Command Interface Logic Controller Schematic |
| VS70-764359 | Mid Power Control Assy-2 Schematic                  |
| VS70-763362 | Fwd Power Control Assy-3 Schematic                  |
| VS70-590119 | Ku-Band Antenna Deployment MMCA 2&4 Schematic       |

Electronic Assembly No. 1

|         |                                   |
|---------|-----------------------------------|
| 3555131 | Servo Loop Shaping Schematic      |
| 3555141 | Rate Integrating Gyro Schematic   |
| 3555151 | Motor Driver Schematic            |
| 3555161 | MDM Interface Schematic           |
| 3555171 | PN Despreader (BD #2) Schematic   |
| 3555181 | PN Despreader (BD #1) Schematic   |
| 3555191 | PSK Demodulator (BD #1) Schematic |
| 3555201 | PSK Demodulator (BD #2) Schematic |
| 3555231 | Gyro HTR/Loop Electronics         |
| 3582672 | LVPS Schematic                    |
| 3582685 | Linear Reg/Logic Schematic        |
| 3680761 | I/O Processor (BD #1) Schematic   |
| 3680750 | I/O Processor (BD #2) Schematic   |
| 3680755 | Microcomputer (BD #2) Schematic   |

3707579 Microcomputer (BD #1) Schematic  
3680767 MDM Interface (BD #2) Schematic  
3680799 MDM Interface (BD #1) Schematic  
3526101-410 EA-1 Block Diagram

Electronic Assembly No. 2

3526140-210 EA-2 Schematic  
3555692 LVPS (EA-2) Schematic  
3582615 Linear Reg/Logic Schematic  
3555615 Analog Proc. Schematic  
3555625 Preprocessor Schematic  
3555635 Master Timing/Control Schematic  
3555645 Filter Proc. Schematic  
3555655 PDI & Sequence Data Schematic  
3555665 Detection/AGC Schematic  
3555675 Range/Velocity Schematic  
3555685 Angle/Serial Data Schematic

Signal Processor Assembly

3526150-410 Signal Proc. Assy I/F Diagram  
3582632 LVPS (SPA) Schematic  
3582651 Linear Reg/Logic Schematic  
3555411 Convolutional Encoder Schematic  
3555441 Mgt./Handover Schematic  
3555431 FM Switch/Generator Schematic  
3555080 FM Module Interconnect  
3555461 QPSK Modulator Interconnect  
3555451 Bit Sync Schematic  
3555561 Bit Sync Schematic  
3555571 Bit/Frame/Decomm Schematic

Deployed Assembly

3526180-310 DEA Schematic  
3561952 LVPS Schematic  
3561962 Linear Reg/Logic Schematic  
3555811 Standby Control Logic Schematic  
3555821 Pulse Width Modulator Schematic  
3555831 RF Enable Logic Schematic  
3555841 Microwave Logic Schematic  
3555851 PWM Reg. Schematic  
3555861 Filament Reg/Converter Schematic  
3555871 D.C. Motor Drive Schematic  
3555881 Transmitter Pwr/Reg Schematic  
3555891 High Voltage Rect/Reg Schematic



|         |                                     |
|---------|-------------------------------------|
| 3561801 | Exciter Schematic                   |
| 3561811 | Harmonic Phase Comparator Schematic |
| 3561826 | Self Test Logic I/F Schematic       |
| 3561831 | Buff/Div/27 dB Ampl Schematic       |
| 3561841 | Freq Synthesizer Schematic          |
| 3561851 | FET Limiting Ampl Schematic         |
| 3561891 | GUNN Volt. Reg. Schematic           |
| 3561868 | Rcvr Blanking Logic Schematic       |
| 3599951 | ECL Logic I/F Schematic             |
| 3599961 | ML Logic I/F Schematic              |
| 3555901 | Microwave Assy Schematic            |
| 3574801 | Receiver Schematic                  |
| 3574811 | IF Ampl (Comm) Schematic            |
| 3574821 | IF Ampl (Radar) Schematic           |
| 3574831 | 2nd IF Ampl (Radar) Schematic       |
| 3574841 | Buffer Ampl (Radar) Schematic       |
| 3574851 | Receive Trk Logic Schematic         |
| 3555802 | Transmitter Interconnection         |
| 3561589 | DMA Wiring Diagram                  |
| 3561601 | DA Wiring Diagram                   |
| 3555788 | DEA Block Diagram                   |

## 9.17 KU-BAND OPERATIONAL NOTES/ANOMALIES

As a result of Ku-band system operation during ground test and flight, certain operational characteristics have been noted (which were not clearly defined) and failures have occurred. This section will be used to document these events and record the operational signature of the system.

### 9.17.1 Anomalies

- A. On STS-8, the antenna did not point to the commanded azimuth and elevation angles for about 1/2 hour, during which time the alpha gimbal temperature increased 30° F. After an antenna “whiparound,” the commanded and actual angles agreed and the temperature returned to normal.

Postflight analysis failed to identify the cause of the anomaly but postulated two theories to explain what happened:

1. The alpha gimbal encoder Light Emitting Diode (LED) was blocked, thus the alpha angle readout stayed the same until the commanded alpha angle was on the other side of the alpha stop. This caused the antenna to whip around, and during its travel it passed through the angle at which the MIP is output to EA-1. This resets the alpha angle counter in EA-1 (to the MIP angle +116.5°) and the incremental gimbal encoder continues to update the alpha angle

counter. At the end of the whiparound the commanded and actual angles agreed.

2. This theory differs from the first in that it assumes the alpha angle counter was reset by a "glitch" and continued to operate normally. The same scenario as in the first theory finally reset the counter.
- B. On STS-9, the gyro temperature (V74T2967A) increased to 250° F before the crew could open the heater circuit breaker. Subsequent checks of the gyro heater indicated normal operation. Postflight analysis concluded that the thermostat temporarily failed on, and cycling the circuit breaker restored the circuit to normal operation.
- C. On STS-9, the TWT amplifier failed to turn on when commanded. Cycling power from ON to STANDBY to ON had no effect, but ON to OFF to ON resulted in normal operation. This return to normal operation indicated that the TWT protection circuit was latched (three faults detected in 3 seconds sets the latch), and high voltage was removed from the TWT. If the system is powered OFF for more than 3 seconds but less than 9 seconds, the latch is reset and the 3.5-minute warmup is bypassed.

This fault could have been caused by a transient when commanding the TWT OFF (observed in ground tests) or by the TWT arcing. This arcing phenomenon is generally associated with new TWTs and is caused by contaminants in the tube that are burned out by normal operation as the tube ages.

- D. On STS 41-B, the system failed the first self-test and failed to track the EV-1 crewmember in the GPC antenna steering mode.

Postflight self-tests resulted in 18 out of 19 tests passed. Because of system timing inaccuracies, these results are considered normal. Regarding the inability of the system to track EV-1, it is thought that RFI, source undetermined, interfered and prevented the system from tracking EV-1.

- E. On STS 41-B, the system "operate" bit went low and there was no RF output. Power was cycled OFF and back ON, and the system operated normally for the rest of the mission.

The conclusion is that the fault detection circuit threshold was overly sensitive, and it was adjusted when the system was returned to the manufacturer.

- F. On STS 41-C, RFI was observed during radar self-tests and radar operations, indicated by sporadic spiking on the AGC telemetered signal and occasional false "detect" signals. Although the system failed 8 of 11 self-tests, radar operations were nominal. Tests to determine the RFI source were made on orbit and postflight by changing the communication system configuration and cycling power

on other orbiter systems. No source could be determined from the on-orbit test, and during the postflight test the interfering signal could not be reproduced.

Although exhaustive analysis and testing have been done since the flight, no source of the RFI has been identified.

- G. On STS 41-D, the antenna steering mode switch was left in the GPC position after the crew completed the cable positioning procedure. The antenna began a scan and before it was completed the antenna experienced undamped oscillations and hit the gimbal stops in both the alpha and beta axes. The crew stopped the antenna oscillations by turning the system off. Postflight analysis and tests have revealed an incompatibility between the microprocessor computed gimbal drive rates and their implementation in the alpha gimbal servo loop. The alpha gimbal drive rates are a function of the beta angle (both gimbal gyros are mounted on the beta axis). For radar scans that start at beta angles greater than  $41^\circ$ , the alpha gimbal drive rate will exceed 140 deg/sec during the scan and will enable a tachometer trip switch which will remove the drive from the gimbal motors. This will cause the alpha servo rate loop to saturate, with the resultant undamped antenna oscillation. This motion can be terminated by switching the system to standby or off.
- H. On STS 41-G, one of three screws holding the beta motor brush block assembly came out and shorted the motor windings at the negative stop ( $-85^\circ$ ). This caused the failure of the beta motor drive output transistors in EA-1. This failure also resulted in uncontrolled oscillation of the alpha gimbal when its servo loop became unstable.

Power to the system was cycled off, then on, and since the beta gimbal could not move, the microprocessor in EA-1 set the beta master index pulse register to  $-23.25^\circ$  as if it had found it. Actually, the beta gimbal was positioned at an angle of  $-85^\circ$ . The azimuth and elevation angles were determined using an offline angle transformation program (including the delta beta angle of  $61.75^\circ$ ), and the orbiter was maneuvered to point the Ku-band antenna line of sight to the TDRS and maintained in this attitude (TDRS track) while the TDRS was in view.

During an EVA, the crew performed an In-Flight Maintenance (IFM) procedure to lock the gimbals. The antenna was deployed again (with the gimbals locked) and the TDRS track attitude was used to maintain communications for the remainder of the mission. The deployed assembly was stowed without incident for entry.

- I. On STS 51-D, the antenna exhibited uncontrolled motion in both the alpha and beta axes. Since the motion was in both axes and the DEA "operate" bit was low, it was suspected that the DEA Low Voltage Power Supply (LVPS) was off. The DEA LVPS provides power to the gyro electronics in the Rate Sensor Assembly (RSA), and if removed, will cause both the alpha and beta gimbal servo loops to become unstable, resulting in erratic antenna motion.

Ku-band power was cycled to off and then on and the system operated normally for the rest of the flight. Postflight data analysis and inspection of the DEA LVPS verified that a loose washer in the LVPS caused a momentary short which latched the LVPS off. The LVPS latch can be removed by cycling system power if the short is no longer present.

- J. On STS 51-B, the Radar Signal Processor EA-2 failed when the Ku-band system was activated and a radar self-test was performed. No troubleshooting was performed during the mission and the system operated normally in comm mode for the entire flight. Troubleshooting at KSC indicated a normal probability of pass/fail when about 13 self-tests were performed (1 out of 13 failed). Also, the radar test set, which can access more data than is telemetered, did not uncover any signal that was abnormal.

The Hughes system engineer suspects that one of the angle rate signals, which is converted from D/A and measured against the range of 0 to 5 volts dc may have been converted to a value of 5+ volts dc. Any value greater than 5 V dc would be considered a failure. This D/A conversion error has been observed before in ground tests. There are no plans at present to modify the hardware or software to change the limit.

- K. On STS-49, the Ku-band system failed to point accurately. Postflight test and inspection indicated that the beta gimbal motor failed when it got too hot and caused the epoxy in the motor to extrude, which prevented the motor from pointing accurately. This occurred when the orbiter went to an inertial hold attitude with the Ku-band system in AUTO TRACK mode. In this mode, the antenna will continue to point inertially at the last TDRS coordinates which happened to be at the beta stop. Consequently, the beta gimbal overheated after being driven against the stop for more than 1 hour.

Since this mission, software has been added to avoid this problem. If the Ku-band antenna points in a beta stop region for more than 240 seconds, then the Ku-band system is automatically commanded to standby. Once the antenna points outside the beta stop region, the Ku-band system will be commanded back on.

- L. On STS-47, -54, and -67 (all EA-1 S/N 106) unexplained Ku-band BCE BYPASS messages have occurred several times during on-orbit operations. I/O resets restore the system to normal operations. These have not been repeatable on the ground during testing. No items that can cause the BCE message have been identified as out of tolerance. At present, the unit will be flown until the unit fails or the problem is identified.
- M. On STS-91, the Ku-band system failed to radiate in the COMM mode. After activation, the Ku-band failed to radiate any RF when placed in the COMM mode. The operate bit was low. The Ku-band system power was cycled to off and the activation procedure was performed again with no success. The system operated properly in the RADAR mode, but the COMM mode was never recovered during

the mission. Further troubleshooting revealed that when the Ku-band system was taken from COMM STBY to COMM ON, the HVPS fault protection logic appeared to be activated. It appeared that the RF out would start to ramp up, but after about 3 seconds, the RF out would drop to zero and stay there until the next time the Ku-band was cycled from COMM STBY to COMM ON. The problem was repeated on the ground. Postflight testing revealed that the A9 card in the HVPS had failed.

### 9.17.2 Signatures

#### A. Antenna angles during scan

The antenna angles indicate the scan center during a main scan and the miniscan center if a miniscan is entered; i.e., if there is a “detect” but no subsequent “track.” The angles are not updated during either scan.

#### B. Comm spurious (15 GHz) in radar mode

The exciter upconverter switches to comm mode during the receive time waiting for the radar return signal. If the comm system has been configured to FM mode with modulation ON, the upconverted reference signal (1.875 GHz) does not have a path through the signal processor assembly to the exciter comm upconverter and thus does not generate a spurious signal (15 GHz) during the radar receive time.

#### C. Radar AGC lock-up

Under certain conditions, the radar AGC will lock up; i.e., maintain an erroneous radar received signal strength that is composed of the actual received signal plus an additional 10 db. These conditions are

1. The antenna steering mode is in AUTOTRACK or GPC (with the designated range less than 2,560 feet).
2. The range to the target is less than 2,560 feet and is detected only in the antenna sidelobe.

This condition remains until the target is detected in the main beam, at which time the system reverts to normal operation. If a stronger signal is detected in the sidelobe while the AGC is locked up, the AGC reflects this new value but continues to be locked up; i.e., it does not reflect a decrease in the received signal.

The lockup can be overcome manually by putting the system in AUTOTRACK and doing a search (to break track and reacquire). If break-track does not occur, put the system in MANUAL steering mode and FAST slew to break track, then reinitiate search in either GPC or AUTOTRACK mode. As a last resort, the system can be reset by cycling power to STANDBY, then back to ON.

D. Radar signal strength indication during TWT bypass operation

The radar system always switches to TWT bypass mode while tracking a target when the range is less than 640 feet. The Radar Signal Strength (RSS) circuit in EA-2 is not aware of this switch to the TWT bypass mode and consequently computes the RSS assuming the TWT is radiating full power. The difference in power is 40 dB. Therefore, if tracking a small (less than 1 square meter) target, the indicated RSS is 40 dB lower than the actual RSS. This change corresponds to about a 1.25 V dc change on the RSS measurement (both telemetry and onboard meter), but should not cause any confusion to the crew since normally they are observing the target visually. The range and range rate measurements indicate the correct values.

E. Radar range

The specification value of RANGE in the PASSIVE mode is 12 n. m. The system was designed to be "Modulo 27 n. m.," which just means that the system will provide unambiguous range from 80 ft. to 27 n. m. If the target is large enough, the system locks up and tracks at greater ranges, but only indicates ranges from 80 feet to 27 n. m. As an example, on one flight the KU RADAR locked up on the target at 39 miles, but the telemetry indicated 12 n. m. The crew activates the RADAR at 150K feet so that if they see the target they will lock up and track it. However, they will not take data into the GNC GPC until the range is less than 135K feet. The 135K feet is specified so that "eclipsing" does not occur, which means that part of the returned energy is not being received because the receiver is being turned OFF so that the transmitter can radiate. Consequently, the range that indicated if the system were eclipsing would be incorrect.

F. Ku-Band Channel 2 – PL INTG bent-pipe mode

On STS-85 and STS-95, the Ku-band return link channel 1 data was messed up when channel 2 was set up for PL INTG bent-pipe mode, but no payload data were being received. The system was locking up on noise which ate up the bandwidth, taking bandwidth away from channel 1. Thus, Ku-band should not be configured to bent-pipe mode unless payload data is present. Channel 3 PL INTG bent-pipe mode was not tested.

THIS PAGE INTENTIONALLY BLANK

**SECTION 10 – SOFTWARE DESCRIPTION FOR THE KU-BAND  
INTEGRATED RADAR AND COMMUNICATIONS EQUIPMENT  
ELECTRONIC ASSEMBLY 1**

**CONTENTS**

| <b>Section</b> |  | <b>Page</b> |
|----------------|--|-------------|
| 10.1           | GENERAL .....                                | 10-1        |
| 10.2           | FUNCTIONAL AND PERFORMANCE REQUIREMENTS..... | 10-1        |
| 10.2.1         | Basic Program Structure.....                 | 10-1        |
| 10.2.2         | Database .....                               | 10-3        |
| 10.2.3         | Program Executive .....                      | 10-4        |
| 10.3           | PROCEDURES .....                             | 10-15       |
| 10.3.1         | Initialize Procedure .....                   | 10-15       |
| 10.3.2         | Procedure Termination Procedure.....         | 10-16       |
| 10.3.3         | Recover Procedure.....                       | 10-17       |
| 10.3.4         | Idle Procedure .....                         | 10-18       |
| 10.3.5         | Deploy Procedure .....                       | 10-20       |
| 10.3.6         | Point Procedure .....                        | 10-27       |
| 10.3.7         | Slew Procedure .....                         | 10-28       |
| 10.3.8         | Scan Procedure .....                         | 10-31       |
| 10.3.9         | Track Procedure .....                        | 10-35       |
| 10.3.10        | Self-Test Procedure.....                     | 10-37       |
| 10.4           | PROCEDURE SUPPORTING FUNCTIONS .....         | 10-60       |
| 10.4.1         | Math Functions .....                         | 10-60       |
| 10.4.2         | Position Loop Routine .....                  | 10-64       |
| 10.4.3         | Obscuration Function.....                    | 10-66       |
| 10.4.4         | Data Control Functions .....                 | 10-72       |
| 10.5           | REFERENCES .....                             | 10-93       |



## TABLES

| Table |  | Page  |
|-------|--|-------|
| 10-1  | Software inputs - discrete and serial.....             | 10-5  |
| 10-2  | Software inputs - discrete and serial (continued)..... | 10-6  |
| 10-3  | Software outputs - discrete and serial .....           | 10-6  |
| 10-4  | Gimbal reference data .....                            | 10-20 |
| 10-5  | Lookup table .....                                     | 10-35 |
| 10-6  | Self-test data blocks to the MDM.....                  | 10-43 |
| 10-7  | Self-test data blocks to D&C.....                      | 10-45 |
| 10-8  | Angle transform parameters .....                       | 10-62 |
| 10-9  | Obscuration zone polynomial parameters .....           | 10-68 |

## SECTION 10

### SOFTWARE DESCRIPTION FOR THE KU-BAND INTEGRATED RADAR AND COMMUNICATIONS EQUIPMENT ELECTRONIC ASSEMBLY 1

#### 10.1 GENERAL

The Ku-band 1802 microprocessor software within the Electronic Assembly-1 (EA-1) electronics shall support mission goals by providing (1) dynamic control of the antenna, (2) math functions to implement that control, and (3) general data handling associated with overall operation of the system.

##### A. Dynamic control

The software shall provide mode control of the antenna. It shall select search patterns, move the antenna in response to the azimuth/elevation slew switches or General Purpose Computer (GPC)-designated angle commands, and transition to closed loop tracking as required.

##### B. Math functions

Math functions shall enable the antenna to be moved and aligned in a coordinate system different from that of the orbiter. Specifically, math functions shall provide the capability of driving the antenna to specific designates or driving it in programmed spiral search patterns. They shall also provide the capability of generating servo shaping transfer functions and determining when the antenna line of sight has entered the region of orbiter obscuration.

##### C. Data handling

The software shall coordinate serial and discrete data transfer between the orbiter and other units within the Ku-band system and shall format the data as specified.

#### 10.2 FUNCTIONAL AND PERFORMANCE REQUIREMENTS

##### 10.2.1 Basic Program Structure

The Ku-band flight program shall be designed to operate under the conditions and within the constraints defined below:

- A. The program shall reside within a maximum of 24 1k Programmable Read-Only Memory (PROM) modules (24,576 bytes) and be organized so that the code for each module may be assembled independently, and modifications and reassemblies may be made on an individual module basis.
- B. The dynamic part of the database, comprising inputs, outputs, internal control words, stacks, and scratch pad values, shall be stored in a 1024-byte Random

Access Memory (RAM). There are 35 bytes of input data and 51 bytes of output data, both serial and discrete, to be periodically processed in and out of RAM.

- C. The program shall be interrupt-driven, with an interrupt occurring every 98.304 ms.
- D. Correspondingly, the program shall be designed to have a basic processing cycle of 196.608 ms subdivided into two 98.304-ms periods.
- E. The microprocessor shall be programmed so that it is in an idle (NO-OP) state when the interrupt occurs. That is, no programming sequences shall be permitted to execute for a period greater than 98.304 ms measured from the occurrence of an interrupt. This corresponds to 12,500 two-machine-cycle executed instructions. If, for any reason, processing is still in progress at the occurrence of an interrupt, this processing shall be interrupted and discontinued as a result of transferring control to the interrupt processing routine.
- F. Every time an interrupt occurs, a new 98.304-ms processing period shall be initiated.
- G. The program shall be implemented so that three execution phases shall be defined for each 196.608-ms (200 ms nominal) processing cycle and shall be defined as the A, B, and C phases or branches of the software sequences being executed. Functions that must be performed every 98.304 ms (100 ms nominal) shall be assigned to the A phase. The remaining functions shall be assigned to the B and C phases. At the incidence of every interrupt, the A phase code shall be executed, followed by execution of the B or C phase codes. The B and C phase codes shall be executed in alternate 100-ms periods and shall respectively complete execution by the end of the 100-ms period in which their execution takes place.
- H. The program shall be structured to consist of 4 executive routines and 10 functional software components designated as procedures, each procedure designed to implement a basic program mode. These routines and procedures are designated as follows:
  - 1. Executive routines
    - a. Powerup sequence routine
    - b. Interrupt processing routine
    - c. Configure routine
    - d. Wait routine
  - 2. Procedures
    - a. Initialize procedure
    - b. Procedure termination procedure

- c. Recover procedure
  - d. Idle procedure
  - e. Deploy procedure
  - f. Point procedure
  - g. Slew procedure
  - h. Scan procedure
  - i. Track procedure
  - j. Self-test procedure
- I. The executive comprises the four routines and shall function as a top-level monitor and control to which the procedures shall return at specific points in their execution as follows:
- 1. On the occurrence of an interrupt - (interrupt processing routines).
  - 2. Immediately before the B phase of every procedure in order to strobe in the most current input data and commands from the Multiplexer/Demultiplexer (MDM) and discrete input lines and to reconfigure the program to execute a new procedure if conditions so indicate - (configure routine).
  - 3. After completion of the execution of the code for the B phase or C phase of a procedure in order to prepare for and mark time until the next interrupt - (wait routine).
  - 4. The executive shall also be invoked at power turn-on - (powerup sequence routine).
- J. The program shall be implemented so that during any specific 200-ms processing cycle, 1 of the 10 procedures shall be operative except during the powerup sequence routine.
- K. The procedures themselves shall consist of calls to specific routines required for implementation of that procedure and logic for determining which routine is to be called next.
- L. The routines, which in different combinations and sequences make up the procedures, have been designed to perform specific functions as defined below.

### 10.2.2 Database

The program shall operate into a dynamic database comprising inputs and outputs, controls, stacks, and scratch pad values stored in RAM, and a static database

consisting of individual constants and tables, such as those for trigonometric functions and scan parameters stored in PROM.

### **10.2.2.1 Software Inputs and Outputs**

This section lists all data type inputs to and outputs from the 1802 microprocessor. There are 64 data inputs and 98 data outputs in the dynamic database for the program. This encompasses both parallel and serial data, as well as external function inputs. Inputs are listed in Table 10-1 and outputs in Table 10-3.

### **10.2.3 Program Executive**

#### **10.2.3.1 Purpose**

The purpose of the program executive is to bring the program on line when power is applied to the EA-1 and to coordinate and direct execution of the program during system operation.

#### **10.2.3.2 Executive Function**

The executive function shall be implemented by four special-purpose routines as follows:

- A. Powerup sequence routine
- B. Interrupt processing routine
- C. Configure routine
- D. Wait routine

From a broader perspective, the executive function may be construed to also include the three procedures: (1) initialize procedure, (2) procedure termination procedure, and (3) the recover procedure, as well as the calling sequence structure of all the procedures. However, the executive function shall be defined as limited to the four special purpose routines cited previously. The detailed functional requirements for each of these four routines are specified as follows.

**Table 10-1. Software inputs - discrete and serial**

| Input no. | Title                     | Software label | Source | Logic 1 indicates |
|-----------|---------------------------|----------------|--------|-------------------|
| 1         | Transmit/Scan Enable      | XMIT           | ADA    | True              |
| 2         | Boom STOW Discrete        | BOOM           | ADA    | True              |
| 3         | Radar Standby             | RADSTB         | GCIL   | True              |
| 4         | Radar On                  | RADON          | GCIL   | True              |
| 5         | Comm Standby              | COMSTB         | GCIL   | True              |
| 6         | Comm On                   | COMON          | GCIL   | True              |
| 7         | GPC Designate             | GPCDES         | GCIL   | True              |
| 8         | GPC                       | GPC            | GCIL   | True              |
| 9         | Manual Slew               | MANUAL         | GCIL   | True              |
| 10        | Autotrack                 | AUTO           | GCIL   | True              |
| 11        | Search Initiate           | SIMAN          | D&C    | True              |
| 12        | Radar Active              | RADACT         | D&C    | True              |
| 13        | Slew Rate Fast            | FAST           | D&C    | True              |
| 14        | Slew Rate Slow            | SLOW           | D&C    | True              |
| 15        | Slew Up                   | UP             | D&C    | True              |
| 16        | Slew Down                 | DOWN           | D&C    | True              |
| 17        | Slew Left                 | LEFT           | D&C    | True              |
| 18        | Slew Right                | RIGHT          | D&C    | True              |
| 19        | Lobing Enable Radar       | RLBEN          | EA-2   | FALSE             |
| 20        | Operate                   | OPER           | DA     | True              |
| 21        | Alpha Encoder MIP         | NEWA           | DA     | True              |
| 22        | Beta Encoder MIP          | NEWB           | DA     | True              |
| 23        | Alpha Encoder             | AENCM          | DA     | True              |
| 24        | Beta Encoder              | BENCM          | DA     | True              |
| 25        | New MDM Data (PF1)        | NEWMDM         | EA-1   | True              |
| 26        | Comm Detect               | COSTAS         | EA-1   | True              |
| 27        | Data Present              | DATAD          | EA-1   | True              |
| 28        | Latched Target Hit        | LATCH          | EA-1   | True              |
| 29        | Side Key                  | SKEY           | EA-1   | ASide             |
| 30        | 50 Ms Flag                | (EF2)          | EA-1   | True              |
| 31        | Self Test Comparator      | (EF3)          | EA-1   | True              |
| 32        | Search Initiate GPC       | SIGPC          | MDM    | True              |
| 33        | TDRS East Select          | EAST           | MDM    | True              |
| 34        | TDRS West Select          | WEST           | MDM    | True              |
| 35        | Spread Spectrum Off/On    | SPREAD         | MDM    | Off               |
| 36        | Ku B/A Select             | KUBA           | MDM    | Ku B              |
| 37        | Self Test On/Off          | STEST          | MDM    | On                |
| 38        | Modulation Control 1      | MODC1          | MDM    | True              |
| 39        | Modulation Control 2      | MODC2          | MDM    | True              |
| 40        | Primary Acq Mode Off/On   | PRIACQ         | MDM    | Off               |
| 41        | GPCDES Inert Stab Off/On  | GPCIS          | MDM    | Off               |
| 42        | Forward Link 216/72       | FWDLNK         | MDM    | 216               |
| 43        | Radar Threshold FIX/VAR   | RFTSB          | MDM    | FIX               |
| 44        | Obscuration Override      | OBOVER         | MDM    | True              |
| 45        | TWT Off                   | TWTOFF         | MDM    | True              |
| 46        | Azimuth Angle Designate   | IMDM3          | MDM    | --                |
| 47        | Elevation Angle Designate | IMDM5          | MDM    | --                |
| 48        | Radar Range Designate     | IMDM7          | MDM    | --                |
| 49        | Rdr Angle Rate Data Good  | ARGOOD         | EA-2   | True              |
| 50        | Rdr Angle Data Good       | AGOOD          | EA-2   | True              |
| 51        | Rdr Range Data Good       | RGOOD          | EA-2   | True              |
| 52        | Rdr Range Rate Data Good  | RRGOOD         | EA-2   | True              |
| 53        | Mini Scan 2               | MINI2          | EA-2   | True              |
| 54        | Operate                   | ROPER          | EA-2   | True              |
| 55        | Forward Link Frame Sync   | FSYNC          | SPA    | True              |
| 56        | Radar Sidelobe            | SLOBE          | EA-2   | True              |
| 57        | Radar Detect              | RDETECT        | EA-2   | True              |
| 58        | Radar Track               | RTRACK         | EA-2   | True              |
| 59        | Actual Range              | IRAD3          | EA-2   | --                |
| 60        | Actual Range Rate         | IRAD6          | EA-2   | --                |

**Table 10-2. Software inputs - discrete and serial (continued)**

| Input no. | Title                   | Software label | Source | Logic 1 indicates |
|-----------|-------------------------|----------------|--------|-------------------|
| 61        | Actual Alpha Angle Rate | IRAD8          | EA-2   | --                |
| 62        | Actual Beta Angle Rate  | IRAD10         | EA-2   | --                |
| 63        | Beta/Beta+Mask Select   | EPC            | MDM    | BETA              |
| 64        | Uplinked Beta Angle     | IMDM9          | MDM    | --                |

**Table 10-3. Software outputs - discrete and serial**

| Output no. | Title                    | Software title | Destination | Logic 1 indicates |
|------------|--------------------------|----------------|-------------|-------------------|
| 1          | Linear Polarization      | LINEAR         | DA          | True              |
| 2          | Widebeam Transmit Select | WBTXS          | DA          | True              |
| 3          | Self Test Atten Bit 1    | ATTEN1         | DA          | --                |
| 4          | Self Test Atten Bit 2    | ATTEN2         | DA          | --                |
| 5          | TWT Inh/Self Test Enable | SIGEN          | DA          | TWTOff            |
| 6          | Alpha Analog Output      | ADAM           | DA          | --                |
| 7          | Beta Analog Output       | BDAM           | DA          | --                |
| 8          | Alpha Feed Forward       | TQA            | DA          | --                |
| 9          | Beta Feed Forward        | TQB            | DA          | --                |
| 10         | Stow Enable 1            | BOOMST         | ADA         | True              |
| 11         | Search Talkback          | SEARCH         | D&C         | True              |
| 12         | Track Talkback           | TRACK          | D&C         | True              |
| 13         | Scan Warning Talkback    | SWARN          | D&C         | True              |
| 14         | Acquisition Enable       | ACQENA         | EA-1        | True              |
| 15         | Power Supply On          | PSON           | EA-1        | True              |
| 16         | Spread Spectrum Off/On   | SSPEC          | EA-1        | OFF               |
| 17         | Comm/Radar               | COMRAD         | EA-1        | COMM              |
| 18         | Zero Gimbal Rate         | JAMENA         | EA-1        | True              |
| 19         | Radar Lobing Static      | RSTAT          | EA-1        | True              |
| 20         | Stow Motor Unlock/Lock   | UNLOCK         | EA-1        | UNLOCK            |
| 21         | Stow Motor On/Off        | STOWM          | EA-1        | ON                |
| 22         | Comm Lobing              | COMLB          | EA-1        | False             |
| 23         | Point/Track Servo CNTRL  | PTRACK         | EA-1        | Point             |
| 24         | Motor Driver On/Off      | MOTON          | EA-1        | On                |
| 25         | Self Test Bit 1          | STCON1         | EA-1        | --                |
| 26         | Self Test Bit 2          | STCON2         | EA-1        | --                |
| 27         | Self Test Bit 3          | STCON3         | EA-1        | --                |
| 28         | Self Test Bit 4          | STCON4         | EA-1        | --                |
| 29         | Surge Inhibit            | SRGINH         | EA-1        | True              |
| 30         | Dither Off/On            | DITHR          | EA-1        | OFF               |
| 31         | Not Gain MS Bit          | X4GNOT         | EA-1        | True              |
| 32         | Gain Mid Bit             | X1G            | EA-1        | True              |
| 33         | Not Gain LS Bit          | X2GNOT         | EA-1        | True              |
| 34         | Fine/Coarse Gyro         | FINCRS         | EA-1        | Fine              |
| 35         | High/Low Bandwidth       | HILO           | EA-1        | High              |
| 36         | Reset Latched Hit        | RLH            | EA-1        | --                |
| 37         | Radar/Comm Mode          | RADCOM         | MDM         | Radar             |
| 38         | Ant Mode AUTO            | AUTO           | MDM         | True              |
| 39         | Ant Mode GPC DESIG       | GPCDES         | MDM         | True              |
| 40         | Ant Mode GPC             | GPC            | MDM         | True              |
| 41         | Rdr Angle Data Good      | AGOOD          | MDM         | True              |
| 42         | Rdr Angle Rate Data Good | ARGOOD         | MDM         | True              |
| 43         | Rdr Slf Tst in Progress  | SELF           | MDM         | True              |
| 44         | Ku B/A Select            | KUBA           | MDM         | KU B              |
| 45         | Search                   | SCANNG         | MDM         | True              |
| 46         | Detect                   | DETECT         | MDM         | True              |

**Table 10-2. Software outputs - discrete and serial (continued)**

| Output no. | Title                     | Software title | Destination | Logic 1 indicates |
|------------|---------------------------|----------------|-------------|-------------------|
| 47         | Track                     | TRACK          | MDM         | True              |
| 48         | Operate                   | OPER           | MDM         | True              |
| 49         | EA-1 Sif Tst Status       | E1TEST         | MDM         | PASS              |
| 50         | DA Sif Tst Status         | DATEST         | MDM         | PASS              |
| 51         | EA-2 Sif Tst Status       | E2TEST         | MDM         | PASS              |
| 52         | System Sif Tst Status     | SYSTST         | MDM         | PASS              |
| 53         | TDRS West (Latched)       | TDWEST         | MDM         | True              |
| 54         | TDRS East (Latched)       | TDEAST         | MDM         | True              |
| 55         | Forward Link Frame Sync   | FSYNC          | MDM         | True              |
| 56         | Data Present              | DATAP          | MDM         | True              |
| 57         | Scan Warn Limit           | SCWARN         | MDM         | True              |
| 58         | Rdr Range Data Good       | RGOOD          | MDM         | True              |
| 59         | Rdr Range Rate Data Good  | RRGOOD         | MDM         | True              |
| 60         | Rdr Threshold FIX/VAR     | RFTSB          | MDM         | FIX               |
| 61         | Obscuration Override      | OBOVER         | MDM         | True              |
| 62         | Actual Azimuth Angle      | OMDM5          | MDM         | --                |
| 63         | Actual Elevation Angle    | OMDM7          | MDM         | --                |
| 64         | Actual Range Rate         | OMDM9          | MDM         | --                |
| 65         | Actual Range              | OMDM13         | MDM         | --                |
| 66         | Azimuth Angle Rate        | OMDM17         | MDM         | --                |
| 67         | Elevation Angle Rate      | OMDM19         | MDM         | --                |
| 68         | Actual Azimuth Angle      | ODC1           | D&C         | --                |
| 69         | Actual Elevation Angle    | ODC4           | D&C         | --                |
| 70         | Actual Range Rate         | ODC7           | D&C         | --                |
| 71         | Actual Range              | ODC10          | D&C         | --                |
| 72         | Acquisition Inhibit       | ACQINH         | EA-2        | True              |
| 73         | Ant Mode Bit 1            | MODEB1         | EA-2        | --                |
| 74         | Ant Mode Bit 2            | MODEB2         | EA-2        | --                |
| 75         | Rdr Threshold FIX/VAR     | RFTSB          | EA-2        | FIX               |
| 76         | Main Scan                 | MAIN           | EA-2        | True              |
| 77         | Mini Scan                 | MINI           | EA-2        | True              |
| 78         | Provide Test Target       | TARGET         | EA-2        | True              |
| 79         | Radar Active/passive      | RADACT         | EA-2        | ACT               |
| 80         | Radar Range Designate     | ORAD3          | EA-2        | --                |
| 81         | TDRS East Selected        | TDEAST         | SPA         | True              |
| 82         | TDRS West Selected        | TDWEST         | SPA         | True              |
| 83         | Ku B/A Select             | KUBA           | SPA         | KU B              |
| 84         | Modulation Control 1      | MODC1          | SPA         | True              |
| 85         | Modulation Control 2      | MODC2          | SPA         | True              |
| 86         | Ant Mode Bit 1            | MODEB1         | SPA         | --                |
| 87         | Ant Mode Bit 2            | MODEB2         | SPA         | --                |
| 88         | Forward Link 216/72       | FWDLNK         | SPA         | 216               |
| 89         | Data Present              | DATAP          | SPA         | True              |
| 90         | Signal Present            | SIGNAL         | SPA         | True              |
| 91         | Pri Acq Mode Off/On       | PRIACQ         | SPA         | Off               |
| 92         | Set LSB (OSPA2)           | --             | SPA         | --                |
| 93         | Act Azimuth Angle Rate    | WR             | D&C         | --                |
| 94         | Act Elevation Angle Rate  | WP             | D&C         | --                |
| 95         | Transmit RF Threshold     | --             | EA-1        | --                |
| 96         | Signal Strength Threshold | --             | EA-1        | --                |
| 97         | Alpha Error Threshold     | --             | EA-1        | --                |
| 98         | Beta Error Threshold      | --             | EA-1        | --                |



#### **10.2.3.2.1 Powerup sequence routine**

When power to the EA-1 is switched from OFF to ON, the program shall perform the following functions:

- A. Configure the program executive controls so that on the occurrence of the first interrupt after completing execution of the configuring code, the microprocessor will respond to the interrupt and trap to the interrupt processing subroutine.
- B. Configure the program executive controls so that the first procedure to be called by the interrupt processing routine shall be the initialize procedure.
- C. Enable the hardware interrupt line to the microprocessor.
- D. Maintain the microprocessor in NO-OP state until the first interrupt occurs following enabling of the hardware interrupt line.

#### **10.2.3.2.2 Interrupt processing routine**

When an interrupt occurs, the following functions shall be performed:

- A. The program shall be interrupted, and control shall be transferred to the interrupt processing routine.
- B. The interrupt processing routine shall reconfigure the executive controls of the program so that new 100-ms (nominal) processing period shall be initiated.
- C. The interrupt processing routine shall reenable the interrupt line to the microprocessor before exiting.
- D. The interrupt processing routine shall determine whether or not processing for the previous 100-ms period was completed when the interrupt occurred. If it was not, this routine shall branch to the A branch of the recover procedure. Otherwise, this routine shall branch to the A branch of whichever of the other nine procedures had been previously identified as the current procedure.

#### **10.2.3.2.3 Configure routine**

The purpose of the configure routine shall be to perform the following functions:

- A. Periodically evaluate system status and incoming commands.
- B. Make a determination based on this evaluation as to which system procedure is to be executed for the next program cycle.
- C. Configure executive controls to implement execution of the selected procedure.

##### **10.2.3.2.3.1 Functional requirements for the configure routine**

Functional requirements for the configure routine shall be as follows:

A. Frequency of execution

This routine shall be executed once every 200 ms after the reading in of discrete and MDM inputs and immediately before the B phase of the program cycle.

B. Determination of procedure to execute

Determination of which procedure to execute for the next 200-ms period shall be based on a prioritized sequence of evaluating command and system status flags as specified below.

1. Priority 1 - Initialization. If the initialization procedure is in progress, maintain it in progress until it has been completed.
2. Priority 2 - Determine if the system has been commanded to one of the three valid operating states: COMM ON, RADAR ON, or STANDBY. If so, proceed to priority 3. If none of these states is sensed as being commanded, configure to the idle procedure until one of the operating states is sensed as commanded or until power goes down.
3. Priority 3 - The deployed assembly shall be stowable from either the ON or STANDBY states. Evaluate BOOM. Configure for the deploy procedure if there is a STOW command and no positive indication that the antenna is already locked in the stow position. If there is a positive indication that it is locked, configure for the idle procedure. In the absence of a STOW command, if COMM ON or RADAR ON has been commanded, proceed to priority 4. If STANDBY has been commanded, configure for the idle procedure.
4. Priority 4 - Evaluate transmit/scan enable (XMIT). If false, determine if self-test (STEST) has been commanded for the stowed or 30° deployed position with the RADAR ON mode activated. If so, proceed to the self-test procedure; otherwise, proceed to the idle procedure. Alternatively, if XMIT is true, proceed to priority 5.
5. Priority 5 - Evaluate antenna deployment status. Configure for the deploy procedure if the antenna deployment status is invalid. If valid, proceed to priority 6.
  - a. Deployment status shall by definition be invalid in either of the following cases.
    - (1) From the time power is applied to the EA-1 unit
    - (2) From any time the antenna is positioned to the stow position under a STOW command until the encoders have been (re)initialized and the antenna (re)positioned to the zenith
6. Priority 6 - Evaluate self-test command for fully deployed state. Configure for the self-test procedure if STEST is true and the system is in radar mode.

7. Control system readiness status - If the status of the system is such that the conditions for priorities 1 through 6 have all been tested with the result that none on the associated procedures is currently required, the system is ready for mission assignment. This status is defined as the state of Control System Readiness (CSR) and is represented by the following conditions:
  - a. Initialization is completed.
  - b. COMON or RADON is true.
  - c. BOOM is false.
  - d. XMIT is true.
  - e. Antenna deployment status is valid.
  - f. STEST is false.
8. Priority 7 - Evaluate GPCDES, GPC, AUTO, and MANUAL in that order. At the priority 7 level, selection of the required procedure shall be determined by the indicated steering mode shown in (b) below and, in the case of GPC and AUTO, also by system status conditions as defined in the specified requirements for the individual procedures.
  - a. In the absence of a steering mode input bit, the system shall default to MANUAL.
  - b. Procedures as a function of steering mode.

| <b>Steering mode</b> | <b>Procedure</b>      |
|----------------------|-----------------------|
| GPCDES               | Point                 |
| GPC                  | Point, scan, or track |
| AUTO                 | Slew, scan, or track  |
| MANUAL               | Slew                  |

C. Handover function

When in GPCDES or GPC in comm mode, the configure routine shall test the EAST and WEST flags every cycle (200 ms) to determine if there has been a false to true change in the state of these flags since the last cycle. The ground rule for performing this test is that EAST And WEST will never both be true at the same time. If there has not been a false to true transition of either flag, the program shall proceed normally.

If there has been a false to true change, the following shall be performed:

1. Set or reset the control flags specified below, as indicated by the following equations:

- a.  $EAST \bullet \overline{TDEAST} = \text{Set TDEAST, reset TDWEST}$
- b.  $WEST \bullet \overline{TDWEST} = \text{Set TDWEST, reset TDEAST}$

- 2. Acknowledgment of system recognition of the EAST-WEST flag change shall be transmitted to the MDM in the next MDM serial data output block.
- 3. If the system is tracking when the change occurs, by definition a handover condition is said to exist and the program shall cause the system to break track.
- 4. The program shall cause the system to proceed to the point procedure as the next operational procedure.

D. Timeout function

If, while the system is scanning in either main scan or mini scan, a target detection occurs in either comm or radar mode, a timeout period shall be initiated and the following requirements shall be implemented.

- 1. For both radar and comm modes, the timeout flag shall be true for  $120 \pm 10$  ms and then set false.
- 2. As long as the timeout flag is true, the program shall continue in the scan procedure.
- 3. When the timeout flag is false, the operational procedure selected to be performed next shall be determined according to the requirements specified for the individual procedures.

E. Configuring for procedure termination

The configure routine shall keep track of the procedure currently being executed. Whenever the configure routine determines that the next operational procedure to be executed is different from the current operational procedure, it shall

- 1. Cause the procedure termination procedure to be executed for one 200-ms processing cycle immediately following the current operational procedure and before initiation of the next operational procedure.
- 2. Set the PFIRST flag true. This flag shall remain true only for the first 200-ms cycle of each procedure.

F. Control flags ACQEN and PNTTRK

The ACQEN and PNTTRK control flags shall be set true or false during execution of the configure routine so that, upon exiting from this routine, they shall be in the status defined by the following equations:

\_\_\_\_\_

$$1. \quad ACQEN(1) = CRS \cdot GPC \cdot ZONEI \cdot (TRKING + RADAR + HANDOVER) \\ + CSR \cdot AUTO \cdot \overline{FSTSLW}$$

$$ACQEN(0) = ACQEN(1)$$

$$2. \quad PNTTRK(1) = \overline{PNTTRK(0)}$$

$$PNTTRK(0) = ACQEN \cdot (RLBEN \cdot RADON = COMON \cdot TRKING \cdot \\ PFIRST)$$

G. Target detect signals

The configure routine shall be implemented so that the radar lobing enable input to the program is operative only when the system is in radar mode.

H. Target acquisition timing

1. Radar acquisition - The radar acquisition logic involves two discrettes that are received from the EA-2 radar processor. The target present discrete shall cause the gimbal rate commands to be nulled by analog circuitry within 1 ms and, subsequently, the commanded gimbal rates generated by the microprocessor to be set to zero and maintained at zero until miniscan is initiated. The second logic signal from the EA-2, radar lobing enable, shall cause the radar track loop to be closed.

a. The total time from the initial target detect (TARGET PRESENT) until the first nonzero output gimbal rate in miniscan shall not exceed 470 ms.

b. The total time from the initial target detect (TARGET PRESENT) until the outputting of the miniscan flag (MINI) to the EA-2 shall not exceed 600 ms.

c. The total time from the confirmed target detect (radar lobing enable) until the closing of the track loop (outputting of point/track command in the track state) shall not exceed 200 ms and may be as short as 5 ms.

d. During the radar acquisition process, as the system transitions from scan to track through procedure termination, the following signals shall be switched, as specified in Sections 10.4.4.8.2.3 and 10.4.4.8.2.5:

(1) Bandwidth

(2) Gyro

(4) Dither

The timing requirement is that, upon a detection in miniscan, these signals shall be switched  $205 \pm 10$  ms after point/track is switched to the

track state. This will result in shifting the transients associated with these signals into a time slot occurring approximately 200 to 400 ms after the detection occurred, thus avoiding interference with the positioning of the antenna during the backup process. This requirement shall apply for both GPC and AUTO for radar mode only. This requirement does not apply to switching the above signals for detections occurring when not scanning; for example, during slow slew in AUTO where the gyro shall be switched from coarse to fine at the same time point/track is switched to the track state.

2. COMM acquisition - At target detect (COSTAS) the output rates to the gyros shall be commanded to zero. The zero rate commands shall be held for a period of time such that the total time from a target detect until the events described below shall not exceed the corresponding times specified for each event.
  - a. 480 ms - Transition from main scan to the first nonzero rate output in miniscan
  - b. 730 ms - Transition from miniscan to track
  - c. 1130 ms - Transition from main scan to the first nonzero rate output in miniscan to track when COSTAS LOCK is a step function rather than a pulse

At the completion of the zero rate period, the program shall configure the system as specified below:

- a. If COSTAS LOCK goes true while the system is in main scan, the program shall cause the system to transition to miniscan, regardless of the width of the COSTAS pulse.
- b. If COSTAS LOCK (LATCH) is sensed as true while the system is in miniscan, the program shall cause the system to transition to track, regardless of the width of the COSTAS pulse. In fact, the new COSTAS pulse may be a continuation of the COSTAS pulse that caused the transition from main scan to miniscan.
- c. In COMM GPC with the Line of Sight (LOS) within  $0.3^\circ$  of the designate or in COMM AUTO and not fast slewing, if COSTAS LOCK goes true when the system is not scanning, the program shall cause the system to transition directly to track regardless of the width of the COSTAS pulse.
- d. Once track is entered, the track state shall be maintained for a period of 6 seconds, after which the decision of whether to continue in the track state or break track shall be determined by the presence or absence of COSTAS LOCK.

- e. If the system is in primary acquisition mode, the COSTAS flag in the software database shall be set true every time configure is executed during the initial 6-second track hold so that the system will not be toggled between widebeam and narrowbeam during the 6 seconds, as a result of the possible alternating on-off characteristic of the COSTAS LOCK signal during early phases of acquisition.
- f. If the system is in primary acquisition mode, the total time from a target detect (COSTAS LOCK) in miniscan until the zero-setting of the wideband transmit select command (WBTXS) shall not exceed 530 ms.
- g. The outputting of PNTTRK (low) shall occur  $196.6 \pm 5$  ms after the zero-setting of WBTXS to allow adequate time for switching from widebeam to delta channel select.
- h. When a detection occurs (LATCH), the dither control flag shall be set false and shall remain false until the system enters miniscan or track, at which time the dither control flag shall be set true. Timing requirements are as follows:

| <b>Transitioning from</b> | <b>Dither shall be off</b> |
|---------------------------|----------------------------|
| Main scan to miniscan     | $390 \pm 10$ ms            |
| Miniscan to track         | $510 \pm 10$ ms            |
| Main scan to track        | $905 \pm 10$ ms            |
| Point or slew to track    | $585 \pm 10$ ms            |

#### 10.2.3.2.4 Wait routine

The primary purpose of the wait routine is to hold the program in a NO-OP state during each 100-ms processing period after all program procedure code for that 100-ms period has been executed and until the occurrence of the next interrupt. The following functions shall be performed:

- A. Set a flag to indicate that all processing for the current 100-ms period has been completed.
- B. Set a flag to indicate whether the processing just completed was for the B branch or C branch of the procedure being executed.
- C. Execute NO-OP instructions until the next interrupt occurs.

#### 10.2.3.2.5 Powerdown function

The executive shall also be responsible for the monitoring of conditions that require a powerdown operation. This function shall be implemented as follows:

- A. If and whenever the condition arises that all four of the flags

1. COMON
2. RADON
3. COMSTB
4. RADSTB

are sensed as false for a period of  $2 \pm 0.3$  seconds, the Power Supply On Control (PSON) shall be commanded to the OFF state.

- B. This function shall have priority over stowing the deployed assembly.
- C. This requirement shall be applicable at all times starting with and subsequent to the initialize procedure.

### 10.3 PROCEDURES

#### 10.3.1 Initialize Procedure

##### 10.3.1.1 Purpose

The purpose of the initialize procedure shall be to initialize the program database and controls at the time of power turnon and to provide a 60-second delay for gyro spinup before proceeding to the operational program.

##### 10.3.1.2 Initialization of Database and Controls

As a result of processing the first interrupt after completion of the powerup sequence, the initialize procedure shall be executed. This procedure shall perform the following functions:

- A. During the first 200-ms cycle (and only during that cycle) of the initialize procedure, that part of the RAM database assigned to input words, output words, and control words shall be initialized so that all numerical quantities are zeroed and all control flags are in the off state, with the following exceptions:
  1. Executive control words and flags necessary to implement further execution of the initialize procedure
  2. Flags which actuate the following specified system controls, which shall be set to the states indicated below:
    - a. PSON - commanded to ON
    - b. POINT/TRACK Switch (PNTTRK) - commanded to POINT position
    - c. Transmitter inhibited



- B. The initialize procedure shall cause both feed forward Digital-to-Analog Converters (DACs) to be initialized with the hexadecimal value 80.
- C. The initialize procedure shall continue for a total period of  $60 \pm 1$  seconds.
- D. In addition to the above mentioned specific initialization functions, the following functions shall be performed once every 200 ms during the entire 60-second initialization period.
  - 1. Input discrete data
  - 2. Input MDM data if NEWMDM data are indicated
  - 3. Output discrete data
  - 4. Output Line Replaceable Unit (LRU) serial data if NEWMDM data are indicated
  - 5. Output MDM and D and C serial data

### **10.3.2 Procedure Termination Procedure**

#### **10.3.2.1 Purpose**

The purpose of the procedure termination procedure shall be to provide a smooth transition from one procedure to another by performing specific reinitialization functions during the 200-ms transition period.

#### **10.3.2.2 Conditions for Calling Procedure Termination Procedure**

This procedure shall be called under the conditions specified in Section 10.2.3.2.3.1.E.

#### **10.3.2.3 Functional Requirements**

The following functions shall be performed during the execution of this procedure:

- A. Output zero drive rates ( $\omega\alpha$ ,  $\omega\beta$ ) to the rate DACs.
- B. Output zero feed forward torque (TQA, TQB) to the feed forward DACs.
- C. Zero the position loop integrators.
- D. If the point/track flag indicates track, set system to fine gyro and bandwidth to low.
- E. Zero the angle rate word storage locations so that the values transmitted every 200 ms to the MDM will be zeros unless the track procedure is being executed.
- F. If the previous procedure was either the self-test or idle procedure, command the servo drive motors on (MOTON).

- G. If the previous procedure was the track procedure, reset ZONEI.
- H. Reset those executive words and flags that must be in the zero state at the beginning of the execution of all procedures. This shall include such flags as may be set during any given procedure that could lead to incorrect execution of the subsequent procedure if not zero set.
- I. If the previous procedure was the scan procedure, reset LVSCAN.
- J. Transform designate angles from shuttle coordinates to gimbal coordinates unless entering this procedure from the scan procedure.
- K. Output discrete data.
- L. Output LRU serial data.
- M. Execute the obscuration routine twice; that is, once during each 100-ms processing cycle.
- N. Input encoder position angles once during each 100-ms processing cycle.
- O. Transform encoder position angles from gimbal coordinates to shuttle coordinates.
- P. Output MDM and D and C serial data.

### **10.3.3 Recover Procedure**

#### **10.3.3.1 Purpose**

The purpose of the recover procedure shall be to provide an orderly sequence of events so that if processing is still in progress when the interrupt occurs, the program can recover and resume normal operation.

#### **10.3.3.2 Definition of Resumption of Normal Operation**

- A. In connection with execution of the recover procedure, resumption of normal operation shall be defined as reinitialization of the program through execution of the procedure termination procedure and the subsequent initialization of one of the following procedures:
  - 1. Idle procedure
  - 2. Deploy procedure
  - 3. Point procedure
  - 4. Slew procedure
  - 5. Scan procedure

6. Track procedure
  7. Self-test procedure
- B. The procedure selected by the configure routine shall be executed from the beginning of that procedure, and all data processed by the procedure being executed when the recover procedure was activated shall be considered invalid.

### **10.3.3.3 Conditions for Calling Recover Procedure**

The recover procedure shall be called by the interrupt processing routine as specified in Section 10.2.3.2.2.D.

### **10.3.3.4 Functional Requirements**

- A. The following functions shall be performed during the A branch of this procedure:
1. Output zero drive rates ( $\omega\alpha$ ,  $\omega\beta$ ) to the rate DACs
  2. Output zero feed forward torque (TQA, TQB) to the feed forward DACs
  3. Command dither off
  4. Execute obscuration routine
  5. Determine whether to branch next to the B or C branch of this procedure
- B. The C branch shall be an immediate branch to the wait routine.
- C. In the B branch the following functions shall be performed:
1. Input discrete data
  2. Input MDM data if NEWMDM is true
  3. Branch to the configure routine
- D. The recover procedure shall, by definition, have completed execution upon entering the configure routine. Upon completion of the execution of the configure routine, a different procedure shall have been selected, however, with first a call for the execution of the procedure termination procedure.

### **10.3.4 Idle Procedure**

#### **10.3.4.1 Purpose**

The purpose of the idle procedure shall be to maintain the system in a standby state under the conditions specified below.

#### 10.3.4.2 Transition to the Idle Procedure

Incoming mode commands (COMON, RADON, COMSTB, and RADSTB) are defined as mutually exclusive; however, the program shall sample them in the order given and respond to the first one determined to be true. In light of this, the program shall transition to the idle procedure if one of the following conditions is true, provided that the initialize procedure has been completed.

- A. A standby mode is commanded, and the boom stow command (BOOM) is not present.
- B. All four mode commands are false (switch bounce case).
- C. One of the mode commands is true, boom stow is commanded; however, the antenna is verified as locked.
- D. COMON is true with boom stow and transmit/scan enable (XMIT) false.
- E. RADON is true with boom stow, transmit/scan enable, and radar self-test false.

#### 10.3.4.3 Functions Performed During Idle Procedure

If transition to the idle procedure occurs, that procedure shall be executed so long as at least one of the above conditions exists. During the idle procedure, the following functions shall be performed:

- A. Dither shall be commanded to the state defined in Section 10.4.4.8.2.5.C.
- B. The gimbal motors shall be commanded off.
- C. Once every 100 ms, the following functions shall be performed:
  - 1. The encoder angles shall be read into the database.
  - 2. The obscuration routine shall be executed.
- D. Once every 200 ms, the following functions shall be performed:
  - 1. Input discrete data.
  - 2. Input MDM data if NEWMDM data are indicated.
  - 3. Transform designate angles from shuttle coordinates to gimbal coordinates.
  - 4. Output discrete data.
  - 5. Output LRU serial data.
  - 6. Input LRU serial data.

7. Transform encoder position angles from gimbal coordinates to shuttle coordinates.
8. Output MDM and D and C serial data.

### 10.3.5 Deploy Procedure

#### 10.3.5.1 Purpose

On command from the orbiter, the deploy procedure shall deploy the antenna and initialize the encoders or alternatively stow the antenna and verify that it is locked in the stow position.

#### 10.3.5.2 Subfunctions

The above functions shall be implemented through the use of the following seven independent subfunctions, which shall be executed in different sequences in response to orbiter commands and system status.

- A. Retract locking pins
- B. Insert locking pins
- C. Initialize encoders
- D. Drive to zenith
- E. Drive to stow position
- F. Wiggle test
- G. Gimbal stop check

The following table, Table 10-4, provides gimbal reference data.

**Table 10-4. Gimbal reference data**

| Parameter, degrees       | $\alpha$ axis | $\beta$ axis |
|--------------------------|---------------|--------------|
| Stow angle (nominal)     | 124.3         | -27.5        |
| Master Index Pulse (MIP) | 116.5         | -23.25       |
| Positive stop            | 154.0         | 75.0         |
| Negative stop            | -206.0        | -85.0        |

In the following paragraphs, requirements for each of the individual subfunctions are set forth and the requirements relative to sequencing of these subfunctions are specified.

#### 10.3.5.2.1 Retract locking pins

When called, the following functions shall be performed:

- A. Command gimbal motors off
- B. Command the gimbal lock motor, when activated, to retract the locking pins
- C. Set LOCKED false
- D. After a timeout of 800 ms, command lock motor on
- E. After a further timeout of 30 seconds, command lock motor off
- F. Command gimbal motors on

#### **10.3.5.2.2 Insert locking pins**

When called, the following functions shall be performed:

- A. Command the gimbal lock motor, when activated, to drive the locking pins into the locked position
- B. After a timeout of 4 seconds, command lock motor on
- C. After a timeout of 30 seconds, command lock motor off

#### **10.3.5.2.3 Initialize encoders**

When called, the following functions shall be performed:

- A. The gimbal stop check subroutine shall be executed every 100 ms when the initialize encoders operation is being performed.
- B. The operation to initialize the encoders shall command the antenna along the  $\beta$  axis in the positive direction at the rate of 20 deg/sec. During this time, the  $\alpha$  rate shall be zero.
- C. So long as the  $\beta$  MIP is not sensed in the positive direction, the antenna shall continue in the positive direction until it encounters the positive  $\beta$  stop, at which time it shall reverse direction.
- D. So long as the  $\beta$  MIP is not sensed in the negative direction, the antenna shall continue moving in the negative direction until it encounters the negative  $\beta$  stop.
- E. A time limit of 20 seconds shall be allocated for the entire  $\beta$  MIP search.
- F. The search for the  $\beta$  MIP shall be terminated and the search for the  $\alpha$  MIP shall be initiated when any one of the following conditions becomes true:
  - 1. The  $\beta$  MIP is sensed.

2. The negative  $\beta$  stop has been reached.
  3. The  $\beta$  time limit has elapsed.
- G. Then command the antenna along the  $\alpha$  axis in the negative direction at the rate of 20 deg/sec. During this time, the  $\beta$  rate shall be zero.
- H. So long as the  $\alpha$  MIP is not sensed in the negative direction, the antenna shall continue in the negative direction until it encounters the negative  $\alpha$  stop, at which time it shall reverse direction.
- I. So long as the  $\alpha$  MIP is not sensed in the positive direction, the antenna shall continue moving in the positive direction until it encounters the positive  $\alpha$  stop.
- J. A time limit of 40 seconds shall be allocated for the entire  $\alpha$  MIP search.
- K. The search for the  $\alpha$  MIP shall be terminated when any one of the following conditions becomes true:
1. The  $\alpha$  MIP is sensed.
  2. The positive  $\alpha$  stop has been reached.
  3. The  $\alpha$  time limit has elapsed.
- L. If either the  $\alpha$  MIP or the  $\beta$  MIP is not found in the time allocated, the assumption is that the correct MIP values were actually loaded into the encoder counter registers but there has been a failure in transmitting this fact to the microprocessor. In this case, all system operations shall proceed as if both MIPs had been found, except that the program shall cause the transmitter to be inhibited.

#### 10.3.5.2.4 Drive to zenith

When called, the following functions shall be performed:

- A. Command the servo system to drive the antenna to the zenith position via the position loop subroutine:
- $\alpha = 0^\circ$
- $\beta = 0^\circ$
- B. A time limit of 22 seconds shall be allocated for the antenna to reach the zenith position.
- C. This subfunction shall be terminated when either of the following conditions becomes true:
1. The antenna has reached the zenith position with a tolerance of  $\pm 0.3^\circ$ .

2. The time limit has elapsed.

#### 10.3.5.2.5 Drive to stow position

When called, the following functions shall be performed:

- A. Command the servo system to drive the antenna to the stow position via the position loop subroutine:  
 $\alpha = 124.3 \pm 0.1^\circ$  Az =  $-125^\circ$   
 $\beta = -27.5 \pm 0.1^\circ$  El =  $-29^\circ$
- B. A time limit of 22 seconds shall be allocated for the antenna to reach the stow position.
- C. This subfunction shall be terminated when either of the following conditions becomes true:
  1. The antenna has reached the stow position with a tolerance of  $\pm 0.3^\circ$ .
  2. The time limit has elapsed.

#### 10.3.5.2.6 Wiggle test

When called, the following functions shall be performed:

- A. Command the servo system to drive the antenna in the positive  $\alpha$  and  $\beta$  directions simultaneously at the rate of 20 deg/sec on each axis for a period of 1 second.
- B. The servo system shall then be commanded to drive the antenna in the negative  $\alpha$  and  $\beta$  directions simultaneously at the rate of 20 deg/sec for a period of 1 second.
- C. A measurement shall then be made to determine how much movement, if any, has occurred.
- D. If such movement is determined to be less than  $0.704^\circ$  peak-to-peak on each axis, the wiggle test is defined as having passed.
- E. If such movement is determined to be  $\geq 0.704^\circ$  peak-to-peak on either axis, the wiggle test is defined as having failed.

#### 10.3.5.2.7 Gimbal stop check

The purpose of this subfunction shall be to determine if the antenna has encountered a physical stop.

- A. This function shall be performed for each axis independently every 100 ms during execution of initialize encoders subfunction.



- B. Successive measurements of encoder position shall be processed so that when total movement of the antenna on the axis being tested does not exceed  $0.0880^\circ$  during a 300-ms period, a flag shall be set indicating that the antenna is at a stop position. This requirement is subject to the following exception.
- C. Once the flags have been set for the first stop encountered on the respective axes, they shall not be set for the second stop until it is established that the antenna has actually moved. The criterion for this shall be a measured movement of  $0.704^\circ$  or more within a 300-ms period.

### **10.3.5.3 Sequencing of Subfunctions**

The following subfunction sequences shall be implemented corresponding to the given commands from the orbiter and the stated system status conditions. These sequences shall be implemented only if the initialize procedure has been completed.

#### **10.3.5.3.1 Unstow operation commanded**

- A. This operation shall be performed when all the following conditions exist:
  - 1. COMON or RADON true.
  - 2. BOOM false.
  - 3. XMIT true.
  - 4. Antenna deployment status is invalid, as defined in Section 10.2.3.2.3.1.B(5)(a).
- B. The sequence of subfunctions for this operation shall be as follows:
  - 1. Retract locking pins
  - 2. Initialize encoders
  - 3. Drive to zenith
- C. The program shall then terminate the deploy procedure.

#### **10.3.5.3.2 Stow operation commanded**

- A. This operation shall be performed when the following conditions exist:
  - 1. COMON, RADON, COMSTB, or RADSTB true
  - 2. BOOM true
- B. If there is a positive indication that the antenna is already locked in the stow position, the deploy procedure shall be terminated.

- C. In the absence of a locked condition, if there is a positive indication that the deployment status of the antenna is valid, the sequence of subfunctions shall be as follows:
1. Drive to stow position
  2. Insert locking pins
  3. Wiggle test
    - a. If wiggle test passes:
      - (1) Command gimbal motors off
      - (2) Set LOCKED true
      - (3) Terminate deploy procedure
    - b. If wiggle test fails:
      - (1) Retract locking pins
      - (2) Repeat steps (1), (2), and (3) ad infinitum
- D. If power has just been applied to the EA-1, of necessity, the locked status and deployment status of the antenna are electronically unknown and, therefore, the sequence of subfunctions for this case shall be as follows:
1. Command gimbal motors on
  2. Wiggle test
    - a. If wiggle test passes:
      - (1) Command gimbal motors off
      - (2) Set LOCKED true
      - (3) Terminate deploy procedure
    - b. If wiggle test fails:
      - (1) Retract locking pins
      - (2) Initialize encoders
      - (3) Drive to stow position
      - (4) Insert locking pins
      - (5) Wiggle test

If wiggle test passes:

- (a) Command gimbal motors off
- (b) Set LOCKED true
- (c) Terminate deploy procedure

If wiggle test fails:

- (a) Retract locking pins
- (b) Drive to stow position
- (c) Insert locking pins
- (d) Wiggle test - If test fails, repeat these last four steps ad infinitum or until the wiggle test passes.

- E. If a BOOM command occurs while the system is performing the unstow operation and before that operation is completed, the program shall perform the same sequence of functions as specified in paragraph D above, beginning with subfunction D.2.

#### **10.3.5.4 Other Functions Performed During Deploy Procedure**

- A. Once every 100 ms, the following functions shall be performed:
  - 1. Read encoder angles into the database.
  - 2. Execute obscuration routine.
  - 3. Perform gimbal stop check function.
- B. Once every 200 ms, the following functions shall be performed:
  - 1. Input discrete data.
  - 2. Input MDM data if NEWMDM data are indicated.
  - 3. Output discrete data.
  - 4. Output LRU serial data.
  - 5. Input LRU Serial data.
  - 6. Transform encoder position angles from gimbal coordinates to shuttle coordinates.
  - 7. Output MDM and D and C serial data.

### 10.3.6 Point Procedure

#### 10.3.6.1 Purpose

The purpose of the point procedure shall be to implement the pointing function and associated operations when the system is in GPCDES or GPC mode and is responding to orbiter-generated designates.

#### 10.3.6.2 Conditions for Calling Point Procedure

If the system is in a state of control system readiness, this procedure shall be called under one of the following conditions:

- A. When in GPC designate mode
- B. When in GPC mode with antenna LOS more than  $0.3^\circ$  away from the designate
- C. When in GPC mode with antenna less than  $0.3^\circ$  from the designate, scanning has not started, there is no indication of target detection in either comm or radar mode, and at least one of the following conditions is true:
  - 1. There is NEWMDM data.
  - 2. There is no GPC command to initiate scanning.
- D. When in GPC mode with antenna less than  $0.3^\circ$  from the designate and scanning has not started, but the system is in radar mode with target present true. The purpose of this requirement is to preclude initiating a scan pattern if there is a detection precisely at or very close to the designate, and to hold the system in pointing mode until radar lobing enable is activated.

#### 10.3.6.3 Functional Requirements

The following functions shall be performed during the execution of the point procedure:

- A. Once every 100 ms the following functions shall be performed:
  - 1. Read encoder angles into the data base
  - 2. Execute position loop routine
  - 3. Execute obscuration routine
- B. Once every 200 ms the following functions shall be performed:
  - 1. Input discrete data.
  - 2. Input MDM data if NEWMDM data are indicated.
  - 3. Output discrete data.

4. Transform designate angles from shuttle coordinates to gimbal coordinates.
5. Output LRU serial data.
6. Input LRU serial data.
7. Transform encoder position angles from gimbal coordinates to shuttle coordinates.
8. Output MDM and D and C serial data.

### **10.3.7 Slew Procedure**

#### **10.3.7.1 Purpose**

The purpose of the slew procedure shall be to implement slewing of the antenna in response to slew commands from the orbiter when the system is in AUTO TRACK or MANUAL SLEW mode. These commands are received in the EA-1 unit in the form of discrettes to slew fast, slow, right, left, up, or down with reference to the orbiter azimuth/elevation coordinate system.

#### **10.3.7.2 Conditions for Calling Slew Procedure**

If the system is in a state of control system readiness, this procedure shall be called under one of the following conditions:

- A. When in MANUAL SLEW mode
- B. When in AUTO TRACK mode and
  1. Scanning has not started and
  2. There is no control panel search command to initiate scanning and
  3. There is no indication of a target detection in either comm or radar mode
- C. When in AUTO TRACK mode and
  1. Scanning has not started and
  2. The system is in radar mode with target present true

#### **10.3.7.3 Functional Requirements**

The following functions shall be performed during the execution of the slew procedure:

- A. Pseudo-designates shall be calculated as a function of slew commands in accordance with the following requirements:

1. In order to calculate a pseudo-designate that will result in a slew of the proper direction and speed, the following equation shall be executed twice, once for each axis:

$$D = D_{t-1} \pm \Delta P$$

where:

D = Designate in shuttle coordinates, a 16-bit Binary Fraction (BF) of 180°

$D_{t-1}$  = The back value of D in degrees

$\Delta P$  = Position delta, which will result in a slew of the correct speed; a 16-bit BF of 180°

$\Delta P$  = (20 deg/sec x  $\Delta t$ ) for fast slew

$\Delta P$  = (0.4 deg/sec x  $\Delta t$ ) for slow slew

$\Delta t$  = 200 ms, the sampling rate

2. The switch inputs shall be processed as follows:

| <b>Switch input</b> | <b>Processing</b>                        |
|---------------------|--|
| Right               | Add delta to azimuth coordinate          |
| Left                | Subtract delta from azimuth coordinate   |
| Up                  | Add delta to elevation coordinate        |
| Down                | Subtract delta from elevation coordinate |

3. The initial value of  $D_{t-1}$  shall be the measured position of the antenna in azimuth/elevation coordinates at the initiation of the slewing process. These coordinates shall be obtained from the MDM serial output buffer, rescaled, and converted to 2's complement as a BF 180°.
4. The required accuracy shall be as follows:
  - a. The delta position between subsequent designates shall reflect a rate equivalent to  $20 \pm 5$  deg/sec in fast slew and  $0.4 \pm 0.2$  deg/sec in slow slew.
  - b. The interpolation computation shall generate designate values for inputting to position loop that shall be equal to the arithmetic mean of the adjacent values to an accuracy of  $\pm 5$  percent.

- B. The above calculations shall be performed in azimuth/elevation coordinates in 2's complement arithmetic scaled to BF 180°.

- C. The pseudo-designates shall then be transformed to alpha/beta coordinates.
- D. The above calculations shall be performed once every 200 ms; however, antenna drive rates shall be output every 100 ms. Therefore, the following interpolation computation shall be executed:
- $$P1 = (P2 - P2B)/2 + P2B$$
- where:
- P1 = The interpolated designate
- P2 = The full value designate from paragraph C
- P2B = The back value of P2
- E. Position loop shall be executed every 100 ms. The first time through position loop in each 200-ms cycle, P1 values shall be used as the coordinates of the designate. The second time through, P2 values shall be used. The outputs from position loop will be the required drive rates.
- F. In addition, once every 100 ms the following functions shall be performed:
1. Read encoder angles into the database.
  2. Execute obscuration routine.
- G. In addition to the foregoing, once every 200 ms the following functions shall be performed:
1. Input discrete data.
  2. Input MDM data if NEWMDM data are indicated.
  3. Output discrete data.
  4. Output LRU serial data.
  5. Input LRU serial data.
  6. Transform encoder position angles from gimbal coordinates to shuttle coordinates.
  7. Output MDM and D and C serial data.
  8. If in MANUAL and no slew switch (UP, DOWN, RIGHT, LEFT) is activated, the dither control flag shall be set false.

#### 10.3.7.4 Input/Output

- A. The input to the slewing function shall be as follows:

1. Slew commands
  - a. Fast
  - b. Slow
  - c. Right
  - d. Left
  - e. Up
  - f. Down

Note: Fast is mutually exclusive with respect to slow. Right is mutually exclusive with respect to left. Up is mutually exclusive with respect to down.

2. Antenna position
  - a. Azimuth
  - b. Elevation

B. The outputs from the slewing function shall be as follows:

1. From calculation in shuttle coordinates - Pseudo-designates in azimuth/elevation
2. From angle transformation calculation - Pseudo-designates in alpha/beta
3. From interpolation calculations - Pseudo-designates in alpha/beta processed for outputting at 100-ms intervals.
4. From position loop/analog output - Rate commands for slewing
  - a.  $\omega\alpha$
  - b.  $\omega\beta$

### **10.3.8 Scan Procedure**

#### **10.3.8.1 Purpose**

The purpose of the scan procedure is to implement the main and miniscans for both radar and comm searches by causing the antenna to move in spiral scan patterns.

#### **10.3.8.2 Conditions for Calling Scan Procedure**

If the system is in a state of control system readiness, this procedure shall be called if one of the following conditions exists:



- A. When in GPC mode in either comm or radar and the antenna is less than  $0.3^\circ$  from the designate, there is no indication of a target detection, there are no NEWMDM data, and the GPC command to initiate scanning is in the true state.
- B. When in GPC mode in either comm or radar and the antenna is less than  $0.3^\circ$  from the designate, there is no indication of a target detection, and scanning is already in process with conditions for terminating scanning not present.
- C. When in AUTO TRACK mode in either comm or radar and the system is not fast slewing, there is no indication of a target detection, and the D&C panel SEARCH switch, to initiate scanning, is in the true state.
- D. When in AUTO TRACK mode in either comm or radar and the system is not fast slewing, there is no indication of a target detection, and scanning is already in process with conditions for terminating scanning not present.
- E. When in GPC or AUTO TRACK mode in radar during scan and target present has caused LATCH to be high, a timeout period shall be implemented. This period shall be nominal 200 ms. During this timeout period, the scan procedure shall continue to be called. At the completion of timeout, the scan procedure shall be called again and the transition to miniscan shall be implemented.
- F. When in GPC or AUTO TRACK mode in comm during scan and COSTAS LOCK has caused LATCH to be high, a timeout period shall be implemented. This period shall be a nominal 200 ms. During this timeout period, the scan procedure shall continue to be called. At the completion of timeout, if COSTAS LOCK is no longer present, the scan procedure shall be called again and the transition to miniscan shall be implemented.

### 10.3.8.3 Functional Requirements

The following functions shall be performed during execution of the scan procedure:

- A. The LOS of the antenna shall be caused to execute a spiral scan pattern about a given scan center. The position of the scan center, magnitude of the conical angular coverage, angular velocity, rate of expansion and contraction of the spiral, and duration of the scan cycle are functions of system parameters and shall be determined in accordance with the specifications and equations defined below.
- B. In general, a scan pattern shall consist of two regions, a variable dwell region and a constant dwell region. Dwell time is defined as the time required for the antenna beam width to traverse a point target. In the variable dwell region, dwell time varies continuously, monotonically decreasing for an expanding spiral. In the constant dwell region, the time required to traverse the target is constant, regardless of where the LOS may be in the spiral pattern. The variable dwell region shall be the inner region of the spiral; that is, the region between the center of the spiral and the half-cone angle value which defines the switch point between

the variable dwell and the constant dwell regions. The constant dwell region shall be the outer region of the spiral pattern.

- C. For radar scans the switchpoint shall be at 9°.
- D. For comm scans the switchpoint shall be at 4°.
- E. For radar scans the spiral shall expand to a maximum half-cone angle, which is a function of range, and then spiral back into the center and stop. This pattern may not be completed if the scan is stopped as a function of other controlling conditions.
- F. The radar scan shall be complete when time =  $60.60 \pm 0.05$  seconds or when the scan has spiraled back to the center.
- G. The comm scan shall spiral out and be complete when the half-cone angle equals 10°, which shall be accomplished in  $145.50 \pm 0.05$  seconds.
- H. It is also required that three miniscans shall be implemented. These scans shall be generated (centered about the point of detection) when a target has been detected during the main scan but a transition to tracking is not implemented as a result of this detection.
  - 1. The comm miniscan shall consist of the variable dwell region of the comm main scan.
  - 2. There shall be two miniscans for radar, both consisting of the variable dwell region of the radar main scan. Miniscan 1 parameters shall be identical to the parameters of the main scan being executed when the detection occurred. Thus, miniscan 1 shall be a function of range.
  - 3. Miniscan 2 shall be independent of range. Its scan frequency (angular velocity) at the switchpoint is specified in Section 10.3.8.3.M.2.
  - 4. Implementation of miniscan 1 or 2 is selected by the EA-2 and indicated by a bit, MINI2, in the serial data from the EA-2 to EA-1.
- I. In GPC mode, range information required for generating radar scan patterns shall be available from the MDM serial input words - estimated radar range. In AUTO TRACK mode, the range shall be defined as belonging to range group 1.
- J. A scan shall be terminated when any one of the following occurs:
  - 1. Steering mode is changed to GPCDES or MANUAL.
  - 2. 60.6 seconds expires in radar scan or 145.5 seconds expires in comm scan.
  - 3. The half-cone angle reaches 10° in comm.
  - 4. Tracking is initiated.
  - 5. A miniscan reaches the end of variable dwell region.

6. A detection occurs in miniscan.
7. In radar mode, the spiral has expanded and contracted back to the center.
8. The radar/comm selection is changed.
9. The LOS enters the obscured region when in radar mode with obscuration override false.
10. The LOS crosses the guard line when in radar mode with obscuration override false and the scan center below the guard line.
11. If system readiness condition ceases to be valid; that is, if one or more of the following occurs:
  - a. COMON and RADON both become false.
  - b. The boom stow discrete is received.
  - c. Transmit scan enable goes false.
  - d. The self-test command is received (radar mode only).
- K. The update rate for all scans shall be 50 ms nominal.
- L. The maximum delay from beta measured to outputting of the commanded rates shall be 10 ms.
- M. Scan equations. The scan pattern shall be generated by two sets of equations. The first set generates the parameters that define a spiral; the second set generates rates in gimbal coordinates to drive the antenna LOS in the spiral pattern defined by the first set of equations.
  1. Calculation of spiral parameters. Every 50 ms the microprocessor shall generate a value of P, the half-cone angle, and a value of  $\theta R$ , the spiral phase angle for each successive position along the spiral path. In general,  $\theta R$  will be larger than  $360^\circ$ . The fundamental relationship is  $P = f \theta R$ .
  2. F (R) table. In radar mode, the variables  $K_1$ ,  $K_2$ , and PN are functions of range. The variables (all 8-bit values) are accessed from the lookup table that follows (Table 10-5).

*Table 10-5. Lookup table*

| Range group | Radar range miles | PN deg | K <sub>1</sub> deg/sec | K <sub>2</sub> deg/sec |
|-------------|-------------------|--------|------------------------|------------------------|
| 1           | 0 - 7.58          | 30.2   | 286.9                  | 44.6                   |
| 2           | 7.58 - 9.26       | 27.4   | 286.9                  | 44.6                   |
| 3           | 9.26 - 10.10      | 24.6   | 286.9                  | 44.6                   |
| 4           | 10.10 - 11.79     | 21.8   | 286.9                  | 44.6                   |
| 5           | 11.79 - 15.16     | 19.7   | 275.6                  | 42.9                   |
| 6           | 15.16 - 25.27     | 16.2   | 205.3                  | 32.7                   |
| 7           | 25.27 - 39.59     | 13.4   | 154.7                  | 23.9                   |
| 8           | 39.59 - 64.86     | 11.3   | 120.9                  | 19.0                   |
| 9           | 64.86 - 144.89    | 8.4    | 87.2                   | -                      |
| 10          | R > 144.89        | 6.3    | 67.5                   | -                      |
| Comm        |                   | 10.0   | 43.1                   | 3.0                    |
| MINI2       |                   | 9.0    | 56.1                   | -                      |

Note: K<sub>2</sub> is not defined for groups 9 and 10 since, for those groups, PN is less than 9°; i.e., the constant dwell region is never reached.

N. Scan input.

The inputs shall be as follows:

1. Estimated range
2.  $\beta_{ENC}$
3. MINI2

**10.3.9 Track Procedure**

**10.3.9.1 Purpose**

The purpose of the track procedure shall be to support the tracking operation with specified data processing functions while the servo system is in the closed loop tracking configuration.

### **10.3.9.2 Conditions for Entering the Track Procedure**

#### **10.3.9.2.1 Radar mode**

When RADON is true, either of the following conditions shall cause the program to enter the track procedure:

- A. System readiness condition true, GPC true, antenna LOS less than  $0.3^\circ$  from the designate, and radar lobing enable true
- B. System readiness condition true, AUTO true, system not fast slewing, and radar lobing enable true

#### **10.3.9.2.2 Comm mode**

When COMON is true and the antenna is scanning, either of the following conditions shall cause the program to enter the track procedure:

- A. System readiness condition true, GPC true, antenna LOS less than  $0.3^\circ$  from the designate, timeout completed, and COSTAS LOCK true
- B. System readiness condition true, AUTO true, system not fast slewing, timeout completed, and COSTAS LOCK true

When COMON is true and the antenna is not scanning, either of the following conditions shall cause the program to enter the track procedure:

- A. System readiness condition true, GPC true, antenna LOS less than  $0.3^\circ$  from the designate, and COSTAS LOCK true
- B. System readiness condition true, AUTO true, system not fast slewing, and COSTAS LOCK true

### **10.3.9.3 Conditions for Maintaining the System in the Track Procedure**

Once the program has entered the track procedure, it shall continue to execute the track procedure as long as the conditions of Section 10.3.9.2 are met, with radar lobing enable or COSTAS LOCK, whichever is applicable, remaining true and with the exception that the position of the antenna LOS with respect to the designate position shall no longer be relevant.

### **10.3.9.4 Conditions for Terminating the Track Procedure**

The track procedure shall be terminated and the system shall enter a break track state when one of the following conditions occurs:

- A. The system readiness status goes from true to false.
- B. Steering mode changes from GPC or AUTO to GPCDES or MANUAL.

- C. Angle track enable or COSTAS LOCK, whichever is applicable, goes from true to false.
- D. In comm mode, a command to perform a handover operation occurs.

#### **10.3.9.5 Functions Performed During the Track Procedure**

- A. Dither shall be on at all times during the track procedure.
- B. Once every 100 ms, the following functions shall be performed:
  - 1. Read encoder angles into the database.
  - 2. Execute obscuration routine.
- C. Once every 100 ms, the following functions shall be performed:
  - 1. Input discrete data.
  - 2. Input MDM data if NEWMDM data are indicated.
  - 3. Output discrete data.
  - 4. Output LRU serial data.
  - 5. Input LRU serial data.
  - 6. Transform encoder position angles from gimbal coordinates to shuttle coordinates.
  - 7. If in radar mode, transform angle track rates from gimbal coordinates to shuttle coordinates, scale and output to rate meter.
  - 8. Output MDM and D and C serial data.

#### **10.3.10 Self-Test Procedure**

##### **10.3.10.1 Purpose**

The purpose of the self-test procedure is to perform a series of specific tests to demonstrate that the system and specifically the EA-1, the EA-2, and the DA units are operational, or in case of a system failure, to output fault isolation indicators to the MDM indicating which LRUs have failed.

##### **10.3.10.2 Conditions for Calling the Self-Test Procedure**

The self-test procedure shall be called when:

The SELF TEST INITIATE command is true, the system is in radar mode, the initialization procedure has been completed, the BOOM STOW command is false, and one of the following two conditions exists:

- A. The boom is in its stowed position or the 30° deploy position, or
- B. The boom is fully deployed with the gimbal encoders initialized, and the LOS has been initialized to the zenith position.

### 10.3.10.3 Functional Requirements

The functional requirements for the self-test procedure are as follows:

- A. Once every 100 ms the following functions shall be performed:
  - 1. The encoder angles shall be read into the database.
  - 2. The obscuration routine shall be executed.
  - 3. The designate angles shall be transformed from shuttle coordinates to gimbal coordinates when required for execution of the position loop routine.
  - 4. The position loop routine shall be executed when positioning of the antenna is required.
- B. Once every 200 ms, the following functions shall be performed in the B phase of the procedure.
  - 1. Discrete data shall be read into the database.
  - 2. MDM data shall be read into the database if NEWMDM data are available.
  - 3. Self-test initialization as specified in Section 10.3.10.E.1 shall be implemented.
  - 4. LRU serial data shall be read into the database.
  - 5. One of the 10 self-test tasks, as defined below, shall be executed. Execution of a specific task shall be performed incrementally and sequentially every B phase until that task has been completed. After completion of any given task, the next task scheduled shall be initiated during the next B phase. Unless self-test is aborted, this process shall continue until task 10 is completed. Thereafter, task 10 shall be re-executed every B phase until the SELF TEST INITIATE command is removed.
- C. Once every 200 ms, the following functions shall be performed in the C phase of that procedure.
  - 1. The encoder angles shall be transformed from gimbal coordinates to shuttle coordinates.
  - 2. The lamp test shall be performed as specified in Section 10.3.10.3.F (10.7).

3. Discrete data shall be output.
  4. LRU data shall be output.
  5. MDM and D and C data shall be output as specified in Section 10.3.10.3.E (1.3).
- D. Self-test shall comprise a self-test executive and 10 software routines that shall be designated "tasks" as follows. A task may include one or more subtasks, which shall be designated "sequences."



| Task number | Task designation                 |
|-------------|----------------------------------|
| 1           | CPU: Deleted                     |
| 2           | PROM self-check test             |
| 3           | EA-2 power form test             |
| 4           | Initialize antenna position test |
| 5           | Antenna servo test               |
| 6           | Transmitter power check test     |
| 7           | Range and range rate test        |
| 8           | Angle track test                 |
| 9           | Radar sensitivity test           |
| 10          | Self-test quiescent state        |

E. Self-test executive

The functional requirements for the self-test executive are

1. Initialization - Upon entering the self-test procedure, the executive shall
  - (1.1) Clear a dedicated work area in RAM
  - (1.2) Set the SELF flag for output to the MDM to indicate that self-test is in progress
  - (1.3) Implement logic to initiate a 10-second idle period which, in general, shall be used to mark time between tasks or subtasks while the resulting outputs from the task or subtask just completed are output to the MDM and D and C. These outputs shall be held constant for the duration of the 10-second period plus the time until the next set of task or subtask outputs is ready for transmission
  - (1.4) Cause the transmitter to be inhibited from transmitting
  - (1.5) Cause the EA-2 to suppress actuating the test target until the test target is required for tasks 7, 8, 9, and 10
  - (1.6) Implement logic to suppress calling the position loop routine until it is required in the antenna positioning tests
  - (1.7) Zero flags timeshared for both task IDs and, ultimately, for final results. These flags are outputs to the MDM; specifically
    - DATEST

- E2TEST
- E1TEST
- SYSTST

2. Pause - The pause routine, when called, shall implement the 10-second idle period defined in Section 10.3.10.3.E(1.3). For the duration of the pause, all tests shall be held in abeyance; however, all other self-test procedure functions, except outputting MDM and D and C data, shall proceed as normal. The pause routine shall also initialize or reinitialize controls as required for the task or subtask that will follow the pause period.

(2.1) Except as noted in Section 10.3.10.3 E.6, there shall be a total of 18 pauses, including the pause following self-test initialization but preceding tasks 1, 2, and 3. The final quiescent static state following task 10 shall not be included in the above count.

(2.2) The 18 pauses shall occur as follows:

| <b>Pause</b> | <b>Shall occur after</b>       |
|--------------|--------------------------------|
| 1            | Initialization of self-test    |
| 2            | Initialization pass for task 4 |
| 3            | Initialization pass for task 5 |
| 4            | Sequence 1 of task 5           |
| 5            | Sequence 2 of task 5           |
| 6            | Initialization pass for task 6 |
| 7            | Sequence 1 of task 6           |
| 8            | Initialization pass for task 7 |
| 9            | Sequence 1 of task 7           |
| 10           | Sequence 2 of task 7           |
| 11           | Initialization pass for task 8 |
| 12           | Sequence 1 of task 8           |
| 13           | Sequence 2 of task 8           |
| 14           | Initialization pass for task 9 |
| 15           | Sequence 1 of task 9           |
| 16           | Sequence 2 of task 9           |
| 17           | Sequence 3 of task 9           |
| 18           | Sequence 4 of task 9           |

3. Task scheduling - The function of the task scheduler routine shall cause the execution of each task over the time period required for that task which, in general, will be on the order of several seconds for each task. After completion of each task, the task scheduler routine shall sequence to the next task. Tasks shall be executed in the order of their task numbers except as specified below. Task scheduler routine shall also implement execution of the pause routine as required.
  - (3.1) Exceptions to sequential scheduling. Under the following conditions, sequential scheduling shall be superseded by the task-to-task transitions as specified for each case below.
    - a. If task 2 fails, self-test shall jump from task 2 to task 10.
    - b. If task 4 fails, self-test shall jump from task 4 to task 7.
    - c. If task 5 fails, self-test shall jump from task 5 to task 7.
    - d. If at any time during fully deployed self-test while executing task 6, 7, 8, or 9 the antenna LOS becomes positioned so that it is pointing into the obscured region, that task shall be aborted at that time and self-test shall jump to task 10 during the next B phase.
    - e. If self-test is being executed with the boom in its stowed position or in the 30° deploy position, the sequencing of tasks shall be 1, 2, 3, 6, 7, 8, 9, and 10. In this case, the only jump condition shall occur from task 2 to task 10 if task 2 has failed.
4. Task IDs - Four-bit task ID codes shall be generated for each task and output to the MDM as part of the output status data as shown in Table 10-6. Tasks 1, 2, and 3 have the same ID codes, and task 10 does not have an ID code, as such.
5. Output status data - During normal self-test, 19 discrete blocks of data shall be output to the MDM, and a separate 19 blocks of data shall be output to the D and C. The contents of each block of data shall be output to the MDM and D and C, respectively, in the C phase preceding the start of each pause period, except that the 19th and final blocks of data shall be output to the MDM and D and C at the completion of the first execution of task 10. At the MDM and the D and C, each block of data will remain unchanged for a period of time corresponding to the time intervals between the start times of successive pause periods. In general, these intervals will be greater than 10 seconds each, because after each 10-second pause period there is test execution time before the start of the next pause period. The only exception to the above, with respect to the static nature of the outputs, is that the signal strength, scan warn, and track signals to the D and C shall dynamically reflect the real-time current status of the respective functions and the latter two

Table 10-6. Self-test data blocks to the MDM

| Test data blk | Data task/seq | Data ID |    |    |     | Ant strg mode ① | Oper on | System status |     |     | Rcvd sig str (V dc) | RF pwr out (W) | Range/rate ② |    |               |    | Angle ①  |          |    | Angle rate |            |    | Time (sec) |
|---------------|---------------|---------|----|----|-----|-----------------|---------|---------------|-----|-----|---------------------|----------------|--------------|----|---------------|----|----------|----------|----|------------|------------|----|------------|
|               |               | E1      | E2 | DA | SYS |                 |         | sch           | det | trk |                     |                | range (ft)   | gd | rate (ft/sec) | gd | az (deg) | el (deg) | gd | az (deg/s) | el (deg/s) | gd |            |
| 1             | -             | 0       | 0  | 0  | 0   | ACT             | ON      | 0             | 0   | 0   | 0.0                 | 0.0            | 2621439      | 0  | 1638.4        | 0  | ACT      | ACT      | 0  | 00.0       | 00.0       | 0  | 000        |
| 2             | 1,2,3         | 0       | 0  | 0  | 1   | ACT             | OFF     | 0             | 0   | 0   | 0.0                 | 0.0            | 2621439      | 0  | 1638.4        | 0  | ACT      | ACT      | 0  | 00.0       | 00.0       | 0  | 15         |
| 3             | 4             | 0       | 1  | 1  | 1   | DES             | OFF     | 0             | 0   | 0   | 0.0                 | 0.0            | 2621439      | 0  | 1638.4        | 0  | 0.0      | 0.0      | 0  | 00.0       | 00.0       | 0  | 25         |
| 4             | 5 1           | 0       | 1  | 0  | 1   | DES             | OFF     | 0             | 0   | 0   | 0.0                 | 0.0            | 2621439      | 0  | 1638.4        | 0  | 0.0      | 30.0     | 0  | 00.0       | 00.0       | 0  | 40         |
| 5             | 5 2           | 0       | 1  | 0  | 1   | DES             | OFF     | 0             | 0   | 0   | 0.0                 | 0.0            | 2621439      | 0  | 1638.4        | 0  | -30.0    | 30.0     | 0  | 00.0       | 00.0       | 0  | 55         |
| 6             | 5 3           | 0       | 1  | 0  | 1   | DES             | OFF     | 0             | 0   | 0   | 0.0                 | ≥20            | 2621439      | 0  | 1638.4        | 0  | 0.0      | 0.0      | 0  | 00.0       | 00.0       | 0  | 70         |
| 7             | 6 1           | 0       | 0  | 1  | 1   | DES             | ON      | 0             | 0   | 0   | 0.0                 | ≥20            | 2621439      | 0  | 1638.4        | 0  | 0.0      | 0.0      | 0  | 00.0       | 00.0       | 0  | 80         |
| 8             | 6 2           | 0       | 0  | 1  | 1   | DES             | ON      | 0             | 0   | 0   | >0.6                | 0.0            | 2621439      | 0  | 1638.4        | 0  | 0.0      | 0.0      | 0  | 00.0       | 00.0       | 0  | 90         |
| 9             | 7 1           | 1       | 0  | 0  | 1   | MAN             | OFF     | 0             | D   | T   | 0.0                 | 0.0            | 5320         | 1  | 0.0           | 1  | 0.0      | 0.0      | 0  | 00.0       | 00.0       | 0  | 100        |
| 10            | 7 2           | 1       | 0  | 0  | 1   | MAN             | OFF     | 0             | 0   | 0   | >0.0                | 0.0            | 0            | 0  | 0.0           | 0  | 0.0      | 0.0      | 0  | 00.0       | 00.0       | 0  | 110        |
| 11            | 7 3           | 1       | 0  | 0  | 1   | MAN             | OFF     | 0             | D   | T   | >0.0                | 0.0            | 10240        | 1  | 0.0           | 1  | 0.0      | 0.0      | 0  | 00.0       | 00.0       | 0  | 120        |
| 12            | 8 1           | 1       | 0  | 1  | 1   | AUT             | OFF     | 0             | D   | 0   | >0.0                | 0.0            | 10240        | 1  | 0.0           | 1  | 0.0      | 0.0      | 1  | 00.0       | 00.0       | 1  | 130        |
| 13            | 8 2           | 1       | 0  | 1  | 1   | AUT             | OFF     | 0             | D   | T   | >0.0                | 0.0            | 10240        | 1  | 0.0           | 1  | 0.0      | 0.0      | 1  | -16.4      | 00.0       | 1  | 140        |
| 14            | 8 3           | 1       | 0  | 1  | 1   | AUT             | OFF     | 0             | D   | 0   | >0.0                | 0.0            | 10240        | 1  | 0.0           | 1  | 0.0      | 0.0      | 1  | -16.4      | -16.4      | 1  | 150        |
| 15            | 9 1           | 1       | 1  | 0  | 1   | GPC             | OFF     | 0             | D   | T   | 0.0                 | 0.0            | 10240        | 1  | 0.0           | 1  | 0.0      | 0.0      | 1  | -16.4      | -16.4      | 1  | 160        |
| 16            | 9 2           | 1       | 1  | 0  | 1   | GPC             | OFF     | 0             | D   | T   | 0.0                 | 0.0            | 10240        | 1  | 0.0           | 1  | 0.0      | 0.0      | 1  | -16.4      | -16.4      | 1  | 170        |
| 17            | 9 3           | 1       | 1  | 0  | 1   | GPC             | OFF     | 0             | D   | T   | 0.0                 | 0.0            | 10240        | 1  | 0.0           | 1  | 0.0      | 0.0      | 1  | -16.4      | -16.4      | 1  | 180        |
| 18            | 9 4           | 1       | 1  | 0  | 1   | GPC             | OFF     | 0             | D   | T   | 0.0                 | 0.0            | 10240        | 1  | 0.0           | 1  | 0.0      | 0.0      | 1  | -16.4      | -16.4      | 1  | 190        |
| 19            | 10 -          | Note ③  |    |    |     | ACT             | OFF     | S             | D   | T   | 0.0                 | 0.0            | 888800       | 1  | 0.0           | 1  | ACT      | ACT      | 0  | 00.0       | 00.0       | 0  | 200        |

Notes: ① ACT = actual antenna steering mode or actual angle.  
 ② PASS = 888,800 ft., FAIL = 333,300 ft.  
 ③ For each LRU a "1" indicates PASS, a "0" FAIL. A "1" in SYS indicates all three LRUs passed.

signals shall be updated and output to the D and C at the rate of five times per second. For that reason, the track lamp at the D and C, for example, will not be in synchronism with the track flag transmitted to the MDM because the latter is output after the completion of a test and held static for at least 10 seconds. Thus, during the 10-second outputting of test data block 8, the D and C track lamp will be on while the track flag to the MDM will not appear as true until test data block 9. The 19th block of outputs as viewed, for example, at the D and C, will remain static until the self-test ON/OFF command is removed through the GPC. The contents of these data blocks shall be as specified Table 10-6 and Table 10-7. It shall be the function of each task, in addition to the test functions performed by each task, to set registers and flags and to fetch variables to cause the output data blocks to conform to these tables.

6. Exceptions for 30° deploy self-test - If self-test is being executed with the boom in its stowed position or in the 30° deploy position, since tasks 4 and 5 will not be executed, pauses 2, 3, 4, and 5 will not occur and test data blocks 3, 4, 5, and 6 will not be output. In this case there will be a total of only 14 pauses and 15 test data blocks, and the values of azimuth and elevation that are output to the MDM and D and C will be random but static. Also, in determining LRU fault isolation, tasks 4 and 5 shall be construed as having passed their respective tasks.

#### F. Self-test tasks

Each task shall perform one or more tests or measurements. Where multiple tests or measurements are involved, the task shall be organized into numbered sequences, sequence 1 being preceded by a task initialization processing cycle that shall be executed during the first 200 ms of the task. This cycle shall then be followed by a 10-second pause, during which time the results from the last performed sequence of the previous task are output. The functional requirements for the individual tests are defined below. As each test passes or fails, a unique test result flag specifically reserved for that test shall be set or reset. The true state of the flag shall correspond to the PASS condition.

1. Task 1: CPU - Task deleted. One 200-ms processing cycle shall be assigned to the program to bypass the call to this task. The executive shall be structured to provide the capability of performing a task 1 if such is redefined in the future.
2. Task 2: PROM self check - Each of the 24 PROM modules shall be provided with an 8-bit checksum that shall be stored in the last byte location of each PROM. The value of the checksum shall be such that when all bytes in the PROM including the checksum are summed, modulo 25610, the total shall equal zero. This test shall sum the contents of all 24 PROMs, processing 1 PROM every 200 ms. After the summing process has been completed for all 24 PROMs, the program shall verify that the aggregate sum is equal to zero,

which shall correspond to the PASS condition. A nonzero sum shall correspond to the fail condition. The test result flag for this test shall be set accordingly.

(2.1) System input data signals required for the execution of this task

None

(2.2) System output control signals required for the execution of this task

Self-test signal enable - True

**Table 10-7. Self-test data blocks to D&C**

| Test data block | Data task/seq | Range ① ② (k ft) | Range rate ② (ft/s) | Angle ② (deg) |       | Sig str ② (V dc) | Talkbacks ② ③ |      |      | Time (sec) |
|-----------------|---------------|------------------|---------------------|---------------|-------|------------------|---------------|------|------|------------|
|                 |               |                  |                     | (deg)         | (deg) |                  | Scan warn     | Srch | Trck |            |
| 1               | -             | 2621.            | 1638.               | ACT           | ACT   | 0.0              | bp            | bp   | bp   | 00         |
| 2               | 1,2,3         | 2621.            | 1638.               | ACT           | ACT   | 0.0              | bp            | bp   | bp   | 15         |
| 3               | 4             | 2621.            | 1638.               | 000.0         | 000.0 | 0.0              | bp            | bp   | bp   | 25         |
| 4               | 5             | 2621.            | 1638.               | 000.0         | 30.0  | 0.0              | bp            | bp   | bp   | 40         |
| 5               | 5             | 2621.            | 1638.               | -30.0         | 30.0  | 0.0              | bp            | bp   | bp   | 55         |
| 6               | 5             | 2621.            | 1638.               | 000.0         | 000.0 | 0.0              | bp            | bp   | bp   | 70         |
| 7               | 6             | 2621.            | 1638.               | 000.0         | 000.0 | 0.0              | bp            | bp   | bp   | 80         |
| 8               | 6             | 2621.            | 1638.               | 000.0         | 000.0 | >0.0             | bp            | bp   | gry  | 90         |
| 9               | 7             | 5.320            | 000.0               | 000.0         | 000.0 | 0.0              | bp            | bp   | bp   | 100        |
| 10              | 7             | 0.000            | 000.0               | 000.0         | 000.0 | >0.0             | bp            | bp   | gry  | 110        |
| 11              | 7             | 3                | 10.24               | 000.0         | 000.0 | >0.0             | bp            | bp   | gry  | 120        |
| 12              | 8             | 1                | 10.24               | 000.0         | 000.0 | >0.0             | bp            | bp   | gry  | 130        |
| 13              | 8             | 2                | 10.24               | 000.0         | 000.0 | >0.0             | bp            | bp   | gry  | 140        |
| 14              | 8             | 3                | 10.24               | 000.0         | 000.0 | >0.0             | bp            | bp   | gry  | 150        |
| 15              | 9             | 1                | 10.24               | 000.0         | 000.0 | >0.0             | bp            | bp   | gry  | 160        |
| 16              | 9             | 2                | 10.24               | 000.0         | 000.0 | >0.0             | bp            | bp   | gry  | 170        |
| 17              | 9             | 3                | 10.24               | 000.0         | 000.0 | >0.0             | bp            | bp   | gry  | 180        |
| 18              | 9             | 4                | 10.24               | 000.0         | 000.0 | >0.0             | bp            | bp   | gry  | 190        |
| 19              | 10            | -                | 888.8               | 000.0         | 000.0 | >0.0             | gry           | gry  | gry  | 200        |

- as:
- ① PASS = 888.8k feet, FAIL = 333.3k feet.
  - ② Range/range rate and angle data are displayed on panel A2; signal strength and talkback data are displayed on panel A1U.
  - ③ Barberpole (bp) = zero state, gray (gry) = set state.

3. Task 3: EA-2 power form test - The state of the operate bit from the EA-2 shall be determined. A true state shall correspond to PASS, the false state to FAIL. The test result flag for this test shall be set accordingly.

(3.1) System input data signals required specifically for the execution of this task

Serial data operate bit from the EA-2

System output control signals required specifically for the execution of this task

Self-test signal enable - True

4. Task 4: Initialize antenna position test - The self-test program shall command the antenna to move to the zenith position while in GPC designate mode. The program shall verify that the servo system positions the antenna to within  $\pm 0.3^\circ$  of the commanded position. The program shall also verify that the zenith is reached in less than 10 seconds. There shall be no test result flag for this test. If this test fails, the task shall be aborted, and self-test shall jump to task 7 as the next task to be executed.
  - (4.1) System input data signals required specifically for the execution of this task
    - Alpha and beta encoder values
  - (4.2) System output control signals required specifically for the execution of this task
    - a. Alpha and beta analog outputs - The servo drive rates,  $\omega_\alpha$  and  $\omega_\beta$
    - b. Dither command (inverted) - DITHR: Shall be output as false
    - c. Self-test signal enable - True
5. Task 5: Antenna servo test - With the system in GPC designate mode, the self-test program shall command the antenna to elevate to an angle of  $+30^\circ$  from the zenith with the azimuth angle held constant at  $0^\circ$ . Then the program shall command the antenna to an azimuth angle of  $-30^\circ$  holding the elevation angle constant at  $+30^\circ$ . The antenna shall then be commanded back to the zenith position. The program shall verify that the servo system positions the antenna to within  $\pm 0.3^\circ$  of the commanded positions and that the commanded positions are reached within the time periods specified below.
  - (5.1) Three test result flags shall be implemented as follows:
    - a. Maximum time flag - If all three of the tests, elevation, azimuth, and return to zenith are each completed in 10 seconds or less, this flag shall be set to indicate PASS. If any one of the three tests is not completed in 10 seconds or less, this flag shall be set to indicate FAIL, the remainder of task 5 aborted, and self-test caused to jump to task 7 as the next task to be executed.
    - b. Elevation time flag - If the elevation test is completed in 7 seconds or less, this flag shall be set to indicate PASS. If the elevation test exceeds 7 seconds, this flag shall be set to indicate FAIL.
    - c. Azimuth time flag - If the azimuth test is completed in 7 seconds or less, this flag shall be set to indicate PASS. If the azimuth test exceeds 7 seconds, this flag shall be set to indicate FAIL.

- (5.2) Task 5 shall consist of an initialization pass and three sequences. The first sequence shall implement the elevation test; the second, the azimuth test; and the third, the return to zenith test.
- (5.3) System input data signals required specifically for the execution of this task.
  - Alpha and beta encoder values
- (5.4) System output control signals required specifically for the execution of this task
  - a. Alpha and beta analog outputs - the servo drive rates,  $\omega\alpha$  and  $\omega\beta$
  - b. Dither command (inverted) - DITHR: Shall be output as false
  - c. Self-test signal enable - True
- 6. Task 6: Transmitter power check test - With the system in GPC designate mode and the antenna pointing toward the zenith, the transmitter shall be activated at full Traveling Wave Tube (TWT) power. This task shall verify that the DA operate bit is true and that the transmit Radio Frequency (RF) power signal is equal to or greater than the minimum threshold. Task 6 shall comprise an initialization pass and two test sequences that shall be implemented as follows:
  - (6.1) Initialization pass
    - a. The following system output control signals shall be implemented during this pass and shall be maintained unchanged throughout the entire task.
      - (1) Wide beam transmit select - False
      - (2) Encoded mode bit 1 - True
      - (3) Encoded mode bit 2 - True
      - (4) Radar active/passive - Set to passive
      - (5) Provide test target - False
      - (6) Acquisition inhibit - False
      - (7) Motor drive on/off - Off
    - b. The following system output control signals shall be implemented during this pass in order to set up conditions for sequence 1.
      - (1) Estimated radar range - Set to 12,000 feet.



- (2) Self-test signal enable - False
- (3) Self-test atten control bit 1 - False
- (4) Self-test atten control bit 2 - False
- c. The following system input flags, data, and voltage levels shall be verified during the pass.
  - None required
- (6.2) Sequence 1 - DA operate bit test
  - a. The following system-generated input flag shall be verified during this sequence, and a test result flag shall be provided specifically for this parameter. This test result flag shall be set to indicate PASS if this parameter is as indicated below.
    - DA operate bit - True
  - b. The following system output control signals and comparator voltage level shall be implemented at the end of this sequence in order to set up conditions for sequence 2.
    - (1) Self-test control bits 1 through 4 set to select transmit RF power signal voltage as the input to the voltage comparator.
    - (2) Transmit RF power threshold = +3.5 V dc. This value shall be output to the alpha DAC.
- (6.3) Sequence 2 - Transmit RF power test
  - a. The following system input voltage level shall be verified during this sequence, and a test result flag shall be provided specifically for this parameter. This test result flag shall be set to indicate PASS if this parameter is as indicated below.
    - Transmit RF power  $\geq$  +7 V dc. The actual input to the program shall be the output flag of the comparator which indicates whether the voltage under test is above or below the specific threshold voltage provided to the comparator from the program.
- 7. Task 7: Range and range rate test - With the system in the MANUAL mode and the servo motors off, tests shall be performed with the test target both on and off and in both the active and passive states. This task shall comprise an initialization pass and three test sequences that shall be implemented as follows.
  - (7.1) Initialization pass

- a. The following system output control signals shall be implemented during this pass and shall be maintained unchanged throughout the entire task.
  - (1) Self-test signal enable - True
  - (2) Self-test atten control bit 1 - False
  - (3) Self-test atten control bit 2 - False
  - (4) Wide beam transmit select - False
  - (5) (2) Encoded mode bit 1 - True
  - (6) Encoded mode bit 2 - False
  - (7) Acquisition Inhibit - False
  - (8) Motor drive on/off - Off
  - (9) Self-test control bits 1 through 4 set to select radar signal strength voltage as the input to the voltage comparator.
- b. The following system output control signals shall be implemented during this pass in order to set up conditions for sequence 1.
  - (1) Estimated radar range - Set to 10,250 feet
  - (2) Radar active/passive - Set to active
  - (3) Provide test target - True
- c. The following system input flags, data, and voltage levels shall be verified during this pass.

None required

(7.2) Sequence 1 - Radar active - Test target present

- a. The following output signals shall be output to the alpha DAC during this sequence in order to verify the signals that are tested by the voltage comparator.
  - (1) Radar signal strength threshold 1 = +0.3 V dc
  - (2) Radar signal strength threshold 2 = +0.9 V dc
- b. The following system-generated input flags, data, and voltage levels shall be verified during this sequence and a separate test result flag shall be provided for each parameter tested. Each

test result flag shall be set to indicate PASS if the state of the parameter tested is as indicated below.

- (1) Track flag - True
- (2) Lobing enable radar - False
- (3) Measured range =  $5320 \pm 500$  ft
- (4) Radar range data good flag - True
- (5) Measured range rate =  $0.0 \pm 0.3$  ft/sec
- (6) Radar range rate data good flag - True
- (7) Radar signal strength  $\geq +0.6$  V dc
- (8) Radar signal strength  $\leq +1.8$  V dc

c. The following system output control signals shall be implemented at the end of this sequence in order to set up conditions for sequence 2.

- (1) Provide test target - False
- (2) Radar active/passive - Set to passive

(7.3) Sequence 2 - Radar passive - No test target

a. The following system-generated input flags shall be verified during this sequence and a separate test result flag shall be provided for each parameter tested. Each test result flag shall be set to indicate PASS if the state of the parameter tested is as indicated below.

- (1) Detect flag - False
- (2) Track flag - False

b. The following system output control signals shall be implemented at the completion of this sequence in order to set up conditions for sequence 3.

- (1) Provide test target - True
- (2) Radar active/passive - Set to passive

(7.4) Sequence 3 - Radar passive - Test target present

- a. The following output signals shall be output to the alpha DAC during this sequence in order to verify the signals that are tested by the voltage comparator.
    - (1) Radar signal strength threshold 1 = +0.0 V dc
    - (2) Radar signal strength threshold 2 = +0.9 V dc
  - b. The following system-generated input flags, data, and voltage levels shall be verified during this sequence and a separate test result flag shall be provided for each parameter tested. Each test result flag shall be set to indicate PASS if the state of the parameter tested is as indicated below.
    - (1) Track flag - True
    - (2) Lobing enable radar - False
    - (3) Measured range = 10,240  $\pm$  500 feet
    - (4) Radar range data good flag - True
    - (5) Measured range rate = 0.0  $\pm$  0.3 ft/sec
    - (6) Radar range rate data good flag - True
    - (7) Radar signal strength > +0.0 V dc
    - (8) Radar signal strength  $\leq$  +1.8 V dc
8. Task 8: Angle track test - With the system in AUTO TRACK mode, the servo motors off, and the test target on, tests shall be performed to determine if the range, range rate, angle, and angle rate good flags are true and if the delta alpha and delta beta error signals are within prescribed tolerances. This task shall comprise an initialization pass and three test sequences that shall be implemented as follows:
- (8.1) Initialization pass

The following system output control signals shall be implemented during this pass and shall be maintained unchanged through the entire task.

    - (1) Self-test signal enable - True
    - (2) Self-test atten control bit 1 - False
    - (3) Self-test atten control bit 2 - False
    - (4) Wide beam transmit select - False

- (5) Encoded mode bit 1 - False
  - (6) Encoded mode bit 2 - False
  - (7) Radar active/passive - Set to passive
  - (8) Provide test target - True
  - (9) Acquisition inhibit - False
  - (10) Estimated radar range - Set to 10,250 feet
- (8.2) Sequence 1 - Flags test
- a. The following system-generated input flags shall be verified during this sequence and a separate test result flag shall be provided for each parameter tested. Each test result flag shall be set to indicate PASS if the state of the parameter tested is as indicated below.
    - (1) Radar range data good flag - True
    - (2) Radar range rate data good flag - True
  - b. The following system output control signals shall be implemented at the end of this sequence in order to set up conditions for sequence 2.
  - c. Self-test control bits 1 through 4 set to select the delta alpha error signal as the test input to the voltage comparator.
- (8.3) Sequence 2 - Delta alpha error test
- a. The following output signals shall be output to the alpha DAC during this sequence in order to verify the signal that is to be tested by the voltage comparator.
    - (1) Alpha error threshold 1 = +0.705 V dc
    - (2) Alpha error threshold 2 = -0.705 V dc
  - b. The following system-generated input voltage level shall be verified during this sequence, and a separate test result flag shall be provided for each of the two tests. Each test result flag shall be set to indicate PASS if the state of the parameter tested is as indicated below.
    - (1) Delta alpha error voltage  $\leq$  +5.0 V dc
    - (2) Delta alpha error voltage  $\geq$  -5.0 V dc

- c. This sequence shall indicate a PASS condition for delta alpha error by outputting azimuth rate as all 1s to the MDM if both test result flags have been set to PASS.
- d. The following system output control signals shall be implemented at the end of this sequence in order to set up conditions for sequence 3.

Self-test control bits 1 through 4 set to configuration to select delta beta error signal as the input to the voltage comparator.

(8.4) Sequence 3 - Delta beta error test

- a. The following output signals shall be output to the alpha DAC during this sequence in order to verify the signal that is to be tested by the voltage comparator.
  - (1) Beta error threshold 1 = +0.705 V dc
  - (2) Beta error threshold 2 = -0.705 V dc
- b. The following system-generated input voltage level and control flag shall be verified during this sequence, and a separate test result flag shall be provided for each of the three tests. Each test result flag shall be set to indicate PASS if the state of the parameter tested is as indicated below.
  - (1) Delta beta error voltage  $\leq$  +5.0 V dc
  - (2) Delta beta error voltage  $\geq$  -5.0 V dc
  - (3) Lobing enable radar - True
- c. This sequence shall indicate a PASS condition for delta beta error by outputting elevation rate as all 1s to the MDM if both test result flags associated with the delta beta error have been set to PASS.

9. Task 9: Radar sensitivity test - With the system in GPC mode, the servo motors off, and the test target on, tests shall be performed to determine that the track flag is true, that the radar signal strength is within a prescribed tolerance, that the measured range and measured range rate values are within tolerance, and that the delta alpha and delta beta error signals are within prescribed limits. This test shall comprise an initialization pass and four test sequences which shall be implemented as follows:

(9.1) Initialization pass

- a. The following system output control signals shall be implemented during this pass and shall be maintained unchanged throughout the entire task.
  - (1) Self-test signal enable - True
  - (2) Wide beam transmit select - False
  - (3) Encoded mode bit 1 - False
  - (4) Encoded mode bit 2 - True
  - (5) Radar active/passive - Set to passive
  - (6) Provide test target - True
  - (7) Acquisition inhibit - False
  - (8) Estimated radar range - Set to 10,250 feet
- b. The following system output control signals shall be implemented as shown below in order to set up conditions for sequence 1.
  - (1) Self-test atten control bit 1 - False
  - (2) Self-test atten control bit 2 - False

(9.2) Sequence 1 - Track flag test

- a. The following system-generated input flag shall be verified during this sequence, and a test result flag shall be provided specifically for this parameter. This test result flag shall be set to indicate PASS if the state of the parameter tested is as indicated below.

Track flag - True

- b. The following system output control signals shall be implemented at the end of this sequence in order to set up conditions for sequence 2.
  - (1) Self-test atten control bit 1 - False
  - (2) Self-test atten control bit 2 - True
  - (3) Self-test control bits 1 through 4 set to configuration to select radar signal strength voltage as the test input to the voltage comparator

(9.3) Sequence 2 - Radar signal strength test

- a. The following signals shall be output to the alpha DAC during this sequence in order to verify the signals which are to be tested by the voltage comparator.
  - (1) Radar signal strength threshold 3 = -0.07 V dc
  - (2) Radar signal strength threshold 4 = +0.25 V dc
- b. The following system-generated input voltage levels shall be verified during this sequence, and a separate test result flag shall be provided for each of the two tests. Each test result flag shall be set to indicate PASS if the state of the parameter tested is as indicated below.
  - (1) Radar signal strength > -0.14 V dc
  - (2) Radar signal strength < +0.50 V dc
- c. The following system output control signals shall be implemented at the end of this sequence in order to set up conditions for sequence 3.
  - (1) Self-test atten control bit 1 - True
  - (2) Self-test atten control bit 2 - False
  - (3) Self-test control bits 1 through 4 set to select the delta alpha error signal as the test input to the voltage comparator

(9.4) Sequence 3 - Delta alpha error test

- a. The following output signals shall be output to the alpha DAC during this sequence in order to verify the signal which is to be tested by the voltage comparator.
  - (1) Alpha error threshold 1 = +0.705 V dc
  - (2) Alpha error threshold 2 = -0.705 V dc
- b. The following system-generated input voltage levels shall be verified during this sequence, and a separate test result flag shall be provided for each of the two tests. Each test result flag shall be set to indicate PASS if the state of the parameter tested is as indicated below.
  - (1) Delta alpha error voltage  $\leq$  +5.0 V dc
  - (2) Delta alpha error voltage  $\geq$  -5.0 V dc



- c. The following system output control signals shall be implemented at the end of this sequence in order to set up conditions for sequence 4.
  - (1) Self-test atten control bit 1 - False
  - (2) Self-test atten control bit 2 - False
  - (3) Self-test control bits 1 through 4 set to select the delta beta error signal as the test input to the voltage comparator

(9.5) Sequence 4 - Delta beta error test

- a. The following signals shall be output to the alpha DAC during this sequence in order to verify the signal which is to be tested by the voltage comparator.
  - (1) Beta error threshold 1 = +0.705 V dc
  - (2) Beta error threshold 2 = -0.705 V dc
- b. The following system-generated input voltage level and data values shall be verified during this sequence, and a separate test result flag shall be provided for each of the four tests. Each test result flag shall be set to indicate PASS if the state of the parameter tested is as indicated below.
  - (1) Delta beta error voltage  $\leq +5.0$  V dc
  - (2) Delta beta error voltage  $\geq -5.0$  V dc
  - (3) Measured range =  $10,240 \pm 500$  feet
  - (4) Measured range rate =  $0.0 \pm 0.3$  feet/second

(9.6) At the completion of sequence 4, a 10-second pause shall be implemented before task 10 begins.

10. Task 10: Self-test quiescent state - With the system configured in MANUAL mode with the test target on, the program shall evaluate the internally generated test result flags and then shall indicate the results by appropriately setting the four self-test flags in MDM status word 2. In each bit position, a "1" shall indicate PASS, and a "0" shall indicate FAIL.

(10.1) For task 10, the following output control signals shall be implemented and maintained unchanged throughout the entire task.

- (1) Self-test signal enable - True
- (2) Self-test atten control bit 1 - True

- (3) Self-test atten control bit 2 - False
  - (4) Wide beam transmit select - False
  - (5) Encoded mode bit 1 - True
  - (6) Encoded mode bit 2 - False
  - (7) Radar active/passive - Set to passive
  - (8) Provide test target - True
  - (9) Acquisition inhibit - False
  - (10) Estimated radar range - Set to 10,250 feet
- (10.2) Task 10 shall indicate a failure for the EA-1 LRU if any of the following conditions are true.
- a. In task 2, the PROM self-check test failed.
  - b. In task 5, any of the following occurred:
    - (1) Antenna elevation test failed.
    - (2) Antenna azimuth test failed.
    - (3) Maximum time to perform entire task was exceeded.
  - c. In task 7, for either the active or passive tests, the following conditions occurred:
    - (1) The track flag was true and
    - (2) The range data was within tolerance and
    - (3) The range rate data was within tolerance and
    - (4) The test result flags for the radar signal strength test indicate FAIL
- (10.3) Task 10 shall indicate a failure for the EA-2 LRU if any of the following conditions are true.
- a. In task 3 the EA-2 power from test failed.
  - b. In task 7, for either the active or passive test, any of the following occurred:
    - (1) The track flag was false.
    - (2) The range data was out of tolerance.

- (3) The range rate data was out of tolerance.
  - c. In task 7, for the test target off-test, either of the following occurred:
    - (1) The detect flag was true.
    - (2) The track flag was true.
  - d. In task 8, any of the following occurred:
    - (1) The lobing enable radar flag was false.
    - (2) The delta alpha error was out of tolerance.
    - (3) The delta beta error was out of tolerance.
  - e. In task 9, any of the following occurred:
    - (1) The track flag was false.
    - (2) The delta alpha error was out of tolerance.
    - (3) The delta beta error was out of tolerance.
- (10.4) Task 10 shall indicate a failure for the DA LRU if any of the following conditions are true.
- a. In task 6, either of the following occurred:
    - (1) The DA operate bit was false.
    - (2) The transmit RF power signal voltage was less than the specified minimum.
  - b. In task 7, either of the following occurred:
    - (1) The active radar signal strength voltage was less than the specified maximum, and the passive radar signal strength voltage was less than the specified minimum.
    - (2) The active radar signal strength voltage was greater than the specified maximum, and the passive radar signal strength voltage was greater than the specified minimum.
  - c. In task 7, for either the active or passive tests, the following occurred:
    - (1) The track flag was false and
    - (2) The range data was within tolerance and

- (3) The range rate data was within tolerance and
- (4) The radar signal strength voltage was out of tolerance
- (10.5) If and only if all three LRU fault indication bits in MDM status word 2 are set to "1" shall the radar system test status bit be set to "1," indicating that the system has passed self-test.
- (10.6) As shown in Table 10-4 and Table 10-5 for test data block 19, range values shall be output to the MDM and D and C as follows:
  - a. 888,800 feet for self-test PASS
  - b. 333,300 feet for self-test FAIL
- (10.7) Upon the completion of task 10, a lamp test shall be executed. This test shall cause the EA-1 to continuously output a 28-V dc signal to the search, track, and scan warning talkbacks on D and C panel A1U. These lamps shall remain gray so long as the self-test ON/OFF bit from the MDM is maintained in the "1" state.

## 10.4 PROCEDURE SUPPORTING FUNCTIONS

### 10.4.1 Math Functions

This section contains routines that perform static math calculations and form a math foundation to support calculations in the dynamics sections. These functions are as follows:

- G. Angle transformation
- H. Angle rate transformation
- I. Sine/cosine
- J. Secant
- K. Arcsine

### 10.4.1.1 Angle Transformation Function

#### 10.4.1.1.1 Purpose

The angle transformation function shall perform coordinate transformations between the two coordinate systems for all angle values transmitted from the shuttle to EA-1 and from EA-1 to the shuttle. The antenna coordinate system is a right orthogonal system (as is the orbiter) using two gimbals arranged so that the outer (alpha) gimbal carries the inner (beta) gimbal. The alpha axis is rotated +67° in yaw from the orbiter +X axis in the XY plane. The beta axis is perpendicular to it. The origin of the alpha/beta coordinate system is considered the same as the orbiter; i.e., alpha = 0° and beta = 0° when the antenna LOS is along the orbiter -Z axis. Positive alpha motion is toward the right wing, and positive beta motion is toward the payload bay. The origin of the azimuth/elevation coordinate system is the same as the orbiter, and azimuth = 0° and elevation = 0° are along the orbiter -Z axis. Positive azimuth motion is toward the left wing, and positive elevation motion is toward the nose of the orbiter.

#### 10.4.1.1.2 Functional Requirements

There shall be three types of transformations as follows:

A. Shuttle designates to gimbal designates

Shuttle designates are provided in sign magnitude via serial data from the MDM. These angles shall be transformed and stored as 2's complement gimbal designates.

B. Measured gimbal angles to shuttle angles

The measured angles are read from the gimbal encoders. They are periodically transformed to shuttle angles with the proper scaling factors for the MDM and display and control interface.

C. Internal shuttle designates to gimbal designates

Pseudo shuttle designates shall be generated in the microprocessor based on slew commands from the shuttle. The slew commands are: up, down, right, left, fast, and slow. The pseudo designates shall be generated in 2's complement, transformed, and stored as the gimbal designates. This procedure shall enable the microprocessor to command slewing motions referenced to the shuttle coordinate system.

#### 10.4.1.1.3 Equations

The equations for the angle transformations function shall be as follows:

A.  $A = \arcsine [(-\cos Y \cdot \sin D \cdot \cos C + K \cdot \sin C) \sec B]$

$$B = \arcsine (-\cos Y \cdot \sin C - K \cdot \sin D \cdot \cos C)$$

- B. The direction of the transformation and associated operators shall be in accordance with Table 10-7.

**Table 10-8. Angle transform parameters**

| Identifier | Shuttle/gimbal | Gimbal/shuttle |
|------------|----------------|----------------|
| A          | Alpha          | Azimuth        |
| B          | Beta           | Elevation      |
| C          | Elevation      | Beta           |
| D          | Azimuth        | Alpha          |
| K          | - Sin 67°      | Sin 67°        |

- C. Variables in both coordinate systems are bounded by

$$-180^\circ \leq A \leq 180^\circ$$

$$-90^\circ \leq B \leq 90^\circ$$

However, since the arcsine function as implemented is limited to

$$-90^\circ \leq \arcsine \leq 90^\circ$$

it is necessary to determine which quadrant A is in, as follows:

1. Define a discriminant Z where  $Z = \text{sign of } (\cos C \cdot \cos D)$ .
2. Define  $A_q$  where  $A_q = A$  corrected for the proper quadrant.
3. The correction is as follows:

If Z is positive, then  $A_q = A$

If Z is negative and A is negative, then  $A_q = -180^\circ - A$

If Z is negative and A is positive, then  $A_q = 180^\circ - A$

### 10.4.1.2 Angle Rate Transformation Function

#### 10.4.1.2.1 Purpose

The angle rate transformation function shall perform transformation of LOS angle track rates from the gimbal coordinate system to the orbiter coordinate system. The results shall be scaled and output to the MDM and D and C as an analog voltage.

#### 10.4.1.2.2 Functional requirements

This function shall be used only in radar mode.

#### 10.4.1.2.3 Equations

Equations for the angle rate transformation function shall be as follows:

$$\omega_A = \omega_\alpha (-\cos Y \cdot \cos \beta + \sin Y \cdot \sin \alpha \cdot \sin \beta) + \omega_\beta (\sin Y \cdot \cos \alpha)$$

$$\omega_E = \omega_\alpha (\sin Y \cdot \cos \beta + \cos Y \cdot \sin \alpha \cdot \sin \beta) - \omega_\beta (\cos Y \cdot \cos \alpha)$$

$\omega_A$  = Orbiter azimuth LOS angle rate

$\omega_E$  = Orbiter elevation LOS angle rate

$\omega_\alpha$  = Alpha LOS angle rate

$\omega_\beta$  = Beta LOS angle rate

$\alpha$  = Alpha gimbal angle

$\beta$  = Beta gimbal angle

$Y$  = Offset angle of the deployed assembly from the +X axis in the yaw plane = 67°

### 10.4.1.3 Sine/Cosine Function

#### 10.4.1.3.1 Purpose

The sine/cosine function shall calculate the sine or cosine of an angle.

#### 10.4.1.3.2 Functional requirements

A. This function shall calculate

$$X = \sin(\text{angle}) \text{ or } X = \cos(\text{angle})$$

B. Implementation of this function shall be by means of a lookup table with linear interpolation.



#### 10.4.1.4 Secant Function

##### 10.4.1.4.1 Purpose

The secant function shall calculate the secant of an angle.

##### 10.4.1.4.2 Functional requirements

A. This function shall calculate

$$X = \sec(\text{angle})$$

B. Implementation of this function shall be by means of a lookup table with linear interpolation.

C. The secant as implemented is limited to a value of 16. This limits the range of angles.

$$-86.4^\circ \leq \text{angle} \leq 86.4^\circ$$

#### 10.4.1.5 Arcsine Function

##### 10.4.1.5.1 Purpose

The arcsine function shall calculate the angle which has a sine equal to a number X.

##### 10.4.1.5.2 Functional requirements

A. This function shall calculate

$$\text{angle} = \arcsine X$$

B. Implementation of this function shall be by means of a lookup table with linear interpolation.

C. This function shall be defined only for the range

$$-90^\circ \leq \text{angle} \leq 90^\circ$$

#### 10.4.2 Position Loop Routine

##### 10.4.2.1 Purpose

The purpose of the position loop routine shall be to dynamically calculate in real time the gimbal drive rates required as inputs to the servo loop to drive the antenna in the specified manner from its instantaneous current position to the designate position. This routine shall also determine when the designate has been reached. In addition, this function shall determine whether the system shall be inertially or body stabilized.

### 10.4.2.2 Functional Requirements

- A. This routine shall calculate output rates  $\omega\alpha$  and  $\omega\beta$  in accordance with the equations defined below.
- B. The range of possible motion in the beta axis, which is determined by physical constraints, is limited to:  $-85^\circ \leq \beta \leq +75^\circ$ .
- C. The range of motion in the alpha axis is defined to be  $-206^\circ \leq \alpha \leq +154^\circ$ ; however, since the physical stops may be driven a degree or so in either direction, the position of the antenna on the alpha axis may be slightly more negative than  $-206^\circ$  or slightly more positive than  $+154^\circ$ . This situation, however, can occur only in slew mode. Thus, when in slew mode, if either of these conditions should occur, the position loop function shall output an alpha rate of  $10^\circ$  per second times cosine  $\beta$  in the direction to unwrap the alpha gimbal. This rate shall be maintained until alpha is again in the range  $-206^\circ \leq \alpha \leq +154^\circ$ . Once alpha is in that range, whiparound of the antenna shall occur so that the LOS of the antenna shall rotate rapidly in the reverse direction on the alpha axis to intercept that point in space that continued rotation in the original direction would mathematically reach if the operator had continued activation of the slew switches during cable unwrap and whiparound. Once that point is reached, rotation in the original direction shall be resumed, and slewing shall continue as if there had been no interruption. On the other hand, if the operator discontinues activation of the slew switches at some point after the start of cable unwrap and whiparound, the whiparound motion shall continue to that point and the system shall become body stabilized at that point if in MANUAL or inertially stabilized if in AUTO. As a consequence of paragraph D below, the rate of rotation during whiparound is a function of whether or not the slew switches are activated during the whiparound. If they are, the rate will be  $56.25 \text{ deg/sec}$  times cosine  $\beta$ . If they are not activated, the rate will be  $20 \text{ deg/sec}$  times cosine  $\beta$ . Thus, the rate can actually change during whiparound.
- D. The outputs from this function shall be limited at all times to a maximum value of  $20 \text{ deg/sec}$  except when executing the slew procedure with at least one of the slew switches (UP, DOWN, RIGHT, LEFT) activated, in which case the limit shall be  $56.25 \text{ deg/sec}$ . In the case of  $\omega\alpha$ , the limitation shall be applied before the  $\cos \beta$  correction.
- E. When the position delta is less than  $3^\circ$  in both axes simultaneously, the outer zone flag (ZONEO) shall be set.
- F. When the position delta is less than  $0.3^\circ$  in both axes simultaneously, the inner zone flag (ZONEI) shall be set to indicate that the designate has been reached.

- G. This function shall also command the system to either initiate inertial stabilization or to maintain body referenced stabilization according to the following conditions:
1. The system shall be inertially stabilized if
    - a.  $GPC \cdot ZONEI \cdot \overline{BOOM}$  or
    - b.  $GPCDES \cdot ZONEI \cdot \overline{GPCIS} \cdot \overline{BOOM}$  or
    - c.  $AUTO \cdot \overline{SLEWING} \cdot (ZONEI \cdot \overline{BOOM} + INSTAB)$
  2. Under all other conditions, the system shall be maintained in the body referenced mode.
- H. If the system is determined to have satisfied the conditions for inertial stabilization, zeros shall be output to the rate DACs unless one or more of the following conditions exist, in which case this routine shall continue to calculate and output drive rates to drive the antenna toward the designate.
1. There is an indication of NEWMDM data.
  2. The antenna is being slewed.
- I. This routine shall set dither true if the routine is being executed under the point procedure.
- J. The position loop routine shall implement the positioning function of and be callable by the following procedures:
1. Point procedure
  2. Slew procedure
  3. Deploy procedure
  4. Self-test procedure

### 10.4.3 Obscuration Function

#### 10.4.3.1 Purpose

The purpose of the obscuration function shall be to perform computations necessary to set the scan warn flag true when the LOS is in the obscured region (provided that certain other conditions are true as defined below) and to prevent the TWT from transmitting when the antenna LOS is in the obscured region or may be in the obscured region.

### 10.4.3.2 Functional Requirements

- A. The obscuration function shall be accounted for in all 10 procedures.
- B. All calculations shall be performed in gimbal coordinates.
- C. The orbiter obscuration profile is specified in azimuth and elevation coordinates in Table 10-8.
- D. The curve defined in Table 10-8 shall be converted to the alpha-beta coordinate system for the right side of the orbiter. This curve shall then be graphed as a planar curve with alpha and beta as the abscissa and ordinate, respectively. This curve shall be designated as alpha-beta curve 1. The actual obscuration profile curve to be stored in tabular form in memory shall be a curve generated in the alpha-beta plane  $3^\circ$  in the positive direction from curve 1. This curve shall be designated alpha-beta curve 2. Positive is defined as the direction away from the obscured region, which region is defined as the region above curve 1.
- E. A transition zone shall be defined so that
  - 1. In the region of the payload bay, which is represented by azimuth-elevation curve segments 5, 6, 7, and 8, this zone shall extend from curve 1 to a curve defined by curve 1 +  $5^\circ$ .
  - 2. In all other regions, this zone shall extend from a curve defined by curve 1 -  $1^\circ$  to a curve defined by curve 1 +  $5^\circ$ .
  - 3. The transition zone shall include the boundary lines that define the transition zone.
- F. The scan warn flag (SCWARN) shall meet the following functional requirements:
  - 1. When the antenna is pointing to a position on the negative side of the transition zone, SCWARN shall be true.
  - 2. When the antenna is pointing to a position on the positive side of the transition zone, SCWARN shall be false.
  - 3. When the antenna is pointing to a position within the transition zone, SCWARN may be true or false.
  - 4. When it is not possible for the program to determine where the antenna is pointing, specifically during initialization, or if the MIPS have not been found, SCWARN shall be false.
  - 5. When the program is executing self-test in the  $30^\circ$  deployed or in the stowed position, SCWARN shall be false.
  - 6. Except when executing powerup or the initialize procedure, the program shall determine what state SCWARN shall be set to during the A phase of every

procedure; that is, this determination shall be made at a nominal rate of once every 100 ms.

**Table 10-9. Obscuration zone polynomial parameters**

$$\text{Azimuth} = \sum_{i=0-4} a_i (\text{Elevation})^i \text{ in degrees}$$

| Curve no. | Elevation (deg) | a <sub>0</sub> | a <sub>1</sub> | a <sub>2</sub> | a <sub>3</sub> | a <sub>4</sub> |
|-----------|-----------------|----------------|----------------|----------------|----------------|----------------|
| 1         | -1 <EI< 3       | -113.25        | -22.25         | 0              | 0              | 0              |
| 2         | -58<EI<-1       | -91.1          | -0.105         | 0              | 0              | 0              |
| 3         | -85<EI<-58      | -125.8         | -0.703         | 0              | 0              | 0              |
| 4         | -85<EI<-80      | 1039.0         | 13.0           | 0              | 0              | 0              |
| 5         | -80<EI<-64      | 99.0           | 1.25           | 0              | 0              | 0              |
| 6         | -66<EI<-64      | -864.2         | -13.8          | 0              | 0              | 0              |
| 7         | -66<EI<-23      | 58.392         | -0.2782        | -5.28E-3       | 0              | 0              |
| 8         | -23<EI<-19      | 21.75          | -1.75          | 0              | 0              | 0              |
| 9         | -19<EI<24       | 55.0           | 0              | 0              | 0              | 0              |
| 10        | 24<EI<70        | 49.7936        | 0.301218       | -8.59E-3       | 2.085E-4       | 0              |
| 11        | 100<AZ<140      | EI = 70        |                |                |                |                |
| 12        | 50<EI<70        | -11005.08      | 757.88         | -19.1928       | 0.215179       | -9.02E-4       |
| 13        | 0<EI<50         | 175.0          | -0.22          | 0              | 0              | 0              |
| 14        | 175<EI<180      | 0              |                |                |                |                |

- G. The obscuration profile as stored in PROMS shall be divided into two zones, the fine zone and the coarse zone.
  - 1. The fine zone shall be defined by curve segments 5, 6, 7, and 8.
  - 2. The coarse zone shall be defined by curve segments 1, 2, 3, 4, 9, 10, 11, 12, 13, and 14.
  
- H. The profile values stored shall be alpha values as a function of beta. The current value of beta measured at any given time shall serve as an index into the tables. The alpha values shall represent the ends of line segments which are horizontal to the alpha axis and terminate at the points where these lines intersect the obscuration profile. Seven regions for the obscuration profile shall be implemented as follows:

| Region | Beta measured                                | Alpha line segments represent | No. of alpha line segments |
|--------|--|-------------------------------|----------------------------|
| 1      | $61.523^\circ \leq \beta$                    | Obscured region               | 0                          |
| 2      | $19.512^\circ \leq \beta \leq 61.523^\circ$  | Unobscured region             | 1                          |
| 3      | $1.406^\circ \leq \beta \leq 19.512^\circ$   | Unobscured region             | 1                          |
| 4      | $-5.625^\circ \leq \beta \leq 1.406^\circ$   | Unobscured region             | 2                          |
| 5      | $-12.65^\circ \leq \beta \leq -5.625^\circ$  | Obscured region               | 2                          |
| 6      | $-68.90^\circ \leq \beta \leq -12.656^\circ$ | Obscured region               | 1                          |
| 7      | $\beta \leq -68.906^\circ$                   | Unobscured region             | 0                          |

An individual table of alpha values shall be provided for each of the following regions: 2, 3, 4, 5, and 6.

- I. In order to meet the performance specified in paragraphs E and F, the following implementation shall be effected:
  1. In the fine zone,  $19.512^\circ \leq \beta \leq 61.523^\circ$ , the granularity of a  $\beta$  used in indexing the obscuration table shall be  $0.17578125^\circ$ .
  2. For the remaining tables, which correspond to the coarse zone, the granularity of the  $\beta$ -table index shall be  $1.406250$ .
  3. In the fine zone,  $19.512^\circ \leq \beta \leq 61.523^\circ$ , the granularity of  $\alpha$  stored in the table shall be  $0.08789063^\circ$ .
  4. For the remaining tables, the granularity of  $\alpha$  stored shall be  $1.40625^\circ$ .
- J. Independent of setting or resetting SCWARN, the program shall cause the transmitter to be inhibited under certain specific conditions.
  1. In this connection, a prediction of antenna position shall be made, when required, for that point in time which will occur nominally 100 ms after the current position is measured. Equations for the predicted position are
    - a. Predicted =  $\alpha$  current +  $\omega\alpha \cdot \Delta t$  where  $\Delta t = 100$  ms
    - b. Predicted =  $\beta$  current +  $\omega\beta \cdot \Delta t$
  2. The predicted position shall be calculated under the following conditions:
    - a. When SCWARN is true and the system is in the point or scan procedure and not being inertially stabilized
    - b. When SCWARN is false and the system is in the slow mode of the slew procedure and not being inertially stabilized

3. When the predicted position is calculated, a determination shall be made as to whether or not the predicted position lies in the obscured region as follows:

The predicted position shall be defined as being in the obscured region if it lies in or on the negative side of curve 2.

K. Then the transmitter shall be controlled as follows:

1. If TWTOFF is true, EA-1 shall send out the command to inhibit the transmitter regardless of any other conditions. As a consequence of this requirement, if TWTOFF is true, self-test tasks 6, 7, 8, and 9 will fail because the execution of these tasks requires the use of the transmitter control signals.
2. If TWTOFF is false and OBOVER is true, EA-1 shall send out the command to enable the transmitter regardless of any other conditions, except that when self-test is being executed, OBOVER shall have no effect.
3. Neither TWTOFF nor OBOVER shall have any effect on SCWARN.
4. If TWTOFF and OBOVER are both false, the transmitter shall be inhibited for any one of the following conditions:
  - a. MIPS not found.
  - b. System in INIT, IDLE, DEPLOY, or RECOVER.
  - c. Antenna fast slewing.
  - d. Less than 1 second has elapsed since fast slewing ceased.
  - e. Antenna slow slewing with the LOS more than  $3^\circ$  from the pseudo-designate.
  - f. System in radar SLEW while antenna is slow slewing with the LOS equal to or less than  $3^\circ$  from the pseudo-designate and either SCWARN2 is true or the predicted position is in the obscured region, or both.
  - g. System in POINT with the LOS more than  $3^\circ$  from the designate.
  - h. System in radar POINT with the LOS equal to or less than  $3^\circ$  from the designate, both SCWARN is true, and the predicted position is in the obscured region.
  - i. System in radar SCAN with both SCWARN true, and the predicted position is in the obscured region.
  - j. System in radar SCAN, the scan center designate below the guard line and the LOS having crossed the guard line into the protected zone. The guard line is the line defined by the following points:  $\alpha = 0^\circ$ ,  $\beta = 55^\circ$ , and

$\alpha = 60^\circ$ ,  $\beta = 26^\circ$ . The protected zone is the region between the guard line and curve 2.

- k. System in radar TRACK with SCWARN true.
  - l. System in radar PTERM with SCWARN true.
  - m. System in radar self-test with SCWARN true.
5. With system in COMM, if TWTOFF and OBOVER are both false and the measured beta angle is greater than the beta guard angle, then the transmitter shall be inhibited for any one of the following conditions:
- a. System in SLEW while antenna is slow slewing with the LOS equal to or less than  $3^\circ$  from the pseudo-designate and either SCWARN is true or the predicted position is in the obscured region or both.
  - b. System in POINT with the LOS equal to or less than  $3^\circ$  from the designate and both SCWARN is true and the predicted position is in the obscured region.
  - c. System in SCAN with both SCWARN true, and the predicted position is in the obscured region.
  - d. System in TRACK with SCWARN true.
  - e. System in PTERM with SCWARN true.
  - f. Extended payload control (EPC) is true.
6. With system in COMM, if TWTOFF and OBOVER are both false and conditions in 4.a to 4.d are all false and the measured beta angle is equal to or less than the beta guard angle, the transmitter shall be enabled for any one of the following conditions:
- a. System in TRACK
  - b. System in POINT with the LOS equal to or less than  $3^\circ$  from the designate
  - c. System in SLEW with the LOS equal to or less than  $3^\circ$  from the pseudo-designate
  - d. System in SCAN
  - e. System in PTERM



- L. The following SCAN requirements shall also be met as part of the obscuration function:
1. All radar scans shall be aborted at that point in time that the transmitter is commanded to be inhibited except when the command to inhibit is caused by TWTOFF. Comm scans shall not be aborted as part of the obscuration function.
  2. Radar scans, the scan centers which lie in or on the negative side of curve 2, shall not be initiated. This is in contrast to comm scans, which shall be initiated and performed regardless of where the scan centers may be. When conditions in 10.4.3.2 K. 5 and 6 are met, the transmitter shall be inhibited or enabled as the LOS moves into the obscured region or into the unobscured region, respectively. In the transition zone, the transmitter may be inhibited or enabled.
  3. Radar scans, the scan center designates which lie in the protected zone, shall be performed with range group 10 parameters.
- M. In self-test during the execution of tasks 6, 7, 8, and 9, if SCWARN goes true, self-test shall be aborted and the program shall jump to task 10.
- N. When it is determined that the transmitter is to be inhibited, the following bits in parallel output word 5 shall be set:
- |                                 |       |
|---------------------------------|-------|
| TWTA INHIBIT/SIGNAL ENABLE      | Bit 1 |
| SELF TEST ATTENUATION CONTROL 1 | Bit 2 |
| SELF TEST ATTENUATION CONTROL 2 | Bit 3 |
- O. When it is determined that the transmitter is not to be inhibited, the above 3 bits shall be reset with the exception that when in PTERM or self-test, the above 3 bits shall not be reset as a part of the obscuration function.
- P. Immediately after the setting or resetting of the above bits in parallel output word 5, this word shall be output to the DA.

#### 10.4.4 Data Control Functions

This section specifies input/output requirements. The data are comprised of input and output words which consist of both parallel and serial data. The parallel data are also referred to as discrete data and subdivided into synchronous and nonsynchronous data. The synchronous data are input and output once per sample time (once every 200-ms period). The nonsynchronous data may be input or output at any time in the program; in general, it is data that are required to be as current as possible.

The data control functions are defined for the following:

- A. Setting of signal status flags
- B. Discrete inputs
- C. Discrete outputs
- D. LRU serial data inputs
- E. LRU serial data outputs
- F. MDM serial data inputs
- G. MDM and D and C serial data outputs
- H. Nonsynchronous discrete inputs and outputs

#### **10.4.4.1 Set Signal Status Function**

##### **10.4.4.1.1 Purpose**

The purpose of the set signal status function shall be to periodically set or reset certain control bits and flags which are to be output to the EA-2, SPA, MDM, or control circuits within the EA-1 itself.

##### **10.4.4.1.2 Timing constraints**

This function shall be performed immediately before execution of

- A. Output discrete data
- B. Output MDM serial data

##### **10.4.4.1.3 Required logic**

The control bits and flags specified below shall be set under the conditions defined by the following equations:

- A.  $RADCOM(1) = \overline{COMON} \cdot \overline{COMSTB} \cdot (RADON + RADSTB)$
- B.  $DETECT(1) = RADON \cdot RDETCT + COMON \cdot COASTA$
- C.  $DATAP(1) = \overline{RADCOM} \cdot DATAD$
- D.  $SIGNAL(1) = COMON \cdot COASTA \cdot (GPCDES + MANUAL + TRKING \cdot (GPC + AUTO))$
- E.  $TRACK(1) = RADON \cdot RTRACK + COMON \cdot SIGNAL$

- F.  $ACQINH(1) = (GPCDES + GPC) \cdot \overline{ZONEI} \cdot \overline{SELF} + (MANUAL + AUTO) \cdot FSTSLW$
- G.  $TDEAST(1) = EAST$
- H.  $TDWEST(1) = WEST$
- I.  $COMLB(1) = COMON \cdot (GPC + AUTO)$
- J.  $WBTXSL(1) = COMON \cdot (GPC + AUTO) \cdot \overline{SIGNAL} \cdot PRIACQ$
- K.  $RLSTAT(1) = RADON \cdot (GPC + AUTO)$
- L.  $SRGINH(1) = FINCRS + \overline{MOTON}$

#### 10.4.4.2 Discrete Inputs Function

##### 10.4.4.2.1 Purpose

The discrete inputs function shall implement inputting of synchronous discrete data into the database.

##### 10.4.4.2.2 Functional requirements

- A. The processor shall initiate, control, and terminate inputting of discrete data.
- B. Each time this function is executed, 5 bytes of synchronous discrete data shall be strobed into the microprocessor and stored as parallel input words in RAM.
- C. This function shall be performed at the rate of five times per second.

##### 10.4.4.2.3 Input format

The format of the discrete input data shall be as follows:

###### A. Parallel input word 1

- |           |                      |
|-----------|----------------------|
| 1. MANUAL | Manual slew select   |
| 2. AUTO   | Auto track select    |
| 3. GPCDES | GPC designate select |
| 4. GPC    | GPC select           |
| 5. RADACT | Radar active         |
| 6. NEWMDM | New MDM data         |

7. \*

8. \*

B. Parallel input word 2

- |           |                                |
|-----------|--------------------------------|
| 1. SIMAN  | Search initiate                |
| 2. COASTA | Costas lock                    |
| 3. DATAD  | Data detect                    |
| 4. RLBEN  | Radar lobing enable (neg true) |
| 5. *      |                                |
| 6. LATCH  | Latched target hit             |
| 7. OPER   | Operate                        |
| 8. *      |                                |

C. Parallel input word 3

- |          |                      |
|----------|----------------------|
| 1. *     |                      |
| 2. SKEY  | Side key             |
| 3. SLOW  | Slew rate slow       |
| 4. FAST  | Slew rate fast       |
| 5. DOWN  | Elevate down select  |
| 6. UP    | Elevate up select    |
| 7. LEFT  | Azimuth left select  |
| 8. RIGHT | Azimuth right select |

D. Parallel input word 4

- |           |               |
|-----------|---------------|
| 1. RADON  | Radar on      |
| 2. RADSTB | Radar standby |
| 3. NEWA   | New alpha MIP |
| 4. COMON  | Comm on       |
| 5. COMSTB | Comm standby  |



A. Parallel output word 1

1. ACQENA = ACQEN                      Acquisition enable
2. LINEAR = RADON •  $\overline{\text{RADACT}}$       Linear polarization
3. \*
4. \*
5. \*
6. PSON                                      Power supply on
7. \*
8. \*

B. Parallel output word 2

1. SEARCH = SCANNG                      System in program scan
2. \*
3. TRACKO = TRACK                      Comm or radar track
4. SSPEC =  $\overline{\text{SPREAD}}$                       Spread spectrum on
5. WBTXS = WBTXSL                      Widebeam transmit select
6. COMRAD =  $\overline{\text{RADCOM}}$                       Comm/radar
7. JAMENA = ACQEN                      D/A jam enable
8. RSTAT = RLSTAT                      Radar lobing static state

C. Parallel output word 3

1. BOOMST = LOCKED                      Boom stow enable 1
2. \*
3. UNLOCK                                      Stow motor unlock/lock
4. STOWM                                      Stow motor on/off
5. \*
6. SWARN = SCWARN                      Obscuration flag

- 7. \*
  - 8. COMLB =  $\overline{\text{COMLB}}$                       Comm lobing (neg true)
- D. Parallel output word 4
- 1. PTRACK = PNTTRK                      Point/track servo
  - 2. \*
  - 3. \*
  - 4. \*
  - 5. \*
  - 6. \*
  - 7. MOTON                                  Servo motor drive on/off
  - 8. \*
- E. Parallel output word 5
- 1. SIGEN                                  TWTA inhibit/self-test signal enable
  - 2. ATTEN1                                Self-test attenuation control 1
  - 3. ATTEN2                                Self-test attenuation control 2
  - 4. STCON1                                Self-test control bit 1
  
  - 5. STCON2                                Self-test control bit 2
  - 6. STCON3                                Self-test control bit 3
  - 7. STCON4                                Self-test control bit 4
  - 8. \*
- F. Parallel output word 6
- 1. \*
  - 2. SRGINH                                Surge inhibit command
  - 3. DITHR = DITHER                      Dither command out (neg true)
  - 4. X4GNOT                                Complement of MS gain bit

- |           |                           |
|-----------|---------------------------|
| 5. X2G    | Middle gain bit           |
| 6. X1GNOT | Complement of LS gain bit |
| 7. FINCRS | Fine/coarse gyro          |
| 8. HILO   | High/low bandwidth        |

#### 10.4.4.4 LRU Serial Data Input Function

##### 10.4.4.4.1 Purpose

The LRU serial data input function shall implement inputting of serial data from EA-2 when in radar mode and from the SPA when in comm mode.

##### 10.4.4.4.2 Functional requirements

- A. The processor shall initiate, control, and terminate inputting of serial data.
- B. It shall interrogate the appropriate LRU at the rate of five times per second.
- C. When in radar mode, 11 bytes of serial data from EA-2 shall be input and stored in the database.
- D. When in comm mode, 1 byte of serial data from the SPA shall be input and stored in the database.
- E. When in radar mode, the SPA serial input area of the data base shall be zeroed; and when in comm mode, the EA-2 serial input area of the database shall be zeroed.

##### 10.4.4.4.3 Input formats

###### 10.4.4.4.3.1 Input from the EA-2

The data content of the LRU serial data input bytes from EA-2 is specified as follows:

- |          |  |
|----------|--|
| A. IRAD1 | Radar status   |
| B. IRAD2 | Radar status   |
| C. IRAD3 | Measured range MSB no sign;<br>MS bit = 1,310,720 ft |
| D. IRAD4 | Measured range MID bits                              |
| E. IRAD5 | Measured range LSB                                   |
| F. IRAD6 | Measured range rate MSB                              |



- G. IRAD7 BF 1,638.4 ft/sec  
Measured range rate LSB
- H. IRAD8 Measured alpha angle rate MSB  
BF 1.18 deg/sec
- I. IRAD9 Measured alpha angle rate LSB
- J. IRAD10 Measured beta angle rate MSB  
BF 1.18 deg/sec
- K. IRAD11 Measured beta angle rate LSB

The bits of the radar status words shall be formatted as follows:

- A. IRAD1
  - 1. ARGOOD Radar angle rate data good
  - 2. AGOOD Radar angle data good
  - 3. \*
  - 4. \*
  - 5. \*
  - 6. ROPER Operate
  - 7. RGOOD Radar range data good
  - 8. RRGOOD Radar range rate data good
- B. IRAD2
  - 1. MINI 2 Miniscan 2
  - 2. SLOBE Sidelobe
  - 3. RDETCT Radar detect flag
  - 4. RTRACK Radar track flag
  - 5. \*
  - 6. \*
  - 7. \*
  - 8. \*



- C. ORAD3 Estimated radar range MSB no sign bit MS bit = 1,310,720 feet
- D. ORAD4 Estimated radar range MID
- E. ORAD5 Estimated radar range least significant two bits positioned in the two most significant bits of the word. The lower four bits of this word contain the four most significant bits of the beta guard angle.

**10.4.4.5.3.1 EA-2 status word bits**

EA-2 status word bits shall be formatted as follows:

A. Status word 1

- 1. \*
- 2. MODEBI Encoded mode bit 1
- 3. MODEB2 Encoded mode bit 2
- 4. ACQINH Acquisition inhibit
- 5. RFTSB Radar threshold VAR/FIX
- 6. MAIN Main scan
- 7. MINI Miniscan
- 8. TARGET Test target activate

B. The encoded mode bits shall be encoded as follows:

| Encoded mode bit 1 | Encoded mode bit 2 |        |
|--------------------|--------------------|--------|
| 0                  | 0                  | AUTO   |
| 0                  | 1                  | GPC    |
| 1                  | 0                  | MANUAL |
| 1                  | 1                  | GPCDES |

C. The MAIN and MINI flags shall be configured as follows:

| MAIN | MINI |               |
|------|------|---------------|
| 0    | 0    | <u>SCANNG</u> |



- 7. MODC1 Modulation control 1
- 8. MODC2 Modulation control 2
- B. SPA status word 2
  - 1. MODEB1 Encoded mode bit 1
  - 2. MODEB2 Encoded mode bit 2
  - 3. FWDLNK Forward link mode 2/1
  - 4. DATAP Data present
  - 5. SIGNAL Signal present
  - 6. PRIACQ Primary acquisition mode off/on
  - 7. 0
  - 8. 1

#### **10.4.4.6 MDM Serial Data Input Function**

##### **10.4.4.6.1 Purpose**

The MDM serial data input function shall implement input of serial data from the MDM.

##### **10.4.4.6.2 Functional requirements**

- A. The processor shall initiate, control, and terminate inputting of MDM serial data into the database.
- B. It shall interrogate the MDM whenever the NEWMDM data flag in the discrete input data is true. This flag shall be checked at the rate of five times per second. In general, new MDM data will be available only once every 2 seconds.
- C. Each time this function is performed, 10 bytes of data from the MDM shall be transferred into the processor and stored in the database.

##### **10.4.4.6.3 Input words from the MDM**

The input words from the MDM shall be as follows:

- A. IMDM1 Status
- B. IMDM2 Status
- C. IMDM3 Azimuth angle designate MSB BF 360°

- D. IMDM4 Azimuth angle designate LSB
- E. IMDM5 Elevation angle designate MSB BF 180°
- F. IMDM6 Elevation angle designate LSB
- G. IMDM7 Radar range estimate MSB no sign;  
MS bit = 1,310,720 ft
- H. IMDM8 Radar range estimate MID
- I. IMDM9 Radar range estimate least significant two bits  
positioned in the two most significant bits of the  
word. Beta guard angle most significant four bits  
positioned in the four least significant bits. BF  
180°
- J. IMDM10 Beta guard angle LSB

The individual bits of the MDM status words shall be formatted as follows:

A. IMDM1

- 1. SIGPC Search initiate GPC
- 2. EAST TDRS east select
- 3. WEST TDRS west select
- 4. SPREAD Spread spectrum off/on
- 5. KUBA KU B/A select
- 6. STEST Self-test on/off
- 7. MODC1 Modulation control 1
- 8. MODC2 Modulation control 2

B. 1MDM2

- 1. PRIACQ Primary acquisition mode off/on
- 2. GPCIS GPCDES inert stab on/off
- 3. FWDLNK Forward link mode 1/2
- 4. RFTSB Radar threshold FIX/VAR
- 5. OBOVER Obscuration INTLK override
- 6. TWTOFF TWTA off

- 7. EPC Extended payload control on/off
- 8. \*

#### **10.4.4.7 MDM and D and C Serial Data Output Function**

##### **10.4.4.7.1 Purpose**

The MDM serial data output function shall implement formatting and outputting of serial data to the MDM for both the MDM and the D and C.

##### **10.4.4.7.2 Functional requirements**

- A. The processor shall initiate, control, and terminate outputting of MDM and D and C serial data.
- B. Each time this function is performed, 20 bytes of MDM data and 12 bytes of D and C data shall be accessed or derived from other data as necessary, formatted and output to the MDM as two separate blocks of data.
- C. Formatting of the D and C data shall include the insertion of parameter IDs for the four variables output for the D and C, as indicated in paragraph 10.4.4.7.3.2.
- D. This function shall be performed at the rate of five times per second except during self-test when outputting to the MDM shall be performed approximately once every 10 seconds. At the conclusion of self-test, after the final results of self-test have been transmitted to the MDM, no further outputs shall be provided to the MDM until the self-test command is removed.

##### **10.4.4.7.3 Output to MDM**

The sequencing of the serial data words to the MDM shall be as defined in the following paragraphs.

##### **10.4.4.7.3.1 MDM output words**

All numerical quantities output to the MDM shall be sign magnitude (with the exception of measured radar range). Output words for the MDM shall be as follows:

- A. OMDM1 Status word 1
- B. OMDM2 Status word 2
- C. OMDM3 Status word 3
- D. OMDM4 Status word 4

|    |        |   |
|----|--------|---|
| E. | OMDM5  | Measured azimuth angle MSB BF 360°, but parameter is actually limited to $\pm 180^\circ$  |
| F. | OMDM6  | Measured azimuth angle LSB  |
| G. | OMDM7  | Measured elevation angle MSB BF 180°, but parameter is actually limited to $\pm 90^\circ$ |
| H. | OMDM8  | Measured elevation angle LSB  |
| I. | OMDM9  | Measured radar range rate MSB BF 1638.4 ft/sec  |
| J. | OMDM10 | Measured radar range rate LSB   |
| K. | *      |   |
| L. | *      |   |
| M. | OMDM13 | Measured radar range MSB<br>no sign; MS bit=1,310,720 ft                                  |
| N. | OMDM14 | Measured radar range MID  |
| O. | OMDM15 | Measured radar range MID  |
| P. | OMDM16 | Measured radar range LSB  |
| Q. | OMDM17 | Measured radar azimuth angle rate MSB BF 16.384 deg/sec                                   |
| R. | OMDM18 | Measured radar azimuth angle rate LSB   |
| S. | OMDM19 | Measured radar elevation angle rate MSB BF 16.384 deg/sec                                 |
| T. | OMDM20 | Measured radar elevation angle rate LSB   |

The bits of the MDM status words shall be formatted as follows:

|    |       |                             |
|----|-------|-----------------------------|
| A. | OMDM1 |                             |
|    | 1.    | RADCOM Radar/comm           |
|    | 2.    | AUTO Auto track select      |
|    | 3.    | GPCDES GPC designate select |
|    | 4.    | GPCACQ GPC select           |
|    | 5.    | *                           |



- 6. \*
- 7. \*
- 8. AGOOD Radar angle data good
- B. OMDM2
  - 1. ARGOOD Radar angle rate data good
  - 2. SELF Self-test
  - 3. KUBA KU B/A select
  - 4. RFTSB Radar threshold FIX/VAR
  - 5. OBOVER Obscuration INTLK override
  - 6. \*
  - 7. \*
  - 8. \*
- C. OMDM3
  - 1. SCANNG Scanning
  - 2. DETECT Detect
  - 3. TRACK Track
  - 4. OPER DA operate
  - 5. E1TEST EA-1 radar test status
  - 6. DATEST DA radar test status
  - 7. E2TEST EA-2 radar test status
  - 8. SYSTEST System test status
- D. OMDM4
  - 1. TDWEST TDRS west (latched)
  - 2. TDEAST TDRS east (latched)
  - 3. \*
  - 4. FSYNC Forward link data frame sync

- |    |        |                            |
|----|--------|----------------------------|
| 5. | DATAP  | Data present               |
| 6. | SCWARN | Scan warn limit            |
| 7. | RGOOD  | Radar range data good      |
| 8. | RRGOOD | Radar range rate data good |

**10.4.4.7.3.2 D and C output words**

All parameters output to the D and C shall be sign magnitude (except radar range). The output words for the D and C shall be as follows:

- |    |       |  |
|----|-------|--|
| A. | ODC1  | Measured azimuth angle MSB<br>BF 204.8°                            |
| B. | ODC2  | Measured azimuth angle MID   |
| C. | ODC3  | Measured azimuth angle LSB   |
| D. | ODC4  | Measured elevation angle MSB<br>BF 102.4°                          |
| E. | ODC5  | Measured elevation angle MID                                       |
| F. | ODC6  | Measured elevation angle LSB                                       |
| G. | ODC7  | Radar range rate MSB<br>BF 1638.4 ft/sec                           |
| H. | ODC8  | Radar range rate MID   |
| I. | ODC9  | Radar range rate LSB (the six least significant bits shall be 0's) |
| J. | ODC10 | Radar range MSB no sign;<br>MSB = 1,310,720 ft                     |
| K. | ODC11 | Radar range MID  |
| L. | ODC12 | Radar range LSB  |

The parameter IDs for the D and C shall be the most significant three bits of the MSB of each parameter as specified below. The numerical values of the data shall be right-shifted three bits for each parameter to accommodate the IDs.

| ID  | Parameter                |
|-----|--------------------------|
| 001 | Measured azimuth angle   |
| 010 | Measured elevation angle |
| 011 | Radar range rate         |
| 100 | Radar range              |

#### 10.4.4.8 Nonsynchronous Data Input/Output Functions

##### 10.4.4.8.1 Purpose

This section specifies the requirements for processing the following nonsynchronous parameters.

- A. Alpha and beta encoder inputs
- B. Alpha loop gain compensation outputs
- C. High/low bandwidth selection output
- D. Fine/coarse gyro selection output
- E. Analog voltage outputs
- F. Dither control output

##### 10.4.4.8.2 Functional requirements

- A. The inputting, processing, formatting, and storing of  $\alpha$  and  $\beta$  encoder values and the generation, formatting, and outputting of the three alpha gain bits, high/low bandwidth control bit, and fine/coarse gyro control bit, all as specified below, shall be implemented in one routine (ENCODER) that shall be called and executed in all procedures except INITIALIZATION and RECOVER.
- B. The alpha loop gain compensation code, high/low bandwidth selection bit, and fine/coarse gyro selection bit shall be formatted as discrete outputs in parallel output word 6 as specified in paragraph 10.4.4.3.3.F.
- C. A separate routine shall be provided for outputting analog voltage outputs.

##### 10.4.4.8.2.1 Alpha and beta encoder inputs

The alpha encoder angle is provided to EA-1 as a 2's complement BF 360° and shall be stored as such in the database. It shall also be scaled to a BF 180° and stored with that scaling in the database. The beta encoder angle is provided to EA-1 as a 2's complement BF 180° and shall be stored as such in the database.

- A.  $\alpha$  ENC actual      Alpha axis encoder input; BF 360° stored as 16 bits with sign plus 12 bits of significance
- B.  $\alpha$  ENC              Alpha axis encoder input; BF 180° stored as 16 bits with sign plus 11 bits of significance
- C.  $\beta$  ENC                Beta axis encoder input; BF 180° stored as 16 bits with sign plus 11 bits of significance

**10.4.4.8.2.2 Alpha loop gain compensation outputs**

The alpha gain compensation for the rate stabilization loop shall be implemented as a three-bit code, and shall have eight discrete values that are determined as a function of the MSB of the beta angle as indicated below:

| Beta angle                              |                                       | Alpha gain<br>(db) | 3-bit<br>code |
|---|---------------------------------------|--------------------|---------------|
| Negative                                | Positive                              |                    |               |
| $-27^\circ \leq \beta \leq +35^\circ$   |                                       | 1.684              | 101           |
| $-42^\circ \leq \beta \leq -27^\circ$   | $35^\circ \leq \beta \leq 47.5^\circ$ | 5.206              | 100           |
| $-53^\circ \leq \beta \leq -42^\circ$   | $47.5^\circ \leq \beta \leq 58^\circ$ | 8.701              | 111           |
| $-65^\circ \leq \beta \leq -53^\circ$   | $58^\circ \leq \beta \leq 68^\circ$   | 12.22              | 110           |
| $-73.5^\circ \leq \beta \leq -65^\circ$ | $68^\circ \leq \beta$                 | 15.69              | 001           |
| $-79^\circ \leq \beta \leq -73.5^\circ$ | NA                                    | 19.22              | 000           |
| $-82.5^\circ \leq \beta \leq -79^\circ$ | NA                                    | 22.71              | 011           |
| $R \leq -82.5^\circ$                    | NA                                    | 26.23              | 010           |

**10.4.4.8.2.3 High/low bandwidth - fine/coarse gyro selection**

- A. One discrete control bit shall be generated and output to indicate the program's selection of high or low bandwidth.
- B. One discrete control bit shall be generated and output to indicate the program's selection of fine or coarse gyro.
- C. The state of the two control bits specified above shall be determined according to the following table:

| Procedure                             | Bandwidth     | Gyro          |
|---------------------------------------|---------------|---------------|
| POINT                                 | Low           | Coarse        |
| SLEW                                  | Low           | Coarse        |
| TRACK                                 | Low           | Fine          |
| COMM SCAN                             | Low           | Fine          |
| RADAR SCAN $\beta \leq 30^\circ$      | High          | Coarse        |
| RADAR SCAN $\beta > 30^\circ$         | Low           | Coarse        |
| DEPLOY                                | Low           | Coarse        |
| IDLE                                  | Low           | Coarse        |
| SELF TEST                             | Low           | Coarse        |
| INITIALIZATION                        | Low           | Coarse        |
| RECOVER                               | Not specified | Not specified |
| TERMINATION<br>going into radar track | Low           | Fine          |

TERMINATION  
all other cases

Same as in previous  
procedure

Same as in previous  
procedure

- D. In RADAR SCAN at the beginning of the procedure, the bandwidth control bit shall be set high or low depending upon the absolute magnitude of  $\beta$ . In the case where it is initially set high, if subsequently the absolute magnitude of  $A$  should exceed  $30^\circ$ , the bandwidth control bit shall be set low at that point in time and remain low for the remainder of the scan.

#### 10.4.4.8.2.4 Analog voltage outputs

- A. The analog voltage outputs (in binary form), which serve as inputs to the digital to analog converters (DACs), shall consist of:
1. Commanded servo rates
  2. LOS angle tracking rates
  3. Self-test threshold values ( $\alpha$  DAC only)
- B. These three outputs shall be mutually exclusive. The actual values to be output shall be computed and scaled by other routines and stored in the database to serve as inputs to this routine when it is called. The function of this routine is to convert these values from 2's complement to sign magnitude and output them to the respective DACs. The sign magnitude numbers which are output to the DACs shall have the following sign convention:
1. For alpha values the sign bit shall be 1 for positive numbers.
  2. For beta values the sign bit shall be 0 for positive numbers.
  3. The outputs shall be as follows:
 

|    |                |   |
|----|----------------|---|
| a. | $\omega\alpha$ | Alpha axis commanded drive rate (16 bits)<br>Coarse gyro - sign magnitude (BF 56.25 deg/sec)<br>Fine gyro - sign magnitude (BF 11.25 deg/sec) |
| b. | $\omega\beta$  | Beta axis commanded drive rate (16 bits)<br>Coarse gyro - sign magnitude (BF 56.25 deg/sec)<br>Fine gyro - sign magnitude (BF 11.25 deg/sec)  |
| c. | $\omega E$     | Elevation axis LOS angle tracking rate (16 bits)<br>Sign magnitude BF 20 mr/sec. Output via alpha DAC   |
| d. | $\omega A$     | Azimuth axis LOS angle tracking rate (16 bits)<br>Sign magnitude BF 20 mr/sec. Output via beta DAC  |
| e. | Thresholds     | Sign magnitude BF 10.0 V  |

#### 10.4.4.8.2.5 Dither control

- A. One discrete control bit shall be generated and output to command dither on or off.
- B. For the following procedures, DITHER shall be commanded ON:
  - 1. DEPLOY
  - 2. POINT
  - 3. SLOW SLEW
  - 4. COMM SCAN
  - 5. TRACK
  - 6. SELF TEST (tasks 4 and 5 only)
- C. For the following procedures, DITHER shall be commanded OFF:
  - 1. INITIALIZATION
  - 2. IDLE
  - 3. RECOVER
  - 4. FAST SLEW
  - 5. RADAR SCAN
  - 6. SELF TEST (all tasks except 4 and 5)
- D. For the following procedure, DITHER shall be neither commanded ON nor commanded OFF:

PROCEDURE TERMINATION

#### 10.5 REFERENCES

- A. HS237-4479A Electronic Assembly No. 1, Flight Software, Release XII Software Requirements Specification, August 1984, Hughes Aircraft Co.
- B. HS237-4488A Electronic Assembly No. 1, Flight Software, Release XII Software Description Document, August 1984, Hughes Aircraft Co.
- C. HS237-4455A Electronic Assembly No. 1, Flight Software, Release XII Flow Charts, August 1984, Hughes Aircraft Co.

THIS PAGE INTENTIONALLY BLANK

## SECTION 11 - GROUND COMMAND INTERFACE LOGIC CONTROLLER

| Section | Page   |
|---------|--|
| 11.1    | GENERAL ..... 11-1   |
| 11.2    | COMMAND DATA FLOW ..... 11-1                                     |
| 11.3    | DESCRIPTION OF THE SYSTEM ..... 11-1                             |
| 11.3.1  | Power Supply Subsystem ..... 11-2                                |
| 11.3.2  | MDM Data Buffer Cards ..... 11-3                                 |
| 11.3.3  | Decoder/Driver Cards ..... 11-6                                  |
| 11.4    | INSTALLATION ..... 11-12   |
| 11.4.1  | Location ..... 11-12   |
| 11.4.2  | Cooling ..... 11-12  |
| 11.5    | CREW CONTROLS ..... 11-13  |
| 11.5.1  | Power ..... 11-13  |
| 11.5.2  | Mode Control Switches ..... 11-13                                |
| 11.5.3  | Crew SPEC Control ..... 11-13                                    |
| 11.6    | TELEMETRY ..... 11-13  |
| 11.7    | OPERATIONAL PROCEDURES ..... 11-14                               |
| 11.7.1  | GCIL Powerup Sequence ..... 11-14                                |
| 11.7.2  | GCIL-Only Commands ..... 11-15                                   |
| 11.7.3  | Ground Command, GCIL, Controller, and LRU Interfaces ..... 11-16 |
| 11.8    | OPERATION INSTRUCTIONS ..... 11-17                               |
| 11.9    | REFERENCES ..... 11-18   |

### TABLES

| Table |  | Page  |
|-------|--|-------|
| 11-1  | DSM command names and descriptions ..... 11-15   | 11-15 |
| 11-2  | Column titles and descriptions ..... 11-17   | 11-17 |
| 11-3  | GCIL functions, drivers, and CMD numbers with telemetry, supply<br>voltage sources, ground commands, and DSM numbers ..... 11-19 | 11-19 |

### FIGURES

| Figure |   | Page  |
|--------|---|-------|
| 11-1   | Functional diagram of the power supply cards ..... 11-2 | 11-2  |
| 11-2   | Ku fail-safe logic ..... 11-4                           | 11-4  |
| 11-3   | Functional flow for the decoders ..... 11-8             | 11-8  |
| 11-4   | Hybrid driver ..... 11-9                                | 11-9  |
| 11-5   | Example of the GCIL driver drawing symbol ..... 11-11   | 11-11 |



THIS PAGE INTENTIONALLY BLANK

## SECTION 11 GROUND COMMAND INTERFACE LOGIC CONTROLLER

### 11.1 GENERAL

The Ground Command Interface Logic (GCIL) controller provides the capability of controlling selected subsystem functions in either PANEL or COMMAND mode. In PANEL mode, given subsystems are under control of the manual Displays and Controls (D&C) panel switches; in COMMAND mode, these subsystems are controlled by uplinked ground commands or by commands entered via orbiter keyboards. There are five PANEL/COMMAND mode switches to control given functions of the following subsystems: S-band Phase Modulation (PM), S-band Frequency Modulation (FM), TV, Ku-band, and payload.

The GCIL will accept a maximum rate of one command word every 150  $\mu$ sec. Two command words are required per Real-Time Command (RTC), an ALL ZERO command word and a DATA command word. Each data word must be preceded by an ALL ZERO word.

The GCIL logic duplicates the functions of the D&C switches. Multiposition switch functions are implemented by the GCIL Programmable Read-Only Memory (PROM) decoding scheme. Multiple drivers may be turned ON or OFF with a single RTC.

### 11.2 COMMAND DATA FLOW

The GCIL receives command data from the payload MDM, decodes the command data, then outputs the function to the proper Line Replaceable Units (LRUs). Command data from MDM PF1 are routed to MDM data buffer A, while Command data from MDM PF2 are routed to MDM data buffer B.

### 11.3 DESCRIPTION OF THE SYSTEM

The GCIL is made up of multiple specialized cards in one LRU. They interface with external systems including power, D&C switch panels, communications equipment and payload MDMs.

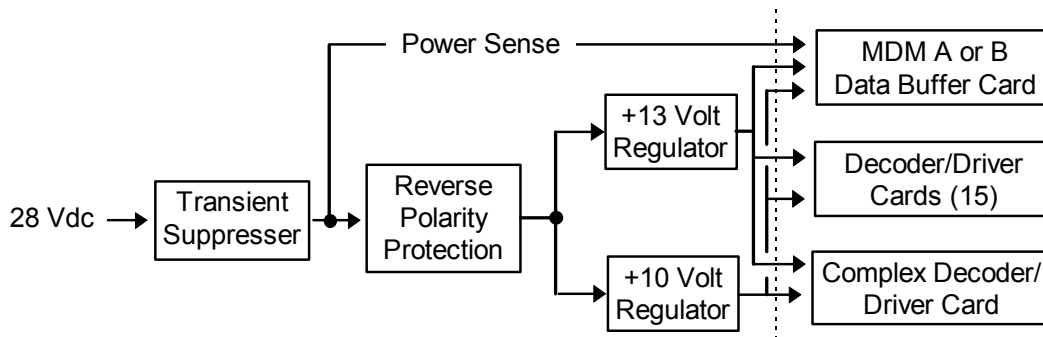
The cards internal to the LRU are

- Two power supply cards
- Two MDM data buffer cards
- 15 decoder/driver cards
- One complex decoder/driver card.

Each of these subsystems (cards) is discussed in the following text

### 11.3.1 Power Supply Subsystem

The GCIL has two cards that are used to regulate the power that is needed by the various cards in the LRU. The two power supply cards are each powered by 28 V dc, consuming 60 watts maximum. The two power supply cards provide redundant power to all the GCIL decoder and driver cards. Card A19 is powered from the main A bus via a 3-amp Circuit Breaker (CB) on panel R14. A20 is powered from the main C power bus via another 3-amp CB on the same panel. Figure 11-1 is a functional diagram of the power supply cards.



**Figure 11-1. Functional diagram of the power supply cards**

There is circuit protection on the power supply cards. This protection will prevent transient overvoltage (32 V dc) and undervoltage (22 V dc) conditions as well as failures caused by polarity reversals. A power sense indication is supplied to the MDM data buffer cards. Power supply card A19 sends the power sense to MDM A data buffer card in slot A1. Power supply card A20 sends the power sense to MDM B data buffer card in slot A2. See the MDM data buffer card subsection for more information on the power sense and power-on reset logic.

Internal to the power supply cards are two regulators which generate +13 V dc and +10 V dc output respectively. These regulated power levels are sent to each card in the GCIL. The +10 V dc is later regulated down to +6 V dc by each card.

Vital statistics on the power supplies

- Voltage: 28 V dc (22 V dc min/32 V dc max.)
- Source: Panel R14 Row B CB 44 Mn A R14 (3A)  
CB 49 Mn C R14 (3A)
- Consumption: 60 W max

### 11.3.2 MDM Data Buffer Cards

The MDM A and B data buffer cards are essentially identical cards with minor differences in the control logic and interlock circuitry. Each buffer card consists of six functional elements:

- MDM data buffer
- Ku/S-band fail-safe control logic
- Power-on/power reset logic
- Mode control voltage current limiting and OR'ing circuit
- Series interlock logic
- Safety (exclusive) interlock logic

#### 11.3.2.1 MDM Data Buffer

The MDM data buffer cards are used to collect the command bits (9) and an MDM data buffer card selection bit from their respective payload MDMs. Card A1 is connected to Payload MDM 1, while card A2 is connected to payload MDM 2. The GCIL continues to process commands even if one of the payload MDMs fails. GCIL commands can be routed to either MDM.

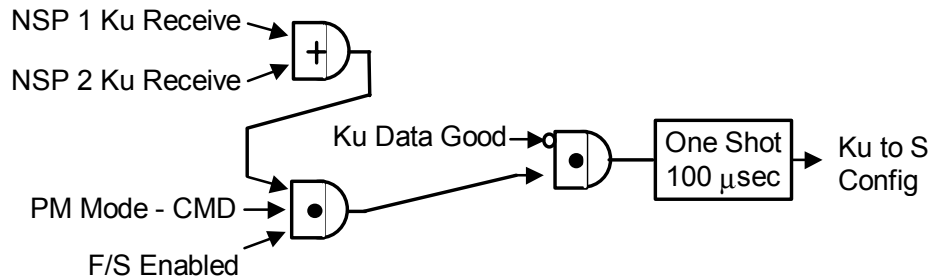
These cards contain logic to detect when a new command is to be processed and passed to the decoder/driver cards. This function is called ALL ZERO. Each of the 9 command bits are set to a zero value before the next command is sent down the same lines. Each of the command data lines are inverted and sent through an AND gate. The output from the gate resets the select decoder A or B discrete; so when a low-to-high transition is detected on any one of the nine data lines, it triggers the SEL DEC discrete, enabling the SEL DEC on the decoder/drive cards to decode the nine data (command) lines.

#### 11.3.2.2 Ku-Band/S-Band Fail-Safe Logic

The Ku-band/S-band fail-safe circuits direct the appropriate decoder/drivers to configure the S-band PM communications equipment to provide an uplink if the Ku-band forward link loses lock for more than 13 seconds or fails for any reason, as long as the following conditions are met:

- S-band PM CMD/PNL mode switch is in the CMD position
- Ku-band/S-band fail-safe has been enabled via uplink command
- NSP is configured with Ku-band as the source

See Figure 11-2 for the fail-safe logic.



**Figure 11-2. Ku fail-safe logic**

The fail-safe will result in the following changes:

- NSP data source - S-BD
- NSP uplink - LDR
- Uplink coding - ON
- S-band mode - TDRS
- S-band transponder filter - NARROW

**11.3.2.3 Power-On/Power Reset Logic**

The Power Reset (PR) (A or C) circuitry detects a power-on, poweroff or an undervoltage of less than 22 V dc for a period of  $\geq 400 \mu\text{sec}$ . The PRA discrete is set by card A1 while PRC is set by card A2. Both card A1 and A2 process both PR conditions to determine if the other card and associated power supply card have a power problem. Loss of both PRA and PRC causes the GCIL to revert to the D&C switch configuration for all systems.

The +10 volt and +13 volt regulated power are tested for overvoltage and undervoltage conditions in the MDM data buffer cards. The following table gives the ranges for each. If an undervoltage or overvoltage condition is detected by this process, the POWER SENSE discrete is set low. This action sets the telemetry term for the power supply status to low (0 = off).

| Regulated | Overvolts | Undervolts |
|-----------|-----------|------------|
| +10       | 8.8       | 12.5       |
| +13       | 9.9       | 13.8       |

**11.3.2.4 Mode Control Voltage Current Limiting (PNL/CMD Modes)**

Mode control voltage is used to determine if the control switch for a subsystem is in the panel position or not. Mn A and Mn C power from the GCIL CBs on panel R14 supply the power to the mode control switches for each of the systems. The power passes through the command side of the switches to tell the GCIL whether the system is in

command mode or panel mode. The two buses are current limited, then diode OR'd together to establish the signal to the GCIL MDM data buffer cards. The isolation prevents one power bus from causing a failure of the mode logic for the subsystem. A listing of the subsystems mode switches and which MDM data buffer card they pass through follows.

| Panel/command switch | MDM A (card A1) | MDM B (card A2) |
|----------------------|-----------------|-----------------|
| TV (panel A7)        | ✓               |                 |
| FM (panel A1R)       | ✓               |                 |
| PL (panel A1L)       | ✓               |                 |
| KU (panel A1U)       |                 | ✓               |
| PM (panel C3)        |                 | ✓               |

### 11.3.2.5 Series Interlock Logic

The design of the GCIL provides simulation, in the uplink command mode, of mechanical D&C switches connected in series. The decoder/driver cards accept and maintain the command. The output signal from the driver on the decoder/driver card is sent only after receiving the last command in the series group.

Example: The payload power 1 or 2 must be on for the PI and or the PSP to turn on.

Some of the communications string 1 driver series interlocks are tied to the like function on string 2 so that both system configurations are the same when going from panel to command. This allows for cross strapping of communication strings. The following table lists which series interlock logic is located on which MDM data buffer cards.

| Series interlock logic         | MDM A (card A1) | MDM B (card A2) |
|--------------------------------|-----------------|-----------------|
| Transponder 1 direct (1 and 2) | ✓               |                 |
| Transponder 2 direct (1 and 2) |                 | ✓               |
| Spread spectrum disable        | ✓               | ✓               |
| Antenna SW freq high no. 1     | ✓               |                 |
| Antenna SW freq high no. 2     |                 | ✓               |
| Antenna SW freq low no. 1      | ✓               |                 |
| Antenna SW freq low no. 2      |                 | ✓               |
| STDN high xpndr no. 1          | ✓               |                 |
| STDN high xpndr no. 2          |                 | ✓               |

### 11.3.2.6 Safety (Exclusive) Interlock Logic

Safety interlocks duplicate the mechanical exclusion positions of a switch when in the command mode. The switch position driver interlock output is inverted, then applied to another switch position series driver interlock input to prevent that LRU from turning on when the first LRU is already on.

Example: When NSP 1 is on, its interlock output is inverted and sent to NSP 2 series interlock input. This prevents NSP 2 from turning on while NSP 1 is on.

The following table shows which safety interlock logic is located on which MDM data buffer cards.

| Safety interlock logic | MDM A (card A1) | MDM B (card A2) |
|------------------------|-----------------|-----------------|
| RADAR power on         | ✓               |                 |
| Comm A power on        | ✓               |                 |
| NSP no. 1 control      |                 | ✓               |
| NSP no. 2 control      | ✓               |                 |
| XPNDR no. 1 on control |                 | ✓               |
| XPNDR no. 2 on control | ✓               |                 |
| VCU MNB - on           |                 | ✓               |
| VCU MNA - on           | ✓               |                 |

### 11.3.3 Decoder/Driver Cards

There are 16 decoder/driver cards in the GCIL, 15 standard (slots A4-A9 and A11-A18) and 1 complex (slot A10). The decoder/driver cards are used to decode the commands that are received, to determine which driver on the card to stimulate, and to isolate the power so that one decoder or driver failure does not affect the other cards. The standard card has 8 decoders (PROMS) and 16 hybrid drivers. The complex driver card has 6 decoders (PROMS) and 10 hybrid drivers. Each decoder/driver card consists of the following items.

- Bus isolation resistors
- 6-volt regulators and 13-volt isolation
- Strobe generator and power strobe
- PROM decoders
- Hybrid drivers
- Z-bar circuits

### 11.3.3.1 Bus Isolation Resistors

The isolation resistor limits the failure to a single card if a short occurs within the decoder/driver card.

### 11.3.3.2 6-Volt Regulators and +13 Volt Isolation

The power supply cards send +10 volts each to the decoder/driver cards. The decoder/driver isolates the voltage, then regulates it down the +6 volts needed by the CMOS devices on the card. Each of the power sources is sent to both of the regulators (6VA and 6VB). The loss of one or the other power supply cards does not affect the operation of the decoder/driver cards.

The +13 volts from each of the power supply cards is handled in much the same way as the +10 volts although they are not regulated to a different power level. They are simply combined, then output as 13VA and 13VB. The loss of one of these power supplies does not adversely affect the operation of the card.

### 11.3.3.3 Decoder

The decoders are used to determine which drivers are to receive the signals that were requested by the incoming command. There are two identical sets of decoders per card; one for the MDM data buffers A channel, one for the MDM B channel. They can both process the same stimuli, but only the set that has the SEL DEC discrete set high sends the signal on to the appropriate drivers.

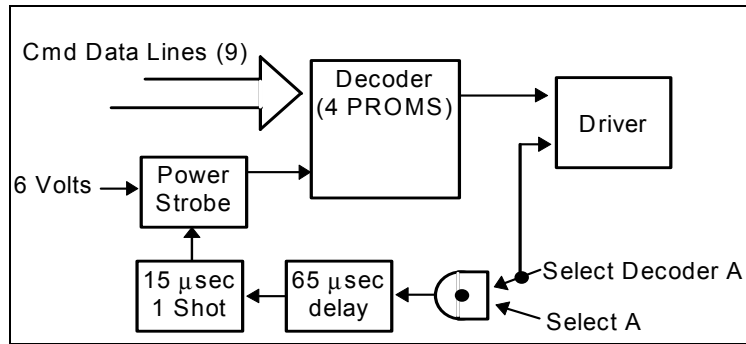
Each of the 4 PROMs (3 on the complex decoder/driver cards) in a decoder can service 4 hybrid drivers (two lines to each driver) for a total of 16 drivers per decoder/ driver card. One line is the on command and the other is the off command.

### 11.3.3.4 Strobe Generator and Power Strobe

Strobe generation is performed when one of the MDM data buffer cards indicates that a command is ready to be processed by the decoder/driver card. The select A or select B signal is set high to indicate which MDM data buffer card has the command. Once the select decoder signal is set high, indicating that at least one command data line has gone from a 0 to a 1 state, there is a delay of 65  $\mu$ sec before a 15  $\mu$ sec single shot is triggered to allow 6 volts of power to go to the decoder from the regulator. This process is called the power strobe. When the power is received at the decoder, it deciphers the command coming from the MDM data buffer card and commands the appropriate driver. The reason for the 65- $\mu$ sec delay is to allow the command data lines coming from the MDM data buffer card to stabilize before the decoder tries to process it. The power strobe is only outputting the 6 volts for between 15 and 300  $\mu$ sec. This was designed to reduce the duty cycle on the decoders to extend their life span.

The functional flow for the decoders is shown in Figure 11-3.



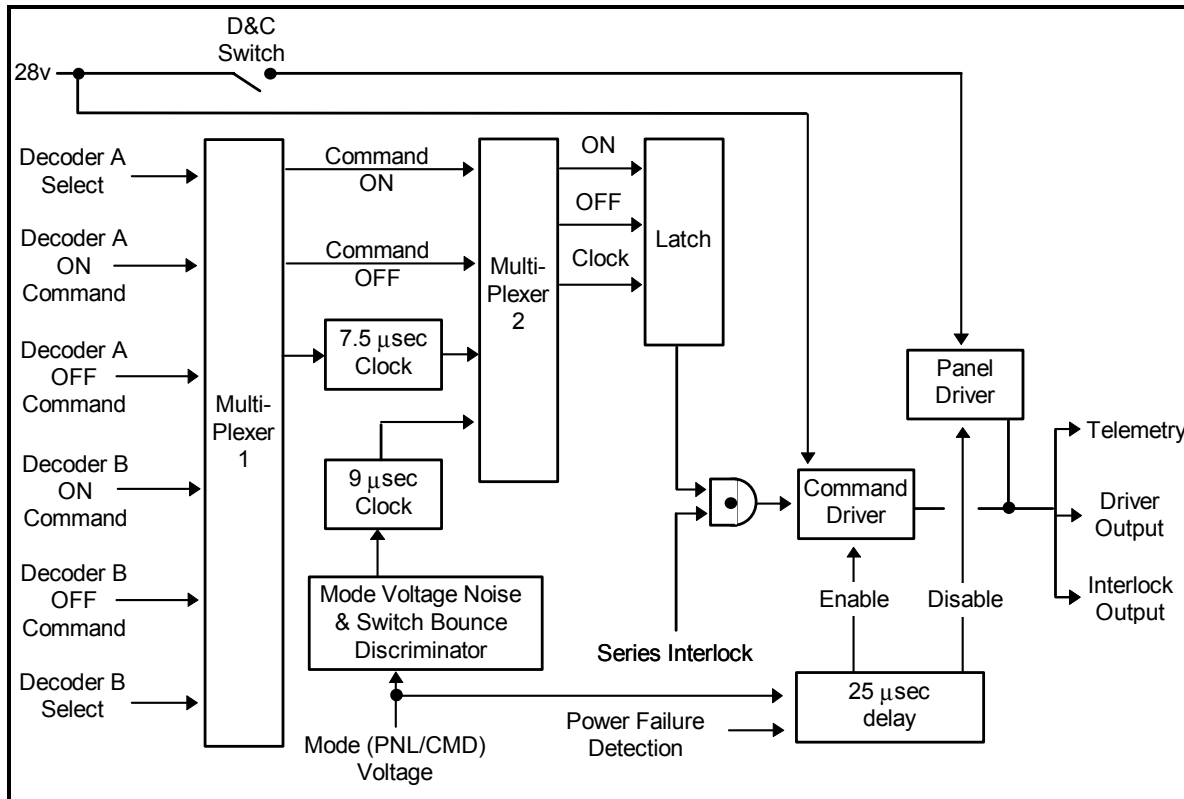


**Figure 11-3. Functional flow for the decoders**

### 11.3.3.5 Hybrid Driver

The hybrid drivers (Figure 11-4) provide the discretes to the subsystem LRUs to select different functions. The hybrid driver is controlled by uplinked command when in CMD mode, and D&C switches when in PNL mode or when the GCIL is powered off. The hybrid driver consists of the following capabilities:

- Process uplink commands
- Process panel switch inputs
- Mode control (PNL/CMD)
- Power failure detection logic



**Figure 11-4. Hybrid driver**

**11.3.3.5.1 Process uplink commands**

Each hybrid driver has the capability to receive commands from either of the MDM data buffer cards. An isolation circuit located at the front end of the driver prevents any failure within the driver from affecting any other driver. Once the signals are converted from 6 to 13 volts, they are passed to the first multiplexer. This multiplexer determines which MDM data buffer input to accept as the command source. This is determined by which SEL DEC signal is set high. See the MDM data buffer card discussion for more on this signal. A command clock generator is used to allow the command signal lines to stabilize before the command is output to the second multiplexer. The second multiplexer processes the command or the panel input. This is determined by the status of the power on/off reset logic and the panel/command switch position. If there was not a power on/off reset and the control switch position is command, the command signal passes on through to the command driver. The command driver sends the on or off state to the LRU.

There are some functions that do not have panel switch positions. These functions can only be commanded. If the GCIL is powered off, these functions revert to a hard-wired configuration. As long as the GCIL remains powered, these functions do not change state, no matter what the positions of any of the panel control switches. The following list is the default hard-wired configurations for the GCIL-only functions.

- Spread spectrum - ENABLED
- S-band PM frequency - HIGH
- S-band preamp standby - ON
- S-band transponder mode select - T/R
- S-band payload transmitter sweep - NARROW
- Ku/S-band fail-safe - DISABLE

#### **11.3.3.5.2 Process Panel Switch Inputs**

The panel driver is enabled when the mode control (CMD/PNL) is set low, panel mode. If the second multiplexer receives a mode control to panel, the switch position state is passed to the panel driver and the command driver is disabled. The panel driver remembers the last position of the panel switch. This can be a problem if the crew changes the configuration for a system, then turns it off, followed by the ground turning on the system.

Example: Crew configures the PI for channel 281/281, then turns off the system. The ground turns on the system, then plans to configure the channels. Channel 281 interferes with the currently selected PM frequency pair, and the ground loses communication with the crew.

#### **11.3.3.5.3 Mode Control (PNL/CMD)**

Mode control is the process of determining if the commands from the ground or the panel switch positions should be processed by the GCIL. Each driver determines which action to take, based on the position of the LRUs control panel switch and the power on/off reset state. The drivers wait 25  $\mu$ sec before processing any mode changes to eliminate switch bounce noise. Mode can be changed by a power failure to the GCIL. Each card determines if it has received a PRA and PRB from MDM data buffer cards A and B. If the power goes off, the panel mode is selected and the driver processes the panel switch positions.

#### **11.3.3.5.4 Power Failure Detection Logic**

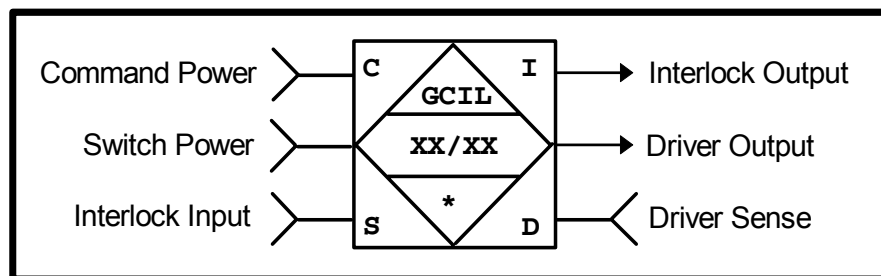
Each driver monitor the power status of the GCIL to determine if the panel switches should be processed. The power failure detection logic in each driver senses the PRA and PRB signals. If they both go high for more than 10  $\mu$ sec, the driver deactivates the command driver and activates the panel driver. In the case of the GCIL-only drivers, they revert to the default hard-wired state as noted in Section 11.3.3.5.1.

### 11.3.3.6 Z Bar Circuits

All the decoder/driver cards use the same printed circuit design. The input signals (switch inputs, command power inputs, mode voltage, driver sense, driver interlock, +13 volts and ground) are fed from the back plane connector pins to the Z-bar on the decoder/driver card. The Z-bar is a terminal board with jumper wires used to jumper combinations to assign signals from one driver to another to perform separate functions. See the drawing at the end of this brief for the actual Z-bar hook ups on each decoder/driver cards.

### 11.3.3.7 Hybrid Driver Drawing Symbol

The drawing symbol of the hybrid drivers (Figure 11-5) is used to explain the inputs and outputs for the driver circuit in the Space Shuttle Systems Handbook, JSC-11174. There are four inputs and two outputs to the symbol, with the driver identification and which panel switch is used to control whether the driver is in panel or command mode. The following list describes each component of the driver symbol.



**Figure 11-5. Example of the GCIL driver drawing symbol**

- A. XX/XX - The first XX is the card designator (A3-A18). The second XX is the driver number (1-16) on that card.
- B. Command Power - Source of the power used by the driver to determine if command is to be output.
- C. Switch Power - Source of power used by the driver to output if not in command mode. The switch position is forwarded to the LRU if the command power goes away.
- D. Series Interlock Input - When set high (1) or not connected (forced high), enables the command driver to be active.
- E. Interlock Output - Designates the state the driver is outputting to other drivers as part of the series interlock or safety (exclusive) interlock.
- F. Driver Output - Turns on or off the LRU attached to the driver.
- G. Driver Sense - Designates the state of the associated drivers in the interlock sequence. Some drivers use an external source (another driver's interlock output),

but some use their own driver output for the driver sense signal. Drivers 1-6 and 9-14 use their own driver output, while 7, 8, 15, and 16 use an external signal in the standard decoder/driver cards. Drivers 1-3 and 6-8 use their own driver output while 4, 5, 9, and 10 use an external signal in the complex decoder/driver cards.

H. Asterisk (\*) - Indicates the panel switch used to determine whether the driver will pass commands on the panel switch positions to the LRU.

1. PM - S-Band PM Crew Control Switch (Panel C3)
2. FM - S-Band FM Crew Control Switch (Panel A1R)
3. Ku - Ku-Band Crew Control Switch (Panel A1U)
4. PL - Payload Comm Crew Control Switch (Panel A1L)
5. TV - CCTV Crew Control Switch (Panel A7)
6. N - No crew control
7. M - Mode voltage not from crew control switch

#### 11.3.3.8 Complex Decoder/Driver

The complex decoder/driver card (slot A10) is essentially the same as the standard decoder/driver cards except that it only contains 2 decoders with 3 PROMs each to support the 10 drivers.

### 11.4 INSTALLATION

Sections 11.4.1 and 11.4.2 discuss the location of the GCIL and cooling requirements.

#### 11.4.1 Location

The GCIL is installed in avionics bay 3A, shelf 3. See Communications and Instrumentation System Water and Air Cooled Equipment for more details.

#### 11.4.2 Cooling

The GCIL is mounted on dual cold plates.

Temperature range:

|              |                                 |
|--------------|---------------------------------|
| Operating    | +0° F minimum, +140° F maximum  |
| Nonoperating | -65° F minimum, +150° F maximum |

The GCIL temperature is monitored by the temperature of the water loops feeding the cold plates. There is no direct temperature measurement of the GCIL LRU.

## 11.5 CREW CONTROLS

The crew cabin contains several switches and circuit breakers that the crew use to manage the GCIL. Sections 11.5.1, 11.5.2, and 11.5.3 discuss each of those controls.

### 11.5.1 Power

The power for the GCIL is supplied through two CBs that are located on panel R14 row B and are titled MN A GCILC and MN C GCILC.

### 11.5.2 Mode Control Switches

- PNL C3            S-band PM control            (S9)
- PNL A1U          Ku-band control                (S6)
- PNL A1L          S-band payload control        (S1)
- PNL A1R          S-band FM control            (S1)
- PNL A7U          TV power control              (S52)

### 11.5.3 Crew SPEC Control

If the crew must issue a command to a GCIL-controlled LRU, they can key any RTC into the DPS utility display (SPEC 1).

## 11.6 TELEMETRY

The GCIL has a very limited amount of telemetry available. All the telemetry is channelized through OI MDM OF4. Descriptions of all the telemetry received on the ground from the GCIL follow.

|           |                   |                  |
|-----------|-------------------|------------------|
| V74S3995E | S-band PM control | 1 = CMD, 0 = PNL |
| V74S6550E | S-band FM control | 1 = CMD, 0 = PNL |
| V74S2430E | Ku-band control   | 1 = CMD, 0 = PNL |
| V74S0793E | CCTV control      | 1 = CMD, 0 = PNL |
| V74S5600E | Payload control   | 1 = CMD, 0 = PNL |

The following parameter indicates the position of the PNL/CMD control switch, which provides the command control voltage to transfer control from the panel switch drivers to the uplink command drivers for the subsystem.

|           |                      |                         |
|-----------|----------------------|-------------------------|
| V74X4809E | Ku fail-safe disable | 1 = Enable, 0 = Disable |
|-----------|----------------------|-------------------------|

The following parameter indicates the GCIL-only driver status of the Ku fail-safe discrete.

|           |                      |                       |
|-----------|----------------------|-----------------------|
| V74X5052X | GCIL active (config) | 1 = Active, 0 = Panel |
|-----------|----------------------|-----------------------|

The GCIL ACTIVE parameter is a telemetry measurement generated by OR'ing the output of two hybrid drivers (4 and 9) on card 10. The two hybrid drivers are GCIL-only functions; therefore, they can only be set (turned on) by command.

The two conditions required to set the GCIL ACTIVE parameter to the high state (1) are: one of two power supplies is working, and command 4376, REVERT TO PANEL RST, has been sent. The low state (0) of this discrete indicates that both GCIL power supplies have lost power or an undervoltage condition existed for at least 400  $\mu$ sec, causing all hybrid drivers to revert to the panel driver configuration.

The parameter does not reflect the state of the crew-controlled PANEL/COMMAND switches nor will it affect command capability. It is only an indicator that GCIL power at both power supplies was interrupted when the discrete was armed. If telemetry indicates that either one or both GCIL power supplies are operable, the ground still has normal command capability to the GCIL. Sending DSM 4376, REVERT TO PANEL RST, again enables the parameter to indicate subsequent power supply problems.

The GCIL ACTIVE parameter, V74X5052E, is located on the comm\_mgmt display in the GCIL section. The parameter title is GCIL Config. The states are 1 = CMD, 0 = PNL.

The onboard display is COMM (SPEC 76). The parameter title is GCIL CONFIG. The states are 1 = CMD, 0 = PNL

|           |                     |                 |
|-----------|---------------------|-----------------|
| V74X4730E | GCIL power supply 1 | 1 = On, 0 = Off |
| V74X4731E | GCIL power supply 2 | 1 = On, 0 = Off |

These parameters indicate that the respective GCIL power supply +13 V dc and preregulated +10 V dc are present and the power supply is ON or they are not present and the power supply is OFF.

## 11.7 OPERATIONAL PROCEDURES

To manage the GCIL system, several procedures should be understood. The following descriptions of some of those procedures are for reference only. See the INCO Console Handbook for the most current versions of all command-related procedures.

### 11.7.1 GCIL Powerup Sequence

#### A. Apply power to the GCIL

On panel R14 row B, close GCIL CB44 for main A and CB49 for main C.

Verify: On the Comm Mgmt display

|                          |               |
|--------------------------|---------------|
| GCIL power supply 1 = On | V74X4730E = 1 |
| GCIL power supply 2 = On | V74X4731E = 1 |

B. Enable the GCIL decoders

Send CMD 4370 GCIL DCDR 1 SEL  
4372 GCIL DCDR 2 SEL

Verify: By sending a command through the GCIL

C. Reset the GCIL config discrete

Send CMD 4376 REVERT TO PANEL RST

Verify: On the Comm Mgmt display

GCIL config = CMD            V74X5052X = 1

D. Select GCIL ground command control

Select the CMD position of the following switches:

Panel C3 S-band PM control = CMD  
A1U Ku-band control = CMD  
A1L S-band payload control = CMD  
A1R S-band FM control = CMD  
A7U TV power control = CMD

Verify: On the Comm Mgmt display

S-band PM control = CMD    V74S3995E = 1  
Ku-band control = CMD      V74S2430E = 1  
Payload control = CMD      V74S5600E = 1  
S-band FM control = CMD    V74S6550E = 1  
CCTV control = CMD        V74S0793E = 1

**11.7.2 GCIL-Only Commands**

Table 11-1 gives DSM command names and descriptions.

**Table 11-1. DSM command names and descriptions**

| <b>DSM</b> | <b>Command name</b>   | <b>Description</b>  |
|------------|-----------------------|---|
| 4370       | GCIL DCDR 1 SEL - ON  | Enables decoder no.1 to receive and decode commands         |
| 4371       | GCIL DCDR 1 SEL - OFF | Inhibits decoder no. 1 from receiving and decoding commands |
| 4372       | GCIL DCDR 2 SEL - ON  | Enables decoder no. 2 to receive and decode commands        |
| 4373       | GCIL DCDR 2 SEL - OFF | Inhibits decoder no. 2 from receiving and decoding commands |



*Table 11-1. DSM command names and descriptions (concluded)*

| <b>DSM</b> | <b>Command name</b>   | <b>Description</b>   |
|------------|-----------------------|--|
| 4374       | GCIL ALL ZEROS - RST  | Test command that sets all command discretes to zero                   |
| 4375       | GCIL ALL ONES - TEST  | Test command that sets all command discretes to one                    |
| 4376       | REVERT TO PANEL RST   | Resets telemetry parameter GCIL CONFIG to one (CMD)                    |
| 4738       | SPREAD SPECTRUM - ON  | Enables spread spectrum by turning spread spectrum disable OFF         |
| 4739       | SPREAD SPECTRUM - OFF | Disables spread spectrum by turning spread spectrum disable ON         |
| 4740       | FREQUENCY - LOW       | Selects S-band PM frequency low for xpndr, preamp, and ANT electronic  |
| 4741       | FREQUENCY - HIGH      | Selects S-band PM frequency high for xpndr, preamp, and ANT electronic |
| 4742       | S-BD XPNDR MODE - T/R | Selects T/R mode for S-band PM transponder                             |
| 4743       | S-BD XPNDR MODE - RCV | Selects receive-only mode for the S-band PM transponder                |
| 4725       | PREAMP HEATERS - OFF  | Turns both preamp 1 and 2 heaters OFF                                  |
| 4726       | PREAMP HEATERS - ON   | Turns both preamp 1 and 2 heaters ON                                   |
| 4140       | KU/S FAIL SAFE - ENA  | Enables the Ku- to S-band fail-safe circuit                            |
| 4141       | KU/S FAIL SAFE - DIS  | Disables the Ku- to S-band fail-safe circuit                           |
| 4820       | PL INTGR SWP - NAR    | Selects the narrow position for the payload interrogator sweep circuit |
| 4821       | PL INTGR SWP - WIDE   | Selects the wide position for the payload interrogator sweep circuit   |

### 11.7.3 Ground Command, GCIL, Controller, and LRU Interfaces

Table 11-2 gives column titles and descriptions. Table 11-3 relates GCIL functions, drivers, and CMD numbers to their telemetry, supply voltage sources, ground commands, and DSM numbers.

**Table 11-2. Column titles and descriptions**

| Column | Title and description of the column   |
|--------|---|
| 1      | (DSM) - Command Identification numbers  |
| 2      | (CMD NAME) - The command name assigned to each DSM number   |
| 3      | (GCL CMD) - The number assigned in the GCIL to that command   |
| 4      | (GCIL DRIVER) - The GCIL driver that controls a particular function. (XX/XX = board/driver) NOTE: ON or OFF describes the state that the command puts the GCIL driver in, not the function!   |
| 5      | (GCIL FUNCTION) - The GCIL mnemonic for that function   |
| 6      | (SERIES INTERLOCK) - The related GCIL drivers that are required for this function to operate. XX/XX is a driver required to be on for operation of the function. Not XX/XX is a driver required to be off for operation of the function |
| 7      | (MODE SRCE) - Power supply for the mode input, generated in the GCIL, from the CMD/PNL switch   |
| 8      | (CMD DRIVER PWR) - Power supply for the command driver  |
| 9      | (PNL/SW #/SW NAME) - Panel switch for crew control which supplies power to the panel driver<br><br>** = GCIL only (true or false), not crew controlled function   |
| 10     | (TELEMETRY) - Telemetry from the GCIL for the driver function   |

### 11.8 OPERATION INSTRUCTIONS

The Payload Interrogator (PI) and Payload Signal Processor (PSP) interlock signals were not tied together to provide redundancy in the PI/PSP/BOTH configuration between payload systems 1 and 2 when switching from PNL to CMD. Therefore, when the PL CONTROL switch is moved from PNL to CMD position, PI/PSP/BOTH configuration in the system not powered are incorrectly set to OFF while the powered system configuration is set correctly to ON.

To prevent the PI/PSP/BOTH configuration from turning off when subsequently commanding to the alternate PL system, send one of the following configuration commands before sending P/L system 1 on 4800 or P/L system 2 on 4802.

- PI ON - 4804
- PSP ON - 4803
- PI/PSP ON - 4805

## 11.9 REFERENCES

### A. CONRAC Corporation

1. Drawing 7906817, Logic Diagram, MDM A Data Buffer A1, rev. A, 7/7/81
2. Drawing 7906819, Logic Diagram, MDM B Data Buffer A2, rev. A, 7/6/81
3. Drawing 7906821, Logic Diagram, Decoder Driver A3 through A9 and all through A18, rev. A, 7/7/81
4. Drawing 7906823, Logic Diagram Complex Decoder Driver A10, rev. A, 7/6/81
5. Drawing 7906825, Schematic Diagram Power Supply A19 and A21, rev. A, 7/7/81
6. Document GCIL-TOO-1A, GCIL Theory of Operation; 8/17/79

### B. Rockwell International Corporation

1. Drawing V570-740299, Schematic diagram - C&T Ground Command Interface Logic Controller, rev. B, 4/12/82
2. Document MC450-0051, Controller, Ground Commands Interface Logic, rev. E, 2/15/80

### C. INCO Internal Documentation

GCIL Theory of Operations, J. Conner, Oct. 16, 1995

**Table 11-3. GCIL functions, drivers, and CMD numbers with telemetry, supply voltage sources, ground commands, and DSM numbers**

| DSM no. | CMD name             | GCL CMD | GCIL driver  | GCIL function  | Series interlock       | Mode SRC                                     | CMD driver power   | PNL/SW no./SW name   | MSID  |
|---------|----------------------|---------|--|--|------------------------|--|--|--|---|
| 4101    | KU COMM A PWR - OFF  | 003     | 3/2 OFF<br>3/3 OFF   | COMM A POWER ON<br>COMM A STANDBY  | NOT 3/4                | KU A<br>KU A                                 | VmnB<br>VmnB   | A1U/S12/PWR KU A<br>A1U/S12/PWR KU A   | V74X4818E<br>V74X4807E  |
| 4102    | KU COMM A PWR - ON   | 001     | 3/2 ON<br>3/3 OFF<br>3/4 OFF<br>3/5 OFF                              | COMM A POWER ON<br>COMM A STANDBY<br>RADAR POWER ON<br>RADAR POWER STANDBY                                 | NOT 3/4<br><br>NOT 3/2 | KU A<br>KU A<br>KU A<br>KU A                 | VmnB<br>VmnB<br>VmnB<br>VmnB                             | A1U/S12/PWR KU A<br>A1U/S12/PWR KU A<br>A1U/S12/PWR KU A<br>A1U/S12/PWR KU A                             | V74X4818E<br>V74X4807E  |
| 4103    | KU COMM A PWR - STBY | 002     | 3/3 ON<br>3/2 OFF<br>3/4 OFF<br>3/5 OFF                              | COMM A STANDBY<br>COMM A POWER ON<br>RADAR POWER ON<br>RADAR POWER STANDBY                                 | NOT 3/4<br>NOT 3/2     | KU A<br>KU A<br>KU A<br>KU A                 | VmnB<br>VmnB<br>VmnB<br>VmnB                             | A1U/S12/PWR KU A<br>A1U/S12/PWR KU A<br>A1U/S12/PWR KU A<br>A1U/S12/PWR KU A                             | V74X4807E<br>V74X4818E  |
| 4104    | KU A ANT - GPC       | 007     | 3/11 ON<br>3/12 OFF<br>3/13 OFF<br>3/14 OFF                          | KU-A GPC<br>KU-A ANT-GPC DESIGNATE<br>KU-A MANUAL SLEW<br>KU-A AUTOTRACK                                   |                        | KU A<br>KU A<br>KU A<br>KU A                 | KU EA A1<br>KU EA A1<br>KU EA A1<br>KU EA A1             | A1U/S 7/KU A<br>A1U/S 7/KU A<br>A1U/S 7/KU A<br>A1U/S 7/KU A   | V74X4820E<br>V74X4822E<br>V74X4810E<br>V74X4824E              |
| 4105    | KU A ANT - GPC DESIG | 008     | 3/12 ON<br>3/11 OFF<br>3/13 OFF<br>3/14 OFF                          | KU-A ANT-GPC DESIGNATE<br>KU-A GPC<br>KU-A MANUAL SLEW<br>KU-A AUTOTRACK                                   |                        | KU A<br>KU A<br>KU A<br>KU A                 | KU EA A1<br>KU EA A1<br>KU EA A1<br>KU EA A1             | A1U/S 7/KU A<br>A1U/S 7/KU A<br>A1U/S 7/KU A<br>A1U/S 7/KU A   | V74X4822E<br>V74X4820E<br>V74X4810E<br>V74X4824E              |
| 4106    | KU A ANT - AUTO      | 027     | 3/14 ON<br>3/11 OFF<br>3/12 OFF<br>3/13 OFF                          | KU-A AUTOTRACK<br>KU-A GPC<br>KU-A ANT-GPC DESIG<br>KU-A MANUAL SLEW                                       |                        | KU A<br>KU A<br>KU A<br>KU A                 | KU EA A1<br>KU EA A1<br>KU EA A1<br>KU EA A1             | A1U/S 7/KU A<br>A1U/S 7/KU A<br>A1U/S 7/KU A<br>A1U/S 7/KU A   | V74X4824E<br>V74X4820E<br>V74X4822E<br>V74X4810E              |
| 4107    | KU A ANT - MAN SLEW  | 009     | 3/13 ON<br>3/11 OFF<br>3/12 OFF<br>3/14 OFF                          | KU-A MANUAL SLEW<br>KU-A GPC<br>KU-A ANT-GPC DESIGNATE<br>KU-A AUTOTRACK                                   |                        | KU A<br>KU A<br>KU A<br>KU A                 | KU EA A1<br>KU EA A1<br>KU EA A1<br>KU EA A1             | A1U/S 7/KU A<br>A1U/S 7/KU A<br>A1U/S 7/KU A<br>A1U/S 7/KU A   | V74X4810E<br>V74X4820E<br>V74X4822E<br>V74X4824E              |
| 4110    | KU UL DATA - COMM A  | 014     | 3/9 ON<br>11/3 OFF   | KU-A DATA SELECT<br>KU-B DATA SELECT   |                        | KU A<br>KU B                                 | KU EA A1<br>KU EA B1                                     | A1U/9/KU SPA DTA<br>A1U/9/KU SPA DTA   |   |
| 4121    | KU HDR - OFF         | 016     | 17/16 ON<br>17/2 OFF<br>17/3 OFF<br>17/4 OFF<br>17/5 OFF<br>17/6 OFF | KU HDR OFF<br>KU HDR P/L MAX<br>KU HDR CCTV<br>KU HDR P/L ANALOG<br>KU HDR P/L DIGTAL<br>KU HDR P/L INTERR |                        | KU C<br>KU C<br>KU C<br>KU C<br>KU C<br>KU C | KU SPA<br>KU SPA<br>KU SPA<br>KU SPA<br>KU SPA<br>KU SPA | A1U/15/HI DATA<br>A1U/15/HI DATA<br>A1U/15/HI DATA<br>A1U/15/HI DATA<br>A1U/15/HI DATA<br>A1U/15/HI DATA | V74X4831E<br>V74X4830E<br>V74X4828E<br>V74X4829E<br>V74X4832E |

**Table 11-3. GCIL functions, drivers, and CMD numbers with telemetry, supply voltage sources, ground commands, and DSM numbers (continued)**

| DSM no. | CMD name          | GCL CMD | GCIL driver  | GCIL function   | Series interlock | Mode SRC                                     | CMD driver power   | PNL/SW no./SW name   | MSID  |
|---------|-------------------|---------|--|---|------------------|--|--|--|---|
| 4122    | KU HDR - PL MAX   | 015     | 17/2 ON<br>17/3 OFF<br>17/4 OFF<br>17/5 OFF<br>17/6 OFF<br>17/16 OFF | KU HDR P/L MAX<br>KU HDR CCTV<br>KU HDR P/L ANALOG<br>KU HDR P/L DIGITAL<br>KU HDR P/L INTERR<br>KU HDR OFF |                  | KU C<br>KU C<br>KU C<br>KU C<br>KU C<br>KU C | KU SPA<br>KU SPA<br>KU SPA<br>KU SPA<br>KU SPA<br>KU SPA | A1U/15/HI DATA<br>A1U/15/HI DATA<br>A1U/15/HI DATA<br>A1U/15/HI DATA<br>A1U/15/HI DATA<br>A1U/15/HI DATA | V74X4831E<br>V74X4830E<br>V74X4828E<br>V74X4829E<br>V74X4832E |
| 4123    | KU HDR - PL INT   | 020     | 17/6 ON<br>17/2 OFF<br>17/3 OFF<br>17/4 OFF<br>17/5 OFF<br>17/16 OFF | KU HDR P/L INTERR<br>KU HDR P/L MAX<br>KU HDR CCTV<br>KU HDR P/L ANALOG<br>KU HDR P/L DIGITAL<br>KU HDR OFF |                  | KU C<br>KU C<br>KU C<br>KU C<br>KU C<br>KU C | KU SPA<br>KU SPA<br>KU SPA<br>KU SPA<br>KU SPA<br>KU SPA | A1U/15/HI DATA<br>A1U/15/HI DATA<br>A1U/15/HI DATA<br>A1U/15/HI DATA<br>A1U/15/HI DATA<br>A1U/15/HI DATA | V74X4832E<br>V74X4831E<br>V74X4830E<br>V74X4828E<br>V74X4829E |
| 4124    | KU HDR - PL ANALG | 018     | 17/4 ON<br>17/2 OFF<br>17/3 OFF<br>17/5 OFF<br>17/6 OFF<br>17/16 OFF | KU HDR P/L ANALOG<br>KU HDR P/L MAX<br>KU HDR CCTV<br>KU HDR P/L DIGITAL<br>KU HDR P/L INTERR<br>KU HDR OFF |                  | KU C<br>KU C<br>KU C<br>KU C<br>KU C<br>KU C | KU SPA<br>KU SPA<br>KU SPA<br>KU SPA<br>KU SPA<br>KU SPA | A1U/15/HI DATA<br>A1U/15/HI DATA<br>A1U/15/HI DATA<br>A1U/15/HI DATA<br>A1U/15/HI DATA<br>A1U/15/HI DATA | V74X4828E<br>V74X4831E<br>V74X4830E<br>V74X4829E<br>V74X4832E |
| 4125    | KU HDR - PL DIGI  | 019     | 17/5 ON<br>17/2 OFF<br>17/3 OFF<br>17/4 OFF<br>17/6 OFF<br>17/16 OFF | KU HDR P/L DIGITAL<br>KU HDR P/L MAX<br>KU HDR CCTV<br>KU HDR P/L ANALOG<br>KU HDR P/L INTERR<br>KU HDR OFF |                  | KU C<br>KU C<br>KU C<br>KU C<br>KU C<br>KU C | KU SPA<br>KU SPA<br>KU SPA<br>KU SPA<br>KU SPA<br>KU SPA | A1U/15/HI DATA<br>A1U/15/HI DATA<br>A1U/15/HI DATA<br>A1U/15/HI DATA<br>A1U/15/HI DATA<br>A1U/15/HI DATA | V74X4829E<br>V74X4831E<br>V74X4830E<br>V74X4828E<br>V74X4832E |
| 4126    | KU HDR - TV       | 017     | 17/3 ON<br>17/2 OFF<br>17/4 OFF<br>17/5 OFF<br>17/6 OFF<br>17/16 OFF | KU HDR CCTV<br>KU HDR P/L MAX<br>KU HDR P/L ANALOG<br>KU HDR P/L DIGITAL<br>KU HDR P/L INTERR<br>KU HDR OFF |                  | KU C<br>KU C<br>KU C<br>KU C<br>KU C<br>KU C | KU SPA<br>KU SPA<br>KU SPA<br>KU SPA<br>KU SPA<br>KU SPA | A1U/15/HI DATA<br>A1U/15/HI DATA<br>A1U/15/HI DATA<br>A1U/15/HI DATA<br>A1U/15/HI DATA<br>A1U/15/HI DATA | V74X4830E<br>V74X4831E<br>V74X4828E<br>V74X4829E<br>V74X4832E |
| 4131    | KU LDR - OFF      | 021     | 17/9 OFF<br>17/10 OFF<br>17/11 OFF<br>17/15 OFF                      | KU LDR P/L DIGITAL<br>KU LDR MMU1<br>KU LDR MMU2<br>KU LDR P/L INTERR                                       |                  | KU C<br>KU C<br>KU C<br>KU C                 | KU SPA<br>KU SPA<br>KU SPA<br>KU SPA                     | A1U/16/LO DATA<br>A1U/16/LO DATA<br>A1U/16/LO DATA<br>A1U/16/LO DATA                                     | V74X4839E<br>V74X3448E<br>V74X3449E<br>V74X4836E              |
| 4136    | KU LDR - MMU1     | 023     | 17/10 ON<br>17/9 OFF<br>17/11 OFF                                    | KU LDR MMU1<br>KU LDR P/L DIGITAL<br>KU LDR MMU2  |                  | KU C<br>KU C<br>KU C                         | KU SPA<br>KU SPA<br>KU SPA                               | A1U/16/LO DATA<br>A1U/16/LO DATA<br>A1U/16/LO DATA   | V74X3448E<br>V74X4839E<br>V74X3449E                           |

**Table 11-3. GCIL functions, drivers, and CMD numbers with telemetry, supply voltage sources, ground commands, and DSM numbers (continued)**

| DSM no. | CMD name  | GCL CMD | GCIL driver  | GCIL function  | Series interlock     | Mode SRC   | CMD driver power   | PNL/SW no./SW name  | MSID   |
|---------|---|---------|--|--|----------------------|--|--|---|--|
|         |   |         | 17/15 OFF  | KU LDR P/L INTERR  |                      | KU C   | KU SPA   | A1U/16/LO DATA  | V74X4836E  |
| 4137    | KU LDR - MMU2   | 024     | 17/11 ON<br>17/9 OFF<br>17/10 OFF<br>17/15 OFF   | KU LDR MMU2<br>KU LDR P/L DIGITAL<br>KU LDR MMU1<br>KU LDR P/L INTERR  |                      | KU C<br>KU C<br>KU C<br>KU C   | KU SPA<br>KU SPA<br>KU SPA<br>KU SPA   | A1U/16/LO DATA<br>A1U/16/LO DATA<br>A1U/16/LO DATA<br>A1U/16/LO DATA  | V74X3449E<br>V74X4839E<br>V74X3448E<br>V74X4836E   |
| 4134    | KU LDR - PL DIGI  | 022     | 17/9 ON<br>17/10 OFF<br>17/11 OFF<br>17/15 OFF   | KU LDR P/L DIGITAL<br>KU LDR MMU1<br>KU LDR MMU2<br>KU LDR P/L INTERR  |                      | KU C<br>KU C<br>KU C<br>KU C   | KU SPA<br>KU SPA<br>KU SPA<br>KU SPA   | A1U/16/LO DATA<br>A1U/16/LO DATA<br>A1U/16/LO DATA<br>A1U/16/LO DATA  | V74X4839E<br>V74X3448E<br>V74X3449E<br>V74X4836E   |
| 4135    | KU LDR - PL INT   | 029     | 17/15 ON<br>17/9 OFF<br>17/10 OFF<br>17/11 OFF   | KU LDR P/L INTERR<br>KU HDR P/L DIGITAL<br>KU LDR MMU1<br>KU LDR MMU2  |                      | KU C<br>KU C<br>KU C<br>KU C   | KU SPA<br>KU SPA<br>KU SPA<br>KU SPA   | A1U/16/LO DATA<br>A1U/16/LO DATA<br>A1U/16/LO DATA<br>A1U/16/LO DATA  | V74X4836E<br>V74X4839E<br>V74X3448E<br>V74X3449E   |
| 4140    | KU/S FAIL SAFE - ENA  | 025     | 3/7 ON   | KU FAIL-SAFE ENABLE  |                      | KU SPA   | KU SPA   | GCIL ONLY FALSE   | V74X4809E  |
| 4141    | KU/S FAIL SAFE - DIS  | 026     | 3/7 OFF  | KU FAIL-SAFE ENABLE  |                      | KU SPA   | KU SPA   | GCIL ONLY FALSE   | V74X4809E  |
| 4200    | VCU MNA BUS/SYNC-SEL  | 121     | 11/7 OFF<br>17/7 ON  | VIDEO CONTROL UNIT MN B-ON<br>VIDEO CONTROL UNIT MN A-ON   | Not 17/7<br>Not 11/7 | TV-A<br>TV-A   | CNTL AB 1<br>CNTL BC 1   | A7U/S12/TVC PWR<br>A7U/S12/TVC PWR  | V74X4880E<br>V74X4881E   |
| 4201    | VCU - OFF   | 123     | 11/7 OFF<br>17/7 OFF   | VIDEO CONTROL UNIT MN B-ON<br>VIDEO CONTROL UNIT MN A-ON   | Not 17/7<br>Not 11/7 | TV-C<br>TV-A   | CNTL BC 1<br>CNTL AB 1   | A7U/S12/TVC PWR<br>A7U/S12/TVC PWR  |  |
| 4202    | VCU MNB BUS/SYNC-SEL  | 122     | 17/7 OFF<br>11/7 ON  | VIDEO CONTROL UNIT MN A-ON<br>VIDEO CONTROL UNIT MN B-ON   | Not 11/7<br>Not 17/7 | TV-C<br>TV-A   | CNTL BC 1<br>CNTL AB 1   | A7U/S12/TVC PWR<br>A7U/S12/TVC PWR  | V74X4881E<br>V74X4880E   |
| 4376    | REVERT TO PANEL RST   | 510     | 10/4 ON<br>10/9 ON   | REVERT TO PANEL (GCIL)<br>REVERT TO PANEL (GCIL)   |                      | VmnA<br>VmnA   | VmnA<br>VmnC   | GCIL ONLY FALSE<br>GCIL ONLY FALSE  | V74X5052E<br>V74X5052E   |
| 4470    | TDRS S-BAND MODE<br>S-MODE - TDRS<br>UPLINK - LDR<br>DNLINK - LDR<br>UPLINK CODING - ON<br>DNLINK CODING - ON | 241     | 5/16 ON<br>4/12 ON<br>9/16 ON<br>4/14 ON<br>5/9 ON<br>5/11 ON<br>5/4 ON<br>5/5 ON<br>4/16 ON<br>5/8 ON<br>13/16 ON<br>12/12 ON | S-BD R/L DATA ENABLE<br>XPNDR #1 U/L FLTR - NAR<br>RANGING DISABLE<br>TDRS XPNDR #1<br>DATA RATE #1 LOW XMIT<br>DATA RATE #1 LOW RCV<br>(NSP) #1 CODING RCV ON<br>(NSP) #1 CODIN G XMIT ON<br>XPNDR T/R #1 MODE<br>UPLINK DATA SOURCE #1 S-BD<br>S-BD R/L DATA ENABLE<br>XPNDR #2 U/L FLTR - NAR |                      | PM A<br>PM A<br>PM A<br>PM A<br>PM A<br>PM A<br>PM A<br>PM A<br>BC 1<br>PM A<br>PM C<br>PM C | N1/L2/VmnB<br>X1/L2/VmnB<br>X1/L2/VmnB<br>X1/L2/VmnB<br>N1/L2/VmnB<br>N1/L2/VmnB<br>N1/L2/VmnB<br>N1/L2/VmnB<br>X1/L2/VmnB<br>N1/L2/VmnB<br>N2/L3/VmnC<br>X2/L3/VmnC | A1L/ 6/S-BD PM MOD<br>A1L/19/DATA RT RCV<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/18/DATA RT XMT<br>A1L/19/DATA RT RCV<br>A1L/22/CODE RCV<br>A1L/21/CODE XMIT<br>GCIL ONLY TRUE<br>A1L/20/UPLK DATA<br>A1L/ 6/S-BD PM MOD<br>A1L/19/DATA RT RCV | V74X4735E<br>V74X4791E<br>V74X4786E<br>V74X4754E<br>V74X4756E<br>V74X4796E<br>V74X4797E<br>V74X4741E<br>V74X4795E<br>V74X4735E |

**Table 11-3. GCIL functions, drivers, and CMD numbers with telemetry, supply voltage sources, ground commands, and DSM numbers (continued)**

| DSM no. | CMD name              | GCL CMD | GCIL driver | GCIL function              | Series interlock          | Mode SRC | CMD driver power | PNL/SW no./SW name | MSID      |
|---------|-----------------------|---------|-------------|----------------------------|---------------------------|----------|------------------|--------------------|-----------|
|         | DATA SOURCE - S       |         | 18/16 ON    | RANGING DISABLE            |                           | PM C     | X2/L3/VmnC       | A1L/ 6/S-BD PM MOD | V74X4786E |
|         |                       |         | 12/14 ON    | TDRS XPNDR #2              |                           | PM C     | X2/L3/VmnC       | A1L/ 6/S-BD PM MOD | V74X4754E |
|         | SPD SPM - ON          |         | 13/9 ON     | DATA RATE #2 LOW XMIT      |                           | PM C     | N2/L3/VmnC       | A1L/18/DATA RT XMT | V74X4756E |
|         |                       |         | 13/11 ON    | DATA RATE #2 LOW RCV       |                           | PM C     | N2/L3/VmnC       | A1L/19/DATA RT RCV | V74X4796E |
|         | S-BD XPNDR MODE - T/R |         | 13/4 ON     | (NSP) #2 CODING RCV ON     |                           | PM C     | N2/L3/VmnC       | A1L/22/CODE RCV    | V74X4797E |
|         |                       |         | 13/5 ON     | (NSP) #2 CODING XMIT ON    |                           | PM C     | N2/L3/VmnC       | A1L/21/CODE XMT    | V74X4741E |
|         | S-BD R/L DATA ENA-ON  |         | 12/16 ON    | XPNDR T/R #2 MODE          |                           | BC 2     | X2/L3/VmnC       | GCIL ONLY TRUE     | V74X4795E |
|         |                       |         | 13/8 ON     | UPLINK DATA SOURCE #2 S-BD |                           | PM C     | N2/L3/VmnC       | A1L/20/UPLK DATA   |           |
|         | RANGING - OFF         |         | 9/8 OFF     | SPREAD SPECTRUM DISABLE    | 4/14 + 12/14              | BC 1     | X1/L2/VmnB       | GCIL ONLY FALSE    | V74X4790E |
|         |                       |         | 4/5 OFF     | SGLS XPNDR #1              |                           | PM A     | X1/L2/VmnB       | A1L/ 6/S-BD PM MOD | V74X4789E |
|         | XPNDR DIRECT - OFF    |         | 4/2 OFF     | STDN HIGH XPNDR #1         |                           | PM A     | X1/L2/VmnB       | A1L/ 6/S-BD PM MOD | V74X4787E |
|         |                       |         | 4/10 OFF    | STDN LOW XPNDR #1          |                           | PM A     | X1/L2/VmnB       | A1L/ 6/S-BD PM MOD | V74X4788E |
|         |                       |         | 5/1 OFF     | DATA RATE #1 HIGH XMIT     |                           | PM A     | N1/L2/VmnB       | A1L/18/DATA RT XMT | V74X4753E |
|         |                       |         | 5/3 OFF     | DATA RATE #1 HIGH RCV      |                           | PM A     | N1/L2/VmnB       | A1L/19/DATA RT RCV | V74X4794E |
|         |                       |         | 5/10 OFF    | UPLINK DATA SOURCE 1 KU-BD |                           | PM A     | N1/L2/VmnB       | A1L/20/UPLK DATA   | V74X4758E |
|         |                       |         | 4/6 OFF     | XPNDR 1 DIRECT 1           | 4/5 + 4/10 + 12/5 + 12/10 | PM A     | X1/L2/VmnB       | A1L/ 6/S-BD PM MOD | V74X4780E |
|         |                       |         |             | XPNDR 1 DIRECT 2           |                           |          |                  |                    |           |
|         |                       |         | 5/12 OFF    | (NSP) #1 CODING RCV OFF    |                           | PM A     | N1/L2/VmnB       | A1L/22/CODE RCV    | V74X4752E |
|         |                       |         | 5/13 OFF    | (NSP) #1 CODING XMIT OFF   |                           | PM A     | N1/L2/VmnB       | A1L/21/CODE XMT    | V74X4751E |
|         |                       |         | 4/8 OFF     | RCVR #1 ONLY (XPNDR 1)     |                           | BC 1     | X1/L2/VmnB       | GCIL ONLY FALSE    | V74X4743E |
|         |                       |         | 4/4 OFF     | XPNDR #1 U/L FLTR - WIDE   |                           | PM A     | X1/L2/VmnB       | A1L/19/DATA RT RCV |           |
|         |                       |         | 18/8 OFF    | SPREAD SPECTRUM DISABLE    | 12/14 + 4/14              | BC 2     | X2/L3/VmnC       | GCIL ONLY FALSE    | V74X4790E |
|         |                       |         | 12/5 OFF    | SGLS XPNDR #2              |                           | PM C     | X2/L3/VmnC       | A1L/ 6/S-BD PM MOD | V74X4789E |
|         |                       |         | 12/2 OFF    | STDN HIGH XPNDR #2         |                           | PM C     | X2/L3/VmnC       | A1L/ 6/S-BD PM MOD | V74X4787E |
|         |                       |         | 12/10 OFF   | STDN LOW XPNDR #2          |                           | PM C     | X2/L3/VmnC       | A1L/ 6/S-BD PM MOD | V74X4788E |
|         |                       |         | 13/1 OFF    | DATA RATE #2 HIGH XMIT     |                           | PM C     | N2/L3/VmnC       | A1L/18/DATA RT XMT | V74X4753E |
|         |                       |         | 13/3 OFF    | DATA RATE #2 HIGH RCV      |                           | PM C     | N2/L3/VmnC       | A1L/19/DATA RT RCV | V74X4794E |
|         |                       |         | 13/10 OFF   | UPLK DATA SRCE #2 KU RCV   |                           | PM C     | N2/L3/VmnC       | A1L/20/UPLK DATA   | V74X4758E |
|         |                       |         | 12/6 OFF    | XPNDR 2 DIRECT 1           | 12/5 + 12/10+ 4/5 + 4/10  | PM C     | X2/L3/VmnC       | A1L/ 6/S-BD PM MOD | V74X4781E |
|         |                       |         |             | XPNDR 2 DIRECT 2           |                           |          |                  |                    |           |
|         |                       |         | 13/12 OFF   | (NSP) #2 CODING RCV OFF    |                           | PM C     | N2/L3/VmnC       | A1L/22/CODE RCV    | V74X4752E |
|         |                       |         | 13/13 OFF   | (NSP) #2 CODING XMIT OFF   |                           | PM C     | N2/L3/VmnC       | A1L/21/CODE XMT    | V74X4751E |
|         |                       |         | 12/8 OFF    | RCVR XPNDR #2 ONLY         |                           | BC 2     | X2/L3/VmnC       | GCIL ONLY FALSE    | V74X4743E |
|         |                       |         | 12/4 OFF    | XPNDR #2 U/L FLTR - WIDE   |                           | PM C     | X2/L3/VmnC       | A1L/19/DATA RT RCV |           |
| 4471    | STDN LOW SBAND MODE   | 242     | 5/16 ON     | S-BD R/L DATA ENABLE       |                           | PM A     | N1/L2/VmnB       | A1L/ 6/S-BD PM MOD | V74X4735E |
|         |                       |         | 4/10 ON     | STD LOW XPNDR #1           |                           | PM A     | X1/L2/VmnB       | A1L/ 6/S-BD PM MOD | V74X4788E |
|         | S-BD MODE - STDN LO   |         | 5/1 ON      | DATA RATE #1 HIGH XMIT     |                           | PM A     | N1/L2/VmnB       | A1L/18/DATA RT XMT | V74X4753E |
|         |                       |         | 5/3 ON      | DATA RATE #1 HIGH RCV      |                           | PM A     | N1/L2/VmnB       | A1L/19/DATA RT RCV | V74X4794E |
|         | UPLINK - HDR          |         | 4/6 ON      | XPNDR 1 DIRECT 1           | 4/5 + 4/10 +              | PM A     | X1/L2/VmnB       | A1L/ 6/S-BD PM MOD | V74X4780E |

**Table 11-3. GCIL functions, drivers, and CMD numbers with telemetry, supply voltage sources, ground commands, and DSM numbers (continued)**

| DSM no. | CMD name   | GCL CMD | GCIL driver   | GCIL function  | Series interlock  | Mode SRC   | CMD driver power   | PNL/SW no./SW name  | MSID  |
|---------|--|---------|---|--|---|--|--|---|---|
|         | DNLINK - HDR<br>UPLINK CODING - OFF<br>DNLINK CODING - OFF<br>DATA SOURCE - S<br>RANGING - ON<br>S-BD XPNDR MODE - T/R<br>S-BD R/L |         | 5/12 ON<br>5/13 ON<br>4/16 ON<br>4/4 ON<br>5/8 ON<br>13/16 ON<br>12/10 ON<br>13/1 ON<br>13/3 ON<br>12/6 ON<br>13/12 ON<br>13/13 ON<br>12/16 ON  | XPNDR 1 DIRECT 2<br>(NSP) #1 CODING RCV OFF<br>(NSP) #1 CODING XMIT OFF<br>XPNDR T/R #1 MODE<br>XPNDR #1 U/L FLTR - WIDE<br>UPLINK DATA SOURCE #1 S-BD<br>S-BD R/L DATA ENABLE<br>STDN LOW XPNDR #2<br>DATA RATE #2 HIGH XMIT<br>DATA RATE #2 HIGH RCV<br>XPNDR 2 DIRECT 1<br>XPNDR 2 DIRECT 2<br>(NSP) #2 CODING RCV OFF<br>(NSP) #2 CODING XMIT OFF<br>XPNDR T/R #2 MODE   | 12/5 + 12/10<br><br><br><br><br><br><br><br><br><br><br>12/5 + 12/10+<br>4/5 + 4/10 | PM A<br>PM A<br>BC 1<br>PM A<br>PM A<br>PM C<br>PM C<br>PM C<br>PM C<br>PM C<br>PM C<br>PM C<br>PM C<br>BC 2   | N1/L2/VmnB<br>N1/L2/VmnB<br>X1/L2/VmnB<br>X1/L2/VmnB<br>N1/L2/VmnB<br>N2/L3/VmnC<br>X2/L3/VmnC<br>N2/L3/VmnC<br>N2/L3/VmnC<br>N2/L3/VmnC<br>X2/L3/VmnC<br>N2/L3/VmnC<br>N2/L3/VmnC<br>X2/L3/VmnC   | A1L/22/CODE RCV<br>A1L/21/CODE XMT<br>GCIL ONLY TRUE<br>A1L/19/DATA RT RCV<br>A1L/20/UPLK DATA<br>A1L/6/S-BD PM MOD<br>A1L/6/S-BD PM MOD<br>A1L/18/DATA RT XMT<br>A1L/19/DATA RT RCV<br>A1L/6/S-BD PM MOD<br>A1L/22/CODE RCV<br>A1L/21/CODE XMT<br>GCIL ONLY TRUE   | V74X4752E<br>V74X4751E<br>V74X4741E<br><br>V74X4795E<br>V74X4735E<br>V74X4788E<br>V74X4753E<br>V74X4794E<br>V74X4781E<br><br>V74X4752E<br>V74X4751E<br>V74X4751E  |
|         |  |         | 12/4 ON<br>13/8 ON<br>4/12 OFF<br>9/16 OFF<br>4/5 OFF<br>4/2 OFF<br>4/14 OFF<br>5/9 OFF<br>5/11 OFF<br>5/10 OFF<br>5/4 OFF<br>5/5 OFF<br>4/8 OFF<br>12/12 OFF<br>18/16 OFF<br>12/5 OFF<br>12/2 OFF<br>12/14 OFF<br>13/9 OFF<br>13/11 OFF<br>13/10 OFF<br>13/4 OFF<br>13/5 OFF<br>12/8 OFF | XPNDR #2 U/L FLTR - WIDE<br>UPLINK DATA SOURCE #2 S-BD<br>XPNDR #1 U/L FLTR - NAR<br>RANGING DISABLE<br>SGLS XPNDR #1<br>STDN HIGH XPNDR #1<br>TDRS XPNDR #1<br>DATA RATE #1 LOW XMIT<br>DATA RATE #1 LOW RCV<br>UPLK DATA SOURCE #1 KU<br>(NSP) #1 CODING RCV ON<br>(NSP) #1 CODING XMIT ON<br>RCVR XPNDR #1 ONLY<br>XPNDR #2 U/L FLTR - NAR<br>RANGING DISABLE<br>SGLS XPNDR #2<br>STDN HIGH XPNDR #2<br>TDRS XPNDR #2<br>DATA RATE #2 LOW XMIT<br>DATA RATE #2 LOW RCV<br>UPLK DATA SOURCE #2 KU RCV<br>(NSP) #2 CODING RCV ON<br>(NSP) #2 CODING XMIT ON<br>RCVR XPNDR #2 ONLY |   | PM C<br>PM C<br>PM A<br>PM A<br>PM A<br>PM A<br>PM A<br>PM A<br>PM A<br>PM A<br>PM A<br>PM A<br>BC 1<br>PM C<br>PM C<br>PM C<br>PM C<br>PM C<br>PM C<br>PM C<br>PM C<br>PM C<br>PM C<br>PM C<br>BC 2 | X2/L3/VmnC<br>N2/L3/VmnC<br>X1/L2/VmnB<br>X1/L2/VmnB<br>X1/L2/VmnB<br>X1/L2/VmnB<br>X1/L2/VmnB<br>N1/L2/VmnB<br>N1/L2/VmnB<br>N1/L2/VmnB<br>N1/L2/VmnB<br>N1/L2/VmnB<br>X1/L2/VmnB<br>X2/L3/VmnC<br>X2/L3/VmnC<br>X2/L3/VmnC<br>X2/L3/VmnC<br>N2/L3/VmnC<br>N2/L3/VmnC<br>N2/L3/VmnC<br>N2/L3/VmnC<br>N2/L3/VmnC<br>N2/L3/VmnC<br>X2/L3/VmnC | A1L/19/DATA RT RCV<br>A1L/20/UPLK DATA<br>A1L/19/DATA RT RCV<br>A1L/6/S-BD PM MOD<br>A1L/6/S-BD PM MOD<br>A1L/6/S-BD PM MOD<br>A1L/6/S-BD PM MOD<br>A1L/18/DATA RT XMT<br>A1L/19/DATA RT RCV<br>A1L/20/UPLK DATA<br>A1L/22/CODE RCV<br>A1L/21/CODE XMT1<br>GCIL ONLY FALSE<br>A1L/19/DATA RT RCV<br>A1L/6/S-BD PM MOD<br>A1L/6/S-BD PM MOD<br>A1L/6/S-BD PM MOD<br>A1L/6/S-BD PM MOD<br>A1L/18/DATA RT XMT<br>A1L/19/DATA RT RCV<br>A1L/20/UPLK DATA<br>A1L/22/CODE RCV<br>A1L/21/CODE XMT<br>GCIL ONLY FALSE | V74X4741E<br>V74X4795E<br><br><br>V74X4791E<br>V74X4789E<br>V74X4787E<br>V74X4786E<br>V74X4754E<br>V74X4758E<br>V74X4796E<br>V74X4797E<br>V74X4743E<br><br>V74X4791E<br>V74X4789E<br>V74X4787E<br>V74X4786E<br>V74X4754E<br>V74X4756E<br>V74X4758E<br>V74X4796E<br>V74X4797E<br>V74X4743E |
| 4472    | STDN HI S-BAND MODE<br>S-BD MODE - STDN HI   | 243     | 5/16 ON<br>4/2 ON<br>5/1 ON   | S-BD R/L DATA ENABLE<br>STDN HIGH XPNDR #1<br>DATA RATE #1 HIGH XMIT   |   | PM A<br>PM A<br>PM A   | N1/L2/VmnB<br>X1/L2/VmnB<br>N1/L2/VmnB   | A1L/6/S-BD PM MOD<br>A1L/6/S-BD PM MOD<br>A1L/18/DATA RT XMT  | V74X4735E<br>V74X4787E<br>V74X4753E   |



**Table 11-3. GCIL functions, drivers, and CMD numbers with telemetry, supply voltage sources, ground commands, and DSM numbers (continued)**

| DSM no. | CMD name              | GCL CMD | GCIL driver | GCIL function              | Series interlock             | Mode SRC | CMD driver power | PNL/SW no./SW name | MSID      |
|---------|-----------------------|---------|-------------|----------------------------|------------------------------|----------|------------------|--------------------|-----------|
|         | UPLINK - HDR          |         | 5/3 ON      | DATA RATE #1 HIGH RCV      |                              | PM A     | N1/L2/VmnB       | A1L/19/DATA RT RCV | V74X4794E |
|         |                       |         | 5/12 ON     | (NSP) #1 CODING RCV OFF    |                              | PM A     | N1/L2/VmnB       | A1L/22/CODE RCV    | V74X4752E |
|         | DNLINK - HDR          |         | 5/13 ON     | (NSP) #1 CODING XMIT OFF   |                              | PM A     | N1/L2/VmnB       | A1L/21/CODE XMT    | V74X4751E |
|         |                       |         | 4/16 ON     | XPNDR T/R #1 MODE          |                              | BC 1     | X1/L2/VmnB       | GCIL ONLY TRUE     | V74X4741E |
|         | UPLINK CODING - OFF   |         | 4/4 ON      | XPNDR #1 U/L FLTR - WIDE   |                              | PM A     | X1/L2/VmnB       | A1L/19/DATA RT RCV |           |
|         |                       |         | 5/8 ON      | UPLK DATA SOURCE #1 S-BD   |                              | PM A     | N1/L2/VmnB       | A1L/20/CODE RCV    | V74X4795E |
|         | DNLINK CODING - OFF   |         | 13/16 ON    | S-BD R/L DATA ENABLE       |                              | PM C     | N2/L3/VmnC       | A1L/6-SB PM MOD    | V74X4735E |
|         |                       |         | 12/2 ON     | STDN HIGH XPNDR #2         |                              | PM C     | X2/L3/VmnC       | A1L/6/S-BD PM MOD  | V74X4787E |
|         | DATA SOURCE - S       |         | 13/1 ON     | DATA RATE #2 HIGH XMIT     |                              | PM C     | N2/L3/VmnC       | A1L/18/DATA RT XMT | V74X4753E |
|         |                       |         | 13/3 ON     | DATA RATE #2 HIGH RCV      |                              | PM C     | N2/L3/VmnC       | A1L/19/DATA RT RCV | V74X4794E |
|         | RANGING - ON          |         | 13/12 ON    | (NSP) #2 CODING RCV OFF    |                              | PM C     | N2/L3/VmnC       | A1L/22/CODE RCV    | V74X4752E |
|         |                       |         | 13/13 ON    | (NSP) #2 CODING XMIT OFF   |                              | PM C     | N2/L3/VmnC       | A1L/21/CODE XMT    | V74X4751E |
|         | S-BD XPNDR MODE- T/R  |         | 12/16 ON    | XPNDR T/R #2 MODE          |                              | BC 2     | X2/L3/VmnC       | GCIL ONLY TRUE     | V74X4741E |
|         |                       |         | 12/4 ON     | XPNDR #2 U/L FLTR - WIDE   |                              | PM C     | X2/L3/VmnC       | A1L/19/DATA RT RCV |           |
|         | S-BD R/L DATA ENA -ON |         | 13/8 ON     | UPLINK DATA SOURCE #2 S-BD |                              | PM C     | N2/L3/VmnC       | A1L/20/UPLK DATA   | V74X4795E |
|         |                       |         | 4/12 OFF    | XPNDR #1 U/L FLTR - NAR    |                              | PM A     | X1/L2/VmnB       | A1L/19/DATA RT RCV |           |
|         | XPNDR DIRECT -OFF     |         | 9/16 OFF    | RANGING DISABLE            |                              | PM A     | X1/L2/VmnB       | A1L/6/S-BD PM MOD  | V74X4791E |
|         |                       |         | 4/5 OFF     | SGLS XPNDR #1              |                              | PM A     | X1/L2/VmnB       | A1L/6/S-BD PM MOD  | V74X4789E |
|         |                       |         | 4/10 OFF    | STDN LOW XPNDR #1          |                              | PM A     | X1/L2/VmnB       | A1L/6/S-BD PM MOD  | V74X4788E |
|         |                       |         | 4/14 OFF    | TDRS XPNDR #1              |                              | PM A     | X1/L2/VmnB       | A1L/6/SBD PM MOD   | V74X4786E |
|         |                       |         | 5/9 OFF     | DATA RATE #1 LOW XMIT      |                              | PM A     | N1/L2/VmnB       | A1L/18/DATA RT XMT | V74X4754E |
|         |                       |         | 5/11 OFF    | DATA RATE #1 LOW RCV       |                              | PM A     | N1/L2/VmnB       | A1L/19/DATA RT RCV | V74X4756E |
|         |                       |         | 5/10 OFF    | UPLK DATA SOURCE #1 KU-BD  |                              | PM A     | N1/L2/VmnB       | A1L/20/UPLK DATA   | V74X4758E |
|         |                       |         | 4/6 OFF     | XPNDR 1 DIRECT 1           | 4/5 + 4/10 +<br>12/5 + 12/10 | PM A     | X1/L2/VmnB       | A1L/6/S-BD PM MOD  | V74X4780E |
|         |                       |         |             | XPNDR 1 DIRECT 2           |                              | PM A     |                  |                    |           |
|         |                       |         | 5/4 OFF     | (NSP) #1 CODING RCV ON     |                              | PM A     | N1/L2/VmnB       | A1L/22/CODE RCV    | V74X4796E |
|         |                       |         | 5/5 OFF     | (NSP) #1 CODING XMIT ON    |                              | PM A     | N1/L2/VmnB       | A1L/21/CODE XMT    | V74X4797E |
|         |                       |         | 4/8 OFF     | RCVR XPNDR #1 MODE         |                              | BC 1     | X1/L2/VmnB       | GCIL ONLY FALSE    | V74X4743E |
|         |                       |         | 12/12 OFF   | XPNDR #2 U/L FLTR - NAR    |                              | PM C     | X2/L2/VmnC       | A1L/19/DATA RT RCV |           |
|         |                       |         | 18/16 OFF   | RANGING DISABLE            |                              | PM C     | X1/L3/VmnC       | A1L/6/S-BD PM MOD  | V74X4791E |
|         |                       |         | 12/5 OFF    | SGLS XPND R #2             |                              | PM C     | X2/L3/VmnC       | A1L/6/S-BD PM MOD  | V74X4789E |
|         |                       |         | 12/10 OFF   | STDN LOW XPNDR #2          |                              | PM C     | X2/L3/VmnC       | A1L/6/S-BD PM MOD  | V74X4788E |
|         |                       |         | 12/14 OFF   | TDRS XPNDR #2              |                              | PM C     | X2/L3/VmnC       | A1L/6/S-BD PM MOD  | V74X4786E |
|         |                       |         | 13/9 OFF    | DATA RATE #2 LOW XMIT      |                              | PM C     | N2/L3/VmnC       | A1L/18/DATA RT XMT | V74X4754E |
|         |                       |         | 13/11 OFF   | DATA RATE #2 LOW RCV       |                              | PM C     | N2/L3/VmnC       | A1L/19/DATA RT RCV | V74X4756E |
|         |                       |         | 13/10 OFF   | UPLK DATA SOURCE KU RCV    |                              | PM C     | N2/L3/VmnC       | A1L/20/UPLK DATA   | V74X4758E |
|         |                       |         | 12/6 OFF    | XPNDR #2 DIRECT 1          | 12/5 + 12/10+<br>4/5 + 4/10  | PM C     | X2/L3/VmnC       | A1L/6/S-BD PM MOD  | V74X4781E |
|         |                       |         |             | XPNDR #2 DIRECT 2          |                              |          |                  |                    |           |
|         |                       |         | 13/4 OFF    | (NSP) #2 CODING RCV ON     |                              | PM C     | N2/L3/VmnC       | A1L/22/CODE RCV    | V74X4796E |
|         |                       |         | 13/5 OFF    | (NSP) #2 CODING XMIT ON    |                              | PM C     | N2/L3/VmnC       | A1L/21/CODE XMT    | V74X4797E |
|         |                       |         | 12/8 OFF    | RCVR XPNDR #2 ONLY         |                              | BC 2     | X2/L3/VmnC       | GCIL ONLY FALSE    | V74X4743E |

**Table 11-3. GCIL functions, drivers, and CMD numbers with telemetry, supply voltage sources, ground commands, and DSM numbers (continued)**

| DSM no.  | CMD name  | GCL CMD | GCIL driver | GCIL function              | Series interlock             | Mode SRC   | CMD driver power   | PNL/SW no./SW name | MSID      |
|----------|---|---------|-------------|----------------------------|------------------------------|------------|--------------------|--------------------|-----------|
| 4473     | <u>SGLS S-BAND MODE</u><br><br>S-BD MODE - SGLS<br><br>UPLINK - HDR<br><br>DNLINK - HDR<br><br>UPLINK CODING - OFF<br><br>DNLINK CODING - OFF<br><br>DATA SOURCE - S<br><br>RANGING - ON<br><br>S-BD XPNDR MODE- T/R<br><br>XPNDR DIRECT - ON<br><br>S-BD R/L DATA ENA-ON | 244     | 5/16 ON     | S-BD R/L DATA ENABLE       | 4/5 + 4/10 +<br>12/5 + 12/10 | PM A       | N1/L2/VmnB         | A1L/6/S-BD PM MOD  | V74X4735E |
|          |   |         | 4/5 ON      | SGLS XPNDR #1              |                              | PM A       | X1/L2/VmnB         | A1L/6/S-BD PM MOD  | V74X4789E |
|          |   |         | 5/1 ON      | DATA RATE #1 HIGH XMIT     |                              | PM A       | N1/L2/VmnB         | A1L/18/DATA RT XMT | V74X4753E |
|          |   |         | 5/3 ON      | DATA RATE #1 HIGH RCV      |                              | PM A       | N1/L2/VmnB         | A1L/19/DATA RT RCV | V74X4794E |
|          |   |         | 4/6 ON      | XPNDR 1 DIRECT 1           |                              | PM A       | X1/L2/VmnB         | A1L/6/S-BD PM MOD  | V74X4780E |
|          |   |         |             | XPNDR 1 DIRECT 2           |                              |            |                    |                    |           |
|          |   |         | 5/12 ON     | (NSP) #1 CODING RCV OFF    |                              | PM A       | N1/L2/VmnB         | A1L/22/CODE RCV    | V74X4752E |
|          |   |         | 5/13 ON     | (NSP) #1 CODING XMIT OFF   |                              | PM A       | N1/L2/VmnB         | A1L/21/CODE XMT    | V74X4751E |
|          |   |         | 4/16 ON     | XPNDR T/R #1 MODE          |                              | BC 1       | X1/L2/VmnB         | GCIL ONLY TRUE     | V74X4741E |
|          |   |         | 4/4 ON      | XPNDR #1 U/L FLTR - WIDE   |                              | PM A       | X1/L2/VmnB         | A1L/19/DATA RT RCV |           |
|          |   |         | 5/8 ON      | UPLK DATA SOURCE #1 S-BD   | PM A                         | N1/L2/VmnB | A1L/20/UPLK DATA   | V74X4795E          |           |
|          |   |         | 13/16 ON    | S-BD R/L DATA ENABLE       | PM C                         | N2/L3/VmnC | A1L/6/S-BD PM MOD  | V74X4735E          |           |
|          |   |         | 12/5 ON     | SGLS XPNDR #2              | PM C                         | X2/L3/VmnC | A1L/6/S-BD PM MOD  | V74X4789E          |           |
|          |   |         | 13/1 ON     | DATA RATE #2 HIGH XMIT     | PM C                         | N2/L3/VmnC | A1L/18/DATA RT XMT | V74X4753E          |           |
|          |   |         | 13/3 ON     | DATA RATE #2 HIGH RCV      | PM C                         | N2/L3/VmnC | A1L/19/DATA RT RCV | V74X4794E          |           |
|          |   |         | 12/6 ON     | XPNDR 2 DIRECT 1           | PM C                         | X2/L3/VmnC | A1L/6/S-BD PM MOD  | V74X4781E          |           |
|          |   |         |             | XPNDR 2 DIRECT 2           | PM C                         |            |                    |                    |           |
|          |   |         | 13/12 ON    | (NSP) #2 CODING RCV OFF    | PM C                         | N2/L3/VmnC | A1L/22/CODE RCV    | V74X4752E          |           |
|          |   |         | 13/13 ON    | (NSP) #2 CODING XMIT OFF   | BC 2                         | N2/L3/VmnC | A1L/21/CODE XMIT   | V74X4751E          |           |
|          |   |         | 12/16 ON    | XPNDR T/R #2 MODE          | PM C                         | X2/L3/VmnC | GCIL ONLY TRUE     | V74X4741E          |           |
| 12/4 ON  | XPNDR #2 U/L FLTR - WIDE  | PM C    | X2/L3/VmnC  | A1L/19/DATA RT RCV         |                              |            |                    |                    |           |
| 13/8 ON  | UPLINK DATA SOURCE #2 S-BD  | PM A    | N2/L3/VmnC  | A1L/20/UPLK DATA           | V74X4795E                    |            |                    |                    |           |
| 4/12 OFF | XPNDR #1 U/L FLTR - NAR   |         | X1/L2/VmnB  | A1L/19/DATA RT RCV         |                              |            |                    |                    |           |
| 9/16 OFF | RANGING DISABLE   | PM A    | X1/L2/VmnB  | A1L/6/S-BD PM MOD          | V74X4791E                    |            |                    |                    |           |
| 4/2 OFF  | STDN HIGH XPNDR #1  | PM A    | X1/L2/VmnB  | A1L/6/S-BD PM MOD          | V74X4787E                    |            |                    |                    |           |
| 4/10 OFF | STDN LOW XPNDR #1   | PM A    | X1/L2/VmnB  | A1L/6/S-BD PM MOD          | V74X4788E                    |            |                    |                    |           |
|          |   |         | 4/14 OFF    | TDRS XPNDR #1              |                              | PM A       | X1/L2/VmnB         | A1L/6/S-BD PM MOD  | V74X4786E |
|          |   |         | 5/9 OFF     | DATA RATE #1 LOW XMIT      |                              | PM A       | N1/L2/VmnB         | A1L/18/DATA RT XMT | V74X4754E |
|          |   |         | 5/11 OFF    | DATA RATE #1 LOW RCV       |                              | PM A       | N1/L2/VmnB         | A1L/19/DATA RT RCV | V74X4756E |
|          |   |         | 5/10 OFF    | UPLK DATA SOURCE #1 KU-BD  |                              | PM A       | N1/L2/VmnB         | A1L/20/UPLK DATA   | V74X4758E |
|          |   |         | 5/4 OFF     | (NSP) #1 CODING RCV ON     |                              | PM A       | N1/L2/VmnB         | A1L/22/CODE RCV    | V74X4752E |
|          |   |         | 5/5 OFF     | (NSP) #1 CODING XMIT ON    |                              | PM A       | N1/L2/VmnB         | A1L/21/CODE XMIT   | V74X4751E |
|          |   |         | 4/8 OFF     | RCVR XPNDR #1 ONLY         |                              | BC 1       | X1/L2/VmnB         | GCIL ONLY FALSE    | V74X4743E |
|          |   |         | 12/12 OFF   | XPNDR #2 U/L FLTR - NAR    |                              | PM C       | X2/L3/VmnC         | A1L/19/DATA RT RCV |           |
|          |   |         | 18/16 OFF   | RANGING DISABLE            |                              | PM C       | X2/L3/VmnC         | A1L/6/S-BD PM MOD  | V74X4791E |
|          |   |         | 12/2 OFF    | STDN HIGH XPNDR #2         |                              | PM C       | X2/L3/VmnC         | A1L/6/S-BD PM MOD  | V74X4787E |
|          |   |         | 12/10 OFF   | STDN LOW XPNDR #2          |                              | PM C       | X2/L3/VmnC         | A1L/6/S-BD PM MOD  | V74X4788E |
|          |   |         | 12/14 OFF   | TDRS XPNDR #2              |                              | PM C       | X2/L3/VmnC         | A1L/6/S-BD PM MOD  | V74X4786E |
|          |   |         | 13/9 OFF    | DATA RATE #2 LOW XMIT      |                              | PM C       | N2/L3/VmnC         | A1L/18/DATA RT XMT | V74X4754E |
|          |   |         | 13/11 OFF   | DATA RATE #2 LOW RCV       |                              | PM C       | N2/L3/VmnC         | A1L/19/DATA RT RCV | V74X4756E |
|          |   |         | 13/10 OFF   | UPLK DATA SOURCE #2 KU-RCV |                              | PM C       | N2/L3/VmnC         | A1L/20/UPLK DATA   | V74X4758E |
|          |   |         | 13/4 OFF    | (NSP) #2 CODING RCV ON     |                              | PM C       | N2/L3/VmnC         | A1L/22/CODE RCV    | V74X4796E |
|          |   |         | 13/5 OFF    | (NSP) #2 CODING XMIT ON    |                              | PM C       | N2/L3/VmnC         | A1L/21/CODE XMIT   | V74X4797E |

**Table 11-3. GCIL functions, drivers, and CMD numbers with telemetry, supply voltage sources, ground commands, and DSM numbers (continued)**

| DSM no. | CMD name              | GCL CMD                  | GCIL driver | GCIL function              | Series interlock   | Mode SRC   | CMD driver power   | PNL/SW no./SW name | MSID   |
|---------|-----------------------|--------------------------|-------------|----------------------------|--------------------|------------|--------------------|--------------------|--|
|         |                       |                          | 12/8 OFF    | RCVR XPNDR #2 ONLY         |                    | BC 2       | X2/L3/VmnC         | GCIL ONLY FALSE    | V74X4743E  |
| 4474    | TDRS RNG S-BAND MODE  | 246                      | 4/12 ON     | XPNDR #1 U/L FLTR - NAR    | 4/14 + 12/14       | PM A       | X1/L2/VmnB         | A1L/19/DATA RT RCV | V74X4786E<br>V74X4756E<br>V74X4796E<br>V74X4741E<br>V74X4795E<br>V74X4786E<br>V74X4756E<br>V74X4796E<br>V74X4741E<br>V74X4795E<br>V74X4735E<br>V74X4790E<br>V74X4791E<br>V74X4789E<br>V74X4787E<br>V74X4788E<br>V74X4794E<br>V74X4758E<br>V74X4752E<br>V74X4743E |
|         | S-BD MODE - TDRS RNG  |                          | 4/14 ON     | TDRS XPNDR #1              |                    | PM A       | X1/L2/VmnB         | A1L/6/S-BD PM MOD  |  |
|         | SPD SPM - ON          |                          | 5/11 ON     | DATA RATE #1 LOW RCV       |                    | PM A       | N1/L2/VmnB         | A1L/19/DATA RT RCV |  |
|         | S-BD XPNDR MODE- T/R  |                          | 5/4 ON      | (NSP) #1 CODING RCV ON     |                    | PM A       | N1/L2/VmnB         | A1L/22/CODE RCV    |  |
|         | UPLINK - LDR          |                          | 4/16 ON     | XPNDR T/R #1 MODE          |                    | BC 1       | X1/L2/VmnB         | GCIL ONLY TRUE     |  |
|         | UPLINK CODING - ON    |                          | 5/8 ON      | UPLK DATA SOURCE #1 S-BD   |                    | PM A       | N1/L2/VmnB         | A1L/20/UPLK DATA   |  |
|         | DATA SOURCE - S       |                          | 12/12 ON    | XPNDR #2 U/L FLTR - NAR    |                    | PM C       | X2/L3/VmnC         | 1L/19/DATA RT RCV  |  |
|         | RANGING - ON          |                          | 12/14 ON    | TDRS XPNDR #2              |                    | PM C       | X2/L3/VmnC         | A1L/ 6/S-BD PM MOD |  |
|         | S-BD R/L DATA ENA-OFF |                          | 13/11 ON    | DATA RATE #2 LOW RCV       |                    | PM C       | N2/L3/VmnC         | A1L/19/DATA RT RCV |  |
|         |                       |                          | 13/4 ON     | (NSP) #2 CODING RCV ON     |                    | PM C       | N2/L3/VmnC         | A1L/22/CODE RCV    |  |
|         |                       |                          | 12/16 ON    | XPNDR T/R #2 MODE          |                    | BC 2       | X2/L3/VmnC         | GCIL ONLY TRUE     |  |
|         |                       |                          | 13/8 ON     | UPLK DATA SOURCE #2 S-BD   |                    | PM C       | N2/L3/VmnC         | A1L/20/UPLK DATA   |  |
|         |                       |                          | 5/16 OFF    | S-BD R/L DATA ENABLE       |                    | PM A       | N1/L2/VmnC         | A1L/ 6/S-BD PM MOD |  |
|         |                       |                          | 9/8 OFF     | SPREAD SPECTRUM DISABLE    |                    | BC 1       | X1/L2/VmnB         | GCIL ONLY FALSE    |  |
|         |                       |                          | 9/16 OFF    | RANGING DISABLE            |                    | PM A       | X1/L2/VmnB         | A1L/ 6/S-BD PM MOD |  |
|         |                       |                          | 4/5 OFF     | SGLS XPNDR #1              |                    | PM A       | X1/L3/VmnB         | A1L/ 6/S-BD PM MOD |  |
|         |                       |                          | 4/2 OFF     | STDN HIGH XPNDR #1         |                    | PM A       | X1/L2/VmnB         | A1L/ 6/S-BD PM MOD |  |
|         |                       |                          | 4/10 OFF    | STDN LOW XPNDR #1          |                    | PM A       | X1/L2/VmnB         | A1L/ 6/S-BD PM MOD |  |
|         |                       |                          | 5/3 OFF     | DATA RATE #1 HIGH RCV      |                    | PM A       | N1/L2/VmnB         | A1L/19/DATA RT RCV |  |
|         |                       |                          | 5/10 OFF    | UPLK DATA SOURCE 1 KU-BD   |                    | PM A       | N1/L2/VmnB         | A1L/20/UPLK DATA   |  |
|         | 5/12 OFF              | (NSP) #1 CODING RCV OFF  | PM A        | N1/L2/VmnB                 | A1L/22/CODE RCV    |            |                    |                    |  |
|         | 4/8 OFF               | RCVR XPNDR #1 ONLY       | BC 1        | X1/L2/VmnB                 | GCIL ONLY FALSE    |            |                    |                    |  |
|         | 4/4 OFF               | XPNDR #1 U/L FLTR - WIDE | PM A        | X1/L2/VmnB                 | A1L/19/DATA RT RCV |            |                    |                    |  |
|         | 13/16 OFF             | S-BD R/L DATA ENABLE     | PM C        | N2/L3/VmnC                 | A1L/6/S-BD PM MOD  |            |                    |                    |  |
|         | 18/8 OFF              | SPREAD SPECTRUM DISABLE  | BC 2        | X2/L3/VmnC                 | GCIL ONLY FALSE    |            |                    |                    |  |
|         | 18/16 OFF             | RANGING DISABLE          | PM C        | X2/L3/VmnC                 | A1L/6/S-BD PM MOD  |            |                    |                    |  |
|         | 12/5 OFF              | SGLS XPNDR #2            | PM C        | X2/L3/VmnC                 | A1L/6/S-BD PM MOD  |            |                    |                    |  |
|         | 12/2 OFF              | STDN HIGH XPNDR #2       | PM C        | X2/L3/VmnC                 | A1L/6/S-BD PM MOD  |            |                    |                    |  |
|         | 12/10 OFF             | STDN LOW XPNDR #2        | PM C        | X2/L3/VmnC                 | A1L/6/S-BD PM MOD  |            |                    |                    |  |
|         |                       |                          | 13/3 OFF    | DATA RATE #2 HIGH RCV      | PM C               | N2/L3/VmnC | A1L/19/DATA RT RCV | V74X4794E          |  |
|         |                       |                          | 13/10 OFF   | UPLK DATA SOURCE #2 KU RCV | PM C               | N2/L3/VmnC | A1L/20/UPLK DATA   | V74X4758E          |  |
|         |                       |                          | 13/12 OFF   | (NSP) #2 CODING RCV OFF    | PM C               | N2/L3/VmnC | A1L/22/CODE RCV    | V74X4752E          |  |
|         |                       |                          | 12/8 OFF    | RCVR XPNDR #2 ONLY         | BC 2               | X2/L3/VmnC | GCIL ONLY FALSE    | V74X4743E          |  |
|         |                       |                          | 12/4 OFF    | XPNDR #2 U/L FLTR - WIDE   | PM C               | X2/L3/VmnC | A1L/19/DATA RT RCV |                    |  |
| 4475    | S-BAND TO KU-BAND     | 245                      | 9/16 ON     | RANGING DISABLE            |                    | PM A       | X1/L2/VmnB         | A1L/6/S-BD PM MOD  | V74X4791E  |
|         | DATA SOURCE - KU      |                          | 5/1 ON      | DATA RATE #1 HIGH XMIT     |                    | PM A       | N1/L2/VmnB         | A1L/18/DATA RT XMT | V74X4753E  |
|         |                       |                          | 5/3 ON      | DATA RATE #1 HIGH RCV      |                    | PM A       | N1/L2/VmnB         | A1L/19/DATA RT XMT | V74X4794E  |
|         |                       |                          | 5/10 ON     | UPLK DATA SOURCE #1 KU-BD  |                    | PM A       | N1/L2/VmnB         | A1L/20/UPLK DATA   | V74X4758E  |
|         | UPLINK - HDR          |                          | 5/12 ON     | (NSP) #1 CODING RCV OFF    |                    | PM A       | N1/L2/VmnB         | A1L/22/CODE RCV    | V74X4752E  |
|         |                       |                          | 5/13 ON     | (NSP) #1 CODING XMIT OFF   | PM A               | N1/L2/VmnB | A1L/21/CODE XMIT   | V74X4751E          |  |

**Table 11-3. GCIL functions, drivers, and CMD numbers with telemetry, supply voltage sources, ground commands, and DSM numbers (continued)**

| DSM no. | CMD name              | GCL CMD | GCIL driver | GCIL function              | Series interlock      | Mode SRC | CMD driver power | PNL/SW no./SW name | MSID      |
|---------|-----------------------|---------|-------------|----------------------------|-----------------------|----------|------------------|--------------------|-----------|
|         | DNLINK - HDR          |         | 4/8 ON      | RCVR XPNDR #1 ONLY         |                       | BC 1     | X1/L2/VmnB       | GCIL ONLY FALSE    | V74X4743E |
|         | UPLINK CODING - OFF   |         | 4/4 ON      | XPNDR #1 U/L FLTR - WIDE   |                       | PM A     | X1/L2/VmnB       | A1L/19/DATA RT RCV |           |
|         |                       |         | 18/16 ON    | RANGING DISABLE            |                       | PM C     | X2/L3/VmnC       | A1L/6/S-BD PM MOD  | V74X4791E |
|         | DNLINK CODING - OFF   |         | 13/1 ON     | DATA RATE #2 HIGH XMIT     |                       | PM C     | N2/L3/VmnC       | A1L/18/DATA RT XMT | V74X4753E |
|         |                       |         | 13/3 ON     | DATA RATE #2 HIGH RCV      |                       | PM C     | N2/L3/VmnC       | A1L/19/DATA RT RCV | V74X4794E |
|         | S-BD PA OPR - OFF*    |         | 13/10 ON    | UPLK DATA SOURCE #2 KU-RCV |                       | PM C     | N2/L3/VmnC       | A1L/20/UPLK DATA   | V74X4758E |
|         |                       |         | 13/12 ON    | (NSP) #2 CODING RCV OFF    |                       | PM C     | N2/L3/VmnC       | A1L/22/CODE RCV    | V74X4752E |
|         | S-BD XPNDR MODE - RCV |         | 13/13 ON    | (NSP) #2 CODING XMIT OFF   |                       | PM C     | N2/L3/VmnC       | A1L/21/CODE XMIT   |           |
|         |                       |         | 12/8 ON     | RCVR XPNDR #2 ONLY         |                       | BC 2     | X2/L3/VmnC       | GCIL ONLY FALSE    | V74X4751E |
|         |                       |         | 12/4 ON     | XPNDR #2 U/L FLTR - WIDE   |                       | PM C     | X2/L3/VmnC       | A1L/19/DATA RT RCV | V74X4743E |
|         | RANGING - OFF         |         | 4/9 OFF     | PA #1 OPERATE              | (4/13+12/13)<br>N12/9 | PM A     | PCA 2            | A1L/12/PWR AMP OP  |           |
|         |                       |         | 4/12 OFF    | XPNDR #1 U/L FLTR - NAR    |                       | PM A     | X1/L2/VmnB       | A1L/6/S-BD PM MOD  | V74X4784E |
|         |                       |         | 5/9 OFF     | DATA RATE #1 LOW XMIT      |                       | PM A     | N1/L2/VmnB       | A1L/18/DATA RT XMT |           |
|         |                       |         | 5/11 OFF    | DATA RATE #1 LOW RCV       |                       | PM A     | N1/L2/VmnB       | A1L/19/DATA RT RCV | V74X4754E |
|         |                       |         | 5/4 OFF     | (NSP) #1 CODING RCV ON     |                       | PM A     | N1/L2/VmnB       | A1L/22/CODE RCV    | V74X4756E |
|         |                       |         | 5/5 OFF     | (NSP) #1 CODING XMIT - ON  |                       | PM A     | N1/L2/VmnB       | A1L/21/CODE XMIT   | V74X4752E |
|         |                       |         | 4/16 OFF    | XPNDR T/R #1 MODE          |                       | BC 1     | X1/L2/VmnB       | GCIL ONLY TRUE     | V74X4751E |
|         |                       |         | 5/8 OFF     | UPLK DATA SOURCE #1 S-BD   | (4/13+12/13)<br>N4/9  | PM A     | N1/L2/VmnB       | A1L/20/UPLK DATA   | V74X4741E |
|         |                       |         | 12/9 OFF    | PA #2 OPERATE              |                       | PM C     | PCA 3            | A1L/12/PWR AMP OP  | V74X4795E |
|         |                       |         | 12/12 OFF   | XPNDR #2 U/L FLTR - NAR    |                       | PM C     | X2/L3/VmnC       | A1L/19/DATA RT RCV | V74X4785E |
|         |                       |         | 13/9 OFF    | DATA RATE #2 LOW XMIT      |                       | PM C     | N2/L3/VmnC       | A1L/18/DATA RT XMT |           |
|         |                       |         | 13/11 OFF   | DATA RATE #2 LOW RCV       |                       | PM C     | N2/L3/VmnC       | A1L/19/DATA RT RCV | V74X4754E |
|         |                       |         | 13/4 OFF    | (NSP) #2 CODING RCV ON     |                       | PM C     | N2/L3/VmnC       | A2L/22/CODE XMIT   | V74X4756E |
|         |                       |         | 13/5 OFF    | (NSP) #2 CODING XMIT ON    |                       | PM C     | N2/L3/VmnC       | A2L/21/CODE XMIT   | V74X4796E |
|         |                       |         | 12/16 OFF   | XPNDR T/R #2 MODE          |                       | BC 2     | X2/L3/VmnC       | GCIL ONLY TRUE     | V74X4797E |
|         |                       |         | 13/8 OFF    | UPLK DATA SOURCE #2 S-BD   |                       | PM C     | N2/L3/VmnC       | A1L/20/UPLK DATA   | V74X4741E |
| 4709    | S-BD ANT ELEC SW - 1  | 031     | 11/8 ON     | ANTENNA SW #1-ON           |                       | PM A     | CNTL BC 1        | A1L/5/SP ANT SW EL | V74X4782E |
|         |                       |         | 17/8 OFF    | ANTENNA SW #2-ON           |                       | PM C     | CNTL BC 2        | A1L/5/SP ANT SW EL | V74X4783E |
| 4710    | ANT ELEC SW - OFF     | 042     | 11/8 OFF    | ANTENNA SW #1-ON           |                       | PM A     | CNTL BC 1        | A1L/5/SP ANT SW EL | V74X4782E |
|         |                       |         | 17/8 OFF    | ANTENNA SW #2-ON           |                       | PM C     | CNTL BC 2        | A1L/5/SP ANT SW EL | V74X4783E |
| 4711    | S-BD AND ELEC SW - 2  | 030     | 17/8 ON     | ANTENNA SW #2-ON           |                       | PM C     | CNTL BC 2        | A1L/5/SP ANT SW EL | V74X4782E |
|         |                       |         | 11/8 OFF    | ANTENNA SW #1-ON           |                       | PM A     | CNTL BC 1        | A1L/5/SP ANT SW EL | V74X4782E |
| 4722    | PREAMP 1 - ON         | 057     | 4/13 ON     | PREAMP #1 ON (PM)          |                       | PM A     | CNTL BC 1        | A1L/10/S-PM PREAMP | V74X4776E |
|         |                       |         | 12/13 OFF   | PREAMP #2 ON (PM)          |                       | PM C     | CNTL BC 2        | A1L/10/S-PM PREAMP | V74X4777E |
| 4723    | PREAMP 1/2 - OFF      | 058     | 4/13 OFF    | PREAMP #1 ON (PM)          |                       | PM A     | CNTL BC 1        | A1L/10/S-PM PREAMP | V74X4776E |
|         |                       |         | 12/13 OFF   | PREAMP #2 ON (PM)          |                       | PM C     | CNTL BC 2        | A1L/10/S-PM PREAMP | V74X4777E |

**Table 11-3. GCIL functions, drivers, and CMD numbers with telemetry, supply voltage sources, ground commands, and DSM numbers (continued)**

| DSM no. | CMD name             | GCL CMD | GCIL driver   | GCIL function  | Series interlock    | Mode SRC   | CMD driver power   | PNL/SW no./SW name   | MSID   |
|---------|----------------------|---------|---|--|---------------------|--|--|--|--|
| 4724    | PREAMP 2 - ON        | 059     | 4/13 OFF<br>12/13 ON  | PREAMP #1 ON (PM)<br>PREAMP #2 ON (PM)   |                     | PM A<br>PM C   | CNTL BC 1<br>CNTL BC 2   | A1L/10/S-PM PREAMP<br>A1L/20/S-PM PREAMP   | V74X4776E<br>V74X4777E   |
| 4725    | PREAMP HEATERS - OFF | 061     | 9/7 OFF<br>18/7 OFF   | PREAMP #1 ON-STBY<br>PREAMP #2 ON-STBY   |                     | BC 1<br>BC 2   | CNTL BC 1<br>CNTL BC 2   | GCIL ONLY TRUE<br>GCIL ONLY TRUE   | V74X4707E<br>V74X4708E   |
| 4726    | PREAMP HEATERS - ON  | 060     | 9/7 ON<br>18/7 ON   | PREAMP #1 ON-STBY<br>PREAMP #2 ON-STBY   |                     | BC 1<br>BC 2   | CNTL BC 1<br>CNTL BC 2   | GCIL ONLY TRUE<br>GCIL ONLY TRUE   | V74X4707E<br>V74X4708E   |
| 4730    | S-BD XPNDR 1 - ON    | 062     | 4/3 ON<br>12/3 OFF  | S-BD XPNDR 1 ON CONTROL<br>S-BD XPNDR 2 ON CONTROL   | NOT 12/3<br>NOT 4/3 | PM A<br>PM C   | CNTL BC 1<br>CNTL BC 2   | CNTL BC 1<br>CNTL BC 2   | V74X4745E<br>V74X4746E   |
| 4731    | S-BD XPNDR 1/2 - OFF | 063     | 4/3 OFF<br>12/3 OFF   | S-BD XPNDR 1 ON CONTROL<br>S-BD XPNDR 2 ON CONTROL   | NOT 12/3<br>NOT 4/3 | PM A<br>PM C   | CNTL BC 1<br>CNTL BC 2   | CNTL BC 1<br>CNTL BC 2   | V74X4745E<br>V74X4746E   |
| 4732    | S-BD XPNDR 2 - ON    | 064     | 12/3 ON<br>4/3 OFF  | S-BD XPNDR 2 ON CONTROL<br>S-BD XPNDR 1 ON CONTROL   | NOT 4/3<br>NOT 12/3 | PM C<br>PM A   | CNTL BC 2<br>CNTL BC 1   | CNTL BC 2<br>CNTL BC 1   | V74X4746E<br>V74X4745E   |
| 4733    | S-BD MODE - TDRS     | 065     | 5/16 ON<br>13/16 ON<br>9/16 ON<br>18/16 ON<br>4/5 OFF<br>12/5 OFF<br>4/2 OFF<br>12/2 OFF<br>4/10 OFF<br>12/10 OFF<br>4/14 ON<br>12/14 ON<br>4/6 OFF<br>12/6 OFF | S-BD R/L DATA ENABLE<br>S-BD R/L DATA ENABLE<br>RANGING DISABLE<br>RANGING DISABLE<br>SGLS XPNDR 1<br>SGLS XPNDR 2<br>STDN HIGH XPNDR 1<br>STDN HIGH XPNDR 2<br>STDN LOW XPNDR 1<br>STDN LOW XPNDR 2<br>TDRS XPNDR 1<br>TDRS XPNDR 2<br>XPNDR 1 DIRECT 1<br>XPNDR 1 DIRECT 2<br>XPNDR 2 DIRECT 1<br>XPNDR 2 DIRECT 2 |                     | PM A<br>PM C<br>PM A<br>PM C<br>PM A<br>PM C<br>PM A<br>PM C<br>PM A<br>PM C<br>PM A<br>PM C<br>PM A<br>PM C<br>PM A<br>PM C<br>PM A<br>PM C | N1/L2/VmnB<br>N2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC | A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD | V74X4735E<br>V74X4735E<br>V74X4791E<br>V74X4791E<br>V74X4789E<br>V74X4789E<br>V74X4787E<br>V74X4787E<br>V74X4788E<br>V74X4788E<br>V74X4788E<br>V74X4786E<br>V74X4786E<br>V74X4786E<br>V74X4780E<br>V74X4781E |
| 4734    | S-BD MODE - STDN HI  | 066     | 4/2 ON<br>12/2 ON<br>5/16 ON<br>13/16 ON<br>4/5 OFF<br>12/5 OFF   | STDN HIGH XPNDR 1<br>STDN HIGH XPNDR 2<br>S-BD R/L DATA ENABLE<br>S-BD R/L DATA ENABLE<br>SGLS XPNDR 1<br>SGLS XPNDR 2   |                     | PM A<br>PM C<br>PM A<br>PM C<br>PM A<br>PM C   | X1/L2/VmnB<br>X2/L3/VmnC<br>N1/L2/VmnB<br>N2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC   | A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD   | V74X4788E<br>V74X4788E<br>V74X4735E<br>V74X4735E<br>V74X4789E<br>V74X4789E   |

**Table 11-3. GCIL functions, drivers, and CMD numbers with telemetry, supply voltage sources, ground commands, and DSM numbers (continued)**

| DSM no. | CMD name            | GCL CMD | GCIL driver   | GCIL function  | Series interlock   | Mode SRC   | CMD driver power   | PNL/SW no./SW name   | MSID   |
|---------|---------------------|---------|---|--|--|--|--|--|--|
|         |                     |         | 9/16 OFF<br>18/16 OFF<br>4/10 OFF<br>12/10 OFF<br>4/14 OFF<br>12/14 OFF<br>4/6 OFF<br><br>12/6 OFF  | RANGING DISABLE<br>RANGING DISABLE<br>STDN LOW XPNDR 1<br>STDN LOW XPNDR 2<br>TDRS XPNDR 1<br>TDRS XPNDR 2<br>XPNDR 1 DIRECT 1<br>XPNDR 1 DIRECT 2<br>XPNDR 2 DIRECT 1<br>XPNDR 2 DIRECT 2   | 4/5 + 4/10 +<br>12/5 + 12/10<br>12/5 + 12/10 +<br>4/5 + 4/10 | PM A<br>PM C<br>PM A<br>PM C<br>PM A<br><br>PM A<br>PM C   | X1/L2/VmnB<br>X2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC<br>X1/L2/VmnB<br><br>X1/L2/VmnB<br>X2/L3/VmnC   | A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br><br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD   | V74X4791E<br>V74X4791E<br>V74X4788E<br>V74X4788E<br>V74X4786E<br><br>V74X4780E<br>V74X4781E  |
| 4735    | S-BD MODE - STDN LO | 067     | 5/16 ON<br>13/16 ON<br>9/16 OFF<br>18/16 OFF<br>4/5 OFF<br>12/5 OFF<br>4/2 OFF<br>12/2 OFF<br>4/10 ON<br>12/10 ON<br>4/14 OFF<br>12/14 OFF<br>4/6 ON<br><br>12/6 ON | S-BD R/L DATA ENABLE<br>S-BD R/L DATA ENABLE<br>RANGING DISABLE<br>RANGING DISABLE<br>SGLS XPNDR 1<br>SGLS XPNDR 2<br>STDN HIGH XPNDR 1<br>STDN HIGH XPNDR 2<br>STDN LOW XPNDR 1<br>STDN LOW XPNDR 2<br>TDRS XPNDR 1<br>TDRS XPNDR 2<br>XPNDR 1 DIRECT 1<br>XPNDR 1 DIRECT 2<br>XPNDR 2 DIRECT 1<br>XPNDR 2 DIRECT 2 | 4/5 + 4/10 +<br>12/5 + 12/10<br>12/5 + 12/10 +<br>4/5 + 4/10 | PM A<br>PM C<br>PM A<br>PM C<br>PM A<br>PM C<br>PM A<br>PM C<br>PM A<br>PM C<br>PM A<br>PM C<br>PM A<br>PM C | N1/L2/VmnB<br>N2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC | A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD | V74X4735E<br>V74X4735E<br>V74X4791E<br>V74X4791E<br>V74X4789E<br>V74X4789E<br>V74X4787E<br>V74X4787E<br>V74X4788E<br>V74X4788E<br>V74X4786E<br>V74X4786E<br>V74X4780E<br>V74X4781E |
| 4736    | S-BD MODE - SGLS    | 068     | 5/16 ON<br>13/16 ON<br>9/16 OFF<br>18/16 OFF<br>4/5 ON<br>12/5 ON<br>4/2 OFF<br>12/2 OFF<br>4/10 OFF<br>12/10 OFF<br>4/14 OFF<br>12/14 OFF<br>4/6 ON<br><br>12/6 ON | S-BD R/L DATA ENABLE<br>S-BD R/L DATA ENABLE<br>RANGING DISABLE<br>RANGING DISABLE<br>SGLS XPNDR 1<br>SGLS XPNDR 2<br>STDN HIGH XPNDR 1<br>STDN HIGH XPNDR 2<br>STDN LOW XPNDR 1<br>STDN LOW XPNDR 2<br>TDRS XPNDR 1<br>TDRS XPNDR 2<br>XPNDR 1 DIRECT 1<br>XPNDR 1 DIRECT 2<br>XPNDR 2 DIRECT 1                     | 4/5 + 4/10 +<br>12/5 + 12/10<br>12/5 + 12/10 +               | PM A<br>PM C<br>PM A<br>PM C<br>PM A<br>PM C<br>PM A<br>PM C<br>PM A<br>PM C<br>PM A<br>PM C<br>PM A<br>PM C | N1/L2/VmnB<br>N2/L3/VmnC<br>X1/L2/VmnB<br>X2/L2/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC | A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD | V74X4735E<br>V74X4735E<br>V74X4791E<br>V74X4791E<br>V74X4789E<br>V74X4789E<br>V74X4787E<br>V74X4787E<br>V74X4788E<br>V74X4788E<br>V74X4786E<br>V74X4786E<br>V74X4780E<br>V74X4781E |

**Table 11-3. GCIL functions, drivers, and CMD numbers with telemetry, supply voltage sources, ground commands, and DSM numbers (continued)**

| DSM no. | CMD name             | GCL CMD | GCIL driver  | GCIL function  | Series interlock   | Mode SRC   | CMD driver power   | PNL/SW no./SW name   | MSID  |
|---------|----------------------|---------|--|--|--|--|--|--|---|
|         |                      |         |  | XPNDR 2 DIRECT 2   | 4/5 + 4/10   |  |  |  |   |
| 4737    | S-BD MODE - TDRS TRK | 071     | 5/16 OFF<br>13/16 OFF<br>9/16 ON   | S-BD R/L DATA ENABLE<br>S-BD R/L DATA ENABLE<br>RANGING DISABLE  |  | PM A<br>PM C<br>PM A   | N1/L2/VmnB<br>N2/L3/VmnC<br>X1/L2/VmnB   | A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD   | V74X4735E<br>V74X4735E<br>V74X4791E   |
|         |                      |         | 18/16 ON<br>4/5 OFF<br>12/5 OFF<br>4/2 OFF<br>12/2 OFF<br>4/10 OFF<br>12/10 OFF<br>4/14 ON<br>12/14 ON | RANGING DISABLE<br>SGLS XPNDR 1<br>SGLS XPNDR 2<br>STDN HIGH XPNDR 1<br>STDN HIGH XPNDR 2<br>STDN LOW XPNDR 1<br>STDN LOW XPNDR 2<br>TDRS XPNDR 1<br>TDRS XPNDR 2  |  | PM C<br>PM A<br>PM C<br>PM A<br>PM C<br>PM A<br>PM C<br>PM A<br>PM C | X2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC | A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/6/S-BD PM MOD1<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD | V74X4791E<br>V74X4789E<br>V74X4789E<br>V74X4787E<br>V74X4787E<br>V74X4788E<br>V74X4788E<br>V74X4786E<br>V74X4786E |
| 4738    | SPD SPM - ON         | 069     | 9/8 OFF<br>18/8 OFF  | SPREAD SPECTRUM DISABLE<br>SPREAD SPECTRUM DISABLE   | 4/14<br>12/14  | BC 1<br>BC 2   | X1/L2/VmnB<br>X2/L3/VmnC   | GCIL ONLY FALSE<br>GCIL ONLY FALSE   | V74X4790E<br>V74X4790E  |
| 4739    | SPD SPM - OFF        | 070     | 9/8 ON<br>18/8 ON  | SPREAD SPECTRUM DISABLE<br>SPREAD SPECTRUM DISABLE   | 4/14<br>12/14  | BC 1<br>BC 2   | X1/L2/VmnB<br>X2/L3/VmnC   | GCIL ONLY FALSE<br>GCIL ONLY FALSE   | V74X4790E<br>V74X4790E  |
| 4740    | FREQ - LOW           | 073     | 4/15 ON<br><br>12/15 ON<br><br>4/7 OFF<br>12/7 OFF<br>* 6/7 ON<br>* 14/7 ON<br>* 6/8 OFF               | XPNDR 1 LOW FREQ<br>S-BD PREAMP XPNDR 1 FREQ LO<br>XPNDR 2 LO FREQ<br>S-BD PREAMP XPNDR 2 FREQ LO<br>XPNDR 1 HI FREQ<br>S-BD PREAMP-XPNDR 2 FREQ HI<br>XPNDR 2 HI FREQ<br>S-BD PREAMP-XPNDR 2 FREQ HI<br>ANTENNA FREQ LO 1<br><br>ANTENNA FREQ LO 2<br><br>ANTENNA FREQ HI 1 | 4/7<br><br>12/7<br><br>4/15<br>12/15<br><br>(4/2 + 4/14 + 12/2 + 12/14)N6/8<br><br>(12/2 + 12/14 + 4/2 + 4/14)N14/8<br><br>(4/2 + 4/14 + 12/2 + 12/14)N6/7 | BC 1<br><br>BC 2<br><br>BC 1<br>BC 2<br><br>BC 1<br>BC 2<br><br>BC 1 | X1/L2/VmnB<br><br>X2/L3/VmnC<br><br>X1/L2/VmnB<br>X2/L3/VmnC<br><br>CNTL BC 1<br>CNTL BC 2<br><br>X1/L2/VmnB<br>X2/L3/VmnC | GCIL ONLY FALSE<br><br>GCIL ONLY FALSE<br><br>GCIL ONLY FALSE<br>GCIL ONLY FALSE<br><br>GCIL ONLY FALSE<br>GCIL ONLY FALSE<br><br>A1L/6/S-BD PM MOD  | V74X4792E<br><br>V74X4792E<br><br>V74X4793E<br>V74X4793E<br><br>V74X4778E<br>V74X4778E<br><br>V74X4779E           |

**Table 11-3. GCIL functions, drivers, and CMD numbers with telemetry, supply voltage sources, ground commands, and DSM numbers (continued)**

| DSM no. | CMD name            | GCL CMD | GCIL driver                                | GCIL function  | Series interlock                 | Mode SRC                     | CMD driver power                                     | PNL/SW no./SW name   | MSID   |
|---------|---------------------|---------|--|--|----------------------------------|------------------------------|--|--|--|
|         |                     | *       | 14/8 OFF                                   | ANTENNA FREQ HI 2  | (4/2 + 4/14 + 12/2 + 12/14)N14/7 | BC 2                         | X2/L3/VmnC<br>X1/L2/VmnB                             | A1L/6/S-BD PM MOD  | V74X4779E  |
| 4741    | FREQ - HI           | 074     | 4/15 OFF                                   | XPNDR 1 LOW FREQ   | 4/16                             | BC 1                         | X1/L2/VmnB   | GCIL ONLY FALSE  | V74X4792E  |
|         |                     |         | 12/15 OFF                                  | S-BD PRAMP-XPNDR 1 FREQ LO<br>XPNDR 2 LOW FREQ<br>S-BD PREAMP-XPNDR 2 FREQ LO      | 12/16                            | BC 2                         | X2/L3/VmnC   | GCIL ONLY FALSE  | V74X4792E  |
|         |                     |         | 4/7 ON                                     | XPNDR 1 HI FREQ<br>S-BD PREAMP-XPNDR 1 FREQ HI                                     | 4/15                             | BC 1                         | X1/L3/VmnC   | GCIL ONLY FALSE  | V74X4793E  |
|         |                     |         | 12/7 ON                                    | XPNDR 1 HI FREQ<br>S-BD PREAMP-XPNDR 2 FREQ HI                                     | 12/15                            | BC 2                         | X2/L3/VmnC   | GCIL ONLY FALSE  | V74X4793E  |
|         |                     | *       | 6/7 OFF                                    | ANTENNA FREQ LO 1  | (4/2 + 4/14 + 12/2 + 12/14)N6/8  | BC 1                         | CNTL BC 1  | GCIL ONLY FALSE  | V74X4778E  |
|         |                     | *       | 14/7 OFF                                   | ANTENNA FREQ LO 2  | (12/2 + 12/14 + 4/2+4/14)N14/8   | BC 2                         | CNTL BC 2  | GCIL ONLY FALSE  | V74X4778E  |
|         |                     | *       | 6/8 ON                                     | ANTENNA FREQ HI 1  | (4/2 + 4/14 + 12/2 + 12/14)N6/7  | BC 1                         | X1/L2/VmnB   | A1L/6/S-BD PM MOD  | V74X4778E  |
|         |                     | *       | 14/8 ON                                    | ANTENNA FREQ HI 2  | 4/2 + 4/14 + 12/2 + 12/14)N14/7  | BC 2                         | X2/L3/VmnC<br>X1/L2/VmnB                             | A1L/6/S-BD PM MOD  | V74X4779E  |
| 4742    | S-BD MODE - T/R     | 075     | 4/16 ON<br>12/16 ON<br>4/8 OFF<br>12/8 OFF | XPNDR T/R #1 MODE<br>XPNDR T/R #2 MODE<br>RCVR XPNDR #1 ONLY<br>RCVR XPNDR #2 ONLY |                                  | BC 1<br>BC 2<br>BC 1<br>BC 2 | X1/L2/VmnB<br>X2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC | GCIL ONLY TRUE<br>GCIL ONLY TRUE<br>GCIL ONLY FALSE<br>GCIL ONLY FALSE   | V74X4779E  |
| 4743    | S-BD MODE - RCV     | 076     | 4/16 OFF<br>12/16 OFF<br>4/8 ON<br>12/8 ON | XPNDR T/R #1 MODE<br>XPNDR T/R #2 MODE<br>RCVR XPNDR #1 ONLY<br>RCVR XPNDR #2 ONLY |                                  | BC 1<br>BC 2<br>BC 1<br>BC 2 | X1/L2/VmnB<br>X2/L3/VmnC<br>X1/L2/VmnB<br>X2/L3/VmnC | GCIL ONLY FALSE<br>GCIL ONLY FALSE<br>GCIL ONLY FALSE<br>GCIL ONLY FALSE | V74X4741E<br>V74X4741E<br>V74X4743E<br>V74X4743E |
| 4744    | S-BD R/L DATA - ENA | 072     | 5/16 ON<br>13/16 ON                        | S-BD R/L DATA ENABLE<br>S-BD R/L DATA ENABLE                                       |                                  | PM A<br>PM C                 | N1/L2/VmnB<br>N2/L3/VmnC                             | A1L/6/S-BD PM MOD<br>A1L/6/S-BD PM MOD                                   | V74X4741E<br>V74X4741E                           |
| 4750    | S-BD PA STBY - 1    | 054     | 4/1 ON                                     | PA-1 STDBY - ON  |                                  | PM A                         | CNTL BC 1  | A1L/12/PWR AMP SBY   | V74X4747E  |



**Table 11-3. GCIL functions, drivers, and CMD numbers with telemetry, supply voltage sources, ground commands, and DSM numbers (continued)**

| DSM no. | CMD name              | GCL CMD | GCIL driver                                | GCIL function  | Series interlock                              | Mode SRC                     | CMD driver power                                     | PNL/SW no./SW name   | MSID   |
|---------|-----------------------|---------|--|--|---|------------------------------|--|--|--|
| 4751    | S-BD PA STBY - OFF    | 055     | 4/1 OFF<br>12/1 OFF                        | PA-1 STDBY - ON<br>PA-2 STDBY - ON   |   | PM A<br>PM C                 | CNTL BC 1<br>CNTL BC 2                               | A1L/12/PWR AMP SBY<br>A1L/12/PWR AMP SBY   | V74X4747E<br>V74X4749E                           |
| 4752    | S-BD PA STBY - 2      | 056     | 12/1 ON                                    | PA-2 STDBY - ON  |   | PM C                         | CNTL BC 2  | A1L/12/PWR AMP SBY   | V74X4749E  |
| 4754    | S-BD PA OPR - 1 ON    | 051     | 4/9 ON<br>12/9 OFF<br>10/3 ON<br>10/8 OFF  | PA #1 NORMAL (PM)<br>PA #2 NORMAL (PM)<br>PA SYS #1<br>PA SYS #2                               | (4/13+12/13)<br>N12/9<br>(4/13+12/13)N4<br>/9 | PM A<br>PM C<br>PM A<br>PM C | PCA 2<br>PCA 3<br>CNTL BC 1<br>CNTL BC 2             | A1L/12/PWR AMP OP<br>A1L/12/PWR AMP OP<br>A1L/12/PWR AMP OP<br>A1L/12/PWR AMP OP     | V74X4784E<br>V74X4785E<br>V74X4747E<br>V74X4749E |
| 4755    | S-BD PA OPR - 1/2 OFF | 052     | 4/9 OFF<br>12/9 OFF                        | PA #1 NORMAL (PM)<br>PA #2 NORMAL (PM)   | (4/13+12/13)<br>N12/9<br>(4/13+12/13)N4<br>/9 | PM A<br>PM C                 | PCA 2<br>PCA 3                                       | A1L/12/PWR AMP OP<br>A1L/12/PWR AMP OP   | V74X4784E<br>V74X4785E                           |
|         |                       |         | 10/3 OFF<br>10/8 OFF                       | PA SYS #1<br>PA SYS #2   |   | PM A<br>PM C                 | CNTL BC 1<br>CNTL BC 2                               | A1L/12/PWR AMP OP<br>A1L/12/PWR AMP OP   | V74X4747E<br>V74X4749E                           |
| 4756    | S-BD PA OPR - 2 ON    | 053     | 4/9 OFF<br>12/9 ON<br>10/3 OFF<br>10/8 ON  | PA #1 NORMAL<br>PA #2 NORMAL<br>PA SYS #1<br>PA SYS #2   | (4/13+12/13)<br>N12/9<br>(4/13+12/13)N4<br>/9 | PM A<br>PM C<br>PM A<br>PM C | PCA 2<br>PCA 3<br>CNTL BC 1<br>CNTL BC 2             | A1L/12/PWR AMP OP<br>A1L/12/PWR AMP OP<br>A1L/12/PWR AMP OP<br>A1L/12/PWR AMP OP     | V74X4784E<br>V74X4785E<br>V74X4747E<br>V74X4749E |
| 4758    | NSP UPLINK - LDR      | 126     | 5/3 OFF<br>13/3 OFF<br>5/11 ON<br>13/11 ON | DATA RATE #1 HIGH RCV<br>DATA RATE #2 HIGH RCV<br>DATA RATE #1 LOW RCV<br>DATA RATE #2 LOW RCV |   | PM A<br>PM C<br>PM A<br>PM C | N1/L2/VmnB<br>N2/L3/VmnC<br>N1/L2/VmnB<br>N2/L3/VmnC | A1L/19/DATA RT RCV<br>A1L/19/DATA RT RCV<br>A1L/19/DATA RT RCV<br>A1L/19/DATA RT RCV | V74X4794E<br>V74X4794E<br>V74X4756E<br>V74X4756E |
| 4759    | NSP UPLINK - HDR      | 127     | 5/3 ON<br>13/3 ON<br>5/11 OFF<br>13/11 OFF | DATA RATE #1 HIGH RCV<br>DATA RATE #2 HIGH RCV<br>DATA RATE #1 LOW RCV<br>DATA RATE #2 LOW RCV |   | PM A<br>PM C<br>PM A<br>PM C | N1/L2/VmnB<br>N2/L3/VmnC<br>N1/L2/VmnB<br>N2/L3/VmnC | A1L/19/DATA RT RCV<br>A1L/19/DATA RT RCV<br>A1L/19/DATA RT RCV<br>A1L/19/DATA RT RCV | V74X4794E<br>V74X4794E<br>V74X4756E<br>V74X4756E |
| 4760    | NSP 1 - ON            | 080     | 5/2 ON<br>13/2 OFF                         | NSP 1 - ON<br>NSP 2 - ON   | NOT 13/2<br>NOT 5/2                           | PM A<br>PM C                 | CNTL BC 1<br>CNTL BC 2                               | A1L/23/NSP PWR<br>A1L/23/NSP PWR   | V74X4760E<br>V74X4761E                           |
| 4761    | NSP 1/2 - OFF         | 081     | 5/2 OFF<br>13/2 OFF                        | NSP 1 - ON<br>NSP 2 - ON   | NOT 13/2<br>NOT 5/2                           | PM A<br>PM C                 | CNTL BC 1<br>CNTL BC 2                               | A1L/23/NSP PWR<br>A1L/23/NSP PWR   | V74X4760E<br>V74X4761E                           |
| 4762    | NSP 2 - ON            | 082     | 5/2 OFF                                    | NSP 1 - ON   | NOT 13/2                                      | PM A                         | CNTL BC 1  | A1L/23/NSP PWR   | V74X4760E  |

**Table 11-3. GCIL functions, drivers, and CMD numbers with telemetry, supply voltage sources, ground commands, and DSM numbers (continued)**

| DSM no. | CMD name            | GCL CMD | GCIL driver                                | GCIL function  | Series interlock | Mode SRC                     | CMD driver power                                     | PNL/SW no./SW name   | MSID   |
|---------|---------------------|---------|--|--|------------------|------------------------------|--|--|--|
|         |                     |         | 13/2 ON                                    | NSP 2 - ON   | NOT 5/2          | PM C                         | CNTL BC 2  | A1L/23/NSP PWR   | V74X4761E  |
| 4763    | DNLINK - LDR        | 084     | 5/9 ON<br>13/9 ON<br>5/1 OFF<br>13/1 OFF   | DATA RATE #1 LOW XMIT<br>DATA RATE #2 LOW XMIT<br>DATA RATE #1 HIGH XMIT<br>DATA RATE #2 HIGH XMIT             |                  | PM A<br>PM C<br>PM A<br>PM C | N1/L2/VmnB<br>N2/L3/VmnC<br>N1/L2/VmnB<br>N2/L3/VmnC | A1L/19/DATA RT XMT<br>A1L/19/DATA RT XMT<br>A1L/18/DATA RT XMT<br>A1L/18/DATA RT XMT | V74X4754E<br>V74X4754E<br>V74X4753E<br>V74X4753E |
| 4764    | DNLINK - HDR        | 083     | 5/1 ON<br>13/1 ON<br>5/9 OFF<br>13/9 OFF   | DATA RATE #1 HIGH XMIT<br>DATA RATE #2 HIGH XMIT<br>DATA RATE #1 LOW XMIT<br>DATA RATE #2 LOW XMIT             |                  | PM A<br>PM C<br>PM A<br>PM C | N1/L2/VmnB<br>N2/L3/VmnC<br>N1/L2/VmnB<br>N2/L3/VmnC | A1L/18/DATA RT XMT<br>A1L/18/DATA RT XMT<br>A1L/18/DATA RT XMT<br>A1L/18/DATA RT XMT | V74X4753E<br>V74X4753E<br>V74X4754E<br>V74X4754E |
| 4765    | XPNDR U/L FLTR-NAR  | 086     | 4/4 OFF<br>12/4 OFF<br>4/12 ON<br>12/12 ON | XPNDR 1 U/L FLTR - WIDE<br>XPNDR 2 U/L FLTR - WIDE<br>XPNDR 1 U/L FLTR - NAR<br>XPNDR 2 U/L FLTR - NAR         |                  | PM A<br>PM C<br>PM A<br>PM C | X1/L2/VmnB<br>X1/L3/VmnC<br>X1/L2/VmnB<br>X1/L3/VmnC | A1L/19/DATA RT RCV<br>A1L/19/DATA RT RCV<br>A1L/19/DATA RT RCV<br>A1L/19/DATA RT RCV |  |
| 4766    | XPNDR U/L FLTR-WIDE | 085     | 4/4 ON<br>12/4 ON<br>4/12 OFF<br>12/12 OFF | XPNDR 1 U/L FLTR - WIDE<br>XPNDR 2 U/L FLTR - WIDE<br>XPNDR 1 U/L FLTR - NAR<br>XPNDR 2 U/L FLTR - NAR         |                  | PM A<br>PM C<br>PM A<br>PM C | X1/L2/VmnB<br>X1/L3/VmnC<br>X1/L2/VmnB<br>X1/L3/VmnC | A1L/19/DATA RT RCV<br>A1L/19/DATA RT RCV<br>A1L/19/DATA RT RCV<br>A1L/19/DATA RT RCV |  |
| 4745    | RANGING - OFF       | 120     | 9/16 ON<br>18/16 ON                        | RANGING DISABLE<br>RANGING DISABLE   |                  | PM A<br>PM C                 | X1/L2/VmnB<br>X1/L3/VmnC                             | A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD   | V74X4791E<br>V74X4791E                           |
| 4746    | RANGING - ON        | 119     | 9/16 OFF<br>18/16 OFF                      | RANGING DISABLE<br>RANGING DISABLE   |                  | PM A<br>PM C                 | X1/L2/VmnB<br>X1/L3/VmnC                             | A1L/ 6/S-BD PM MOD<br>A1L/ 6/S-BD PM MOD   | V74X4791E<br>V74X4791E                           |
| 4767    | DATA SOURCE - KU    | 087     | 5/10 ON<br>13/10 ON<br>5/8 OFF<br>13/8 OFF | UPLK DATA SOURCE #1 KU-BD<br>UPLK DATA SOURCE #2 KU-BD<br>UPLK DATA SOURCE #1 S-BD<br>UPLK DATA SOURCE #2 S-BD |                  | PM A<br>PM C<br>PM A<br>PM C | N1/L2/VmnB<br>N2/L3/VmnB<br>N1/L2/VmnB<br>N2/L3/VmnC | A1L/20/UPLK DATA<br>A1L/20/UPLK DATA<br>A1L/20/UPLK DATA<br>A1L/20/UPLK DATA         | V74X4758E<br>V74X4758E<br>V74X4795E<br>V74X4795E |
| 4768    | DATA SOURCE - S     | 088     | 5/10 OFF<br>13/10 OFF<br>5/8 ON<br>13/8 ON | UPLK DATA SOURCE #1 KU-BD<br>UPLK DATA SOURCE #2 KU-BD<br>UPLK DATA SOURCE #1 S-BD<br>UPLK DATA SOURCE #2 S-BD |                  | PM A<br>PM C<br>PM A<br>PM C | N1/L2/VmnB<br>N2/L3/VmnC<br>N1/L2/VmnB<br>N2/L3/VmnC | A1L/20/UPLK DATA<br>A1L/20/UPLK DATA<br>A1L/20/UPLK DATA<br>A1L/20/UPLK DATA         | V74X4758E<br>V74X4758E<br>V74X4795E<br>V74X4795E |
| 4770    | UPLINK CODING - ON  | 089     | 5/4 ON<br>13/4 ON<br>5/12 OFF<br>13/12 OFF | #1 CODING RCV ON<br>#2 CODING RCV ON<br>#1 CODING RCV OFF (NSP)<br>#2 CODING RCV OFF (NSP)                     |                  | PM A<br>PM C<br>PM A<br>PM C | N1/L2/VmnB<br>N2/L3/VmnC<br>N1/L2/VmnB<br>N2/L3/VmnC | A1L/22/CODE RCV<br>A1L/22/CODE RCV<br>A1L/22/CODE RCV<br>A1L/22/CODE RCV             | V74X4796E<br>V74X4796E<br>V74X4752E<br>V74X4752E |
| 4771    | UPLINK CODING - OFF | 090     | 5/4 OFF                                    | #1 CODING RCV OFF (NSP)  |                  | PM A                         | N1/L2/VmnB   | A1L/22/CODE RCV  | V74X4796E  |

**Table 11-3. GCIL functions, drivers, and CMD numbers with telemetry, supply voltage sources, ground commands, and DSM numbers (continued)**

| DSM no. | CMD name            | GCL CMD | GCIL driver                                  | GCIL function  | Series interlock   | Mode SRC                     | CMD driver power                                     | PNL/SW no./SW name   | MSID   |
|---------|---------------------|---------|--|--|--|------------------------------|--|--|--|
|         |                     |         | 13/4 OFF<br>5/12 ON<br>13/12 ON              | #2 CODING RCV OFF (NSP)<br>#1 CODING RCV OFF (NSP)<br>#2 CODING RCV OFF (NSP)                                |  | PM C<br>PM A<br>PM C         | N2/L3/VmnC<br>N1/L2/VmnB<br>N2/L3/VmnC               | A1L/22/CODE RCV<br>A1L/22/CODE RCV<br>A1L/22/CODE RCV                                | V74X4796E<br>V74X4752E<br>V74X4752E              |
| 4772    | DNLINK CODING - ON  | 091     | 5/5 ON<br>13/5 ON<br>5/13 OFF<br>13/13 OFF   | #1 CODING XMIT ON (NSP)<br>#2 CODING XMIT ON (NSP)<br>#1 CODING XMIT OFF (NSP)<br>#2 CODING XMIT OFF (NSP)   |  | PM A<br>PM C<br>PM A<br>PM C | N1/L2/VmnB<br>N2/L3/VmnC<br>N1/L2/VmnB<br>N2/L3/VmnC | A1L/21/CODE XMIT<br>A1L/21/CODE XMIT<br>A1L/21/CODE XMIT<br>A1L/21/CODE XMIT         | V74X4797E<br>V74X4797E<br>V74X4751E<br>V74X4751E |
| 4773    | DNLINK CODING - OFF | 092     | 5/5 OFF<br>13/5 OFF<br>5/13 ON<br>13/13 ON   | #1 CODING RCV ON (NSP)<br>#2 CODING RCV ON (NSP)<br>(NSP) #1 CODING XMIT OFF<br>(NSP) #2 CODING XMIT OFF     |  | PM A<br>PM C<br>PM A<br>PM C | N1/L2/VmnB<br>N2/L3/VmnC<br>N1/L2/VmnB<br>N2/L3/VmnC | A1L/21/CODE XMIT<br>A1L/21/CODE XMIT<br>A1L/21/CODE XMIT<br>A1L/21/CODE XMIT         | V74X4797E<br>V74X4797E<br>V74X4751E<br>V74X4751E |
| 4774    | RCDR VOICE ½ - ON   | 094     | 5/15 OFF<br>13/15 OFF<br>5/7 ON<br>13/7 ON   | DATA VOICE CHAN ½ OFF<br>DATA VOICE CHAN ½ OFF<br>DATA-VOICE #1 CHAN ½ - ON<br>DATA-VOICE #1 CHAN ½ - ON     |  | PM A<br>PM C<br>PM A<br>PM C | N1/L2/VmnB<br>N2/L3/VmnC<br>N1/L2/VmnB<br>N2/L3/VmnC | A1L/15/V RCD SEL 1<br>A1L/15/V RCD SEL 1<br>A1L/15/V RCD SEL 1<br>A1L/15/V RCD SEL 1 | V74X4798E<br>V74X4798E<br>V74X4799E<br>V74X4799E |
| 4775    | RCDR VOICE ½ - OFF  | 093     | 5/15 ON<br>13/15 ON<br>5/7 OFF<br>13/7 OFF   | DATA VOICE CHAN ½ - OFF<br>DATA VOICE CHAN ½ - OFF<br>DATA-VOICE #1 CHAN ½ - ON<br>DATA-VOICE #2 CHAN ½ - ON |  | PM A<br>PM C<br>PM A<br>PM C | N1/L2/VmnB<br>N2/L3/VmnC<br>N1/L2/VmnB<br>N2/L3/VmnC | A1L/15/V RCD SEL 1<br>A1L/15/V RCD SEL 1<br>A1L/15/V RCD SEL 1<br>A1L/15/V RCD SEL 1 | V74X4798E<br>V74X4798E<br>V74X4799E<br>V74X4799E |
| 4780    | FM SYSTEM 1 - ON    | 101     | 10/1 ON<br>10/2 ON<br>10/6 OFF<br>10/7 OFF   | FM SIG PROG #1 ON<br>FM XMTR #1 ON<br>FM SIG PROC #2 ON<br>FM XMTR #2 ON                                     | N(10/6+10/7)<br>N(10/6+10/7)<br>N(10/1+10/2)<br>N(10/1+10/2) | FM A<br>FM A<br>FM C<br>FM C | CNTL BC 1<br>CNTL BC 1<br>CNTL BC 2<br>CNTL BC 2     | A1R/ 3/S-BD FM PWR<br>A1R/ 3/S-BD FM PWR<br>A1R/ 3/S-BD FM PWR<br>A1R/ 3/S-BD FM PWR | V74X6120E<br>V74X6121E                           |
| 4781    | FM SYSTEM ½ - OFF   | 102     | 10/1 OFF<br>10/2 OFF<br>10/6 OFF<br>10/7 OFF | FM SIG PROC #1 ON<br>FM XMTR #1 ON<br>FM SI PROC #2 ON<br>FM XMTR #2 ON                                      | N(10/6+10/7)<br>N(10/6+10/7)<br>N(10/1+10/2)<br>N(10/1+10/2) | FM A<br>FM A<br>FM C<br>FM C | CNTL BC 1<br>CNTL BC 1<br>CNTL BC 2<br>CNTL BC 2     | A1R/ 3/S-BD FM PWR<br>A1R/ 3/S-BD FM PWR<br>A1R/ 3/S-BD FM PWR<br>A1R/ 3/S-BD FM PWR | V74X6120E<br>V74X6121E                           |
| 4782    | FM SYSTEM 2 - ON    | 103     | 10/6 ON<br>10/7 ON<br>10/1 OFF<br>10/2 OFF   | FM SIG PROC #2 ON<br>FM XMTR #2 ON<br>FM SI PROC #1 ON<br>FM XMTR #1 ON                                      | N(10/1+10/2)<br>N(10/1+10/2)<br>N(10/6+10/7)<br>N(10/6+10/7) | FM C<br>FM C<br>FM A<br>FM A | CNTL BC 2<br>CNTL BC 2<br>CNTL BC 1<br>CNTL BC 1     | A1R/ 3/S-BD FM PWR<br>A1R/ 3/S-BD FM PWR<br>A1R/ 3/S-BD FM PWR<br>A1R/ 3/S-BD FM PWR | V74X6121E<br>V74X6120E                           |
| 4783    | FM - OFF            | 104     | 6/1 OFF<br>6/4 OFF<br>6/5 OFF<br>6/10 OFF    | FM #1 P/L ANALOG<br>FM #1 DOD ENCODER<br>FM #1 TV<br>FM #1 MMU2  |  | FM A<br>FM A<br>FM A<br>FM A | F1/L2/VmnB<br>F1/L2/VmnB<br>F1/L2/VmnB<br>F1/L2/VmnB | A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE | V74X4804E<br>V74X4805E<br>V74X4806E<br>V74X3446E |

**Table 11-3. GCIL functions, drivers, and CMD numbers with telemetry, supply voltage sources, ground commands, and DSM numbers (continued)**

| DSM no. | CMD name      | GCL CMD | GCIL driver   | GCIL function  | Series interlock | Mode SRC   | CMD driver power   | PNL/SW no./SW name   | MSID   |
|---------|---------------|---------|---|--|------------------|--|--|--|--|
|         |               |         | 6/11 OFF<br>6/12 OFF<br>6/13 OFF<br>14/1 OFF<br>14/4 OFF<br>14/5 OFF<br>14/10 OFF<br>14/11 OFF<br>14/12 OFF<br>14/13 OFF  | FM #1 MAIN ENGINE<br>FM #1 MMU1<br>FM #1 P/L DIGITAL<br>FM #2 P/L ANALOG<br>FM #2 DOD ENCODER<br>FM #2 TV<br>FM #2 MMU2<br>FM #2 MAIN ENGINE<br>FM #2 MMU1<br>FM #2 P/L DIGITAL  |                  | FM A<br>FM A<br>FM A<br>FM C<br>FM C<br>FM C<br>FM C<br>FM C<br>FM C<br>FM C                                 | F1/L2/VmnB<br>F1/L2/VmnB<br>F1/L2/VmnB<br>F2/L3/VmnC<br>F2/L3/VmnC<br>F2/L3/VmnC<br>F2/L3/VmnC<br>F2/L3/VmnC<br>F2/L3/VmnC<br>F2/L3/VmnC   | A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE   | V74X4801E<br>V74X3447E<br>V74X4803E<br>V74X4804E<br>V74X4805E<br>V74X4806E<br>V74X3446E<br>V74X4801E<br>V74X3447E<br>V74X4803E   |
| 4727    | FM - MMU2     | 105     | 6/10 ON<br>14/10 ON<br>6/1 OFF<br>14/1 OFF<br>6/4 OFF<br>14/4 OFF<br>6/5 OFF<br>14/5 OFF<br>6/11 OFF<br>14/11 OFF<br>6/12 OFF<br>14/12 OFF<br>6/1 OFF<br>14/1 OFF   | FM #1 MMU2<br>FM #2 MMU2<br>FM #1 P/L ANALOG<br>FM #2 P/L ANALOG<br>FM #1 DOD ENCODER<br>FM #2 DOD ENCODER<br>FM #1 TV<br>FM #2 TV<br>FM #1 MAIN ENGINE<br>FM #2 MAIN ENGINE<br>FM #1 MMU1<br>FM #2 MMU1<br>FM #1 P/L DIGITAL<br>FM #2 P/L DIGITAL |                  | FM A<br>FM C<br>FM A<br>FM C<br>FM A<br>FM C<br>FM A<br>FM C<br>FM A<br>FM C<br>FM A<br>FM C<br>FM A<br>FM C | F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnB<br>F1/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L3/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC | A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE | V74X3446E<br>V74X3446E<br>V74X4804E<br>V74X4801E<br>V74X4805E<br>V74X4805E<br>V74X4806E<br>V74X4806E<br>V74X4801E<br>V74X4801E<br>V74X3447E<br>V74X3447E<br>V74X4803E<br>V74X4803E |
| 4785    | FM - MAIN ENG | 106     | 6/11 ON<br>14/11 ON<br>6/1 OFF<br>14/1 OFF<br>6/4 OFF<br>14/4 OFF<br>6/5 OFF<br>14/5 OFF<br>6/10 OFF<br>14/10 OFF<br>6/12 OFF<br>14/12 OFF<br>6/13 OFF<br>14/13 OFF | FM #1 MAIN ENGINE<br>FM #2 MAIN ENGINE<br>FM #1 P/L ANALOG<br>FM #2 P/L ANALOG<br>FM #1 DOD ENCODER<br>FM #2 DOD ENCODER<br>FM #1 TV<br>FM #2 TV<br>FM #1 MMU2<br>FM #2 MMU2<br>FM #1 MMU1<br>FM #2 MMU1<br>FM #1 P/L DIGITAL<br>FM #2 P/L DIGITAL |                  | FM A<br>FM C<br>FM A<br>FM C<br>FM A<br>FM C<br>FM A<br>FM C<br>FM A<br>FM C<br>FM A<br>FM C<br>FM A<br>FM C | F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC | A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE | V74X4801E<br>V74X4801E<br>V74X4804E<br>V74X4804E<br>V74X4805E<br>V74X4805E<br>V74X4806E<br>V74X4806E<br>V74X3446E<br>V74X3446E<br>V74X3447E<br>V74X3447E<br>V74X4803E<br>V74X4803E |
| 4728    | FM - MMU1     | 107     | 6/12 ON<br>14/12 ON<br>6/1 OFF  | FM #1 MMU1<br>FM #2 MMU1<br>FM #1 P/L ANALOG   |                  | FM A<br>FM C<br>FM A   | F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnB   | A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE   | V74X3447E<br>V74X3447E<br>V74X4804E  |

**Table 11-3. GCIL functions, drivers, and CMD numbers with telemetry, supply voltage sources, ground commands, and DSM numbers (continued)**

| DSM no. | CMD name     | GCL CMD | GCIL driver   | GCIL function  | Series interlock | Mode SRC   | CMD driver power   | PNL/SW no./SW name   | MSID   |
|---------|--------------|---------|---|--|------------------|--|--|--|--|
|         |              |         | 14/1 OFF<br>6/4 OFF<br>14/4 OFF<br>6/5 OFF<br>14/5 OFF<br>6/10 OFF<br>14/10 OFF<br>6/11 OFF<br>14/11 OFF<br>6/13 OFF<br>14/13 OFF                                   | FM #2 P/L ANALOG<br>FM #1 DOD ENCODER<br>FM #2 DOD ENCODER<br>FM #1 TV<br>FM #2 TV<br>FM #1 MMU2<br>FM #2 MMU2<br>FM #1 MAIN ENGINE<br>FM #2 MAIN ENGINE<br>FM #1 P/L DIGITAL<br>FM #2 P/L DIGITAL   |                  | FM C<br>FM A<br>FM C<br>FM A<br>FM C<br>FM A<br>FM C<br>FM A<br>FM C<br>FM A<br>FM C                         | F2/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC   | A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE   | V74X4804E<br>V74X4805E<br>V74X4805E<br>V74X4806E<br>V74X4806E<br>V74X3446E<br>V74X3446E<br>V74X4801E<br>V74X4801E<br>V74X4803E<br>V74X4803E  |
| 4787    | FM - PL DIGI | 108     | 6/13 ON<br>14/13 ON<br>6/1 OFF<br>14/1 OFF<br>6/4 OFF<br>14/4 OFF<br>6/5 OFF<br>14/5 OFF<br>6/10 OFF<br>14/10 OFF<br>6/11 OFF<br>14/11 OFF<br>6/12 OFF<br>14/12 OFF | FM #1 P/L DIGITAL<br>FM #2 P/L DIGITAL<br>FM #1 P/L ANALOG<br>FM #2 P/L ANALOG<br>FM #1 DOD ENCODER<br>FM #2 DOD ENCODER<br>FM #1 TV<br>FM #2 TV<br>FM #1 MMU2<br>FM #2 MMU2<br>FM #1 MAIN ENGINE<br>FM #2 MAIN ENGINE<br>FM #1 MMU1<br>FM #2 MMU1 |                  | FM A<br>FM C<br>FM A<br>FM C<br>FM A<br>FM C<br>FM A<br>FM C<br>FM A<br>FM C<br>FM A<br>FM C<br>FM A<br>FM C | F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnC<br>F2/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC | A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE | V74X4803E<br>V74X4803E<br>V74X4804E<br>V74X4804E<br>V74X4805E<br>V74X4805E<br>V74X4806E<br>V74X4806E<br>V74X3446E<br>V74X3446E<br>V74X4801E<br>V74X4801E<br>V74X3447E<br>V74X3447E |
| 4788    | FM - PL ANLG | 109     | 6/1 ON<br>14/1 ON<br>6/4 OFF<br>14/4 OFF<br>6/5 OFF<br>14/5 OFF<br>6/10 OFF<br>14/10 OFF<br>6/11 OFF<br>14/11 OFF<br>6/12 OFF<br>14/12 OFF<br>6/13 OFF<br>14/13 OFF | FM #1 P/L ANALOG<br>FM #2 P/L ANALOG<br>FM #1 DOD ENCODER<br>FM #2 DOD ENCODER<br>FM #1 TV<br>FM #2 TV<br>FM #1 MMU2<br>FM #2 MMU2<br>FM #1 MAIN ENGINE<br>FM #2 MAIN ENGINE<br>FM #1 MMU1<br>FM #2 MMU1<br>FM #1 P/L DIGITAL<br>FM #2 P/L DIGITAL |                  | FM A<br>FM C<br>FM A<br>FM C<br>FM A<br>FM C<br>FM A<br>FM C<br>FM A<br>FM C<br>FM A<br>FM C<br>FM A<br>FM C | F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC<br>F1/L2/VmnB<br>F2/L3/VmnC | A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE<br>A1R/ 4/FM DTA SRCE | V74X4804E<br>V74X4804E<br>V74X4805E<br>V74X4805E<br>V74X4806E<br>V74X4806E<br>V74X3446E<br>V74X3446E<br>V74X4801E<br>V74X4801E<br>V74X3447E<br>V74X3447E<br>V74X4803E<br>V74X4803E |

**Table 11-3. GCIL functions, drivers, and CMD numbers with telemetry, supply voltage sources, ground commands, and DSM numbers (continued)**

| DSM no. | CMD name         | GCL CMD | GCIL driver | GCIL function     | Series interlock | Mode SRC | CMD driver power | PNL/SW no./SW name | MSID      |
|---------|------------------|---------|-------------|-------------------|------------------|----------|------------------|--------------------|-----------|
| 4789    | FM - DOD         | 110     | 6/4 ON      | FM #1 DOD ENCODER |                  | FM A     | F1/L2/VmnB       | A1R/ 4/FM DTA SRCE | V74X4805E |
|         |                  |         | 14/4 ON     | FM #2 DOD ENCODER |                  | FM C     | F2/L3/VmnC       | A1R/ 4/FM DTA SRCE | V74X4805E |
|         |                  |         | 6/1 OFF     | FM #1 P/L ANALOG  |                  | FM A     | F1/L2/VmnB       | A1R/ 4/FM DTA SRCE | V74X4804E |
|         |                  |         | 14/1 OFF    | FM #2 P/L ANALOG  |                  | FM C     | F2/L3/VmnC       | A1R/ 4/FM DTA SRCE | V74X4804E |
|         |                  |         | 6/5 OFF     | FM #1 TV          |                  | FM A     | F1/L2/VmnB       | A1R/ 4/FM DTA SRCE | V74X4806E |
|         |                  |         | 14/5 OFF    | FM #2 TV          |                  | FM C     | F2/L3/VmnC       | A1R/ 4/FM DTA SRCE | V74X4806E |
|         |                  |         | 6/10 OFF    | FM #1 MMU2        |                  | FM A     | F1/L2/VmnB       | A1R/ 4/FM DTA SRCE | V74X3446E |
|         |                  |         | 14/10 OFF   | FM #2 MMU2        |                  | FM C     | F2/L3/VmnC       | A1R/ 4/FM DTA SRCE | V74X3446E |
|         |                  |         | 6/11 OFF    | FM #1 MAIN ENGINE |                  | FM A     | F1/L2/VmnB       | A1R/ 4/FM DTA SRCE | V74X4801E |
|         |                  |         | 14/11 OFF   | FM #2 MAIN ENGINE |                  | FM C     | F2/L3/VmnC       | A1R/ 4/FM DTA SRCE | V74X4801E |
|         |                  |         | 6/12 OFF    | FM #1 MMU1        |                  | FM A     | F1/L2/VmnB       | A1R/ 4/FM DTA SRCE | V74X3447E |
|         |                  |         | 14/12 OFF   | FM #2 MMU1        |                  | FM C     | F2/L3/VmnB       | A1R/ 4/FM DTA SRCE | V74X3447E |
|         |                  |         | 6/13 OFF    | FM #1 P/L DIGITAL |                  | FM A     | F1/L2/VmnB       | A1R/ 4/FM DTA SRCE | V74X4803E |
|         |                  |         | 14/13 OFF   | FM #2 P/L DIGITAL |                  | FM C     | F2/L3/VmnC       | A1R/ 4/FM DTA SRCE | V74X4803E |
| 4790    | FM - TV          | 111     | 6/5 ON      | FM #1 TV          |                  | FM A     | F1/L2/VmnB       | A1R/ 4/FM DTA SRCE | V74X4806E |
|         |                  |         | 14/5 ON     | FM #2 TV          |                  | FM C     | F2/L3/VmnC       | A1R/ 4/FM DTA SRCE | V74X4806E |
|         |                  |         | 6/1 OFF     | FM #1 P/L ANALOG  |                  | FM A     | F1/L2/VmnB       | A1R/ 4/FM DTA SRCE | V74X4804E |
|         |                  |         | 14/1 OFF    | FM #2 P/L ANALOG  |                  | FM C     | F2/L3/VmnC       | A1R/ 4/FM DTA SRCE | V74X4804E |
|         |                  |         | 6/4 OFF     | FM #1 DOD ENCODER |                  | FM A     | F1/L2/VmnB       | A1R/ 4/FM DTA SRCE | V74X4805E |
|         |                  |         | 14/4 OFF    | FM #2 DOD ENCODER |                  | FM C     | F2/L3/VmnC       | A1R/ 4/FM DTA SRCE | V74X4805E |
|         |                  |         | 6/10 OFF    | FM #1 MMU2        |                  | FM A     | F1/L2/VmnB       | A1R/ 4/FM DTA SRCE | V74X3446E |
|         |                  |         | 14/10 OFF   | FM #2 MMU2        |                  | FM C     | F2/L3/VmnC       | A1R/ 4/FM DTA SRCE | V74X3446E |
|         |                  |         | 6/11 OFF    | FM #1 MAIN ENGINE |                  | FM A     | F1/L2/VmnB       | A1R/ 4/FM DTA SRCE | V74X4801E |
|         |                  |         | 14/11 OFF   | FM #2 MAIN ENGINE |                  | FM C     | F2/L3/VmnC       | A1R/ 4/FM DTA SRCE | V74X4801E |
|         |                  |         | 6/12 OFF    | FM #1 MMU1        |                  | FM A     | F1/L2/VmnB       | A1R/ 4/FM DTA SRCE | V74X3447E |
|         |                  |         | 14/12 OFF   | FM #2 MMU1        |                  | FM C     | F2/L3/VmnC       | A1R/ 4/FM DTA SRCE | V74X3447E |
|         |                  |         | 6/13 OFF    | FM #1 P/L DIGITAL |                  | FM A     | F1/L2/VmnB       | A1R/ 4/FM DTA SRCE | V74X4803E |
|         |                  |         | 14/13 OFF   | FM #2 P/L DIGITAL |                  | FM C     | F2/L3/VmnC       | A1R/ 4/FM DTA SRCE | V74X4803E |
| 4800    | PL SYSTEM 1 - ON | 131     | 10/5 ON     | P/L SYS #1        | NOT 10/10        | PL A     | CNTL BC 1        | A1L/13/PL SYS PWR  |           |
|         |                  |         | 10/10 OFF   | P/L SYS #2        |                  | PL C     | CNTL BC 2        | A1L/13/PL SYS PWR  |           |
| 4801    | PL SYSTEM - OFF  | 133     | 10/5 OFF    | P/L SYS #1        | NOT 10/10        | PL A     | CNTL BC 1        | A1L/13/PL SYS PWR  |           |
|         |                  |         | 10/10 OFF   | P/L SYS #2        |                  | PL C     | CNTL BC 2        | A1L/13/PL SYS PWR  |           |
| 4802    | PL SYSTEM 2 - ON | 132     | 10/10 ON    | P/L SYS #2        | NOT 10/5         | PL C     | CNTL BC 2        | A1L/13/PL SYS PWR  |           |
|         |                  |         | 10/5 OFF    | P/L SYS #1        |                  | PL A     | CNTL BC 1        | A1L/13/PL SYS PWR  |           |
| 4803    | PL PSP - SEL     | 134     | 7/6 ON      | P/L SIG PROC #1   | 10/5             | PL A     | CNTL BC 1        | A1L/14/PWR SELECT  | V74X4890E |
|         |                  |         | 15/6 ON     | P/L SIG PROC #2   |                  | PL C     | CNTL BC 2        | A1L/14/PWR SELECT  | V74X4891E |
|         |                  |         | 8/7 OFF     | P/L INTERR #1     |                  | PL A     | CNTL BC 1        | A1L/14/PWR SELECT  | V74X4323E |

**Table 11-3. GCIL functions, drivers, and CMD numbers with telemetry, supply voltage sources, ground commands, and DSM numbers (continued)**

| DSM no. | CMD name             | GCL CMD | GCIL driver   | GCIL function  | Series interlock               | Mode SRC                                     | CMD driver power   | PNL/SW no./SW name   | MSID   |
|---------|----------------------|---------|---|--|--------------------------------|--|--|--|--|
|         |                      |         | 16/7 OFF  | P/L INTERR #2  | 10/10                          | PL C   | CNTL BC 2  | A1L/14/PWR SELECT  | V74X4353E  |
| 4804    | PL INTGR - SEL       | 135     | 8/7 ON<br>16/7 ON<br>7/6 OFF<br>15/6 OFF                        | P/L INTERR #1<br>P/L INTERR #2<br>P/L SIG PROC #1<br>P/L SIG PROC #2   | 10/5<br>10/10<br>10/5<br>10/10 | PL A<br>PL C<br>PL A<br>PL C                 | CNTL BC 1<br>CNTL BC 2<br>CNTL BC 1<br>CNTL BC 2                                 | A1L/14/PWR SELECT<br>A1L/14/PWR SELECT<br>A1L/14/PWR SELECT<br>A1L/14/PWR SELECT   | V74X4323E<br>V74X4353E<br>V74X4890E<br>V74X4891E                           |
| 4805    | PL PSP/INTGR - SEL   | 136     | 7/6 ON<br>15/6 ON<br>8/7 ON<br>16/7 ON                          | P/L SIG PROC #1<br>P/L SIG PROC #2<br>P/L INTERR #1<br>P/L INTERR #2   | 10/5<br>10/10<br>10/5<br>10/10 | PL A<br>PL C<br>PL A<br>PL C                 | CNTL BC 1<br>CNTL BC 2<br>CNTL BC 1<br>CNTL BC 2                                 | A1L/14/PWR SELECT<br>A1L/14/PWR SELECT<br>A1L/14/PWR SELECT<br>A1L/14/PWR SELECT   | V74X4890E<br>V74X4891E<br>V74X4323E<br>V74X4325E                           |
| 4806    | PL XMTR PWR OUT - HI | 137     | 7/3 ON<br>15/3 ON<br>7/4 OFF<br>15/4 OFF<br>7/5 OFF<br>15/5 OFF | #1 RF POWER HI<br>#2 RF POWER HI<br>#1 RF POWER MED<br>#2 RF PWER MED<br>#1 RF POWER LOW<br>#2 RF POWER LOW  |                                | PL A<br>PL C<br>PL A<br>PL C<br>PL A<br>PL C | PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC | A1L/4/SPL XMTR PWR<br>A1L/4/SPL XMTR PWR<br>A1L/4/SPL XMTR PWR<br>A1L/4/SPL XMTR PWR<br>A1L/4/SPL XMTR PWR<br>A1L/4/SPL XMTR PWR | V74X4313E<br>V74X4313E<br>V74X4314E<br>V74X4314E<br>V74X4315E<br>V74X4315E |
| 4807    | PL XMTR PWR OUT - MD | 138     | 7/4 ON<br>15/4 ON<br>7/3 OFF<br>15/3 OFF<br>7/5 OFF<br>15/5 OFF | #1 RF POWER MED<br>#2 RF POWER MED<br>#1 RF POWER HI<br>#2 RF POWER HI<br>#1 RF POWER LOW<br>#2 RF POWER LOW |                                | PL A<br>PL C<br>PL A<br>PL C<br>PL A<br>PL C | PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC | A1L/4/SPL XMTR PWR<br>A1L/4/SPL XMTR PWR<br>A1L/4/SPL XMTR PWR<br>A1L/4/SPL XMTR PWR<br>A1L/4/SPL XMTR PWR<br>A1L/4/SPL XMTR PWR | V74X4314E<br>V74X4314E<br>V74X4313E<br>V74X4313E<br>V74X4315E<br>V74X4315E |
| 4808    | PL XMTR PWR OUT - LO | 139     | 7/5 ON<br>15/5 ON   | #1 RF POWER LOW<br>#2 RF POWER LOW   |                                | PL A<br>PL C                                 | PI/L2/VmnB<br>PI/L3/VmnC   | A1L/4/SPL XMTR PWR<br>A1L/4/SPL XMTR PWR   | V74X4315E<br>V74X4315E   |

**Table 11-3. GCIL functions, drivers, and CMD numbers with telemetry, supply voltage sources, ground commands, and DSM numbers (continued)**

| DSM no. | CMD name             | GCL CMD | GCIL driver                                  | GCIL function  | Series interlock | Mode SRC                     | CMD driver power                                     | PNL/SW no./SW name   | MSID   |
|---------|----------------------|---------|--|--|------------------|------------------------------|--|--|--|
|         |                      |         | 7/3 OFF<br>15/3 OFF<br>7/4 OFF<br>15/4 OFF   | #1 RF POWER HI<br>#2 RF POWER HI<br>#1 RF POWER MED<br>#2 RF POWER MED   |                  | PL A<br>PL C<br>PL A<br>PL C | PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC | A1L/4/SPL XMTR PWR<br>A1L/4/SPL XMTR PWR<br>A1L/4/SPL XMTR PWR<br>A1L/4/SPL XMTR PWR | V74X4313E<br>V74X4313E<br>V74X4314E<br>V74X4314E |
| 4812    | PL PSP CMD OUT - INT | 143     | 7/9 ON<br>15/9 ON<br>7/10 OFF<br>15/10 OFF   | PSP COMMAND OUT INTERR #1<br>PSP COMMAND OUT INTERR #2<br>PSP COMMAND OUT P/L UMB #1<br>PSP COMMAND OUT P/L UMB #2 |                  | PL A<br>PL C<br>PL A<br>PL C | SP/L2/VmnB<br>SP/L3/VmnC<br>SP/L2/VmnB<br>SP/L3/VmnC | A1L/15 PSP CMD<br>A1L/15 PSP CMD<br>A1L/15 PSP CMD<br>A1L/15 PSP CMD                 | V74X4894E<br>V74X4894E<br>V74X4895E<br>V74X4895E |
| 4813    | PL PSP CMD OUT - UMB | 144     | 7/10 ON<br>15/10 ON<br>7/9 OFF<br>15/9 OFF   | PSP COMMAND OUT P/L UMB #1<br>PSP COMMAND OUT P/L UMB #2<br>PSP COMMAND OUT INTER #1<br>PSP COMMAND OUT INTERR #2  |                  | PL A<br>PL C<br>PL A<br>PL C | SP/L2/VmnB<br>SP/L3/VmnC<br>SP/L2/VmnB<br>SP/L3/VmnC | A1L/15 PSP CMD<br>A1L/15 PSP CMD<br>A1L/15 PSP CMD<br>A1L/15 PSP CMD                 | V74X4895E<br>V74X4895E<br>V74X4894E<br>V74X4894E |
| 4814    | PL ANT POL - LT CIRC | 145     | 7/11 ON<br>15/11 ON<br>7/12 OFF<br>15/12 OFF | P/L ANT #1 LH CIRCULAR<br>P/L ANT #2 LH CIRCULAR<br>P/L ANT #1 RH CIRCULAR<br>P/L ANT #2 RH CIRCULAR               |                  | PL A<br>PL C<br>PL A<br>PL C | PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC | A1L/2/ANT POLAR<br>A1L/2/ANT POLAR<br>A1L/2/ANT POLAR<br>A1L/2/ANT POLAR             | V74X5603E<br>V74X5604E<br>V74X5604E<br>V74X5603E |
| 4815    | PL ANG POL - RT CIRC | 146     | 7/12 ON<br>15/12 ON<br>7/11 OFF<br>15/11 OFF | P/L ANT #1 RH CIRCULAR<br>P/L ANT #2 RH CIRCULAR<br>P/L ANT #1 LH CIRCULAR<br>P/L ANT #2 LH CIRCULAR               |                  | PL A<br>PL C<br>PL A<br>PL C | PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC | A1L/2/ANT POLAR<br>A1L/2/ANT POLAR<br>A1L/2/ANT POLAR<br>A1L/2/ANT POLAR             | V74X5604E<br>V74X5603E<br>V74X5603E<br>V74X5604E |
| 4816    | PL FREQ SWP - ON     | 147     | 7/13 ON<br>15/13 ON<br>8/6 OFF<br>16/6 OFF   | #1 P/L FREQ SWEEP ON<br>#2 P/L FREQ SWEEP ON<br>P/L FREQ SWP #1 OFF<br>P/L FREQ SWP #2 OFF                         |                  | PL A<br>PL C<br>PL A<br>PL C | PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC | A1L/8/FREQ SWEEP<br>A1L/8/FREQ SWEEP<br>A1L/8/FREQ SWEEP<br>A1L/8/FREQ SWEEP         | V74X4300E<br>V74X4300E<br>V47X4901E<br>V47X4901E |
| 4817    | PL FREQ SWP - OFF    | 148     | 8/6 ON<br>16/6 ON<br>7/13 OFF<br>15/13 OFF   | P/L FREQ SWP #1 OFF<br>P/L FREQ SWP #2 OFF<br>#1 P/L FREQ SWEEP ON<br>#2 P/L FREQ SWEEP ON                         |                  | PL A<br>PL C<br>PL A<br>PL C | PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC | A1L/8/FREQ SWEEP<br>A1L/8/FREQ SWEEP<br>A1L/8/FREQ SWEEP<br>A1L/8/FREQ SWEEP         | V47X4901E<br>V47X4901E<br>V74X4300E<br>V74X4300E |
| 4818    | PL MOD - ON          | 149     | 9/1 ON<br>18/1 ON<br>8/14 OFF                | #1 MODULATION ON<br>#2 MODULATION ON<br>MODULATION #1 OFF  |                  | PL A<br>PL C<br>PL A         | SP/L2/VmnB<br>SP/L3/VmnC<br>SP/L2/VmnB               | A1L/9/MODULATION<br>A1L/9/MODULATION<br>A1L/9/MODULATION                             | V74X4320E<br>V74X4320E<br>V74X4903E              |



**Table 11-3. GCIL functions, drivers, and CMD numbers with telemetry, supply voltage sources, ground commands, and DSM numbers (continued)**

| DSM no. | CMD name             | GCL CMD | GCIL driver                                  | GCIL function  | Series interlock | Mode SRC                     | CMD driver power                                     | PNL/SW no./SW name   | MSID   |
|---------|----------------------|---------|--|--|------------------|------------------------------|--|--|--|
|         |                      |         | 16/14 OFF                                    | MODULATION #2 OFF  |                  | PL C                         | SP/L3/VmnC   | A1L/9/MODULATION   | V74X4903E  |
| 4819    | PL MOD - OFF         | 150     | 8/14 ON<br>16/14 ON<br>9/1 OFF<br>18/1 OFF   | MODULATION #1 OFF<br>MODULATION #2 OFF<br>#1 MODULATION ON<br>#2 MODULATION ON                                   |                  | PL A<br>PL C<br>PL A<br>PL C | SP/L2/VmnB<br>SP/L3/VmnC<br>SP/L2/VmnB<br>SP/L3/VmnC | A1L/9/MODULATION<br>A1L/9/MODULATION<br>A1L/9/MODULATION<br>A1L/9/MODULATION | V74X4903E<br>V74X4903E<br>V74X4320E<br>V74X4320E |
| 4820    | PL INTGR SWP - NAR   | 151     | 7/15 ON<br>15/15 ON<br>7/16 OFF<br>15/16 OFF | P/L INTERR #1 SWEEP NARROW<br>P/L INTERR #2 SWEEP NARROW<br>P/L INTERR #1 SWEEP WIDE<br>P/L INTERR #2 SWEEP WIDE |                  | BC 1<br>BC 2<br>BC 1<br>BC 2 | PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC | GCIL ONLY TRUE<br>GCIL ONLY TRUE<br>GCIL ONLY FALSE<br>GCIL ONLY FALSE       | V74X4302E<br>V74X4302E<br>V74X4301E<br>V74X4301E |
| 4821    | PL INTGR SWP - WIDE  | 152     | 7/16 ON<br>15/16 ON<br>7/15 OFF<br>15/15 OFF | P/L INTERR #1 SWEEP WIDE<br>P/L INTERR #2 SWEEP WIDE<br>P/L INTERR #1 SWEEP NARROW<br>P/L INTERR #2 SWEEP NARROW |                  | BC 1<br>BC 2<br>BC 1<br>BC 2 | PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC | GCIL ONLY FALSE<br>GCIL ONLY FALSE<br>GCIL ONLY TRUE<br>GCIL ONLY TRUE       | V74X4301E<br>V74X4301E<br>V74X4302E<br>V74X4302E |
| 4822    | PL FREQ UNIT SEL - 1 | 161     | 8/3 ON<br>16/3 ON                            | INTERR #1 CHAN 1<br>INTERR #2 CHAN 1   |                  | PL A<br>PL C                 | PI/L2/VmnB<br>PI/L3/VmnC                             | A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL                                       | V74X5629E<br>V74X5630E                           |
| 4823    | PL FREQ UNIT SEL - 2 | 162     | 8/4 ON<br>16/4 ON                            | INTERR #1 CHAN 2<br>INTERR #2 CHAN 2   |                  | PL A<br>PL C                 | PI/L2/VmnB<br>PI/L3/VmnC                             | A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL                                       | V74X5631E<br>V74X5632E                           |
| 4824    | PL FREQ UNIT SEL - 4 | 163     | 8/5 ON<br>16/5 ON                            | INTERR #1 CHAN 4<br>INTERR #2 CHAN 4   |                  | PL A<br>PL C                 | PI/L2/VmnB<br>PI/L3/VmnC                             | A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL                                       | V74X5633E<br>V74X5634E                           |
| 4825    | PL FREQ UNIT SEL - 8 | 164     | 8/1 ON<br>16/1 ON                            | INTERR #1 CHAN 8<br>INTERR #2 CHAN 8   |                  | PL A<br>PL C                 | PI/L2/VmnB<br>PI/L3/VmnC                             | A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL                                       | V74X5635E<br>V74X5636E                           |
| 4826    | PL FREQ TENS SEL - 1 | 171     | 8/9 ON<br>16/9 ON                            | INTERR #1 CHAN 10<br>INTERR #2 CHAN 10   |                  | PL A<br>PL C                 | PI/L2/VmnB<br>PI/L3/VmnC                             | A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL                                       | V74X5637E<br>V74X5638E                           |
| 4827    | PL FREQ TENS SEL - 2 | 172     | 8/10 ON<br>16/10 ON                          | INTERR #1 CHAN 20<br>INTERR #2 CHAN 20   |                  | PL A<br>PL C                 | PI/L2/VmnB<br>PI/L3/VmnC                             | A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL                                       | V74X5639E<br>V74X5640E                           |
| 4828    | PL FREQ TENS SEL - 4 | 173     | 8/11 ON<br>16/11 ON                          | INTERR #1 CHAN 40<br>INTERR #2 CHAN 40   |                  | PL A<br>PL C                 | PI/L2/VmnB<br>PI/L3/VmnC                             | A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL                                       | V74X5641E<br>V74X5642E                           |
| 4829    | PL FREQ TENS SEL - 8 | 174     | 8/12 ON<br>16/12 ON                          | INTERR #1 CHAN 80<br>INTERR #2 CHAN 80   |                  | PL A<br>PL C                 | PI/L2/VmnB<br>PI/L3/VmnC                             | A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL                                       | V74X5643E<br>V74X5644E                           |

**Table 11-3. GCIL functions, drivers, and CMD numbers with telemetry, supply voltage sources, ground commands, and DSM numbers (concluded)**

| DSM no. | CMD name            | GCL CMD | GCIL driver  | GCIL function  | Series interlock | Mode SRC   | CMD driver power   | PNL/SW no./SW name   | MSID   |
|---------|---------------------|---------|--|--|------------------|--|--|--|--|
| 4830    | PL FREQ 100 SEL - 1 | 181     | 8/13 ON<br>16/13 ON  | INTERR #1 CHAN 100<br>INTERR #2 CHAN 100   |                  | PL A<br>PL C   | PI/L2/VmnB<br>PI/L3/ VmnC  | A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL   | V74X5645E<br>V74X5646E   |
| 4831    | PL FREQ 100 SEL - 2 | 182     | 8/8 ON<br>16/8 ON  | INTERR #1 CHAN 200<br>INTERR #2 CHAN 200   |                  | PL A<br>PL C   | PI/L2/ VmnB<br>PI/L3/VmnC  | A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL   | V74X5647E<br>V74X5648E   |
| 4832    | PL FREQ 100 SEL - 4 | 183     | 8/15 ON<br>16/15 ON  | INTERR #1 CHAN 400<br>INTERR #2 CHAN 400   |                  | PL A<br>PL C   | PI/L2/VmnB<br>PI/L3/VmnC   | A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL   | V74X5649E<br>V74X5650E   |
| 4833    | PL FREQ 100 SEL - 8 | 184     | 8/16 ON<br>16/16 ON  | INTERR #1 CHAN 800<br>INTERR #2 CHAN 800   |                  | PL A<br>PL C   | PI/L2/VmnB<br>PI/L3/VmnC   | A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL   | V74X5651E<br>V74X5652E   |
| 4834    | PL FREQ SEL - RESET | 191     | 8/1 OFF<br>16/1 OFF<br>8/3 OFF<br>16/3 OFF<br>8/4 OFF<br>16/4 OFF<br>8/5 OFF<br>16/5 OFF<br>8/8 OFF<br>16/8 OFF<br>8/9 OFF<br>16/9 OFF<br>8/10 OFF<br>16/10 OFF<br>8/11 OFF<br>16/11 OFF<br>8/12 OFF<br>16/12 OFF<br>8/13 OFF<br>16/13 OFF<br>8/15 OFF<br>16/15 OFF<br>8/16 OFF<br>16/16 OFF | INTERR #1 CHAN 8<br>INTERR #2 CHAN 8<br>INTERR #1 CHAN 1<br>INTERR #2 CHAN 1<br>INTERR #1 CHAN 2<br>INTERR #2 CHAN 2<br>INTERR #1 CHAN 4<br>INTERR #2 CHAN 4<br>INTERR #1 CHAN 200<br>INTERR #2 CHAN 200<br>INTERR #1 CHAN 10<br>INTERR #2 CHAN 10<br>INTERR #1 CHAN 20<br>INTERR #2 CHAN 20<br>INTERR #1 CHAN 40<br>INTERR #2 CHAN 40<br>INTERR #1 CHAN 80<br>INTERR #2 CHAN 80<br>INTERR #1 CHAN 100<br>INTERR #2 CHAN 100<br>INTERR #1 CHAN 400<br>INTERR #2 CHAN 400<br>INTERR #1 CHAN 800<br>INTERR #2 CHAN 800 |                  | PL A<br>PL C<br>PL A<br>PL C<br>PL A<br>PL C<br>PL A<br>PL C<br>PL A<br>PL C<br>PL A<br>PL C<br>PL A<br>PL C<br>PL A<br>PL C<br>PL A<br>PL C<br>PL A<br>PL C<br>PL A<br>PL C<br>PL A<br>PL C | PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC | A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL<br>A1L/7/CHANNEL SEL | V74X5635E<br>V74X5636E<br>V74X5629E<br>V74X5630E<br>V74X5631E<br>V74X5632E<br>V74X5633E<br>V74X5634E<br>V74X5647E<br>V74X5648E<br>V74X5637E<br>V74X5638E<br>V74X5639E<br>V74X5640E<br>V74X5641E<br>V74X5642E<br>V74X5643E<br>V74X5644E<br>V74X5645E<br>V74X5646E<br>V74X5649E<br>V74X5650E<br>V74X5651E<br>V74X5652E |
| 4835    | PDI PWR - ON        | 185     | 9/14 ON<br>18/14 ON  | PL DATA INTERLEAVER RPC A<br>PL DATA INTERLEAVER RPC C   |                  | PL-A<br>PL-C   | VmnA FPC1<br>VmnC FPC3   | A1L/S17/PDI PWR<br>A1L/S17/PDI PWR   | V76X4376E<br>V76X4378E   |
| 4836    | PDI PWR - OFF       | 186     | 9/14 OFF<br>18/14 OFF  | PL DATA INTERLEAVER RPC A<br>PL DATA INTERLEAVER RPC C   |                  | PL-A<br>PL-C   | VmnA FPC1<br>VmnC FPC3   | A1L/S17/PDI PWR<br>A1L/S17/PDI PWR   | V76X4376E<br>V76X4378E   |

THIS PAGE INTENTIONALLY BLANK

**SECTION 12 - NETWORK SIGNAL PROCESSOR**  
**CONTENTS**

| <b>Section</b> |  | <b>Page</b> |
|----------------|--|-------------|
| 12.1           | GENERAL DESCRIPTION.....                         | 12-1        |
| 12.2           | RETURN LINK PROCESSING .....                     | 12-2        |
| 12.2.1         | PCMMU Interface.....                             | 12-3        |
| 12.2.2         | Return Link Timing.....                          | 12-3        |
| 12.2.3         | Frequency Converter .....                        | 12-3        |
| 12.2.4         | Internal Mode .....                              | 12-6        |
| 12.2.5         | Data Path .....                                  | 12-8        |
| 12.2.6         | Recorder Output.....                             | 12-11       |
| 12.2.7         | Return Link Outputs .....                        | 12-11       |
| 12.3           | FORWARD LINK PROCESSING.....                     | 12-11       |
| 12.3.1         | Overview .....                                   | 12-11       |
| 12.3.2         | Forward Link Inputs.....                         | 12-12       |
| 12.3.3         | Data path.....                                   | 12-15       |
| 12.3.4         | Forward Link Support.....                        | 12-36       |
| 12.4           | SUMMARY BITE.....                                | 12-39       |
| 12.4.1         | Voltage Comparator (Secondary Power Check) ..... | 12-39       |
| 12.4.2         | Forward Link Voice Demultiplexer Check.....      | 12-39       |
| 12.4.3         | Record Mode Processor (RMP BITE) .....           | 12-40       |
| 12.4.4         | Bit Sync Quality and Bit Sync Lock Logic.....    | 12-40       |
| 12.4.5         | MDM BITE Register .....                          | 12-42       |
| 12.4.6         | MDM BITE Register Outputs.....                   | 12-42       |
| 12.5           | NSP UPMODE LOGIC .....                           | 12-46       |
| 12.5.1         | General .....                                    | 12-46       |
| 12.5.2         | GPC Interface Notes .....                        | 12-46       |
| 12.5.3         | GNC Response to NSP Block .....                  | 12-48       |

## TABLES

| Table |                                   | Page  |
|-------|-----------------------------------|-------|
| 12-1  | PCM internal selector modes ..... | 12-4  |
| 12-2  | Uplink program.....               | 12-36 |
| 12-3  | Latch decoder functions .....     | 12-38 |
| 12-4  | Bit sync threshold values.....    | 12-41 |
| 12-5  | Mode parity check.....            | 12-45 |

## FIGURES

| Figure |  |       |
|--------|--|-------|
| 12-1   | NSP interface connections .....                  | 12-2  |
| 12-2   | Convolutional encoder.....                       | 12-10 |
| 12-3   | Sync lock logic state diagram.....               | 12-18 |
| 12-4   | Sync lock logic timing diagram.....              | 12-19 |
| 12-5   | Convolutional encoder.....                       | 12-20 |
| 12-6   | Input waveforms.....                             | 12-21 |
| 12-7   | Forward link data format .....                   | 12-26 |
| 12-8   | NSP data output format.....                      | 12-31 |
| 12-9   | NSP DPS/MDM word format.....                     | 12-31 |
| 12-10  | NSP DPS/MDM data retrieval discrete.....         | 12-32 |
| 12-11  | Forward link generator outputs.....              | 12-32 |
| 12-12  | NSP output formatter and controller timing ..... | 12-35 |
| 12-13  | BSQ and BSL state diagram .....                  | 12-41 |

## SECTION 12 NETWORK SIGNAL PROCESSOR

### 12.1 GENERAL DESCRIPTION

The Network Signal Processor (NSP) acts as the primary data/command link between the S-band communications system and the rest of the orbiter. The NSP can use the Ku-band system in place of the S-band system and/or as a supplement to the S-band.

The NSP, for the forward (ground-to-orbiter) link,

- A. Bit syncs and digitizes the analog data stream provided to the NSP by the S-band or Ku-band system.
- B. Convolutionally decodes the uplink, if required.
- C. If the forward link is encrypted, routes the bit-sync'd stream to the Communications Security (COMSEC) for decryption prior to demultiplexing.
- D. Demultiplexes the bit-sync'd data stream into voice and command stream.
- E. BCH validates and routes the command stream to the General Purpose Computers (GPCs) via Multiplexer/Demultiplexer (MDM) Flight Forward 1 (FF1) (for NSP 1) or MDM FF3 (for NSP 2).
- F. Routes the voice stream(s) to the delta demodulators, where the voice is converted to analog and sent to the Audio Central Control Unit (ACCU). Alternatively, the NSP can send the digital voice stream to the Payload Station (PS), but that capability is not used.

For the return (orbiter-to-ground) link, the NSP

- A. Digitizes analog audio signals provided by the ACCU.
- B. Receives two data streams (64 and 128 kbps) from the active Pulse Code Modulation Master Unit (PCMMU) and processes one for downlink.
- C. Multiplexes voice (ACCU or PS) and Low Data Rate (LDR) or High Data Rate (HDR) channels into a downlink stream.
- D. If required, sends the downlink stream to the COMSEC for encryption.
- E. If required, convolutionally encodes the downlink stream.
- F. Sends the downlink stream to the Ku-band signal processor, the S-band transponder, and (if selected) the Ground Support Equipment (GSE).
- G. Multiplexes a data stream to be recorded on the onboard operations recorders. There are three formats.
  - 1. NASA submode 1, called data only, which are clear 128-kbps data.

2. NASA submode 2, called voice and data, which are clear 128-kbps data multiplexed with two selected voice channels.
3. Department of Defense (DOD) mode, called DOD, which are encrypted downlink data (64 or 128 kbps) multiplexed with Air-to-Ground (A/G) 1 and A/G 2 voice channels.

The NSP consists of four functional sections: forward link data processing, return link data processing, recorder data processing, and the Built-In Test Equipment (BITE) monitoring section.

The NSP interfaces with the communication system and the Data Processing System (DPS) are shown in Figure 12-1.

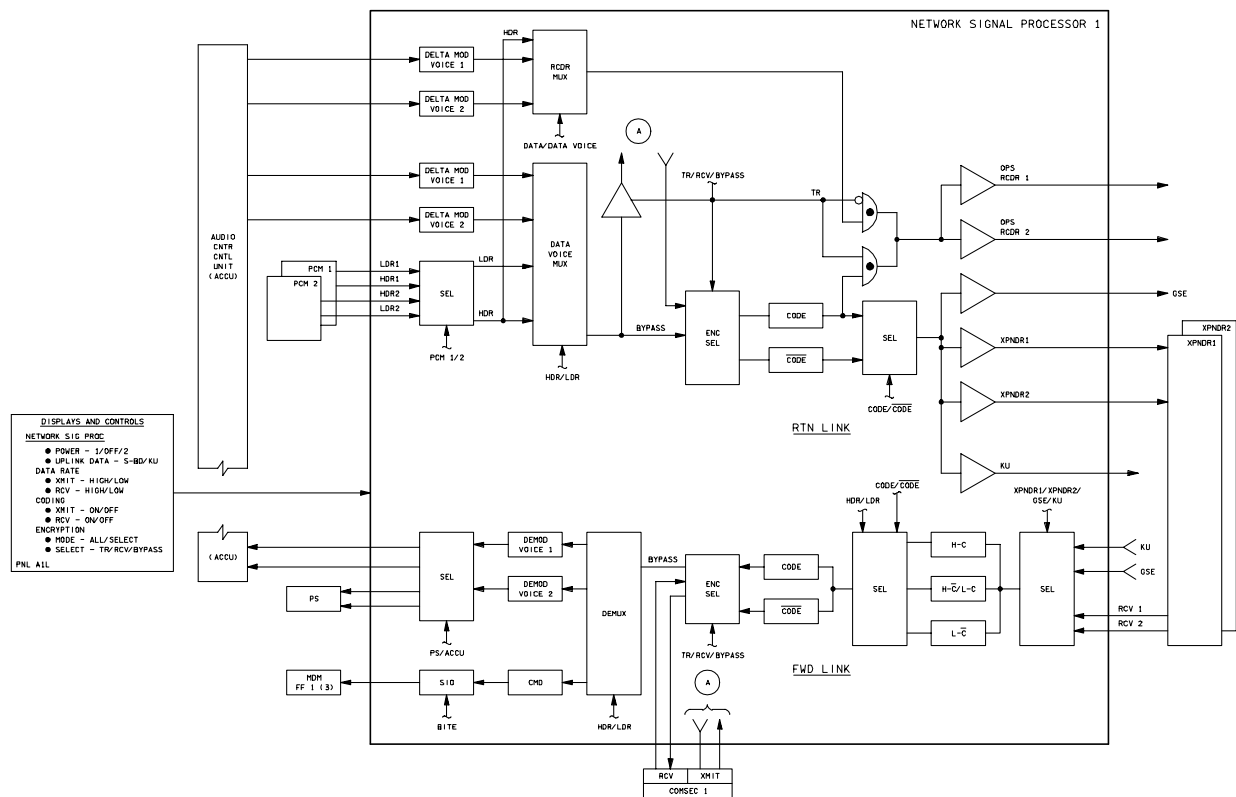


Figure 12-1. NSP interface connections

## 12.2 RETURN LINK PROCESSING

The return link consists of data from the PCMMU and voice from the ACCU/PS, multiplexed together with timing signals provided by the PCMMU (external mode) or NSP (internal mode).

## 12.2.1 PCMMU Interface

The data are supplied by the active PCMMU as serial streams. The PCMMU sends the NSP two data streams: 128 kbps (HDR) and 64 kbps (LDR). The PCMMU also supplies two timing signals: 1.152 MHz and 100 pulses per second (pps). The skew of all four signals is specified to be within 100 nanoseconds of one another.

The selected data stream and both timing signals are checked; if there is a problem with any of them, the NSP is shifted into the internal mode. The specific checks and internal mode in general are discussed in Section 12.2.3. Normal operations are done in the external mode, using the PCM external signals.

### 12.2.1.1 PCMMU Data Signals

The Manchester II, biphasic-L, serial data stream consists of 100 frames of data per second. The NSP treats these as individual frames.

### 12.2.1.2 PCMMU Timing Signals

The 1.152-MHz signal is a timing reference provided for use in the NSPs return link processing. It has a duty cycle specified at 50 percent  $\pm$  5 percent. The 1.152-MHz clock is also sent by the NSP to the S-band and Ku-band transponders to reclock the return link data. This is intended to generate more accurate biphasic transitions and, thus, improve the Radio Frequency (RF) link margin.

The 100-pps clock is the PCM frame sync signal whose leading edge coincides with the first bit of each frame sync pattern. It is used by the return link multiplexer to determine the position of each PCM frame sync (100 frames/sec).

## 12.2.2 Return Link Timing

The return link uses timing circuits to process its data streams. In the external mode, the timing signals are based primarily on the PCMMUs timing signals. In the internal mode, the NSP generates its own. This section discusses how the clocks are generated; the other sections describes how they are used.

## 12.2.3 Frequency Converter

The return link frequency converter provides voice, PCM and sync clock, timing signals for multiplexing voice, and telemetry data into the return link data stream in the coded and uncoded modes. In the internal mode, it provides these signals derived from the NSP internal oscillator. In the external mode, they are provided by the PCMMU 1.152-MHz and 100-pps clocks.

### A. Frequency converter PCM internal selector

The PCM internal selector selects PCM 1, PCM 2, or the internal 1.152-MHz clock to derive voice and PCM timing and sync signals. The address control lines accomplish this as shown in Table 12-1.



**Table 12-1. PCM internal selector modes**

| Inputs       | Address control |            | Outputs         |                 |
|--------------|-----------------|------------|-----------------|-----------------|
|              | (PCM 1 / 2)     | (INTL 2/0) | A               | B               |
| 0 (A) PCM 2  | 0               | 0          | PCM 2 1.152 MHz | PCM 2 1.152 MHz |
| 1(A) PCM 1   | 1               | 0          | PCM 1 1.152 MHz | PCM 1 1.152 MHz |
| 1.152 INTL 2 | 0               | 1          | 1.152 MHz INTL  | PCM 2 1.152 MHz |
| 1.152 INTL 2 | 1               | 1          | 1.152 MHz INTL  | PCM 1 1.152 MHz |
| (0) B PCM 2  | 0               | 0          | PCM 2 1.152 MHz | PCM 2 1.152 MHz |
| (1) B PCM 1  | 1               | 0          | PCM 1 1.152 MHz | PCM 1 1.152 MHz |
| (2) B PCM 2  | 0               | 1          | 1.152 MHz INTL  | PCM 2 1.152 MHz |
| (3) B PCM 1  | 1               | 1          | 1.152 MHz INTL  | PCM 1 1.152 MHz |

**B. Frequency converter voice clock and sync select circuit**

The sync select circuit has two modes to derive sync 1 and sync 2 signals. In the internal mode, a counter chain driven by the 1.152-MHz internal clock input is used to produce the 100-pps sync 1 and sync 2 signals. In the normal mode, this same counter clocked by the PCM 1.152-MHz is operated in sync with the PCM sync (100 pps) signal.

The 32-kHz voice clock signal is derived by the 1.152-MHz input from a pickoff of one of the counter stages.

**C. Frequency converter data clock circuit**

The data clock circuit uses either the PCM or internal 1.152-MHz clock to derive the return link coded mode (576/288-kHz) clock and the upcoded mode clock (192/96 kHz). The comm clock is a 192/96-kHz signal derived from the 192/96-kHz clock.

**12.2.3.1 Clocks/Timing Signals**

All timing signals with the exception of the 100-pps signal are either generated by or pass through the frequency converter. The 100-pps signal comes from the PCMMU only (the record mode processor picks the PCMMU from which to get the 100-pps signal). This section describes what each sync signal is for, and where it is generated.

**A. 1.152 MHz**

There are two of these clocks in the NSP.

1. The one most used originates at the frequency converter's PCM internal selector. This unit selects one of three sources: PCMMU 1, PCMMU 2, and the NSP's internal clock. The output of the selector is used to generate most of the other timing signals in the NSP.
2. The other clock is generated by the NSP internal oscillator. It may be selected by the internal selector to act as the timing source described above. However, it is always used to generate the 70-Hz clock used by the internal mode logic sync success/fail counter.

B. Sync 1

Sync 1 marks the beginning of each PCM frame. In the external mode, sync 1 is generated by the 100-pps PCM signal. In the internal mode, sync 1 is generated by a countdown chain in the voice clock and sync select circuit.

C. Sync 2

Sync 2 is the sync 1 delayed by 1.152-MHz clock period. In the internal mode, sync 1 and sync 2 are generated by a countdown chain in the voice clock and sync select circuit.

D. 128/64 clock

The 128/64 clock is generated in the Telemetry (TLM) clock section of the frequency converter by the selected 1.152-MHz clock ( $128 = 1152 \div 9$ ).

E. 192/96 clock

The selected 1.152-MHz clock is derived by the data clock circuit to generate the 192/96-kHz clock, used to clock the uncoded downlink ( $192 = 1152 \div 6$ ).

F. 576/288 clock

The selected 1.152-MHz clock is derived by the data clock circuit to generate the 576/288-kHz clock, used to clock the coded downlink ( $576 = 1152 \div 2$ ).

G. COM CLK

The COMSEC clock 192/96-kHz signal derived from the 192/96 clock and used by the COMSEC interface and the return link interface.

H. TLM CLR

Derived from the PCM 100-pps input signal.

I. TLM CLK

Generated by the clock sync section of the return link data buffers. The clock sync synchronizes the 128/64- and 32-kHz clocks to the 1.152-MHz clock. It is used to clock voice and PCM data into the return link data buffers.

J. PCM SYNC

Same as TLM CLR.

K. 32-kHz clocks

There are two 32-kHz clocks, generated differently.

1. One is derived from the selected 1.152-MHz clock by the record mode processors frequency converter and sent on. The clock goes to that section's data/voice multiplexer and the record mode delta modulators.
2. The other clock is also derived from the selected 1.152-MHz clock, but in the frequency converter voice clock and sync select. This 32-MHz clock is used by the A/G 1 and A/G 2 return link delta modulators and by the return link data buffers to clock in the digital voice. In addition, it is shipped off to the payload station.

L. 70-Hz clock

This clock is derived from the NSP internal oscillator and is used to clock the internal mode logic PCM input tests.

#### 12.2.4 Internal Mode

What sets the NSP to internal mode?

The NSP checks the PCM inputs, both timing and data, in the internal mode logic unit. The selected data stream (LDR or HDR) is checked for its first sync word 1111 1010 (FA<sub>HEX</sub>), the 1.152-MHz signal and the 100-pps signal. If any one of the three is incorrect, the test fails. If three consecutive failures are detected, the NSP goes to internal mode. If three consecutive successes are detected, the NSP goes to external mode. The NSP checks for these failures at 70-Hz rate; three failures would take about 43 milliseconds to occur.

The check works as follows: The return link PCM data from the output of the record mode processor arrive at the internal mode logic unit. There they are shifted into the shift register on the rising edge of the 128/64-kHz data clock. The sync pattern check and gate output goes high if, after 8 bits, the sync word 1 bit pattern (FA<sub>HEX</sub>) is found in the shift register.

The sync pattern check and gate output are strobed into a sync detect flip-flop at the PCM sync word 1 time slot derived from the PCM 100-pps sync clock and the 128/64-KHz data clock. This flip-flop is reset by the 70-Hz clock.

The 100-pps signal is used to define the start of each frame. If the 100-pps signal is incorrect or absent, the sync word will not be found. Also, the 100-pps signal is required to set the output to "three successful."

What happens in internal mode?

When in internal mode, the NSP assumes the PCMMU is not working, ignores all PCMMU inputs, and tries to salvage NSP voice capabilities. The NSP does this by generating its own clock and sync signals and by substituting alternating ones and zeros for the data the PCMMU should be delivering. It also forces the frame counter to zero and the format Identification (ID) to 170 decimal.

Note on ground equipment response to internal mode: the Front End Processors (FEPs) in building 30 monitor the frame counter. If the frame counter stops incrementing, the FEP stops data from flowing and alerts the operator, who makes a "static frame" call. The flight controllers cannot tell what the frame counter or format ID is and, therefore, cannot tell a PCMMU static frame from an NSP internal mode problem.

A. Record mode processor in internal mode

In internal mode, the record mode processor continues to use the PCM data and clocks; it does not use internal clocks. This means that if LDR data are lost, HDR data will still go successfully to the recorders, even though no data will go to the downlink.

A test was run in SAIL to see what would be sent to the recorders in internal mode. With any of the three inputs missing, mostly unrecoverable data was sent to the recorders when RCD VOICE was ON (the solid state recorders will increment but data and voice will not be properly multiplexed). If RCD VOICE is OFF, the 128K data, if present, goes uninterrupted to the recorders.

B. Return link data buffers in internal mode

In the external mode, the output of the sync pattern and fill generator is inhibited by the output (called INTL TLM) of the internal mode logic going low.

The internal sync pattern and fill generator is loaded with the PCM sync pattern when sync 2 goes high, waits for TLM CLK to activate, and clocks out 32 bits of frame sync pattern (FAF320<sub>H</sub>) and sync count, followed by an alternating 1-0-1-0 pattern, beginning with a "1" for the 33rd PCM data bit. In the internal mode, this sync pattern, frame count, and dummy data are selected in place of the PCM sync and data. Word 5, internal mode format ID, is 170 decimal.

The internal sync pattern is the same as the PCMMU sync pattern. These data are sent to the TLM voice Multiplexer (MUX) to be multiplexed with voice and sent on to the return link interface. The following table shows the first five words of a static frame, disregarding the two voice words after the sync words.

| Word | Bits  | Code                 |
|------|-------|----------------------|
| 1    | 1-8   | 11111010 sync        |
| 2    | 9-16  | 11110011 sync        |
| 3    | 17-24 | 00100000 sync        |
| 4    | 25-32 | 00000000 frame count |
| 5    | 33-40 | 10101010 format ID   |

## 12.2.5 Data Path

### 12.2.5.1 Record Mode Processor

Both HDR and LDR streams and the 100-pps timing signal go first to the record mode processor, where the NSP, using the power status of each PCMMU, selects which PCMMU it will use as a source of data and clock.

The selected HDR stream is passed on to the record mode multiplexer, which generates the data stream to be put on the recorders if the NSP is in a NASA mode. If the Ground Control Interface Logic (GCIL) commands the NSP into the data-only mode, the HDR stream is passed directly through without change. If in data and voice mode, the HDR stream is multiplexed with the two selectable voice channels provided by the ACCU and digitized in the NSP by the return link delta modulators. The output of the record mode multiplexer goes to the return link interface section and is called the record mode data.

The selected (PCMMU 1 or PCMMU 2) HDR and LDR streams are also passed to a logic gateway which uses the GCIL selected downlink rate to determine which stream (HDR or LDR) is passed. This stream, called the return link PCM stream, is passed on to the internal mode logic section for integrity checks and to the return link data buffers for downlink.

### 12.2.5.2 Internal Mode Logic

See Section 12.2.3 for details of this section and what it does with the return link PCM stream.

There is one part of the internal mode logic that is used in the external mode. The voice and telemetry multiplexer controller uses sync 1 and sync 2 signals to mark the beginning of a frame so that the 192/96 clock can be used by a counter to count down to the voice A/G 1, voice A/G 2, and TLM bit segments of each frame. This determines how many bits are in each time slot, as well as the time slot sequence, according to the data format defined. VOICE AG 1 SELECT, VOICE AG 2 SELECT, and TLM SELECT are control signals that define these time slots for use in the multiplexer section of the return link data buffers (see Section 12.2.4).

### 12.2.5.3 Return Link Data Buffers

The return link PCM stream is passed from the record mode processor and sent to the return link data buffers telemetry buffer, a 16-bit shift register. The TLM CLK signal clocks in the data. When TLM CLK and 192/96 sync up, the 16 bits are clocked out (it is at this point that substitution of fill data will occur in the internal mode). The data are multiplexed in the TLM VOICE MUX with two voice channels, according to control signals (VOICE AG 1 SELECT, VOICE AG 2 SELECT, and TLM SELECT) sent from the voice and telemetry multiplex controller in the internal mode logic.

The TLM VOICE MUX circuit is made up of two AND gates, two OR gates, and a flip-flop clocked by the 192/96-kHz data clock. The multiplexing of voice is enabled by the VOICE AG 1 SELECT and VOICE AG 2 SELECT inputs going high into the respective AND gates at the proper time slot in the format. The TL SELECT input to the TLM buffer controls the buffer output which is OR'd with the voice data, which are low during the TLM time slot in the data format.

Note that when the uplink is LDR and the downlink is HDR, A/G 2 is inhibited on the downlink. This is not done inside the NSP. The output of the NSP data rate Receive (RCV) switch is sent to the Pilot (PLT) Mission Specialist (MS) Audio Terminal Unit (ATU), and these two ATUs instruct the ACCU to inhibit A/G 2. If A/G 2 is inhibited, then at this multiplexer stage its downlink window will be filled with zeros.

The 128/64-kHz TLM clock and 32-kHz voice clock are synchronized to the 1.152-MHz clock and routed to the voice and TLM buffers for clocking the incoming voice and TLM data into the respective buffers.

TLM and voice data are clocked into their respective buffers by the input clocks and clocked out at the proper time slot by the 192/64-kHz output clock. Control of the time sequence and multiplexing is accomplished by the VOICE AG 1 SELECT, VOICE AG 2 SELECT, and TLM SELECT signals.

The function of the VOICE AG 1 and VOICE AG 2 BUFF BITE is to examine any unbalanced input and output data flow. Normally, the number of input bits should be equal to the number of output data bits. If an error signal occurs due to an underflow, the VOICE AG 1 or AG 2 BUFF BITE goes low, and the MUX CHECK BIT status bit goes high.

The data leaving the return link data buffers are called the return link data and are routed to both the return link interface and the COMSEC interface.

### 12.2.5.4 COMSEC Interface

This section amplifies and isolates (70 dB isolation between secure and nonsecure data) signals to and from the COMSEC. If the Encryption Mode A1 Switches are properly configured to signal that the transmit will be encrypted, the transmit amps are powered and the return link data and 192/96 clock are sent to the COMSECs for encryption. When the data return, they are shipped to the return link interface.

### 12.2.5.5 Return Link Interface

The COMSEC data, record mode data, and return link data are input to the return link interface circuit. The mode of the circuit is controlled by the ENCRYPTION MODE control and the encoding ON/OFF control.

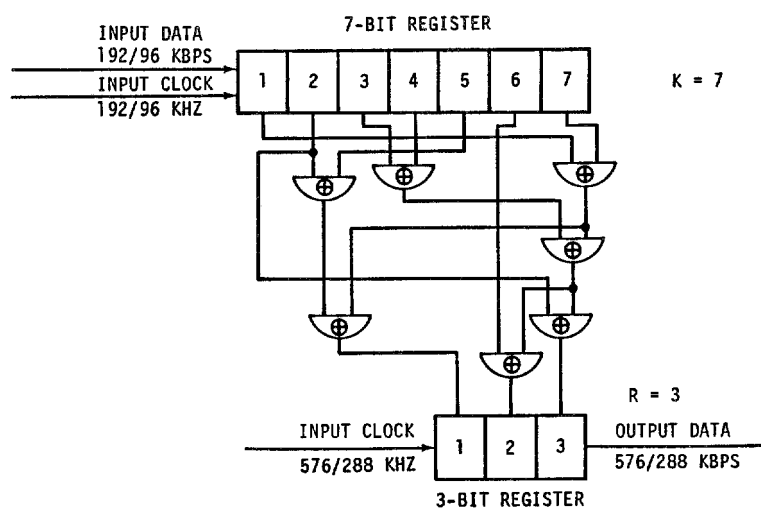
The return mode data from the record mode processor go to a couple of logic gates leading to the recorders. If the data are not to be encrypted (inverse of RCD ENC), then they will be output to the amplifiers that send the data to both Solid State Recorders (SSRs). If RCD ENC is TRUE, then these data will be stopped here, and the uncoded COMSEC data will be allowed to go to the recorders.

In the ENCR MODE ALL, COMSEC data obtained by routing the return link data through the encryption box and back into the NSP are output to the SSRs, Ku-band, S-band transponders, and GSE. The TLM data rate recorded is either 96 kbps or 192 kbps, depending on the downlink data rate selected. This defines either the 64-kbps or 128-kbps TLM data rate.

In the ENCR SELECT mode, the return link data rate is independent of the record mode data rate. The COMSEC data and return link data can be coded or uncoded.

In the coded mode, the return link data are coded by the convolutional encoder. The input data rate of the encoder is 192/96 kbps, and the output data rate is 576/288 kbps because of rate 3 coding. For each data bit shifted into the seven-stage input register, three data bits are shifted out of the three-stage output register.

The convolutional encoder operates as shown in Figure 12-2.



**Figure 12-2. Convolutional encoder**

Each bit shifted into the encoder results in one of two possible output bit sequences; one corresponding to shifting in a zero and one to shifting in a one. The specific bit sequence that results when a bit is shifted into the register, however, depends on the

previous bits that are retained in the encoder. It is this dependency that the decoder (discussed in paragraph 12.3.3.3, convolutional decoder) uses to make a decision as to what was the most likely bit received, a "1" or "0."

The Non-Return-to-Zero (NRZ) coded and uncoded data are converted to biphase data by exclusive OR'ing the NRZ data and clock.

The coded data are controlled by the SET input to the coded data flip-flop. In the uncoded mode, the ENCODING ON/OFF control is low. This sets the flip-flop high through an inverter, so that the coded data input to the flip-flop cannot be clocked to the output. This same high on inverter output enables the NAND gate to pass uncoded data. The control selection for the coded mode works in a similar manner.

### 12.2.6 Recorder Output

ENCR SELECT - 128 kbps (HDR data only) unencrypted

192 kbps (HDR data plus two voice channels) unencrypted

ENCR MODE ALL - 96 kbps (LDR data + A/G-1) encrypted

192 kbps (HDR data plus two voice channels) encrypted

If return mode is set to HDR, two voice channels will be recorded regardless of forward data rate. If forward data rate is set for LDR, the second voice channel will be all zeros.

### 12.2.7 Return Link Outputs

#### 12.2.7.1 Data Rates

Ku-band 96/192 (uncoded), 288/576 kbps (coded)

S-band 96/192 (uncoded), 288/576 kbps (coded)

GSE 96/192 (uncoded), 288/576 kbps (coded)

Recorder 96/192 (data plus voice), 128 kbps (data only)

#### 12.2.7.2 Data Formats

The Return Link Data Buffers build the downlink format by alternating 32 bits of PCMMU data with 16 bits of voice data, as depicted in S-Band PM SB 3.2.3.2.

## 12.3 FORWARD LINK PROCESSING

### 12.3.1 Overview

The NSP forward link receives an analog data stream from the Ku-band or S-band systems and decommutates it into voice and command streams. The voice stream(s) are sent to the ACCU (as analog) or PS (as digital). The command stream is decoded into command words and passed onto MDM FF1 (if NSP1) or FF3 (if NSP2), for



transmission on the GPCs. The same message that can carry command words also carries the BITE status word for downlist to the ground.

The NSP forward link processing is coordinated and commanded by the NSP's uplink programmer, which runs a program stored in read-only memory.

### 12.3.2 Forward Link Inputs

The NSP forward link has several inputs: RF from the S-band, Ku-band, and GSE; discrete commands from GPCs (through MDMs); and command inputs from crew switches and GCIL.

#### 12.3.2.1 Input Data Rates

S-band        32/72 kbps (uncoded), 96/216 kbps (coded)

Ku-band       32/72 kbps (uncoded)

GSE           32/72 kbps (uncoded), 96/216 kbps (coded)

#### 12.3.2.2 Input Data Formats

HDR input data comes in fifty 1440-bit frames per second, consisting of sync words FAF320<sub>H</sub>, 8 bits of station ID, and 256 bits of voice alternating with 32 bits of command data, as depicted in Figure 12-7. The LDR format is similarly depicted in the same place. Station ID is a default value which is decoded by the NSP but not forwarded anywhere.

#### 12.3.2.3 BCH Encoded Commands (embedded input data)

All uplink commands have 77 bits of BCH validation added to each 50 bits of command data, as depicted in S-Band PM SB 3.2.3.1.

#### 12.3.2.4 NSP Panel Switches

The crew has eight panel switches to control the NSP.

##### A. NETWORK SIG PROC - POWER

Three-way switch, panel A1, works through GCIL

1 (upper) - Applies power to NSP1

OFF (middle) - Removes power from both NSPs

2 (lower) - Applies power to NSP2

**B. NETWORK SIG PROC - UPLINK DATA**

Two-way switch, panel A1, works through GCIL

S-BD (upper) - S-band system selected to provide forward link data

KU (lower) - Ku-band system selected to provide forward link data

**C. NETWORK SIG PROC - DATA RATE XMIT**

Two-way switch, panel A1, works through GCIL

HIGH (upper) - Sets NSP to HDR on downlink

LOW (lower) - Sets NSP To LDR on downlink

**D. NETWORK SIG PROC - DATA RATE RCV**

Two way switch, panel A1, WORKS THROUGH GCIL

HIGH (upper) - Sets NSP to HDR on uplink

LOW (lower) - Sets NSP to LDR on uplink

**E. NETWORK SIG PROC - CODING XMIT**

Two-way switch, panel A1, works through GCIL

ON (upper) - Sets coding on for downlink

OFF (lower) - Sets coding off for downlink

**F. NETWORK SIG PROC - CODING RCV**

Two-way switch, panel A1, works through GCIL

ON (upper) - Sets coding on for uplink

OFF (lower) - Sets coding off for uplink

**G. NETWORK SIG PROC - ENCRYPTION MODE**

Two-way switch, panel A1, works through GCIL

ALL (upper) - Puts NSP into DOD mode, decrypting the uplink and encrypting the downlink. Also puts the data stream output by NSP (LDR or HDR) and A/G 1 and A/G 2 onto the ops recorders (all encrypted). This is the normal mode of operation on a classified DOD mission.

SELECT (lower) - Puts the NSP into a NASA mode, as selected by the NSP encryption select switch (see below). With this switch position selected, the data

going onto the recorders will NOT be encrypted, regardless of the position of the encryption select switch.

#### H. NETWORK SIG PROC - ENCRYPTION SELECT

Three-way switch, panel A1, works through GCIL

T/R (upper) - Sets the NSP to encrypt the downlink and decrypt the uplink.

RCV (middle) - Sets the NSP to decrypt the uplink, but send an unencrypted downlink to S-band and Ku-band. This is the normal mode of operation on NASA flights.

BYPASS (lower) - Sets the NSP to process the uplink without decryption and sends an unencrypted downlink to the S-band and Ku-band.

#### I. UPLINK BLOCK

Three-way lever lock switch, panel C3, does NOT work through GCIL.

The uplink block switch is used to prevent commands from being accepted and processed onboard. This may be used to augment or replace the SM/BFS automatic uplink block function.

NSP BLOCK (upper) - In this position, the NSP forces the GPC to bypass the NSPs. This causes a BCE STG 1 NSP message onboard. The crew must perform a Guidance, Navigation, and Control (GNC) (or, if Backup Flight System (BFS) is engaged, a BFS) input/output (I/O) reset to regain the NSP. With the NSP bypassed, commands will not be able to get to the GPCs for processing

GPC BLOCK (middle) - In this position, the GPC receives the commands but refuses to process them. This is the switch position normally used to “configure for Loss of Signal (LOS)”, because it does not require an I/O reset to regain command capability. The GPC will not block commands unless both switch poles are indicating GPC Block and thus will not work if FF1 or FF3 is bypassed or if one switch pole is failed open.

ENABLE (lower) - This allows any valid commands received to be processed. This is the normal switch position.

#### 12.3.2.5 NSP Crew Spec Inputs

All crew inputs to the NSP are done by hardware switches. There are no spec inputs to the NSP.

### 12.3.2.6 NSP Ground Commands

| DSM  | Nomenclature         | Notes   |
|------|----------------------|---|
| 4760 | NSP 1 ON             | GCIL interlocks prevent both NSPs from being on at the same time. |
| 4762 | NSP 2 ON             |   |
| 4761 | NSP 1/2 OFF          | Normally safed in the Server                                      |
| 4758 | NSP UPLINK - LDR     | Normally safed (after STS-115)                                    |
| 4759 | NSP UPLIN - HDR      |   |
| 4763 | DNLINK - LDR         | Normally safed (after STS-115)                                    |
| 4764 | DNLINK - HDR         |   |
| 4770 | UPLINK CODING - ON   | Normally safed in the Server                                      |
| 4771 | UPLINK CODING - OFF  |   |
| 4772 | DNLINK CODING - ON   |   |
| 4773 | DNLINK CODING - OFF  |   |
| 4767 | DATA SOURCE - KU     |   |
| 4768 | DATA SOURCE - S      |   |
| 4774 | RCDR VOICE 1/2 - ON  |   |
| 4775 | RCDR VOICE 1/2 - OFF |   |

### 12.3.3 Data path

Data are input to the bit synchronizer from four sources (S-band XPNDR 1, S-band XPNDR 2, Ku-band, or GSE), only one of which is selected for data processing at any one time. When bit synchronization is achieved, data and clock are presented to the convolutional decoder for decoding in the DECODE ON mode. The decoded data or the hard decision data are sent, depending on the mode, to the frame synchronizer.

The data invert control in the frame synchronizer is activated only in the UNCODED mode. In the coded mode, the convolutional decoder provides its own data inversion. In the ENCR BYP UNCODED mode, if complement correlation is detected, a data invert command is sent to the invert logic. In the ENCR RCV UNCODED mode, if no positive correlation is detected within 500 msec, a data invert command is sent to the data invert logic. This process is repeated until a positive correlation is detected. Once frame sync lock is achieved, demultiplexing of voice, command, and Doppler station ID can take place.

The voice data are rate buffered and sent to PS when mode control selects PS or to the delta demodulators when the mode control selects ACCU. In this case, the demodulated voice data are then sent to the ACCU. The 8 bits station ID data are sent to the Doppler extractor at the received data rate once per frame time. The commands arriving in the command channel are checked for errors in the operational Bose-Chaudhuri-Hocquenghen (BCH) decoder and stored in a buffer. A message valid pulse is sent to the Operational Instrumentation (OI) MDM, via the summary BITE circuit, for every command word that passes the BCH check and vehicle address check. After 10 commands have been received, a signal is sent to the OI MDM, indicating a data

present status. Upon request from the Data Processing System (DPS) MDM, 32 16-bit words are sent. The first word contains the BITE status of the NSP, the second through 31st words contain commands, and the 32nd word contains a bit for each command transmitted, representing the validity of that command.

### 12.3.3.1 Bit Synchronizer

#### A. Analog/digital conversion

The Analog/Digital (A/D) converter contains a 3-bit A/D converter that quantizes the incoming 216K, 96K, 72K, or 32K signal, treated as an analog signal, into one of eight possible levels and outputs a 3-bit word corresponding to the input level. The quantization takes place at 32 times the data rate ( $32 \text{ FREQ}_{\text{SIGNAL}} \text{ (FS)}$ ).

#### B. Soft decision data detection and clock generation

An accumulator sums the quantized signal samples for eight ( $32 \text{ FS}$ ) clock times and outputs a 6-bit digital word representing the quarter ( $32 \div 8 = 4$ ) symbol integration for Manchester data detection and full symbol addition. Full symbol addition produces an eight-level estimate of the received signal strength. This signal is quantized into one of eight states by the data mapping (quantizing) process, and a 3-bit word representing the quantization state is produced, which is the numerical estimate of data for use by the viterbi decoder. The most significant bit out of the bit sync is the hard decision data which are used in the uncoded mode. Soft decision data are used by the convolutional decoder and gives a 2-dB gain, along with the 3-dB coding gain. These soft decision data provide the decoder with a weighted estimate of the received data. The decoder then uses this information, along with the coding information, to determine the maximum likelihood of what the received data are, a one or a zero.

A phase lock loop is used to zero the phase error between the incoming data and derived clock, producing the reconstructed data clock.

#### C. Lock detection

The lock detector alternately adds and subtracts the absolute values of the in-phase and quadrature half-symbol integrations performed by the data detector. The lock detector algorithm processes the half-symbol integrations by taking the absolute value of the in-phase terms and subtracting them from the absolute value of the quadrature terms. If the half-symbol integration is to be added and is positive, or if it is to be subtracted and is negative, the value of the half-symbol integration is passed to the lock detector unchanged. If the half-symbol integration is to be subtracted and is positive, or if it is to be added and is negative, the value of the half-symbol integration is multiplied by minus one before being processed.

The lock detector requires an integration time of  $2^{14}$  (16,384) symbol times (0.076 sec for HDR coded and 0.17 sec for LDR coded). An up/down counter is utilized to count the over/under flows, which results in accumulating the half symbol integrations. When adding a number into the accumulator, a carryout of one from

the accumulator indicates that the counter should be advanced one count. When subtracting a number from the accumulator and a zero carryout results, the counter is decremented by one count.

After integrating for  $2^{14}$  symbol times, the output of the lock detector must be compared to a previously determined threshold. This is accomplished by presetting the counter to the negative threshold and allowing the counter to integrate. When the output of the counter exceeds zero, the lock detector is determined to be in lock. The threshold is dependent upon the RCV ENCR ON/BYP and decoding ON/OFF modes.

### 12.3.3.2 Frame Synchronizer Detect and Lock Logic

The frame sync detect logic computes the hamming distance (minimum number of errors) between any 24 bits of the data stream and the known frame sync pattern and then determines if a positive or negative correlation has been detected. Less than three errors is a positive correlation (+Cor) or greater than 21 errors is a negative correlation (-Cor). The data are input to the 24-bit serial input-parallel output register. The 24 parallel bits are then summed, and 5 bits representing the sum of the 24 parallel bits are sent to the correlation logic that determines if the correlation is (+Cor) or (-Cor). The input sync pattern is 1111, 1010, 1111, 0011, 0010, 0000.

#### A. Data inversion

In RCV BYP uncoded (mode 1), if a negative correlation occurs, an invert data command is sent to the NASA/DOD selector to invert the data. There is no loss of data due to the invert command.

In RCV ENCR uncoded (mode 2), every 500 + 100 msec a data invert signal is sent until frame sync correlation is obtained.

In coded mode, the frame sync decoder operates only on the data true state inputs (+Cor).

#### B. Lock logic

The frame sync lock logic algorithm is illustrated in Figure 12-3. The actual logic operates as follows: In the search mode (SEARCH 1), the frame sync detect decoder is routinely operating on the data bit by bit, looking for a negative (-COR) or positive (+COR), and when the first correlation is detected, the logic shifts to the acquisition test mode (ACQ = 1). If a second consecutive correlation occurs, frame sync is assumed to be acquired and the logic shifts to the frame sync lock mode (lock = 1).

If while in the lock mode, a correlation failure occurs followed by a second consecutive correlation failure, the logic reverts to the search mode. Should a correlation failure occur, followed by correlation, the logic enters state A and returns to Bracket Data Status (BDS) state without a loss of lock indication. It should be noted that BDS drops out for one frame because of no correlation

(+Cor = 0). BDS = 1 indicates the sync lock logic has received two consecutive valid sync correlations, and the data bracketed can be transmitted.

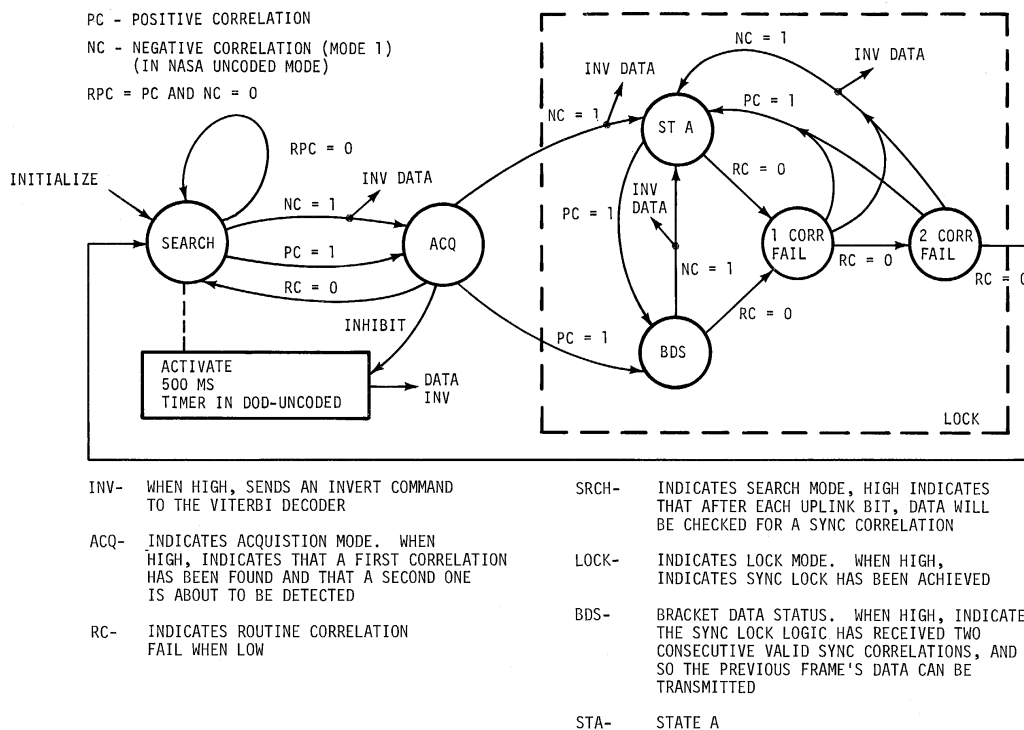
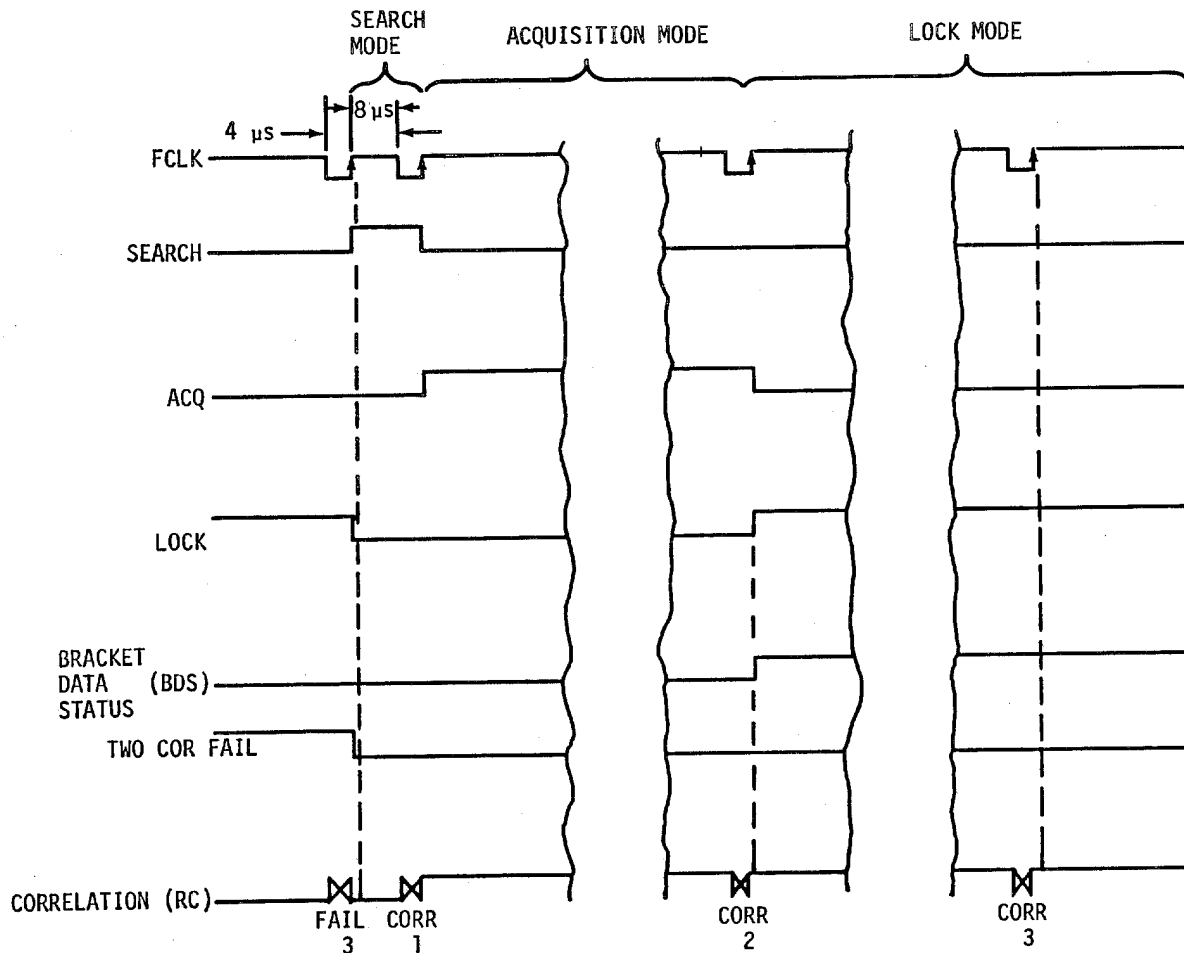


Figure 12-3. Sync lock logic state diagram

C. Timing

The following discussion is in reference to the timing diagram (Figure 12-4) F CLK is used to strobe the various logic circuits and is derived from the 250-kHz (4 μsec) strobe clock.

The timing sequence starts out with the lock logic indicating lock. After three correlations have failed (Two Cor Fail = 0), the lock indicator shows lock loss (Lock = 0). Bracket data status drops out (BDS = 0) on the first correlation failure.



**Figure 12-4. Sync lock logic timing diagram**

When lock is lost after three consecutive correlation failures (Two Cor Fail = 0), the search mode is selected (Search = 1) until the first correlation is detected. The acquisition mode is selected (ACQ = 1). Upon the next consecutive correlation, the logic selects the lock mode (Lock = 1) and bracket data status (BDS = 1) is output. This completes a typical sequence of the frame sync lock logic.

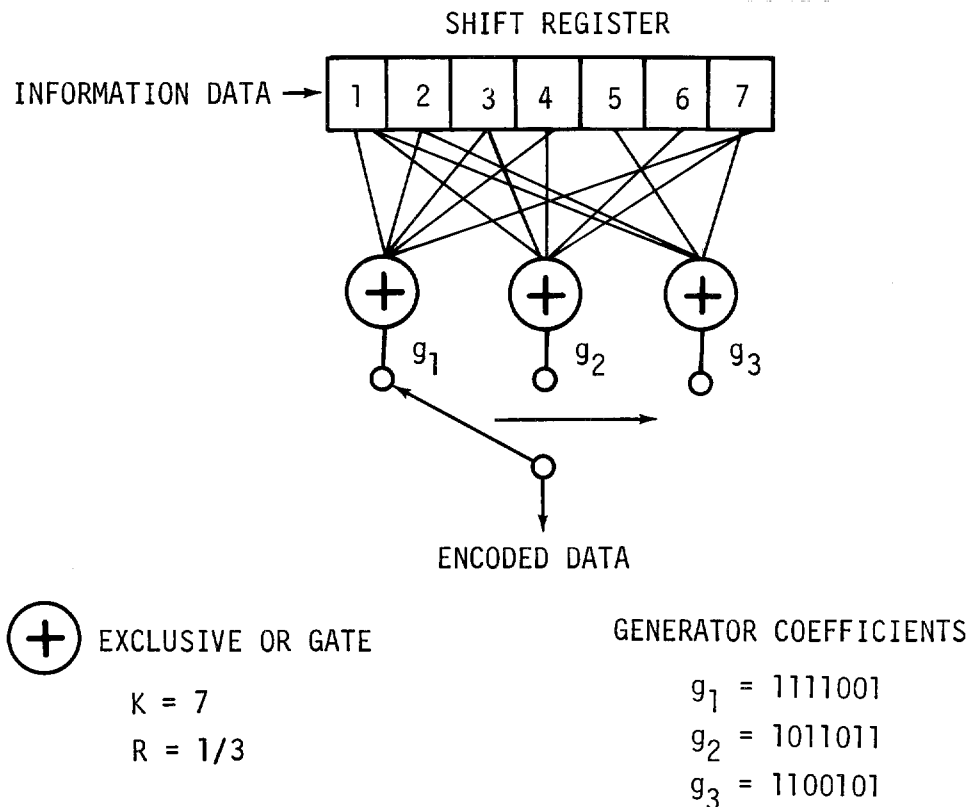
### 12.3.3.3 Convolutional Decoder

The convolutional decoder is a rate 1/3 phase shift keyed data decoder with a constraint length of 7 bits, a decoder integration time of 40 bits, and soft decision decoding.

To understand the decoder, it is necessary to understand the encoder and the coding sequence of the data to be decoded. The decoder contains a duplicate encoder.

The following discussion applies to the encoder shown in Figure 12-5.





**Figure 12-5. Convolutional encoder**

For each bit shifted into the encoder, 3 bits of coded data are produced, 1 bit for each exclusive OR gate output; thus, the encoder is said to have a rate of 1/3. The constraint length of the encoder of seven is determined by the length of the shift register.

Each bit shifted into the encoder results in one of two possible output bit sequences, one corresponding to shifting in a zero and one to shifting in a one. The specific bit sequence that results when a bit is shifted into the register, however, depends on the previous bits that are retained in the encoder.

Now that the received data sequence is understood, the operation of the decoder can be discussed. The following is a description of the fundamental operation of a decoder.

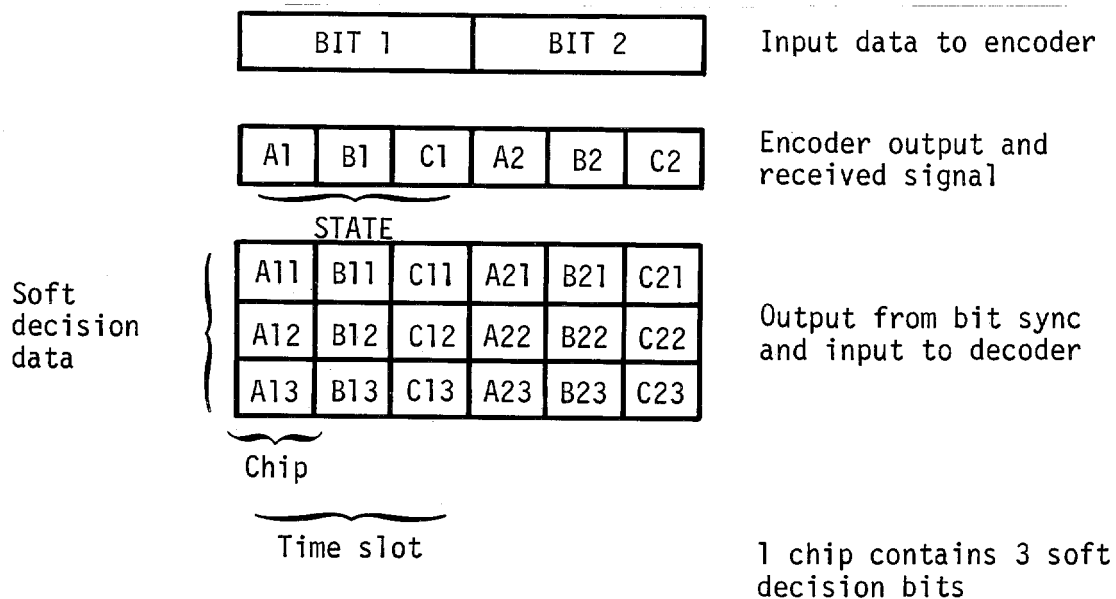
Decoding of convolutional codes is based on a state diagram structure. Each node in the diagram corresponds to the various possible states the received sequence can take. The decoder chooses the path through the state diagram that has maximum likelihood of what the received sequence should be, given the actual received sequence. In other words, the decoded message sequence will provide a coded output sequence that is closer (differs in fewer bit positions) to the actual transmitted sequence mixed with noise than the coded output sequence corresponding to any other possible message sequence. In this manner, bit errors can be corrected.

The sequences are stored, up to 30 bits, before a decision is made. Decoding then occurs on a bit-by-bit basis.

The following discussion applies to the functional schematic of the convolutional decoder in the SSSHB, drawing 16.3, sheet 2, Network Signal Processor Forward Link.

A. Input

The input to the convolutional decoder is a soft decision input provided by the bit synchronizer (Figure 12-6).



**Figure 12-6. Input waveforms**

“Time slot” refers to the period where three-three soft decision input bits (corresponding to one encoder input bit) are received, and one decoder output bit is sent out.

B. Data input circuits

The count three logic counts the number of resync tries, and after three tries, the data invert circuit inverts the data. The data are buffered in the three-three bit holding latches.

C. Timing Logic

The timing logic provides the basic control signal for operation of the convolutional decoder. The term “time slot” refers to the time period when three encoded soft decisions (corresponding to one encoder input bit) are received, and one decoded bit is sent out.

D. Branch metric generator

The input noise-corrupted encoded data are compared with all 64 possible correct encoded sequences derived from the duplicate encoder. For each pair of states (a one input and zero input to encoder), a likelihood measure, or “metric”, is generated. The lower the metric after comparison, the closer the received sequence will be to that corresponding encoded sequence.

E. Metric memory

The metric memory is used to store the accumulated branch metrics (called path metrics) along each possible path the decoder wishes to track. Only 64 paths need to be watched each process cycle. The metric memory sends the path metrics to the add-compare-select logic for processing, then receives updated new path metrics which it must save.

F. Add-compare-select

There are 64 states possible in the encoder with constraint length  $K = 7$ . During each time slot, 64 path metrics will be determined. The decoder makes all its decisions on a “best path” basis; therefore, only the best path into each state (or “node” on the trellis diagram) need be save. The “decision” indicating which of the two remerging paths is more likely is sent to the path retrace circuitry.

G. Renormalization

Since the numerical value of the metric can become large, a “renormalization metric” is subtracted from all survivor metrics so that large numbers will not have to be stored.

H. Best state logic

The first survivor metric received will be accepted as the best. Subsequent comparisons will be made between this running “best metric” and all that are received. The best state at the end of the process cycle (having the best metric) will be designated as the end point of the most likely path (or sequence of received data). This best state is presented to the path retrace logic.

I. Path retrace logic

The path retrace must be examined in two modes; those of input and output or retrace.

Input data are received from the add-compare select logic as a single-bit “decision.” Each timeslot is given a numerical index that the path retrace can trace. Decisions are recorded for 31 process cycles. If any state is to be addressed, the decision (0 or 1) leading into that state can be recalled, leading back to a unique state in the previous time slot.

The retrace function begins with the best state from the previous timeslot. This is the most likely path end point. The retrace logic then goes back along the unique best path traced out by past add-compare select decisions and picks out a decision made along that path as the output. The further back the decoder looks, the less errors it will make; however, for this decoder, the process goes on for 30 bits and the 30th bit out of the retrace logic is used as the output.

#### J. Resync circuitry

The resync determines and corrects for phase ambiguities in the three-soft decision input data.

In the resynchronization process, the sum of minimum (or best) metrics over a time slot interval is accumulated. At the end of that interval, a constant is subtracted from the accumulated sum, which, if the decoder is in synchronization with the data, will leave a number very close to or equal to zero. If the input symbols or data bits are not in sync with the decoder states, a resync pulse is generated which time shifts the data stream by one bit. This process is repeated until the data are again in sync.

#### K. Analog bit error rate (BER)

A 0 to 5V dc signal for a BER of  $10^{-1}$  to  $10^{-4}$  is provided. With no noise, the best metrics will always be zero. Increasing noise will cause the metrics to grow; consequently, sending more pulses to the integrator causes an increase in the BER signal. The Resistor Capacitor (RC) time constant of the integrator is greater than 0.1 second. Telemetry is inverted, resulting in zero BER = 5V. BER stays at 5V when uplink decoding is off.

### 12.3.3.4 ACCU/Payload Station Voice and Clock

#### A. Voice buffer 1 and 2

Each voice buffer operates as a 128-bit serial in/serial out buffer. Control of buffer 1 and buffer 2 is as follows: If uplink frame sync lock is not present (lock = 1), an INHIBIT will be set, no data will be sent out of the voice buffers, and the buffer will be reset. When frame sync lock occurs (lock = 0), the buffer accepts data if voice inhibit (voice reinitialize = 0) is low. However, the OUTPUT INHIBIT will still be present until 64 voice bits have been buffered, and then the inhibit will be cleared, allowing data to be read out by the audio clock (32 kHz = HI data rate or 24 kHz = LO data rate) buffer output clock.

The inhibit will remain cleared until the uplink lock is lost (lock = 1) or the BITE circuitry detects an error in the voice transmission and sets VOICE REINITIALIZE high.

VOICE AG1 ENABLE high gates the uplink data clock (uplink clock) at the appropriate time to shift the voice data bits into the voice buffers from the serial data stream (demultiplexes voice bits).

OUTPUT INHIBIT, when high, enables voice AG1 CLOCK output and, internal to the voice buffer, enables audio clock 1 to shift the voice bits out of the buffer provided (voice reinitialize = 0) and (lock = 0). Also, output inhibit enables the PS to receive audio clock 2 in the PS mode. Underflow 1 is low when the buffer output register is empty, signifying that no voice data in the buffer have been transferred to the output register or the buffer contains no voice data when it should have. Similarly, overflow 1, when low, indicates the input register is full and data have not been transferred into the buffer when it should have been. These signals are tested for at the appropriate time in the summary BITE circuit board, and, if an error is detected, voice inhibit (voice reinitialize = 1) inhibits voice data bits from being output from the voice buffer.

B. Forward link audio clock generator

In the HDR mode, the audio clock generator counts down the eight times bit frequency signal (eight FS clock) from the bit synchronizer to obtain the 32-kHz audio clock.

In the LDR mode, the audio clock generator counts down the eight times bit frequency signal (eight FS clock) from the bit synchronizer to obtain the 24-kHz audio clock.

In the low data rate mode, a phase lock loop locked to the eight times bit frequency signal (eight FS clock) from the bit frequency signal is used to obtain a 24-kHz audio clock.

| Eight FS clock          | Coding off | Coding on |
|-------------------------|------------|-----------|
| High data rate (72 kbs) | 576 kHz    | 1728 kHz  |
| Low data rate (32 kbs)  | 256 kHz    | 768 kHz   |

C. PS/ACCU selector

The PS/ACCU control when high (PS/ACCU\_SEL = 1) routes the digital voice data out of the voice buffer and voice clock (32 kHz - high data rate; 24 kHz - low data rate) to the PS. Voice is routed to the voice delta demodulators when (PS/ACCU = 0).

**12.3.3.5 Delta Demodulator**

The Delta Demodulator (DD) reconstructs the original analog voice signal from the digital input bit stream. To understand the DD, it is necessary to understand how the delta modulator operates, which is presented in Section 12.3.3.7. The operation of the DD is essentially identical in manner as the delta modulator, except it does not have a feedback/comparator loop.

The operation of the overflow-underflow prevention circuitry has three purposes.

- A. When the system is first turned on, the demodulator predictor value may be different from that stored in the modulator predictor. Then, any predictor increase or decrease in the modulator would cause an equal increase or decrease in the demodulator. It is possible for this increase or decrease to cause the demodulator predictor register to overflow or underflow if its magnitude is near enough to its maximum or minimum value.
- B. Accumulated bit errors in the received serial digital input could cause the demodulator predictor to overflow or underflow.
- C. Loss of serial digital information without loss of the clock could cause a continuous overflowing or underflowing of the demodulator predictor. This condition would result in a full-scale oscillation of the demodulator analog output. The demodulator overflow-underflow prevention circuitry monitors the magnitude stored in the accumulator. If the magnitude stored in the predictor is within eight step sizes of its maximum or minimum magnitude while the accumulator is being incremented positively or negatively, respectively, the overflow underflow prevention circuitry prevents the new value from being loaded into the accumulator at that bit time by inhibiting the clock which loads the accumulator with the new value.

#### **12.3.3.5.1 MFX Capabilities**

If the crew configures for MFX per Orbit Operations OCA S-Band Modern (MFX) Activation, A/G#2 will be used for OCA via the PS ATU.

The OCA MFX uplink will be shipped to the NSP Forward link A/G#2 128-bit Voice Buffer then on to the Voice Delta Demodulator and route a converted analog signal to the ACCU then on to the PS CCU which is connected to the OCA laptop. The OCA laptop will receive this analog information and convert it back to digital signal and process it accordingly.

The OCA laptop will convert the digital signals to analog then ship this analog information to the PS CCU (configured solely to A/G#2) which will route it to the ACCU and then on to the NSP. The NSP return link A/G#2 Delta Modulator receives the analog signal converts it to digital and sends it in the downlink.

Due to the inefficiencies of the Analog to Digital Conversions (and D/A conversions) between the OCA laptop and the NSP A/G#2 processor, the bandrate of OCA MFX is only 1.48 kbps, thus only allowing text to be transferred.

#### **12.3.3.6 Command Processor Operations**

The command processor demultiplexes each command from the uplink data stream (Figure 12-7) and stores the command in the command buffer while the received BCH code (77 parity bits) is being verified. At the end of the verification period, the command is sent to the 10-command double buffer, and the validity bit is sent to the output formatter and controller if the command passed the BCH code verification check. If the command failed the BCH code verification, the Vehicle Address (VA) is cleared to all zeros and the validity for that command is set to zero in the MDM validity word.



The function of the BCH decoder is to determine if the 50 information bits and 77 parity bits contained in each 128-bit command word constitute a proper BCH encoded sequence. This is accomplished by generating 77 parity bits from the received 50 information bits and then comparing them with the 77 parity bits transmitted in the 128-bit BCH coded command. If an error occurs, the vehicle address of the 48-bit command word in the 48-bit register is cleared (set to all zeros) by the DOP ENB/ERROR NOR gate whose output logic is (CLEAR = DOP EN • ERROR).

The clearing of the vehicle address to zero forces the COMMAND VAL signal low via the COMMAND VAL NOR gate whose output logic is (COMMAND VAL = VA • BCH VALID).

The COMMAND VAL signal will also be forced low when the vehicle address (bits 1-5) are all low (zero), such as when there are no commands on the uplink; in this case, BCH VALID is also high, indicating a command has failed the BCH code test or BDS is lost. The command VAL signal will be high, indicating a valid command was received, only when a nonzero vehicle address is present and BCH VALID is low, indicating a command has passed the BCH code test.

The COMMAND VAL signal is sent to the 10-command status double buffer via the flip-flop, which is clocked by DOP ENB signal at the beginning of the next frame, provided BDS is high. The buffered validity status is then sent to the Message Valid flip-flop, which is clocked by Voice 1 ENB and sent to the summary BITE register.

Message Valid goes high when a valid command is received and stays high until a nonvalid command is received because of one of the following: a zero vehicle address in the idle pattern; BDS is low, indicating a failure in frame sync correlation; or command has failed BCH code test. If individual RTCs are being uplinked, Message Valid will be high <165 msec, while an RTC is in the 10-command buffer, before it is fetched by the FF MDM.

D. 10-command double buffer

The 10-command buffers A and B provide storage for commands prior to their being requested by the FF MDM. After 10 commands have been stored, DATA READY is set to 1 if at least 1 of the 10 commands is valid.

Data are clocked into the buffers by CLOCK IN at the uplink clock rate and clocked out by CMD CLK at 1 MHz.

If frame sync lock is lost during buffer loading, ACQ goes high and the data clock is inhibited (BUFFER CLK INH). The partially received command will not be transferred from the command buffer into the 10-command double buffer. The status of frame sync lock (ACQ) is checked at the end of each count of 48 out of the command processor counter.



The toggle buffer signals the buffers from being loaded to being read at the end of the 480 count.

E. Data ready flip-flop

Data ready flip-flop is inhibited (cleared) during the last 20 msec of the 200-msec buffer read time.

Data ready flip-flop is cleared at the end of the first polling.

Data ready flip-flop output is driven to zero by the count 36 clock signal just prior to the first command being completely loaded into the 10-command double buffer.

Message valid preconditions the data ready flip-flop the first time a valid command generates a message valid signal, signifying the command has passed BCH code verification. Data ready flip-flop is clocked at the count of 480, and if at least one valid command was received, data ready goes high. Data ready high freezes the BITE data in the MDM BITE register until the NSP is polled.

F. Disable data flag

In the command processor, the DISABLE DATA FLAG inhibits the Com CLK from shifting data out of the 10-command double buffer. The other functions of the disable flag will be covered in the output formatter and controller discussion.

G. Message discrete control logic

The message discrete control logic clears the data ready flip-flop after the first poll (message discrete). If a second poll should occur during the 200-msec poll period or if it is the last 20 msec of the poll period, the data disable flag will go high and inhibit the data relock flip-flop in the output formatter and controller from outputting words 2 through 32 to the FF MDM.

### 12.3.3.7 Voice Delta Modulator

Voice Delta Modulator - The adaptive (variable slope) delta modulator is a simple type of predictive quantizing system which is essentially a one-digit differential PCM system. The system is based on transmission of the quantized difference between successive sample values, rather than the samples themselves. Both the modulator and the demodulator make an estimate or prediction of the input signal value, based on the previously transmitted signal.

A. Functional operation

In the modulator, the value of the input signal at each sample time is predicted to be a nonlinear function of the past values of the quantized signal. Introducing nonlinear prediction into delta modulation provides a useful means of extending the range over which the system yields its optimum performance. The quantizing level is not fixed and varies in discrete steps at each sample time, depending on the sequence of previous comparison results. The modulator predictor value is

compared to the input signal and the predictor is incremented or decremented, depending on the result at that sample time by a quantizing level which is dependent on the sequence of present and previous comparison results. The quantizing level or step size sequence is produced by means of the abate algorithm. The abate algorithm used in this system has 16 step sizes which vary from -8 through +8, excluding zero. The magnitude of the incoming analog signal is compared to the magnitude which is currently stored in the predictor section of the modulator. The input magnitude is increased or decreased, respectively, to track the magnitude of the incoming signal. The digital result of the comparison (0, if the input is greater than the predictor; 1, if the input is less than the predictor) is stored in an 8-bit shift register. The step size, or the amount by which the predictor is incremented, is based on the last eight comparison results. Using the last eight comparison results enables the predictor increment to be any one of the 16 values, depending on the comparison results starting at the last comparison result and proceeding through previous comparison results until an opposite bit is encountered determines the magnitude and sign of the predictor increment; i.e., three, four, or five 1's before encountering a "0" would cause the predictor to be incremented by -3, -4, or -5, respectively, while three, four or five 0's before encountering a "1" would cause the predictor to be incremented by +3, +4, or +5, respectively.

There is no magnitude comparison done in the demodulator. The results of the previous comparison in the modulator are transmitted to the demodulator and the operation of the demodulator is essentially the same as that of the modulator. The predictor magnitude in the demodulator is Digital-to-Analog (D/A) converted, and this provides the demodulated signal output.

#### B. Hardware description

A 10-kHz low pass filter on the input is used to reject high frequency ripple and noise. Output of the filter feeds one input to a voltage comparator (+input). The second input (-input) is the analog voltage (predictor value) from the digital to analog converter. A hysteresis of 7 mV is added to the comparator to reduce noise switching at the output.

The first of a two-stage register samples the state of the comparator on the leading edge of each clock pulse. The state of this stage provides the digital output of the delta modulator and up/down control signal to the step size counter. The second stage stores the state of the previous sample. An EX-OR gate is used to identify a change of sample polarity.

During the change of sample polarity signal, zeros or ones are loaded into the step size counter when incremental or decremental signal is applied, respectively, from the first-stage register. The counter is incremented or decremented if the two stages are in the same state. The step size counter consists of an UP/DOWN counter. When the delta value increases up to seven or the delta value decreases

down to zero, the control logic overflow control provides inhibit signal to stop the step size counter until the change of sample polarity.

The step size counter is connected to the digital integrator, consisting of an 8-bit parallel adder and holding register. The value of the step size counter is added to the contents of the accumulator every bit time. The new sum is clocked back into the holding register during the mid-bit time. Subtraction is accomplished with addition of two's complement when the step control signal is counting down.

In the add mode, a multifunction gate is forced to become an AND gate. When the most significant 5 bits are high, the overflow control generates an inhibit signal to stop adding step size to the accumulator. In the subtract mode, the gate becomes a NOR gate. When the most significant 5 bits are low, the overflow control generates an inhibit signal to stop subtracting step size from the accumulator.

The accumulator output feeds an 8-bit D/A converter/buffer section which generates scaled analog signal for comparison with the voice input. The maximum count is between 248 to 256 units.

### 12.3.3.8 Output Formatter and Controller

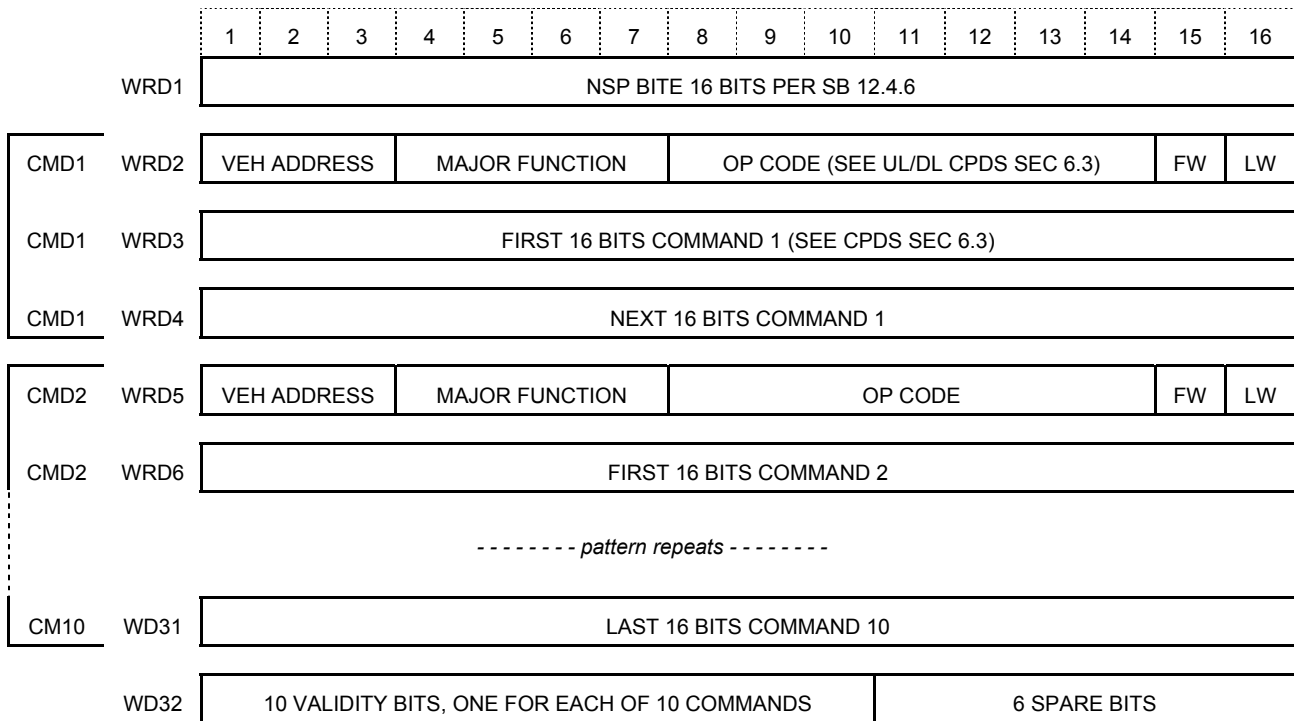
#### A. Description

The output formatter and controller is designed to respond to the DPS MDM by means of a message discrete pulse and a word discrete pulse for retrieval of each data word.

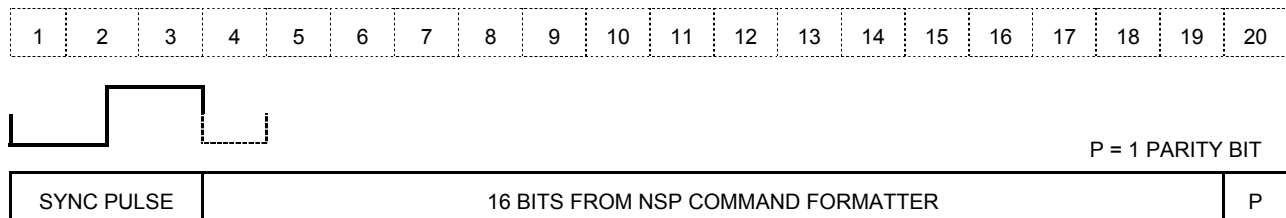
Upon receipt of a word discrete pulse, a sync word is generated, followed by 16 bits of BITE status, command, or validity data, and a parity bit. The Manchester II (bi $\phi$ -L) data are sent to the DPS/MDM.

#### B. Serial word format

Figure 12-8 shows the NSP data output format before the three bits of word sync and odd parity bit are added to the total data that are transferred to the DPS MDM. The sync word, data word, and parity bit format is shown in Figure 12-9.



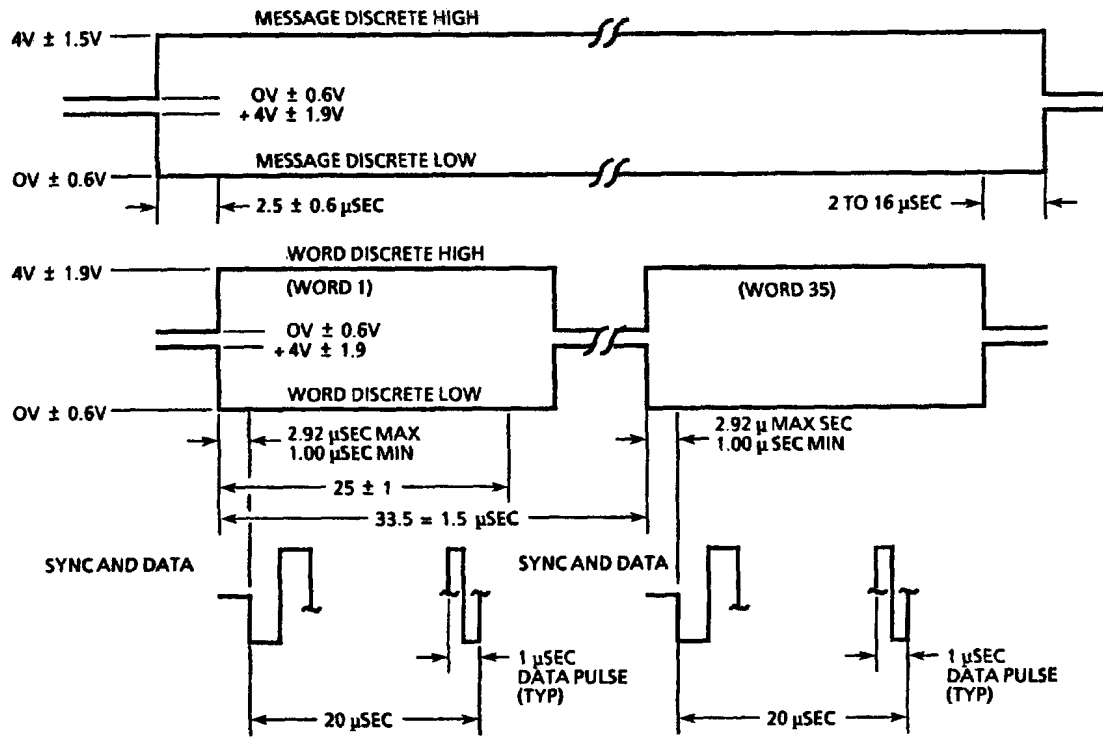
**Figure 12-8. NSP data output format**



**Figure 12-9. NSP DPS/MDM word format**

C. NSP-DPS MDM serial bit retrieval discrettes

The message discrete (MSG DISC) and word discrete (WORD DISC) relationships are shown in Figure 12-10. The word discrete goes high at the beginning of each word and then goes low at the completion of the word transfer.



NOTE: All voltages referenced to NSP signal ground

Figure 12-10. NSP DPS/MDM data retrieval discrete

D. Forward link frequency generator

The word discrete goes high and enables the Forward Link Frequency Generator (FLFG) to output. the 4-MHz clock is used to derive the output square wave clock signals for the various logic outputs. The clock timing wave form is shown in Figure 12-11.

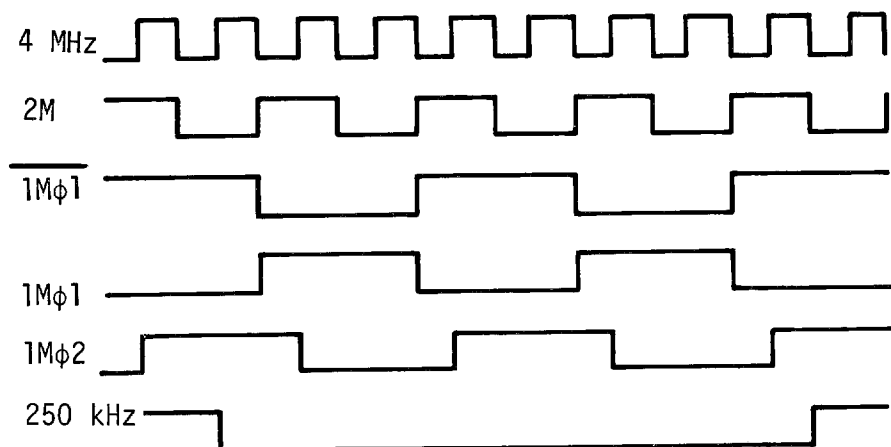


Figure 12-11. Forward link generator outputs

E. Control flip flops

The control flip-flops clocked by  $1M\Phi 1$  and  $1M\Phi 2$  generate ENABLE 1 and SYNC TRIG if Parity (PAR) signal is high and the clear input is low. The clear input causes ENABLE 1 and SYNC TRIG to go low if BLOCK ALL is high (selected) and the word counter is in the word 2 to 31 state (word 1/32 is low). Note that the clear input in this case inhibits the data output driver after word 1 has been transmitted by ENABLE 1 going high. ENABLE 1 is also high between WORD DISC request.

The control flip-flops are also cleared by the initialize signal when the NSP is turned on or the input voltage drops below 24 V dc.

F. Word counter (32)

The word counter, clocked by SYNC TRIG going low, counts each word discrete request and controls the data processing as required. The word counter is reset to zero when the message discrete goes high. Each word discrete causes a sync trigger low output pulse from the control flip-flops and the counter increments. The output of the word counter provides an address to the data MUX and clock DEMUX to gate the BITE status, command data, and validity clocks at the proper time and sequence.

G. Data MUX and data reclock flip-flop

Serial BITE, command, and validity data from the data MUX are reclocked by the  $1M\Phi 1$  (1-MHz) clock. The data reclock flip-flop is cleared if a disable flag is received during word 2 through 32 time period of the second data request during the 200-msec data time period. This inhibits the output of command and command validity data, and no data are sent to the MDM for words 2 through 32.

H. Biphase converter

The serial BITE, command, and status data are clocked through the converter by  $1M\Phi 2$  (1-MHz) clock. The data switch is only enabled during the send data bits 1-16 period, which is controlled by the AND gate (PAR .SEND DATA).

I. Odd parity generator

The serial data are input to the odd parity generator where the bits which are high are tracked, and if an odd number of ones occurs, a 1 bit is added at the end of the 16-bit word.

The  $1M\Phi 1$  clock is used to clock a J-K flip which is tracking the receipt of an even or odd number of one's. The  $1M\Phi 2$  clock gates the parity exclusive OR gate which outputs the parity bit. The PARITY control signals gate the decision output of the parity generator at the parity bit time slot in the data word.

J. Sync Pattern Generator

The sync pattern generator outputs a 3-bit nonvalid Manchester II code. This output is added to the front end of the data word through the sync/data/parity OR gate.

The sync data signal (Q5 output) is generated as follows:

SYNC TRIG going low as a result of word discrete request gates the 2-MHz clock to sequence the sync pattern generator (five-stage shift register). The Q4 output is used to produce the send data signals from the data enable flip-flops.

K. Bit counter (16)

The bit counter is loaded with zero by SYNC TRIG and enabled to be incremented by WORD DISC. The counter counts 16 clock pulses (data bit periods) and outputs a PARITY signal to add the parity bit to the 16-bit word plus sync data.

- L. The data enable flip-flops provide SEND DATA DELAYED and SEND DATA signals. The output sequence starts as follows after ENABLE 1 (EN 1) clears SEND DATA and PARITY has cleared (send data delayed): Q4 output of the sync pattern generator (five-stage shift counter) goes high as a result of the word discrete request input to the word discrete send data AND gate output, removing the reset to the sync pattern generator and allowing the sync clock input pulses to increment the sync pattern generator.

When Q4 goes high, send data goes high clocked by 1MΦ1, allowing the biphasic converter to pass data. Send data delayed goes low after Command Enable (CEN) goes high when clocked by 2M, allowing the 1MΦ1 clock to generate the data clocks (BITE CLK, CMD CLK, and validity CLK).

M. Timing diagram

The timing relationship between the key signals controlling the data flow requests and output is shown in Figure 12-12.

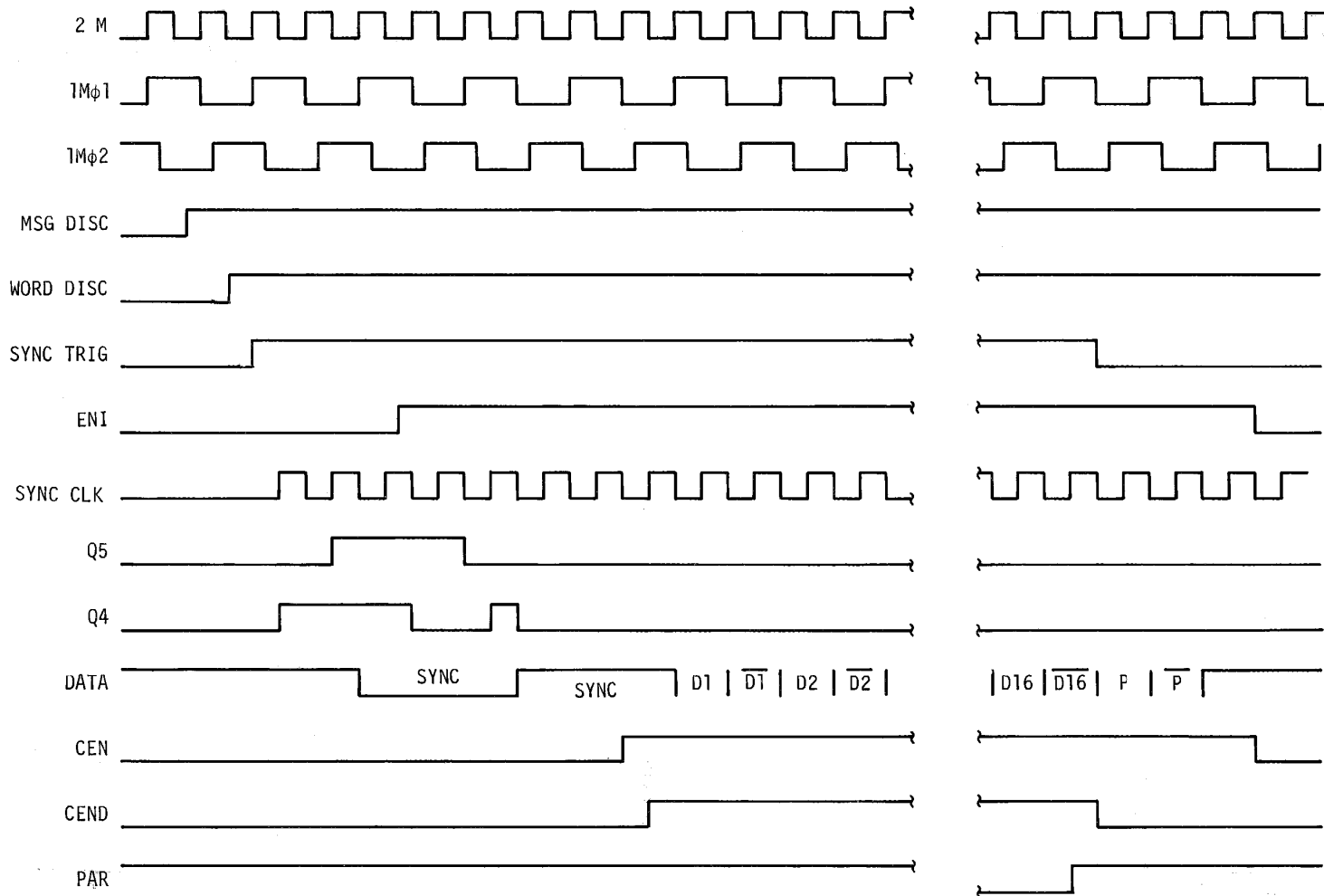


Figure 12-12. NSP output formatter and controller timing



### 12.3.3.9 Doppler Buffer

The Doppler buffer demultiplexes, stores, and delays the received station ID data. If bracket data status is high from the previous frame, the station ID data are transmitted to the Doppler extractor. This output is not used.

### 12.3.4 Forward Link Support

#### 12.3.4.1 Uplink Programmer

The uplink programmer provides timing signals for demultiplexing the uplink voice, command, and Doppler station ID as shown in Table 12-2.

**Table 12-2. Uplink program**

| Program location             | Command Duration | Low rate format demultiplexing programs                    |
|------------------------------|------------------|--|
| 0/ LOWRATE: DOP ENABLE       | 8                | Send 8 bits to Doppler extractor                           |
| 1 VOICE AG1 ENABLE           | 96               | Send 96 bits to voice channel 1                            |
| 2 NOP                        | 1                | Discard 1 bit  |
| 3 BCH 1 ENABLE               | 2                | Send two information bits to BCH decoder only              |
| 4 CMD ENABLE BCH 1 ENABLE    | 29               | Send 29 information bits to command buffer and BCH decoder |
| 5 VOICE AG1 ENABLE           | 96               | Send 96 bits to voice channel 1                            |
| 6 CMD ENABLE<br>BCH 1 ENABLE | 19               | Send 19 more bits to command buffer and BCH decoder        |
| 7 BCH 2 ENABLE               | 13               | Send 13 parity bits to BCH decoder                         |
| 8 VOICE AG1 ENABLE           | 96               | Send 96 bits to voice channel 1                            |
| 9 BCH 2 ENABLE               | 32               | Send 32 parity bits to BCH decoder                         |
| 10 VOICE AG1 ENABLE          | 96               | Send 96 bits to voice channel 1                            |
| 11 BCH 2 ENABLE              | 32               | 32 parity bits to BCH decoder                              |
| 12 VOICE AG1 ENABLE          | 96               | Send 96 bits to voice channel 1                            |
| 13 FRAME ENABLE              | 24               | Send 24 frame sync bits                                    |
| 32 HIRATE: DOP ENABLE        | 8                | High rate format demultiplexing program                    |
| 33 VOICE AG1 ENABLE          | 128              | Send 128 bits to voice channel 1                           |

*Table 12-2. Uplink program (continued)*

| Program location              | Command Duration | Low rate format demultiplexing programs                      |
|-------------------------------|------------------|--|
| 34 VOICE AG2 ENABLE           | 128              | Send 128 bits to voice channel 2                             |
| 35 NOP                        | 1                | Discard a bit  |
| 36 BCH 1 ENABLE               | 2                | Send two information bits to BCH decoder only                |
| 37 CMD ENABLE<br>BCH 1 ENABLE | 29               | Send 29 information bits into command buffer and BCH decoder |
| 38 VOICE AG1 ENABLE           | 128              | Send 128 bits to voice channel 1                             |
| 39 VOICE AG2 ENABLE           | 128              | Send 128 bits to voice channel 2                             |
| 40 CMD ENABLE BCH 1<br>ENABLE | 19               | Send 19 more bits to command buffer and BCH decoder          |
| 41 BCH 2 ENABLE               | 13               | Send 13 parity bits to BCH decoder                           |
| 42 VOICE AG1 ENABLE           | 128              | Send 128 bits to voice channel 1                             |
| 43 VOICE AG2 ENABLE           | 128              | Send 128 bits to voice channel 2                             |
| 44 BCH 2 ENABLE               | 32               | Send 32 parity bits to BCH decoder                           |
| 45 VOICE AG1 ENABLE           | 128              | Send 128 bits to voice channel 1                             |
| 46 VOICE AG2 ENABLE           | 128              | Send 128 bits to voice channel 2                             |
| 47 BCH 2 ENABLE               | 32               | Send 32 parity bits to BCH decoder                           |
| 48 VOICE AG1 ENABLE           | 128              | Send 128 bits to voice channel 1                             |
| 49 VOICE AG2 ENABLE           | 128              | Send 128 bits to voice channel 2                             |
| 50 FRAME ENABLE               | 24               | Send 24 frame sync bits                                      |

A. Program counter

The program counter addresses the instruction store Read-Only Memory (ROM) to provide the next instruction each time carry goes low. During the time the NSP is acquiring sync, the programmer is resynchronized by ACQ going high after the recognition of the first sync correlation.

B. Instruction store

The instruction store ROM loads the bit counter with the duration of the instruction (in bit periods) and loads the latch decoder with the desired timing functions listed in Table 12-3.

**Table 12-3. Latch decoder functions**

| <b>Latch decoder code</b> | <b>Timing function (output)</b> |
|---------------------------|---------------------------------|
| 0                         | FRAME ENABLE                    |
| 1                         | DOP ENABLE                      |
| 2                         | VOICE AG1 ENABLE                |
| 3                         | VOICE AG2 ENABLE                |
| 4                         | CMD ENABLE AND BCH 1 ENABLE     |
| 5                         | BCH 1 ENABLE                    |
| 6                         | BCH 2 ENABLE                    |
| 7                         | (no output)                     |

**C. Bit counter**

The bit counter receives a count from the instruction store ROM which is the duration of the instruction in bit periods. The uplink clock decrements the counter to zero (terminal count), which causes carry to increment the program counter, and the next instruction begins.

**12.3.4.2 Power Converter**

A buck-boost power circuit is used to provide input-output electrical transient isolation and multiple regulated output voltages. The nominal switching frequency is 43 kHz at 28 V dc. Output voltage sensing is from the +10 V dc output for close-loop voltage regulation.

**A. Input filter**

A two-stage L-section filter is used to control Electromagnetic Interference (EMI).

**B. Starting circuit**

The starting circuit provides a positive pulse to the power transistor at turn on, and then switches to the active mode after the converter moves into steady state operation.

C. Driver

Driver Q1 is used as a power switch and is cyclically turned on and off by the duty cycle generator, which keeps the load voltage constant when the input voltage changes.

D. Output filters and rectifiers

Voltages from the secondary windings of transformer T1 are diode rectified and filtered to provide the voltage and ripple voltage requirements.

E. Integrator and bistable comparator

The average dc output voltage and the quasisquare wave ac feedback signal fed into the integrator provide a triangular voltage into the bistable comparator, which is used as a threshold detector.

The bistable comparator compares the reference voltage magnitude with the instantaneous magnitude of the triangular voltage and then generates a binary voltage of either a high or low at the output of the comparator.

F. Input/output isolation and duty cycle generator

The feedback control is isolated from the input circuit by a transformer with a square-loop flux versus Magneto Motive Force (MMF) characteristic used in the duty cycle generator to provide a control signal to driver Q1.

## 12.4 SUMMARY BITE

The summary BITE circuit generates NSP BITE bits for transmission to the BFS and GNC GPC(s) through FF1 and FF3 MDMs

### 12.4.1 Voltage Comparator (Secondary Power Check)

The voltage comparator acts as a power glitch detector and a 10-V supply output low voltage detector ( $\leq 8.6$  V). Under normal operations, the output is low. Fast power glitches result in a 100-microsec pulse which will reinitialize the NSP. When either a low voltage condition exists or a power glitch has occurred, the secondary power check bit is set high.

### 12.4.2 Forward Link Voice Demultiplexer Check

Voice A/G 1 and A/G 2 input check logic and voice A/G 1 and A/G 2 output check logic are determining if the FWD link audio clock generator or the uplink programmer is sending too many (overflow) or too few (underflow) bits per frame to voice buffer A/G 1 or voice buffer A/G 2, or if the voice buffers are failing and are periodically empty or full.

The Demultiplexer (DEMUX) check logic will detect these error indications and, when an error is detected, will set the DEMUX check bit high in the BITE status word and reinitialize the voice buffers by setting the VOICE INIT line high.

### 12.4.3 Record Mode Processor (RMP BITE)

The PCM units generate a fixed frame sync pattern, beginning on the rising edge of the 100-pps signal. In the vdata mode, (data/vdata mode control line low), these biphasic data are converted to NRZ data, multiplexed with voice data, and the result reconverted to biphasic data. In the data mode (RCD data/vdata high), the PCM data are gated directly through to the output.

The latter mode is of little interest to BITE, as it involves only a few gates. The vdata mode is of prime importance, as it tests the majority of the Record Mode Processor (RMP) circuitry. Two bits of the biphasic frame sync pattern in the output data stream (biphase 1 and 0) are examined for accuracy. If either of the bits are incorrect or not biphasic encoded, an error will be indicated. The PCM frame sync pattern is shown below.

Examine these bits (6th and 7th)

1 1 1 1 1 0 1 0 1 1 1 1 0 0 1 1 0 0 1 0 0 0 0 0

The RMP BITE will be operating at all times, and the summary BITE ignores the error flag in the data mode.

Operation - The first PCM frame sync bit will be transmitted from the RMP on the 129th rising edge of RM 384 kHz after RM SYNC fires. The sixth and seventh bits of the sync pattern will be in the register after the 142nd falling edge of RM 384 kHz. By starting the countdown at 141, when the counter reaches 0, the sixth and seventh biphasic sync bits will be in the BITE register as "0-1-1-0".

If a discrepancy occurs, the RECORD MODE MUX check bit goes HIGH until reset by word discrete.

Note that the RMP BITE is reset LOW when in the record data only mode and the ENCR ALL mode.

### 12.4.4 Bit Sync Quality and Bit Sync Lock Logic

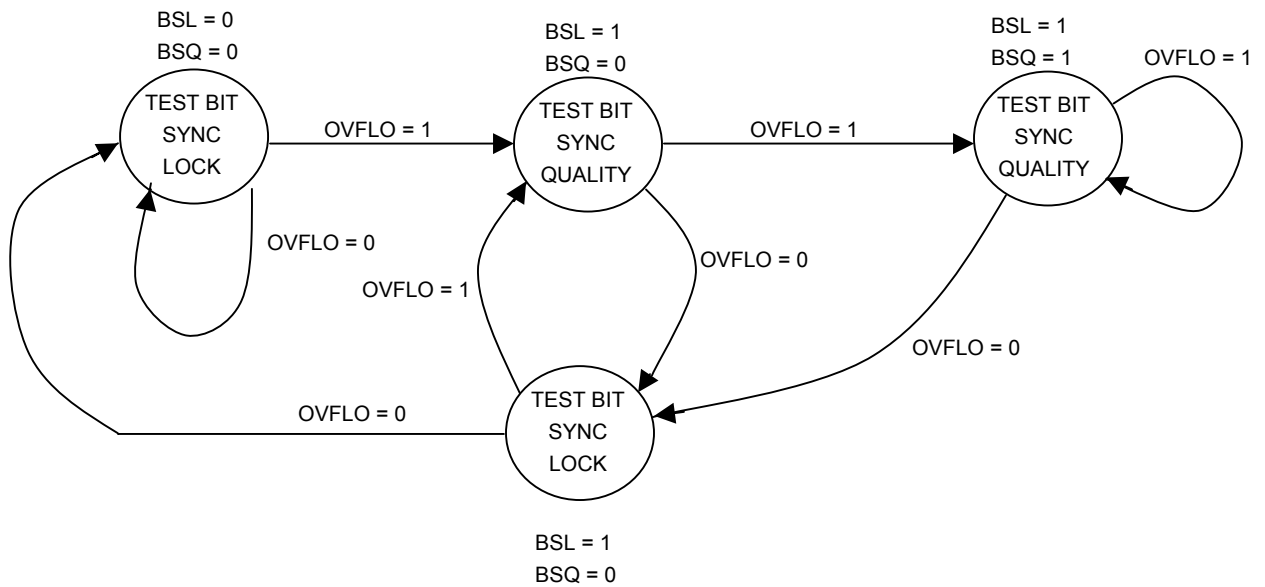
The Bit Sync Quality (BSQ) and Bit Sync Lock (BSL) logic determines if the bit synchronizer

- A. Is in lock
- B. Has a signal above a certain quality level

It performs these two functions by varying the value of the threshold sent to the bit sync, waiting for 40,960 uplink data bit periods, and then examining whether or not the signal is above that threshold ( $10^{-2}$  BER).

The threshold sent to the bit synchronizer is determined by the mode of the NSP in the bit sync threshold logic on the mode control circuit.

The BSL and BSQ circuit on the summary BITE board performs the various operations shown in Figure 12-13.



- Notes:
1. Bit sync lock detector requires a maximum of 32K bits after threshold has been set to produce a stable value on overflow (OVFLO = 1).
  2. BSQ and BSL BITE data inverted relative to the states on this diagram.

**Figure 12-13. BSQ and BSL state diagram**

The bit sync threshold values for the various modes of the NSP are shown in Table 12-4.

**Table 12-4. Bit sync threshold values**

|                          |             |
|--------------------------|-------------|
| Lock                     | > -5 dB SNR |
| Quality NON-ENCR coded   | -3 dB SNR   |
| Quality ENCR coded       | 0 dB SNR    |
| Quality NON-ENCR uncoded | +4 dB SNR   |
| Quality ENCR uncoded     | +7 dB SNR   |

### 12.4.5 MDM BITE Register

The MDM BITE register stores and then sends BITE data to the output formatter and controller upon demand from the DPS/MDM.

Bits shifted out of the MDM BITE register are recycled through the flip-flop, so that, if the new data are locked out from entry to the register, the BITE status word will repeat. This will occur if the MSP is polled twice in the 200-msec command buffer fill time.

When DATA READY is LOW and Message (MSG) DISC is low, BITE data appearing on the parallel inputs are loaded into the register. When DATA READY is HIGH or MSG DISC is HIGH, the status word is ready for transmission.

The MDM BITE register is loaded (updated) continuously until the message discrete or data ready is HIGH.

### 12.4.6 MDM BITE Register Outputs

V92X6081X Data Ready Stat B1 RDY = ("1") NO = ("0")

NSP Serial Input/Output (SIO) word 1 bit 1 parameter

RDY - Indicates one command word in the 10-command double buffer has passed

- BCH DECODER CHECK
- BRACKET DATA STATUS CHECK
- VALID VEHICLE ADDRESS CHECK (any nonzero address)
- BUFFER FILL TIME COMPLETE

NO - Indicates no commands received or no valid commands received.

V92X6082X NSP CMD PATH B2 BLK = ("1") CMD = ("0")

NSP SIO word 1 bit 2 parameter

BLK - Indicates panel C3, UPLINK BLOCK switch in the NSP BLOCK position and only word 1, the status word, is transmitted. The NSP will not allow the CMD words or the validity word to be transmitted.

CMD - Indicates panel C3, UPLINK BLOCK switch in the ENABLE or GPC BLOCK position, or power was lost to the switch.

V92X6083X Bit SYNC Lock B3 LOSS = ("1") BIT = ("0")

NSP SIO word 1 bit 3 parameter

BIT - Indicates the NSP bit sync threshold detector threshold has been exceeded and the bit sync is in lock. Lock occurs at > -5 db SNR.

(1 X 10 Bit Error Rate (BER))

LOSS - Indicates the NSP bit sync is out of lock due to one or more instances of bit synchronization loss.

V92X6084X Frame SYNC Lock B4 LOSS = ("1") FRM = ("0")

NSP SIO word 1 bit 4 parameter

FRM - Indicates the NSP frame sync lock logic has detected two consecutive frame sync correlations with three or less frame sync errors.

LOSS - Indicates the NSP frame sync lock logic has detected three consecutive frame sync correlation failures and the NSP forward link data processing is inhibited.

V92X6085X Bracket Data B5 LOSS = ("1") BRKT = ("0")

NSP SIO word 1 bit 5 parameter

BRKT - Indicates the NSP sync lock logic has indicated lock and has received two consecutive valid frame sync correlations, and the data bracketed by the sync correlations are valid.

LOSS - Indicated one or more frame sync correlation failures have occurred, and NSP command and Doppler data processing is inhibited.

V92X6086X DEMUX UPLINK VOICE Check B6 FAIL = ("1") NORM = ("0")

NSP SIO word 1 bit 6 parameter

FAIL - Indicates a data overflow or underflow condition has been detected in one or both forward link voice buffers because of a timing or data transmission error.

NORM - Indicates both forward link buffers are operating properly in HDR or LDR or no signal is present.

V92X6087X MUX DOWNLINK VOICE Check B7 FAIL = ("1") NORM = ("0")

NSP SIO word 1 bit 7 parameter

FAIL - Indicates a data overflow condition has been detected in one or both return link voice buffers due to a timing or data transmission error.

NORM - Indicates all other conditions.

V92X6088X Internal Mode B8INTL = ("1") EXTL = ("0")

NSP SIO word 1 bit 8 parameter

INTL - Indicates the NSP has detected a failure of the PCMMU sync word in three successive frames, or failure of the 100-pps sync signal or 1.152-MHz clock. The NSP



in the internal mode provides the data stream with a sync pattern and alternating I's and O's in the TLM data (PCMMU) blocks. Voice data are available in this mode.

EXTL - Indicates normal operation of the NSP.

V92X6089X SEC PWR Check B9 FAIL = ("1") NORM = ("0")

NSP SIO word 1 bit 9 parameter

FAIL - Indicates a momentary loss of the NSP 10 V regulator output and the NSP data will be in error at the time of the undervoltage.

NORM - Indicates the 10-V regulator is operating properly and input voltage is greater than 24-V dc.

V92X6090X RCD Mode MUX B10 FAIL = ("1") NORM = ("0")

NSP SIO word 1 bit 10 parameter

FAIL - Indicates one or more errors have been detected in bits 6 ("0") and 7 ("1") in the record mode frame sync pattern. Check is only done in the record data/voice mode.

NORM - Indicates all other conditions.

V92X6091X Bit SYNC QUAL B11 FAIL = ("1") NORM = ("0")

NSP SIO word 1 bit 11 parameter

FAIL - Indicates the data level is below threshold level. Threshold levels are set at a given signal to noise ratio dependent on the mode selected as follows: LOCK -5 dB, NON-ENCR CODED -3 dB, ENCR CODED 0 dB, NON-ENCR UNCODED +4 dB, and ENCR UNCODED +7 dB. Minimum BER for lock is  $10^{-2}$ .

NORM - Indicates signal above the mode threshold and bit sync is in lock.

V92X6092X BCH VAL B12 VAL = ("1") No = ("0")

NSP SIO word 1 bit 12 parameter

VAL - Indicates at least one correct decoded message has occurred since the last MDM polling. Messages are checked for BCH code and nonzero vehicle address.

NO - Indicates no commands were sent or all commands sent failed the above checks.

V92X6093X BCH INVAL B13 INVL = ("1") No ("0")

NSP SIO word 1 bit 13 parameter

INVL - Indicates at least one incorrect BCH decoded message has occurred since the last MDM polling.

NO - Indicates no commands were sent or all commands passed the BCH check.

V92X6094X Mode Parity Even B14 EVEN = ("1") Blank = ("0")

NSP SIO word 1 bit 14 parameter

EVEN - Indicates the mode logic equation is a logic "1".

$$(PS + ENCODING) + (DECODING + DOD) + (RCV HI) = "1"$$

See Table 12-5 for possible combinations.

V92X6095X Mode Parity Odd B15 ODD = ("1") Blank = ("0")

NSP SIO word 1 bit 15 parameter

This parameter is the logic inversion of V92X6094X MODE PARITY EVEN.

V92X6096X NSP Status B16 FAIL = ("1") GOOD = ("0")

NSP SIO word 1 bit 16 parameter

GOOD - Indicates the proper operation of the forward link voice (A/G 1 and A/G 2) buffers, the return link voice (A/G 1 and A/G 2) buffers, and that there has not been an NSP 10-V dc supply undervoltage condition. Failure of any one of these functions for 0.5 second or more will cause the parameters to indicate FAIL.

**Table 12-5. Mode parity check**

| <b>Mode</b> | <b>PS</b> | <b>ENC</b> | <b>DEC</b> | <b>DOD</b> | <b>HI</b> | <b>Parity V92X6094X</b> |
|-------------|-----------|------------|------------|------------|-----------|-------------------------|
| TDRS        | 0         | 1          | 1          | 0          | 0         | 0 (Odd)                 |
| STDN - LO   | 0         | 0          | 0          | 0          | 1         | 1 (Even)                |
| STDN - HI   | 0         | 0          | 0          | 0          | 1         | 1 (Even)                |
| SGLS (1)    | 0         | 0          | 0          | 1          | 1         | 0 (Odd)                 |
| SGLS (2)    | 1         | 0          | 0          | 1          | 1         | 1 (Even)                |
| SGLS (3)    | 0         | 0          | 0          | 1          | 0         | 1 (Even)                |
| SGLS (4)    | 1         | 0          | 0          | 1          | 0         | 0 (Odd)                 |
| SGLS (5)    | 0         | 0          | 0          | 0          | 1         | 1 (Even)                |
| SGLS (6)    | 0         | 0          | 0          | 0          | 0         | 0 (Odd)                 |

## 12.5 NSP UPMODE LOGIC

### 12.5.1 General

The NSP-MDM command input serial data I/O transaction is a GPC Systems Software function that is handled by the GPC that has the flight critical bus assigned to it; this GPC, normally assigned to the GNC major function, controls appropriate parts of the process, such as the I/O reset.

The software uses a bus masking scheme to determine whether or not to upmode NSP data I/O. Although the NSP I/O uses somewhat standard BCE bypass logic, the logic for restoring NSP data I/O is uniquely tailored to accommodate swapping NSP's as a function of the comm management process.

The Systems Software maintains the status of each NSP as either "current" for the active NSP or "alternate" for the bypassed NSP. After an I/O reset or port mode on the affected flight critical string, NSP polling is restored only to the "current" NSP.

With a nominal NSP swap, the upmode logic will redesignate the new NSP as "current" and the old as "alternate" only after, first, the old "current" NSP data is bypassed, and second, the old "alternate" power discrete is set high. An I/O reset is not needed for the upmode to occur.

After the old "current" NSP is bypassed, the Systems Software will begin looking for the power discrete on the old "alternate" NSP only; if the old "current" NSP is powered back on at this time, the data I/O can be restored with a GNC I/O reset. Also, if the "alternate" power discrete suddenly fails high, the logic will not attempt to "swap" NSP's until the "current" NSP is bypassed.

Notably, if the NSP swap is commanded into a failed power discrete on the "alternate" NSP, the upmode will not automatically complete for the new NSP. For this case, the following action is needed to restore the NSP data I/O: the NSP power discrete status must be comm faulted with a power cycle of either FF1(3) MDM, regardless of which NSP is being upmoded, followed by a GNC I/O reset (BFS I/O reset if engaged). When this occurs, both NSP data paths will be temporarily upmoded until the unpowered NSP is again bypassed, and the NSP's will be redesignated. After this, the newly designated "current" NSP will be the one to be polled after each I/O reset or port mode.

The information above was provided by PASS User Note 34656.

### 12.5.2 GPC Interface Notes

#### 12.5.2.1 I/O ERROR, BCE

A PASS I/O ERROR denotes detection of a System Software I/O error that generally results in down-modding, or a cessation of all polling from the affected I/O, although GPC commanding through the MDM may not be terminated (e.g., I/O ERROR FF3 would indicate that all transaction elements, including NSP2, are bypassed). BFS System Software works similarly, but the BFS application may use the I/O ERROR message for

loss of complete or partial I/O, and BFS doesn't necessarily cease all I/O polling (e.g., on the IP bus).

A BCE STRG x message is used by PASS to indicate a bypass of a specific I/O element, such as NSP, while not bypassing the remainder of the MDM interface. However, a BCE STRG x announced by the BFS indicates a loss of polling or tracking on the entire FC string. The "general" reason why the BFS needs its own I/O reset to resume tracking a string after the PASS is cleaned up is that the BFS always bypasses any string where the PASS bypass status is different from the BFS bypass status, and the BFS bypass and reset logic is different enough from the PASS bypass and reset logic that the BFS will remain bypassed during the PASS cleanup.

A BYP message is a PASS indication of a partial bypass on a particular interface, unless accompanied by an I/O ERROR.

### 12.5.2.2 Impacts to Commanding

Any time an FF MDM is power cycled, the data I/O between the MDM and GPC remains bypassed (including NSP command transactions) until I/O Reset is commanded (or via port mode). A Port Mode is a software function that includes a functional I/O Reset to restore data I/O to the port moded string (no additional I/O Reset is needed).

A GNC port mode performs the I/O reset only for the GNC function (an additional BFS I/O reset may be required to allow the BFS to regain tracking of the flight critical string).

If the failure is at the Flight Critical (FC) MDM (either FA or FF), then the BFS will not loose track, and will only bypass that MDM. If the failure is at the (GNC) GPC, then the BFS will stop tracking the entire string.

Here is a secret decoder ring using the OFS messages to differentiate between a failure at the MDM vs. at the GPC.

#### **Scenario #1 - Failure: Down at the MDM**

GNC issues an I/O ERROR FF1(2,3,4)

BFS issues an I/O ERROR FF1(2,3,4)

#### **Scenario #2 - Failure: Down at the GPC**

GNC issues an I/O ERROR FF1(2,3,4)

BFS issues a BCE STRING 1(2,3,4)

Here's a brief look at the logic: The GNC GPC issues a separate, special LISTEN command over the FC bus, before it ships out every "normal" command sequence (i.e., a command sequence for requesting data from a FC MDM). This LISTEN command is received by the BFS in order to prepare it for listening to an incoming data request. When the BFS is receiving these LISTEN commands, then it will continue to track the string. When the BFS is not receiving the LISTEN commands, then it will conservatively bypass the entire string. So for the case where the failure is at the MDM, the BFS is still receiving LISTEN commands going out from the GNC GPC, but it is not receiving the response from the MDM. Therefore it will annunciate the same I/O

ERROR FF1(2,3,4) message that the PASS issues, and will bypass that MDM only, and continue to track the rest of the flight critical string.

### 12.5.2.3 I/O TERM B(A)

An I/O TERM B is a GPC hardware inhibit to the GPC outputting anything on all FC buses (disables the transmitters for the 8 FC buses), such as fetching commands from the MDM. Since this shows up only as simple I/O ERROR FF1-4/FA1-4 fault messages on OFS, the TERM B must be announced by DPS. The problem could be in the GPC or the panel O6 OUTPUT switch. Data is available in the downlist to help DPS troubleshoot the failure.

An I/O TERM A is a GPC hardware inhibit for both PL buses and inhibits SM or BFS commanding via both PL buses. The symptom will appear as an I/O ERROR on both PL buses simultaneously, along with red bypass indications on INCO MGMT. Another possible problem with similar symptoms is called a silent takeover of the PL buses by the BFS. In this case, there will be no I/O ERROR annunciated on OFS, but both PL buses will show a red bypass indication on Orbit INCO MGMT. This can only be caused by an internal GPC error, and data is available in the downlist to help DPS troubleshoot the failure.

### 12.5.2.4 MDM OUTPUT Message

Per DPS SB Section 7.11.8, each PASS GPC periodically checks each FC and PL MDM interface that it is monitoring, using a mode equivalent to the dynamic wraparound test (same op code). The GPC in charge of the bus outputs a test command with alternating ones/zeros, followed by a command with the complementary pattern. All PASS GPCs that are monitoring that bus will check to make sure the MDM returns the same bit pattern, unless there has been an I/O ERROR downmoding on that bus. When a GPC detects two consecutive errors, it will annunciate the MDM OUTPUT x (FF1-4, FA1-4, PL1-2) message and stop this output mode processing until an I/O RESET or port mode occurs. The error could be on the GPC output or the MDM output to the GPC.

If the MDM OUTPUT message occurs for an FC MDM, DPS has additional BITE indications to try to isolate the failure. However, it is not always possible to isolate the failure, so all MDM inputs and outputs may be suspect unless cleared by an I/O RESET. SM does not have the same level of BITE processing available, so any time this message occurs, all MDM inputs and outputs are suspect unless cleared by an I/O RESET. BFS does not annunciate this message.

### 12.5.3 GNC Response to NSP Block

When NSP Block is active, the NSP will send only word 1 in response to a poll from the GNC. The GNC poll is the same regardless of NSP Block status. If the GNC sees only one word instead of 32 words returned in response to the poll (twice in a row), it will bypass the NSP polling until the next I/O reset, and it will not be looking for the power discrete on the alternate NSP as would happen with the NSP swap. BFS response to

NSP Block is not detailed in the Backup System Services document but appears to work similarly.

THIS PAGE INTENTIONALLY BLANK

**SECTION 13 - COMSEC**  
**CONTENTS**

| <b>Section</b> |  | <b>Page</b> |
|----------------|--|-------------|
| 13.1           | GENERAL DESCRIPTION .....                            | 13-1        |
| 13.2           | MCC PROCESSES DATA TO THE UPLINK DATA STREAM .....   | 13-1        |
| 13.2.1         | MCC Bose-Chaudhuri-Hocquenghen (BCH) Processor ..... | 13-2        |
| 13.2.2         | MCC Time Authentication .....                        | 13-2        |
| 13.2.3         | MCC Uplink Front End Processor .....                 | 13-3        |
| 13.2.4         | MCC COMSEC .....                                     | 13-3        |
| 13.2.5         | MCC Uplink Digital Stream .....                      | 13-3        |
| 13.3           | THEORY OF OPERATION .....                            | 13-4        |
| 13.3.1         | COMSEC Uplink Data Format .....                      | 13-4        |
| 13.3.2         | COMSEC Downlink Data Format .....                    | 13-5        |
| 13.4           | SUBSYSTEMS DESCRIPTIONS .....                        | 13-5        |
| 13.4.1         | Serial KG 28/46 Transmit Module .....                | 13-5        |
| 13.4.2         | Serial KG 57 Receive Module .....                    | 13-6        |
| 13.4.3         | Control Core Module .....                            | 13-6        |
| 13.4.4         | Frame Sync Circuit .....                             | 13-6        |
| 13.4.5         | Demultiplexer and Authenticate Module .....          | 13-7        |
| 13.4.6         | Time Authentication .....                            | 13-8        |
| 13.4.7         | BCH Check .....                                      | 13-9        |
| 13.4.8         | COMSEC Multiplexer .....                             | 13-10       |
| 13.4.9         | Power Supply .....                                   | 13-11       |
| 13.4.10        | Red and Black Input/Output Circuits .....            | 13-12       |
| 13.4.11        | Key Filler Port .....                                | 13-12       |
| 13.4.12        | BITE Assembly .....                                  | 13-12       |
| 13.5           | INSTALLATION .....                                   | 13-13       |
| 13.5.1         | Connector Data .....                                 | 13-13       |
| 13.5.2         | Cooling .....  | 13-16       |
| 13.5.3         | Weight .....   | 13-16       |
| 13.6           | DESCRIPTION OF CREW AND GROUND OPERATIONS .....      | 13-16       |
| 13.6.1         | Crew Controls .....                                  | 13-16       |
| 13.6.2         | Crew Display .....                                   | 13-17       |
| 13.6.3         | Ground Commands .....                                | 13-18       |
| 13.6.4         | Mode Telemetry .....                                 | 13-18       |
| 13.6.5         | BITE Status Telemetry .....                          | 13-19       |



| Section |  | Page  |
|---------|--|-------|
| 13.7    | OPERATIONAL NOTES .....                          | 13-21 |
| 13.7.1  | Ground Responses to BITE status Indications..... | 13-21 |
| 13.7.2  | ESTL Test Results .....                          | 13-21 |
| 13.7.3  | Alarm Meaning .....                              | 13-22 |
| 13.7.4  | Receiver False Lock.....                         | 13-22 |
| 13.7.5  | Operational Instructions .....                   | 13-22 |
| 13.8    | SPECIAL TELEMETRY COMPUTATIONS.....              | 13-23 |
| 13.9    | REFERENCES.....                                  | 13-23 |
| 13.10   | SUMMARY DATA .....                               | 13-23 |

## TABLES

| Table |   |       |
|-------|---|-------|
| 13-1  | Power Sources.....                            | 13-11 |
| 13-2  | Connect Descriptions .....                    | 13-14 |
| 13-3  | Mode Switch Functions .....                   | 13-17 |
| 13-4  | Commands to Configure the Downlink Rate ..... | 13-18 |
| 13-5  | COMSEC Telemetry Responses.....               | 13-18 |
| 13-6  | BITE Indications .....                        | 13-20 |

## FIGURES

| Figure |  |       |
|--------|--|-------|
| 13-1   | COMSEC Interface Diagram .....                       | 13-1  |
| 13-2   | 128 bit BCH Check.....                               | 13-2  |
| 13-3   | 128 bit Time Authentication Process.....             | 13-2  |
| 13-4   | One Frame of Multiplexed Command and Audio Data..... | 13-3  |
| 13-5   | General COMSEC Uplink Processor.....                 | 13-5  |
| 13-6   | Frame Sync State Diagram .....                       | 13-7  |
| 13-7   | IRIG-B Time Format from MTU .....                    | 13-9  |
| 13-8   | BCH Processor .....                                  | 13-10 |
| 13-9   | Power loss monitor circuit .....                     | 13-12 |
| 13-10  | COMSEC Connectors .....                              | 13-13 |
| 13-11  | Crew Controls .....                                  | 13-16 |
| 13-12  | SPEC 76 .....  | 13-18 |

## SECTION 13 COMSEC

### 13.1 GENERAL DESCRIPTION

Communications Security (COMSEC) equipment, also called the KGX-60, was developed by TRW Corporation to decrypt the uplink, Time Authenticate and BCH check commands, and encrypt the downlink from the orbiter. COMSEC 1 is hardwired to Network Signal Processor (NSP) 1 and COMSEC 2 is hardwired to NSP 2.

The NSP/COMSEC combination can operate in four primary modes (Receive, Transmit/Receive, All, or Bypass). Generally, shuttle missions only operate in the Receive mode so only the forward link to the orbiter is encrypted. These four modes can only be selected by the Crew Members via switches on Panel A1. For missions which require the downlink to be encrypted, the system can be operated in Transmit/Receive (TR) mode (NASA mode) where the forward and the return links are encrypted but the data going to the Solid State Recorders (SSRs) is not encrypted. "All" (Department of Defense mode) will encrypt the forward, return and data going to the SSRs.

The COMSEC has the capability to unencrypt/encrypt the NSP high data rate (HDR) or low data rate (LDR) NSP output.

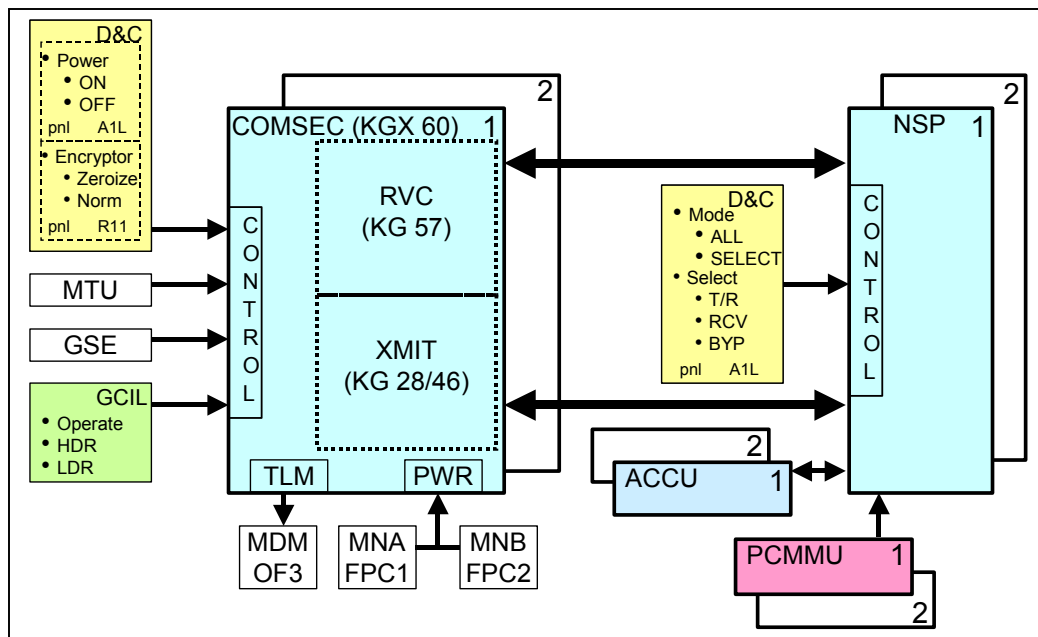


Figure 13-1. COMSEC Interface Diagram

### 13.2 MCC PROCESSES DATA TO THE UPLINK DATA STREAM

This section is a quick review of MCC processes to both Commands and Audio data within the uplink which should aid in understanding the Orbiter COMSEC Uplink Process.

### 13.2.1 MCC Bose-Chaudhuri-Hocquenghen (BCH) Processor

Generic Commanding Server (GCS) processes uplink 48-bit Command Words from the Flight Controller Workstation (namely INCO). The GCS will attach 2-dummy bits to the 48-bit Command Word. This 50-bit word is sent to the Bose-Chaudhuri-Hocquenghen (BCH) processor which outputs a 77-bit BCH Code. Next, the GCS processor will add 1-dummy bit to the beginning of the 50-bit word and attach the 77-bit BCH Code to the end of the 50-bit word outputting a 128-bit uplink word.

$$1 \text{ dummy bit} + [ ( 2 \text{ dummy bits} + 48 \text{ bit Command Word} ) + 77 \text{ bit BCH Check} ] = 128 \text{ bits}$$

Figure 13-2. 128 bit BCH Check

### 13.2.2 MCC Time Authentication

Next the GCS exclusive ORs the 128-bit uplink word to the current GMT time, represented as 128 bits (Time Authentication).

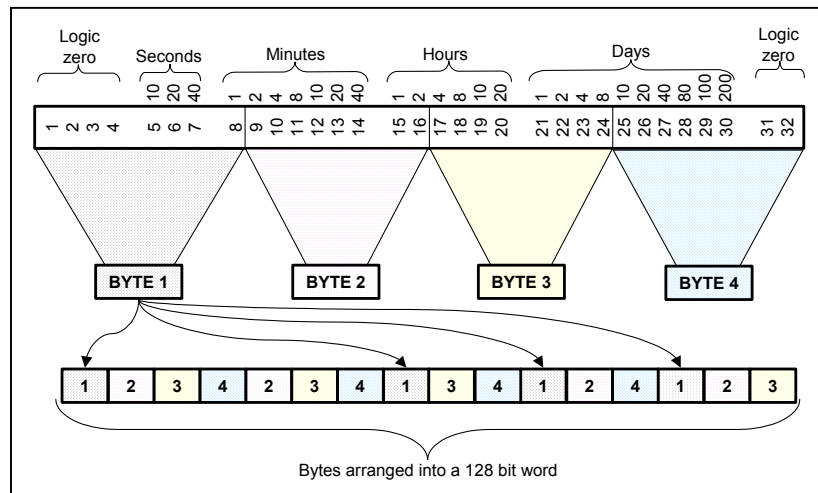


Figure 13-3. 128 bit Time Authentication Process

The time word is made up of 32 bits broken up in to four 8-bit bytes. These bytes are repeated sequentially to make up 128 bits so that the time word can be combined (exclusive Or'd) as described to make up the final command product for uplink. Figure 13-3 shows how this combination of bytes are done to make up the 128 bits of the time word.

Time is in 10 second increments with bits 31 and 32 set to zero. The bit increments are added together to give an accurate time to within 10 seconds. Example GMT 235/18:51:4x would be represented as "200 + 20 + 10 + 4 + 1 : 10 + 8 : 40 + 10 + 1 : 40" which is binary 0000 0011 0001 0100 0110 1010 1010 0100 or in hex 3146AA4.

The output of the GCS now is the Command Word that has been BCH Checked and Time Authenticated. This 128-bit digital uplink stream now exits the GCS and is shipped to the Uplink Front End Processor (FEP).

### 13.2.3 MCC Uplink Front End Processor

The 128-bits of command data is multiplexed, 32 bits at a time, with the audio for uplink to the orbiter. The first 32 bit byte does not include command data but does include the synchronization pattern (FAF320<sub>HEX</sub>) along with a station ID number, which is not used onboard the orbiter. There are two different formats that can be generated. The low data rate (LDR), at 32 KBPS, includes the command data and one voice channel uplink while, the high data rate (HDR), at 72 KBPS, includes the command data and 2 channels of voice. Figure 13-4 shows the output of this multiplexing process.

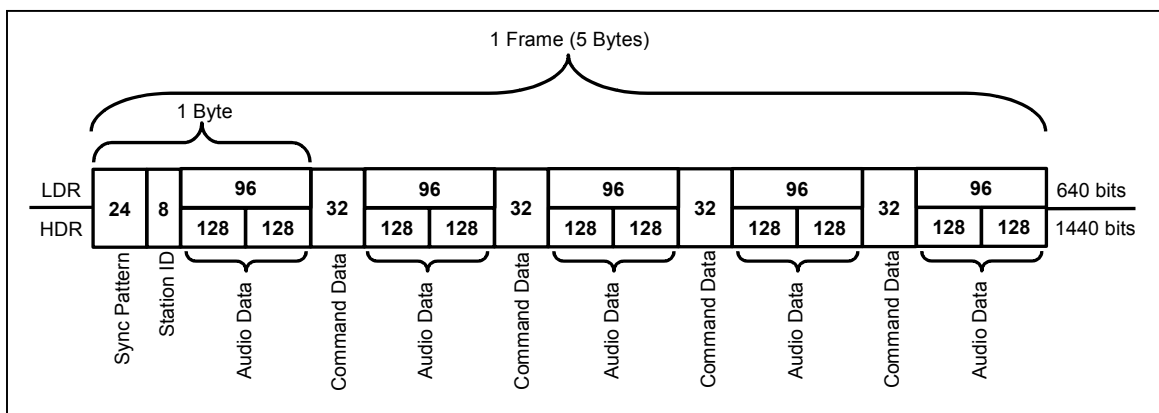


Figure 13-4. One Frame of Multiplexed Command and Audio Data

### 13.2.4 MCC COMSEC

After all the data has been multiplexed together in 1 serial digital stream, it is then routed to an MCC KG-60 to be encrypted for uplink to the orbiter at 50 frames/second.

### 13.2.5 MCC Uplink Digital Stream

The MCC will then uplink a continuous digital stream at either 72kbps or 32kbps. Remember the original Command Word and audio are embedded within this digital stream. In summary, the MCC Uplink is produced by the following series of processes:

Command → BCH → Time Authentication → Audio Multiplexed → Encrypted

It is important to understand that the **goal** is to have the Orbiter COMSEC and NSP pair “extract” the original 48-bit Command Word and Audio Signals out of the digital uplink stream; thus the Orbiter must **reverse** the MCC processes to extract the Audio and Commands.

### 13.3 THEORY OF OPERATION

The following paragraphs will detail how the COMSEC processes the encrypted uplink and downlink. Descriptions of the subsystems in the COMSEC are discussed later.

#### 13.3.1 COMSEC Uplink Data Format

The COMSEC receives the forward link (uplink) data from the NSP, after the NSP has bit synchronized the data. The COMSEC receives the uplink digital data stream which has been processed as follows in MCC.

Command → BCH → Time Authentication → Audio Multiplexed → Encrypted

The COMSEC takes the bits data and clock from the NSP bit synchronizer and first passes them through the serial KG 57 receive module to decrypt them. The uplink digital data stream now is unencrypted.

Command → BCH → Time Authentication → Audio Multiplexed

The COMSEC next determines where the 24-bit Frame Sync is located in the Uplink Digital Data stream and then demultiplexes the Audio data from the Command Data. The uplink digital data stream is now demultiplexed and the Air to Ground Loops are sent back to the NSP.

The Command Data Storage Logic will collect four 32-bit “command data” sections to assemble 128-bit uplink command data information which is still BCH and Time Authenticated.

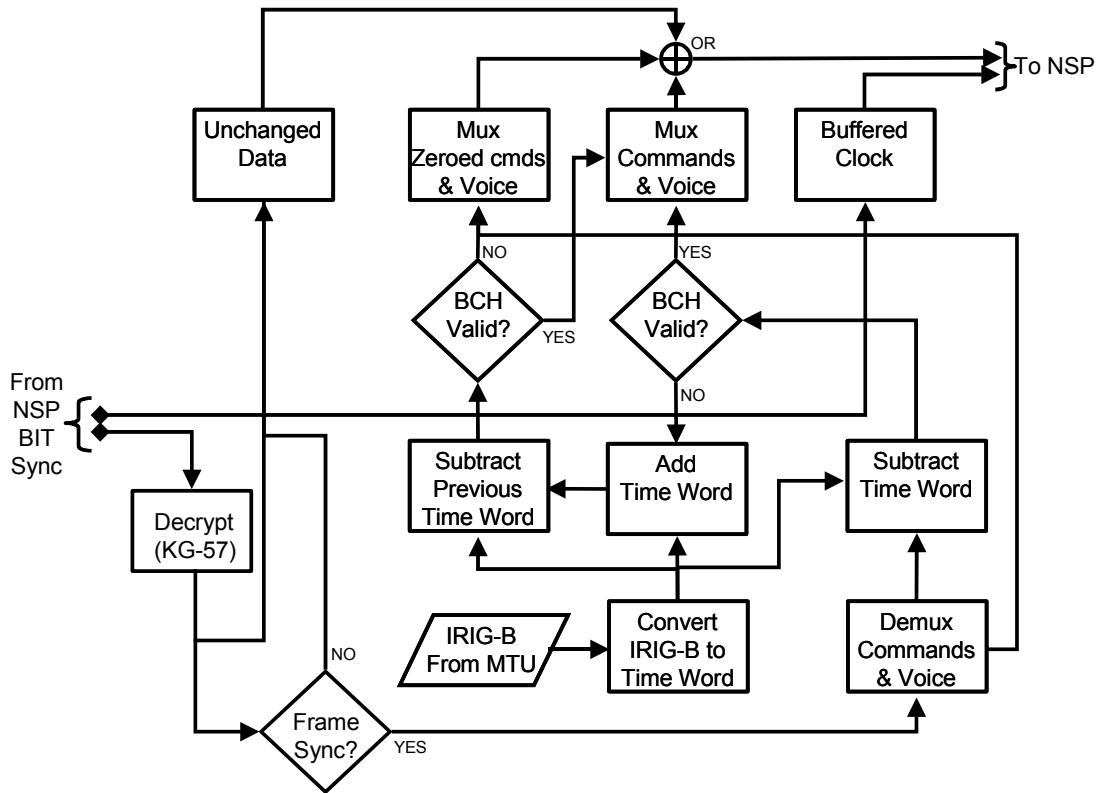
Command → BCH → Time Authentication

The COMSEC will process this 128-bit uplink command data by Exclusive ORing an onboard Time Authentication 128-bit signal to derive the following:

Command → BCH

The COMSEC will then remove the original 50-bit Word (2 dummy bits and 48-bit Command Word) and generate an independent Bose-Chaudhuri-Hocquenghen (BCH) code. If the uplinked 77-bit BCH Code matches the COMSEC generated BCH Code, the COMSEC will take the original uplink 128-bit Command + BCH checked data and send it to the COMSEC Output MUXer. This 128-bit Command + BCH checked data is multiplexed back with the audio data and sent to the NSP for more processing. In general, COMSEC Uplink Digital Output looks like:

Command → BCH → Audio Multiplexed



**Figure 13-5. General COMSEC Uplink Processor**

### 13.3.2 COMSEC Downlink Data Format

If the COMSEC is required to encrypt the downlink data in Transmit/Receive, the NSP sends the multiplexed data from the Pulse Code Modulation Master Unit and the Audio Central Control Unit (ACCU) to the COMSEC serial KG 28/46 transmit module. Once the data are encrypted, the COMSEC returns the data to the NSP for transmission to the downlink systems (S Band and Ku Band) as well as the Ground Support Equipment (GSE).

## 13.4 SUBSYSTEMS DESCRIPTIONS

The subsystems descriptions section explains the operation of each module, shown on Space Shuttle Systems Handbook, drawing 16.3 sheet 3, COMSEC 1/2.

### 13.4.1 Serial KG 28/46 Transmit Module

The KG 28/46 under the control of the core module performs a self-test and encrypts the downlink NSP High Data Rate (HDR) or Low Data Rate (LDR) as determined by the NSP configuration.

The Encryption device is classified.

### 13.4.2 Serial KG 57 Receive Module

The KG 57 under the control of the core module performs a self-test and decrypts the NSP uplink HDR or LDR data stream as determined by the NSP configuration.

The Encryption device is classified.

### 13.4.3 Control Core Module

The control core module provides control signals between itself and the serial KG 57 receive, serial KG 28/46 transmit, red I/O, black I/O, and DMA modules. Built-In Test Equipment (BITE) status data determined by this module are output to telemetry. Fill data input is processed in this module, as well as data rate control functions and the zeroize, standby, and power monitor functions.

### 13.4.4 Frame Sync Circuit

Frame sync is implemented using the same sync logic employed in the NSP. If the incoming sync pattern contains two or fewer errors, frame sync is declared valid.

If three or more errors are noted, frame sync is declared invalid and the plain text data are passed unchanged to the NSP, the NSP cannot frame sync since it has the same frame sync logic.

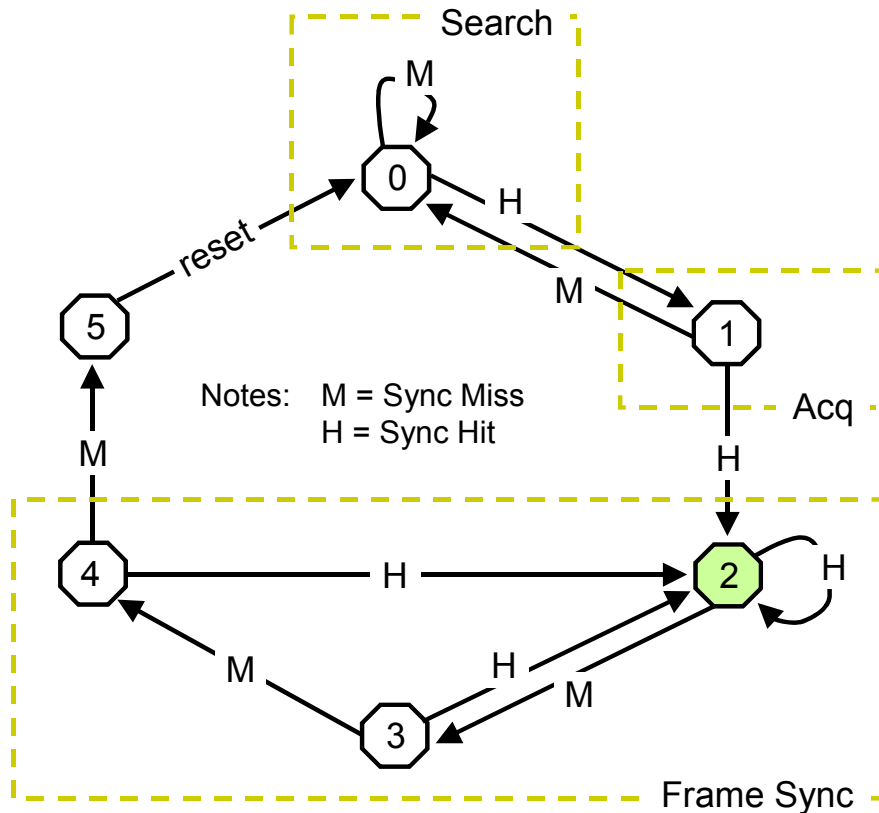
However if there is a COMSEC sync circuit failure, COMSEC LRU will not get a Frame Sync, but the NSP Frame Sync locks; in this specific case voice will still be available but commands will not pass the NSP BCH check because the CMD data are still time coded.

The frame sync circuit operates in the same way as the NSP frame sync circuit. The frame sync word detector monitors the states of the 24-bit shift register looking for the frame sync pattern (FAF320<sub>HEX</sub>). The presence or loss of sync is tracked by the frame sync counter and provides the decode logic with this information to determine system state.

The system states are:

- Search
- Acquisition
- Frame sync

The bit decoder mode is set by the data rate mux output and provides a count of 24 to the frame sync counter control, a fetch data signal for demultiplexing or remultiplexing the 128-bit command, and timing for the byte counter. Figure 13-6 shows the process for frame sync determination.



**Figure 13-6. Frame Sync State Diagram**

### 13.4.5 Demultiplexer and Authenticate Module

Once the COMSEC LRU achieves frame sync lock, the 128-bit command is demultiplexed from the data in the Demultiplex and Authenticate (DMA) circuit for separate processing. The audio data is sent on to be remux'd with either the valid command data or the "zeroed out" command data.

This module contains the processes for frame sync, command data storage, BCH and time authentication as well as some parts of the BITE logic.

#### 13.4.5.1 Command Data Storage Logic

The command data storage logic demultiplexes the 128-bit command in each frame and stores it in the 128-bit data register. These unauthenticated command data are then routed to the time authenticate circuit



### 13.4.6 Time Authentication

The Time Authentication Circuit receives the Command Data Storage Logic 128-bit data register input and the MTU IRIG Time Input and performs EX-OR ( $\oplus$ ) logic, i.e., Orbiter time is subtracted from command + MCC Time. The resulting command data are routed to the BCH authenticate circuit. The 128-bit command, which was demultiplexed from the audio data has the current time, which was received from the MTU, modulo-2 subtracted from it. If the time was the same as what was uplinked then what is left is the time authenticated command data. (If the MTU time differs from the uplinked time the command data can not pass the BCH check which is next).

#### 13.4.6.1 MTU Interface

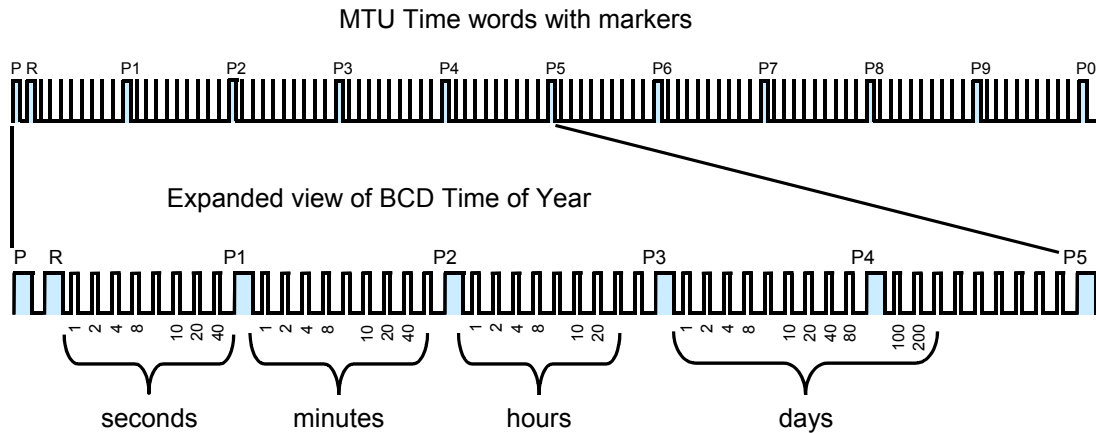
The COMSEC LRU receives an Inter-Range Instrumentation Group B (IRIG-B) time input from the Master Timing Unit (MTU). The IRIG-B time is used to construct the current 128-bit authenticating time word; the time word changes every 10 seconds. The current time word and previous time word are stored in registers in the time word storage circuit.

The time code output of the Master Timing Unit (MTU) is continually updated using Inter-Range Instrumentation Group (IRIG) modified time code format B. The format is modified so that the straight binary seconds that begins at index count 80 will not be generated. The IRIG format is unmodulated with a 100-pps output rate and a resolution of 10 msec. The IRIG-B format code will be transmitted with the least significant bit transmitted first. The MTU is deigned to preclude the possibility of any difference in time between the continually updated output and the demand output. The time will roll over at the end of year (day 365) to all zeroes, except that GMT days will be 001.

#### 13.4.6.2 Time Word Storage Circuit

The master clock is divided down to provide a 100-KHz clock and a 1-KHz clock. The 100-KHz clock is the timing clock for the command data storage logic, time authenticate circuit, and BCH authenticate circuit. The 1-KHz clock is used internally to process the IRIG-B time word.

Note: The Shuttle MTU does not follow modern IRIG-B format requirements. The pulses between the markers are added to create the time value while more modern IRIG-B formats use binary logic to create the time values from the pulses.



**Figure 13-7. IRIG-B Time Format from MTU**

The IRIG-B time word processing is illustrated in Figure 13-3, 128-bit timeword generation procedure. The timing counter determines the start of the IRIG-B time word and translates the IRIG-B code into logic 1's and 0's and sends this information to the data detector circuit that outputs the time word markers P1 through P9 to the marker counter. The marker counter counts to 5 and outputs the end-of-time word to the time word shift register and the greater-than-10-second compare logic.

The data detector also outputs the logic 1 and 0 data and enable signal to load the time word in the time word shift register.

The time word shift register outputs the 32-bit time word to the time word format multiplexer for reformatting into 128 bits. The 10-second and 20-second bits are also output and are used to determine the time word transfer control to the time word storage circuit.

The transfer time word signal from the greater-than-10-second compare logic is used by the time word storage circuit as a queue for storing the new or the new  $\oplus$  old time word.

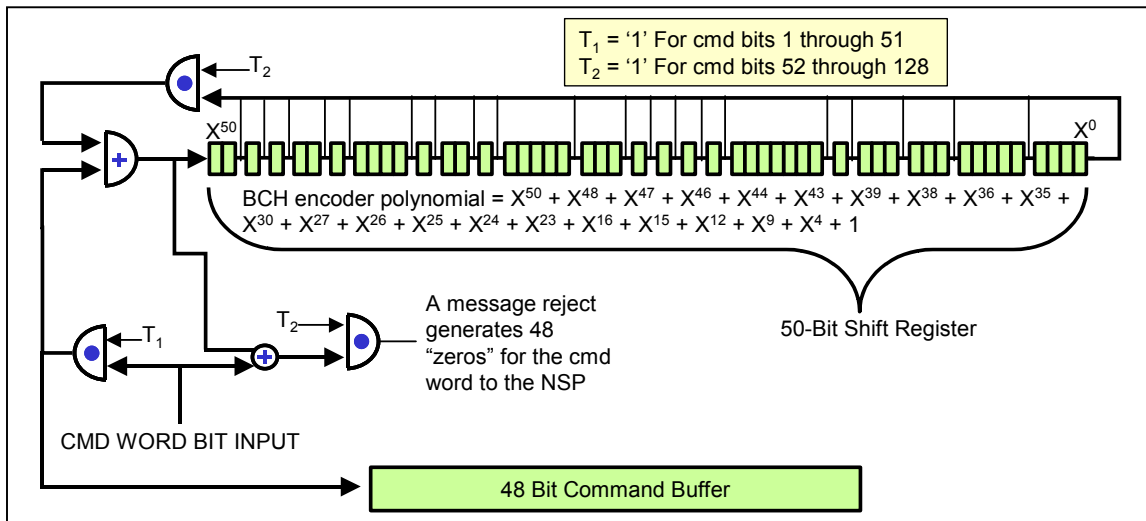
The start time word 2 consecutive marks circuit outputs a signal that queues the time word shift register to output the 10-second and 20-second bit data in the register to the greater-than-10-second compare logic.

### 13.4.7 BCH Check

The BCH check is done by taking the 50 bits of the command data (2 dummy bits + 48 bits of command data) being output from the Time Authentication Processor and passing them through the COMSEC BCH encoder. The COMSEC BCH encoder is a 50-bit shift register which uses the BCH polynomial to generate the 77 bits of the BCH code. The freshly calculated 77 BCH code is compared, one bit at a time, to the 77-bit BCH code that was attached to the command data. If they compare then the command data has passed the BCH check. If the two BCH codes do not match then the command data has failed the BCH check; command data all is zeroized from the 128 bits and the data is sent on to the

NSP. Neither the COMSEC nor the NSP use BCH to correct transmission errors in the command data.

If the **first BCH check fails** the current time is re-added to the command data. A second time authentication check is made using the previous 10-second time word EX-OR code check. The second check allows for transmission delays that may occur when using the Tracking and Data Relay Satellite (TDRS). If the second BCH check is valid, the command word is remultiplexed with the audio data and is still delayed by only one frame.



**Figure 13-8. BCH Processor**

If the BCH check is unsuccessful for both the current and the previous 10-second time word, the command fails to authenticate, the 48-bit command data word is zeroized and the remaining time-processed 80 bits (3 dummy and 77 BCH parity) of the 128-bit command are remultiplexed with the audio data. This will ensure two things:

1. the command data will fail the NSP BCH check that uses the same logic as the COMSEC LRU
2. The audio will be processed by the NSP and passed on to the ACCU with at most a 10 bit delay as compared to the input.

### 13.4.8 COMSEC Multiplexer

If the command passes either the new time or new  $\oplus$  old time and BCH validation check, the mux control logic allows the authenticated command to be remultiplexed into the data stream one frame later than its original position.

### 13.4.9 Power Supply

The power supply receives redundant +28 V dc ( $\pm 4$  V dc) power from the orbiter power control assemblies (Forward Power Controller (FPC) 1 and FPC 2) and divides it between two circuits, the operate circuit and the standby circuit.

**Table 13-1. Power Sources**

|          | <b>RPC Control power</b> | <b>Operate Power</b> |
|----------|--------------------------|----------------------|
| COMSEC 1 | CNTR AB1                 | MNB FPC2             |
|          | CNTR AB3                 | MNA FPC1             |
| COMSEC 2 | CNTR AB1                 | MNA FPC1             |
|          | CNTR AB3                 | MNB FPC 2            |

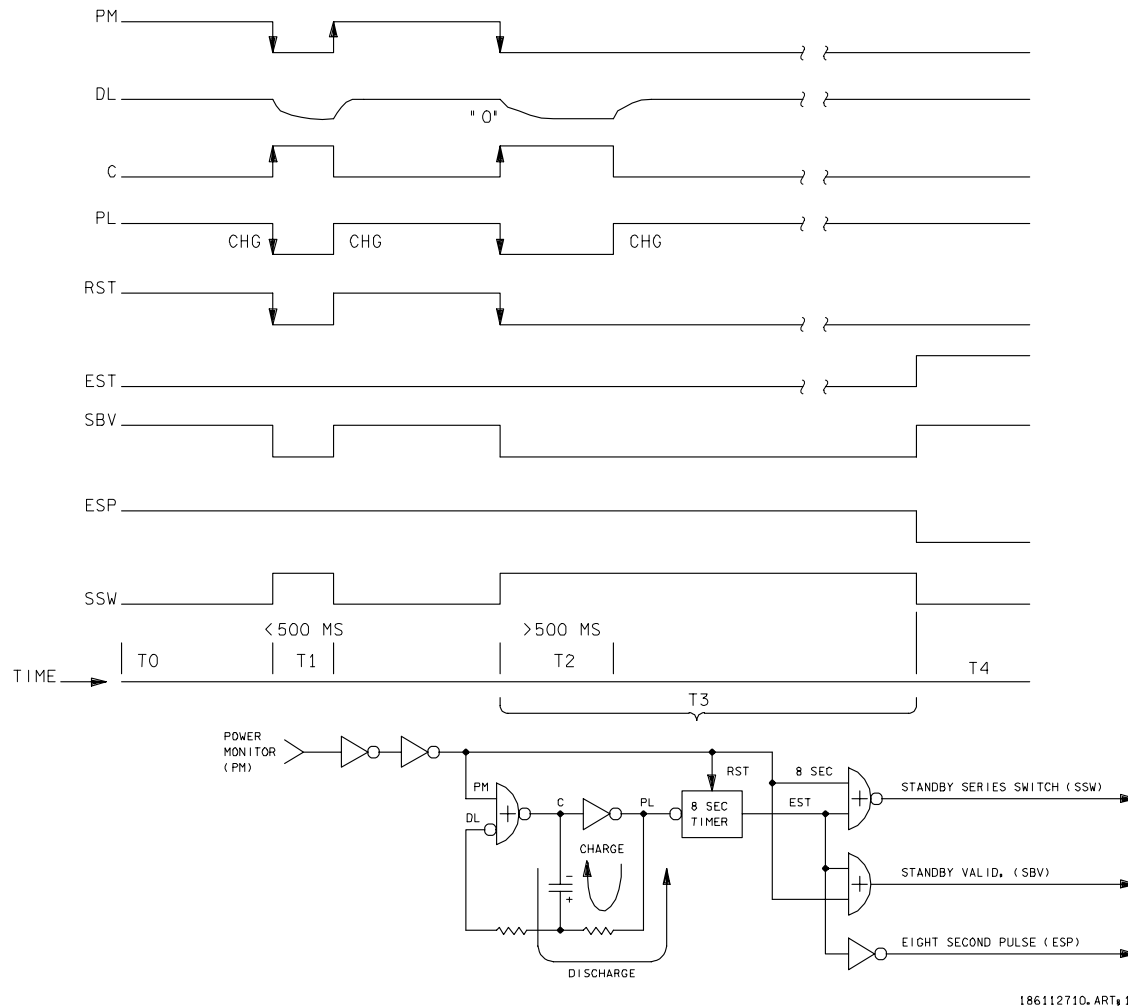
The standby circuit provides power to the BITE assembly and the core Cryptovisible Memory (CVM) and standby power for the core control circuits. Also, this circuit contains a power monitor circuit for controlling short and long power interruption functions. The short function provides the core control with a standby valid signal, and the long term function provides a pulse (8-second) for power losses of 8 seconds or more to the core control circuit for zeroizing the CVM.

The power loss monitor is shown in Figure 13-9. Its purpose is to prevent short term power transients from zeroizing the CVM and to provide CVM zeroizing for long term power losses.

The operate circuit is activated by the COMSEC operate control function which receives its stimulus from the NSP GCIL command driver power for the active NSP. This circuit brings the power supply and the COMSEC LRU up to full operation.

#### 13.4.9.1 Power

- Standby - 2.5 watts
- Operate - 25 watts



**Figure 13-9. Power loss monitor circuit**

### 13.4.10 Red and Black Input/Output Circuits

The Input/Output (I/O) data circuits are under the control of the core module via enable signals that allow data to be processed. The red I/O data are not encrypted (plain text) and the black I/O data are encrypted and, therefore, secure.

### 13.4.11 Key Filler Port

The COMSEC key is loaded via an isolated fill device. This device is plugged into the COMSEC at connector J4. Generally this process is done while the orbiter is on the pad so the J4 connector has an extension cable that puts a connector in front of Av bay 3A. The isolated filler device is battery powered.

### 13.4.12 BITE Assembly

The BITE assembly signal conditions the IRIG-B time signal (GMT), provides optical isolation of the receive HDR/LDR control inputs, filters the input current from the

Encryption Zeroize switch, receives status information from the core and the demux/authenticate circuit and outputs the BITE telemetry to the OI MDM OF3.

### 13.5 INSTALLATION

The COMSEC 1 and 2 are mounted side by side in bay 3A shelf 3. The following sections discuss the structure, size, location, weight and cooling for these LRUs.

#### 13.5.1 Connector Data

There are 5 connectors on the front of the LRU. The J1 connector is used to return the processed forward link data back to the NSP and to receive the return link data for encryption. The J2 connector is used to pass the required clocks for both the forward and the return links as well as receive the encrypted forward link and return the encrypted return link to the NSP. The J3 connector is used to receive the control bits and power. The J4 connector is used to fill the crypto key. The J5 connector is used to send the BITE status to the OI MDM OF3 as well as receive GMT from the MTU. Figure 13-10 shows the connectors on the LRU.

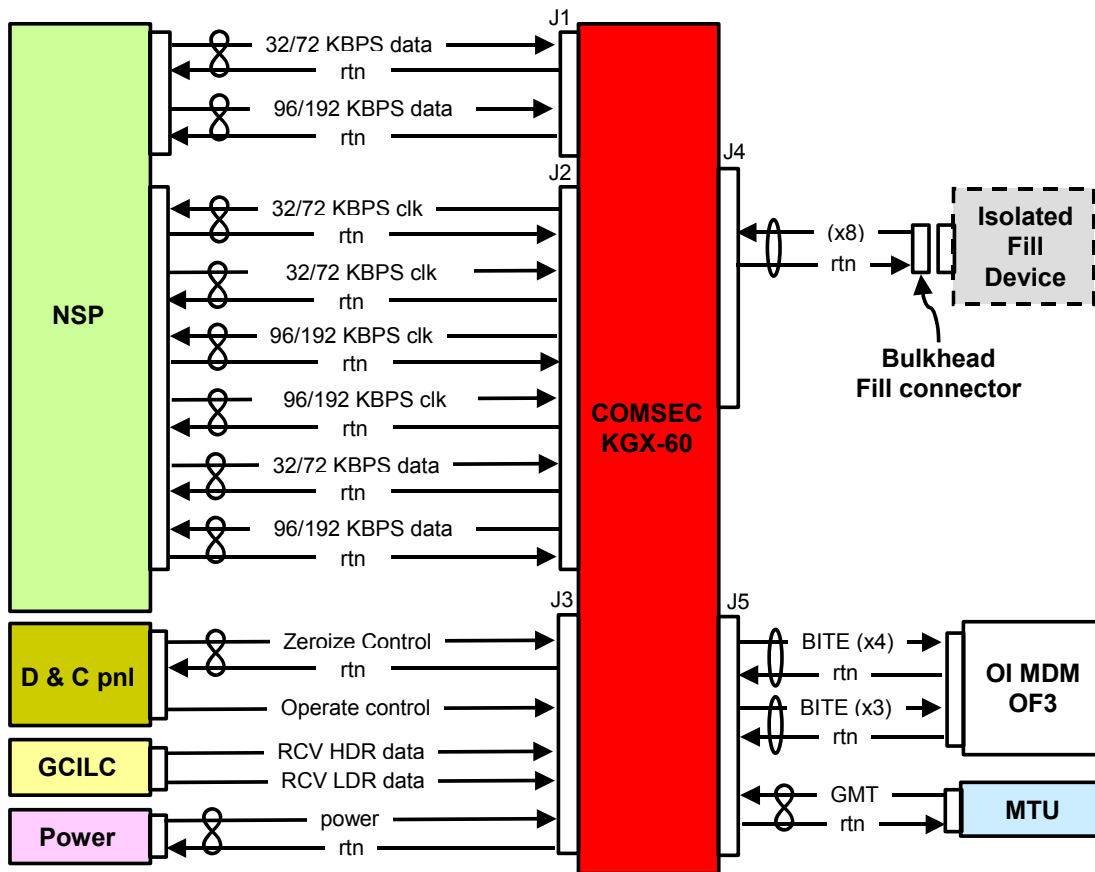


Figure 13-10. COMSEC Connectors

Table 13-2 shows the pins on each connector.

**Table 13-2. Connect Descriptions**

| Connector | Pin | Function           | Signal Origin | Volts | Cable Descriptor |
|-----------|-----|--------------------|---------------|-------|------------------|
| J1        | A   | 32/72 kbps data    | COMSEC        | 5     | TSP              |
|           | B   | 96/192 kbps data   | NSP           | 5     | TSP              |
|           | C   | 32/72 kbps return  | COMSEC        | -     | TSP              |
|           | D   | 96/192 kbps return | NSP           | -     | TSP              |
|           | E   | Ground             | -             | -     | -                |
|           | F   | Shield - ground    | -             | -     | -                |

| Connector | Pin                     | Function                 | Signal Origin | Volts | Cable Descriptor |
|-----------|-------------------------|--------------------------|---------------|-------|------------------|
| J2        | A                       | 32/72 kbps clock         | COMSEC        | 5     | TSP              |
|           | B                       | 32/72 kbps data return   | NSP           | -     | TSP              |
|           | C                       | 32/72 kbps clock         | NSP           | 5     | TSP              |
|           | D                       | 96/192 kbps data return  | COMSEC        | -     | TSP              |
|           | E                       | 96/192 kbps clock        | COMSEC        | 5     | TSP              |
|           | F                       | 32/72 kbps clock return  | NSP           | -     | TSP              |
|           | G                       | 96/192 kbps clock        | NSP           | 5     | TSP              |
|           | H                       | 96/192 kbps clock return | NSP           | -     | TSP              |
|           | J                       | 32/72 kbps data          | NSP           | 5     | TSP              |
|           | K                       | 96/192 clock return      | COMSEC        | -     | TSP              |
|           | L                       | 96/192 kbps data         | COMSEC        | 5     | TSP              |
|           | M                       | Shield - ground          | -             | -     | -                |
|           | N                       | Ground                   | -             | -     | -                |
|           | P                       | Ground                   | -             | -     | -                |
|           | Q                       | Spare                    | -             | -     | -                |
| R         | 32/72 kbps clock return | COMSEC                   | -             | TSP   |                  |

| Connector | Pin | Function        | Signal Origin | Volts  | Cable Descriptor |
|-----------|-----|-----------------|---------------|--------|------------------|
| J3        | A   | Power           | PCA           | +28vdc | TP               |
|           | B   | Spare           | -             | -      | -                |
|           | C   | Power return    | PCA           | -      | TP               |
|           | D   | Spare           | -             | -      | -                |
|           | E   | Zeroize Control | D&C           | +5vdc  | TSP              |

**Table 13-2. Connect Descriptions (concluded)**

| Connector | Pin | Function                | Signal Origin | Volts  | Cable Descriptor |
|-----------|-----|-------------------------|---------------|--------|------------------|
|           | F   | Operate control (KGX60) | LCA           | +28vdc | MCS              |
| J3        | G   | Zeroize return          | D&C           | -      | TSP              |
|           | H   | Shield ground           | -             | -      | -                |
|           | J   | Receive, HDR            | GCIL          | +28vdc | MCS              |
|           | K   | Receive, LDR            | GCIL          | +28vdc | MCS              |

| Connector | Pin | Function        | Signal Origin | Volts  | Cable Descriptor |
|-----------|-----|-----------------|---------------|--------|------------------|
| J4        | A   | Fill Data       | Fill          | 0,5vdc | MCS              |
|           | B   | Fill clock      | Fill          | 0,5vdc | MCS              |
|           | C   | Sense reference | Fill          | 0,5vdc | MCS              |
|           | D   | Sense           | Fill          | 0,5vdc | MCS              |
|           | E   | Parity          | Fill          | 0,5vdc | MCS              |
|           | F   | Zeroized        | Fill          | 0,5vdc | MCS              |
|           | G   | Request         | Fill          | 0,5vdc | MCS              |
|           | H   | Signal return   | Fill          | 0,5vdc | MCS              |

| Connector | Pin | Function                      | Signal Origin | Volts | Cable Descriptor |
|-----------|-----|-------------------------------|---------------|-------|------------------|
| J5        | A   | Status 1 - Alarm Condition    | COMSEC        | 5vdc  | MCS              |
|           | B   | Status 3 - Receive full oper  | COMSEC        | 5vdc  | MCS              |
|           | C   | Status 5 - master BITE        | COMSEC        | 5vdc  | MCS              |
|           | D   | Return                        | COMSEC        | 5vdc  | MCS              |
|           | E   | Status 2 - Transmit Full oper | COMSEC        | 5vdc  | MCS              |
|           | F   | Status 4 - CVM Zeroized       | COMSEC        | 5vdc  | MCS              |
|           | G   | Status 6 - Frame Sync         | COMSEC        | 5vdc  | MCS              |
|           | H   | Status 7 - Authenticate       | COMSEC        | 5vdc  | MCS              |
|           | J   | Return                        | COMSEC        | -     | -                |
|           | K   | GMT                           | MTU           | +5vdc | TSP              |
|           | L   | GMT return                    | MTU           | -     | TSP              |
|           | M   | Shield - ground               | -             | -     | -                |



### 13.5.2 Cooling

Cooling is supplied by a cold plate. The operating temperature range is 35° F to 120° F. Non operating temperature range is -29° F to 120° F with allowances for up to 150° F for a maximum of 6 hours per day. For details of the coolant loop temperature control, see Section 20, Communication and Instrumentation System Water and Air-Cooled Equipment.

### 13.5.3 Weight

20 pounds (max).

## 13.6 DESCRIPTION OF CREW AND GROUND OPERATIONS

The COMSEC operates in either HDR or LDR mode as selected by the NSP uplink data rate switch or associated Ground Control Interface Logic (GCIL) commands. Downlink data are processed at whatever data rate is received from the NSP. The following section discusses what actions the ground can make, what telemetry the ground can see, what actions the crew can make and what telemetry the crew can see.

### 13.6.1 Crew Controls

The crew has limited control of the COMSEC. The following are the switches which the crew can use to change the configuration of the NSP/COMSEC. Figure 13-11 shows the panel A1L and R11L switches the crew can use to control this LRU.

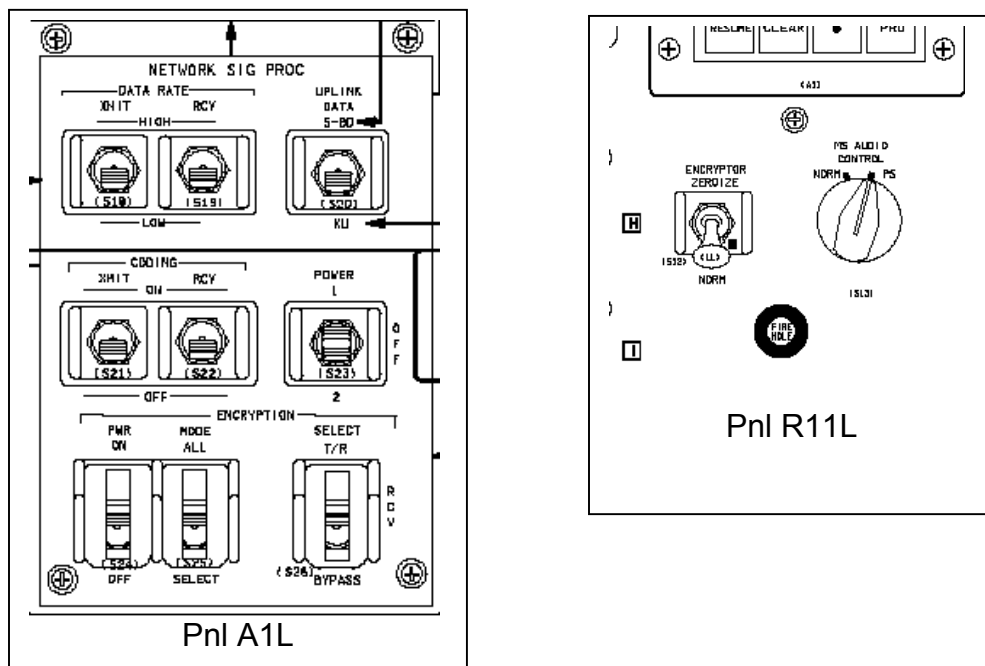


Figure 13-11. Crew Controls

**13.6.1.1 Panel A1L**

NSP ENCRYPTION      PWR      - ON(OFF)  
                               MODE      - SELECT(ALL)  
                               SELECT    - RCV(TR, BYPASS)

The first switch position for each of the above switches is the nominal position. The other position(s) are selectable but generally not used. The following table explains what capabilities are available in each of the combinations of these switches.

**Table 13-3. Mode Switch Functions**

| Mode (switches)  |        | Link function                               |
|------------------|--------|---|
| All<br>(DOD)     |        | RCD ENC <sup>a</sup><br>XMIT ENC<br>RCV ENC |
| Select<br>(NASA) | T/R    | RCD CLR <sup>b</sup><br>XMIT ENC<br>RCV ENC |
|                  | RCV    | RCD CLR <sup>b</sup><br>XMIT CLR<br>RCV ENC |
|                  | Bypass | RCD CLR <sup>b</sup><br>XMIT CLR<br>RCV CLR |

<sup>a</sup>Data rate determined by NSP downlink data rate switch.

<sup>b</sup>HDR only.

**13.6.1.2 Panel R11L**

ENCRYPTOR      - NORM(ZEROIZE)

The COMSEC LRU CVM can be zeroized by the zeroize control switch or by removing power from the LRU. The zeroize function causes the LRU to be functionally inoperable (both transmit and receive, both COMSEC 1 & 2) until the memory can be restored postflight by the Isolated fill device.

**13.6.2 Crew Display**

The crew can use SPEC 76 to view the status of the COMSEC. Figure 13-12 is SPEC 76.

```

XXXXXXXX/XXX/076 COMMUNICATIONS XX X DDD/HH:MM:SS
                                DDD/HH:MM:SS
S-BAND PM          XXXXS          KU-BAND
FREQ  XXS          1          2    PA TEMP          ±XXXS
ANT FI FC          XXS          XXS  GIMPAI  TFMP  A          +XXXS
XPNDR              XXS          XXS          B          ±XXXS
PREAMP              XXS          XXS  GYRO TEMP          ±XXXS
PWR AMPL              XXS          XXS  PWR OUT              XXS
OPER                XXS          XXS  FRM SYNC              XXS
STBY                XXXXS         XXXXS  MODE                  XXXXS
PWR OUT              XXS          XXS  FAIL SAFE              XXS
TEMP                XXXXS         XXXXS  AUTO K TO S           XXX
NSP                  1          2    AUTO S TO K           XXX
BIT SYNC            XXXS          XXS  SSOR                  1    2
FRM SYNC            XXXS          XXS  FRM SYNC              XXS  XXS
BITE                XXXXS         XXXXS  PROC STAT              XXS  XXS
COMSEC BITE         XXXXS         XXXXS  PWR LEVEL              ±XX.XS
                                STATUS              X.XS
UL DATA SOURCE      XXS          GCIL CONFIG            XXXS
DATA RATE XMIT       XXS          CCTV CAMR OVRTMP     XXXS
RCV                  XXS
CODING XMIT          XXXS
RCV                  XXXS
                                (XX)
    
```

Figure 13-12. SPEC 76

13.6.3 Ground Commands

There are no ground commands to the COMSEC but commands to the NSP will control how the COMSEC operates.

Table 13-4. Commands to Configure the Downlink Rate

| RTC  | Nomenclature | Indications   | MSID      |
|------|--------------|---|-----------|
| 4763 | DNLINK -LDR  | Configures the active NSP to downlink the low data rate source from the PCMMU.                | V74K3124U |
| 4764 | DNLINK -HDR  | Configures the active NSP to downlink the high data rate source from the PCMMU (default mode) | V74K3123U |

13.6.4 Mode Telemetry

The following Table 13-5 documents the telemetry available from the COMSEC LRUs.

Table 13-5. COMSEC Telemetry Responses

| MSID      | Nomenclature                | Indications   | Data Rate |
|-----------|-----------------------------|---|-----------|
| V76X3065E | FWD PCA COMSEC 1 RPC A - ON | '1' - indicates RPC 46 is outputting 28 volts from MNA FPC1 | 1/S       |
| V76X3066E | FWD PCA COMSEC 1 RPC B - ON | '1' - indicates RPC 47 is outputting 28 volts from MNB FPC2 | 1/S       |
| V76X3067E | FWD PCA COMSEC 2 RPC A - ON | '1' - indicates RPC 45 is outputting 28 volts from MNA FPC1 | 1/S       |

**Table 13-5. COMSEC Telemetry Responses (concluded)**

| MSID      | Nomenclature                | Indications   | Data Rate |
|-----------|-----------------------------|---|-----------|
| V76X3068E | FWD PCA COMSEC 2 RPC B - ON | '1' - indicates RPC 48 is outputting 28 volts from MNB FPC2   | 1/S       |
| V74S5005E | ENCRYPTION COMSEC           | '1' - indicates the NSP Encryption Power switch is in the ON position, CNTLAB1 is providing control power through the switch to the RPCs. | 1/S       |
| V74X5390E | NSP 1 RCV ENCRYPTED         | '1' - indicates the NSP will forward the forward link to the COMSEC for processing.   | 1/S       |
| V74X5391E | NSP 1 XMIT ENCRYPTED        | '1' - indicates the NSP will send the encrypted return link from the COMSEC to the downlink.  | 1/S       |
| V74X5392E | NSP 1 RCD ENCRYPTED         | '1' - indicates the ENCRYPTION Mode switch is in "ALL" so the data going to the recorders is encrypted.                                   | 1/S       |
| V74X5590E | NSP 2 RCV ENCRYPTED         | '1' - indicates the NSP will forward the forward link to the COMSEC for processing.   | 1/S       |
| V74X5591E | NSP 2 XMIT ENCRYPTED        | '1' - indicates the NSP will send the encrypted return link from the COMSEC to the downlink.  | 1/S       |
| V74X5592E | NSP 2 RCD ENCRYPTED         | '1' - indicates the ENCRYPTION Mode switch is in "ALL" so the data going to the recorders is encrypted.                                   | 1/S       |
| V74S5007E | COMSEC ZEROIZE              | '1' - indicates that the Zeroize switch on panel R11L is in the "ZEROIZE" position.   | 1/S       |

### 13.6.5 BITE Status Telemetry

The BITE in the COMSEC monitors several components of the LRU. The COMSEC 1 (COMSEC 2) status bits from the KGX-60 are defined as follows:

**Table 13-6. BITE Indications**

| MSID                 | Nomenclature                      | Indications  | Data Rate |
|----------------------|-----------------------------------|--|-----------|
| V74X5017E<br>(5018E) | COMSEC 1(2)<br>ALARM<br>CONDITION | Status 1 is the <u>Alarm Condition</u> indicator. If a problem exists in either transmit or receive or both, a "1" (high) indicates the KGX-60 is not operating properly (failure of the unit or failure of the memory). A "0" (low) is correct operation.   | 1/S       |
| V74X5013E<br>(5014E) | COMSEC 1(2) XMIT<br>FULL-OPERATE  | Status 2 is the <u>Transmit Full Operate</u> indicator. If a "1," the unit is in the transmit or downlink stage and is fully operable. This is proper operation. A "0" indicates failure of the transmit mode. Other indicators, as discussed herein, are required to establish the exact problem within the unit.   | 1/S       |
| V74X5015E<br>(5016E) | COMSEC 1(2) RCV<br>FULL-OPERATE   | Status 3 is the <u>Receive Full Operate</u> indicator. If a "1," the unit is in the receive or uplink stage and is fully operable. This is proper operation. A "0" indicates failure of the receive mode. Other indicators, as discussed herein, are required to establish the problem.  | 1/S       |
| V74X5011E<br>(5012E) | COMSEC 1(2) CVM<br>ZEROIZE        | Status 4 is the <u>CVM Zeroized</u> indicator. If a "1," the unit's CVM has been zeroized or erased, and the unit is not operable. If a "0," the KGX-60 is operating properly with the proper key in the memory. This is the proper operational condition.   | 1/S       |
| V74X5003E<br>(5004E) | COMSEC 1(2)<br>MASTER BITE        | Status 5 is the <u>Master BITE</u> indicator. If a "1," the unit is operating properly. This is proper operation. A "0" indicates failure of an SRU within the LRU. This status must be compared to the power ON 28 V dc to be valid. The same statement applies to all "0" indicators.  | 1/S       |
| V74X5019E<br>(5020E) | COMSEC 1(2)<br>FRAME SYNC         | Status 6 is the <u>Frame Sync</u> indicator. If a "1," the data prior to authentication have been frame sync'd. It has the same meaning as the NSP. A "1" is proper operation. A "0" indicates no frame sync.  | 10/S      |
| V74X5001E<br>(5002E) | COMSEC 1(2)<br>AUTHENTICATE       | Status 7 is the <u>Command Authenticated</u> indicator. If a "1," the command is authenticated. A "0" indicates an individual command has not been authenticated. The message valid status of the NSP and the command authenticate of the KGX-60 operate identically. Both stay low (0), except when a command is authenticated or a message is valid, then the indicator goes high (1). | 50/S      |

## 13.7 OPERATIONAL NOTES

### 13.7.1 Ground Responses to BITE status Indications

If status 3 (RCV FULL OPR) is a "1" and status 2 (XMIT FULL OPR) is a "0," status 4 (CVM ZEROIZED) may indicate a "1." This indicates the transmit key has been zeroized or the key was not loaded properly.

If status 2 (XMIT FULL OPR) is a "1" and status 3 (RCV FULL OPR) is a "0" then status 4 (CVM ZEROIZED) may indicate a "1." This indicates the receive key has been zeroized or the key was not loaded properly.

Status 4 (CVM ZEROIZED) does not indicate which key (XMIT/RCV) is zeroized, only that one or both keys are zeroized.

Any error in the BCH code will cause the 48-bit command to be zeroized and forwarded to the NSP. The NSP will indicate BCH not valid.

A loss of input clock from the NSP can hold status bits 6 (FRM SYNC) and 7 (CMD AUTH) as "1" or as a "1" and "0," respectively (last memory state prior to failure). The true meaning can be determined from the NSP FRAME SYNC data. The clock updates both status bits 6 and 7.

Failure or loss of the MTU time word signal is indicated by status bit 7 (CMD AUTH) being a "0" and NSP message valid a "0" over a period of time, with time code commands being uplinked.

Power failure of the KGX-60 will force all status bits to "0."

Status 7 (CMD AUTH) can be a "1" and NSP message valid a "0." The KGX-60 checks for command authentication and BCH parity. The NSP checks for BCH parity and nonzero vehicle address.

When the KGX-60 is turned ON (power applied), BITE bits (1 through 7) read 000000. When the unit has been filled and is in operate, the bits read 0110100.

Since idle patterns are sent without authentication time, the NSP will indicate a non-valid message and BCH errors in the NSP status word. The same occurs when the bit sync or convolutional decoder passes errors.

### 13.7.2 ESTL Test Results

Electronic Systems Test Laboratory Test Report, SD-274

- A. With the KGX-60 active, removal of clock or data or both at the input to the KGX-60 encryptor does not alter KGX-60 status indications.
- B. Loss of clock or loss of clock and data into the KGX-60 decryptor causes the KGX-60 FRAME SYNC indication to maintain the status indicated the last time the clock was present. This loss of clock causes the AUTHENTICATE line to go low.

- C. Loss of data only into the KGX-60 decryptor causes the KGX-60 FRAME SYNC indication and the AUTHENTICATE indication to go low.
- D. Selection of the wrong data rate on the KGX-60 will cause the KGX-60 FRAME SYNC indication and the AUTHENTICATE indication to go low. The KGX-60 will pass data to the NSP, and the NSP will show good frame sync, but it is not commandable.
- E. Selection of STANDBY on the KGX-60 causes all status indications to go low.
- F. Selection of ZEROIZE on the KGX-60 causes all status indications to go low, except CVM ZEROIZED, which goes high.
- G. Improper time (on the forward link data) causes the AUTHENTICATE indication to go low. NSP frame sync is high, but the NSP is not commandable.
- H. Loss of clock into the NSP will cause the NSP frame sync indication to maintain the status shown the last time clock was present.
- I. Power OFF to the KGX-60, removal of clock to the KGX-60 decryptor, selection of STANDBY at the KGX-60, and KGX-60 ZEROIZE all cause loss of clock to the NSP.

### 13.7.3 Alarm Meaning

Unless a specific failure occurs that causes the MASTER BITE, TRANSMIT FULL OPERATE, or RECEIVE FULL OPERATE status signals to stay high, independent of the condition of the box, all the status signals, with the possible exception of ZEROIZE, will go low whenever ALARM goes high. Therefore, it is unlikely that you will ever encounter a condition where ALARM is high and either TRANSMIT FULL OPERATE or RECEIVE FULL OPERATE is also high.

Refer to RSOC Task Order Memo TM 3R1-87-043, July 2, 1987

### 13.7.4 Receiver False Lock

The COMSECs are prone to lose frame sync lock without showing the frame sync lock telemetry as "0." This is called a false lock and prevents commands from being processed although audio is not affected. To correct this problem drop the forward link modulation then reapply it. This will cause the frame sync logic in the COMSEC to reset then reacquire, thereby allowing commands to be processed again.

### 13.7.5 Operational Instructions

- A. Loss of power, for 8 seconds, will zeroize the CVM.
- B. If the alarm condition was caused by a KG 28/46 transmit problem, the COMSEC will not process commands until the LRU is taken to standby then back to operate. This can be done by power cycling the associated NSP.

### **13.8 SPECIAL TELEMETRY COMPUTATIONS**

None

### **13.9 REFERENCES**

Elwell 11 Preliminary Design Review, Motorola, Inc., January 29-31, 1980.

Schematic Diagram - C&T S-Band Network Signal Processor, VS70-740229.

Installation Drawing - Avionics Equipment Instl - Crew Module, V070-703000.

Installation Drawing - Coolant Installation, Avionics Equipment, Crew Module, Bay 3A, V070-613362.

ICD - Network COMSEC Equipment/Orbiter KGX-60/TSEC, ICD-3-6761-01, Rev B.

### **13.10 SUMMARY DATA**

None



THIS PAGE INTENTIONALLY BLANK

## SECTION 14 - ANTENNA MANAGEMENT

### CONTENTS

| Section |   | Page  |
|---------|---|-------|
| 14.1    | INTRODUCTION .....                                      | 14-1  |
| 14.1.1  | SM Antenna Management Overview .....                    | 14-2  |
| 14.1.2  | BFS Antenna Management Overview.....                    | 14-4  |
| 14.2    | SM DETAILS .....  | 14-5  |
| 14.2.1  | S-Band Switch-Beam/Hemi-Antenna Management - SM .....   | 14-5  |
| 14.2.2  | TDRS Computations - SM .....                            | 14-12 |
| 14.2.3  | Ku-Band Antenna Management - SM.....                    | 14-13 |
| 14.2.4  | Auto-Handovers Between S-Band and Ku-Band .....         | 14-19 |
| 14.2.5  | Antenna Management ICC Data.....                        | 14-20 |
| 14.2.6  | OPS Transition Points .....                             | 14-20 |
| 14.3    | BFS DETAILS.....  | 14-21 |
| 14.3.1  | TDRS Mode .....   | 14-21 |
| 14.3.2  | BFS SPEC 51 .....                                       | 14-22 |
| 14.4    | CREW INTERFACES .....                                   | 14-22 |
| 14.4.1  | BFS S-Band Communication Reconfiguration (SPEC 51)..... | 14-23 |
| 14.4.2  | SM Displays.....  | 14-23 |
| 14.4.3  | Panel Controls and Readouts.....                        | 14-25 |
| 14.5    | ANTENNA MANAGEMENT IDIOSYNCRACIES .....                 | 14-30 |

### FIGURES

| Figure |   |       |
|--------|---|-------|
| 14-1   | SM antenna management .....               | 14-3  |
| 14-2   | SM AM logic flow for TDRS selection ..... | 14-7  |
| 14-3   | SPEC 51 .....                             | 14-23 |
| 14-4   | SM SPEC 201.....                          | 14-24 |
| 14-5   | Panel C3.....                             | 14-26 |
| 14-6   | Panel F9 .....                            | 14-27 |
| 14-7   | Panel A1U.....                            | 14-28 |
| 14-8   | Panel A1L .....                           | 14-29 |

**THIS PAGE INTENTIONALLY BLANK**

## SECTION 14 ANTENNA MANAGEMENT

### 14.1 INTRODUCTION

Antenna Management (AM) is a function performed in the orbiter General Purpose Computers (GPCs) that automatically performs antenna selection, steering, and communications systems reconfiguration control in some cases. Based on the orbiter position and the position of the tracking station or Tracking and Data Relay Satellite (TDRS), the AM function calculates the optimum antenna selection, commands the switching to that antenna if it is not already selected, and verifies that the antenna switch is correctly configured for the selected antenna.

During ascent/entry, the AM function is performed in the Backup Flight System (BFS) computer. During on-orbit operations, the AM function is performed in the System Management (SM) computer.

The BFS computer performs only S-band Phase Modulation (PM) quad-antenna and S-band Frequency Modulation (FM) hemi-antenna selection. It does not provide Ku-band steering. When the BFS is selecting quad-antennas to point at TDRS, it does not perform any S-band hemi-antenna selection. The BFS does not provide any onboard display of antenna selection or performance. The BFS does not provide crew notification for failure in antenna selection. It does not provide notification to the ground.

The SM computer performs selection of S-band PM quad-antennas and S-band FM hemi-antennas, as well as steers the Ku-band dish antenna. The Ku-band antenna can be steered by the SM computer to either point at the TDRS satellite (for Ku-band communications) or at a rendezvous target (for Ku-band rendezvous RADAR operations). The S-band PM and S-band FM antennas are selected separately. Even if the S-band PM antennas are being selected for TDRS, the S-band FM hemis are automatically selected for any ground stations that are enabled and in view. The SM computer provides a display that shows the pointing angles from the orbiter to TDRS and ground stations. The SM provides a message to the crew, ("2011 ANTENNA"), and to the ground if antenna selection is not occurring properly.

Both BFS and SM antenna pointing can be inhibited by ground command to allow direct ground command selection of antennas. In BFS this command is accomplished via Table Maintenance Block Update (TMBU). In SM this is accomplished by use of a dedicated antenna Operation (OP) code. The SM antenna OP code also provides the capability for control of the AM software.

The crew can override selection of antennas at any time by the use of the antenna select rotary switch on panel C3. Whenever this switch is rotated out of the GPC position, it overrides all computer inputs at the antenna electronics unit. The SM GPC reads the position of this switch and does not issue antenna selection alarms if the switch is not in the GPC position.

The BFS GPC is initialized (K - LOAD) with the ideal locations for three TDRS satellites:

Slot 1 - 171

Slot 2 - 47

Slot 3 - 275

The SM GPC is initialized (I - LOAD) with the ideal locations for six TDRS Satellites:

State Vector 1 - 171

State Vector 2 - 47

State Vector 3 - 275

State Vector 4 - 41

State Vector 5 - 171

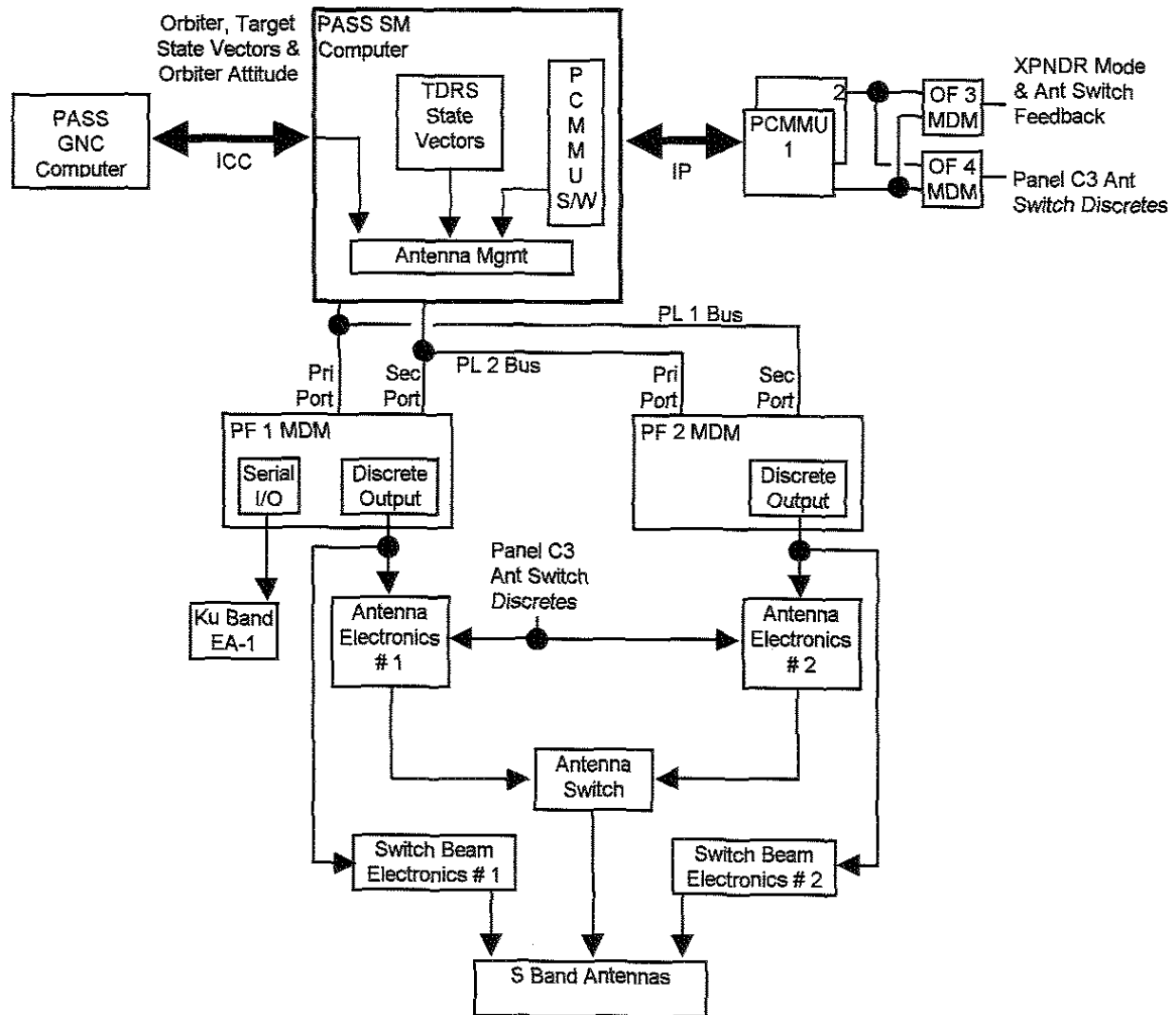
State Vector 6 - 47

Both the SM and BFS GPCs can be updated, from the ground, with a current TDRS state vector command.

BFS OI-30 software allows all three TDRS state vectors to be updated prelaunch.

#### **14.1.1 SM Antenna Management Overview**

Figure 14-1 shows the data flow for SM antenna management. The Guidance, Navigation, and Control (GNC) computer uses the Intercomputer Communication (ICC) bus to give the orbiter position and attitude to the SM computer. The SM computer then uses the previously loaded value for TDRS position along with the GNC values for the orbiter position and attitude to calculate the antenna that should be selected.



**Figure 14-1. SM antenna management**

Once the SM has calculated the proper antenna to be selected, it issues the commands to select that antenna. Commands are issued once every 1.92 seconds, the equivalent of one complete AM cycle. For S-band PM and S-band FM antennas, these commands are issued via both Payload Forward (PF) 1 and PF 2 Multiplexer/Demultiplexers (MDMs). For S-band PM and FM selection commands, the PF 1 and PF 2 MDMs send the selections as discretes to the S-band system 1 and system 2 antenna electronics units and switched beam electronics units. Although commands are always sent to both systems 1 and 2, only one of these systems is powered on at a time. If the SM GPC cannot communicate with the PF MDM connected to the currently powered antenna electronics unit (PL MDM BYPASS), then proper antenna selection does not occur.

Antenna steering commands for the Ku-band are issued via Serial Input/Output (SIO) card 8, located only on PF 1 MDM.

Once the selection commands have been sent to the S-band PM and FM antenna electronics, the SM GPC attempts to verify that the selection has been accomplished successfully. This information is collected by reading the status of the antenna switch discretes from the OI system, Pulse-Code Modulation Master Unit (PCMMU). These discretes are acquired for the PCMMU by the Operational Forward 3 MDM (OF3 MDM). If the antenna discretes show that the antenna selected by the SM is not correctly selected in the hardware and that the crew has not overridden the GPC by use of the cockpit switch, the SM GPC issues a 2011 ANTENNA message. The 2011 ANTENNA message is only issued for errors in the S-band PM antennas. It is not issued for a problem in selecting S-band FM hemi-antennas.

If synchronization between the GNC and SM computers is lost, then the SM computer is not updated with the latest orbiter state vector (position and attitude). AM continues to use the last orbiter state and attitude information; which will be stale, thus no new antenna selection will occur. A critical part of SM AM is the technique by which SM determines the target at which it should be pointing. The following rules are implemented in the AM software in the SM computer:

- A. The S-band FM system can only work with ground stations, so the S-band FM antennas are selected to the ground station currently in view and not inhibited (not dependent on S-band PM transponder mode).
- B. The S-band quad-antennas are selected to the appropriate TDRS in view if the transponder mode is set to TDRS. The AM software determines the mode of the transponder by reading the PCMMU. The transponder mode is communicated to the PCMMU by MDM OF 3. If the transponder is not in TDRS mode, the AM software selects antennas to communicate with any ground stations in view and not inhibited. If the SM computer cannot access the PCMMU, SM cannot be informed when the transponder changes modes and antenna selection does not keep up with transponder mode commands. In this case, the crew can force the SM to select the correct antenna to point to TDRS via item entry on SM Specialist Function (SPEC) 201. The SM will disregard the indication of the transponder mode and assume TDRS mode.
- C. If multiple TDRSs are in view, then the AM software selects the TDRS to be used for pointing for both S-band and Ku-band based on the Priority (PRI) configuration bits. These bits can be controlled by ground command and crew entries from the SM Antenna display. The S-band and Ku-band can be selected to different satellites.
- D. The Ku-band is pointed at TDRS unless the GNC pointing flag has been enabled. Enabling the rendezvous antenna pointing (item 2) on SPEC 33 (REL NAV) in the GNC GPC enables this flag.

#### **14.1.2 BFS Antenna Management Overview**

BFS AM for S-band PM and FM is very similar to SM. The main difference is that the BFS always uses its own navigation information to determine antenna pointing, rather

than relying on the GNC computers. It does navigation processing as part of the entire BFS task to be ready to fly the vehicle at any time, based on its own information.

In a pre-engage scenario, the BFS acquires navigation sensor data, such as Inertial Measurement Unit (IMU) rates, by listening to the GNC computer transactions on the flight-critical buses. If BFS loses track on flight-critical buses 1-3, it no longer has any IMU data, its navigation state goes bad, and antenna selection is not correct. If this problem occurs, antenna selection must be performed by the crew or by ground command.

In the case of a BFS engage, the BFS is in direct command of the navigation sensors and acquires its navigation data by direct transactions with the navigation sensors.

If the BFS determines that the transponder is in TDRS mode, it no longer attempts to command the S-band FM antennas. The FM antennas must be selected via ground command.

The BFS does not include any calculations for steering the Ku-band antenna. The assumption is that the Ku-band system will not be active while the BFS is being used; therefore, there are no requirements for the BFS to command the Ku-band system.

## **14.2 SM DETAILS**

The AM sequence consists of Ku-band steerable AM, S-band quad- and hemi-AM, and a common function used to determine the position of the Tracking and Data Relay Satellite System (TDRSS), when the TDRSS is in view. Full AM is performed in SM OPS 2.

The parameters acquired from the GNC application (orbiter state vector and attitude) via ICC bus are processed as time-homogeneous data sets so that the AM function will not be confused by another update of the data on the ICC bus.

### **14.2.1 S-Band Switch-Beam/Hemi-Antenna Management - SM**

The AM selects the proper S-band switch-beam antenna (Forward (FWD) or AFT) for each of the upper right, upper left, lower right, and lower left) to communicate with the selected TDRS or the current Spacecraft Tracking and Data Network/Spacecraft Ground Link Subsystem (STDN/SGLS) site and to select the proper S-band hemi-antenna to communicate with a STDN/SGLS site.

S-band switch-beam AM is performed as defined below once every 1.92 seconds.

S-band antenna coverage is based only on theoretical coverage of a quadrant, which is further divided into forward and aft parts for the switch-beam quads and a hemisphere for the hemi-antennas.

#### **14.2.1.1 S-Band Quad-AM for TDRS Communications**

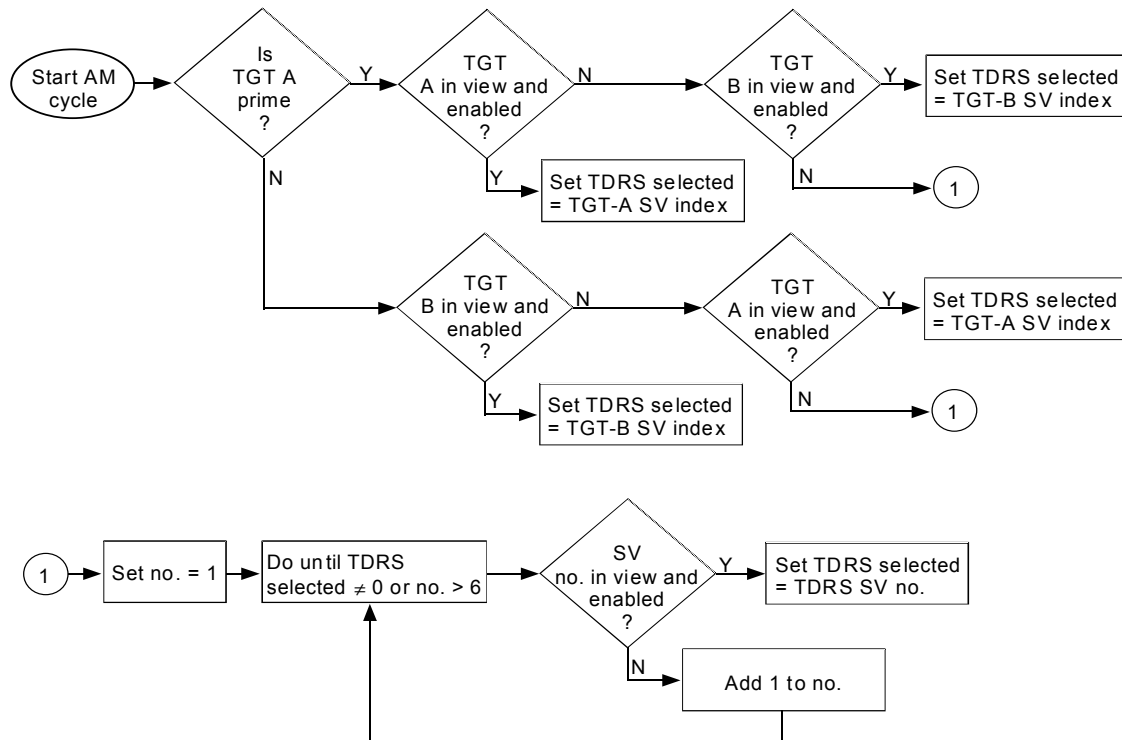
The SM contains six TDRS vectors that can be assigned to the eight available TDRS targets that are displayed on SPEC 201. The default assignments are as follows:



| Vector slot | Longitude | Default target | Slot enabled |
|-------------|-----------|----------------|--------------|
| 1           | -171 W    | A              | Yes          |
| 2           | -47 W     | B              | Yes          |
| 3           | -275 W    |                | Yes          |
| 4           | -41 W     |                | Yes          |
| 5           | -171 W    |                | Yes          |
| 6           | -47 W     |                | Yes          |

AM attempts to point the antennas first at the target (A or B) that is prime if it is in view and the State Vector (SV) slot assigned to that target is enabled. If the prime target is not in view or the SV slot is not enabled, the other target is selected if it is in view and its associated SV slot is enabled. SPEC 201 displays “A” and/or “B” if these targets are in view and enabled. If neither target is selected, AM tests each of the SV slots to see if any are enabled and in view.

The first slot that is in view and enabled is selected. SPEC 201 displays the slot number for the selected TDRS vector. If either target comes into view and is enabled during the next AM cycle, it is selected and the SV slot number is no longer displayed on SPEC 201. An attempt to inhibit a state vector that is currently being selected is rejected with V92X0352X - “TEC AM SV INVALID INHIBIT REQ” or an UPLINK INVALID REQUEST flag depending if the attempt is via TEC or real-time, respectively. Figure 14-2 shows the logic flow for selection of a TDRS SV to use for commanding the antennas.



j\_18611\_001.cv5

**Figure 14-2. SM AM logic flow for TDRS selection**

### 14.2.1.2 S-Band Switch-Beam/Hemi AM for STDN/SGLS Communications

This computation determines the STDN/SGLS site to be used and the line-of-sight look angle to the selected site. These computations are based on the current orbiter position received via ICC from the GNC application for SM and an STDN/SGLS site location table that contains the predefined position (latitude, longitude, and Earth radius or the equivalent of these parameters) and site Identification (ID) of each of the 16 STDN/SGLS sites. All 16 STDN/SGLS site locations and site IDs can be changed via TMBU.

The orbiter attitude data used to compute AM to sites are modified from the current data on the ICC to compensate for data transport delays by the attitude compensator. Data transport delay is defined as the sum of the difference between the current Greenwich Mean Time (GMT) and the GMT timetag associated with the state vector plus an attitude data set, adjusted by a constant factor “t” μsec (in seconds) to compensate for additional delays. This delay factor (V9OW1013C) can be updated via TMBU.

All these sites can be prevented from being used in AM processing. If the discrete corresponding to a particular site is set to 1, that site is inhibited and will not be used in AM processing. These site inhibit discrettes can be changed via the Table Maintenance (TM) SPEC or TMBU. The position and site ID of each of the 16 STDN/SGLS sites is specified in SM Level C Flight Systems Software Requirements (FSSR) and in the INCO/COMM Console Handbook (JSC-12829) TMBU SCP.

If auto-STDN/SGLS site AM sequence selects, as the current site, the first enabled site in the site location table that is in view of the orbiter at least  $X^\circ$  above the geocentric horizon at that site. The minimum STDN site elevation (V92H1005C) can be changed via the TM SPEC or TMBU. Sites are tested in the order in which they are stored in the site location table, regardless of the location in the site location table at which the test is started. If none of the enabled sites is in view of the orbiter, no current site is selected for that cycle. Once a current site is selected as defined above, that site remains selected during subsequent computation cycles until it is no longer in view of the orbiter. AM can be forced to select the next site by one of three methods: command (next site command), TEC, or by inhibiting the currently selected site by TMBU.

Each time the next site item is selected via keyboard input on the AM display or via TEC or uplink, the AM sequence selects, as the new current site, the enabled site in the site location table after the present current site that is in view of the orbiter at least  $X^\circ$  above the geocentric horizon at the site. If no other enabled site is in view, the currently selected site is automatically reselected by default. After the one-time search (once per next-site item entry), the program reverts to the auto mode. If a current site is selected by any of the above methods, the line-of-sight roll/pitch angle from the orbiter to the current site is computed in orbiter coordinates. The ID of the current site is displayed onboard and downlisted to the ground. If no current site is selected, site 16 (blank; spare) is downlisted as the current site. In addition, the current STDN/SGLS site-in-view indication is passed to system S/W where it is used as part of the site-in-view flag for control of the automatic uplink enable inhibit function. This indication is passed system wide to all GPCs on the ICC buses. More detail on this capability is specified in SM Level C FSSR.

#### **14.2.1.3 S-Band Antenna Target and Antenna Selection**

If auto S-band antenna selection is enabled via item entry on SPEC 201 or uplink, S-band switch-beam/hemi-antennas are selected as defined below.

If the S-band PM transponder is in the TDRS mode (as determined by the SM GPC reading the S-band transponder mode telemetry via the PCMMU), the AM sequence determines which S-band switch-beam quad-antenna contains the roll component of the look angle to the selected TDRS. The pitch component of the look angle is used to determine the forward or aft beam selection of the quad-antenna selected from the roll component of the look angle. The antenna selection is commanded via discrete outputs through both PL MDMs (PL 1 for Antenna Electronics 1, PL 2 for Antenna Electronics 2). The previously selected antenna is deselected prior to selecting the new antenna. Only one of the switch-beam quad-antennas can be selected at a time. If no TDRS is selected, the ground has the ability to command the antennas without inhibiting the SM first.

If the S-band PM transponder is in the TDRS position and a STDN/SGLS site is selected, the AM sequence determines which S-band FM hemi-antenna contains the roll part of the look angle to the current STDN/SGLS site. The hemi-antenna determined is selected via discrete outputs via both PL MDMs. The previously selected

hemi-antenna is deselected prior to selecting the new antenna. If there is no STDN/SGLS site in view, the PL MDM outputs are not changed. This function allows the FM to be pointed to a ground site while the PM is pointed to TDRS.

If the S-band PM transponder is not in the TDRS position and a current STDN/SGLS site is selected, the AM sequence determines which S-band switch-beam quad-antenna contains the roll component for the look angle to the current STDN/SGLS site. Additionally, the pitch component of the look angle is used to determine the FWD or AFT selection of the switch-beam quad-antenna selected above. The switch-beam quad-antenna determined above and the corresponding hemi-antenna are selected via discrete outputs via both PL MDMs, subject to the switching restriction specified below. The previously selected switch-beam quad- and hemi-antennas are deselected prior to selecting the new antennas. If one of the upper switch-beam quads is selected, the corresponding hemi is the upper hemi. If one of the lower switch-beam quads is selected, the corresponding hemi is the lower hemi. If a current STDN/SGLS site does not exist, the PL MDM outputs are not changed.

If there is a problem with the data transferred from the PCMMU to the SM because of an MDM OF3 failure, the crew can override the erroneous STDN/SGLS mode indication via item entry on SPEC 201.

If GPC antenna command of the S-band antenna selection is inhibited on SPEC 201 by item entry or via uplink, the switch-beam and/or hemi-antennas determined above are not selected via payload MDM outputs. This allows the ground to control the antennas via uplink of MDM discrete commands.

The detail formulation for the above functions is specified in SM Level C FSSR.

Switching restriction: After the initial selection, a new switch-beam antenna is selected only when the roll and pitch component parts of the look angle to the given target point are outside the transition region. The transition region is defined as each quadrant boundary axis  $\pm 2^\circ$  and as defined by constants specified in SM Level C FSSR for beam switching.

#### **14.2.1.4 S-Band Quad- and Hemi-Antenna Selection Verification**

If S-band AM is enabled on SPEC 201 or via uplink and the S-band PM ANTENNA SELECT switch on panel C3 is in the GPC position, the switch-beam antenna commanded during the last previous computation cycle described above for either the TDRS or STDN/SGLS is compared with the actual switch-beam antenna selected at the Radio Frequency (RF) switch during this computation cycle. If this comparison fails, a discrete parameter is enabled (value = 1) to indicate the failure and SM Fault Detection and Annunciation (FDA) generates the message "Antenna". If the comparison is satisfied or is not performed, the discrete parameter is disabled (= 0). The computation of the actual switch-beam antenna selected at the RF switch assembly is specified in SM Level C FSSR and summarized below.

If S-band AM is enabled on SPEC 201, S-band-to-STDN communications are being performed, and the S-band FM ANTENNA SELECT switch on panel A1 is not in the UPPER HEMI or LOWER HEMI position (i.e., in the GPC position), the selected hemi-antenna computed during the previous computation cycle is compared with the actual hemi-antenna selected at the RF switch during this computation cycle. If this comparison fails, a discrete parameter is enabled to indicate the failure. The crew does not have insight into this failure nor do they receive an error message. If the comparison is satisfied or is not performed, the discrete parameter is disabled. Computation of the actual hemi-antenna selected at the RF switch assembly is specified in the SM Level C FSSR. A summary follows.

A. Verification of quad-antenna selection

1. The following input parameters are required:

| <b>Symbol</b> | <b>Measurement name</b>         | <b>Measurement no.</b> |
|---------------|---------------------------------|------------------------|
| a             | S-BAND QUAD ANT SEL - S1A ON    | V74X7070E              |
| b             | S-BAND QUAD ANT SEL - S1B ON    | V74X7072E              |
| c             | S-BAND QUAD ANT SEL - S2A ON    | V74X7074E              |
| d             | S-BAND QUAD ANT SEL - S2B ON    | V74X7076E              |
| e             | S-BAND QUAD ANT SEL - S3A ON    | V74X7078E              |
| f             | S-BAND QUAD ANT SEL - S3B ON    | V74X7080E              |
| g             | S-BAND QUAD ANT SEL - S4A ON    | V74X7082E              |
| h             | S-BAND QUAD ANT SEL - S4B ON    | V74X7084E              |
| l             | GCIL - XPNDR 1 DIRECT           | V74X4780E              |
| m             | GCIL - XPNDR 2 DIRECT           | V74X4781E              |
| n             | GCIL - PREAMP HIGH FREQ         | V74X4779E              |
| p             | GCIL - PREAMP LOW FREQ          | V74X4778E              |
| q             | S-BAND QUAD ANT UPPER LEFT FWD  | V74X7090E              |
| r             | S-BAND QUAD ANT UPPER LEFT AFT  | V74X7091E              |
| s             | S-BAND QUAD ANT UPPER RIGHT FWD | V74X7092E              |
| t             | S-BAND QUAD ANT UPPER RIGHT AFT | V74X7093E              |
| u             | S-BAND QUAD ANT LOWER LEFT FWD  | V74X7094E              |
| v             | S-BAND QUAD ANT LOWER LEFT AFT  | V74X7095E              |
| w             | S-BAND QUAD ANT LOWER RIGHT FWD | V74X7096E              |
| x             | S-BAND QUAD ANT LOWER RIGHT AFT | V74X7097E              |

2. The following sets of logical expressions denote valid antenna selections. All others indicate improper selection.

Valid selections for UPPER RIGHT quad are

$$s \cdot [(a \cdot h \cdot l) + (b \cdot d \cdot m) + (a \cdot g \cdot n) + (b \cdot c \cdot p)] = \text{true for FWD beam}$$

$$t \cdot [(a \cdot h \cdot l) + (b \cdot d \cdot m) + (a \cdot g \cdot n) + (b \cdot c \cdot p)] = \text{true for AFT beam}$$

Valid selections for LOWER RIGHT quad are

$$w \cdot [(f \cdot g \cdot l) + (c \cdot e \cdot m) + (f \cdot h \cdot n) + (d \cdot e \cdot p)] = \text{true for FWD beam}$$

$$x \cdot [(f \cdot g \cdot l) + (c \cdot e \cdot m) + (f \cdot h \cdot n) + (d \cdot e \cdot p)] = \text{true for AFT beam}$$

Valid selections for LOWER LEFT quad are

$$u \cdot [(e \cdot g \cdot l) + (c \cdot f \cdot m) + (e \cdot h \cdot n) + (d \cdot f \cdot p)] = \text{true for FWD beam}$$

$$v \cdot [(e \cdot g \cdot l) + (c \cdot f \cdot m) + (e \cdot h \cdot n) + (d \cdot f \cdot p)] = \text{true for AFT beam}$$

Valid selections for UPPER LEFT quad are

$$q \cdot [(b \cdot h \cdot l) + (a \cdot d \cdot m) + (b \cdot g \cdot n) + (a \cdot c \cdot p)] = \text{true for FWD beam}$$

$$r \cdot [(b \cdot h \cdot l) + (a \cdot d \cdot m) + (b \cdot g \cdot n) + (a \cdot c \cdot p)] = \text{true for AFT beam}$$

Note: (•) Indicates logical AND function.  
(+) Indicates logical OR function.

3. Output

|                                     |                        |
|-------------------------------------|------------------------|
| <b>Measurement name</b>             | <b>Measurement no.</b> |
| S-BAND QUAD ANT SELECTED (COMPUTED) | V92J1057C              |

| <b>For selected antenna =</b> | <b>Output code (binary equivalent)</b> |
|-------------------------------|--|
| UPPER RIGHT                   | 1                                      |
| LOWER RIGHT                   | 2                                      |
| LOWER LEFT                    | 3                                      |
| UPPER LEFT                    | 4                                      |

|                                    |           |
|------------------------------------|-----------|
| S-BAND SW BEAM SELECTED (COMPUTED) | V92J1062C |
|------------------------------------|-----------|

| <b>For selected switch-beam =</b> | <b>Output code binary equivalent</b> |
|-----------------------------------|--------------------------------------|
| FWD                               | 1                                    |
| AFT                               | 2                                    |
| Destination: AM function          |                                      |

B. Verification of hemi-antenna selection

1. The following input parameters are required:

| Symbol | Measurement name           | Measurement no. |
|--------|----------------------------|-----------------|
| j      | S-BAND FM ANT SEL - S5A ON | V74X6675E       |
| k      | S-BAND FM ANT SEL - S5B ON | V74X6676E       |
| q      | FM TRANSMITTER PWR ON 1    | V74X6120E       |
| r      | FM TRANSMITTER PWR ON 2    | V74X6121E       |

2. The following sets of logical expressions denote valid antenna selections. All others indicate improper selection.

Valid selection for UPPER HEMI is if  $(j \bullet q) + (j \bullet r) = \text{true}$

Valid selection for LOWER HEMI is if  $(k \bullet q) + (k \bullet r) = \text{true}$

Note: (•) Indicates logical AND function.  
(+) Indicates logical OR function.

3. Output

| Measurement name                    | Measurement no. |
|-------------------------------------|-----------------|
| S-BAND HEMI ANT SELECTED (COMPUTED) | V92H1056C       |

| For selected antenna =   | Output code binary equivalent |
|--------------------------|-------------------------------|
| UPPER HEMI               | 1                             |
| LOWER HEMI               | 2                             |
| Destination: AM Function |                               |

### 14.2.2 TDRS Computations - SM

AM calculates the positions of each TDRS every 1.92 seconds. The positions of each TDRS is computed via an “ $\omega \times WT$ ” process using the current GMT timetag of the Navigation (NAV) state vector, the inclination of the satellite orbit, the longitude of the ascending node for a specified equatorial crossing, the magnitude of the TDRS position vector, and the GMT timetag of the ascending node crossing. Six computed TDRS position vectors are made available for downlist. These constants can be changed with each TDRS state vector command uplinked.

Based on the computed position of each TDRS and the current orbiter position received via ICC from the GNC application, the AM sequence computes the line-of-sight vector from the orbiter to the TDRS and the corresponding line-of-sight roll/pitch look angles in the orbiter coordinate system to each TDRS. The orbiter attitude data used in the above computation are updates of the current ICC data as compensated for data transport delay by the attitude compensator. Data transport delay is defined as the sum

of the computed difference between the current GMT and the GMT timetag associated with the attitude data set and a constant factor “t” msec (in seconds) to compensate for additional delays. In addition, a discrete parameter is computed for each TDRS, which indicates whether or not the TDRS is in the Line of Sight (LOS) of the orbiter at least  $X^\circ$  (or the equivalent of  $X^\circ$ ) above the geocentric horizon. This in-view parameter is used for automatic uplink control. The value of the “t” msec delay (V90W1013C) (in seconds) and the value of the  $X^\circ$  constant (V92H1006C) can be changed via the TM SPEC or TMBU.

The detail formulation for this computation is specified in the SM Level C FSSR.

### 14.2.3 Ku-Band Antenna Management - SM

The Ku-band AM sequence consists of the following functions:

- Selection of TDRSs available for use
- Computation of pointing data for the Ku-band Communications (COMM) rendezvous RADAR antenna to the selected TDRS or GNC designated target.

These functions are performed cyclically (once every 2 seconds). In addition to these functions, the auto-acquisition sequence of the Ku-band antenna for acquisition of either the selected TDRS or the GNC designated target can be controlled. If the GNC angle-pointing flag is inhibited, the Ku-band antenna is controlled as described in Section 14.2.3.1. If the GNC angle-pointing flag (GNC SPEC 33 item 2) is enabled, the Ku-band antenna is controlled as described in Section 14.2.3.4. The current value of the GNC angle-pointing flag is made available for display and/or downlist.

Data acquisition of Ku-band antenna data over the payload MDM (PL 1, Card 8, Channel 2) Serial Input/Output (SIO) channel is performed regardless of the state of the GNC angle-pointing flag. The number of words transferred to the Ku-band antenna is the same in both the communication and RADAR modes. The number of words acquired from the Ku-band antenna is also the same in both the RADAR and the communication modes.

The SM, via PL1, and GNC, via FF3, requests for data from the Ku-band antenna are normally spaced, with respect to each other, so that a minimum of 122  $\mu$ sec elapses between the last data word of a message and the first data word of the next response message at the MDM output(s) to the Ku-band antenna. This action is required because of Ku-band hardware restrictions in the Ku-band signal processor.

#### 14.2.3.1 Ku-Band AM for TDRS Communications

The SM contains six TDRS vectors. AM attempts to point the antenna first at the target (A or B) that is prime if it is in view and the SV slot assigned to that target is enabled. If the prime target is not in view or the SV slot is not enabled, the other target is selected if it is in view and its associated SV slot is enabled. If neither target is selected, then AM tests each of the SV slots to see if any are enabled and in view. The first slot that is in



view and enabled will be selected. SPEC 201 will display a box (□) around selected TDRS vector number or target.

### **14.2.3.2 Ku-Band Antenna Pointing**

Using the computed line-of-sight vector (in orbiter coordinates) to the selected Ku-band TDRS, the AM sequence biases the LOS vector from the orbiter to the selected TDRS in orbiter coordinates, using a 3 by 3 matrix (defined preflight). The roll and pitch look-angle values to the selected TDRS are then computed in a roll-pitch sequence from this vector. The value of each of the elements in the 3 by 3 matrix can be changed via the TM constant display. The ability to change the matrix via ground command was deleted from the new generic command server. These constant values are included in the SM checkpoint. The detail formulation for these computations is specified in SM Level C FSSR.

### **14.2.3.3 Ku-Band Antenna Control - SM**

The AM function in the SM computer also contains the ability to configure certain Ku-band functions. This is performed via the Ku-band SIO interface from PF 1 MDM.

One of the major purposes of the SIO channel on PF 1 is to allow the SM computer to pass pointing angles to the Ku antenna. Pointing angles are passed to the Ku-band in two modes, GPC and GPC designate. These modes are used when the Ku-band system is configured for either communications or RADAR. The other two modes of the Ku antenna, auto and manual, do not require SM software pointing.

In GPC mode, the Ku-band is initially commanded to the angles calculated by AM for the intended target (TDRS or a rendezvous target). The Ku-band is then commanded to perform a hardware search about this point. If the Ku-band finds the target (by detecting a signal), the search is terminated and the Ku-band hardware is used to autotrack the target.

GPC designate is a programmed mode of pointing. In this mode, the SM GPC continuously calculates pointing angles to the target and then issues commands to the Ku-band hardware to slew to those pointing angles. Autotrack functions of the Ku-band hardware are not used in this mode. There are roll (+90 and -90 azimuth) and pitch (+90 and -90 elevation) angles at which the SM GPC cannot calculate pointing angles because of a mathematical singularity. These roll and pitch angles will cause the SM to stop commanding the Ku antenna dish to move, thereby losing forward link lock. Once the calculations for the roll angle have moved to the other side of the singularity, the SM AM continues to command the correct roll or pitch angles.

In addition to passing Ku pointing angles over the PF 1 SIO channel, the SM GPC can pass command signals to Ku-band microprocessor over this SIO link. The following signals can be passed to the Ku-band processor over this link:

A. Discretes

Ku-band Comm BRK TRK CMD TGL1  
Ku-band Comm BRK TRK CMD TGL2  
  
Spread/spectrum ON/OFF  
KU A/B select  
Self-test on/off  
Modulation control (ON/OFF AUTO)  
Primary acquisition mode ON/OFF  
GPC designate inertial stabilization ON/OFF  
Forward link 72/216 kbps  
RADAR threshold variable/fixed  
Traveling Wave Tube Amplifier (TWTA) ON/OFF  
Beta masking mode

B. Numbers

Designated angle - azimuth  
Designated angle - elevation  
Designated radar range  
Beta angle value

Descriptions of the functions that the Ku-band microprocessor performs in response to these discretes and numbers, can be found in Systems Brief 10, Ku-Band Software Description for EA-1. All of the above functions can be set from the ground by using the Ku-/S-band antenna OP code except the beta value. The beta value may be set by SM TMBU.

Basically, the SM GPC takes the uplinked values, then places them in a buffer that is cyclically transmitted to the Ku-band electronics via the SIO channel on PF 1.

The crew can access the following functions in the Ku-band SIO antenna control word from the SM 201 ANTENNA SPEC:

Ku radar range minimum (Auto, item 16; Min, item 17)  
Self-test (item 7)  
I/O reset (item 8)  
TDRS Ku Pri (A, item 9; B, item 10)

In addition, the crew can reset the Input/Output (I/O) between the SM computer and the Ku-band by specific item entry on the ANTENNA SPEC or by a general SM I/O reset.

Commanded as well as actual Ku-band pointing angles are also displayed for the crew on the ANTENNA SPEC. For more details on the ANTENNA SPEC see Section 14.4.2.

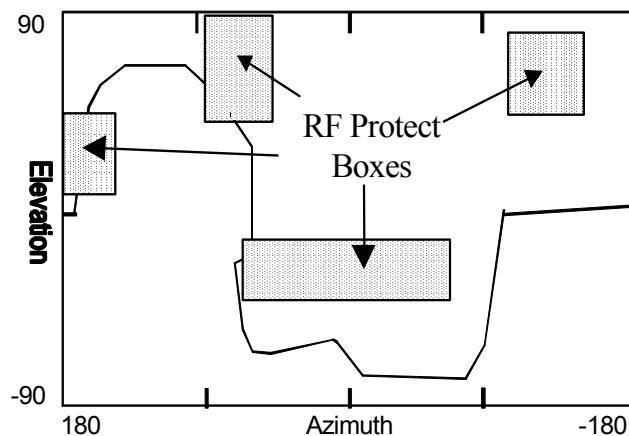
#### 14.2.3.3.1 Ku RF Protection Boxes

The Traveling Wave Tube (TWT) generates the carrier that is put out through the Ku-band antenna. There are several ways to control the ON/OFF state of this device. The following paragraph discusses this process.

The SM software has the capability to turn the TWT off, dependent on the pointing angles returned from the Ku-band antenna via the PL 1 MDM. The development of four RF Protect Boxes, stored within SM GPC software defined by groups of azimuth (roll) and elevation (pitch) angles is designed to protect the EVA crew and hardware as well as protecting the Ku-band system from reflected RF radiation. If GNC Pointing is inhibited, when the SM detects that the pointing angles are within an enabled RF Protect Box, the SM commands the TWT off.

Each of the boxes can be individually enabled or inhibited. Default state for all four boxes is inhibited.

The RF Protect Boxes subroutines are bypassed in RADAR Mode; the SM GPC receives the GNC GPC SPEC 33 Item 2 via the ICC Bus to determine whether Ku-Band is in RADAR Mode.



The ground can command the TWT back on after the SM has turned it off, but that is not advised.

The process is well documented in Section 6.3.2 of the Space Shuttle Computer Program Development Specification (CPDS), Functional Level Requirements, Systems Management (SS-P-0002-580).

#### 14.2.3.3.2 Beta Gimbal Limit Protection

The SM software protects an area near both beta ( $\beta$ ) gimbal limits to ensure that the antenna drive does not force the antenna against the hard stops for an excessive period of time, which could damage the gimbal motor. This problem has occurred on earlier flights. The area to be protected is called the forbidden zone. It is defined as:

- $\beta \geq 74.5^\circ$  for the positive beta stop
- $\beta \leq -83.5^\circ$  for the negative beta stop

These angles are the actual angles and not the designated (commanded) angles.

The software monitors the angles, and, if the forbidden zone is entered, a counter (V92Q0103C) is started and a flag (V92X0104X, Ku-Band Beta Stop Flag) is set. The counter increments to 125 (1.92 seconds/count) or 240 seconds before the Ku-band system is commanded to standby mode via both PF 1 and PF 2 MDMs (Ground Command Interface Logic (GCIL) command). This prevents the antenna from moving any farther into the forbidden zone. If the forbidden zone is exited before the counter reaches 125, the counter is reset to 0 and the flag is turned off. When the Ku-band system is commanded to standby, the counter and flag are also reset to 0.

Another flag (V92X0993X, Ku-Band Beta Limit) is turned on when the Ku system is commanded to standby so that the ground understands why this action took place. Once the Ku-band system is commanded to standby, the software monitors the designated beta angles to determine when the system commands a beta angle that is outside of the forbidden zones. The SM commands the system back on once the designated angles are outside the forbidden zones.

#### 14.2.3.3.3 Acquisition Sequences

There is only one antenna mode of the Ku-band where there is special SM GPC software processing. This is the GPC mode. In GPC mode, the SM GPC is programmed to set the search initiate discrete whenever the Ku-band is not detecting a target (a radar return or the Ku-band forward link from the TDRS) or whenever a handover between satellites has occurred. After a new detect has occurred, indicating that the Ku-band hardware has found the target or the TDRS forward link, the SM GPC deactivates the search initiate discrete.

In fact, the key to understanding the GPC mode of the Ku-band is to understand how this mode was labeled early in the program. Early in the program this mode was called GPC ACQ for GPC-controlled acquisition. The basic concept for this mode is for the SM GPC to steer the antenna close to the target (either a rendezvous target or TDRS) and then initiate a Ku-band hardware search. The idea was that the initial GPC pointing would be close enough to get the target within the search radius of the Ku-band and thus allow the Ku-band to lock up and autotrack.

Each AM cycle, it checks to see if the Ku-band antenna is in GPC mode and the interface is enabled. If it is in GPC mode, then the SM checks to see if the selected TDRS is in view. If it is in view, AM checks to see if Ku-band is locked on the TDRS. If it is locked, SM special processing terminates and the angles are output to the Ku-band via the SIO (PL 1 MDM) link. In this situation the Ku-band ignores the angles because it is already tracking the TDRS (or a rendezvous target if the GNC pointing flag is enabled).

If, however, SM determines that the selected TDRS (or rendezvous target) is in view, in GPC acquisition mode, and the Ku-band is not locked (either because of a drop or a new Acquisition of Signal (AOS)), the AM starts an acquisition sequence.

The acquisition sequence consists of two parts. First, the SM GPC uses Break Track Logic bits (SIO Control Word 1, bits 1 and 2) to direct EA-1 to look at the new Designate Azimuth and Elevation Angles. The purpose of this is to force the Ku-band to break autotrack on one satellite when handing over to another satellite. On the next cycle, the SM GPC sets both satellite select discrettes (in the SIO control word) to zero to avoid interfering with future operations.

At this point in the acquisition procedure, two important things have happened. First, the SM GPC has told the Ku-band where to steer. EA-1 will now steer using "rate control logic", within EA-1, towards those designate AZ and EL angles. When the Ku-Band Dish actual AZ and EL angles are within .3 degrees of the designated SM GPC AZ and EL angles; EA-1 will process any uplink carrier for received signal strength and verify uplink modulation with a "DETECT". EA-1 will send this "DETECT" back to the SM GPC, via SAO Status Word 2 bit 1; the Ku-Band EA-1 will begin tracking the forward link errors in AZ and EL carrier signal to maintain communication with the TDRS Satellite. If SM GPC does not receive the "DETECT" bit back within 20 seconds, the SM GPC will turn on the search initiate discrete, via SIO Card 8, WD 2 Bit 0, to the Ku-band hardware. When the Ku-band hardware receives the search initiate discrete, it starts a search procedure in the Ku-band hardware under the control of the Ku microprocessor in EA-1. The Ku-band echoes the search status back to the SM GPC.

When the SM GPC sees the search discrete on in the Ku-band response word, it turns the search initiate discrete off in the SIO command buffer. If there is no DETECT when the search discrete in the Ku-band response word goes low, then the SM GPC initiates another acquisition sequence. In this way, the GPC continues to start the search routines. Note that the designated angles to the target change as the GPC computes new pointing angles. In this way, the chances of a search being successful are increased because the antenna is always being pointed to the best estimate of the TDRS (or rendezvous target) position.

The 20-second delay parameter can be modified by TMBU uplink or from SPEC 60. This parameter is identified by Measurement Stimulus Identification (MSID) V92W1010C KU BAND GPC ACQ DELAY TIME and is I-loaded to 20 seconds.

#### **14.2.3.4 Ku-Band Antenna Pointing Based on GNC Target Position**

The GNC computer can use the Ku-band in RADAR mode to target some object for a rendezvous. The AM software is designed to take pointing information from the GNC in much the same way for the RADAR mode and the communications mode of the Ku-band. AM senses that the GNC needs to point the Ku-band RADAR at a target when the GNC angle-pointing flag is enabled (GNC SPEC 33 – item 2). Once this item is selected, AM starts using the GNC target vector in place of the TDRS target data to point the Ku-band antenna.

There are two range modes that the Ku-band RADAR can operate in. When the minimum radar range mode item is selected from SPEC 201, parameters used to start a search for the target are set to a range of 2400 feet with the antenna angles set to azimuth (roll) = 0 and elevation (pitch) = 0. This range mode is used when the target is close to the orbiter. When the minimum radar range item is deselected, the GNC vector required to point at a target is used instead of the fixed values in the minimum range mode. The roll and pitch look-angles to the target are computed. First the roll component, then the pitch component is calculated (roll-pitch sequence) and output each AM cycle, rather than the roll and pitch angles to the selected TDRS. The estimated range of the target also is computed from the resulting vector. This parameter is converted to hardware angles and output to the antenna drive motors.

On the OI-26/-27 version of SPEC 201, there is a capability to select a RADAR threshold. The Ku-band system never implemented this capability, so if one of the item entries for this function is selected on the display, the Ku ignores it. For OI-28 the item entries have been removed from the display.

#### **14.2.3.5 Ku-Band Communications Control**

When SM is initialized from mass memory, Ku-band PF 1 SIO communications is enabled. Generally, this communication is then bypassed because the Ku-band system is not activated until after the SM is initialized. The SM application must re-enable the communication between the GPC and the Ku-band PF 1 SIO channel via onboard display item entry (SPEC 201 item 8) or command uplink. Once communications are established, the SM application resets the Bus Control Element (BCE) used for communicating with the Ku-band PF 1 SIO channel. If a communications problem occurs, the SM annunciates the error message BCE BYPASS KU and bypasses the BCE that sends commands to and receives data from the Ku-band system.

#### **14.2.4 Auto-Handovers Between S-Band and Ku-Band**

The SM AM software will be able to automatically configure the forward link from the S-band system to the Ku-band system and back. The reason for this enhancement was to simplify the amount and type of commanding required to force the systems to hand over to and from each other. The SM AM will determine if the capability has been enabled before executing the auto handover. The crew cannot enable or disable this capability. When the SM is initialized, the capability is disabled, but it can be enabled via command from the ground. If the S to K handover is enabled, the AM looks for the DATA PRESENT equal to 1 (V74X2613J) and a signal strength greater than -100 dB. Once these conditions are satisfied, AM waits 15 seconds to be sure that the link is stable; then it sends GCIL commands to configure the Network Signal Processor (NSP) (Source Ku and Uplink Coding OFF) to use the Ku-band as the forward link for commands and voice. If the K to S handover is enabled, the AM looks for Ku data present to be low (0) for 5 seconds. If this condition is met, AM issues GCIL commands to configure the NSP (Source S-band and Uplink Coding ON) to use the S-band system as the forward link for commands and voice. If the Ku-band system is taken to RADAR or Standby, the auto-handover capability sends the TDRS Salvo GCIL command,

followed by GCIL commands for uplink high data rate, downlink high data rate, and transponder filter wide. Some of the controlling conditions may be adjusted via SM TMBU. The following table lists the MSIDs and their default values.

| MSID      | Default value | TMBU | Nomenclature (name)            |
|-----------|---------------|------|--------------------------------|
| V93V1017C | 1.04 volts    | YES  | Auto Ku to S H/O Min AGC       |
| V93W1018C | 15 Sec        | YES  | Auto S-BD to Ku-BD H/O Time    |
| V93W1019C | 5 Sec         | YES  | Auto Ku-BD to S-BD H/O Time    |
| V93X1012X | 0             | NO   | Auto Ku-BD to S-BD H/O Enable  |
| V93X1013X | 1             | NO   | Auto Ku-BD to S-BD H/O Inhibit |
| V93X1015X | 0             | NO   | Auto S-BD to Ku-BD H/O Enable  |
| V93X1016X | 1             | NO   | Auto S-BD to Ku-BD H/O Inhibit |

#### 14.2.5 Antenna Management ICC Data

The SM acquires the parameters listed below from the GNC application via ICC in a time-homogeneous data set at least once per 1.92 seconds. The homogeneity of this data set is maintained in the performance of the AM function. The parameters are defined below; no parameter status is required. If an I/O error occurs that affects these data, the last valid update is processed by the AM function.

- A. Current orbiter position in the Greenwich True of Date (TOD) Cartesian coordinate system. The position consists of three double-precision floating-point parameters (x, y, z).
- B. Current orbiter velocity in the Greenwich TOD Cartesian coordinate system. The velocity consists of three single-precision floating-point parameters ( $\dot{x}$ ,  $\dot{y}$ ,  $\dot{z}$ ).
- C. GMT timetag of the above parameters in one double-precision floating-point word.
- D. Current orbiter attitude that describes the orientation of the orbiter body axes relative to the Greenwich TOD Cartesian coordinate system. The attitude consists of three single-precision floating-point parameters (roll, pitch, yaw).
- E. Current orbiter attitude rates in the orbiter body axes. These data consist of three single-precision floating-point parameters (roll rate, pitch rate, yaw rate).
- F. GMT timetag of the above parameters in one double-precision floating-point word.

#### 14.2.6 OPS Transition Points

The transition from any OPS to any other OPS is legal after SM is initialized. All OPS mode transitions are via OPS mode number entry. There is no interface (transition of processing or data) between the SM major function and the Backup Flight Control System (BFCS) memory configuration. The values that are maintained during and after and Ops transition are documented in the Systems Management CPDS (SS-P-0002-580).

### 14.3 BFS DETAILS

The primary purpose for the AM function resident in the BFS computer is to automatically select antennas for S-band communication during ascent and entry mission phases (OPS modes 1, 3, and 6). BFS AM is not available in OPS 0. Manual antenna selection via crew switch or uplink command is required in this operational mode. The BFS cannot command the Ku-band antenna since that system is designed to be stowed and turned off during the phases of flight that the BFS software is used. The BFS AM commands both the S-band PM and the S-band FM antenna selections. The S-band PM antenna selection is dependent on the mode of the S-band transponder (TDRS or STDN/SGLS). The FM antenna selection is also dependent on the S-band transponder mode (no antenna selection when transponder in TDRS mode) but only selects antennas to point to ground sites.

The AM function computes the current position of the orbiter and the current position of the target (TDRS or Ground) and determines if the target is in view of the orbiter during each AM cycle (every 1.92 sec). If it is in view, the antennas are chosen based on the target placement within the theoretical coverage of a spherical quadrant, for the PM antennas, and a hemisphere, for the FM antennas. The input data for the computation of the orbiter position and attitude are obtained, via the COMPOOL, from the Navigation Application function. The PM transponder mode data are obtained through the PCMMU from MDM OF3.

The BFS commands a new antenna to point to the target if the target point is at least 2° past the quadrant (for PM antennas) boundary. For the PM antennas, the orbiter pitch is used to determine which beam of the antenna to select. The forward beam is selected if the pitch is less than 83°. If the pitch angle is greater than 87°, the aft beam is commanded. If the pitch is between 83° and 87°, no beam is commanded. For the FM antennas, if the S-band transponder is not in TDRS mode and an upper quad is selected, the upper hemi-antenna is selected. If the lower quad is selected, the lower hemi is selected. The BFS deselects the current antenna before commanding the new antenna.

BFS OI-30 software now contains the correct Ponce DeLeon (PDL) ground station position data (X,Y,Z) and the correct default Site Inhibit Flags with the PDL site enabled and the MILA site inhibited.

#### 14.3.1 TDRS Mode

During each AM cycle, if the PM transponder is in TDRS mode, the current position and visibility of the three TDRS state vectors are determined. The TDRS with the lowest state vector number that is in view is selected. If no TDRS is in view or if the BFS is in OPS 0, the BFS does not attempt to command any antenna change. The FM antennas are not commanded while the transponder is in TDRS mode.



#### 14.3.1.1 STDN/SGLS Mode

During each AM cycle, if the PM transponder is selected to STDN/SGLS mode, the current station is selected from a table based upon which ground site is visible and enabled for communication. The visibility test is conducted for all sites in the order in which they are listed in the table, regardless of where the test is started. There are 16 sites listed in the table. These site positions can be updated via a TMBU command.

The site enable/inhibit status can also be changed via TMBU command. Once a site has been selected, the BFS selects both the PM and the FM antennas for best communications with that site. The BFS continues to point the antennas at that site until it is no longer in view. If the BFS cannot find a site that is in view and enabled or if the BFS is in OPS 0, it does not attempt to command any antenna.

#### 14.3.2 BFS SPEC 51

Due to the inability for the crewmembers to reach panel A1, a capability is added to the BFS software to allow the crew to force the BFS to send GCIL Salvo commands to configure S-Band PM System. On SPEC 51 the override display, the crew can issue:

Item 46 for TDRS mode

Item 47 for STDN HI mode

Item 48 for STDN LO mode

Item 49 for SGLS mode.

NOTE: If the powered NSP is bypassed, the BFS will not process these item entries.

### 14.4 CREW INTERFACES

The crew has the capability to control some of the functions of the AM system. The following sections discuss the equipment (switches and meters) and displays that the crew has available.

### 14.4.1 BFS S-Band Communication Reconfiguration (SPEC 51)

During ascent and entry phases, the crew cannot easily reach the switches on panel A1 to perform a communications system reconfiguration. Item entries were added to the BFS Override SPEC for OI-28 so that the crew could more easily select transponder modes (TDRS, STDN high power, STDN low power, or SGLS). There is no AM display for the crew to monitor the AM software running in the BFS, but SPEC 51 (Figure 14-3) informs the crew when they have NSP frame lock. The display shows LOCK if one or both NSPs have a forward link frame sync and NOLK if neither has a forward link frame sync. The crew is dependent on the ground for insight into the BFS antenna software. The following is an example of the comm-related area of SPEC 51.

```

0 0 1 1 2 2 3 3 4 4 5
0123456789012345678901234567890123456789012345678901
0 |-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
1 - XXXX/051/ |-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
2 |-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
3 -ABORT MODE |-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
4 - TAL 1X |-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
5 - ATO 2X |-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
6 -ABORT 3X |-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
7 -MAX THROT 4X |-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
8 |-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
9 - PRPLT DUMP |-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
10 |-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
11-XXX ICNCT 5 XXXX |-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
12-OMS DUMP |-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
13- ARM 6X |-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
14- START 7X |-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
15- STOP 8X |-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
16- 9 QUAN/SIDE XXX |-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
17-OMS DUMP TTG XXX |-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
18 |-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
19-AFT RCS 13 XXX |-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
20- 14 TIME XXX |-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
21 |-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
22-FWD RCS 15 XXX |-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
23- 16 TIME XXX |-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
24 |-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
25----- (message line) ----- (XX)
26----- (scratch pad line) -----

```

Figure 14-3. SPEC 51

### 14.4.2 SM Displays

The primary means for the crew to manipulate the AM is through SM displays. The primary display is SPEC 201, which has several item entries that are used to select modes for AM.

#### 14.4.2.1 SPEC 201

The SPEC 201 display shown in Figure 14-4 was modified for the OI-29 flight software release because there were a couple of capabilities on the display that either were not implemented in the hardware (Ku RADAR threshold fixed or variable) or the function was not required by the crew (Scan Warn Override). The OI-29 version of the display added information about the six TDRS state vectors so that the crew would be able to tell which state vectors were activity being used by the antenna management software.

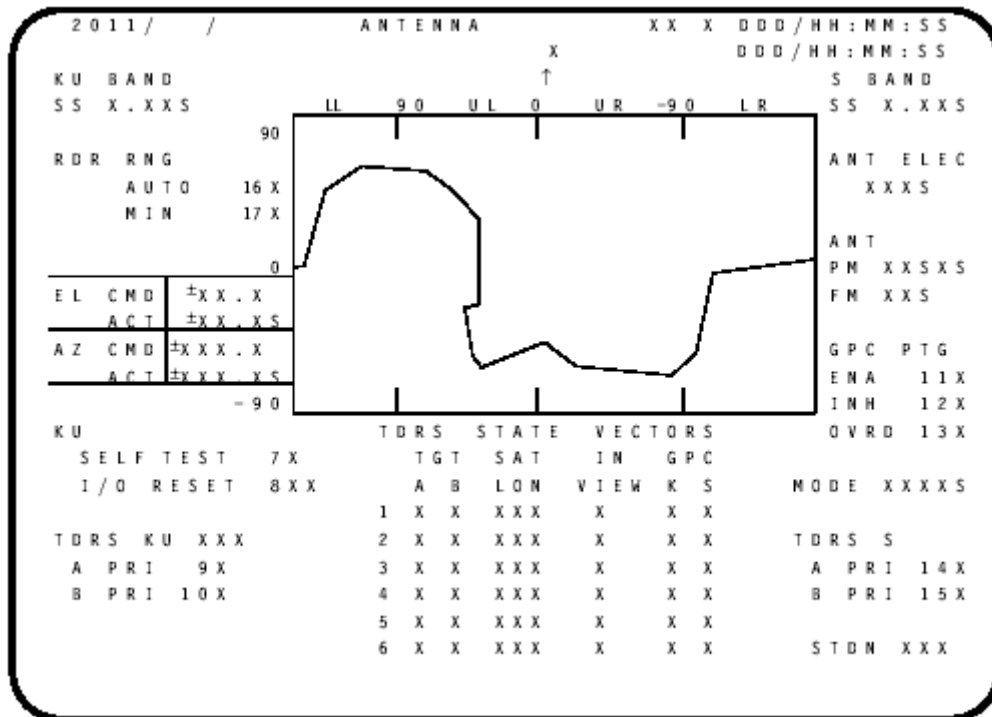


Figure 14-4. SM SPEC 201

SPEC 201 Item entries descriptions as referenced by DPS Dictionary:

ITEMS 1 through 6 TDRS TGT SELECT A or B – used to assign any of the 6 TDRS state vectors, to targets A or B. An '\*' is displayed in the 'A' column adjacent to the TDRS state vector slot number (1–6), if that TDRS state vector slot is selected as the 'A' target. An '\*' is displayed in the 'B' column adjacent to the TDRS state vector slot number (1–6), if that TDRS state vector slot is selected as the 'B' target. Only one TDRS state vector slot can be assigned to target 'A' or 'B' at a time. The same TDRS state vector slot can be assigned to both 'A' and 'B'.

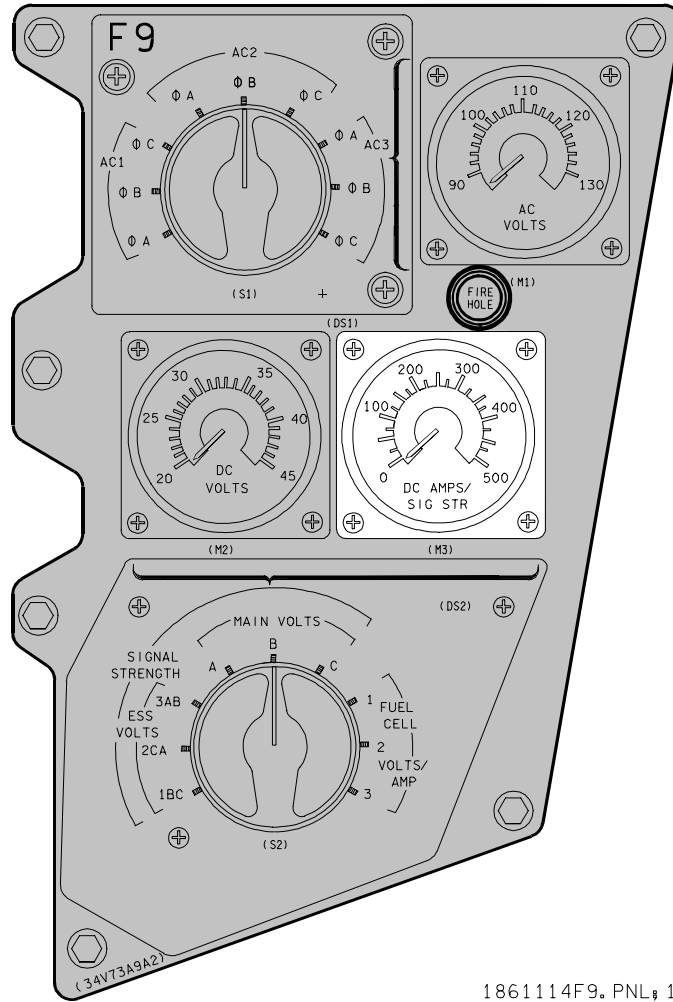
|                 |   |
|-----------------|---|
| ITEMS 16 and 17 | RDR RNG – used to control the range estimate output (AUTO or MIN) to the Ku-band Rendezvous Radar/COMM A system. An '*' is displayed next to the selected item. Initialization is in AUTO.  |
| ITEM 7          | SELF-TEST – used to select or terminate the radar self-test function. An '*' appears next to item 7 when the self-test is selected. After the 3-minute test is completed, item 7 must be reexecuted to deselect the self-test function and blank the test results (displayed on the Range meter on panel A2).   |
| ITEM 8          | I/O RESET KU – used to initiate communication between SM GPC and the Ku-band system. An '*' is displayed next to the item whenever the interface is enabled, otherwise an 'M' is displayed. When the SM is initialized, the interface is enabled.   |
| ITEMS 9 and 10  | TDRS KU PRI A/B – item 9 allows the SM Antenna Management (AM) software to select TDRS target 'A' for primary pointing of the Ku-band Comm antenna, if it is in view. If target 'A' is not in view but target 'B' is in view, the target 'B' TDRS satellite will be utilized for pointing. If neither target 'A' nor 'B' is in view, the lowest numbered TDRS state vector slot in view will be utilized for pointing (as denoted by the '*' located in the 'IN VIEW' column of the TDRS STATE VECTORS table). Item 10 allows AM to select TDRS target 'B' for primary pointing if it is in view. If target 'B' is not in view but target 'A' is in view, the target 'A' TDRS satellite will be utilized for pointing. If neither is in view the lowest numbered slot in view will be used for pointing. An '*' is displayed next to the selected item entry. Initialization is in TDRS Ku A PRI. |
| ITEMS 11 and 12 | GPC ANT CMD ENA/INH – used to enable or inhibit AM selection of S-band antennas. An '*' is displayed next to the selected function. ENA is selected at SM initialization.   |
| ITEMS 13        | OVRD – used to force AM to TDRS mode and remain there. This will allow AM to select the best S-Band antenna to TDRS even if there is a status problem preventing AM from knowing what is the correct mode. An '*' is displayed next to the item when it is enabled. The display is initialized with item 13 inhibited.  |
| ITEM 14 and 15  | TDRS S-Band PRI A/B – works the same as the Ku-band PRI A/B function but for the S-Band antennas.   |

### 14.4.3 Panel Controls and Readouts

The crew has four switch panels that they can use to control the selection of the S-band antennas and the Ku-band system. Panel C3 (Figure 14-6) includes a switch that is used to directly select an S-band PM antenna or to allow the SM or BFS AM software to automatically select the best antenna. Panel A1U is used to control the pointing function of the Ku-band antenna. Panel A1L is used to control the S-band PM system selection. Panel A1R is used to control the S-band FM system selection as well as antenna selection.

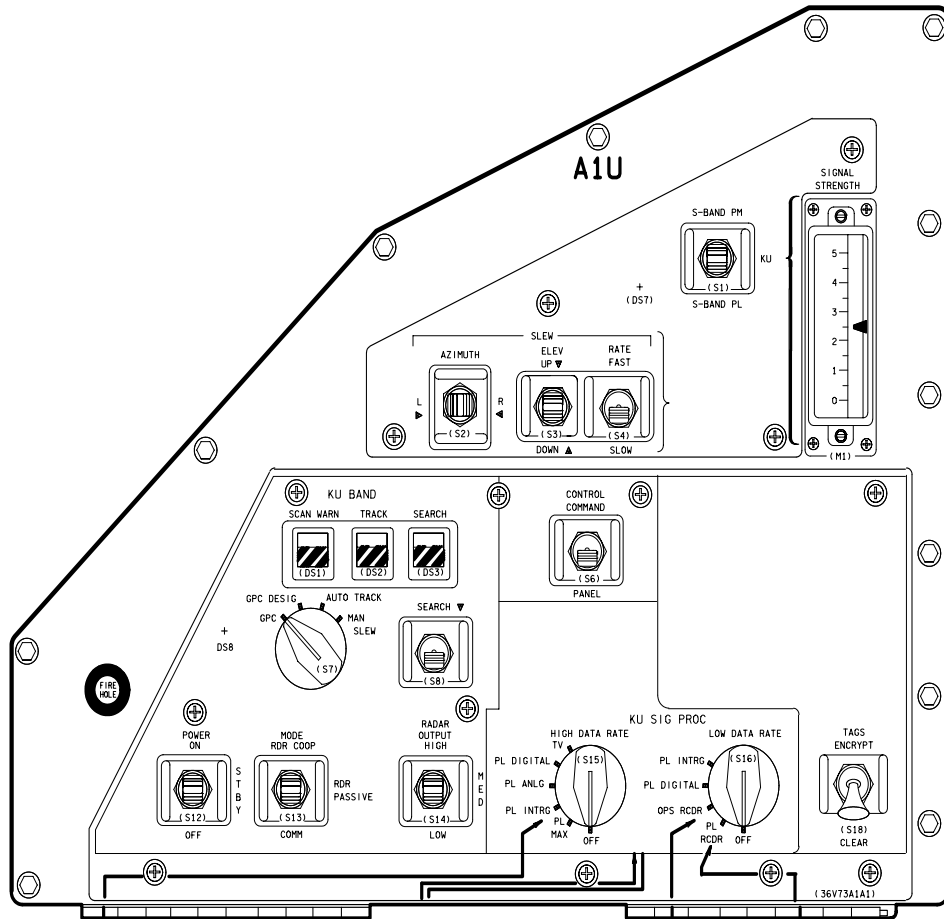
The crew has two locations to view signal strength of the forward link on the S-band PM and Ku-band systems. One of the meters is located on panel A1U, and the other is located on panel F9 (Figure 14-7). Panels AIU and A1U are shown in Figure 14-8.





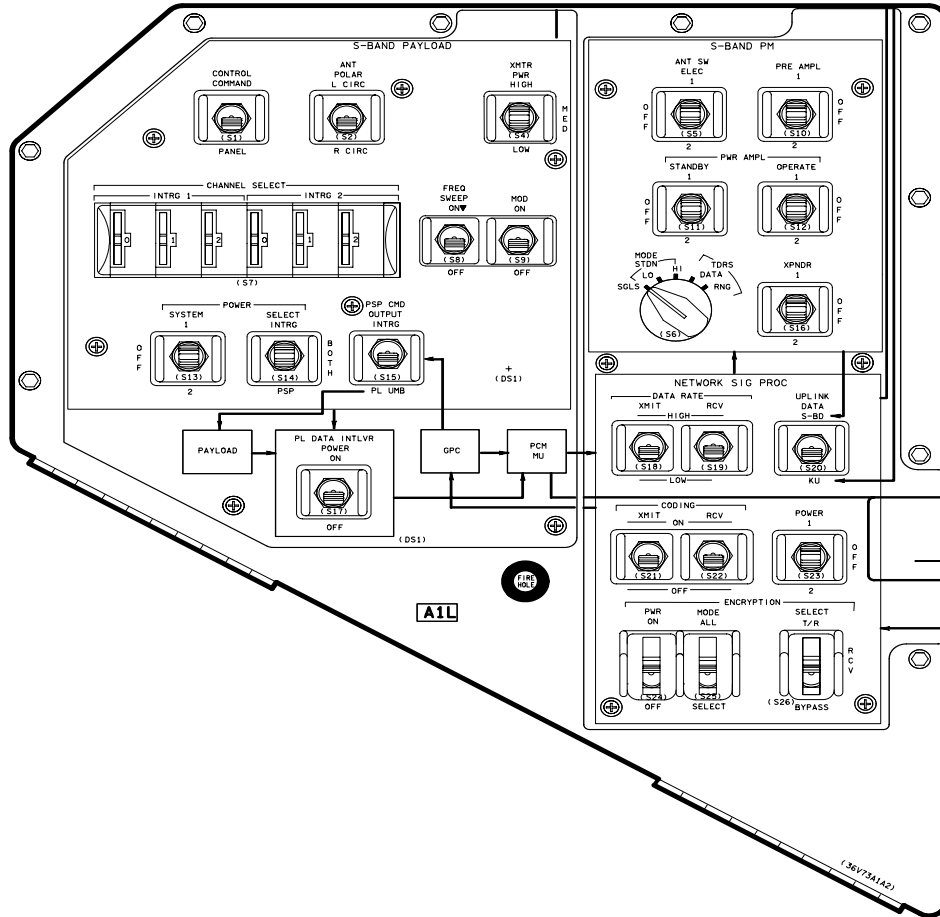
1861114F9, PNL# 1  
jsc\_18611\_4f9.cv5

Figure 14-6. Panel F9



1861114AU, PNL 1

Figure 14-7. Panel A1U



1861114AL.PNL+1

Figure 14-8. Panel A1L



## 14.5 ANTENNA MANAGEMENT IDIOSYNCRACIES

- A. If the SM computer crashes while the TDRS or an STDN site is in view, the SITE IN VIEW flag is locked on. The GNC computer does not reset this flag if the SM computer fails. If the SM crashes while the orbiter is LOS, the SITE IN VIEW flag is locked off. If commanding to GNC OPS 2 or 8 is required before the SM can be restored, use SPEC 1 uplink control - enable (item 36).
- B. AM uses data from OF3 MDM to determine if the target for S-band antenna selection should be TDRS or a ground station. AM software reads the value of V74X4786E GCIL S-BAND PM TRANSPONDER MODE - TDRS from the PCMMU. This value is the currently selected mode of the transponder as commanded by the crew or ground. If this parameter is a "1," the AM program selects the S-band antenna pointed at TDRS. If the parameter is "0" and a ground site is in view, AM selects the antenna pointed at the currently selected ground site. If the OF3 MDM fails or the PCMMU interface to the SM GPC fails, the SM GPC is not notified when the transponder changes modes. For example, if an SPC changes transponder modes from STDN to TDRS with OF3 MDM bypassed, the SM computer continues to select antennas for STDN.

If this is the case and the current major function is SM, the crew can execute an item 13 on SPEC 201 to force the SM to point antennas to TDRS. If the BFS is the major function, the crew has to select best antenna, or the ground can inhibit pointing and manually command the best antenna.

- C. SM AM verifies correct antenna selection by examining telemetry acquired via the PCMMU. If the SM GPC bypasses the PCMMU or the OI MDMs, the SM GPC is no longer able to get the antenna select discrettes. In this case, the AM program correctly selects antennas, but issues 2011 ANTENNA messages because it has stale data. The 2011 ANTENNA message can be inhibited by TMBU.
- D. If a problem occurs transferring the orbiter state vector data from the GNC to the SM via the ICC bus, the SM continues to process the stale orbiter data it receives as valid and to command the same S-band antenna. The eventual result is a loss of S-band communications, without generating any messages for the crew. They must select the best antenna from the panel C3 switch to recover S-band comm.
- E. In the GNC software there is a protection in place to prevent it from attempting to calculate Euler angles when the orbiter yaw angle is at  $\pm 90^\circ$ . This prevents the GNC from sending the SM new roll, pitch and yaw angle data (orbiter attitude goes static). If the Ku-band is in GPC Designate mode, the SM continues to command the antenna to the same angles since the data from the GNC are static. Since the Ku-band is a very small beam ( $3^\circ$ ), it loses lock on the forward link very quickly. The solution is to not operate the Ku-band system in GPC Designate at these times, if possible, or expect a temporary loss of Ku uplink and downlink. This problem was last seen on STS-88, during a Public Affairs Office event.
- F. Ku-Band Acquisition inside a RF Protect Box. In COMM Mode, the SM GPC RF Protect Box software is programmed to inhibit the TWT from turning on, if AZ and

EL are inside an enabled RF Protect Box. If the Ku-Band changes satellites to initial acquire inside an enabled RF Protect Box, EA-1 will automatically point the new TDRS, then EA-1 protocols will perform two parallel processes.

- If it detects the TDRS uplink, EA-1 will automatically start to radiate. This automatic process takes milliseconds to perform.
- EA-1 sends the AZ & EL information to the SM GPC. The SM GPC determines that Ku-Band dish is pointing inside an enabled RF Protect Box. The SM GPC will then command Ku-Band TWT-Off (Command WD 1 Bit 13). This takes a minimum of 1.92 seconds.

Operationally, the Ku-Band will initially acquire inside an enabled RF Protect Box, if EA-1 detects the uplink "faster" than 1.92 seconds, it will radiate inside the RF Protect Box, until SM GPC turns off TWT.

INCOs correct this action by predicting when the Ku-Band, acquires in an enabled RF Protect Box. INCOs will operationally send a Time Execute Command (TEC) to set Inhibit TWT - On prior to the TDRSS handover, and turn it back on ~ 1 minute after the Scheduled TDRSS Event starts.

- G. If the Ku-Band enters either of the two Beta Stops, the SM GPC will start incrementing a 126-counter clock (~4 min). If the Ku-Band continually points within this "forbidden zone" for > 126 clock cycles, the SM GPC will command Ku-Band to Standby. Once the SM GPC, using AM, designate angles are outside the "forbidden zone"; SM Software will command Ku-Band back to On. Because the Negative Beta Stop is near the Orbiter Docking Station (which contains pyros), INCOs have been commanding Ku-Band to STBY in this region (for a single failure case).

Operationally, INCOs prepare for a single failure case TWT radiating the ODS by predicting when the Ku-Band counts to 126 in the "forbidden zone" and send the Ku-Band TWT - Off command prior to SM GPC commanding Ku-Band to On.

- H. If we command Ku-Band to STBY then H/O to next TDRS and command Ku-Band back On, Ku-Band angles will still point to the old TDRS not the current active TDRS. The reason for this idiosyncrasy is, EA-1 is not programmed to "read" the EA-1 Serial Data Word through PF 1 when in STBY, so EA-1 "misses" the Break Track Toggles when in STBY so it initiates a search around the last angles it has stored in memory. After ~ 140 seconds of this search, EA-1 will receive the current active TDRS Pointing Angles in AZ and EL; EA-1 will then drive the Alpha and Beta motors to the newly active TDRS.

If you don't want to wait 140 seconds, just command Ku-Band to GPC Designate and command EA-1 to immediately look at the newly active TDRS Pointing Angles.

THIS PAGE INTENTIONALLY BLANK

**SECTION 15 - AUDIO DISTRIBUTION SYSTEM**  
**CONTENTS**

| <b>Section</b> |  | <b>Page</b> |
|----------------|--|-------------|
| 15.1           | GENERAL .....                                      | 15-1        |
| 15.2           | INTERFACES .....                                   | 15-1        |
| 15.3           | SYSTEM DESCRIPTION .....                           | 15-2        |
| 15.3.1         | Electrical.....                                    | 15-2        |
| 15.3.2         | Mechanical .....                                   | 15-5        |
| 15.4           | INSTALLATION.....                                  | 15-5        |
| 15.4.1         | Location.....                                      | 15-5        |
| 15.4.2         | Cooling .....                                      | 15-5        |
| 15.5           | OPERATIONAL DESCRIPTION .....                      | 15-10       |
| 15.5.1         | Crew Controls .....                                | 15-10       |
| 15.6           | SYSTEM OPERATION .....                             | 15-14       |
| 15.6.1         | ATU Subassembly .....                              | 15-14       |
| 15.6.2         | ACCU Subassembly.....                              | 15-18       |
| 15.6.3         | Speaker Unit .....                                 | 15-22       |
| 15.7           | SUMMARY DATA .....                                 | 15-22       |
| 15.8           | THE ACCU J3 and J4 BYPASS .....                    | 15-30       |
| 15.8.1         | The ACCU Bypass .....                              | 15-32       |
| 15.9           | SUGGESTED INCO ACTIONS FOR ACCU MALFUNCTIONS ..... | 15-35       |

## TABLES

| Table |   | Page  |
|-------|---|-------|
| 15-1  | Audio interface characteristics.....    | 15-1  |
| 15-2  | Hardline interface characteristics..... | 15-2  |
| 15-3  | Electrical characteristics .....        | 15-3  |
| 15-4  | Mechanical characteristics.....         | 15-5  |
| 15-5  | ATU/ACCU serial control data word ..... | 15-16 |
| 15-6  | ACCU J Plug Configuration .....         | 15-31 |

## FIGURES

| Figure |  |       |
|--------|--|-------|
| 15-1   | ADS .....  | 15-4  |
| 15-2   | ACCU LRU configuration.....                        | 15-6  |
| 15-3   | ATU LRU configuration.....                         | 15-7  |
| 15-4   | Flight Deck SU LRU on Panel A2 and Panel A13 ..... | 15-8  |
| 15-5   | HIU configuration .....                            | 15-9  |
| 15-6   | ATU panel.....                                     | 15-11 |
| 15-7   | ACCU panel controls .....                          | 15-13 |
| 15-8   | Audio control panel controls .....                 | 15-14 |
| 15-9   | Configuration control diagram.....                 | 15-21 |
| 15-10  | Flight Deck Speaker Control Logic .....            | 15-22 |
| 15-11  | Multiple headset adapter .....                     | 15-24 |
| 15-12  | Crew remote unit .....                             | 15-25 |
| 15-13  | Audio interface unit.....                          | 15-26 |
| 15-14  | Handheld mic.....                                  | 15-26 |
| 15-15  | Launch and entry helmet .....                      | 15-27 |
| 15-16  | Very lightweight headset.....                      | 15-28 |
| 15-17  | Headset interface unit.....                        | 15-29 |
| 15-18  | ACCU Hardware .....                                | 15-30 |
| 15-19  | ACCU Hardware J Plugs Wiring .....                 | 15-30 |
| 15-20  | ACCU Bypass Connector .....                        | 15-35 |

## SECTION 15 AUDIO DISTRIBUTION SYSTEM

### 15.1 GENERAL

The Audio Distribution System (ADS) provides the means for space shuttle crewmembers to communicate with each other and with the Mission Control Center (MCC) and to record voice annotation on the Solid State Recorders (SSR). It consists of redundant components designed to ensure at least one means of maintaining voice contact between the orbiter crew and the MCC.

The primary purpose of the ADS is to provide voice communication between the space shuttle orbiter crew and the flight control team in the MCC. In addition, the ADS provides a means for the crew to talk among themselves throughout the orbiter without shouting between the flight deck and the middeck and to record their conversations onto an SSR for later playback in the MCC.

### 15.2 INTERFACES

The ADS interfaces with the Network Signal Processors (NSPs) for communication with the MCC via the S-band Phase Modulation (PM) or the Ku-band systems and with the Ultrahigh Frequency (UHF) transceiver for communication with the MCC via the UHF voice system. Interfaces to external comm systems are established via control selections on the audio center panel. The audio center configuration control data route Audio Central Control Unit (ACCU) audio signals to and from the docking ring, Spacelab intercom system, UHF transceiver, the payload bay, and to the SSRs via the NSP (see Table 15-1 and Table 15-2 for interface characteristics).

**Table 15-1. Audio interface characteristics**

| Interface            | Waveform | Signal level                                | Source impedance  | Load impedance   |
|----------------------|----------|---|---|--|
| ADS to NSP           | Analog   | 0 dbm $\pm$ 3 db at 1 kHz into 600 ohms     | Balanced  | 600 $\Omega$ $\pm$ 10% at 1 kHz, dc isolated, balanced |
| NSP to ADS           | Analog   | 0 dbm $\pm$ 3 db at 1 kHz into 600 ohms     | 600 $\Omega$ $\pm$ 10% at 1 kHz, dc isolated, balanced  | --   |
| ADS to               | Analog   | 0 dbm $\pm$ 3 db at 1 kHz into 600 ohms     | Balanced  | 600 $\Omega$ $\pm$ 10% at 1 kHz, DC isolated, balanced |
| IR AM, IR FM, to ADS | Analog   | 0 dcdBm $\pm$ 3 db at 1 kHz into 600 ohms   | 600 $\Omega$ $\pm$ 10% at 1 kHz, dc isolated, balanced  | --   |
| KEY*                 | DC       | --  | --  | --   |
| NAVAIDS to ADS       | Analog   | +17 dbm $\pm$ 3 db at 1350 Hz into 600 ohms | 40 $\Omega$ $\pm$ 10% at 1 kHz, dc grounded, unbalanced | --   |

**Table 15-1. Audio interface characteristics (concluded)**

|                                |        |                                     |          |   |
|--------------------------------|--------|-------------------------------------|----------|---|
| ADS to NSP, in relay mode only | Analog | 0 dbm ± 4 db at 1 kHz into 600 ohms | Balanced | 600 Ω ± 10% at 1 kHz, dc isolated, balanced |
|--------------------------------|--------|-------------------------------------|----------|---|

\*NOTE: key requires switch closure Insert SSOR characteristics for all EVA XCVR or change EVA XCVR to UHF and add SSOR  
XCVR source impedance 1 200 ohms  
XCVR open circuit voltage - 28 Vdc

**Table 15-2. Hardline interface characteristics**

| Interface  | Waveform  | Signal Level                     | Source impedance                            | Load impedance                              |
|--|---|----------------------------------|---|---|
| Docking ring, attached payload, launch umbilical, payload bay station to ADS | Analog  | 0 dbm ± 3 db at 1 KHz into 600 Ω | 600 Ω ± 10% at 1 KHz, DC isolated, balanced | --  |
| ADS to docking ring attached payload, launch umbilical payload bay station   | Analog  | 0 dbm ± 3 db at 1 KHz into 600 Ω | Balanced                                    | 600 Ω ± 10% at 1 KHz, dc isolated, balanced |
| Page key from docking ring, attached payload                                 | Switch closure at docking ring, attached payload<br>Switch closed impedance <100 ohms<br>Switch open impedance >100K ohms |                                  |   |   |

### 15.3 SYSTEM DESCRIPTION

The components of the ADS include the following:

- A. Two ACCUs (both ACCUs are housed in a single Line Replaceable Unit (LRU))
- B. Six Audio Terminal Units (ATUs)
- C. Crewman Communications Umbilicals (CCUs) for each crewmember
- D. Headset Interface Units (HIUs) for each crewmember
- E. Headsets for each crewmember
- F. Two Speaker Units (SUs)

As noted in item B above, the main difference between the orbiter ADSs is the number of ATUs. In order to accommodate the same number of CCUs and SMUs on all orbiters, some rearrangement has been done between these and the ATUs as depicted in Figure 15-1.

#### 15.3.1 Electrical

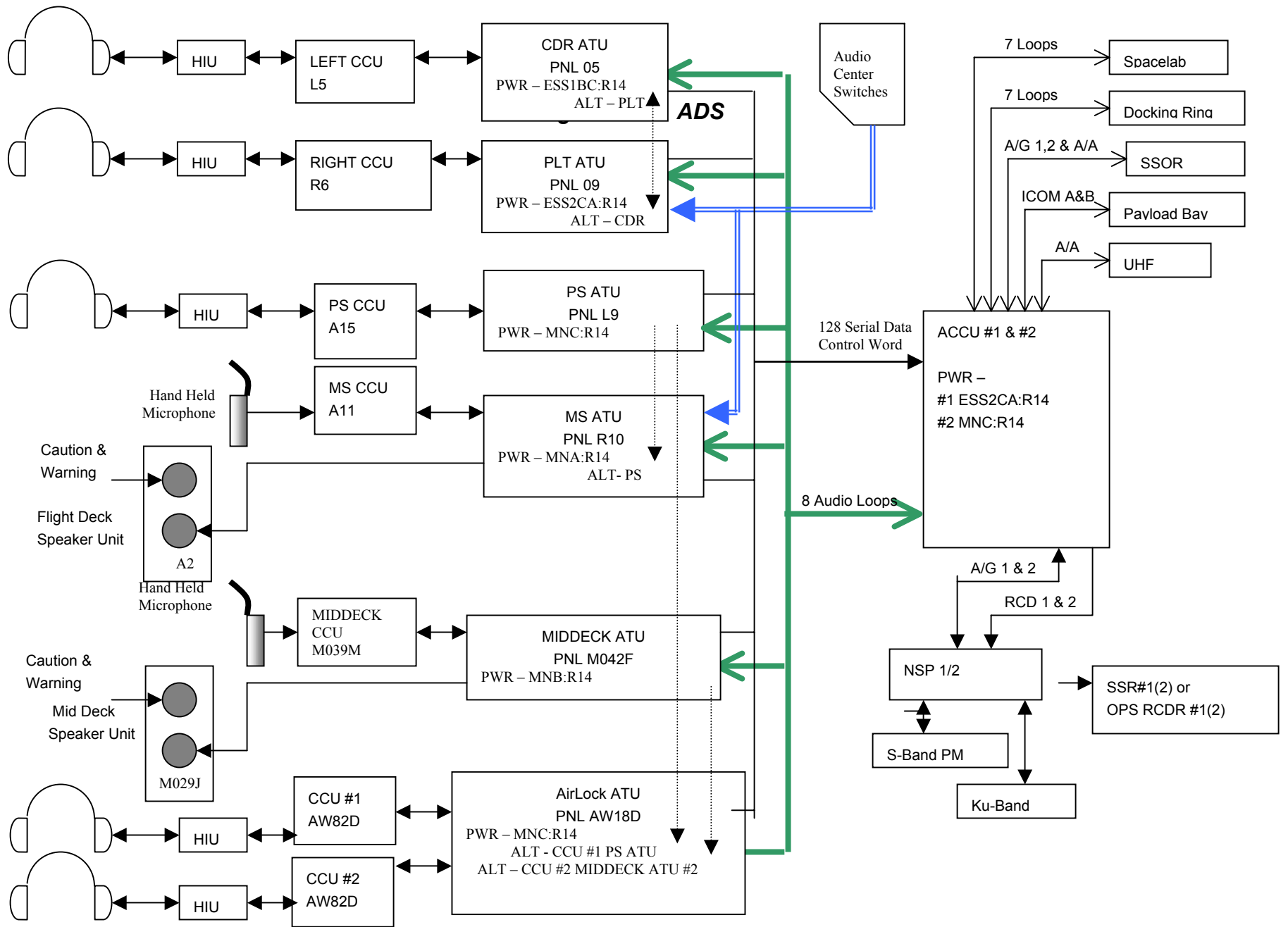
The electrical power sources and operating requirements for each component of the ADS are listed in Table 15-3. **Note:** the emphasis placed on the ACCUs and the ATUs

for the Pilot (PLT) and Commander (CDR) being powered by Essential Power; compared to the other ATUs being powered by only a single main DC power bus.

**Table 15-3. Electrical characteristics**

|             | Power source (bus) | Power consumption (watts) | Notes          |
|-------------|--------------------|---------------------------|----------------|
| ACCU-1      | ESS 2CA:R14        | 36.3                      |                |
| ACCU-2      | MNC:R14            | 36.3                      |                |
| ATU-CDR     | ESS1BC:R14         | 11.8                      | ATU mode       |
| ATU-PLT     | ESS2CA:R14         | 11.8                      | No sig - 4.3 W |
| ATU-MS      | MNA:R14            | 11.8                      |                |
| ATU-PS      | MNC:R14            | 11.8                      |                |
| ATU-MIDDECK | MNB:R14            | 11.8                      |                |
| ATU-AIRLOCK | MNC:R14            | 11.8                      |                |
| SU-FLT DECK | MNA:R14            | 14.9                      | SU mode        |
| SU-MIDDECK  | MNB:R14            | 14.9                      | No sig - 3.9 W |





### 15.3.2 Mechanical

The mechanical characteristics of the ADS components are given in Table 15-4. A more detailed description is shown by Figure 15-2 through Figure 15-5.

**Table 15-4. Mechanical characteristics**

| ADS component | Size (L by W by H) | Weight (lb) |
|---------------|--------------------|-------------|
| ACCU          | 5.0 x 19.0 x 17.0  | 24.0        |
| ATU           | 6.0 x 7.35 x 3.0   | 4.5         |
| SU            | 4.5 x 3.0 x 5.0    | 3.75        |
| HIU           | 2.5 x 1.56 x 5.25  | 1.25        |

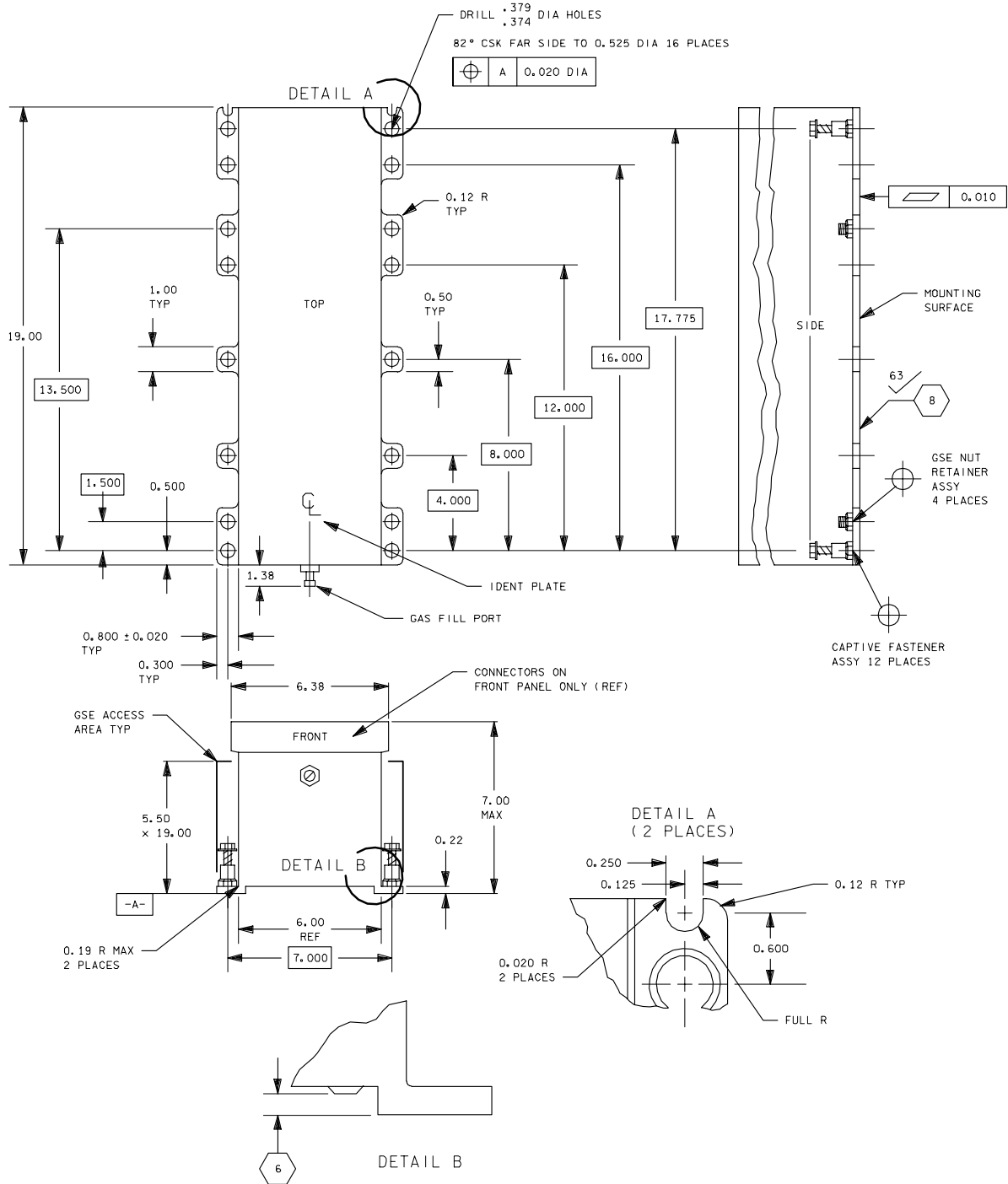
## 15.4 INSTALLATION

### 15.4.1 Location

The ACCU is located in middeck forward avionics bay 1. One of the two speaker units is located in the flight deck aft station, and the other is located in the middeck. The ATUs are distributed throughout the crew cabin.

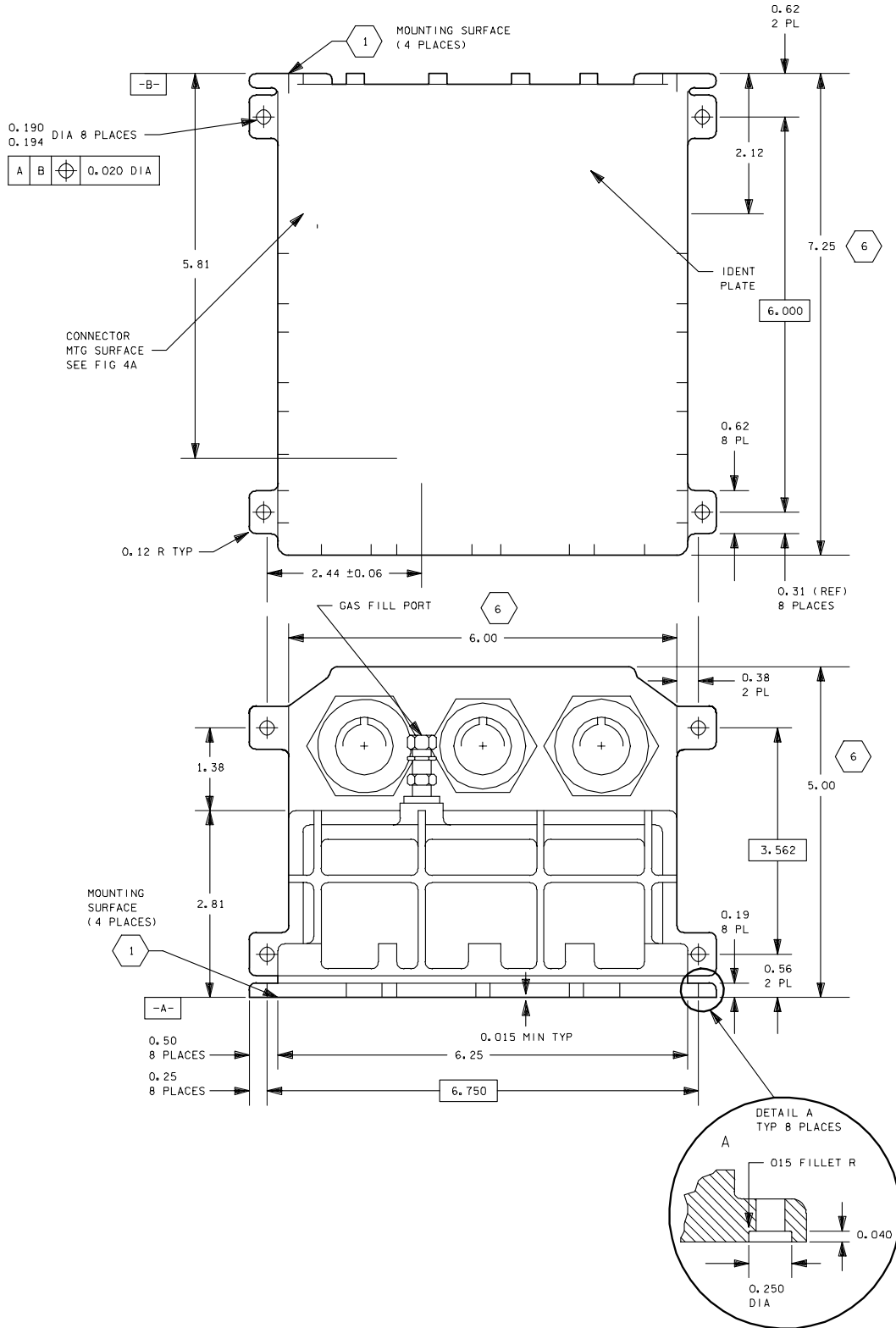
### 15.4.2 Cooling

The ADS is designed for passive cooling. The ACCU is water-loop cooled, while the rest of the ADS components are cooled by air convection.



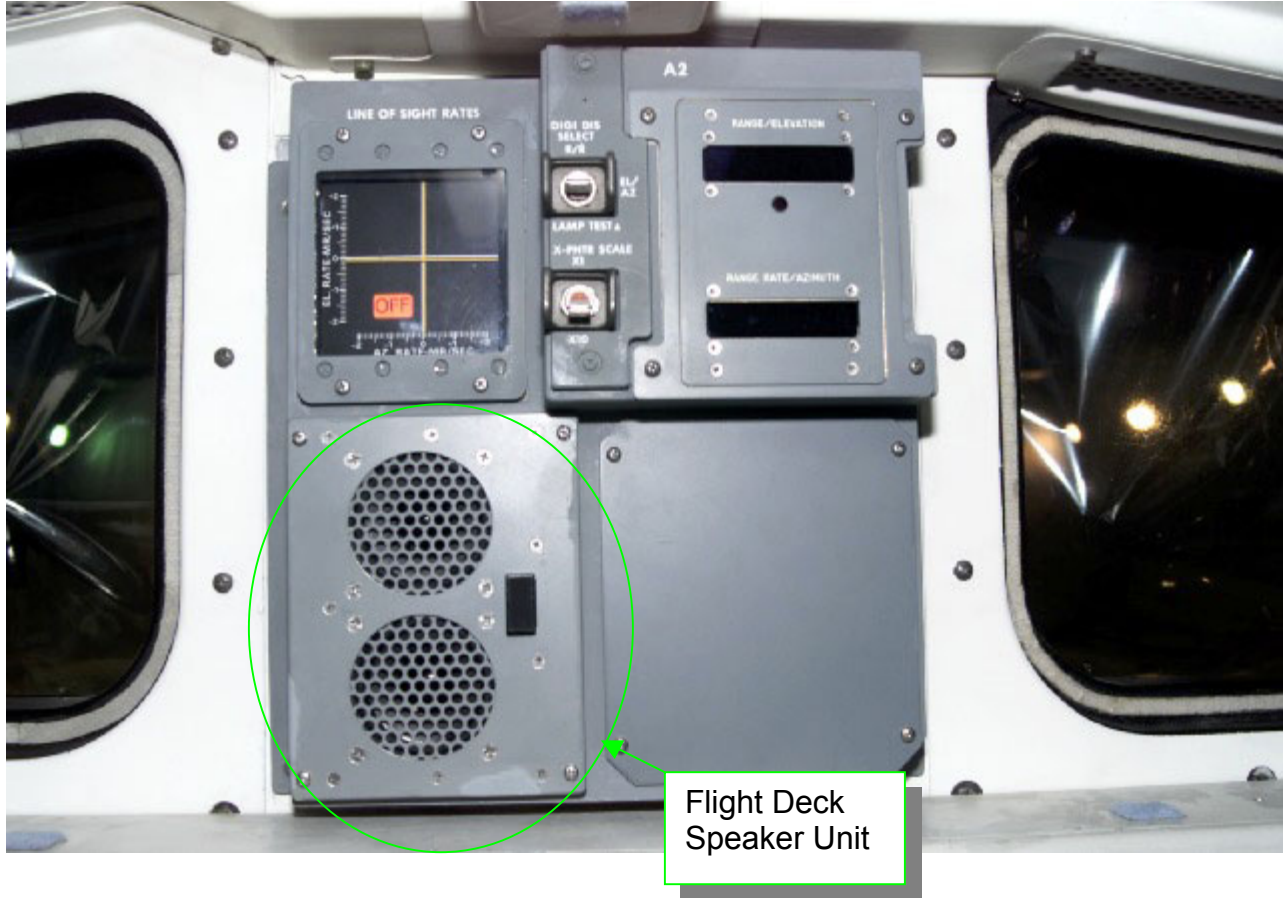
186111203.ART 1

Figure 15-2. ACCU LRU configuration

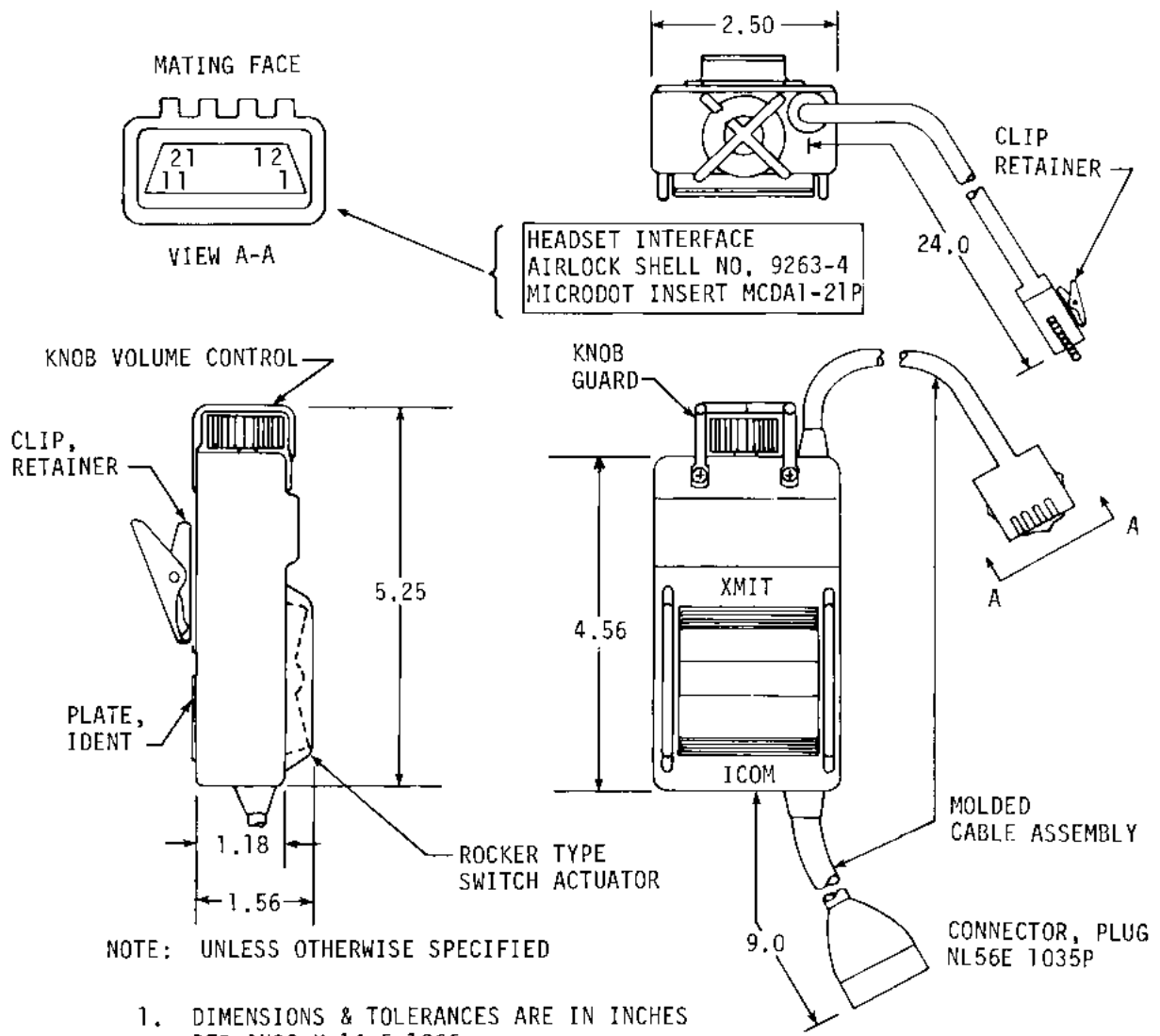


186111204. ART: 2

Figure 15-3. ATU LRU configuration



**Figure 15-4. Flight Deck SU LRU on Panel A2 and Panel A13**



NOTE: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS & TOLERANCES ARE IN INCHES PER ANSI Y 14.5-1966
2. TWO LENGTHS OF AUDIO CABLES .2 FT AND 4 FT, ARE PROVIDED FOR USE BETWEEN THE HIU AND THE CCU PANEL OUTLET, THE CABLES MAY BE CONNECTED IN SERIES FOR ADDITIONAL LENGTH.

**Figure 15-5. HIU configuration**

## 15.5 OPERATIONAL DESCRIPTION

Operation of the ADS is entirely under control of the crew.

### 15.5.1 Crew Controls

#### 15.5.1.1 ATU Panel

The ATUs (Figure 15-6) allow crewmembers to access the various voice loops over which to transmit and/or receive audio signals. Each ATU converts parallel switch input signals to serial data for input to the ACCU where the actual voice loop selection takes place.

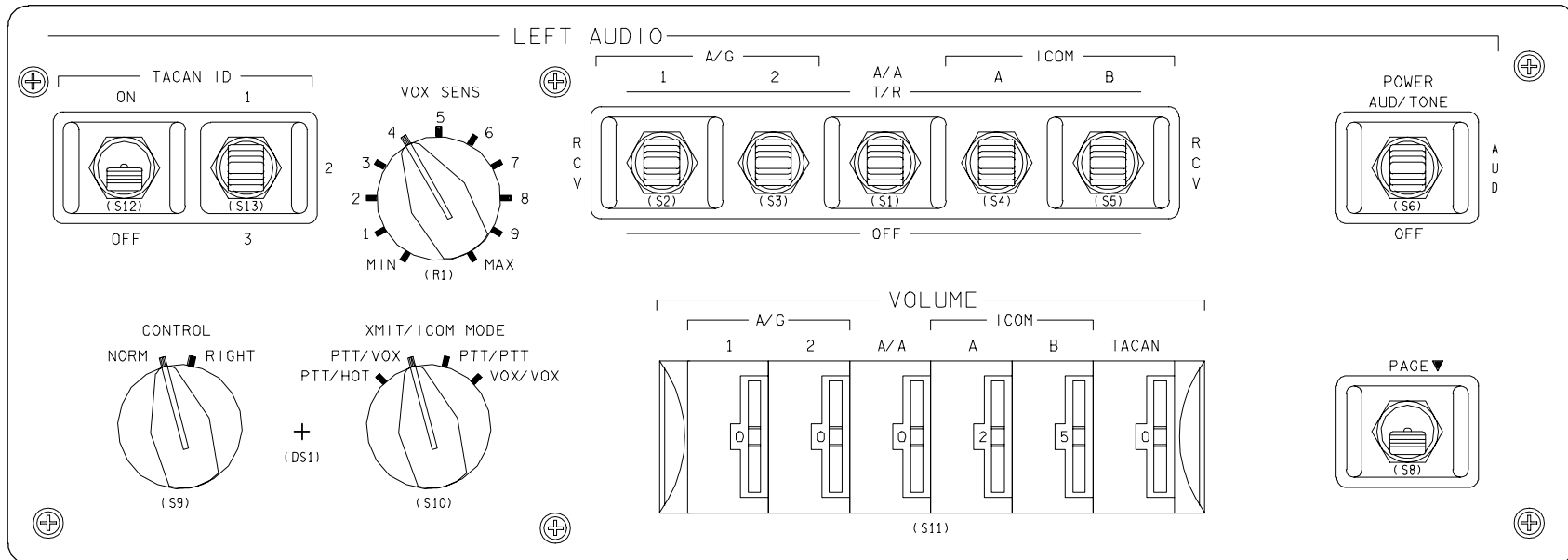
Communication between crewmembers takes place over the ICOM A and ICOM B loops. For voice transmission to and from mission control, Air-to-Ground (A/G) loops 1 and 2 have been provided. For UHF capability, an Air-to-Air (A/A) loop is available.

The ATUs also allow crewmembers to select volume settings for the voice signals as well as select the mode in which to transmit them. The XMIT/ICOM mode switch enables any one of four modes. In the PTT/HOT mode, external transmission is accomplished by Push-To-Talk (PTT) activation of the CDR's and PLT's Rotation Hand Controller (RHC), or any HIU (for the headset, the Transmit (XMIT) pushbutton must be keyed). Internal communications will be continuous or HOT.

In the PTT/VOX mode of operation, again external communications will be via the XMIT function or the PTT function of the RHC. ICOM signals are voice operated. The Voice Operated Transmission (VOX) mode works in conjunction with the VOX sensitivity control. This switch sets the threshold level of the VOX circuitry contained within the ATU. The higher the setting, the more sensitive the circuitry and the more easily it will be activated. When the voice level exceeds the threshold value, the VOX circuitry is tripped and audio transmission takes place. Maximum and minimum threshold levels are 0 db and -3 db, respectively. In the PTT/PTT mode, both external and ICOM communication is activated by XMIT keying of an HIU or the PTT function of an RHC. In the VOX/VOX mode, both external and ICOM comm is voice activated.

The paging switch makes available a fifth mode of operation. When continuously held, it enables voice transmission to all other crew stations, attached payload, and docking ring circuits.

The control switch is available to four ATUs: the PLT, CDR, Mission Specialist (MS), and the airlock station. This switch provides backup capability in the event of a failure or malfunction. In the normal position, all functions are under control of the ATU from which the functions were selected. In the alternate or backup position, the functions



186111207. ART: 1

Figure 15-6. ATU panel



are switched to the designated ATU, and any functions lost due to a failure or malfunction will be restored. However, if the malfunction results in the loss of power to the ATU, all voice transmissions from that ATU are permanently lost. Placing the control switch in the alternate position will restore listen capability only. All mic capability will be lost.

The control of the CDR's panel may be switched to the PLT's ATU (alternate position labeled "right") and the PLT's to the CDR's ATU (alternate position labeled "left"). The control of the MS's ATU may be switched to the payload specialist's ATU, and control of the airlock crew stations may be switched to the middeck ATUs.

The CDR's and PLT's ATUs have Tactical Air Navigation (TACAN) switches, which establish an interface with the TACAN system for Morse code transmissions and selection of the TACAN station to serve as the source of those transmissions.

When in the AUD/TONE position, the power switch allows a crewmember to transmit voice signals and receive both voice signals and Caution and Warning (C&W) tones. In the AUD position, all C&W signals are blocked.

#### 15.5.1.2 ACCU Panel Operation

The primary function of the ACCU is to identify, switch, and distribute signals to the various ADS components. The only crew control for the ACCU is located on panel C3 (Figure 15-7). Position 1 selects ACCU 1, and position 2 selects ACCU 2. It should be noted that when switching ACCUs, take the switch to the OFF position for about 1 sec, then to the desired ACCU; otherwise, latching of the power supplies may occur and neither ACCU will work.

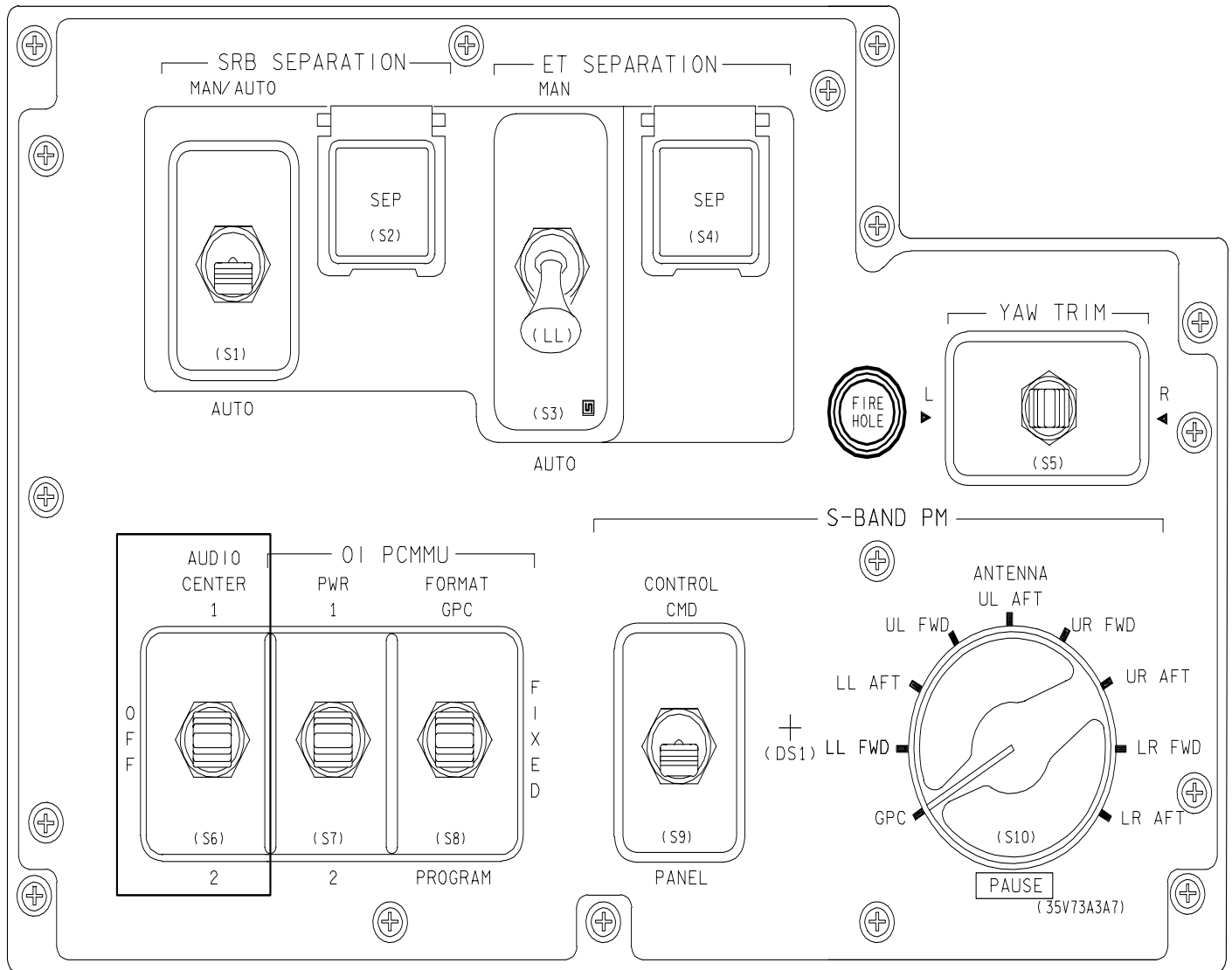
#### 15.5.1.3 Audio Center Panel

The audio center panel (Figure 15-9) provides configuration control data that enable signal routing to and from the docking ring, Spacelab intercom, the UHF transceiver or SSOR, payload bay outlets, and to the SSRs.

#### 15.5.1.4 Speaker Unit Operations

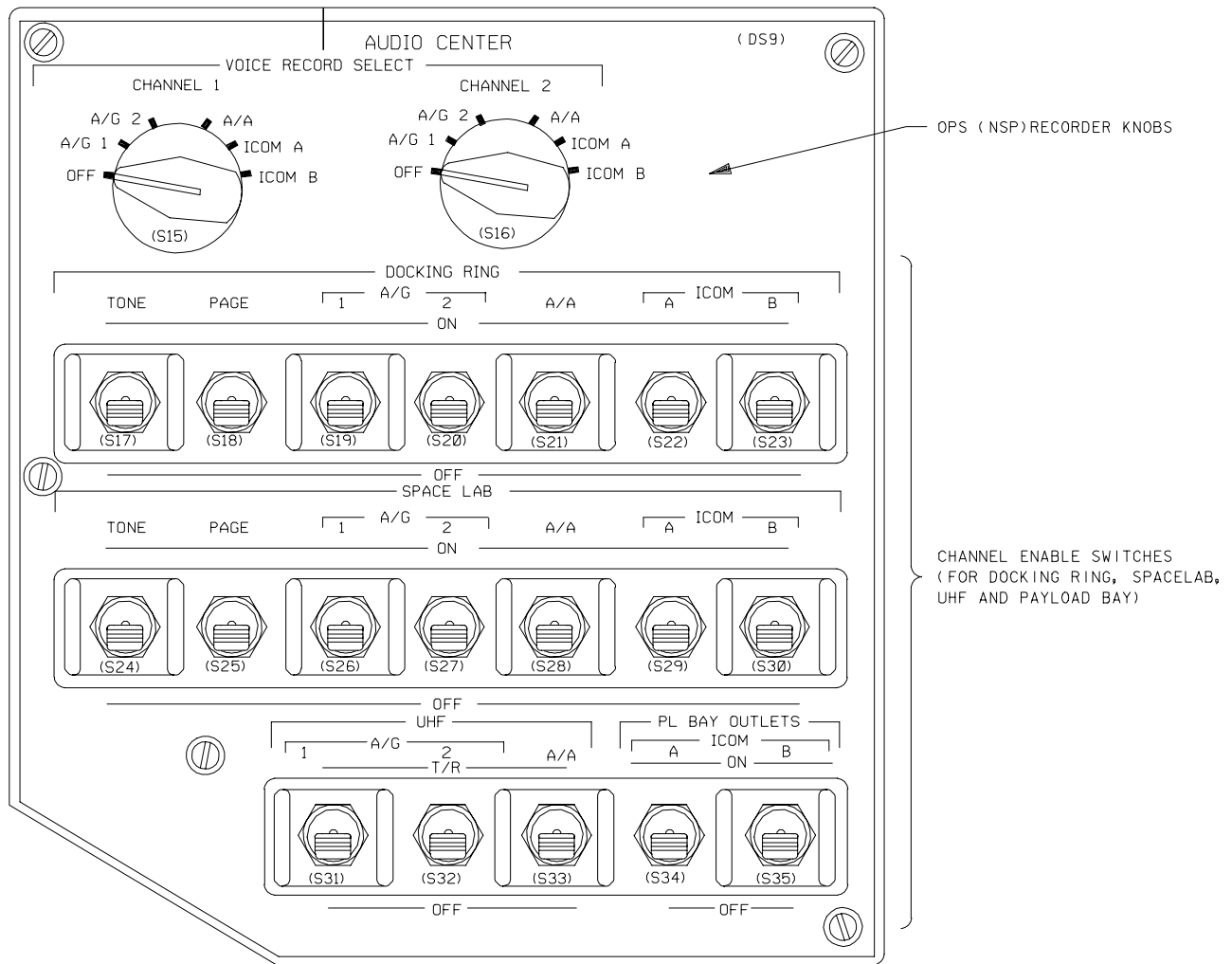
The MS ATU controls the power and received Audio Signals going to the Flight Deck Speaker Unit. The Middeck ATU control the Power and received Audio Signals of the Mid Deck speaker unit. See Figure 15-5.

The SU power switch is a three-position power switch labeled OFF, SPKR, and SPKR/MIC. In the OFF position, no signals go through the ATU. In the SPKR/MIC or SPKR position, **the unit can be used as a speaker only (i.e., MIC doesn't work).**



186111208. ART# 2

Figure 15-7. ACCU panel controls



186111209. ART 2

**Figure 15-8. Audio control panel controls**

## 15.6 SYSTEM OPERATION

### 15.6.1 ATU Subassembly

#### 15.6.1.1 Digital Subsystem

Six ATUs are included in the composition of the ADS. All audio routing is accomplished in the ACCU under control of switch selections from the ATUs. The ATU switching commands are transmitted to the ACCU in the form of serial links, one from each ATU. The serial data transmission is one way only, from ATU to ACCU, and no reverse digital data flow is required. The bit breakdown of the serial data word is shown in Figure 15-5. The station control signals to the ACCU from a given ATU include:

- Desired listen volume settings in digital format for each audio loop being routed to the ATU
- Audio talk/listen bus selections
- VOX and transmitter key signals

These control signals are unique to the individual ATU and represent the switch selections made by the crewmember at that particular station.

Every ATU sends the ACCU 128 Serial Data Word, as shown in Table 15-5, but it is important to note that some ATUs don't contain all relevant information to fill the 128 serial data word. Ex: the PLT and CDRs ATU will have relevant TACAN data in bits 57-63, the other 4 ATUs will contain null values within these particular bits.

In addition to the station control signals unique to each ATU, Audio Center Panel A1R switch Positions are sent to both the MS and PLT ATUs to "fill" the configuration control signals(bits 16-18; 64-69; 84-85; 96-102;112-118). This configuration data are routed to the two ATUs from the audio center panel and passed on to the ACCU, establishing an interface between the ADS and external comm systems. Again, the 4 other ATUs contain null information within these particular bits.

When on ACCU #1, the ACCU will process the MS ATU's configuration control signals out of the 128-bit serial data word. ACCU #2 will process the PLTs ATU respectfully.

Table 15-5. ATU/ACCU serial control data word

| Bit | Signal                        | Bit                               | Signal  | Bit          | Signal                       |
|-----|-------------------------------|-----------------------------------|---|--------------|------------------------------|
| 0   | FRAME SYNC                    | 44                                | A/G 1 VOLUME  | 88           | VOX                          |
| 1   |                               | 45                                |   | 89           |                              |
| 2   |                               | 46                                |   | 90           |                              |
| 3   |                               | 47                                |   | 91           |                              |
| 4   |                               | A/G 2 VOLUME                      | 48  | 92           |                              |
| 5   |                               |                                   | 49  | 93           |                              |
| 6   |                               |                                   | 50  | 94           |                              |
| 7   | 51                            | 52                                | A/A VOLUME  | 95           | AUDIO CENTER SPACELAB ON     |
| 8   | VOX                           | 53                                |   | 96           |                              |
| 9   | SPARES                        | 54                                |   | 97           |                              |
| 10  |                               | 55                                |   | 98           |                              |
| 11  |                               | 56                                | SPARE   | 99           |                              |
| 12  |                               | 57                                | NAV 1 TACAN   | 100          |                              |
| 13  |                               | 58                                | NAV 2 TONE  | 101          |                              |
| 14  |                               | 59                                | NAV 3 SELECT  | 102          |                              |
| 15  | 103                           | SPARE                             | 104   | VOX          |                              |
| 16  | A/G1 } AUDIO CENTER UHF (EVA) | 60                                | TACAN TONE VOLUME                                     |              | 105                          |
| 17  | A/G2 }                        | 61                                |   |              | 106                          |
| 18  | A/A }                         | 62                                |   |              | 107                          |
| 19  | SPARES                        | 63                                |   |              | 108                          |
| 20  |                               | 64                                | RECORD CHAV1 } AUDIO CENTER OPS RECORDER VOICE SELECT |              | 109                          |
| 21  | PAGE } UHF (EVA)              | 65                                |   | 67           | AUDIO CENTER DOCKING RING ON |
| 22  | SPARES                        | 66                                | 68  |              |                              |
| 23  |                               | 68                                | 112   |              |                              |
| 24  |                               | 69                                | 113   |              |                              |
| 25  | PTT/ICOM                      | 70                                | NSP 1 A/G 1   | 114          |                              |
| 26  | PTT/ A/G XMIT                 | 71                                |   | NSP 2 SELECT | 115                          |
| 27  | A/G VOXENA                    | 72                                | VOX   | 116          |                              |
| 28  | A/G C&W ENA                   | 73                                | NSP 1 A/G 2   | 117          |                              |
| 29  | A/G 2 ENA                     | 74                                |   | NSP 2 SELECT | 118                          |
| 30  | A/A ENA                       | 75                                | SPARES  | 119          |                              |
| 31  | PAGE ENA                      | 76                                |   | 120          |                              |
| 32  | ICOM A VOLUME                 | 77                                |   | 121          |                              |
| 33  |                               | 78                                |   | 122          |                              |
| 34  |                               | 79                                | 123   |              |                              |
| 35  | ICOM B VOLUME                 | 80                                | A/A IRFM UHF  | 124          |                              |
| 36  |                               | 81                                | SPARES  | DEAD TIME    |                              |
| 37  |                               | 82                                |   |              |                              |
| 38  |                               | 83                                |   |              |                              |
| 39  | 84                            | ICOM A } AUD CTR P/L BAY RECR ENA | 125   |              |                              |
| 40  | SPARE                         |                                   | 85  | 126          |                              |
| 41  | ICOM B ENA                    | 86                                | SPARES  | 127          |                              |
| 42  | ICOM A ENA                    | 87                                |   | 127          |                              |
| 43  | A/G 1 ENA                     |                                   |   |              |                              |

These configuration control signals perform switching and routing functions within the ACCU, such as

- Loop selections to interface with the UHF transceiver
- Routing of A/G 1 and A/G 2 loops to the NSP currently in use
- Audio from selected loops to recorders
- Which loops to the launch umbilical, Spacelab, payload bay, and docking ring are active

As stated earlier, panel A1R, configuration control information is encoded in a segment of the digital word from the MS and PLT ATUs. The MS digital word is the prime source of configuration control data when switch S6 on panel C3 (audio center switch) is in position 1, and the PLT data word is the primary source when S6 is in position 2.

If both systems controlling ATUs fail or are powered off, all routing functions within the ACCU will be lost. The ACCU will not maintain the last known configuration but will instead shut practically everything off.

However, communications can be recovered by cycling ACCU power or by switching ACCUs. When an ACCU is powered up with no system-controlling ATU present, it always comes up in a known configuration of practically everything operational (recorder select bits remain disabled).

#### **15.6.1.2 ATU Unique Characteristics**

The individual crew ATUs are listed below along with information unique to that ATU

CDR - Audio panel 05  
Headset outlet panel L5  
Additional audio interface with CDR helmet

PLT - Audio panel 09  
Headset outlet panel R6  
Additional audio interface with PLT helmet  
Provides configuration control data to ACCU #2

MS - Audio panel R10  
Headset outlet A11  
Also drives flight deck SU panel A2  
Provides configuration control data to ACCU #1

PS - Audio panel L9  
Headset outlet AI5

Middeck ATU - Audio panel M042F  
Headset outlet M039M

Drives middeck SU and CCU  
Airlock ATU - Audio panel AW18D  
Drives two headset outlets and two Extravehicular  
Mobility Unit (EMU) outlets on panel AW82D

## 15.6.2 ACCU Subassembly

### 15.6.2.1 Circuit Protection and Redundancy

Circuit protection for the audio system is provided for by means of redundancy. There are six sets of printed circuit boards within the ACCU, one for each associated ATU. Primary/secondary power input into each circuit board is isolated by local power regulators. The partitioning of the circuits on separate power supplies isolates them in the event of a failure.

The local power regulators have built-in overload protection that prevents a load fault from drawing an excessive amount of current from the main power supply. So, in the case of a main power supply failure or a fault in the load, the system would be recoverable. In the event that a fault occurs in the power regulator itself, the main power supply is protected by a fuse which, when blown, decouples the regulator from the main power input.

### 15.6.2.2 Digital Subsystem

The ACCU receives six asynchronous serial data inputs over separate dedicated mux links routed from each ATU and converts the serial data to a parallel format used in controlling the audio subsystem. The 128-bit serial data Manchester encoded data word (125 bits serial data, 3 bits of dead time) is decoded in the ACCU into frame sync, clock, and data. The 125-bit storage register is used to store the previous frame of data, which enables a bit-by-bit comparison of the previous and present data. It also provides an output which serves as input to the 40-bit station control register. When both frames of data have compared identically, the frame sync pulse is used to generate a strobe that transfers the data at the input gates to the output latches.

The 16-bit counter serves as a timing circuit that provides the necessary information needed to strip out the high speed VOX bits from the serial data word. The 16-bit counter comprises two 8-bit counters with separate clock pulses. The clock pulse from the first component occurs at the bit times which correspond to the occurrence of the VOX bits within the serial data word. The second clock pulse strobes the VOX bits into the VOX detect circuitry. If two identical VOX bits are detected, validity is assured and the VOX bits are combined with the VOX mode bit and the PTT bits to enable the various XMIT and ICOM analog talk switches.

While all ATUs transmit serial data to the ACCU containing station control information, it is the MS and PLT ATUs that transmit both station control and configuration control data. Station control data are information within the serial data word that controls audio signal routing, channel volume levels, etc., for a particular ATU or audio station. Configuration control data are information which is transmitted from the audio center

panel to the ACCU via the MS and PLT ATUs that control or establish interfaces between the orbiter audio system and external comm systems, such as the Spacelab audio system or the network signal processors.

When operating in the normal mode, primary power is applied to the ACCU and all configuration comes from the primary configuration registers. When operating in the secondary mode, configuration comes from the redundant configuration registers. Control of both sets of registers may be achieved by either ATU. To accomplish control by either ATU, each ATU input is assigned two Manchester Decoders (MDs), one that is located on the configuration control card and another that is located on the station control card.

Selection of the proper decoder is based on mode of operation and the status of the operating circuitry. When the ACCU is operating in the primary mode, data input to the distribution logic is from the PRIMARY CONFIGURATION control card and the MS ATU. The input selector looks for a frame sync pulse every 5 ms. If the MS serial data word is present, frame sync is detected as good, and data transfer from the MD on the primary configuration control card is enabled. If a failure occurs in the MS ATU or in the decoder, a loss of frame sync will be detected and the input selector will switch the select gate to the MD located on the PLT's STATION control card, enabling the partially decoded mux data from the PLT's ATU to hold the primary configuration. This form of switching is nonlatching, such that if the RAW MUX 3 data link becomes operable again, control will revert back to the MD located on the primary configuration card.

In the secondary mode of operation, the serial data word from the PLT ATU will have control over the secondary configuration control register. If a failure occurs, control will be switched to the MD located on the MS's STATION control card, and input to the REDUNDANT CONFIGURATION control distribution logic will be from the MS serial data word.

Nominally, when operating in the primary mode, the MS serial data word provides information to the distribution logic. If a failure occurs, the primary configuration is held by the PLT ATU. In the secondary mode of operation, configuration data are provided by the PLT ATU as long as no anomalous conditions occur in which the data input to the distribution logic will be derived from the MS serial data word. (See Figure 15-9.)

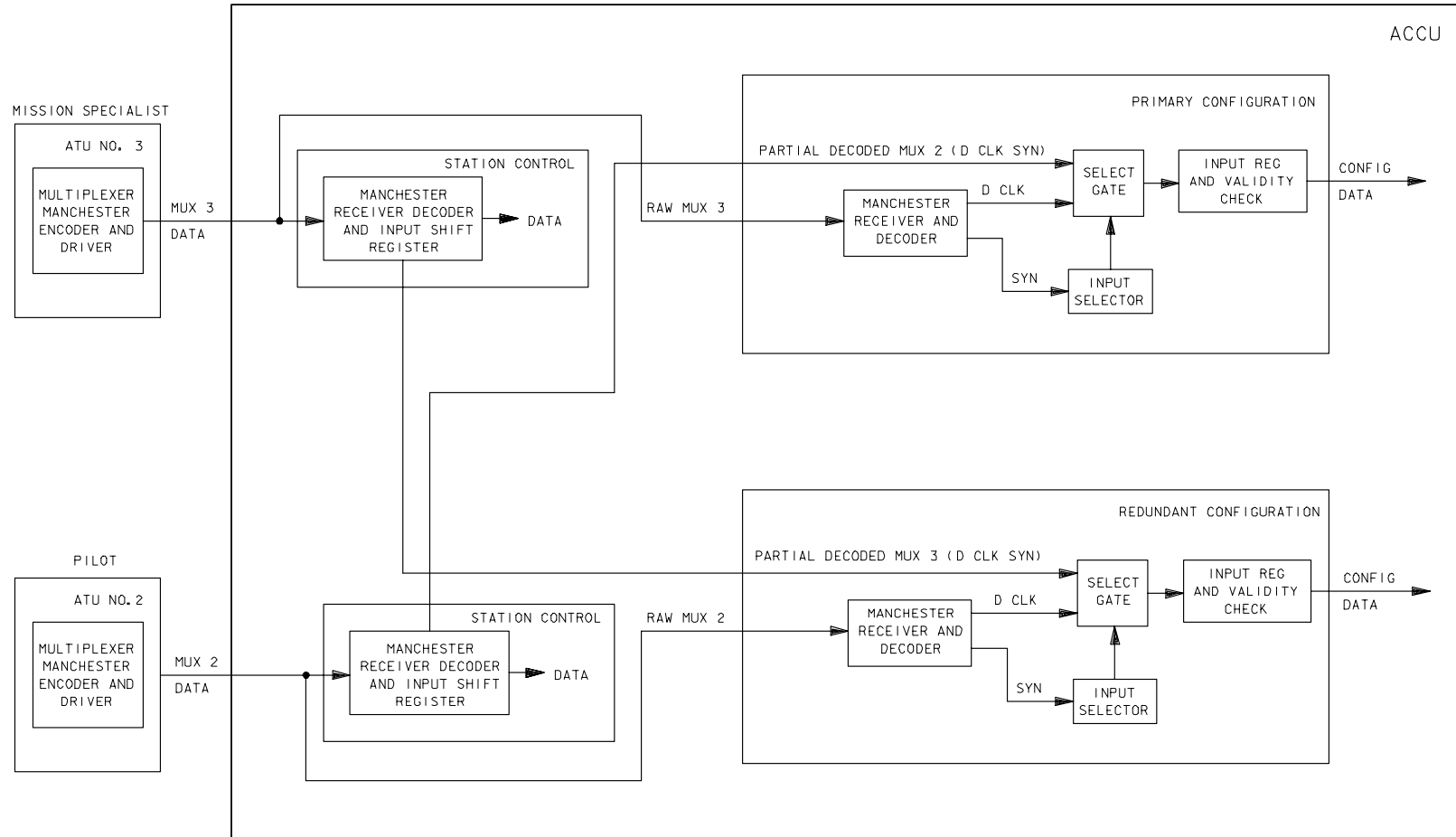
### 15.6.2.3 Audio Signals

Microphone audio signals are coupled into the ACCU through a dedicated input transformer and buffering amplifier. The voice signals are passed to the solid-state talk switches and onto the designated buses via a summing network. The summing network is capable of handling inputs from any or all of the ATUs, the UHF transceiver, Spacelab, docking ring, launch umbilical, and payload bay. The composite of these signals, along with C&W tones, comprise the listen audio which is routed to those stations configured to receive it. In the case of the audio station where the microphone signal originated, the out-of-phase voice signal from the inverting amplifier cancels out the talk input from the relay switches preventing feedback conditions. The voice signal will be present on the designated buses but will not be returned to the speaker's ATU.



However, the speaker will be able to hear his or her own voice through a sidetone injection at the ATU.

This concept also applies to the other circuits within the ACCU. For example, to prevent input to the UHF audio circuits from being routed back to the UHF transmitter, the incoming signal is routed to the bus circuits where it is inverted, passed to the switching circuits and out to the individual crew stations, and then back to the UHF audio circuit via either one of the air-to-ground buses or the air-to-air bus. The out-of-phase signal from the bus is combined with the signal from the UHF receiver, and the two signals cancel. It is by this design that feedback is prevented.

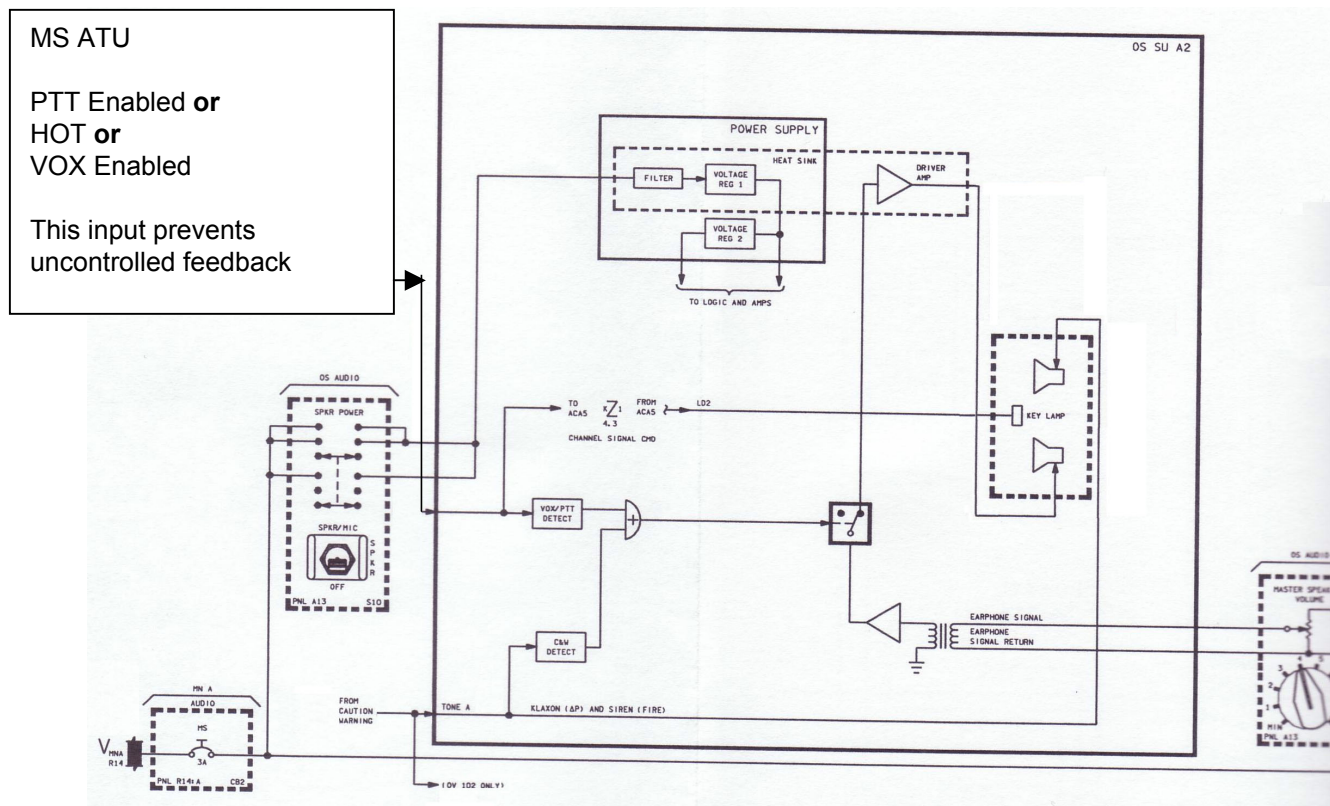


186111211. ART# 2

Figure 15-9. Configuration control diagram

### 15.6.3 Speaker Unit

#### 15.6.3.1 Control Logic



**Figure 15-10. Flight Deck Speaker Control Logic**

## 15.7 SUMMARY DATA

If one of the systems controlling ATUs fails (MS, PLT), primary configuration control data will be supplied to the ACCU from the remaining one. If both the MS and PLT ATUs fail, cycling power on the ACCU will cause the ACCU to be powered up in a default mode of practically everything ON.

If a mic is keyed and there is no voice signal present, the AGC increases gain until the background noise is at an irritable level. This condition is usually noticed when in the HOT or VOX mode of operation.

If an ATU fails, switching to the backup mode usually regains comm capability. If the failure is one that will cause the breaker to blow, switching to the backup mode will only regain listen capability. To restore mic capability, try turning off the failed ATU and resetting the breaker.

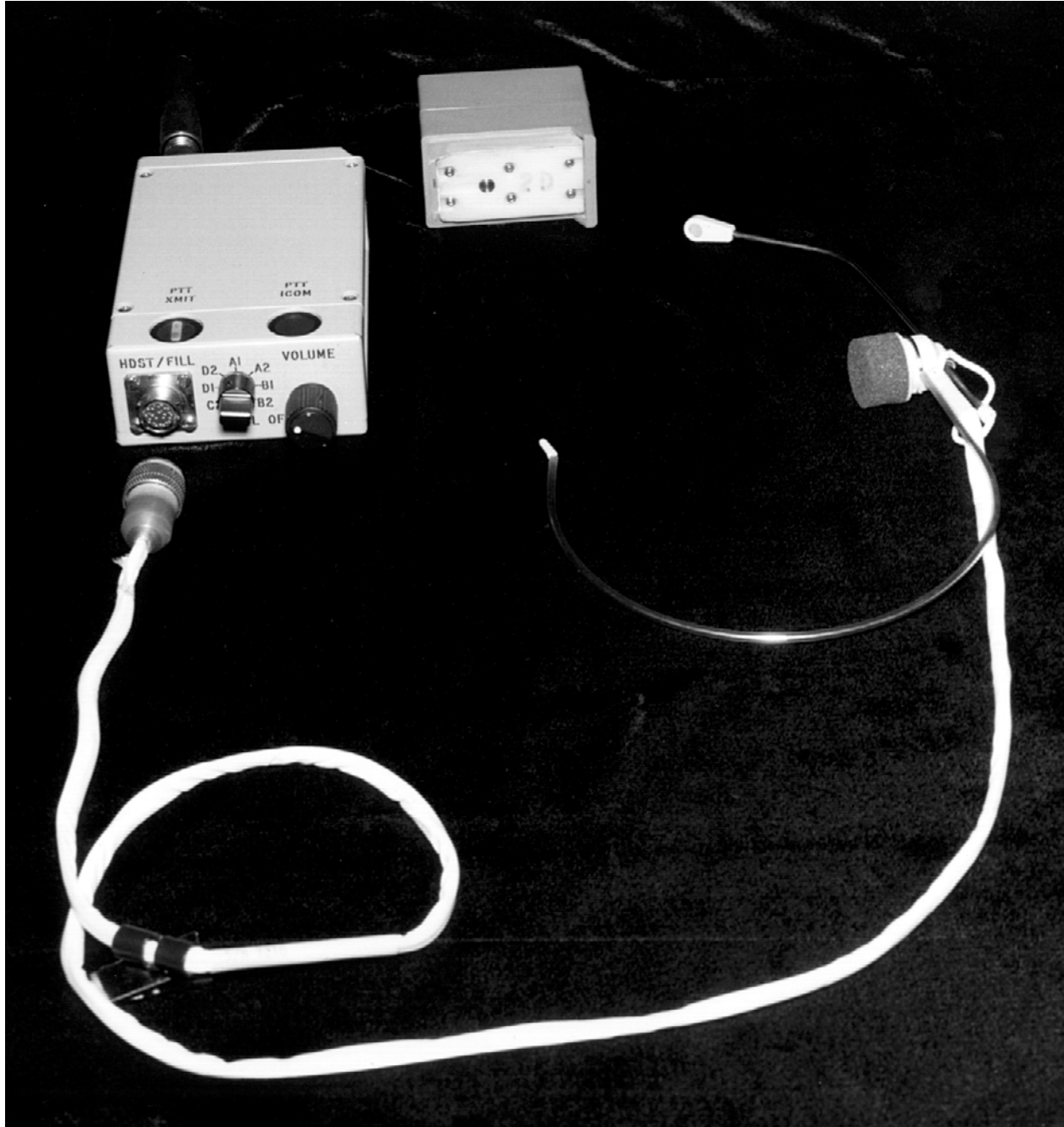
Switching ACCUs too fast can cause both to latch, leaving them in an unpowered state. To avoid this, one should always take the power switch from the initial position to the OFF position for about 1 second, and then to the desired position.

Operation of two SUs simultaneously is virtually impossible. Operation of the SU in conjunction with the Handheld Mics (HHMs) is usually the route to go. It is highly recommended that the HHMs be connected to the same ATU that control the SU. This will ensure proper operation of both pieces of equipment. Otherwise, audio squeals will be generated whenever the HHMs are keyed, due to feedback conditions.

The following pieces of equipment are shown in Figure 15-11 through Figure 15-17: Multiple Headset Unit (MHA), Crew Remote Unit (CRU), Audio Interface Unit (AIU), HHM, Launch and Entry Helmet (LEH), Very Lightweight Headset (VLWH), and HIU.



*Figure 15-11. Multiple headset adapter*

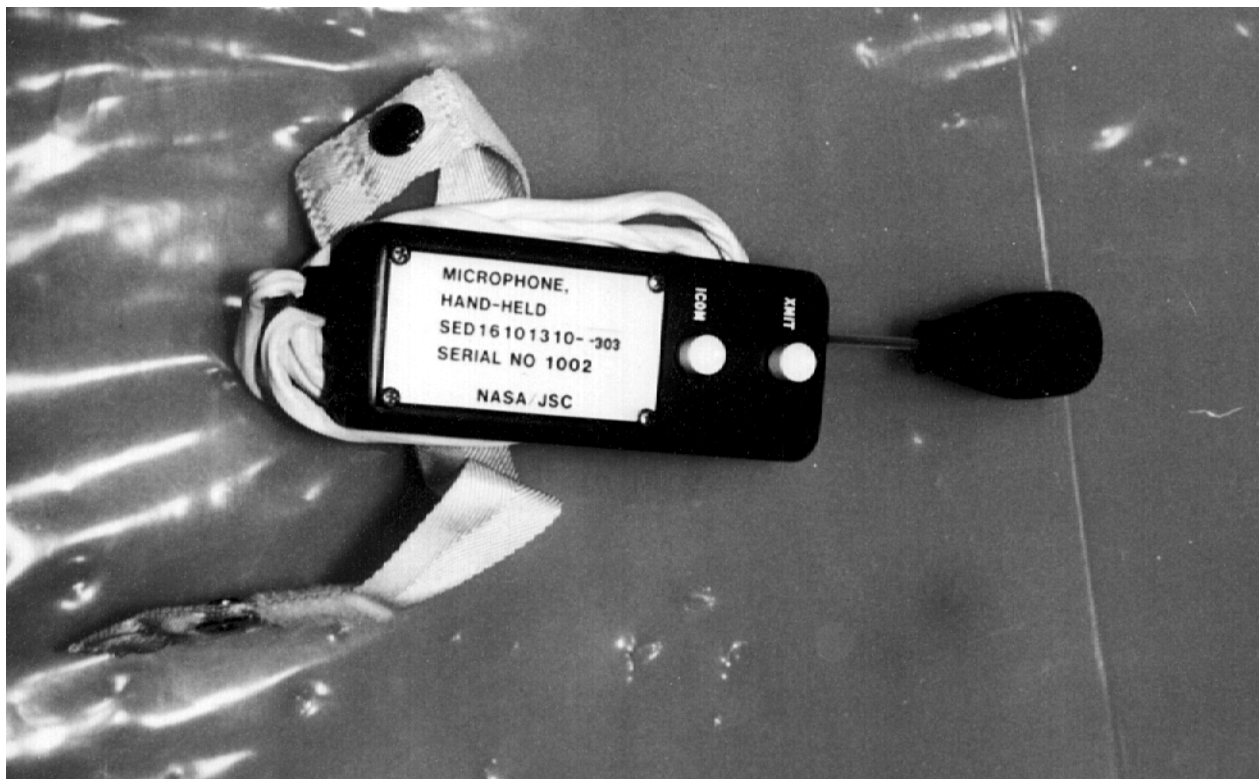


*Figure 15-12. Crew remote unit*





*Figure 15-13. Audio interface unit*

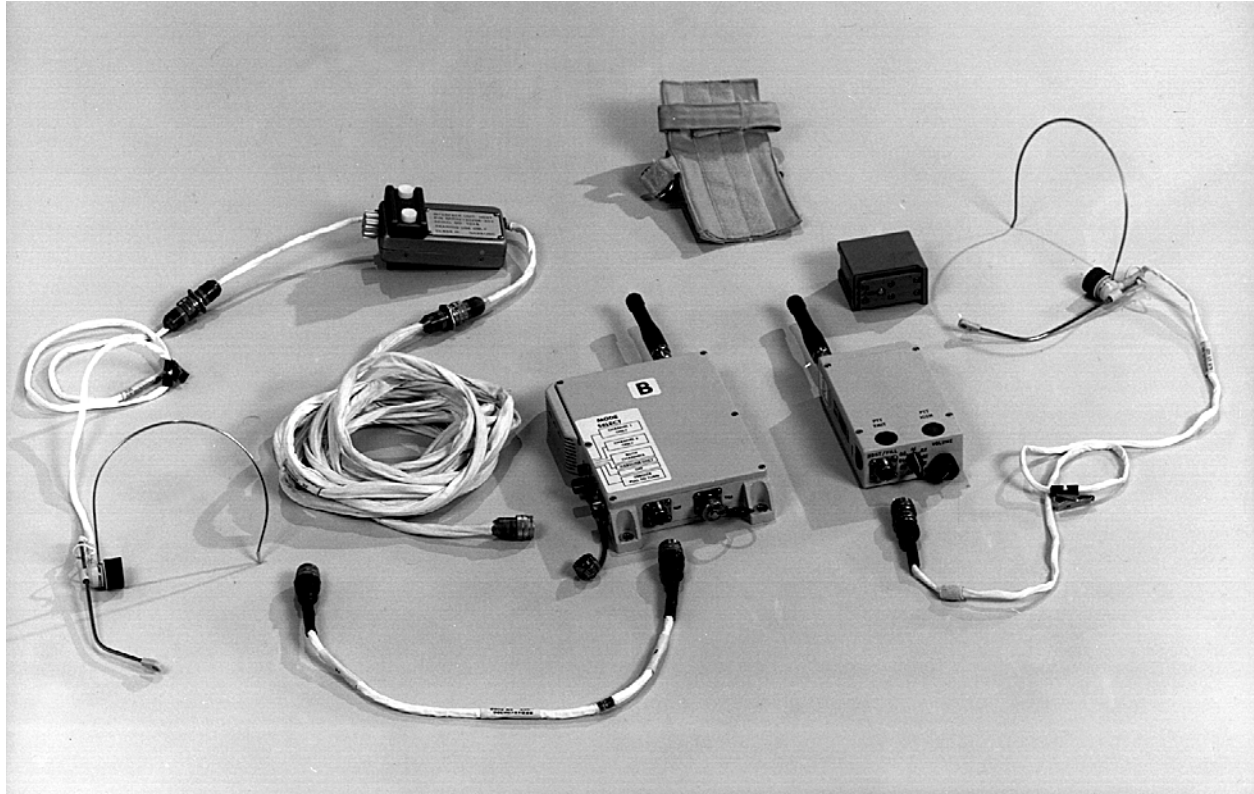


*Figure 15-14. Handheld mic*

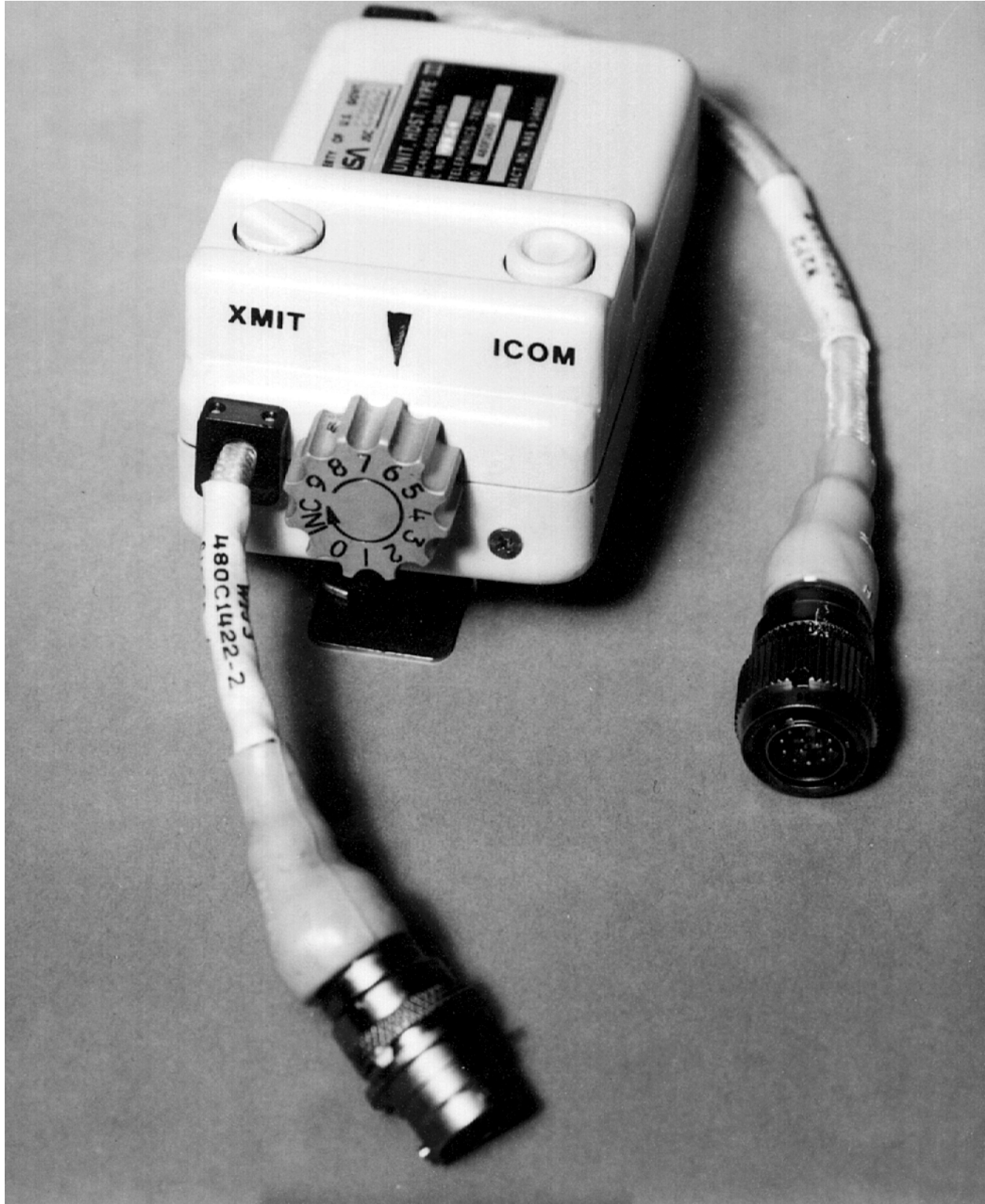


*Figure 15-15. Launch and entry helmet*





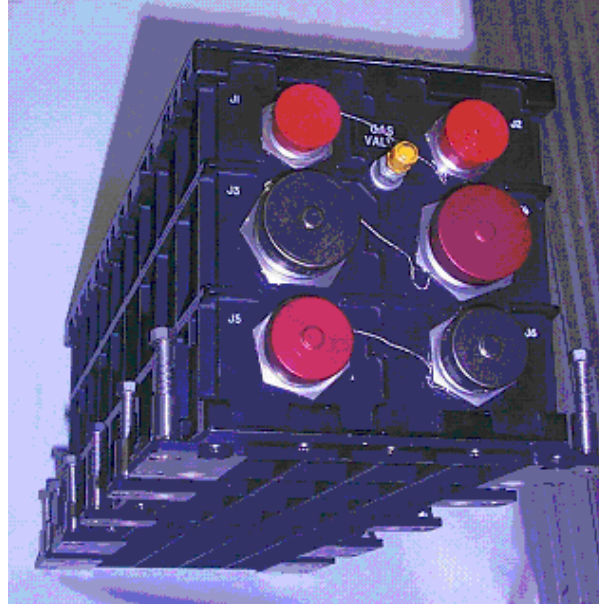
*Figure 15-16. Very lightweight headset*



*Figure 15-17. Headset interface unit*

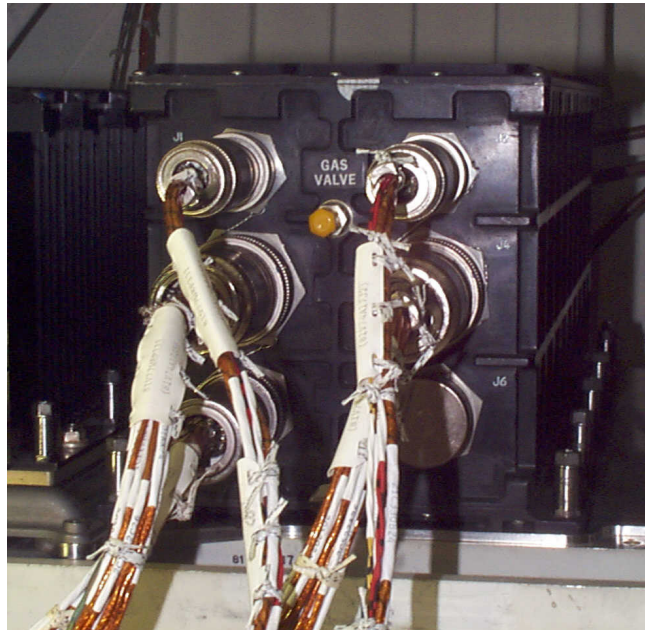
### 15.8 THE ACCU J3 AND J4 BYPASS

The ACCU resides in AV BAY 1 and is wired to the Orbiter via six Jack Plug connections shown in Figure 15-18.



**Figure 15-18. ACCU Hardware**

Inside AV BAY 1, the ACCU appears wired as shown in Figure 15-19 (notice the J6 plug is not wired).



**Figure 15-19. ACCU Hardware J Plugs Wiring**



As stated earlier within this System Brief, there is only one hardware ACCU with redundant cards powered from either ESS 2CA (ACCU #1) or Main C:R14 (ACCU#2).

Each of the Plugs connected to the ACCU provides a specific signal/power to the ACCU. The specific Jack Plug Layout for the ACCU Wire connections are as follows:

**Table 15-6. ACCU J Plug Configuration**

|    | <b>Pin Hi</b> | <b>Pin Lo</b> | <b>INCO Common Nomenclature</b>                             |
|----|---------------|---------------|---|
| J1 | V             | A             | Power comes from ESS 2CA                                    |
| J1 | B             | P             | MS ATU 128 bit Serial Data Word (& Panel A1 Config) to ACCU |
| J1 | F             | S             | Mid Deck ATU 128 bit Serial Data Word to ACCU               |
| J1 | K             | L             | Docking Ring Page Key input                                 |
| J1 | M             | N             | CDRs ATU 128 bit Serial Data Word                           |

|    | <b>Pin Hi</b> | <b>Pin Lo</b> | <b>INCO Common Nomenclature</b>                                |
|----|---------------|---------------|--|
| J2 | V             | A             | Power comes from Main C: R14                                   |
| J2 | B             | P             | Payload Station ATU 128 bit Serial Data Word to ACCU           |
| J2 | D             | C             | Payload Station Distribution Panel Page Key input              |
| J2 | H             | J             | Airlock ATU 128 bit Serial Data Word                           |
| J2 | K             | L             | Used for IRFM to the UHF System                                |
| J2 | M             | N             | PLT's ATU 128 bit Serial Data Word (& Panel A1 Config) to ACCU |

|    | <b>Pin Hi</b> | <b>Pin Lo</b> | <b>INCO Common Nomenclature</b>  |
|----|---------------|---------------|--|
| J3 | A             | W             | CDRs ATU Voice going to ACCU   |
| J3 | B             | X             | MS ATUs Voice going to ACCU  |
| J3 | C             | Y             | Mid Deck ATU Voice going to ACCU   |
| J3 | E             | -A            | NSP #1 A/G1 AUDIO to ACCU  |
| J3 | F             | -B            | NSP #2 A/G2 AUDIO to ACCU  |
| J3 | H             | -D            | TACAN #2 ID TONE sends a command V74K0195E to the ACCU                   |
| J3 | J             | -E            | Payload Bay Voice on ICOM A to ACCU (Used for KSC Testing)               |
| J3 | K             | -F            | ACCU Listen Audio Signal going to CDRs ATU                               |
| J3 | L             | -G            | ACCU Listen Audio Signal going to MS ATU and Flight Deck SU              |
| J3 | M             | -H            | ACCU Listen Audio Signal going to Mid Deck ATU and Mid Deck Speaker Unit |
| J3 | P             | -J            | ACCU to NSP #1 A/G1 Audio Input  |
| J3 | R             | -K            | ACCU to NSP #2 A/G2 Audio Input  |
| J3 | T             | -N            | AUDIO voice going to SSOR  |
| J3 | U             | V             | Payload Bay Voice on ICOM A from ACCU (Used for KSC Testing)             |
| J3 | -P            | GG            | ICOM A Audio Signals from ACCU to T-0 GSE (Used for lift off)            |
| J3 | -Q            | CC            | TACAN #1 ID TONE sends a command V74K0194E to the ACCU                   |
| J3 | -R            | -S            | SSOR Audio going ACCU  |
| J3 | -W            | EE            | AUDIO RCD CH 2 to NSP #2   |
| J3 | -X            | FF            | AUDIO RCD CH 1 To NSP #1   |
| J3 | AA            | BB            | ICOM A Audio Signals from T-0 GSE (Used for lift off) to ACCU            |
| J3 | HH            | DD            | C&W TONE A Inputs to ACCU  |

**Table 15-6. ACCU J Plug Configuration (concluded)**

|    | Pin Hi | Pin Lo | INCO Common Nomenclature   |
|----|--------|--------|--|
| J4 | A      | W      | Pilot's ATU Voice going to ACCU  |
| J4 | B      | X      | Payload Station ATU going to ACCU  |
| J4 | D      | Z      | Airlock ATU going to ACCU  |
| J4 | E      | -A     | NSP #1 A/G2 Audio Output to ACCU   |
| J4 | F      | -B     | NSP #2 A/G1 Audio Output to ACCU   |
| J4 | H      | -D     | TACAN #3 ID TONE sends a command V74K0196E to the ACCU                   |
| J4 | J      | -E     | ICOM B Audio Signals from the Payload Bay to ACCU (Used for KSC Testing) |
| J4 | K      | -F     | ACCU Voice Analog Signal going to Pilot's ATU                            |
| J4 | L      | -G     | ACCU Voice Analog Signal going to Payload Station's ATU                  |
| J4 | N      | -I     | ACCU Voice Analog Signal going to Airlock's ATU                          |
| J4 | P      | -J     | NSP #1 A/G2 AUDIO IN from ACCU   |
| J4 | R      | -K     | NSP #2 A/G1 AUDIO IN from ACCU   |
| J4 | T      | -N     | ACCU Audio Out to the UHF  |
| J4 | -P     | BB     | C&W TONE B Inputs to ACCU  |
| J4 | -R     | -S     | UHF Audio going to ACCU  |
| J4 | -T     | -U     | ICOM B Audio Signals from ACCU to T-0 GSE (Used for lift off)            |
| J4 | -W     | -X     | ICOM B Audio Signals from T-0 GSE (Used for lift off) to ACCU            |
| J4 | -Z     | -Y     | AUDIO RCD CH 2 going to NSP 1  |
| J4 | FF     | EE     | ICOM B Audio Signals from ACCU to Payload Bay (Used for KSC Testing)     |
| J4 | AA     | GG     | AUDIO RCD CH 1 going to NSP 2  |

|    | Pin Hi | Pin Lo | INCO Common Nomenclature         |
|----|--------|--------|----------------------------------|
| J5 | A      | B      | PSDP to ACCU A/G 1               |
| J5 | C      | D      | PSDP to ACCU A/G 2               |
| J5 | E      | F      | PSDP to ACCU A/A                 |
| J5 | G      | H      | PSDP to ACCU ICOM A              |
| J5 | K      | L      | ACCU to PSDP A/G 1               |
| J5 | M      | N      | ACCU to PSDP A/G 2               |
| J5 | P      | R      | ACCU to PSDP A/A                 |
| J5 | S      | -E     | C&W Output Signals going to PSDP |
| J5 | V      | W      | PSDP to ACCU ICOM B              |
| J5 | X      | Y      | PSDP to ACCU PAGE Audio Signals  |
| J5 | -A     | -B     | ACCU to PSDP ICOM A              |
| J5 | -C     | -D     | ACCU to PSDP ICOM B              |
| J5 | -H     | -J     | ACCU to PSDP PAGE Audio Signals  |

**J6 - This Jack Plug is used solely for the Docking Ring (this cable is not installed)**

### 15.8.1 The ACCU Bypass

INCO developed a set of procedures which could be used in case of an internal ACCU fire, causing loss of both sets of redundant ACCU Cards. INCO developed an In-Flight

Maintenance Procedure (IFM) called the ACCU Bypass which uses turnaround plugs on the J3 and J4 jacks to disconnect the ACCU from the A/G1 audio circuit.

### 15.8.1.1 J3 Bypass

The INCO who was assigned to this procedure, noticed that the J3 plug wiring contained all four wires to support the NSP #1 A/G1 Talk and Listen circuits to the CDR's ATU. In theory, if the ACCU had an Internal Fault, the crew members would just need to disconnect the J3 plug from the ACCU and install a "turnaround plug" which connected NSP #1 A/G1 directly into the CDR's ATU.

|    | Pin Hi | Pin Lo | INCO Common Nomenclature  |
|----|--------|--------|---|
| J3 | A      | W      | CDRs ATU Voice going to ACCU  |
| J3 | B      | X      | MS ATUs Voice going to ACCU   |
| J3 | C      | Y      | Mid Deck ATU Voice going to ACCU  |
| J3 | E      | -A     | NSP #1 A/G1 AUDIO to ACCU   |
| J3 | F      | -B     | NSP #2 A/G2 AUDIO to ACCU   |
| J3 | H      | -D     | TACAN #2 ID TONE sends a command V74K0195E to the ACCU                                    |
| J3 | J      | -E     | Payload Bay Voice on ICOM A to ACCU (Used for KSC Testing)                                |
| J3 | K      | -F     | ACCU Listen Audio Signal going to CDRs ATU  |
| J3 | L      | -G     | ACCU Listen Audio Signal going to MS ATU and Flight Deck SU                               |
| J3 | M      | -H     | ACCU Listen Audio Signal going to Mid Deck ATU and Mid Deck Speaker Unit                  |
| J3 | P      | -J     | ACCU to NSP #1 A/G1 Audio Input   |
| J3 | R      | -K     | ACCU to NSP #2 A/G2 Audio Input   |
| J3 | T      | -N     | AUDIO voice going to SSOR<br>Payload Bay Voice on ICOM A from ACCU (Used for KSC Testing) |
| J3 | U      | V      |   |
| J3 | -P     | GG     | ICOM A Audio Signals from ACCU to T-0 GSE (Used for lift off)                             |
| J3 | -Q     | CC     | TACAN #1 ID TONE sends a command V74K0194E to the ACCU                                    |
| J3 | -R     | -S     | SSOR Audio going ACCU   |
| J3 | -W     | EE     | AUDIO RCD CH 2 to NSP #2  |
| J3 | -X     | FF     | AUDIO RCD CH 1 to NSP #1  |
| J3 | AA     | BB     | ICOM A Audio Signals from T-0 GSE (Used for lift off) to ACCU                             |
| J3 | HH     | DD     | C&W TONE A Inputs to ACCU   |

This procedure would recover A/G 1 through NSP #1 (via the CDR's ATU) and would be a great IFM for a complete loss of all internal ACCU functions, but it has two significant drawbacks:

- A. If we only have a partial loss of internal ACCU functions and the J3 bypass is installed, it will disconnect the following functions:
  - MS ATU (\*important)
  - Flight Deck Speaker Unit (\*important)
  - Mid Deck ATU (\*important)
  - Mid Deck Speaker Unit (\*important)
  - A/G #2 on NSP #2 (\*important)

- TACAN 1 and 2
- SSOR
- C&W Tone A
- Channel 2 Voice Recording on NSP #2
- Channel 1 Voice Recording on NSP #1

B. If NSP #1 or CDR's ATU is also disabled, J3 Bypass won't work.

### 15.8.1.2 J4 Bypass

The individual, who developed J3 Bypass, looked at its disadvantages and developed a second procedure... the J4 Bypass. The J4 Bypass allows the crew to disconnect the J4 Plug from the ACCU and install a second "Turnaround Plug" which directly connects the Pilot's ATU to NSP #2's A/G 1.

|    | Pin Hi | Pin Lo | INCO Common Nomenclature   |
|----|--------|--------|--|
| J4 | A      | W      | Pilot's ATU Voice going to ACCU  |
| J4 | B      | X      | Payload Station ATU going to ACCU  |
| J4 | D      | Z      | Airlock ATU going to ACCU  |
| J4 | E      | -A     | NSP #1 A/G2 Audio Output to ACCU   |
| J4 | F      | -B     | NSP #2 A/G1 Audio Output to ACCU   |
| J4 | H      | -D     | TACAN #3 ID TONE sends a command V74K0196E to the ACCU                   |
| J4 | J      | -E     | ICOM B Audio Signals from the Payload Bay to ACCU (Used for KSC Testing) |
| J4 | K      | -F     | ACCU Voice Analog Signal going to Pilot's ATU                            |
| J4 | L      | -G     | ACCU Voice Analog Signal going to Payload Station's ATU                  |
| J4 | N      | -I     | ACCU Voice Analog Signal going to Airlock's ATU                          |
| J4 | P      | -J     | NSP #1 A/G2 AUDIO IN from ACCU   |
| J4 | R      | -K     | NSP #2 A/G1 AUDIO IN from ACCU   |
| J4 | T      | -N     | ACCU Audio Out to the UHF  |
| J4 | -P     | BB     | C&W TONE B Inputs to ACCU  |
| J4 | -R     | -S     | UHF Audio going to ACCU  |
| J4 | -T     | -U     | ICOM B Audio Signals from ACCU to T-0 GSE (Used for lift off)            |
| J4 | -W     | -X     | ICOM B Audio Signals from T-0 GSE (Used for lift off) to ACCU            |
| J4 | -Z     | -Y     | AUDIO RCD CH 2 going to NSP 1  |
| J4 | FF     | EE     | ICOM B Audio Signals from ACCU to Payload Bay (Used for KSC Testing)     |
| J4 | AA     | GG     | AUDIO RCD CH 1 going to NSP 2  |

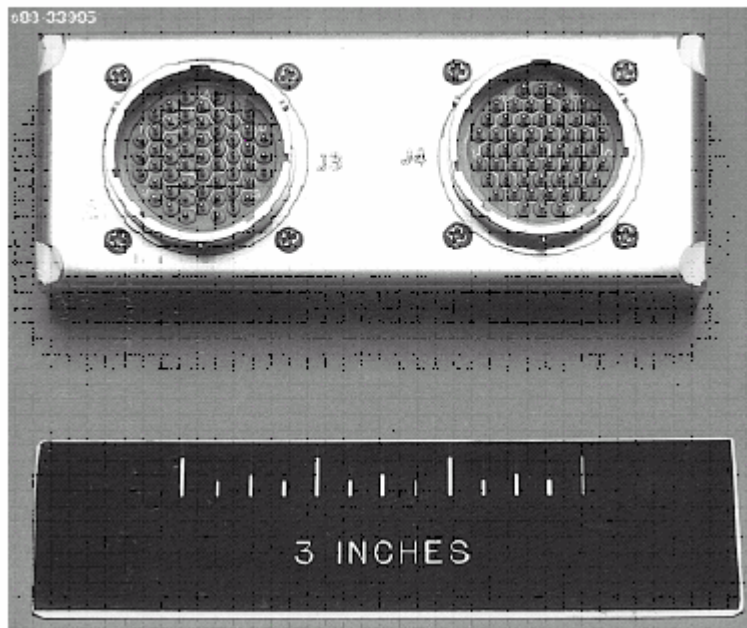
The J4 Bypass procedure will directly connect the Pilot's ATU to NSP #2's A/G1. As you can see by the above table, if the J4 bypass is performed on a partial loss of ACCU, it will also disconnect the following ACCU functions:

- Payload Station ATU
- Mid Deck ATU
- A/G 2 on NSP #1 (*\*important*)
- TONE 3
- UHF (*\*important*)

- C&W Tone B
- Channel 2 Voice Recording on NSP #1
- Channel 1 Voice Recording on NSP #2

Once INCO had developed the procedures, the MMACS community developed one small assembly which contained two “turn-around” plugs and the supporting IFM.

#### ACCU BYPASS CONNECTOR



*Figure 15-20. ACCU Bypass Connector*

### 15.9 SUGGESTED INCO ACTIONS FOR ACCU MALFUNCTIONS

- A. If an internal ACCU fire somehow disables all the internal ACCU cards, the Full Bypass IFM will be installed, you are limited to only having the following voice communications:
- If Ku-Band is out you may have OCA Communication and
  - A/G 1, if you are on NSP #2 hot mike to Pilot's ATU (J4) or
  - A/G 1, if you are on NSP #1 hot mike on CDR's ATU (J3)

During Entry, you will **not** have UHF, A/G 2, or ICOM loops. You will have either the CDR or PLT on A/G#1. INCO should discuss the Pros and Cons of either using a MHA to the “Hot Miked” ATU or allowing CDR's ATU (PLT's ATU) to go to Left (Right) to allow both front seat positions to talk/listen on A/G#1 during Entry.

- B. If ACCU #1 fails due to internal power failure, stay on ACCU #2 do not install the J3 or J4 IFM. Now with ACCU#1 down your next worst failures will be:



- Lose ACCU#2 Internal P/S, Perform both J3 & J4 Bypass (OCA Avail)
- Lose Main C:R14, perform both J3 & J4 Bypass
- Lose Main C, perform only J3 Bypass & swap to NSP #1

Provide a heads up to the crew that if any of these second failures occur, perform the ACCU J3 and J4 Bypass.

C. If ESS 2CA fails, you will lose ACCU#1 and Pilot's ATU, stay on ACCU#2, do not install the J3 or J4 IFM. In this configuration your next worst failures will be:

- Lose ACCU#2 Power Supply, perform only the J3 Bypass & swap to NSP #1 (OCA Avail)
- Lose Main C:R14, perform only the J3 Bypass & swap to NSP #1
- Lose Main C, perform only the J3 Bypass & swap to NSP #1

Provide a heads up to the crew that if any of these second failures occur, perform the ACCU Half Bypass (only J3) IFM and swap to NSP #1 for communications.

D. If Main C:R14 fails, it takes out ACCU#2. Stay on ACCU #1. In this configuration your next worst failures will be:

- Lose ACCU#1 Power Supply, perform J3 and J4 Bypass
- Lose ESS 2CA, perform only the J3 Bypass & swap to NSP #1

Provide a heads up to the crew that if any of these second failures occur, perform J3 and J4 ACCU Bypass IFM.

E. If ACCU#2 R14 cb is open, stay on ACCU #1. In this configuration your next worst failures will be:

- Lose ACCU#1 Power Supply, perform J3 and J4 Bypass (OCA Avail)
- Lose ESS2CA, perform only the J3 Bypass & swap to NSP #1 (OCA Avail)

Provide a heads-up to the crew that if any of these second failures occur, perform the J3 and J4 ACCU Bypass IFM.

F. For a loss of Main C, it takes out ACCU #2 and NSP #2 (J4 Bypass won't work). In this configuration your next worst failure is:

- Lose ACCU#1 Power Supply, perform only the J3 Bypass
- Lose ESS2CA, perform only the J3 Bypass

Provide a heads-up to the crew that if any of these second failures occur, perform the J3 Bypass IFM.

**SECTION 16 - OPERATIONAL WIRELESS CREW  
COMMUNICATIONS SYSTEM**

**CONTENTS**

| <b>Section</b> |  | <b>Page</b> |
|----------------|--|-------------|
| 16.1           | GENERAL DESCRIPTION.....                 | 16-1        |
| 16.1.1         | Interfaces .....                         | 16-1        |
| 16.2           | DESCRIPTION.....                         | 16-2        |
| 16.2.1         | Commonality and Interchangeability ..... | 16-3        |
| 16.2.2         | CRU Operation.....                       | 16-8        |
| 16.2.3         | AIU Operation .....                      | 16-10       |
| 16.2.4         | Module Descriptions.....                 | 16-11       |
| 16.2.5         | Power .....                              | 16-29       |
| 16.2.6         | Frequency Plan Considerations .....      | 16-34       |
| 16.3           | PHYSICAL DESCRIPTION .....               | 16-40       |
| 16.4           | INSTALLATION.....                        | 16-40       |
| 16.4.1         | Locations.....                           | 16-40       |
| 16.4.2         | Cooling.....                             | 16-41       |
| 16.5           | REFERENCES.....                          | 16-41       |

## TABLES

| <b>Table</b> |   | <b>Page</b> |
|--------------|---|-------------|
| 16-1         | Receiver module performance.....  | 16-9        |
| 16-2         | Transmitter module performance .....  | 16-9        |
| 16-3         | IF AMP/DEMODO module performance .....  | 16-17       |
| 16-4         | Receive audio module performance .....  | 16-20       |
| 16-5         | Transmit audio module performance.....  | 16-21       |
| 16-6         | Synthesizer module performance .....  | 16-24       |
| 16-7         | Frequency programming module performance.....   | 16-25       |
| 16-8         | Stowage matrix for wireless crew communications system Li-BCX<br>battery (P/N SED33103846-709)..... | 16-33       |
| 16-9         | Flight and MOD training frequency plan* .....   | 16-35       |
| 16-10        | Spacelab flight frequency plan.....   | 16-36       |
| 16-11        | SMS fixed base frequency plan .....   | 16-37       |
| 16-12        | SMS motion base plan .....  | 16-38       |
| 16-13        | SMS red plan .....  | 16-39       |
| 16-14        | SLS plan .....  | 16-40       |

## FIGURES

| <b>Figure</b> |   |       |
|---------------|---|-------|
| 16-1          | WCCS functional diagram .....                         | 16-4  |
| 16-2          | CRU hardware view.....                                | 16-5  |
| 16-3          | AIU hardware view.....                                | 16-5  |
| 16-4          | CRU block diagram.....                                | 16-6  |
| 16-5          | AIU block diagram .....                               | 16-7  |
| 16-6          | Receiver block diagram .....                          | 16-11 |
| 16-7          | Transmitter module.....                               | 16-14 |
| 16-8          | IF amplifier/demodulator module .....                 | 16-14 |
| 16-9          | Digital discriminator/demodulator block diagram ..... | 16-16 |
| 16-10         | Receive audio module .....                            | 16-19 |
| 16-11         | Transmit audio module .....                           | 16-22 |
| 16-12         | Synthesizer module .....                              | 16-23 |
| 16-13         | Frequency programming module.....                     | 16-25 |
| 16-14         | Audio summer module block diagram .....               | 16-27 |
| 16-15         | Amplifier/regulator module.....                       | 16-28 |
| 16-16         | CRU battery pack .....                                | 16-31 |
| 16-17         | Battery discharge curve .....                         | 16-32 |
| 16-18         | Location of AIU A.....                                | 16-42 |
| 16-19         | Location of AIU B.....                                | 16-43 |
| 16-20         | Location of AIU C .....                               | 16-43 |

## SECTION 16 - OPERATIONAL WIRELESS CREW COMMUNICATIONS SYSTEM

### 16.1 GENERAL DESCRIPTION

The operational Wireless Crew Communications System (WCCS) is a full duplex voice communication system for use within the space shuttle orbiter and Spacelab. The system transmits and receives audio as 32 kbps digital streams in the frequency range of 340 to 390 MHz. The Crew Remote Unit (CRU) and Audio Interface Unit (AIU) are the major components of the system.

The CRU is a full duplex, multichannel Radio Frequency (RF) transceiver worn by individual space shuttle crewmembers to provide wireless communications to other crewmembers and to the ground communications via a WCCS AIU and the orbiter Audio Distribution System (ADS). The CRU is battery operated and is normally worn attached to the crewmember's leg. Audio interfaces are with a standard shuttle headset. The CRU is capable of operation in either a plain text mode or optional secure voice mode by use of separately supplied plug-in Communications Security (COMSEC) modules.

The AIU is a two-channel, full duplex RF receiver/transmitter which provides wireless communications between space shuttle crewmembers and downlinks communications via WCCS CRU and the orbiter ADS. The AIU is normally wall-mounted in the flight deck, ceiling-mounted in the middeck, and panel-mounted in Spacelab. Audio, control, and power interfaces are with standard ADS Crewmember Communications Umbilical/Headset Interface Unit (CCU/HIU) connectors. Primary capabilities link crewmembers on two AIU channels, intercom (intercommunications system, also called INCO) and transmit, controlled by decoded Push-To-Talk (PTT) commands from the crewmembers' CRUs. A secondary function provides an optional hardline link via an HIU-III connected directly to an AIU CCU/HIU connector. The AIU is capable of operation in either a plain text mode or optional secure voice mode by use of separately supplied plug-in COMSEC or plain text modules.

#### 16.1.1 Interfaces

The AIU is connected to the Audio Terminal Unit (ATU) audio port by a short, standard cable changed by replacing the HIU receptacle with an HIU cable end connector. This cable supplies the AIU with its power supply stimulus and return, headset earphone audio signals for the transmit channels, and returns audio from the receive channels to the HIU mic pin at the ATU. PTT XMIT and ICOM switch closure controls are also accomplished through this cable. A Crypto Variable Fill Adapter connection is provided and is used only during loading operations preflight. Another connector on the AIU case is for the CCU/ HIU, which allows hardline use of the ATU without disconnecting the AIU.

The CRU headset connector operates as a standard headset connector, but it has a second function. Offset pin locations and a specially keyed connector provide an interface with the Crypto Variable Fill Adapter.

## 16.2 DESCRIPTION

The WCCS/ADS functional block diagram shown in Figure 16-1 is provided to help show the system concept and audio routing. The CRU hardware is shown on Figure 16-2, and the ATU hardware is shown on Figure 16-3. The block diagrams shown in Figure 16-4 and Figure 16-5 illustrate the basic operation of both the CRU and AIU along with their modules. It may aid retention to closely study the block diagrams along with the following module lists.

The CRU (Figure 16-4) is made up of the following modules:

- Ultrahigh Frequency (UHF) transmit module
- Synthesizer module (two)
- UHF receiver module
- Intermediate Frequency (IF) amplifier/demodulator module
- Plain Text Interconnect (PTI) module (two)\*
- COMSEC module (two)\*
- Receive audio module
- Transmit audio module
- Frequency Programming Module (FPM) (CRU only)

\*Operation in a secure voice mode is optional, provided by interchanging each PTI module with a COMSEC module.

The AIU (Figure 16-5) is made up of the following modules:

- UHF transmit module (two)
- Synthesizer module (four)
- UHF receiver module (two)
- IF amplifier/demodulator module (two)
- PTI module (four)\*
- COMSEC module (four)\*
- Receive audio module (two)
- Transmit audio module (two)
- Audio summer module (AIU only)
- Amplifier/regulator module (AIU only)

\*Operation in a secure voice mode is optional, provided by interchanging each PTI module with a COMSEC module.

### **16.2.1 Commonality and Interchangeability**

The operational WCCS is designed with a high level of commonality and interchangeability (both electrically and mechanically) between CRU and the AIU. Only the audio summer, amplifier/regulator, and frequency programming modules are unique as shown by the previous lists of modules.

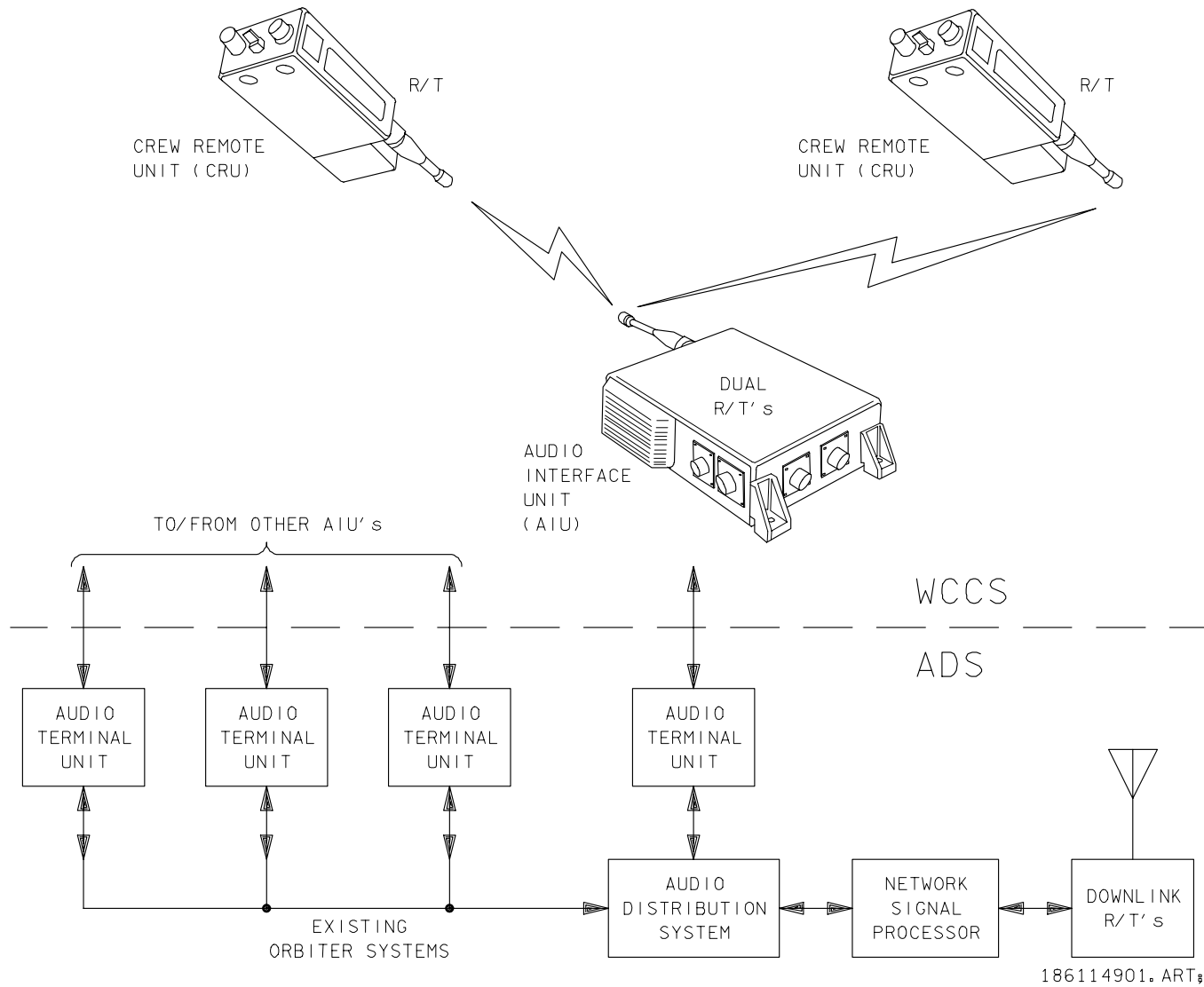


Figure 16-1. WCCS functional diagram



Figure 16-2. CRU hardware view

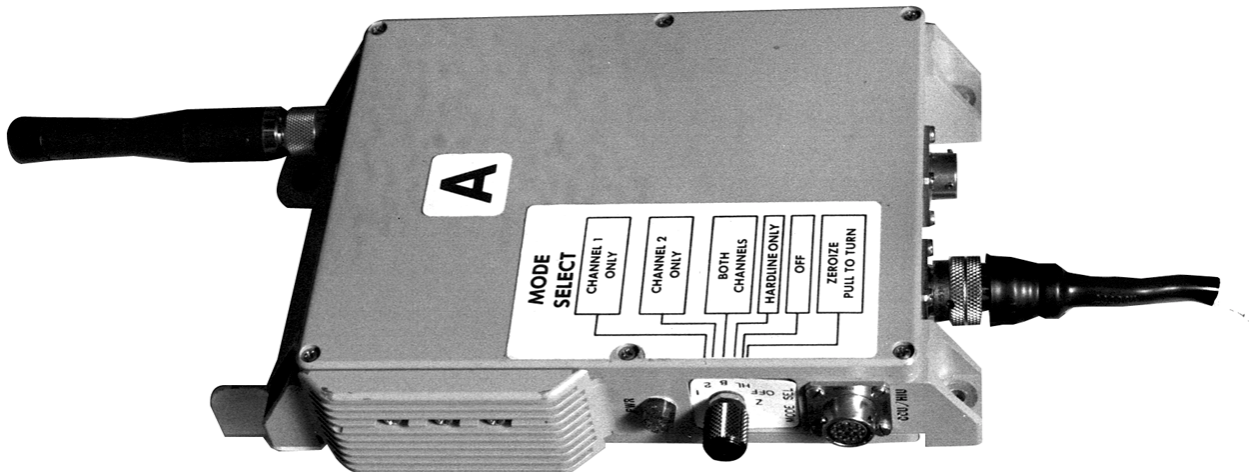


Figure 16-3. AIU hardware view





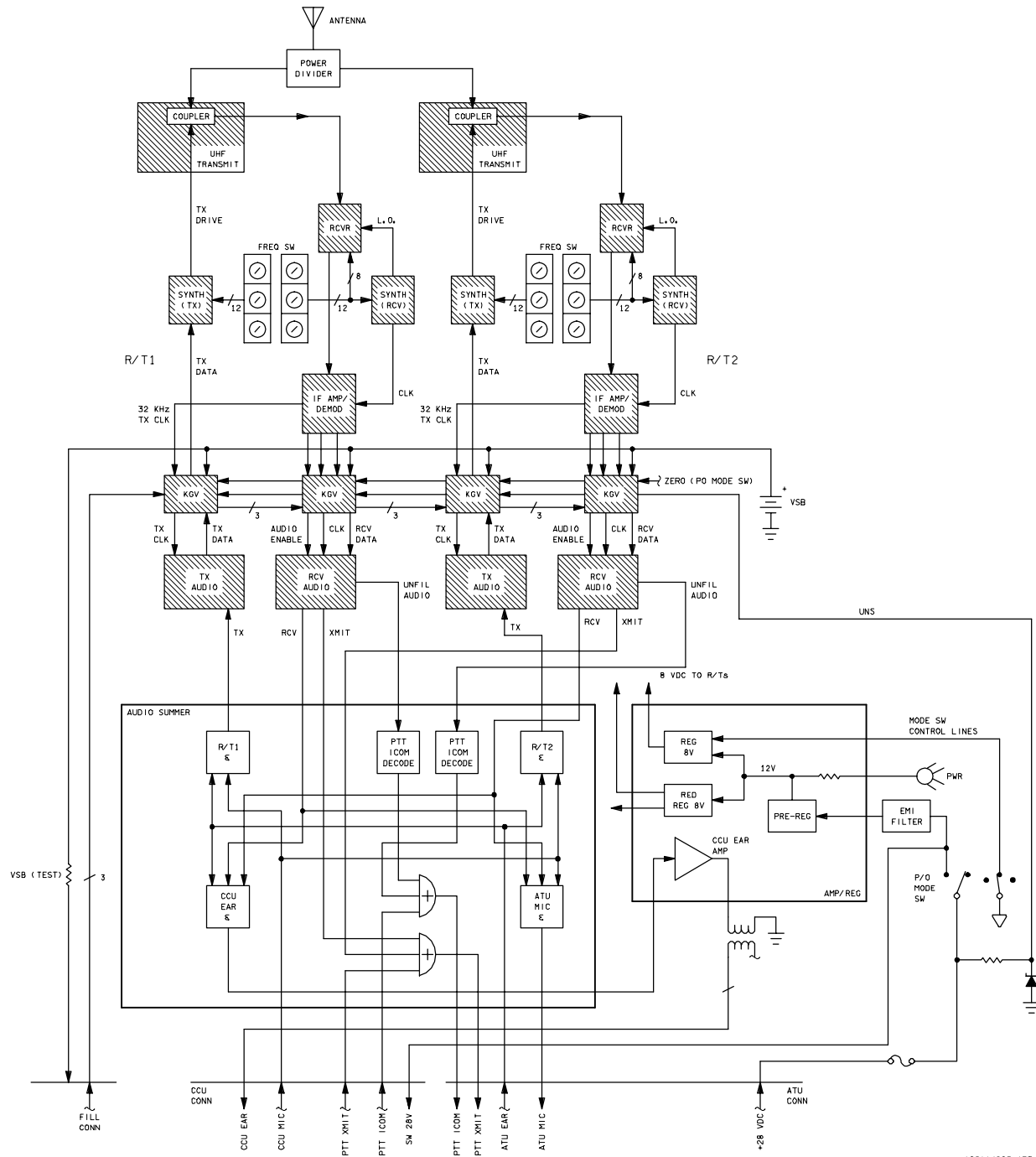


Figure 16-5. AIU block diagram

186114905, ART 2

### 16.2.2 CRU Operation

The CRU operates in a full duplex mode with a continuous wave transmitter (f1 - transmit/f2 - receive) on any of eight operator selectable preset channels.

The mode of operation is operator selected as either

- ON - Continuous full duplex receive/transmit
- Zeroize - Operator-selected mode to zeroize crypto variables when the CRU is operated in the COMSEC mode
- OFF - No RF operations. Keep alive voltage supplied to crypto variable

The PTT modes provide a link between crewmembers connected to other AIU/ATU destinations, or specific downlinking is provided through the use of PTT modes. Subaudible tones are generated in the CRU and mixed with transmit voice prior to digitization and subsequently filtered and decoded in an AIU for recognition of a specific PTT control signal. The WCCS AIU provides switch closure signals to an ATU and hence to the ADS for appropriate control.

When the PTT ICOM switch is pressed on a CRU, a 94.8-Hz subaudible tone is generated and transmitted for the purpose of controlling selected linking to other crewmembers via the intercom.

When the PTT XMIT switch is pressed on a CRU, a 79.7-Hz subaudible tone is generated and transmitted for the purpose of controlling selected linking to other crewmembers via the intercom, plus selected (at an ATU) downlinking.

The CRU frequency selection is operator-controlled by an external rotary switch which is set to any one of eight preset duplex RF channels. It is the switch position which controls the addressed channel pair of frequencies in the FPM Programmable Read Only Memory (PROM). The frequencies stored in the PROM are loaded preflight according to a frequency plan developed to provide the most efficient use of the available frequency band. Separation of a selected predefined channel Transmitter/Receiver (T/R) frequencies and those of another channel are required to be 100 KHz over the 340.0 to 389.9 MHz band. The two frequency plans are shown in Table 16-1 and Table 16-2.

**Table 16-1. Receiver module performance**

| Parameter                       | Performance                |
|---------------------------------|----------------------------|
| Frequency range                 | 340 to 390 MHz             |
| Sensitivity in WCCS application | 102 dBm for 25 dB SINAD CT |
| Gain                            | -5 dB minimum              |
| Dynamic range                   | 90 dB minimum              |
| RF bandwidth                    |                            |
| 0.5 dB                          | 5 MHz minimum              |
| 20 dB                           | 26 MHz maximum             |
| Spurious rejection              | 80 dB minimum              |
| Intermodulation                 | -66 dB minimum             |
| Reverse radiated power (L.O.)   | -73 dBm maximum            |

**Table 16-2. Transmitter module performance**

| Parameter        | Performance   |
|------------------|---|
| RF output power  | +10.5 dBm nominal into 50 ohms (at antenna connector) |
| Frequency range  | 340 to 389.9 MHz                                      |
| Output harmonics | -50 dBc second and third<br>-50 dBc above third       |
| Protection       | No damage under variable load conditions              |

The system operates with voice sampled at the rate of 32 KHz and encoded/decoded digitally using the Continuously Variable Slope Deltamodulation (CVSD) algorithm. The modulation type used is binary Frequency Shift Keying (FSK).

The CRU is capable of operating in either the cryptographic or noncryptographic mode. Encryption is obtained by the use of the KGV-99 COMSEC modules. When the secure voice is not required, the noncryptographic mode is obtained by replacing the COMSEC modules with functional PTI modules. A connector is provided on the CRU to accept a cryptographic variable from a KYK-13 fill device through the WCCS fill adapter. The COMSEC circuitry is on whenever the unit power is on. An internal keep-alive power supply is provided to prevent loss of the cryptographic variable storage when switching to the OFF position of the power switch or when changing the battery pack.

### 16.2.3 AIU Operation

Each AIU Receiver/Transmitter (R/T) channel operates in a full duplex mode (f1 - transmit/f2 - receive) on one or both preset channels. The mode is operator-selected by the mode switch as either

- ZERO - Overt action, pull-to-turn zeroizing of cryptovvariable when in COMSEC operation
- OFF - All power down except a sustaining voltage for COMSEC operation
- H/L - Hardline operation only via HIU-III and CCU/HIU connector
- BOTH - Simultaneous RF/hardline operation with both R/Ts operational, providing links for crewmembers whose CRUs are on these channels via the ADS as selected
- 2 - Simultaneous RF/hardline operational with only R/T 2 operational, providing links from one crewmember (whose CRU is on this channel), via the ADS as selected
- 1 - Simultaneous RF/hardline operation with only R/T 1 operational, providing links from one crewmember (whose CRU is on this channel) via the ADS as selected

When a PTT subaudible tone from a CRU is detected by the AIU by the presence of the PTT ICOM subaudible tone (94.8 Hz + 0.5 percent) or PTT XMIT subaudible tone (79.7 Hz + 0.5 percent) on either incoming audio channel, the AIU responds by providing a switch closure for the appropriate function at the AIU-ATU interface connector. PTT switch commands for both ICOM and XMIT modes from an HIU-III at the AIU hardline connector shall be logically OR'd with decoded PTT tone commands from either AIU receiver. The single switch closure provided by the AIU necessitates caution on the part of the users, since a single PTT command can enable up to three mics at the same time.

The AIU operates in a continuous wave transmission mode under the same modulation, COMSEC, and frequency requirements as the CRU. Determination of AIU channel

frequency differs from the CRU in that the CRU employs a PROM, while the AIU frequencies are determined by preset, internal, rotary switches. The frequency allocation plan applies to the AIU also.

The AIU is capable of operating in either the cryptographic or noncryptographic mode. Encryption is obtained by the use of the KGV-99/TSEC COMSEC modules. The PTI module provides unencrypted operation as in the CRU. A cryptographic variable fill connector is provided on the AIU the same as with the CRU. Also as in the CRU, an internal keep-alive circuit is provided to prevent loss of the cryptographic variable storage when switching to the OFF position of the power switch or during disconnection from the ATU power.

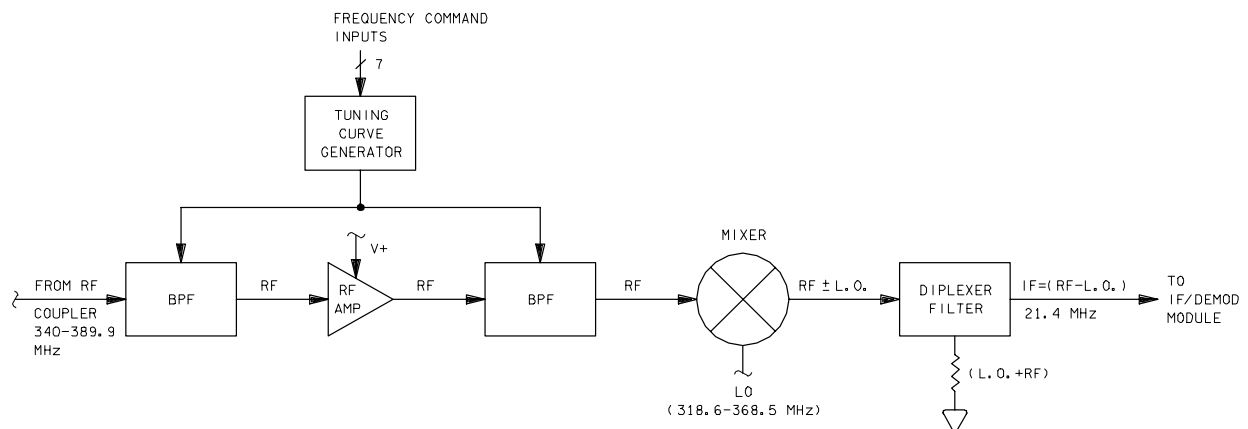
PTT ICOM and PTT XMIT functions of the AIU-operate are described in Section 16.2.2, CRU Operation.

### 16.2.4 Module Descriptions

The following sections are the descriptions of the individual modules used in the WCCS.

#### 16.2.4.1 Receiver Module

The receiver module shown in Figure 16-6 is a tunable, active RF preselector/frequency converter which interfaces between the antenna coupler and the IF amplifier/demodulator module. The receiver module performs two basic signal processing functions.



186114906, ART: 2

**Figure 16-6. Receiver block diagram**

- A. Electronically tunes the receiver to the selected RF operating frequency by means of a frequency converter (mixer) and a precisely offset variable frequency local oscillator (synthesizer) and outputs an IF signal centered at 21.400 MHz to the IF amplifier/demodulator module.
- B. In conjunction with the subsequent IF crystal filter, establishes the receiver sensitivity and dynamic range by providing appropriate gain and spectrum limiting (RF and IF bandwidths) to minimize signal-to-noise degradation by the inherent internal thermal noise and by both internally and externally generated spurious signals.

The functional characteristics of the various circuit blocks within the receiver module are described below.

A. Bandpass filter

The bandpass filter is a voltage-controlled, varactor-tuned RF filter employing miniature discrete components. The filter maintains a constant absolute passband shape and bandwidth as it is tuned across the 340 to 390 MHz frequency range. The tuning voltage ranges from 4.25 volts at 340 MHz to 17.4 volts at 390 MHz and is supplied by the Tuning Curve Generator (TCG) integrated circuit.

B. RF amplifier

The RF amplifier is a hybrid wideband (10 to 500 MHz), low-noise RF device. The amplifier provides a minimum of 14 dB gain and has a maximum noise figure of 2.5 dB over the 340- to 390-MHz frequency range. The 1-dB gain compression point of this amplifier occurs at approximately 0-dBm output. The amplifier circuit operates on 10 milliamperes maximum current drain and 6 volts minimum supply voltage.

C. Mixer

The mixer is a standard miniature wideband (1 to 1000 MHz), double-balanced Shottky-diode mixer. With an L.O. drive level between +4 and +8 dBm, the mixer has a conversion loss of 6 dB and a noise figure of 7 dB maximum over the 340- to 390-MHz frequency range.

D. Diplexer Filter

The filter features a wideband input and two separate outputs: a low-pass output for the 21.4-MHz IF signal and an internally terminated high-pass output. The crossover frequency is approximately 60 MHz, and the insertion loss at the IF frequency is under 0.5 dB. The filter presents the mixer with a constant 50ohm impedance at all frequencies of interest; i.e., IF, RF L.O., and RF + L.O.

## E. Tuning Curve Generator

The TCG is a Large Scale Integration (LSI) chip which decodes the frequency information supplied in Binary Coded Decimal (BCD) format and translates it into a corresponding analog dc voltage level, which becomes the reverse bias voltage for the varactors within the tunable RF bandpass filters. The TCG output voltage versus frequency is exponential as required by the varactor diode characteristics and includes temperature compensation.

### 16.2.4.1.1 Receiver signal flow

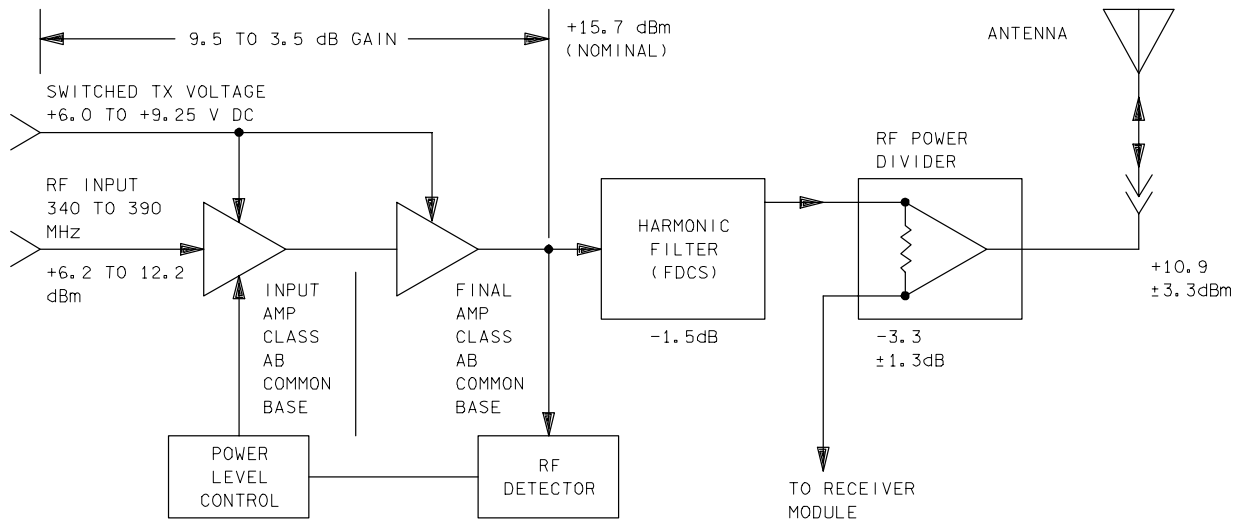
The received signal from the antenna coupler passes through an RF bandpass filter, tuned to the selected center frequency, limiting the spectrum bandwidth applied to the subsequent RF circuits. The low-noise RF amplifier provides a minimum of 14-dB RF gain to ensure satisfaction of the receiver sensitivity requirements. A second tuned RF bandpass filter identical to the first filter further limits the RF spectrum bandwidth applied to the following mixer to minimize generation of potential spurious outputs. The mixer heterodynes the receiver RF signal with the local oscillator signal, tuned exactly 21.4 MHz below the selected receiver frequency and generates two output frequency spectra: one centered at 21.4 MHz and the other at the sum frequency. A diplexer filter separates these two signals, passing the desired 21.4 MHz (IF) spectrum to the IF amplifier/demodulator module for further processing and terminating the undesired sum frequency spectrum, as well as any residual RF and L.O. signals appearing at the mixer output in a resistive 50-ohm load, to ensure consistent balance performance of the mixer circuit.

### 16.2.4.2 Transmitter Module

The transmit module (Figure 16-7) provides the interface between the synthesizer and the antenna. It also provides the necessary RF power gain. Another function of the module is separation of the receive and transmit signals to and from the antenna.

The RF input from the synthesizer and the switched transmit dc voltage are always present in the WCCS full duplex Continuous Wave (CW) operation. The RF gain of the first amplifier is set low to provide good isolation for the synthesizer. Both stages use similar transistor types, selected for high device isolation. Selection of a common base circuit and the use of high quality base circuit decoupling capacitors provide improved isolation. This high isolation prevents synthesizer frequency pulling if the antenna impedance changes in an abrupt manner. The final amplifier output is passed through the low pass/harmonic filter (nominal insertion loss = 0.7 dB) to the two-way, in-phase power divider, to the antenna circuit.





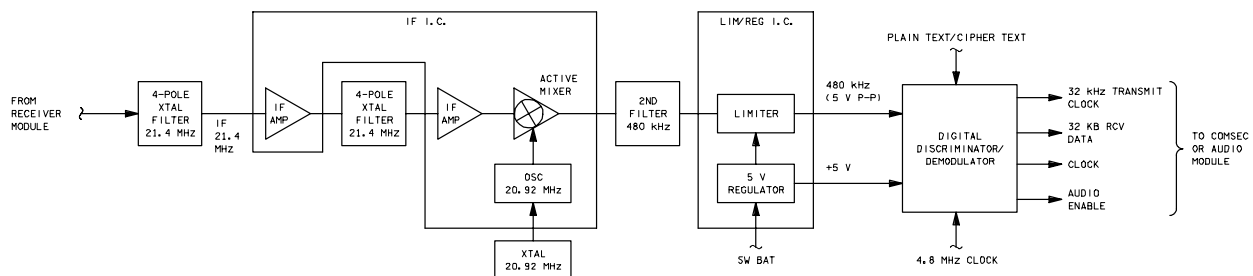
186114907. ART 2

**Figure 16-7. Transmitter module**

A simple in-phase, two-way RF power divider is used to separate the receive and transmit signals from/to the antenna. The RF frequency plan makes this scheme workable by the transmit and receive frequencies being defined about 20 MHz apart, thus enabling effective receiver front-end filtering. The isolation between the power divider receive and transmit ports is sensitive to antenna Voltage Standing Wave Ratio (VSWR), which can vary between 13 and 22 dB. This inexpensive, simple approach eliminates the need for complex-tuned RF frequency separation circuits.

### 16.2.4.3 IF Amplifier/Demodulator Module

The IF amplifier/demodulator module (Figure 16-8) performs the following functions:



186114908. ART 2

**Figure 16-8. IF amplifier/demodulator module**

- A. Provides most of the receiver signal gain
- B. Establishes the final receiver bandwidth
- C. Performs the second frequency translation to an output center frequency of 480 KHz, compatible with digital demodulation capabilities

- D. Limits the amplitude of the IF output to supply a constant peak amplitude (5 volts) to the discriminator/demodulator
- E. Demodulates the FSK data and provides clock synchronization for baseband 32 kb/s data
- F. Provides squelch operation as a function of RF channel to audio SINAD performance characteristics

The IF section provides most of the signal amplification required in the receiver. The IF signal passes through a four-pole crystal filter which limits the signal bandwidth applied to the first IF amplifier. Use of only four poles at this point limits losses, affecting sensitivity, ahead of the first IF amplifier.

The first IF amplifier establishes the sensitivity of the IF section. A second four-pole filter removes the thermal image noise contribution of the first IF amplifier, centered at 20.44 MHz, prior to the second frequency conversion. The combined response of the two filters establishes the overall IF bandwidth and spurious rejection of the receiver. A second, identical IF amplifier followed by an active mixer provides the remainder of the linear IF gain and the second frequency translation to a 480-KHz center frequency.

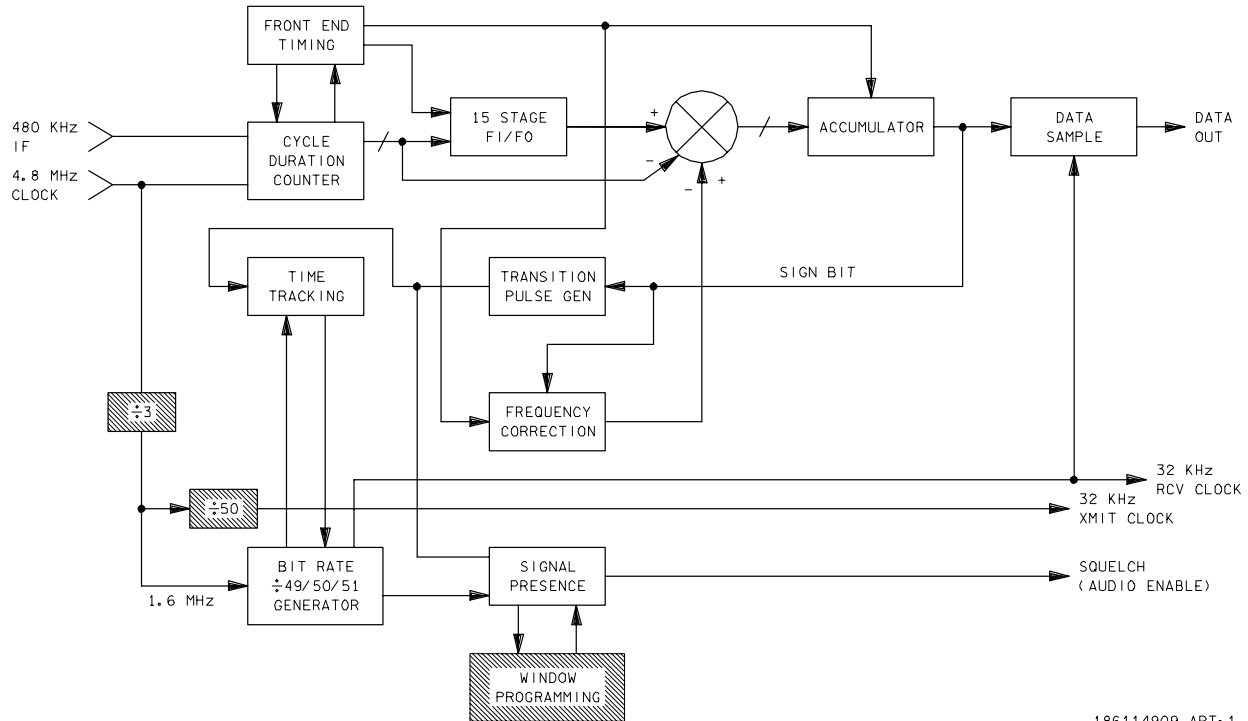
The second IF bandpass filter (480 KHz) removes the undesired components resulting from the second frequency conversion (21.4 MHz IF, 20.92 MHz LO, 42.32 MHz sum sideband) and the very low frequency noise inserted by the active mixer and then passes the signal and noise present within the desired receiver bandwidth to the limiter. The limiter normalizes the amplitude of the receiver output and supplies the FSK digital demodulator with a 5-volt peak-to-peak input.

Two sets of four-pole crystal filters are used at 21.4 MHz by the IF stage of the module. The first IF amplifier/active mixer are two master circuits on a single IC. Each IF amplifier is a cascade type to provide sufficient isolation between the various stages. Following the active mixer, the limiter/regulator circuit provides the remainder of the receiver gain at 480 KHz. The limiter and a 5-volt regulator are contained on one bipolar chip packaged in a 24 Input/Output (I/O) leadless chip carrier. The 5-volt regulator serves limiter output swing and provides the IF amplifiers with a stable reference bias for a constant impedance match to the crystal filters.

The discriminator/demodulator is fabricated using isolated field Complementary Metal Oxide Semiconductor (CMOS) technology. The chip performs the functions of discrimination, integrate-and-dump filter demodulation, and clock recovery. A frequency correction function allows for operation with IF frequency error without performance degradation. A digital squelch control function is also part of the demodulator chip.

In the cycle duration counter, the deviation of each cycle of the IF is measured with respect to the 4.8-MHz sampling rate. The value is compared with the nominal value of the unmodulated IF, and a signed difference value is generated for each IF cycle. These values are stored in a first-in/ first-out register, which stores a number of values equal to 480 Hz divided by the data rate, thus acting as a 1 bit delay. The difference

values are continually subtracted from the delayed difference values, and the results are continually accumulated. These operations constitute the digital equivalent of a discriminator and an integrate-and-dump filter.



186114909. ART 1

**Figure 16-9. Digital discriminator/demodulator block diagram**

Transitions of the sign bit of the accumulator (the demodulator signal) are phase-compared to a locally generated bit rate. The results are integrated in the time tracker and applied to the bit rate generation as phase corrections. A signal from the reconstructed clock is used to sample the demodulator signal, forming a retimed data output.

The bit rate generator consists of a variable divider of ratio 49/50/51 with nominal value 50. For this application, a divide by three generates 1.6-MHz from the 4.8-MHz clock. The 1.6-MHz clock allows the time/frequency correction circuitry to operate at the 32-kbps data rate.

An error in the nominal frequency of the IF signal causes the accumulator value to be offset. This offset is measured by comparing the amount of the time the sign bit is high to the amount of the time it is low. The difference is averaged over a large number of bits, and corrections are applied to the accumulator until its output is balanced.

Signal presence (AIU receiver “usable voice” squelch control) is determined by comparing the time of occurrence of demodulated signal transitions with the expected time of arrival, as defined by an adjustable “window” generated by the bit rate generator. When the number of data transitions which fall in the window exceeds the number

which do not (equivalent to an open “eye” pattern) for a certain number of transitions, squelch is opened. Squelch is closed when the reverse situation occurs.

**Table 16-3. IF AMP/DEMODO module performance**

| Parameter                   | Performance                                   |
|-----------------------------|---|
| Linear active gain          | 66 dB + 3 dB                                  |
| Limiter (low signal) gain   | 70 dB   |
| Bandwidth:<br>6 dB<br>70 dB | 50 KHz nom.<br>+200 KHz max.                  |
| Limiter output frequency    | 480 KHz center                                |
| Limiter output              | 5 volts peak to peak                          |
| FSK demodulation            | Provide recovered data and synchronous clock  |
| SINAD based squelch         | Programmable over range of usable voice SINAD |

#### 16.2.4.4 Receive Audio Module

The receive audio module (Figure 16-10) provides Digital-to-Analog (D/A) conversion using 32-kbps CVSD demodulation and receive analog processing. When used in the CRU, the module generates and injects to the transmit modulation one of two subaudible tones for PTT ICOM and PTT XMIT control signals. In the AIU it serves to decode these subaudible tones and supplies PTT control lines to the ATU for transmit control. A “beep” tone generator circuit is activated to alert the operator to a low battery condition.

The received audio is first reconstructed by the CVSD and then sent to the volume/control circuit. This analog unfiltered audio signal is also routed off the module for use in the AIU by the tone detector on the AIU audio summer module to detect the ICOM tone while the XMIT tone is detected by the tone generator and detector. The volume/control circuit contains the control logic to ensure proper receive mode operation under the various operating modes. It contains the low battery detector and introduces a beep tone in the audio path. Volume control is achieved by varying the dc voltage from the volume control rotary on the CRU. In the AIU, this level is set constant. The variable dc approach minimizes audio pickup on other sensitive unit level interconnections. The Voice-Operated Transmission (VOX) portion of the circuit is not operative, since it was not incorporated due to a slow attack time. When used in the

CRU, the audio is routed directly from the CVSD to the volume/control circuit because the tone reject high-pass filter is not needed, and turning the detector off saves power.

Following the volume/control circuits, the audio amp/regulator circuit provides the required CRU low- and high-pass filtering. Adequate gain is provided by the amplifier to provide the 100-mW requirement for WCCS. Due to the 600-ohm impedance of the headset and the low 7.2 V dc supply voltage, an output transformer is required. This transformer is mounted off the module as part of the radio case. Due to the low power level, a small transformer is used.

In the CRU, tone generation is accomplished by dividing the 1-MHz reference frequency of the crystal oscillator. Harmonics in the transmit tone spectrum are greater than 40 dB down due to filtering and can therefore be summed in with the audio with minimal degradation of audio Signal To Input Noise and Distortion (SINAD). A tone level of -12 dB relative to the nominal 0.4 Vrms audio level is sufficient for tone detection and degrades an 800-Hz SINAD by less than 0.25 dB when suitably filtered out at the receive (AIU) side.



**Table 16-4. Receive audio module performance**

| Parameter                            | Performance  |
|--------------------------------------|--|
| Receive audio response               | 300 to 2700 Hz   |
| Subaudible tones                     | PTT ICOM 94.8 Hz<br>PTT XMIT 79.7 Hz                                       |
| (SINAD)                              | >28dB at 300 Hz with allowable rolloff to 3 kHz                            |
| Subaudible tone decode time (in AIU) | ≤220 msec  |
| Voice encoding                       | 32 kb/s CVSD at 0.4 Vrms   |
| CRU volume control range to headset  | -20 to +20 dBm   |
| Low battery beeper                   | Low battery monitor<br>Tone = 1 kHz<br>Rate = 1.3 sec.<br>Duty cycle = 10% |

The ICOM and XMIT tones selected are 94.8 Hz and 79.9 Hz. Included in the tone generator/detector section of the module is a tone detection circuit which has a fast rolloff high-pass filter to prevent the voice signals from degrading the operation of the tone detector in the receive (AIU) path. The high-pass filter in the receive path effectively removes the tone as the post-CVSD spectrum of the 79.7-Hz tone is -12 dB before the high-pass filter and -58 dB after the filter.

#### 16.2.4.5 Transmit Audio Module

The input from the CRU headset microphone or the RCV/XMIT channel summer is amplified and leveled over the -72 to -44 dBV input range by the Preamp/ Automatic Gain Control (AGC) circuit. This circuit has a greater than 30-dB AGC range and operates at a low power level. AGC range and time constants perform well for a wide range of users from low level audio to loud shouts in a high noise environment.

Transmit frequency shaping (300 to 3000 Hz) is also accomplished by the preamp/AGC circuit and the audio output variation over the microphone input range controlled within 2 dB. The measured variation in SINAD from the low level microphone input of the preamp/AGC chip through a CVSD encoder/decoder at a 32-KHz clock rate is quite small over a 40-dB range (-90 to -50 dBV). The SINAD tests have shown it to remain below the 28-dB requirement for the WCCS.

Following the preamp/AGC circuit, the audio is summed with one of two subaudio tones as a function of ICOM or XMIT PTT operation of the CRU. Tone generation and detection (used in the AIU application) is done by an MX335 device produced by Microcircuits for communications. This device is located on the receive audio module.

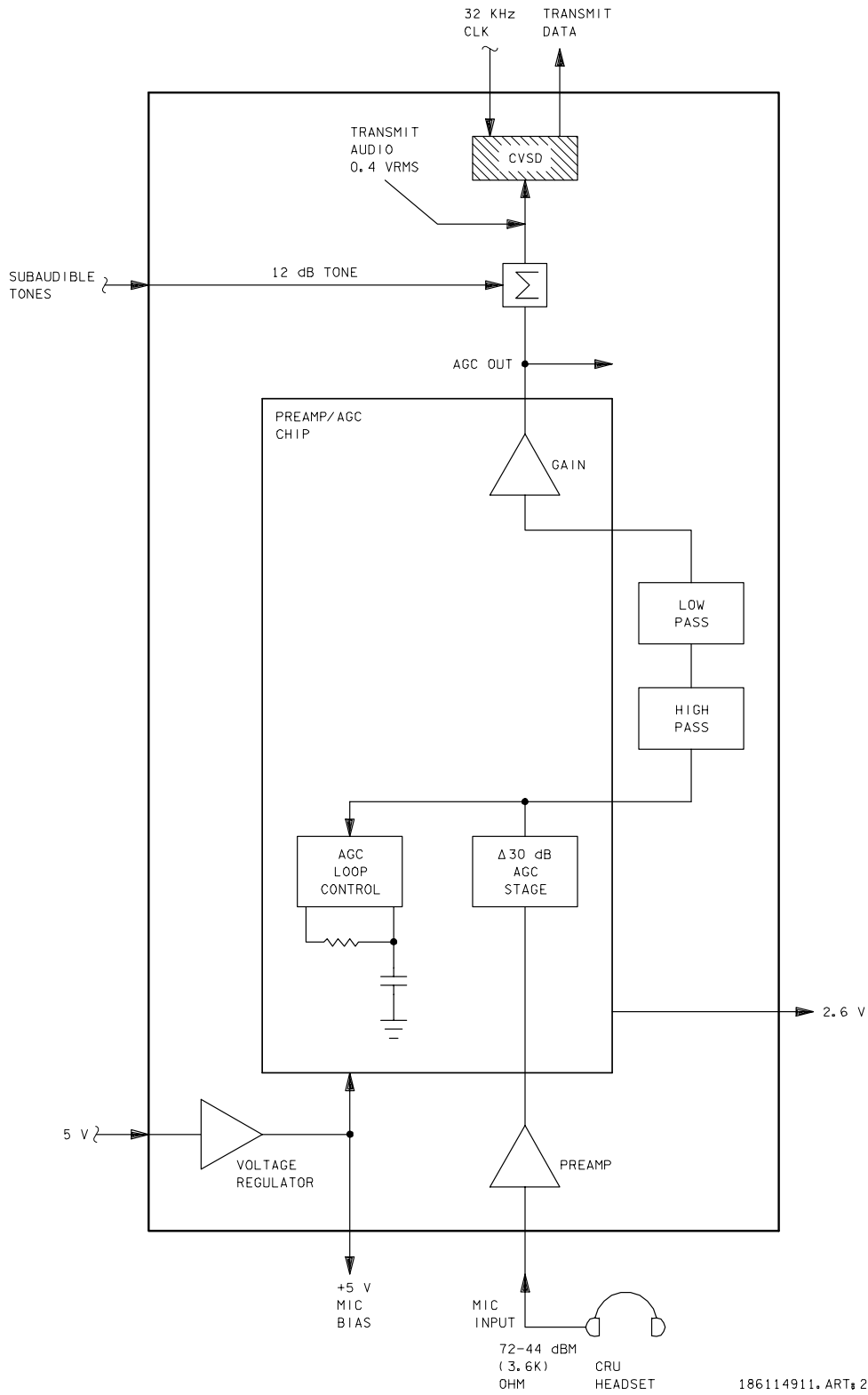
Subaudible tones from the CRU receive audio module inserts harmonics into the transmit tone spectrum which are greater than 40 dB down due to filtering and can therefore be summed in with the transmit audio with minimal degradation of audio SINAD. A tone level of -12 dB relative to the nominal 0.4 Vrms audio level is sufficient for tone detection and degrades an 800-Hz SINAD by less than 0.25 dB when suitably filtered out at the receiving AIU.

After the subaudible tone is added to the transmit audio signal, the resultant analog signal is digitized by the double integration CVSD operating at a 32-KHz clock rate. The CVSD CRU-to-AIU and AIU-to-CRU (double encoding/decoding) link at the nominal drive level of 0.4 Vrms, using a double integration feedback loop and low-pass filtering, performs within the SINAD requirements of greater than 28 dB at 300 Hz with the allowable rolloff to 3 KHz. Degradation due to the double encoding/decoding of the CRU-to-CRU link is on the order of 3 dB.

**Table 16-5. Transmit audio module performance**

| Parameter               | Performance                                      |
|-------------------------|--|
| Mic input range (CRU)   | -72 to -44 dBV                                   |
| Transmit audio response | 300 to 2700 Hz                                   |
| Transmit audio AGC      | 2-dB variation to CVSD                           |
| SINAD                   | >28 dB at 300 Hz with allowable rolloff to 3 kHz |
| Voice encoding          | 32-kbps CVSD with 0.4 Vrms drive                 |





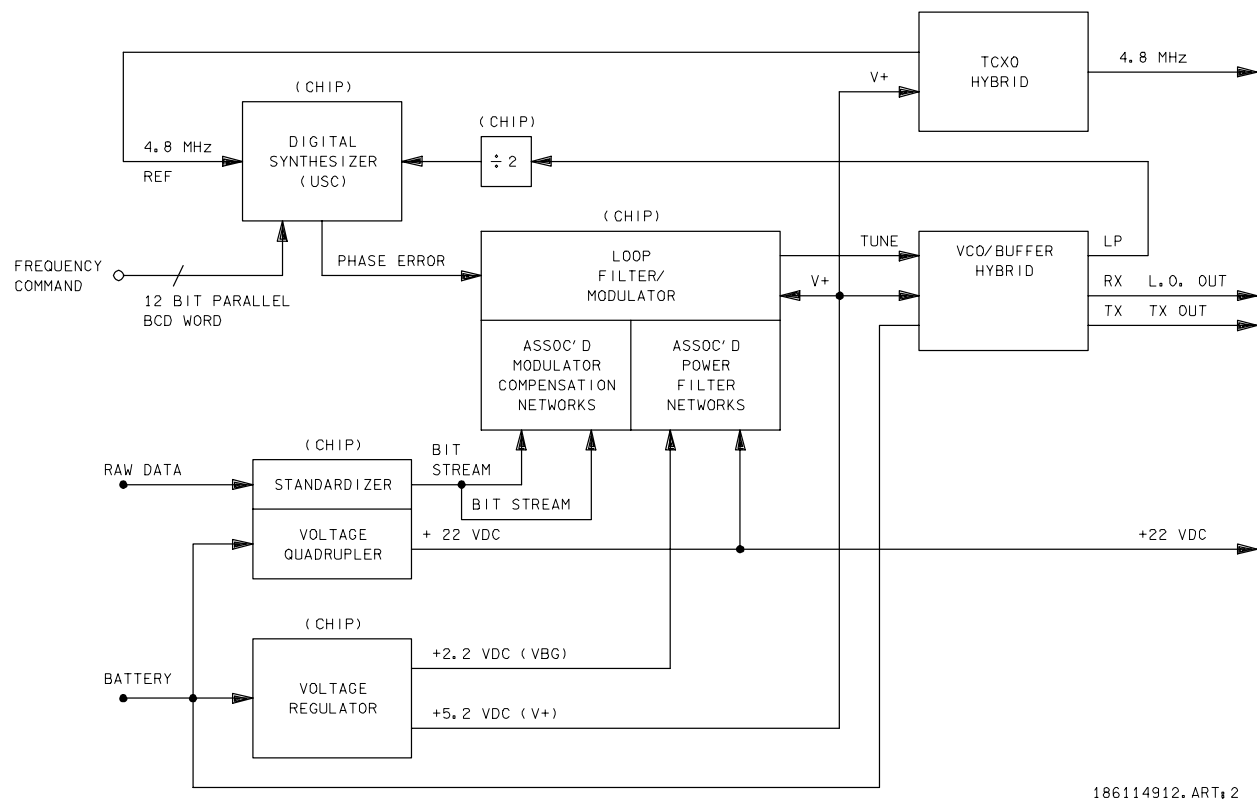
186114911, ART# 2

Figure 16-11. Transmit audio module

### 16.2.4.6 Synthesizer Module

The receiver side of the WCCS uses the synthesizer module (Figure 16-12) to provide the first local oscillator to the receiver module. When dedicated to a transmit channel, the synthesizer module provides the 32-kbps FSK modulation to the digitized audio from the CVSD. Also provided by this module are the reference frequency inputs to the digital demodulator and the transmit clock.

The WCCS synthesizer is an indirect, single-loop design, digitally programmable in 100-kHz increments across the frequency range of 318.6 to 389.9 MHz, supporting a 340- to 389.9-MHz operating range (with the L.O. signal 21.4 MHz below the received RF). Absolute frequency is within  $\pm 2$  KHz due to the use of a self-contained TCXO at 4.8 MHz, designed specifically to tolerate extreme shock. The input frequency designations are received in a BCD format from the frequency programming module.



**Figure 16-12. Synthesizer module**

The transmitted audio binary FSK (FM) frequency modulation is accomplished by applying the digital data stream directly to the synthesizer loop. Incidental FM is less than 1.3 kHz peak, worst-case. Intersymbol interference under wide-band modulation is held to less than  $\pm 15$  percent across the transmitted band.

Operating voltages are internally derived from the battery input with a high degree of regulation. An elevated voltage (+22 V) is generated and used internally to service the

Voltage-Controlled Oscillator (VCO) that is tuning voltage range, as well as being supplied to the receiver module for filter tuning. A band-gap reference voltage derived within the low voltage regulator (+5.2 V) is used by low-level analog circuitry in the loop filter/modulation circuit.

As defined by the module use, in the transmit or receive stream, the synthesizer output frequency will occur at either the Transmitter (TX) or the Receive (RX) buffer output and also at the loop buffer output of the VCO/buffer hybrid. The loop return signal is applied to the digital synthesizer chip, where it undergoes first a fixed frequency division (divide-by-3), then a controlled frequency division (3186 to 3899), resulting in a closed-loop output frequency of 33-1/3 kHz, which is compared in a phase-frequency detector circuit on that chip to a reference signal derived from the 4.8-MHz clock.

The phase detector output is processed through the loop filter/modulator circuit to provide integration, low-pass and notch filtering, and voltage scaling to tune the VCO over its required frequency range. The loop bandwidth supports a TX/RX switching time of 10 milliseconds.

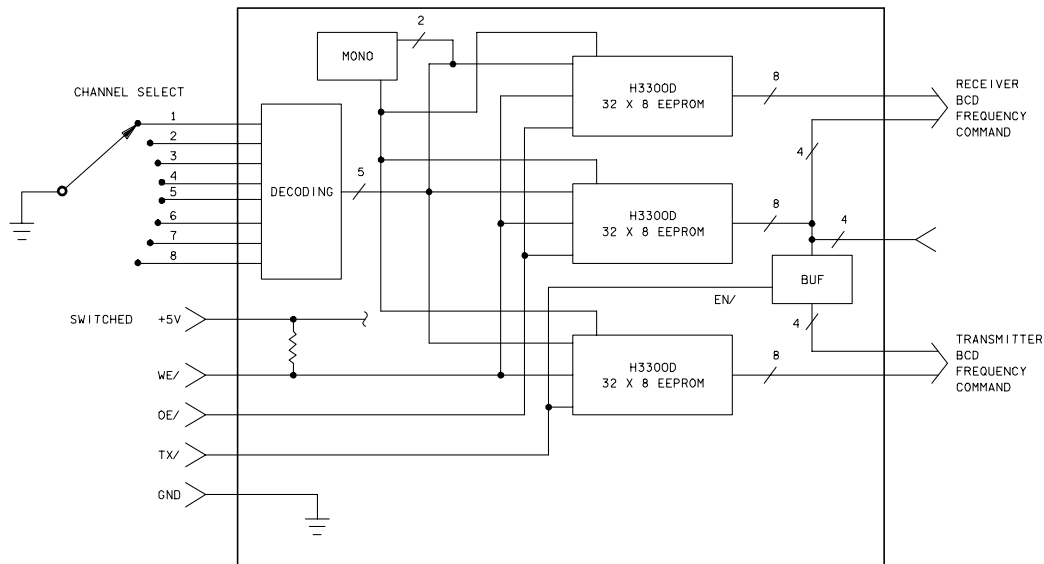
**Table 16-6. Synthesizer module performance**

| Parameter                 | Performance       |
|---------------------------|-------------------|
| Transmit freq. range      | 340 - 389.9 MHz   |
| Receive freq. range       | 318.6 - 368.5 MHz |
| Number of channels        | 500               |
| Channel spacing           | 100 kHz           |
| Transmit/receive spurious | -80 dBc max       |
| Transmit harmonics        | -20 dBc max       |
| FSK modulation            | 32 kbps           |
| FSK modulation index      | 0.7 + 10%         |
| dc power budget           | 320 mW max        |

#### 16.2.4.7 FPM

The FPM (Figure 16-13), used only in the CRUs, stores and maintains in memory frequency information used to program the receive and transmit synthesizer modules in the CRU. The FPM allows operator selection of any of eight preset duplex channels, which will be stored preflight for a predetermined combination of AIUs.

The FPM decodes the setting of the channel select control on eight input lines. The input decoding circuitry identifies the channel command as a five-bit binary word. This word then is used to address two of eight frequency commands, which are stored in Electrically Erasable Programmable Read-Only Memory (EEPROM), and to supply those commands to the receive and transmit synthesizers for duplex operation. The frequency information is passed from the FPM to the synthesizers as 12-bit parallel commands with one 12-bit interface dedicated to the receiver synthesizer and the other 12 dedicated to the transmitter.



186114913, ART. 2

**Figure 16-13. Frequency programming module**

The preflight frequency programming of the EEPROM modules is done at a maintenance facility. The modules are removed from the CRU case and programmed by the Bench Maintenance Equipment (BME) according to the frequency plan defined for the particular flight or SMS training configuration. Refer to Section 16.2.6 for more details on the frequency plans and requirements.

**Table 16-7. Frequency programming module performance**

| Parameter          | Performance              |
|--------------------|--------------------------|
| Frequency range    | 340.0 to 389.9 MHz       |
| Channel separation | 100 kHz                  |
| Output format      | BCD logic to synthesizer |
| Number of channels | Eight full duplex        |
| Memory retention   | Nonvolatile EEPROM       |

#### 16.2.4.8 Audio Summer Module

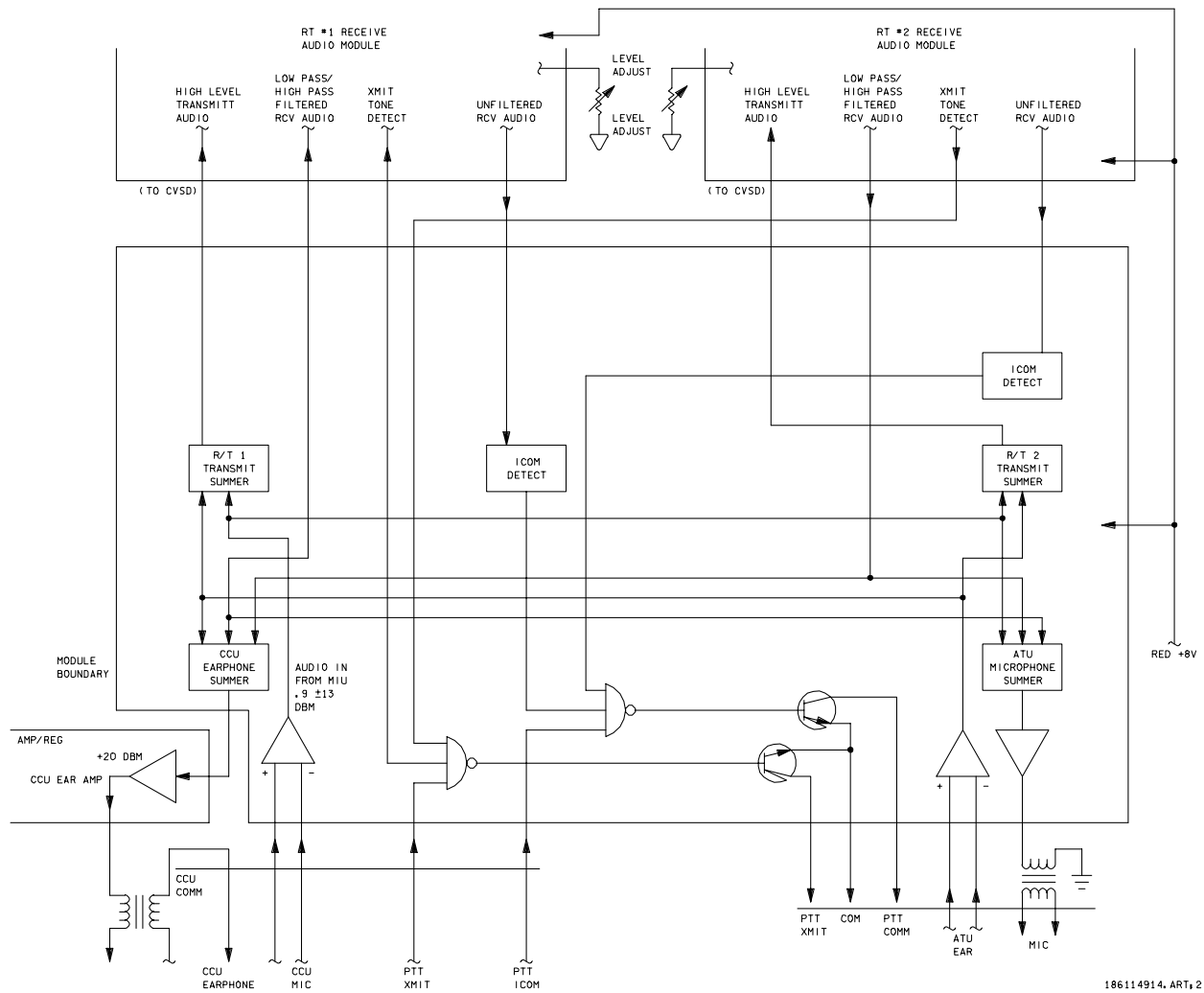
The audio summer/regulator module (Figure 16-14) is used only in the AIU. It interfaces with the CRU via RF and ATU via hardline to provide a conferencing mode of operation and to support downlink communications. Information presented at the external interfaces is directed to the audio modules in R/T 1 and R/T 2 to provide complete crew communication capability.

When a signal is received from a CRU 1, the audio is passed through the audio amp and low-pass filter on the audio module, as in the CRU. However, for the AIU applications the waveform is passed through the sharp rolloff high-pass filter in the tone detector before the receive audio module high-pass filtering. The receive audio module tone detector, when used in the AIU, also monitors this signal for presence of the XMIT subaudible tone from the CRU. The filtered receive audio signal is then passed on to the CCU earphone summer and R/T 2 transmit summer for conferencing and transmission to the second CRU.

Unfiltered audio (that does not pass through the high-pass filter) is also sent to the tone decoder on the audio summer module proper to decode the presence of the ICOM subaudio tone. When a detect occurs from either R/T 1 or R/T 2, the control signal is then passed on to the ATU. The tone detector used in the audio summer module is the same Integrated Circuit (IC) used in the receive audio module tone generator/detector used in a detect only mode. For AIU applications, the tone generator on the audio module is turned off.

After being summed with the audio from the other receiver, the ATU, or the CCU port, the audio signal is sent to the transmit high-level input (directly to the CVSD) for transmission to the CRU. Proper gain for the CCU audio output earphone signal is provided by the amplifier/regulator module.

Transmit audio from the HIU (CCU connector) is first single-ended through a balanced to single-ended converter and injected into the summing amplifier. The dynamic range of the HIU microphone signal is limited to +13, -9 dB so it is not required to first pass it through an AGC, as the CVSD can handle such signal levels.

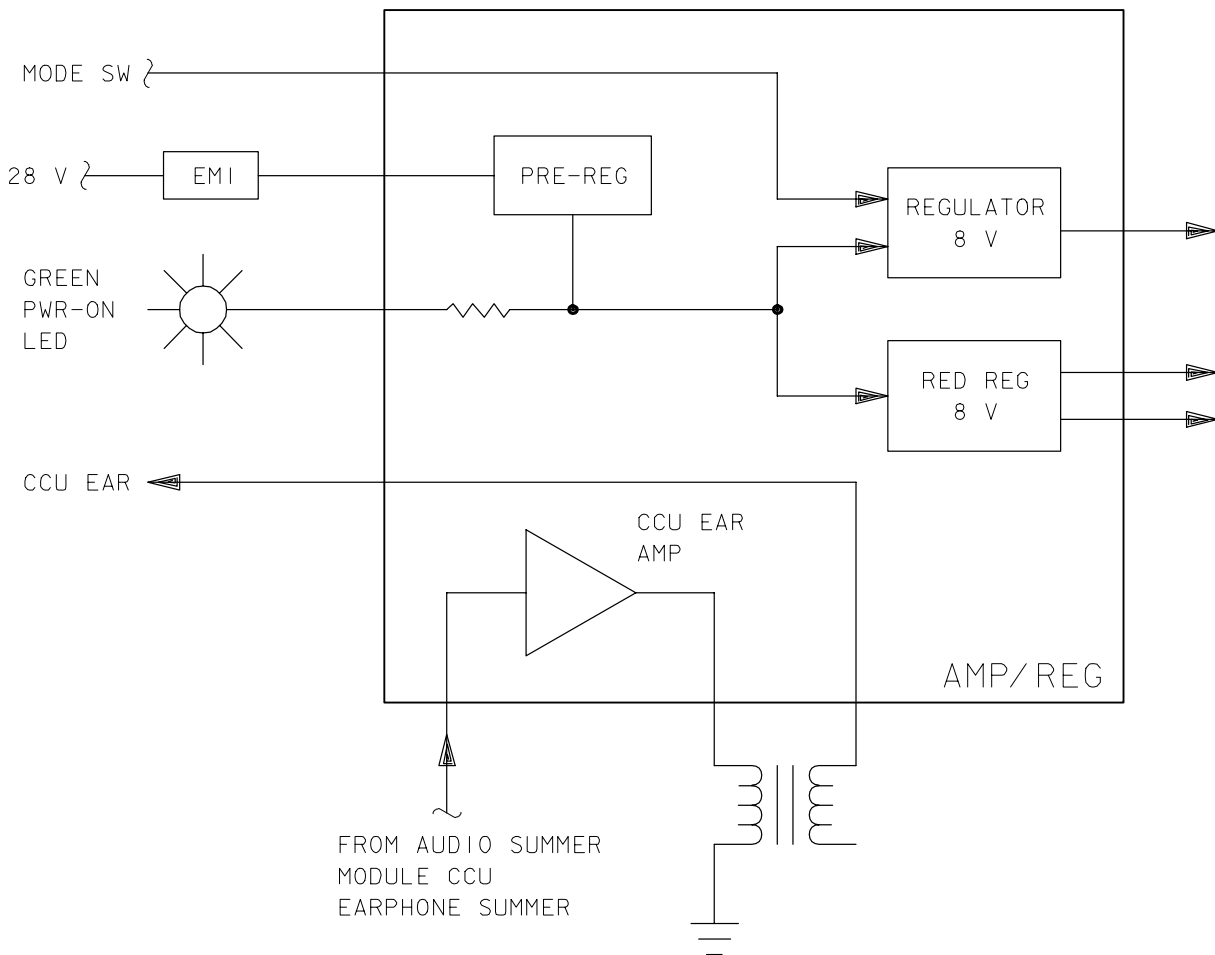


186114914, ART. 2

**Figure 16-14. Audio summer module block diagram**

### 16.2.4.9 Amplifier/Regulator Module

The amplifier/regulator module (Figure 16-15) provides dc-dc regulation and isolation from the 28 V orbiter power down to 12 V dc. The 12 V is then converted to both red and black 8-V module power supply, as required by security for the COMSEC. The module also provides amplification of the summed audio for the CCU earphone.



186114915. ART 2

**Figure 16-15. Amplifier/regulator module**

Supply regulation and isolation from the 28-V dc line is accomplished through the use of a preregulator (off the module) and a set of two on card regulators to generate the +8V black. R/T 1 and R/T 2 regulated power and the 8 V red regulator. Proper TEMPEST (Air Force security program) design is achieved by using separate regulators for the black and red portions of the AIU. Current ripple that passes through the red 8-V regulator will result in minimal audio ripple on the 12-V supply as the output impedance of the regulator is 20 milliohms over the audio range. This ripple is further attenuated by the load regulation of the black +8 V regulator to meet the TEMPEST requirements. Maximum supply current for the entire AIU unit is 510 milliamps.

#### 16.2.4.10 Crypto and Plain Text Modules

The crypto module for WCCS provides the encrypt/decrypt functions of 32-kb/s data stream and provides the required TEMPEST protection needed to handle secret level traffic. The module uses the KGV-99/TSEC encryption IC. The IC is a low-power CMOS encryption chip developed by NASA as the algorithm source. This device

operates without the need for a lengthy preamble at the beginning of each transmission and quickly and automatically resynchronizes following a loss of receive signal. The module contains the necessary circuitry to verify proper functionality of the encryption process and provides an alarm flag to disable transmissions when any process error occurs or when the variable is zeroized. It accepts key variable data from a KYK-13 fill device. An adaptor cable having an initiate button is used to connect the KYK-13 to the AIU/ CRU to be loaded.

The crypto module operates from the main power of the CRU or AIU and provides its own internal regulation of all voltages to maintain isolation. During periods when the CRU battery pack is being changed or when the unit is turned off, the key variable is retained by allowing certain circuits to be powered by either the main battery directly or by the small Lithium keep-alive battery that is case-mounted in both the AIU and the CRU. This eliminates the need for large capacitors to store energy sufficient to power the crypto module and the possible risk of loss of variable. As an additional benefit, this method of variable retention will allow loading variables into all CRUs, including those spares to be stowed without main batteries for later use. Also, this allows the AIU to be disconnected from ATU power.

The crypto module can be removed from the CRU and replaced with the PTI module for nonsecure transmissions. The PTI module has no active devices onboard, as it serves to only route the clear digitized audio to the point normally fed by the particular crypto module. This method of switching to clear operation minimizes the problems of TEMPEST protection otherwise required if a switch function were placed around the crypto module. The procedure to reconfigure the WCCS from encrypted to clear, or the reverse, is to remove the present module and replace it with the other type, as they both reside in the same plug.

### **16.2.5 Power**

The CRU power is supplied by two lithium (Li)-Bromine Complex (BCX) C cells assembled into a battery pack (Figure 16-16). The battery nominally provides 35 hours of operational power.

The receive audio circuitry includes a low battery indicator circuit which monitors battery voltage and senses when the voltage drops to  $6.2 \pm 0.325$  volts. A drop below this level causes the battery sensor to introduce a beep tone into the receive audio path. The beep tone has a nominal level of -21 dB relative to the receive audio level and a nominal 1-kHz frequency with a duty cycle of 10 percent and a 1.3-second rate.

The cells consist of a Li anode and a catholyte of thionyl chloride (SOC1) with BCX reacting on an inert carbon cathode to generate voltage. The cells have a 2-year shelf life.

The battery case is the same external case and slide assembly that was previously used with the zinc-air cells. The case was designed by a NASA subsystem engineer, and internal modifications have been made to accommodate the Li-BCX C cells. The case consists of 12 nonfunctional air holes on 4 of 6 sides. The fifth side consists of a



Velcro patch and labels showing the shelf life dates of the cells and the serial number of the assembled unit. The slide guide which attaches to the CRU and makes the electrical connection is located on the last side.

The assembled battery (SED33103846-709) contains two Li-BCX C cells connected in series and protected by a 1.5-amp fuse, 162° F thermofuse, parallel bypass diodes, and an internal cell 4-amp fuse (Figure 16-16).

**DUE TO THE FAILURE MODE OF AN INTERNAL CELL SHORT THAT COULD RESULT IN VENTING AND/OR EXPLOSION, THE BATTERY IS DEFINED AT CRIT 1/1 AND A WAIVER IS REQUIRED.**

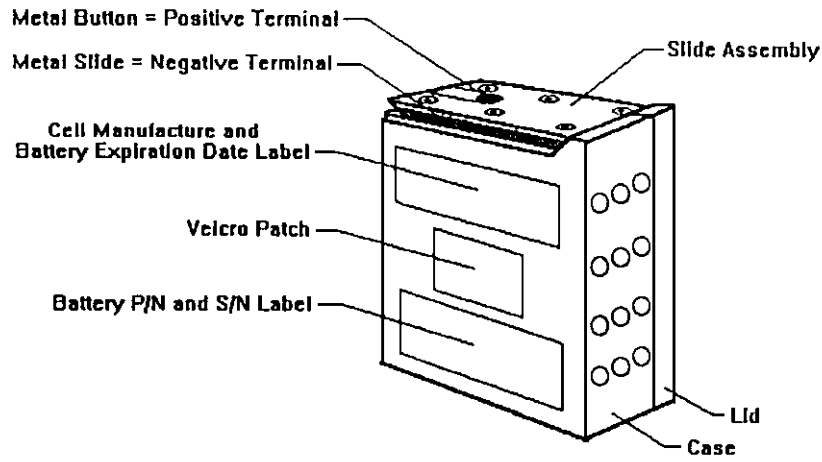
The following cell design features and manufacturing tests minimize the failure mode:

- A. Electrodes are checked for burrs and misalignment, and the fiberglass separator material between the positive and negative electrodes insulates against internal shorts.
- B. The stainless steel cell case is designed to contain cell contents without leakage up to 30° F; the maximum operating temperature is limited to 162° F by the thermofuse.
- C. All cells per lot are made from a common batch of materials within four consecutive calendar days.
- D. X-ray inspection, high temperature tolerance, visual, and open circuit voltage tests are completed on 100 percent of cell lot.
- E. Vibration, capacity discharge, short circuit tolerance, and high temperature exposure tests are completed on lot samples.

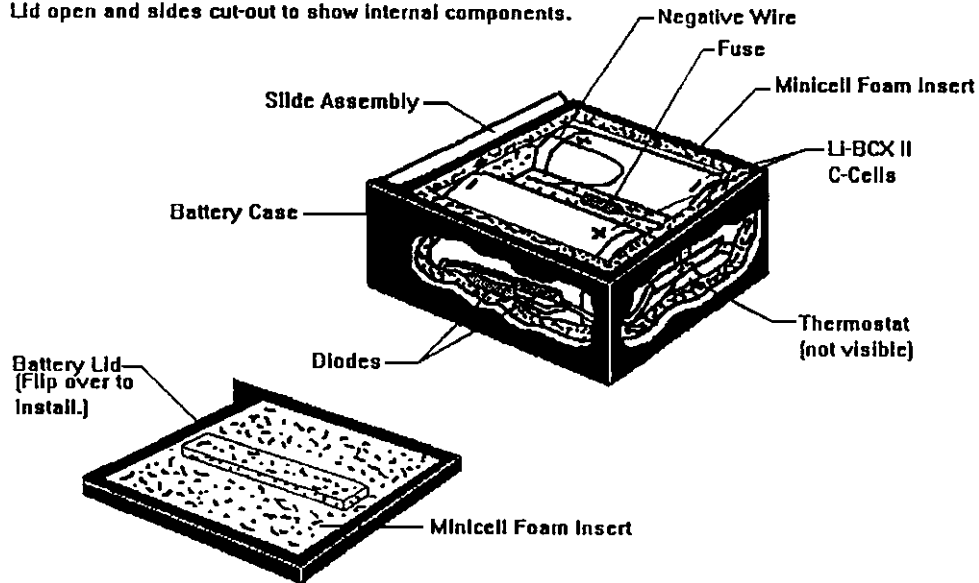
No failures have been reported in nearly 1000 Li-BCX cells flown on the shuttle, over 4000 cells tested at JSC, and over 2 million cells manufactured.

The expected battery performance is summarized as follows (Figure 16-17). The initial battery open circuit voltage is approximately 7.8 volts with a loaded voltage of about 7.5 volts when initially placed on the radio. Within 5 to 6 hours, the voltage stabilizes to 6.5-6.8 volts for the majority of the discharge. After 35 hours, the battery voltage begins to drop off to a 6.2-volt cutoff. On a radio with a high setting for the low battery voltage beep, it may be possible to receive up to 5 hours of additional operation from the battery after the beeping starts until the voltage is too low to operate the radio.

WCCS BATTERY EXTERNAL CASE



LI-BCX WCCS BATTERY  
Lid open and sides cut-out to show internal components.



Schematic

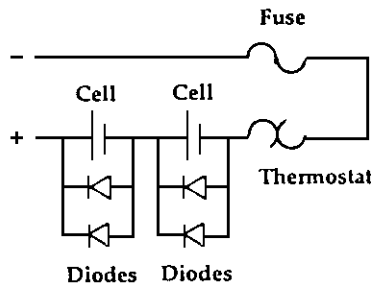
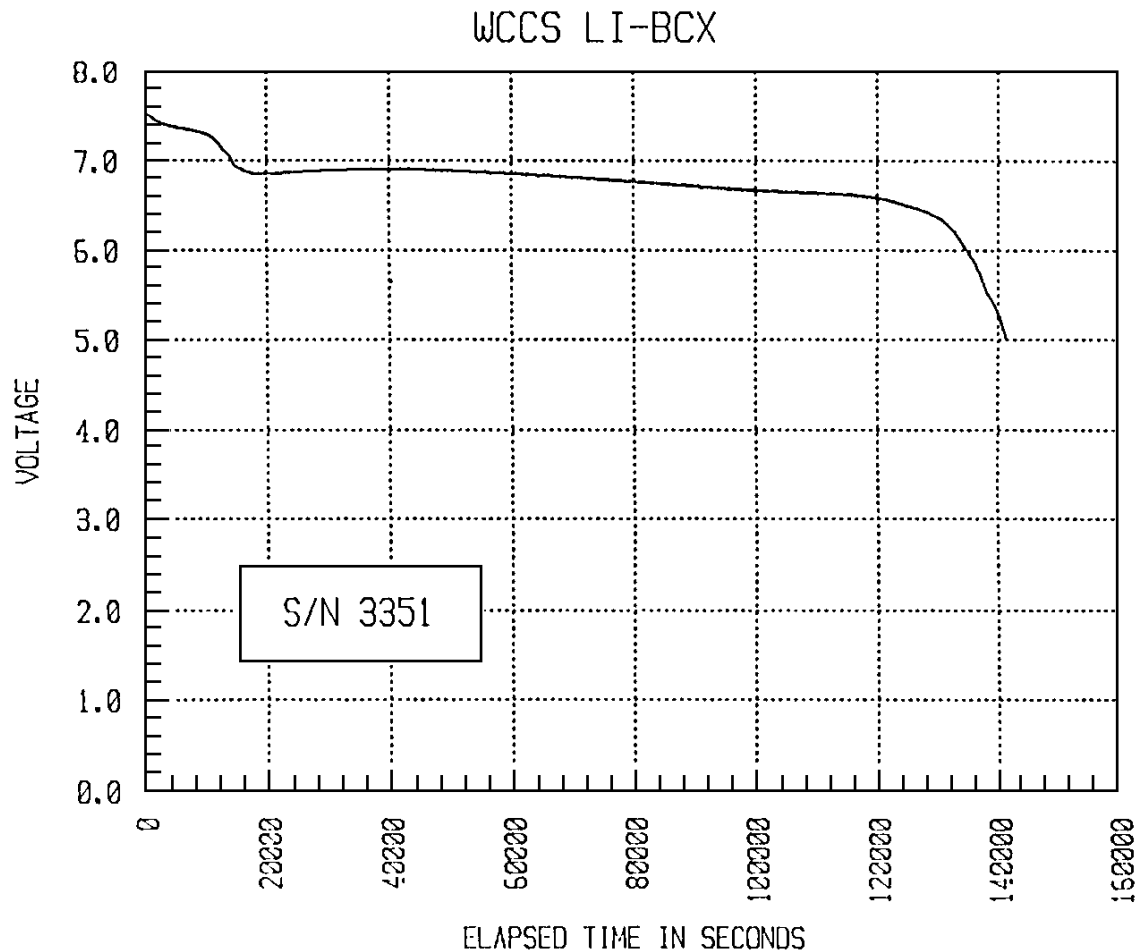


Figure 16-16. CRU battery pack



**Figure 16-17. Battery discharge curve**

The lithium chemistry has side reactions that could build a passivation layer inside the cell. This layer may form if a battery is partially used then not used again for several days. The delivered voltage will be lowered when use is resumed; however, the application of a load will “burn through” the passivation layer within seconds or minutes, and the normal operating voltage will be restored.

Operational notes:

- A. Remove battery only for use as need arises.
  - 1. No activation time is required.
  - 2. Unused batteries can be reflown.
- B. Remove and discard piece of Kapton tape covering the slide.
- C. The CRU should always be powered OFF when loading a battery.
- D. The battery slide mates with the CRU guide when the battery is attached to the radio. Variance in the width of the slide or guide affects the fit of the battery to the

CRU. Some battery-radio combinations may be too tight, which may be relieved by trying another battery.

- E. Turn off CRU when not in use to conserve battery power.
- F. In response to low-voltage beep from CRU, remove battery, place in Ziplock bag, and restow bagged battery in locker.
- G. The number of batteries flown is a function of crew size and mission duration. Check the flight-specific Reference Data book for actual number. See Table 16-8.
- H. During missions, the Mission Evaluation Room (MER) provides support through the Propulsion/Power group.

**Table 16-8. Stowage matrix for wireless crew communications system  
Li-BCX battery (P/N SED33103846-709)**

| Mission duration<br>[days] | Batteries required |               |               |
|----------------------------|--------------------|---------------|---------------|
|                            | Crew size - 5      | Crew size - 6 | Crew size - 7 |
| 5                          | 16                 | 19            | 22            |
| 6                          | 16                 | 19            | 22            |
| 7                          | 21                 | 25            | 29            |
| 8                          | 21                 | 25            | 29            |
| 9                          | 26                 | 31            | 36            |
| 10                         | 26                 | 31            | 36            |
| 11                         | 31                 | 37            | 43            |
| 12                         | 31                 | 37            | 43            |
| 13                         | 36                 | 43            | 50            |
| 14                         | 41                 | 49            | 57            |
| 15                         | 41                 | 49            | 57            |

Notes:

1. Assumes 18 hours/mission day.
2. Based on 35 hours/battery to a 6.2-V cutoff at 160-mA constant current.
3. For 2-day contingency, use row corresponding to specified mission duration +2 days. Example: For a specified 13-day mission with 2-day contingency, determine battery stowage requirements from the row for a mission duration of 15 days.

### 16.2.6 Frequency Plan Considerations

For the proper wireless comm performance, a frequency plan must be developed to guard against the effects of

- A. Transmitter to transmitter intermodulation within each AIU. Since two RF signals are radiated from each AIU, intermodulation components produced by the imperfectly linear output amplifier can lead to spurious output signals. A properly designed frequency plan will not allow the spurious outputs to fall on top of other designated channels.
- B. Transmitter-to-transmitter intermodulation between CRUs. Since the path loss between CRUs can be as tight as -20 dB, intermodulation components can be produced with such CRU transmitter-to-transmitter coupling and an imperfectly linear output amplifier. This intermodulation process is often referred to as “back-intermodulation.”
- C. AIU transmitter-to-CRU transmitter intermodulation. The path loss coupling can also be as tight as -20 dB, in this case. This back intermodulation can also lead to spurious components on top of other designated channels.
- D. Transmitter intermodulation between different AIUs. The coupling between the transmitters of different AIUs is estimated to correspond to -40 dB of path loss. The intermodulation components, in this instance, are likely to be below detectability.
- E. Desensitization of a CRU receiver when an interfering CRU transmitter is brought into close coupling (-20 dB path loss) with the target CRU receiver.
- F. Desensitization of a CRU receiver when the CRU is brought into close coupling (-20 dB path loss) with an interfering AIU transmitter.
- G. Desensitization of an AIU receiver when an interfering CRU transmitter is closely coupled.
- H. Desensitization of an AIU or CRU receiver by its own duplexed transmitter.
- I. Production of third order on-frequency intermodulation components within the AIU or CRU receiver front end when receiving two interfering signals, as well as the desired signal. The possibly deleterious effects of this intermodulation process are avoided by the same frequency plan that avoids undesirable intermodulation between transmitters.
- J. Frequency spacings between channel assignments of 0.8, 4.8, and 14.4 MHz are to be avoided due to discrete spurious transmitter output at those spacings.
- K. Frequency spacings between channels of 21.4 MHz are to be avoided due to possible interference by low-level receiver local oscillator leakage radiation.

Two frequency plans which meet the requirements outlined above are listed in Table 16-9 and Table 16-10. The first plan was constructed for use on non-Spacelab flights and for use while in the Mission Operations Directorate (MOD) training facilities; building 9 Crew Compartment Trainer, building 4 Single System Trainer, and the building 39 Spacelab mockup. The other plan was developed for use on flights with a Spacelab, requiring two wall units in the lab.

**Table 16-9. Flight and MOD training frequency plan\***

| <b>Channel designator</b> | <b>CRU mode</b> | <b>AIU mode</b> | <b>Frequency (MHz)</b> |
|---------------------------|-----------------|-----------------|------------------------|
| A1                        | Receive         | Transmit        | 340.7                  |
| A1                        | Transmit        | Receive         | 374.7                  |
| A2                        | Receive         | Transmit        | 343.6                  |
| A2                        | Transmit        | Receive         | 376.3                  |
| B1                        | Receive         | Transmit        | 345.8                  |
| B1                        | Transmit        | Receive         | 377.7                  |
| B2                        | Receive         | Transmit        | 347.2                  |
| B2                        | Transmit        | Receive         | 380.0                  |
| C1                        | Receive         | Transmit        | 349.3                  |
| C1                        | Transmit        | Receive         | 383.4                  |
| C2                        | Receive         | Transmit        | 351.0                  |
| C2                        | Transmit        | Receive         | 386.1                  |
| D1                        | Receive         | Transmit        | 359.7                  |
| D1                        | Transmit        | Receive         | 388.3                  |
| D2                        | Receive         | Transmit        | 372.7                  |
| D2                        | Transmit        | Receive         | 389.6                  |

\*Building 9 Crew Compartment Trainer.  
Building 4 Single System Trainer.  
Building 39 Spacelab mockup.

**Table 16-10. Spacelab flight frequency plan**

| Channel designator* | Orbiter CRU mode | Spacelab CRU mode | AIU      | Frequency (MHz) |
|---------------------|------------------|-------------------|----------|-----------------|
| A1                  | Receive          | Receive           | Transmit | 340.7           |
| A1                  | Transmit         | Transmit          | Receive  | 372.7           |
| A2                  | Receive          |                   | Transmit | 343.6           |
| A2                  | Transmit         |                   | Receive  | 373.0           |
| B1                  | Receive          | Receive           | Transmit | 345.8           |
| B1                  | Transmit         | Transmit          | Receive  | 374.7           |
| B2                  | Receive          |                   | Transmit | 347.0           |
| B2                  | Transmit         |                   | Receive  | 376.3           |
| C1                  | Receive          | Receive           | Transmit | 347.2           |
| C1                  | Transmit         | Transmit          | Receive  | 380.0           |
| C2                  | Receive          | Receive           | Transmit | 348.9           |
| C2                  | Transmit         | Transmit          | Receive  | 385.5           |
| D1                  | Receive          | Receive           | Transmit | 349.3           |
| D1                  | Transmit         | Transmit          | Receive  | 386.1           |
| D2                  |                  | Receive           | Transmit | 349.9           |
| D2                  |                  | Transmit          | Receive  | 388.3           |
| E1                  | Receive          | Receive           | Transmit | 351.0           |
| E1                  | Transmit         | Transmit          | Receive  | 389.2           |
| E2                  |                  | Receive           | Transmit | 359.7           |
| E2                  |                  | Transmit          | Receive  | 389.6           |

\*AIUs A, B, and C are orbiter AIUs; D and E are Spacelab AIUs.

The frequency plan used for nonsecure training in the Shuttle Mission Simulator (SMS) fixed base simulator is shown in Table 16-11. This allows for three AIUs to be installed, with a fourth available as a backup. A second allocation of frequencies is shown in Table 16-12. These are provided for operations in the SMS motion base simultaneously with wireless audio operations in the fixed base.

Consideration has been given to a red frequency plan, shown in Table 16-13, to be used simultaneously with either of the other two SMS plans. This approach includes a complete set of hardware which is marked as red and installed for secure SMS training only. The reason for the third set of hardware is to save wear on the COMSEC modules and sockets, as well as making the security procedures more simple and reducing the chance for compromising errors.

**Table 16-11. SMS fixed base frequency plan**

| <b>Channel designator</b> | <b>Orbiter CRU mode</b> | <b>Spacelab CRU mode</b> | <b>Frequency (MHz)</b> |
|---------------------------|-------------------------|--------------------------|------------------------|
| A1                        | Receive                 | Transmit                 | 340.7                  |
| A1                        | Transmit                | Receive                  | 372.7                  |
| A2                        | Receive                 | Transmit                 | 343.6                  |
| A2                        | Transmit                | Receive                  | 374.7                  |
| B1                        | Receive                 | Transmit                 | 345.8                  |
| B1                        | Transmit                | Receive                  | 377.7                  |
| B2                        | Receive                 | Transmit                 | 348.9                  |
| B2                        | Transmit                | Receive                  | 383.4                  |
| C1                        | Receive                 | Transmit                 | 349.3                  |
| C1                        | Transmit                | Receive                  | 386.1                  |
| C2                        | Receive                 | Transmit                 | 351.0                  |
| C2                        | Transmit                | Receive                  | 389.2                  |
| D1*                       | Receive                 | Transmit                 | 350.3                  |
| D1*                       | Transmit                | Receive                  | 375.9                  |
| D2*                       | Receive                 | Transmit                 | 352.3                  |
| D2*                       | Transmit                | Receive                  | 383.2                  |

\*These frequencies are assigned for the SMS/SLS backup AIU. CRU D1 and D2 channels are used only when the backup AIU is required.



**Table 16-12. SMS motion base plan**

| <b>Channel designator</b> | <b>CRU mode</b> | <b>AIU mode</b> | <b>Frequency (MHz)</b> |
|---------------------------|-----------------|-----------------|------------------------|
| A1                        | Receive         | Transmit        | 340.5                  |
| A1                        | Transmit        | Receive         | 374.6                  |
| A2                        | Receive         | Transmit        | 341.1                  |
| A2                        | Transmit        | Receive         | 375.6                  |
| B1                        | Receive         | Transmit        | 341.6                  |
| B1                        | Transmit        | Receive         | 375.7                  |
| B2                        | Receive         | Transmit        | 367.3                  |
| B2                        | Transmit        | Receive         | 383.1                  |
| C1                        | Receive         | Transmit        | 368.5                  |
| C1                        | Transmit        | Receive         | 385.2                  |
| C2                        | Receive         | Transmit        | 372.8                  |
| C2                        | Transmit        | Receive         | 388.9                  |
| D1*                       | Receive         | Transmit        | 350.3                  |
| D1*                       | Transmit        | Receive         | 375.9                  |
| D2*                       | Receive         | Transmit        | 352.3                  |
| D2*                       | Transmit        | Receive         | 383.2                  |

\*These frequencies are assigned for the SMS/SLS backup AIU. CRU D1 and D2 channels are used only when the backup AIU is required.

**Table 16-13. SMS red plan**

| <b>Channel designator</b> | <b>CRU mode</b> | <b>AIU mode</b> | <b>Frequency (MHz)</b> |
|---------------------------|-----------------|-----------------|------------------------|
| A1                        | Receive         | Transmit        | 342.9                  |
| A1                        | Transmit        | Receive         | 373.0                  |
| A2                        | Receive         | Transmit        | 343.9                  |
| A2                        | Transmit        | Receive         | 376.3                  |
| B1                        | Receive         | Transmit        | 347.0                  |
| B1                        | Transmit        | Receive         | 380.0                  |
| B2                        | Receive         | Transmit        | 349.3                  |
| B2                        | Transmit        | Receive         | 385.5                  |
| C1                        | Receive         | Transmit        | 349.9                  |
| C1                        | Transmit        | Receive         | 388.3                  |
| C2                        | Receive         | Transmit        | 359.7                  |
| C2                        | Transmit        | Receive         | 389.6                  |
| D1*                       | Receive         | Transmit        | 350.3                  |
| D1*                       | Transmit        | Receive         | 375.9                  |
| D2*                       | Receive         | Transmit        | 352.3                  |
| D2*                       | Transmit        | Receive         | 383.2                  |

\*These frequencies are assigned for the SMS/SLS backup AIU. CRU D1 and D2 channels are used only when the backup AIU is required.

The frequency plan to be used in the SLS is shown in Table 16-14.

**Table 16-14. SLS plan**

| Channel designator | CRU mode | AIU mode | Frequency (MHz) |
|--------------------|----------|----------|-----------------|
| A1                 | Receive  | Transmit | 346.0           |
| A1                 | Transmit | Receive  | 360.6           |
| A2                 | Receive  | Transmit | 352.2           |
| A2                 | Transmit | Receive  | 367.0           |
| B1                 | Receive  | Transmit | 352.5           |
| B1                 | Transmit | Receive  | 377.4           |
| B2                 | Receive  | Transmit | 355.4           |
| B2                 | Transmit | Receive  | 389.3           |
| C1*                | Receive  |          | 350.3           |
| C1*                | Transmit |          | 375.9           |
| C2*                | Receive  |          | 352.3           |
| C2*                | Transmit |          | 383.2           |
| D1*                | Receive  | Transmit | 350.3           |
| D1*                | Transmit | Receive  | 375.9           |
| D2*                | Receive  | Transmit | 352.3           |
| D2*                | Transmit | Receive  | 383.2           |

\*These frequencies are assigned for the SMS/SLS backup AIU. CRU D1 and D2 channels are used only when the backup AIU is required.

### 16.3 PHYSICAL DESCRIPTION

#### A. Size

CRU 7.75 by 3.50 by 1.62 inches with battery less antenna/controls

AIU 7.13 by 5.50 by 1.62 inches less antenna/controls/mounting feet

#### B. Weight CRU 2.5 lb, AIU 4 lb

### 16.4 INSTALLATION

#### 16.4.1 Locations

AIU A is located below panel L5; when in use, it is connected to L5, the CDRs comm panel. AIU B is mounted below its comm panel, MS comm panel A11. The middeck AIU C is ceiling mounted near MO52J and is connected to the middeck comm panel

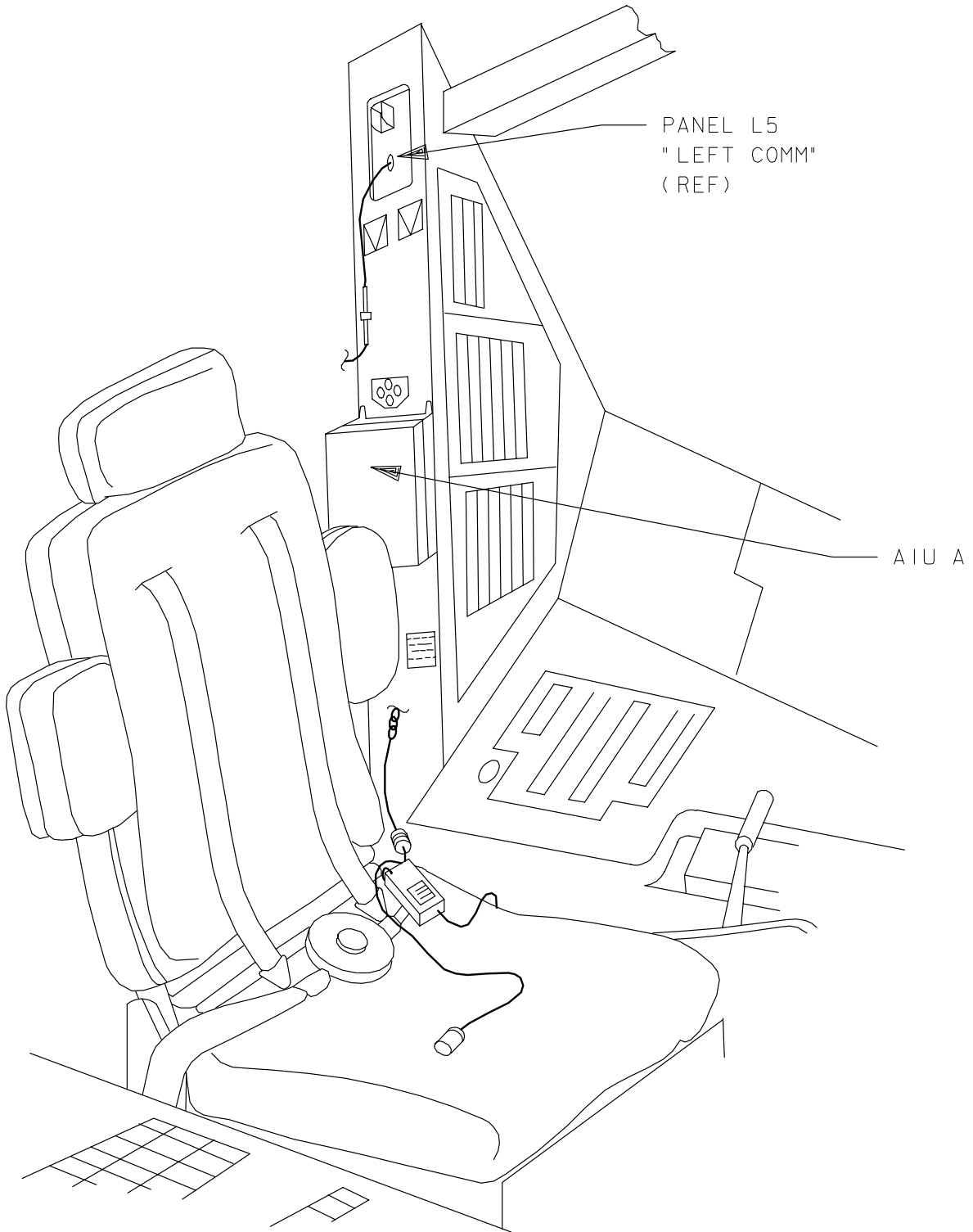
through the multiple headset adapter. The Spacelab AIU D and E locations are mission-dependent. (See Figure 16-18, Figure 16-19, and Figure 16-20.)

#### 16.4.2 Cooling

All components within the WCCS Line Replaceable Units (LRUs) rely on passive cooling except the two regulators and the CCU ear amp, which are considered probable hot spots in the AIU. To accommodate these components, the amp/reg module is located close to AIU case, as shown by the internal view of the Station Set Handbook (SSHB) WCCS AIU drawing 16.2-1. This view shows that the module is mounted next to an externally mounted heat sink, which provides cooling for the three mentioned components.

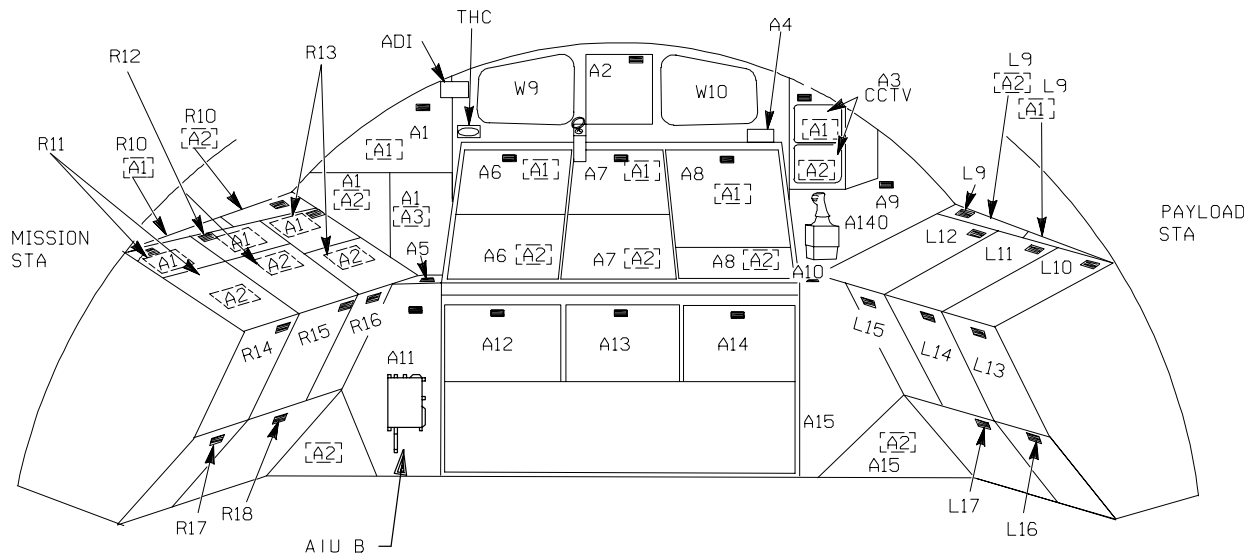
#### 16.5 REFERENCES

- A. NASA Wireless Crew Communications System Critical Design Review, GTE Government Systems Corporation, July 30 - August 1, 1986.
- B. WCCS Wireless Crew Communications System Product Information, GTE Government Systems Corporation, 1986.
- C. Proposal for a Wireless Crew Communications Systems Volume 1 Technical and Management, GTE Government Systems Corporation, March 5, 1984.
- D. Space Shuttle Wireless Crew Communications System Frequency Plan, Lockheed Engineering and Management Services Co., Inc., September 1985.
- E. GTE Schematics, 00-1388201, 00-1388301, 02-1388200, 02-1388300, 00-0380321, 00-1388351, 00-1388111, 00-1388141, 00-1388151, 00-1388161, 00-1388171, 00-1388191, 1985.
- F. Interface Control Document, Level III, Shuttle Orbiter Wireless Crew Communications System, ICD-3-0061-15.
- G. Contract End Item Specification, KGV-99/TSEC Module, Department of Defense, July 1986.
- H. Contract End Item Specification, AIU, GTE Government Systems Corporation, November 1985.
- I. Contract End Item Specification, CRU, GTE Government Systems Corporation, November 1985.



186114920. ART# 2

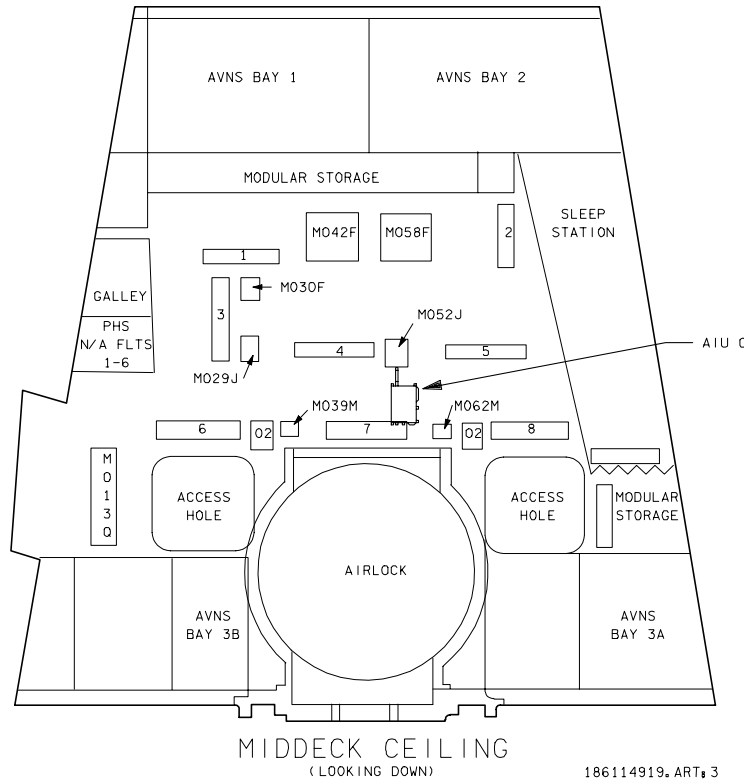
**Figure 16-18. Location of AIU A**



AFT STATION

186114918. ART 2

Figure 16-19. Location of AIU B



186114919. ART 3

Figure 16-20. Location of AIU C

THIS PAGE INTENTIONALLY BLANK

**SECTION 17 - ULTRAHIGH FREQUENCY SYSTEM**  
**CONTENTS**

| <b>Section</b> |   | <b>Page</b> |
|----------------|---|-------------|
| 17.1           | GENERAL .....                                   | 17-1        |
| 17.2           | TRANSCEIVER .....                               | 17-1        |
| 17.3           | RECEIVER .....                                  | 17-14       |
| 17.4           | XMITTER.....                                    | 17-14       |
| 17.5           | POWER AMP .....                                 | 17-14       |
| 17.6           | UHF ACCESS.....                                 | 17-15       |
| 17.7           | TELEMETRY .....                                 | 17-15       |
| 17.8           | ANTENNA .....                                   | 17-15       |
| 17.9           | ORBITER UHF TRANSCEIVER POWER CONSUMPTION ..... | 17-16       |

**TABLES**

| <b>Table</b> |  |       |
|--------------|--|-------|
| 17-1         | Orbiter transceiver modes .....        | 17-3  |
| 17-2         | UHF transceiver control functions..... | 17-5  |
| 17-3         | Mode select logic states .....         | 17-6  |
| 17-4         | UHF receiver operation.....            | 17-14 |

**FIGURES**

| <b>Figure</b> |  |       |
|---------------|--|-------|
| 17-1          | UHF transceiver controls .....               | 17-2  |
| 17-2          | UHF control logic .....                      | 17-4  |
| 17-3          | Location of UHF channel enable switches..... | 17-15 |



THIS PAGE INTENTIONALLY BLANK

## SECTION 17 ULTRAHIGH FREQUENCY SYSTEM

### 17.1 GENERAL

The Ultrahigh Frequency (UHF) Air Traffic Control (ATC) system provides voice communications between the orbiter and supporting ground sites during the ascent and entry phases of the flight. Another UHF system that is used for Extravehicular Activity (EVA) and rendezvous communications is called the Space-to-Space Orbiter Radio (SSOR). A small amount of information about the SSOR is covered in this brief; a more detailed description can be found in Systems Brief 19, Space-to-Space Communications System.

The orbiter UHF ATC radio has four receivers: 296.8 MHz, 259.7 MHz, 279.0 MHz (not used), and 243.0 MHz. The radio has three transmitters: 296.8, 259.7, and 243.0. A description of the UHF ATC radio can be found in the Space Shuttle Systems Handbook (SSSH) drawing 17.9.

### 17.2 TRANSCEIVER

The transceiver is located in avionics bay 3A. It is powered constantly by two isolated buses, MNA and MNC. In the event of a bus loss, the power supply is designed to operate efficiently on one bus. High power output is 10 W; low power mode is 0.25 W.

#### A. Power supply

MNA and MNC are brought into the UHF radio through two isolated power converters that, in turn, power the modules associated with the transceiver. MNA power converter supplies the 10-W power amp and all other transceiver functions, while MNC only supplies the transceiver functions excluding the power amp. If MNA fails, the 10-W power amp is automatically inhibited, changing the UHF transceiver into a low power mode. If MNC fails, then all functions are retained, including the power amp.

Transmit (XMIT) range of the orbiter radio in low power is 90 miles and in high power, 350 miles.

#### B. Logic and controls

On panel O6, control of the UHF and the SSOR is accomplished. These controls are located on the Commander's (CDR's) overhead panel. Four two-position toggle switches, labeled SPLX/EVA XMIT FREQ, SPLX/EVA PWR AMPL, SPLX SQUELCH, and EVA STRING, and a five-position rotary switch, labeled UHF MODE, are shown in Figure 17-1.

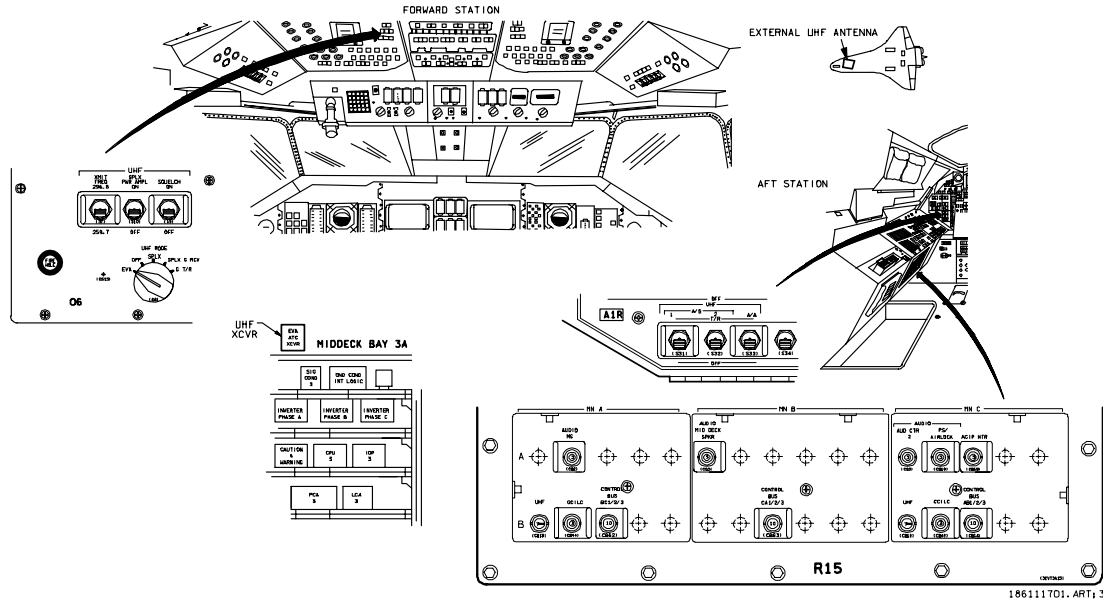


Figure 17-1. UHF transceiver controls

**SPLX/EVA XMIT FREQ** - Permits selection of one of two UHF frequencies, 296.8 MHz or 259.7 MHz, for external transmission in simplex. If the EVA mode is selected on the rotary switch, XMIT FREQ switch permits the selection of one of the SSOR frequencies, 417.1 MHz or 414.2 MHz.

**SPLX/EVA PWR AMPL** - This switch enables or disables the 10-W power amp for any of the three frequencies used for transmission in simplex and guard transmit/receiver (G T/R). If the EVA mode is selected on the rotary switch, this switch enables (ON) or disables (OFF) the 1.44-W power amp for the SSOR.

**SPLX SQUELCH** - Permits selection (ON) or deselection (OFF) of UHF squelch.

**EVA STRING** - Permits selection of one of two strings for SSOR communications.

The MODE switch enables the following:

**EVA** - When operating in the EVA mode the SSOR system is activated; see Section 19 for details on the SSOR system.

**SIMPLEX** - UHF transmissions and receptions are made on the frequency selected.

**SIMPLEX + G RCV** - Same as SIMPLEX, except that reception of UHF guard (243.0 MHz) is possible.

**G T/R** - UHF transmissions and reception are made on guard (243.0 MHz) frequency. UHF guard is the international distress frequency.

**ENCRYPT** - Toggle switch enables (ON) and disables (OFF) encryption of commands over the SSOR system from the orbiter to station.

**IRFM** – To activate the ACCU’s IRFM Key, an ATU must be configured for A/A in Transmit/Receive(activates bit 30) **and** the XMIT pressed. If these two signals are “high” the ACCU switching circuits will activate the IRFM signal, which is sent to the UHF LRU and physically activates the UHF carrier frequency and shifts the simplex to Transmit.

If IRFM is not activated within the ACCU, the UHF will remain in Receive only.

Table 17-1 contains data on orbiter transceiver modes.

**Table 17-1. Orbiter transceiver modes**

|                  |       | EVA  | OFF | SIMPLEX                         | SIMPLEX<br>+G RCV               | GT/R                            |
|------------------|-------|--|-----|---------------------------------|---------------------------------|---------------------------------|
| X<br>M<br>I<br>T | 296.8 | N/A<br>In this mode the<br>SSOR system is<br>activated | OFF | 296.8 MHz AM<br>T/R keyed voice | 296.8 MHz AM<br>T/R keyed voice | 243.0 MHz AM<br>T/R keyed voice |
|                  |       |  |     | Xmit 10 W<br>or 0.25 W          | 243.0 MHz AM<br>rcv voice       | Xmit 10 W<br>or 0.25 W          |
| F<br>R<br>E<br>Q | 259.7 | N/A<br>In this mode the<br>SSOR system is<br>activated | OFF | 259.7 MHz AM<br>T/R keyed voice | 259.7 MHz AM<br>T/R keyed voice | 243.0 MHz AM<br>T/R keyed voice |
|                  |       |  |     | Xmit 10 W<br>or 0.25 W          | 243.0 MHz AM<br>rcv voice       | Xmit 10 W<br>or 0.25 W          |

Figure 17-2 shows the orbiter UHF logic circuitry, and Table 17-2 presents the control logic input and output functions designation and defines the logic status for each function.

Note: The orbiter transceiver receivers are powered on continuously. The logic circuitry is designed to mute the receivers corresponding to the mode and frequency selected.

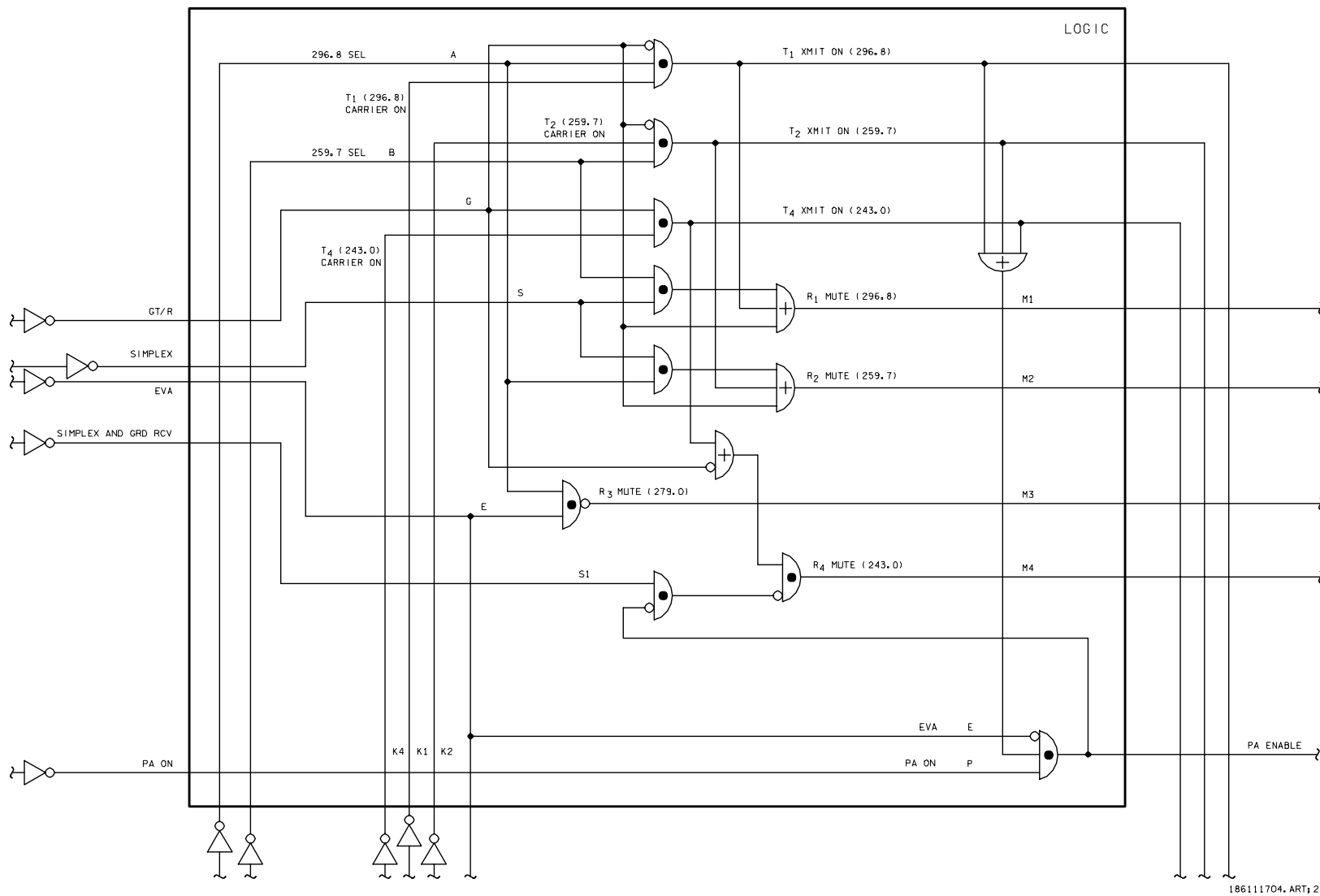


Figure 17-2. UHF control logic

**Table 17-2. UHF transceiver control functions**

| INPUTS                 |                                | OUTPUTS                         |                                  |
|------------------------|--------------------------------|---------------------------------|----------------------------------|
| S6 - UHF MODE          |                                | XMTR KEY                        |                                  |
| G                      | 0 = G T/R                      | T <sub>1</sub>                  | 1 = 296.8 XMTR KEY               |
| S                      | 0 = SIMPLEX OR SIMPLEX + G RCV | T <sub>2</sub>                  | 1 = 259.7 XMTR KEY               |
| E                      | 0 = EVA                        | T <sub>4</sub>                  | 1 = 243.0 XMTR KEY               |
| S1                     | 0 = SIMPLEX + G RCV            | RCVR MUTE                       |                                  |
| S7 - UHF XMIT FREQ     |                                | M <sub>1</sub>                  | 1 = 296.8 RCVR MUTE              |
| A                      | 0 = 296.8                      | M <sub>2</sub>                  | 1 = 259.7 RCVR MUTE              |
| B                      | 0 = 259.7                      | M <sub>3</sub>                  | 1 = 279.0 RCVR MUTE              |
| S9 - UHF SQUELCH       |                                | M <sub>4</sub>                  | 1 = 243.0 RCVR MUTE              |
| Q                      | 1 = ON                         | PWR AMPL                        |                                  |
| S10 - UHF SPLX PWR AMP |                                | P <sub>1</sub>                  | 1 = ENABLE                       |
| P                      | 0 = ON                         | P <sub>0</sub>                  | 1 = SELECT                       |
| PTT KEY (ACCU)         |                                | BIOMED DATA                     |                                  |
| K                      | 0 = ON                         | D                               | 1 = ENABLE                       |
| PTT KEY (ISOLATED)     |                                | XMTR/RCVR - QUADRIplexER SELECT |                                  |
| K <sub>1</sub>         | 0 = T <sub>1</sub> KEY         | K <sub>11</sub>                 | 1 = 296.8 XMTR<br>0 = 296.8 RCVR |
| K <sub>2</sub>         | 0 = T <sub>2</sub> KEY         | K <sub>21</sub>                 | 1 = 259.7 XMTR<br>0 = 259.7 RCVR |
| K <sub>4</sub>         | 0 = T <sub>4</sub> KEY         | K <sub>41</sub>                 | 1 = 243.0 XMTR<br>0 = 243.0 RCVR |
| POWER CIRCUIT BREAKERS |                                |                                 |                                  |
| CB13                   | 0 = 296.8                      |                                 |                                  |
| CB18                   | 0 = 259.7                      |                                 |                                  |
| C                      | 1 = POWER CONVERTERS ON        |                                 |                                  |

Table 17-3 shows the logic states of each mode when selected on panel O6 UHF Mode (S6), SPLX PWR AMP (S10), and XMIT FREQ (S7) switches.

**Table 17-3. Mode select logic states**

| S6 - UHF MODE           | E | S1 | S | G |
|-------------------------|---|----|---|---|
| EVA                     | 0 | 1  | 1 | 1 |
| OFF                     | 0 | 0  | 0 | 0 |
| SIMPLEX                 | 1 | 1  | 0 | 1 |
| SIMPLEX + G RCV         | 1 | 0  | 0 | 1 |
| G T/R                   | 1 | 1  | 1 | 0 |
| S10 UHF<br>SPLX PWR AMP | P |    |   |   |
| PA ON                   | 0 |    |   |   |
| OFF                     | 1 |    |   |   |
| S7 UHF<br>XMIT FREQ     | A | B  |   |   |
| A (296.8)               | 0 | 1  |   |   |
| B (259.7)               | 1 | 0  |   |   |

From Figure 17-2, Table 17-2, and Table 17-3, we can define the following logic output equations.

A. Transmitter key functions ("1" = XMIT)

$$T_1 = G \cdot \bar{K}_1 \cdot \bar{A}$$

$$T_2 = G \cdot \bar{K}_2 \cdot \bar{B}$$

$$T_4 = \bar{G} \cdot \bar{K}_4$$

$$T = T_1 + T_2 + T_4$$

B. RCVR mute functions ("0" = rcv)

$$M_1 = T_1 + \bar{G} + (\bar{B} \cdot \bar{S})$$

$$M_2 = T_2 + \bar{G} + (\bar{A} \cdot \bar{S})$$

$$M_3 = \bar{\bar{A}} \cdot \bar{\bar{E}} = A + E$$

$$M_4 = (T_4 + G) \cdot \left[ \bar{\bar{S}}_1 \cdot (\bar{\bar{E}} \cdot \bar{\bar{P}}) \cdot T \right]$$

C. Power amp functions

$$P_1 = E \cdot \bar{P} \cdot (T_1 + T_2 + T_4)$$

$$P_0 = \bar{K} \cdot E \cdot \bar{P} \cdot (T_1 + T_2 + T_4)$$

D. Quadriplexer XMT/RCV functions

$$RCV_A = \bar{K}_{11} \quad XMT_A = K_{11}$$

$$RCV_B = \bar{K}_{21} \quad XMT_B = K_{21}$$

$$RCV_4 = \bar{K}_{41} \quad XMT_4 = K_{41}$$



The MODE functions are as follows:

Simplex A (296.8) mode

A.  $RCV_A = (CB13 + CB 18) \cdot \overline{M_1} \cdot \overline{K_{11}}$   
(296.8)

B.  $XMIT_A = (CB 18) \cdot G \cdot \overline{K_1} \cdot \overline{A} \cdot K_{11} \cdot P_0$   
(High Pwr)

$P_0 = \overline{K} \cdot E \cdot \overline{P} \cdot (CB 13) \cdot (T_1 + T_2 + T_4)$

C.  $XMT_A = (CB13 + CB 18) \cdot G \cdot \overline{K_1} \cdot \overline{A} \cdot K_1 \cdot \overline{P + E}$   
(Low Pwr)

Simplex B (259.7) mode

A.  $RCV_B = (CB\ 13 + CB\ 18) \cdot \overline{M_2} \cdot K_{21}$   
(259.7)

$\overline{M_2} = \overline{T_2} \cdot G \cdot (\overline{A} \cdot \overline{S})$

B.  $XMITA = (CB\ 18) \cdot G \cdot \overline{K_1} \cdot \overline{B} \cdot K_{21} \cdot P_0$   
259.7  
(High Pwr)

$P_0 = \overline{K} \cdot E \cdot \overline{P} \cdot (CB\ 13) \cdot (T_1 + T_2 + T_4)$

C.  $XMIA = (CB\ 13 + CB\ 18) \cdot G \cdot \overline{K_1} \cdot A \cdot K_1 \cdot \overline{P+E}$   
(Low Pwr)

EVA mode

$$\begin{aligned}
 \text{A. RCV A} &= (\text{CB } 13 + \text{CB } 18) \cdot \overline{M_1} \cdot \overline{K_{11}} \\
 &= (\text{CB } 13 + \text{CB } 18) \cdot \overline{T} \cdot G \cdot \overline{(B \cdot S)}
 \end{aligned}$$

┌─── SIMPLEX B NOT selected  
 └─── G T/R NOT selected  
 └─── 296.8 XMTR NOT keyed

$$\begin{aligned}
 \text{B. XMT A} &= (\text{CB } 13 + \text{CB } 18) \cdot G \cdot \overline{K_1} \cdot \overline{A} \cdot K_{11} \cdot (P + \overline{E}) \\
 \text{296.8} & \\
 \text{(Low Pwr)} &
 \end{aligned}$$

┌─── Pwr amp NOT selected  
 └─── XMTR 1 to quadriplexer  
 └─── 296.8  
 └─── ACCU key  
 └─── Guard NOT selected

$$\begin{aligned}
 \text{C. RCV (B)} &= (\text{CB } 13 + \text{CB } 18) \cdot \overline{M_2} \cdot \overline{K_{21}} \\
 &= (\text{CB } 13 + \text{CB } 18) \cdot \overline{T_2} \cdot G \cdot \overline{(A \cdot S) \cdot K_{21}}
 \end{aligned}$$

┌─── 296.8 simplex NOT selected  
 └─── G T/R NOT selected  
 └─── 259.7 XMTR NOT keyed ON

$$\begin{aligned}
 \text{D. RCV}_3 &= \overline{A} \cdot D \cdot \overline{E} \cdot (\text{CB } 13 + \text{CB } 18) \\
 &
 \end{aligned}$$

┌─── EVA  
 └─── BIOMED SUBCARRIER  
 └─── 296.8

Simplex + Guard RCV (296.8 Selected)

A.  $RCV_A (296.8) = (CB\ 13 + CB\ 18) \cdot \bar{T}_1 \cdot G \cdot \bar{K}_{11} \cdot (\bar{B} \cdot \bar{S})$

——— SIMPLEX 259.7  
       B NOT selected  
 ——— RCVR to quadriplexer  
 ——— G T/R NOT selected  
 ——— 296.8 NOT keyed XMTR

B.  $XMT_A (296.8) = (CB\ 18) \cdot G \cdot \bar{K} \cdot \bar{A} \cdot K_{11} \cdot P_0$   
(High Pwr)

——— Pwr amp selected  
 ——— XMTR to quadriplexer  
 ——— 296.8 selected  
 ——— ACCU key  
 ——— G T/R NOT selected

C.  $RCV (243.0) = CB\ 13 + CB\ 18 \cdot \bar{M}_4 \cdot \bar{K}_{41}$

——— RCVR (243.0) to multiplexer  
 ——— RCVR R4 NOT muted

$\bar{M}_4 = \bar{G} \cdot K_4 + \bar{S}1 \cdot (E \cdot \bar{P} \cdot T)$

(243.0 RCVR NOT muted when in  
simplex + GRD RCV and PWR  
amp not keyed or selected

243.0 XMTR NOT keyed in  
SIMPLEX + GRD RCV MODE

Simplex + Guard RCV (259.7 Selected)

A.  $RCV_B = (CB\ 13 + CB\ 18) + M_2 \cdot K_{21}$   
(259.7)

$\left. \begin{array}{l} \text{RCVR R2 input tied to quadriplexer} \\ \text{RCVR R2 not muted} \\ \text{UHF MN}_A \text{ or MN}_C \\ \text{CB CLOSED} \end{array} \right\}$

$\bar{M}_2 = \bar{T}_2 \cdot G \cdot (\bar{A} \cdot \bar{S})$

$\left. \begin{array}{l} \text{Simplex A not selected} \\ \text{G T/R not selected} \\ \text{259.7 XMTR NOT keyed ON} \end{array} \right\}$

B.  $XMT_B = (CB\ 18) \cdot G \cdot \bar{K}_2 \cdot \bar{B} \cdot K_{21} \cdot P_0$   
(High Pwr)

$\left. \begin{array}{l} \text{PWR AMPL mode selected (see below)} \\ \text{XMTR T}_2 \text{ tied to quadriplexer} \\ \text{259.7 selected} \\ \text{ACCU key} \\ \text{G T/R mode not selected} \end{array} \right\}$

$\left. \begin{array}{l} \text{UHF MN}_C \\ \text{CB 18} \\ \text{CLOSED} \end{array} \right\}$

POWER AMP  
SELECTED

$P_0 = \bar{K} \cdot E \cdot \bar{P} \cdot (CB\ 13) \cdot (T_1 + T_2 + T_4)$

$\left. \begin{array}{l} \text{UHF MN}_A \text{ CB closed} \\ \text{PWR AMPL mode selected} \\ \text{EVA mode not selected} \\ \text{ACCU XMT key ON} \end{array} \right\}$

C.  $RCV_4 = (CB\ 13 + CB\ 18) \cdot \bar{M}_4 \cdot K_{41}$

$\left. \begin{array}{l} \text{RCV R}_4 \text{ tied to quadriplexer} \\ \text{RCVR R}_4 \text{ not MUTED} \end{array} \right\}$

$\left. \begin{array}{l} \text{UHF MN}_A \\ \text{or MN}_C \text{ CB} \\ \text{Closed} \end{array} \right\}$

$\bar{M}_4 = K_4 + S_1 \cdot (\bar{E} + P)$

$\left. \begin{array}{l} \text{RCVR}_4 \text{ not muted when in} \\ \text{simplex + G RCV mode and} \\ \text{power ampl not selected} \\ \text{XMTR T}_4 \text{ not keyed} \\ \text{ON IN SIMPLEX +} \\ \text{GRD RCV} \end{array} \right\}$

GT/R (296.8 or 259.7)\*

A.  $RCV_4 = (CB\ 13 + CB\ 18) \cdot M_4 \cdot K_{41}$

243.0

UHF MN<sub>A</sub>  
or MN<sub>C</sub> CB  
CLOSED

RCVR R<sub>4</sub> tied to quadriplexer  
RCVR R<sub>4</sub> not muted

$\overline{M}_4 = \overline{G} \cdot K_4 + \overline{S}_1 \cdot (\overline{E} \cdot \overline{P} \cdot T)$

RCVR<sub>4</sub> not muted when  
in simplex + G RCV  
mode and pwr ampl not  
selected or keyed

XMTR T<sub>4</sub> not keyed  
on in G T/R mode

B.  $XMT_4 = (CB\ 18) \cdot T_4 \cdot K_{41} \cdot P_0$   
(High Pwr)

$= (CB\ 18) \cdot \overline{G} \cdot \overline{K}_4 \cdot K_{41} \cdot P_0$

UHF MN<sup>A</sup> CB closed

G T/R selected

ACCU K<sub>4</sub> isolated key

XMTR T<sub>4</sub> tied to quadriplexer

PWR AMPL on

$P_0 = \overline{K} \cdot E \cdot \overline{P} \cdot (CB\ 13) \cdot (T_1 + T_2 + T_4)$

ACCU XMT

Key on EVA mode not selected

PWR AMPL mode selected

UHF MN<sub>C</sub> CB closed

\*UHF XMT FREQ select has no effect on G T/R mode.

### 17.3 RECEIVER

The orbiter is equipped with four receivers: 296.8 MHz, 259.7 MHz, 279.0 MHz (not used), and 243.0 MHz. In the transceiver the dc output of the Intermediate Frequency (IF) stage is isolated, downlinked, and converted to decibels with respect to 1 milliwatt (dBm) for each receiver at all times. The diode detector looks for dc and modulation and ships the signal to the audio gate and to the Automatic Gain Control (AGC) components to maintain constant gain in the RCVR. The audio gate is a Field Effect Transistor (FET) controlled by a comparator that switches, depending on the level of the squelch amp. Modulation is shipped to the RCV audio circuit for summing, volume control, and further amplification before going to the ACCU. Table 17-4 contains UHF receiver operation data.

Typical UHF squelch thresholds are

- 296.8 - 113 dBm
- 259.7 - 110 dBm
- 279.0 - 110 dBm (not used)
- 243.0 - 112 dBm

**Table 17-4. UHF receiver operation**

| MODE          | SIMPLEX (S)              |                          | SIMPLEX +<br>G RCV (S1) |              | G T/R (G)                |                          | OFF |
|---------------|--------------------------|--------------------------|-------------------------|--------------|--------------------------|--------------------------|-----|
|               | 296 (A)                  | 259 (B)                  | 296 (A)                 | 259 (B)      | 296 (A)                  | 259 (B)                  |     |
| 296.8<br>RCVR | RCV<br>voice<br>T1 MUTES | MUTED                    | T1 MUTES                | MUTED        | MUTED                    | MUTED                    | OFF |
| 259.7<br>RCVR | MUTED                    | RCV<br>voice<br>T2 MUTES | MUTED                   | T2 MUTES     | MUTED                    | MUTED                    | OFF |
| 279.0<br>RCVR | MUTED                    | MUTED                    | MUTED                   | MUTED        | MUTED                    | MUTED                    | OFF |
| 243.0<br>RCVR | MUTED                    | MUTED                    | RCV<br>VOICE            | RCV<br>VOICE | RCV<br>VOICE<br>T4 MUTES | RCV<br>VOICE<br>T4 MUTES | OFF |

### 17.4 XMITTER

The XMITTERS are activated by a switch closure in the ACCU that enables the XMIT control key.

### 17.5 POWER AMP

The 10-W power amp in the orbiter radio operates on the frequencies 243.0, 259.7 and 296.8 MHz in the simplex and the guard modes. Its maximum continuous transmission

time is 2 hours if the coldplate fails and forever if the coldplate is good. Maximum XMIT range is 350 miles. The power amp is powered by main A only. The SPLX power amp switch is used to bypass the power amp in case of a failure. The XMIT control key and a logic enable are necessary for operation.

## 17.6 UHF ACCESS

The transmission and reception signals from the UHF ATC radio are hardwired to the air-to-air channel keyed on panel 06.

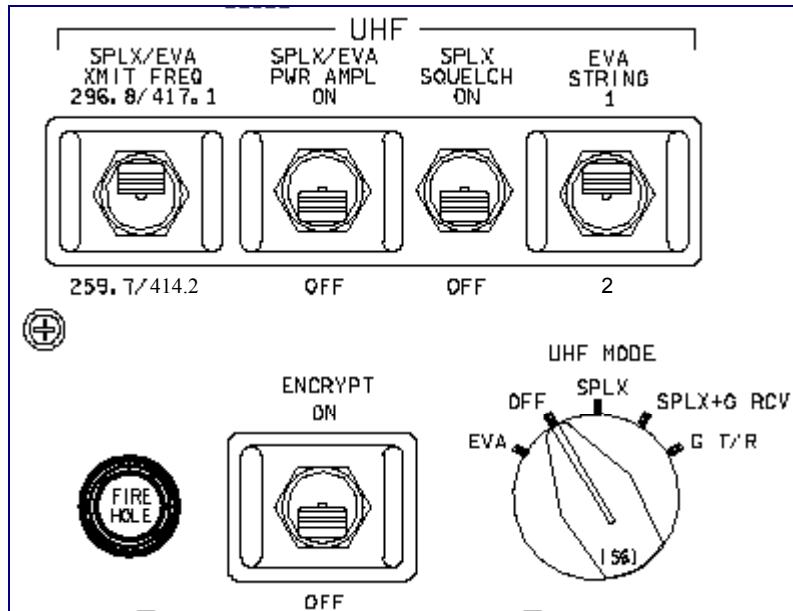


Figure 17-3. Location of UHF channel enable switches

## 17.7 TELEMETRY

Telemetry for the UHF transceiver will be downlinked on Operational Instrumentation (OI) and available on Manual Select Keyboard (MSK) 0970. SPLX/EVA XMIT FREQ, SPLX SQUELCH, SIMPLEX, SPLX + G/RCV, G T/R, EVA are switch scans. RCVR AGC 1, 2, 3, 4 are analog parameters.

V74S2032E - UHF TRANSCIVER MODE-EVA  
 V74S2034E - UHF TRANSCIVER MODE-SIMPLEX  
 V74S2036E - UHF XCVR MODE-SIMPLEX&GUARD RCV  
 V74S2010E - UHF MODE GUARD XCVR T/R  
 V74S2016E - UHF PWR AMPLIFIER - OFF  
 V74S2001E - UHF SQUELCH OFF

V74S2040E - UHF XMIT FREQ 296.8 SELECT  
 V74V2041A - UHF RCVR 1 AGC  
 V74V2042A - UHF RCVR 2 AGC  
 V74V2043A - UHF RCVR 3 AGC  
 V74V2044A - UHF RCVR 4 AGC

## 17.8 ANTENNA

The orbiter antenna is a single annular slot antenna that is flush mounted on the orbiter lower surface. The antenna provides only lower hemisphere coverage. The internal UHF antenna is no longer connected to the UHF ATC radio. It has been removed and replaced with a new internal antenna that is connected to the SSOR.



## 17.9 ORBITER UHF TRANSCEIVER POWER CONSUMPTION

|                   |       |
|-------------------|-------|
| Simplex XMIT      | 158 W |
| Simplex RCV       | 25 W  |
| Simplex + GRD RCV | 25 W  |
| Guard XMIT        | 165 W |
| Guard RCV         | 25 W  |

**SECTION 19 - SPACE-TO-SPACE COMMUNICATIONS SYSTEM**  
**CONTENTS**

| <b>Section</b> |  | <b>Page</b> |
|----------------|--|-------------|
| 19.1           | SYSTEM DESCRIPTION .....                   | 19-1        |
| 19.1.1         | SSCS External and Internal Interfaces..... | 19-1        |
| 19.1.2         | SSOR External Interfaces .....             | 19-2        |
| 19.2           | SSOR HARDWARE .....                        | 19-7        |
| 19.2.1         | Baseband Signal Processor .....            | 19-7        |
| 19.2.2         | Modem .....                                | 19-12       |
| 19.2.3         | Transceiver .....                          | 19-22       |
| 19.2.4         | Power Supply System .....                  | 19-25       |
| 19.3           | SSCS TDMA NETWORK.....                     | 19-26       |
| 19.3.1         | Local User Frames.....                     | 19-26       |
| 19.3.2         | Acquisition and Tracking .....             | 19-26       |
| 19.3.3         | Network Faults .....                       | 19-27       |
| 19.3.4         | Specific Network Cases .....               | 19-27       |
| 19.4           | SSOR OPERATIONAL CONFIGURATION.....        | 19-28       |
| 19.4.1         | Location.....                              | 19-28       |
| 19.4.2         | Electrical Requirements .....              | 19-28       |
| 19.4.3         | Cooling Requirements.....                  | 19-29       |
| 19.4.4         | Mechanical Requirements.....               | 19-29       |
| 19.4.5         | Nominal Operational Configuration .....    | 19-29       |
| 19.5           | REFERENCES.....                            | 19-31       |

## TABLES

| Table |   | Page  |
|-------|---|-------|
| 19-1  | SSOR measurements (from STS-95 MML).....            | 19-6  |
| 19-3  | Vehicle type values.....                            | 19-17 |
| 19-4  | Example slot image status word data of radio A..... | 19-19 |
| 19-5  | SSOR power requirements.....                        | 19-29 |

## FIGURES

| Figure |   |       |
|--------|---|-------|
| 19-1   | SSCS external/internal RF and data interfaces .....       | 19-2  |
| 19-2   | SSCS SSO external interfaces .....                        | 19-3  |
| 19-3   | SSOR controls on panel O6 .....                           | 19-4  |
| 19-4   | Audio distribution system UHF controls on panel A1R ..... | 19-5  |
| 19-5   | SSOR circuit breakers on panel R14 (from STS-95) .....    | 19-7  |
| 19-6   | SSOR BSP received side data flow .....                    | 19-8  |
| 19-7   | SSOR BSP transmit side data flow.....                     | 19-8  |
| 19-8   | SSOR baseband signal processor memory map.....            | 19-11 |
| 19-9   | TDMA frame and user slot construction .....               | 19-14 |
| 19-10  | Status word data fields .....                             | 19-16 |
| 19-11  | Status word programmable field - SRL command .....        | 19-18 |
| 19-12  | Status word programmable field - slot image data .....    | 19-19 |
| 19-13  | Three-radio network example .....                         | 19-19 |
| 19-14  | Acquisition and tracking modes .....                      | 19-22 |
| 19-15  | Internal SSOR antenna location .....                      | 19-23 |
| 19-16  | Network frame synchronization .....                       | 19-26 |
| 19-17  | LNI slot image format .....                               | 19-27 |
| 19-18  | Mechanical outline of SSOR.....                           | 19-30 |

## SECTION 19 SPACE-TO-SPACE COMMUNICATIONS SYSTEM

### 19.1 SYSTEM DESCRIPTION

The Space-to-Space Communications System (SSCS) is an Ultra High Frequency (UHF) Time Division Multiple Access (TDMA) system that provides the capability to transmit and receive voice and data to multiple space vehicles containing portions of the SSCS. The SSCS allows vehicles in close proximity to transmit and receive voice, commands, and telemetry directly via Radio Frequency (RF) links. Vehicles planning to use the SSCS include the Space Shuttle Orbiter (SSO), the International Space Station (ISS), and the Extravehicular Mobility Unit (EMU). Free-Flyers (FFs) can also use the SSCS to communicate directly with the ISS. The SSCS radios were developed as Government-Furnished Equipment (GFE). These radios are the Space-to-Space Orbiter Radio (SSOR), the Space-to-Space EMU Radio (SSER), and the Space-to-Space Station Radio (SSSR). While the different radios are similar in their internal design, they contain unique functions and external interfaces.

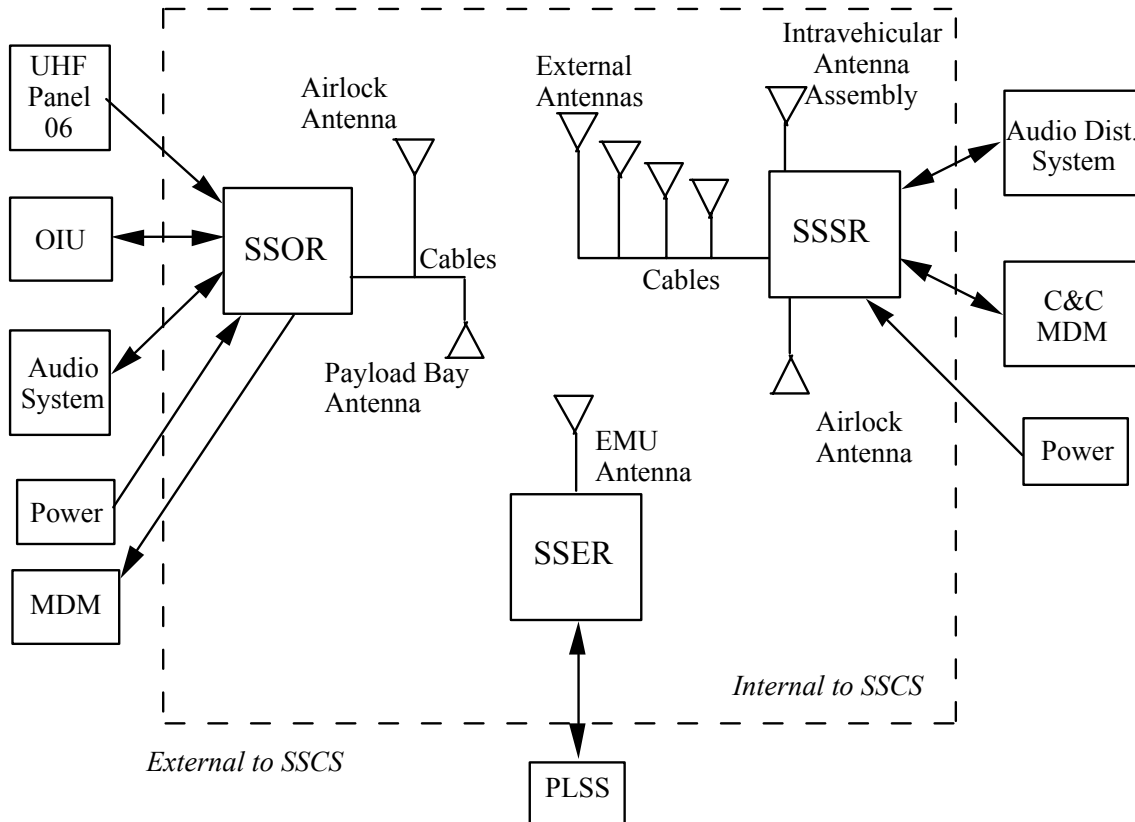
The SSOR provides duplex voice communications between the SSO and EMUs and between the SSO and the ISS. The SSOR supports reception of digitized analog Biological Medical (BIOMED) and EMU status data from the EMU, the transmission of commands to the ISS, and reception of telemetry from the ISS. The SSOR replaces the Extravehicular Activity (EVA) function of the Air Traffic Control (ATC) transceiver on the orbiter. The orbiter ATC transceiver maintains its ground link functions.

The SSER provides duplex voice communications between EMU and the SSO EMU to EMU(s) and between EMU and ISS. The SSER also transmits digitized analog BIOMED and EMU status data to the SSO and to the ISS.

The SSSR provides duplex voice communications between the ISS and the SSO and between ISS and the EMUs. The SSSR supports reception of digitized analog BIOMED and EMU status data from the EMUs, the reception of commands from the SSOR, and the transmission of telemetry to the SSOR.

#### 19.1.1 SSCS External and Internal Interfaces

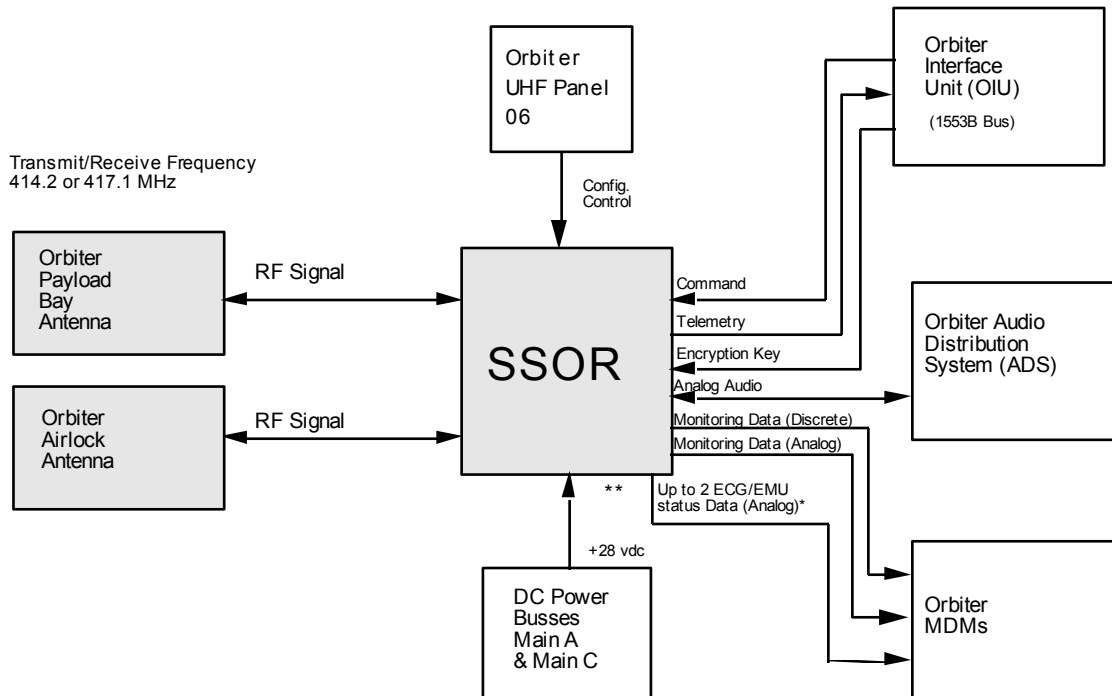
The SSCS external and internal interfaces are shown in Figure 19-1.



**Figure 19-1. SSCS external/internal RF and data interfaces**

**19.1.2 SSOR External Interfaces**

The SSCS interfaces to the orbiter through the SSOR. The SSOR interfaces to the orbiter through panel O6, the Orbiter Interface Unit (OIU), the Audio Distribution System (ADS), dc power buses, and orbiter MDMs. The SSCS SSO external interfaces are shown in Figure 19-2.



\* The orbiter MDM can accept only two channels of ECG/EMU status data simultaneously. The other two channels are time-shared.

\*\*Cooling is forced air.

**Figure 19-2. SSCS SSO external interfaces**

### 19.1.2.1 SSOR Crew Configuration Interface (Panel O6)

The crew can configure the SSOR using five switches located on panel O6. These switches are shown in Figure 19-3.

#### A. UHF SPLX/EVA XMIT FREQ

1. **259.7/414.2** - When selected, the SSOR transmits and receives on 414.2 MHz. This switch is shared with the UHF/ATC system.
2. **296.8/417.1** - When selected, the SSOR transmits and receives on 417.1 MHz. This switch is shared with the UHF/ATC system.

#### B. UHF SPLX/EVA PWR AMPL

1. **ON** - When selected, the SSOR is in HIGH power mode. This switch is shared with the UHF/ATC system.
2. **OFF** - When selected, the SSOR is in LOW power mode. This switch is shared with the UHF/ATC system.

C. UHF EVA STRING

1. When selected, the SSOR uses its PRIMARY string of hardware (string 1).
2. When selected, the SSOR uses its BACKUP string of hardware (string 2).

D. UHF MODE

1. **EVA** - When selected, the SSOR is powered on. This switch is shared with the UHF/ATC system.
2. **OFF/SIMPLEX/SIMPLEX + G RCV/G T/R/** - When selected, the SSOR is powered off. This switch is shared with the UHF/ATC system.

E. ENCRYPT

1. **ON** - When selected, encryption is turned on in the SSOR. The SSOR encrypts all data received from the OIU before transmission to the SSSR or SSERs. The Data Encryption Standard (DES) is used.
2. **OFF** - When selected, encryption is turned off in the SSOR. The SSOR does not encrypt data received from the OIU before transmission to the SSSR or SSERs.

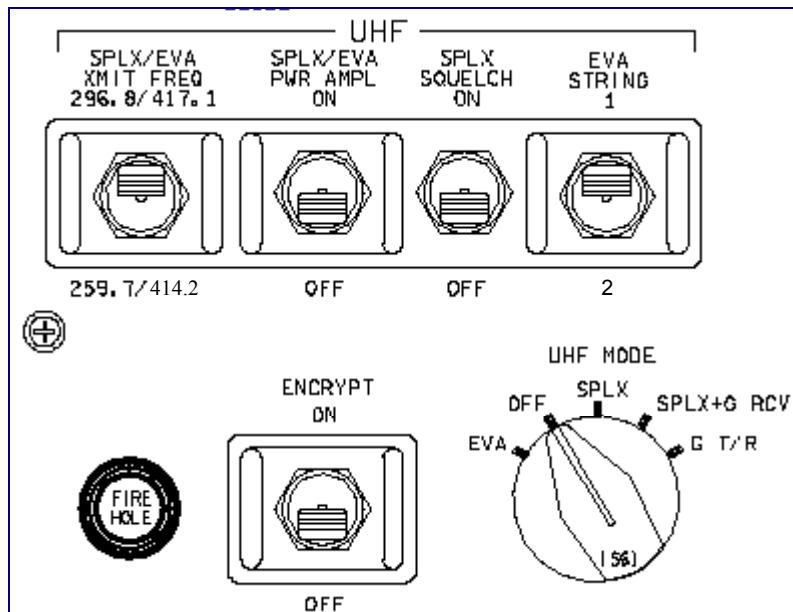


Figure 19-3. SSOR controls on panel O6

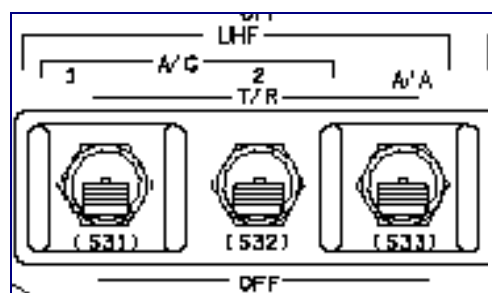
### 19.1.2.2 Orbiter Interface Unit Interface

The SSOR will have an output to the OIU and an input from the OIU through a 1553B data interface. The SSOR outputs forty 16-bit words of digital data (received from the SSSR) to three subaddresses which will be polled by the OIU every 100 milliseconds. The SSOR produces the standard MIL-STD-1553B status bits. The SSOR also has a wraparound function. At the request of the OIU, the SSOR sends words received from the OIU back to the OIU.

The SSOR accepts two types of data from the OIU: command and configuration. Command data are accepted at a maximum rate of one command per second. The command message size is sixty-four 16-bit words (1024 bits). The only configuration data sent to the SSOR via the OIU is the selection of 1 of 4096 encryption keys. The SSOR must have encryption – on, to accept uplinked encryption keys.

### 19.1.2.3 Audio Distribution System Interface

The SSOR transmits/receives audio to/from the ADS through the Audio Central Control Unit (ACCU). The routing of the orbiter audio to/from the SSOR is controlled through the ACCU section of panel A1R. UHF can be routed on three voice loops – Air-to-Ground (A/G) 1, A/G 2, and Air-to-Air (A/A). If a particular voice loop is selected to Transmit/Receive (T/R) for UHF on panel A1R, then any transmissions on the voice loop are transmitted out through the SSOR and any audio received through the SSOR is broadcast on that voice loop. If a particular voice loop is configured for OFF, then any transmissions on the voice loop are not sent to the SSOR, and any audio received through the SSOR is not broadcast on that voice loop. These switches are shown in Figure 19-4.



**Figure 19-4. Audio distribution system UHF controls on panel A1R**

### 19.1.2.4 Orbiter Instrumentation System Interface

There are eight SSOR measurements which are collected from the SSOR via the orbiter instrumentation system. There are two ECG status measurements which are gathered from the SSOR via the orbiter instrumentation system as well. All 10 measurements are listed in Table 19-1.



- A. RF POWER LEVEL - V74E2045A - This parameter indicates the RF power output at the duplexer. This measurement ranges from 15 to 45 dBm.
- B. POWER STATUS - V74C2047A - This parameter indicates the current consumption of the SSOR on the power distribution board. This provides a status on either string 1 or string 2 of the SSOR. It is expected to be between 0 and 5 amps. The measurement is capable of measuring from 0 to 7 amps.
- C. PRIMARY FRAME SYNC STATUS - V74X2050E - When this parameter is high, the SSOR has acquired frame synchronization with at least one other user on string 1.
- D. BACKUP FRAME SYNC STATUS - V74X2053E - When this parameter is high, the SSOR has acquired frame synchronization with at least one other user on string 2.
- E. PRIMARY SIGNAL PROC STATUS - V74X2051E - When this parameter is high, the signal processor on string 1 has a good status.
- F. BACKUP SIGNAL PROC STATUS - V74X2052E - When this parameter is high, the signal processor on string 2 has a good status.
- G. ENCRYPT ON - V74S2048E - When this parameter is high, the ENCRYPT switch on panel O6 is in the ON position. When this parameter is low, the ENCRYPT switch on panel O6 is in the OFF position.
- H. STRING SELECT - V74S2049E - When this parameter is high, the STRING SELECT switch on panel O6 is in the position to select string 1. When this parameter is low, the STRING SELECT switch on panel O6 is in the position to select string 2.
- I. EMU STATUS/ECG 1 - V67V0100A - This contains status data from the SSER with the lowest radio identification code.
- J. EMU STATUS/ECG 2 - V67V0200A - This contains status data from the SSER with the second lowest radio identification code.

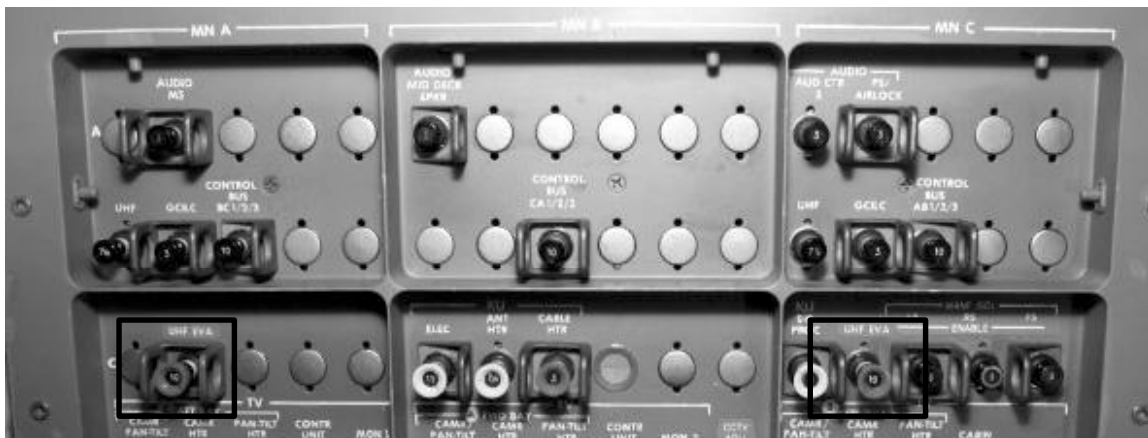
**Table 19-1. SSOR measurements (from STS-95 MML)**

| MSID      | Nomenclature                   | MDM | Card | Channel | DSC         |
|-----------|--------------------------------|-----|------|---------|-------------|
| V74E2045A | SSOR RF POWER LEVEL            | OF3 | 7    | 11      | N/A         |
| V74C2047A | SSOR POWER STATUS              | OF3 | 15   | 5       | N/A         |
| V74X2050E | SSOR PRIMARY FRAME SYNC STATUS | OF3 | 10   | 2       | N/A         |
| V74X2053E | SSOR BACKUP FRAME SYNC STATUS  | OF3 | 10   | 2       | N/A         |
| V74X2051E | SSOR PRIMARY SIGNAL PROC       | OF3 | 10   | 2       | N/A         |
| V74X2052E | SSOR BACKUP SIGNAL PROC STATUS | OF3 | 10   | 2       | N/A         |
| V74S2048E | SSOR COM ENCRYPT ON            | OF4 | 13   | 1       | N/A         |
| V74S2049E | SSOR COM STRING SEL 1 ON       | OF4 | 12   | 1       | N/A         |
| V67V0100A | CHANNEL 1 ECG                  | OF2 | 15   | 2       | OF3 (power) |
| V67V0200A | CHANNEL 2 ECG                  | OF2 | 15   | 3       | OF3 (power) |

### 19.1.2.5 Orbiter Power System Interface

The 28 V dc power to the SSOR is provided from two isolated buses, main A and main C. Main A powers the primary string (string 1), and main C powers the backup string (string 2). The maximum power required when transmitting in the normal operations mode is 56 W at high power and 30 W at low power. The power requirement when the SSOR is OFF is 5 W.

Two circuit breakers labeled UHF EVA on panel R14 control the interface from main A and main C to the SSOR. These circuit breakers are shown in Figure 19-5.



**Figure 19-5. SSOR circuit breakers on panel R14 (from STS-95)**

## 19.2 SSOR HARDWARE

### 19.2.1 Baseband Signal Processor

The purpose of the Baseband Signal Processor (BSP) is to process and distribute the majority of baseband data. The BSP receives data from the modem, modifies the data, and redirects them to different locations (audio output, BIOMED output, etc.). The BSP receive data flow block diagram is shown in Figure 19-6. The BSP takes in data from different sources (audio input, command input (1553 interface), etc.), formats the data, and transmits them to the modem. The BSP transmit data flow block diagram is shown in Figure 19-7.

#### 19.2.1.1 BSP-to-Modem Interface

Communications between the BSP and the modem occur over a serial interface. The data rate is 8/9 of 695 kHz, or approximately 618 kHz. When data are received by the modem, the 8/9 encoding is removed before the data are delivered to the BSP.

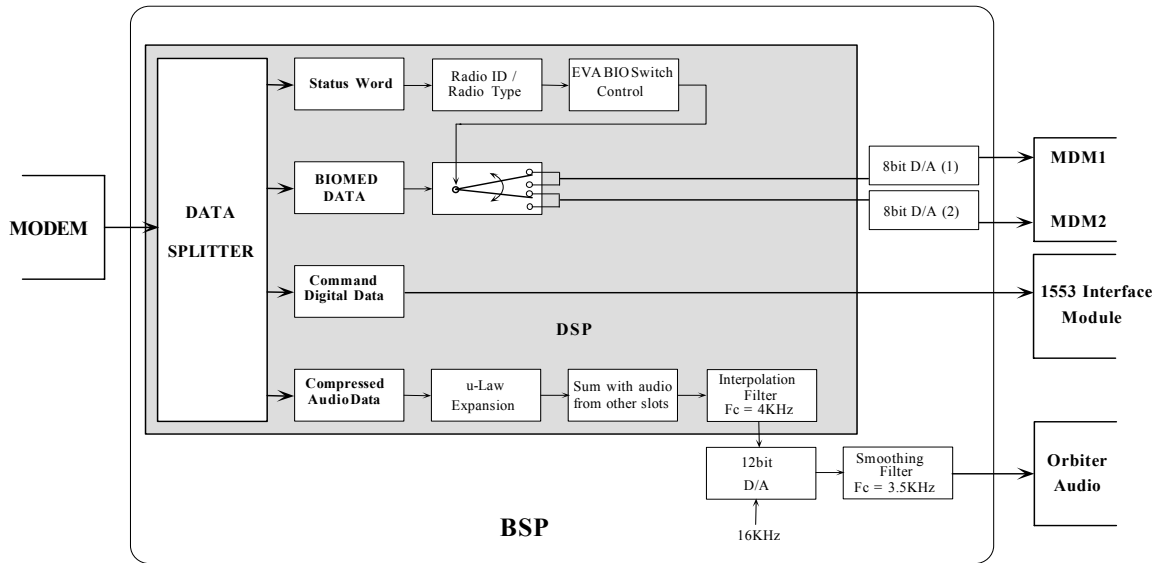


Figure 19-6. SSOR BSP received side data flow

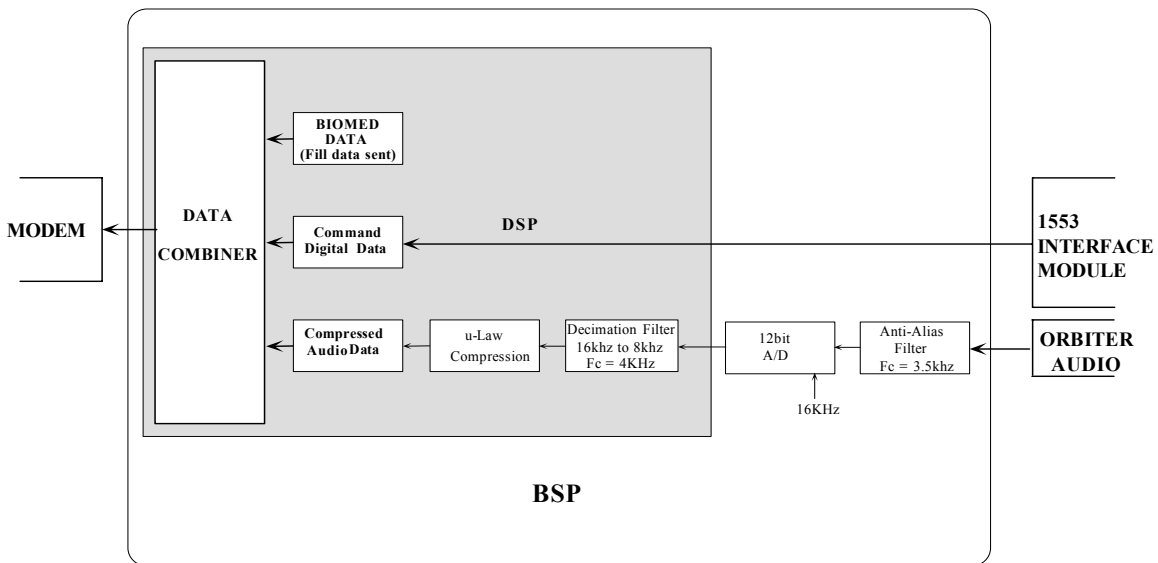


Figure 19-7. SSOR BSP transmit side data flow

The interface is synchronous with the modem as master and the BSP as slave. Upon request from the modem, the BSP delivers 608 bits of data. The data consist of 32 BIOMED bits, 64 digital bits (commands to the SSSR), and 512 audio bits. The modem sends 640 bits of data, consisting of 32 status bits, 32 BIOMED bits, 64 digital bits (telemetry from the SSSR), and 512 audio bits to the BSP.

The hardware interface consists of a T/R clock, T/R data, and a T/R frame sync/cover pulse. The setup and format of the serial port is controlled in firmware. The transmit side is set up to transmit 32 bit blocks of data on the rising edge of the transmit clock. On the receive side, data are accepted at 8 bits per block. This allows for quick expansion of audio data (compressed for transmission to 8 bits) as they are received. An interrupt occurs after 8 bits have been received, telling the firmware to retrieve the data byte.

### **19.2.1.2 Digital Signal Processor**

The Digital Signal Processor (DSP) is a major element of the BSP. All data signals pass through the DSP. The DSP has the purpose of both a controller and a signal processor.

#### **19.2.1.2.1 DSP: Controller**

As a controller, the DSP controls the flow of audio and digital data on to and off of the board (with the exception of the serial interface that is a slave to the modem). Data flow timing is controlled by the modem, but the order and format are controlled by the BSP. Switching information, such as frequency control, power levels, and data encryption, is processed via the DSP. For example, all acquisition timing is controlled internally in the DSP.

#### **19.2.1.2.2 DSP: Signal Processor**

As a signal processor, the DSP deals with three types of signals – BIOMED data, command/telemetry digital data, and digital audio data.

BIOMED data, received from an SSER radio (through the modem), are sent to the D/A converter in sets of 8 bits 500 times every second (4kHz). The D/A converter (located outside of the DSP but within the BSP) sends the BIOMED data on to the orbiter Multiplexer/Demultiplexers (MDMs). Fill data are placed in the BIOMED data slot for transmission to the modem.

All command digital data are obtained from the 1553 interface module and transmitted to the SSSR via the modem. Telemetry digital data are received from the SSSR via the modem. It may also be referred to as “received digital command data” because on the SSOR/1553 interface, digital telemetry is effectively the same as a digital command. No signal processing takes place on the command/telemetry digital data.

Most signal processing in the DSP takes place on the digital audio data. All audio is sampled at 16 kHz, passed through a lowpass Finite Impulse Response (FIR) filter with cutoff frequency of 4 kHz, and internally decimated to the system sample rate of 8 kHz. Using a digital highpass filter, the audio data are ac-coupled to remove dc bias. The data are then passed to the ulaw compression algorithm. Upon receiving the audio data, the DSP uses a table to expand the ulaw data back to 12 bits. The data are then passed through another highpass Infinite Impulse Response (IIR) filter to remove any dc components, passed through an Automatic Volume Control (AVC) routine, interpolated

to 16 kHz, and passed through a lowpass FIR filter ( $F_c = 4\text{kHz}$ ). The processed data, now 12 bits at 16 kHz, are sent to a D/A converter (located outside of the DSP but within the BSP). Note: All audio data are 2x oversampled to reduce the complexity of the external anti-aliasing and smoothing filters.

#### **19.2.1.2.2.1 Ulaw Compression**

Ulaw companding is a compression/expansion technique used in telecommunications to reduce bandwidth requirements while preserving speech quality. The ulaw algorithm is implemented to reduce the amount of audio data sent between radios. Data are compressed from 14 to 8 bits for transmission. On the receive side, a ulaw expansion table is created to speed up the expansion of incoming data.

#### **19.2.1.2.2.2 Automatic Volume Control**

An AVC routine is implemented on SSOR BSP for audio balance and level control. The SSOR BSP has an AVC routine on the receive side. The AVC routine provides a constant output of approximately 0 dBm.

#### **19.2.1.2.3 Power Protection**

A watchdog circuit exists within the BSP that puts the DSP into reset when the voltage on the BSP board drops below 4.65 V or if the DSP does not supply the watchdog a signal every 1.6 sec.

#### **19.2.1.3 Acquisition Module**

Digital and analog reconstruction of audio and BIOMED signals are taken care of by the acquisition module of the BSP. All Analog-to-Digital (A/D) converters and Digital-to-Analog (D/A) converters are located here, along with the smoothing filters for the D/A converters.

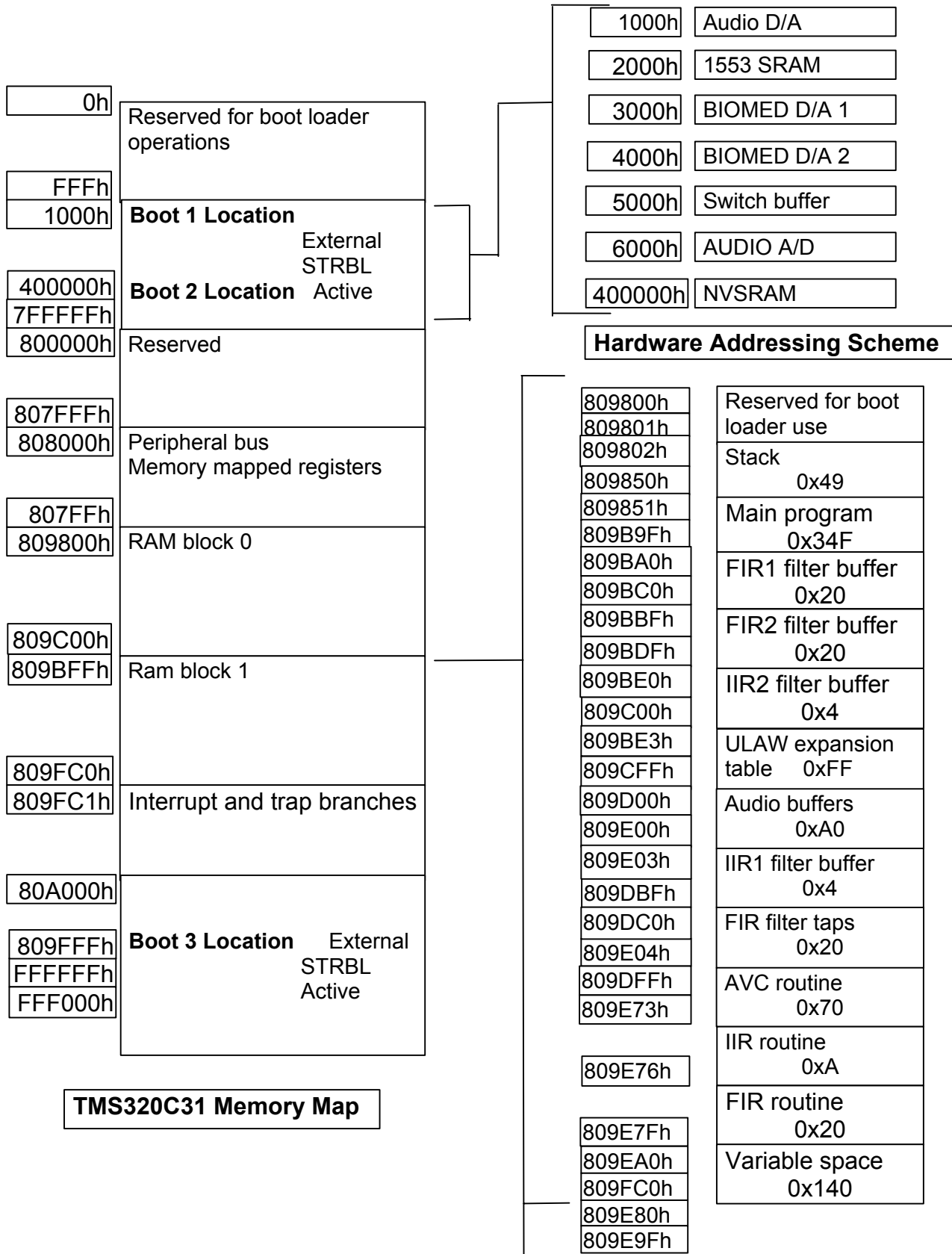
All A/D and D/A converters are 12-bit converters except the BIOMED output D/A converter, which is an 8-bit D/A. All 12-bit converters are run at 16 kHz, twice the system rate. All decimation and interpolation take place in the DSP. The 8-bit D/A runs at 500 Hz.

#### **19.2.1.4 BSP Firmware**

The BSP firmware is stored in Nonvolatile Static Random Access Memory (NVS RAM) until powerup, when the firmware is downloaded into DSP memory. The system is designed so that no memory external to the DSP is required after bootup. The firmware implements the controlling and signal processing functions of the DSP.

The memory map of the BSP is shown in Figure 19-8. This memory map shows the TMS320C31 memory organization.

The BSP firmware allows the DSP to perform its functions as controller and signal processor.



**TMS320C31 Memory Map**

**Figure 19-8. SSOR baseband signal processor memory map**

## **19.2.2 Modem**

SSCS data are transmitted based on a five-user TDMA network system with a user data rate of 512 kbits/sec. The SSOR modem board input accepts a serial data stream from the BSP board, adds synchronization and network information, encodes the data with error correction coding, and transmits these data on a Continuous Phase Frequency Shifted Keyed (CPFSK) Intermediate Frequency (IF) carrier centered at 21.4 MHz. These transmitted data use one of the five user slots. The SSOR modem board also receives up to four data streams (slots) from the SCS network and synchronizes and processes these data streams. The received data are then sent to the BSP to process and transform the data to their respective interfaces. The same modem board is used for the SSOR, SSER, and SSSR.

### **19.2.2.1 Modem Interfaces**

The modem interfaces with the RF transceiver, BSP, and power converter. The modem requests data (commands and audio) from the BSP. The modem then adds the status word and encodes the data. Next, the modem adds the preamble and the Unique Word (UW) and modulates the data onto an IF carrier centered at 21.4 MHz. The modem outputs the IF signal directly to the RF transceiver.

The modem receives the demodulated IF signal (baseband encoded data) from the RF transceiver. The 8/9 encoding is removed before the status word data, BIOMED data, and SSSR telemetry and audio data are delivered to the BSP. The BSP is a slave to the modem. Therefore, all modem/BSP data transfers are controlled by the modem.

### **19.2.2.2 Modem Architecture**

#### **19.2.2.2.1 DSP Embedded Controller**

The modem board is built around a Texas Instruments TMS320C31 DSP with extensive utilization of an Altera Complex Programmable Logic Device (CPLD). This controller selects the transmit slot for the host radio, triggers the transmission of the slot by the host radio hardware, and establishes and maintains synchronization with other radios in the network. This controller also generates Status Words (SWs) containing network status data and commands, processes SW data and commands received from other radios, and detects and resolves network fault conditions.

#### **19.2.2.2.2 Decoder**

The baseband data received from the RF transceiver are first sent to the bit synchronizer to recover the data clock. The recovered clock and data are then sent to the UW detector.

#### 19.2.2.2.1 Bit Synchronizer

The purpose of the bit synchronizer is to produce a data clock by detecting data transitions on the demodulator data input. A signal is created whenever a bit transition is detected (called `edge_gate`). An internal reference clock exists within the bit synchronizer. It is created by dividing a fixed clock by an integer to get the nominal frequency. With no data transitions, the internal reference clock will be free-running at a frequency that is close to the received bit rate. A phase detector and accumulator is created by exclusive OR'ing the internal reference clock and the signal `edge_gate` together. The phase detector accumulates phase if the internal reference clock is late or loses phase if the internal reference clock is early. The phase detector is implemented using an up/down counter with saturating limits. Once the limits are exceeded, the internal reference clock is adjusted and the up/down counter is set to its midvalue. The correction to the internal reference clock is accomplished by a phase-controlled oscillator by adding an extra pulse or dropping a pulse from a fixed high frequency clock source to the internal reference clock divider. Extra logic is provided to perform a false lock detection operation. The bit synchronizer design is essentially a first-order digital phase lock loop.

#### 19.2.2.2.2 Unique Word Detector

All SSCS radios have a common SSCS UW pattern. The UW pattern is E07E07h (1110 0000 0111 1110 0000 0111 b).

The UW detector is implemented such that if the UW has more than one error, the slot of data is not processed any further. However, if the UW is detected with one or no errors, the slot of data is processed.

For more information on UWs, see Section 19.2.3.3.2.

#### 19.2.2.2.3 Encoder

The encoder receives user data from the BSP and local SW data from the embedded controller. First, this information is transmission-encoded, using Reed-Solomon (RS) coding. Then it is translation-encoded, using the 8/9 (0,4) Run-Length Limited (RLL) block code. For more information on the coding, see Section 19.2.3.3.4.

Timing for transmission is controlled by an internal timing interrupt generated by the embedded controller. When the transmission interrupt is initiated, the encoder transmits the preamble and UW followed by the encoded SW and user data. The baseband data are then sent to a Numerically Controlled Oscillator (NCO), which generates an 8-bit digital representation of the first alias of the IF CPFSK signal. These digital data are then run into a D/A converter, followed by an IF filter and amplifier, which picks off the 21.4-MHz IF signal. The IF output is sent to the RF module for transmission.

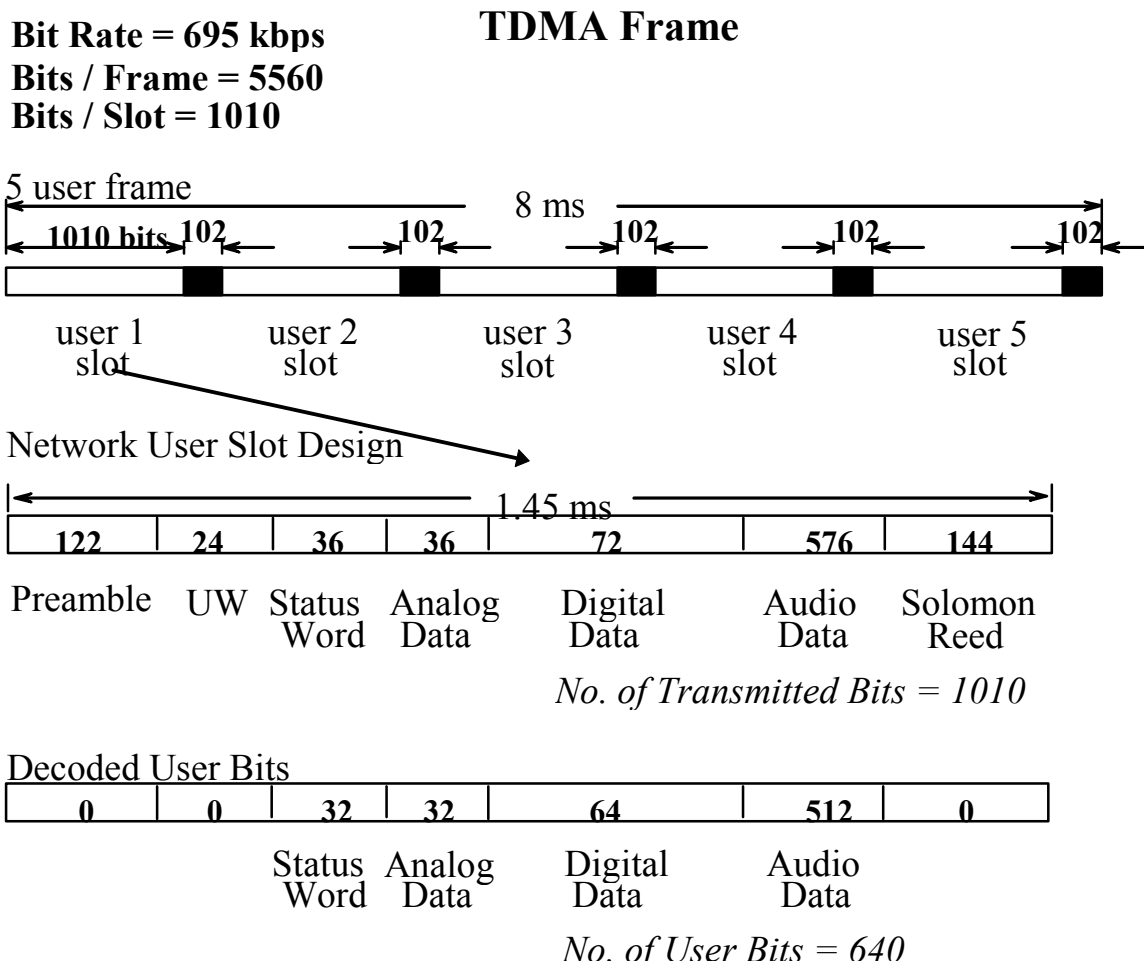
#### 19.2.2.3 Modem Frame and Slot Design

The modem frame and slot design allows the SSCS to support five users simultaneously with a transmission data rate of 695 kbit/sec and an end user data rate



of 512 kbit/sec. Figure 19-9 shows the structure of the TDMA frame and the structure of the user slots.

Each TDMA frame consists of five user slots. Each user slot is made up of the preamble, UW, SW, digitized analog BIOMED data, digital command/telemetry data (to/from SSSR), digitized analog audio data, and the RS coding parity check bits.



**Figure 19-9. TDMA frame and user slot construction**

**19.2.2.3.1 Preamble**

The preamble, or synchronization field, is a one-zero pattern 122 bits in length. This provides a predictable bit synchronization and dc bias elimination period. The duration of the one-zero pattern was optimized based on the performance of the bit synchronizer. The preamble is nonencoded data.

The preamble is used by the bit synchronizer to align the bits of the received, demodulated data and to generate a bit synchronization clock.

**19.2.2.3.2 Unique Word**

The purpose of the UW is to synchronize the receiving modem to the beginning of the user slot. The modems rely on UW detection for all slot tracking and synchronization functions. The integrity of the UW is key to network performance.

In order to minimize the possibility of false UW detection, to minimize data-induced dc biasing, and to guarantee bit synchronization performance, the SSCS codes the data transmitted as follows:

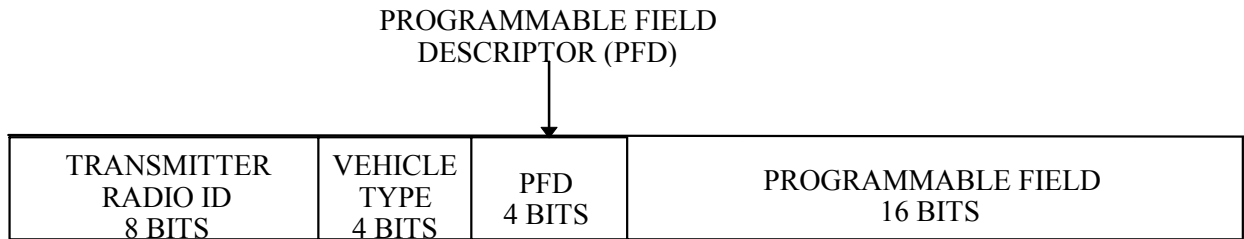
- 8/9 (0,4) RLL code is used (see Section 19.2.3.3.4).
- The encoded data have no more than four zeros in a row.
- Non-Return to Zero Inverse (NRZ-I) or Non-Return to Zero Mark (NRZ-M) encoding is used.
- The dc component of the baseband data is minimized.
- The baseband data bandwidth is limited.

The UW is then designed to have five zeros in a row. Since the user data are encoded (as mentioned above) such that there are no more than four zeros in a row, this scheme guarantees that the encoded user data cannot contain a UW. The UW is nonencoded data.

For information on UW detection, see Section 19.2.3.2.3.

#### **19.2.2.3.3 Status Word**

The SW is used to transmit acquisition and tracking information between different modems in the network. The data fields contained in the SW are shown in Figure 19-10.



| <b><u>PFD</u></b><br><b><u>(hexadecimal)</u></b> | <b><u>Network Message Type</u></b>    |
|--|---------------------------------------|
| 0  | Unused                                |
| 1  | PUNT command                          |
| 2  | Slot Reacquisition List (SRL) command |
| 3  | Tracking data, slot 0                 |
| 4  | Tracking data, slot 1                 |
| 5  | Tracking data, slot 2                 |
| 6  | Tracking data, slot 3                 |
| 7  | Tracking data, slot 4                 |
| 8  | Unused                                |
| 9  | Unused                                |
| A  | Unused                                |
| B  | Unused                                |
| C  | Unused                                |
| D  | Unused                                |
| E  | Slot image                            |
| F  | Information age counter value         |

**Figure 19-10. Status word data fields**

**19.2.2.3.3.1 Transmitter Radio ID**

This field contains a unique radio Identification (ID) of the transmitting radio. Each SSOR has two 8-bit radio IDs: one for string 1 and one for string 2. The codes 00h and FFh are reserved and specified to be unused by the SSOR.

**19.2.2.3.3.2 Vehicle Type**

The vehicle type identifies the radio type of the transmitting radio. The SSOR vehicle type is 2h. All vehicles types are shown in Table 19-2.

**Table 19-2. Vehicle type values**

| Type (h) | Vehicle | Host radio |
|----------|---------|------------|
| 0        | Unused  | Unused     |
| 1        | ISS     | SSSR       |
| 2        | SSO     | SSOR       |
| 3        | EMU     | SSER       |
| 4        | Unused  | Unused     |
| 5        | Unused  | Unused     |
| 6        | Unused  | Unused     |
| 7        | FF      | SSFR       |
| 8        | Unused  | Unused     |
| 9        | GSE     | GSE SSOR   |
| A        | GSE     | GSE SSOR   |
| B        | GSE     | GSE SSER   |
| C        | Unused  | Unused     |
| D        | Unused  | Unused     |
| E        | Unused  | Unused     |
| F        | GSE     | GSE SSFR   |

**19.2.2.3.3.3 Programmable Field Descriptor and Programmable Field**

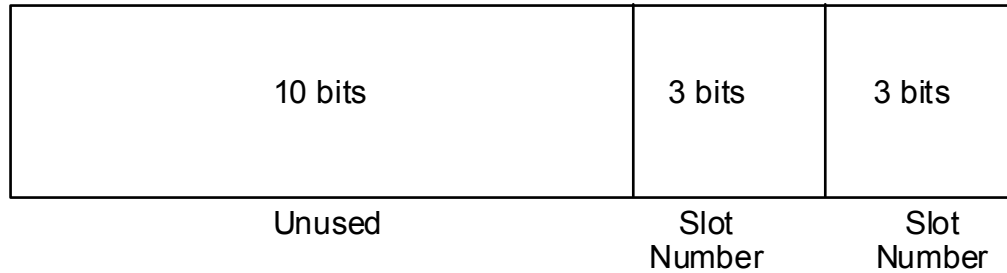
The Programmable Field Descriptor (PFD) identifies the content of the programmable field. There are five types of programmable fields – the Peremptory Unilateral Network Tracking (PUNT) reacquisition command, the Slot Reacquisition List (SRL) command, tracking data, the slot image, and the Information Age Counter (IAC) value.

**A. PUNT command**

The PUNT command (PUNT reacquisition) may be sent by any radio in the SSCS. The PUNT command is sent in response to certain network faults (i.e., phase error, three simultaneous slot conflicts). The PUNT command causes a network reset and a reacquisition of all radios. The PUNT command has a PFD = 1h and a programmable field of all zeros.

**B. SRL command**

Under some circumstances, the host radio drops out of a network because of a network fault. In such cases, the reacquiring radio holds its slot for up to 30 seconds. This is a feature known as squatters' rights. This reacquisition is accomplished with the SRL command. The SRL programmable field contains 10 bits of zeros (unused) and two 3-bit slot numbers from 0h to 4h, with 7h being the null value. The structure of the SRL programmable field is shown in Figure 19-11. If the reacquiring radio is unable to claim a previously held transmit slot, it selects the lowest-indexed unoccupied slot.



**Figure 19-11. Status word programmable field - SRL command**

Radios which recognize either slot in the SRL as their transmit slot must reacquire.

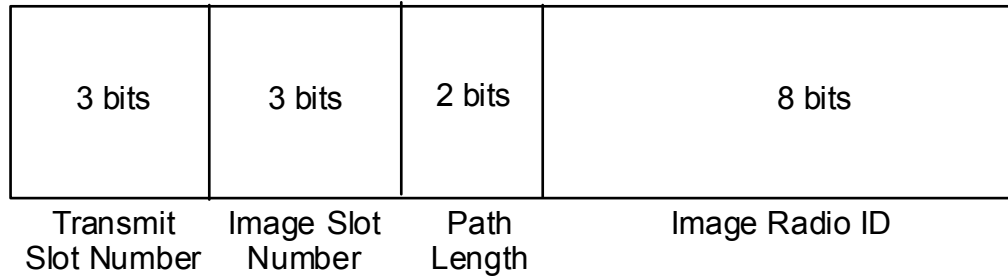
C. Tracking data

In tracking mode, each radio sends the phase errors it measures for each slot of data received from another radio. The phase errors are transmitted in the SW according to the appropriate slot. For example, if the SSOR is receiving data from the SSSR in slot 3, the SSOR transmits the phase error measured on the data received in slot 3 in a SW with a PFD = 6h. This format of this tracking data field is a 16-bit 2's complement integer.

D. Slot image data

For the SSCS network to exist, a Local Network Image (LNI) exists within each radio. This LNI contains a five-entry buffer indexed by the slot number. Each LNI entry contains the radio ID of the slot occupant and the path length to the occupant. To construct the LNI entries, the radio must receive information detailing which radios are transmitting in a given slot and the path length to the radio. To do this, each radio transmits information about one other radio it can talk to and how far the path to that radio is. This other radio is called the transmitting radio's image. The information is sent in the SW with a slot image in the programmable field (PFD = Eh).

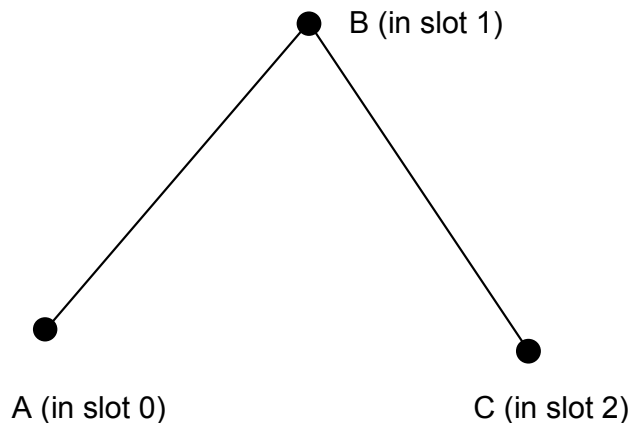
In this programmable field, a radio sends its transmit slot number (slots are numbered 0 through 4) in the first 3 bits. The next 3 bits contain the slot number of the radio's image (another radio that the transmitting radio can talk to). The next 2 bits contain the path length to the image. If the path length is three or greater, a value of three is entered in the path length field. The last 8 bits contain the image radio ID. The actual bit structure of the 16-bit programmable field of slot image data is shown in Figure 19-12.



**Figure 19-12. Status word programmable field - slot image data**

To understand this better, see the following example:

There are three radios – radio A, radio B, and radio C. Radio A can talk to radio B, but cannot talk to radio C. Radio C can talk to radio B, but cannot talk to radio A. See Figure 19-13. Since each radio passes along slot image data, radio A knows about radio C from radio B and vice versa. Each radio keeps a table of the network (the LNI) in its memory and it updates it using the slot image data that it gets from the other radios.



**Figure 19-13. Three-radio network example**

Table 19-3 shows the slot image SWs that radio A would send out.

**Table 19-3. Example slot image status word data of radio A**

| PFD (h) | Transmitting radio slot | Image slot | Path length | Image ID       |
|---------|-------------------------|------------|-------------|----------------|
| E       | 0                       | 1          | 1           | Radio B ID no. |

E. IAC value

This field is a 16-bit positive integer indicating the age of the network data. The IAC is a counter within each radio that counts the number of frames. When the

value of the IAC reaches 1870 (1870 frames = 14.96 seconds), the radio clears all radios from its LNI with a path length of three and then resets all the remaining radios in its LNI to have a path length of three. Therefore, a radio must be absent from the network for one or two IAC cycles before it is purged from LNIs of the other network members.

The radios maintain their own IAC value. Each radio transmits its IAC value to the other members of the network once every 11 frames. If a radio receives an IAC value higher than its own, it will bump up its IAC value to match the received value. This keeps the IAC values approximately the same to make sure all the radios in the network purge their LNIs at approximately the same time. This prevents ghosting (i.e., the erroneous reintroduction of absent radios into member LNIs). The IAC synchronizes the LNI bookkeeping cycles of the radios in an SSCS network.

#### Summary of programmable fields

Each radio transmits its 5-slot LNI alternately with its 5-slot phase error table at the rate of 1 slot per frame over 10 frames and transmits its IAC value in the 11th frame. The LNI and phase error table transmit cycles are asynchronous. Furthermore, the 11-frame SW cycles for different radios are not synchronized.

Network fault conditions may trigger the transmission of PUNT or SRL commands by one or more radios; error messages defer the normal 11-frame cycle and thus temporarily extend it.

#### **19.2.2.3.4 Data Encoding**

##### **19.2.2.3.4.1 Reed-Solomon Coding**

The RS error correction code is used to provide channel error correction for the SW, digitized analog BIOMED data, digital command data, and digitized analog audio data. The preamble and UW are not encoded with the RS code.

##### **19.2.2.3.4.2 Run-Length Limited Code**

The 8/9 (0,4) RLL block code is used to encode a slot of data. The RLL code used for transmit data encoding increases the minimum Hamming distance between the user data and the UW.

Hamming distance is defined as the number of positions in which two binary numbers differ.

For example, the Hamming distance between 101101 and 001100 can be computed as follows:

$$101101 \oplus 001100 = 100001$$

Therefore, the Hamming distance (101101, 001100) = 2

By increasing the minimum Hamming distance between the user data and the UW, the RLL code decreases the chances that the user data could be falsely detected as the UW.

Eight bits of nonencoded user data turn into 9 bits of RLL encoded data. Hence, the 8/9 at the beginning of the name.

Furthermore, the RLL code only allows a maximum of four zeros in a row. Since the UW has a minimum of five zeros in a row, this increases the differences between the encoded user data and the UW.

The SW, digitized analog BIOMED data, digital command data, digitized analog audio data, and the RS coding parity check bits are all encoded using the RLL scheme. The preamble and UW are not encoded using the RLL scheme.

The RLL code is implemented using a table lookup. The RLL table lookup also incorporates the Non-Return to Zero Level (NRZ-L) to NRZ-I or NRZ-M conversion.

#### **19.2.2.4 Slot Acquisition**

One important function of the SSCS modem is radio slot acquisition. In this process each modem must select a TDMA transmit slot. As shown in Figure 19-12, the TDMA frame supports five user slots. Therefore, each radio must identify an unused slot (acquisition) and then align its transmission time with the available user slot (tracking).

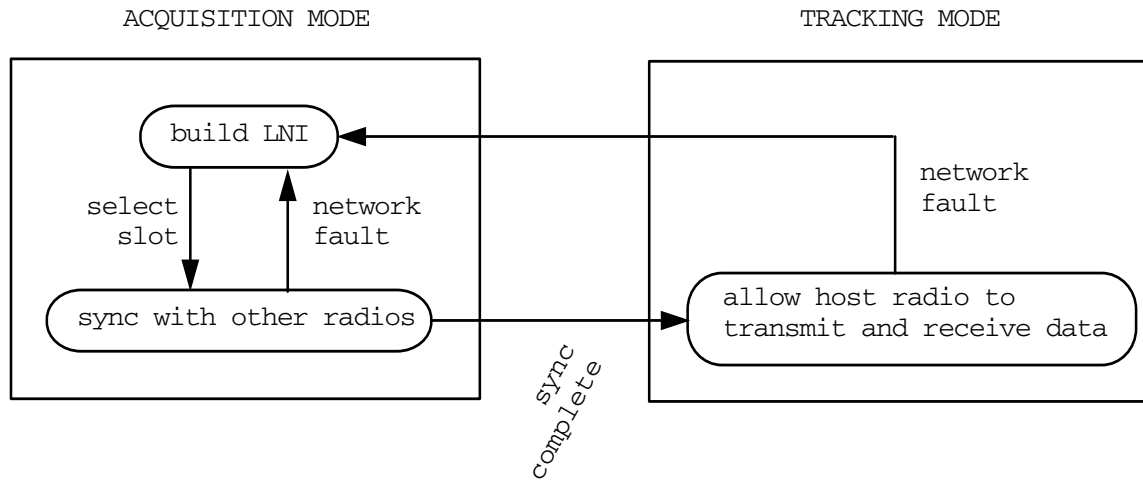
Slot acquisition is accomplished using the DSP embedded controller. Upon activation, each SSCS radio enters the acquisition mode. During this period, the unit forms an LNI of the current network configuration based upon both direct observations of transmitters and received SW data describing the current network images of other users. The LNI created by the acquiring radio includes the slot allocations of SSCS units that the acquiring radio is unable to receive directly because of insufficient link margin, provided that a complete relay path exists via other SSCS units (e.g., radio A in Figure 19-13).

The initial construction of the LNI continues until a randomly generated timeout of approximately 0.53 to 1.0 second (66 to 128 frames). (This time period does not include the initial bootup and configuration of the SSCS radio hardware.) At timeout, the embedded controller selects an unoccupied slot from the LNI and synchronizes the start of the acquiring radio's frame with the chosen slot. Once the radio measures a sufficiently low synchronization error, the controller enters tracking mode. Note that a controller that reaches timeout without receiving other radios selects slot 0 and enters the tracking mode without adjusting its phase.

In the tracking mode, the modem accepts user data from the BSP, assembles and transmits slots to other radios, recovers user and network status data from received signals, and passes user data from other radios to the BSP. The controller generates SWs for transmission to other radios and processes SWs received from other radios. The controller also monitors the network for slot conflicts of a loss-of-network condition



and returns to the acquisition mode if necessary. See Figure 19-14 for a pictorial representation of the acquisition and tracking modes.

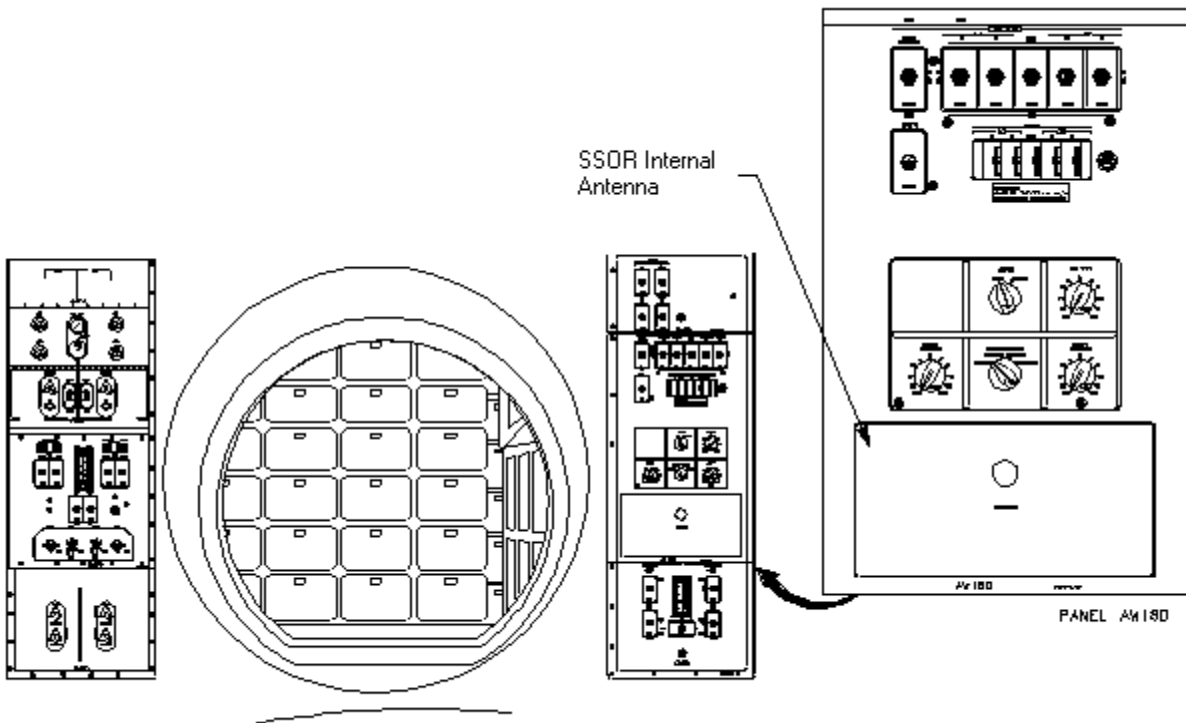


**Figure 19-14. Acquisition and tracking modes**

**19.2.3 Transceiver**

**19.2.3.1 Antenna Distribution**

The SSOR is has two physical Antennas. The internal SSOR antenna location is shown in Figure 19-15. The External SSOR antenna is located on the Orbiter Docking System (ODS) support truss just aft and slightly starboard of the ODS. RF Protect constraints are listed in the EVA checklist for Crew Members physical distance to the SSOR Antenna in low power.



186111703.ART, 1

**Figure 19-15. Internal SSOR antenna location**

### 19.2.3.2 Transmitter

The transmitter receives a -5 dBm input signal from the modem at 21.1568 MHz (for a data input of 1) and 21.6433 MHz (for a data input of 0). The IF center frequency is 21.4 MHz. The input signal is ac-coupled into the transmitter through a 4700 pF capacitor.

#### 19.2.3.2.1 IF Lowpass Filter

Following the dc-blocking capacitor, the input to the transmitter is filtered by a lowpass filter. The purpose of the filter is to reduce the upper frequency harmonics produced by the modem, in particular the second harmonics of the IF and of the modem clock in the 40-55 MHz frequency band. The filter introduces approximately 3 dB of insertion loss, reducing the IF signal to -8 dBm.

#### 19.2.3.2.2 Up-Converter

The IF signal is then up-converted to the desired output frequency. When the SSCS radio is in low frequency mode, the transmit IF of 21.4 MHz is mixed with a local oscillator signal of 392.8 MHz, resulting in output signals of 414.2 and 371.4 MHz. When the SSCS radio is in high frequency mode, the transmit IF of 21.4 MHz is mixed with a local oscillator signal of 395.7 MHz, resulting in output signals of 417.1 and 374.3 MHz.

### **19.2.3.2.3 RF Bandpass Filters**

Following the up-conversion, the RF signal is passed through two bandpass filters to reduce the image frequencies of 371.4 and 374.3 MHz, as well as any other harmonics produced in the up-conversion. Following the two bandpass filters, the output signal level to the T/R switch in the transmitter is -2 dBm.

### **19.2.3.2.4 Transmit/Receive Switch**

A T/R switch is included in the transmitter after the bandpass filter to reduce the signal levels which can get into the receiver through the circulator in the duplexer. This switch ensures that there is not a transient or noise input into the Intermediate Power Amplifier (IPA) during receive portions of the TDMA frame. When the T/R control signal from the modem goes low, the RF signal is sent to the power amplifier. However, when the T/R control signal from the modem goes high, the RF signal is fed to a terminating 50-ohm resistor.

### **19.2.3.2.5 Attenuator**

An attenuator is placed before the IPA so that the IPA is not overdriven. After the attenuator, the input signal to the IPA is -13.4 dBm.

### **19.2.3.2.6 Intermediate Power Amplifier**

The IPA is made up of two RF amplifiers cascaded. After the RF signal is fed through the IPA, the expected output to the PA is +19.1 dBm.

### **19.2.3.2.7 Power Amplifier**

The Power Amplifier (PA) is a bipolar transistor configured so that transmitter signals are not produced when an SSCS radio is in the receive portion of the TDMA frame. Transient signals from the transmitter during this time period could cause errors in the receive data. The transistor typically has a 12.5 dB gain that results in an output power for the transmitter of +31.6 dBm or 1.44 W.

### **19.2.3.2.8 Transmitter dc/dc Converter Board**

The transmitter dc/dc converter board provides conversion of input power to +12 and +5 V dc. It also provides 5 V dc power to the oscillators in the receiver in response to inputs from the signal processor.

## **19.2.3.3 Receiver**

### **19.2.3.3.1 RF Bandpass Filter**

A bandpass filter is placed at the input to the receiver to filter spurious products from the duplexer low noise amplifier. The filter is rated for an average power of 1 watt.

#### **19.2.3.3.2 Low Noise Amplifier**

The Low Noise Amplifier (LNA) is used to provide gain in the receiver. The LNA is specified to operate under a maximum input level of +13 dBm. The maximum input level to the LNA is expected to be +10 dBm in the SSCS.

#### **19.2.3.3.3 Down-Converter**

The RF signal is down-converted from the received frequency to the IF of 21.4 MHz. When the SSCS radio is in low frequency mode, the received 414.2 MHz signal out of the receiver LNA is mixed with a local oscillator signal of 392.8 MHz, resulting in output signals of 807 and 21.4 MHz. When the SSCS radio is in high frequency mode, the received 417.1 MHz signal out of the receiver LNA is mixed with a local oscillator signal of 395.7 MHz, resulting in output signals of 812.8 and 21.4 MHz.

#### **19.2.3.3.4 IF Bandpass Filter**

An IF bandpass filter is placed between the output of the down-converter and the input to the demodulator to eliminate the image frequencies of 807 and 812.8 MHz, as well as other mixing products. The IF bandpass filter also provides the proper noise filtering prior to demodulation.

#### **19.2.3.3.5 Local Oscillator**

The high and low frequency local oscillators are colocated on one board in the receiver module. This board provides an output for the receiver and the transmitter. High or low frequency is selected based upon which oscillator receives power from the transmitter dc/dc converter board. The control signal to the transmitter dc/dc converter board is provided by the signal processor.

#### **19.2.3.4 Demodulator**

The primary function of the demodulator is to demodulate a frequency shift keying signal and provide the data output to the SSCS modem. A secondary function is to provide a coupled output of the IF signal.

### **19.2.4 Power Supply System**

#### **19.2.4.1 Power Distribution Board**

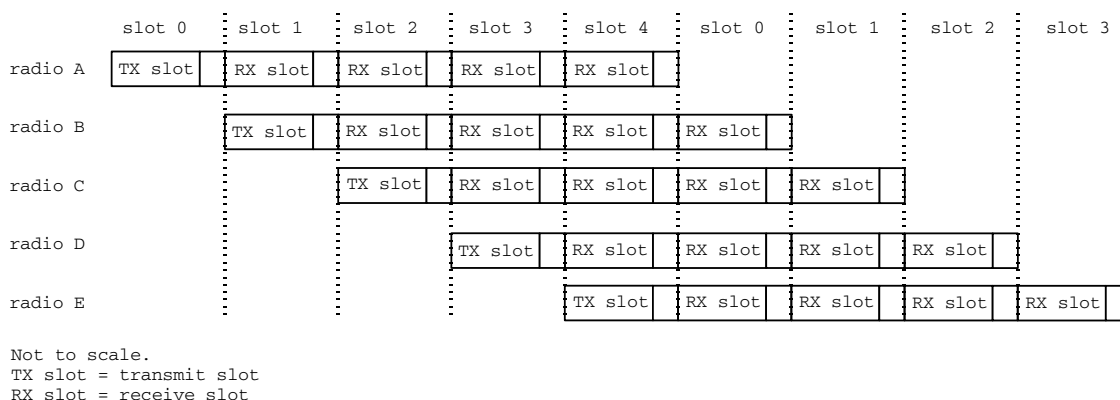
The SSOR power distribution board distributes the +28 V dc from the orbiter Main A power bus to the SSOR string 1 RF modules, Modem/Signal Processor Power Converter (MSPPC), and 1553 interface modules. The SSOR power distribution board distributes the +28 V dc from the orbiter main C power bus to the SSOR string 2 RF modules, MSPPC, and 1553 interface modules. The orbiter main A and main C power inputs can be active simultaneously or independently. In addition, it provides the mode control of the SSOR, including string selection, ON/OFF control, and control of the RF power switching. The SSOR power distribution board also provides a current sensor output for the SSOR (V74C2047A).

### 19.3 SSCS TDMA NETWORK

The SSCS TDMA system allows five users to communicate simultaneously by dividing each SSCS frame into five discrete periods of time (slots). Each user gets one slot in which to send its data to the SSCS network. See Figure 19-9 to see how the TDMA frame is designed.

#### 19.3.1 Local User Frames

In addition to the SSCS network frame, each SSCS radio has a local frame. The local frames are staggered such that each radio transmits at the start of their local frame. See Figure 19-16 to view the staggering of the local radio frames.



**Figure 19-16. Network frame synchronization**

#### 19.3.2 Acquisition and Tracking

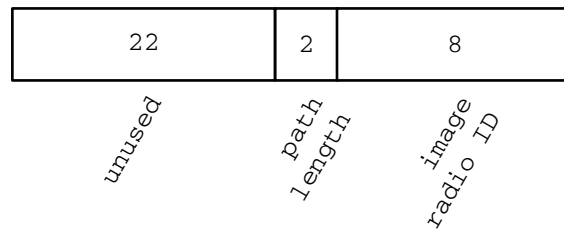
Upon activation, each SSCS radio goes into acquisition mode. In acquisition mode, the radio does not transmit and the radio does not pass on received data. The radio builds an LNI. The radio then selects an unoccupied slot from the LNI and synchronizes the start of its local frame with the chosen slot. Once the radio measures a sufficiently low synchronization error, the radio enters tracking mode. In tracking mode, the radio transmits data once per frame and passes on received data. For more information on acquisition and tracking mode, see Section 19.2.3.4.

##### 19.3.2.1 Local Network Image

Each radio builds an LNI based on received SW data. The LNI is used to pick a slot in acquisition mode, and it is used to maintain the network in tracking mode.

The actual LNI within the radio consists of a five-entry buffer indexed by slot entry. Each LNI entry consists of the radio ID of the occupant and the path length to the occupant. Figure 19-17 shows one of the five entries in the LNI buffer. For information about the use of the LNI, see Section 19.2.3.3.3, D. For information about purging absent radios from the LNI, see Section 19.2.3.3.3, E.

Not to scale. Field lengths in bits.



**Figure 19-17. LNI slot image format**

### 19.3.3 Network Faults

#### 19.3.3.1 PUNT Command

When any SSCS radio receives a PUNT reacquisition command via an SW, it returns to acquisition mode. A radio will transmit a PUNT command if there are discrepancies in the slot numbering system (i.e., large phase errors) or in response to slot conflicts in more than two slots. Discrepancies in the slot numbering system may occur if two independent SSCS networks were combined. The radio transmitting the PUNT command will transmit it for 12 consecutive frames and then return to acquisition mode. If the radio transmitting the PUNT command receives the PUNT command from another radio, it returns to acquisition mode immediately.

#### 19.3.3.2 Two Radios In Same Slot

If a radio receives an SRL (Section 19.2.3.3.3, B) containing the slot index that it is occupying, it will return to acquisition mode. Furthermore, if any radio receives evidence via an SW that another radio is occupying its transmit slot, it will return to acquisition mode.

#### 19.3.3.3 No Acknowledgment from Network Members

If a radio fails to receive any acknowledgment from other network members over an entire tracking mode timeout period, the controller returns to the acquisition mode.

#### 19.3.3.4 All Slots Occupied

If a radio is trying to join the network and all slots are occupied, the radio remains in acquisition mode until a slot is available.

### 19.3.4 Specific Network Cases

#### 19.3.4.1 Single Radio Network

Assuming that one radio is starting a network, when the radio builds its LNI, it will not see any other radios. It will choose slot 0 and enter tracking mode. However, it considers it a fault when it does not receive any acknowledgment from other network

members, and it will go back to acquisition mode. This cycling between acquisition and tracking mode is called pinging. The SSCS will continue this cycling until a second radio is added to the network.

#### **19.3.4.2 Temporarily Isolated Radio**

A radio that is temporarily isolated will begin to ping, but retains its transmit slot for up to 30 seconds. The blocked radio returns to its transmit slot without disrupting the network when the blockage problem is resolved, provided that other events do not cause the reorganization of the network or that the blockage does not last too long. If other events do cause the reorganization of the network or the blockage does last too long, the returning radio selects a new slot without affecting the network.

#### **19.3.4.3 Failed Receiver**

A radio that cannot receive any other radios but can itself be received by them is unable to acquire the network and pings continuously. Other radios able to receive the pinging radio select slots and adjust their phases to avoid contention, so the pinging radio does not prevent the formation of a stable network.

#### **19.3.4.4 Failed Transmitter**

A radio that can receive the other radios in the SSCS network but cannot itself be received also pings continuously but does not affect the network.

### **19.4 SSOR OPERATIONAL CONFIGURATION**

#### **19.4.1 Location**

The SSOR is located in avionics bay 3A.

#### **19.4.2 Electrical Requirements**

Table 19-4 shows the maximum power specified to be required by the SSOR, as well as the actual current draw measured on the STS-95 flight unit.

**Table 19-4. SSOR power requirements**

| Mode             | Power level | Actual current draw @ 28 volts, amps* | Max. power req'd, watts** | Period of use   |
|------------------|-------------|---------------------------------------|---------------------------|-----------------|
| TDMA             | High        | 1.21                                  | 56                        | Orbit           |
| TDMA             | Low         | 0.74                                  | 30                        | Orbit           |
| Transmit only    | High        | 3.57                                  | 150                       | Ground use only |
|                  | Low         | 0.93                                  | 150                       | Ground use only |
| Receive only     | N/A         | 0.71                                  | Not specified             | Ground use only |
| Transmit pattern | High        | 1.21                                  | Not specified             | Ground use only |
|                  | Low         | 0.74                                  | Not specified             | Ground use only |
| OFF              |             | Not measured                          | 5                         | N/A             |

\*Actual data on the SSOR that was delivered to KSC for STS-95.

\*\*Max power required in SPEC.

### 19.4.3 Cooling Requirements

The SSOR is designed to use forced air cooling. However, it is able to operate indefinitely without forced air cooling in low power mode. The SSOR is able to operate for 30 minutes without forced air cooling in high power mode.

### 19.4.4 Mechanical Requirements

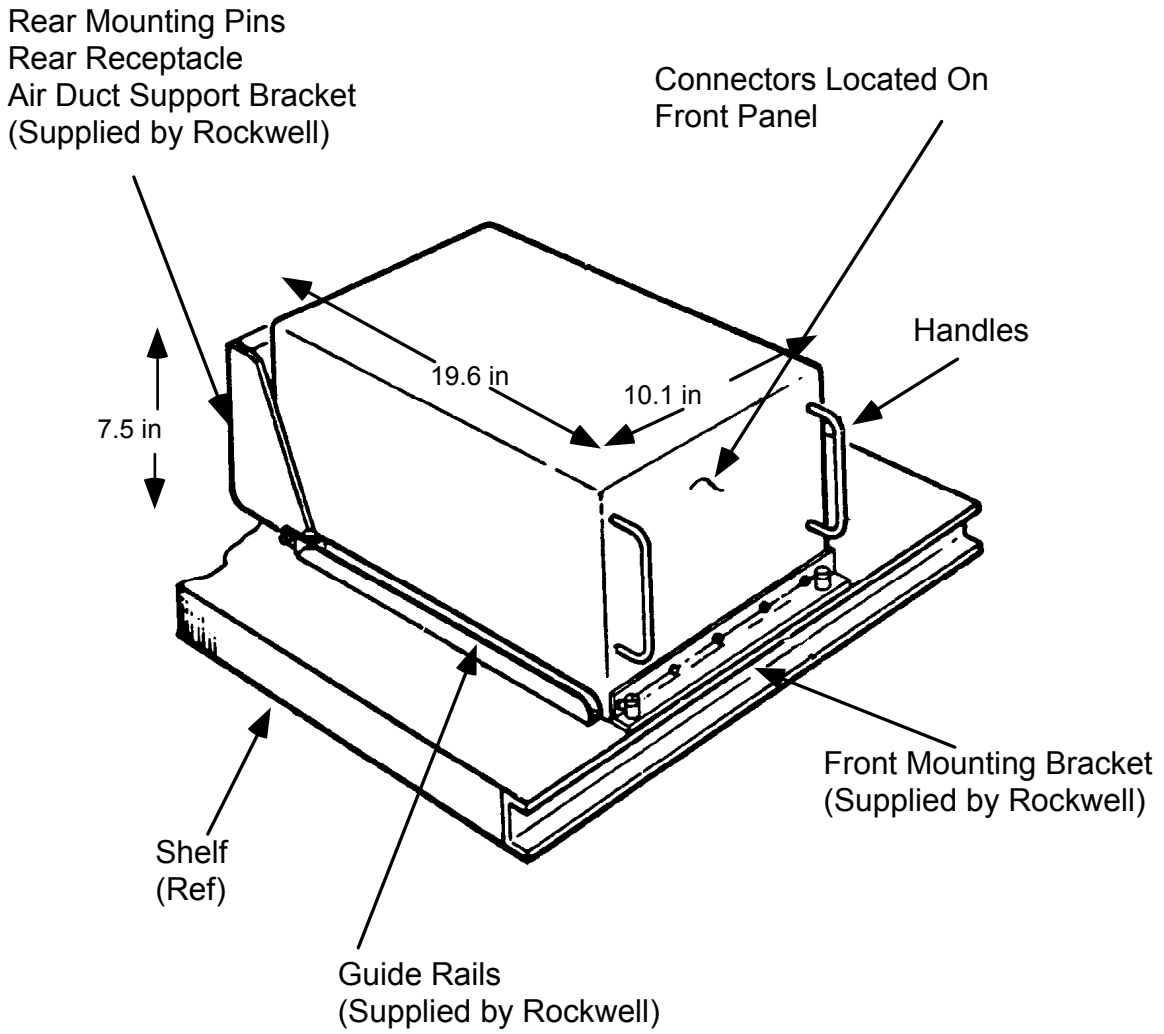
The SSOR weighs less than 30 pounds. An outline of the SSOR is shown in Figure 19-18.

### 19.4.5 Nominal Operational Configuration

For EVA operations, the SSOR is nominally configured for EVA string 1, EVA frequency 414.2 MHz, and EVA power amp off.

For Space Station rendezvous operations, the SSOR is nominally configured for EVA string 1, EVA frequency 414.2 MHz, EVA power amp on, and UHF encryption on.





**Figure 19-18. Mechanical outline of SSOR**

## 19.5 REFERENCES

- A. Vang: Time Division Multiple Access (TDMA) Design & Radio Networks presentation. SSCS Radio Critical Design Review, May 1997. ([http://www4.jsc.nasa.gov/eaprojects/sscs/cdr\\_radio/cdr\\_presentation/network.ppt](http://www4.jsc.nasa.gov/eaprojects/sscs/cdr_radio/cdr_presentation/network.ppt))
- B. Ziemer and Tranter: Principles of Communications: Systems, Modulation, and Noise. John Wiley & Sons, Inc., 1995. (<http://usa1.unitedspacealliance.com/sfocdata/SELS/JSC/11174/11174.PDF>)
- C. Design Document, Space to Space Communications (SSCS) Embedded Network Controller. JSC-27788, May 1997. ([http://www4.jsc.nasa.gov/eaprojects/SSCS/Documents/Baseline\\_Released/System/Networkddd/jsc27788.doc](http://www4.jsc.nasa.gov/eaprojects/SSCS/Documents/Baseline_Released/System/Networkddd/jsc27788.doc))
- D. OV-103 Panel Photos. (<http://stic.jsc.nasa.gov/collections/Photos/VITO>)
- E. Space Shuttle Systems Handbook, Rev F. JSC-11174, Sept 1997. (<http://usa1.unitedspacealliance.com/sfocdata/SELS/JSC/11174/11174.PDF>)
- F. Space-to-Space Orbiter Radio Detailed Design Document, Baseline. JSC-28157, April 1998. ([http://www4.jsc.nasa.gov/eaprojects/sscs/documents/baseline\\_released/ssor/ddd/jsc28157.doc](http://www4.jsc.nasa.gov/eaprojects/sscs/documents/baseline_released/ssor/ddd/jsc28157.doc))
- G. Specification, Space to Space Orbiter Radio (SSOR), Rev A. JSC-26799, July 1997. ([http://www4.jsc.nasa.gov/eaprojects/sscs/documents/baseline\\_released/ssor/spec/jsc26799B.doc](http://www4.jsc.nasa.gov/eaprojects/sscs/documents/baseline_released/ssor/spec/jsc26799B.doc))
- H. STS-95 Master Measurements List. (<http://p51.ksc.nasa.gov/seekmmlmsidd.html>)

THIS PAGE INTENTIONALLY BLANK

**SECTION 20 - COMMUNICATIONS AND INSTRUMENTATION SYSTEM  
WATER AND AIR-COOLED EQUIPMENT**

**CONTENTS**

| <b>Section</b> |                                       | <b>Page</b> |
|----------------|---------------------------------------|-------------|
| 20.1           | GENERAL .....                         | 20-1        |
| 20.2           | WATERFLOW DISTRIBUTION SYSTEM.....    | 20-1        |
| 20.2.1         | Water Coolant System Description..... | 20-6        |
| 20.2.2         | Coldplate Temperature TM.....         | 20-9        |
| 20.3           | AIRFLOW DISTRIBUTION SYSTEM.....      | 20-9        |
| 20.3.1         | Convection Air Cooling .....          | 20-9        |
| 20.3.2         | Forced Air Cooling.....               | 20-11       |
| 20.3.3         | AirFlow System TM.....                | 20-15       |
| 20.3.4         | References .....                      | 20-16       |

**FIGURES**

| <b>Figure</b> |  |       |
|---------------|--|-------|
| 20-1          | Digital Television - Aft flight deck payload station (L10) ..... | 20-3  |
| 20-2          | OIU - Aft flight deck payload station (L11).....                 | 20-4  |
| 20-3          | Coldplate installation.....                                      | 20-5  |
| 20-4          | Coolant waterflow distribution, bay 1 and bay 2 .....            | 20-7  |
| 20-5          | Bay 3A and bay 3B .....  | 20-8  |
| 20-6          | Water coolant loop block diagram .....                           | 20-10 |
| 20-7          | Flight deck air ducting.....                                     | 20-12 |
| 20-8          | Middeck air ducting.....   | 20-13 |
| 20-9          | ECLSS bay air ducting.....                                       | 20-14 |

THIS PAGE INTENTIONALLY BLANK

## SECTION 20 COMMUNICATIONS AND INSTRUMENTATION SYSTEM WATER AND AIR-COOLED EQUIPMENT

### 20.1 GENERAL

Communication and instrumentation electronic Line Replaceable Units (LRUs) are cooled by the H<sub>2</sub>O cooled distribution system (coldplates) or airflow system (convection air or forced air).

### 20.2 WATERFLOW DISTRIBUTION SYSTEM

The following communication and instrumentation LRUs are mounted on dual coldplates, except the S-band antenna switch and the switch beam control electronics.

#### Bay 1 LRUs

ACCU 1/2 - Audio center control unit  
CIU - Communications interface unit  
MDM PF 1 - Payload 1 Multiplexer/Demultiplexer (MDM)  
P/L DATA INTLV - Payload data interleaver (FLT 5)  
MMU 1 - Solid State Recorder 1  
PCM MAST 1 - PCM master unit 1  
SIG COND OF 1 - Dedicated signal conditioner OF 1  
MDM OF 1

#### Bay 2 LRUs

MDM PL 2 - Payload 2 MDM  
MMU 2 = Solid State Recorder 2  
P/L SP 1 - Payload signal processor 1  
P/L SP 2 - Payload signal processor 2  
P/L INTER 1 - Payload interrogator 1  
P/L INTER 2 - Payload interrogator 2  
PCM MAST 2 - PCM master unit 2  
SIG COND OF 2 - Dedicated signal conditioner OF 2  
MDM OF 2

Bay 3A LRUs

COM SEC 1 - Communications security no. 1  
COM SEC 2 - Communications security no. 2  
FM XMT 1 - S-band Frequency Modulator (FM) transmitter 1  
FM XMT 2 - S-band FM transmitter 2  
GCIL - Ground command interface logic  
KU-BD COMM A1 - Ku-band electronics no. 1  
KU-BD COMM A2 - Ku-band electronics no. 2  
MDM FF-3 - Flight forward 3 MDM  
NSP 1 - Network signal processor 1  
NSP 2 - Network signal processor 2  
MDM OF 3  
S/B ANT SW - S-band quad antenna switch (air-cooled only)  
S/B PWR AMP 1/2 - S-band power amplifiers 1 and 2  
S/B PRE AMP 1/2 - S-band preamplifiers 1 and 2  
S/B SW BEAM - S-band switch beam electronics (air-cooled only)  
S/B XPNDR 1 - S-band transponder 1  
S/B XPNDR 2 - S-band transponder 2  
SIG COND 3 - Dedicated signal conditioner OF 3  
MDM OF 3  
UHF EVA ATC - Ultrahigh Frequency (UHF) transceiver  
SSOR - Space to Space Orbiter Radio  
COMSEC 3 - encryption bypass isolation unit

Bay 3B LRUs

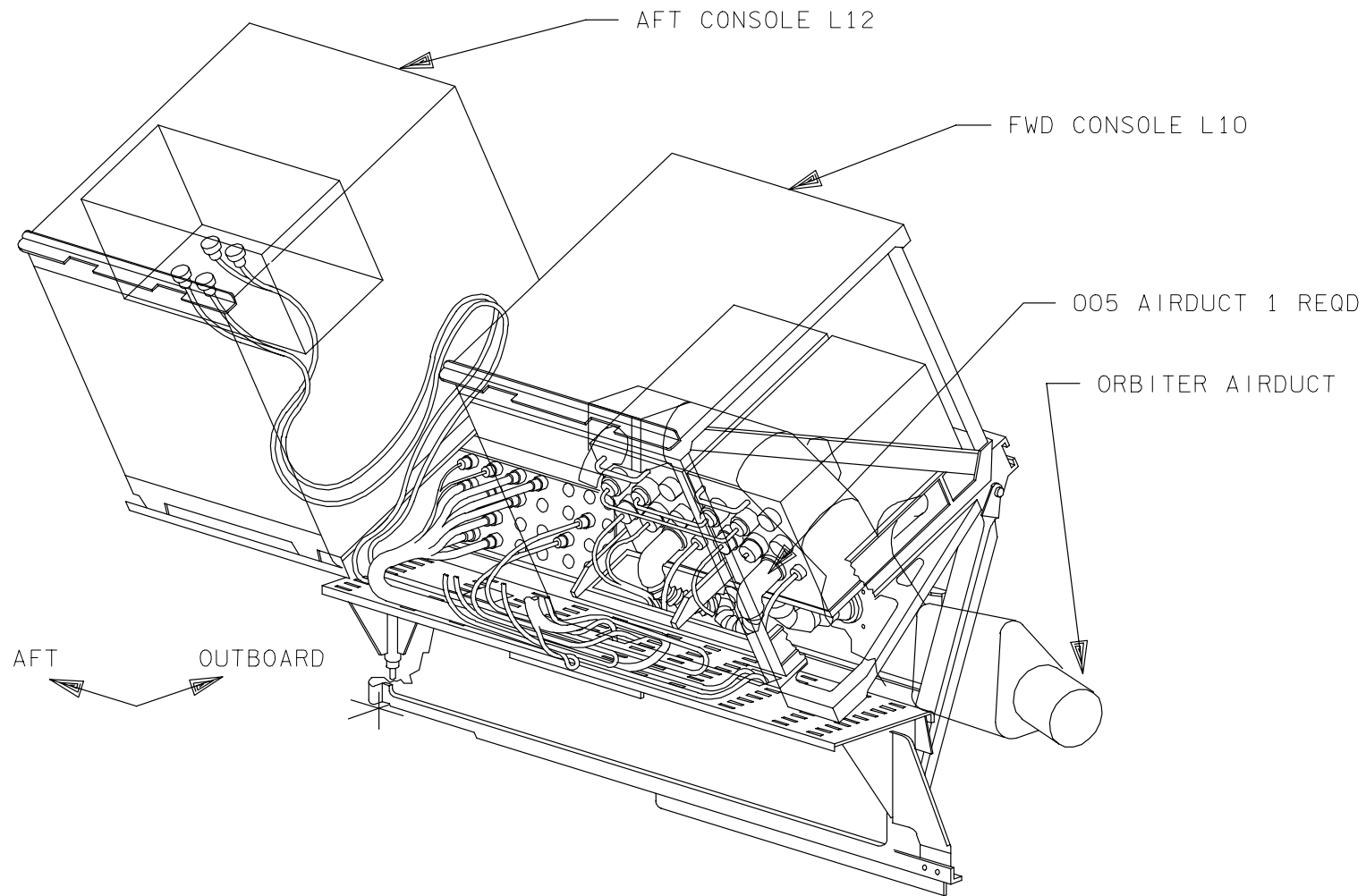
KU-BD SP - Ku-band signal processor  
MTU - Master timing unit

Aft flight deck payload station LRUs

L10 - Digital Television  
L11 - Orbiter Interface Unit(s)  
R12 - Video Processing Unit (VPU)

Figure 20-3 shows an isometric drawing of the coldplate installation.

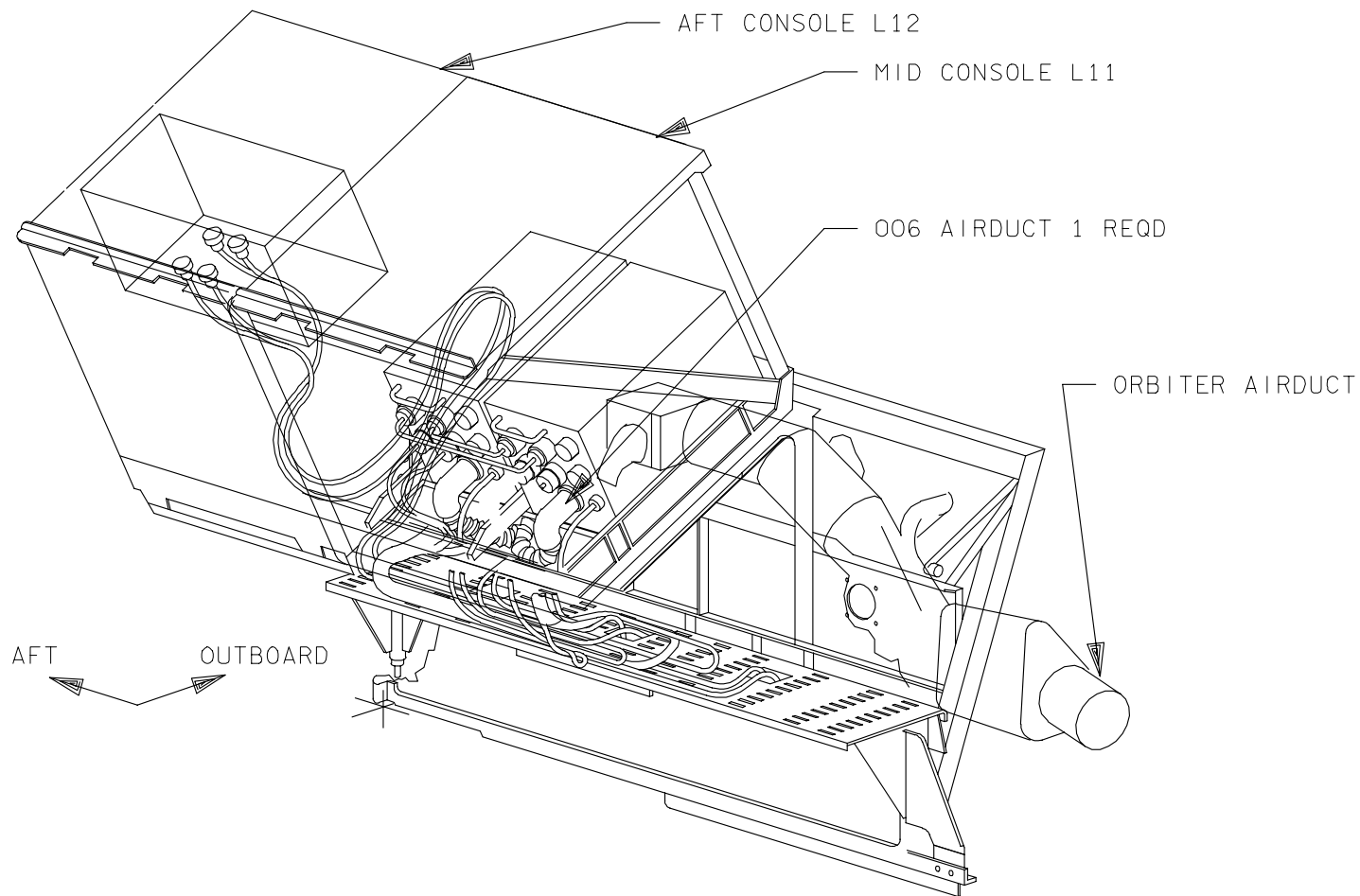
For more schematic detail of the H<sub>2</sub>O loop refer to Space Shuttle System Handbook (SSSH) Drawing 7.4, ARS H<sub>2</sub>O Coolant Loops.



186112001. ART# 1

**Figure 20-1. Digital Television - Aft flight deck payload station (L10)**





186112002. ART; 1

**Figure 20-2. OIU - Aft flight deck payload station (L11)**

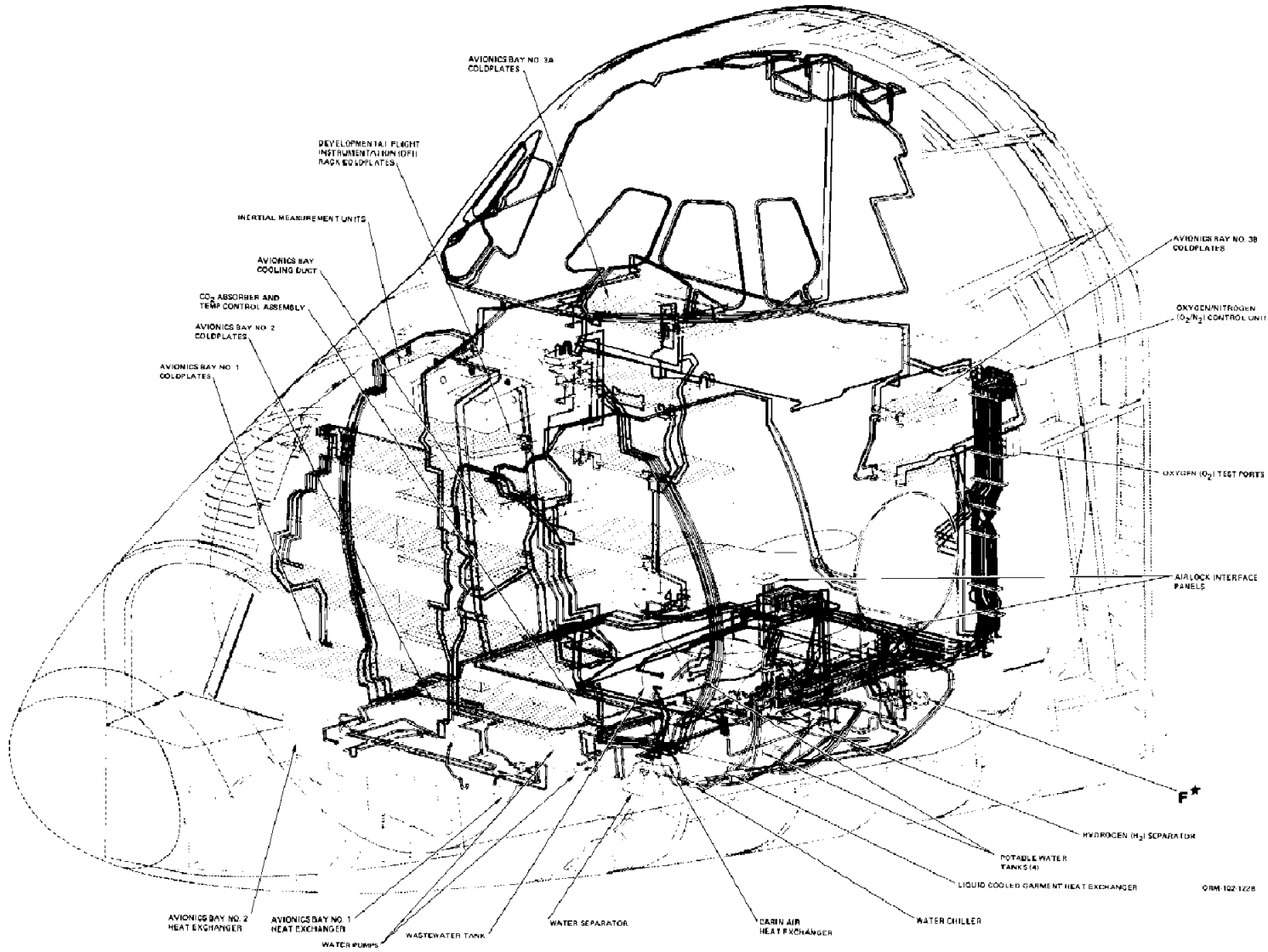


Figure 20-3. Coldplate installation

### 20.2.1 Water Coolant System Description

Figure 20-4 and Figure 20-5 show the location of the LRUs on the coldplate shelves and the water loop flow direction and distribution through the coldplates. The coldplates are part of the water loop coolant system shown in Figure 20-3.

Each coldplate has two water loops flowing through it. The coldplate is arranged in a sandwich fashion between the shelf and the LRU. Loop 1 is next to the LRU and loop 2 next to the shelf.

The two complete and separate water coolant loops flow side by side through the same areas. Loop 1 has two pumps and loop 2 only one. A controlled amount of water through the H<sub>2</sub>O Freon interchanger is maintained by a bypass controller valve which is regulated by the sensed pumpout temperature. Both loops are used for ascent and entry; loop 2 is used on orbit.

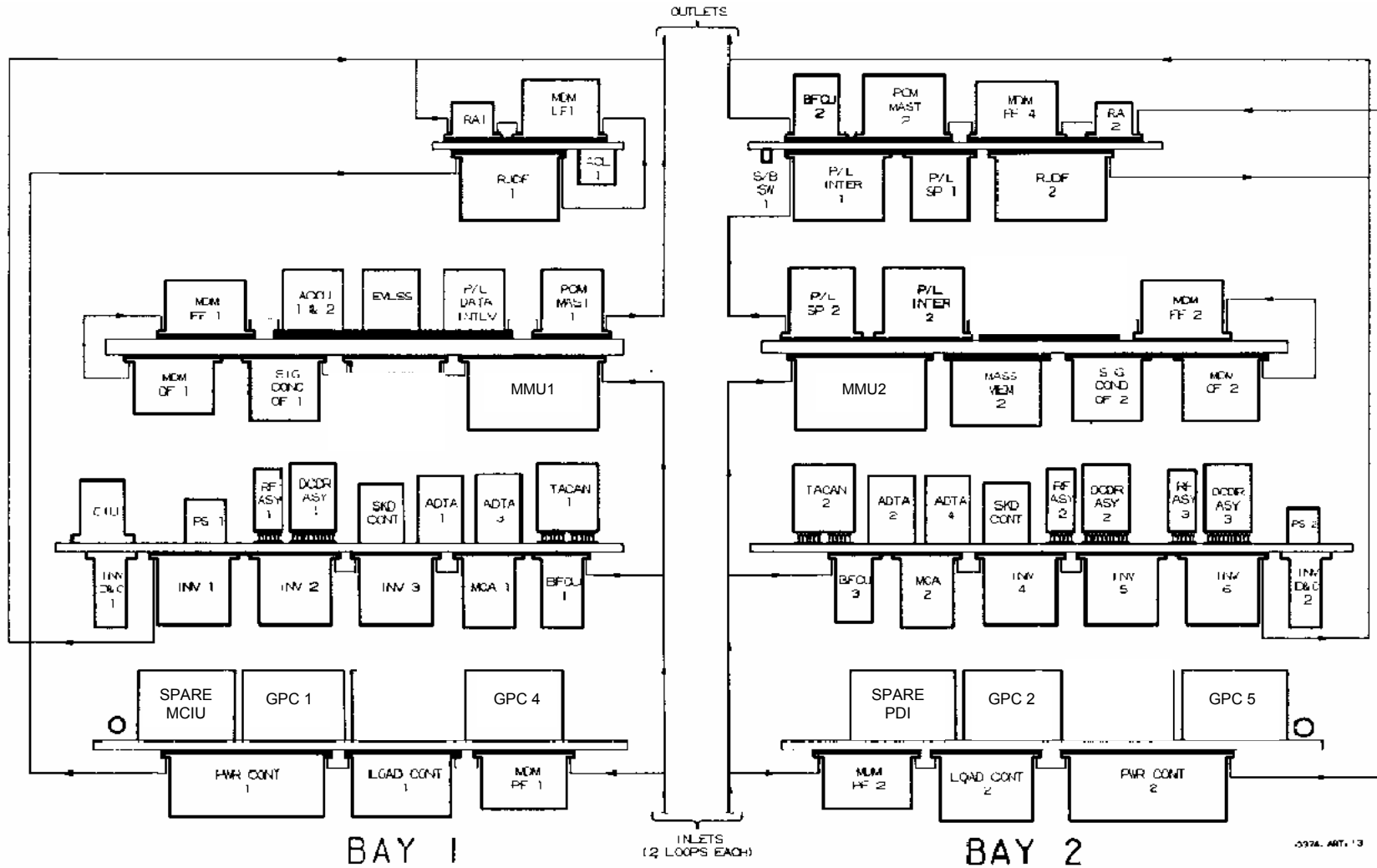


Figure 20-4. Coolant waterflow distribution, bay 1 and bay 2

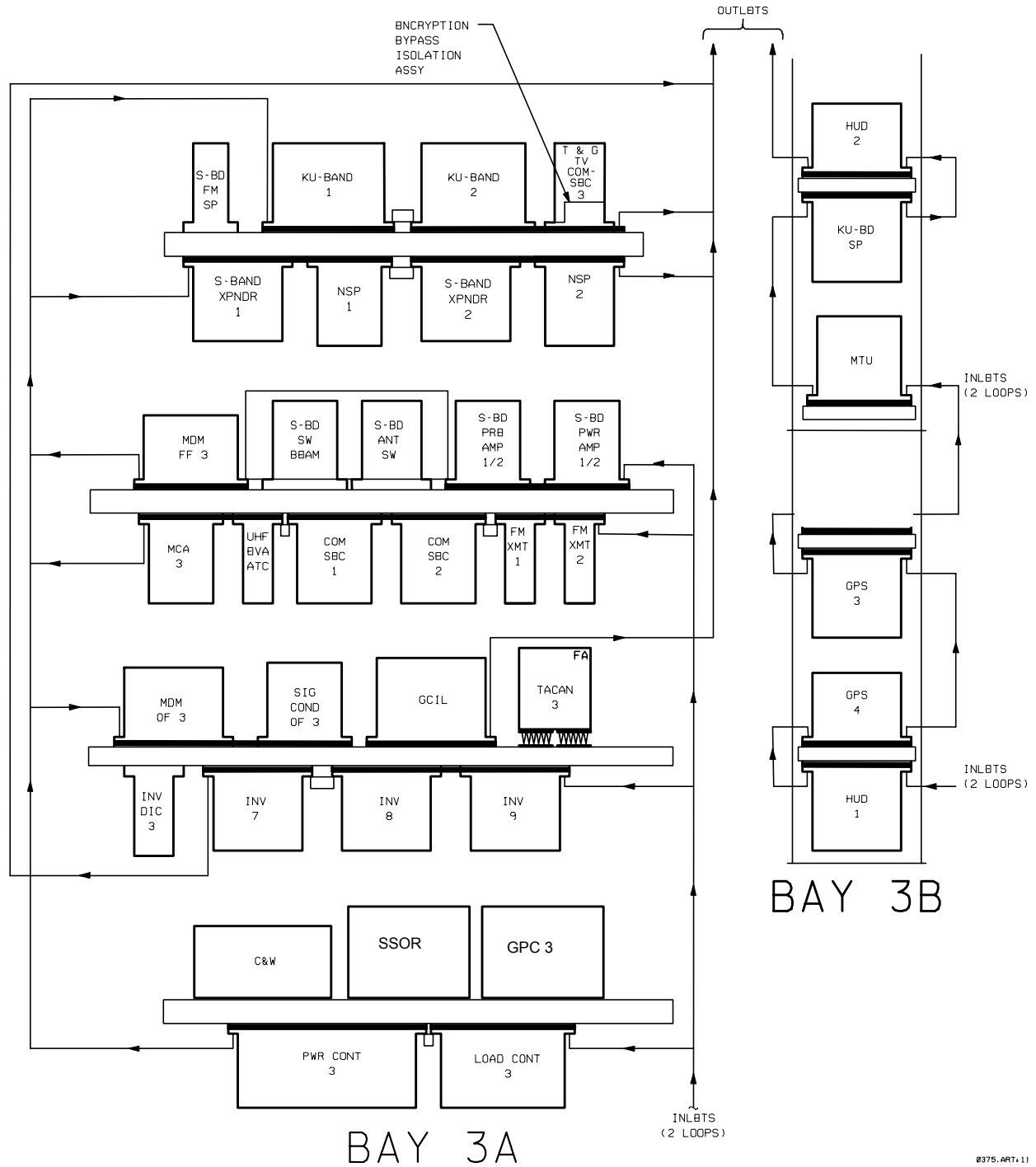


Figure 20-5. Bay 3A and bay 3B

0375.ART.11

## 20.2.2 Coldplate Temperature TM

The water temperature flowing into and out of the coldplates can be monitored by the following Telemetry (TM).

Note: Normally two loops are used for launch and entry, and loop 2 for orbit.

### Avionics Bay 1

V61T2615A LP 1 H<sub>2</sub>O AV BAY 1 HX OUT TEMP  
V61T2624A LP 1 H<sub>2</sub>O AV BAY 1 C/P OUT TEMP  
V61T2616A LP 2 H<sub>2</sub>O AV BAY 2 HX OUT TEMP  
V61T2625A LP 2 H<sub>2</sub>O AV BAY 2 C/P OUT TEMP

### Avionics Bay 2

V61T2618A LP 1 H<sub>2</sub>O AV BAY 2 HX OUT TEMP  
V61T2627A LP 1 H<sub>2</sub>O AV BAY 2 C/P OUT TEMP  
V61T2619A LP 2 H<sub>2</sub>O AV BAY 2 HX OUT TEMP  
V61T2628A LP 2 H<sub>2</sub>O AV BAY 2 C/P OUT TEMP

### Avionics Bay 3A

V61T2621A LP 1 H<sub>2</sub>O AV BAY 3A HX OUT TEMP  
V61T2630A LP 1 H<sub>2</sub>O AV BAY 3A C/P OUT TEMP  
V61T2662A LP 2 H<sub>2</sub>O AV BAY 3A HX OUT TEMP  
V61T2631A LP 2 H<sub>2</sub>O AV BAY 3A C/P OUT TEMP

### Avionics Bay 3B

NO INLET/OUTLET TEMPERATURES

## 20.3 AIRFLOW DISTRIBUTION SYSTEM

The airflow distribution system consists of convection air cooling and forced air cooling of the avionics bay LRUs. Detail of the system can be found on SSSH schematics 6.2, Atmosphere Circulation and 7.4, ARS H<sub>2</sub>O Coolant Loops.

### 20.3.1 Convection Air Cooling

Avionics bays 1, 2, and 3A have two fans each. One fan in each bay provides the required airflow through the bay. The bay is not airtight and some air can pass into the cabin. The air circulated is cooled by the ARS H<sub>2</sub>O heat exchangers shown in Figure 20-6.

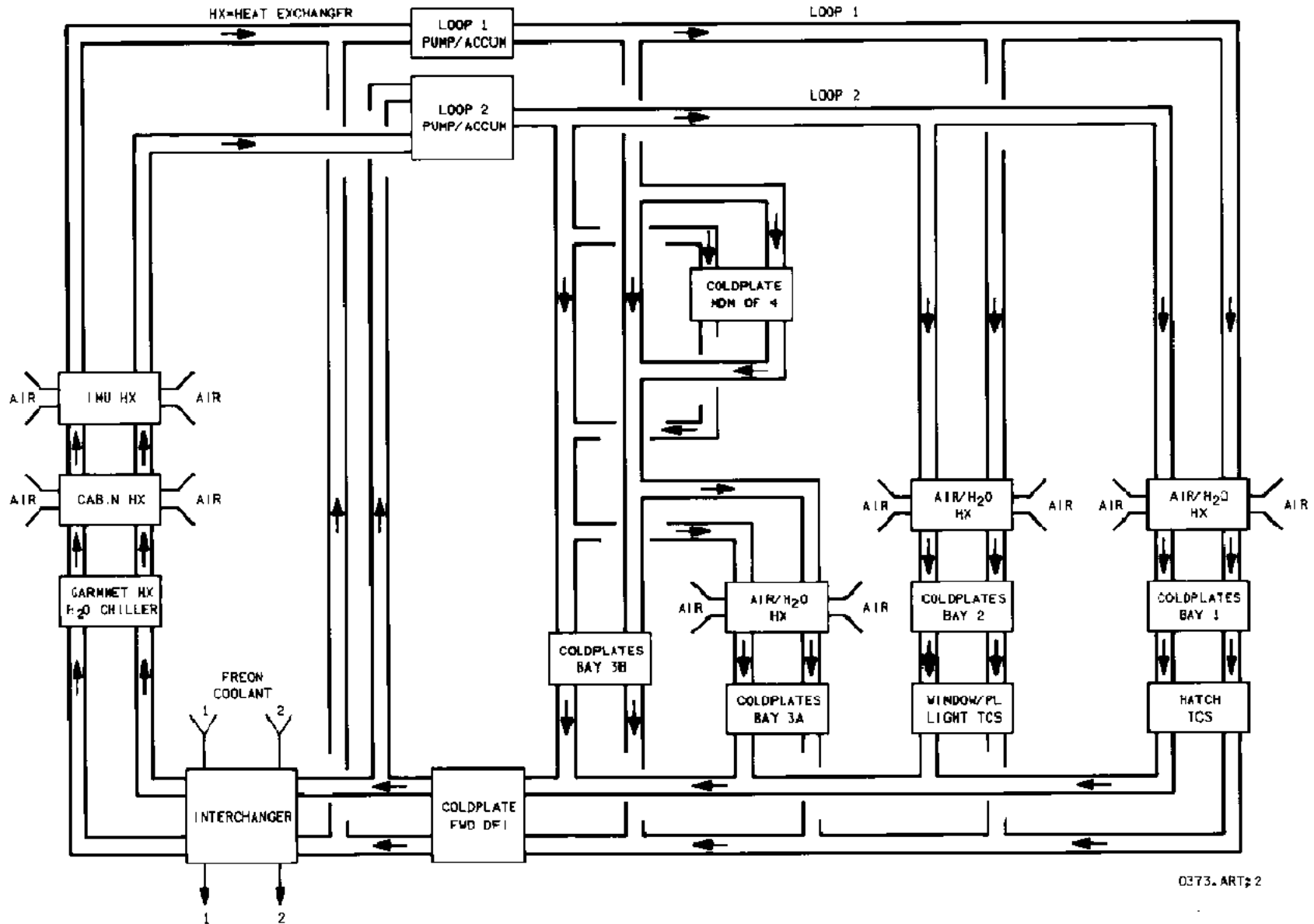


Figure 20-6. Water coolant loop block diagram

Convection Cooled Instrumentation/Communications LRUs

Bay 1

(None)

Bay 2

(None)

Bay 3A

S-band FM signal processor  
S-band FM multiplexer  
S-band quad antenna switch  
S-band FM RF switch  
S-band switch beam electronics

**20.3.2 Forced Air Cooling**

The forced air system has two fans. Air is either blown or sucked past the LRUs through the ducts shown in Figure 20-7. The cabin heat exchanger shown in Figure 20-8 cools the air. Environmental Control and Life Support System (ECLSS) bay air ducting is shown in Figure 20-9.

Forced Air-Cooled Instrumentation/Communications LRUs

Supply side (blown air)

Wideband (WB) mission recorder

Return side (suction air)

Remote Control Unit (RCU)\*

Video Select Unit (VSU)\*

TV monitor 1\*\*

TV monitor 2\*\*

MADS recorder

---

\*There is no time limit for operation if cooling is lost.

\*\*If cooling is lost and cabin is at 72° F and no monitor fault light, maximum operating time is 70 minutes. If cabin is at 95° F and no fault light, maximum operating time is 22 minutes.



- IMU - INERTIAL MEASUREMENT UNIT
- DEU - DISPLAY ELECTRONICS UNIT
- AVVI - ALTITUDE/VERTICAL VELOCITY INDICATOR
- VSU - VIDEO SWITCHING UNIT
- DDU - DISPLAY DRIVER
- AMI - ANGLE OF ATTACK/MACH INDICATOR
- RCU - TV REMOTE CONTROL UNIT
- MCIU - MANIPULATOR CONTROL INTERFACE UNIT
- DU - DISPLAY UNIT
- GFE - GOVERNMENT FURNISHED EQUIPMENT
- MSS - MISSION SYSTEM SPECIALIST

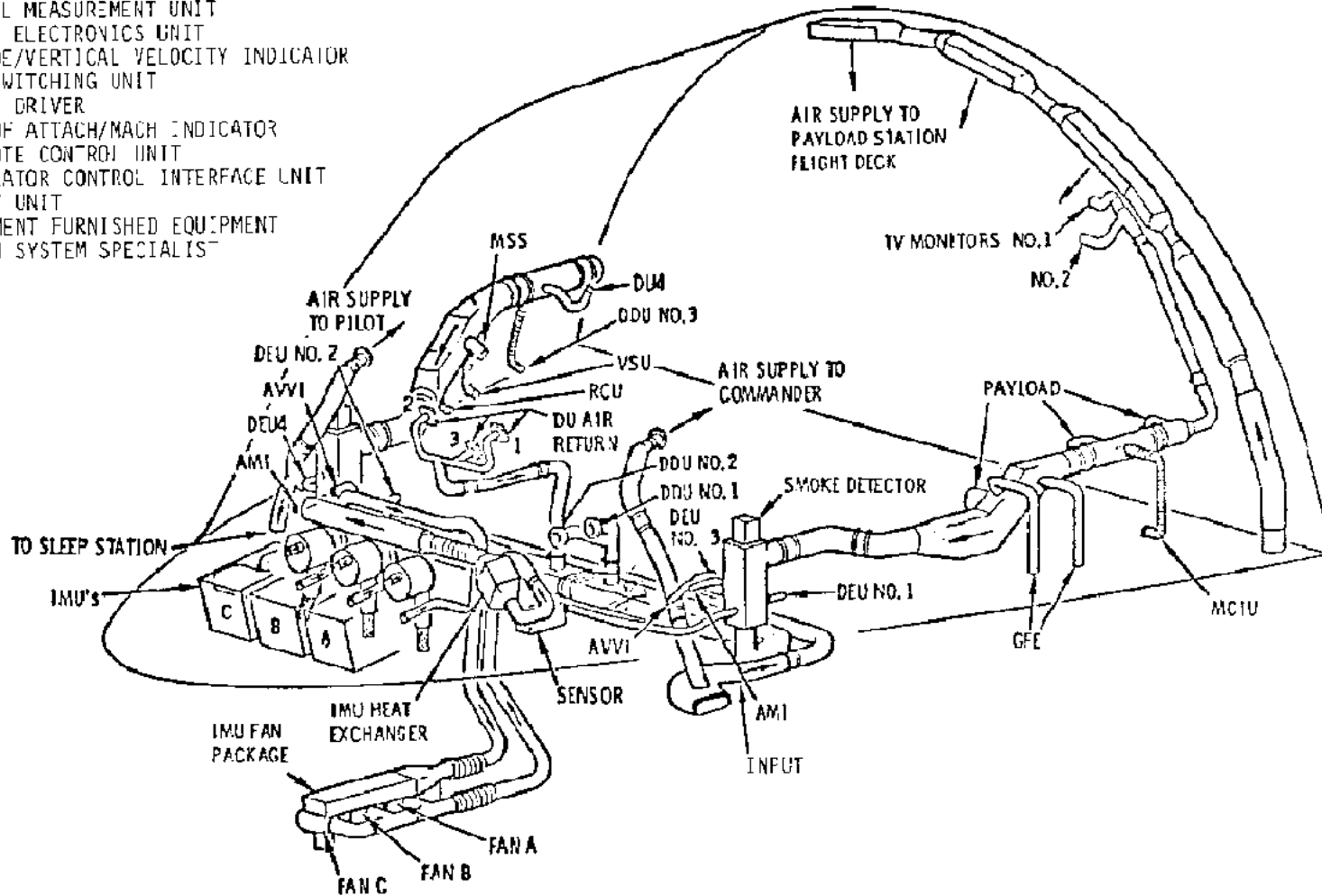


Figure 20-7. Flight deck air ducting

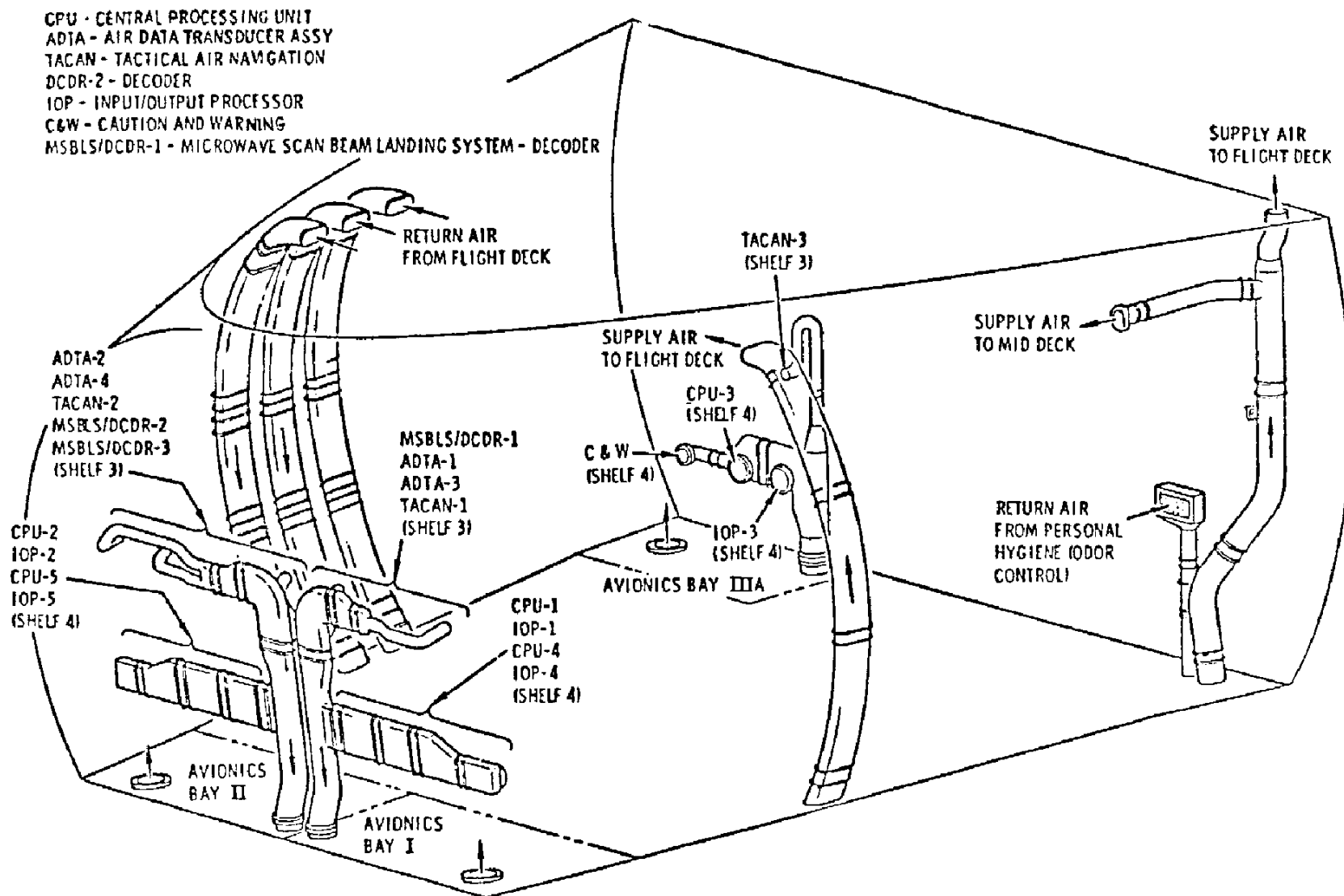


Figure 20-8. Middeck air ducting

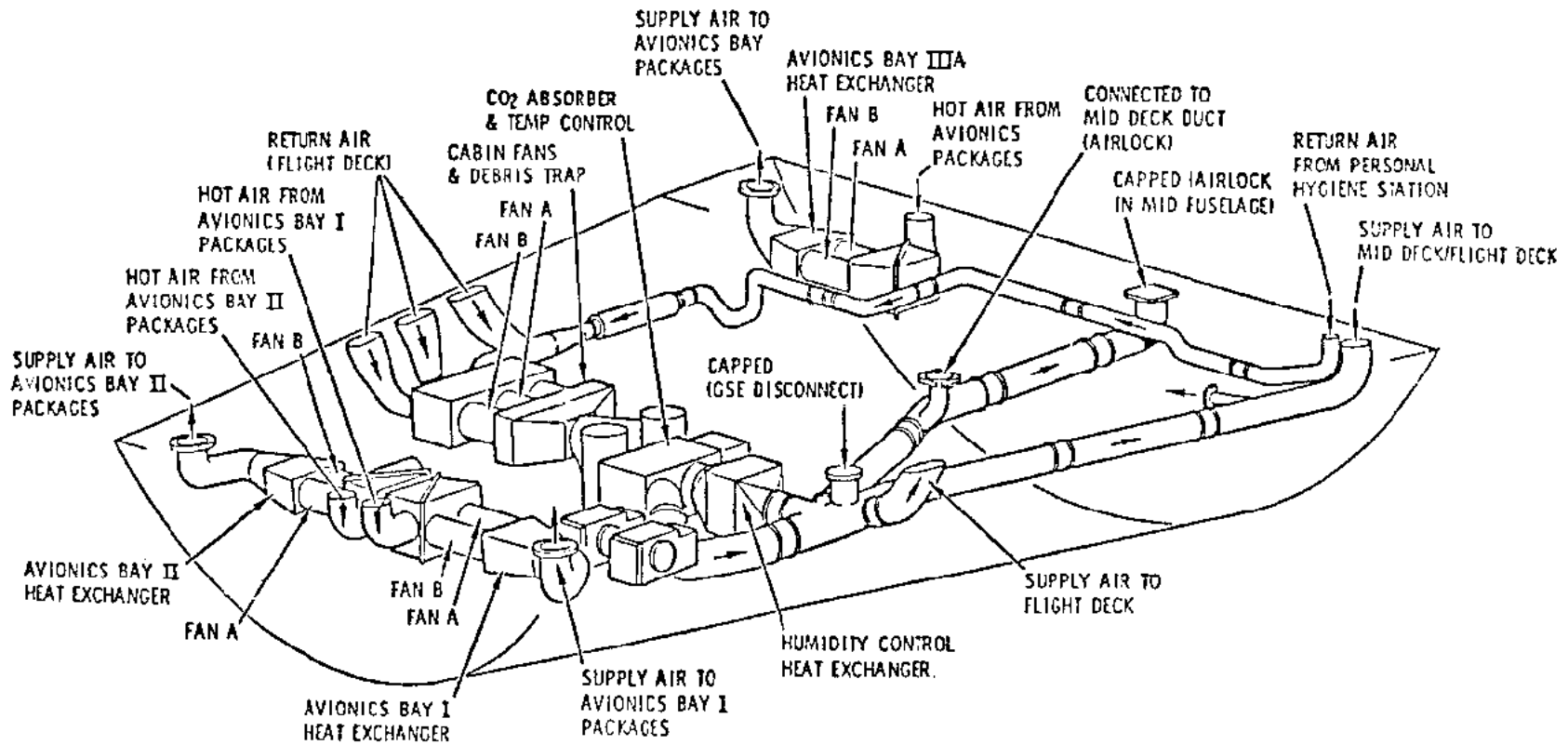


Figure 20-9. ECLSS bay air ducting

### 20.3.3 AirFlow System TM

The temperature of the air forced out of the cabin heat exchanger can be monitored on the following TM.

V61T2635A CAB HX AIR OUT TEMP

The temperature of the convection air into the bay 1, 2, and 3A heat exchangers can be monitored on the following TM.

V61T2645A AV BAY 1 AIR OUT TEMP

V61T2650A AV BAY 2 AIR OUT TEMP

V61T2661A AV BAY 3 AIR OUT TEMP

#### 20.3.4 References

V070-613360 Coolant Installation, Avionics Equipment, Forward Bays 1 and 2

V070-613361 Coolant Installation, Avionics Equipment, Crew Module, Bay 3B

V070-613362 Coolant Installation, Avionics Equipment, Crew Module, Bay 3A

V070-613760 Ducting Installation, Air Supply Flight Deck, ECLSS

V070-613780 Ducting Installation, Air Return Flight Deck, ECLSS

V070-613400 Ducting Installation, Avionics Bays 1, 2, and 3

V070-613650 TBS

V070-613724 TBS

V070-613438 Equipment Installation

V070-613999 Heat Exchanger Installation

V070-613891 ARS Water Coolant System Installation, Crew Module, Mid Deck to Flight Deck

V070-613890 Water System Installation, ARS Cooling Cabin, ECLSS

V070-703014 Equipment Installation - Forward Avionics Bay 3B

## SECTION 26 - ORBITER OPERATIONAL INSTRUMENTATION OVERVIEW

### CONTENTS

| <b>Section</b>                               | <b>Page</b> |
|--|-------------|
| 26.1 GENERAL DESCRIPTION .....               | 26-1        |
| 26.2 EXTERNAL INTERFACES .....               | 26-2        |
| 26.2.1 Description of Interfaces .....       | 26-2        |
| 26.3 DATA TYPES AND ROUTING .....            | 26-3        |
| 26.3.1 Description of Data Types .....       | 26-3        |
| 26.3.2 Data Routing .....                    | 26-4        |
| 26.4 OI EQUIPMENT AND OPERATION .....        | 26-4        |
| 26.4.1 Operation .....                       | 26-5        |
| 26.4.2 Crew Controls .....                   | 26-6        |
| 26.4.3 Ground Commands .....                 | 26-6        |
| 26.4.4 Operating Instructions .....          | 26-6        |
| 26.5 OI TELEMETRY .....                      | 26-7        |
| 26.6 MECHANICAL AND ELECTRICAL SUMMARY ..... | 26-9        |

### TABLES

| <b>Table</b>                            |       |
|---|-------|
| 26-1 OI equipment .....                 | 26-5  |
| 26-2 DSC/MDM telemetry parameters ..... | 26-8  |
| 26-3 PCMMU telemetry parameters .....   | 26-8  |
| 26-4 PDI telemetry parameters .....     | 26-9  |
| 26-5 OI electrical summary .....        | 26-10 |
| 26-6 OI mechanical summary .....        | 26-11 |

### FIGURES

| <b>Figure</b>                           |      |
|---|------|
| 26-1 OI system .....                    | 26-1 |
| 26-2 Real-time downlink data flow ..... | 26-4 |
| 26-3 Telemetry routing .....            | 26-7 |

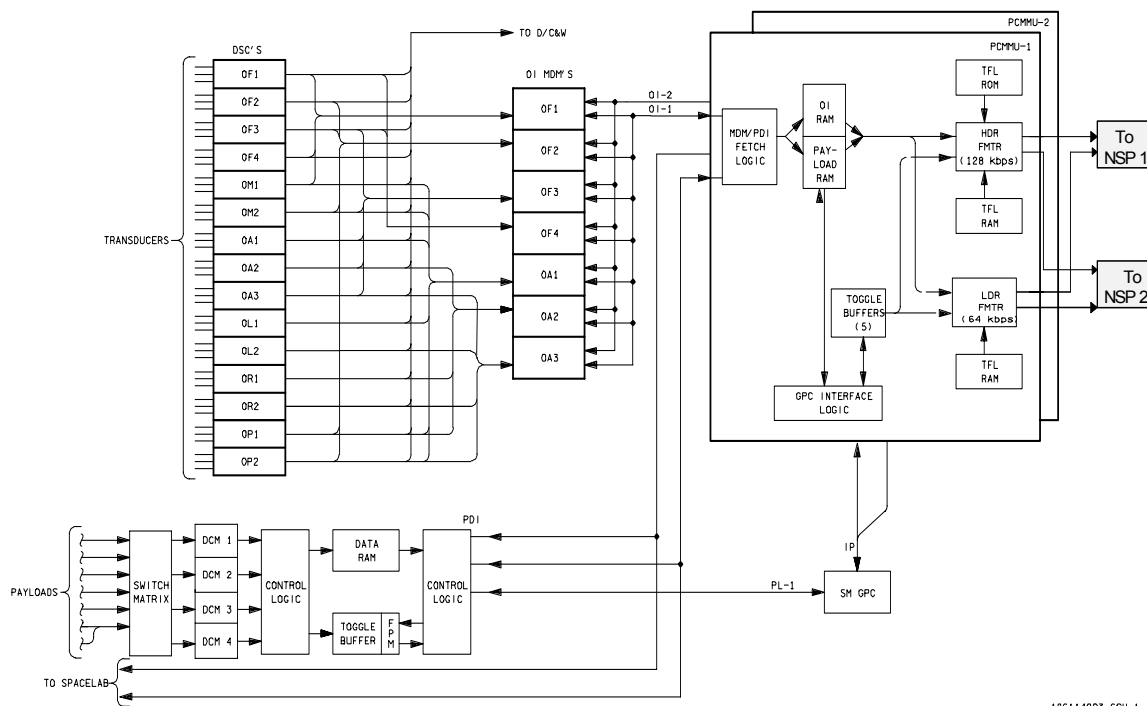
THIS PAGE INTENTIONALLY BLANK

## SECTION 26 ORBITER OPERATIONAL INSTRUMENTATION OVERVIEW

### 26.1 GENERAL DESCRIPTION

The orbiter Operational Instrumentation (OI) system contains equipment that is used to collect, route, and process information from sensors, such as transducers, located throughout the orbiter and its payloads. The telemetry collected from the sensors can be analog or digital. Once data is collected from the various sensors, the OI system digitizes (analog data only), scales, and stores the data. The stored data is then retrieved and assembled into two digital streams for downlink via the Ku-band or S-band communication system.

The OI system (Figure 26-1) equipment includes 14 Dedicated Signal Conditioners (DSCs), a Payload Data Interleaver (PDI), two Pulse Code Modulation Master Units (PCMMUs), encoding equipment, master timing equipment, onboard checking equipment, and seven Multiplexer/Demultiplexers (MDMs), called OI MDMs.



186114803, SCH 1

**Figure 26-1. OI system**



## 26.2 EXTERNAL INTERFACES

The OI system interfaces with the following orbiter systems and equipment:

- Sensors (Transducers)
- Payloads
- Electrical Power Distribution Subsystem (EPDS)
- Environmental Control and Life Support System (ECLSS)
- Data Processing System (DPS)
- Displays and Caution and Warning (D/C&W)

## 26.3 DESCRIPTION OF INTERFACES

### A. Sensors

Sensors are located throughout the orbiter and are an integral part of the orbiter systems, including payloads. Signal leads from each sensor are routed to a DSC then MDM in a serial manner or just to an MDM for signal processing and downlink. Sensors can include switches, thermistors, strain gages, logic gates, and transducers.

### B. Payloads

Telemetry data from the orbiter payloads is routed through the PDI to the PCMMU. The PDI is capable of interfacing to six payloads at a time: five “attached” (i.e., Spacehab onboard experiments) and one “deployed” (i.e., satellites). The PDI is configured premission via computer commands.

### C. EPDS

The EPDS is part of the orbiter Electrical Power System (EPS) and comprises three main buses and three essential buses. The main buses (28 V) are the prime source of dc power to orbiter electrical loads. The three main buses are powered by fuel cells and provide power to the OI system. Each OI system component is redundantly powered by two of the three buses through circuit breakers or Remote Power Controllers (RPCs).

### D. ECLSS

OI system components are installed throughout the orbiter and are located in Avionics (AV) bays 1 through 6. The OI system components installed in AV bays 1, 2, and 3 (and flight deck) are mounted on coldplates for water loop cooling. Similarly, components installed in AV bays 4, 5, and 6 are mounted on coldplates

for Freon loop cooling. All other components are mounted on surfaces (without coldplates) and are cooled by conduction.

E. DPS

The DPS receives data from the OI system via Instrumentation/PCMMU (IP) buses. These buses transmit the payload and orbiter instrumentation data from the PCMMUs to the Systems Management (SM) General Purpose Computers (GPCs). Likewise, the DSCs interface to Flight-Critical (FC) MDMs via FC data buses that interface with components needed for vehicle control.

F. D/C&W

Telemetry data from orbiter systems (EPS, ECLSS, Mechanical (MECH), Auxiliary Power Unit (APU), etc.) are routed from sensors to a DSC. The data can be received from the DSCs by an orbiter-dedicated display or Caution and Warning (C&W) system alarm. These data may also be routed to DPS and/or downlinked via the S-band or Ku-band systems (not discussed in this brief).

## 26.4 DATA TYPES AND ROUTING

There are three types of telemetry data that flow within the OI system:

- Orbiter (operational) data
- Payload data
- Downlist data

### 26.4.1 Description of Data Types

A. Orbiter (operational) data

Sensors, which include switches, thermisters, strain gages, logic gates, and transducers, all have output voltage signals. A sensor voltage output may have to be routed through a DSC to process, amplify, or convert its output to the 0-5Volts dc range to allow input into an MDM. The analog or discrete signals enter the MDM will be converted to digital data to allow the PCMMU to retrieve, store, and downlink to the ground. For crew safety, data from orbiter sensors that are used to announce fire, change in pressure, change in air quality, etc. are directly routed to the C&W system for crew notification.

B. Payload data

Payload data are originated as operational data and are received by the PDI as digital signals (IRIG standards). Once received, data are then buffered and passed on to the PCMMU for downlink.

Note: For detached payloads, data is received by the Payload Interrogator (PI) shipped to the PDI and to the K-Band system.

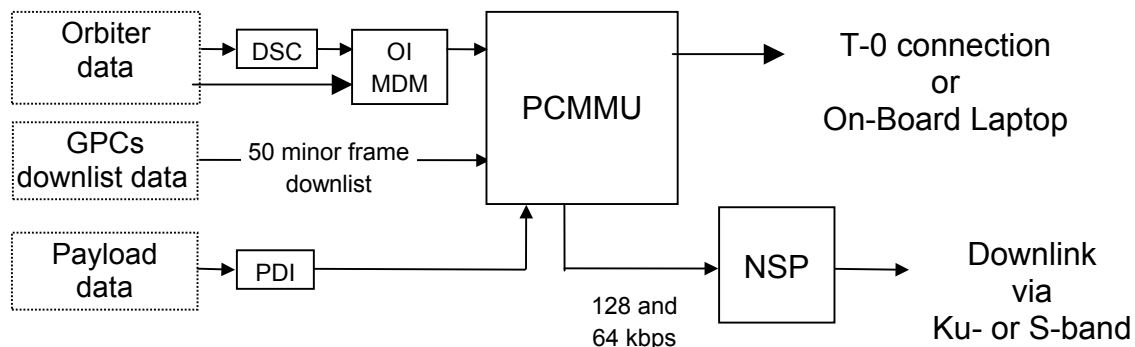
C. Downlist data

These data originate in one or more of the GPCs as 16-bit length words. They are used to maintain the status of onboard systems and are called the downlist. The GPC-collected data include a set of parameters that are chosen preflight. At the discretion of the GPCs, these data are sent on to the PCMMU.

**26.4.2 Data Routing**

Of the 3000 sensors onboard, approximately 60% need to be converted by the DSCs into output signals (0-5Volt dc) to allow them be read by the OI MDMs and, if need be, the FC MDMs. The OI MDMs collect and multiplex the signals, and send the data on to the PCMMU.

Each of the three types of data resides in memory modules within the PCMMU. The orbiter data and payload data reside in the OI Random Access Memory (RAM), the downlist data reside within toggle buffers. After each type of data is collected and stored in the respective memory modules, two formatters load data words into two PCM telemetry data streams (128 or 64 kbps) that are routed to the Network Signal Processor (NSP). The NSP combines the voice and data, then routes the combined information to the Radio Frequency (RF) systems (Ku- or S-band). See Figure 26-2. Downlink data rates range from 1 sample/sec to 100 samples/sec.



**Figure 26-2. Real-time downlink data flow**

**26.5 OI EQUIPMENT AND OPERATION**

The OI system components are installed throughout the orbiter and the temperature of each component is maintained by a specific cooling method. The OI system equipment list follows (Table 26-1). Each component is assigned a specific DSM number used to trace the component telemetry via software.

Table 26-1 lists the OI system components, Identification (ID) number, location, and cooling method.

### 26.5.1 Operation

The OI system requires minimal crew intervention during nominal flight activity. The system components are configured using ground command. Only abnormal situations require crew configuration changes onboard, specifically, Telemetry Format Loads (TFLs) and Decommutation Format Loads (DFLs).

**Table 26-1. OI equipment**

| Label         | ID       | Location       | Cooling method |
|---------------|----------|----------------|----------------|
| <b>DSCs</b>   |          |                |                |
| OF1           | 81V75A16 | AV bay 1       | Water loop     |
| OF2           | 82V75A17 | AV bay 2       | Water loop     |
| OF3           | 83V75A18 | AV bay 3       | Water loop     |
| OF4           | 22V75A22 | FWD RCS module | Passive        |
| OA1           | 54V75A19 | AV bay 4       | Freon loop     |
| OA2           | 55V75A20 | AV bay 5       | Freon loop     |
| OA3           | 56V76A21 | AV bay 6       | Freon loop     |
| OM1           | 40V75A23 | Mid fuselage   | Passive        |
| OM2           | 40V75A74 | Mid fuselage   | Passive        |
| OM3           | 40V75A80 | Mid fuselage   | Passive        |
| OL1           | 51V75A25 | Left OMS pod   | Passive        |
| OL2           | 51V75A77 | Left OMS pod   | Passive        |
| OR1           | 52V75A24 | Right OMS pod  | Passive        |
| OR2           | 52V75A78 | Right OMS pod  | Passive        |
| <b>MDMs</b>   |          |                |                |
| OF1           | 81V75A16 | AV bay 1       | Water loop     |
| OF2           | 82V75A11 | AV bay 2       | Water loop     |
| OF3           | 83V75A12 | AV bay 3       | Water loop     |
| OF4           | 30V75A9  | Flight deck    | Water loop     |
| OA1           | 54V75A13 | AV bay 4       | Freon loop     |
| OA2           | 55V75A14 | AV bay 5       | Freon loop     |
| OA3           | 56V75A15 | AV bay 6       | Freon loop     |
| <b>PDI</b>    | 81V75A8  | AV bay 1       | Water loop     |
| <b>PCMMUs</b> |          |                |                |
| 1             | 81V75A1  | AV bay 1       | Water loop     |
| 2             | 81V75A2  | AV bay 2       | Water loop     |

### 26.5.2 Crew Controls

Each PCMMU in the OI system has two crew controls. The first crew control selects the PCMMU to an operative state, with power applied to it.

The second control selects the format of the PCMMU operation. The PCMMU can be in a FIXED, PROGRAM, or GPC format:

- **FIXED:** Selects the Read-Only Memory (ROM)-based High Data Rate (HDR) TFL
- **PROGRAM:** Selects the RAM-based HDR TFL
- **GPC:** Allows the SM GPC to select the appropriate TFL

Other operations within the PCMMU must be commanded through the GPCs via Specification (SPEC) 62 or by ground (uplink) command.

There are no operating controls for the DSCs and MDMs except for circuit breakers and power switches onboard. Only under extremely rare conditions will these require crew attention. Likewise, the PDI has only one crew control - power ON/OFF. All other operations must be commanded through the GPCs via SPEC 62 or ground (uplink) commands.

### 26.5.3 Ground Commands

All operations that are not controlled by physical panel switches onboard the orbiter must be commanded through the GPCs via SPEC 62 or by ground (uplink) commanding. The commands that are entered by the crew (via SPEC 62) can be uplinked from the Mission Control Center (MCC) and vice versa. These commands are referred to as GPC commands. (Note: No GPC commands exist for the DSCs and MDMs).

The PDI operations (except power ON/OFF) are conducted via the GPC commands. PDI operations include: the selecting of inputs, the loading of DFLs, the loading of Fetch Pointer Memory (FPM), the enabling of Fault Detection and Annunciation (FDA), and Input/Output (I/O) reset initiation. PCMMU operations, including the loading of TFLs and I/O resets, are performed via GPC commands as well. No GPC commands exist for the DSCs or MDMs.

### 26.5.4 Operating Instructions

The DSC and MDM power ON/OFF switches will be in the ON position for mission duration.

The PDI is configured by the crew or by GPC commands at several points during each mission, based on payload activities. Detailed instructions for operating and configuring the PDI are contained in SB 30.

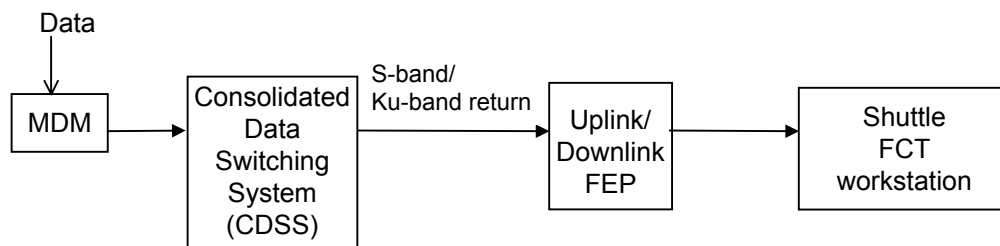
The PCMMU has different TFLs loaded at specific points during flight, based on specific parameters:

- Flight phase (ascent, orbit, entry, etc.)
- Payload/experiment activities
- Troubleshooting procedures

SB 22 contains instructions for operation and configuration of the PCMMUs.

## 26.6 OI TELEMETRY

Telemetry from the OI system components is received by the shuttle uplink/downlink Front End Processor (FEP) and sent to the shuttle command server where it can be “seen” by the Instrumentation and Communications Officer (INCO) flight controller (Instrument (INST) officer) via displays on the workstation. Telemetry from the PDIs, DSCs, seven MDMs, and PCMMU can be monitored on a real-time basis during flight. Figure 26-3 provides a general description of how telemetry is routed to the ground support workstations; for a more detailed explanation, see Space Network Self-Study Manual, Vol. II (SFOC-FL1058, January 1998).



**Figure 26-3. Telemetry routing**

Of the 14 DSCs, 9 internally generate a power supply compare discrete (1 or 0) signal. The seven MDMs generate 16-bit signals in addition to 16-bit Wraparound (WRAP) test signals. Figure 26-2 lists telemetry parameters for the DSCs and MDMs.

**Table 26-2. DSC/MDM telemetry parameters**

| <b>Power status</b>    |                      |
|------------------------|----------------------|
| V75S2157E DSC OA 1/2/3 | V75S2160E DSC OL 1/2 |
| V75S2801E MDM OA 1/2/3 | V75S2165E DSC OR 1/2 |
| <b>DSC status</b>      |                      |
| V75X2171E OF1 BITE     | V75X2181E OM1 BITE   |
| V75X2172E OF2 BITE     | V75X2182E OM2 BITE   |
| V75X2173E OF3 BITE     | V75X2183E OM3 BITE   |
| V75X2174E OA1 BITE     |                      |
| V75X2175E OA2 BITE     |                      |
| V75X2176E OA3 BITE     |                      |
| <b>MDM status</b>      |                      |
| V72M8020P OF1 BITE     | V75X4020D OF1 WRAP   |
| V72M8040P OF2 BITE     | V75X4021D OF2 WRAP   |
| V72M8060P OF3 BITE     | V75X4022D OF3 WRAP   |
| V72M8080P OF4 BITE     | V75X4023D OF4 WRAP   |
| V72M8100P OA1 BITE     | V75X4024D OA1 WRAP   |
| V72M8120P OA2 BITE     | V75X4025D OA2 WRAP   |
| V72M8140P OA3 BITE     | V75X4026D OA3 WRAP   |

The PCMMU in use provides data concerning its power status, its number identification (1 or 2), TFL IDs, ROM/RAM based HDR TFL in use, and a 16-bit Built-In Test Equipment (BITE) signal. Table 26-3 lists these parameters.

**Table 26-3. PCMMU telemetry parameters**

| <b>PCMMU-1</b>             | <b>PCMMU-2</b>             |
|----------------------------|----------------------------|
| V75S2107E Power ON         | V75S2109E Power ON         |
| V76X4265E RPC 1 ON         | V76X4272E RPC 1 ON         |
| V76X4267E RPC 2 ON         | V76X4274E RPC 2 ON         |
| V75S1001E Format - GPC     | V75S1002E Format - GPC     |
| V75S1003E Format - PROGRAM | V75S1004E Format - PROGRAM |
| V75M2120P PCMMU BITE       |                            |
| V75X4070D FORMAT ID        |                            |

The PDI telemetry parameters (Table 26-4) are in the OI downlist and Systems Management (SM) downlist. These parameters are fetched by the PCMMU from the PDI data RAM and toggle buffer. The telemetry data provide information concerning the PDI power status, communication status between the PDI and PCMMU, DFLs, and BITE status.

**Table 26-4. PDI telemetry parameters**

|           |                             |
|-----------|-----------------------------|
| V75X5100E | Power ON                    |
| V76X4376E | RPC A ON                    |
| V76X4378E | RPC C ON                    |
|           |                             |
| V75M5110P | Switch matrix configuration |
|           |                             |
| V75J5132D | DCM 1 ID                    |
| V75J5152D | DCM 2 ID                    |
| V75J5172D | DCM 3 ID                    |
| V75J5192D | DCM 4 ID                    |
|           |                             |
| V75M6400P | BITE word 1                 |
| V75M6520P | BITE word 2                 |

## 26.7 MECHANICAL AND ELECTRICAL SUMMARY

Table 26-5 includes a summary of the OI components power sources and control locations. Table 26-6 provides information including the OI system component, height, width, depth, and weight (see footnote with Table 26-6).



Table 26-5. OI electrical summary

| Control  |     |      | Power (28 V dc) |        |      |                 | DSCs    |       |       |     |     |     | MDMs    |       |  |
|----------|-----|------|-----------------|--------|------|-----------------|---------|-------|-------|-----|-----|-----|---------|-------|--|
| Location |     | ID   | CB/RPC          | Source |      |                 | 0000    | 000   | 000   | 00  | 00  | 00  | 0000    | 000   |  |
| Pnl      | Row |      | Rating          | CTRL   | Main | APC             | FFFF    | AAA   | MMM   | LL  | RR  | PP  | FFFF    | AAA   |  |
|          |     |      | (A)             |        |      |                 | 1 2 3 4 | 1 2 3 | 1 2 3 | 1 2 | 1 2 | 1 2 | 1 2 3 4 | 1 2 3 |  |
| 014      | B   | CB2  | 5               |        | A    |                 | X X     |       |       |     |     |     |         |       |  |
| 014      | B   | CB2  | 5               |        | A    |                 |         |       | XX    |     |     |     |         |       |  |
| 014      | B   | CB3  | 5               |        | A    |                 |         |       |       |     |     |     | X X     |       |  |
| 014      | B   | CB4  | 7.5             |        | A    |                 |         |       |       |     |     |     | X X     |       |  |
| 014      | B   | CB5  | 7.5             |        | A    |                 |         |       |       |     |     |     |         |       |  |
| 015      | B   | CB2  | 5               |        | B    |                 | X X     |       |       |     |     |     |         |       |  |
| 015      | B   | CB3  | 5               |        | B    |                 | X X     |       |       |     |     |     |         |       |  |
| 015      | B   | CB4  | 5               |        | B    |                 |         |       | XX    |     |     |     | X X     |       |  |
| 015      | B   | CB5  | 7.5             |        | B    |                 |         |       |       |     |     |     |         |       |  |
| 015      | A   | CB37 | 3               |        | B    |                 |         |       |       | X   |     |     |         |       |  |
| 016      | B   | CB2  | 5               |        | C    |                 |         |       |       |     |     |     | X X     |       |  |
| 016      | B   | CB3  | 7.5             |        | C    |                 | X X     |       |       |     |     |     |         |       |  |
| 016      | B   | CB31 | 3               |        | C    |                 |         |       |       | X   |     |     |         |       |  |
| 017      | C   | S13  | 5               | AB-2   | A    | 1               |         |       |       | XX  |     |     |         |       |  |
|          |     |      | 5               | BC-2   | B    | 2               |         |       |       | X   |     |     |         |       |  |
|          |     |      | 5               | CA-2   | C    | 3               |         |       |       |     |     |     |         |       |  |
| 017      | C   | S14  | 5               | AB-3   | A    | 1               |         |       |       |     |     |     |         |       |  |
|          |     |      | 5               | BC-3   | B    | 2               |         |       |       |     | X   |     |         |       |  |
|          |     |      | 5               | CA-3   | C    | 3               |         |       |       |     |     | XX  |         |       |  |
| 017      | D   | S17  | 5               | AB-2   | A    | 4               |         |       | X X   |     |     |     |         |       |  |
|          |     |      | 5               | BC-2   | B    | 5               |         |       | XX    |     |     |     |         |       |  |
|          |     |      | 5               | CA-1   | C    | 6               |         |       |       |     |     | X   |         |       |  |
| 017      | D   | S19  | 5               | AB-1   | A    | 4               |         |       | X     |     |     |     |         | X X   |  |
|          |     |      | 5               | BC-1   | B    | 5               |         |       | X     |     |     |     |         | X X   |  |
|          |     |      | 5               | CA-2   | C    | 6               |         |       |       |     |     |     |         | XX    |  |
| A1       |     | S17  | 5               | BC-1   | A    | <b>FPC</b><br>1 | PDI     |       |       |     |     |     |         |       |  |
|          |     |      | 5               | BC-2   | C    | 3               | PDI     |       |       |     |     |     |         |       |  |
| C3       |     | S7   | 5               | CA-1   | C    | <b>FPC</b><br>3 | PCMMU-1 |       |       |     |     |     |         |       |  |
|          |     |      | 5               | AB-1   | A    | 1               | PCMMU-1 |       |       |     |     |     |         |       |  |
|          |     |      | 5               | AB-1   | A    | 1               | PCMMU-2 |       |       |     |     |     |         |       |  |
|          |     |      | 5               | BC-1   | B    | 2               | PCMMU-2 |       |       |     |     |     |         |       |  |

*Table 26-6. OI mechanical summary*

| LRU          |     | Height<br>(in.) | Width<br>(in.) | Depth<br>(in.) | Weight*<br>(lb) |
|--------------|-----|-----------------|----------------|----------------|-----------------|
| <b>DSC</b>   | OF1 | 7.00            | 8.00           | 16.00          | 11.5            |
|              | OF2 | 7.00            | 8.00           | 16.00          | 11.5            |
|              | OF3 | 7.00            | 8.00           | 16.00          | 11.5            |
|              | OF4 | 7.00            | 8.00           | 16.00          | 11.5            |
|              | OA1 | 7.00            | 8.00           | 16.00          | 11.5            |
|              | OA2 | 7.00            | 8.00           | 16.00          | 11.5            |
|              | OA3 | 7.00            | 8.00           | 16.00          | 11.5            |
|              | OM1 | 7.00            | 8.00           | 16.00          | 11.5            |
|              | OM2 | 7.00            | 8.00           | 16.00          | 11.5            |
|              | OM3 | 7.00            | 8.00           | 16.00          | 11.5            |
|              | OL1 | 7.00            | 8.00           | 10.80          | 8.0             |
|              | OL2 | 7.00            | 8.00           | 10.80          | 8.0             |
|              | OR1 | 7.00            | 8.00           | 10.80          | 8.0             |
|              | OR2 | 7.00            | 8.00           | 10.80          | 8.0             |
| <b>MDM</b>   | OF1 | 6.50            | 11.00          | 13.00          | 37.0            |
|              | OF2 | 6.50            | 11.00          | 13.00          | 37.0            |
|              | OF3 | 6.50            | 11.00          | 13.00          | 37.0            |
|              | OF4 | 6.50            | 11.00          | 13.00          | 37.0            |
|              | OA1 | 6.50            | 11.00          | 13.00          | 37.0            |
|              | OA2 | 6.50            | 11.00          | 13.00          | 37.0            |
|              | OA3 | 6.50            | 11.00          | 13.00          | 37.0            |
| <b>PDI</b>   |     | 7.00            | 19.00          | 6.60           | 27.0            |
| <b>PCMMU</b> | 1   | 7.00            | 6.60           | 19.00          | 30.0            |
|              | 2   | 7.00            | 6.60           | 19.00          | 30.0            |

\*All weights are maximums; variations exist depending on the card complement in each DSC and MDM.

THIS PAGE INTENTIONALLY BLANK

**SECTION 27 - OI DEDICATED SIGNAL CONDITIONERS**  
**CONTENTS**

| <b>Section</b> |  | <b>Page</b> |
|----------------|--|-------------|
| 27.1           | GENERAL DESCRIPTION.....               | 27-1        |
| 27.2           | CIRCUIT-MOTHER INTERCONNECT BOARD..... | 27-1        |
| 27.2.1         | Telemetry-BITE.....                    | 27-1        |
| 27.2.2         | Power Supplies.....                    | 27-1        |
| 27.2.3         | DSC Configuration.....                 | 27-1        |
| 27.2.4         | Operating Parameters.....              | 27-4        |
| 27.3           | CARDS.....                             | 27-5        |
| 27.3.1         | Specific Cards.....                    | 27-6        |
| 27.3.2         | Interchangeability.....                | 27-12       |
| 27.4           | INTERFACES.....                        | 27-13       |
| 27.5           | DATA ROUTING.....                      | 27-13       |
| 27.6           | DSC LOCATIONS.....                     | 27-13       |
| 27.7           | COOLING.....                           | 27-14       |
| 27.8           | INFORMATION SOURCES.....               | 27-14       |
| 27.9           | CREW CONTROLS.....                     | 27-15       |
| 27.10          | EQUIPMENT PHYSICAL DESCRIPTION.....    | 27-15       |
| 27.11          | OPERATIONAL NOTES.....                 | 27-22       |
| 27.12          | REFERENCES.....                        | 27-22       |

## TABLES

| Table |                              | Page  |
|-------|------------------------------|-------|
| 27-1  | OI DSC power bus table ..... | 27-3  |
| 27-2  | The 15-card DSCs .....       | 27-3  |
| 27-3  | The 30-card DSCs .....       | 27-4  |
| 27-4  | DSC Power Consumption.....   | 27-5  |
| 27-5  | Card reference table .....   | 27-6  |
| 27-6  | PD ranges.....               | 27-7  |
| 27-7  | D ranges .....               | 27-8  |
| 27-8  | VA ranges .....              | 27-9  |
| 27-9  | A ranges .....               | 27-12 |

## FIGURES

### Figure

|      |   |       |
|------|---|-------|
| 27-1 | Dedicated signal conditioner block diagram .....  | 27-2  |
| 27-2 | DSC location.....   | 27-13 |
| 27-3 | 8/4 channel outputs .....   | 27-14 |
| 27-4 | Chassis-mother interconnect board-dedicated signal conditioner<br>configuration -0001/-2001/-3001.....            | 27-16 |
| 27-5 | Chassis-mother interconnect board-dedicated signal conditioner<br>configuration -0002.....                        | 27-17 |
| 27-6 | Chassis-mother interconnect board-dedicated signal conditioner<br>configuration -0003/-2003/-3003.....            | 27-18 |
| 27-7 | Chassis-mother interconnect board-dedicated signal conditioner<br>connector configuration -0001/-2001/-3001 ..... | 27-19 |
| 27-8 | Chassis-mother interconnect board-dedicated signal conditioner<br>connector configuration -0002 .....             | 27-20 |
| 27-9 | Chassis-mother interconnect board-dedicated signal conditioner<br>connector configuration -0003/-2003/-3003.....  | 27-21 |

## SECTION 27 OI DEDICATED SIGNAL CONDITIONERS

### 27.1 GENERAL DESCRIPTION

The Operational Instrumentation (OI) Dedicated Signal Conditioners (DSCs), which provide acquisition and conditioning of vehicle data, contain a Chassis-Mother Interconnect Board (CMIB) and a selectable mix of conditioning cards. Figure 27-1 shows the basic framework of a DSC. (Refer to SSSH drawing 17.1 for specific detail.) The measurements conditioned by the DSCs are scaled as a 0 to 5 V dc signal proportional to the input signal and output to the flight-critical and OI Multiplexer/Demultiplexers (MDMs), the dedicated displays, and the Caution and Warning (C&W).

### 27.2 CIRCUIT-MOTHER INTERCONNECT BOARD

The Circuit-Mother Interconnect Board (CMIB) is a circuit board which forms the mainframe of a DSC into which all of the signal conditioning cards are plugged. Each CMIB contains 10/15/30 card connectors, two power supplies, and Built-In Test Equipment (BITE).

#### 27.2.1 Telemetry-BITE

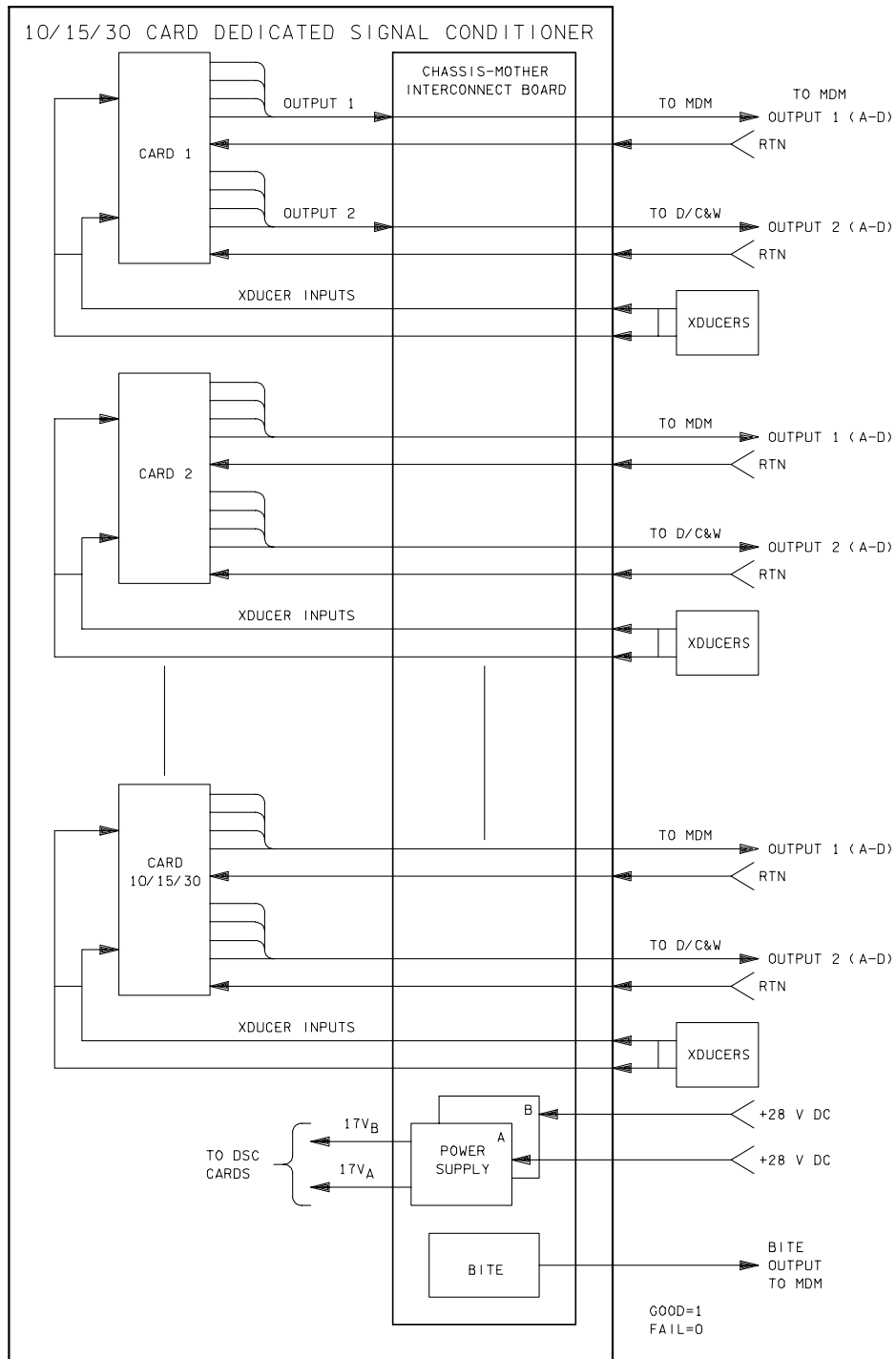
The DSC BITE monitors the state of the two CMIB power supplies, though not all DSCs have a BITE. If either supply fails or is out of tolerance (0.5 percent of 17 V dc), the BITE identifies failure by outputting 0 V dc, logic zero. Proper operation is signified by an output of +5 V dc, logic one. A BITE indication of a failure can also occur if one of the 28 V power sources, from the orbiter, powering a DSC is lost. If a DSC BITE indicates a failure, the DSC may continue to condition data properly. See Section 26 for BITE Measurement Stimulation Identifications (MSIDs).

#### 27.2.2 Power Supplies

An OI DSC's power is provided by two orbiter 28 V dc sources. Internally the two CMIB power supplies convert the 28 V dc to 17 V dc for use by the cards and the BITE circuits. See Figure 27-1, OI DSC power bus table.

#### 27.2.3 DSC Configuration

The 14 orbiter DSCs are assembled and installed with their cards configured in accordance with Table 27-2 and Table 27-3.



186114701.SCH# 2  
SYS BR

Figure 27-1. Dedicated signal conditioner block diagram

**Table 27-1. OI DSC power bus table**

| <b>DSC</b> | <b>PWR and CNTL (1)</b> |          | <b>PWR and CNTL (2)</b> |          |
|------------|-------------------------|----------|-------------------------|----------|
| OA1        | MNB APC5                | CNTL BC2 | MNA APC4                | CNTL AB2 |
| OA2        | MNB APC5                | CNTL BC2 | MNC APC6                | CNTL CA1 |
| OA3        | MNA APC4                | CNTL AB2 | MNC APC6                | CNTL CA1 |
| OF1        | MNB O15                 |          | MNA O14                 |          |
| OF2        | MNB O15                 |          | MNC O16                 |          |
| OF3        | MNB O15                 |          | MNC O16                 |          |
| OF4        | MNB O15                 |          | MNA O14                 |          |
| OL1        | MNB APC2                | CNTL BC2 | MNA APC1                | CNTL AB2 |
| OL2        | MNC APC3                | CNTL CA2 | MNA APC1                | CNTL AB2 |
| OM1        | MNA O14                 |          | MNB O15                 |          |
| OM2        | MNA O14                 |          | MNB O15                 |          |
| OM3        | MNB O15                 |          | MNC O16                 |          |
| OR1        | MNC APC3                | CNTL CA3 | MNB APC2                | CNTL BC3 |
| OR2        | MNA APC1                | CNTL AB3 | MNB APC2                | CNTL BC3 |

**Table 27-2. The 15-card DSCs**

**DSC vs. card configuration<sup>a</sup>**

| <b>Card no.</b> | <b>15-card DSCs</b> |             |             |             |
|-----------------|---------------------|-------------|-------------|-------------|
|                 | <b>OL 1</b>         | <b>OL 2</b> | <b>OR 1</b> | <b>OR 2</b> |
| 1               | D                   | D           | D           | D           |
| 2               | D                   | D           | D           | D           |
| 3               | A (INT)             | A (INT)     | A (INT)     | A (INT)     |
| 4               | A (INT)             | A (INT)     | A (INT)     | A (INT)     |
| 5               | A (INT)             | A (INT)     | A (INT)     | A (INT)     |
| 6               | A (INT)             | A (INT)     | A (INT)     | A (INT)     |
| 7               | A (INT)             | A (INT)     | A (INT)     | A (INT)     |
| 8               | D                   | A (INT)     | D           | A (INT)     |
| 9               | D                   | D           | D           | D           |
| 10              | D                   | D           | D           | D           |
| 11              | D                   | D           | D           | D           |
| 12              | D                   | D           | D           | D           |
| 13              | A (INT)             | A (INT)     | A (INT)     | A (INT)     |
| 14              | D                   | D           | D           | D           |
| 15              | A (INT)             | D           | A (INT)     | D           |

<sup>a</sup>See Table 27-5 to cross-reference the card and identifier.





- D. Analog error, full-scale output  $\pm 1.0$  percent
- E. Operating temperature range/error
  - 65° to 160° F
  - $\pm 1.0$  percent
  - 160° to 200° F
  - $\leq 2.0$  percent
- F. Ripple, noise, and crosstalk
  - 1. Peak-to-peak 5.0 mV
  - 2. Signal output load resistance  $>1.5 \text{ M}\Omega$
- G. Self test
  - 1. Logic 1, go  $5.0 \pm 1.0 \text{ V dc}$
  - 2. Logic 0, no-go  $0.0 \text{ }_{-0.0}^{+0.5} \text{ V dc}$
- H. Excitation supply deviation, maximum  $\pm 0.5$  percent
- I. Power consumption

**Table 27-4. DSC Power Consumption**

| DSC | Power, W | DSC | Power, W |
|-----|----------|-----|----------|
| OA1 | 36.2*    | OL2 | 21.4*    |
| OA2 | 29.2*    | OR1 | 23.7*    |
| OA3 | 29.0*    | OR2 | 21.4*    |
| OF1 | 24.5*    | OM1 | 20.1*    |
| OF2 | 32.4*    | OM2 | 28.5*    |
| OF3 | 26.5*    | OM3 | 13.1*    |
| OF4 | 19.5*    | OP1 | 8.5      |
| OL1 | 23.7*    | OP2 | 8.5      |

\*Based on OV-102, STS-109 configuration requirements

### 27.3 CARDS

The DSC card is a printed circuit board with an internal power supply and individual conditioning paths or channels, and when required, the card provides an internal transducer excitation source. The internal power supply of a card is a  $\pm 17 \text{ V dc}$  supply which provides power to the channel's processing circuits. A card may contain three, four, or eight channels. In operation a channel receives a signal from its transducer, processes the signal, and outputs a 0 to 5 V dc signal to a MDM) and/or displays/C&W.

DSC card types:

- DC amplifier, analog buffer, attenuators
- Converter, variable resistance to dc voltage
- Converter, pulse to dc voltage
- Buffer 5 V dc discrete
- Converter, voltage discrete ac
- Converter, voltage ac to dc

**Table 27-5. Card reference table**

| Card name                  | IPCL identifier | X-ducer power | Channels | Different ranges |
|----------------------------|-----------------|---------------|----------|------------------|
| Converter, pulse to dc     | PD              | Ext.          | A-C      | 4                |
| Converter, var. res. to dc | D               | Int.          | A-D      | 53               |
| Converter, V ac to dc      | VA              | Ext.          | A-D      | 2                |
| Converter, V discrete ac   | VD              | Ext.          | A1-D2    | 1                |
| Buffer, 5 V dc discrete    | 5D              | Ext.          | A-D      | 1                |
| Amp., buffer, atten.       | A               | Int./ext.     | A-D      | 22               |

### 27.3.1 Specific Cards

#### 27.3.1.1 Converter, Pulse to DC (PD) - Three Channels

The conditioning cards that convert pulse rates to levels of V dc have the following characteristics:

- Signal input Table 27-6
- Signal output Dual A and B, isolated, ungrounded, 0 to 5 V dc  
Output current, each output 250  $\mu$ A  
A and B (full scale)  
Under/overvoltage limiting -1.0 to 6.5 V dc  
Response time  $\geq$ 90 percent in 125 msec  
Ripple, noise, and crosstalk  $\leq$ 5 mV peak-to-peak, 2.0 kHz to full scale, 74 mV peak-to-peak max  $\geq$  2 kHz

Impedance 100  $\Omega$  or less

- Example measurement

Main engine N no. 1 LH2 receive pump speed, range 0 to 2000 rpm

A card of this type has the identifying number MC473-0033-XXXX with the last four digits being associated with its input range/source impedance.

**Table 27-6. PD ranges**

| Control part number | Input freq. range (Hz) | Impedance ( $\Omega$ ) |
|---------------------|------------------------|------------------------|
| MC473-0033-0001     | 0-400                  | 50K                    |
| MC473-0033-0002     | 0-1100                 | 50K                    |
| MC473-0033-0003     | 0-4000                 | 50K                    |
| MC473-0033-0005     | 0-4000                 | 30K                    |

### 27.3.1.2 Converter, Variable Resistance to DC (D) - Four Channels

The cards that convert variable resistance to V dc are designed to have the following characteristics:

- Signal input Table 27-7
- Signal output Dual A and B, isolated, ungrounded, 0 to 5 V dc
- Output current, each output A and B (full scale) 250  $\mu$ A
- Under/overvoltage output limiting -1.0 to 6.5 V dc
- Impedance  $\leq 100 \Omega$
- Data frequency response
  - Passband 1 percent of dc to 4 Hz  
5 percent of 4 Hz to 10 Hz
  - Roll off 3 dB at 35 Hz  
 $\geq 30$  dB at 400 Hz  
12 dB per octave  
 $\geq 400$  Hz
  - Error  $\leq 1.2$  percent

- Example measurement

APU 3 fuel line temp no. 2, range 0 to 250° F

The identifying number of the D card is MC 450-0034-XXXX with the last four digits specifying individual ranges.

**Table 27-7. D ranges**

| Control<br>part number<br>MC450-0034<br>ID. no. | Temp<br>range (°F) | Input<br>ΔR (Ω) | Control<br>part number<br>MC45C-0034<br>ID. no. | Temp<br>range (°F) | Input<br>ΔR (Ω) |
|---|--------------------|-----------------|---|--------------------|-----------------|
| 0001  | -450 to +450       | 189.29          | 0028  | 0 to +200          | 604.00          |
| 0002  | -450 to +1500      | 385.83          | 0029  | 0 to +250          | 54.59           |
| 0003  | -430 to +200       | 136.42          | 0030  | 0 to +400          | 86.10           |
| 0004  | -429 to -379       | 75.25           | 0031  | 0 to +500          | 107.72          |
| 0005  | -425 to +400       | 178.61          | 0032  | 0 to +750          | 156.69          |
| 0006  | -325 to +300       | 140.28          | 0033  | 0 to +1000         | 204.39          |
| 0007  | -325 to +125       | 102.69          | 0034  | 0 to +1500         | 293.02          |
| 0008  | -320 to -270       | 166.07          | 0035  | +40 to +210        | 511.31          |
| 0009  | -300 to +500       | 175.86          | 0036  | +200 to +2000      | 327.19          |
| 0010  | -300 to +200       | 112.92          | 0037  | -300 to -250       | 165.14          |
| 0011  | -300 to +2000      | 433.55          | 0038  | +25 to +130        | 318.30          |
| 0012  | -200 to -100       | 317.01          | 0039  | -250 to +1000      | 261.56          |
| 0013  | -250 to +250       | 111.66          | 0040  | +20 to +70         | 55.21           |
| 0014  | -200 to +200       | 89.21           | 0041  | -430 to -379       | 75.46           |
| 0015  | -200 to +400       | 131.53          | 0042  | -325 to +500       | 181.90          |
| 0016  | -200 to +2000      | 409.84          | 0043  | -200 to +450       | 141.89          |
| 0017  | -150 to +650       | 170.03          | 0044  | +32 to +140        | 5,116.10        |
| 0018  | -100 to +250       | 76.94           | 0045  | -325 to -250       | 244.48          |
| 0019  | -100 to +500       | 129.17          | 0046  | -430 to +600       | 219.64          |
| 0020  | -100 to +2000      | 386.86          | 0047  | -430 to -405       | 38.68           |
| 0021  | -75 to +175        | 55.18           | 0048  | -305 to -255       | 165.54          |
| 0022  | -75 to +300        | 81.92           | 0049  | -425 to +475       | 970.57          |
| 0023  | -65 to +200        | 58.32           | 0050  | -200 to +1500      | 47.46           |
| 0024  | -65 to +500        | 121.26          | 0051  | 0 to +250          | 27.25           |
| 0025  | -50 to +300        | 76.29           | 0052  | 0 to +160          | 175.74          |
| 0026  | -50 to +500        | 117.89          | 0053  | +20 to +100        | 88.16           |
| 0027  | 0 to +150          | 484.83          |   |                    |                 |

### 27.3.1.3 Converter, Voltage AC to DC (VA) - Four Channels

Conditioning cards that convert ac voltages to dc are designed to meet the following characteristics:

- Signal input Table 27-8  
 Impedance, minimum 500 kΩ  
 Frequency 400 ±20 Hz
- Signal output (directly proportional to input) Dual A and B, isolated,  
ungrounded, 0 to 5.0 V dc

|   |                               |
|---|-------------------------------|
| Impedance                                       | $\leq 100 \Omega$             |
| Current each amplifier,<br>A and B (full scale) | 250 $\mu$ A                   |
| Under/over voltage limiting                     | -1.0 to +6.5 V dc             |
| Ripple  | $\leq 10$ mV peak-to-peak     |
| Response  | $\geq 90$ percent in 125 msec |

- Example measurement

AC bus 1 phase A volts, range 0 to 140 V ac

These cards have the associated identifying number MC450-0037-XXXX with the last four digits specifying ranges.

**Table 27-8. VA ranges**

| Control part number | Input                            |
|---------------------|----------------------------------|
| MC450-0037-0001     | 0 to 140 V ac<br>400 $\pm$ 20 Hz |
| MC450-0037-0002     | 0 to 5 V ac<br>400 $\pm$ 20 Hz   |

#### 27.3.1.4 Converter, Voltage Discrete AC (VD) - Eight Channels

This type card converts discrete ac voltages to dc logic. These meet the following characteristics:

- Signal input
 

|                    |                                    |
|--------------------|------------------------------------|
| Logic 1            | 100 to 400 V ac                    |
| Logic 0            | 0 to 40 V ac                       |
| Impedance, minimum | 100 K $\Omega$                     |
| Frequency          | 400 $\pm$ 20 Hz                    |
| Signal output      | Single isolated step voltage level |
| Logic 1, maximum   | 5.0 $\pm$ 1.0 V dc, 125 mA<br>+0.5 |

|                    |                              |
|--------------------|------------------------------|
| Logic 0            | 0.0 -0.0 V dc                |
| Impedance, maximum | 100 $\Omega$                 |
| Rise and fall time | >20 $\mu$ sec, $\leq$ 1 msec |
| Response time      | $\leq$ 100 msec              |

- Example measurement

MPS-E1 ac power no. 1 on cmd, range OFF-ON

A card of this type has the identifying number MC450-0049-0001. The ranging indication always shows 0001 since there is only one.

### 27.3.1.5 Buffer 5 V DC Discrete (5D) - Four Channels

This type card conditions discrete voltages dc to dc logic. Their design characteristics are

- Signal input  
Logic 1 5.0  $\pm$  1.0 V dc  
Logic 0 0.0  $\pm$  1.0 V dc  
Impedance, minimum 10 k $\Omega$
- Sensor excitation voltage supplied by B5D +5 V dc
- Signal output  
Dual A and B, isolated, step voltage level  
Logic 1, maximum 5.0  $\pm$  1.0 V dc, 1.25 mA  
Logic 0 <sup>+0.5</sup> 0.0 -0.0 V dc  
Impedance, maximum 100  $\Omega$   
Rise and fall time <20  $\mu$ sec,  $\leq$  1 msec  
Response time  $\geq$ 100 msec  
Under/overvoltage limiting -1.0 to +6.5 V dc
- Example measurement  
Recorder-tape motion on MADS, range OFF-ON

A card of this type is identified by MC473-0109-0001. The ranging indication always shows 0001 since there is only one.

### 27.3.1.6 Amplifier, Buffer, Attenuator (A) - Four Channels

The card that converts variable voltages to V dc are designed with the following characteristics:

- Signal inputs Table 27-9
  - Impedance, minimum 500 k $\Omega$
  - Overvoltage - no damage +32 V dc for unipolar  
+18 V dc for bipolar
- Sensor excitation voltage supplied by ABA Table 27-8
- Signal output (directly proportional to input) Dual A and B, isolated, ungrounded, 0 to 5 V dc
  - Output current, each amplifier A and B at full scale 250  $\mu$ A
  - Under/overvoltage output limiting -1.0 to +6.5 V dc
  - Impedance  $\leq$ 100  $\Omega$
- Data frequency response
  - Passband 1 percent of dc to 4 Hz  
5 percent of 4 Hz to 10 Hz
  - Roll off 3 dB at 35 Hz  
 $\geq$ 30 dB at 400 Hz  
12 dB per octave  
 $\geq$ 400 Hz
- Example measurement
  - Airlock diff press no. 2, range -20 to +20 psid

The identifying number of the A card is MC473-0110-XXXX, the last four digits specify individual range.



*Table 27-9. A ranges*

| Control part number<br><u>MC473-0110</u><br>ID. N | Input signal     | Sensor voltage source<br>(INT/EXT) |
|---|------------------|------------------------------------|
| 0001  | 0 to 6 m V dc    | Int                                |
| 0002  | 0 to 10 m V dc   | Int                                |
| 0003  | 0 to 10 m V dc   | Int                                |
| 0004  | 0 to 15 m V dc   | Int                                |
| 0005  | 0 to 20 m V dc   | Int                                |
| 0006  | 0 to 20 m V dc   | Int                                |
| 0007  | 0 to 30 m V dc   | Int                                |
| 0008  | 0 to 30 m V dc   | Int                                |
| 0009  | 0 to 35 m V dc   | Int                                |
| 0010  | 0 to 40 m V dc   | Int                                |
| 0011  | 0 to 40 m V dc   | Int                                |
| 0012  | 0 to 50 m V dc   | Int                                |
| 0013  | 0 to 50 m V dc   | Int                                |
| 0014  | 0 to 100 m V dc  | Int                                |
| 0015  | 0 to 100 m V dc  | Int                                |
| 0016  | 0 to 2.5 V dc    | Int                                |
| 0017  | 0 to 5.0 V dc    | Int                                |
| 0018  | 0 $\pm$ 5.0 V dc | Ext                                |
| 0019  | 0 to 32 V dc     | Ext                                |
| 0020  | 0 to 40 V dc     | Ext                                |
| 0021  | 0 to 15 V dc     | Ext                                |
| 0022  | 0 to 60 m V dc   | Ext                                |

### 27.3.2 Interchangeability

Any card contained in a DSC may be placed in any card socket on the CMIB. To place a card of one type into a plug previously occupied by another type, the input and output wiring external to the DSC must be rerouted to the appropriate transducers. If the cards are of the same type and of the same range, it is a straight replacement.

## 27.4 INTERFACES

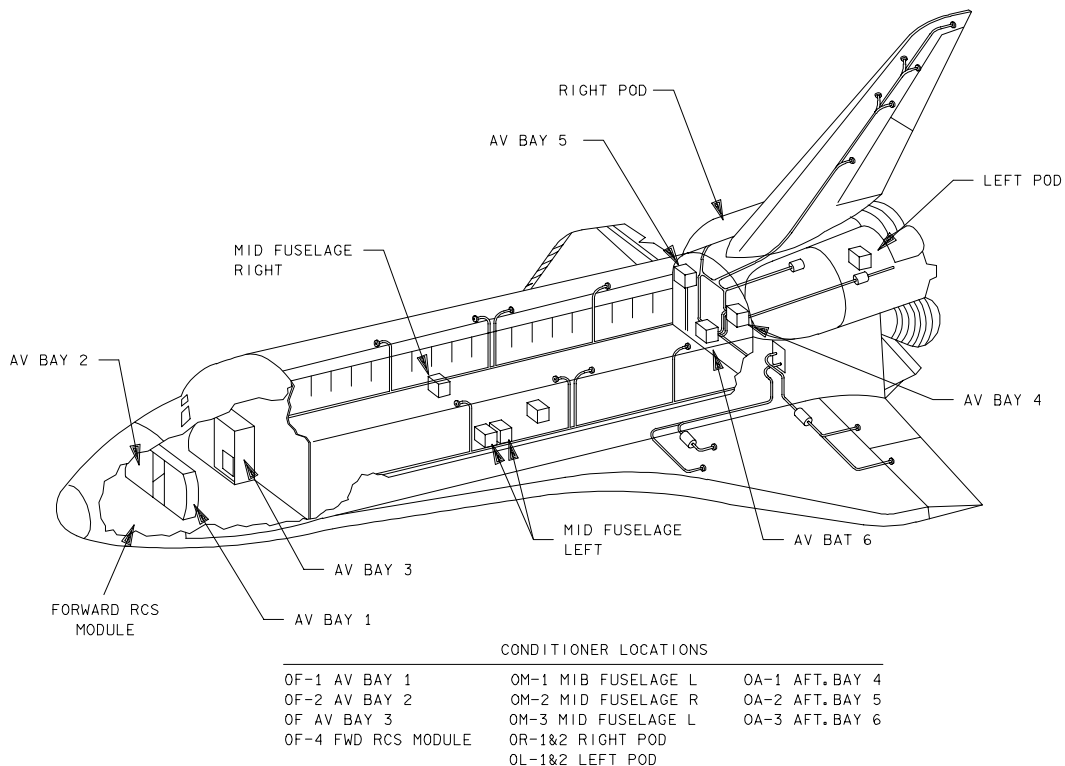
The cards of a DSC interconnect with the CMIB through the CMIB interface sockets. Through these sockets the cards receive transducer signals, operating power, and transmit output signals. The connectors external to the DSC case supply routing of transducer signals to the channel inputs and routing of channel outputs to the MDMs and Displays/C&W.

## 27.5 DATA ROUTING

Each DSC has two outputs, one designated as output A, the other as output B. These may be routed as required to the OI MDMs, FC MDMs, dedicated displays, and C&W. The usual method is to route the A output to the OI and the B output to the other system requiring the measurement. It is common for the measurement to be required by more than two systems; in which case the B output is taken to the input of an A-type DSC card to produce an isolated third output.

## 27.6 DSC LOCATIONS

The OI DSCs are located throughout the vehicle, as shown in Figure 27-2.



2085. ART 2

**Figure 27-2. DSC location**

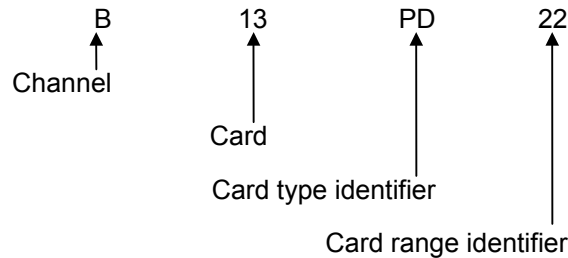
**27.7 COOLING**

See Section 26 for DSC cooling information.

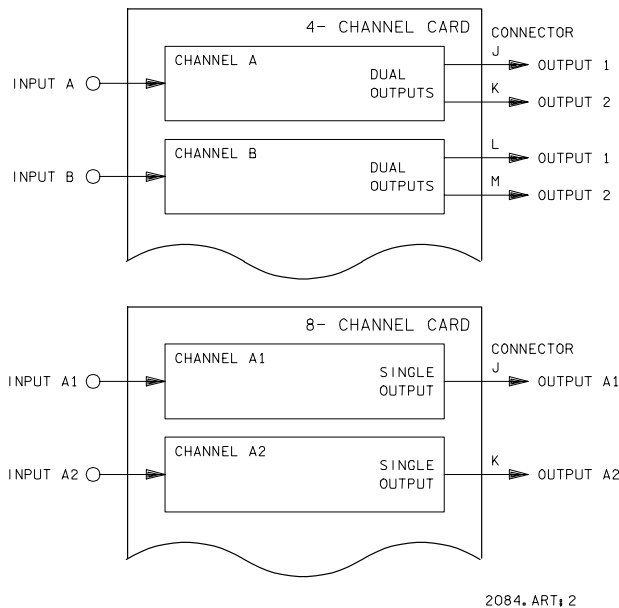
**27.8 INFORMATION SOURCES**

The Instrumentation Program and Component List (IPCL) format gives the DSC card and channel information in the following way:

The Shuttle Configuration Analysis Program (SCAP) gives card and channel in titled columns.



Both of these listings are programmed for maximum of four channels. This leaves the eight channel cards to be listed as A,B,C,D and A,B,C,D. Thus, giving the appearance that two measurements are processed by the same card and channel. Actually one of the measurements is conditioned by the first channel and the other by the second channel. The output routing of these channels is the same as for a channel with dual outputs. The channel notation A1,A2,B1,...,D2, as used in Table 27-5 (the card reference table), and the 8-channel card comparison to a 4-channel card shown by Figure 27-3 should help make the difference clear.



**Figure 27-3. 8/4 channel outputs**

## 27.9 CREW CONTROLS

See Section 26 for DSC power switch and circuit breaker information, TELEMETRY

### A. DSC power status

| MSID      | Title        | SCAP Nomenclature                |
|-----------|--------------|----------------------------------|
| V75S2157E | DSC OA 1/2/3 | AFT DED SIG COND POWER AB2 - ON  |
| V75S2160E | DSC OL 1/2   | SIGNAL CONDITIONER OL 1/2 PWR ON |
| V75S2165E | DSC OR 1/2   | SIGNAL CONDITIONER OR 1/2 PWR ON |

### B. DSC BITE parameters

| MSID      | Title        | IPCL/SCAP Nomenclature     |
|-----------|--------------|----------------------------|
| V75X2171E | DSC OF1 BITE | BAY1 DSC                   |
| V75X2172E | DSC OF2 BITE | BAY2 DSC                   |
| V75X2173E | DSC OF3 BITE | BAY3 DSC                   |
| V75X2174E | DSC OA1 BITE | BAY4 DSC                   |
| V75X2175E | DSC OA2 BITE | BAY5 DSC                   |
| V75X2176E | DSC OA3 BITE | BAY6 DSC                   |
| V75X2181E | DSC OM1 BITE | MID1 DSC (LH SIDE)         |
| V75X2182E | DSC OM2 BITE | MID2 DSC (RT SIDE)         |
| V75X2183E | DSC OM3 BITE | NUD3 DSC (LH SIDE) SHELF 6 |

## 27.10 EQUIPMENT PHYSICAL DESCRIPTION

The following figures (Figure 27-4 through Figure 27-9) are the chassis requirements for the DSCs.

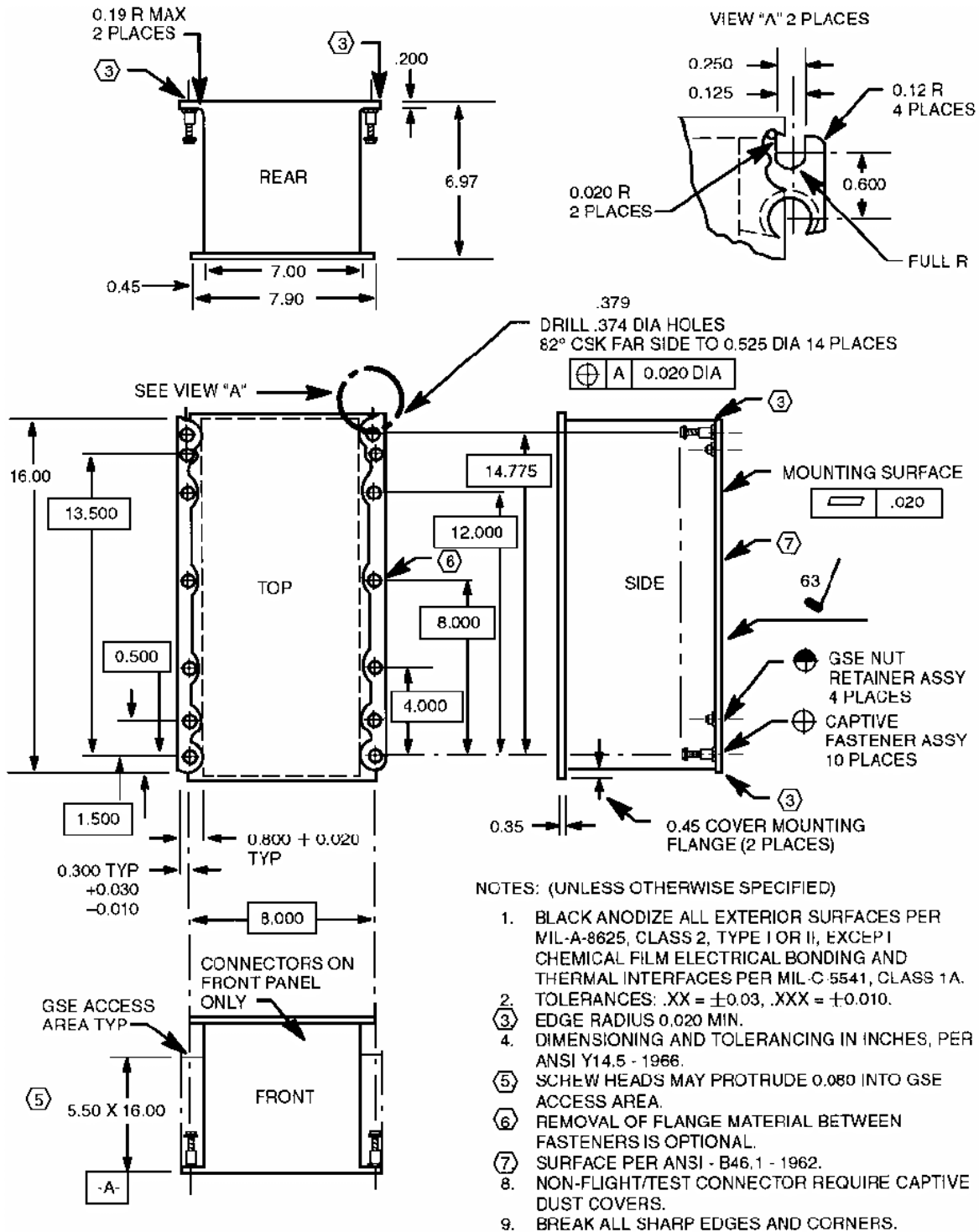
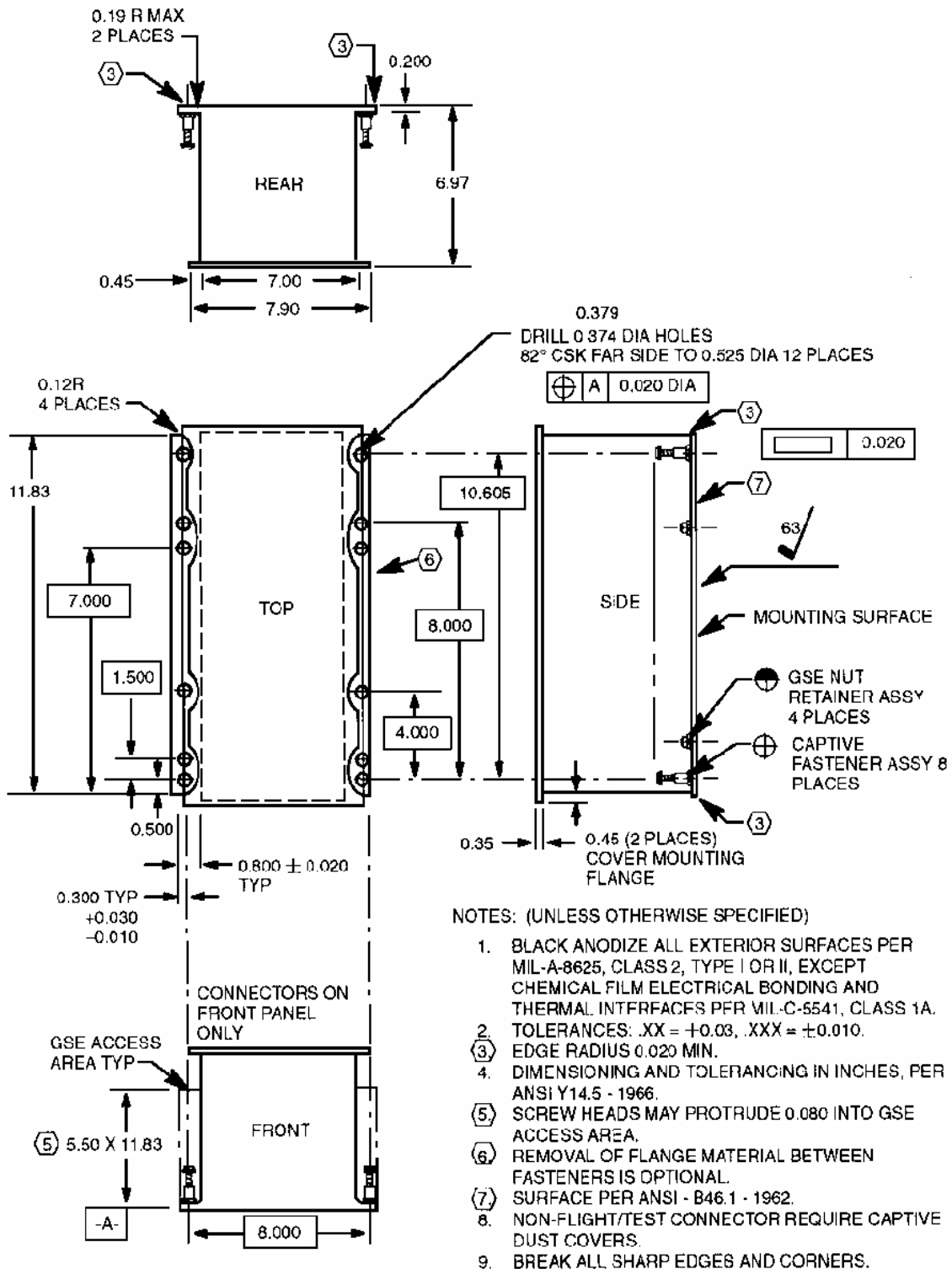
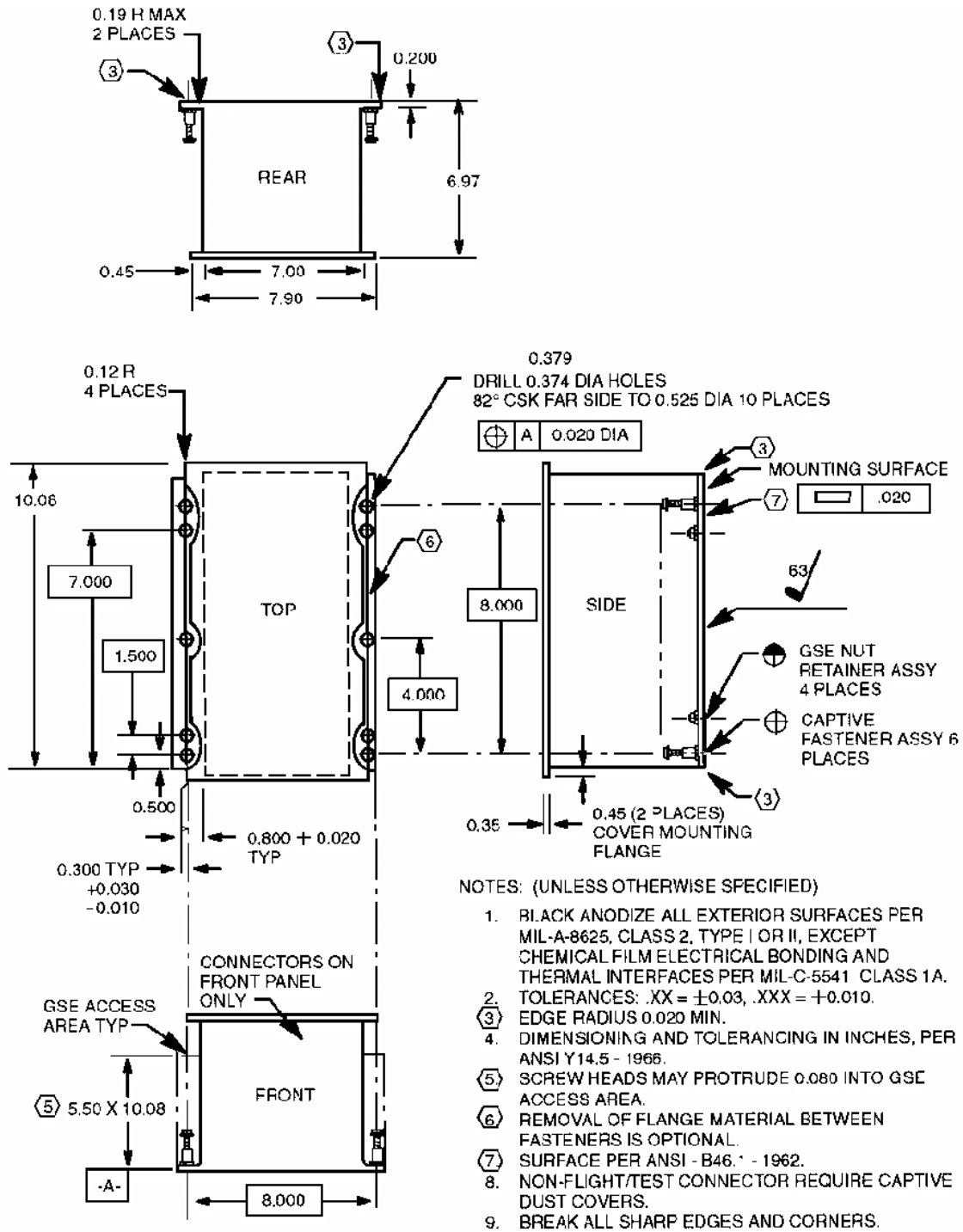


Figure 27-4. Chassis-mother interconnect board-dedicated signal conditioner configuration -0001/-2001/-3001



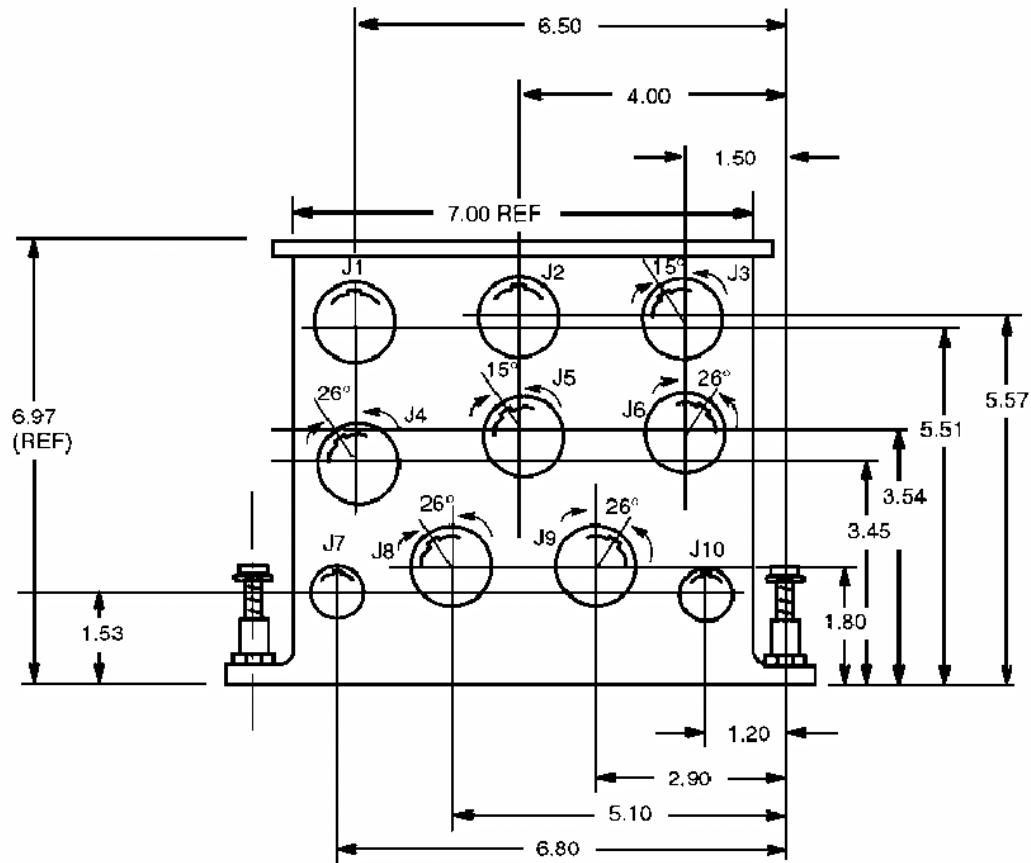
\_18611\_4706

Figure 27-5. Chassis-mother interconnect board-dedicated signal conditioner configuration -0002



18611\_4707

**Figure 27-6. Chassis-mother interconnect board-dedicated signal conditioner configuration -0003/-2003/-3003**



| CONNECTOR DATA |             |          |         |
|----------------|-------------|----------|---------|
| REF DES        | PART NO.    | FUNCTION | X NO.   |
| J1             | NLSOE2435P  | INPUT    | X17-X23 |
| J2             | NLSOE2235P  | OUTPUT   | X17-X23 |
| J3             | NLSOE2435PA | INPUT    | X24-X30 |
| J4             | NLSOE2435PB | INPUT    | X1 -X8  |
| J5             | NLSOE2435PA | OUTPUT   | X24-X30 |
| J6             | NLSOE2435PC | INPUT    | X9 -X16 |
| J7             | NBOE10-6PNC | POWER    |         |
| J8             | NLSOE2235PB | OUTPUT   | X1 -X8  |
| J9             | NLSOE2235PC | OUTPUT   | X9 -X16 |
| J10            | NBOE10-6PWC | POWER    |         |

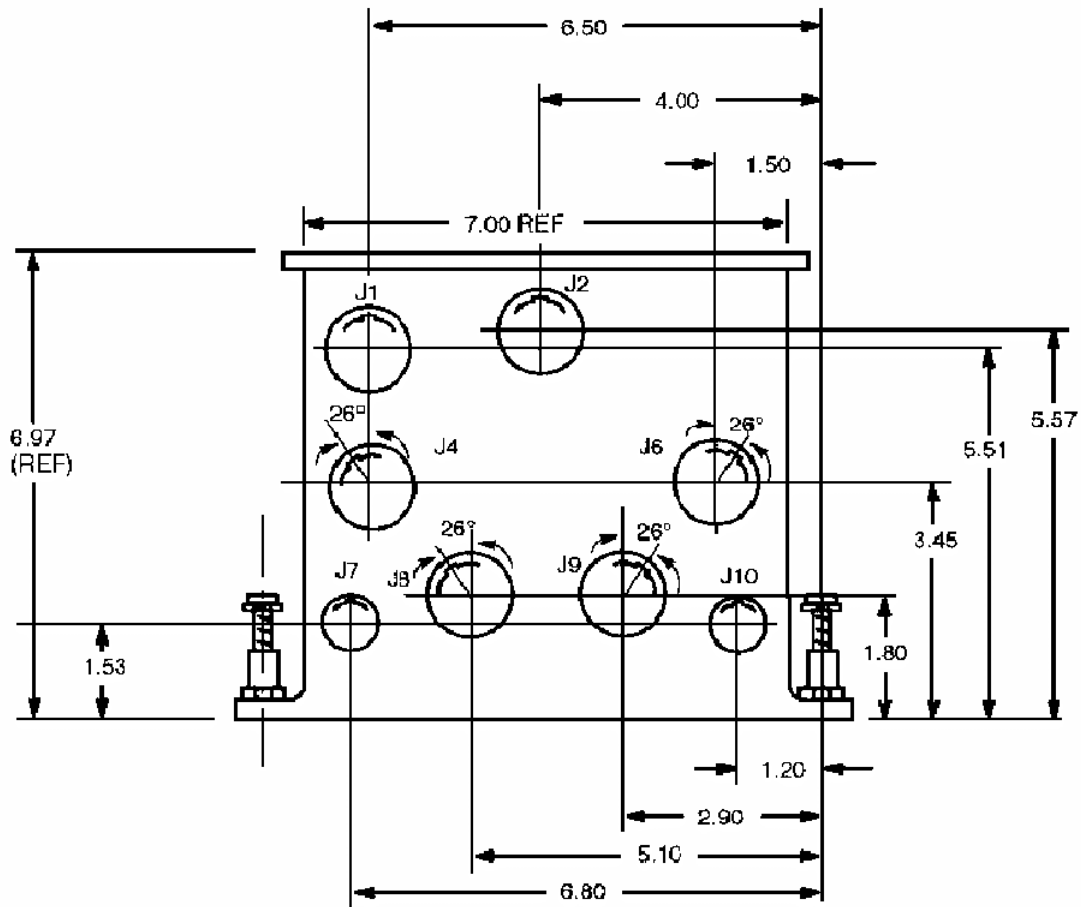
NOTES: (UNLESS OTHERWISE SPECIFIED)

1. CONNECTOR LOCATION DIMENSIONS  $\pm 0.06$ .
2. CONNECTOR KEYWAY LOCATIONS ARE SHOWN FOR REF ONLY.

j\_18611\_4708

**Figure 27-7. Chassis-mother interconnect board-dedicated signal conditioner connector configuration -0001/-2001/-3001**





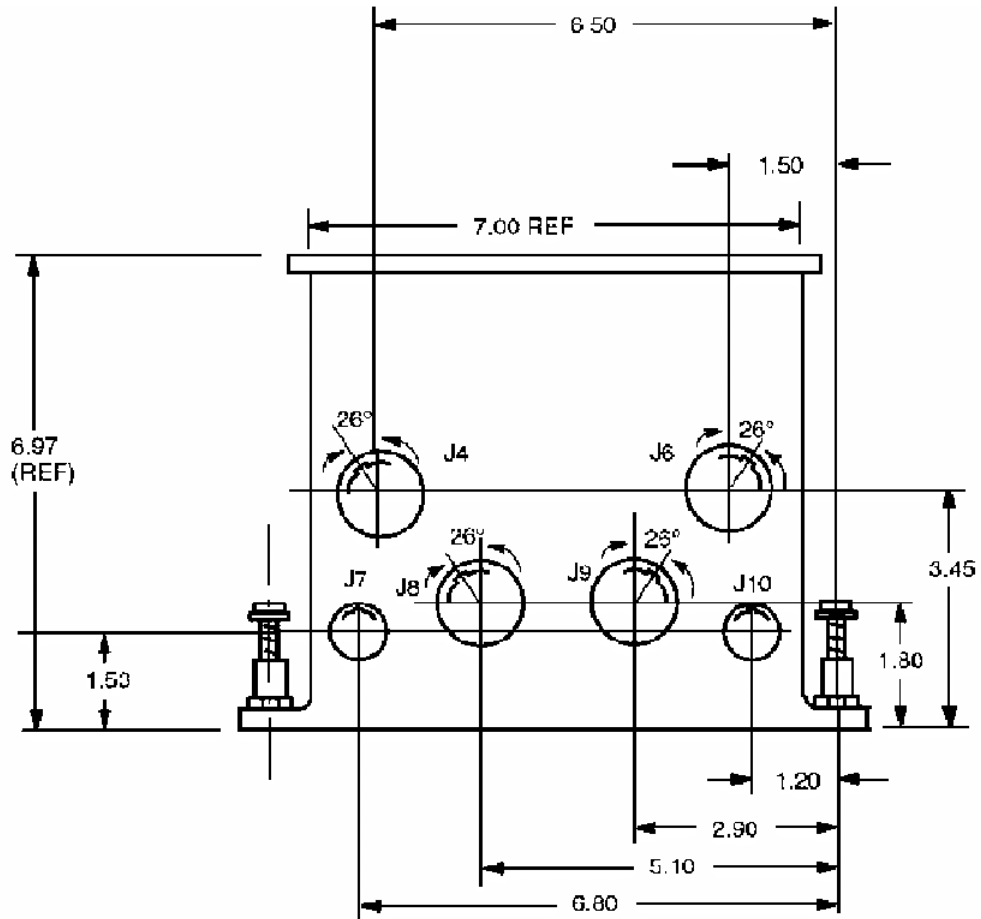
| CONNECTOR DATA |             |          |         |
|----------------|-------------|----------|---------|
| REF DES        | PART NO.    | FUNCTION | X NO.   |
| J1             | NLSOE2435P  | INPUT    | X17-X23 |
| J2             | NLSOE2235P  | OUTPUT   | X17-X23 |
| J4             | NLSOE2435PB | INPUT    | X1 -X8  |
| J6             | NLSOE2435PC | INPUT    | X9 -X16 |
| J7             | NBOE10-6PNC | POWER    |         |
| J8             | NLSOE2235PB | OUTPUT   | X1 -X8  |
| J9             | NLSOE2235PC | OUTPUT   | X9 -X16 |
| J10            | NBOE10-6PWC | POWER    |         |

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. CONNECTOR LOCATION DIMENSIONS  $\pm 0.06$ .
2. CONNECTOR KEYWAY LOCATIONS ARE SHOWN FOR REF ONLY.

1.18611.4709

**Figure 27-8. Chassis-mother interconnect board-dedicated signal conditioner connector configuration -0002**



| CONNECTOR DATA |             |          |         |
|----------------|-------------|----------|---------|
| REF DES        | PART NO.    | FUNCTION | X NO.   |
| J4             | NLSOE2435PB | INPUT    | X1 -X8  |
| J6             | NLSOE2435PC | INPUT    | X9 -X16 |
| J7             | NBOE10-6PNC | POWER    |         |
| J8             | NLSOE2235PB | OUTPUT   | X1 -X8  |
| J9             | NLSOE2235PC | OUTPUT   | X9 -X16 |
| J10            | NBOE10-6PWC | POWER    |         |

- NOTES: (UNLESS OTHERWISE SPECIFIED)  
 1. CONNECTOR LOCATION DIMENSIONS  $\pm 0.06$ .  
 2. CONNECTOR KEYWAY LOCATIONS ARE SHOWN FOR REF ONLY.

j\_18611\_4710

**Figure 27-9. Chassis-mother interconnect board-dedicated signal conditioner connector configuration -0003/-2003/-3003**

### 27.11 OPERATIONAL NOTES

The DSC BITE/power status can be observed on the OI MDM/DSC display, MSK 0995. The event lights will show the BITE parameters only; the signal conditioners that do not have their BITEs instrumented must be observed on the display.

Real-time data of DSC/MDMs may be observed on the DSC/MDM parameters, MSK 0999. The analog measurements shown on this display are a good indication of the general status of the DSC; if they all go to zero, all DSC data should be suspect until an in-depth investigation is completed.

### 27.12 REFERENCES

- A. Dedicated Signal Conditioners Specification (MC476-0131), Rockwell International, June 1, 1978.
- B. Shuttle Operational Data Book, JSC-08934, pg. 4.5.5-9, Vol. II, September 1982.
- C. Chassis-Mother Interconnect Board Specification (MC476-0147), Rockwell International, June 30, 1978.
- D. ELDEC Schematic Drawings, S7-040300, S7-040400, S7-043, S7-044, S7-047, S7-049, S7-051, S7-052.
- E. 16-Day EDO Pallet, VS70-450242, Rockwell International.

**SECTION 28 - MULTIPLEXER/DEMULTIPLEXER**  
**CONTENTS**

| <b>Section</b> |                                | <b>Page</b> |
|----------------|--------------------------------|-------------|
| 28.1           | GENERAL DESCRIPTION.....       | 28-1        |
| 28.1.1         | Interfaces .....               | 28-2        |
| 28.1.2         | Block Diagrams .....           | 28-4        |
| 28.2           | DESCRIPTION.....               | 28-5        |
| 28.2.1         | Input/Output Functions.....    | 28-5        |
| 28.2.2         | Power Supply System .....      | 28-7        |
| 28.2.3         | MDM Information Transfer ..... | 28-8        |
| 28.2.4         | Sequence Control Unit .....    | 28-9        |
| 28.2.5         | A/D Converter .....            | 28-16       |
| 28.2.6         | SCU PROM.....                  | 28-16       |
| 28.3           | ELECTRICAL .....               | 28-21       |
| 28.3.1         | Power .....                    | 28-22       |
| 28.4           | PHYSICAL CHARACTERISTICS.....  | 28-22       |
| 28.5           | INSTALLATION.....              | 28-23       |
| 28.5.1         | Location.....                  | 28-23       |
| 28.5.2         | Cooling .....                  | 28-24       |
| 28.6           | DESCRIPTION OF OPERATION.....  | 28-28       |
| 28.6.1         | Crew Controls .....            | 28-28       |
| 28.6.2         | Telemetry .....                | 28-28       |
| 28.7           | SPECIAL COMPUTATIONS .....     | 28-29       |
| 28.8           | EMDM ENHANCEMENTS .....        | 28-29       |
| 28.8.1         | Gate Array Logic .....         | 28-30       |
| 28.8.2         | MIA/SCU Interface .....        | 28-30       |
| 28.8.3         | IOM Power Supplies .....       | 28-30       |
| 28.8.4         | IOM Interface .....            | 28-31       |
| 28.9           | REFERENCES.....                | 28-31       |

## TABLES

| Table |  | Page  |
|-------|--|-------|
| 28-1  | MDM I/O card mix.....                    | 28-5  |
| 28-2  | Power switches and circuit breakers..... | 28-21 |
| 28-3  | Supply power/consumption.....            | 28-22 |
| 28-4  | OI MDM locations .....                   | 28-23 |
| 28-5  | OI MDM cooling .....                     | 28-24 |
| 28-6  | BITE/wrap computations.....              | 28-29 |

## FIGURES

| Figure |   |       |
|--------|---|-------|
| 28-1   | Basic multiplexer diagram.....            | 28-2  |
| 28-2   | OI MDM system diagram .....               | 28-3  |
| 28-3   | Relationship of MDM components.....       | 28-4  |
| 28-4   | MDM connector configuration.....          | 28-23 |
| 28-5   | Hardware locations .....                  | 28-24 |
| 28-6   | Component locations, bay 1 .....          | 28-25 |
| 28-7   | Component locations, bay 2 .....          | 28-26 |
| 28-8   | Component locations, bay 3A.....          | 28-27 |
| 28-9   | Component locations, flight deck.....     | 28-28 |
| 28-10  | Power distribution: MDM versus EMDM ..... | 28-30 |

## SECTION 28

### MULTIPLEXER/DEMULTIPLEXER

#### 28.1 GENERAL DESCRIPTION

The multiplexer receives analog, discrete, or serial digital information from the shuttle subsystems and converts and formats these data into serial digital words for transmission to the data bus of the controlling unit, the Input/Output Processor (IOP), Pulse-Code Modulation Master Unit (PCMMU), or Ground Support Equipment (GSE).

The demultiplexer accepts serial digital information from the controlling unit and converts it to analog, discrete, or serial digital form for transmission to the shuttle subsystems.

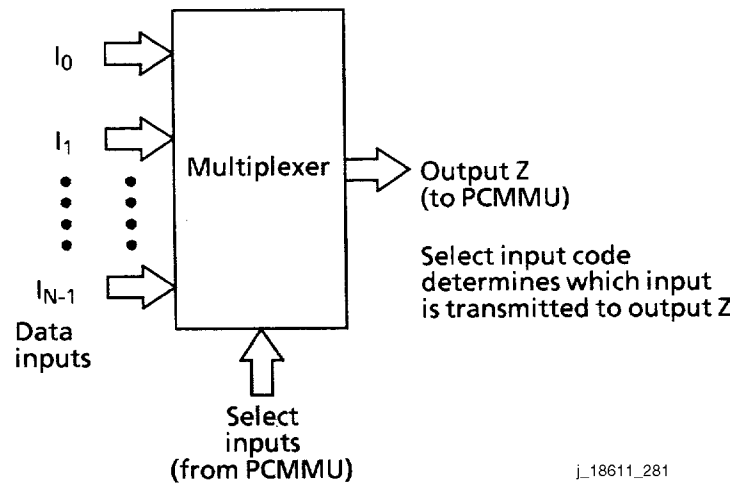
The basic types of orbiter Multiplexer/Demultiplexers (MDMs) are

- Flight critical MDMs FF 1-4
- Flight critical MDMs FA 1-4
- Operational instrumentation MDMs OF 1-4, OA 1-3
- Mission critical MDMs PF 1-2
- Ground interface (prelaunch) MDMs LF 1, LA 1

The difference between the MDM types is in the selection of the Input/Output Module (IOM) cards and their corresponding power supply modules, the Sequence Control Unit (SCU) Programmable Read-Only Memory (PROM), which reflects the IOM configuration, and the individual MDM wired addresses. Other than these differences, the MDMs are identical.

In the case of the Operational Instrumentation (OI) MDMs, only the multiplex function is performed. The scope of this brief is limited to the OI MDMs which utilize a small portion of the MDM capabilities. Information on the other functions may be found in the OPS Shuttle Flight Operations Manual and drawing 8.8 of the Shuttle Systems Handbook.

The OI MDMs are used by the OI subsystem for the acquisition of data from various sensors, either directly from the sensor itself or through the signal conditioners. Signals input to the MDMs are data types defined as single-ended dc, differential dc, discrete 0 to 5 V dc and 0 to 28 V dc, and serial digital. The MDM (Figure 28-1) will convert the analog inputs to digital data and then output serial digital data to the PCMMU upon request. The request from the CMMU is made by the PCMMU addressing a specific MDM for a specific measurement. An MDM will respond by selecting the appropriate channel, digitizing the parameter, and sending the requested data to the PCMMU in serial digital form.

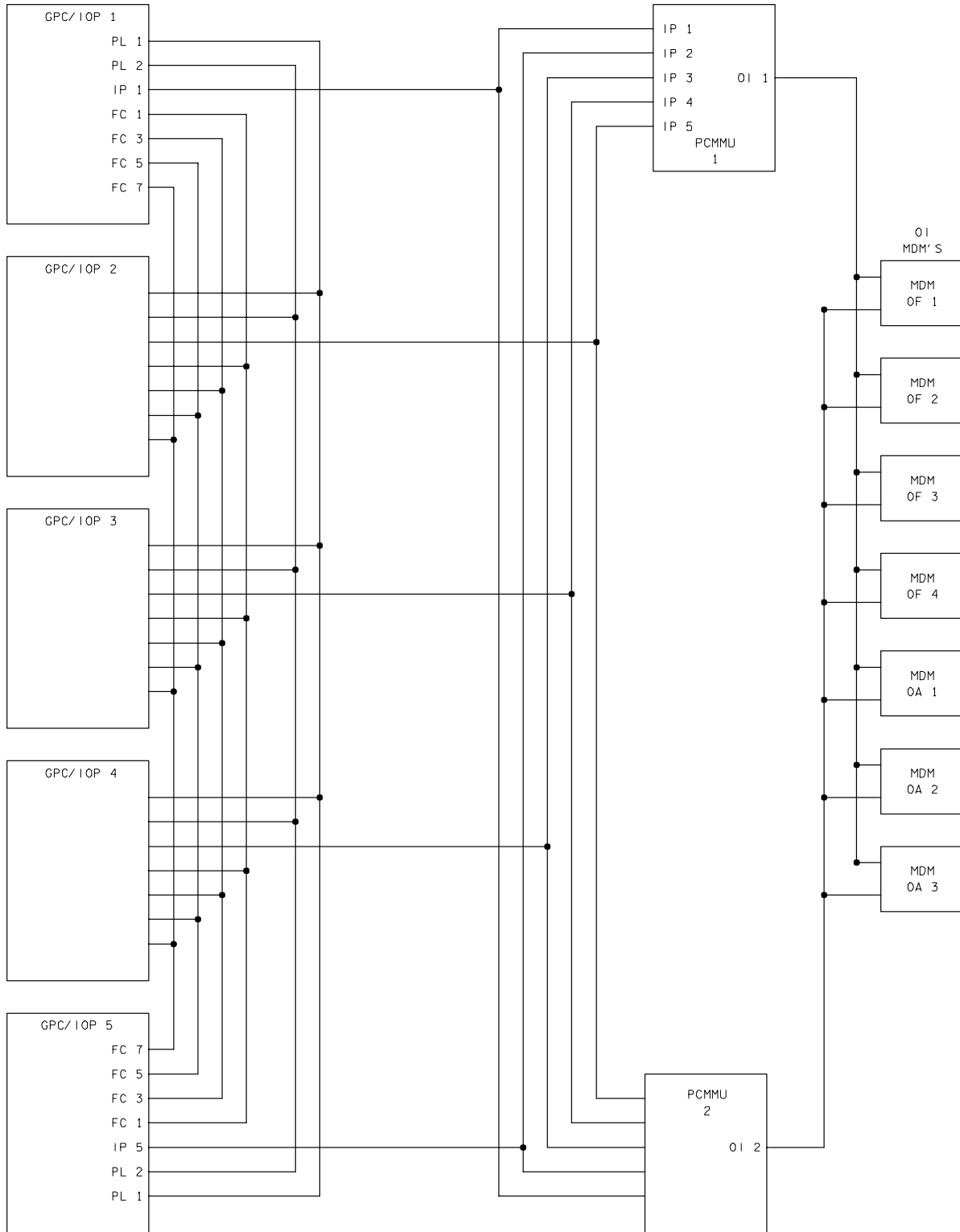


**Figure 28-1. Basic multiplexer diagram**

### 28.1.1 Interfaces

As shown by the diagrams of Figure 28-1 and Figure 28-2, only the PCMMUs are selecting data inputs and receiving the OI MDM digital outputs. Instrumentation subsystem data are accessed by the General Purpose Computers (GPCs) through these PCMMUs.

The various inputs shown in Figure 28-1 can be from numerous sources. There are 14 Dedicated Signal Conditioners (DSCs) which provide the majority of the signals. Other signal sources are directly wired from transducers, digital inputs from orbiter systems are available, and DSC type inputs are provided by orbiter Line Replaceable Units (LRUs) which contain DSC cards.



1617. ART 3

Figure 28-2. OI MDM system diagram



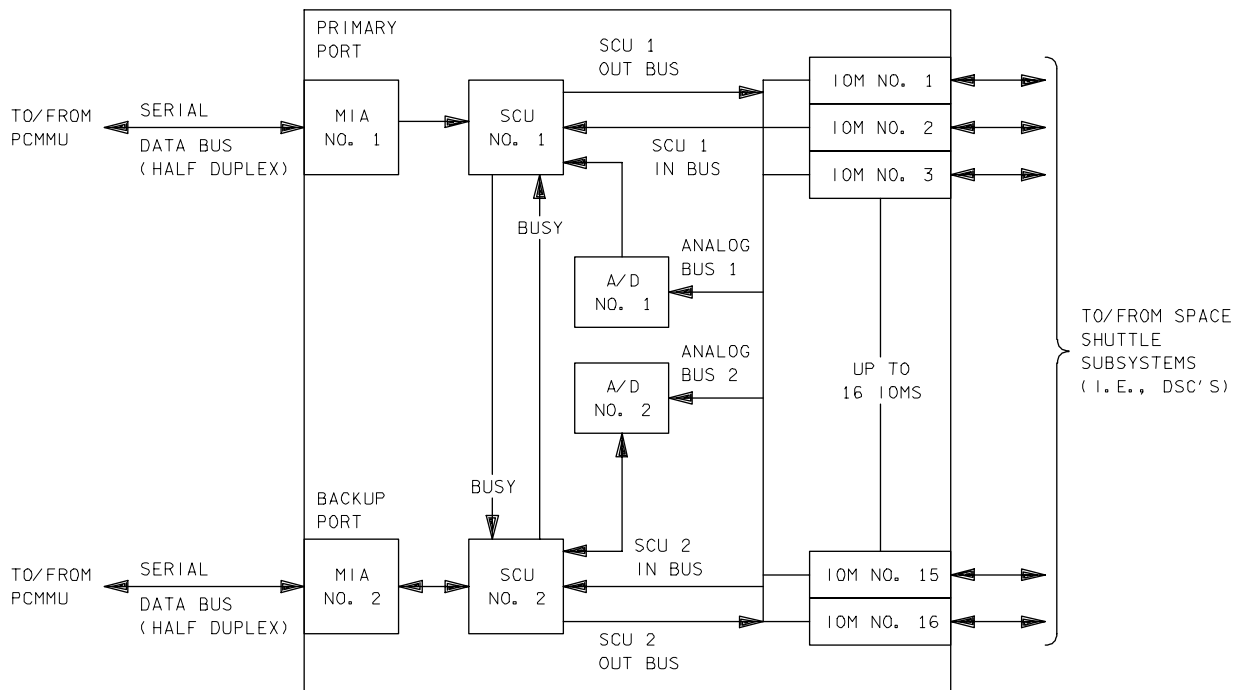
## 28.1.2 Block Diagrams

### 28.1.2.1 MDM System Block Diagram

Figure 28-2 shows the relationship between the GPCs, the PCMMUs, and the OI MDMs. The data bus paths have been simplified for clarity. The actual bus paths and positions of the data bus couplers are illustrated in the Space Shuttle Systems Handbook, drawing 17.1-1.

### 28.1.2.2 MDM Block Diagram

An MDM consists of two Multiplexer Interface Adapters (MIAs) which connect the MDM to the data buses; two SCUs for controlling internal MDM operation; a redundant power supply system; two Analog-to-Digital (A/D) converters; and up to 16 IOMs to interface with the space shuttle subsystems. Figure 28-3 illustrates the relationship of the MDM components.



MIA - MULTIPLEXER INTERFACE ADAPTER  
SCU - SEQUENCE CONTROL UNIT  
IOM - INPUT/OUTPUT MODULE  
A/D - ANALOG TO DIGITAL CONVERTER  
PCMMU - PULSE CODE MODULATION MASTER UNIT

186112805. ART; 2

**Figure 28-3. Relationship of MDM components**

## 28.2 DESCRIPTION

The following paragraphs describe the operations of the OI MDMs.

### 28.2.1 Input/Output Functions

#### A. Multiplexer Interface Adapter

The MDM interfaces with the PCMMU through the MIA, which provides for bidirectional, half duplex, serial data flow. The MIA performs the following tasks.

1. Listens for and recognizes host address
2. Provides impedance match to bus
3. Checks for proper waveform of incoming data
4. Checks and counts number of data words host is expecting
5. Checks validity of data by parity count
6. Converts data bus coding (Bi $\phi$ -L, also called Manchester), into host coding Non-Return-to-Zero (NRZ)
7. Accepts NRZ data from host to be transmitted on bus
8. Converts NRZ code to Bi $\phi$ -L
9. Assigns parity bit, adds a sync pattern, and transmits data to bus

Each MDM can be controlled through either of two ports (primary and backup), but not simultaneously. Normally, an MDM is controlled through the primary port, over the primary serial data bus. Should a failure occur in the primary serial data bus or to the primary MIA, SCU, or A/D within the MDM, fault recovery can be achieved by switching to the backup port. The switch is accomplished by performing a "port mode" on an MDM which interfaces with the GPCs or by switching PCMMUs when an OI MDM is at fault. This will result in the use of the backup MIA, SCU, and A/D within the MDM.

#### B. Input/Output Modules

The OI MDMs may have up to 16 various IOMs. Table 28-1 shows the mix of cards contained in the MDMs along with a key to IOM types.

**Table 28-1. MDM I/O card mix**

| MDM | IOM location |     |     |     |     |     |     |     |      |     |     |     |     |     |     |     |
|-----|--------------|-----|-----|-----|-----|-----|-----|-----|------|-----|-----|-----|-----|-----|-----|-----|
|     | 0            | 1   | 2   | 3   | 4   | 5   | 6   | 7   | 8    | 9   | 10  | 11  | 12  | 13  | 14  | 15  |
| OF1 | SIO          | AIS | DIL | AIS | DIH | AIS | DIH | AIS | AID* | AIS | DIL | AIS | DIH | AIS | DIH | AIS |
| OF2 | SIO          | AIS | DIL | AIS | DIH | AIS | DIH | AIS | AID  | AIS | DIL | AIS | DIH | AIS | DIH | AIS |

**Table 28-1. MDM I/O card mix (concluded)**

|           |      |     |     |     |     |     |     |     |      |     |     |     |     |     |     |     |
|-----------|------|-----|-----|-----|-----|-----|-----|-----|------|-----|-----|-----|-----|-----|-----|-----|
| OF3       | SIO* | AIS | DIL | AIS | DIH | AIS | DIH | AIS | AID  | AIS | DIL | AIS | DIH | AIS | DIH | AIS |
| OF4       | DIL  | AIS | DIH | DIL | DIH | DIH | AIS | DIH | DIL* | AIS | DIH | AIS | DIH | DIH | AIS | DIH |
| OA1 - AO3 | AIS  | DIH | AIS | DIL | AIS | DIH | AIS | DIH | DIL* | AIS | DIH | AIS | DIH | AIS | DIL | AIS |

\*IOMs present but not used

|     | IOMs                         | Range              | Maximum       |
|-----|------------------------------|--------------------|---------------|
| AIS | - Analog input single-ended  | -5.12 to 5.11 V dc | 5.12 V dc In  |
| AID | - Analog input differential  | -5.12 to 5.11 V dc | 5.12 V dc In  |
| AOD | - Analog output differential | -5.12 to 5.11 V dc | 5.12 V dc Out |
| DIL | - Discrete input low         | 0 and 5 V dc       |               |
| DOL | - Discrete output low        | 0 and 5 V dc       |               |
| DIH | - Discrete input high        | 0 and 28 V dc      |               |
| DOH | - Discrete output high       | 0 and 28 V dc      |               |
| SIO | - Serial input/output        | -5 and 5 V dc      |               |

Although the IOMs do not incorporate redundant circuit design, functional redundancy for critical subsystems is achieved by using two same-type IOMs to carry redundant signals. Individual IOM failures will remain isolated to that IOM.

1. DC analog input module, single-ended (AIS)

This module accepts up to 32 single-ended dc inputs (channels) in the range of -5.12 to 5.11 V dc. The maximum allowable voltage difference between a signal and its return is 5.12 V. The AIS module provides unity voltage gain, and high current gain. The dc input voltages are subsequently A/D converted and sent to the PCMMU. Accuracy of converted signals is 0.5 percent RMS of the full-scale input (5.12 V dc).

Self-test for each analog input channel is performed by using a Built-In Test Equipment (BITE) reference voltage and the actual analog input signal. The input signal is reduced by half, the BITE reference voltage is added, and the resultant signal is A/D converted. This approach allows all channels, including those at full-scale input, to be tested with the same procedure. Two words are sent to the PCMMU for each channel tested. The first word contains one-half the analog input value plus the BITE reference voltage. The second word contains the analog input value. The controlling unit subtracts one-half of the second word from the first word. If the resulting signal is equal to the BITE reference voltage, the channel is verified.

2. DC analog input module, differential (AID)

This module can accept up to 16 pairs (channels) of differential input voltages in the range of -5.12 to 5.11 V dc. The maximum allowable voltage differential of a signal pair is 5.12 V dc. The module provides unity voltage gain and high current gain. The dc input voltages are subsequently A/D converted and sent

to the PCMMU. Accuracy of converted signals is 0.5 percent Root Mean Square (RMS) of full-scale input (5.12 V dc).

Self-test for each analog input channel is performed as described for the AIS module.

3. Discrete input (5 V) module (DIL)

This module accepts up to 48 discrete low-level signals (0 to 5 V dc levels) from space shuttle subsystems and formats the data into three 16-bit words for serial transmission to the PCMMU.

Self-test is performed by inserting BITE true and complement test words into each of the input channels as commanded by the SCU. A different BITE test word is provided for each of the three channels. The PCMMU controlling the MDM operation checks the BITE test patterns to verify module performance.

4. Discrete input (28 V) module (DIH)

This module accepts up to 48 discrete high-level signals (0 or 28 V dc levels) from space shuttle subsystems and formats the data into three 16-bit words for serial transmission to the PCMMU.

Self-test is performed in the same manner as for the DIL module described above.

5. Serial input/output module (SIO)

This module contains four identical serial Input/Output (I/O) data channels for interface to four space shuttle subsystems. Each serial I/O channel is dedicated to a single subsystem. Data transmission over each channel is half duplex, Bi- $\phi$ L (Manchester) format, in 20 bit words, 1 microsecond per bit.

### 28.2.2 Power Supply System

The MDM incorporates a redundant power supply system to provide redundant power to each circuit card and IOM within the MDM. All power supplies operate continuously, deriving their power from both 28 V dc input buses. However, a single primary 28 V dc bus is capable of providing power for the entire MDM. A failure in any of the supply units leads to an automatic switchover to the alternate power supply.

### A. Powerup Sequence

At powerup (normal or after the occurrence of a power transient) the MDM is operational within 10 milliseconds from the time the input power reaches 24 V dc. This is the minimum primary voltage specified for MDM operation. The MDM then runs a series of SCU BITE tests. If an SCU fails, its MIA is held reset. Thus an initial failure condition is indicated by the MDMs lack of response to commands directed to it after the 10 millisecond turn-on period.

Following the powerup sequence, the MDM returns the first commanded response data word with an invalid SEV pattern (S-bit cleared to 0), and bit 1 of the BITE Status Register (BSR) is set (power interrupt bit). The invalid S-bit indicates all analog and discrete outputs have been reset to 0 V dc (if the first response data word contains the contents of the BITE status register, the SEV is forced to the valid 101 pattern, to ensure the PCMMU receives the information. In this case, bit 1 of the BSR serves to indicate that a powerup sequence has occurred). Refer to Section 28.2.6.B (Data Words) for more on SEV codes.

### B. Loss of Input Power

The power supply can lose both 28 V dc inputs for periods less than 2 milliseconds without affecting MDM operation. If the loss of input exceeds this time, the poweroff sequence is initiated and runs to completion, regardless of a subsequent return of input power. The poweroff sequence sets bit 1 in the BSR and resets all MDM outputs. A return of one or both primary sources to a voltage level above +24 V dc initiates a new powerup sequence.

### C. Power Supply BITE Test

The power supply incorporates test equipment that is initiated by the controlling IOP, which is the PCMMU for the OI MDMs. However, this function is not available in the PCMMU. The BITE tests determine if power capability is available for each IOM, SCU, A/D, and MIA. The test is accomplished by interrupting the reference voltage on one power supply while monitoring the load current output of the other side. A failure on either side sets bit 2 (incoming data error) in the BSR.

## 28.2.3 MDM Information Transfer

When information is being received from a shuttle subsystem, it is referred to as input response data. Information flow from the PCMMU controlling an MDM operation occurs in the form of serial 28 bit words called command words. The command words are retained by the SCU for internal mode control and initialization.

The data received from the space shuttle subsystems (in analog, discrete, and serial digital form) are converted and formatted into 28 bit words for retransmission to the PCMMU which requested the information. These words are referred to as response data words. Each word consists of either one A/D converted analog signal, 16 discrete signals, or 16 bits of serial digital data.

In the direct mode, up to 32 response data words may be initiated by one command word. In the indirect mode, through use of the SCU PROM, up to 512 response data words (non-BITE), and up to 1024 BITE words may be recovered in a single block.

### 28.2.4 Sequence Control Unit

The SCU controls all operations of the MDM by executing microprograms from a 512-word, 40-bit/word programmable PROM contained within the SCU. Command words are received by the MIA and converted into control signals for operation of the IOMs. Similarly, the SCU accepts information from the IOMs and formats it into serial response data words for retransmission by the MIA to the PCMMU.

There are two SCUs within the MDM, only one of which controls the MDM at any one time. The primary and backup SCUs connect to the primary and backup MIAs, respectively. An SCU provides all MDM timing and contains counters, registers (including the 16-bit BITE status register), and two Read-Only Memories (ROMs). The functional parts of the SCU are described below:

#### A. Receiver Sync Logic

This logical element serially receives the incoming command from the MIA and synchronizes it to SCU timing. The element also performs various tests on the incoming information. The tests consist of verification of: proper sync for the incoming word (command sync for first word of a message, data sync for all subsequent words); proper gap time between the incoming word and the preceding word; proper MDM address; proper Manchester, bit count, and parity indications from the MIA; and the absence of an indication that the other SCU is busy.

In addition to the error detection circuitry, the element consists of a 5-bit shift register to receive the incoming serial information (1 MHz bit rate). The information is then parallel-transferred either four or five bits at a time onto a 5-bit internal SCU bus. During the reception of the first part of a command word, the receiver sync logic operates independently of SCU microinstruction control. Thereafter, SCU microinstructions, in part, control operation of the element.

The following illustrates the fields comprising command words specifying direct and indirect modes of operation.

| Command word<br>(direct mode) |                       | Command word<br>(direct mode) |                       |
|-------------------------------|-----------------------|-------------------------------|-----------------------|
| <u>Bits</u>                   | <u>Function</u>       | <u>Bits</u>                   | <u>Function</u>       |
| 1-3                           | sync (removed at MIA) | 1-3                           | sync (removed at MIA) |
| 4-8                           | MDM address           | 4-8                           | MDM address           |
| 9                             | Spare                 | 9                             | Spare                 |
| 10-13                         | Mode control field    | 10-13                         | Mode control field    |
| 14-17                         | Module address        | 14-22                         | PROM starting address |

18-22 Channel address  
23-27 Number of words (channels)

23-27 Number of instructions

After the MIA has received a valid sync pattern (bits 1 through 3), the subsequent bits of the incoming word are serially shifted to the receiver sync logic circuitry. At bit time 8 (referenced to the bits of the incoming word) the receiver sync logic compares the MDM address with the address of the incoming word. If the address matches and the MIA indicates a command sync code, the element power strobes SCU control store to begin microinstruction execution.

Bits 10 through 13 (mode control field) are then shifted into the receiver sync logic. At bit time 13, the information is parallel-transferred to a register file, where the information is accessible to the SCU microcode. At this point, microinstructions executed at the rate of one per microsecond, examine the mode field and determine if the command word is specifying a direct or indirect mode of operation. Based on this determination, subsequent 4- and 5-bit fields of incoming information will be directed to various holding registers of the register file.

#### B. Register File

The register file consists of a total of eight 5-bit registers. These registers hold the mode, IOM address, channel address, and number-of-words-to-be-transferred fields for direct operation. They also hold, for indirect mode (sequence memory PROM) operations, the sequence memory address and number of sequence memory instruction to be executed. One of the 5-bit registers of the register file consists of bits 12 to 16 of the BITE status register.

#### C. BITE Status Register

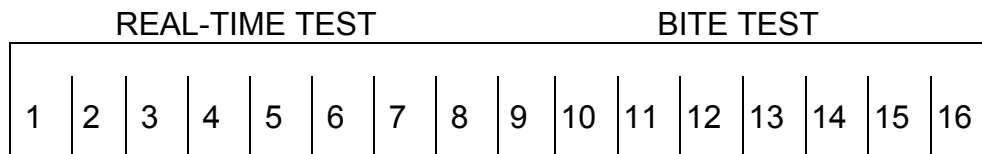
The SCU performs extensive real-time tests during MDM input and output operations. The result of these tests is to set a bit in the SCU BSR if an error is detected. The information remains in the BSR until a command word is received to send the contents of the BSR to the PCMMU. The response data word containing the BSR contents also contains a forced proper SEV (101) pattern to guarantee that the word will be accepted by the controlling unit requesting the MDM status. The status register is reset when read. The register is also reset by a command word specifying a master reset. In the case of a master reset, all IOMs are simultaneously reset. All analog signals are reset to 0 volt and all discrete signals to logical zero.

If the BITE circuitry detects an error during a response data word transaction, the MDM sets a bit in the BSR and sets an invalid SEV pattern in the word in transit. The SEV bits for any subsequent response data words are reset to the proper 101 pattern if no errors are detected.

Bits 1 through 11 are operational during normal MDM operation and during BITE tests.

Bits 12 through 16 are only operational when the MDM is performing BITE tests; otherwise, they remain in the zero state.

The 16-bit MDM BSR is illustrated below. A separate BSR exists in each SCU. When an error condition is detected, a bit is set in the BSR of the SCU which is active at the time of the error. A bit is not set in the BSR of the second SCU. An exception exists for power anomalies. During the powerup and powerdown sequences, a power-applied interrupt bit is set in both BSRs. The first 11 bits of the BSR are operational during normal MDM operation and during BITE tests. Bits 12 through 16 are only operational for BITE tests; they remain in the zero state otherwise.



- | BIT | INDICATION  |
|-----|---|
| 1   | Power interrupt                                   |
| 2   | Incoming data error (command word, command data   |
| 3   | Operation requested on a nonexistent channel      |
| 4   | Unable to transfer data to/from IOM               |
| 5   | Too many words in last message                    |
| 6   | Last command not completed                        |
| 7   | Simultaneous execution on primary and backup data |
| 8   | Illegal mode commanded                            |
| 9   | Internal error detected                           |
| 10  | Gap time error                                    |
| 11  | Successful BITE completion                        |

Bits 1 to 11 are held by the BSR and bits 12 to 16 are held by the register file described in a previous section.

In the following descriptions of the BSR bits only the five preceded by INST are of any real interest to the Instrumentation/Integrated Communications Officer (INST/INCO) personnel. The other bits are used to analyze the status of the Data Processing System (DPS) MDMs and are included for completeness.

**INST**

**Bit 1** power interrupt - This bit is set in only two instances: during the powerup sequence and 100 ms prior to MDM shutdown. The bit indicates that all analog and discrete outputs have been, or are about to be, reset to 0 V dc.



INST

Bit 2 incoming data error - This bit indicates that the incoming command word or command data word was detected to have an error.

For command words (with valid MDM address) the error was either nonvalid Manchester code, too few bits, or bad parity. If the command word is part of a command data word message, subsequently appearing command data words are discarded and cause no additional bits to be set in the BSR.

For command data words, bit 2 is set for incorrect MDM address, nonvalid Manchester code, too few bits, improper SEV code or parity error. The word is not processed. Subsequent command data words of the same message are also not processed. Bit 2 is also set during power supply BITE test failure. Refer to Section 28.2.1.C (Power Supply BITE Test).

Bit 3 operation requested on a nonexistent channel - This bit can be set during command data and response data messages. The occurrence of the error does not halt the command data or response data word message sequence.

The command word channel address field allows 32 channels to be addressed; however, not all IOM types have 32 channels. The above bit is set if the channel address field specifies an address beyond the range of the selected IOM. If this error occurs, BSR bit 4 is also set (unable to transfer data to/from selected IOM).

For command data word messages, subsequent command data words are accepted if the channels are subsequently correctly addressed. During indirect mode processing (use of SCU PROM) this implementation will cause outputs to be accepted and issued by the remaining IOMs of the PROM sequence.

For response data word messages, an operation requested on a nonexistent channel does not prevent a serial data bus word from being issued to IOP, PCM, or GSE units. The data contained within the response data word are invalid, however, and the V-bit is cleared to a logical "0" to indicate this condition. Processing continues. V-bit decisions are made on a response data word basis thereafter.

BSR bit 3 is set during command data and response data word times. If the IOM is operating properly, the actual error occurred in the preceding command word. This command word had an improper value in one or more of the following command word fields: module address, starting channel address, or number of words to be transmitted/received.

INST

Bit 4 unable to transfer data to/from IOM - This bit can be set during command data and response data messages. Processing can continue after the error condition. The bit is set if the IOM fails to reply to the SCU with a data transferred (operation completed) signal. For response data words, the V-bit is cleared for the word that encountered the error. Thereafter, V-bit decisions are made word by word.

Bit 5 too many words in last message - This bit can be set only during command data word messages. The first extra command data word of the command data word message causes the bit to be set. The extra command data word must fall within the allowable gap time limits (4 to 11  $\mu$ s); otherwise BSR bit 8 is set (illegal mode), indicating receipt of a command data word with no previous command word.

Additional command data words of the message are discarded and cause no additional bits to be set in the BSR.

Bit 6 last command not completed - This bit is set if a new command word is received on the same bus prior to the completion of processing for the previous command word on that bus. The new command will be accepted.

INST

Bit 7 simultaneous execution on primary and backup data bus - This bit is set if a command word is received by one SCU while the other SCU is busy. The condition will result in an immediate halt of processing for both SCUs. The interrupted SCU does not wait to complete processing for the command data or response data word in progress at the time of the interrupt. Either SCU will continue processing when it receives a new command word.

Bit 8 illegal mode commanded - This bit can be set by either a command word or a command data word

For command words, the bit is set for an incompatibility between the mode control and module address fields; for example, an output operation is specified for an input module. The bit is also set if an SCU PROM program attempts to execute both input and output operations in the same program. The bit is set if one of the four spare modes is commanded. The bit is set if one of the first 16 PROM words classifies an IOM as spare and the SCU attempts to address this IOM.

For command data words, the error condition is detected if the MDM receives a command data word without a prior command word.

INST

Bit 9 internal error detected - When this bit is set, the message (command data or response data) in progress is terminated upon occurrence of the error. However, a response data word in transit at the time of the error is completed with the V-bit cleared to a logical 0. BSR bit 9 is set in four instances: parity error for any of the 512 words of the sequence memory PROM; the IOM reply line is a logical one prior to the channel present time slot; the A/D reply line is a logical one prior to the data transferred (operation completed) time slot; or the SCU in bus check bits contain an invalid code.

Bit 10 gap time error - The SCU monitors the gap time between command words and between the command word and the first command data word. If an improper gap time is detected, the gap time error bit is set. All subsequent command data words are ignored until a new command word is received. The nominal proper gap between all words is  $5.5 \pm 0.5 \mu\text{s}$ .

Bit 11 successful BITE completion - This bit indicates that a successful self-test was performed.

Bit 12 BITE test - This field indicates progression through the BITE tests. The field to is only applicable during SCU, power supply and 16 A/D BITE tests.

Bit 16

D. Upper Counter, Lower Counter

These two counters are respectively 5- and 4-bit up/down counters, controllable via SCU microinstructions. The counters function, at times, to count down the number of words to be transferred, to increment channel addresses, and to hold and increment a 9-bit address for sequence memory (PROM) execution.

E. Sequence Memory (PROM)

The sequence memory is a 512-word by 16-bit memory. The first 16 locations of the PROM are used during direct operations to determine the type (class) of IOM at a particular IOM address. During these operations, the IOM address (initially held in the register file) is used to access one of the first 16 PROM locations. The IOM class field contained at the accessed address is then transferred to the register file for subsequent SCU microinstruction access. The IOM class field overlays the IOM address in the register file.

F. Control Store and Control Store Addressing Logic

The control store consists of a 512-word by 40-bit memory, used to hold SCU microinstructions. The microinstructions are 40 bits in length. A microinstruction contains separate fields for SCU in bus management, SCU out bus management, SCU internal bus select, register file transfers, sensing and setting condition codes, and conditional branching. Each microinstruction also contains a 9-bit field to allow

a direct branch to any of the other microinstructions. This 9-bit field is also used to store a cyclic check constant for real-time tests of SCU operation.

Microinstruction addressing is in the form of a 9-bit polynomial code, implemented via a shift register incorporating feedback. The shift register feedback arrangement produces 511 unique binary codes (patterns). The shift register is shifted or otherwise modified (via a control store mixer) once per microinstruction (microsecond). The 511 binary codes consist of all 9-bit codes except the code of all zeros. The all-zeros pattern constitutes a valid address, however; it may only be reached via a direct branch.

An 8-word by 9-bit pushdown stack allows subroutine branching and returns within a particular microprogram. The return address is placed at the top of the pushdown stack at the time of the subroutine branch. The pushdown stack (first in/last out) allows subroutines within subroutines to a level of eight.

#### G. Condition Set Decoding Logic

A total of 28 separate conditions (discrettes) may be set under microinstruction control for internal SCU operation. The conditions are used to initiate SCU logic operations or to record events during microinstruction execution.

#### H. Condition Sense Multiplexer

Fourteen conditions are detectable by the condition sense multiplexer. The conditions are used to modify microinstruction execution as a result of the occurrence of events such as error conditions.

#### I. Cyclic Matrix, Cyclic Register, Comparator, and Compare Register

This logic allows the real-time monitoring and test of the execution of all SCU microinstructions. During the execution of each microinstruction, a total of 46 control points (defining the present SCU status) is reduced by the cyclic matrix to an 8-bit number. A running sum of these numbers (one per microinstruction) is maintained, and approximately every tenth microinstruction is compared against a sum-check constant. The sum-check constant is contained within the 40-bit microinstruction field of the microinstruction presently being executed. A comparison indicates the validity of all SCU operations since the previous sum check. A noncomparison results in an immediate reset of both the MIA and SCU, truncating any operation in progress. The reset condition can be removed only by removal and reapplication of power to the MDM.

Cyclic sum checks are performed a minimum of three times for each sequence of microinstructions associated with the processing of each command, command data, or response data word. Every microinstruction executed by the SCU forms a part of some sum check. A failure of one SCU by the cyclic comparison tests leaves the operational capabilities of the redundant SCU unaffected.

J. SCU Out Bus Merge

This logic formats the serial control words from the SCU to the IOMs. The logical 0/logical 1 inputs to this logic are used to set the task and check bit codes during the task and check bit time slots.

K. SCU In Bus Merge

This logic formats the SCU in data into a response data word for retransmission by the MIA. The logical 1 inputs to this logic are used to set valid SEV bits during the BITE status register transmissions.

L. System Clock

The SCU contains a 16-MHz crystal oscillator to provide all timing for the MDM. A 16-MHz clock is provided to the MIA for its operation. A 1-MHz clock is provided for SCU operation. An 8-MHz clock is provided to the serial I/O IOM. All other IOMs receive a 1-MHz clock for IOM operation.

### 28.2.5 A/D Converter

There are two A/D converters, primary and backup, which interface with the primary and backup SCUs, respectively. The A/Ds function to convert analog input signals received from shuttle subsystems into digital signals for retransmission to the IOP, PCMMU, or GSE unit requesting the information. Each A/D converter connects to all analog input IOMs via separate analog buses. The module provides A/D conversion for 5.12 V (maximum) single-ended and differential dc signals, providing a 10-bit output (sign plus nine bits) in two's complement form, Least Significant Bit (LSB) equals 10 millivolts.

Analog signals are sampled, converted, and sent to the PCMMU at 1  $\mu$ s per bit.

### 28.2.6 SCU PROM

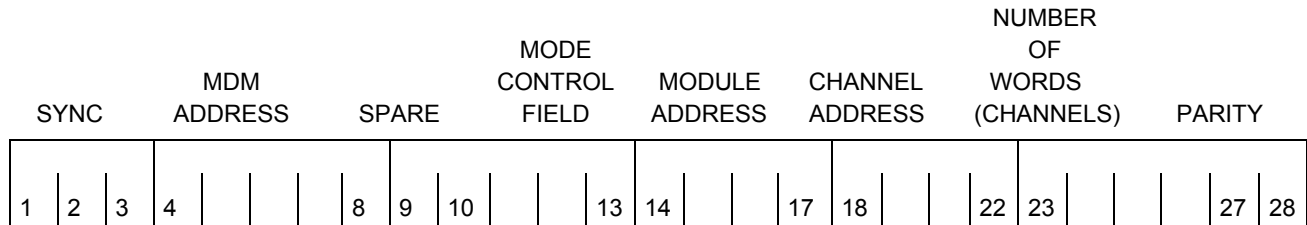
The 512-word SCU PROM dictates the flow of the indirect mode of data transfer. The first 16 PROM words reflect the IOM module configuration for the particular MDM. Each of the remaining 496 memory words resembles a command word.

The PROM contains a number of fixed programs. The maximum length of each program is 32 command words. When the contents of the first command sent to the MDM specify the indirect mode, the PROM starting address is read from the command word and the MDM transfer is then controlled by the corresponding PROM program. Where IOP, PCMMU, and GSE command words can initiate a response of up to 32 non-BITE (or 64 BITE) data words, the PROM command words can only solicit up to 16 non-BITE (or 32 BITE) data words. Thus, the maximum possible PROM-mode data transfer is 16 data words by 32 command words-per-program = 512 non-BITE words (or 32 by 32 = 1024 BITE words).

A. Command Words

The command words for the direct and indirect modes are illustrated below. Also shown in the PROM command word.

1. PCMMU Command Word - Direct mode



- a. MDM address - This 5-bit field specifies one of the seven IO MDMs within the space shuttle, 19 within the space shuttle orbiter data processing system and 4 within the solid rocket booster.
- b. Mode control field (PCM) - This field determines the operational mode of the MDM. The MDM modes of operation are defined as follows.

| <u>MDM control field</u> | <u>Description</u>  |
|--------------------------|---|
| 0001                     | BITE function: return the word at the specified PROM address                                  |
| 0010                     | Indirect mode: execute the word at the PROM address   |
| 0100                     | SCU BITE test   |
| 0101                     | A/D BITE test   |
| 0110                     | Power supply BITE test  |
| 0111                     | IOM BITE test   |
| 1000                     | Direct mode (output)  |
| 1001                     | Direct mode (input)   |
| 1010                     | Return the contents of the MDM BITE status register and reset the register.                   |
| 1011                     | Master reset: reset all outputs (discrete signals to logical "0"; analog signals to 0 volts). |

1100 BITE function: return the command word. The word that is returned actually differs from the word sent. Bits 1-8 of the return word contain the sync and MDM address fields. Bits 9-22 contain the module address, channel address, and number-of-words fields. Bits 23, 24 contain zeros. Bits 25-27 contain a SEV pattern. Bits 9-13 of the original command words are absent in the return command word.

1110 BITE function: load the MDM status register with the command data word that follows

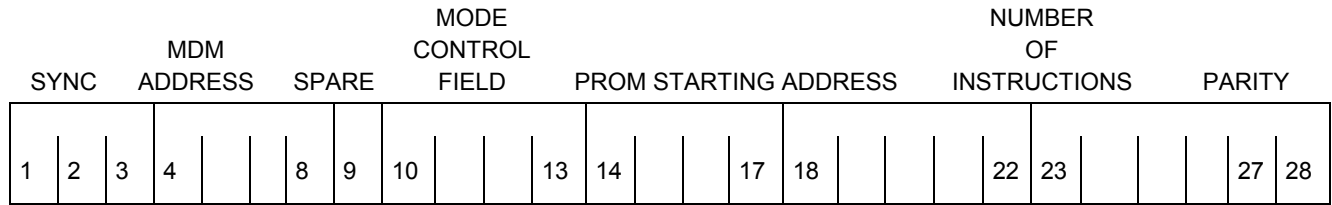
0000, 0011, SPARES  
1101, 1111

- c. Module address - This field specifies the card location of the IOM. There are 16 card locations (IOMs) numbered 0 through 15.
- d. Channel address -

| <u>IOM</u>                    | <u>Number of channels</u>   | <u>Addresses</u> |
|-------------------------------|---|------------------|
| Discrete input:               | 3 channels (16 signals/channel)   | 0 - 2            |
| Discrete output:              | 3 channels (16 signals/channel)   | 0 - 2            |
| Analog input (single-ended):  | 32 channels (1 signal/channel)  | 0 - 31           |
| Analog input (differential):  | 16 channels (1 signal pair/channel)                                     | 0 - 15           |
| Analog output (differential): | 16 channels (1 differential pair/channel)                               | 0 - 15           |
| Serial I/O:                   | 4 channels (1 bidirectional serial bus/channel)                         | 0 - 3            |
| TACAN radar altimeter:        | 3 channels (1 channel: 16 discrettes; 2 channels: simplex serial buses) | 0 - 1            |

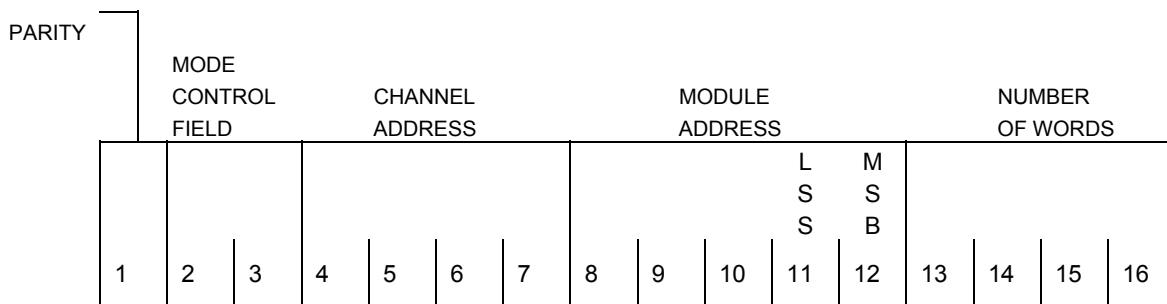
- e. Number of words (channels) - The SCU provides the capability for sequentially accessing up to 32 channels in direct mode (16 channels in indirect mode). The first channel is accessed by the module address and channel address fields described above. Thereafter, channels are sequentially accessed, in increasing order, until the required number of channels has been accessed. For the module that has 32 channels (analog input, single-ended) a wraparound capability exists. For this module, 32 sequential channels starting at any channel address can be read by one command word. Channel addressing proceeds from the last channel address to the first channel address automatically. This feature is implemented by a 5-bit (channel address) binary counter which increments to zero (first channel) after reaching the count of all ones (32nd channel).

2. IOP, PCMMU, GSE Command Word - Indirect mode



- a. PROM starting address - This 9-bit field defines the starting address for the PROM program used in the indirect mode of operation. The first 16 locations in the 512-word PROM memory are used for a special look-up function; PROM programs for indirect mode input/output begin at the 17th memory location.
- b. Number of PROM instructions - This 5-bit field defines the number of consecutive PROM instructions (command words) to be executed. The 5-bit field allows the specification of a 32-instruction (command word) program, maximum. PROM command words can initiate a 16-word data transfer (non-BITE-related) in contrast to IOP, PCMMU, or GSE command words, which can initiate a 32-word data transfer. A 32-instruction program could thus be used to control a 512-word (32 by 16) non-BITE data transfer.
- c. MDM address and mode control fields are identical to those described in the direct mode.

3. PROM Command Word



- a. Mode control field (PROM) - The contents of this field are defined as follows.
  - 00 - Initiate command data transfer
  - 01 - Initiate response data transfer
  - 10 - end the BITE status register and reset the BITE status register
  - 11 - Initiate IOM BITE
- b. Module address (PROM) - The 4-bit module address found in the PROM command word differs from the 4-bit module address found in the direct mode command word. The four bits are not straight binary



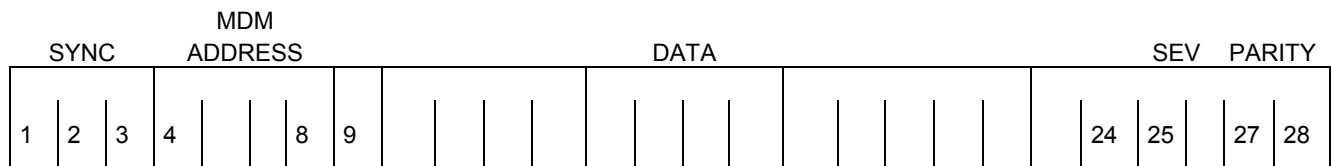
with the LSB on the right. The LSB is located in bit position 11, with the next higher bits located in bit positions 10 and 9. The MSB is located in bit position 12.

- c. Channel address (PROM) - The contents of this field are identical to that described for the direct mode channel address.
- d. Number of words (PROM) - For serial IOMs, this field determines the number of serial words to be transferred. The specification of a 16-word transfer is possible by this field. For all other IOMs, it specifies the number of consecutive channels to be addressed.

B. Data Words

Illustrated below is the command data word or response data word format. The command data word is issued to the MDM from an IOP, PCMMU, or GSE unit. The response data word is issued from the MDM to the IOP, PCMMU, or GSE unit requesting space shuttle subsystem status.

1. Command Data Word or Response Data Word



- a. Data - This 16-bit field defines the data to be sent to or received from a selected channel. The contents of the field are a function of each particular IOM type.
- b. SEV - These three bits are used for message validity test. A proper (valid) code is always 101. Command data words contain an SEV code, in contrast to command words, which do not. If the MDM receives any SEV code other than 101, neither the command data word, nor any subsequent command data words of the same message are processed. The MDM waits for the receipt of a new command word to initiate a new processing sequence.

Response data words also contain an SEV code. The SEV code for a response data word containing the contents of the MDM BITE status register is always forced to a valid 101 code to guarantee acceptance of the response word by IOP, PCMMU, or GSE units requesting such information.

Following the powerup sequence, the MDM clears the S-bit for the first requested response word (providing the word does not contain the contents of the BITE status register). The cleared S-bit serves as a flag

to indicate that all analog and discrete outputs have been reset to 0 V dc. The S-bits of subsequent response data words are not cleared.

The E-bit is associated with serial I/O modules. If serial I/O data are not successfully received (no data, improper sync, invalid Manchester code, or bad parity), the E-bit is set to a logical "1" (invalid). The E-bit is not set for data transmissions involving any other IOM.

The V-bit is cleared to a logical "0" (invalid) whenever an error has been detected inside the MDM for the response data word being transmitted.

### 28.3 ELECTRICAL

**Table 28-2. Power switches and circuit breakers**

| MDM      | Panel location                       |                                      |
|----------|--------------------------------------|--------------------------------------|
| OF1, OF2 | (014:B)<br>cb MNA OI MDM<br>OF 1/2 A | (015:B)<br>cb MNA OI MDM<br>OF 1/2 B |
| OF3, OF4 | (014:B)<br>cb MNA OI MDM<br>OF 3/4 A | (016:B)<br>cb MNC OI MDM<br>OF 3/4 B |
| OA1      | (017:D)<br>MDM, OA 1/2/3             | MNA, MNB                             |
| OA2      | (017:D)<br>MDM OA 1/2/3              | MNB, MNC                             |
| OA3      | (017:D)<br>MDM OA 1/2/3              | MNA, MNC                             |

28.3.1 Power

**Table 28-3. Supply power/consumption**

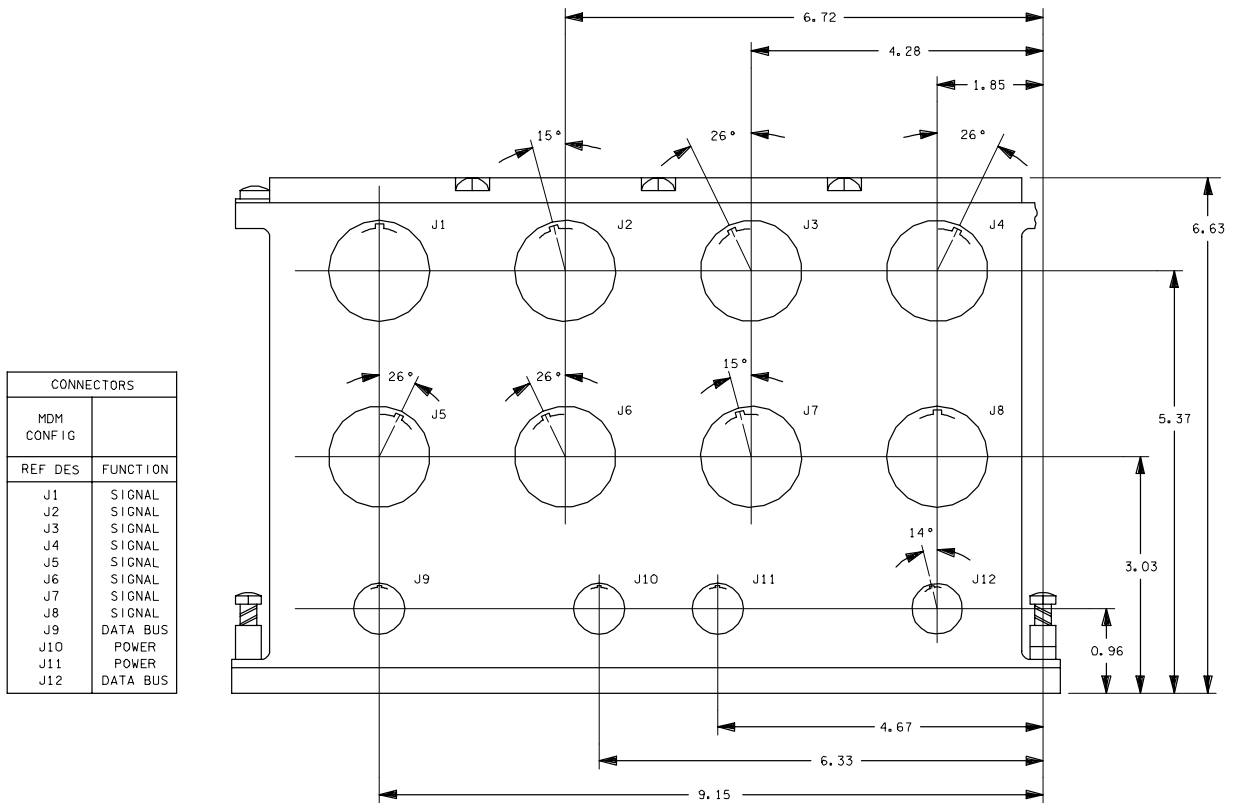
| MDM | Power consumption, W | Power bus            | Circuit protection       |
|-----|----------------------|----------------------|--------------------------|
| OF1 | 44.1                 | MNA 014<br>MNB 015   | 014 CB4<br>015 CB5       |
| OF2 | 44.1                 | MNA 014<br>MNB 015   | 014 CB4<br>015 CB5       |
| OF3 | 44.1                 | MNA 014<br>MNC 016   | 014 CB5<br>016 CB3       |
| OF4 | 44.1                 | MNA 014<br>MNC 016   | 014 CB5<br>016 CB3       |
| OA1 | 41.0                 | MNB APC5<br>MNA APC4 | RPC 5A<br>017 S19 RPC 5A |
| OA2 | 42.0                 | MNC APC6<br>MNB APC5 | RPC 5A<br>017 S19 RPC 5A |
| OA3 | 42.0                 | MNC APC6<br>MNA APC4 | RPC 5A<br>017 S19 RPC 5A |

**28.4 PHYSICAL CHARACTERISTICS**

- Manufacturer - Sperry Flight Systems  
Phoenix, Arizona
- Part number - MC 615-0004

Orbiter

- Size (LxWxH-inches) 13.0x11.6x6.6
- Weight (≈pounds max.) 38.5
- Number of IOMs 16



186112804.ART, 1

Figure 28-4. MDM connector configuration

## 28.5 INSTALLATION

The following is a description of the OI MDMs installation locations and cooling.

### 28.5.1 Location

Table 28-4. OI MDM locations

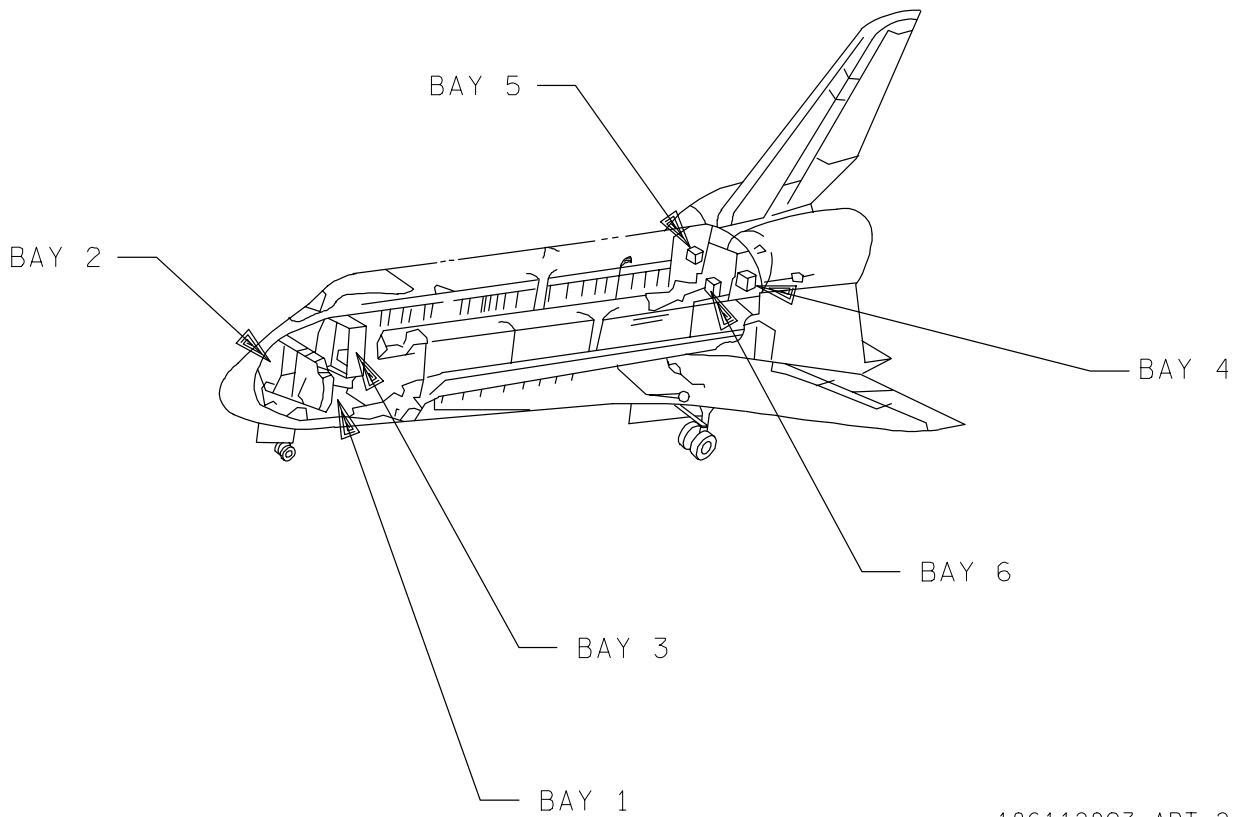
| MDM | Location    |
|-----|-------------|
| OF1 | AV Bay 1    |
| OF2 | AV Bay 2    |
| OF3 | AV Bay 3A   |
| OF4 | Flight Deck |
| OA1 | AV Bay 4    |
| OA2 | AV Bay 5    |
| OA3 | AV Bay 6    |

Figure 28-5 to Figure 28-9 show the locations of the MDMs.

28.5.2 Cooling

**Table 28-5. OI MDM cooling**

| MDM | Location        |
|-----|-----------------|
| OF1 | Coldplate/water |
| OF2 | Coldplate/water |
| OF3 | Coldplate/water |
| OF4 | Coldplate/water |
| OA1 | Coldplate/Freon |
| OA2 | Coldplate/Freon |
| OA3 | Coldplate/Freon |



186112803. ART; 2

**Figure 28-5. Hardware locations**

MODULAR LOCKERS MF --

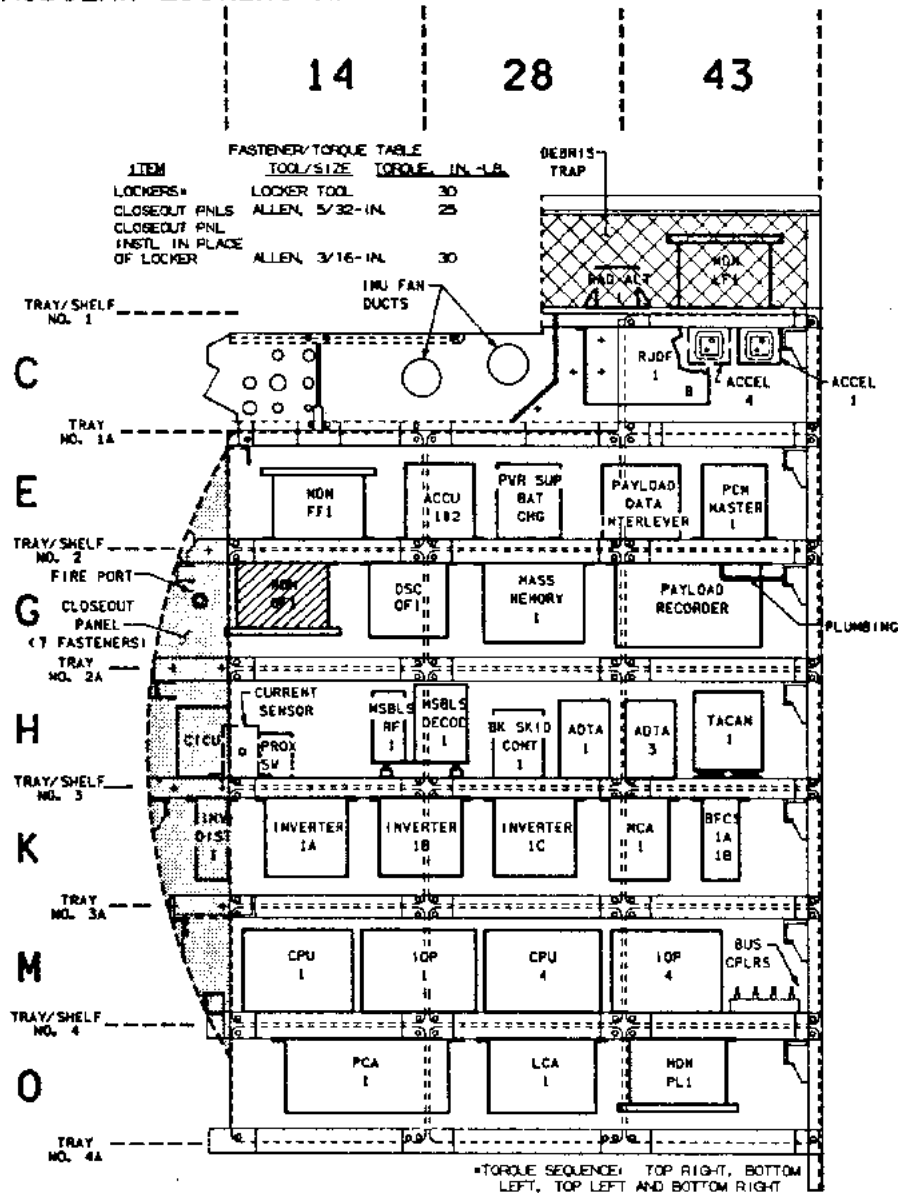


Figure 28-6. Component locations, bay 1

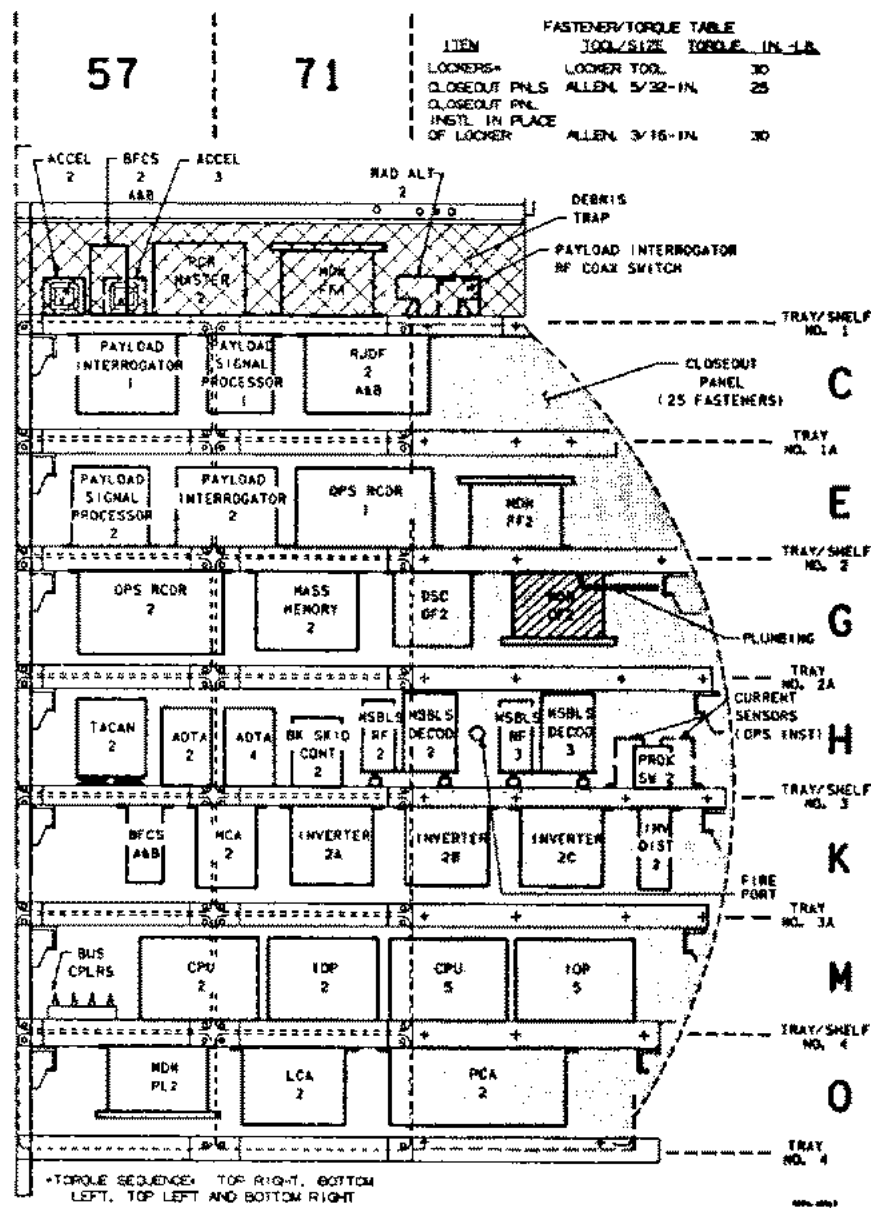


Figure 28-7. Component locations, bay 2

MODULAR LOCKERS MA --

| ITEM                                   | FASTENER/TORQUE TABLE |                |
|--|-----------------------|----------------|
|  | TOOL/SIZE             | TORQUE IN L.B. |
| LOCKERS*                               | LOCKER TOOL           | 30             |
| CLOSEOUT PANELS                        | ALLEN 5/32-IN.        | 25             |
| CLOSEOUT PNL INSTL. IN PLACE OF LOCKER | ALLEN 3/16-IN.        | 30             |

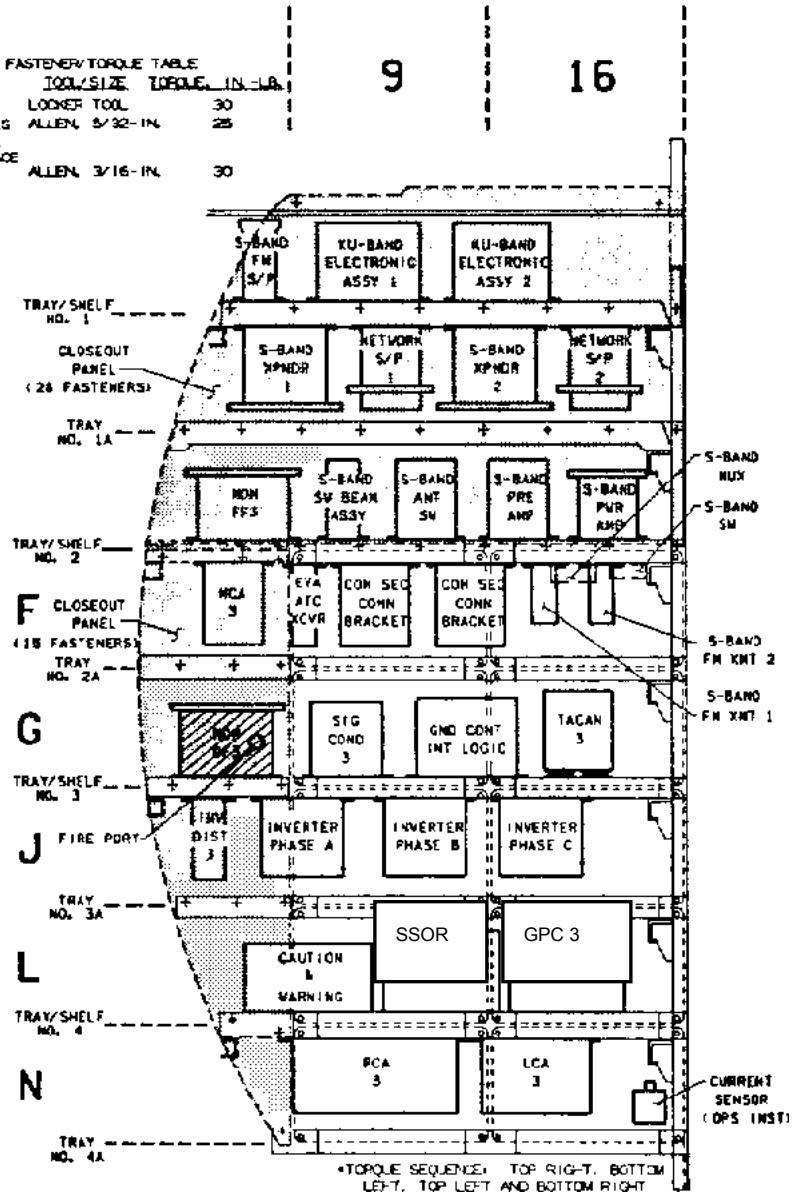


Figure 28-8. Component locations, bay 3A



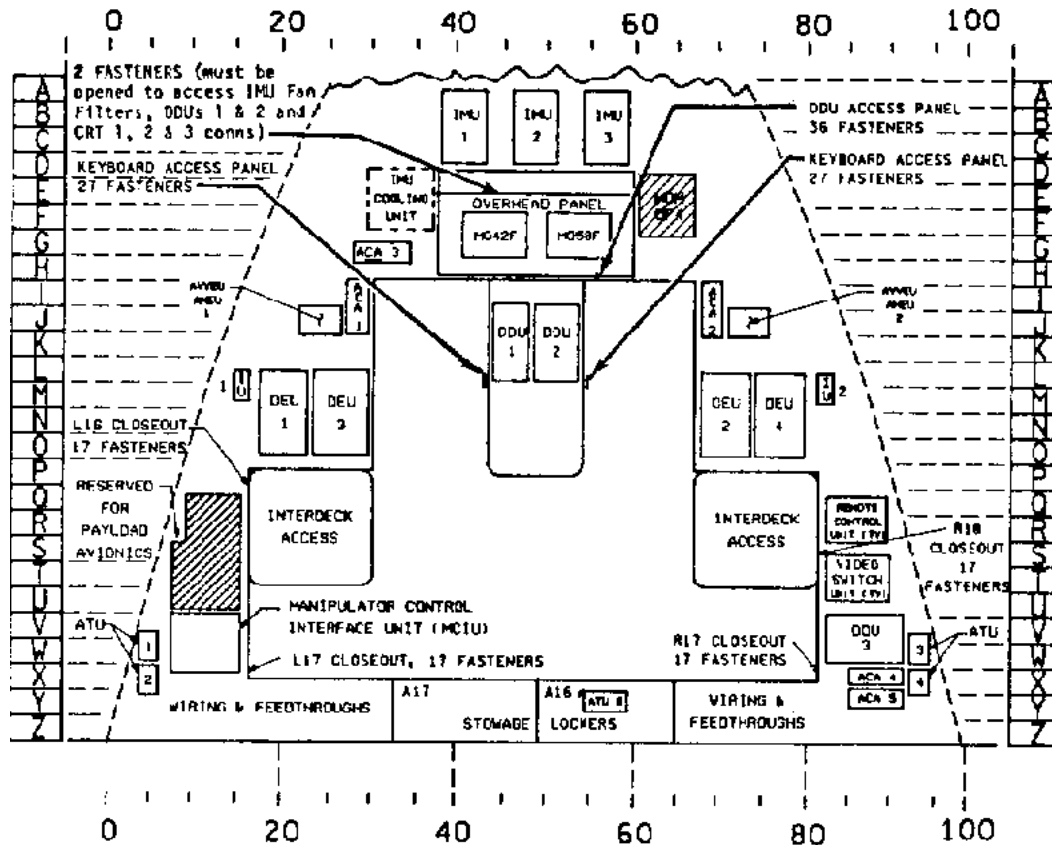


Figure 28-9. Component locations, flight deck

## 28.6 DESCRIPTION OF OPERATION

### 28.6.1 Crew Controls

The OI MDM port usage is determined by the powered PCMMU. The crew has total control of the panel C3 switch which selects PCMMU 1 or 2.

The only other control of the OI MDMs is the orbiter power switches shown in Section 28.3.

### 28.6.2 Telemetry

#### 28.6.2.1 MDM BITE

A detailed description of the BITE status register is given in Section 28.2.4,C of this brief.

The MDMs can be thought of as incorporating two different modes of BITE testing: real-time and commanded. The real-time tests occur during MDM input and output operations. Errors found in this mode are indicated in bits 1 through 10 of the BITE status register.

The MDM controlling unit (IOP, PCMMU, or GSE) has the capability to command BITE tests to be performed, the results of which are stored in bits 1 through 16 of the BITE status register.

The OI MDM BITE special computations M01I0800E through M07I0800E are derived from all 16 bits, but because the PCMMU does not use the BITE test command capability, bits 11 through 16 should always be zeros. A “1” in any bit position will drive the special comp, indicating a failure.

Four bits of the BSR are especially relevant to the INCO/INST console positions in determining the status of the OI MDMs and are displayed on a Digital Display Driver (DDD) format. For a detailed description of the BITE BITS see Section 28.2.4.C.

### 28.6.2.2 MDM Wrap

The 8-bit OI validation word from each MDM is received by the PCMMU at 10 samples/second. The wrap test special computation, performed by the Mission Operations Computer (MOC) on two consecutive samples/second, fails if the second sample is not the ones complement of the first.

## 28.7 SPECIAL COMPUTATIONS

**Table 28-6. BITE/wrap computations**

| MDM | BITE comp | Input parameter | Wrap comp | Input parameter |
|-----|-----------|-----------------|-----------|-----------------|
| OF1 | M01I0800E | V72M8020P       | M01I0500E | V75X4020D       |
| OF2 | M02I0800E | V72M8040P       | M02I1500E | V75X4021D       |
| OF3 | M03I0800E | V72M8060P       | M03I1500E | V75X4022D       |
| OF4 | M04I0800E | V72M8080P       | M04I1500E | V75X4023D       |
| OA1 | M05I0800E | V72M8100P       | M05I1500E | V75X4024D       |
| OA2 | M06I0800E | V72M8120P       | M06I1500E | V75X4025D       |
| OA3 | M07I0800E | V72M8140P       | M07I1500E | V75X4026D       |

- A logic 1 in any of the BSR bits 1 through 16 drives the BITE computation for the appropriate MDM. A 1 indicates FAIL.
- The 8-bit OI validation word from each MDM is received at 10 samples/second. The wrap computation is driven when the two consecutive samples are not complements of each other. For example, 10101010 and 01010101 are complements and would not drive the comp, but 10101010 and 01010111 will drive the comp and indicates a failure.

## 28.8 EMDM ENHANCEMENTS

The newest addition to the capabilities of the MDM is the Enhanced MDM (EMDM). The EMDM has several new features that are not available in the original MDMs.

These changes do not affect the way the MDMs are operated but do affect the insight that the Instrumentation office has into failure modes. The following subsections explain the main enhancements for the EMDM.

### 28.8.1 Gate Array Logic

The original MDMs used a set of digital and analog logic circuits to perform their tasks. The EMDM was redesigned to use a newer technology called gate array logic. Gate array logic is used to “enhance long-term productivity and reduce the parts count.” This newer technique requires that several subsystems in the MDM be replaced or modified. One of the drawbacks of the EMDM gate array logic is that the SCU can have a logic lockup at powerup. This lockup has happened several times in premission checkout procedures at KSC. The solution to the problem is to remove power from the MDM completely, then reapply power. Every EMDM that has shown an SCU lockup has started working after the power cycle.

### 28.8.2 MIA/SCU Interface

The internal wraparound test verifies that the interface between the MIA and the SCU is error free. The SCU sets the transmit and receive enable lines to true. The MIA sends the same data it is receiving from the SCU back to the SCU. The SCU verifies that the data it received is the same as it sent to the MIA plus an internally generated parity bit. If a wraparound error is detected, the SCU halts execution of the current microprogram and sets bit 2 in the BSR (incoming data error).

### 28.8.3 IOM Power Supplies

The IOMs in an EMDM do not share a power supply the same way that the original IOMs did. The original IOMs received power from the core power supply through a shared power supply for eight IOM boards. Each IOM has its own power supply that is fed by the EMDM core power supply. See Figure 28-10 for a graphical representation of the differences between the MDM and the EMDM.

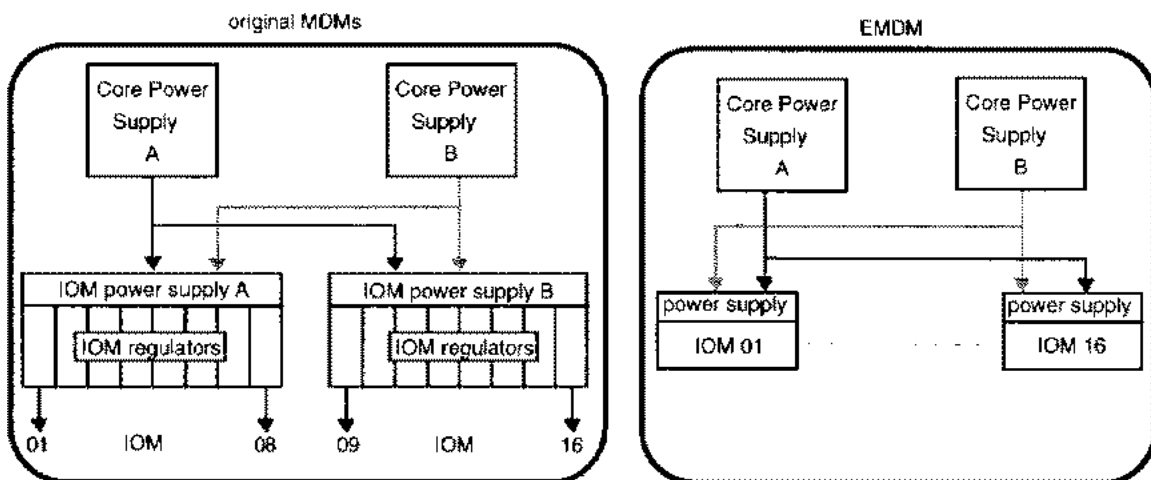


Figure 28-10. Power distribution: MDM versus EMDM

#### 28.8.4 IOM Interface

The EMDMs were updated to replace the shared SCU-to-IOM data bus with a discrete line between the SCU and each IOM. In the original MDM a shared IOM data bus was used, and the SCU requested data by sending an IOM address out on the data bus, allowing for some error. The original MDMs could request data from the wrong IOM by simply dropping a bit in the address for the correct IOM. The correction of the problem was to create a triply redundant address checker and add discrete lines from the SCU to the IOM. If the IOM address is determined to be wrong, the V-bit is set. This action stops all processing of the response word.

#### 28.9 REFERENCES

- A. Data Processing Subsystem Principles of Operation SD 74-SH-0203C, Rockwell International, April 1978
- B. MDM Program Interpretation Handbook Flight Control Division, Guidance and Propulsion System Branch, Rev A, June 30, 1980
- C. Multiplexer/Demultiplexer Specification (MC615-0004), Rockwell International; February 14, 1984
- D. Adapter Interface Serial Multiplexer (MIA) Specification (MC615-0010), Rockwell International; June 18, 1980

THIS PAGE INTENTIONALLY BLANK

## SECTION 29 - PULSE-CODE MODULATION MASTER UNIT

### CONTENTS

| Section |  | Page  |
|---------|--|-------|
| 29.1    | GENERAL DESCRIPTION.....                   | 29-1  |
| 29.1.1  | Interfaces .....                           | 29-1  |
| 29.1.2  | Block Diagram.....                         | 29-1  |
| 29.2    | PCMMU DESCRIPTION .....                    | 29-3  |
| 29.2.1  | Electrical Description.....                | 29-3  |
| 29.2.2  | Timing Signals.....                        | 29-7  |
| 29.2.3  | Mechanical Description .....               | 29-7  |
| 29.2.4  | Software .....                             | 29-9  |
| 29.2.5  | Software Constructions .....               | 29-16 |
| 29.2.6  | GPC/PCMMU Software Interfaces .....        | 29-21 |
| 29.3    | INSTALLATION.....                          | 29-27 |
| 29.3.1  | Location.....                              | 29-27 |
| 29.3.2  | Cooling.....                               | 29-27 |
| 29.4    | DESCRIPTION OF OPERATION.....              | 29-28 |
| 29.4.1  | Crew Controls .....                        | 29-28 |
| 29.4.2  | Ground Commands.....                       | 29-28 |
| 29.4.3  | Telemetry .....                            | 29-28 |
| 29.4.4  | Operating Instructions SM Operations ..... | 29-47 |
| 29.4.5  | Operating Instructions GNC G9 .....        | 29-49 |
| 29.4.6  | TFL Flight Software Idiosyncracies .....   | 29-49 |
| 29.5    | REFERENCES.....                            | 29-51 |

## TABLES

| Table |                              | Page  |
|-------|------------------------------|-------|
| 29-1  | Operation codes .....        | 29-23 |
| 29-2  | Starting address field ..... | 29-24 |

## FIGURES

### Figure

|       |   |       |
|-------|---|-------|
| 29-1  | PCMMU operational interface diagram .....                 | 29-2  |
| 29-2  | General PCMMU block diagram .....                         | 29-4  |
| 29-3  | PCMMU block diagram .....                                 | 29-5  |
| 29-4  | PCMMU power supply block diagram .....                    | 29-6  |
| 29-5  | PCMMU central timing block diagram .....                  | 29-8  |
| 29-6  | MDM command word format .....                             | 29-10 |
| 29-7  | MDM response data word format .....                       | 29-11 |
| 29-8  | PDI command word format .....                             | 29-12 |
| 29-9  | PDI response data word format .....                       | 29-13 |
| 29-10 | Spacelab command word format .....                        | 29-14 |
| 29-11 | Spacelab response data word format .....                  | 29-15 |
| 29-12 | Sample rate counters .....                                | 29-18 |
| 29-13 | 128-kbps formatter PROM/RAM format .....                  | 29-19 |
| 29-14 | 128/64-kbps format output .....                           | 29-20 |
| 29-15 | Command word format from computer to PCM unit (CDW) ..... | 29-25 |
| 29-16 | Command word format from computer to PCM unit (CW) .....  | 29-25 |
| 29-17 | PCMMU response data word format .....                     | 29-26 |
| 29-18 | Panel C3 .....  | 29-29 |
| 29-19 | SPEC 62 .....   | 29-30 |

## SECTION 29 PULSE CODE MODULATION MASTER UNIT

### 29.1 GENERAL DESCRIPTION

The Pulse-Code Modulation Master Unit (PCMMU) gathers parametric and digital data from all shuttle subsystems. The data are interleaved according to format instructions within the PCMMU and output to recorders, ground support equipment, and the orbiter communications subsystem for downlink.

#### 29.1.1 Interfaces

Data sources with which the PCMMU interfaces (Figure 29-1) are:

- Primary Avionics Software System (PASS) Guidance, Navigation And Control (GN&C) computers
- PASS Systems Management (SM) computer
- BACKUP FLIGHT SYSTEM (BFS) computer
- Operational Instrumentation (OI)
- Payload Data Interleaver (PDI)
- Spacelab

#### 29.1.2 Block Diagram

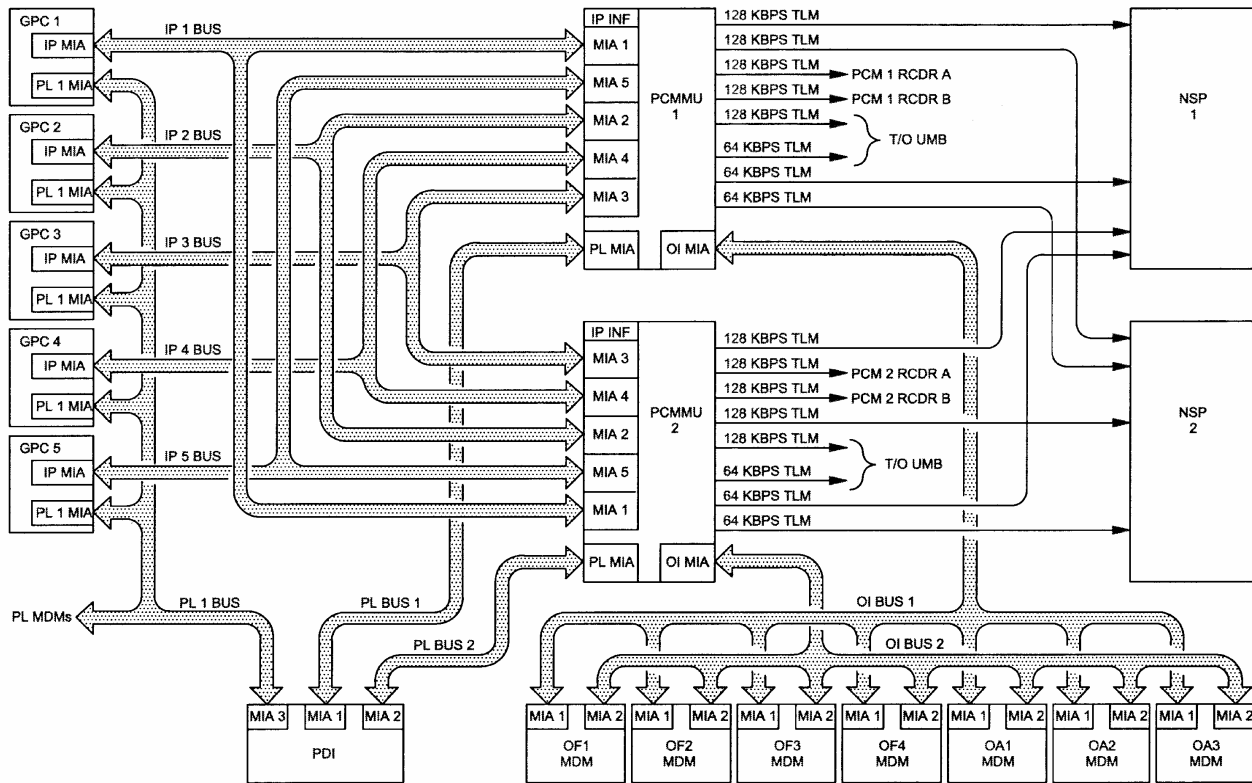
The five shuttle General Purpose Computers (GPCs) gather information according to their internal programs, independent of PCMMU operations, and format selected parameters for output to the PCMMU. In addition to shuttle systems data, the formatted output to the PCMMU includes software and hardware status (Figure 29-1) of the GPCs.

The remaining shuttle subsystems (exclusive of payloads not serviced directly by the GPCs) constitute the OI parameters. The OI parameters include analogs, discretely, and digital; e.g., time words from the Master Timing Unit (MTU) which must be signal-conditioned, digitized, or buffered before presentation to the PCMMU. Signal processing of OI data are the responsibility of the signal conditioners and the Multiplexer/ Demultiplexer (MDM) Line Replaceable Units (LRUs). The PCMMU then interrogates the MDMs to acquire the OI data.

Payload support systems as well as attached and detached payloads submit their data to an interface unit called the PDI. The PDI buffers the signal-processed and digitized data into its internal memory locations, which allows the PCMMU to address and acquire the data in the same manner as it acquires data from an MDM.

Spacelab has two computers for gathering data: the Experiment Computer (EXC) and Subsystem Computer (SSC). The PCMMU acquires Spacelab data through input/output units (SSIO and EXIO) by giving a start address and number of words.





**Figure 29-1. PCMMU operational interface diagram**

Spacelab and PDI share the payload Multiplexer Interface Adapter (MIA). The addressing for Spacelab and PDI is different. The PDI command/response word uses bits 4 to 6 with a bit pattern 001. The Spacelab command/response word uses bits 4 to 8 with a bit pattern 11000 for EXC and 10000 for SSC.

The technique for collecting data from the various sources uses a Time-Division Multiplexed (TDM'd) bus. This allows several subscribers to communicate with each other using only one bus. Each subscriber is assigned a digital address and accepts and processes data on the bus only when it recognizes its own coded address preceding the data.

Each subscriber unit hooked to a data bus contains an MIA. The MIA is responsible to its host for providing a common interface between its host and the data bus. In doing so, the MIA performs the following:

- A. Listens and recognizes host address
- B. Provides impedance match to bus

- C. Checks for proper waveform of incoming data
- D. Checks and counts number of data words host is expecting
- E. Checks validity of data by parity count
- F. Converts data bus coding (Bi $\phi$ L) into host coding (non-return-to-zero level (NRZ-L))
- G. Accepts NRZ data from host to be transmitted on bus
- H. Converts NRZ code to Bi $\phi$ L
- I. Assigns parity bit and transmits data to bus

The PCMMU formats acquired data into two separate bit streams. One outputs data at a rate of 128 kbps; the other outputs data at 64 kbps. Each format is output simultaneously to the Network Signal Processor (NSP), which selects one format for downlink. Both outputs have a Ground Support Equipment (GSE) interface through the T-0 umbilical. (See handbook drawing 17.2.)

## 29.2 PCMMU DESCRIPTION

Figure 29-2 and Figure 29-3 and handbook drawing 17.2 depict the major internal design of the PCMMU. The power supply, timing interfaces, MDM/PDI interface, data storage, GPC interface, and Telemetry (TLM) format functions are detailed in the following discussions.

### 29.2.1 Electrical Description

See Figure 29-4 and handbook drawing 17.2. The internal PCMMU conversion unit uses direct current from the orbiter +28 V dc distribution system.

There are two OI PCMMUs in each orbiter. Only one PCMMU is powered on at a time.

Each PCMMU is coupled to two of the three main dc buses; PCMMU 1 uses main A and main C, and PCMMU 2 uses main A and main B. The PCMMU works satisfactorily on input voltage of 22 to 36 V dc and is protected from voltage above 36 V dc by switching itself off. It will remain off until the overvoltage condition disappears.

The average power used by the PCMMU is 68 watts.

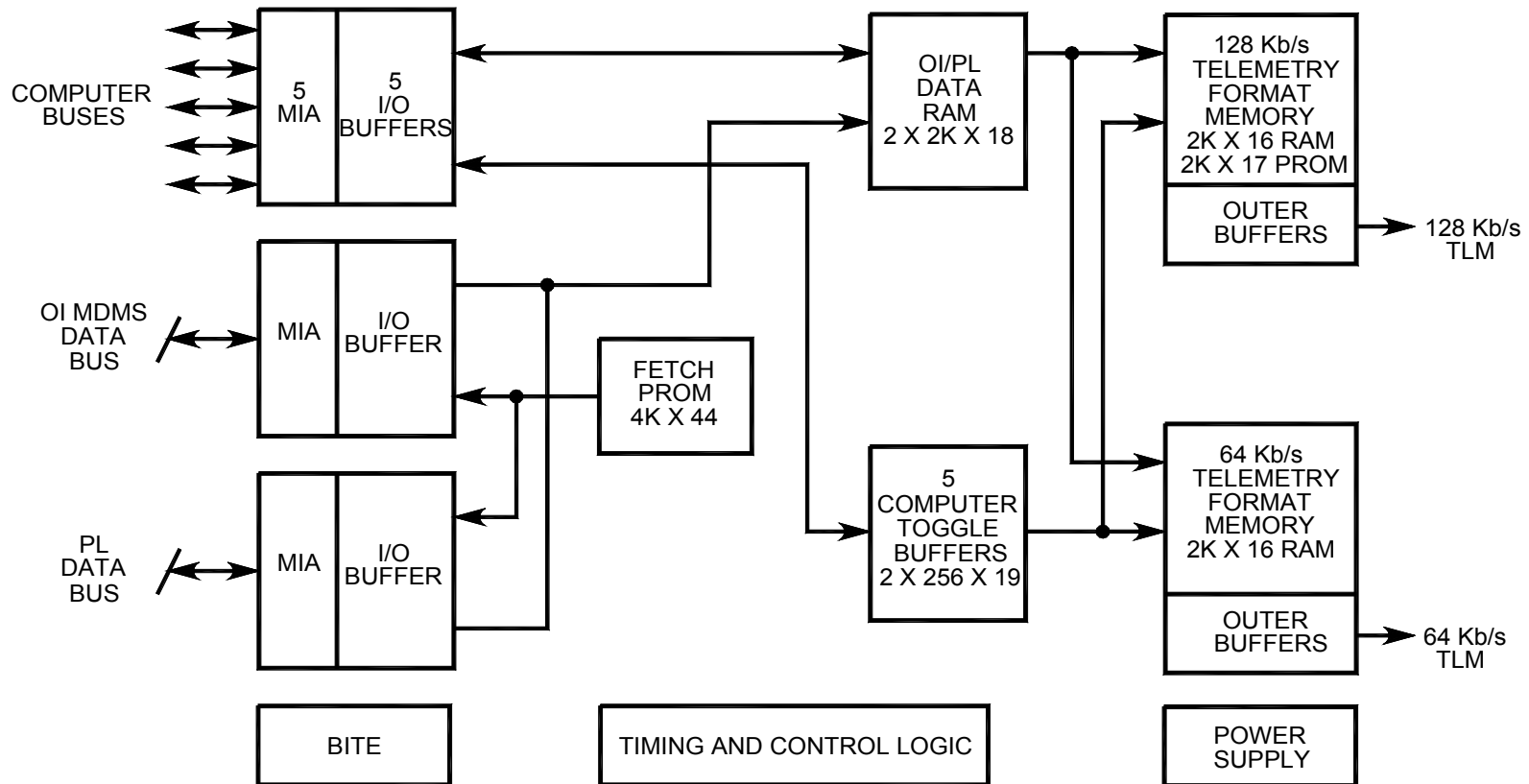


Figure 29-2. General PCMMU block diagram

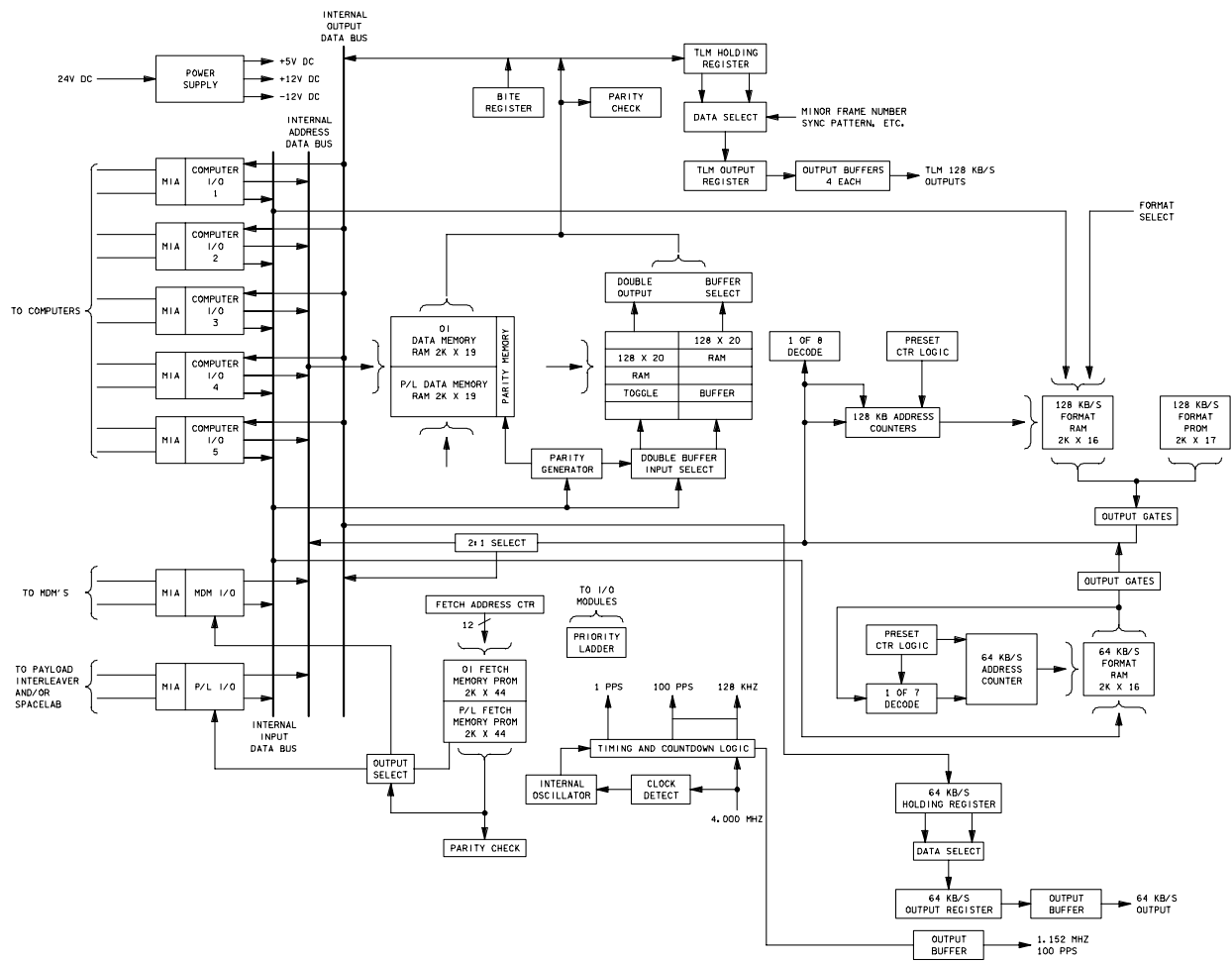
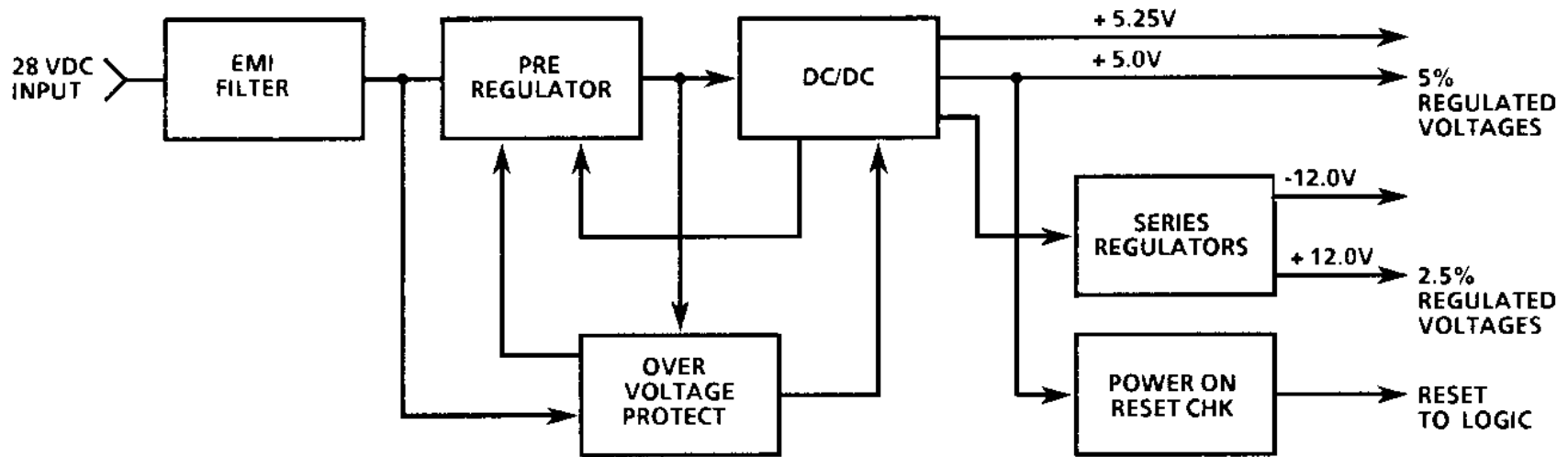


Figure 29-3. PCMMU block diagram



18611-007

Figure 29-4. PCMMU power supply block diagram

### 29.2.2 Timing Signals

The PCMMU receives a 4.608-MHz signal directly from the MTU (see Figure 29-5 and handbook drawing 17.2). This signal is counted down inside the PCMMU for logic operations. The PCMMU contains a circuit that monitors frequency and amplitude of the MTU input. Should the MTU input fail, an internal 4.608-MHz oscillator is brought on line to provide timing to the PCMMU. The PCMMU continues to function from its own oscillator until the MTU input reappears in good condition.

The PCMMU outputs 1.152-MHz and 100-Hz timing signals. The 1.152-MHz timing signal is output to the NSPs and the PDI. The 100-Hz timing signal is output only to the NSPs (see handbook drawing 17.2).

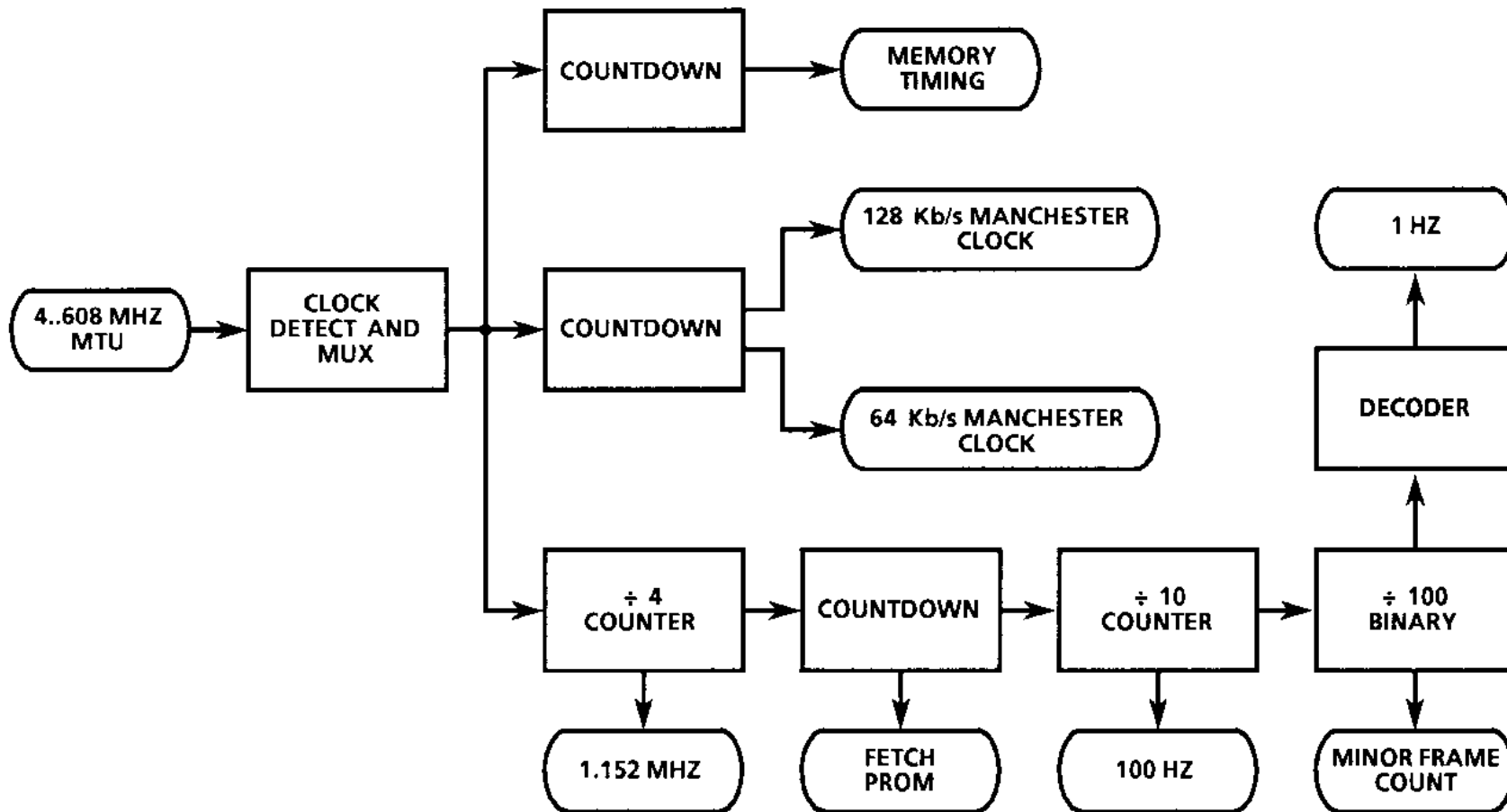
### 29.2.3 Mechanical Description

Manufacturer - Harris Corporation, Electronic Systems Division

|                             |                          |
|-----------------------------|--------------------------|
| Physical - Mounting surface | 8.2 W by 19.0 L          |
| - PCMMU                     | 6.6 W by 7.0 H by 19.0 L |
| - Weight                    | 30 pounds                |

Environmental - Unit shall meet operating performance requirements during and after exposure to:

|                       |  |
|-----------------------|--|
| Temperature (ambient) | 0° to 145° F (nonoperational -65° to 150° F)   |
| Pressure              | 8 to 18 psia (nonoperational 3.28 to 18 psia)  |
| Humidity              | 8 to 100 percent RH  |
| Salt Fog              | 1 percent salt solution by weight  |
| Ozone                 | 3 to 6 phm, up to 60 phm for 1 to 3 hours in any 24 hours  |
| Fungus                | Non-nutrient   |
| Vibration             | 10.23 Grms random (0.09 G <sup>2</sup> /Hz maximum P.S.D.) for 48 minutes per axis   |
| Acceleration          | +5 g all major axes  |
| Shock                 | Landing: various levels from 0.023 Gp/170 ms to 1.5 Gp/260 ms<br>Transient: equivalent to sine vibration at 0.25 Gp 5-35 Hz<br>Crash safety: must remain intact 40 g, 11 ms sawtooth |
| Sand and dust         | As encountered in desert and ocean beach areas   |
| Coldplate             | 130° F maximum mounting surface temperature (depending on heat flux)   |



CENTRAL TIMING

18611\*008

Figure 29-5. PCMMU central timing block diagram

#### 29.2.4 Software

The program for acquiring OI/Payload (PL) data are stored in a FETCH Programmable Read-Only Memory (PROM). The FETCH PROM is nonvolatile. Before STS-16, the FETCH PROM was reprogrammed for each flight. Starting with STS-16, a universal FETCH PROM was installed for standardization and cost savings.

There is physically only one FETCH PROM programmed with both OI and PL FETCH commands. It contains 4096 (command) words, each 44 bits long. The 4096 words are divided evenly between the OI and PL. The OI commands are interleaved with PL commands so that when they are clocked out of the PROM, each data bus is equally time-shared; i.e., giving one bus time to respond while the other is being commanded. The commands are all clocked out of the FETCH PROM in 1 second, then the cycle repeats. A power-on reset is provided by the power supply so that the FETCH command sequence always starts at a predetermined initial location.

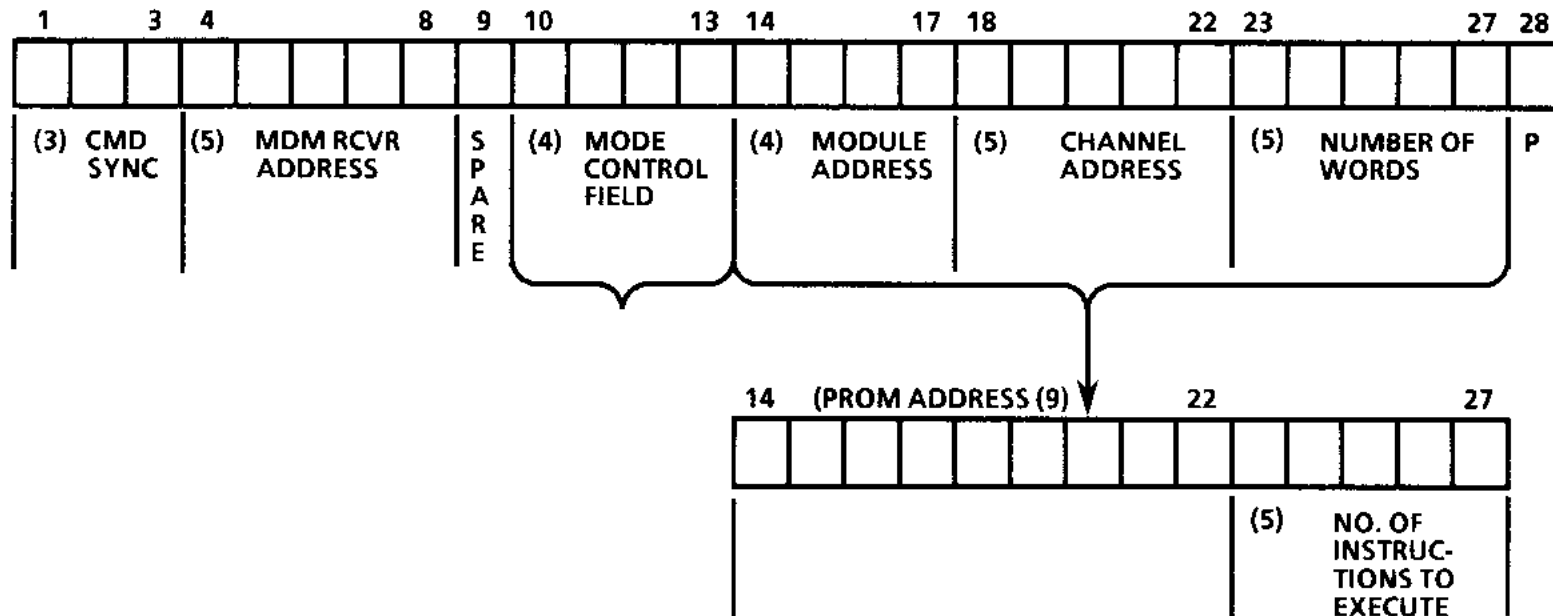
The PCMMU acquires OI data by interrogating MDMs connected to a common data bus. The PCMMU/MDM communication is called a demand/response technique. None of the MDMs on the OI data bus does anything until addressed and commanded to sample, process, and send data back by the PCMMU; i.e., the PCMMU demands data from an MDM and the MDM responds automatically by sending the requested data to the data bus addressed to the PCMMU. See Figure 29-6 and Figure 29-7 for a description of a command word from the PCMMU and the response word from an MDM. A single command word from the PCMMU can result in up to 32 response words from an MDM. Only one MDM may be addressed by the PCMMU in any one common word.

The parameter channelization codes and their required sequence of acquisition are stored in the FETCH PROM. Also, the location within the OI data Random Access Memory (RAM) where the parameter is to be stored is included in the FETCH PROM. Command words are strobed out of the FETCH PROM at a constant rate and the cycle repeats itself once each second. Data returning to the PCMMU are directed into a predetermined storage location in the OI data RAM. Any OI parameter may be commanded to the PCMMU at a rate of 1, 2, 5, 10, 20, 25, 50, or 100 times a second. Thus, the OI data RAM memory locations are updated at a rate determined by the sample rate for data programmed into the FETCH PROM.

Acquisition of data from the PL is the same as OI data collection, with one exception: there is a dedicated data bus between the PCMMU and the PL (see handbook drawing 17.2). The FETCH and storage functions are the same as OI. See Figure 29-8 and Figure 29-9 for a description of PDI command and response formats, and Figure 29-10 and Figure 29-11 for a description of Spacelab command and response formats.

PCMMU Data Ram is physically separated into **two** read/write memory cards, the OI Data Ram and PL Data Ram, each with the ability to store 2048 18-bit words. The FETCH PROM command steers the response words from the OI and PL data buses respectfully into their predetermined address locations within either OI Data Ram or PL Data Ram. \*\* The OI and PL Data Rams nomenclatures can be a misnomer. OI or PDI telemetry is physically read/write to specific OI or PL Data Ram addresses locations.

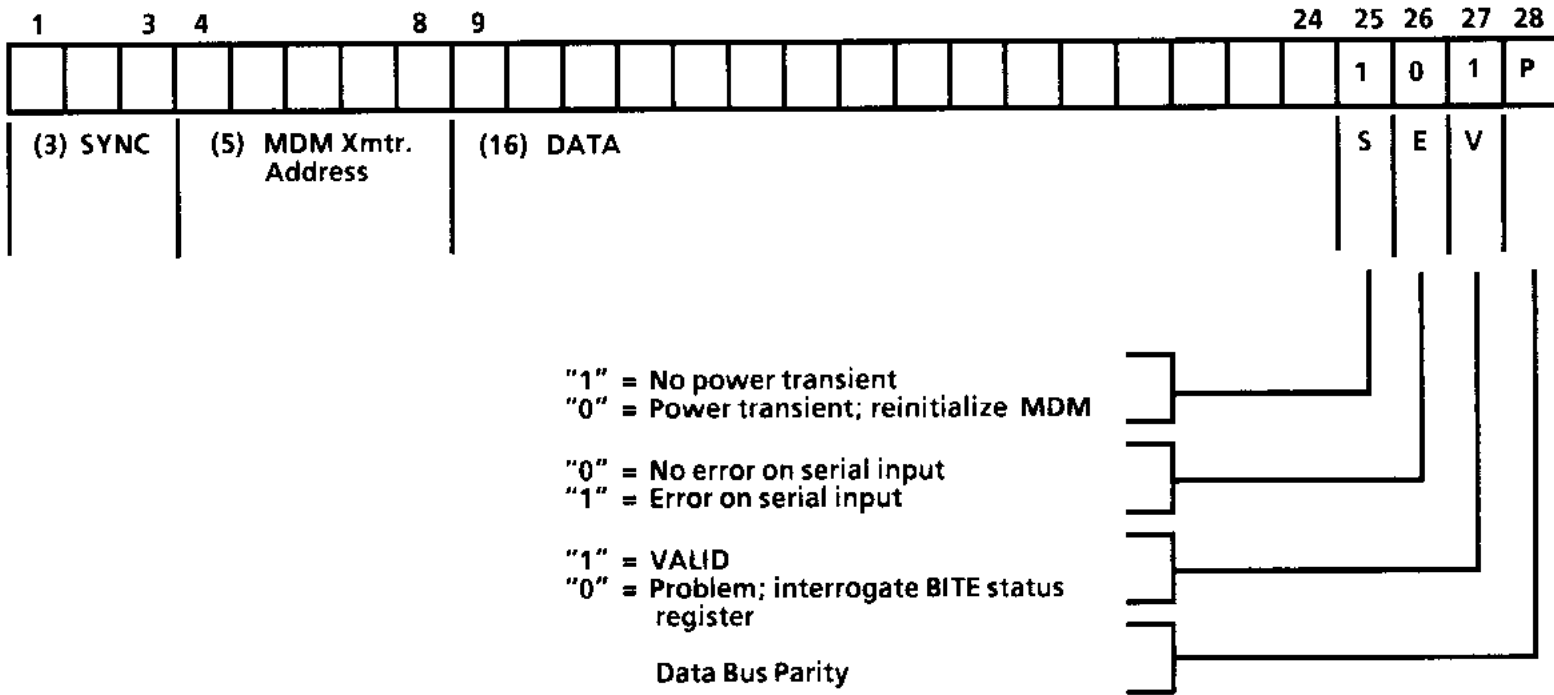




| BITS | 10 | 11 | 12 | 13 | OPERATION   |
|------|----|----|----|----|---|
|      | 0  | 0  | 0  | 0  | Spare   |
|      | 0  | 0  | 0  | 1  | Return the word at the PROM address                                   |
|      | 0  | 0  | 1  | 0  | Execute the word at the PROM address                                  |
|      | 0  | 0  | 1  | 1  | Spare   |
|      | 0  | 1  | 0  | 0  | Command BITE Test 1   |
|      | 0  | 1  | 0  | 1  | Command BITE Test 2   |
|      | 0  | 1  | 1  | 0  | Command BITE Test 3   |
|      | 0  | 1  | 1  | 1  | Command BITE Test 4   |
|      | 1  | 0  | 0  | 1  | Prepare MDM to transmit response data                                 |
|      | 1  | 0  | 1  | 0  | Send the BITE status and reset the BITE status register               |
|      | 1  | 1  | 0  | 0  | Return the received command   |
|      | 1  | 1  | 1  | 0  | Load BITE status register (re: on-line test of BITE status register ) |
|      | 1  | 1  | 1  | 1  | Spare   |

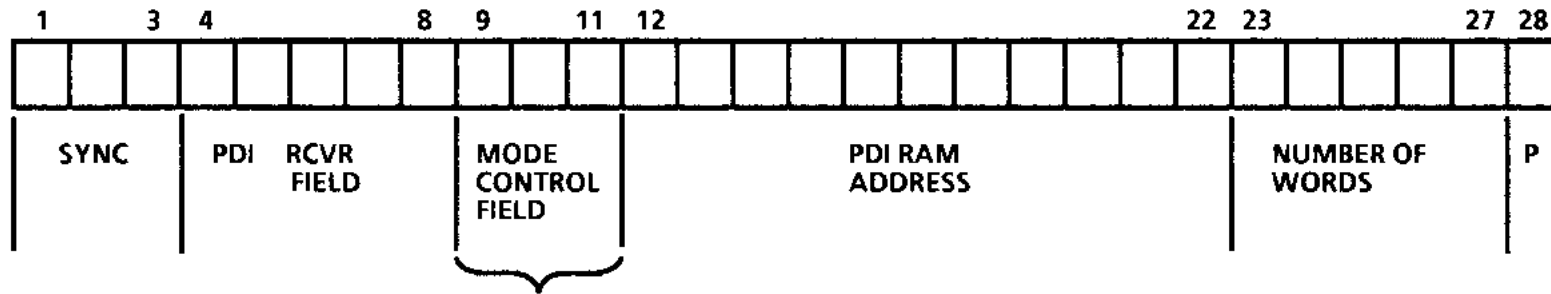
18611\*009

Figure 29-6. MDM command word format



18611\*010

Figure 29-7. MDM response data word format

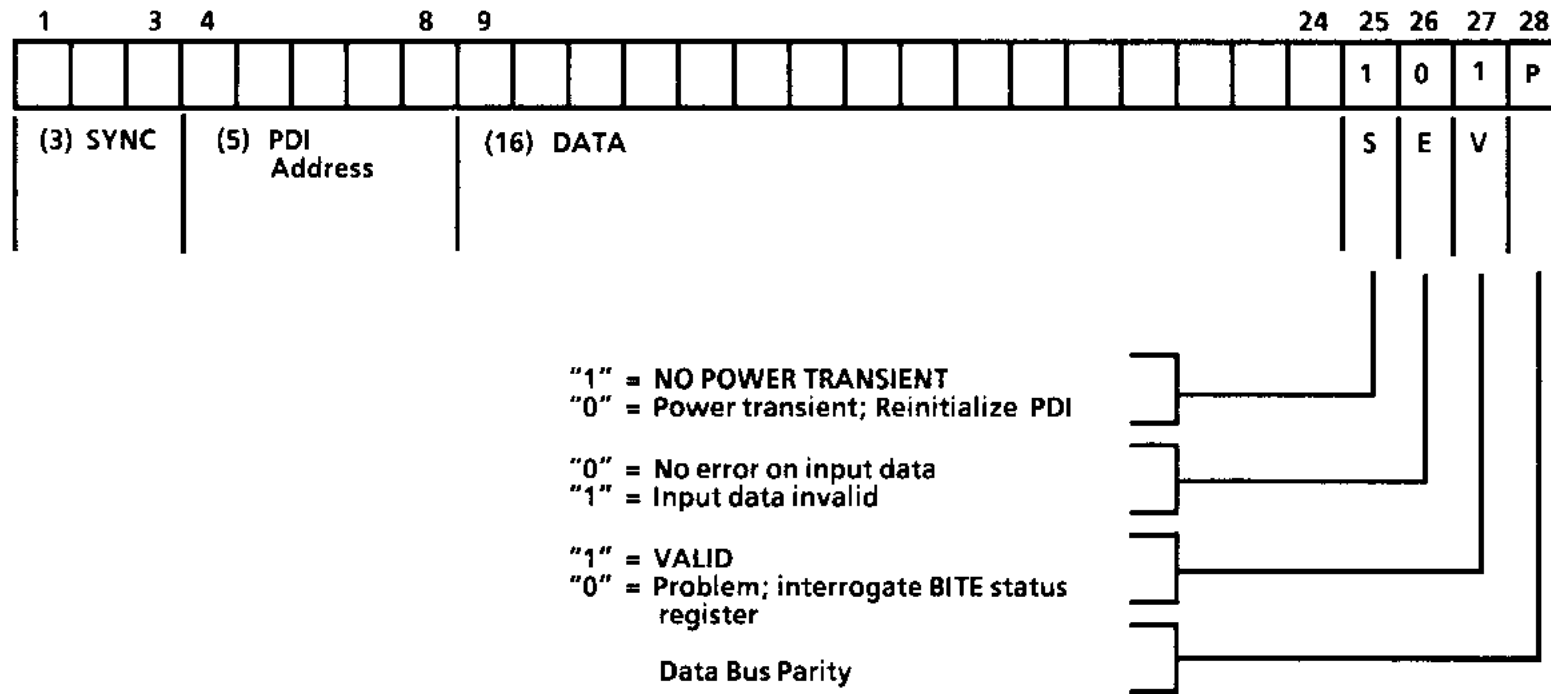


| BITS | 9 | 10 | 11 | OPERATION  |
|------|---|----|----|--|
|      | 1 | 0  | 0  | PREPARE PDI TO TRANSMIT RESPONSE DATA                    |
|      | 1 | 0  | 1  | RETURN RECEIVED WORD                                     |
|      | 0 | 1  | 0  | SEND BITE STATUS REGISTER AND RESET BITE STATUS REGISTER |

ALL OTHER COMBINATIONS  
ARE SPARE

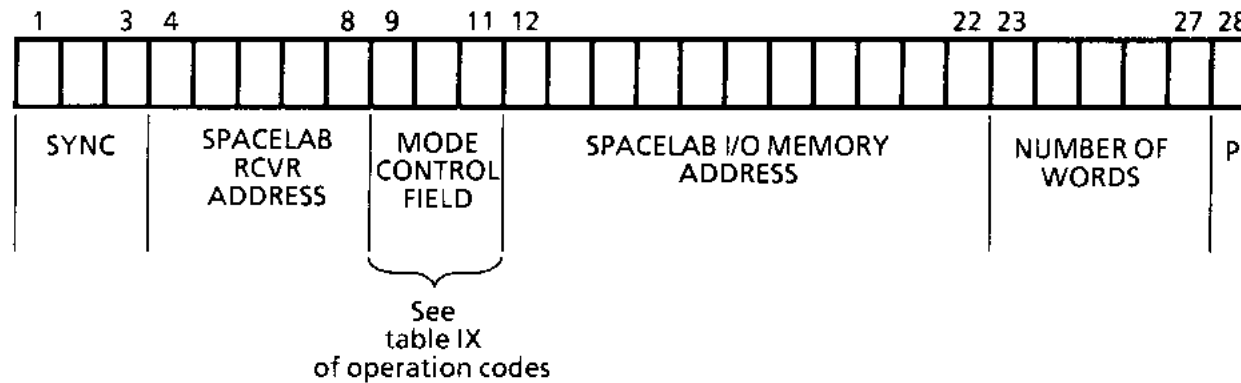
18611\*011

Figure 29-8. PDI command word format



18611\*012

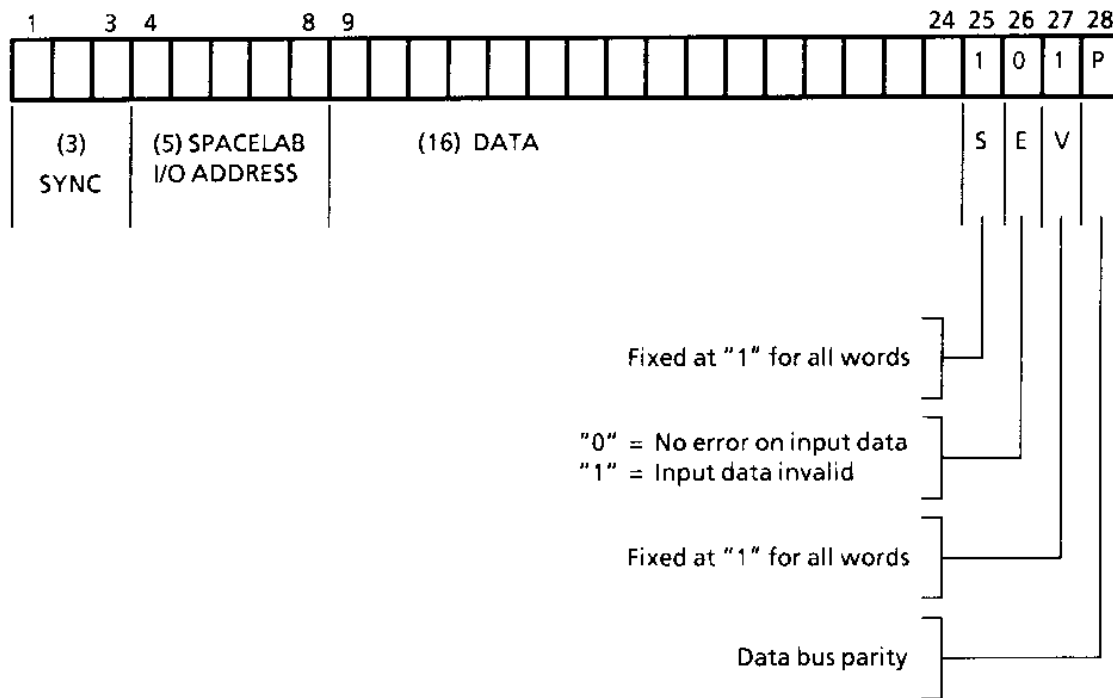
Figure 29-9. PDI response data word format



| <u>Spacelab address code</u> |          |          |          |          | <u>I/O</u> | <u>Operation codes</u> | <u>Spacelab operation codes</u> |           |           | <u>Description</u>  |
|------------------------------|----------|----------|----------|----------|------------|------------------------|---------------------------------|-----------|-----------|---|
| <u>Bits</u>                  | <u>4</u> | <u>5</u> | <u>6</u> | <u>7</u> | <u>8</u>   |                        | <u>9</u>                        | <u>10</u> | <u>11</u> |   |
|                              | 1        | 0        | 0        | 0        | 0          | Subsystem              | 0                               | 0         | 0         | Read data from the I/O memory starting with the requested address as defined by bits 12 through 22 and transmit to the requesting device. |
|                              | 1        | 1        | 0        | 0        | 0          | Experiment             |                                 |           |           |   |
|                              |          |          |          |          |            |                        | 1                               | 0         | 1         |   |
|                              |          |          |          |          |            |                        | 1                               | 0         | 0         | Transmit the contents of the BSR to the requesting device.  |

18611\*014

**Figure 29-10. Spacelab command word format**



18611\*015

**Figure 29-11. Spacelab response data word format**

The GPC obtains OI or PL data from the PCMMU by addressing the PCMMU with a command word that contains the OI/PL data RAM storage location(s) of the desired parameters. The PCMMU decodes the GPC command word and honors the request by transmitting the data from the RAM back over the same GPC/PCMMU data bus from which the request came; i.e., the PCMMU responds only to the GPC which commanded it. Each GPC command word may request from 1 to 32 data words (each 16 bits) from the PCMMU. However, the desired response words must be in numerically adjacent storage locations within the PCMMU data RAM because the GPC command word contains a starting address within the PCMMU data RAM, plus the number of (sequential) addresses to be sent back, up to 32 maximum.

In addition to obtaining OI and PL data from the PCMMU, the GPCs may read the contents of the TLM FORMATTER memories, except the 128-kbps PROM. The GPC command word contains unique codes to inform the PCMMU which one of the memories is to be read: OI/PL, 128-kbps RAM, or 64-kbps RAM. Also, the GPC can read the Built-In-Test Equipment (BITE) status register in the PCMMU.

The PCMMU communicates with each of the five GPCs via a dedicated bus between each GPC and the PCMMU. Although the content of data may vary at different times during the mission or from one GPC interface to another, the method of data transfer to and from each GPC is the same. The following discussion will focus on only one GPC/PCMMU interface, but the same is true for all of them.

By changing the bit structure in the operations code of the command, the GPC may inform the PCMMU to expect subsequent words (up to 32) to contain data to be stored for downlink, or to change or update instructions in the 128-kbps format memory RAM or the 64-kbps format memory RAM. Note that the PCMMU does not request data transfers from the GPCs, rather the GPCs send the PCMMU a Command Word (CW) followed by Command Data Words (CDWs) at the discretion of the GPC software. Because of this, special consideration must be given to GPC data which will be downlinked; i.e., the PCMMU must interleave the GPC data into a format containing OI and PDI data. To achieve a semblance of synchronized data formatting in the PCMMU, the GPC data are stored in alternate halves of a toggle buffer and the PCMMU commands the data from the half not being written into by the GPC. Thus, the PCMMU telemetry format function may acquire GPC data at an appropriate time in the interleaving cycle to build a coherent format for recording and/or downlink. See Section 29.2.6 for a description of the GPC/PCMMU data transfer specifics.

The TLM subsystem within the PCMMU is responsible for selecting parameters from the OI RAM, PL RAM, and computer toggle buffer and formatting the data to be sent to the NSP. There are two data streams output: 128 kbps and 64 kbps. Refer to handbook drawing 17.2. The 128-kbps TLM output can operate using format instructions contained in either the 128-kbps format RAM or the 128-kbps format PROM. The PROM is loaded with a desired format before a mission and remains fixed, whereas the RAM can be formatted in flight by the SM computer from the MMU. The SM computer reformats both 128 kbps and 64 kbps. The BFS computer only formats the 64-kbps during ascent and entry after switching PCMMUs. The 64-kbps format comes from the BFS software.

The required number of 128-kbps and 64-kbps output formats is determined premission and put onto the orbiter computer mass memory. During appropriate mission phases, the PCMMU format RAMs are changed to a different format by GPC action. The GPC is instructed either by keyboard entry or Radio Frequency (RF) ground command to access a given format on mass memory and transfer it into the 128-kbps or 64-kbps format RAM. The new format simply writes over the old one. In the case of the 64-kbps format RAM, it may be changed any time; however, to change the 128-kbps RAM, the PROM (or FIXED) format must be selected and remain there while the RAM is being updated due to hardware constraints.

### **29.2.5 Software Constructions**

As mentioned earlier, the PCMMU can be programmed to satisfy various mission requirements that are dictated by payload complement, test and checkout, orbital operations, and communication link constraints. The logic mechanization which permits this flexibility is reviewed in the following discussions.

The format memory organization is functionally divided into eight sample rate groups, a sample rate words partition, and an initial address word partition. The sample rate groups represent the data RAM address locations (OI/PL, GPC buffers) of the TLM data for the various sample rates. For example, the one sample per second (s/s) group

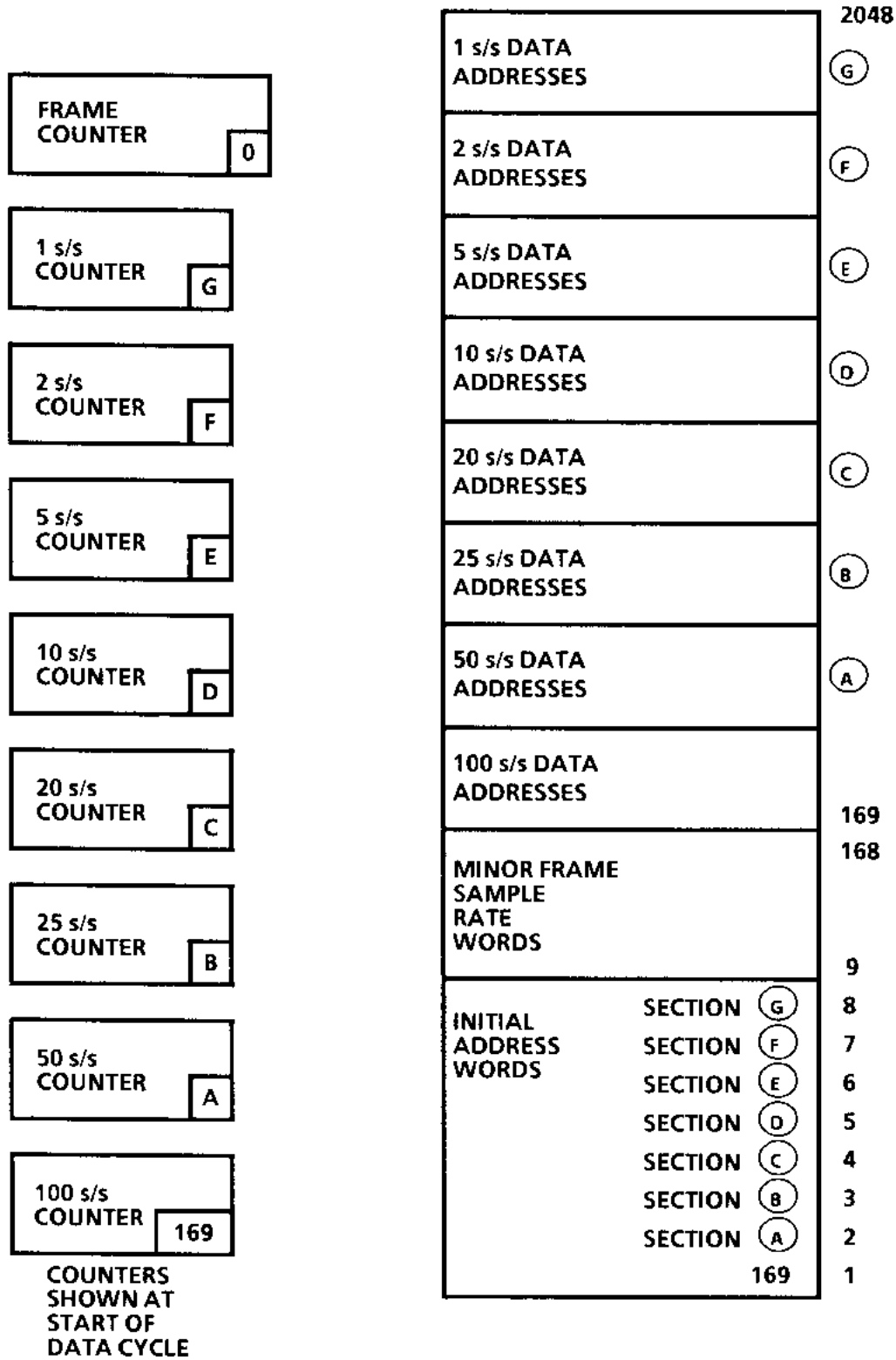
contains the data memory locations of all one s/s data to be output by this format. The number of entries in each group can vary from format to format, hence the starting location within the format memory to initial address words partition (eight words in length) contains the starting address within the TLM format memory of the eight sample rate groups. The sample rate words partition (words 9 to 168) contains the sample rate of the data to be output during each of the 160 minor frame time slots.

At the beginning of each major frame, which is divided into 100 minor frames of 160 words each, a 1-Hz clock will trigger the resetting of each of the sample rate counters (see Figure 29-12). Each of these counters will be loaded with the starting address of its assigned sample rate group for the TLM output format. The reading of these addresses from the format memory and loading into the appropriate sample rate counters is executed by the initial address words logic. After the eight counters have been set to the appropriate starting address, the beginning of the first minor frame output is ready to start. The minor frame begins by enabling one of the eight sample rate counters to request a read of the first word in its associated sample rate group and update its address counter by one. When the word is read out, its Operational Sequence (OPS) code (Figure 29-13) will be interrogated and the data address portion of the word will be steered to the desired data memory location in order to read the requested TLM data word from the data memory. The data word is then loaded into the TLM holding register and finally output per the OPS code request after being converted to the BiφL format. At this time, the second time slot sample rate word will be read and a similar sequence of events will result in outputting of the second TLM data word. Then the third word will be read and so on, until the end of the minor frame occurs and all 160 words have been read.

At the end of every minor frame, the 100-s/s counters will be reset to the initial addresses of the 100-s/s group within the TLM format. Similarly, the 50-s/s counters are reset every alternate minor frame, the 25-s/s counters are reset every fourth minor frame and so forth, until the end of the major frame where the 1 s/s counters are reset. The cycle then repeats itself. Both the 128-kbps TLM RAM and PROM function identically as described above. Transmission rate is 16,000 (8-bit) words per second.

The 64-kbps TLM output operates from a single 2K word RAM in a mode similar to that of the 128-kbps described above. Structurally, the format memory organization is the same as that of the 128-kbps TLM, except that the sample rate words partition contains only 80 entries instead of 160. This is because the 64-kbps major frame is divided into 100 minor frames each consisting of 80 words with a transmission rate of 8000 (8-bit) words per second. A comparison of the two formats is given in Figure 29-14.





18611\*003

Figure 29-12. Sample rate counters

| WORDS   | 1                                     | 11 12  | 16 17         | SYS | CODE |
|---------|---------------------------------------|--------|---------------|-----|------|
| 1 - 8   | STARTING ADDRESS FOR THE SAMPLE RATES | SPARES | VALID-ITY BIT | 1   | 000  |
|         |                                       |        |               | 2   | 001  |
|         |                                       |        |               | 5   | 010  |
|         |                                       |        |               | 10  | 011  |
|         |                                       |        |               | 20  | 100  |
|         |                                       |        |               | 25  | 101  |
| 9 - 168 |                                       | SPARES | VALID-ITY BIT | 50  | 110  |
|         |                                       |        |               | 100 | 111  |
|         |                                       |        |               |     |      |

Bits 1-3, above, assign the downlist sample rates for each of the time slots for the 128-kbps format according to the code at the right.

|          | 1  | 13 14         | 15                 | 16          | 17            |
|----------|--|---------------|--------------------|-------------|---------------|
| 169-2048 | BITE REG., OI, PDI OR COMPUTER RAM ADDRESS | RIGHT OR LEFT | FORMAT OR RAM DATA | PAR-ITY BIT | VALID-ITY BIT |

When address in bits 1-13 is an OI RAM address, then bit 14 is defined as:

- 1 = Acquire bits 1 and 10-16 of the stored OI MDM response word
- 0 = Acquire bits 2-9 of the stored MDM response word

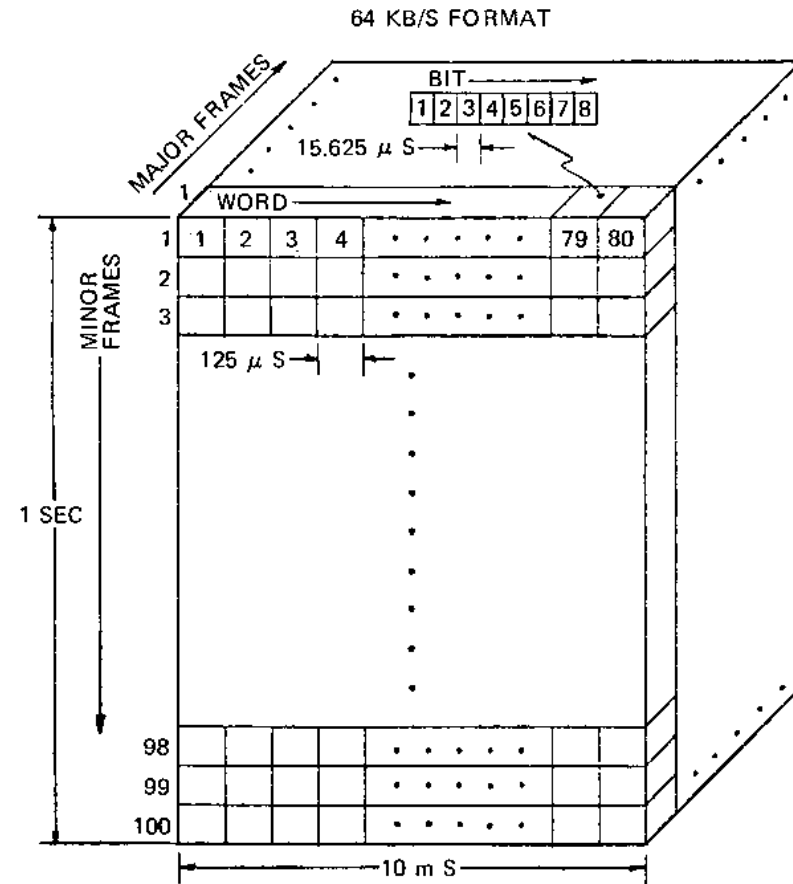
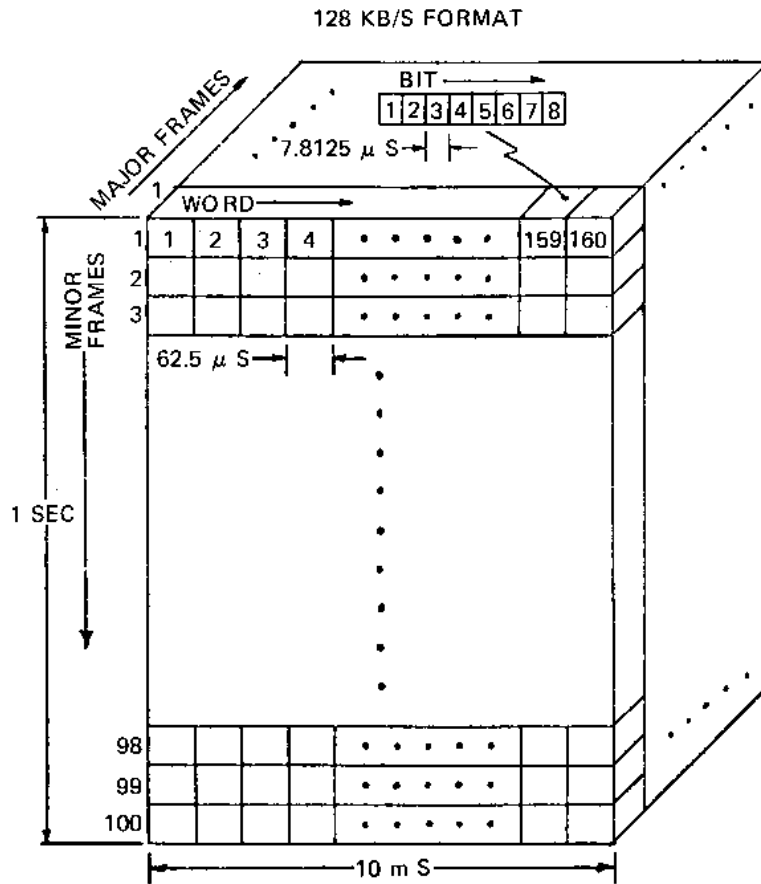
When address in bits 1-13 is a computer data RAM, BITE Req. or PDI RAM, then bit 14 is defined as:

- 1 = Acquire bits 1-8 of the required data
- 0 = Acquire bits 9-16 of the required data

When bit 15 is a 1, then bit 14 is defined as:

- 1 = Acquire bits 1-8 of this TLM format memory word as defined by bit 14
- 0 = Acquire data from the data RAM in the normal fashion

**Figure 29-13. 128-kbps formatter PROM/RAM format**



FILL = ALL "1's"

| DIVISION    | RATE    | PERIOD         |
|-------------|---------|----------------|
| BIT         | 128 kHz | 7.8125 $\mu$ S |
| WORD        | 16 kHz  | 62.5 $\mu$ S   |
| MINOR FRAME | 100 Hz  | 10 mS          |
| MAJOR FRAME | 1 Hz    | 1 S            |

| DIVISION    | RATE   | PERIOD         |
|-------------|--------|----------------|
| BIT         | 64 kHz | 15.625 $\mu$ S |
| WORD        | 8 kHz  | 125 $\mu$ S    |
| MINOR FRAME | 100 Hz | 10 mS          |
| MAJOR FRAME | 1 Hz   | 1 S            |

Figure 29-14. 128/64-kbps format output

As the PCMMU internal routines progress through their cycles, various subsystems of the PCMMU are checked for proper operation. These tests consist of such things as monitoring the presence of input power, MTU signal presence, parity bit comparisons, and comparison of a word which has been looped around (between the Multiple Unit (MU) and MDMs) with its stored value. If a subsystem fails its test, a bit is set (or changes state) in a register. This register contains 16 bits, some of which may represent multiple inputs logically summed to one bit, and it may be read out by the TLM formatters and the GPCs. This BITE register is reset according to the following design: when both the 128-kbps TLM and a GPC has read it, or every other major frame, whichever comes first. The bit definition is given in Section 29.4.3.1.

The PCMMU contains internal logic which continuously sums selected bits in the BITE register and forms a discrete (hardline) output which can be used to drive a light or other display on the orbiter Display and Control (D&C) panels.

## **29.2.6 GPC/PCMMU Software Interfaces**

### **29.2.6.1 GPC**

Up to five GPCs outputting data to five PCMMU toggle buffers.

A GPC outputs data to PCMMU in data blocks - up to 25 frames per second.

Each data block contains up to 128 CDWs (16 bits of data to be downlinked per CDW).

Any GPC can address data to any toggle buffer.

Any GPC can request data from the side of a toggle buffer being read by the output formatter. (A GPC cannot request data from the side being loaded by a GPC.)

Any GPC can request data from the OI/PL data RAM. (When a GPC requests data, it does so by requesting a readout of a particular memory location.)

### **29.2.6.2 Toggle Buffers**

There are five toggle buffers.

Each half of each buffer can contain up to 128 16-bit GPC words.

At any time, one side of each toggle buffer is connected to the GPCs and the other side to the PCMMU output formatter.

Each toggle buffer independently switches its GPC/PCMMU output formatter connection when one of the following sets of conditions are met for that toggle buffer:

- A. An End of Message (EOM) has been received indicating that the side of the toggle buffer being updated by the GPC has a complete data set.
- B. All of the data set in the side of the toggle buffer outputting to the output formatter has been read by the 128-kbps output formatter.

or when both the following have occurred:

- A. The PCMMU has just been turned on.
- B. The first EOM for that toggle buffer has been received from the GPCs.

### 29.2.6.3 GPC/PCMMU Data Transactions

The message for transfer of data from a computer to the PCM unit shall consist of one CW followed by 1 to 32 CDWs from the computer. The message formats for the CW and the CDW are shown in Figure 29-15 and Figure 29-16, respectively, and are described as follows.

The command word shall contain the following information:

|            |   |
|------------|---|
| Bits 1-3   | Command Sync - Three-bit nonvalid Manchester code as defined by MC615-0010.   |
| Bits 4-6   | Address Bits - The PCM unit will respond only if these bits correspond to the address programmed at connector J6.   |
| Bits 7-9   | Operation Code - See Table 29-1 for description.  |
| Bit 10     | Input/Output - Logic 1 signifies computer transfer to PCM; 0 signifies computer request for data. Not used with all operation codes, see Table 29-1.  |
| Bits 11-22 | Starting Address - The content of these 12 bits varies depending on the operation code, see Table 29-2 for description.   |
| Bits 23-27 | Number of Words - Identifies the number of data words in the message. The allowable number is 1 to 32. For multiple word transmissions, the PCM unit shall store consecutive words in monotonically increasing storage locations. |
| Bit 28     | Parity - Odd parity check bit.  |

The CDW shall contain the following information:

|           |   |
|-----------|---|
| Bits 1-3  | Data Sync - A three-bit nonvalid Manchester code as defined in MC615-0010.                              |
| Bits 4-8  | Address Code - A five-bit code which will be identical to bits 4 to 8 of the CW which preceded the CDW. |
| Bits 9-24 | Data - A 16-bit field containing the data to be transferred to the PCM unit.                            |

*Table 29-1. Operation codes*

| Operation code                   |          | Description   |
|----------------------------------|----------|---|
| Name                             | Bits     |   |
| Load 128-kbps TLM format program | 7 8 9 10 | Load data transmitted from the computer into the 128-kbps output format RAM   |
| Read 128-kbps TLM format program | 1 0 0 0  | Read requested data from the 128-kbps output format RAM and transmit to the requesting computer   |
| Load 64-kbps TLM format program  | 1 0 1 1  | Load data transmitted from the computer into the 64-kbps output format RAM  |
| Read 64-kbps TLM format program  | 1 0 1 0  | Read requested data from the 64-kbps output format RAM and transmit it to the requesting computer   |
| Write computer data RAM          | 0 1 0 1  | Load data transmitted from the computer into the toggle buffer defined by bits 11 through 13 and starting address defined by bits 15 through 22 |
| Read computer data RAM           | 0 1 0 0  | Read requested data from toggle buffer and transmit to the requesting computer  |
| Read OI/PL RAM                   | 0 1 1 0  | Read requested data from the OI/PL RAM and transmit to the requesting computer  |
| BITE register read               | 1 1 0 0  | Transmit the contents of the BITE register to the requesting computer and reset the BITE register   |
| Format selection                 | 1 1 0 1  | Use the selected 128-kbps output format memory  |
| End of message                   | 1 1 1 X* | End of homogenous set of data   |
| Invalid codes                    | 0 0 0 X* | Not used. These codes conflict with computer nonzero address requirements   |
|                                  | 0 0 1 X* |   |

\* = spare

**Table 29-2. Starting address field**

| Operation code                              | Description   |
|---|---|
| Computer RAM                                | Bits 11 12 13   |
|   | 0 0 0 Spare   |
|   | 0 0 1 Buffer 1  |
|   | 0 1 0 Buffer 2  |
|   | 0 1 1 Buffer 3  |
|   | 1 0 0 Buffer 4  |
|   | 1 0 1 Buffer 5  |
|   | 1 1 0 Spare   |
|   | 1 1 1 Spare   |
|   | Bit 14 - Spare  |
| Bits 15 - 22 toggle buffer starting address |   |
| 128-kbps TLM format program                 | Bits 11 - 22 contain the 128-kbps format RAM starting address   |
| 64-kbps TLM format program                  | Bits 11 - 22 contain the 64-kbps format RAM starting address    |
| End of message                              | Bits 11 12 13   |
|   | 0 0 0 Spare   |
|   | 0 0 1 Buffer 1  |
|   | 0 1 0 Buffer 2  |
|   | 0 1 1 Buffer 3  |
|   | 1 0 0 Buffer 4  |
|   | 1 0 1 Buffer 5  |
|   | 1 1 0 Spare   |
|   | 1 1 1 Spare   |
|   | Bit 14 - Spare  |
| Bits 15 - 22 address for EOM                |   |
| OI/PL RAM                                   | Bits 11 - 22 contain the OI/PL RAM starting address             |
| Format select                               | Bits 11 - 21 - Spare  |
|   | Bit 22 0 = Hard format select<br>1 = Programmable format select |
| BITE register read                          | Bits 11 - 22 - Spare  |

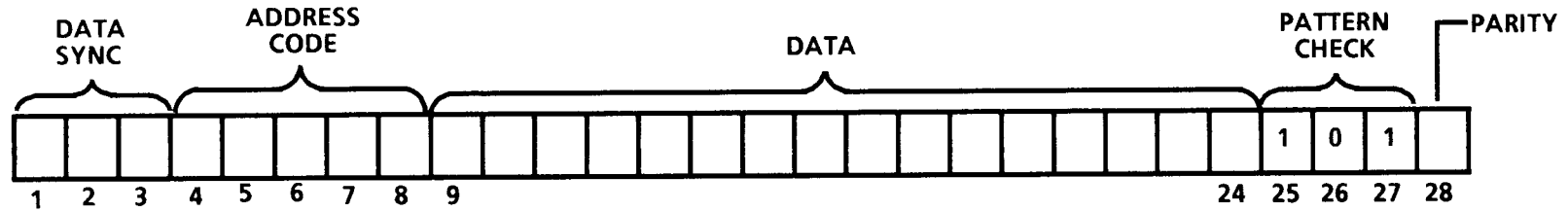
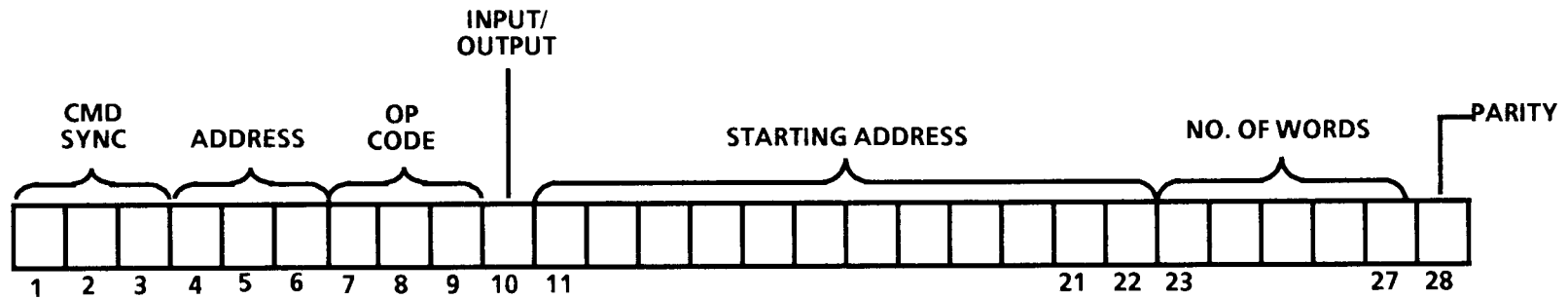


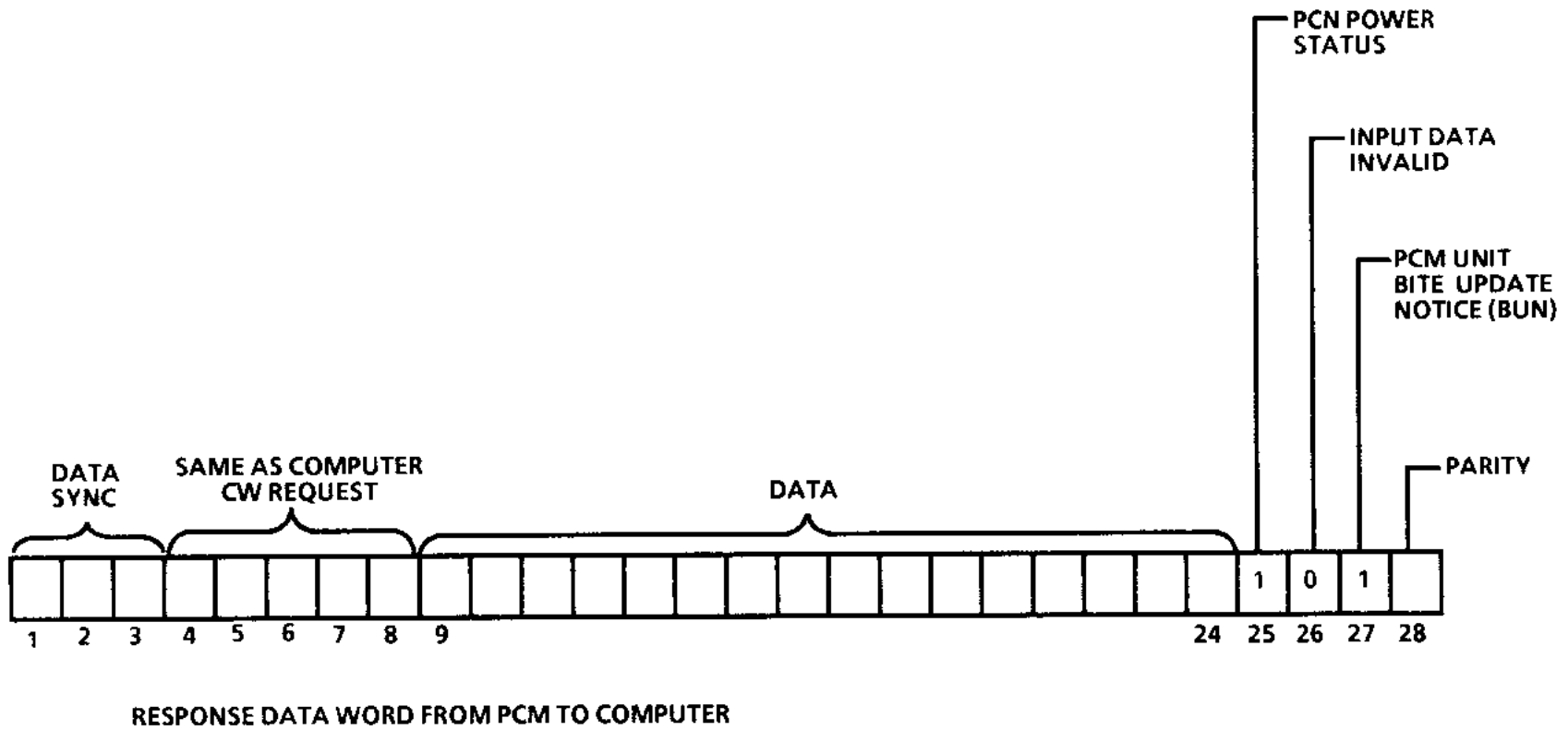
Figure 29-15. Command word format from computer to PCM unit (CDW)



18611\*004

Figure 29-16. Command word format from computer to PCM unit (CW)





18611\*005

Figure 29-17. PCMMU response data word format



## 29.4 DESCRIPTION OF OPERATION

### 29.4.1 Crew Controls

See Figures 29-18 and 29-19.

- A. OI PCMMU format switch panel C3 (S8)
  - 1. FIXED position - Selects the 128-kbps PROM format
  - 2. PROGRAM position - Selects the 128-kbps RAM format
  - 3. GPC position - Allows SPEC 62 or ground command to select either the PROM format or the RAM format
- B. OI PCMMU power switch panel C3 (S7)

This powers either PCMMU 1 or 2.

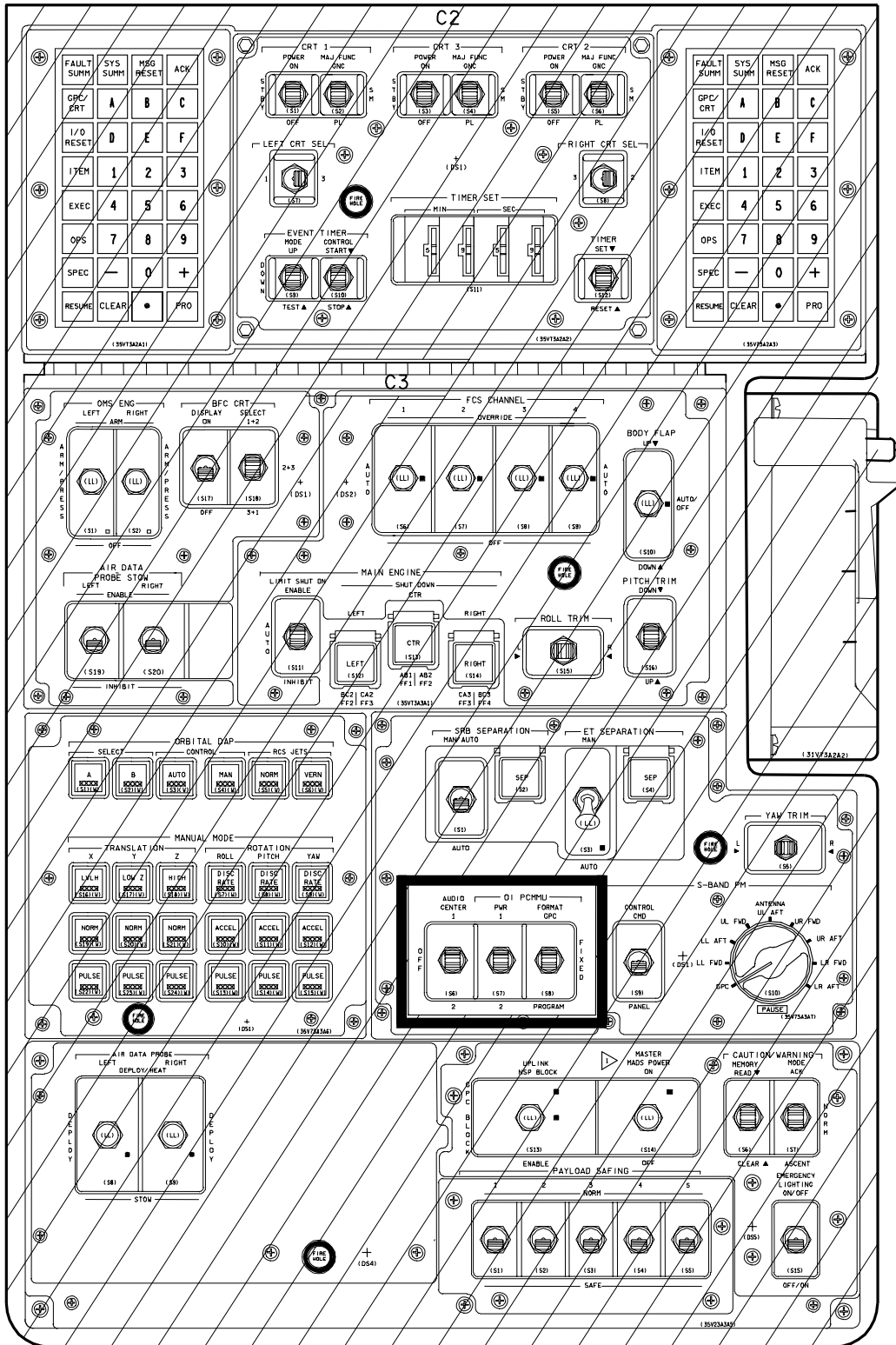
### 29.4.2 Ground Commands

There are no ground commands to switch PCMMUs. An OP CODE LOAD can be sent to the SM to load the Telemetry Format Loads (TFLs).

### 29.4.3 Telemetry

#### 29.4.3.1 PCMMU BITE Word

V75M212OP PCMMU BITE word (parent word) displayed in HEX.



186112203. ART. 2

Figure 29-18. Panel C3

```

XXXX / 062 /          PCMMU / PL COMM  XX X  DDD / HH : MM : SS
SM COM BUFF XXX          DDD / HH : MM : SS
PCMMU
BITE WORD XXXX
FMT
SEL FXD      1XS
      PGM      2XS
PGM ID 64 XXX
      128 XXX
3 SEL ID  XXX
  LOAD 4 XXXX

I / O RESET
      PCM      5XX

PSP
I / O RESET          1 CHANNEL XXXS
      PSP1  6XX  2 CHANNEL XXXS
      PSP2  7XX  PHASE LOCK XXXS
SYNC BIT XXXS          ERR ±XXXS
      FRAME XXXS  XMIT PWR XX.XXS
LOAD XXXX XXXX  PL SIG STR X.XXS

PDI
I / O RESET 8XX
BITE WORD XXXX
9 SEL DECOM X
10 SEL FMT XXX
  LOAD 11 XXXX
12 SEL INPUT X
  LOAD 13
DECOM INPUT FMT
  1 X XXXS
  2 X XXXS
  3 X XXXS
  4 X XXXS
5 - FPM XXX
DECOM ENA ENA
FDA 1 14X 3 16X
      2 15X 4 17X
18 TFL GPC SEL X
DOWNLIST
19 SEL FMT ID XX

```

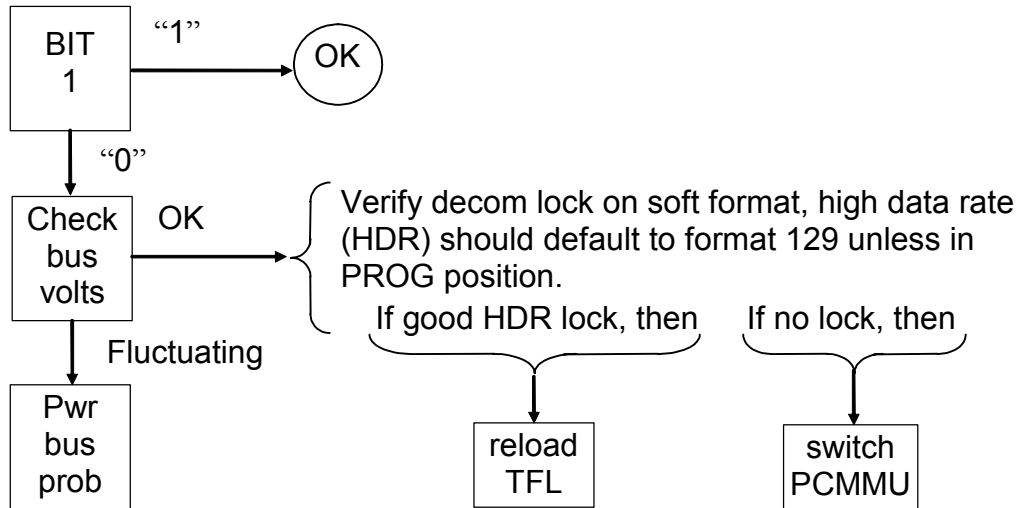
(XX)

Figure 29-19. SPEC 62

POWER STATUS

BIT 1 V75X121D

“PCM Unit Power Status Good.” Logic 1 indicates that the +5 V MU power has not dropped out during that major frame. Logic 0 indicates a power dropout.



|         |     |           |
|---------|-----|-----------|
| PCMMU 1 | CA1 | V76V0320A |
|         | AB1 | V76V0120A |
|         | MNA | V76V0100A |
|         | MNC | V76V0300A |

|         |     |           |
|---------|-----|-----------|
| PCMMU 2 | AB1 | V76V0120A |
|         | BC1 | V76V0220A |
|         | MNA | V76V0100A |
|         | MNB | V760200A  |

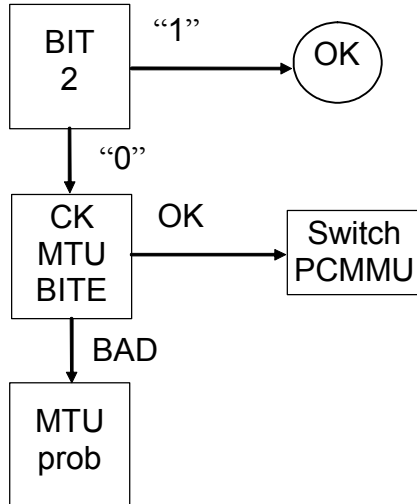
Potential PCMMU problem

- Internal power supply
- BITE status register (BSR)

MTU GOOD

Bit 2 V75X2122D

“MTU Good.” Logic 1 indicates that the MU is operating from the shuttle MTU clock. Logic 0 indicates that the MU is using the MUs internal oscillator.



NOTES:

1. GPC will lose pseudo-sync
2. Check PCMMU BITE bit 10 for MTU problem indication
3. If there is a decom dropout at the time bit 2 goes false then the PCMMU has switched to internal clock

Potential MTU problem

- Driver
- 4.608-MHz signal

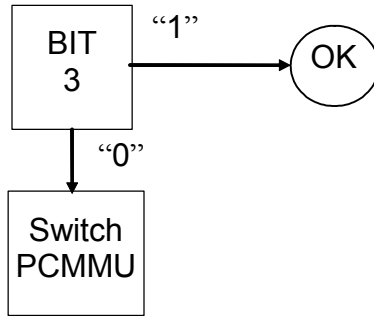
Potential PCMMU problem

- BSR
- 4.608-MHz receiver

FETCH PROM PARITY

Bit 3 V75X2123D

“FETCH PROM Parity Good.” Logic 1 indicates correct parity in the FETCH PROM and the FETCH PROM parity checker is operating normally. Logic 0 indicates either a parity error or parity checker failure.



Impact: Lost data

Potential PCMMU problem

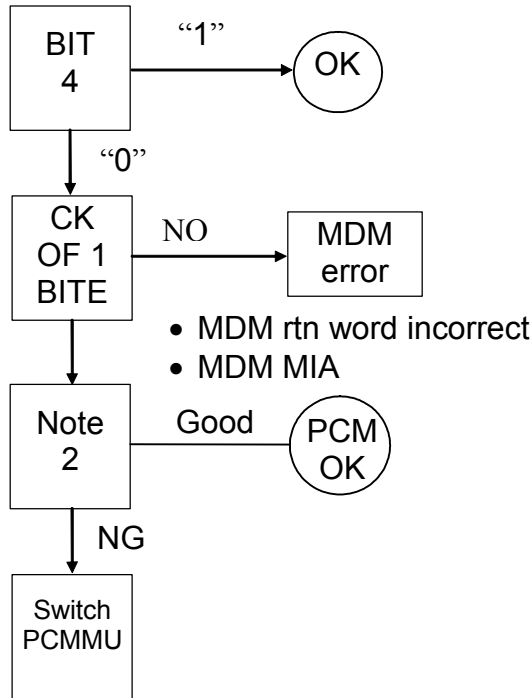
- PROM
- Parity logic
- BSR



128 TLM DOWNLINK GOOD

Bits 4 & 5      V75X2124D      V75X2125D

“128-kbps (64 kbps) TLM Downlink Good.” Logic 1 indicates that the 128-kbps (64-kbps) TLM can access both the OI and PDI memories and that these data reach the NRZ-to-Manchester converter.



NOTES:

1. Bit 4 utilizes the static wraparound bit pattern (10101010) from MDM OF 1, V75X4002D
2. If soft format in use, switch to fixed and check BSR. If good reload soft format and check BSR in soft format.
3. Check dynamic wraparound (V75X4020D) bit pattern should alternate between 10101010 and 01010101 and check bit 15
4. Data quality unknown
5. If both bits 4 and 5 are “0” then look at MDM output

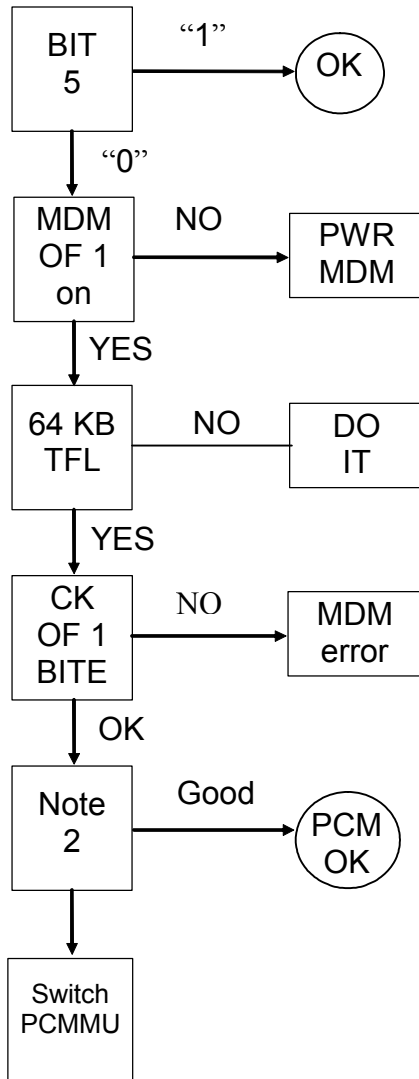
Potential PCMMU problem

- MIA
- Data RAM
- Formatter
- BSR

64 KBS TLM DOWNLINK GOOD

BIT 5

V75X2125D



- MDM rtn word incorrect
- MDM MIA

NOTES:

1. See 128-kbps TLM D/L notes
2. During a 64-kbps TFL (about 16 sec) bits 5, 12, 13 and possibly 8 and 11 may show bad until the TFL is complete.

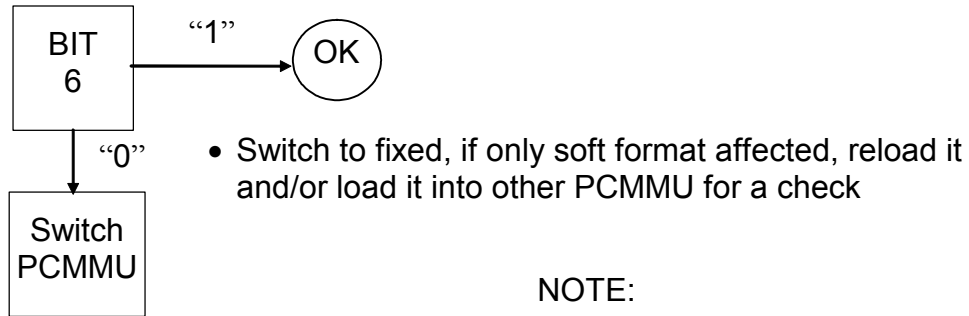
Potential PCMMU Problems

- MIA
- Data RAM
- Formatter
- BSR

128 TLM PARITY GOOD

Bit 6 V75X2126D

“128-kbps TLM Parity Good.” Logic 1 indicates correct parity in either RAM or ROM and that the 128-kbps parity checker is operating normally. Logic 0 indicates either a parity error or parity checker failure.



NOTE:

1. Data quality is unknown

Potential PCMMU problems

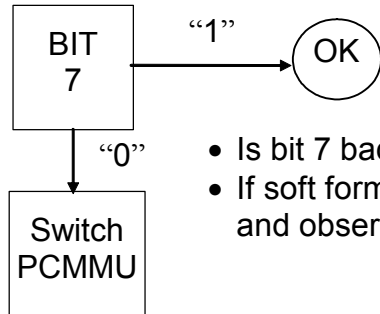
- Fixed format
  - PROM
- Soft formats
  - Parity generator
  - Memory
  - Formatter
- General
  - BSR

128 KBS TLM COUNTERS GOOD

Bit 7

V75X2127D

“128-kbps TLM Counters Good.” Logic 1 indicates that the 128-kbps TLM sample rate counters are operating correctly. Logic 0 indicates a sample rate counter failure.



- Is bit 7 bad for other formats? Are all TFL's affected?
- If soft format involved, then load it into other PCMMU and observe

NOTE:

1. Data quality unknown

Potential PCMMU problems

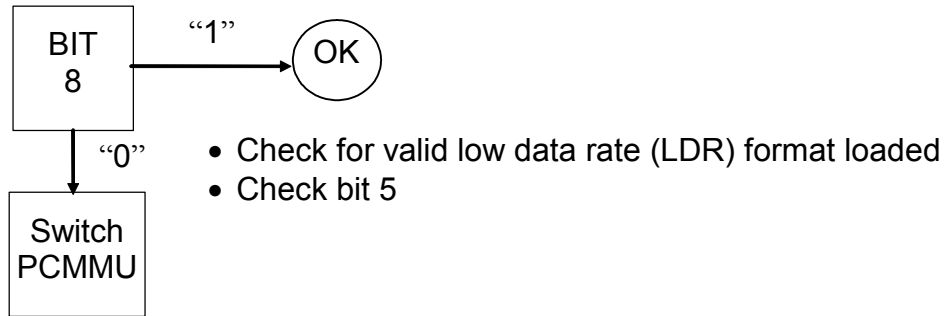
- Sample rate counter
- Compare counter
- BSR

64 KBS TLM RAM PARITY/COUNTERS GOOD

Bit 8

V75X2128D

“64-kbps TLM RAM Parity Good/Counters Good.” Logic 1 indicates correct parity, correct parity checker operations, and correct sample rate counter operation. Logic 0 indicates failure in one of the three proceeding areas.



NOTE:

1. Data quality unknown

Potential PCMMU problems

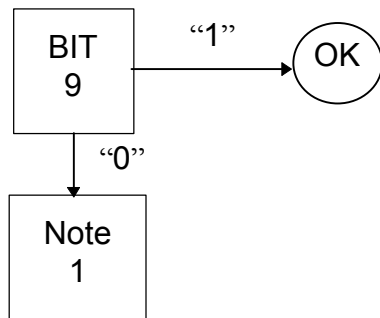
- Sample rate counter
- Compare counter
- Parity generator
- Memory
- BSR

RECORDER DATA GOOD

Bit 9 V75X2129D

“RCDR DATA” Logic 1 indicates the recorder data are changing states (1 to 0 and vice versa). Logic 0 indicates the recorder data are static.

This PCMMU BSR bit verifies the data output of the “secondary” 128kbps stream. This HDR output was designed as a secondary manual input into the Operations Recorder, but was never implemented. The current configuration allows manually cabling this “secondary” 128kbps output to the crewmembers laptop computers for WINDECOM data.



NOTE:

1. SWAP PCMMUs

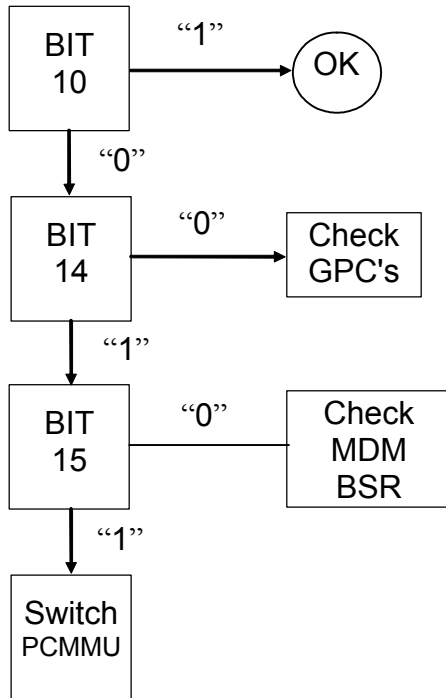
Potential PCMMU problem

- Output drivers
- BSR

INPUT DATA INVALID

Bit 10 V75X2130D

“Input Data Invalid.” Logic 1 indicates no invalid input data received. Logic 0 indicates an "Input Data Invalid" condition existed on one of seven input lines.



- Response WD error

- Response WD error
- MTU off or failed, check bit 2

NOTES:

1. If problem caused by:
  - PCMMU MIA - then all D/L data may be bad
  - MDM MIA - then related D/L data may be bad
2. Check Greenwich mean time (GMT) and mission elapsed time (MET) for updating. MDM will give a nonvalid SEV if MTU is not responding

Other problems

- MDM MIA
- Data bus coupler
- Data bus

Potential PCMMU problems

- MIA
- BSR

OI & PL RAM PARITY

PCMMU Data Ram is physically separated into **two** read/write memory cards:

(1) OI Data Ram \*\*Currently contains OI and PDI data

(2) PL Data Ram \*\*Currently contains OI, PDI, and SL data

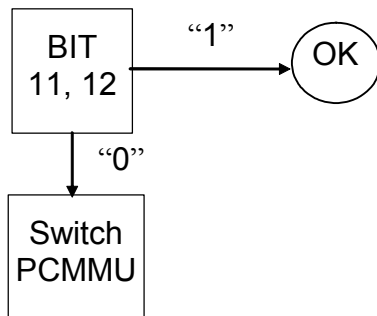
The PCMMU processes odd parity checks directly off each individual RAM.

**Bit 11** V75X2131D

“OI RAM Parity Good.” Logic 1 indicates a parity match. Logic 0 indicates the OI or PDI data being read from OI RAM parity doesn’t match its parity bit.

**Bit 12** V75X2132D

“PL RAM Parity Good.” Logic 1 indicates a parity match. Logic 0 indicates the OI, PDI, or SL data being read from PL RAM parity doesn’t match its parity bit.



NOTE:

1. Bits will indicate “0” until all MDMs are powered on. Once all are on there is no impact if an MDM is turned off
2. Data quality is unknown
3. If bit 15 is also “0” the problem could be caused by an MDM

Potential PCMMU problem

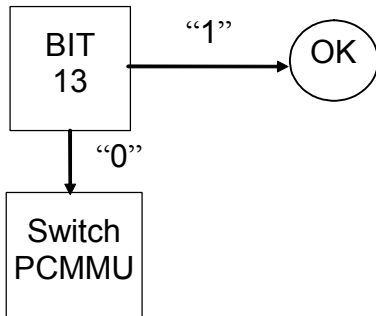
- Parity generator
- RAM
- BSR



TOGGLE BUFFER PARITY

Bit 13 V75X2133D

“Toggle Buffer Parity Good.” Logic 1 indicates correct parity in all of the five toggle buffers. Logic 0 indicates a parity error exists in one of the five toggle buffers.



NOTE:

1. Parity in a toggle buffer is inhibited until a GPC writes into that toggle buffer. It only requires one GPC.
2. Data quality of GPC downlist is unknown.

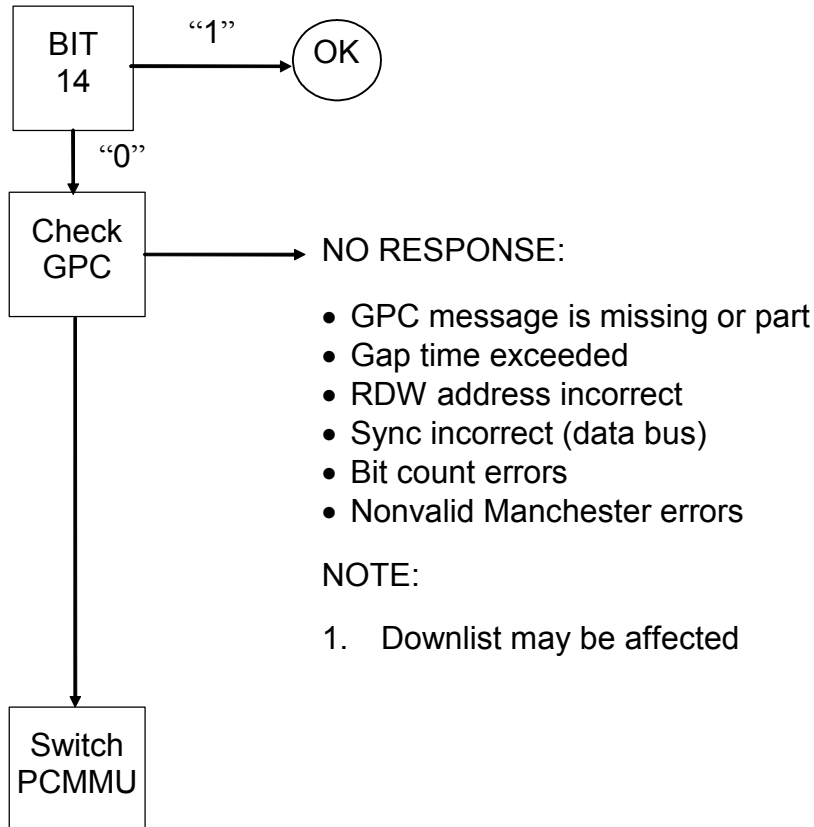
Potential PCMMU problem

- Parity generator
- Toggle buffer
- BSR

NO RESPONSE COMPUTER BUS

Bit 14 V75X2134D

“No Response Computer Bus.” Logic 1 indicates all computers are transmitting properly. Logic 0 indicates that a “No Response” condition existed on one of the five computer buses.



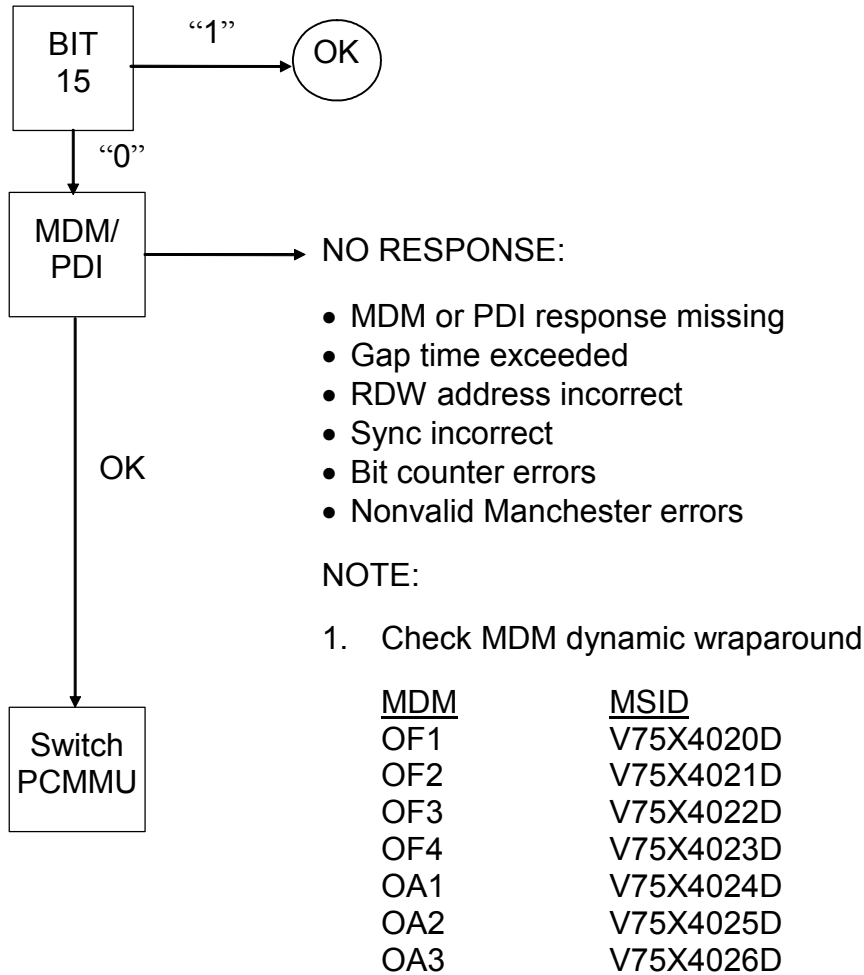
Potential PCMMU problem

- MIA
- BSR

NO RESPONSE MDM/PDI

Bit 15 V75X2135D

“No Response MDM or PDI.” Logic 1 indicates all MDMs and PDIs are responding properly. Logic 0 indicates that a “No Response” condition existed on either the MDM or PDI bus.



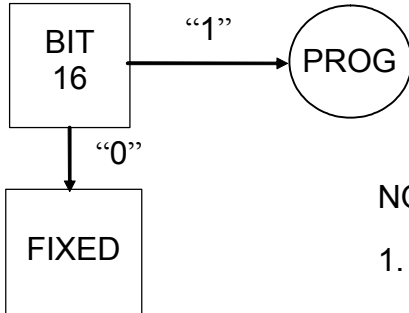
Potential PCMMU problems

- MIA
- PROM
- BSR

128 KBS PROGRAMMABLE FORMAT/FIXED FORMAT

Bit 16 V75X2136D

“128-kbps Programmable Format/Fixed Format.” Logic 1 indicates that the 128-kbps TLM is operating using its RAM. Logic 0 indicates use of PROM.



NOTE:

1. Confirm by format identification (ID) in D/L

### 29.4.3.2 PCMMU Switch Scan Measurements

V75S1001E PCMMU 1 format select - GPC  
 V75S1002E PCMMU 2 format select - GPC  
 V75S1003E PCMMU 1 format select - program  
 V75S1004E PCMMU 2 format select - program  
 V75S2107E PCMMU 1 power ON  
 V75S2109E PCMMU 2 power ON

### 29.4.3.3 PCMMU Discrete Measurements

|    |           |         |  |       |      |
|----|-----------|---------|--|-------|------|
| A. | V76X4265E | PCMMU 1 | Remote power controller (RPC) A power discrete | 0=OFF | 1=ON |
| B. | V76X4267E | PCMMU 1 | RPC C power discrete                           | 0=OFF | 1=ON |
| C. | V76X4272E | PCMMU 2 | RPC A power discrete                           | 0=OFF | 1=ON |
| D. | V76X4274E | PCMMU 2 | RPC B power discrete                           | 0=OFF | 1=ON |

### 29.4.3.4 PCMMU SM Measurements

A. V92J0050C HDR

Format ID of the HDR TFL sent to the programmable RAM in the active PCMMU by the SM 2 GPC.

B. V92J0052C LDR

Format ID of the LDR TFL sent to the programmable RAM in the active PCMMU by the SM 2 GPC.

C. V92J0053C STAT

TFL load status for the SM machine. 00 = no previous TFL by SM, 01 = TFL load in progress, 02 = last TFL good, 03 = last TFL failed.

### 29.4.3.5 PCMMU BFS Measurement

V98X0716X                      BFS TFL                      0 = fail 1 = good

If the BFS autoloads a low rate TFL and the readback does not compare, the BFS flags the load as bad. It has been estimated that the BFS will fail to load 50 percent of the time during normal OPS and 80 percent during engaged cases due to the 10 profile of the BFS. BFS will autoload if item 29 on SPEC 1 BFS memory is enabled (\*); if blank, fail will be indicated.

### 29.4.3.6 Special TM Computations

The following is the special computation for Mission Operations Computer (MOC) display of PCMMU operating mode.

MOII0700R MODE

Computation comprising V75SI001E, V75S1002E, V75SI003E, and V75S1004E

| V75S1001E | V75S1002E | V75S1003E | V75S1004E |   | Test output |
|-----------|-----------|-----------|-----------|---|-------------|
| 1         | 0         | 0         | 0         | = | GPC         |
| 0         | 1         | 0         | 0         | = | GPC         |
| 0         | 0         | 1         | 0         | = | PGM         |
| 0         | 0         | 0         | 1         | = | PGM         |
| 0         | 0         | 0         | 0         | = | FIXD        |

All other combinations are invalid and the output will be blank.

### 29.4.4 Operating Instructions SM Operations

SPEC 62 or an RF ground command (Op Code Load) is used to update the 64-kbps format RAM or 128-kbps format RAM, figure 29.19 (SPEC 62) and Console Handbook Procedure 3.45 - OP CODE LOAD. The following is a discussion of how a TFL is loaded by SPEC 62.

A. Item 1 EXEC

This will select the FIXED format or PROM. If updating the 64-kbps format only, this step is not needed.

B. Item 3+XXX

This step is for selecting the TFL. XXX is the TFL number. If XXX is less than 128, then the SM software knows to update the 64-kbps RAM.

C. Item 4 EXEC

This starts the load process. The following is an explanation of what happens.

The TFL process begins by setting the TFL status for display to RUN and zeroing the Mass Memory (MM) checksum. The word count and block address are then assigned for the MM read. Next, if an OPS transition has not occurred, an MM read is issued, with checksum, for 12 words of telemetry format data into the SM common buffer. If an OPS transition or an MM read error occurs, the error flag is set on to terminate all processing (SM common buffer freed, TFL status for display driven to FAIL, loaded 64-or 128-kbps format ID zeroed and blanked on the display based on the selected format RAM, PCMMU/PL COMM uplink error flag set on for uplink use only, Class 4 annunciation message issued, and PCMMU TFL in-progress flag set off); otherwise, the MM checksum is incremented by the checksum word in the SM common buffer and a

write is issued to load the 512 words of format data in the SM common buffer into the selected format RAM (64- or 128-kbps) of the PCMMU (for the first write to the 64-kbps format RAM of the PCMMU only, word 88 of the SM common buffer is replaced with ones before being written, and the actual contents of word 88 are saved for writing to the PCMMU later). The MM read block address and PCMMU write 64- or 128-kbps format RAM address are incremented for the next MM read and PCMMU write, respectively. This load process is repeated until all four blocks of the 2048-word telemetry format data are loaded or until an OPS transition or MM read error occurs. The PCMMU write 64- and 128-kbps format RAM addresses are reset to zero when the load is completed.

Once the load completes, the PCMMU checksum is initialized to zero and a process whereby the telemetry format data are read back from the PCMMU and checksummed is initiated. Based on the selected format RAM of the PCMMU, 512 words of telemetry format data are read into the SM common buffer and the PCMMU read 64- or 128-kbps format RAM address is incremented for the next PCMMU read. (On the first 64-kbps format RAM read of the PCMMU only, word 88 that was saved previously is written to the PCMMU before the read). If no PCMMU read error occurs, a checksum is performed on the format data in the SM common buffer and the result is used to increment the PCMMU checksum; otherwise, the error flag is set on to terminate processing. This process is repeated until all telemetry format data have been read from the PCMMU and checksummed or until a PCMMU read error occurs. The PCMMU read 64- and 128-kbps format RAM addresses are reset to zero and the SM common buffer is freed when this process completes.

If no PCMMU read error has occurred, the load process is verified by comparing the MM checksum and PCMMU checksum. If they are equal, a status bit in the ICC buffer is set on for the particular GPC processing; otherwise, it is set off (since, due to hardware configuration, only the selected or, if none is selected, the prime GPC that actually performed the PCMMU write, and read, will satisfy this checksum compare). Before a wait of 200 ms to allow the status bits to be ICC'd to all GPCs, the selected or prime GPC is determined, and then the status bit for the GPC is checked. If the status on the bit is on, the TFL status for display is set to CPLT, the HDR-LDR loaded frame length flags are assigned from the TFL MM directory for the selected telemetry format ID. Also based on the selected format RAM, the loaded 64- or 128-kbps format ID is set to the selected telemetry format ID and updated on the display. If the status bit is off, then the TFL status for display is set to FAIL, the loaded 64- or 128-kbps format ID is zeroed and blanked on the display based on the selected format RAM; the PCMMU/PL COMM uplink error flag is set ON for uplink use only; and a class 4 annunciation message is issued.

The TFL process ends by setting the PCMMU telemetry format load in-progress flag off.

If more than one TFL change is required, then do items 3 and 4 again.

Item 2 EXEC - This selects the 128-kbps format RAM.

The ground command words the same way as described above except, if SPEC 62 is up or is called up while the uplink load is in progress, the load processing shall continue and all PCMMU/PL COMM SPEC item entries are rejected.

#### **29.4.5 Operating Instructions GNC G9**

Remember, GNC Ops 9 contains SPEC 62 to allow KSC Ground Processors to perform TFL changes for payload checkouts. During G9 post-wheel stop, the crew can, via SPEC 62, swap TFLs. GPC 1, which contains the G9 software, will perform the TFL load of the PCMMU via the following normal SPEC entries:

A. Item 1 EXEC (as required)

This will select the FIXED format or PROM. If updating the 64-kbps format only, this step is not needed.

B. Item 3+XXX EXEC

This step is for selecting the TFL. XXX is the TFL number. If XXX is less than 128, then the SM software knows to update the 64-kbps RAM.

C. Item 4 EXEC

This starts the load process.

D. Item 2 EXEC

The GPC forces the PCMMU to use the Soft HDR TFL.

The capability exists for the crew to assign another GNC GPC (2,3 or 4) in the redundant set to load the TFL. The crew will assign the GPC via SPEC 62 Item 18 to load the TFL using the following procedure.

A. Item 1 EXEC (as required)

B. Item 18 + 2 EXEC (GPC 2 will now load the TFL)

C. Item 3+XXX EXEC

D. Item 4 EXEC

E. Item 2 EXEC

#### **29.4.6 TFL Flight Software Idiosyncrasies**

If you drop SPEC 62 (PCMMU.PL COMM) while a TFL is in progress, the TFL will fail. (DR 37584-R)

Several fields on SPEC 62 initialize to zero on the display instead of blank. Ignore the zeros and enter the data normally. (DR 44247-R)



When the SPEC 62 SM COMMON BUFFER BUSY indication is on, all TFL related item entries are ignored. (DR 48843-R)

If SPEC 62 is active on two Display Electronic Units (DEUs) it is possible for ILLEGAL ENTRY messages to be sent to the wrong CRT if an invalid entry is made. (DR 51821)

If the PDI is powered off (as in a Spacelab flight) an "M" will be displayed on SPEC 62 next to ITEM 5 PCMMU I/O RESET. This is because the GPC is still attempting to acquire PDI BITE status. Executing an item 5 will momentarily clear the "M" but it will return. Use the FAULT SUMMARY display to determine if there is any other PCMMU read element bypass causing the "M". (DR 55003)

If the PDI is not locked onto a data stream which supplies parameters for FDA, there may be occasional spurious Fault Detection And Annunciation (FDA) alarms. (DR 55302)

During a PDI load it is important to proceed from item 9 to item 13 on SPEC 62 in sequential order. If you select a DECOM and format to be loaded, and then select an FPM prior to executing the DECOM load, then the FPM load request will result in the DECOM being loaded. (DR 52750)

Do not stack the DECOM select and FORMAT select items on SPEC 62 in one keyboard entry (e.g., item 9 + 1 + 4). This will result in an illegal entry when you attempt to load the format with an item 11. Selecting items 9 and 10 independently will avoid this problem. (DR 48499-F)

Backup Flight System (BFS)

Due to timing differences between the Primary Avionics Software System (PASS) and BFS, the PCMMU may periodically reject a single BFS downlist frame. This usually happens when BFS in OPS-O and on internal time (not tracking PASS MTU transactions). This will occur approximately once every 16 minutes in this situation. (DR B08062)

## 29.5 REFERENCES

- A. SSHB, DWG 17.2 PCMMU
- B. PCMMU PDR, December 3 to 5, 1974
- C. PCMMU CDR, April 29 to May 1, 1975
- D. PCMMU Specification, Rev-D, February 20, 1978, MC476-0130
- E. PCMMU Compiler II program, Rev-D, January 23, 1984, MC615-0021
- F. PDI Compiler program, Rev-D, March 26, 1985, MC615-0024
- G. SM SOFTWARE, Rev-0I7, February 15, 1985, Format Load Processing Module (SFL FORMAT LOAD)
- H. INCO Console Handbook, section 3.24, PCMMU PRGM Mode Select
- I. INCO Console Handbook, section 3.26, OI ACT/DEACT
- J. INCO Console Handbook, section 3.27, Real Time TLM Processing Configuration and TLM Format
- K. INCO Console Handbook, section 3.45, TFL/DFL OP Code Uplink CMD Processing
- L. INCO Console Handbook, section 4.6, Loss of HDR TLM
- M. INCO Systems Brief, section 30, SM I/O and Error Processing Software for the PCMMU INCO Systems Brief, section 26, Orbiter OI

THIS PAGE INTENTIONALLY BLANK

**SECTION 30 - SM INPUT/OUTPUT AND ERROR PROCESSING  
SOFTWARE FOR PCMMU**

**CONTENTS**

| <b>Section</b> |   | <b>Page</b> |
|----------------|---|-------------|
| 30.1           | GENERAL .....                                       | 30-1        |
| 30.2           | PCMMU DATA ACQUISITION .....                        | 30-1        |
| 30.3           | PCMMU DATA ACQUISITION ERROR HANDLING.....          | 30-1        |
| 30.4           | SM GPC PCMMU OP CODES.....                          | 30-2        |
| 30.5           | SM ACQUISITION/DISPLAY OF PCMMU DATA OVERVIEW ..... | 30-2        |
| 30.5.1         | SM GPC DART Generation for PCMMU data .....         | 30-3        |
| 30.5.2         | FCOS Error Handling of PCMMU Data I/O .....         | 30-3        |
| 30.6           | I/O ERROR PCM .....                                 | 30-4        |
| 30.6.1         | SM GPC PCMMU Bypass Processing .....                | 30-4        |
| 30.7           | TIO AND SVC READ ELEMENT SPECIFICS.....             | 30-5        |
| 30.8           | GPC DOWNLIST .....                                  | 30-12       |
| 30.8.1         | Downlist Basics .....                               | 30-12       |
| 30.8.2         | Downlist Controls .....                             | 30-12       |
| 30.8.3         | I/O Error Downlist.....                             | 30-12       |

**FIGURES**

| <b>Figure</b> |   |       |
|---------------|---|-------|
| 30-1          | Typical set of PMU read tables (1 of 5) ..... | 30-6  |
| 30-2          | Typical set of PMU read tables (2 of 5) ..... | 30-7  |
| 30-3          | Typical set of PMU read tables (3 of 5) ..... | 30-8  |
| 30-4          | Typical set of PMU read tables (4 of 5) ..... | 30-9  |
| 30-5          | Typical set of PMU read tables (5 of 5) ..... | 30-10 |
| 30-6          | Typical PCMMU transaction.....                | 30-11 |

THIS PAGE INTENTIONALLY BLANK

## SECTION 30 SM INPUT/OUTPUT AND ERROR PROCESSING SOFTWARE FOR PCMMU

### 30.1 GENERAL

The Systems Management (SM) General Purpose Computer (GPC) provides the capability to acquire orbiter Operational Instrumentation (OI) and Payload Data Interleaver (PDI) data from the Pulse Code Modulation Master Unit (PCMMU) for onboard display and Fault Detection and Annunciation (FDA). In addition, the SM GPC to PCMMU interface is used to transfer the SM telemetry downlist which contains data previously acquired and processed from Payload Bus Terminal Units (BTUs), (Payload Multiplexer/Demultiplexers (PF1 & PF2 MDMs), flex MDMs, and the MCIU; this format is included in the Operational Downlink (OD).

This brief will provide an overview of the PCMMU fetching of digital data and describe the SM GPC to PCMMU data acquisition operation.

### 30.2 PCMMU DATA ACQUISITION

The PCMMU acquires data from OI MDMs and the Payload Data Interleaver (PDI) by following a set of instructions found in the Fetch Programmable Read-Only Memory (PROM). As long as the PCMMU is operating, this fetch sequence continues to poll the seven OI MDMs and PDI information continually overwriting the PCMMU OI/PL Data Ram address locations; this PCMMU Fetch sequence never varies.

### 30.3 PCMMU DATA ACQUISITION ERROR HANDLING

When the PCMMU acquires data from the OI or Payload (PL) bus, it performs a set of validation tests on the transaction before it stores the data in the OI/PL Random Access Memory (RAM). The OI/PL RAM consists of 4096 addresses, each address consists of 18 bits (16 contain the specific polled data, bit 17 is validity, bit 18 is a parity check).

If the transaction fails any of these tests, the PCMMU will not store the data into the 16-bit address (this address will then be "static"), but it will set Validity bit (#17) "high" at the applicable RAM address. The PCMMU telemetry formatter is not programmed to poll bit 17; so MCC operators "may be" unaware static information is stored at a specific OI/PL RAM Address; The original PCMMU designers needed to conserve RF bandwidth, so they decided to exclude bit 17 from each TFL poll.

The GPC to PCMMU interface does not have this "bandwidth" limitation, so when the SM GPC performs data acquisition on a PCMMU OI/PL RAM location which contains static data, the static data is sent to the GPC, but when the PCMMU I/O buffer sees the Validity bit 17 set, it will set the E bit (in the SEV pattern) "high" when it sends the static data to the GPC. The SEV pattern, as well as the 28-bit transfer format, are discussed in the MDM Systems Brief INCO/COMM SB 28.

### 30.4 SM GPC PCMMU OP CODES

The SM GPC is designed to poll the PCMMU for various operations.

|           |                           |            |                           |
|-----------|---------------------------|------------|---------------------------|
| OP Code 4 | Select PGM Format         | OP Code 10 | Read LDR RAM for Checksum |
| OP Code 5 | Download to Toggle Buffer | OP Code 11 | Load LDR TFL              |
| OP Code 6 | SM: Read OI/PL Data Ram   | OP Code 12 | Bite Status (Wrap Word)   |
| Op Code 7 | Not Used                  | OP Code 13 | Select Hard Format        |
| OP Code 8 | Read HDR RAM for Checksum | OP Code 14 | TCS: Read OI/PL Data Ram  |
| OP Code 9 | Load HDR TFL              | OP Code 15 | Not used                  |

SM Data Acquisition/FDA software is scheduled to operate once every four minor cycles (160 milliseconds) by the SM OPS control segment. A total of 12 PCMMU I/O transactions generated out of data Acquisition (ACQ)/FDA will occur over on SM major cycle of 2 seconds or 6 transactions over a 1-second system software major cycle.

OP Code 6 was developed to acquire data stored within the PCMMU OI/PL Data Ram. A RAM read command will also contain the RAM starting address and number of consecutive words to be returned to the SM GPC.

### 30.5 SM ACQUISITION/DISPLAY OF PCMMU DATA OVERVIEW

The SM GPC is designed to acquire approximately 20% of all the PCMMU OI/PL Data Ram addresses to eventually be stored within the SM Parameter Data Tables. The data within the SM Parameter Data Tables are used for SM GPC CRT Display and Fault Detection and Annunciation.

A quick overview is necessary to understand the detail of the SM to PCMMU transactions. The SM GPC software needs specific MSIDs from the PCMMU OI/PL Data Ram for Display and Fault Detection and Annunciation. The SM GPC stores the specific PCMMU OI/PL Data Ram address locations where these specific MSIDs are located within the Data Acquisition and Read Table (DART).

The SM software will use the information within the DART and create 12 specific Read Cycles commands which are built to collect the “needed” OI/PL Data Ram information within 1.92 seconds. The 12 specific Read Cycles are broken down into two groups, the 6 Timer Initiated (TIO) Tables and 6 Supervisor Calls (SVCs) Tables are functionally similar. A TIO/SVC may contain up to 24 read elements; each read element may request up to 32 continuous PCMMU OI/PL Data Addresses.

After the SM GPC has “acquired” the TIO/SVC information from the PCMMU, SM Software passes the acquired data to the SM GPC input buffer. As part of the Input

Buffer Processing, PCMMU Read Elements are subject to FCOS error detecting processing.

If the data within the input buffer is satisfactory, the SM Data Acquisition/FDA software will determine which of the acquired data needs to be stored in engineering units (EU); it then calls forward scaling to perform this computation prior to being finally stored within the SM Parameter Data Tables for use on the SM CRTs and FDA. If data needs to be used in PCM count format, SM Data Acquisition/FDA will bypass forward scaling and pass the parameter directly from the Input Buffer to the SM Parameter Data Table.

### **30.5.1 SM GPC DART Generation for PCMMU data**

Since the parameters acquired from the PCMMU may vary, the SM preprocessor must incorporate general rules to build efficient I/O profiles (the DART) according to a specific flight.

The SM GPC will chain these PCMMU read elements by linking multiple word group commands into a single PCMMU read request called an I/O transaction.

Each of these transactions consist of up to 24 Timer Initiated PCMMU read (TIO) elements. Each read element in a transaction has an associated element ID. The 1.04-Hz element IDs will be from 1 to 24; however, 0.52 Hz element IDs can be 1 to 24 or 25 to 48 indicating in which portion of the 2-second SM MAJOR CYCLE transaction a 0.52-Hz element resides.

Supervisor Call (SVC) initiated read element transactions are used for any additional PCMMU reads that may be required over the 24 timer initiated read element chains (per transaction). SVC read element IDs are defined in the same manner as timer initiated reads. A brief description of timer initiated reads and SVC reads are included at the end of this brief.

If SVC PCMMU reads are required for a given mission, they will be executed along with low rate MDM SVC reads by data ACQ/FDA after the PCMMU timer initiated reads, within a scheduled data ACQ/FDA cycle. This is done so that the timer reads may be processed by data ACQ/FDA while the IOP is acquiring the SVC read element data. All PCMMU timer initiated reads as well as high rate MDM timer initiated reads are initialized on at SM OPS transition time and are subsequently set up by the data ACQ/FDA software via Data Acquisition Read Table (DART) entries at the end of the preceding cycles execution. This fact will be of special interest in later discussion on I/O error responses. Figure 30-1 describes a typical set of PCMMU read tables (transactions).

### **30.5.2 FCOS Error Handling of PCMMU Data I/O**

The bus-level I/O transactions are handled by the Flight Computer Operating System (FCOS). As a part of all I/O processing, PCMMU read elements are subjected to the



FCOS error detection processing, which includes checks on parity, response, and the SEV pattern contained in each 28-bit data transfer from the PCMMU.

### 30.6 I/O ERROR PCM

When the FCOS detects a IP bus interface failure, it will “bypass” the whole bus and annunciate the I/O Error PCM, vice individual Bus Control Element Bypass OF A, OF B, OA, and PL messages. The action involved with any Bus Control Element Bypass is a cessation of all read and write commands associated with that particular OP Code. To restore the SM GPC polling of the PCMMU, either an SM I/O Reset or an PCMMU I/O Reset must be performed.

An I/O reset is accomplished for all PCMMU read elements by any of the following: (1) I/O reset function being executed from the keyboard when Display Electronic Unit (DEU) is selected to SM major function, (2) execution of the I/O reset PCMMU item 5 entry on S62 PCMMU/PL COMM, (3) SM OPS transitions involving SM memory reconfiguration, and (4) PCMMU I/O reset by uplink using the TFL/DFL Op Code.

#### 30.6.1 SM GPC PCMMU Bypass Processing

If an error occurs and the PCMMU Response Word contains the SEV “E bit”, the SM GPC FCOS will maintain a Read Element Input Buffer Error Displacement code for each PCMMU transaction.

After SM data ACQ/FDA has transferred the read element data to FCOS, FCOS will begin reading data into SM until an error occurs on a read element or the transaction is complete. Upon receiving a failed read in a PCMMU transaction, SM data ACQ/FDA will set its own Commfault Status Bits on the Read Elements of the PCMMU transaction based on this Error Displacement Code sent by FCOS. The good read elements prior to the error are processed normally.

If, on the next issuance of a PCMMU transaction request involving a previously Commfaulted Read Element, any failure occurs within the same rate group, the failed element in the second transaction will be removed (bypassed) from all subsequent read requests by SM data ACQ/FDA until an I/O reset PCMMU occurs. A rate group of elements is that portion of a transaction request consisting of all elements for a given data acquisition rate (1.04 Hz or 0.52 Hz). Only one read element is bypassed in a given SM PCMMU read cycle.

Anytime specific PCMMU read elements are bypassed, a class 3 annunciation output corresponding to the PCMMU source (7 OI MDMs or PDI) is output. The specific message outputs are: S62 BCE BYP OF A (OI MDMs OF 1 and OF 2), S62 BCE BYP OF B (OI MDMs OF 3 and OF 4), S62 BCE BYP OA (OA 1/2/3 MDMs) and S62 BCE BYP PL (PDI). Annunciation output for a specific source is not enabled again until a PCMMU I/O reset occurs.

The SM data ACQ/FDA software maintains a group of **Read Element Status Indicators** and **Read Element Bypass Indicators** for each unique PCMMU read element. Read Element Status indicators are reset prior to each read. If an I/O error occurs for a read element, its status indicator and those of all subsequent read elements in that transaction are set. The corresponding Read Element Bypass indicator is OR'ed to the read element status indicator after the I/O transaction. The resulting status is referred to as Commfault Status. Read Element Bypass indicators are set when an element has bypassed due to either Read Element Bypass or PCMMU No Response processing. If any of the PCMMU elements are bypassed, the PCMMU I/O reset discrete is set to "off".

To minimize the downlist bandwidth required to determine PCMMU or I/O error status, two 16-bit words are generated by SM which ORs all 24 read elements of a PCMMU transaction (Read Cycle) into one bypass parameter. The first 16-bit word contains the six timer-initiated PCMMU transaction bypass parameters and six SVC-initiated bypass parameters for a GPC major cycle plus a 4-bit code of the read cycle (transaction) ID of the last logged error. The second 16-bit word will include a 6-bit code of the read element number (ID) of the last error, within a transaction and also a PCMMU element I/O error counter. The element I/O error counter contains an integer count of the number of I/O errors that have occurred on the PCMMU IP bus since the last PCMMU I/O reset.

Prior to a given flight, a list of individual read element IDs and transactions are compiled which will provide the source; OI MDM 1-7, PDI of each PCMMU read element. This data will allow the ground to determine the specific source of failed PCMMU read element, as well as, an internal PCMMU failure. Decoding of these bits is described in the console handbook.

### 30.7 TIO AND SVC READ ELEMENT SPECIFICS

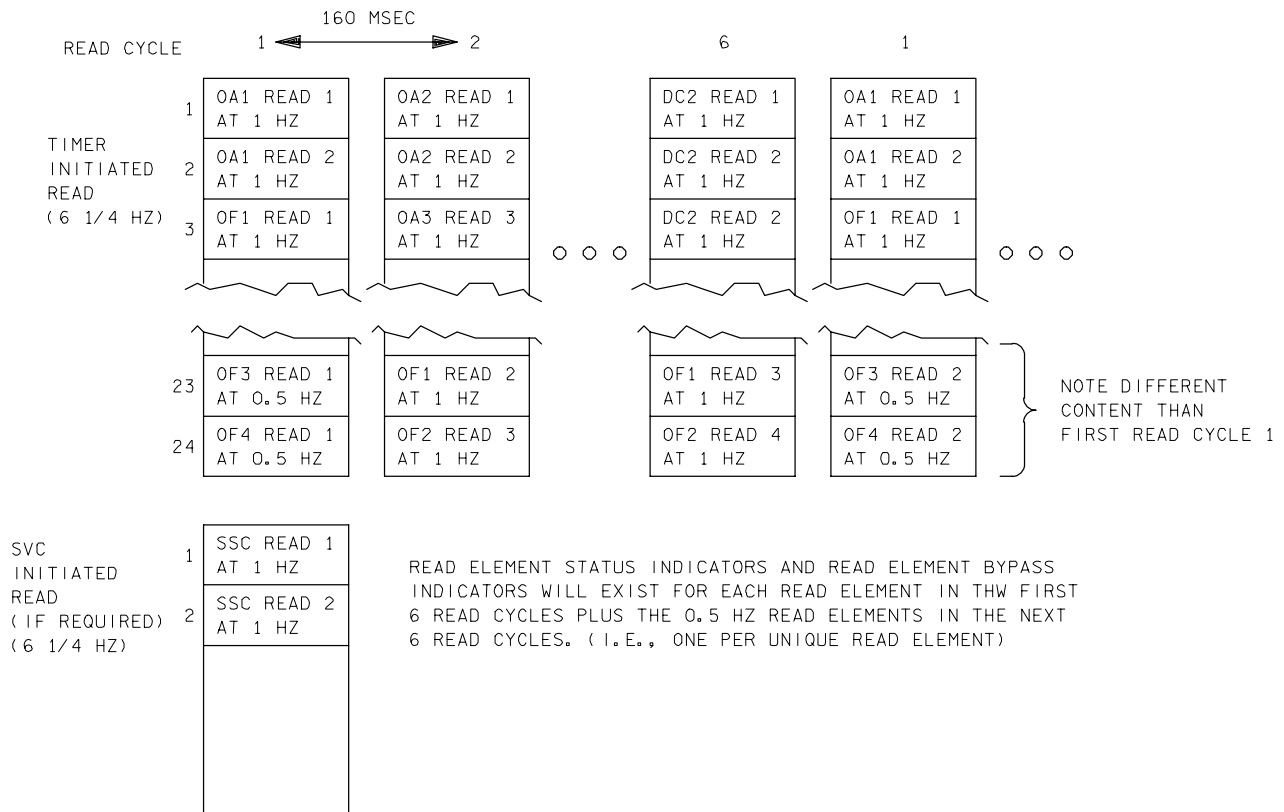
Timer Initiated and SVC Read Elements - As previously noted, PCMMU I/O can be accomplished by two different mechanisms: TIO read elements and SVC read elements. Timer-initiated read elements are associated directly with the scheduled run time of the process; in this case data ACQ/FDA. It can be thought of as automatic I/O. When the data ACQ/FDA process is due per its operations schedule, it is checked by process control in FCOS to see if it has associated timer initiated I/O. If it does, the transaction ID is automatically moved to the I/O que for I/O processing based on its priority. Process control calls the SM data ACQ/FDA process to begin processing. As noted previously, data ACQ/FDA sets up its next timer I/O read elements at the end of its process cycle (i.e., it fills out the transaction skeleton contained in FCOS for the timer reads which occur in the next cycle). This means that all the necessary data for an I/O read is already in a transaction table and ready to be executed when the data ACQ/FDA process is next scheduled to run. See Figure 30-1 to Figure 30-5.

PCMMU SVC read elements are executed external to the standard data ACQ/FDA process itself during its sequential execution; i.e., this is an "on demand" input request

and the PCMMU read only occurs when the SVC is issued. If additional PCMMU read elements are required in a specific cycle of data ACQ/FDA, it builds the MACRO (instruction set) in that cycle and issues an SVC read request to FCOS. This request is fielded by the SVC handler in FCOS. The requested transaction is added to the I/O queue based on its priority.

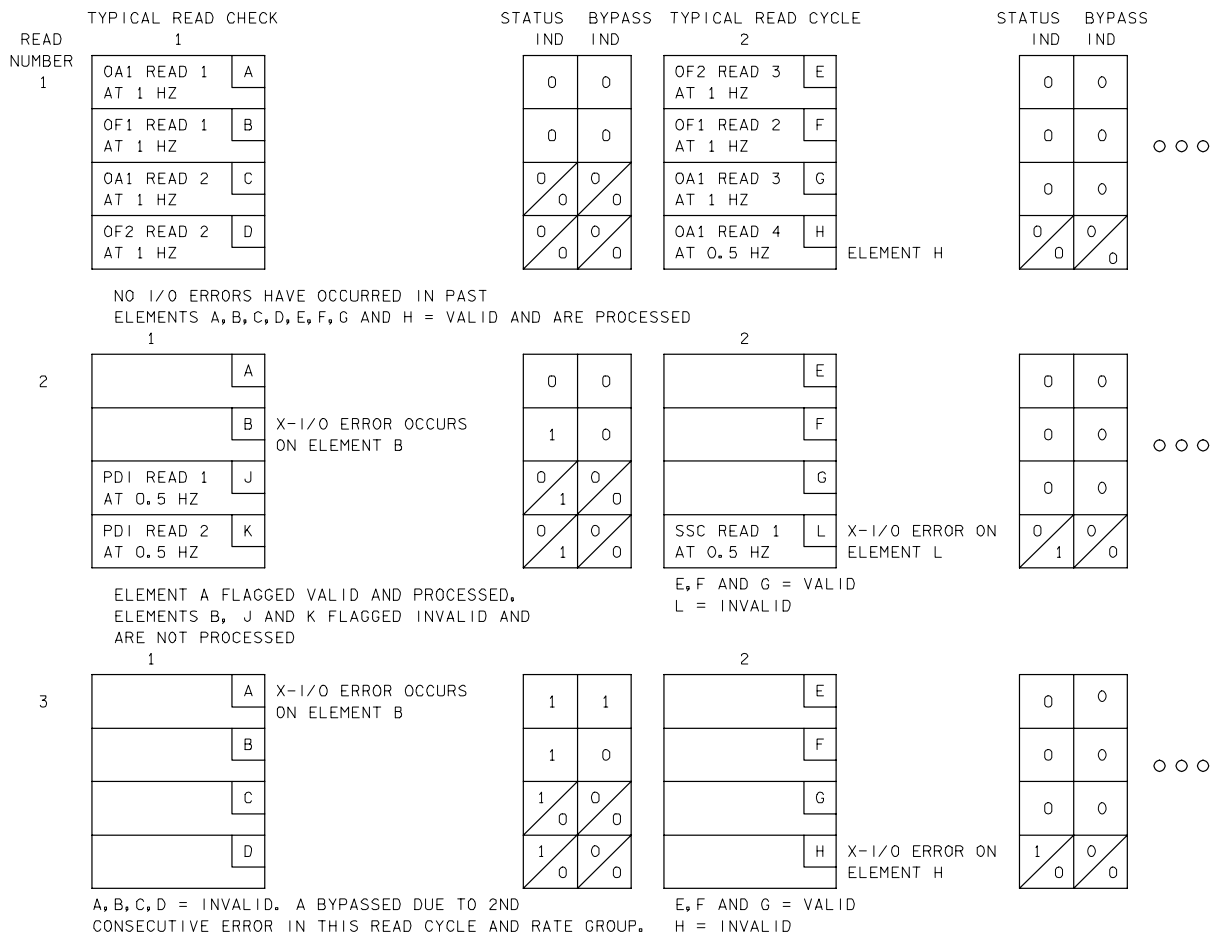
Basically, TIO reads are cyclic data reads which are automatically accomplished whenever the process is scheduled to run; while SVC reads are on demand data reads scheduled out of the operating process when it requires extra data.

There are some exceptions to this rule. The SM GPC Payload Signal Processor (PSP) cyclic module performs all of its I/O as SVC reads/writes, because the I/O rate will change depend on whether a command is sent to the PSP. Normally the SM GPC will cycle 1 Hz SVC read of PSP status data; however, when a command is sent to the PSP, it "upmodes" the PSP status read request to 12.5 Hz so that PSP status data can be used in error processing. Figure 30-6 should be used to aid in understanding the above explanations.



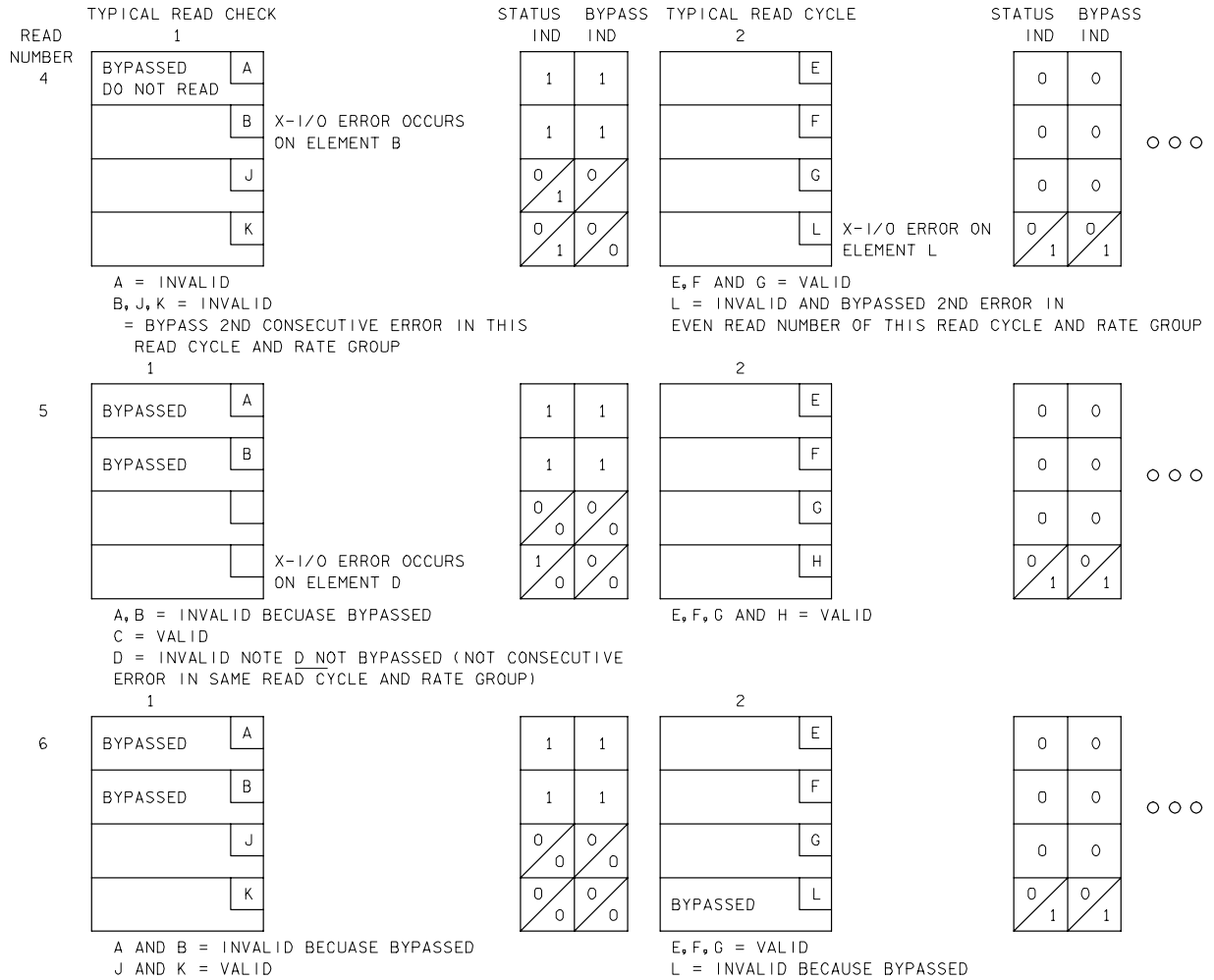
1064. ART 3

Figure 30-1. Typical set of PMU read tables (1 of 5)



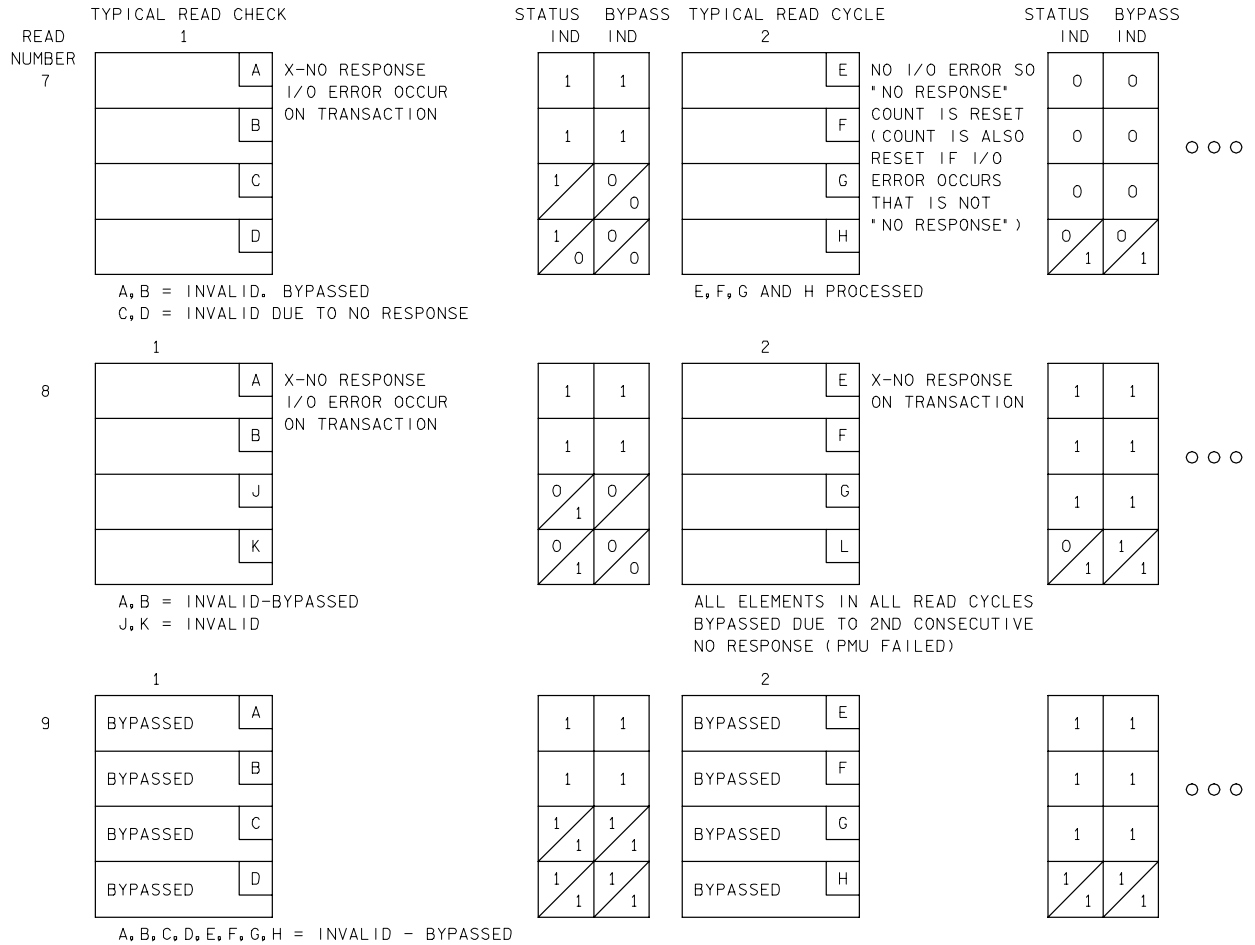
1064. ART, 3

Figure 30-2. Typical set of PMU read tables (2 of 5)



1064. ART, 3

Figure 30-3. Typical set of PMU read tables (3 of 5)



1064. ART. 3

Figure 30-4. Typical set of PMU read tables (4 of 5)

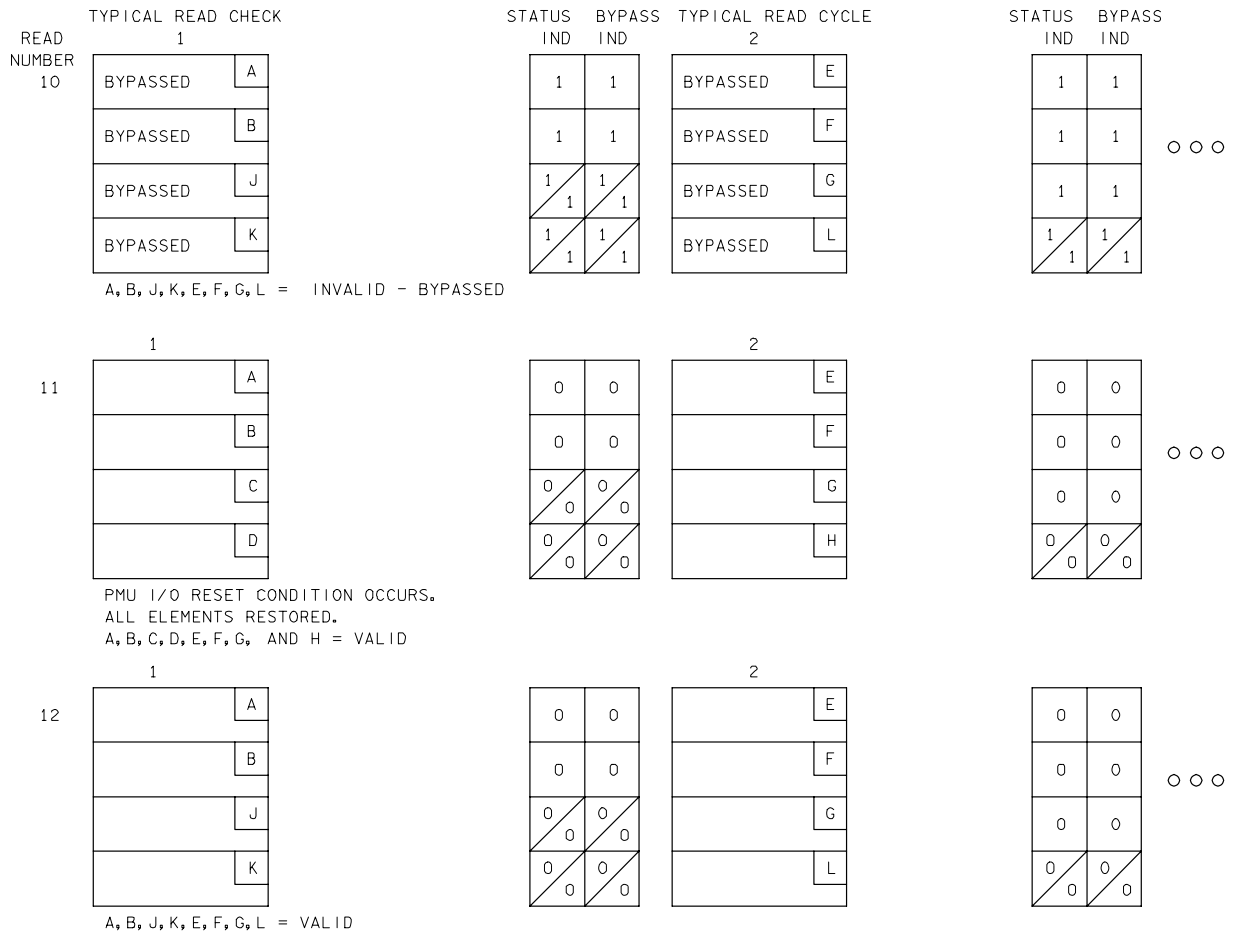
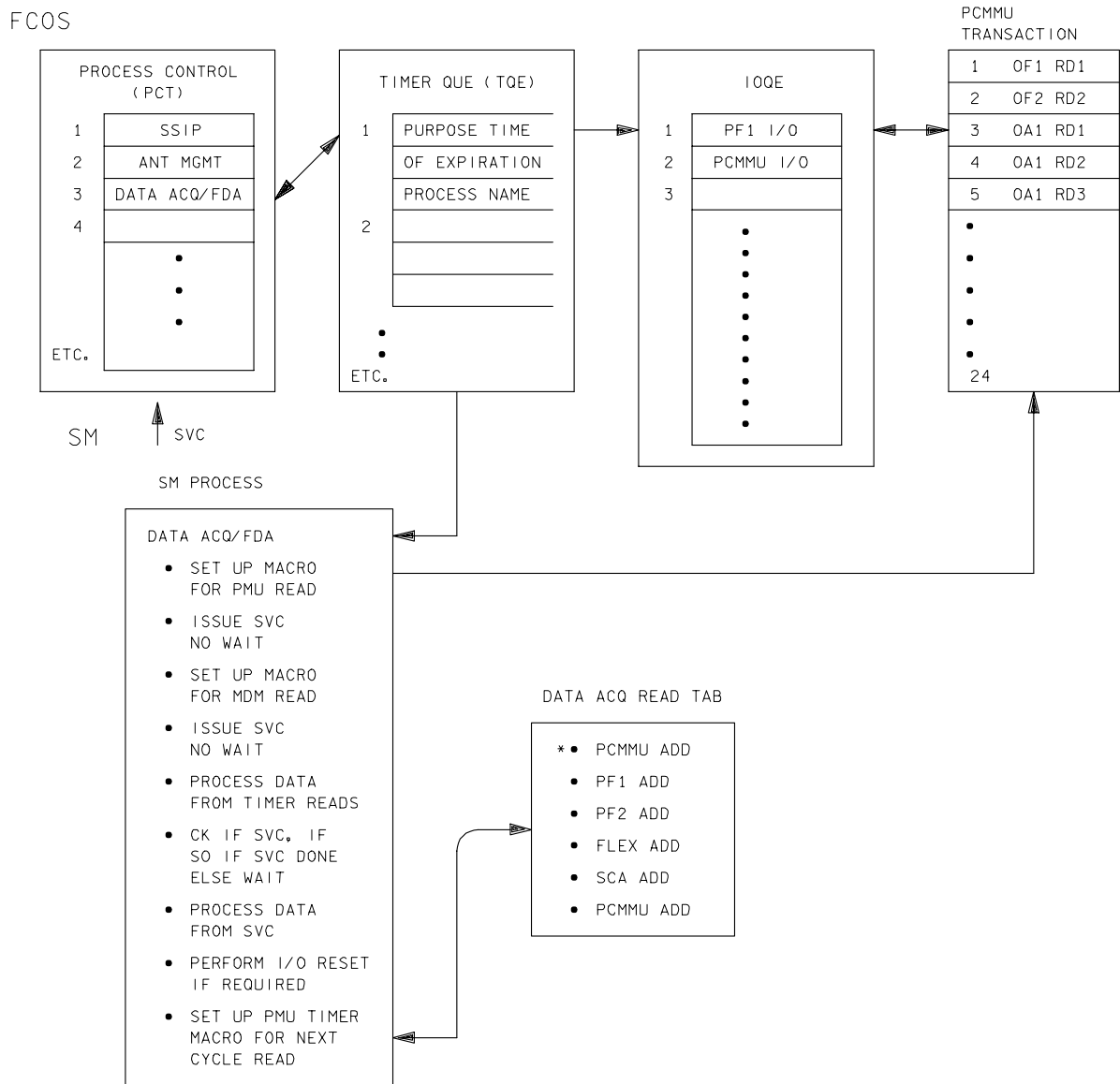


Figure 30-5. Typical set of PMU read tables (5 of 5)



1064. ART: 3

**Figure 30-6. Typical PCMMU transaction**



## 30.8 GPC DOWNLIST

### 30.8.1 Downlist Basics

The GPC downlist software is of very simple nature. All it does is fetch the data located in memory locations and throughput these data to the Input/Output (I/O) systems software.

The I/O software conveys these data to the communications system via the PCMMU IP Bus. The processor is activated 25 times a second. Each time it is activated, it creates a frame of data according to a table which is frame count and memory configuration dependant.

The maximum downlist rate is 25Hz, other legal downlist rates for parameters are 12.5Hz, 5Hz, and 1Hz. The maximum bandrate 51.2 kbps.

### 30.8.2 Downlist Controls

There are three kinds of controls for the downlist

1. There is a sequence of item numbers that can be used to define the frame length of a dump downlist, the start and stop address of the area to be dumped, and finally the dump. Examples of this type are the HISAM and Software Dump.

2. There is also a control that defines which GPC will talk to Toggle Buffer 1 in the PCMMU. The permissible values to enter with SPEC 1 (ITEM 44+ 1,2,3,4,5). The software module that starts executing when this is done alters the GPC ID for TB 1 and calls the ICC routine that places the identify of the new Toggle Buffer 1 down list into the set of data that is ICC'd. This allows the other computers in the common set to know who the TB 1 user is. Remember the other GPCs still build the downlist and ship it to the PCMMU via their own independent IP buses. However the PCMMU discards the data because the downlist data are built with an invalid user adapter (IUA) address.

3. There is a control of OPS 0 ENA that allows the nonprime OPS 0 GPC to downlist through TB 4. Although, INCO must remember to get a TFL that uses TB 4 to see OPS 0 data on the ground.

On orbit, the nominal situation is for the lowest numbered GNC GPC to downlist to TB 1 and the SM GPC to talk to TB 2.

### 30.8.3 I/O Error Downlist

This GPC error occurs on the second consecutive I/O error detected by the I/O Processor during downlist write transactions. In theory, this can be caused by a GPC IP bus MIA transmitter failure, or the corresponding PCMMU IP Bus MIA receiver failure.

**SECTION 31 - PAYLOAD INTERROGATOR**  
**CONTENTS**

| <b>Section</b> |  | <b>Page</b> |
|----------------|--|-------------|
| 31.1           | GENERAL DESCRIPTION.....   | 31-1        |
| 31.2           | INTERFACES .....   | 31-1        |
| 31.2.1         | Control and Displays .....   | 31-3        |
| 31.3           | DESCRIPTION.....   | 31-5        |
| 31.3.1         | Electrical.....  | 31-7        |
| 31.3.2         | Power .....  | 31-26       |
| 31.3.3         | Mechanical .....   | 31-26       |
| 31.3.4         | Software .....   | 31-26       |
| 31.4           | INSTALLATION.....  | 31-26       |
| 31.4.1         | Location.....  | 31-26       |
| 31.4.2         | Temperature.....   | 31-26       |
| 31.5           | DESCRIPTION OF OPERATION.....  | 31-28       |
| 31.5.1         | Example of Flight Controller commands for PI Receiver Lock: .....    | 31-28       |
| 31.5.2         | Example of Flight Controller commands for PI Transmitter Lock: ..... | 31-28       |
| 31.5.3         | Telemetry .....  | 31-28       |
| 31.6           | SPECIAL TELEMETRY COMPUTATIONS.....                                  | 31-29       |
| 31.7           | REFERENCES.....  | 31-31       |
| 31.8           | OPERATIONAL NOTES .....  | 31-31       |

## TABLES

| Table |   | Page  |
|-------|---|-------|
| 31-1  | Synthesizer channel frequency allocation.....   | 31-32 |
| 31-2  | PI telemetry switch and/or command control..... | 31-33 |

## FIGURES

| Figure |   |       |
|--------|---|-------|
| 31-1   | PI interface diagram .....  | 31-2  |
| 31-2   | Panel A1L .....   | 31-4  |
| 31-3   | SPEC 62, PCMMU/PL COMM display.....   | 31-5  |
| 31-4   | PI triplexer.....   | 31-8  |
| 31-5   | PI Receiver Sweep Prior to Lock .....   | 31-10 |
| 31-6   | Block diagram payload interrogator receiver .....   | 31-11 |
| 31-7   | AGC amplifier, detectors, loop filters, and threshold detector<br>simplified diagram..... | 31-13 |
| 31-8   | Synthesizer functional block diagram .....  | 31-16 |
| 31-9   | PI Transmitter Sweeps .....   | 31-18 |
| 31-10  | PI transmitter power amplifier block diagram.....   | 31-19 |
| 31-11  | Power switching block diagram reflective hybrid switching matrix .....                    | 31-21 |
| 31-12  | Power converter block diagram .....   | 31-23 |
| 31-13  | Command processor block diagram .....   | 31-24 |
| 31-14  | AV bay layout.....  | 31-27 |

## SECTION 31 PAYLOAD INTERROGATOR

### 31.1 GENERAL DESCRIPTION

The Payload Interrogator (PI) is a Line Replaceable Unit (LRU) capable of receiving and transmitting signals compatible with the Space Ground Link Station (SGLS) and Spaceflight Tracking and Data Network/Deep Space Network (STDN/DSN) operational modes and signal formats.

### 31.2 INTERFACES

The PI has interfaces (Figure 31-1) with the following:

Payload Signal Processor (PSP) - For transfer of data to the crew's payload station and to the Payload Data Interleaver (PDI) for downlink. Data rate can be 1 to 16 kbps. Also for transfer of 16KHz subcarrier used to modulate the PI transmitter for uplink commands (2 kbps).

Ku-band signal processor - For bent-pipe transmission to the ground. It can have a bandwidth up to 4 MHz.

Payload station - Used with Department of Defense (DOD) payloads. Basically just disables the PSP/PI interface for secure operations.

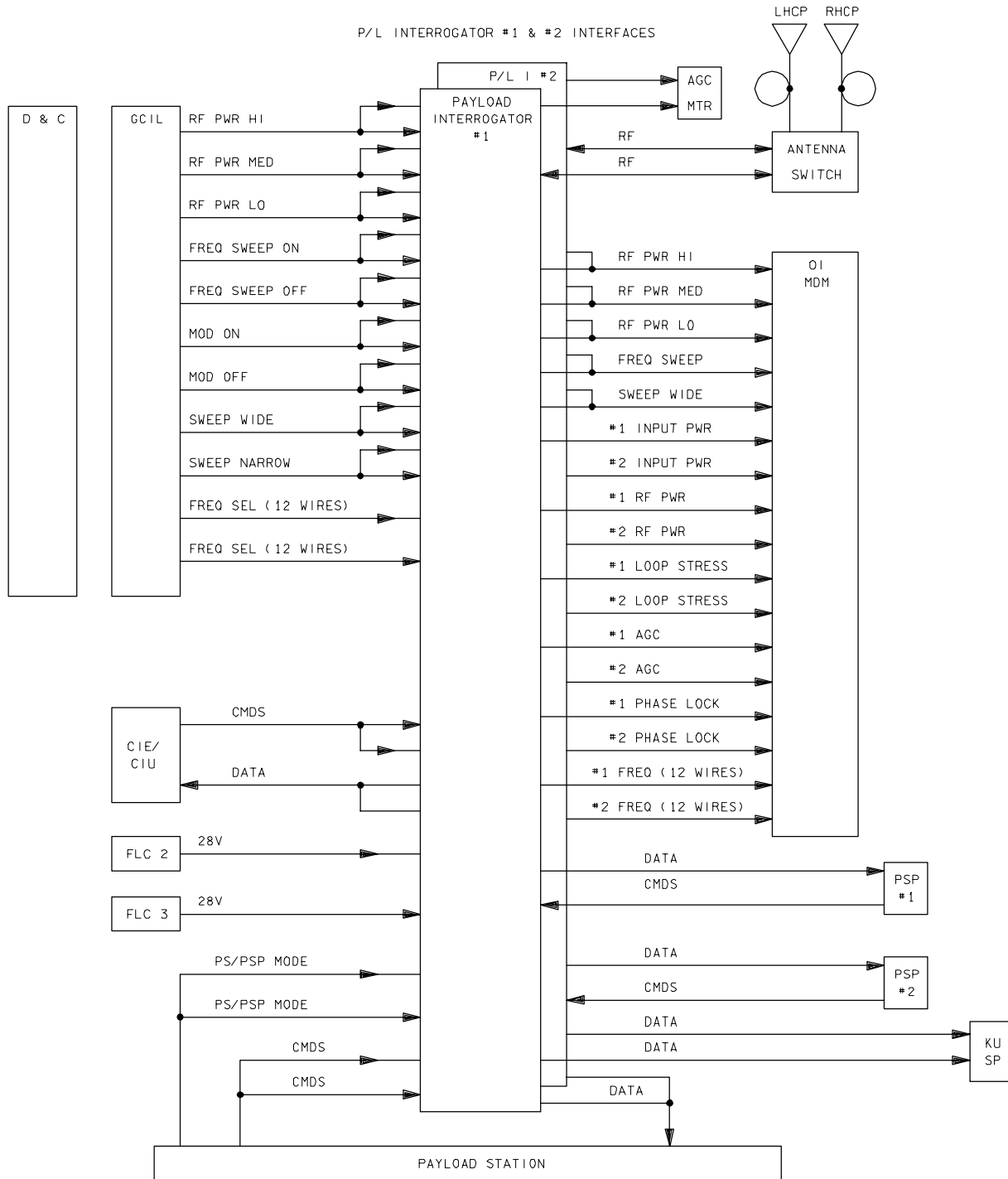
Payload antenna switch - Provides the interface between the PI and PI antenna. Determines which circular pattern is to be used (Left-Hand Circular Polarization (LHCP) or Right-Hand Circular Polarization (RHCP)).

Ground Control Interface Logic (GCIL) - Allows the PI to be controlled by panel or by command.

Orbiter Instrumentation (OI) Multiplexer/Demultiplexers (MDMs) OF2 and OF4 - Provide telemetry data concerning system operation.

Meter M1 on panel A1U - For signal strength.

Communications Interface Unit (CIU) - Function same as PSP. Used with IUS/TDRS.



1575. ART 3

**Figure 31-1. PI interface diagram**

## 31.2.1 Control and Displays

### 31.2.1.1 Control, Panel A1L

This panel (Figure 31-2) is used by the crew to configure the PI. The available functions are as follows:

ANT POLAR (S2) - This switch is used to select left-hand circular or right-hand circular patterns. These inputs go through the GCIL and directly to the antenna switch.

XMIT PWR (S4) - This switch is used to select the output power of the transmitter. This input goes through the GCIL to the PI.

CHANNEL SELECT (S7) - This switch is used to select the payload frequency. These inputs go through the GCIL to the PI.

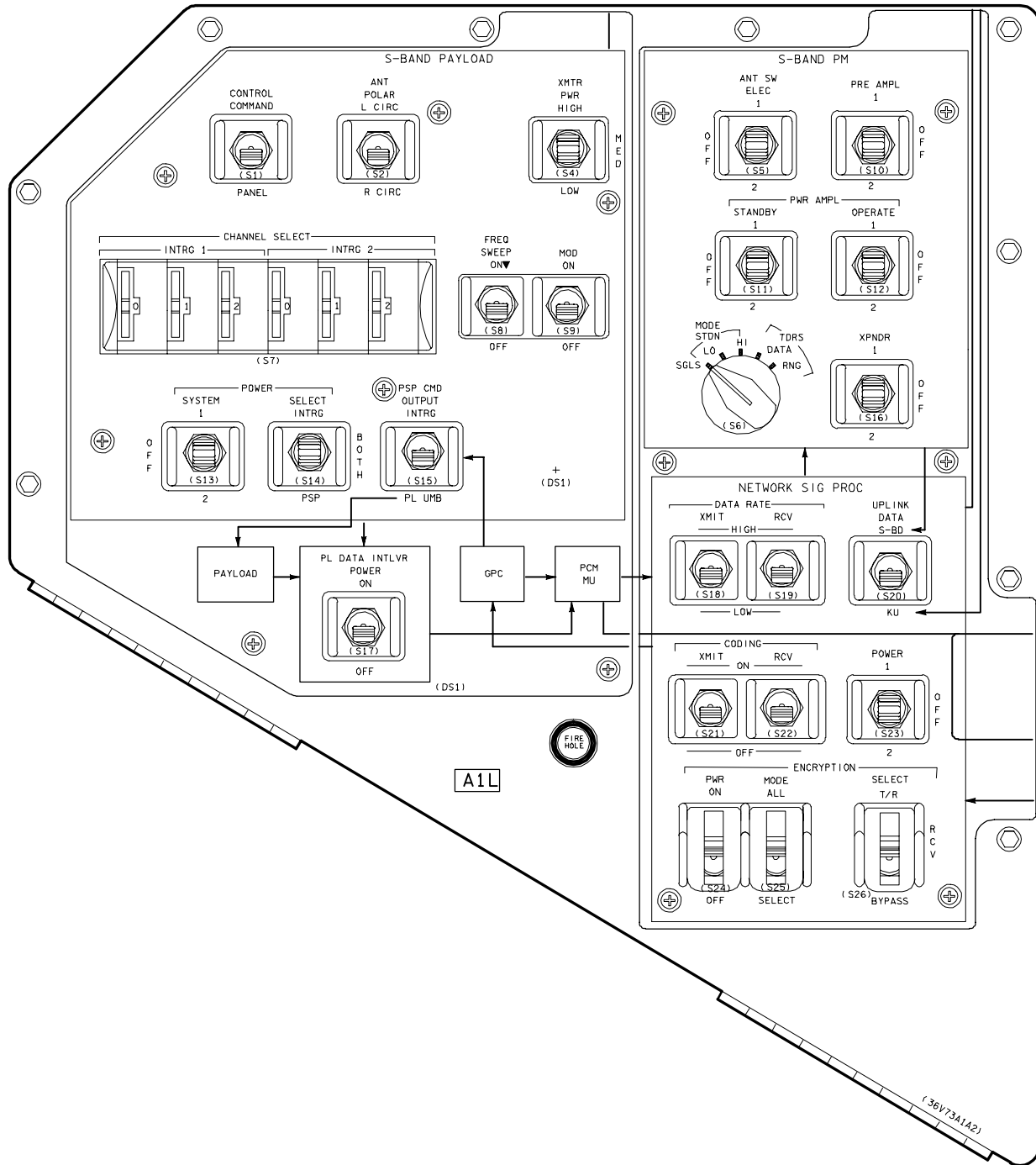
FREQ SWEEP (S8) - This is a momentary switch that is used to enable the transmitter sweep function. This function is active only while the switch is held down. This input goes through the GCIL to the PI.

MOD ON (S9) - This switch is used to enable the transmitter to place a modulated signal on the carrier. This input goes through the GCIL to the PI.

POWER, SYSTEM (S13) - This switch is used to select payload system 1 (PSP1/PI1) or payload system 2 (PSP2/PI2). This input goes through the GCIL to the PI.

POWER, SELECT (S14) - This switch is used to determine which payload system device(s) will be powered up, the PSP, the PI, or both. This input goes through the GCIL to the PI.

CONTROL (S1) - This switch is used to select either the SM command link or the A1L panel switch as the source controlling the PI (or actually the PL COMM system) via the GCIL.



186113402, PNL 1

Figure 31-2. Panel A1L

### 31.2.1.2 GPC SPEC 62, PCMMU/PL COMM Display

This onboard (Figure 31-3) display is used to determine the PI system status. These data fields show the last commanded channel selection, the phase lock and error

status, the interrogator transmit power, and the received payload signal strength in Systems Management (SM) OPS 2 and 4.

```

XXXX/062/          PCMMU/PL COMM  XX X DDD/HH: MM: SS
SM COM BUFF   XXX          DDD/HH: MM: SS
PCMMU
BITE WORD XXXX
FMT
SEL FXD      1XS
  PGM        2XS
PGM ID 64 XXX
      128 XXX
3 SEL ID   XXX
  LOAD 4 XXXX

I/O RESET
  PCM   5XX

-----
PSP          PL INTRG
I/O RESET   1 CHANNEL XXXS
  PSP1     6XX   2 CHANNEL XXXS
  PSP2     7XX   PHASE LOCK XXXS
SYNC BIT XXXS          ERR ±XXS
  FRAME XXXS   XMIT PWR XX.XXS
LOAD XXXX XXXX   PL SIG STR X.XXS 18 TFL GPC SEL X

PDI
I/O RESET 8XX
BITE WORD XXXX
9 SEL DECOM X
10 SEL FMT XXX
  LOAD 11 XXXX
12 SEL INPUT X
  LOAD 13
DECOM INPUT FMT
  1 X XXS
  2 X XXS
  3 X XXS
  4 X XXX
5-FPM
DECOM ENA
  FDA 1 14X
      2 15X
      3 16X
      4 17X

(XX)

```

186113403. CRT; 1

**Figure 31-3. SPEC 62, PCMMU/PL COMM display**

### 31.3 DESCRIPTION

A summary of the PI use/function is given below.

- A. Provides two-way communications with SGLS and STDN payloads.
- B. Receive-only mode for DSN channels.
- C. Automatic signal acquisition and tracking with false lock protection.
- D. Provides data transmission in the absence of received signals.
- E. Demodulates Phase Modulation (PM) signals received from SGLS or STDN/DSN payloads and provides these data to the Ku-band bent-pipe and payload station or PSP.



- F. PM modulates the S-band transmit carrier with data in either of the two modes.
- G. Provides commandable transmit sweep for DOD and NASA modes at two rates and two ranges.
- H. Provides three commandable power output levels (0 to 10 watts range)
  - 1. High power - 5.0 to 10.6 watts
  - 2. Medium power - 0.5 to 1.6 watts
  - 3. Low power - 2.5 to 7.9 milliwatts

The basic PI configuration is the same for both the SGLS and STDN modes, with the differences in frequency and step sizes set by commandable frequency counters in the synthesizer. The receive and transmit channels, which are noncoherent, are derived from an 80-MHz Temperature-Controlled Crystal Oscillator (TCXO). In the transmit path, Voltage-Controlled Crystal Oscillators (VCXO) provide the transmit sweep.

The receive function consists of S-band preamplification and down conversion to the first and second Intermediate Frequencies (IF) of 215 and 31 MHz, respectively. Each IF contains Automatic Gain Control (AGC) amplification and bandpass filtering. Receiver tuning is accomplished by varying the frequency of the Local Oscillator (LO) signal injected into the first mixer; a frequency synthesizer adjusts the LO frequency by external command. The second IF is part of a carrier tracking loop that is closed through a low pass (loop) filter, an 18.4-MHz VCXO, and a frequency multiplier (X10) to the second mixer. The receive function is completed by data demodulation in the wideband detector, followed by signal leveling and buffering at the output.

The transmit functions consist of PM of externally-received data onto a 320-MHz carrier followed by frequency multiplication (X4) to 1280 MHz and an up conversion to the S-band transmit channel. Broadband, low-level amplification then precedes separate power amplification to the requisite level for each service. A selection is made to route the S-band signal through the appropriate power amplifier for subsequent injection into the triplexer assembly.

Tuning for the receive and transmit functions is provided by two synthesizers. Each synthesizer is of conventional programmed frequency divider, phase-locked loop design. To implement transmit/receive frequency ratios, however, the reference for the transmit synthesizer is derived from the output of the receiver synthesizer. On the other hand, the latter may be viewed as independent since its reference is the signal from an 80-MHz TCXO. The transmit synthesizer does have an additional feature, namely, a precision frequency sweep capability. This is implemented with two sets of VCXOs and frequency multipliers with corresponding wide and narrow sweep.

The operational sequence starts with the reception of a new set of configuration commands by the command processor. The processor decodes these commands and, in turn, implements the selections in the triplexer, receiver, and power amplifier. The synthesizers are programmed so that the received and transmitted signals will conform

to the desired payload channels. The correct frequency is automatic because of the synthesizer implementations.

The transmitter signal carrier is frequency-modulated by the sweep function discussed above; a linear triangular frequency sweep is supplied to the carrier to enable signal acquisition at the payload. When the payload acquires the PI transmitted signal, the return signal from the payload will then exhibit the same frequency sweep by the turnaround ratio.

Although it is the sweeping payload return signal that the PI receiver must acquire, nonetheless, the receiver employs additional frequency sweeping for signal acquisition. Before acquisition, control logic causes the output frequency of the 18.4-MHz VCXO to be swept over a range that is wider than the total deviation of the received carrier frequency and at a much higher rate. The desired carrier frequency will then be within the loop capture range repeatedly each second. At one such occurrence, the receiver control logic will stop the receiver sweep and declare "signal lock." The receiver will then track the input signal, including the sweep from the transmitted PI signal. This latter sweep can be disabled manually.

### 31.3.1 Electrical

The PI comprises six boards:

- A. Triplexer assembly - Contains high- and low-band receive and transmit filters, associated Radio Frequency (RF) cables, and coaxial switches for S-band signal routing.
- B. Receiver - Provides signal acquisition and data demodulation of the incoming S-band signal.
- C. Synthesizer - Provides the first LO of the receiver which determines the receive channel. The S-band transmit frequency is also derived in the synthesizer, is provided with PM modulation, and then is supplied to the power amplifier.
- D. Power amplifier - Amplifies the signal and routes it to the appropriate port of the triplexer.
- E. Command processor - Reformats the commands and routes them to the appropriate assembly.
- F. Power converter - Provides isolated secondary power to the PI circuits.

#### 31.3.1.1 Triplexer

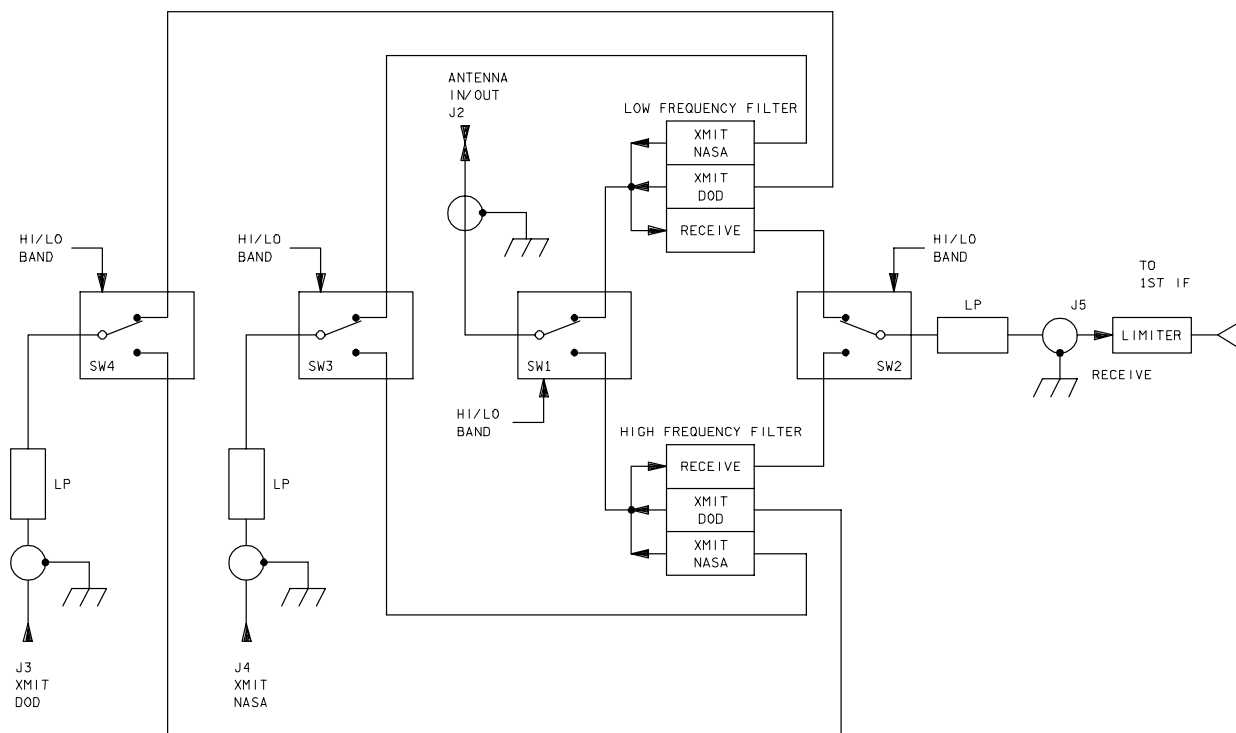
The triplexer assembly (Figure 31-4) consists of two triplexers, four identical switches, three identical low-pass filters, and associated interconnecting RF cables and dc wires.

Two triplexers will provide six filter channels designated as high/low frequency bands of NASA transmit, DOD transmit, and receive. Each filter channel uses high-Q combine

structures with an integrated cross-coupled notch network to provide optimum electrical characteristics. Selection of appropriate filter channel is provided by a switch matrix that is integrated into the triplexers without requiring external RF cables.

A low-pass filter structured with an alternating impedance is incorporated into three RF interfaces (NASA, DOD, and receive) to maintain high-stop band attenuation up to 16 GHz.

The diode board is the heart of all dc interfaces. It interfaces command signals to switch control leads and provides a set of monitoring circuits.



186113404. ART# 1

**Figure 31-4. PI triplexer**

### 31.3.1.2 Receiver

The receiver (Figure 31-5) is designed to search for and acquire S-band residual carrier at any frequency within the 2200 to 2300 MHz frequency range when provided with a first LO signal 215 MHz below the carrier. The receiver operates in either of two modes: NASA or DOD. In addition to the NASA or DOD mode, the receiver provides a baseband output for the Ku-band bent-pipe signal. After acquisition, the receiver performs the following functions:

- A. (NASA mode) Receive and coherently demodulate residual carrier signals consisting of a 1.024-MHz sinusoidal subcarrier, bi-phase or Non-Return-to-Zero

(NRZ) modulated. The outputs are provided to the PSP and to the Ku-Signal Processor (KuSP).

- B. (DOD mode) Receive and coherently demodulate residual carrier consisting of a 1.024-MHz sinusoidal subcarrier, bi-phase modulated and/or a 1.7-MHz sinusoidal subcarrier, Frequency Modulation/Frequency Multiplexing (FM/FM), or Pulse Code Modulation/Phase Shift Keying (PCM/PSK) modulated. The outputs are provided to the Payload Station Distribution Panel (PSDP) and the KuSP.
- C. Provide noncoherent amplitude leveling to the NASA, DOD, and Ku outputs.
- D. Accept mode commands from the command processor.
- E. Provide analog and digital telemetry outputs.

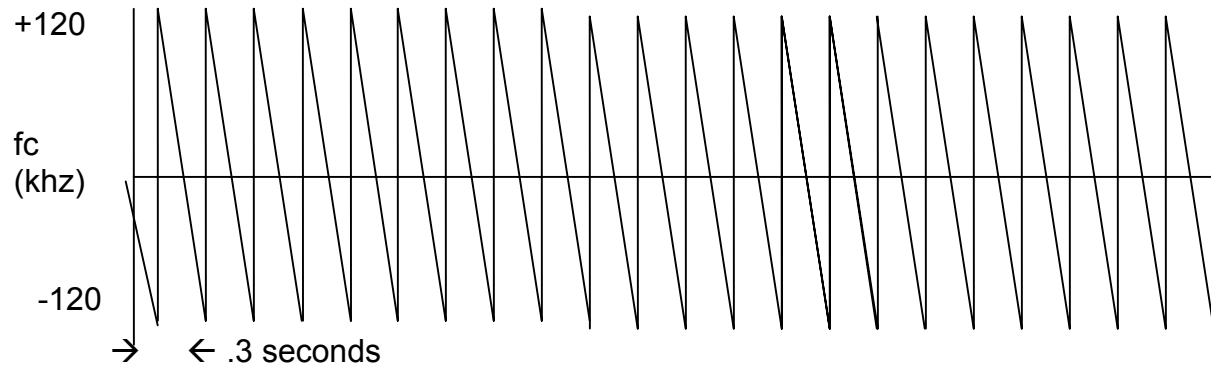
The receiver is configured as a short-loop, phase-lock loop receiver with double conversion, capable of receiving residual carrier PM signals. The receiver consists of a preamplifier and three modules (listed below and discussed in detail in the following paragraphs).

- A. Preamplifier/first IF module
- B. Second IF module
- C. Baseband module

Received S-band RF signals are amplified in a low noise (3.1 dB Noise Figure (NF), max.) hybrid Microwave Integrated Circuit (MIC) preamplifier, which includes an input limiter to protect the preamplifier to an RF input level of up to +36 dBm, and down converted to a first IF frequency of 215 MHz. Downconverted first IF signals are routed to an AGC amplifier, filtered through a five-pole Bandpass Filter (BPF), further amplified and filtered through two AGC amplifiers and five-pole BPF, and downconverted to the second IF frequency of 31 MHz. The second mixer is followed by a BPF with a 30-MHz bandwidth to reject second mixer spurious signals and a 31-MHz AGC IF amplifier. The output of this amplifier is fed to a three-pole BPF, with a bandwidth of 18.0 MHz, nominal 3 dB down, and onto a second 31-MHz AGC amplifier. The output of this circuit is the output of the first IF module and is coupled to the second IF module through a coaxial cable.

### 31.3.1.3 Receiver Operations

When you turn the PI on, the receiver will automatically start performing Frequency Sweeps “around the center frequency”. When the incoming signal breaks threshold level ( $> -117$  dbm) the PI RX should lock up within 0.4 second with a 90 percent probability. This is PI Phase Lock. Figure 31-5 displays the PI Receiver Sawtooth Sweep around the center frequency (fc).



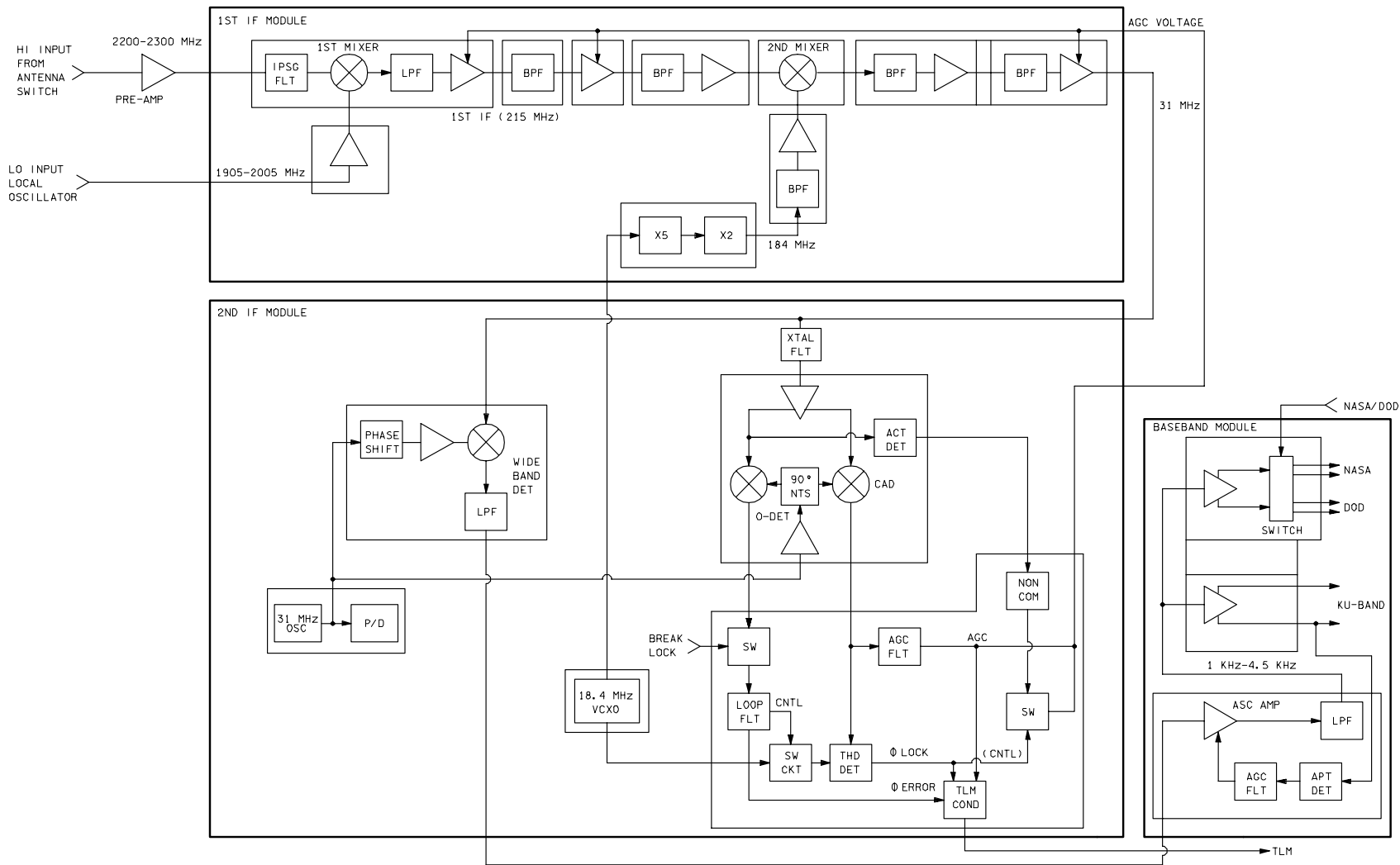
**Figure 31-5. PI Receiver Sweep Prior to Lock**

#### **31.3.1.4 Receiver Telemetry**

Phase Lock XXX – displays whether **PI Receiver** has locked; displays a “yes” or “no.”

ERR +\_XXs – Difference between the receive center frequency of channel and actual frequency received; units in kilohertz; actual frequency – channel frequency = phase error. This is a misnomer should be frequency error. Good indications of Doppler shifts (frequency will go up if going towards satellite and vice versa).

PL Signal Strength X.XXs – Signal Strength PI is receiving from the incoming Payload. Signal Strength can be used to watch range. (i.e., signal strength should increase, as range gets closer)



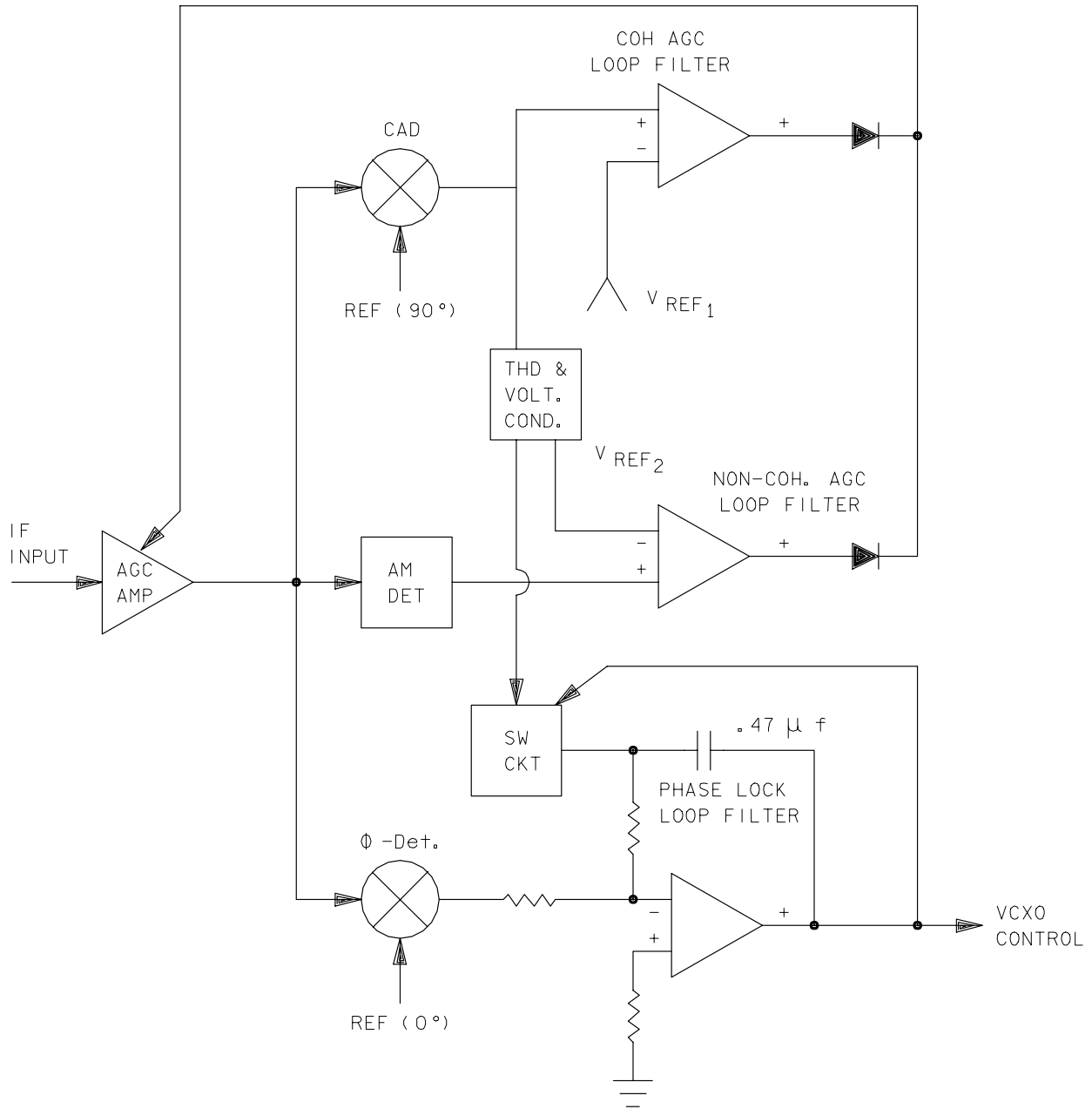
186113405, SCH# 1

Figure 31-6. Block diagram payload interrogator receiver

In the second IF module, the signal is divided between the phase-lock loop channel and the wideband data channel. The wideband data channel has a buffer amplifier to provide isolation between the two channels. The output of the buffer amplifier is then applied to the wideband detector, where phase demodulation occurs. The output of the wideband detector is buffered, low-pass filtered (12-MHz bandwidth, min.), and coupled to the second IF data output connector. The phase-lock loop channel has a crystal filter with a 300-KHz bandwidth. This bandwidth was selected to enable the noncoherent AGC (before acquisition) to maintain a constant IF gain throughout the VCXO sweep period. The output of the crystal filter is amplified and fed to the RF ports of the phase detector and Coherent Amplitude Detector (CAD). A reference signal at the second IF frequency (31 MHz) is applied to a 90° hybrid and applied in quadrature to the LO ports of the phase detector and CAD. The output of the phase detector, a 0 to 242-kHz difference in frequency signal before phase-lock and a dc error voltage after phase-lock is applied to a Field Effect Transistor (FET) switch for breaklock control, and the output of the switch is applied to the phase-lock loop filter. The output of the loop filter is used to control the frequency of the VCXO (18.4 MHz to 13.2 kHz) from which the second IF frequency is derived: 215 MHz (first IF) -  $18.4 \times 10$  MHz (VCXO x 10) at 31 MHz (second IF).

The CAD output signal is in quadrature with the phase detector; and, after acquisition of a dc voltage equivalent to the phase detector scale factor, the signal is present and is applied to the coherent AGC loop filter amplifier. A reference or delay voltage is also applied to the coherent AGC loop filter amplifier. When the coherent AGC loop is closed, the output of the CAD is maintained at the reference dc voltage. The output of the coherent AGC amplifier is summed with the noncoherent AGC control voltage through two diodes that form an automatic switch. See Figure 31-6 for a simplified block diagram of the switching of the AGCs. The AGC action is such that the AGC loop which requires the least IF gain to achieve balance takes control of the IF amplifiers. At tracking threshold, either AGC loops can be active. Above tracking threshold, the noncoherent AGC is active before acquisition, and the coherent AGC is active after acquisition.

The phase-lock board receives inputs from the phase detector and CAD board. Prior to RF signal acquisition, the noncoherent AGC filter, driven by the Amplitude Modulation (AM) detector, controls the AGC voltage supplied to the first IF module AGC amplifiers. The sweep circuit drives the VCXO control line, causing the VCXO to sweep through its frequency range. At signal acquisition, the CAD output trips the threshold detector, which, in turn, stops the sweep circuit, enabling the phase detector output to drive the loop filter and control the VCXO frequency. The threshold detector also switches the AGC control voltage from the noncoherent to coherent AGC filter. Telemetry conditioners monitor the loop stress and receiver AGC as well as provide indications of receiver phaselock and AGC meter functions. The break-lock command opens the loop by disconnecting the loop filter input when activated.



0979. ART; 2

**Figure 31-7. AGC amplifier, detectors, loop filters, and threshold detector simplified diagram**



The output of the CAD is also applied to a low-pass filter and a threshold detector. The low-pass filter sets the VCXO sweep delay voltage (50 to 90 ms), and the threshold detector provides the required information for the phase-lock telemetry and the sweep circuits. The noncoherent AGC is derived from the output of the amplifier just ahead of the phase detector and CAD. A zero-bias Schottky diode is used to detect the RF signal, and the resultant dc voltage is applied to a loop filter similar to the coherent AGC loop filter. The output of the noncoherent AGC loop filter is summed with the coherent AGC control voltage, as mentioned above, and the resultant dc voltage is used to control the gain of the IF amplifiers, thus closing the AGC loop.

The output of the data channel of the second IF module is coupled to the baseband module through a coaxial cable. A noncoherent AGC with over 50 dB dynamic range is provided in the baseband module to maintain a constant output at the NASA/DOD and Ku-band output. This noncoherent AGC is implemented with FETs as voltage variable resistors and a matched pair of Schottky diodes. One diode is used as an AM detector and the other as part of a temperature tracking reference voltage source. The output of the detector is applied to an active loop filter, and the output of the loop filter is used to control the resistance of the two FETs, closing the AGC loop. The AGC loop bandwidth is greater than 1 Hz and less than 100 Hz.

The input to the AM detector is also fed to two video amplifiers. One of the two amplifiers is provided for the Ku-band channel and drives a differential power amplifier. This channel is always enabled. The other video amplifier drives an identical differential power amplifier for PSP and DOD outputs. The PSP or DOD output is selected by a miniature latch relay. A minimum isolation of 40 dB between the switched baseband outputs is maintained to 15 MHz.

### 31.3.1.5 Synthesizer

The synthesizer simultaneously generates two noncoherent S-band signals, one a Command Word (CW) frequency in one of 861 channels between 1985 MHz and 2085.875 MHz to be used as the first Local Oscillator (RxLO) signal in the first downconverter of the PI receiver. The other is a phase-modulated signal in one of 861 channels between 1763.720714 MHz and 2119.792438 MHz to be applied to the PI Transmitter (Tx) as the forward link signal. The RxLO signal is 215 MHz below the expected received frequency. The two signals are generated in such a way that the turnaround ratio between the received frequency and the transmitted frequency will be approximately 256/205 in the SGLS frequency mode and 240/221 in the STDN/DSN frequency modes. The capability is provided to sweep the transmitter carrier frequency over two ranges (33 kHz or 75 kHz).

The transmitter carrier may be phase-modulated at a present modulation index of 1 rad peak by a 16 kHz PSK modulated subcarrier in the PSP DATA or at a variable modulation index between 0.3 and 2.4 rad peak by a Frequency Shift Keying (FSK)/AM sequentially-generated tones of 65 kHz, 76 kHz, and 95 kHz in the DOD DATA mode. The modulation mode selection and the modulation inhibit commands will be received

as Complementary Metal-Oxide Semiconductor (CMOS)-compatible commands from the command processor.

The 861 frequency channels required are generated through the use of phase-locked loops that have programmable dividers in the feedback circuit. The basic theory is that a highly stable reference oscillator is divided down to represent the minimum frequency step between channels. This is presented to the reference input of a phase detector. The other phase detector input is from a Voltage-Controlled Oscillator (VCO) that has been downconverted to a convenient IF frequency and then divided by N (Table 31-1), a number that represents the desired channels of operation. The phase detector drives the loop filter which controls the VCO frequency until phase coherence is achieved, thus the phase-locked loop. When divider N (Table 31-1) is reprogrammed, the frequency changes to the newly programmed channel. The VCO output may then be upconverted to the desired output frequency.

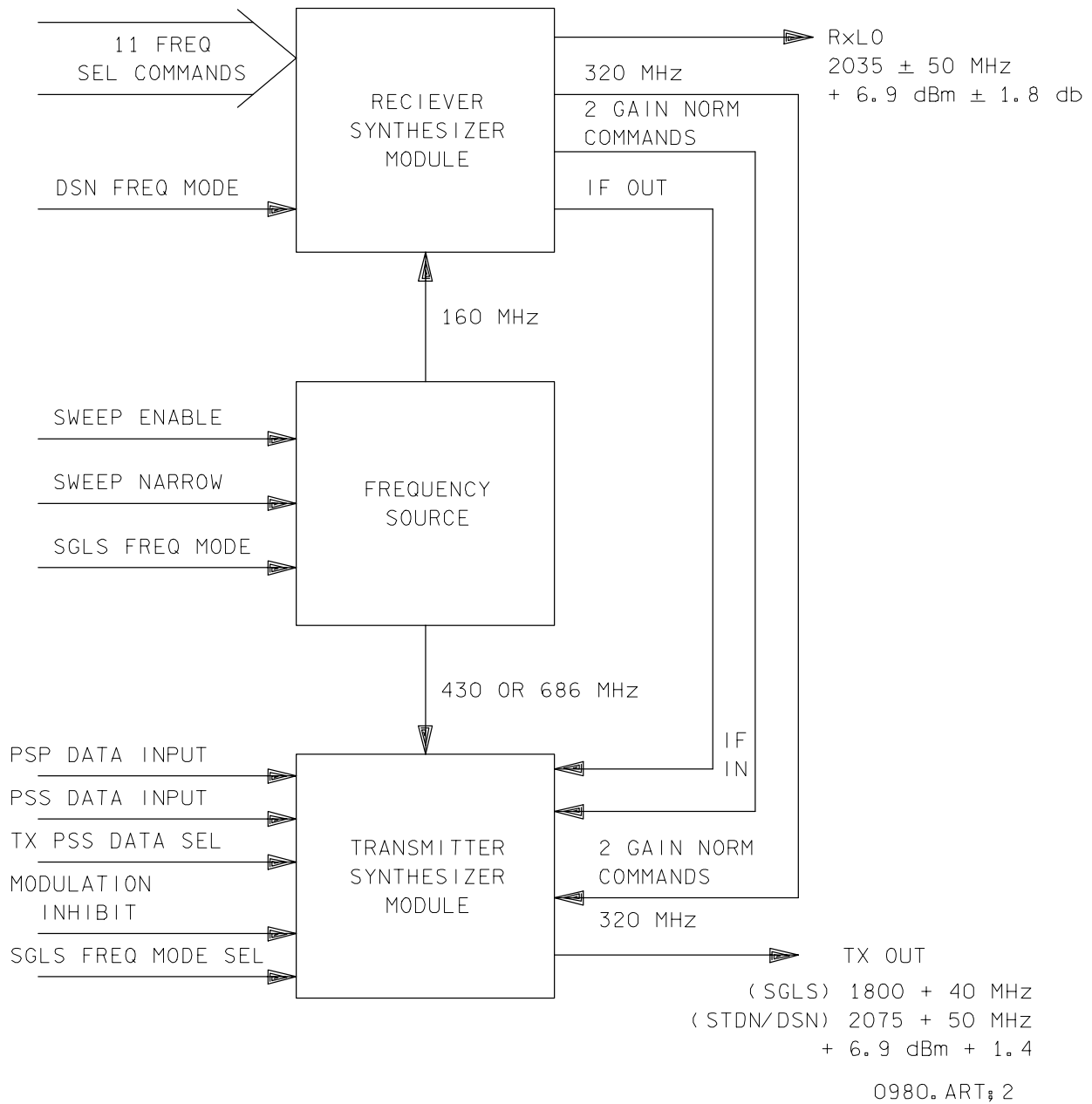
The PI synthesizer uses this type of phase-locked loop to generate the receiver first LO signal. It then uses a second phase-locked loop in a similar configuration to generate the transmitter signal. Table 31-1 presents a review of the frequency channel allocation.

The transmitter output frequency plan is determined by the receiver plan by using a sample of the receiver synthesizer IF frequency and modifying this signal by the turnaround ratio. By controlling the programming on the dividers E and F which control the turnaround ratio and by selecting the proper offset oscillator and then upconverting with the phase-modulated upconversion signal, all transmitter frequency channels are achieved.

The transmitter frequency sweep capability is provided by sweeping the VCXOs that generate the offset frequency.

The synthesizer is divided into three modules as described in the functional block diagram in Figure 31-9. The source module contains the three crystal oscillators, frequency multipliers, and sweep control circuits required to create the very stable 80-MHz reference frequency, and the Tx loop offset frequency which has 0.33- or 75-kHz sweep capability. The Tx offset frequency is switched between 430 and 686 MHz as selected by the command processor.

The receiver synthesizer module contains the 755 to 50 MHz phase-lock synthesizer, the upconverter, and the frequency multipliers necessary to generate the 861 channels of receiver LO signal in the 1985 to 2085 MHz frequency range, all coherently related to the 80-MHz reference oscillator. The channel selection is controlled by 11 binary commands received from the command processor. The receiver synthesizer module also supplies to the transmitter synthesizer module two signals which are coherently related to the 80-MHz reference oscillator, a 320-MHz signal and an IF signal which is a downconverted sample of the receiver LO signal.



**Figure 31-8. Synthesizer functional block diagram**

The transmitter synthesizer module provides the phase-locked synthesizer that, when upconverted, provides the phase-modulated transmitter signal that is delivered to the LRU output through the power amplifier and triplexer. The receiver synthesizer IF signal is used to control the transmitter synthesizer but is modified by the turnaround ratio of either 256/205 or 240/221, as determined by the command processor inputs. The transmitter offset frequency from the source module in conjunction with the selection of the 520 (40 MHz VCO) or the 795 (50 MHz VCO) determines whether the transmitter output will be at 1800 (40 MHz in the SGLS frequency mode) or 2075 (50 MHz in the STDN/DSN frequency modes). The transmitter synthesizer module also contains the frequency multipliers, upconverter, linear phase modulators, and data control circuits to produce the output signal.

The source module provides the three highly stable frequencies used by the receiver synthesizer and transmitter synthesizer modules. The 160-MHz reference output is used continuously in the receiver synthesizer module as the reference frequency in the phase-locked loop to generate the receiver LO signal in any one of the 861 channels between 1985 and 2087.1 MHz. The high stability ( $\leq \pm 10$  parts per million (ppm)) of this signal is necessary to limit the acquisition range requirement of the receiver. The offset source output is either a 685.979166-MHz signal in the STDN and DSN frequency modes or 429.667967 MHz in the SGLS frequency mode. This offset frequency is used in the downconverter of the phase-locked loop of the transmitter synthesizer and provides the fixed frequency necessary to establish the 256/205 (SGLS frequency mode) or the 240/221 (STDN/DSN frequency mode) turnaround ratio. This offset frequency has a swept capability, thus providing the transmitter output with its required sweep range. The high stability requirements of the transmitter output ( $\leq \pm 12$  ppm) place strict stability requirements on these VCXOs ( $\leq \pm 15$  ppm).

### 31.3.1.6 PI Transmitter Operations

Commands, which manipulate GCIL drivers, will configure the PI Transmitter to output a signal necessary for a deployed Satellite to acquire. The following commands are available to Flight Controllers to configure the PI Transmitter.

**PI Channel:** Designates the Transmitter and Receiver Center Frequencies.

**Transmitter Power:** Commands to output Transmitter Power at Low  $\sim .007$  W,  $\sim 1.6$  W Med, or 10 W High Power.

**Sweep On:** Sweep the Transmitter Frequency through its triangular pattern around its center frequency.

**Sweep Off:** Secures Transmitter Frequency Sweep, places frequency back at center.

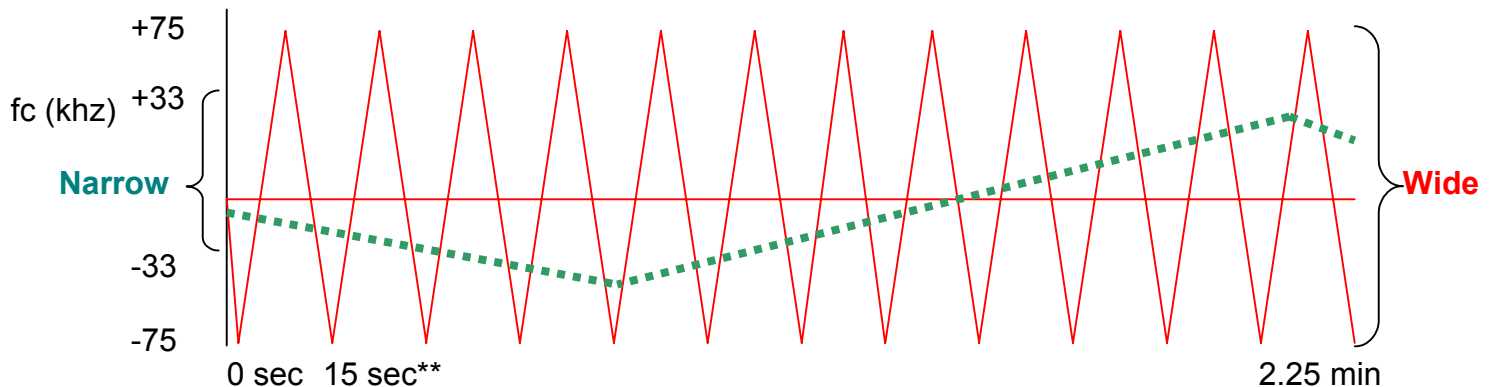
**Sweep Wide:** Establishes the Transmitter Sweep to be  $\pm 75$ khz at a 10khz/sec rate.

**Sweep Narrow:** Establishes the Transmitter Sweep to be  $\pm 33\text{kHz}$  at a  $.25\text{kHz/sec}$  rate

**Modulation On:** (1) Allows commands to be modulated on the transmitter carrier.  
(2) Applying modulation to the carrier subtracts 6dbm of RF energy output.

**Modulation Off:** (1) Turns off modulation from the transmitter carrier.  
(2) Removing modulation from the carrier adds 6dbm of RF energy output.

With PI Transmitter Sweep On, The Transmitter can sweep Wide or Narrow. Figure 31-7 compares the Wide and Narrow the PI Transmitter Triangular Sweep Patterns.



**Figure 31-9. PI Transmitter Sweeps**

### 31.3.1.7 Power Amplifier

The power amplifier receives the transmitter synthesizer output signal in either of two frequency bands, 1760 to 1840 MHz in the SGLS frequency mode or 2025 to 2125 MHz in the STDN/DSN frequency mode at a level of +6 dBm, and supplies the gain necessary to overcome the losses in the triplexer and interconnecting circuitry to provide three PI output levels of 5 to 10 W, 0.5 to 1.6 W, and 2.5 to 7.9 mW. To meet these requirements, the power amplifier must provide output levels of 10.5 to 22.4 W in the high power mode, 1.05 to 2.24 W in the medium power mode, and 5.2 to 11.2 mW in the low power mode. A block diagram is given in Figure 31-10.

This solid state amplifier is actually a dual power amplifier combined into one package. Once the input is received in a common preamplifier, it is switched to either the STDN/DSN driver and final amplifier or the SGLS driver and final amplifier. This switch is done to conserve dc power as the efficiency of an amplifier covering only one band (-80 MHz) can be as high as 50 percent.

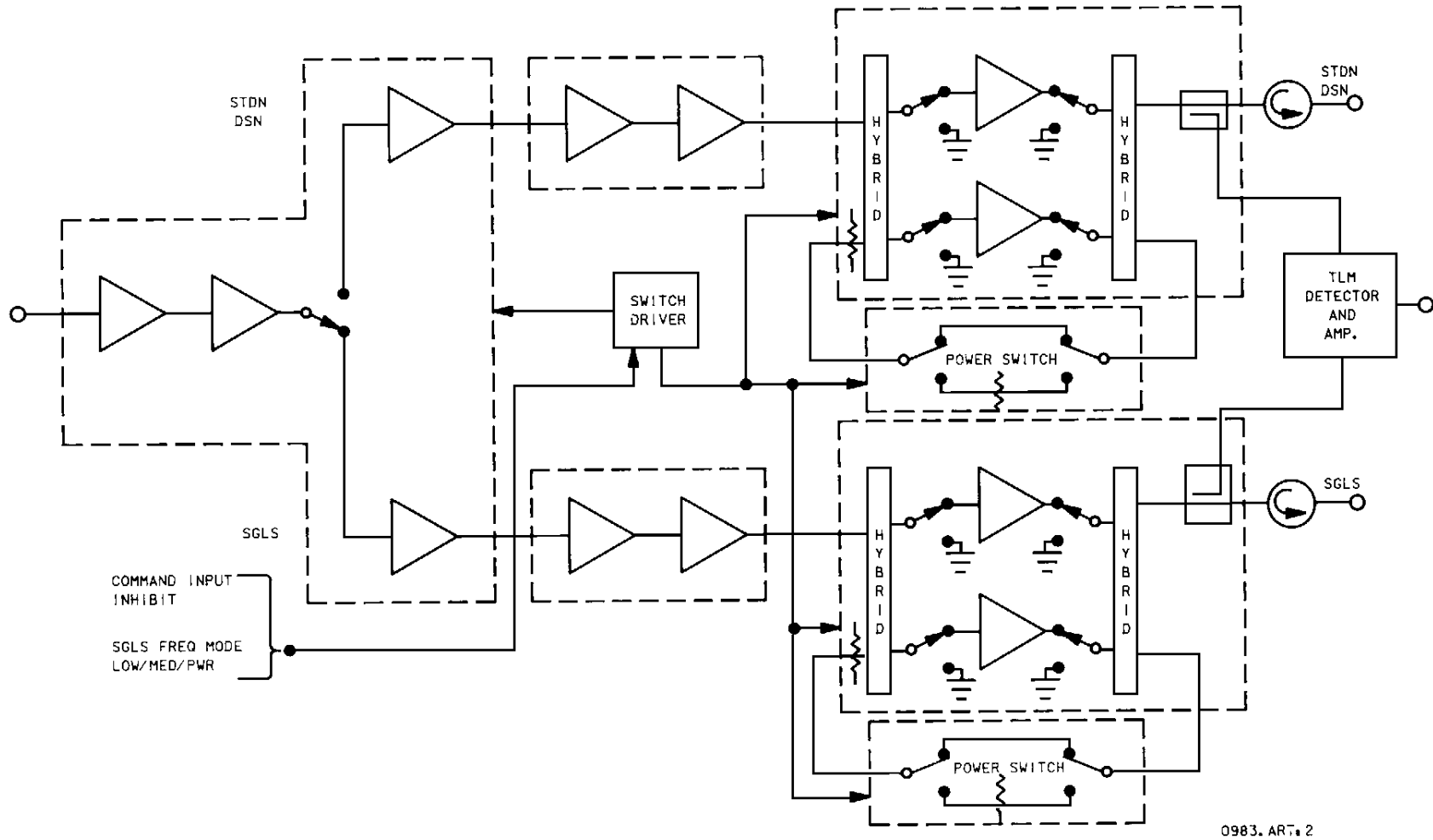


Figure 31-10. PI transmitter power amplifier block diagram

The power amplifier is mounted on the floor of the housing in order to use the very best possible thermal interface to the coldplate. Maximizing the heat dissipation is required because the power amplifier dissipates 63.7 W of dc energy in a footprint area of 55 in<sup>2</sup> while generating 15 W of RF energy.

In general, distributed microstrip design techniques are used. The microstrip is duroid fiberglass-loaded Teflon RF circuit board material. Both distributed and lumped components are used. Where possible, the duroid is soldered onto carrier plates and screwed into the housing, but in the case of the final amplifiers this technique provides excessively long ground paths; thus, the duroid is soldered directly to the housing. A Printed Circuit (PC) board is used for the low-frequency components.

The input signal is first amplified in the wideband preamplifier subassembly. The first two stages, as seen in the power amplifier block diagram, Figure 31-10, are wideband amplifiers in a common emitter configuration. These are class A stages with the first stage providing 6 dB gain while establishing the input characteristics, such as input impedance (50 ohms, Voltage Standing Wave Ratio (VSWR) <2.0:1) and carrier-to-noise ratio for the far outphase noise of -155 dBm/Hz. This requires an equivalent NF of 19 dB. The second stage is operated slightly into compression providing 5 dB of gain. It has been carefully designed to remain in stable operation under any load condition because the Positive-Intrinsic-Negative (PIN) diode switch and inhibit switch can provide a short to its output.

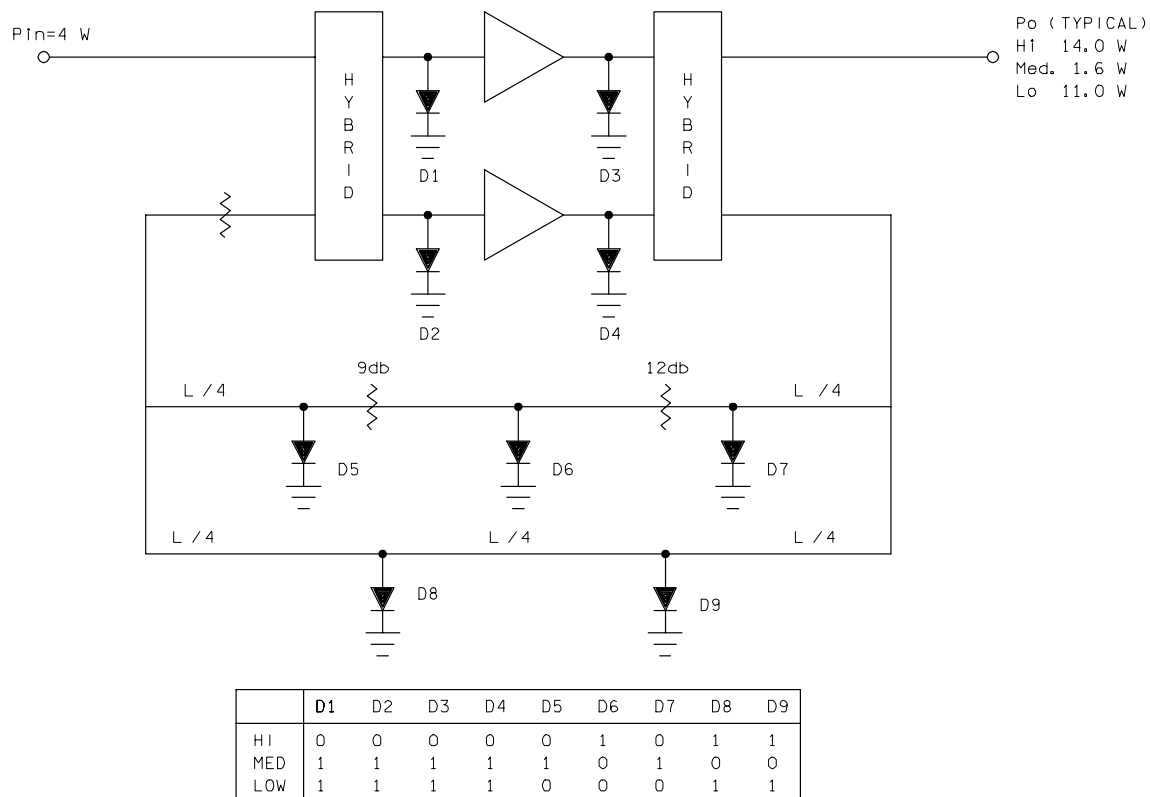
The PIN diode switch provides two shunt-switching diodes that select either the SGLS driver amplifier or the STDN/DSN driver amplifier. In the inhibit mode both of the diodes are shorted by commands received from the telemetry amplifier and switch subassembly. These diodes are controlled by supplying a 15-MHz forward-biasing current from the telemetry amplifier and switch control board. From this point on, the design is the same, only components differ because of the differences in frequency of each mode.

The next stage provides 8 dB of gain and is biased class AB. It ensures that there is sufficient signal under any condition to drive the transistors in the first driver stage by providing a minimum output of 23.8 dBm and up to 25.3 dBm.

The driver stages for the SGLS mode and for the STDN/DSN mode were selected for use because they provide excellent power amplifier characteristics, such as high output power (8 W), high gain (to 8 dB), high thermal dissipation (to 12 W) and  $\theta$  Junction Capacitance (JC) (8.5° C/W), and high efficiency (50 percent). They are internally matched devices which simplify the requirements on output matching circuits, thus providing the small size capability of the power amplifier. The 6-W (-6) parts are mounted on the housing to provide the best heat sinking, whereas the 1-W (-1) parts are mounted on an extra thick carrier plate along with the two circuit boards (drivers A and B) that contain the distributed input and output matching for the -1 parts and the input matching for the 6-W parts. The output matching for the 6-W transistor is on a separate circuit board (driver C) mounted on its own carrier plate. Both the 1-W and 6-W stages are class C common base amplifiers. The -1 stages provide 6 dB of gain

and the -6 stages provide 6 dB of gain. They are both saturated stages which provide compression to the input signal. The output of the driver amplifier at 4 W drives the power switching/final amplifier assemblies.

The key element to the power switching assembly is the hybrid couplers found on the input and output of the final amplifier. Figure 31-11 shows a detailed drawing of the power switching technique. These hybrids serve a dual purpose: They power-split and combine the RF energy between the two final amplifiers, and they also combine any reflected or mismatched power from these amplifiers and transmit it to the fourth hybrid port to be dissipated in a load.



0979. ART; 2

**Figure 31-11. Power switching block diagram reflective hybrid switching matrix**

Medium power is generated by channeling power from the driver through the input branch line coupler (power is reflected out of input coupler port 2 by forward-biasing diodes D1 and D2), through the path containing the reverse biased diodes D8 and D9, then through the output branch line coupler (port 4 to port 3). Power does not flow through the path containing the attenuators because diodes D5 and D7 are conducting. Low-power output is obtained similarly to the medium power mode except the RF signal is channeled through the path containing attenuators. Isolation through the medium power path is achieved by forward-biasing diodes D8 and D9, which are separated by a quarter wavelength. Measurements have shown an isolation of approximately -45 dB,



thereby ensuring that the low-power output is predominantly flowing through the path containing the attenuators. This power-dividing scheme enhances power conservation since the final amplifiers are not operating during medium- or low-power levels. Contained in Figure 31-12 is the truth table, showing the condition of each diode during different transmitter power levels.

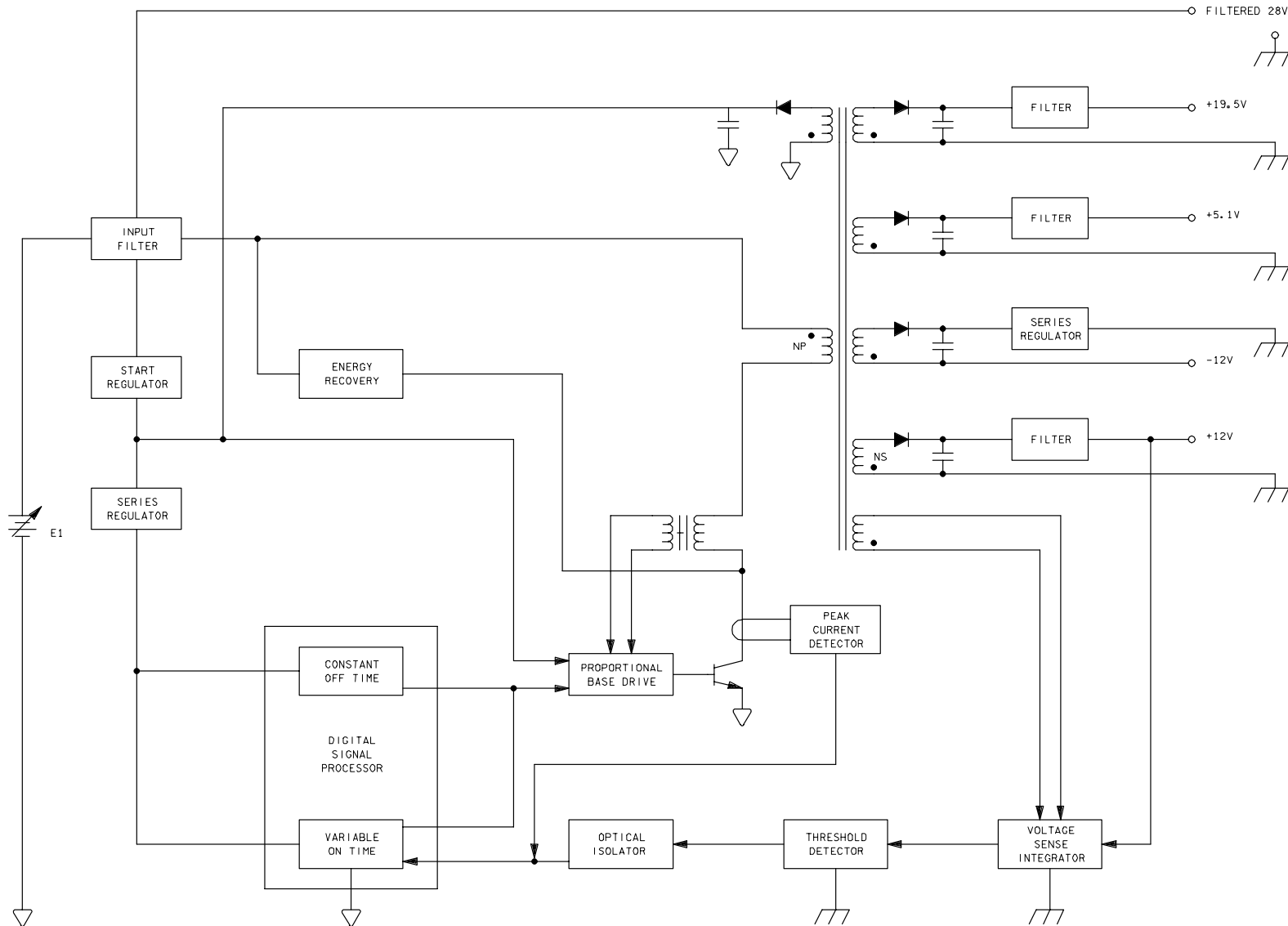
The power switch subassembly is composed of attenuators and diodes located at  $g/4$  intervals on the transmission lines. Some minor impedance matching is done on this board but only to tune out the stray lead inductance created while mounting the diodes and attenuators. Control of the diodes comes from the telemetry amplifier and switch control board by either supplying a back bias voltage or a forward current of about 15 ma.

In the case of the high-power mode the diodes on the input and output of the final amplifier are reverse biased. Now the hybrids act as normal power splitters and combiners. The high-power final amplifier stages each receive 2 W at the amplifier input in the SGLS frequency mode. These amplifiers are common base, class C type. They each provide 5.75 dB of gain and a power level of +39 dBm so that when each amplifier is combined, it provides 16 W of power. Output power adjustment is accomplished through the control of series resistance in the 19.5-V collector voltage line. The final amplifier circuit boards, containing the hybrid coupler, diodes, and input and output matching (final amp A and B) are soldered into the housing. This was done to provide the best possible circuit grounds with the shortest path length to this high-power, high-current stage.

The final amplifier output is fed through the unattenuated port of a directional coupler to a ferrite isolator for the SGLS frequency mode and an isolator in the STDN/DSN frequency mode. These isolators provide 20 dB of isolation to output mismatch, thus the power amplifier may operate safely into any load including a short or an open. The isolators establish the output impedance of the power amplifier (50 ohms VSWR 1.25:1).

Telemetry data are derived by detecting each power amplifier output and then conditioning the signal into a differential, balanced output that will be calibrated to indicate the power levels of medium- and high-power modes. The RF sampling is done with a 20 dB parallel line directional coupler. This type coupler has better than 15 dB directivity and a relatively flat response. A Schottky diode is used as a negative voltage detector. The detector output is fed to an amplifier comprised of two operational amplifiers. Calibration curves on each detector output are provided for each power amplifier.

The telemetry amplifier and switch control board receives all of the commands for the power amplifier and processes them to provide the required control function. The high-, medium-, and low-power commands, the inhibit command, and the SGLS frequency mode command come from the command processor as Transistor-Transistor-Logic (TTL) type signals. These commands are buffered and fed to switch drivers which set the current to the switches.



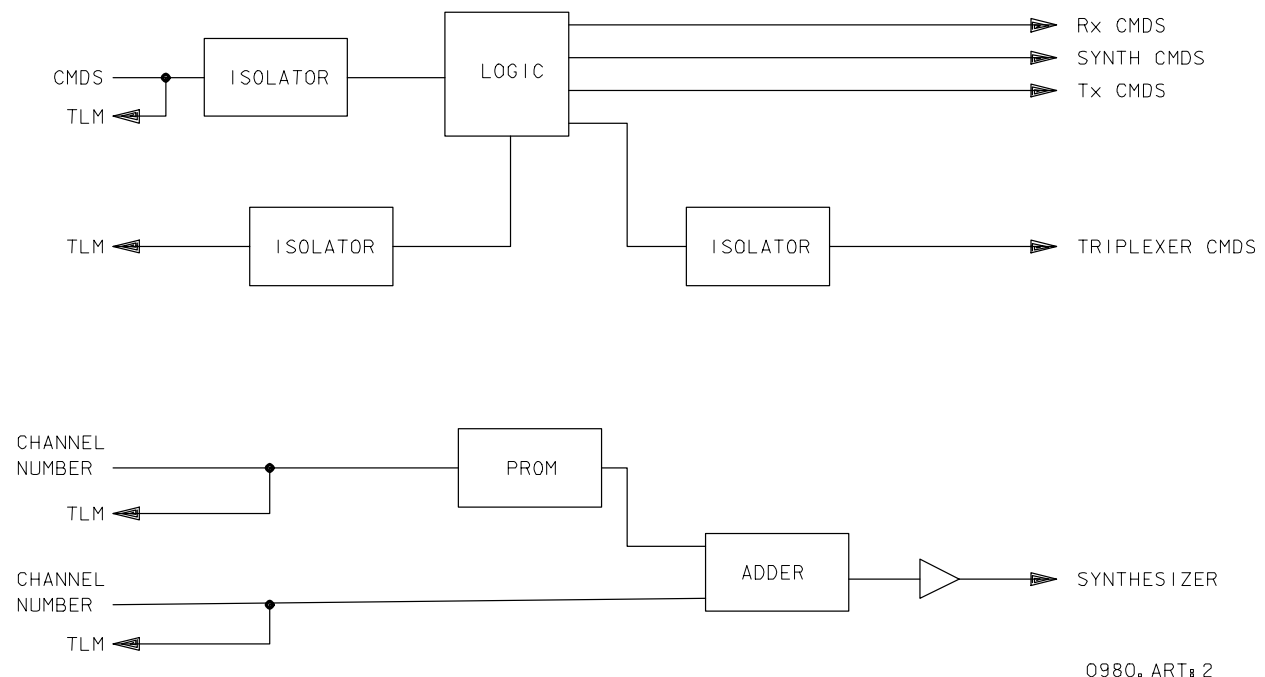
0982. ART. 1

Figure 31-12. Power converter block diagram

The inhibit circuit is activated when a command is received on the inhibit line or when a power mode is changed. This activation is done so that the RF will be removed from the PIN switching diodes during the switching transition. This removal prevents large signal levels from damaging them while they are in the medium resistance state. This inhibit is created on the telemetry amp and switch control board by having digital gates activated through Resistance-Capacitance (RC) time constants. The inhibit pulse comes on immediately after the receipt of a power switch command and remains on for 100 ms, during which time the diodes are switched and all transients settle down.

### 31.3.1.8 Command Processor

The command processor receives discrete +28 V dc mode, control, and frequency control commands from the display and control panel or from the ground. These commands are decoded for use by the receiver, transmitter, triplexer, and the synthesizer (Figure 31-13). Discrete 28 V dc status telemetry indicating the mode status and frequency selected is transmitted to an OI MDM for downlink to the ground.



**Figure 31-13. Command processor block diagram**

### 31.3.1.9 Power Converter

Raw dc bus voltage powers the converter (Figure 31-10) through two Electromagnetic Interference (EMI) filters, a common mode rejection transformer, and a two-stage, Low-Pass Inductance Capacitance (LC) filter prior to the power transistor switch. The principal purpose of the filters is to control the amplitude and frequency content of the power transistor switching current waveform to an acceptable level at the input terminals of the converter.

The buckboost converter is the power-handling portion of the converter. It basically contains an energy storage transformer, a power transistor, output diodes, and filters. The transistor is used as an electronic switch and is cyclically turned on and off by the control of the digital signal processor. Energy is stored inductively in the transformer core when the power switch is turned on.

When the power switch is turned off, the stored energy is delivered to the load through power diodes and output filters. With feedback control of the power transistor timing, the output voltage across the load can be kept constant despite input line or load changes.

A current transformer with positive feedback from a one-turn winding in series with the power transistor collector causes the base current to be sustained at a current proportional to the turns ratio of the base and collector windings. The transistor continues conducting until a large reverse polarity pulse from the drive circuit turns the power transistor off. This pulse also resets the drive transformer until the next drive pulse arrives.

The energy recovery network is used to return flyback energy to the input to improve converter efficiency. Additionally, it reduces stress of the power transistor by eliminating high-transistor current resulting from the recovery of the diode during transistor turn on. Also, the voltage spike appearing on the collector of the transistor is reduced.

A current transformer with a single-turn primary and 240-turn secondary develops secondary voltage across a fixed resistor proportional to the collector current of the power transistor. The fixed resistor is selected so that a preset peak current will develop a signal and cause the digital signal processor to turn off the power transistor early. The ON time is thereby shortened and less energy is transferred to the secondary circuits causing the output voltage to drop.

A summing junction at the input of the integrator sums together a dc error voltage from the +12 V output and an ac voltage proportional to the main bus voltage. The later signal provides a second feedback loop with wider bandwidth than the dc feedback loop, resulting in vastly improved response to input voltage transients, ripple, and noise.

A precision dc reference Zener is used to establish a precise switchover point for the threshold detector and a reference for dc error input of the integrator.

The ON time is set to be approximately equal to the constant OFF time with 28 V input bus voltage; i.e., 50 percent duty cycle. When the input voltage increases to 32 V dc, for example, increased ac feedback voltage into the integrator increases the slope of the integrator output ramp, and so the time required to trigger the threshold detection is shortened. The ON time is thereby decreased. The net result of this is to maintain the volt/second product constant on the primary side of the power transformer. The same volt/second product is maintained on the secondary side; however, the output voltage is also maintained constant by the dc regulation loop.

The digital signal processor provides a constant OFF time and a variable ON time signal to the power transistor proportional drive circuitry. The ON time has a maximum limit set by the digital signal processor. The ON time is variable up to the maximum limit and is controlled by the threshold detector, thus providing the proper timing ratio to maintain converter regulation.

### **31.3.2 Power**

Power requirements are 97.9 W.

### **31.3.3 Mechanical**

Weight is 45.5 pounds.

### **31.3.4 Software**

Not applicable.

## **31.4 INSTALLATION**

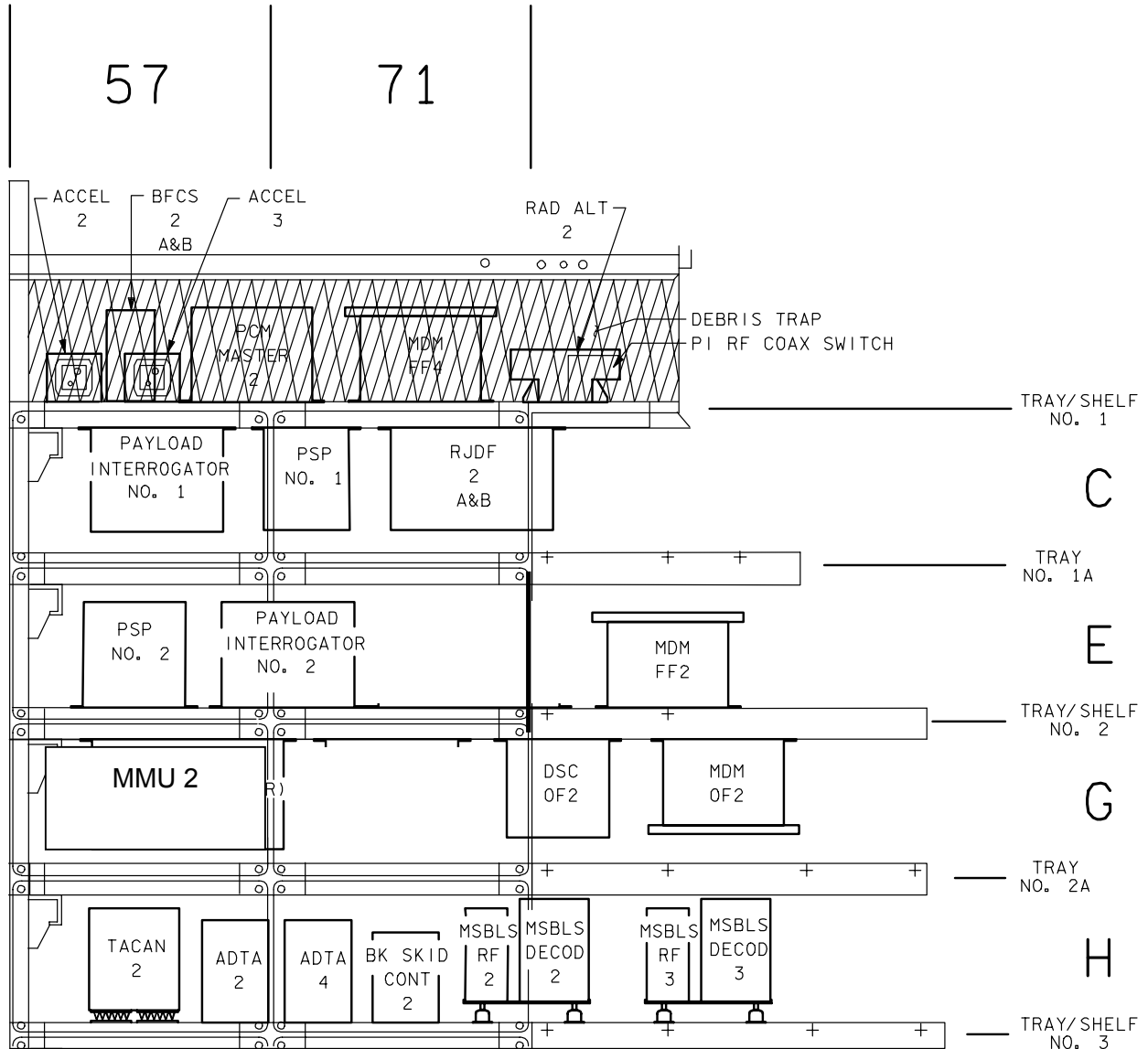
### **31.4.1 Location**

The PIs are located in avionics bay 2 (Figure 31-14).

### **31.4.2 Temperature**

Operating temperature range = -20° to 120° F.

Coolant source = water loop.



1599. ART: 2

**Figure 31-14. AV bay layout**

### 31.5 DESCRIPTION OF OPERATION

The crew controls and ground commands required to operate the PI are in Table 31-2.

#### 31.5.1 Example of Flight Controller commands for PI Receiver Lock:

PI Channel Select: ex. Channel 701  
PI Antenna Polarization ex. LHCP  
PL PSP/INTGR – SEL  
PL SYSTEM 1 (2) – ON ex. PL System 1 ON  
PSP 1(2) I/O ENABLE ex PSP 1 I/O ENA

The Flight Controller will check his telemetry, until **PI Lock** is observed.

#### 31.5.2 Example of Flight Controller commands for PI Transmitter Lock:

PI Channel Select: ex. Channel 701  
PI Xmitter Power Out ex LOW  
PI Ant Polarity ex. Left Hand Circ  
PI Xmit Sweep Wide/Nar ex. PI Xmit Sweep Wide  
PL PSP/INTGR – SEL ex. PL PSP/INTGR - SEL  
PL SYSTEM 1 (2) – ON ex. PL System 1 ON  
PSP 1(2) I/O ENABLE ex PSP 1 I/O ENA  
PI MOD – OFF ex. PL MOD ON  
PI FREQ SWP – ON ex. PL SWP ON (45 sec)  
PI FREQ SWP – OFF ex. PL SWP OFF

Have Payload Customer verify Satellite has acquired PI Transmitter carrier signal.

PL MOD – ON ex. PL MOD ON

Once Modulation is on, the Flight Controller can successfully send commands to the deployable satellite.

#### 31.5.3 Telemetry

The telemetry required to monitor crew control and ground commands is also included in Table 31-2. Additional telemetry points are listed below.

| MSID      | Title                           |
|-----------|---------------------------------|
| V74E5625A | S-band P/L 1 INTGR RF power out |
| V74E5626A | S-band P/L 2 INTGR RF power out |
| V74X5627E | S-band P/L 1 INTGR phase lock   |
| V74X5628E | S-band P/L 2 INTGR phase lock   |
| V74B5655A | S-band P/L 1 INTGR loop stress  |
| V74E5658A | S-band P/L 1 INTGR AGC          |
| V74E5659A | S-band P/L 2 INTGR AGC          |
| V74B5656A | S-band P/L 2 INTGR loop stress  |

Analog-telemetry monitors are provided for AGC signal strength and for loop stress. Signal-strength telemetry is derived from the second IF coherent AGC control voltages. The coherent AGC is dynamic for signal input levels ranging from threshold to -30 dBm.

Loop-stress telemetry is derived from the VCXO control voltage. The VCXO control voltage is amplified and buffered to form this output.

Receiver-lock telemetry is provided to indicate whether or not the receiver has acquired an input RF signal.

### 31.6 SPECIAL TELEMETRY COMPUTATIONS

MOIG3205C PI channel number

#### A. Telemetry input

##### 1. For Units (U) digit

A1 = PI 1 V74X5629E = A1  
A2 = PI 2 V74X5630E = A2  
V74X5631E = A3  
V74X5632E = A4  
V74X5633E = A5  
V74X5634E = A6  
V74X5635E = A7  
V74X5636E = A8

##### 2. For Tens (T) digit

B1 = PI 1 V74X5637E = B1  
B2 = PI 2 V74X5638E = B2  
V74X5639E = B3  
V74X5640E = B4  
V74X5641E = B5  
V74X5642E = B6  
V74X5643E = B7  
V74X5644E = B8



3. For Hundreds (H) digit

C1 = PI 1 V74X5645E = C1  
C2 = PI 2 V74X5646E = C2  
V74X5647E = C3  
V74X5648E = C4  
V74X5649E = C5  
V74X5650E = C6  
V74X5651E = C7  
V74X5652E = C8

B. Manual input

None

C. Formulation and Logic

If A1 = 1 or A2 = 1, set X1 = 1  
If A3 = 1 or A4 = 1, set X2 = 1  
If A5 = 1 or A6 = 1, set X3 = 1  
If A7 = 1 or A8 = 1, set X4 = 1

$0 = X1(20) + X2(21) + X3(22) + X4(23)$ , if  $U > 9$ , U = blank.

If B1 = 1 or B2 = 1, set Y1 = 1  
If B3 = 1 or B4 = 1, set Y2 = 1  
If B5 = 1 or B6 = 1, set Y3 = 1  
If B7 = 1 or B8 = 1, set Y4 = 1

$T = Y1(20) + Y2(21) + Y3(22) + Y4(23)$ , if  $T > 9$ , T = blank.

If C1 = 1 or C2 = 1, set Z1 = 1  
If C3 = 1 or C4 = 1, set Z2 = 1  
If C5 = 1 or C6 = 1, set Z3 = 1  
If C7 = 1 or C8 = 1, set Z4 = 1

$H = Z1(20) + Z2(21) + Z3(22) + Z4(23)$ , if  $H > 9$ , H = blank.

$MO1G3205C = H \cdot 100 + T \cdot 10 + U$

### 31.7 REFERENCES

Specification, S-Band Payload Interrogator, no. MC478-0105, September 14, 1977

SCTE Payload Interrogator Critical Design Review, no. SCTE-64-80-012, June 23, 1980

FSSR, Level C, Volume 2, no. STS83-0020A, section 4.3.5

### 31.8 OPERATIONAL NOTES

Do not use channels 649 to 653 inclusive because of possible interference.

When the PI is turned on, the transmitter and receiver are powered simultaneously. Data retrieval indicates that, if a payload transponder is on the selected frequency, it takes about 2 seconds for the PI receiver to acquire and lock to it.

Data retrieval shows that it takes about 2 minutes for the PI RX to stabilize. This is probably due to the oscillators' warming up.

If the PI is on and a signal is not on the selected channel, the RX will sweep the Center Frequency (FC) approximately  $\pm 120$  kHz. The noncoherent AGC will be active, setting the AGC based on the total power (signal + noise) in the bandwidth of  $\pm 150$  kHz of the FC. When the payload transponder is turned on, the signal is noted by the CAD, the sweep is stopped, and the coherent AGC takes control. If later the incoming signal stops, the sweep will flywheel for about 65 msec, then enable sweep within 40 msec. Therefore, it takes about 100 msec after a dropout in signal strength to reenable sweep.

Whenever the signal breaks threshold level ( $> -117$  dbm) the PI RX should lock up within 0.4 second with a 90 percent probability. The sweep rate is one sweep per 300 msec or about three sweeps per second.

**Table 31-1. Synthesizer channel frequency allocation**

| Mode     | Number of channels | Channel number | Receiver frequency MHz | Receiver lo   |           |                    | Turnaround ratio FRX/FTX | Transmitter        |                    |
|----------|--------------------|----------------|------------------------|---------------|-----------|--------------------|--------------------------|--------------------|--------------------|
|          |                    |                |                        | Frequency MHz | N divider | Step size MHz/chan |                          | Frequency MHz/chan | Step size MHz/chan |
| STDN     | 808                | 001            | 2200.0                 | 1985.0        | 520       | 0.125              | 240/221                  | 2025.83333         | 0.115104           |
|          |                    | 808            | 2300.875               | 2085.875      | 1329      |                    |                          | 2118.722396        |                    |
|          |                    | 809            |                        |               |           |                    |                          |                    |                    |
| Not used | 4                  | 849            |                        |               |           |                    |                          |                    |                    |
|          |                    | 850            | 2290.185185            | 2075.185185   | 419       | 2108.878860        |                          |                    |                    |
|          |                    | 853            | 2291.296296            | 2076.296296   | 422       | 2109.902006        |                          |                    |                    |
| DSN      | 23                 | 854            | 2291.666667            | 2076.666667   | 423       | 0.370370           | 240/221                  | 2110.243056        | 0.341049           |
|          |                    | 876            | 2299.814815            | 2084.814815   | 445       |                    |                          | 2117.746142        |                    |
|          |                    | 877            |                        | 2085.185185   | 446       |                    |                          | 2118.087191        |                    |
|          |                    | 882            | Not used               | 2087.037035   | 451       |                    |                          | 2119.792438        |                    |
|          |                    | 883            |                        |               |           |                    |                          |                    |                    |
| Not used | 6                  | 899            |                        |               |           |                    |                          |                    |                    |
|          |                    | 900            | 2202.5                 | 1987.5        | 540       | 256/205            | 1763.721                 |                    |                    |
| SGLS     | 20                 | 919            | 2297.5                 | 2082.5        | 1300      | 5.0                | 256/205                  | 1839.795           | 4.004              |
|          |                    | 920            |                        |               |           |                    |                          |                    |                    |
|          |                    | 999            |                        |               |           |                    |                          |                    |                    |
| Not used |                    |                |                        |               |           |                    |                          |                    |                    |

**Table 31-2. PI telemetry switch and/or command control**

| DSM no. | CMD name             | GCL CMD | GCIL driver   | GCIL function  | Series Interlock               | Mode SRCE                                    | CMD driver PWR   | PNL/SW no./SW name   | Telemetry  | DWG. no. |
|---------|----------------------|---------|---|--|--------------------------------|--|--|--|--|----------|
|         | DETACHED PL SYS RTCs |         |   |  |                                |  |  |  |  |          |
| 4800    | PL SYSTEM 1 - ON     | 131     | 10/5 ON<br>10/10 OFF  | P/L SYS #1<br>P/L SYS #2   | NOT 10/10<br>NOT 10/5          | PL A<br>PL C                                 | BC 1<br>BC 2   |  |  |          |
| 4801    | PL SYSTEM - OFF      | 133     | 10/5 OFF<br>10/10 OFF   | P/L SYS #1<br>P/L SYS #2   | NOT 10/10<br>NOT 10/5          | PL A<br>PL C                                 | BC 1<br>BC 2   |  |  |          |
| 4802    | PL SYSTEM 2 - ON     | 132     | 10/10 ON<br>10/5 OFF  | P/L SYS #2<br>P/L SYS #1   | NOT 10/5<br>NOT 10/10          | PL C<br>PL A                                 | BC 2<br>BC 1   |  |  |          |
| 4803    | PL PSP - SEL         | 134     | 7/6 ON<br>15/6 ON<br>8/7 OFF<br>16/7 OFF                        | P/L SIG PROC #1<br>P/L SIG PROC #2<br>P/L INTERR #1<br>P/L INTERR #2   | 10/5<br>10/10<br>10/5<br>10/10 | PL A<br>PL C<br>PL A<br>PL C                 | BC 1<br>BC 2<br>BC 1<br>BC 2   | A1/14/PWR SELECT<br>A1/14/PWR SELECT<br>A1/14/PWR SELECT<br>A1/14/PWR SELECT   | V74X4890E<br>V74X4891E<br>V74X4323E<br>V74X4353E                           |          |
| 4804    | PL INTGR - SEL       | 135     | 8/7 ON<br>16/7 ON<br>7/6 OFF<br>15/6 OFF                        | P/L INTERR #1<br>P/L INTERR #2<br>P/L SIG PROC #1<br>P/L SIG PROC #2   | 10/5<br>10/10<br>10/5<br>10/10 | PL A<br>PL C<br>PL A<br>PL C                 | BC 1<br>BC 2<br>BC 1<br>BC 2   | A1/14/PWR SELECT<br>A1/14/PWR SELECT<br>A1/14/PWR SELECT<br>A1/14/PWR SELECT   | V74X4323E<br>V74X4353E<br>V74X4890E<br>V74X4891E                           |          |
| 4805    | PL PSP/INTGR - SEL   | 136     | 7/6 ON<br>15/6 ON<br>8/7 ON<br>16/7 ON                          | P/L SIG PROC #1<br>P/L SIG PROC #2<br>P/L INTERR #1<br>P/L INTERR #2   | 10/5<br>10/10<br>10/5<br>10/10 | PL A<br>PL C<br>PL A<br>PL C                 | BC 1<br>BC 2<br>BC 1<br>BC 2   | A1/14/PWR SELECT<br>A1/14/PWR SELECT<br>A1/14/PWR SELECT<br>A1/14/PWR SELECT   | V74X4890E<br>V74X4891E<br>V74X4323E<br>V74X4353E                           |          |
| 4806    | PL XMTR PWR OUT - HI | 137     | 7/3 ON<br>15/3 ON<br>7/4 OFF<br>15/4 OFF<br>7/5 OFF<br>15/5 OFF | #1 RF POWER HI<br>#2 RF POWER HI<br>#1 RF POWER MED<br>#2 RF POWER MED<br>#1 RF POWER LOW<br>#2 RF POWER LOW |                                | PL A<br>PL C<br>PL A<br>PL C<br>PL A<br>PL C | PI/LW/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI L3/VmnC | A1/4/SPL XMTR PWR<br>A1/4/SPL XMTR PWR<br>A1/4/SPL XMTR PWR<br>A1/4/SPL XMTR PWR<br>A1/4/SPL XMTR PWR<br>A1/4/SPL XMTR PWR | V74X4890E<br>V74X4313E<br>V74X4314E<br>V74X4314E<br>V74X4315E<br>V74X4315E |          |
| 4807    | PL XMTR PWR OUT - MD | 138     | 7/4 ON<br>15/4 ON<br>7/3 OFF<br>15/3 OFF<br>7/5 OFF<br>15/5 OFF | #1 RF POWER MED<br>#2 RF POWER MED<br>#1 RF POWER HI<br>#2 RF POWER HI<br>#1 RF POWER LOW<br>#2 RF POWER LOW |                                | PL A<br>PL C<br>PL A<br>PL C<br>PL A<br>PL C | PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC | A1/4/SPL XMTR PWR<br>A1/4/SPL XMTR PWR<br>A1/4/SPL XMTR PWR<br>A1/4/SPL XMTR PWR<br>A1/4/SPL XMTR PWR<br>A1/4/SPL XMTR PWR | V74X4314E<br>V74X4314E<br>V74X4313E<br>V74X4313E<br>V74X4315E<br>V74X4315E |          |

Table 31-2. PI telemetry switch and/or command control (continued)

| DSM no. | CMD name             | GCL CMD | GCIL driver   | GCIL function  | Series Interlock | Mode SRCE                                    | CMD driver PWR   | PNL/SW no./SW name   | Telemetry  | DWG. no. |
|---------|----------------------|---------|---|--|------------------|--|--|--|--|----------|
| 4808    | PL XMTR PWR OUT - LO | 139     | 7/5 ON<br>15/5 ON<br>7/3 OFF<br>15/3 OFF<br>7/4 OFF<br>15/4 OFF | #1 RF POWER LOW<br>#2 RF POWER LOW<br>#1 RF POWER HI<br>#2 RF POWER HI<br>#1 RF POWER MED<br>#2 RF POWER MED   |                  | PL A<br>PL C<br>PL A<br>PL C<br>PL A<br>PL C | PI/L2/VmnB<br>PI/L2/VmnB<br>PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC | A1/4/SPL XMTR PWR<br>A1/4/SPL XMTR PWR<br>A1/4/SPL XMTR PWR<br>A1/4/SPL XMTR PWR<br>A1/4/SPL XMTR PWR<br>A1/4/SPL XMTR PWR | V74X4315E<br>V74X4315E<br>V74X4313E<br>V74X4313E<br>V74X4314E<br>V74X4314E |          |
| 4812    | PL SPS CMD OUT - INT | 143     | 7/9 ON<br>15/9 ON<br>7/10 OFF<br>15/10 OFF                      | PST COMAND OUT INTERR #1<br>PST COMAND OUT INTERR #2<br>PST COMAND OUT P/L UMB #1<br>PST COMAND OUT P/L UMB #2 |                  | PL A<br>PL C<br>PL A<br>PL C                 | SP/L2/VmnB<br>SP/L3/VmnC<br>SP/L2/VmnB<br>SP/L3/VmnC                             | A1/15/PSP CMD<br>A1/15/PSP CMD<br>A1/15/PSP CMD<br>A1/15/PSP CMD   | V74X4894E<br>V74X4894E<br>V74X4895E<br>V74X4895E                           |          |
| 4813    | PL SPS CMD OUT - UMB | 144     | 7/10 ON<br>15/10 ON<br>7/9 OFF<br>15/9 OFF                      | PST COMAND OUT P/L UMB #1<br>PST COMAND OUT P/L UMB #2<br>PST COMAND OUT INTERR #1<br>PST COMAND OUT INTERR #2 |                  | PL A<br>PL C<br>PL A<br>PL C                 | SP/L2/VmnB<br>SP/L3/VmnC<br>SP/L2 VmnB<br>SP/L3/VmnC                             | A1/15/PSP CMD<br>A1/15/PSP CMD<br>A1/15/PSP CMD<br>A1/15/PSP CMD   | V74X4895E<br>V74X4895E<br>V74X4894E<br>V74X4894E                           |          |
| 4814    | PL ANG POL - RT CIRC | 145     | 7/11 ON<br>15/11 ON<br>7/12 OFF<br>15/11 OF                     | P/L ANT #1 LH CIRCULAR<br>P/L ANT #2 LH CIRCULAR<br>P/L ANT #1 RH CIRCULAR<br>P/L ANT #2 RH CIRCULAR           |                  | PL A<br>PL C<br>PL A<br>PL C                 | PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC                             | A1/2/ANT POLAR<br>A1/2/ANT POLAR<br>A1/2/ANT POLAR<br>A1/2/ANT POLAR   | V74X5603E<br>V74X5604E<br>V74X5604E<br>V74X5603E                           |          |
| 4815    | PL ANG POL - RT CIRC | 146     | 7/12 ON<br>15/12 ON<br>7/11 OFF<br>15/11 OFF                    | P/L ANT #1 RH CIRCULAR<br>P/L ANT #2 RH CIRCULAR<br>P/L ANT #1 LH CIRCULAR<br>P/L ANT #2 LH CIRCULAR           |                  | PL A<br>PL C<br>PL A<br>PL C                 | PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC                             | A1/2/ANT POLAR<br>A1/2/ANT POLAR<br>A1/2/ANT POLAR<br>A1/2/ANT POLAR   | V74X5604E<br>V74X5603E<br>V74X5603E<br>V74X5604E                           |          |
| 4816    | PL FREQ SWP - ON     | 147     | 7/13 ON<br>15/13 ON<br>8/6 OFF<br>16/16 OFF                     | #1 P/L FREQ SWEEP ON<br>#2 P/L FREQ SWEEP ON<br>P/L FREQ SWP #1 OFF<br>P/L FREQ SWP #2 OFF                     |                  | PL A<br>PL C<br>PL A<br>PL C                 | PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC                             | A1/8/FREQ SWEEP<br>A1/8/FREQ SWEEP<br>A1/8/FREQ SWEEP<br>A1/8/FREQ SWEEP   | V74X4300E<br>V74X4300E<br>V74X4901E<br>V74X4901E                           |          |
| 4817    | PL FREQ SWP - OFF    | 148     | 8/6 ON<br>16/6 ON<br>7/13 OFF<br>15/13 OFF                      | P/L FREQ SWP #1 OFF<br>P/L FREQ SWP #2 OFF<br>#1 P/L FREQ SWEEP ON<br>#2 P/L FREQ SWEEP ON                     |                  | PL A<br>PL A<br>PL A<br>PL C                 | PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC                             | A1/8/FREQ SWEEP<br>A1/8/FREQ SWEEP<br>A1/8/FREQ SWEEP<br>A1/8/FREQ SWEEP   | V74X4901E<br>V74X4901E<br>V74X4300E<br>V74X4300E                           |          |

Table 31-2. PI telemetry switch and/or command control (continued)

| DSM no. | CMD name             | GCL CMD | GCIL driver                                  | GCIL function  | Series Interlock | Mode SRCE                    | CMD driver PWR                                       | PNL/SW no./SW name   | Telemetry  | DWG. no. |
|---------|----------------------|---------|--|--|------------------|------------------------------|--|--|--|----------|
| 4818    | PL MOD - ON          | 149     | 9/1 ON<br>18/1 ON<br>8/14 OFF<br>16/14 OFF   | #1 MODULATION ON<br>#2 MODULATION ON<br>MODULATION #1 OFF<br>MODULATION #2 OFF                                   |                  | PL A<br>PL C<br>PL A<br>PL C | SP/L2/VmnB<br>SP/L2/VmnC<br>SP/L2/VmnB<br>SP/L3/VmnC | A1/9/MODULATION<br>A1/9/MODULATION<br>A1/9/MODULATION<br>A1/9/MODULATION | V74X4320E<br>V74X4320E<br>V74X4903E<br>V74X4903E |          |
| 4819    | PL MOD - OFF         | 150     | 8/14 ON<br>16/14 ON<br>9/1 OFF<br>18/1 OFF   | MODULATION #1 OFF<br>MODULATION #2 OFF<br>#1 MODULATION ON<br>#2 MODULATION ON                                   |                  | PL A<br>PL C<br>PL A<br>PL C | SP/L2/VmnB<br>SP/L3/VmnC<br>SP/L2/VmnB<br>SP/L3/VmnC | A1/9/MODULATION<br>A1/9/MODULATION<br>A1/9/MODULATION<br>A1/9/MODULATION | V74X4903E<br>V74X4903E<br>V74X4320E<br>V74X4320E |          |
| 4820    | PL INTGR SWP - NAR   | 151     | 7/15 ON<br>15/15 ON<br>7/16 OFF<br>15/16 OFF | P/L INTERR #1 SWEEP NARROW<br>P/L INTERR #2 SWEEP NARROW<br>P/L INTERR #1 SWEEP WIDE<br>P/L INTERR #2 SWEEP WIDE |                  | BC 1<br>BC 2<br>BC 1<br>BC 2 | PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC | GCIL ONLY TRUE<br>GCIL ONLY TRUE<br>GCIL ONLY FALSE<br>GCIL ONLY FALSE   | V74X4302E<br>V74X4302E<br>V74X4301E<br>V74X4301E |          |
| 4821    | PL INTGR SWP - WIDE  | 152     | 7/16 ON<br>15/16 ON<br>7/15 OFF<br>15/15 OFF | P/L INTERR #1 SWEEP WIDE<br>P/L INTERR #2 SWEEP WIDE<br>P/L INTERR #1 SWEEP NARROW<br>P/L INTERR #2 SWEEP NARROW |                  | BC 1<br>BC 2<br>BC 1<br>BC 2 | PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L2/VmnC | GCIL ONLY FALSE<br>GCIL ONLY FALSE<br>GCIL ONLY TRUE<br>GCIL ONLY TRUE   | V74X4301E<br>V74X4301E<br>V74X4302E<br>V74X4302E |          |
| 4822    | PL FREQ UNIT SEL - 1 | 161     | 8/3 ON<br>16/3 ON                            | INTERR #1 CHAN 1<br>INTERR #2 CHAN 1   |                  | PL A<br>PL C                 | PI/L2/VmnB<br>PI/L3/VmnC                             | A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL                                     | V74X5629E<br>V74X5630E                           |          |
| 4823    | PL FREQ UNIT SEL - 2 | 162     | 8/4 ON<br>16/4 ON                            | INTERR #1 CHAN 2<br>INTERR #2 CHAN 2   |                  | PL A<br>PL C                 | PI/L2/VmnB<br>PI/L3/VmnC                             | A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL                                     | V74X5631E<br>V74X5632E                           |          |
| 4824    | PL FREQ UNIT SEL - 4 | 163     | 8/5 ON<br>16/5 ON                            | INTERR #1 CHAN 4<br>INTERR #2 CHAN 4   |                  | PL A<br>PL C                 | PI/L2/VmnB<br>PI/L3/VmnC                             | A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL                                     | V74X5633E<br>V74X5634E                           |          |
| 4825    | PL FREQ UNIT SEL - 8 | 164     | 8/1 ON<br>16/1 ON                            | INTERR #1 CHAN 8<br>INTERR #2 CHAN 8   |                  | PL A<br>PL C                 | PI/L2/VmnB<br>PI/L3/VmnC                             | A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL                                     | V74X5635E<br>V74X5636E                           |          |
| 4826    | PL FREQ TENS SEL - 1 | 171     | 8/9 ON<br>16/9 ON                            | INTERR #1 CHAN 10<br>INTERR #2 CHAN 10   |                  | PL A<br>PL C                 | PI/L2/VmnB<br>PI/L3/VmnC                             | A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL                                     | V74X5637E<br>V74X5638E                           |          |
| 4827    | PL FREQ TENS SEL - 2 | 172     | 8/10 ON<br>16/10 ON                          | INTERR #1 CHAN 20<br>INTERR #2 CHAN 20   |                  | PL A<br>PL C                 | PI/L2/VmnB<br>PI/L3/VmnC                             | A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL                                     | V74X5639E<br>V74X5640E                           |          |

Table 31-2. PI telemetry switch and/or command control (continued)

| DSM no. | CMD name             | GCL CMD | GCIL driver  | GCIL function  | Series Interlock | Mode SRCE  | CMD driver PWR   | PNL/SW no./SW name   | Telemetry              | DWG. no. |
|---------|----------------------|---------|--|--|------------------|--|--|--|------------------------|----------|
| 4828    | PL FREQ TENS SEL - 4 | 173     | 8/11 ON<br>16/11 ON  | INTERR #1 CHAN 40<br>INTERR #2 CHAN 40   |                  | PL A<br>PL C   | PI/L2/VmnB<br>PI/L3/VmnC   | A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL   | V74X5641E<br>V74X5642E |          |
| 4829    | PL FREQ TENS SEL - 8 | 174     | 8/12 ON<br>16/12 ON  | INTERR #1 CHAN 80<br>INTERR #2 CHAN 80   |                  | PL A<br>PL C   | PI/L2/VmnB<br>PI/L3/VmnC   | A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL   | V74X5643E<br>V74X56443 |          |
| 4830    | PL FREQ 100 SEL - 1  | 181     | 8/13 ON<br>16/13 ON  | INTERR #1 CHAN 100<br>INTERR #2 CHAN 100   |                  | PL A<br>PL C   | PI/L2/VmnB<br>PI/L3/VmnC   | A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL   | V74X5645E<br>V74X5646E |          |
| 4831    | PL FREQ 100 SEL - 2  | 182     | 8/8 ON<br>16/8 ON  | INTERR #1 CHAN 200<br>INTERR #2 CHAN 200   |                  | PL A<br>PL C   | PI/L2/VmnB<br>PI/L3/VmnC   | A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL   | V74X5647E<br>V74X5648E |          |
| 4832    | PL FREQ 100 SEL - 4  | 183     | 8/15 ON<br>16/15 ON  | INTERR #1 CHAN 400<br>INTERR #2 CHAN 400   |                  | PL A<br>PL C   | PI/L2/VmnB<br>PI/L3/VmnC   | A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL   | V74X5649E<br>V74X5650E |          |
| 4833    | PL FREQ 1 - 8        | 184     | 8/16 ON<br>16/16 ON  | INTERR #1 CHAN 800<br>INTERR #2 CHAN 800   |                  | PL A<br>PL C   | PI/L2/VmnB<br>PI/L3/VmnC   | A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL   | V74X5651E<br>V74X5652E |          |
| 4834    | PL FREQ SEL - RESET  | 191     | 8/1 OFF<br>16/1 OFF<br>8/3 OFF<br>16/3 OFF<br>8/4 OFF<br>16/4 OFF<br>8/5 OFF<br>16/5 OFF<br>8/8 OFF<br>16/8 OFF<br>8/9 OFF<br>16/9 OFF<br>8/10 OFF<br>16/10 OFF<br>8/11 OFF<br>16/11 OFF<br>8/12 OFF<br>16/12 OFF<br>8/13 OFF<br>16/13 OFF<br>8/15 OFF<br>16/15 OFF<br>8/16 OFF<br>16/16 OFF | INTERR #1 CHAN 8<br>INTERR #2 CHAN 8<br>INTERR #1 CHAN 1<br>INTERR #2 CHAN 1<br>INTERR #1 CHAN 2<br>INTERR #2 CHAN 2<br>INTERR #1 CHAN 4<br>INTERR #2 CHAN 4<br>INTERR #1 CHAN 200<br>INTERR #2 CHAN 200<br>INTERR #1 CHAN 10<br>INTERR #2 CHAN 10<br>INTERR #1 CHAN 20<br>INTERR #2 CHAN 20<br>INTERR #1 CHAN 40<br>INTERR #2 CHAN 40<br>INTERR #1 CHAN 80<br>INTERR #2 CHAN 80<br>INTERR #1 CHAN 100<br>INTERR #2 CHAN 100<br>INTERR #1 CHAN 400<br>INTERR #2 CHAN 400<br>INTERR #1 CHAN 800<br>INTERR #2 CHAN 800 |                  | PL A<br>PL C<br>PL A<br>PL C<br>PL A<br>PL C<br>PL A<br>PL C<br>PL A<br>PL C<br>PL A<br>PL C<br>PL A<br>PL C<br>PL A<br>PL C<br>PL A<br>PL C<br>PL A<br>PL C<br>PL A<br>PL C<br>PL A<br>PL C | PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC<br>PI/L2/VmnB<br>PI/L3/VmnC | A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL<br>A1/7/CHANNEL SEL |                        |          |

**SECTION 32 - PAYLOAD SIGNAL PROCESSOR**  
**CONTENTS**

| <b>Section</b> |  | <b>Page</b> |
|----------------|--|-------------|
| 32.1           | GENERAL .....                            | 32-1        |
| 32.2           | INTERFACES .....                         | 32-1        |
| 32.2.1         | Control and Displays .....               | 32-2        |
| 32.3           | DESCRIPTION.....                         | 32-4        |
| 32.3.1         | PSK Demodulator .....                    | 32-4        |
| 32.3.2         | Bit Synchronizer and Microprocessor..... | 32-5        |
| 32.3.3         | Telemetry Data Processor.....            | 32-5        |
| 32.3.4         | Command Data Processor .....             | 32-6        |
| 32.3.5         | Power Requirements.....                  | 32-10       |
| 32.3.6         | Mechanical .....                         | 32-10       |
| 32.4           | SOFTWARE.....                            | 32-10       |
| 32.4.1         | PSP-to-GPC Communications .....          | 32-10       |
| 32.4.2         | PSP Status Message .....                 | 32-10       |
| 32.4.3         | PSP Configuration Message .....          | 32-14       |
| 32.4.4         | Command Data Loads for PSP .....         | 32-15       |
| 32.4.5         | PSP Communication Sequence .....         | 32-16       |
| 32.4.6         | Illegal Message Checking .....           | 32-18       |
| 32.5           | INSTALLATION.....                        | 32-19       |
| 32.5.1         | Location.....                            | 32-19       |
| 32.5.2         | Temperature Control .....                | 32-19       |
| 32.6           | DESCRIPTION OF OPERATION.....            | 32-19       |
| 32.6.1         | Ground Commands.....                     | 32-19       |
| 32.6.2         | Telemetry .....                          | 32-22       |
| 32.6.3         | Special Telemetry Computations .....     | 32-23       |
| 32.7           | REFERENCES.....                          | 32-26       |



## TABLES

| Table |   | Page  |
|-------|---|-------|
| 32-1  | Payload signal processor communications inputs .....  | 32-26 |
| 32-2  | Payload signal processor communications outputs ..... | 32-28 |
| 32-3  | Initial PSP configuration .....                       | 32-32 |

## FIGURES

| Figure |  |      |
|--------|--|------|
| 32-1   | PSP interface connection.....                  | 32-1 |
| 32-2   | SPEC 62 .....                                  | 32-2 |
| 32-3   | Panel A1L .....                                | 32-3 |
| 32-4   | PSK demodulator functional block diagram ..... | 32-4 |
| 32-5   | Block diagram command data processing .....    | 32-8 |

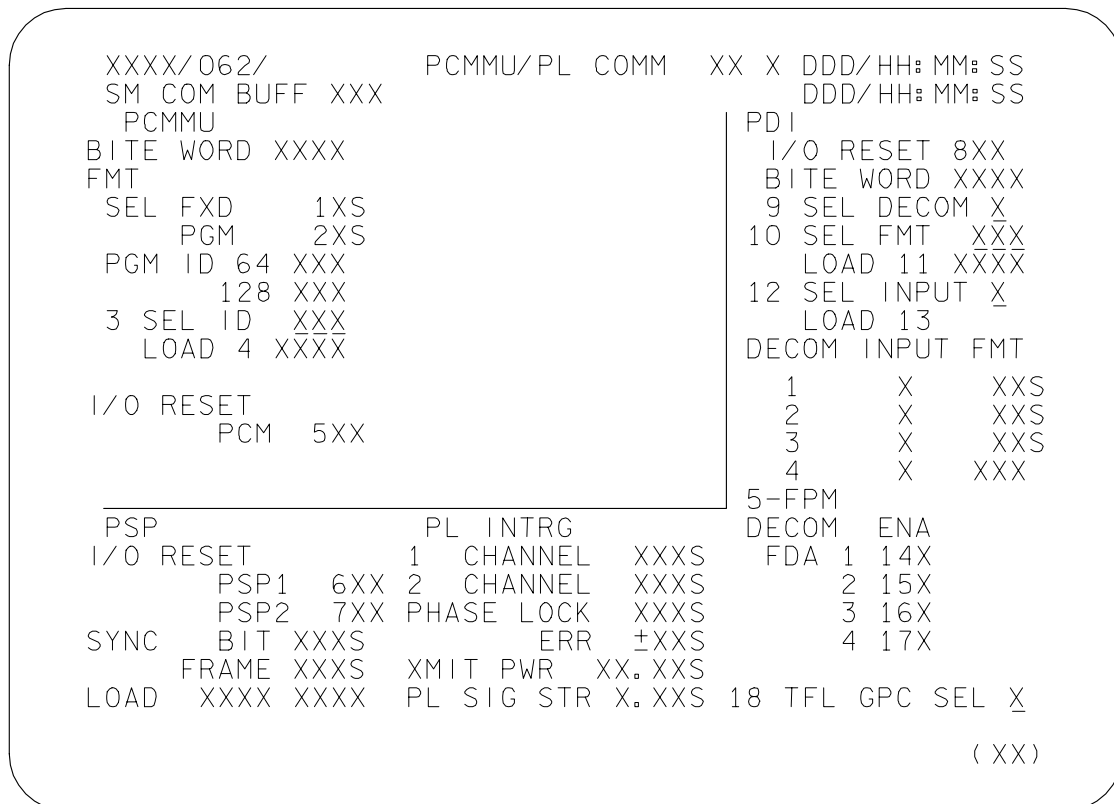


### 32.2.1 Control and Displays

#### 32.2.1.1 SPEC 62

The Systems Management (SM) specialist function display (SPEC 62), available in SM Operations Sequence (OPS) 2, 4, and GNC OPS 9, allows control and monitoring of the PSP. The only control that is available on this display is PSP Input/Output (I/O) reset. Item 6 (for PSP 1) and Item 7 (for PSP 2) are used to reestablish communications between the SM GPC and the desired PSP for communication with the PI or attached payloads.

There are four text fields which are used to display the PSP status. The first two fields display bit and frame sync. The text values in this field will be "yes," "no," or blank. The next two fields represent the status of a load. The first of these fields displays RJCT for rejection of a PSP command, INCP for an incomplete command load, or is blank for nominal PSP operations. The second status field uses double overbright text to identify which PSP command issuer is the source of the rejected or incomplete load. The command types are Time Executed Command (TEC), Payload Control Supervisor (PCS), ITEM (cargo control spec item entry), Uplink (U/L), Guidance, Navigation and Control (GNC), MULT (more than one source), or blank for nominal operation.



186113102. ART 1

Figure 32-2. SPEC 62

32.2.1.2 Panel A1L

There are three switches on panel A1L (Figure 32-3) which are used to control the PSP. The first, S13 (power, system), is a three-position switch that is used to select the system that is to be powered on. These positions are 1, off, and 2. The second switch, S14 (power, select), is a three-position switch that is used to determine if the PSP and the PI will be powered on independently or together. These positions are INTRG, BOTH, and PSP. The third switch, S15 (PSP cmd output), is a two-position switch used to determine the route that the PSP will use to send the commands to the payload. These positions are INTRG and PL UMB.

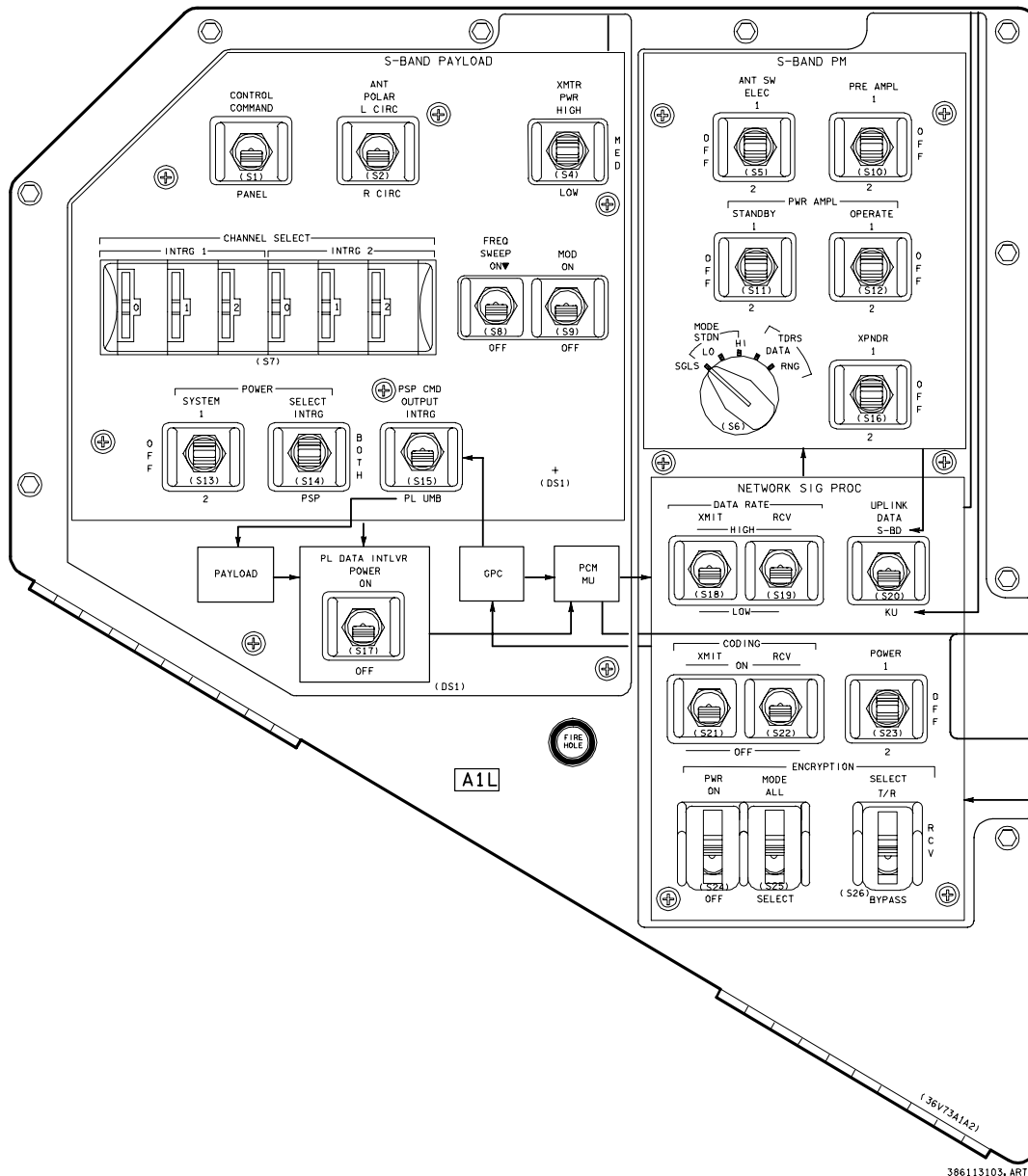


Figure 32-3. Panel A1L

### 32.3 DESCRIPTION

The PSP is comprised of four subassemblies: the PSK demodulator, bit synchronizer, telemetry data processor, and the command data processor.

#### 32.3.1 PSK Demodulator

The PSK demodulator demodulates a 1.024-MHz PSK subcarrier from either PI or the GSE umbilical. Figure 32-4 shows the PSK demodulator block diagram. The PSK demodulator consists of a costas loop with a hard-limited in-phase arm. Two high-level mixers are used as in-phase and quadrature-phase detectors. The 3 dB cutoff frequency of the arm filters are configurable in the order of the selected data rate. The hard-limiter/chopper-type multiplier combination wipes the data off of the error voltage. This error voltage is then integrated by the loop filter and becomes the control voltage which sets the Voltage Controlled Oscillator (VCO) output frequency. The VCO output is nominally set at 20 times the subcarrier frequency. The sine (sin) and cosine (cos) references are obtained by dividing down the VCO output. These are provided to the in-phase and quadrature-phase detectors thereby closing the loop.

The baseband signal is obtained from the in-phase mixer output and sent to the Analog to Digital (A/D) converter for quantization. Also 10.24- and 1.024-MHz signals are sent to the bit sync.

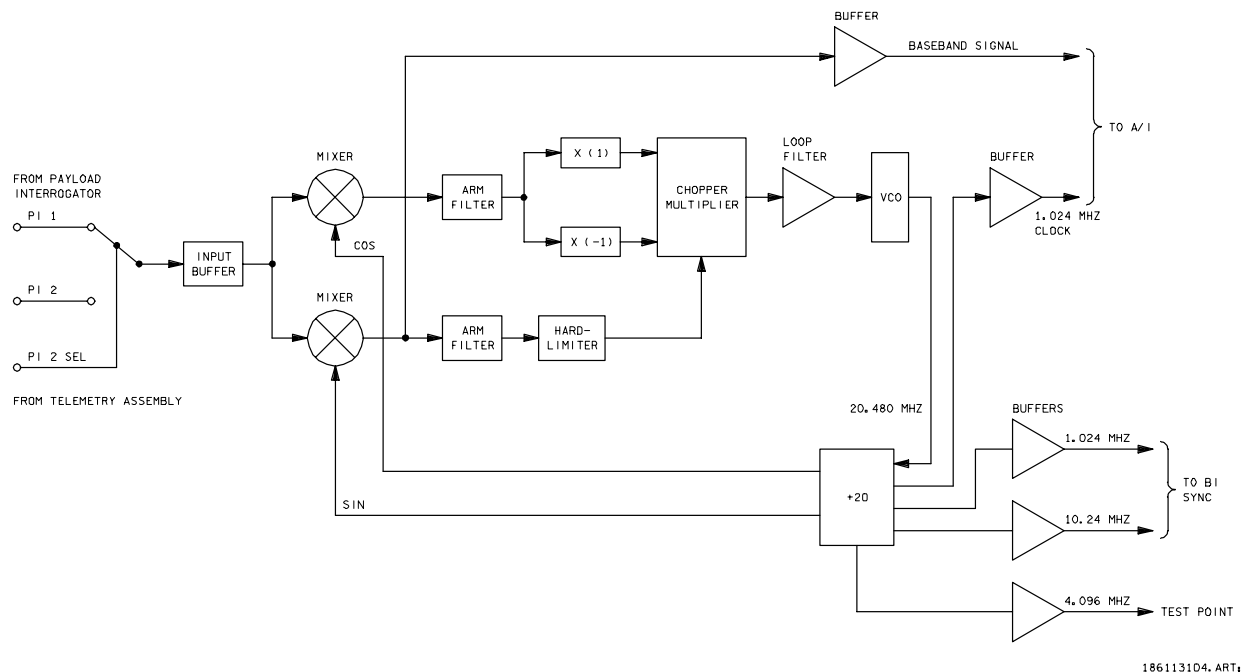


Figure 32-4. PSK demodulator functional block diagram

### 32.3.2 Bit Synchronizer and Microprocessor

The bit synchronizer and microprocessor receives 10.24-MHz signals from the PSK demodulator (Figure 32-4) and uses it as a master clock to generate T1 through T4 four-phase timing clocks for the bit sync. 1.024 B/S and 1.024 B/S1 are used to strobe integration data and to generate dump command for the bit sync. A/D data inputs are 3-bit data and are updated at the leading edge of the 1.024 B/S clock.

There are three interrupt lines to the bit sync from the Telemetry (TLM) data processor: Load Interrupt (LDINT), Read Interrupt (RDINT), and Frame Sync Interrupt (FSINT). LDINT is delayed from the  $\frac{1}{4}$  bit clock by 9 microseconds. The second LDINT is approximately 24 microseconds after the first LDINT with each spacing approximately 8 microseconds in a group. Each LDINT loads an 8-bit word from TLM data processor to bit sync. The RDINT is delayed from the R clock 2 by 9 microseconds when it is initiated from the TLM data processor. When the bit sync acknowledges the TLM data processor request, the bit sync sends six 8-bit words back to the TLM data processor along with ECHO CLK. The six 8-bit words were originally loaded from the TLM data processor. The purpose of this read interrupt is to verify the communication link between the bit sync and the TLM data processor. The frame sync interrupt is delayed from the R clock 3 by 9 ps when it is initiated from the TLM data processor. The FSINT requests the frame sync verification from the bit sync. The R COR, N COR indicates that routine correlation and negative correlation has been achieved, respectively. INTBUSY indicates an interrupt has been received by the bit sync. TLMDAT is the serial data output from the bit sync. BS LOCK indicates whether the bit sync is in lock or not.

### 32.3.3 Telemetry Data Processor

The telemetry data processor contains the logic necessary for performing frame sync lock generation, temporary telemetry data storage, configuration message storage and transmission, status message buffering, and power interrupt initialization. The frame sync lock logic uses the correlation output of the frame sync detect logic to synchronize the demultiplexing action of the PSP telemetry data and memory I/O controller and to provide various indicators relating to the state of acquisition lock logic to the remainder of the PSP. A lock indication is also provided to the Orbiter Instrumentation (OI) MDM. The telemetry data and memory I/O controller performs the demultiplexing, read and write operations on the incoming telemetry data and supplies control to the rest of the TLM data processor. It also contains the data bit, data word, and frame sync bit counters.

The memory section consists of a 32 by 256 random access memory, a serial-to-parallel input buffer, and a parallel-to-serial output buffer and is controlled by the TLM and memory I/O controller.

The telemetry data output buffer is a variable length shift register which is parallel-loaded with the TLM frame sync data. After the TLM frame sync data are parallel-loaded, these data and the TLM data are serially shifted out. The TLM clock generator generates the 50 percent duty cycle TLM data clock. The data and clock are transmitted to the PDI via differential line drivers that are enabled when the Frame Sync (F/S) detect logic goes to F/S lock mode.

The configuration message load controller formats and transmits the configuration data to the bit sync and controls the interval configuration data load. It also generates the bit sync RDINT clock and the FSINT clock.

The configuration message read controller strobes the bit sync for the refresh configuration data and controls the data load. The refresh configuration data are parallel-loaded into the configuration data refresh buffer and then serially shifted into the refresh configuration data storage register. The status message output buffer is parallel-loaded with the status message data after the completion of the configuration data refresh cycle. This information is stored until it is clocked out to the command data processor by the status message clock.

The power transient detector can detect a power blackout, brownout, or transient. It provides a signal to initialize the PSP as well as setting the initialize bit in the status message to a "one" indicating the PSP has just been initialized.

### **32.3.4 Command Data Processor**

The command data processor performs the following: configuration/ command message validation, status message generator, command message double buffer, command message output formatter, configuration message storage, MDM I/O interface, and command message data output selection.

#### **32.3.4.1 Configuration/Command Message Validation**

The configuration/command message validation module performs word sync detection and data strobe by detecting the word sync pattern and then generating the data bit clock. (If a sync pattern is not detected, the data bit clock will not be generated.) It also performs three different word checks. They are the biphase data, the parity check, and the end of data check. The outputs of these three checks are added together with bit count 17 to generate a pulse for every data word. If any of the three checks fail, the word pulse will be inhibited or there will be more than one pulse. This output is called WORD COUNT (WRDCNT) and is used by the message validation logic in the message counter. The configuration message code check part of the configuration/ command message validation function is accomplished by checking the first three configuration words for illegal codes. The check logic is enabled by the configuration word discrete. The three different word check outputs (WRD1C, WRD2C, and WRD3C) are selected by using a multiplexer controlled by the two least significant bit (LSBs) of the configuration word counter (CNFQO and CNFQI) and enabled by CFWD. The error-out is strobed by word discrete and reset by MPUSLEI. The final function is the configuration and command validation logic. This module verifies that there are 5 error-

free configuration words and 32 error-free command words. Before the configuration word is validated, it should pass the illegal code check. The error checks are done by the word check logic, and the illegal code check is done by the configuration message code check (both are discussed previously). Finally the configuration message load control decides on whether to load the configuration message and/or read the command word. The load control is enabled by the outputs of the message validation logic and controlled by various inputs. The output of this section enables the configuration message load logic. After this cycle is complete, the command read is started. The configuration message load logic then controls the loading of the configuration data to the telemetry processor and the loading of the configuration data to permanent storage in the command processor. When the new configuration message is the same as the old configuration message, the load logic will only load the configuration data to the TLM processor. After the configuration data are loaded, the command data read logic is enabled.

#### **32.3.4.2 Status Message Generator**

The status message generator consists of a command link frequency generator, status message controller/formatter, and the status message output buffer.

The command link frequency generator is a 12-MHz oscillator, a countdown circuit (12 MHz to 2 MHz and 1 MHz), and clock driver circuits. The clock countdown circuit divides the 12-MHz oscillator frequency down to a 4-MHz test clock, then down to 2 MHz and 1 MHz. The countdown circuitry is controlled by the word discrete enabled by status message enable. The clock outputs (IMOI, IMOI, IM02, IM02, 2M, and 2M) are driven by clock drivers. The clocks are only controlled during the status message readout; for the remainder of the time they are free running.

The status message output controller and formatter provides the data encoding and timing necessary to drive the Payload (P/L) MDM I/O interface. The controller provides the status message generator with the proper clocks and timing relationships necessary for correct data transmission. The formatter, upon command, serially transfers the status data from the status registers, encodes each 16-bit word into Manchester II format, and generates a word sync and parity bit.



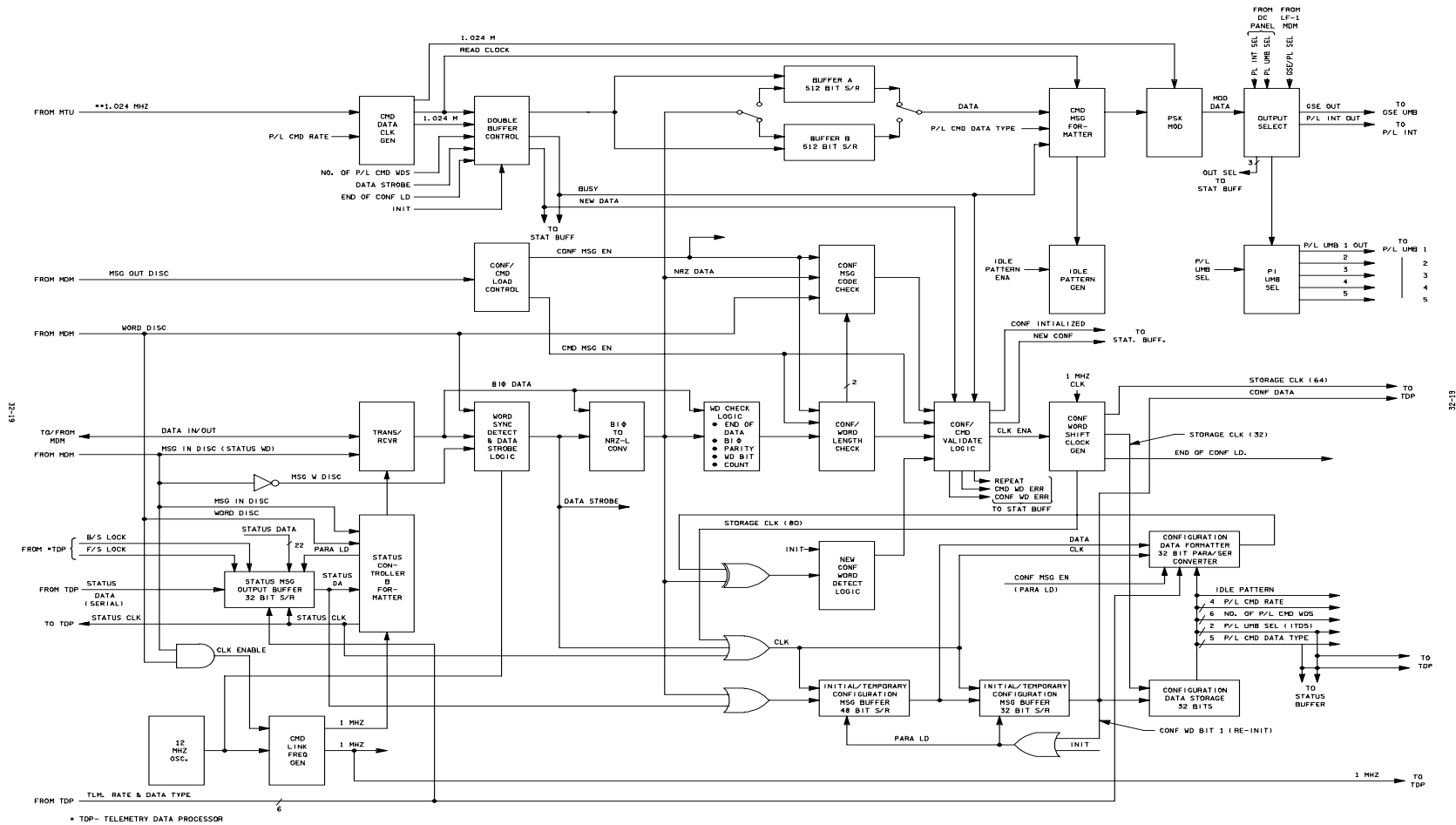


Figure 32-5. Block diagram command data processing

The status message output buffer stores the status message data until the data are serially shifted out by the message controller and formatter. The status message data are parallel-loaded into the output buffer by STATUS MESSAGE ENABLE. Serial status message data are also input from the TLM data processor. Thirty-two bits are stored by the command data processor, and 48 bits are stored by the TLM data processor.

#### **32.3.4.3 Command Message Double Buffer**

The command message double buffer is of A-B double buffer design and consists of two symmetrical sections. When the A section is loaded, data will be read out of A and loaded into B and vice versa. The number of command words transmitted to the PI and read out clock rate are programmable via configuration word. The double buffer is loaded with command data as the data are input from the P/L MDM, at a clock rate of 1 MHz. The CMD readout does not start until the configuration and command message has been verified and a new configuration message loaded (if different from the previous configuration message).

#### **32.3.4.4 Command Message Output Formatter**

The command message output formatter contains the PSK modulator and the output formatter, and its function is to convert the command data to the programmed data type Non-Return-to-Zero Level (NRZ-L), NRZ-M (M), or NRZ-S (S) and add the idle pattern if programmed to do so. After going through the formatter, the data get PSK modulated with a 16-kHz message data output selector. The program is loaded via the configuration message.

#### **32.3.4.5 Configuration Message Storage Module**

The configuration message storage module consists of the initial/temporary configuration message buffer which stores 80 bits of data (five 16-bit words). It is used to store the incoming serial P/L MDM configuration data until the configuration and command messages are verified; then the data are serially transferred to the configuration data storage register. Part of the register is also used to store status message data. These data are compared against the incoming P/L MDM configuration data to determine whether the configuration message has changed or not. Only the last 48 bits are used for this purpose. The configuration data storage register is used to store the first 32 bits of the configuration message data. The data are serially loaded into the register after the configuration and command message data have been verified. The clock used for this, CFWSCLI, is enabled for only the first 32 clocks of the configuration message load cycle.

#### **32.3.4.6 Command Message Data Output**

The command message data output selection is done with relays. The relay drivers and select logic are located in the TLM data processor. The command data can be selected to go to the following output ports exclusively.

GSE umbilical

P/L interrogator

P/L umbilical 1 to 5

#### **32.3.5 Power Requirements**

Power - 38 W maximum

Buses - PSP 1 - Mn B FLC 2

PSP 2 - Mn C FLC 3

#### **32.3.6 Mechanical**

Size - 7.6 inches high by 15.62 inches long by 7.6 inches wide

Weight - 18 pounds maximum

### **32.4 SOFTWARE**

The following paragraphs will discuss the PSP-to-GPC communications, status message, and configuration message.

#### **32.4.1 PSP-to-GPC Communications**

The SM OPS 2 and SM OPS 4 software provides the capability to communicate with either PSP via its corresponding P/L MDM serial channel (PSP 1 - PL MDM 1 CD 8 channel 1 and PSP 2 - P/L MDM 2 CD 8 channel 1). Table 32-1 and Table 32-2 describe the parameters used as inputs and outputs, respectively, to the PSP communication software function. The communications with the PSP involves the use of the PSP status message, the PSP configuration message (Table 32-3) command/data loads.

#### **32.4.2 PSP Status Message**

The PSP status message consists of five 16-bit words which indicate the status of the PSP. The first three bits of the first status word are used by the SM software to evaluate the next step in the communication sequence (refer to Section 32.6). These parameters and the remaining parameters in the current status message from the operating PSP are available for display and downlist. The first three bits, indicated above, are defined as follows.

A. Status Word 1

- Bit 1 NEW DATA - This bit will be logic "one" only when at least one of the PL command I/O buffers of the PSP is capable of receiving a new command/data message. This bit will be logic "zero" for all other conditions. This bit is initialized to logic "one."
- Bit 2 BUSY - This bit will be a logic "one" when the PSP is still processing command/data messages under its current configuration message. This bit will be a logic "zero" for all other conditions. This bit is initialized to a logic "zero."
- Bit 3 REPEAT - This bit will be a logic "one" only when the PSP received erroneous configuration and/or command/data messages (refer to par. 32.6.2). This bit will be a logic "zero" for all other conditions including initialization.

The remaining bits of status word 1 and status words 2 to 5 are not used in interactive software processing and are defined below.

- Bit 4 CONFIGURATION ERROR - This bit will be a logic "one" only when the configuration message received from the PL MDM failed to meet the data validation criteria. The data validation criteria are:
- 1) The bit orientation in the received waveform reflects a valid biphasic code, such that only 10 or 01 patterns occur and that only the proper number of received threshold transitions occur within each bit time. Refer to Figure 32-1 for P/L MDM/PSP timing interface.
  - 2) Each word has exactly 20 bits: 3 sync, 16 data, and 1 odd parity bit.
  - 3) Standard parity bit verification.
  - 4) Legal "payload umbilical select" bit even when PI is selected.
- Bit 5 CONFIGURATION INITIALIZED - This bit will be a logic "one" only when the PSP assumes the initial configuration state. This bit will be a logic "zero" for all other conditions.
- Bit 6 PAYLOAD COMMAND ERROR - This bit will be a logic "one" only when the payload command message received from the PL MDM fails to meet the data validation criteria defined in Bit 4 above. It shall be a logic "zero" for all other conditions. It is initialized to logic "zero."

- Bit 7 NEW CONFIGURATION - This bit will be a logic "one" only when the configuration message received is different from the present configuration while the PSP is still processing payload commands. It will be a logic "zero" for all other conditions.
- Bits 8-11 P/L COMMAND RATE - These bits will indicate the bit rate that the PSP is currently using for transmitting the payload commands. These bits are not a mere "readback" of the configuration message but indicate the actual output processing by the PSP. The PSP is initialized to 2 kbps when powered on.
- Bit 12 Spare - Not used.
- Bit 13 IDLE PATTERN ENABLED - This bit will be a logic "one" when the idle pattern is enabled for transmission and when there are no command data being transmitted. This bit is a logic "zero" for all other conditions. This bit is initialized to a logic "zero" indicating idle pattern is disabled.
- Bit 14 PAYLOAD INTERROGATOR OUTPUT - This bit will be a logic "one" only when the PSP command output to the P/L interrogator is selected. It shall be a logic "zero" for all other conditions. This bit is initialized to a logic "zero" indicating the PI output is not selected.
- Bit 15 PAYLOAD UMBILICAL OUTPUT - This bit will be at logic "one" only when the command output to the P/L umbilical is selected. It shall be at logic "zero" for all other conditions. It is initialized to a logic "zero."
- Bit 16 GSE OUTPUT - This bit will be at logic "one" only when the command output to the GSE is selected. It shall be at logic "zero" for all other conditions. It is initialized to a logic "zero."

B. Status word 2

- Bit 1 PAYLOAD INTERROGATOR INPUT - The payload interrogator input will be at logic "one" only when the telemetry input from the payload interrogator is selected. It will be at logic "zero" for all other conditions. It is initialized to a logic "zero."
- Bit 2 GSE INPUT - This bit will be at logic "one" only when the telemetry input from the GSE is selected. It will be at logic "zero" for all other conditions, and it is initialized to a logic "zero."
- Bits 3-5 TELEMETRY RATE - These bits indicate the bit rate that the PSP is currently using for receiving the PI telemetry data. The PSP is initialized to 16 kbps.
- Bit 6 Spare - Not used.

- Bit 7 BIT SYNC LOCK - This bit will be a logic "one" only when the bit synchronization of incoming PI telemetry data is accomplished. It will be a logic "zero" for all other conditions. It is initialized to a logic "zero."
- Bit 8 FRAME SYNC LOCK - This bit will be a logic "one" only when the frame synchronization of incoming PI telemetry data is accomplished. It will be a logic "zero" for all other conditions. It is initialized to a logic "zero."
- Bits 9-11 PAYLOAD UMBILICAL SELECTED - These bits will indicate the umbilical that PSP has currently selected for command data output to an attached P/L. The PSP is initialized to UMB 0 indicating that the command output to the P/L umbilicals was not selected.
- Bits 12-13 PAYLOAD COMMAND DATA TYPE - These bits will indicate the data waveform (NRZ-L, -M, or -S) of the P/L commands that the PSP is currently using for transmission. The PSP is initialized to NRZ-L.
- Bits 14-16 TELEMETRY DATA TYPE - These bits will indicate the data waveform (biphase-L, -M, -S, NRZ-L, -M, or -S) of the PI telemetry data that the PSP is currently using for processing. The PSP is initialized to biphase-L.

C. Status word 3

- Bits 1-11 TELEMETRY FRAME LENGTH - These bits will indicate the number of 8-bit telemetry words contained between successive frame sync words that the PSP is using for current telemetry processing. The PSP is initialized to 64 8-bit words.
- Bits 12-14 FRAME SYNC WORD LENGTH - These bits will specify the number of bits (8, 16, 24, or 32) in the frame sync word that the PSP is using for current telemetry processing. The PSP is initialized to 32 bits.
- Bits 15-16 Spare - Not used.

D. Status words 4 and 5

- Bits 1-16 TELEMETRY FRAME SYNC WORD - These bits indicate the current (both frame sync pattern used by the PSP to process the current inwords) coming PI telemetry. The PSP is initialized to "all ones."

The PSP is capable of responding to a status request from the SM GPC (polling) by sending a status message, consisting of five 16-bit words, to the P/L MDM at least every 80 ms  $\pm$ 4 ms. Only the first two 16-bit words will be continuously updated. The last three words shall be updated after initialization and after each valid configuration and command message, and will send a true status message after being polled once.

A subsequent polling will show only “zeros” in the last three status words. Refer to Table 32-2 for the status message.

Note: When a new configuration message is sent which is different from the previous configuration message, the buffer will be updated, and dropouts in the received telemetry may occur. No dropouts will occur when the new configuration message is identical to the previous message.

### 32.4.3 PSP Configuration Message

The configuration message consists of five 16-bit words. The configuration message contains instructions for relay of command/data from the orbiter GPC to the P/L. The configuration message also contains instructions that control the telemetry data transfer via the PSP.

The SM application has the capability to access five prestored configuration messages and a reinitialize configuration message. The capability to access the prestored configuration messages is via item execution of a PSP command load, PCS, or via uplink by recognizing a configuration message Identification (ID) number corresponding to the item or in the uplink load.

The configuration message ID (S49035) of the last configuration message (reinitialize = 0 or prestored = 1 to 5) sent to the PSP is made available for display and downlist.

If the reinitialize bit is set to zero, the PSP will set up according to the configuration message (Table 32-3). If the reinitialize bit is set to one, the PSP will set up to a predefined condition set by the PSP. Item execution or uplink of a PSP command load containing a configuration message ID=0 will cause a command load to be initiated containing configuration message data from prestored configuration message number 1 with the reinitialize bit set. The contents of all five configuration messages are specified in the P/L Flight Systems Software Requirements (FSSR) for each mission. This load will be output per the communication sequence defined in Section 32.7. When the PSP receives a message with the reinitialize bit “on,” all data following the configuration message will be ignored.

The SM application will always transmit 32 16-bit words in the command message. The number of valid words will indicate in the number of P/L command words field in the configuration message, and the rest of the Command Data Words (CDWs) in the command message will be whatever command data were left in the command load buffer from the previous command load(s).

The SM application has the capability to compute the number of valid P/L command words to be transferred and insert this value in the number of P/L command words field. If the data are via an item entry input, the number of words is derived from the total number of P/L command words in the command load corresponding to the item. If the data are via uplink (either P/L data, P/L throughput, or Time Execute Command (TEC)), the value to be inserted in the number of P/L command words field is derived from the uplink data total number of P/L command words. If the data are via PCS, the value to

be inserted into the number of P/L command words field is derived from the PCS data total number of P/L command words.

The capability exists, via uplink load, to change a designated configuration message, (1 to 5) that had been stored preflight. The application software will reject the uplink load if the reinitialization bit (S49043) is on in the uplink configuration message or if the configuration message to be changed is configuration message ID 0. A discrete parameter value (S51034 UPLINK INVALID REQUEST) indicating a rejection of the uplink load is made available for display and downlist. This parameter value is disabled when a load is accepted. The ID number of the configuration message which is changed will remain the same as the original ID number. Refer to Figure 32-4 for definition of the configuration message.

#### **32.4.4 Command Data Loads for PSP**

The SM application has the capability to process the following types of command loads.

##### **32.4.4.1 Uplink Data Load Without Configuration Message**

This load consists of up to 64 16-bit P/L command words. The header consists of information indicating the configuration message ID and the total number of P/L command words as described in Section 1.0. Data will be transmitted to the PSP in command messages of not more than 32 16-bit P/L command words per the communication sequence specified in Section 32.4.5. Each P/L CDW transfer for the same load will contain the same configuration message.

##### **32.4.4.2 Command Data Loads via Item Execute**

When a PSP command load is executed from a CC SPEC, the SM application will access the command data load and configuration message corresponding to the item entry and transmit the command load to the PSP per the communication sequence specified in Section 32.4.5. Each command message transfer for the same load contains the same configuration message. The data content of these loads and the number of words in each applicable load will be specified in the P/L FSSR. The SM application is not required to be aware of the data content format internal to these 16-bit words.

##### **32.4.4.3 Command Data Loads From P/L Processes e.g., PCS)**

PL processes as described in the SM Level B document will be able to request output of data via the PSP. Each request will specify the PSP configuration ID to be used and the number of data words in the load, up to a maximum of 64 16-bit words. Data will be transmitted to the PSP in command messages of up to 32 16-bit P/L command words each. Each P/L command message transfer for a load contains the same configuration message.



### 32.4.5 PSP Communication Sequence

The SM application has the capability to enable the communication between the GPC and either PSP via item entry on the Pulse Code Modulation Master Unit (PCMMU)/PL COMM SPEC 62 (Figure 32-2).

When communication has been enabled, the SM application will reset the Backup Control Electronics (BCE) element corresponding to the status message for the selected PSP and communicate with the selected PSP until the BCE element containing the status message for the selected PSP is bypassed by system software.

When a BCE element bypass occurs affecting the receipt of the status message, the SM application will cease the communication, clear all data awaiting transfer or recognition of completed transfer, and cause the PCMMU/PL COMM SPEC to be updated to reflect that the PSP communication is inhibited. If communication has been disabled via I/O error, all requests to generate a PSP command load will be rejected and an indication (S49034 PSP LOAD REJECT) will be generated for display and downlist. When this occurs, PSP communication will not be resumed until either PSP is enabled again via keyboard input. This parameter value will be reset when a subsequent command load is accepted.

While PSP communication is enabled, the SM application will request a status message from the PSP. This request will be initiated every 80 msec if a command load is in progress and at least once per second if no command load is in progress. The status word will be made available for display and downlist, and illegal message checking performed per Section 32.4.6. If this evaluation indicates that the PSP can accept a new configuration message, the command load will be transmitted to the PSP at least 1.2 ms after the last request for status and before the next cyclic request for status. This command load contains the appropriate configuration message (plus the MDM command word) and the first set of P/L CDWs (up to 32) (plus the MDM command word). This configuration message and the P/L CDWs will be retained until the next or a subsequent PSP cyclic status message indicates a valid bit combination of 100 or 110. Until this occurs, the software responds to the PSP per Section 32.4.6. When the bit combination 100 or 110 occurs, the software transmits the remainder (if any) of the command load at least 1.2 ms after the last status message request (and before the next cyclic request for status) and continues evaluating subsequent status messages as defined above.

If a CC SPEC or uplink command load is received for transfer to the PSP while a transfer is in progress, the load is rejected and a discrete parameter value (S49034) is enabled for display and/or downlist to indicate that the load was rejected. This parameter value will be reset when a subsequent command load is accepted.

If a standard GNC data transfer or Inertial Upper Stage (IUS) GNC data transfer requests a data transfer to the PSP while a transfer is in progress, the data transfer is held until current PSP processing is complete.

A load transfer will be defined to be in progress from the time the load is initially accepted by the PSP software for output to the hardware until either the load is successfully output by the hardware or the load transfer is stopped due to an OPS transition, a reinitialize configuration message output request is received, or a PSP status message BCE element bypass occurs.

If the complete load is not transmitted to the PSP due to an error condition specified above or an OPS transition, the remaining load will be cleared and a discrete parameter value (S49004 PSP CMD load transfer incomplete) will be enabled indicating that an incomplete command load was transferred to the PSP. This parameter value will be disabled when a subsequent command load (nonreinitialize load) transfer is initiated. When a load is cleared, the user must retransmit the load via uplink or reinitiate it via keyboard or PCS if the load was generated onboard.

If another load is in progress when a PSP command load containing a configuration message ID=0 is executed, the load in progress will be terminated and a discrete parameter value (S49004 PSP CMD load transfer incomplete) will be enabled indicating that an incomplete command load was transferred to the PSP. This parameter value will be disabled when a subsequent command load transfer is initiated. When a command is rejected or an incomplete load is output, the flag corresponding to the source of the rejected command will also be set on. The flags and command sources are:

| Flag   | Nomenclature             | Command Source          |
|--------|--------------------------|-------------------------|
| S49164 | PSP TEC reject flag      | TEC                     |
| S49167 | PSP sequence reject flag | PCS                     |
| S49620 | PSP uplink reject flag   | UPLINK                  |
| S49261 | PSP GNC XFER reject flag | IUS GNC or STANDARD GNC |
| S49262 | PSP CC SPEC reject flag  | CC SPEC                 |

All of these flags shall be reset when any subsequent PSP command (that does not contain configuration message ID 0) is initiated. A count (S49258) of the number of PSP loads that are rejected or output incompletely will be maintained by the PSP software.

### 32.4.6 Illegal Message Checking

| BIT CONFIGURATION               |                  |                            | Action   |
|---------------------------------|------------------|----------------------------|--|
| N<br>E<br>W<br>D<br>A<br>T<br>A | B<br>U<br>S<br>Y | R<br>E<br>P<br>E<br>A<br>T |  |
| 0                               | 0                | 0                          | Illegal Message: Request status request at the next cyclic time. After three retries, notify crew that illegal status message received via a discrete parameter (S49095) value available for display and/ or downlist. When the status message is valid, reset the indication. |
| 0                               | 0                | 1                          | Illegal Message: Refer to above procedure for code (000).  |
| 0                               | 1                | 0                          | PSP Busy: Request status request at next cyclic 80 ms.   |
| 0                               | 1                | 1                          | Illegal Message: Refer to above procedure for code (000).  |
| 1                               | 0                | 0                          | PSP able to accept old configuration message and command/data message or a new configuration message and command data message.   |
| 1                               | 0                | 1                          | Repeat last command/data message configuration message.  |
| 1                               | 1                | 0                          | PSP able to accept old configuration message and new command/data message but not a new configuration message.   |
| 1                               | 1                | 1                          | Repeat last configuration message and command/data message.  |

#### 32.4.6.1 PSP Configuration and Command Message Rejection

If the configuration or command messages are rejected due to errors, the PSP will request a repeat of the last transmission and indicate whether the error was in the configuration message or the command message via the status message. The PSP will reject both the configuration and command data messages if

- A. The new configuration message does not contain exactly five 16-bit words
- B. Both command input/output buffers (3.2.1.2.2.2 SM LVL B CPDS) contain data to be transmitted

- C. The new configuration message is different than the current configuration message while command data are being transmitted according to the instructions in the current configuration message
- D. The command message does not contain 32 16-bit command words

## 32.5 INSTALLATION

### 32.5.1 Location

Avionics bay 2

### 32.5.2 Temperature Control

Coldplate

## 32.6 DESCRIPTION OF OPERATION

### 32.6.1 Ground Commands

Uplink OP codes which indicate that data are to be transferred to P/Ls via interfaces described in Section 32.9 will be processed as described in this section. Refer to the downlist/uplink CPDS, SS-P-0002-140, for a description of the uplink formats.

#### 32.6.1.1 Payload Uplink Data Format

For each P/L data uplink OP code, control information will be contained for a 16-bit control word. The control word will be formatted as defined in the downlist/uplink CPDS, SS-P-0002-140, and will contain the following fields.

#### A. Destination

Indicates the destination of this uplink operation. Valid destinations are

1. PSP communication (refer to Section 32.7)
2. Standard Serial I/O (SSI)
3. Spacelab Simulator I/O (SLSIO)

#### B. Destination dependent

Contains data used to determine the specific output to perform. It has meaning depending on the destination as follows.

1. For the PSP, this field will indicate the PSP configuration message to be processed.
2. For an SSI, this field will indicate the ID of the SSI via which the data shall be output. Valid SSI IDs for each mission will be specified in the P/L FSSR.

3. For SLSIO, this field will indicate the Spacelab (SL) computer (experiment or subsystem computer) to which the data will be output.

C. Number of data words

Indicates the number of data words to be output. Valid values depend on the destination. The control word followed by the number of 16-bit data words specified by this field shall be made available to the destination interface.

### 32.6.1.2 P/L Data Load

A P/L data load command can be used to request transfer of data to P/Ls via the PSP, SSI, or SLSIO interface. The uplinked data will consist of a control word followed by the data words. The definition of this command is specified in Section 6.3.25 of the downlist/ uplink CPDS, SS-P-0002-140. The fields in the control word will be checked for legal values. If all fields are valid, the uplinked data are made available to the destination interface. If any field is invalid or if an output to an SSI or the SLSIO interface cannot be processed because the specified interface is busy with a previous request of this type, the command will be rejected, and an indication (S51034), UPLINK INVALID REQUEST, will be made available for downlist and display. This indication will be reset when a subsequent P/L data uplink is successfully processed.

### 32.6.1.3 TEC

A TEC will be used to request transfer of data to P/Ls at a specified time via the PSP, SSI, or SLSIO interface. The uplink command will contain a Greenwich Mean Time (GMT) time of execution followed by a control word and data words.

For a TEC, the maximum number of data words in addition to the control words shall be 63. The capability will exist to store 25 TECs concurrently. All TEC storage locations will be initialized to zeros following any SM OPS transition. When a TEC is received, it will be stored for execution at the time specified in the command if fewer than 25 TECs are currently in storage. If 25 TECs are already in storage, the new TEC will be rejected and an indication (TEC STORAGE FULL) made available for display and downlist. This indication will be reset when a TEC is accepted or a TEC BUFFER CLEAR command is received. An indication of the number of TECs in storage will be maintained and will be available for display and downlist. The definition of this command is specified in Section 6.3.32 of the downlist/uplink CPDS, SS-P-0002-140.

The fields of the control word will be checked for legal values as specified in Section 6.3.32 of the downlist/uplink CPDS. If any field is invalid, the command will be rejected and an indication (UPLINK INVALID REQUEST) made available for downlist and display. This indication will be reset when a subsequent P/L data uplink is successfully processed. If all fields are valid, the uplinked data will normally be made available to the specified interface within 2 seconds of the time of execution. If the interface is busy, the TEC command will be made available to the interface within 2 seconds of the time processing of prior requests is completed.

If the GMT time of execution has already occurred when a valid TEC is received, the data will be made available to the specified interface within 2 seconds of receipt by SM unless the interface is busy, in which case the TEC shall be processed as above. The sequential order of execution will be the time order of execution times associated with the commands. If more than one command has the same time of execution, they may be executed in any order. When a TEC has been executed, the storage it occupied will become available for a subsequent uplink.

When a TEC BUFFER CLEAR command is received via uplink, the entire contents of TEC storage will be set to zeros.

#### **32.6.1.4 P/L Throughput Command**

A P/L throughput command can be used to request transfer of data to P/Ls via the PSP, SSI or SLSIO interface. This is a special type of two-stage command as described in Section 6.2 of the downlist/uplink CPDS, SS-P-0002-140. Otherwise, processing of this command is the same as that described for the P/L data load, Section 32.10.1. The definition of this load is specified in Section 6.3.40 of the downlist/uplink CPDS, SS-P-0002-140.

#### **32.6.1.5 Standard GNC Data Transfer**

The capability exists to process orbiter GNC state vector and attitude data obtained via Intercomputer Communication Channel (ICC) for output to P/Ls via the SSIs or the PSP function in response to Process Control Indication (PCIs). This GNC data transfer may be either cyclic via SSIs or on demand via SSIs or the PSP and may consist of any one of the following time-homogenous data sets.

- A. Greenwich True of Date (GTOD) state vector
- B. GTOD attitude/attitude rate
- C. Aries Mean of 50 (M50) state vector
- D. M50 attitude/attitude rate

All parameters are single precision floating point except for the timetags and orbiter position which are double precision floating point parameters and the header words which are integers.

Up to eight PCIs (ON/OFF item entries on CC SPECS) are supported for GNC data transfer. The PL FSSR specifies (on a mission basis) which data set is to be transferred when a specific PCI is on, whether the transfer is to be cyclic or one-shot and the destination (SSI or PSP) of the transfer. It will also specify the PSP configuration ID or the SSI ID as appropriate. While a PCI for a cyclic transfer is on, a request is generated every 1.92 seconds to output the corresponding data set via the specified interface. When a PCI for a one-shot transfer is turned on, a single request is generated to output the corresponding data set via the specified interface, and the PCI is turned off. This request is generated within 2 seconds of the time the PCI is turned

on unless the specified interface is busy, in which case the request will be generated within 2 seconds of the time the interface completes processing of prior requests. The initial state is OFF when SM is initialized from mass memory of each of these indicators.

### 32.6.1.6 IUS GNC Data Transfer

The capability exists to transfer orbiter GNC state vector and attitude data to the IUS via the PSP and an MDM SIO channel. The GNC data are acquired via the ICC as defined in Section 4.1.5.1.1 of the SM Level B CPDS. The two data sets (state vector data and attitude data) will each be processed as a time-homogeneous data set so that parameters from two different ICC updates for a set are not used in one IUS transfer.

### 32.6.2 Telemetry

- V74S3206E - Switch select PSP on, OI, 1 s/s, 1 = on
- V74S3207E - Switch select payload interrogator on, OI, 1 s/s, 1 = on
- V74X4890E - GCIL PSP 1 on, OI, 1 s/s, 1 = on
- V74X4891E - GCIL PSP 2 on, OI, 1 s/s, 1 = on
- V74X4894E - PSP out PI, indicates that the PSP command path is through the PI, OI, 1 s/s, 1 = PI selected
- V74X4895E - PSP out umbilical, indicates that the PSP command path is through the umbilical, OI, 1 s/s, 1 = umbilical selected
- V74X6000E - PSP 1 frame sync, indicates that PSP 1 has achieved frame sync, OI, 1 s/s, 1 = frame sync
- V74X6001E - PSP 2 frame sync, indicates that PSP 2 has achieved frame sync, OI, 1 s/s, 1 = frame sync
- V74X6002E - PSP 1 bit sync, indicates that PSP 1 has achieved bit sync, OI, 1 s/s, 1 = bit sync
- V74X6003E - PSP 2 bit sync, indicates that PSP 2 has achieved bit sync, OI, 1 s/s, 1 = bit sync
- V92X0325X - PSP 1 bypassed, indicates PSP 1 is not communicating with the SM GPC, 1 s/s, 1 = bypass
- V92X0329X - PSP 2 bypassed, indicates PSP 2 is not communicating with the SM GPC, 1 s/s, 1 = bypass
- V92X0809X - PSP idle on, indicates the PSP idle pattern is enabled and no command data are being transmitted, GPC, 1 s/s, 1 = idle on

V92X1102X - PSP load reject, indicates that a PSP load has been rejected, GPC, 1 s/s, 1 = reject

V92X1124X - PSP invalid request, indicates an uplinked command field is invalid or an output to an interface cannot be processed because the specified interface is busy, GPC, 1 s/s, 1 = invalid

V92X1127X - PSP u/l reject, indicates an uplinked command has been rejected, GPC, 1 s/s, 1 = reject

### 32.6.3 Special Telemetry Computations

M01G3203R - Command rate, this indicates the selected PSP command rate

V92J0807C - Selected PSP payload command rate

|   |   |   |   |        |
|---|---|---|---|--------|
| 0 | 1 | 0 | 0 | 125/16 |
| 0 | 1 | 0 | 1 | 125/8  |
| 0 | 1 | 1 | 0 | 125/4  |
| 0 | 1 | 1 | 1 | 125/2  |
| 1 | 0 | 0 | 0 | 125    |
| 1 | 0 | 0 | 1 | 250    |
| 1 | 0 | 1 | 0 | 500    |
| 1 | 0 | 1 | 1 | 1000   |
| 1 | 1 | 0 | 0 | 2000   |

Any other combination is invalid.

M01G3204R - Frame length, this indicates the selected PSP frame length

V92J0823C - Selected PSP telemetry frame length

|                       |      |
|-----------------------|------|
| 0 0 0 0 0 0 0 0 0 0 1 | 1    |
| 0 0 0 0 0 0 0 0 0 1 0 | 2    |
| 0 0 0 0 0 0 0 0 0 1 1 | 3    |
| •                     |      |
| •                     |      |
| •                     |      |
| 0 1 1 1 1 1 1 1 1 1 1 | 1023 |
| 1 0 0 0 0 0 0 0 0 0 0 | 1024 |

Any other combination is output (blank).



M02G3202R - Umbilical select, this indicates the PSP umbilical selected

V92J0817C - Selected PSP umbilical selected

|   |   |   |             |
|---|---|---|-------------|
| 0 | 0 | 0 | (blank)     |
| 0 | 0 | 1 | Umbilical 1 |
| 0 | 1 | 0 | Umbilical 2 |
| 0 | 1 | 1 | Umbilical 3 |
| 1 | 0 | 0 | Umbilical 4 |
| 1 | 0 | 1 | Umbilical 5 |

M02G3203R - Word length, this indicates the number of bits in the frame sync word

V92J0818C - Selected PSP frame sync bit length

|   |   |   |         |
|---|---|---|---------|
| 0 | 0 | 1 | 8 bits  |
| 0 | 1 | 0 | 16 bits |
| 0 | 1 | 1 | 24 bits |
| 1 | 0 | 0 | 32 bits |

M03G3203R - Data rate, this indicates the selected PSP telemetry rate

V92J0815C - Selected PSP telemetry rate

|   |   |   |         |
|---|---|---|---------|
| 0 | 0 | 1 | 1 kbps  |
| 0 | 1 | 0 | 2 kbps  |
| 0 | 1 | 1 | 4 kbps  |
| 1 | 0 | 0 | 8 kbps  |
| 1 | 0 | 1 | 16 kbps |

M04G3203R - Data type, this indicates the selected PSP command type

V92J0808C - Selected PSP payload command data type

|   |   |         |
|---|---|---------|
| 0 | 1 | NRZ-L   |
| 1 | 0 | NRZ-M   |
| 1 | 1 | NRZ-S   |
| 0 | 0 | Invalid |

M05G3203R - PI/umbilical, this indicates which selected PSP output has been selected

|           |                                       |
|-----------|---------------------------------------|
| V92X0810X | Selected PSP P/L Intgr command select |
| V92X0811X | Selected PSP P/L Umb output select    |
| V92X0812X | Selected PSP GSE output select        |

| V92X0810X | V92X0811C | V92X0812X |         |
|-----------|-----------|-----------|---------|
| 0         | 0         | 0         | BLANK   |
| 0         | 0         | 1         | GSE UMB |
| 0         | 1         | 0         | P/S UMB |
| 0         | 1         | 1         | BTH UMB |
| 1         | 0         | 0         | INTEROG |
| 1         | 0         | 1         | INT UMB |
| 1         | 1         | 0         | INT P/L |
| 1         | 1         | 1         | ALL     |

M11I0603R - Data type, this indicates the selected PSP TLM data type

V92J0816C - Selected PSP telemetry data type

|   |   |   |     |    |   |
|---|---|---|-----|----|---|
| 0 | 0 | 1 | B1  | PH | L |
| 0 | 1 | 0 | B1  | PH | M |
| 0 | 1 | 1 | B1  | PH | S |
| 1 | 0 | 0 | NRZ | L  |   |
| 1 | 0 | 1 | NRZ | M  |   |
| 1 | 1 | 0 | NRZ | S  |   |

Any other combination is invalid.

### 32.7 REFERENCES

Payload Signal Processor, Preliminary Design Data Package, Volume 1, SCTE-61-79-095, May 4, 1979.

Payload Signal Processor Specification, MC476-0138, July 17, 1981.

Space Shuttle orbiter Avionics Software, Operational Detailed Design Specification, Volume 3, part 2, System Management, NAS 9-16920.

MCC Level B and C Requirements for Shuttle-Telemetry Data Processing, Volume 1 - Shuttle I Data Processing Complex Software, JSC-11028.

**Table 32-1. Payload signal processor communications inputs**

| M/S ID no. | Mnemon | Nomenclature                       | Source            | Type | Units | ILD |
|------------|--------|------------------------------------|-------------------|------|-------|-----|
| V93X5584X  | S49001 | PSP 1 comm enable item             | P/P SPEC V5.1.16  | I    | CNTL  |     |
| V93X5585X  | S49002 | PSP 2 comm enable item             | P/P SPEC V5.1.16a | I    | CNTL  |     |
| V74X6202J  | S49009 | PSP 1 buffer available WD1B00      | PL MDM            | D    |       |     |
| V74X6203J  | S49010 | PSP 1 processing data WD1B01       | PL MDM            | D    |       |     |
| V74X6204J  | S49011 | PSP 1 repeat message WD1B02        | PL MDM            | D    |       |     |
| V74X6205J  | S49012 | PSP 1 config message errors WD1B03 | PL MDM            | D    |       |     |
| V74X6206J  | S49013 | PSP 1 config initialized WD1B04    | PL MDM            | D    |       |     |
| V74X6207J  | S49014 | PSP 1 PL CMD message error WD1B05  | PL MDM            | D    |       |     |
| V74X6208J  | S49015 | PSP 1 new configuration MSG WD1B06 | PL MDM            | D    |       |     |
| V74J6209J  | S49016 | PSP 1 PL command rate WD1B07-10    | PL MDM            | I    |       |     |
| V74J6223J  | S49017 | PSP 1 PL CMD data type WD2B11-12   | PL MDM            | I    |       |     |
| V74X6211J  | S49018 | PSP 1 idle pattern enbl WD1B12     | PL MDM            | D    |       |     |
| V74X6212J  | S49155 | PSP 1 PL interog CMD SEL WD1B13    | PL MDM            | D    |       |     |
| V74X6213J  | S49119 | PSP 1 PL UMB output SEL WD1B14     | PL MDM            | D    |       |     |
| V74X6214J  | S49156 | PSP 1 GSE output SEL WD1B15        | PL MDM            | D    |       |     |
| V74X6216J  | S49120 | PSP 1 PL interog TLM SEL WD2B00    | PL MDM            | D    |       |     |
| V74X6217J  | S49157 | PSP 1 GSE input SEL WD2B01         | PL MDM            | D    |       |     |
| V74J6218J  | S49021 | PSP 1 TLM rate WD2B02-04           | PL MDM            | I    |       |     |
| V74J6224X  | S49022 | PSP 1 TLM data type WD2B13-15      | P/P MDM           | I    |       |     |
| V74J6210J  | S49161 | PSP 1 umbilical selected WD2B08-10 | P/P MDM           | I    |       |     |
| V74J6228J  | S49023 | PSP 1 frame sync WD LG WD8B11-13   | PL MDM            | I    |       |     |
| V74X6220J  | S49024 | PSP 1 bit sync lock WD2B06         | PL MDM            | D    |       |     |

**Table 32-1. Payload signal processor communications inputs (continued)**

| M/S ID no. | Mnemon  | Nomenclature                       | Source  | Type | Units | ILD |
|------------|---------|------------------------------------|---------|------|-------|-----|
| V74X6221J  | S49025  | PSP 1 frame sync lock WD2B07       | PL MDM  | D    |       |     |
| V74U6232J  | S49027  | PSP 1 TLM frame sync WD1 WD4       | PL MDM  | I    |       |     |
| V74U6233J  | S49165  | PSP 1 TLM frame sync WD2 WD5       | PL MDM  | I    |       |     |
| V74J6227J  | S49154  | PSP 1 TLM frame length WD3B00-10   | PL MDM  | I    |       |     |
| V91X2826X  | A11681  | PF1/PSP 1                          | SYS S/W | D    |       |     |
| V91X2828X  | A11683  | PF2/PSP 2                          | SYS S/W | D    |       |     |
| NOT REQ    | Not REQ | CC SPEC - command datab            | CC SPEC | FP   |       |     |
| V74X6302J  | S49168  | PSP 2 buffer available WD1B00      | PL MDM  | D    |       |     |
| V74X6303J  | S49169  | PSP 2 processing data WD1B01       | PL MDM  | D    |       |     |
| V74X6304J  | S49170  | PSP 2 repeat message WD1B02        | PL MDM  | D    |       |     |
| V74X6305J  | S49171  | PSP 2 config message errors WD1B03 | PL MDM  | D    |       |     |
| V74X6306J  | S49172  | PSP 2 config initialized WD1B04    | PL MDM  | D    |       |     |
| V74X6307J  | S49173  | PSP 2 PL CMD message error WD1B05  | PL MDM  | D    |       |     |
| V74X6308J  | S49174  | PSP 2 new configuration MSG WD1B06 | PL MDM  | D    |       |     |
| V74J6309J  | S49175  | PSP 2 PL command rate WD1B07-10    | PL MDM  | D    |       |     |
| V74X6321J  | S49177  | PSP 2 idle pattern enbl WD1B12     | PL MDM  | I    |       |     |
| V74X6322J  | S49178  | PSP 2 PL interog CMD SEL WD1B13    | PL MDM  | I    |       |     |
| V74X6323J  | S49179  | PSP 2 PL UMB output SEL WD1B14     | PL MDM  | D    |       |     |
| V74X6324J  | S49180  | PSP 2 GSE output SEL WD1B15        | PL MDM  | D    |       |     |
| V74X6326J  | S49181  | PSP 2 PL interog TLM SEL WD2B00    | PL MDM  | D    |       |     |
| V74X6327J  | S49182  | PSP 2 GSE input SEL WD2B01         | PL MDM  | D    |       |     |
| V74X6328J  | S49183  | PSP 2 TLM rate WD2B02-04           | PL MDM  | I    |       |     |
| V74J6324J  | S49184  | PSP 2 TLM data type WD2B13-15      | PL MDM  | I    |       |     |
| V74J6320J  | S49185  | PSP 2 umbilical selected WD2B08-10 | PL MDM  | I    |       |     |
| V74J6328J  | S49186  | PSP 2 frame sync WD LG WD3B11-13   | PL MDM  | I    |       |     |
| V74X6320J  | S49187  | PSP 2 bit sync lock WD2B06         | PL MDM  | D    |       |     |
| V74X6321J  | S49188  | PSP 2 frame sync lock WD2B07       | PL MDM  | D    |       |     |
| V74U6332J  | S49189  | PSP 2 TLM frame sync WD 1 WD4      | PL MDM  | I    |       |     |
| V74U6333J  | S49190  | PSP 2 TLM frame sync WD 2 WD5      | PL MDM  | I    |       |     |
| V74J6327J  | S49191  | PSP 2 TLM frame length WD3B00-10   | PL MDM  | I    |       |     |

<sup>a</sup>The vehicle utility payload interface control spec function sources in this table are used in preflight OPS (SM9 and GNC9). The P/P spec sources are used in SM flight ops.

<sup>b</sup>Item entry on a cargo control spec (refer to Section 5.1.7.4 SM CPDS) can request output of prestored data to a payload via the PSP.

**Table 32-2. Payload signal processor communications outputs**

| M/S ID no. | Mnemon | Nomenclature                       | Destination |        | Type | Units |
|------------|--------|------------------------------------|-------------|--------|------|-------|
|            |        |                                    | Function    | DD/ILS |      |       |
| V92X0800X  | S49192 | Selected PSP buffer available      | PC SPEC     | X      | D    |       |
| V92X0801X  | S49193 | Selected PSP processing data       |             | X      | D    |       |
| V92X0802X  | S49194 | Selected PSP repeat message        |             | X      | D    |       |
| V92X0803X  | S49195 | Selected PSP config message errors |             | X      | D    |       |
| V92X0804X  | S49196 | Selected PSP config initialized    |             | X      | D    |       |
| V92X0805X  | S49197 | Selected PSP PL CMD message error  |             | X      | D    |       |
| V92X0806X  | S49198 | Selected PSP new configuration MSG |             | X      | D    |       |
| V92J0807C  | S49199 | Selected PSP command rate          |             | X      | I    |       |
| V92J0808X  | S49200 | Selected PSP CMD data type         |             | X      | I    |       |
| V92X0809X  | S49201 | Selected PSP pattern enbl          |             | X      | D    |       |
| V92X0810X  | S49202 | Selected PSP PL enterog CMD SEL    |             | X      | D    |       |
| V92X0811X  | S49203 | Selected PSP PL UMB output SEL     |             | X      | D    |       |
| V92X0812X  | S49204 | Selected PSP GSE output SEL        |             | X      | D    |       |
| V92X0813X  | S49205 | Selected PSP PL interog TLM SEL    |             | X      | D    |       |
| V92X0814X  | S49206 | Selected PSP GSE input SEL         |             | X      | D    |       |
| V92J0815C  | S49207 | Selected PSP TLM rate              |             | X      | I    |       |
| V92J0816C  | S49208 | Selected PSP TLM data type         |             | X      | I    |       |
| V92J0817C  | S49209 | Selected PSP umbilical selected    |             | X      | I    |       |
| V92J0818C  | S49219 | Selected PSP frame sync WD log     |             | X      | I    |       |
| V92X0819X  | S49211 | Selected PSP sync lock             |             | X      | D    |       |
| V92X0820X  | X49212 | Selected PSP frame sync lock       |             | X      | D    |       |
| V92X0820X  | S49212 | Selected PSP frame sync lock       |             | X      | D    |       |
| V92J0821C  | S49213 | Selected PSP TLM frame sync WD1    |             | X      | I    |       |
| V92J0822C  | S49214 | Selected PSP TLM frame sync WD2    |             | X      | I    |       |
| V92J0823C  | S49215 | Selected PSP TLM frame length      |             | X      | I    |       |
| V92X1102X  | S49034 | PSP load rejected                  |             | X      | D    |       |
| V92J1103C  | S49035 | Last PSP configuration MSG ID      |             | X      | I    |       |
| V92X1110X  | S49005 | PSP 1 BCE element bypass reset     |             | X      | D    |       |
| V92X1111X  | S49006 | PSP 2 BCE element bypass reset     | SYS S/W     | X      | D    |       |
| V74X6237J  | S49043 | PSP 1 reinitialize WD1B00          | SYS S/W     | X      | D    |       |
| V74J6238J  | S49045 | PSP 1 no. PL CMD words WD1B01-06   | PL MDM      |        | I    |       |
| V74J6239J  | S49046 | PSP 1 PL CMD data rate WD1B07-10   | PL MDM      |        | D    |       |
| V74J6240J  | S49047 | PSP 1 PL CMD data type WD1B11-13   | PL MDM      |        | I    |       |

**Table 32-2. Payload signal processor communications outputs (continued)**

| M/S ID no. | Mnemon | Nomenclature                      | Destination |        | Type | Units |
|------------|--------|-----------------------------------|-------------|--------|------|-------|
|            |        |                                   | Function    | DD/ILS |      |       |
| V74X6244J  | S49048 | PSP 1 CMD subcar idle patt WD2B00 | PL MDM      |        | D    |       |
| V74J6245J  | S49051 | PSP TLM bit rate WD2B01-03M SEL   | PL MDM      |        | I    |       |
| V74J6246J  | S49052 | PSP 1 TLM data type WD2B04-06     | PL MDM      |        | I    |       |
| V74J6257J  | S49053 | PSP 1 TLM frame length WD3B00-10  | PL MDM      |        | I    |       |
| V74J6258J  | S49054 | PSP 1 frame sync WD LG WD3B11-13  | PL MDM      |        | I    |       |
| V74U6262J  | S49055 | PSP 1 TLM frame sync WD1 WD4      | PL MDM      |        | I    |       |
| V74U6263J  | S49258 | PSP 1 frame sync WD2 WD5          | PL MDM      |        | HX   |       |
| V74K6247J  | S49162 | PSP 1 config MSG - UMB select     | PL MDM      |        | I    |       |
| V74U6265J  | S49056 | PSP 1 PL command word 1 WD6       | PL MDM      |        | HX   |       |
| V74U6266J  | S49057 | PSP 1 PL command word 2 WD7       | PL MDM      |        | HX   |       |
| V74U6267J  | S49058 | PSP 1 PL command word 3 WD8       | PL MDM      |        | HX   |       |
| V74U6268J  | S49059 | PSP 1 PL command word 4 WD9       | PL MDM      |        | HX   |       |
| V74U6269J  | S49060 | PSP 1 PL command word 5 WD10      | PL MDM      |        | HX   |       |
| V74U6270J  | S49061 | PSP 1 PL command word 6 WD11      | PL MDM      |        | HX   |       |
| V74U6271J  | S49062 | PSP 1 PL command word 7 WD12      | PL MDM      |        | HX   |       |
| V74U6272J  | S49063 | PSP 1 PL command word 8 WD13      | PL MDM      |        | HX   |       |
| V74U6273J  | S49064 | PSP 1 PL command word 9 WD14      | PL MDM      |        | HX   |       |
| V74U6274J  | S49065 | PSP 1 PL command word 10 WD15     | PL MDM      |        | HX   |       |
| V74U6275J  | S49066 | PSP 1 PL command word 11 WD16     | PL MDM      |        | HX   |       |
| V74U6276J  | S49067 | PSP 1 PL command word 12 WD17     | PL MDM      |        | HX   |       |
| V74U6277J  | S49068 | PSP 1 PL command word 13 WD18     | PL MDM      |        | HX   |       |
| V74U6278J  | S49069 | PSP 1 PL command word 14 WD19     | PL MDM      |        | HX   |       |
| V74U6279J  | S49070 | PSP 1 PL command word 15 WD20     | PL MDM      |        | HX   |       |
| V74U6280J  | S49071 | PSP 1 PL command word 16 WD21     | PL MDM      |        | HX   |       |
| V74U6281J  | S49072 | PSP 1 PL command word 17 WD22     | PL MDM      |        | HX   |       |
| V74U6282J  | S49073 | PSP 1 PL command word 18 WD23     | PL MDM      |        | HX   |       |
| V74U6283J  | S49074 | PSP 1 PL command word 19 WD24     | PL MDM      |        | HX   |       |
| V74U6284J  | S49075 | PSP 1 PL command word 20 WD25     | PL MDM      |        | HX   |       |
| V74U6285J  | S49076 | PSP 1 PL command word 21 WD26     | PL MDM      |        | HX   |       |
| V74U6286J  | S49077 | PSP 1 PL command word 22 WD27     | PL MDM      |        | HX   |       |
| V74U6287J  | S49078 | PSP 1 PL command word 23 WD28     | PL MDM      |        | HX   |       |
| V74U6288J  | S49079 | PSP 1 PL command word 24 WD29     | PL MDM      |        | HX   |       |
| V74U6289J  | S49080 | PSP 1 PL command word 25 WD30     | PL MDM      |        | HX   |       |

**Table 32-2. Payload signal processor communications outputs (continued)**

| M/S ID no. | Mnemon | Nomenclature                      | Destination |        | Type | Units |
|------------|--------|-----------------------------------|-------------|--------|------|-------|
|            |        |                                   | Function    | DD/ILS |      |       |
| V74U6290J  | S49081 | PSP 1 PL command word 26 WD32     | PL MDM      |        | HX   |       |
| V74U6291J  | S49082 | PSP 1 PL command word 27 WD32     | PL MDM      |        | HX   |       |
| V74U6292J  | S49083 | PSP 1 PL command word 28 WD33     | PL MDM      |        | HX   |       |
| V74U6293J  | S49084 | PSP 1 PL command word 29 WD34     | PL MDM      |        | HX   |       |
| V74U6294J  | S49085 | PSP 1 PL command word 30 WD35     | PL MDM      |        | HX   |       |
| V74U6295J  | S49086 | PSP 1 PL command word 32 WD36     | PL MDM      |        | HX   |       |
| V74U6296J  | S49087 | PSP 1 PL command word 32 WD37     | PL MDM      |        | HX   |       |
| V74X6337J  | S49216 | PSP 2 reinitialize WD1B00         | PL MDM      |        | D    |       |
| V74J6338J  | S49217 | PSP 2 no. PL CMD words WD1B01-06  | PL MDM      |        | I    |       |
| V74J6339J  | S49218 | PSP 2 PL CMD data rate WD1B07-10  | PL MDM      |        | I    |       |
| V74J6340J  | S49219 | PSP 2 PL CMD data rate WD1B11-13  | PL MDM      |        | I    |       |
| V74X6344J  | S49220 | PSP 2 CMD subcar idle patt WD2B00 | PL MDM      |        | D    |       |
| V74J6345J  | S49221 | PSP 2 TLM bit rate WD2B01-03      | PL MDM      |        | I    |       |
| V74J6346J  | X49222 | PSP 2 TLM data type WD2B04-06     | PL MDM      |        | I    |       |
| V74J6357J  | S49223 | PSP 2 TLM frame length WD3B00-10  | PL MDM      |        | I    |       |
| V74J6358J  | S49224 | PSP 2 frame sync WD log WD3B11-13 | PL MDM      |        | I    |       |
| V74U6362J  | S49225 | PSP 2 TLM frame sync WD 1 WD4     | PL MDM      |        | HX   |       |
| V47U6363J  | S49258 | PSP 2 frame sync WD 2 WD5         | PL MDM      |        | HX   |       |
| V74K6347J  | S49259 | PSP 2 config MSG - UMB select     | PL MDM      |        | I    |       |
| V74U6365J  | S49226 | PSP 2 PL command word 1           | PL MDM      |        | HX   |       |
| V74U6366J  | S49227 | PSP 2 PL command word 2 WD7       | PL MDM      |        | HX   |       |
| V74U6367J  | S49228 | PSP 2 PL command word 3 WD8       | PL MDM      |        | HX   |       |
| V74U6368J  | S49229 | PSP 2 PL command word 4 WD9       | PL MDM      |        | HX   |       |
| V74U6369J  | S49230 | PSP 2 PL command word 5 WD10      | PL MDM      |        | HX   |       |
| V74U6370J  | S49232 | PSP 2 PL command word 6 WD11      | PL MDM      |        | HX   |       |
| V74U6371J  | S49232 | PSP 2 PL command word 7 WD12      | PL MDM      |        | HX   |       |
| V74U6372J  | S49233 | PSP 2 PL command word 8 WD13      | PL MDM      |        | HX   |       |
| V74U6373J  | S49234 | PSP 2 PL command word 9 WD14      | PL MDM      |        | HX   |       |
| V74X6374J  | S49235 | PSP 2 PL command word 10 WD15     | PL MDM      |        | HX   |       |
| V74U6375J  | S49236 | PSP 2 PL command word 11 WD16     | PL MDM      |        | HX   |       |
| V74J6376J  | S49237 | PSP 2 PL command word 12 WD17     | PL MDM      |        | HX   |       |
| V74J6377J  | S49238 | PSP 2 PL command word 13 WD18     | PL MDM      |        | HX   |       |
| V74X6378J  | S49239 | PSP 2 PL command word 14 WD19     | PL MDM      |        | HX   |       |
| V74J6379J  | S49240 | PSP 2 PL command word 15 WD20     | PL MDM      |        | HX   |       |

**Table 32-2. Payload signal processor communications outputs (continued)**

| M/S ID no. | Mnemon | Nomenclature                     | Destination |        | Type | Units |
|------------|--------|----------------------------------|-------------|--------|------|-------|
|            |        |                                  | Function    | DD/ILS |      |       |
| V74J6380J  | S49241 | PSP 2 PL command word 16 WD21    | PL MDM      |        | HX   |       |
| V74J6381J  | S49242 | PSP 2 PL command word 17 WD22    | PL MDM      |        | HX   |       |
| V74U6382J  | S49243 | PSP 2 PL command word 18 WD23    | PL MDM      |        | HX   |       |
| V74U6383J  | S49244 | PSP 2 PL command word 19 WD24    | PL MDM      |        | HX   |       |
| V47U6384J  | S49245 | PSP 2 PL command word 20 WD25    | PL MDM      |        | HX   |       |
| V74U6385J  | S49246 | PSP 2 PL command word 21 WD26    | PL MDM      |        | HX   |       |
| V74U6386J  | S49247 | PSP 2 PL command word 22 WD27    | PL MDM      |        | HX   |       |
| V74U6387J  | S49248 | PSP 2 PL command word 23 WD28    | PL MDM      |        | HX   |       |
| V74U6388J  | S49249 | PSP 2 PL command word 24 WD29    | PL MDM      |        | HX   |       |
| V74U6389J  | S49250 | PSP 2 PL command word 25 WD30    | PL MDM      |        | HX   |       |
| V74U6390J  | S49251 | PSP 2 PL command word 26 WD32    | PL MDM      |        | HX   |       |
| V74U6391J  | S49252 | PSP 2 PL command word 27 WD32    | PL MDM      |        | HX   |       |
| V74U6392J  | S49253 | PSP 2 PL command word 28 WD33    | PL MDM      |        | HX   |       |
| V74U6393J  | S49254 | PSP 2 PL command word 29 WD34    | PL MDM      |        | HX   |       |
| V74U6394J  | S49255 | PSP 2 PL command word 30 WD35    | PL MDM      |        | HX   |       |
| V74X6395J  | S49256 | PSP 2 PL command word 32 WD36    | PL MDM      |        | HX   |       |
| V74U6396J  | S49257 | PSP 2 PL command word 32 WD37    | PL MDM      |        | HX   |       |
| V92X1115X  | S49095 | PSP illegal status msg           |             |        | D    |       |
| V92X1116X  | S49004 | PSP CMD load transfer incomplete |             | X      | D    |       |
| V92X1120X  | S49164 | PSP TEC reject flag              |             | X      | D    |       |
| V92X1121X  | S49167 | PSP sequence reject flag         | PCS FTNa    | X      |      | D     |
| V92X1127X  | S49260 | PSP uplink reject flag           | TCS FTNa    | X      | D    |       |
| V92X1128X  | S49261 | PSP GNC XFER reject flag         |             | X      | D    |       |
| V92X1129X  | S49262 | PSP CC SPEC reject flag          |             | X      | D    |       |
| V92X1124X  | S51034 | Uplink invalid request           |             | X      | D    |       |
| V92J1104C  | S49258 | PSP load reject/INC counter      |             | X      | I    |       |

<sup>a</sup>The TCS function destination applies to preflight OPS (SM 9 and GNC 9). The PCS function destination applies to SM flight OPS.



**Table 32-3. Initial PSP configuration**

|                                  |   |
|----------------------------------|---|
| Payload command rate             | 2 kbps  |
| Payload command data type        | NRZ-L   |
| Command data subcarrier          | 16 kHz sine wave<br>No modulation   |
| Idle pattern                     | Disabled  |
| Telemetry rate                   | 16 kbps   |
| Telemetry data type              | B-phase L   |
| Telemetry frame length           | 64 8-bit words  |
| Telemetry frame sync word length | 32 bits   |
| Telemetry frame sync word        | All "1's"   |
| Subcarrier output (16 kHz)       | Output to P/L umbilical, P/L interrogator, or<br>GSE umbilical is inhibited |
| Subcarrier inpt (1.024 mHz)      | Input from P/L interrogator or GSE umbilical is<br>inhibited                |

**SECTION 33 - PAYLOAD DATA INTERLEAVER**  
**CONTENTS**

| <b>Section</b> |  | <b>Page</b> |
|----------------|--|-------------|
| 33.1           | GENERAL DESCRIPTION.....   | 33-1        |
| 33.2           | INTERFACES .....   | 33-1        |
| 33.2.1         | Control and Display.....   | 33-2        |
| 33.2.2         | Payload Data.....  | 33-6        |
| 33.2.3         | PDI Health and Status.....   | 33-7        |
| 33.2.4         | PDI Wraparound Test .....  | 33-7        |
| 33.2.5         | Timing .....   | 33-7        |
| 33.3           | SPECIFICATIONS .....   | 33-8        |
| 33.3.1         | Receiver and Switching Matrix.....                                 | 33-8        |
| 33.3.2         | Decommutator.....  | 33-10       |
| 33.3.3         | Word Sync.....   | 33-12       |
| 33.3.4         | Word Selector .....  | 33-22       |
| 33.3.5         | Status Register.....   | 33-25       |
| 33.3.6         | Toggle Buffer.....   | 33-25       |
| 33.3.7         | Data RAM.....  | 33-25       |
| 33.3.8         | FPM and Toggle Buffer Identifier .....                             | 33-26       |
| 33.3.9         | Built-In Test Equipment.....                                       | 33-29       |
| 33.3.10        | PDI Timing .....   | 33-30       |
| 33.3.11        | IRIG Decoder Operation .....                                       | 33-36       |
| 33.3.12        | Data Bus Descriptions.....   | 33-37       |
| 33.3.13        | Power .....  | 33-39       |
| 33.3.14        | Temperature Data .....   | 33-39       |
| 33.3.15        | Location.....  | 33-39       |
| 33.3.16        | IFM.....   | 33-39       |
| 33.4           | SOFTWARE SPECIFICATION .....                                       | 33-39       |
| 33.4.1         | Shuttle Standard Formats .....                                     | 33-39       |
| 33.4.2         | PDI Load Process Overview .....                                    | 33-44       |
| 33.4.3         | Switch Matrix Read .....   | 33-47       |
| 33.4.4         | PDI Data Transfer to the PCMMU.....                                | 33-55       |
| 33.4.5         | FDA Processing for S62 PDI Decom Fail.....                         | 33-55       |
| 33.5           | TELEMETRY.....   | 33-57       |
| 33.5.1         | OI Telemetry .....   | 33-57       |
| 33.5.2         | SM.....  | 33-58       |
| 33.5.3         | Special COMPs.....   | 33-58       |
| 33.6           | OPERATIONAL NOTES .....  | 33-58       |
| 33.6.1         | Idiosyncrasies .....   | 33-58       |
| 33.6.2         | Decom Format Constraints .....                                     | 33-59       |
| 33.6.3         | Payloads .....   | 33-59       |
| 33.7           | ANOMALIES .....  | 33-60       |
| 33.7.1         | SFMDM Warm Starts and PDI False Lock Indications (IFA INCO-04).... | 33-60       |

| Section                       | Page  |
|-------------------------------|-------|
| 33.7.2 I/O Buffer Babble..... | 33-60 |
| 33.8 REFERENCES.....          | 33-60 |

## TABLES

### Table

|                                     |       |
|-------------------------------------|-------|
| 33-1 PDI BITE status words .....    | 33-4  |
| 33-2 DFL numbers .....              | 33-4  |
| 33-3 Switch matrix connection.....  | 33-9  |
| 33-4 Bit sync configuration .....   | 33-14 |
| 33-5 FPM/TBI/TB relationships ..... | 33-27 |
| 33-6 BSR bit descriptions .....     | 33-31 |
| 33-7 OP code table .....            | 33-48 |

## FIGURES

### Figure

|  |       |
|--|-------|
| 33-1 PDI interfaces.....                 | 33-2  |
| 33-2 SPEC 62 .....                       | 33-3  |
| 33-3 PDI subsections and interfaces..... | 33-8  |
| 33-4 Switch matrix.....                  | 33-10 |
| 33-5 Decommutator bit synchronizer.....  | 33-10 |
| 33-6 DCM map basic organization .....    | 33-13 |
| 33-7 Formats.....                        | 33-17 |
| 33-8 FCT, type 1 formats .....           | 33-18 |
| 33-9 FCT, type 2 formats .....           | 33-19 |
| 33-10 FCT, type 3 formats .....          | 33-20 |
| 33-11 FCT, type 4 formats .....          | 33-20 |

## SECTION 33 PAYLOAD DATA INTERLEAVER

### 33.1 GENERAL DESCRIPTION

The Payload Data Interleaver (PDI) design dates to 1977. Harris Corporation designed and built the PDI as well as the Pulse-Code Modulation Master Unit (PCMMU). The PDI contains four decommutators (decoms). The PDI can receive asynchronous data from multiple payloads and store the data internally for retrieval by the PCMMU.

The PDI has seven inputs: five are hardline inputs for attached payloads, the sixth input is for one of the two Payload Signal Processors (PSPs) for detached payloads, and the seventh is used for ground testing. The PDI can process asynchronous data from one to four payloads simultaneously. Each input is directed to a decom that converts the data to Non-Return-to-Zero Level (NRZ-L) (with clock); provides bit, word, and frame sync; and stores data to be retrieved by the PCMMU.

The PDI data are retrieved by the PCMMU in a demand/response fashion for Systems Management (SM) General Purpose Computer (GPC) display and for downlink. The SM GPC has an interface to the PDI that allows it to load Decom Format Loads (DFLs), Fetch Pointer Memory (FPM) Fetch Pointer Loads (FPLs), and configure the switch matrix. The SM GPC reads the DFLs and FPLs during the load process for verification and polls the switch matrix once per second for decom input selection.

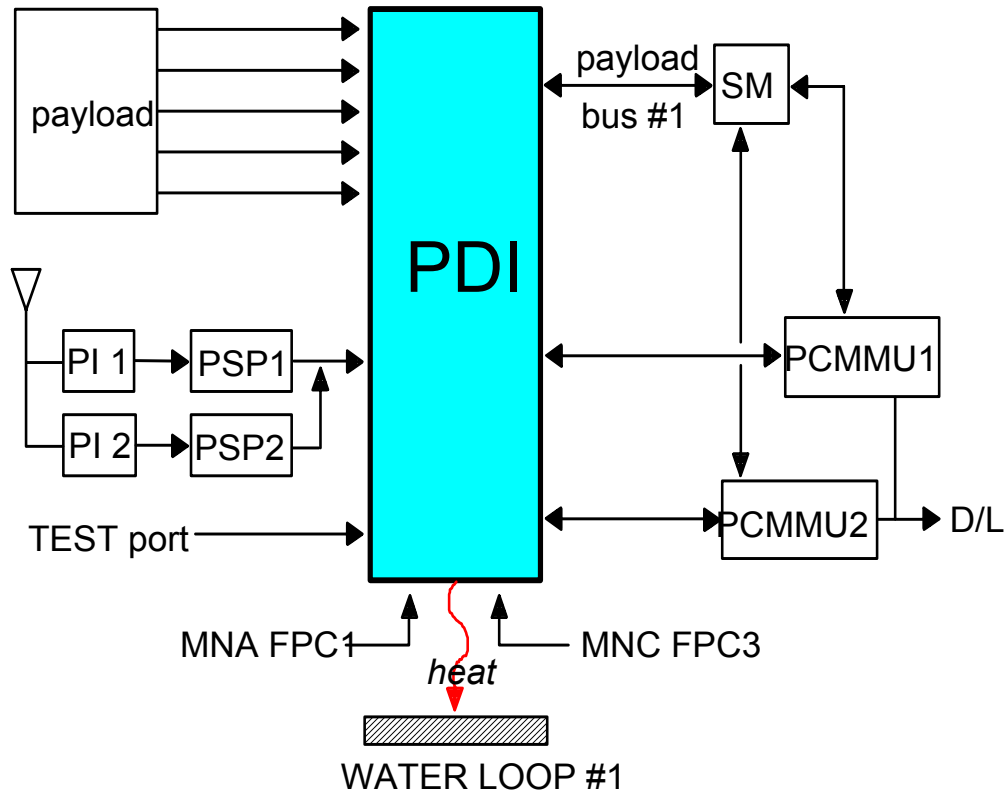
There are seven PDIs in existence: one for each vehicle, two spares, and one located in the Shuttle Avionics Integration Laboratory (SAIL). If needed, the project can borrow a PDI from the Crew Equipment Integration Tester (CEIT); the CEIT has three PDIs (not flight qualified).

### 33.2 INTERFACES

The PDI interfaces with payloads via five hardline cables to the payload bay area and two hardline cables to the PSPs for acquisition of Radio Frequency (RF) data. All payload links are one-way (return link only). See Figure 33-1.

The PDI interfaces with both PCMMUs and an SM or G9 GPC through two-way data buses. All three interfaces are identical, with the exception of the Multiple Interface Adapter (MIA) address. The PDI responds only to specific commands from either a PCMMU or SM GPC and does not initiate any transactions (i.e., demand/response).

There are three timing interfaces: Interrange Instrumentation Group B (IRIG-B) time and 1.152 MHz PCMMU 1 and 2 clocks. All timing interfaces are receive only and are not necessary for basic PDI operations.



**Figure 33-1. PDI interfaces**

### 33.2.1 Control and Display

The PDI to SM GPC interface is provided by Payload Bus 1 (PL1). PDI configuration changes are commanded by the SM GPC. The configuration changes DFLs, FPLs, Fault Detection and Annunciation (FDA) inhibit/enable (affects SM alert tones only), or decom source selection (switch matrix changes). The configuration changes are initiated via SPEC 62 item entry (Section 33.2.1.1.2) or ground uplink loads (Section 33.2.1.2). DFLs and FPL data are stored on the Mass Memory Units (MMUs) (detailed discussion in Sections 33.4.2.2 and 33.4.2.3, respectively).

The PDI power is controlled by one Ground Control Interface Logic (GCIL) switch, located on Panel A1L S17 (see Section 33.2.1.1.1)

#### 33.2.1.1 Crew Control and Displays

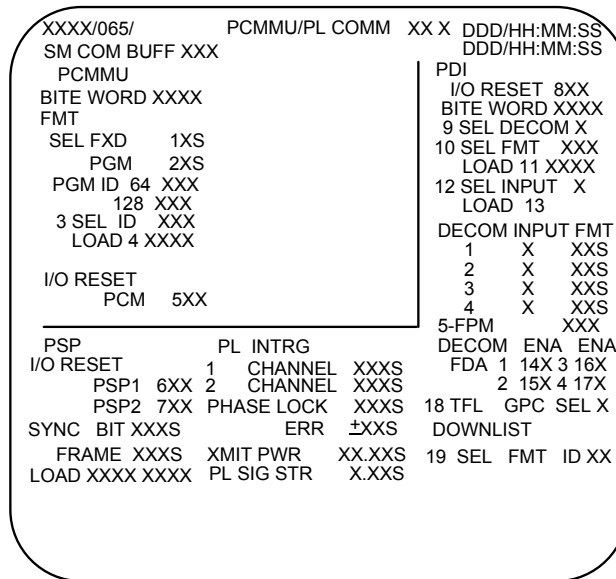
The following sections contain information about the crew's PDI insight and PDI control.

##### 33.2.1.1.1 Panel A1L

Refer to SSSH drawing 20.2, sheet 1, zone U6. The PDI power switch is always in the ON position. The S\_BAND P/L CONTROL switch must be in PANEL for the PDI power switch to be active. All Instrumentation and Communications Officer (INCO) console positions have a quick panel reference on console.

### 33.2.1.1.2 SPEC 62, PCMMU/PL COMM

SPEC 62 (Figure 33-2) is used to configure and monitor the PDI while the SM GPC is in Operational Sequence (OPS) 2 or 4. SPEC 62 is also used in major mode G9 for prelaunch PDI configuration.



**Figure 33-2. SPEC 62**

SPEC 62 inputs/display fields related to the PDI are as follows:

**A. SM COM BUFF (SM common buffer)**

This data field displays the status of the common buffer that is used to load the DFL and the FPL into the PDI. Indications are RDY (ready) and a flashing BSY (busy). All keyboard entries are rejected if a flashing BSY is displayed, and the process currently using the SM common buffer will continue until nominal completion. If a load attempt is rejected because of a BSY common buffer, wait until the common buffer is RDY, then reattempt load. The common buffer will be busy when the MMU is in use (i.e., TFL/DFL/FPLs, Mass Memory Patch, Mass Memory Read/Write, TM SPEC, P/P SPEC, SM Checkpoint).

**B. PDI I/O RESET (item 8)**

This item is used to restore the PDI to SM GPC interface. This action is necessary if the PDI switch matrix read element is bypassed. An overbright "M" is displayed when the switch matrix read element is bypassed, and an "\*" is displayed when it is not bypassed.

**C. PDI BITE WORD**

This field is a hex display of PDI Built-In Test Equipment (BITE) status word 2. See Table 33-1 for a detailed description.

**Table 33-1. PDI BITE status words**

| BITE word1 |                     | BITE word 2 |                               |
|------------|---------------------|-------------|-------------------------------|
| Bit        | Description         | Bit         | Description                   |
| 0          | Master Frame Lock 1 | 0           | No Response Data Bus 1        |
| 1          | Word Lock 1         | 1           | Input Data Invalid Data Bus 1 |
| 2          | Bit Lock 1          | 2           | No Response Data Bus 2        |
| 3          | Bit Rate Accuracy 1 | 3           | Input Data Invalid Data Bus 2 |
| 4          | Master Frame Lock 2 | 4           | No Response Data Bus 3        |
| 5          | Word Lock 2         | 5           | Input Data Invalid Data Bus 3 |
| 6          | Bit Lock 2          | 6           | Toggle Buffer Parity Good     |
| 7          | Bit Rate Accuracy 2 | 7           | Data RAM Parity Good          |
| 8          | Master Frame Lock 3 | 8           | FPM Parity Good               |
| 9          | Word Lock 3         | 9           | DCM 1 Parity Good             |
| 10         | Bit Lock 3          | 10          | DCM 2 Parity Good             |
| 11         | Bit Rate Accuracy 3 | 11          | DCM 3 Parity Good             |
| 12         | Master Frame Lock 4 | 12          | DCM 4 Parity Good             |
| 13         | Word Lock 4         | 13          | MTU IRIG Good                 |
| 14         | Bit Lock 4          | 14          | PCMMU 1.152 MHz Good          |
| 15         | Bit Rate Accuracy 4 | 15          | Power Status                  |

D. SEL DECOM (item 9)

This item is used to select the decom (1-4) to be loaded or FPM (5).

E. SEL FMT (item 10)

This item is used to select the format that is to be loaded into the decom or FPM selected by item 9.

The legal DFL numbers have been assigned in blocks as shown in Table 33-2.

**Table 33-2. DFL numbers**

| DFL number |
|------------|
| 1-11       |
| 14-19      |
| 27-31      |

The legal FPL numbers have been assigned as follows: 501-525. The data associated with FPLs are generated preflight by the PDI compiler. Refer to Section 33.3.8, FPM and Toggle Buffer Identifier.

F. LOAD (item 11)

This item is used to initiate the selections made in items 9 and 10.

G. SELECT INPUT (item 12)

This item is used to select the input (source) for the decom specified by item 9. Legal values are 0-6. Selecting source 0 for the decom disconnects any payload source and inhibit processing by the decom, as well as eliminating spurious FDA messages (refer to Section 33.4.5, FDA Processing for S62 PDI Decom Fail).

H. LOAD (item 13)

This item is used to initiate the selection made in items 9 and 12.

I. DECOM INPUT FMT

These fields are used to display the current payload inputs assigned to each decom and the last loaded format of the decoms and the FPM.

If the SM is re-IPL'd after loading the PDI, SPEC 62 will display all zeros for decom load values even though the PDI decoms are operating properly. Typically, the crew or ground will reload the decoms to reflect the actual PDI status.

If the PDI to SM GPC interface is interrupted, causing a S62 BCE BYP PDI message, SPEC 62 continues to display the proper PDI switch matrix and format load configuration.

If a decom drops lock, an up arrow, ↑, is displayed next to the associated decom format data field.

If the PDI is power cycled, all sources, DFLs, and FPLs must be reloaded.

J. DECOM ENABLE (items 14 to 17)

These are used to alternately enable and disable the FDA for the associated decom. An "\*" is displayed next to the item when the FDA is enabled. This field is blank when the FDA is disabled. FDA processing is described in Section 33.4.5, FDA Processing.

### 33.2.1.2 Ground Control and Displays

The following sections contain information regarding ground controller PDI insight and PDI control. The SCPs referred to are in the INCO/COMM Console Handbook, JSC-12829.

#### 33.2.1.2.1 Loads

All SPEC 62 PDI ITEM entries can be performed via ground uplink command loads. The INST COMMAND BUILD application should be used to build the DFLs and FPLs.



The FDA INH/ENA and PDI I/O RESET loads are prebuilt. Before any PDI loads are uplinked, ensure that the crew is not using or has buried SPEC 62. The load will fail if SPEC 62 is active. To determine if SPEC 62 is active, refer to the Variable Parameter (VP) for SPEC 62 on the orbit INST MGMT display.

### 33.2.1.2.2 Displays

The following displays are normally used:

A. ASCENT/ENTRY INST MANAGEMENT

This display contains the ascent- and entry-related Operational Instrumentation (OI) PDI parameters, as well as the MCC-computed PDI Wraparound (WRAP) status.

B. INST MANAGEMENT

This display contains the PDI WRAP, SPEC 62, orbit-related OI PDI parameters, as well as some SM PDI parameters.

C. COMM & INST BYPASS

This display contains the SM bypass status.

D. PCMMU EVENT

This display contains the emulated Digital Display Drivers (DDD) for the SM PCMMU element bypass status.

E. PDI

This display contains all parameters for the PDI.

F. ELOG

The Event Logger (ELOG) application captures selected PDI telemetry changes, with their appropriate timetags.

### 33.2.2 Payload Data

The PDI can interface with payloads via hardline or RF. There are five hardline inputs. Hardline inputs are typically for attached payloads. If flown, the Extended Range Payload Communications Link (ERPCL) is connected to hardline input no. 5; refer to Systems Brief 34 for a detailed description of the ERPCL. RF inputs are routed from one of two PI/PSPs via hardline or via the ERPCL. All payload links are one way: payload data flowing into the PDI.

### 33.2.3 PDI Health and Status

PDI telemetry parameters are included in the OI downlist and SM downlist. PDI OI status parameters are fetched by the PCMMU from the PDI BITE Status Register (BSR), the PDI Decom Control Memory (DCM), and the PDI switch matrix register.

The SM GPC requests, via the PL1 bus, that the PDI switch matrix register status once per second and announces an S62 BCE BYP PDI message if the switch matrix read fails twice in succession. The SM GPC reads and stores the decom format, source, and FPL only during the loading process; these static values are cyclically downlisted and displayed on SPEC 62. The SM also fetches the PDI BSR data once per second from the PCMMU, displays word 2 on SPEC 62, and uses word 1 in its PDI decom FDA processing. The SM also maintains and downlists decom FDA enable/inhibit status.

See Section 33.6, MSIDs, for a list of the MSIDs and associated descriptions.

### 33.2.4 PDI Wraparound Test

The PDI Wraparound (WRAP) is the same as the Multiplexer/Demultiplexer (MDM) WRAP. The PCMMU issues an 8-bit validation word at 10 samples per second, which the PDI turns around for downlink. The OIMON processor performs the WRAP Computation (COMP). The WRAP COMP is performed on two consecutive samples and fails if the second sample is not the 1's complement of the first. If a PDI WRAP remains on the display, it indicates a loss of communication between the PDI and PCMMU. The S62 BCE BYP PL message will be announced.

### 33.2.5 Timing

Three timing interfaces exist. One of these, IRIG-B time, is used to timetag payload data. The PDI also takes a 1.152-MHz clock from the active PCMMU to time sync the PDI and PCMMU. All timing interfaces are receive-only and are not necessary for basic PDI operations.

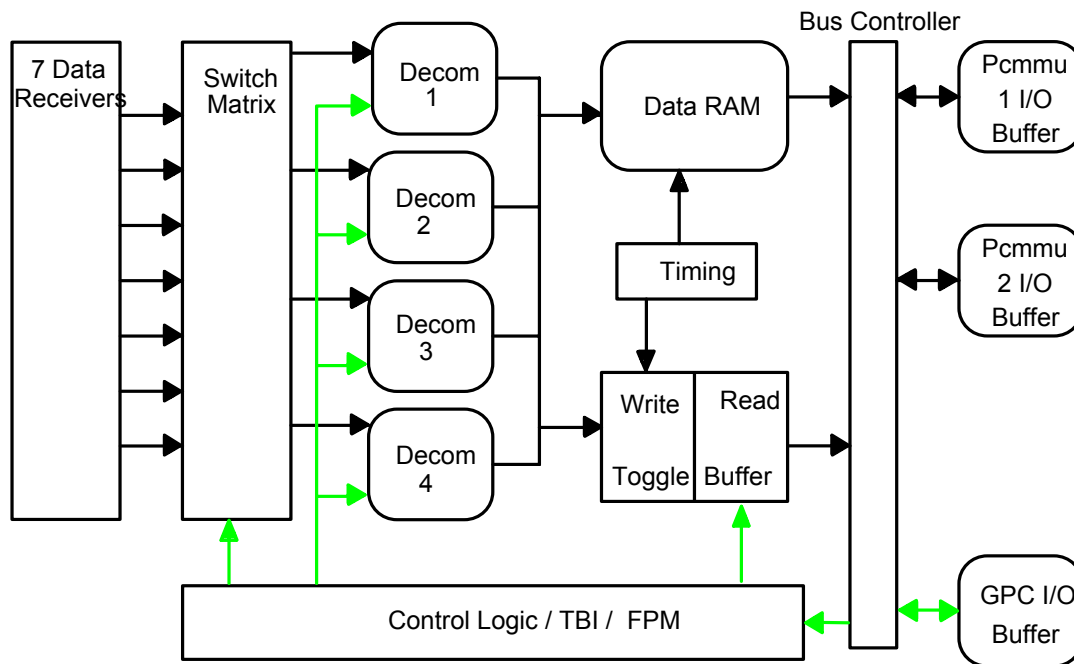
If the MTU IRIG-B input is lost, the PDI uses the 1.152 MHz PCMMU signal to generate a 1-kHz timing signal. The PDIs MTU IRIG-B circuitry is very sensitive; false MTU BAD indications have occurred.

The PDI has an internal 4.608-MHz oscillator that is used if the PCMMU timing source goes out of tolerance or ceases.

See Section 33.3.10, PDI Timing.

### 33.3 SPECIFICATIONS

PDI subsections and interfaces are shown in Figure 33-3.



**Figure 33-3. PDI subsections and interfaces**

#### 33.3.1 Receiver and Switching Matrix

The receiver section consists of seven data receivers and seven NRZ clock receivers. Each data receiver has an associated NRZ clock receiver and is considered a pair. Each pair is capable of handling between 10 bps to 64 kbps (regardless of data code type). For differential inputs, a discrete level is defined by (plus or minus) 2 to 9 volts difference between inputs (less than a 2-volt difference is indeterminate). For single-ended inputs, a high level is detected between 1.5 and 4.5 volts above ground (low level is less than 1.5 volts).

The switching matrix (Figure 33-4) can route data from any of the payload data and NRZ clock receivers (if provided by the payload) to any of the four bit synchronizers. Any input may be routed to one or more bit synchronizers. This will be controlled by the switch matrix control logic. Each channel select receives all seven data/clock pair inputs and routes the selected pair to the bit synchronizer associated with that channel select logic. The channel selects are controlled by the channel select registers. The registers receive inputs from the “load switch matrix” command data word (Table 33-3).

**Table 33-3. Switch matrix connection**

| <b>Bits<br/>1\2</b> | <b>Output to bit<br/>synchronizer no.</b> | <b>Bits<br/>3/4/5</b> | <b>Function</b>    |
|---------------------|---|-----------------------|--------------------|
| 00                  | 1   | 000                   | No connection      |
| 01                  | 2   | 001                   | Payload input 1    |
| 10                  | 3   | 010                   | Payload input 2    |
| 11                  | 4   | 011                   | Payload input 3    |
|                     |   | 100                   | Payload input 4    |
|                     |   | 101                   | Payload input 5    |
|                     |   | 110                   | PSP input          |
|                     |   | 111                   | Special test input |

**Switch matrix read**

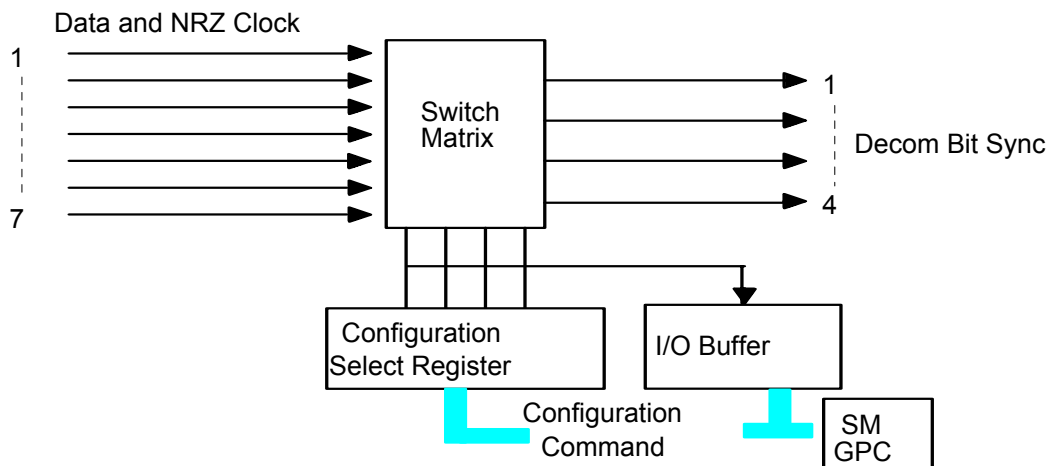
| <b>Switch</b>         | <b>Matrix 1</b>       | <b>Switch</b>         | <b>Matrix 2</b>       |
|-----------------------|-----------------------|-----------------------|-----------------------|
| <b>Bits<br/>1/2/3</b> | <b>Input function</b> | <b>Bits<br/>4/5/6</b> | <b>Input function</b> |
| 000                   | No connection         | 000                   | No connection         |
| 001                   | Payload input 1       | 001                   | Payload input 1       |
| 010                   | Payload input 2       | 010                   | Payload input 2       |
| 011                   | Payload input 3       | 011                   | Payload input 3       |
| 100                   | Payload input 4       | 100                   | Payload input 4       |
| 101                   | Payload input 5       | 101                   | Payload input 5       |
| 110                   | PSP input             | 110                   | PSP input             |
| 111                   | Special test input    | 111                   | Special test input    |

| <b>Switch</b>         | <b>Matrix 3</b>       | <b>Switch</b>            | <b>Matrix 4</b>       |
|-----------------------|-----------------------|--------------------------|-----------------------|
| <b>Bits<br/>7/8/9</b> | <b>Input function</b> | <b>Bits<br/>10/11/12</b> | <b>Input function</b> |
| 000                   | No connection         | 000                      | No connection         |
| 001                   | Payload input 1       | 001                      | Payload input 1       |
| 010                   | Payload input 2       | 010                      | Payload input 2       |
| 011                   | Payload input 3       | 011                      | Payload input 3       |
| 100                   | Payload input 4       | 100                      | Payload input 4       |
| 101                   | Payload input 5       | 101                      | Payload input 5       |
| 110                   | PSP input             | 110                      | PSP input             |
| 111                   | Special test input    | 111                      | Special test input    |

The registers serve three purposes, as follows:

- To select inputs to bit synchronizers
- To inhibit data during decommutator memory loading
- To set switch matrix to no select on powerup or power interruptions over 0.4 ms

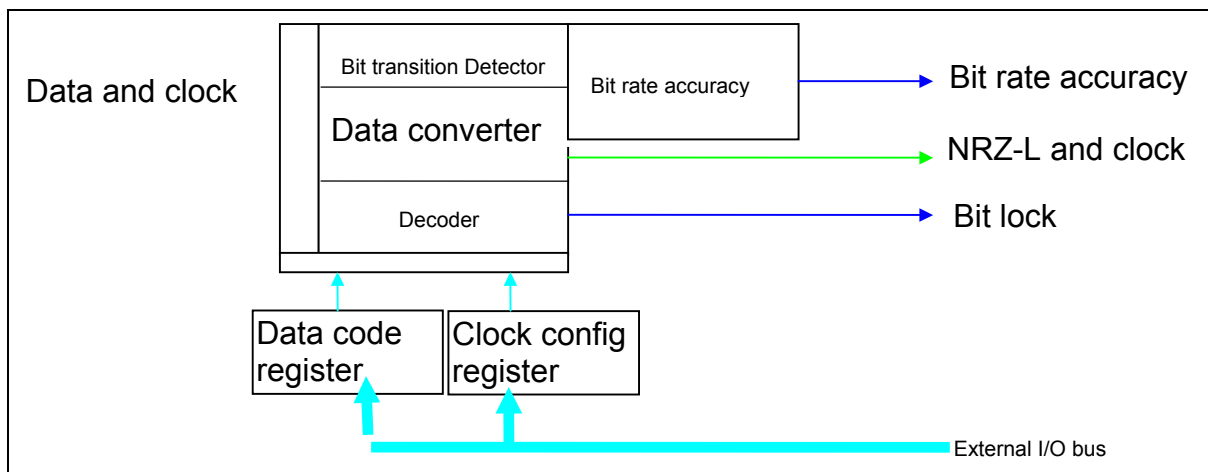
The registers may also be interrogated by the SM GPC for configuration (Table 33-3). This will not interrupt data flow to the bit synchronizers.



**Figure 33-4. Switch matrix**

### 33.3.2 Decommutator

The decom will use information from the DFL to synchronize to the payload data so that the data can be stored in the toggle buffer and data RAM locations. See Figure 33-5.



**Figure 33-5. Decommutator bit synchronizer**

### 33.3.2.1 Bit Sync Section

This section is used to convert input data as received from the payloads into NRZ-L with a clock signal.

Six different code formats may be accepted as input

- A. NRZ-L - non-return-to-zero level
- B. NRZ-M - non-return-to-zero mark
- C. NRZ-S - non-return-to-zero space
- D. Biphas-level
- E. Biphas-mark
- F. Biphas-space

A clock signal is received with the NRZ codes, but not with the biphas codes.

#### 33.3.2.1.1 Bit Sync Configuration

The bit sync configuration circuit is made up of two registers loaded by the external input bus.

- A. Data code register: Contains a 3-bit code which defines the expected input code format.
- B. Clock configuration register: Contains a 19-bit code which defines the expected data rate.

The bit rate, accuracy, and code are checked against the values stored in the Format Constant Table (FCT) as received from the Input/Output (I/O) data port via DFL data.

#### 33.3.2.1.2 Biphas Input Data Path

This circuit is used to generate a clock signal for biphas data. It is made up of two parts, a frequency synthesizer and a counter.

- A. Frequency synthesizer

Contains a 16-MHz oscillator that is routed through a divider circuit configured by the clock configuration register.

- B. Counter

The counter is initialized at each transition of the biphas data. Biphas codes are characterized by transitions either at the beginning of the bit period or at the midpoint of the bit period. The counter is set up to count to  $\text{freq}/2$ . If there is no mid-bit transition, the counter will roll over and count through the second half and

generate the decode pulse (the maximum number of half-bit periods that can occur without a transition is two).

#### **33.3.2.1.3 Code Detection Circuit**

Three consecutive half-bit periods are compared to the expected code type characteristics to resolve bit stream ambiguity. The resolved bit periods are then converted to NRZ-L with clock and passed onto the data selector.

#### **33.3.2.1.4 NRZ Input Data Path**

NRZ payload data bypasses the clock generation circuit and the code detection circuit. The data enters the data converter circuit to be converted from NRZ-S or NRZ-M to NRZ-L. After the conversion, the data is passed through the data selector to the decom. The clock signal is passed through the clock selector to the decom.

#### **33.3.2.1.5 Bit Lock**

The DCM load inhibit acts on the bit lock circuit through the second latch. The bit lock discrete is passed onto the word sync and bit rate accuracy circuits and is part of the BITE status word 1.

#### **33.3.2.1.6 Bit Rate Accuracy Circuit**

The bit rate accuracy tests are made by comparing the incoming bit clock with a reference counter derived from the expected bit rate. Two reference counters are used, one for the NRZ-L clock and the other for the reference signal from the frequency synthesizer. When the NRZ-L counter has counted pulses, a comparison is made with the reference counter. If the actual signal is within  $\pm 6$  bits of the reference signal, it is considered within tolerance. If not, the bit error tolerance latch is set. It should be noted that the bit accuracy check does not affect bit lock. Bit lock can be achieved within  $\pm 10$  bits of the expected bit rate. Bit Rate Accuracy indication is part of the BITE Status Word 1.

### **33.3.3 Word Sync**

The word sync section receives NRZ-L clock, data, and bit lock status from the bit sync section. Two modes of operation are possible: format synchronization and block.

#### **33.3.3.1 Format Synchronization**

In the format synchronization mode the detection of three modes of sync type 1, 2, or 3 is possible under decom control. Type 1 is master frame sync only. Type 2 is minor frame sync with a master frame sync every  $N^{\text{th}}$  minor frame. Type 3 is a minor frame sync with a minor frame count. The format synchronization mode sets up the word sync section to detect the embedded sync word in the incoming data stream. The sync words are programmable and up to four 8-bit words can be used (Table 33-4). The I/O port loads up to four holding registers with the sync pattern for use in four comparator registers. The number of holding registers and comparators used is determined by the

number of sync bits used but only in multiples of 8 bits up to 32 bits. There is no provision for bit error tolerance. The comparators are verified each shift clock period until a match occurs with the sync holding registers and the incoming data shift registers. When a match occurs a bit counter is enabled and dumps the contents of the first incoming shift register into a word holding register. The word counter is also initialized when a match occurs and increments each word time (8 bits). One of the features of the PDI is that it detects sync patterns either in the beginning position or trailing position. The type (leading or lagging) determines the initialization of the word counter. The type is determined by the decom (Table 33-4).

The word count is passed to the decom control logic and sets the word lock discrete. The decom control logic then counts words and commands a sync word check at the expected incoming sync time. The word counter is reset at the end of every minor or master frame. The decom logic inhibits transfer into the word holding register or comparing logic if the bit lock discrete is not set by the bit sync section in the format synchronization mode.

**33.3.3.2 Block Mode**

In the block mode the incoming data stream is grouped into 8-bit words and transferred for further processing.

Block mode operation in the word sync section is treated differently than format sync. If the block mode is selected by the decom (Table 33-4), the incoming data are shifted into the shift register and, if bit lock is present, will transfer this 8-bit word to the word-holding register. The decom logic also receives the word lock discrete because the word counter is enabled after the receipt of 8 bits of data.

The decom section contains the programmable information necessary to select, route, steer, and identify all master frames, minor frames and individual 8-bit words for processing. This is accomplished by the DCM control over the word selector.

**33.3.3.3 Decom Control Memory**

The DCM is organized as four major sections: the word table, the FCT, the initialization tables, and the sample rate tables (Table 33-6).

|            |                                |
|------------|--------------------------------|
| Word 0-511 | OPCODE Constants (Word Tables) |
| 512-519    | Format Constants               |
| 520-575    | Initialization Tables          |
| 576-2045   | Sample Rate Subsections        |
| 2046       | All Zeros Checksum             |
| 2047       | DCM Load Checksum              |

**Figure 33-6. DCM map basic organization**



**Table 33-4. Bit sync configuration**

Values are stored in words 517 (16 bits) and 518 (bits 1-3). 19-bit code

BR synthesis (NRZ)  

$$BR = \frac{4 \times 10^{+6}}{N}$$

| Values of N | Bit rate      |
|-------------|---------------|
| 1           | 4 MHz         |
| 2           | 2 MHz         |
| 3           | 1.33 MHz      |
| 61          | 65.573 kHz    |
| 62          | 64.516 kHz    |
| 63          | 63.492 kHz    |
| 1999        | 2.001 kHz     |
| 2000        | 2.000 kHz     |
| 2001        | 1.999 kHz     |
| 399,998     | 10.0000500 Hz |
| 399,999     | 10.0000250 Hz |
| 400,000     | 10,0000000 Hz |
| 524,284     | 7.6294527 Hz  |
| 524,285     | 7.6294382 Hz  |
| 524,286     | 7.6294236 Hz  |

Word 518 (bits 4-16)

| Word  | Bits       | Format        | Description   |     |            |       |  |       |            |       |           |       |            |       |          |       |            |       |           |       |            |       |          |
|-------|------------|---------------|---|-----|------------|-------|--|-------|------------|-------|-----------|-------|------------|-------|----------|-------|------------|-------|-----------|-------|------------|-------|----------|
| 518   | 5-7        | Types 1,2,3,4 | The data code field which defines one of six bit period formats. The following chart defines the format of the data code field.   |     |            |       |  |       |            |       |           |       |            |       |          |       |            |       |           |       |            |       |          |
|       |            |               | <table border="1"> <thead> <tr> <th>Bit</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>7 6 5</td> <td></td> </tr> <tr> <td>0 0 0</td> <td>Bi-φ SPACE</td> </tr> <tr> <td>0 0 1</td> <td>Bi-φ MARK</td> </tr> <tr> <td>0 1 0</td> <td>Bi-φ LEVEL</td> </tr> <tr> <td>0 1 1</td> <td>NOT USED</td> </tr> <tr> <td>1 0 0</td> <td>NRZ- SPACE</td> </tr> <tr> <td>1 0 1</td> <td>NRZ- MARK</td> </tr> <tr> <td>1 1 0</td> <td>NRZ- LEVEL</td> </tr> <tr> <td>1 1 1</td> <td>NOT USED</td> </tr> </tbody> </table> | Bit | Definition | 7 6 5 |  | 0 0 0 | Bi-φ SPACE | 0 0 1 | Bi-φ MARK | 0 1 0 | Bi-φ LEVEL | 0 1 1 | NOT USED | 1 0 0 | NRZ- SPACE | 1 0 1 | NRZ- MARK | 1 1 0 | NRZ- LEVEL | 1 1 1 | NOT USED |
| Bit   | Definition |               |   |     |            |       |  |       |            |       |           |       |            |       |          |       |            |       |           |       |            |       |          |
| 7 6 5 |            |               |   |     |            |       |  |       |            |       |           |       |            |       |          |       |            |       |           |       |            |       |          |
| 0 0 0 | Bi-φ SPACE |               |   |     |            |       |  |       |            |       |           |       |            |       |          |       |            |       |           |       |            |       |          |
| 0 0 1 | Bi-φ MARK  |               |   |     |            |       |  |       |            |       |           |       |            |       |          |       |            |       |           |       |            |       |          |
| 0 1 0 | Bi-φ LEVEL |               |   |     |            |       |  |       |            |       |           |       |            |       |          |       |            |       |           |       |            |       |          |
| 0 1 1 | NOT USED   |               |   |     |            |       |  |       |            |       |           |       |            |       |          |       |            |       |           |       |            |       |          |
| 1 0 0 | NRZ- SPACE |               |   |     |            |       |  |       |            |       |           |       |            |       |          |       |            |       |           |       |            |       |          |
| 1 0 1 | NRZ- MARK  |               |   |     |            |       |  |       |            |       |           |       |            |       |          |       |            |       |           |       |            |       |          |
| 1 1 0 | NRZ- LEVEL |               |   |     |            |       |  |       |            |       |           |       |            |       |          |       |            |       |           |       |            |       |          |
| 1 1 1 | NOT USED   |               |   |     |            |       |  |       |            |       |           |       |            |       |          |       |            |       |           |       |            |       |          |

**Table 33-4. Bit sync configuration (continued)**

| Word  | Bits          | Format        | Description  |     |            |       |  |     |               |     |               |     |               |     |               |
|-------|---------------|---------------|--|-----|------------|-------|--|-----|---------------|-----|---------------|-----|---------------|-----|---------------|
|       | 8-9           | Types 1,2,3,4 | <p>Format type code which defines one of four format types. The following list defines the coding.</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>9 8</td> <td></td> </tr> <tr> <td>0 0</td> <td>FORMAT TYPE 1</td> </tr> <tr> <td>0 1</td> <td>FORMAT TYPE 2</td> </tr> <tr> <td>1 0</td> <td>FORMAT TYPE 3</td> </tr> <tr> <td>1 1</td> <td>FORMAT TYPE 4</td> </tr> </tbody> </table> | Bit | Definition | 9 8   |  | 0 0 | FORMAT TYPE 1 | 0 1 | FORMAT TYPE 2 | 1 0 | FORMAT TYPE 3 | 1 1 | FORMAT TYPE 4 |
| Bit   | Definition    |               |  |     |            |       |  |     |               |     |               |     |               |     |               |
| 9 8   |               |               |  |     |            |       |  |     |               |     |               |     |               |     |               |
| 0 0   | FORMAT TYPE 1 |               |  |     |            |       |  |     |               |     |               |     |               |     |               |
| 0 1   | FORMAT TYPE 2 |               |  |     |            |       |  |     |               |     |               |     |               |     |               |
| 1 0   | FORMAT TYPE 3 |               |  |     |            |       |  |     |               |     |               |     |               |     |               |
| 1 1   | FORMAT TYPE 4 |               |  |     |            |       |  |     |               |     |               |     |               |     |               |
|       | 10-11         | Types 1,2,3   | <p>Number of 8-bit frame sync words. Bit 11 is the MSB.</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>11 10</td> <td></td> </tr> <tr> <td>0 0</td> <td>1 SYNC WORD</td> </tr> <tr> <td>0 1</td> <td>2 SYNC WORDS</td> </tr> <tr> <td>1 0</td> <td>3 SYNC WORDS</td> </tr> <tr> <td>1 1</td> <td>4 SYNC WORDS</td> </tr> </tbody> </table>   | Bit | Definition | 11 10 |  | 0 0 | 1 SYNC WORD   | 0 1 | 2 SYNC WORDS  | 1 0 | 3 SYNC WORDS  | 1 1 | 4 SYNC WORDS  |
| Bit   | Definition    |               |  |     |            |       |  |     |               |     |               |     |               |     |               |
| 11 10 |               |               |  |     |            |       |  |     |               |     |               |     |               |     |               |
| 0 0   | 1 SYNC WORD   |               |  |     |            |       |  |     |               |     |               |     |               |     |               |
| 0 1   | 2 SYNC WORDS  |               |  |     |            |       |  |     |               |     |               |     |               |     |               |
| 1 0   | 3 SYNC WORDS  |               |  |     |            |       |  |     |               |     |               |     |               |     |               |
| 1 1   | 4 SYNC WORDS  |               |  |     |            |       |  |     |               |     |               |     |               |     |               |
|       |               | Type 4        | Both bits set to ones.   |     |            |       |  |     |               |     |               |     |               |     |               |
|       | 12            | Types 1,2,3   | <p>The sync word position bit identifies the position of the frame sync bits as either the first bits or last bits within the frame. Bit 12 is set to 1 if the sync is located at the beginning of the frame.</p>  |     |            |       |  |     |               |     |               |     |               |     |               |
|       |               | Type 4        | Spare, set to a zero   |     |            |       |  |     |               |     |               |     |               |     |               |
|       | 13            | Type 2        | <p>The master frame sync position bit defines the minor frame location of the master frame location of the master frame sync bit. The master frame zero (bit 13 = 1) or the last minor frame of the master frame (bit 13 = 0).</p>   |     |            |       |  |     |               |     |               |     |               |     |               |
|       |               | Types 1,3,4   | Spare, set to a zero   |     |            |       |  |     |               |     |               |     |               |     |               |
|       | 14            | Type 3        | <p>The up/down control bit used to define the count direction for the minor frame counter. Bit 14 is set to a one for up count and is set to a zero for type 3 downcount</p>   |     |            |       |  |     |               |     |               |     |               |     |               |
|       |               | Type 1,2,4    | Spare, set to a zero   |     |            |       |  |     |               |     |               |     |               |     |               |

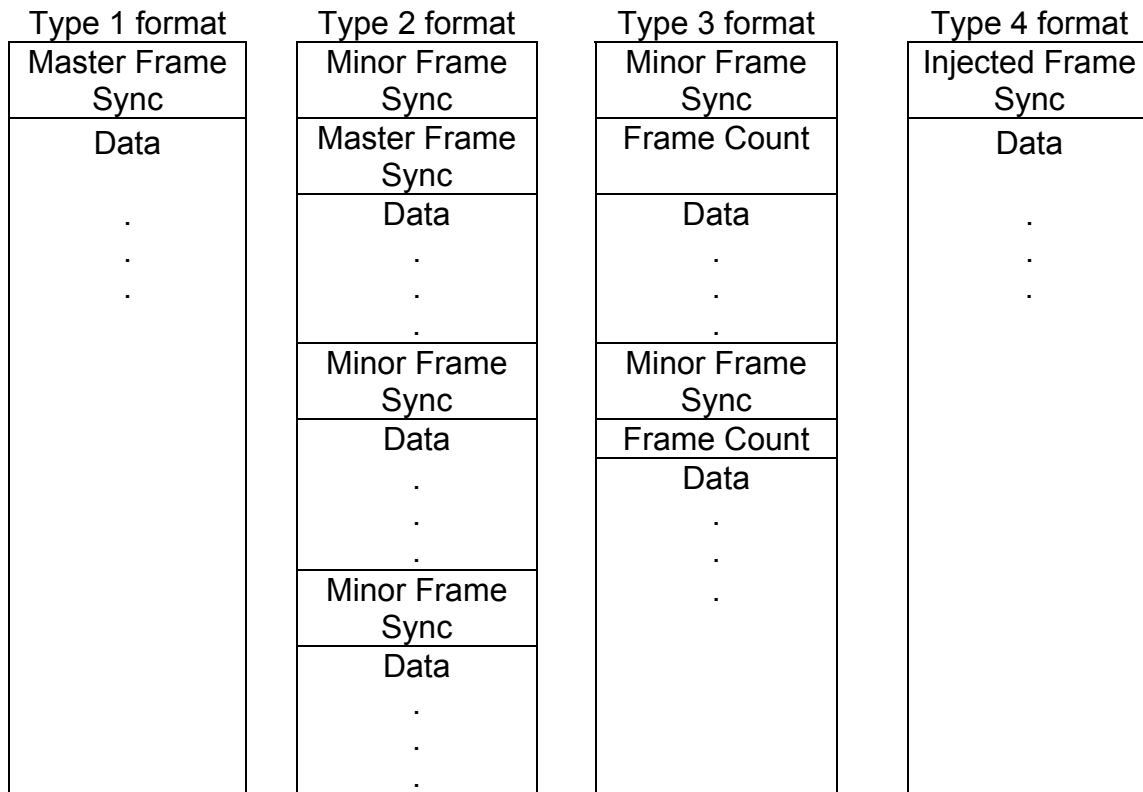
**Table 33-4. Bit sync configuration (continued)**

| Word | Bits | Format    | Description   |
|------|------|-----------|---|
| 519  | 1-10 | Type 1    | The number of 8-bit input words in the master frame (N-1).  |
|      |      | Types 2,3 | Number of 8-bit input words in a minor frame (N-1).   |
|      | 1-10 | Type 4    | The number of 8-bit input words which are grouped in a frame (N-1).   |
| 515  | 9-16 | Type 1    | Master frame sync word one. Bit 16 is MSB.  |
|      |      | Types 2,3 | Minor frame sync word one. Bit 16 is MSB.   |
|      |      | Type 4    | Spare bits, set to zeros.   |
| 515  | 1-8  | Type 1    | Master frame sync word 2. Bit 8 is MSB.   |
|      |      | Types 2,3 | Minor frame sync word 2. Bit 8 is MSB.  |
|      |      | Type 4    | Spare, set to zeros.  |
|      |      |           | Note: If format type 1, 2, or 3 has only one 8-bit sync word, bits 1-8 are set to zeros.  |
| 516  | 9-16 | Type 1    | Master frame sync word 3. Bit 16 is MSB.  |
|      |      | Types 2,3 | Minor frame sync word 3. If the format has 8 or 16 bits of sync, bits 9-16 are set to zeros. Bit 16 is the MSB.                         |
|      |      | Type 4    | Spare, set to zero.   |
| 516  | 1-8  | Type 1    | Master frame sync word 4. Bit 8 is MSB.   |
|      |      | Types 2,3 | Minor frame sync word 4. If the format has 8, 16, or 24 bits of frame sync, bits 1-8 are set to zeros. Bit 8 is the MSB of sync word 4. |
|      |      | Type 4    | Spare, set to zero.   |

**33.3.3.3.1 Word Table and FCT**

The word table is organized with a minimum of one memory word for each input data word. The memory word provides an instruction field and constant field to define the processing required on the data word. There are two basic operational types of input data words, Toggle Buffer (TB) words and data Random Access Memory (RAM) parameters. The last word in the word table has a dual instruction code to identify the processing required on the data word and to define the end of minor frame. The end of minor frame decode is used to reset the word counter. The FCT memory instruction that is assigned to the last sync word generates a check sync signal to be used by the word sync logic to verify periodic sync occurrence.

The word table and FCT must be able to process four types of input data formats. Type 1 formats have master frames with no minor frames. The number of words in the word table is equal to the number of words in a type 1 format master frame. Type 2 formats have master frames with minor frames which have a master frame sync word in the first or last minor frame. The number of words in the word table is equal to the number of words in a minor frame. Type 3 formats have master frames with minor frames that have minor frame count words. The number of words in the word table is equal to the number of words in a minor frame. Type 4 format is the block data format. The number of words in the word table is equal to the number of words in the block data frame, plus up to four additional words for sync output. See Figure 33-7.



**Figure 33-7. Formats**

A. Type 1

Type 1 formats (Figure 33-8) do not require any special operational codes in the word table other than those required to process TB and data RAM parameter data.

In this format, there is a master sync pattern once every master frame. Master frame lock is required for data storage in the toggle buffer and in the data RAM. Therefore, master frame lock is required for downlisting and for crew display.

|     |                |          |    |    |         |                |                                    |   |                |   |          |   |   |   |   |   |
|-----|----------------|----------|----|----|---------|----------------|------------------------------------|---|----------------|---|----------|---|---|---|---|---|
|     | 16             | 15       | 14 | 13 | 12      | 11             | 10                                 | 9 | 8              | 7 | 6        | 5 | 4 | 3 | 2 | 1 |
| 512 | All zeros      |          |    |    |         |                |                                    |   |                |   |          |   |   |   |   |   |
| 513 | All zeros      |          |    |    |         |                |                                    |   |                |   |          |   |   |   |   |   |
| 514 | 0              | Decom ID |    |    |         |                | Toggle Buffer Starting Address     |   |                |   |          |   |   |   |   |   |
| 515 | MF Sync Word 1 |          |    |    |         |                |                                    |   | MF Sync Word 2 |   |          |   |   |   |   |   |
| 516 | MF Sync Word 3 |          |    |    |         |                |                                    |   | MF Sync Word 4 |   |          |   |   |   |   |   |
| 517 | Bit rate       |          |    |    |         |                |                                    |   |                |   |          |   |   |   |   |   |
| 518 | 0              | 0        | 0  | 0  | MF sync | No. Sync Words | 0                                  | 0 | Data type      | 0 | Bit rate |   |   |   |   |   |
| 519 | 0              | 0        | 0  | 0  | 0       | 0              | No. of Words per Master Frame (MF) |   |                |   |          |   |   |   |   |   |

**Figure 33-8. FCT, type 1 formats**

B. Type 2

Type 2 formats (Figure 33-9) have a master frame sync word which can be any word in the minor frame. The word in the word table which corresponds to master frame sync word has a special instruction field. The bits in the instruction word adjacent to the instruction code contains the master frame sync pattern and a dedicated bit to define first or last minor frame. After a new decom load, the first master frame sync pattern compare resets the minor frame counter immediately or at the next end of minor frame, depending on the first or last minor frame bit. The constant which defines the number of minor frames in a master frame is also located in the FCT. The minor frame constant is compared to the minor frame counter to verify periodic occurrence of the master frame sync and also to reject false sync comparisons.

In this format, there is a major frame sync pattern and also a minor frame sync pattern. Two minor frame syncs are required for toggle buffer storage. Two master frame syncs, with valid minor frame syncs in all minor frames, are required for data RAM storage. Therefore, master frame lock is **not** required for downlisting. However, master frame lock **is** required for crew display.

|     |                |          |    |     |           |                   |                                   |   |                |   |          |   |   |   |   |   |
|-----|----------------|----------|----|-----|-----------|-------------------|-----------------------------------|---|----------------|---|----------|---|---|---|---|---|
|     | 16             | 15       | 14 | 13  | 12        | 11                | 10                                | 9 | 8              | 7 | 6        | 5 | 4 | 3 | 2 | 1 |
| 512 | All zeros      |          |    |     |           |                   |                                   |   |                |   |          |   |   |   |   |   |
| 513 | All zeros      |          |    |     |           |                   |                                   |   |                |   |          |   |   |   |   |   |
| 514 | 0              | Decom ID |    |     |           |                   | Toggle Buffer Starting Address    |   |                |   |          |   |   |   |   |   |
| 515 | mf Sync Word 1 |          |    |     |           |                   |                                   |   | mf Sync Word 2 |   |          |   |   |   |   |   |
| 516 | mf Sync Word 3 |          |    |     |           |                   |                                   |   | mf Sync Word 4 |   |          |   |   |   |   |   |
| 517 | Bit rate       |          |    |     |           |                   |                                   |   |                |   |          |   |   |   |   |   |
| 518 | 0              | 0        | 0  | 1/0 | mf<br>syn | No. Sync<br>Words | 0                                 | 1 | Data type      | 0 | Bit rate |   |   |   |   |   |
| 519 | 0              | 0        | 0  | 0   | 0         | 0                 | No. of Words per minor frame (mf) |   |                |   |          |   |   |   |   |   |

**Figure 33-9. FCT, type 2 formats**

C. Type 3

Type 3 formats (Figure 33-10) have minor frame count words which can occur in any word in the minor frame. The word table word which corresponds to the minor frame count word has a special instruction code, the starting minor frame count value and the up/down count instruction. After a new decom load, the first input data word count which compares to the starting minor frame count constant presets the minor frame counter to the starting minor frame count constant value. Every minor frame, after the counter preset, is compared to the input data minor frame word.

In this format, there is a sync pattern every minor frame (i.e., no major frame sync pattern) and every minor frame has a frame count. Two minor frame syncs are required for toggle buffer storage. Two successive minor frame sync patterns and minor frame count patterns are required for data RAM storage. Therefore, master frame sync is **not** required for downlist or crew display.

|     |                |          |          |    |           |                   |                                   |   |                |   |          |   |   |   |   |   |
|-----|----------------|----------|----------|----|-----------|-------------------|-----------------------------------|---|----------------|---|----------|---|---|---|---|---|
|     | 16             | 15       | 14       | 13 | 12        | 11                | 10                                | 9 | 8              | 7 | 6        | 5 | 4 | 3 | 2 | 1 |
| 512 | All zeros      |          |          |    |           |                   |                                   |   |                |   |          |   |   |   |   |   |
| 513 | All zeros      |          |          |    |           |                   |                                   |   |                |   |          |   |   |   |   |   |
| 514 | 0              | Decom ID |          |    |           |                   | Toggle Buffer Starting Address    |   |                |   |          |   |   |   |   |   |
| 515 | mf Sync Word 1 |          |          |    |           |                   |                                   |   | mf Sync Word 2 |   |          |   |   |   |   |   |
| 516 | mf Sync Word 3 |          |          |    |           |                   |                                   |   | mf Sync Word 4 |   |          |   |   |   |   |   |
| 517 | Bit rate       |          |          |    |           |                   |                                   |   |                |   |          |   |   |   |   |   |
| 518 | 0              | 0        | up<br>dn | 0  | mf<br>syn | No. Sync<br>Words | 1                                 | 0 | Data type      | 0 | Bit rate |   |   |   |   |   |
| 519 | 0              | 0        | 0        | 0  | 0         | 0                 | No. of Words per minor frame (mf) |   |                |   |          |   |   |   |   |   |

**Figure 33-10. FCT, type 3 formats**

D. Type 4 (block mode)

In this nonstandard telemetry format (Figure 33-11), the PDI does not recognize that the incoming payload data possesses any format structural properties other than bit intervals. In the block mode format, the frame sync parameter has no significance and is set to "1." The word lock parameter signifies that the word sync is grouping 8 bits of data and transferring them to the word selector. These data are not available to the crew since they are not decommutated.

|     |                |          |    |    |    |    |                                |   |                |           |   |          |   |   |   |   |
|-----|----------------|----------|----|----|----|----|--------------------------------|---|----------------|-----------|---|----------|---|---|---|---|
|     | 16             | 15       | 14 | 13 | 12 | 11 | 10                             | 9 | 8              | 7         | 6 | 5        | 4 | 3 | 2 | 1 |
| 512 | TB Sync Word 1 |          |    |    |    |    |                                |   | TB Sync Word 2 |           |   |          |   |   |   |   |
| 513 | TB Sync Word 3 |          |    |    |    |    |                                |   | TB Sync Word 4 |           |   |          |   |   |   |   |
| 514 | 0              | Decom ID |    |    |    |    | Toggle Buffer Starting Address |   |                |           |   |          |   |   |   |   |
| 515 | All zeros      |          |    |    |    |    |                                |   |                |           |   |          |   |   |   |   |
| 516 | All zeros      |          |    |    |    |    |                                |   |                |           |   |          |   |   |   |   |
| 517 | Bit rate       |          |    |    |    |    |                                |   |                |           |   |          |   |   |   |   |
| 518 | 0              | 0        | 0  | 0  | 0  | 1  | 1                              | 1 | 1              | Data type | 0 | Bit rate |   |   |   |   |
| 519 | 0              | 0        | 0  | 0  | 0  | 0  | No. of Words per block         |   |                |           |   |          |   |   |   |   |

**Figure 33-11. FCT, type 4 formats**

E. Minor frame count

The word table also contains the final count of the minor frame count sequence which is compared to the minor frame counter every time the final count instruction occurs. A final count comparison generates a minor frame counter reset to the

starting minor frame counter. Type 4 format, which is the block data format, has the capability to write decom memory constants into the TB. The word table has an instruction word for each sync word required. The bits adjacent to the instruction code stores the sync pattern.

#### F. TB data words

The word table identifies TB data words as first or second byte words. First byte words are stored in a holding register and are not processed until a second byte input word is processed. Second byte words initiate the decom control logic to write byte one and byte two simultaneously into the TB. All TB write access are on a 16-bit basis. The word table identifies the last TB assignment in the word table with a special instruction field. The decom control logic writes the data word into the TB, then enters a sequence of requesting priority, and writes a status register word into the TB. Until three status register words are written into the TB, the decom control logic sets the write end of message latch to identify the availability of the TB data set.

#### 33.3.3.3.2 Sample Rate Table

The sample rate table is organized as one to five subsections, each consisting of instructions for a dedicated sample rate. Each instruction consists of two 16-bit memory words that define the word column number, the initial minor frame count in which the parameter occurs, the data RAM address where the parameter is stored, and an operation code.

The instructions are listed in each subsection of the sample rate table in the time sequence they occur relative to master frame start. Since the word table is organized in a different word sequence than the sample rate tables, the word column number must be stored in the sample rate table.

The word table identifies a data RAM parameter by sample rate. The sample rate code selects one of five sample rate subsection address counters that are pointing at the next instruction to be processed. The double word instruction is accessed and the word count and minor frame count are checked against the word address and the selected sample rate minor frame counter respectively. If both counts compare, the input word is written into the data RAM at the address contained in the instruction. If the counts do not compare, the subsection pointer address is corrected to point at the first word of the same double word instruction. After an input data word is processed, the operation code is examined to determine if the instruction is the last instruction in the subsection. If the instruction is not the last instruction, the subsection counter is incremented. If the instruction is the last instruction, the preset sample rate "n" latch is set, where n = 1, 2, 3, 4 or 5. When a present "n" latch is set, the next word table instruction with a sample rate "n" code has the preset address resident in the bits adjacent to the instruction bits. The decom recognizes the preset conditions and presets the appropriate counter.



The initial minor frame count in which a data RAM parameter occurs is compared to a counter assigned to the sample rate subsection. The counter is reset to count zero at master frame start and is incremented once each minor frame.

The 384-kHz memory cycle frequency has 48 access periods within the 125-ms minimum word period. There are 15 access cycles available for internal decom processing. To minimize internal access requirements, the data RAM parameter must be listed in the order they occur; that is, first on a minor frame basis, then on a word basis. Nonsequential order of data RAM parameter requires a sequence of access and compare that can require access requirements far in excess of the 15 cycles available. The parameters should also be blocked into sample rate groups to simplify the sample rate repetition cycle control.

The PDI DCM is the same memory module used on the PCMMU. The memory is organized as 2048 words by 18 bits. Each minor frame, the counter is compared to a constant that is equal to the number of minor frames between a sample repetition. The constant is stored in the word table, in adjacent bits to an instruction with a sample rate code that would operationally select the appropriate counter. The instruction code initiates the decom control logic to compare the constant to the counter output. If there is a comparison, the counter is reset at the end of the minor frame. If there is no comparison, the counter is incremented at the end of the minor frame.

If there is a conflict in which two constants require storage in bits adjacent to the same word table instruction, a priority between constants determines which constant is stored. The lower priority constant is stored in the next available sequential spare constant field. Type 2 and 3 formats that have fewer than 1024 words per minor frame or fewer than 512 data RAM parameters can use the spare DCM words as dual word table instructions, as required. To resolve conflicts, the lower priority constant can be stored in the adjacent word table memory location. Both words can be accessed for a single input data word time; however, a relative word address counter is required to generate word table addresses. The absolute word counter is also required to qualify word column numbers in the sample rate table.

### **33.3.4 Word Selector**

The PDI provides a word selector for each of the four decoms. The word selectors, under control of the DCM, select words transferred to it by the decom control logic and transfer them to the TB memory and/or the data RAM. The word selector operates in two modes. The word selector mode is based on the operational mode selected for its associated decom; that is, either block mode or format synchronization mode.

#### **33.3.4.1 Word Selector Control Logic**

The word selector control logic performs the following:

A. Block mode

1. Accept notification of Start of Data Block (SODB) from decom at start of block.

2. Accept all incoming data from decom in 8-bit words.
3. Accept three 16-bit words of status register as the last three words of every homogenous data set.
4. Accept End of Data Block (EODB) from decom at end of block.
5. Supply SODB to TB at start of a block.
6. Transfer all incoming data and status register to TB in 16-bit words (two sequential 8-bit words grouped into one 16-bit word) in the same order as received.
7. Supply EODB to TB at end of block.

B. Format synchronization mode

1. Accept identification of Start of Minor Frame (SOMF) (master frame for formats without minor frames) from decom depending on format type
2. Accept word counter from decom.
3. Accept parallel data from decom in 8-bit words.
4. Accept the three 16-bit words of the status register from decom at End of Minor Frame (EOMF) (master frame formats without minor frames), depending on format type.
5. Select data for storage.
6. Accept identification of EOMF or master frame, depending on format type (EOMF).
7. Supply SOMF identification to TB control logic at the beginning of every minor frame or master frame, as the case may be.
8. Supply selected data to TB in 16-bit words. If the number of 8-bit words identified in a homogenous data set by the DCM is odd, the word selector supplies 8 ones as the second half of the last 16-bit word sent to the TB prior to the status register.
9. Supply three 16-bit words of status register to TB as the last word in every homogenous data set.
10. Supply EOMF identification to TB for every minor frame or master frame.
11. When decom lock is lost, then reestablished, start transferring data to the same side of the TB being written into when decom lock was lost. Start with the first word of the new homogenous data set at the first location of the subsection and continue until that set has been completed.

#### **33.3.4.2 Word Selection for Format Synchronization Mode, Toggle Buffer Storage**

The word selector, under control of the DCM, selects an entire minor frame (master frame for formats without minor frames) or a subset of an entire minor frame of data for storage in its TB subsection. The subset consists of any number of uniquely identifiable 8-bit words from a minor frame and the status register. The words identified by the DCM for selection from a minor frame (master frame for formats without minor frames) must be selected in every minor frame (master frame for formats without minor frames). Identification of the words to be selected is provided by the DCM. The maximum number of 8-bit words identified in the DCM for word selection by the word selector for storage in the TB for any single Pulse Code Modulation (PCM) input format is 1024. The word selector selects the identified words and presents the same to the TB in groups of two in the order they occur in the minor frame (master frame for formats without minor frames). The word selector does not prohibit the selection of the sync patterns or minor frame count words for storage in the TB. If there is an odd number of 8-bit words identified by the PCM for storage in the TB by the word selector, the word selector supplies eight 1's as the second half of the last 16-bit word sent to the TB prior to the three 16-bit words of the status register. The three 16-bit status register words for that bit sync/decom/word selector chain is included as the last three 16-bit words of every minor frame (master frame for formats without minor frames).

#### **33.3.4.3 Word Selection for Format Synchronization Mode, Data RAM Storage**

The word selector, under control of the DCM, selects the parameters for storage in the data RAM from the data supplied by the decom. The DCM supplies the following items for each parameter to be selected for storage in the data RAM by the word selector.

- Word number within minor frame or master frame, depending on format type
- Minor frame number of first parameter sample where applicable
- Sample rate of parameter
- Location within data RAM where parameter is to be stored

The word selector selects every sample of the identified parameter and presents it to the data RAM for storage in the supplied address. Only one parameter is stored in each 8-bit data RAM location. Note that the data RAM words are 16 bits in width and that the word selector may store two of each 8-bit parameters in one 16-bit location. Therefore, the address for storage of a parameter supplied by the DCM to the word selector and subsequently to the data RAM will identify which 8 bits, 1 to 8 or 9 to 16, a parameter is to be stored in, as well as the unique address of the word, 0 to 2047 in the data RAM. A maximum of 512 8-bit parameters can be identified in the DCM for word selection by the word selector for storage in the data RAM for any single input PCM format. The word selector does not prohibit the selection of the sync patterns or the minor frame count word for storage in the data RAM.

### 33.3.5 Status Register

Each bit sync/decommutator/word selector chain has an associated status register. The status register is the last three 16-bit word locations in the assigned TB subsection and is updated at the input data frame or minor frame rate, whichever is applicable. Operationally, it is loaded into the last three 16-bit words sent from the word selector to the TB. The bit definitions for the status register are as follows:

| Word | Bit   | Definition  |
|------|-------|---|
| 1    | 1-10  | Days 1 to 365 in Binary Coded Decimal (BCD), Most Significant Bit (MSB) first |
| 1    | 11-16 | Hours 0 to 23 in BCD, MSB first   |
| 2    | 1-7   | Minutes 0 to 59 in BCD, MSB first   |
| 2    | 8-14  | Seconds 0 to 59 in BCD, MSB first   |
| 2    | 15-16 |   |
| 3    | 1-8   | Milliseconds 0 to 999 in binary MSB first                                     |

### 33.3.6 Toggle Buffer

The PCMMU fetch process requests PDI TB data at 50 samples per second. These data are stored in the PCMMU OI/PL RAM and are incorporated into the downlink.

The TB is organized as two memory pages. Each page is 1024 words by 18 bits. The TB allows loading of a minor frame by the word selector onto one page while the PCMMU reads the other half-buffer via the PDI/PCMMU data bus (PL). A TB can only be accessed by bits within a page and not by page number. Page select is an internal TB control function.

Each page is divided into four subsections, one for each decomm. The size and location of these subsections are defined by the DFL in the decomm. The start and end addresses of each subsection is the same for both pages.

The TB subsections operate as individual TBs. Their pages can be toggled independently. This allows the subsections to fill at different rates without losing data.

The TB accepts data from the four word selectors and stores it for subsequent fetches by the PCMMU. All data are transferred and stored as 16-bit words. The data are stored in such a way that the PCMMU may acquire it as a continuous Time Homogenous Data Set (THDS). The word selector always ensures that all transfers follow this convention.

### 33.3.7 Data RAM

The PCMMU fetch process requests data RAM data at 10 samples per second. These data are stored in the PCMMU OI/PL RAM and are incorporated into the downlink or used by the SM GPC.

Each selected parameter of the subcommutated data has a unique RAM location. All samples of the same parameter are always stored in the same data RAM location. The location of the stored parameters are defined by the DCM. The data RAM is 2048 words by a 16-bit buffer.

The data RAM provides for the storage of parameters from the four decoms one-word selectors for data acquisition by the PCMMU. The memory itself is an 18-bit by 2048-word memory. Since data words are 8 bits in length, data supplied by the word selector are supplied with both an address location and syllable (bits 1 to 8 or 9 to 16) for storage. Each data word has parity generated; therefore, each syllable when read from memory can be parity checked. These parity bits are examined upon a read command via the data buses. All reads are responded to and there is no provision to tag data as to validity; therefore, the requesting device (PCMMU) may receive erroneous data and will propagate the erroneous data to the SM GPC.

The RAM control logic will prevent simultaneous reads and write into an address. In the case of a conflict, the write is inhibited and the read is allowed to process. All reads are by address; that is, two data words per read, four output via the data bus. The data bus does have the capability to write into the data RAM, but this feature is not utilized at the present time. The RAM is sectored by the DCM, each for its own storage, and provides for storage of up to 512 unique parameters.

### **33.3.8 FPM and Toggle Buffer Identifier**

The function of the FPM is to direct (point) each TB fetch request from the PCMMU to one of the four read address counters in the decoms or request that all 1's be returned as determined by the 3-bit code stored in the memory.

The PCMMU fetch command consists of an FPM address and a number of words to be fetched, up to 10 words. That FPM address contains the number of the TB subsection where the data are to be fetched. The read occurs at the location currently pointed to by the TB read address counter, and the read address counter is incremented during the read process.

The FPM is a RAM of 512 words by 4 bits. Three of the bits are instruction bits. The fourth is a parity bit that maintains even parity.

The FPM and Toggle Buffer Identifier (TBI) load is determined pre-mission, by the PDI Compiler, for the optimum read sequence from the TB to the PCMMU. The number of words in the FPM is equal to the number of response data words at each sample rate associated with TB access. See Table 33-5 for a detailed description of the FPM and TBI code.

**Table 33-5. FPM/TBI/TB relationships**

When the FPM receives a TB read request, the FPM will accept the address code, send the contents to the TBI to perform one of the following functions.

| <b>FPM bits</b> |              | <b>Function to be performed</b>                                |
|-----------------|--------------|--|
| <b>1</b>        | <b>2 3 4</b> |  |
| Even Parity     | 1 0 0        | Request one (16-bit) word of TB subsection 1 data from the TBI |
| Even Parity     | 1 0 1        | Request one (16-bit) word of TB subsection 2 data from the TBI |
| Even Parity     | 1 1 0        | Request one (16-bit) word of TB subsection 3 data from the TBI |
| Even Parity     | 1 1 1        | Request one (16-bit) word of TB subsection 4 data from the TBI |
| Even Parity     | 0 X X        | Supply 16-bits of 1's to the data bus port                     |

X = Don't care

The TBI will accept the FPM code and route it to a specific TB section in the following manner.

Initiate requests for TB subsection 1 data to the TB control logic based on the bit pattern present in bits 1, 2, and 3 of the TBI register as defined below.

| <b>Bits</b> |          |          | <b>Function</b>   |
|-------------|----------|----------|---|
| <b>1</b>    | <b>2</b> | <b>3</b> |   |
|             | 1        | 00       | Initiate request for TB subsection 1 data to TB control logic, if FPM requests TB 1 data. |
|             | 1        | 01       | Initiate request for TB subsection 1 data to TB control logic, if FPM requests TB 2 data. |
|             | 1        | 10       | Initiate request for TB subsection 1 data to TB control logic, if FPM requests TB 3 data. |
|             | 1        | 11       | Initiate request for TB subsection 1 data to TB control logic, if FPM requests TB 4 data. |
|             | 0        | XX       | Do not request TB 1 data.   |

X = Don't care

**Table 33-5. FPM/TBI/TB relationships (continued)**

Initiate requests for TB subsection 2 data to the TB control logic based on the bit pattern present in bits 4, 5, and 6 of the TBI register as defined below.

| <b>Bits</b><br><b>4 5 6</b> | <b>Function</b>   |
|-----------------------------|---|
| 100                         | Initiate request for TB subsection 2 data to TB control logic, if FPM requests TB 1 data. |
| 101                         | Initiate request for TB subsection 2 data to TB control logic, if FPM requests TB 2 data. |
| 110                         | Initiate request for TB subsection 2 data to TB control logic, if FPM requests TB 3 data. |
| 111                         | Initiate request for TB subsection 2 data to TB control logic, if FPM requests TB 4 data. |
| 0XX                         | Do not request TB 2 data.   |

X = Don't care

Initiate requests for TB subsection 3 data to the TB control logic based on the bit pattern present in bits 7, 8, and 9 of the TBI register as defined below.

| <b>Bits</b><br><b>7 8 9</b> | <b>Function</b>   |
|-----------------------------|---|
| 100                         | Initiate request for TB subsection 3 data to TB control logic, if FPM requests TB 1 data. |
| 101                         | Initiate request for TB subsection 3 data to TB control logic, if FPM requests TB 2 data. |
| 110                         | Initiate request for TB subsection 3 data to TB control logic, if FPM requests TB 3 data. |
| 111                         | Initiate request for TB subsection 3 data to TB control logic, if FPM requests TB 4 data. |
| 0XX                         | Do not request TB 3 data.   |

X = Don't care

**Table 33-5. FPM/TBI/TB relationships (concluded)**

Initiate requests for TB subsection 4 data to the TB control logic based on the big pattern present in bits 10, 11, and 12 of the TBI register as defined below.

| Bits<br>10 11 12 | Function  |
|------------------|---|
| 100              | Initiate request for TB subsection 4 data to TB control logic, if FPM requests TB 1 data. |
| 101              | Initiate request for TB subsection 4 data to TB control logic, if FPM requests TB 2 data. |
| 110              | Initiate request for TB subsection 4 data to TB control logic, if FPM requests TB 3 data. |
| 111              | Initiate request for TB subsection 4 data to TB control logic, if FPM requests TB 4 data. |
| 0XX              | Do not request TB 4 data.   |

X = Don't care

If an FPM request for TB data does not cause any TB data requests to be initiated by the TBI because of the configuration of the TBI register, the TBI control logic will respond to the FPM request by sending 16 bits of 1's to the requesting data bus port.

The TBI is a function that takes a data request from the fetch pointer section and determines whether any last minute routing changes need to be made. This stage was designed to allow controllers to make updates to the FPM routing process in the event that both the prime and backup decoms fail. If a third decomp is to be used, the only FPL change required is to the 12-bit TBI control word that is contained in the FPL for loading into the PDI. Once the new code is determined, a mass memory patch can be uplinked to mass memory and then loaded into the PDI. The TBI then steers the fetch to the new TB subsection.

### 33.3.9 Built-In Test Equipment

The BSR collects system status from various elements of the PDI. The PDI BITE is intended to check the health of the PDI during normal mission operations and does not indicate component failures that are outside the functional data path for a particular mission. The BITE does not give sufficient information to aid in ground mode maintenance or component failure isolation.

The PDI BITE circuitry has an overall failure detection rate of 97 percent; that is, 97 percent of all failures are detected, which results in loss of PDI data or invalid data



transfer. As in all BITE detection circuitry, some elements may set a failed condition but do not result in the loss of or invalidate PDI data.

The BSR is forced to an all 1's state at the completion of the second BITE word read, and the failed element must set the BSR to zero; therefore, it is important to remember that any failure that is transitory in nature will be reset. Also any device not being used (MIA, DEM, etc.) will be set to a one state. This is especially true in the case of MIAs that have been bypassed. The MIAs, as used in the PDI, are demand response devices; therefore, if a port has been bypassed, the requesting device (GPC, PCM) no longer requests data and does not detect any errors until a PDI I/O reset is done. The reset attempts to reestablish a data path to the PDI. See Table 33-6 for a detailed description of the BITE status bit logic.

### 33.3.10 PDI Timing

The PDI has several timing sources available for use. The first is the 16-MHz oscillator used exclusively in the MIA circuits. The second is the 16-MHz oscillator used in the bit synchronizer transition detector.

The third timing source is one of two external 1.152-MHz sources from PCMMU 1 or 2. Only one is active at a time; they are OR'd after their respective line receivers. The only function of the 1.152-MHz is to provide timing for the PDI IRIG receiver and decoder.

The external 1.152-MHz timer signal from the PCMMU first enters a voltage comparator where a symmetry check is performed. If the incoming wave form is not within 45 to 55 percent duty cycle, the signal is declared bad and the internal clock is selected.

If the timing source either goes out of tolerance or ceases, the PDI selects the PDI internal oscillator for use in 1-kHz clock generation. If the external either comes back or passes the tolerance check, the PDI reselects the external time source.

Note: Internal time is sometimes randomly selected by the PDI because of a design problem in the PDI clock receiver that distorts the incoming wave form.

The fourth source is the PDI internal 4.608-MHz oscillator. In normal operation, it supplies all of the timing requirements for the PDI internal logic. This is exclusive of the MIAs and the generation of the 1-kHz IRIG-B clock if an external source is available and is in tolerance. The 4.608-MHz is divided by 12 to provide the 384.5 kHz basic timing to all memory modules internal data bus, priority generator, etc. The 4.608-MHz is also divided by 4 to produce a 1.152-MHz clock to be used as the frequency tolerance check on the incoming external source (IRIG-B). If the incoming external source is out of tolerance, either in frequency or amplitude, the 1.152-MHz internal clock is selected to produce the 1-kHz IRIG-B clock.

**Table 33-6. BSR bit descriptions**

The PDI BSR is composed of 32 bits (two 16-bit words). The first 16-bit word is allocated to the status of the data stream processing. A bit description follows.

BITE status word 1

|     |    |   |
|-----|----|---|
| Bit | 1  | Master Frame Lock Decom 1<br>If the incoming data are formats 1, 2, or 3, it signifies that frame sync has been achieved. If format 4 (block mode), has no significance, set to 1.  |
|     | 2  | Word Lock Decom 1<br>If the incoming data are formats 1, 2, or 3, it signifies that word sync has been achieved by detecting the imbedded sync word or words in the bit stream. If format 4 (block mode), signifies that the word sync is grouping 8 bits of data and transferring this to the word selector. |
|     | 3  | Bit Lock Decom 1<br>If the incoming data are formats 1, 2, or 3, it signifies that bit lock has been achieved, code detection is correct, and bit rate is in tolerance. If format 4, this will, in turn, force word sync. This bit is forced to 0 during DCM loading.   |
|     | 4  | Bit Rate Accuracy Decom 1<br>Signifies that the incoming bit stream is within $\pm 3.25$ percent of the expected bit rate. If the bit rate is not within tolerance, this will not inhibit data.   |
|     | 5  | Same bit 1 for decom 2  |
|     | 6  | Same bit 2 for decom 2  |
|     | 7  | Same bit 3 for decom 2  |
|     | 8  | Same bit 4 for decom 2  |
|     | 9  | Same bit 1 for decom 3  |
|     | 10 | Same bit 2 for decom 3  |
|     | 11 | Same bit 3 for decom 3  |
|     | 12 | Same bit 4 for decom 3  |
|     | 13 | Same bit 1 for decom 4  |
|     | 14 | Same bit 2 for decom 4  |
|     | 15 | Same bit 3 for decom 4  |
|     | 16 | Same bit 4 for decom 4  |

The next page further defines BITE status word 1.

*Table 33-6. BSR bit descriptions (continued)*

| No. of bits | Name               | Description  |
|-------------|--------------------|--|
| 4           | Bit sync           | The bit assigned to that bit synchronizer will be set to zero when bit sync has not been established. This includes inactive port connections or port connections with wrong data stream for the decom string  |
| 4           | Decom word lock    | The bit assigned to that word synchronizer will be set to zero until such time as bit lock for that string and the synchronization word or words have been found. Word lock cannot be achieved until the entire sync pattern is detected error free. If the PDI is operating in the block mode, word lock is forced when the bit synchronizer achieves bit lock  |
| 4           | Master frame lock  | The bit assigned to that decom section will be set to zero until such time as both bit sync and word sync are detected, plus one of the following conditions   |
|             |                    | <ol style="list-style-type: none"> <li>1. If type 1 (main frame only), two consecutive sync patterns</li> <li>2. If type 2 (minor frame sync with a master frame sync), the detection of two consecutive master frame sync patterns</li> <li>3. If type 3 (minor frame sync with a minor frame counter), the detection of two consecutive minor frame counts</li> <li>4. If type 4 (block mode), set to 1 when bit lock is achieved</li> </ol> |
| 4           | Bit rate tolerance | The bit assigned to that bit synchronizer will be set to zero if the incoming bit rate is $\pm 3.25$ percent of the expected bit rate. These bits are indicators only and will not affect data validity. The bit synchronizers will achieve and hold bit lock $\pm 10$ percent of the expected bit rate  |

**Table 33-6. BSR bit descriptions (continued)**

Bite status word 2

|     |    |   |
|-----|----|---|
| Bit | 1  | No response 1 - Data bus indicates the occurrence of a no response on the associated data bus port (PCM2)   |
|     | 2  | Input data invalid 1 - Data bus - detected an input data invalid on a command data word on the associated data bus port (PCM2)  |
|     | 3  | Same as bit 1 for data bus PCM 1  |
|     | 4  | Same as bit 2 for data bus PCM 1  |
|     | 5  | Same as bit 1 for data bus GPC  |
|     | 6  | Same as bit 2 for data bus GPC  |
|     | 7  | TB parity - A parity error has been detected in the TB  |
|     | 8  | Data RAM parity - Detected a data RAM parity error on read request  |
|     | 9  | Fetch pointer memory parity - Parity error detected during read from the FPM  |
|     | 10 | Decom memory - Parity error detected during read from the DCM on decom 1  |
|     | 11 | Same as bit 10 for decom 2  |
|     | 12 | Same as bit 10 for decom 3  |
|     | 13 | Same as bit 10 for decom 4  |
|     | 14 | MTU IRIG - Detecting of an IRIG time code format error or absence of an IRIG signal   |
|     | 15 | PCM 1.152 MHz - 1.152 MHz time lost from the active PCMMU and is operational on internal time. This also affects the 1 kHz for the IRIG time code logic sense. This is derived from the 1.152-MHz clock; however, the internal 1.152 MHz will generate the 1-kHz IRIG clock. In summary this means both clocks are on internal time |
|     | 16 | Power status denoted that a power loss for greater than 400 ns has occurred   |

*Table 33-6. BSR bit descriptions (continued)*

| No. of bits | Name                       | Description  |
|-------------|----------------------------|--|
| 1           | Power status               | Bit will be set to zero for +5 V dc regulated voltage failure. This may be caused by either a regulator/preregulator failure or by line voltage being below the 22-V limit   |
| 1           | Toggle buffer parity error | Bit will be set to zero whenever a parity error occurs in the TB during a read cycle. No provision is made for write parity errors   |
| 1           | Date RAM parity error      | Bit will be set to zero whenever a parity error is detected in data RAM during a read cycle, since a RAM word is composed of two 8-bit data words. A parity bit is associated with each data word and will set the RAM parity bit for an error on either data word. Parity errors may be encountered upon PDI powerup since the PDI RAM is initialized with a random pattern. The PCMMU will request data via its fetch PROM and will not set a BSR bit to denote a parity error because it computes its own parity and places this in its data RAM. This will enable the GPC (SM 2) to acquire erroneous data from the data RAM |
| 3           | Input data invalid         | The bit assigned to that MIA port will be set to zero when the MIA detects an error on command word (CW) or command data word (CDW). Errors that will cause a zero bit set are: incoming data parity error, bit count, nonvalid manchester biphase code, 101 pattern check on bits 25, 26, and 27 of a CW or CDW. If a CW is flagged, the PDI will not perform the function requested. If, however, the error is detected on a CDW, the PDI will set the bit but will process the data as requested in the previous CW   |

**Table 33-6. BSR bit descriptions (concluded)**

| No. of bits | Name                      | Description  |
|-------------|---------------------------|--|
| 3           | No response               | <p>The bit assigned to that MIA port will be set to zero when the MIA detects an error in gap time from a CW to a CDW or CDW to a CDW, or an incorrect address of a CDW to the previous CW. Gap time errors are defined as:</p> <ul style="list-style-type: none"> <li>• From a CW to the first CDW must be less than 25 <math>\mu</math>s</li> <li>• From a CDW to the next CDW must be less than 17 <math>\mu</math>s</li> </ul> <p>If the error is a gap time error, the PDI will not process any CDWs for that CW</p> <p>If the error is an address error in the CDW, that CDW will not be processed, but all other CDWs in that group will be processed normally</p>                    |
| 1           | Internal oscillator       | <p>Bit will be set to zero if neither PCMMU clock is present or if the active clock does not pass the clock tolerance check. The tolerance check consists of testing for amplitude (<math>5.25 \pm 2</math> V peak-to-peak) and frequency (<math>1.152</math> MHz <math>\pm</math> 11.52 kHz). If the incoming clock fails either or both checks, the PDI will select its internal time to generate the 1-kHz clock for IRIG "B" time. If the clock reverts to normal, passes the tolerance checks, the PDI will accept the external clock and will not set the zero bit in the BSR. The PDI, when on internal time, may have a time skew on the data timetag of <math>\pm 868</math> ns</p> |
| 1           | IRIG "B" error            | <p>Bit will be set to zero if the IRIG "B" decoder detects marker position bits not in proper sequence or position, bit count is in error between marker bits, or bit sync is lost. If the bit is set to zero, loading into the transfer register will not occur and stale time will be transferred to the word selector for data timetagging</p>  |
| 1           | FPM parity                | <p>Bit will be set to zero if a parity error was detected during an FPM read operation. This does not detect errors on a write sequence</p>  |
| 4           | Decom memory parity error | <p>The bit assigned to that decom will be set to zero when a parity error for a read sequence is detected for that decom. This will not detect write parity errors</p>   |

The IRIG-B timing is used for timetagging data only; i.e., “What time is it?” It is not used for any basic PDI timing. The IRIG-B time code follows the normal convention and is a pulse duration modulation stream. The convention is as follows:

- Marker bits (position identifiers) are 8 ms long.
- Two marker bits in a row mark the start of time frame.
- One marker bit delineates time segments (seconds, minutes, hours, days, and hundreds of days).
- A zero is denoted by a pulse length of 2 ms or less.
- A one is denoted by a pulse length greater than 4 ms and no more than 5 ms.

Note: PDI IRIG-B time anomalous counting: The PDI seconds register has been wired improperly when the counter gets to 19 seconds, skips 20, registers 00, and proceeds to 21 or when the counter gets to 39, skips 40, registers 60, and proceed to 41.

### 33.3.11 IRIG Decoder Operation

Since there is a positive transition at the beginning of every IRIG bit, a bit sync pulse is generated by trapping each transition and using the 1.152-MHz clock to generate a pulse 1 clock cycle wide at the beginning of the bit. A 1-kHz clock is generated by counting down from the 1.152-MHz system clock. It is synchronized with the data transitions by resetting a counter at each bit sync. This 1-kHz clock can then be used to run a control counter which is also reset by each bit sync. Since each bit is 10 ms long, the counter reaches a count of 9 during each bit.

Position identification markers are 8 out of 10 ms (no other bit has a longer mark time), and the beginning of the frame is identifiable by two position markers in a row. Position markers can be determined by checking the status of the IRIG data at the count of 7 ms. Frame sync can then be detected by detecting two position markers in a row.

Frame sync is used to resync the millisecond counter to a zero so that it clocks to 1000 during one complete frame. The frame sync also signals the load pulse generator that data are being shifted into the data register.

The data register clocks in data by checking the IRIG data when the counter reaches count 4. Since a 1-bit is marked by a 5-ms high pulse, it is clocked in as high; since a 0-bit is marked by a 2-ms high pulse, it is clocked in as low.

The load pulse generator counts position markers up to four; then, 2 bit times later a load pulse is generated.

Since millisecond time is not part of the IRIG-B time code, a millisecond counter is used. This count begins at the start of a time frame and is transferred when a load pulse is generated. This load pulse loads the appropriate bits from the data register into the

millisecond, seconds, minutes, hours, and days registers. These registers are connected to a common bus through tri-state devices, which are controlled by the four DCMs. The DCM detects the end of TB data and calls for the time word data via the internal data bus. The time word is combined with the DFL and bit rate tolerance bits for inclusion into the TB data.

### 33.3.12 Data Bus Descriptions

#### 33.3.12.1 Input Data Bus

Seven subsections within the PDI have direct memory write access. They are the three I/O data bus ports and the four decom functions. Note that operationally only one data bus port (GPC port) has write access; however, the PDI hardware is designed so that all data bus ports are identical.

The eight data source blocks consist of the seven write access subsections and the IRIG-B decoder block. The IRIG-B decoder block does not have direct memory access and can only transfer data to memory as a function of any of the four decom write access requests.

The 10 data destination or storage devices consist of the data RAM, the FPM, the TB, the 4 DCMs (1, 2, 3, and 4), the switching matrix register, the TBI register, and a set of registers dedicated to storage of synchronization and decom constants. The BSR receives its inputs as discretes isolated from the data input bus and, therefore, is not included as part of the input bus.

The data input bus is a tri-state bus; its input sources are selected and enabled by a priority generator. If an input source has data ready to be loaded in storage device, the source requests priority to use the data input bus. The priority generator grants access to the data input bus to the requesting source for a period of time sufficient to transfer data to the storage device. The priority generator guarantees that only one source can have access to the bus at any time. The data bus control logic, in conjunction with the priority generator, enables one of the storage devices as determined by the address on the address bus.

The priority generator allows access to the PDI memories for the seven PDI subscribers based on the following priorities:

- A. Input/Output Bus (I/OB) 1
- B. I/OB 2
- C. I/OB 3
- D. Decom 1
- E. Decom 2
- F. Decom 3
- G. Decom 4



The input data bus is organized as 2-bit eight buses to accommodate byte structured write access. The I/O data bus port writes 16 bits of data during one access time. The decom functions have two types of write access. Decom write access to the TB utilizes 16 bits of data and uses the data input bus as do the data bus ports. The second type of decom access is a data RAM access which writes only 8 bits at a time to either 8-bit section of the 16-bit word data RAM.

As a form of continuous test of the storage elements, odd parity is written into each storage device during every write access. All storage devices except the data RAM require only one parity bit. Since the data RAM is written only 8 bits at a time, a dual parity system is required, a parity bit for each 8-bit byte. The input data bus block diagram parity blocks are organized as 2-byte parity generators with their outputs accumulated to form a 16-bit parity output.

Control timing generates the timing required to load two types of storage elements: Complimentary Metal Oxide Silicon (CMOS) memory elements and parallel-in/parallel-out registers. All interface elements, tri-state drivers, memory elements, and register on the data input bus are low power CMOS.

### **33.3.12.2 Data Output Bus and Address Bus Description**

The data output bus is the bus used by the data bus ports to access data from the storage elements and transfer the data from the PDI. The three data bus ports are the only subsections within the PDI which have read access via the data output bus. There are 12 basic devices that can output data on the output bus: the data RAM, the TB, the FPM, the four DCMs, the switch matrix register, the TBI register, the BITE status register, the registers used to store constants, and the buffered address bus.

All read access handles 16 bits plus parity. The data RAM read access checks the 2-byte parity bits. The memory control logic in conjunction with the address bus controls use of the data output bus and guarantees only one storage device can output on the data bus at any time. All devices interfacing with the bus have tri-state outputs. The return received command word is implemented by connecting the address bus to the data output bus. The command word bits which are required to be returned are located in the usual starting address field. With none of the storage devices enabled, the address bits are returned to the respective data bus port via the data output bus.

The address bus has the same sources as the data input bus with the exception of the IRIG-B decoder which uses the respective decom supplied address. The six memories that interface with the address bus are the data RAM, the FPM, and the four DCMs. All remaining storage devices, with the exception of the TBs, do not have sufficient word density to require internal address decoders, but instead utilize the bus control decoder. The TB is addressed by two sets of address counters, one set for write access and a second set for read access.

### 33.3.13 Power

The PDI uses 27 watts and draws 1 amp. Buses are MNA FPC1 and MNC FPC3. Control buses are CNTL BC1 and CNTL BC2.

### 33.3.14 Temperature Data

The PDI is cooled by cold plate water loop. Minimum temperature = 35° F and maximum temperature = 120° F. No temperature data are downlinked.

### 33.3.15 Location

One unit is in avionics bay 1, zones 28 and 43E. A spare unit, if flown, is typically located in avionics bay 2, zone 57M. Refer to the In-Flight Maintenance (IFM) book, JSC-48025, to determine the exact storage location.

### 33.3.16 IFM

The PDI Replacement IFM requires 2 hours 33 minutes with a 15-minute checkout. The IFM can be broken into three 50-minute periods: one to remove the tools, lockers, and spare PDI; one to perform the actual replacement; and one to stow the malfunctioning PDI, lockers, and tools. A lot of pad time is built into the procedure; the 50 minutes can be reduced to 33 minutes.

## 33.4 SOFTWARE SPECIFICATION

Software used by the PDI and interfaces with the PDI include DFLs, Fetch Pointer Loads (FPLs), and PCMMU Telemetry Format Loads (TFLs). DFL, FPLs, and TFLs are built using the PDI Compiler (PDIC). TFL/DFL telemetry system configurations for a specific mission can be found in Section 5 of Payload Management Level C Flight Software Requirements, JSC-19478-XX (where XX is the STS mission number). All the PDIC products are delivered on MAST I and MAST II for all flight software builds.

The MMU can hold up to 25 DFL formats and 25 FPM load formats.

The PDIC produces the DFLs, FPLs, and TFLs. The INCO section, the Reconfiguration Management Office, and Payload community work together to develop OI/SM/GN/PDI requirements for a specific flight. The inputs are provided to Boeing/North American Downey, who then builds the TFLs/DFLs/FPLs for the flight.

### 33.4.1 Shuttle Standard Formats

The shuttle orbiter standard telemetry formats for payloads are designated format synchronization mode types 1, 2, and 3. The distinctive characteristic of these three types of payload PCM telemetry formats is that their structure enables both the orbiter PDI and the orbiter GPC software services to process payload measurement data. Each of these three shuttle standard formats also enables the PDI to process payload frame data as time homogenous data sets for inclusion within the orbiter PCM telemetry downlink. Refer to Figure 33-7.

With respect to the orbiter PCM telemetry downlink, a THDS is defined to be those 8-bit words decommutated from payload frame such that those words from one payload frame will never be mixed with those words from any other payload frame within either the PDI or PCMMU. With respect to orbiter GPC software services, maintaining the time homogeneity for both individual multisyllable payload measurements and payload measurement word sets cannot be guaranteed.

#### **33.4.1.1 Orbiter GPC Software Service**

Transferring individual payload measurements to the orbiter GPC software services is implemented via the PDI data RAM. Before individual measurements within the frame can be transferred to the PDI data RAM, recognition of the second consecutive valid frame sync patterns must first occur. When this has happened, data RAM storage for each payload measurement proceeds as follows.

Within each minor frame word column of a master frame, those 8-bit words containing data samples for a payload measurement that is required to be processed by the orbiter GPC software services are stored within the same data RAM byte address.

A multisyllable payload measurement has its 8-bit bytes independently stored within a separate data RAM byte address whenever its word position within the appropriate minor frame is processed.

Maintaining the time homogeneity for both individual multisyllable payload measurements and payload measurement word sets cannot be guaranteed.

The data RAM is a direct read device by the PCMMU; therefore, all addresses are accessible at any time and may contain static or erroneous data. No flags are provided to ascertain the condition of the data.

#### **33.4.1.2 Type 1 Format**

A Type 1 payload format is defined as a format consisting of master frames only and a master frame sync pattern which occurs once every master frame (Figure 33-7). The master frame length can be from 8 to 1024 words long with up to 200 master frames per second. The word size is 8 bits with a master frame sync of 8, 16, 24, or 32 bits; i.e., any pattern located in the first or last words of the master frame. The bit rate can be 10 bits per second (bps) to 64 kilobits per second (kbps).

##### **33.4.1.2.1 Orbiter PCM Telemetry Downlink Service**

Throughputting payload data to the ground via the orbiter PM telemetry downlink is implemented via the PDI TB for individual master frames. Before individual master frames can be transferred to the PDI TB, recognition by the PDI of two successive valid master frame sync patterns must first occur. When this has happened, TB storage of each master frame proceeds as follows.

The THDS within the PDI TB consists of a payload master frame either in total or a subset. Those payload master frame words to be downlinked are partitioned into 16-bit

groups (two consecutive or nonconsecutive 8-bit master frame words) for storage within each TB location.

The remainder of the THDS consists of three additional 6-bit status words appended to the master frame words by the PDI.

### **33.4.1.3 Type 2 Format**

A Type 2 payload format is defined as a format consisting of master frames and minor frames. The bit rate is 10 bps to 64 kbps. Type 2 contains a maximum of seven sample rates per format with one of the sample rates equal to the number of minor frames per master frame.

#### **33.4.1.3.1 Minor Frames**

Every minor frame is identified by a minor frame sync pattern which occurs once each minor frame and will be the same sync pattern for all minor frames. One of the minor frames contains an 8-bit master frame sync word. The minor frame rate is up to 200 minor frames per second. The minor frame sync can be 8, 16, 24, or 32 bits; i.e., any pattern located in the first or last words of every minor frame.

#### **33.4.1.3.2 Master Frames**

A master frame, in general, contains two or more minor frames; otherwise, there is no distinction with a Type 1 format. The start of a master frame is identified as the minor frame which contains the value of the master frame sync word and may be any position in the frame. This master frame sync word will be used to generate a frame counter for decom use in identifying parameters. The master frame length can be from 2 to 256 minor frames with each minor frame containing 8 to 1024 8-bit words. The master frame sync is 8 bits, any pattern located in the first or last minor frame in any word column, other than the minor frame sync column.

#### **33.4.1.3.3 Orbiter PCM Telemetry Downlink Service**

Throughputting payload data to the ground via the orbiter PM telemetry downlink is implemented via the PDI TB for individual minor frames. Before individual minor frames can be transferred to the PDI TB, recognition by the PDI of two successive valid minor frame sync patterns must first occur. When this has happened, TB storage of each minor frame proceeds as follows.

The THDS within the PDI TB consists of a payload master frame either in total or a subset. Those payload master frame words to be downlinked are partitioned into 16-bit groups (two consecutive or nonconsecutive 8-bit master frame words) for storage within each TB location.

The remainder of the THDS consists of three additional 6-bit status words appended to the master frame words by the PDI.

#### **33.4.1.3.4 Orbiter GPC Software Service**

Transferring individual payload measurements to the orbiter GPC software services is implemented via the PDI data RAM. Before individual measurements within the minor frame can be transferred to the PDI data RAM, valid recognition of two successive master frame sync patterns, with valid minor frame syncs in all minor frames, must first occur. Therefore, master frame lock is not required for downlisting, but is required for crew display. When this has happened, data RAM storage for each payload measurement proceeds as follows.

Within each minor frame word column of a master frame, those 8-bit words containing data samples for a payload measurement that is required to be processed by the orbiter GPC software services are stored within the same data RAM byte address.

A multisyllable payload measurement has its constituent 8-bit bytes independently stored within a separate data RAM byte address whenever its word position within the appropriate minor frame is processed.

Maintaining the time-homogeneity for both individual multisyllable payload measurements and payload measurement word sets cannot be guaranteed.

#### **33.4.1.4 Type 3 Format**

A Type 3 payload format is defined as a format consisting of master frames and minor frames. The bit rate is from 10 bps to 64 kbps.

##### **33.4.1.4.1 Minor Frames**

Every minor frame is identified by a minor frame sync pattern which occurs once each minor frame and is the same sync pattern for all minor frames. Every minor frame contains an 8-bit minor frame count word. The minor frame sync is 8, 16, 24, or 32 bits with the pattern positioned in the first or last word(s) of every minor frame.

The minor frame count is an ascending or descending binary count which increments or decrements one count each minor frame. Initial count and word location within minor frames are fixed by the payload customer. The count pattern is always Most Significant Bit (MSB) first and right justified. The minor frame count word must be in the same location for every minor frame.

##### **33.4.1.4.2 Master Frames**

A master frame, in general, contains two or more minor frames; otherwise, there is no distinction with a type 1 format. The start of a master frame is identified as the minor frame which contains a valid minor frame sync word and an initial value of the minor frame count word (there is no distinctive major frame sync pattern). The minor frame count word can appear in any column within the minor frame. The master frame length can be from 2 to 256 minor frames with a minor frame equal to 8 to 1024 8-bit words at up to 200 minor frames per second.

#### **33.4.1.4.3 Orbiter PCM Telemetry Downlink Service**

Throughputting payload data to the ground via the orbiter PM telemetry downlink is implemented via the PDI TB for individual minor frames. Before individual minor frames can be transferred to the PDI TB, recognition by the PDI of two successive valid minor frame sync patterns must occur. When this has happened, TB storage of each minor frame proceeds as follows.

The THDS within the PDI TB consists of a payload master frame either in total or a subset. Those payload master frame words to be downlinked are partitioned into 16-bit groups (two consecutive or nonconsecutive 8-bit master frame words) for storage within each TB location.

The remainder of the THDS consists of three additional 6-bit status words appended to the master frame words by the PDI.

#### **33.4.1.4.4 Orbiter GPC Software Service**

Transferring individual payload measurements to the orbiter GPC software services is implemented via the PDI data RAM. Before individual measurements within the minor frame can be transferred the PDI data RAM, valid recognition of two successive minor frame sync patterns and their corresponding minor frame count patterns must first occur. When this has happened, data RAM storage for each payload measurement proceeds as follows:

Within each minor frame word column of a master frame, those 8-bit words containing data samples for a payload measurement that is required to be processed by the orbiter GPC software services are stored within the same data RAM byte address.

A multisyllable payload measurement has its 8-bit bytes independently stored within a separate data RAM byte address whenever its word position within the appropriate minor frame is processed.

Maintaining the time-homogeneity for both individual multisyllable payload measurements and payload measurement word sets cannot be guaranteed.

#### **33.4.1.5 Shuttle Block Formats**

The designated shuttle orbiter nonstandard telemetry format is the block mode format. The PDI does not recognize that the incoming payload data possess any format structural properties (e.g., master frame, minor frame, word interval, etc.) other than bit intervals and, as such, cannot process individual payload measurements for the orbiter GPC. The PDI will restructure the incoming payload bit intervals into data blocks appropriate for inclusion within the orbiter PCM telemetry downlink.

If flown, the PCDECOM unit can provide the crew access to the block format data. The PCDECOM is essentially a laptop computer with a decommutator that attaches to the spare PCMMU output port. The spare PCMMU port can be accessed via a middeck location.

Throughputting block payload data to the ground via the orbiter PCM telemetry downlink is implemented via the PDI TB for individual data blocks. Before individual data blocks can be transferred to the PDI TB, establishment by the PDI of valid bit lock with the payload must first occur. When this has happened, TB storage for each data block proceeds as follows:

- A. A data block sync word or words, generated by the PDI, is the first to be transferred to the TB.
- B. The sequential payload bit intervals that were input will next be transferred to the TB.
- C. Lastly, the PDI appends three additional 16-bit status word.

#### **33.4.1.6 Subcommutation**

Occasionally, a payload defines decom formats that subcommutate parameters (e.g., IUS). The PDI does not have problems with subcommutation; it is the SM GPC software.

When PDI parameters are subcommutated in the PCMMU (via the normal fetch mechanism); i.e., at time X parameter A is in a PDI RAM address and at time X + 1 parameter B is in that same PDI RAM address, the SM software processes the data as though only one value is being acquired. This error can cause display values to toggle and failure to announce out-of-limit conditions or false annunciation to occur.

For payloads that have subcommutated parameters, be aware that

- A. Cargo control SPEC, typically SPEC 200, data may toggle and display erroneous information. The timing of this data toggle is dependent on the definition of the payload telemetry stream. The status field for FDA parameters may toggle at the same rate.
- B. Class 3 annunciation of an out-of-limit condition for those parameters requiring FDA may not occur. The use of the noise filter to eliminate nuisance alerts should be examined; however, this may also preclude annunciation of an actual alert condition.

#### **33.4.2 PDI Load Process Overview**

These are the actions taken by the GPC when a load request is received from SPEC 62 or from the ground.

- A. If SPEC 62 is terminated at anytime during the load process, the load process is terminated.
- B. If SPEC 62 is active during an uplink load attempt, the load process is not executed.
- C. The load status is set to RUN, displayed on SPEC 62.

- D. The GPC reads the format data into the SM common buffer. An FPL contains 512 bytes. A DFL contains 2048 bytes.
- E. A checksum is performed on the data from the MMU. The GPC calculates a new checksum value during the read from the MMU to the common buffer. The last word of the block contains a predetermined checksum value. A comparison between the two checksums is made. A failure of the comparison causes a read error which terminates the load with a message, I/O ERROR MMU.
- F. The GPC checks for an OPS Transition. If a transition occurs, the load is terminated, and the load status is set to FAIL.
- G. The GPC writes the data into the PDI. All the bytes are sent to the PDI at one time.
- H. The GPC reads the load from the PDI and performs another checksum to verify that the PDI was correctly loaded. If an FPL, all 512 bytes are read as one block. A new checksum is created as the data are read. If a DFL, the 2048 bytes are read four blocks of 512 bytes each.
- I. A new checksum is created as each block is read. After all four blocks are read, the four checksums are added together. The new checksum is compared with the original checksum from the MMU.
- J. The decom format ID and FPM ID are updated after successful completion of the load process.

#### **33.4.2.1 Telemetry Format Load**

Refer to Systems Brief 29, PCMMU, for detailed description of the TFL.

#### **33.4.2.2 Decom Format Load**

The DFL is utilized by the PDI for decommutation of payload measurements. It establishes routing of measurements to the PDI toggle buffer and/or to the PDI data RAM. The payload customer specifies the format of the incoming data stream so that the decom can bit synchronize, decommutate, and select words as required for the mission. Refer to Figure 33-2 for DFL numbers.

Since the inception of Measurement and Stimulus (MAST) II system, it has been standard practice to carry duplicate DFLs for every payload. These duplicates are known as "backup DFLs" and are identified with a different DFL number from the prime DFL and placed in separate decoms. This is done to avoid loss of data in case of decom failure.

The function of a DFL is to program one of the PDIs decom formatters to enable the decom to lock onto a stream of PL data and decommutate those data in accordance with customer specification. A DFL causes decom data to be routed to the PDI toggle buffer and/or the PDI data RAM. The PDI toggle buffer data are intended for



downlinking to the ground via the PCMMU. The PDI data RAM data (parameters data) are intended for use by the GPC for SM and/or BFS and displays.

Recall from the PCMMU brief, PDI data RAM data can be included in the downlist if the TFL and SM downlist format are built properly premission.

A DFL contains signal names, sample rates, and card type for the signals. Also included are start word, number of words, bit rate, PDI sync patterns, format type, and format number.

Decom data may or may not specify PDI data RAM addresses and half word indicators. DFLs are loaded on the MMU unflipped. The MMU contains up to 25 DFLs for a specific flight.

### 33.4.2.3 Fetch Pointer Load

- A. FPLs contain dummy Measurement Stimulation Identifications (MSIDs) and FPM, TBI section numbers and addresses.
- B. Only one FPM load is assigned to a decom configuration.
- C. An FPM load can be assigned to more than one TFL.
- D. FPLs are produced to minimize accesses to the PDI TB sections.
- E. FPLs are loaded on the MM unflipped.
- F. The MMU contains up to 25 FPLs for a specific flight.

### 33.4.2.4 Load Fail

A DFL or FPL process is terminated for the following conditions:

- A. Crew initiates load and terminates SPEC 62 prior to load completion  
Result: DFL or FPM ID unchanged.  
Response: Crew must bring SPEC 62 back up and make appropriate item entries.
- B. Ground initiate load and SPEC 62 active  
Result: DFL or FPM ID unchanged.  
Response: Crew must drop SPEC 62, then re-attempt load uplink
- C. MMU I/O error  
Result: DFL or FPM ID unchanged.  
Response: Call DPS for action to take.

D. PDI I/O or checksum error

Result: DFL or FPM ID shall be blanked, set to zero, and made available for downlist.

Response: Reattempt load. If no joy, ask DPS about the condition of the PL bus and SM GPC.

### 33.4.2.5 Data Flipping

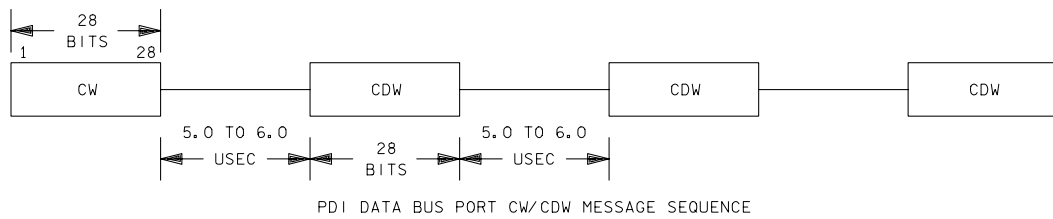
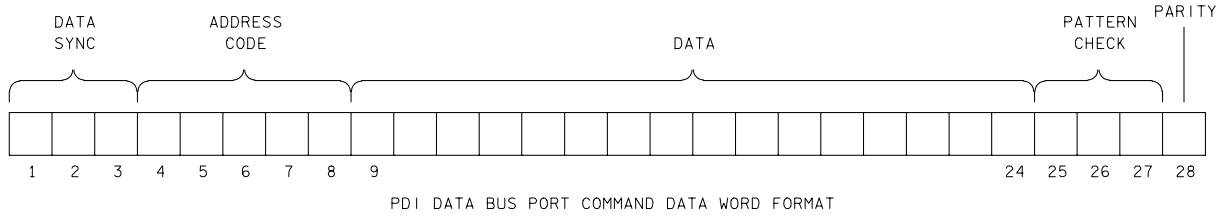
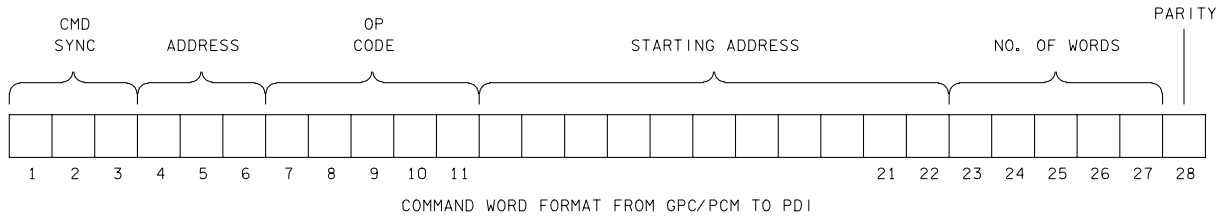
Compared to the PCMMU, the PDI loads DFL and FPL data differently. The data are shifted into a register from the LSB to the MSB. Next, a parallel transfer of all 16 bits for DFLs and 4 MSBs for FPLs into the appropriate memory location is performed. Therefore, the MSB of each CDW ends up in the MSB of each location loaded.

### 33.4.3 Switch Matrix Read

The switch matrix status is displayed to the crew on SPEC 62 and is part of the SM downlist. These data are acquired by the SM GPC via the PL 1 bus interface. The switch matrix data are read cyclically at 1.04 Hz. This read is handled by SM just as any other low rate read from the payload MDMs and is capable of being bypassed if two successive I/O errors occur on switch matrix reads.

The read is actually done out of its own special process as a Supervisor Call (SVC) read macro and is not part of the general SM Data Acquisition Read Table (DART) process. The read is initialized to ON at SM initialization and will announce an error for cases where the PDI is powered off. The read is also capable of being initiated by the PDI I/O reset item entry on SPEC 62 or via ground uplink. Once initiated, if the switch matrix read is subsequently bypassed, a class 3 error message, S62 BCE BYP PDI, is output. See Table 33-7 for a detailed description of the command word format used to initiate this process.

**Table 33-7. OP code table**



186113307. ART 1

| Operation code name | Bits |   |   |    |    | Description   |
|---------------------|------|---|---|----|----|---|
|                     | 7    | 8 | 9 | 10 | 11 |   |
| Load Switch Matrix  | 1    | 1 | 0 | 1  | 0  | Load data contained in following CDW into the switch matrix                               |
| Read Switch Matrix  | 1    | 1 | 0 | 0  | 0  | Read the requested data from the switch matrix and transmit to the requesting device      |
| Load Decom 1        | 0    | 1 | 0 | 1  | 0  | Load data transmitted from the GPC/data bus ports into decom 1 control memory             |
| Read Decom 1        | 0    | 1 | 0 | 0  | 0  | Read the requested data from decom 1 control memory and transmit to the requesting device |
| Load Decom 2        | 0    | 1 | 1 | 1  | 0  | Load data transmitted from the GPC/PCM data bus ports into decom 2 control memory         |
| Read Decom 2        | 0    | 1 | 1 | 0  | 0  | Read the requested data from decom 2 control memory and transmit to the requesting device |

*Table 33-7. OP code table (continued)*

| Operation code name  | Bits |   |   |    |    | Description  |
|----------------------|------|---|---|----|----|--|
|                      | 7    | 8 | 9 | 10 | 11 |  |
| Load Decom 3         | 1    | 0 | 0 | 1  | 0  | Load data transmitted from the GPC/PCM data bus ports into decom 3 control memory  |
| Read Decom 3         | 1    | 0 | 0 | 0  | 0  | Read the requested data from decom 3 control memory and transmit to the requesting device  |
| Load Decom 4         | 1    | 0 | 1 | 1  | 0  | Load data transmitted from the GPC/PCM data bus ports into decom 4 control memory  |
| Read Decom 4         | 1    | 0 | 1 | 0  | 0  | Read the requested data from decom 4 control memory and transmit to the requesting device  |
| Read Toggle Buffer   | 1    | 1 | 1 | 0  | 0  | Read TB data   |
| Write Data RAM       | 0    | 0 | 0 | 1  | 0  | Load data transmitted from the GPC/PCM data bus ports into the data RAM with starting address as defined by bits 12 through 22           |
| Read Data RAM        | 0    | 0 | 0 | 0  | 0  | Read data from the data RAM, starting with the requested address as defined by bits 12 through 22, and transmit to the requesting device |
| Return Received Word | 0    | 0 | 1 | 0  | 1  | Return the received word to the word-requesting device   |
| Read BSR             | 0    | 0 | 1 | 0  | 0  | Transmit the contents of the BSR to the requesting device  |
| Load FPM             | 0    | 0 | 0 | 1  | 1  | Load data into FPM, starting at address defined by bits 14 through 22 of this CW   |
| Read FPM             | 0    | 0 | 0 | 0  | 1  | Read data from FPM, starting at address defined by bits 14 through 22 of this CW   |

*Table 33-7. OP code table (continued)*

| Operation code name                           | Bits                 |    |    |    |          | Description   |
|---|----------------------|----|----|----|----------|---|
|   | 7                    | 8  | 9  | 10 | 11       |   |
| DETAILED CW/CDW/RDW BIT ASSIGNMENT DEFINITION |                      |    |    |    |          |   |
| Load Sw Matrix                                | CMD WD               |    |    |    |          | Bits 12-27 set to all zeros   |
| Read Sw Matrix                                | CMD DATA WD          |    |    |    |          | See end of table  |
|   | CMD WD               |    |    |    |          | Bits 12-22 - Spare set to all zeros<br>Bits 23-27 - Fix to all zero code                                |
|   | RDW                  |    |    |    |          | See end of table  |
| Load Decom 1                                  | CMD WD               |    |    |    |          |   |
|   | Bits 12-22           |    |    |    |          | 11-bit binary code, MSB first, from 0 to 2047 max., defining address of first data word in this message |
|   | Bits 23-27           |    |    |    |          | 5-bit binary code defining the number of cmd data words in this message as follows:                     |
|   | 23                   | 24 | 25 | 26 | 27       |   |
|   | 0                    | 0  | 0  | 0  | 0        | One word  |
|   | 0                    | 0  | 0  | 0  | 1        | Two words   |
|   | X                    | X  | X  | X  | X        | Binary conversion of XXXXX +1 word  |
| 1   | 1                    | 1  | 1  | 1  | 32 words |   |
|   | Bits 4-8             |    |    |    |          | Must be identical to 4-8 of preceding cmd word  |
|   | Bits 9-24            |    |    |    |          | 16 bits of data to be stored in decom format memory   |
|   | Bits 25-27           |    |    |    |          | Fixed to 101 code   |
| Load Decom 2                                  | Same as load decom 1 |    |    |    |          |   |
| Load Decom 3                                  | Same as load decom 1 |    |    |    |          |   |
| Load Decom 4                                  | Same as load decom 1 |    |    |    |          |   |

*Table 33-7. OP code table (continued)*

| Operation code name      | Bits                 |    |    |    |                   | Description  |
|--------------------------|----------------------|----|----|----|-------------------|--|
|                          | 7                    | 8  | 9  | 10 | 11                |  |
| Read Decom 1<br>(cont'd) | CMD WD               |    |    |    |                   |  |
|                          | Bits 12-22           |    |    |    |                   | 11-bit binary code, MSB first, from 0 to 2047 max., defining the location of the first data word requested from the decom control memory |
|                          | Bits 23-27           |    |    |    |                   | 5-bit binary code defining the number of response data words requested by this cmd word as follows:                                      |
|                          | 23                   | 24 | 25 | 26 | 27                |  |
|                          | 0                    | 0  | 0  | 0  | 0                 | One word   |
|                          | 0                    | 0  | 0  | 0  | 1                 | Two words  |
|                          | X                    | X  | X  | X  | X                 | Binary conversion of XXXXX +1 words  |
|                          | 1                    | 1  | 1  | 1  | 1                 | 32 words   |
|                          | Bits 4-8             |    |    |    |                   | Same as preceding command word   |
|                          | Bits 9-24            |    |    |    |                   | 16 bits of data from requested location  |
| Bits 25-27               |                      |    |    |    | Fixed to 101 code |  |
| Read Decom 2             | Same as read decom 1 |    |    |    |                   |  |
| Read Decom 3             | Same as read decom 1 |    |    |    |                   |  |
| Read Decom 4             | Same as read decom 1 |    |    |    |                   |  |
| Read Toggle Buffer       | CMD WD               |    |    |    |                   |  |
|                          | Bits 12-13           |    |    |    |                   | Spare set to logic "0"   |
|                          | Bits 14-22           |    |    |    |                   | 9-bit code, MSB first, from 1-511 binary count defining first location in FPM through which TB data are to be acquired                   |
|                          | Bits 23-27           |    |    |    |                   | Number of words as defined in load decom 1 above   |

*Table 33-7. OP code table (continued)*

| Operation Codes<br>Name        | Bits                  |   |   |    |                   | Description   |
|--------------------------------|-----------------------|---|---|----|-------------------|---|
|                                | 7                     | 8 | 9 | 10 | 11                |   |
| Read Toggle<br>Buffer (conc'd) | Response data<br>word |   |   |    |                   |   |
|                                | Bits 4-8              |   |   |    |                   | Same as preceding command word  |
|                                | Bits 9-24             |   |   |    |                   | 16 bits of data from a TB subsection. The actual TB subsection accessed is a function of the contents of the FPM location accessed and the TBI register |
|                                | Bits 25-27            |   |   |    |                   | Fixed to 101 code   |
| Write Data RAM                 | Command word          |   |   |    |                   | (This function available but not used)  |
|                                | Bits 4-6              |   |   |    |                   | PDI address   |
|                                | Bits 7-11             |   |   |    |                   | OP code   |
|                                | Bits 12-22            |   |   |    |                   | 11-bit binary code, MSB first, from 0-2047, defining starting address in the data RAM of the first CDW in this message                                  |
|                                | Bits 23-27            |   |   |    |                   | Number of words field as defined in load decom 1 above  |
|                                | Command data<br>word  |   |   |    |                   |   |
|                                | Bits 4-8              |   |   |    |                   | Same pattern as preceding CW  |
|                                | Bits 9-14             |   |   |    |                   | 16 bits of data to be stored in data RAM  |
| Bits 25-27                     |                       |   |   |    | Fixed to 101 code |   |
| Read Data RAM                  | Command word          |   |   |    |                   |   |
|                                | Bits 4-6              |   |   |    |                   | PDI address   |
|                                | Bits 7-11             |   |   |    |                   | OP - Code   |
|                                | Bits 12-23            |   |   |    |                   | 11-bit binary code MSB first from 0-2047, defining the starting address in the data   |
|                                | Response data<br>word |   |   |    |                   | RAM from which the first RDW following this command word is to be accessed  |
|                                | Bits 4-8              |   |   |    |                   | Same pattern as preceding CW  |

*Table 33-7. OP code table (continued)*

| Operation Codes<br>Name   | Bits               |   |   |    |                  | Description   |
|---------------------------|--------------------|---|---|----|------------------|---|
|                           | 7                  | 8 | 9 | 10 | 11               |   |
| Read Data RAM<br>(conc'd) | Bits 9-24          |   |   |    |                  | 16 bits of data from requested data RAM location  |
| Read BSR                  | Command word       |   |   |    |                  |   |
|                           | Bits 12-22         |   |   |    |                  | Spare set to logic "0"  |
|                           | Bits 23-27         |   |   |    |                  | Number of words field as identified in load decom 1 above   |
|                           | Response data word |   |   |    |                  |   |
|                           | Bits 4-8           |   |   |    |                  | 5-bit code identical to preceding command word  |
|                           | Bits 9-24          |   |   |    |                  | 16 bits of BSR  |
|                           | Bits 25-27         |   |   |    |                  | Fixed to "101" code   |
| Load FPM                  | Command word       |   |   |    |                  |   |
|                           | Bits 12-13         |   |   |    |                  | Spare set to logic "0"  |
|                           | Bits 14-22         |   |   |    |                  | 9-bit code, MSB first, from 0 to 511 binary count, defining starting address of first CDW in this message |
|                           | Bits 23-27         |   |   |    |                  | Number of words field as defined in load decom 1  |
|                           | Command data word  |   |   |    |                  |   |
|                           | (A) to address "0" |   |   |    |                  | (TBI register load)   |
|                           | Bits 4-8           |   |   |    |                  | Same as preceding CW  |
|                           | Bits 9-20          |   |   |    |                  | 12-bit code to be loaded into TBI register. See end of table  |
|                           | Bits 21-24         |   |   |    |                  | Spare set to logic "0"  |
|                           | Bits 25-27         |   |   |    |                  | Fix to 101 code   |
| (B) to addresses          |                    |   |   |    | 1-511 (FPM load) |   |



*Table 33-7. OP code table (concluded)*

| Operation code name  | Bits                 |   |   |                 | Description  |
|----------------------|----------------------|---|---|-----------------|--|
|                      | 7                    | 8 | 9 | 10 11           |  |
| Load FPM<br>(conc'd) | Bits 4-8             |   |   |                 | Same as preceding CW   |
|                      | Bits 9-12            |   |   |                 | 4-bit code to be loaded into the FPM at the appropriate address  |
|                      | Bits 13-24           |   |   |                 | Spare, set to logic "0"  |
|                      | Bits 25-27           |   |   |                 | Set to 101 code  |
| Read FPM             | Command word         |   |   |                 |  |
|                      | Bits 12-13           |   |   |                 | Spare set to logic "0"   |
|                      | Bits 14-22           |   |   |                 | 9-bit code, MSB first, from 0 to 511 binary count, defining the starting FPM address from which the contents of the first RDW in this message are to be accessed |
|                      | Bits 23-27           |   |   |                 | Number of words field as defined in load decom 1   |
|                      | Response data word   |   |   |                 |  |
|                      | (A) from address "0" |   |   |                 | (TBI register read)  |
|                      | Bits 4-8             |   |   |                 | Same as preceding CW   |
|                      | Bits 9-20            |   |   |                 | 12-bit code accessed from TBI register   |
|                      | Bits 21-24           |   |   |                 | Spare set to logic "0"   |
|                      | Bits 25-27           |   |   |                 | Set to 101 code  |
|                      | (B) from addresses   |   |   |                 | 1-511 (FPM read)   |
|                      | Bits 4-8             |   |   |                 | Same as preceding CW   |
|                      | Bits 9-12            |   |   |                 | 4-bit code accessed from FPM at the appropriate address  |
|                      | Bits 13-24           |   |   |                 | Spare set to logic "0"   |
| Bits 25-27           |                      |   |   | Set to 101 code |  |

If I/O errors occur where a message is announced, the last value of each affected parameter is maintained and an "M" is displayed next to the data on SPEC 62. The values will not be updated until a PDI I/O Reset is performed.

At initial PDI powerup or when a new SM GPC is brought on line, the PDI switch matrix, decoms, and FPM read zero on SPEC 62 and in the SM downlist.

#### **33.4.4 PDI Data Transfer to the PCMMU**

PDI data are transferred to the currently operating PCMMU in response to PCMMU PL fetch commands. The PDI data response is under control of the TB control logic or PDI data RAM control logic. Each of the PCMMU fetch commands contains an OP code that designates it to either the PDI TB, PDI data RAM, BSR read, DCM read, or WRAP test. On initial PDI turn-on, the PDI responds to fetch commands in the following manner:

- A. The data RAM responds with random data.
- B. The TB control logic, not having an FPM loaded, responds with fill ones.
- C. The BSR responds properly with real PDI status.
- D. The WRAP test also responds properly and turns around the PCMMU data.

#### **33.4.5 FDA Processing for S62 PDI Decom Fail**

If the first transition to SM OPS 2 takes place with the PDI powered on, no decoms loaded, and no input PL data stream, the PL data acquired by the PCMMU for SM display and FDA is random and may cause random PL FDA to occur. This is caused by the PDI data RAM coming up in a random state at PDI power-on and also by no data validity of the PDI data RAM being recognized by the PCMMU.

Because of the characteristics of the PDI data RAM/PCMMU interface, a method has been developed to determine the validity of PL data used for onboard display purposes. It should be remembered that for OI MDM data acquired from the PCMMU by the SM GPC, the PCMMU determines the status of such data and flags them as bad data via "E" bit to the SM GPC. When data are declared bad by the PCMMU, the SM GPC places an "M" status indicator next to all those parameters declared bad on all associated SM displays.

Since the PDI data RAM status is unknown to the PCMMU (that is, the PCMMU does not have information available for determining bad data and setting "E" bits and the status indicators), the SM GPC uses the PDI decom sync status to determine data validity. The individual PDI decoms used for PL data acquisition has their bit, word, and master frame status limit-sensed by SM FDA.

FDA processing is available for each decom. The formulas are based on the switch matrix assignment for each decom. The SM FDA processing looks for a source value between 1 and 6. If the source value is 0, the FDA does not announce a message.

Each FDA function for the PDI has two limit sets. Limit set 2 turns the alarm on. Limit set 1 keeps the alarm off. Limit sets are selected by precondition steering. Steering parameters for each decom are the associated bit, word, frame, and FDA enable parameters. To select limit set 2, bit, word, or frame must be 0 and FDA must be enabled. To select limit set 1, bit, word, and frame must be one or FDA must not be enabled.

If the PDI/PCMMU interface fails, the bit, word, and frame parameters go static in the PCMMU. This causes them to be comm faulted. SM will not use these parameters, so precondition processing is not performed. With no precondition steering to select the limit set, the FDA process defaults to limit set 1. The FDA alarm is not triggered. Other messages that occur are not related to the FDA processing described here.

SM provides only a class 3 error message, S62 PDI DECOM FAIL, and an SM alert tone for PDI data determined to be bad/invalid. Errors are flagged against a specific PDI decom. No "M" status indicators on individual PDI processed PL parameters are provided by SM software.

If the switch matrix read is bypassed, FDA processing no longer takes place. No alarm is triggered.

Four item entries on SPEC 62 are used to control the enable/inhibit states of decom FDA and display the status of the four PDI decoms. Each of these item entries can be toggled and will display, on S62, an asterisk adjacent to itself when enabled and a "blank" when inhibited. The items are used in the following manner:

- A given decom is loaded.
- Its input source (PL) selected.
- The PL data system activated.
- Its decom FDA is enabled.

Once this is accomplished, any failure or PL telemetry system problem or PDI decom problem causes the above described class 3 error message, etc. Prior to PL deactivation or switchover to another input port (such as for deploy), the original decom FDA should be inhibited.

Typically, the PDI data RAM data used by the SM GPC and the PDI Toggle Buffer data are downlinked.

### 33.5 TELEMETRY

#### 33.5.1 OI Telemetry

|           |  |
|-----------|--|
| V75M5130P | Decom Format ID (all four)             |
| V75M5110P | Switch Matrix                          |
| V75M6400P | PDI BITE Word 1                        |
| V75M6420P | PDI BITE Word 2                        |
| V75J5111D | Decom 1 Source                         |
| V75J5112D | Decom 2 Source                         |
| V75J5113D | Decom 3 Source                         |
| V75J5114D | Decom 4 Source                         |
| V75J5132D | Decom 1 Format ID                      |
| V75J5152D | Decom 2 Format ID                      |
| V75J5172D | Decom 3 Format ID                      |
| V75J5192D | Decom 4 Format ID                      |
| V75S5100E | PDI Power ON (Switch Scan)             |
| V75X4007D | PDI WRAP (PCM BITE Test Word Number 7) |
| V75X6401D | Decom 1 Frame Sync                     |
| V75X6402D | Decom 1 Word Lock                      |
| V75X6403D | Decom 1 Bit Lock                       |
| V75X6404D | Decom 1 Bit Rate Accuracy              |
| V75X6405D | Decom 2 Frame Sync                     |
| V75X6406D | Decom 2 Word Lock                      |
| V75X6407D | Decom 2 Bit Lock                       |
| V75X6408D | Decom 2 Bit Rate Accuracy              |
| V75X6409D | Decom 3 Frame Sync                     |
| V75X6410D | Decom 3 Word Lock                      |
| V75X6411D | Decom 3 Bit Lock                       |
| V75X6412D | Decom 3 Bit Rate Accuracy              |
| V75X6413D | Decom 4 Frame Sync                     |
| V75X6414D | Decom 4 Word Lock                      |
| V75X6415D | Decom 4 Bit Lock                       |
| V75X6416D | Decom 4 Bit Rate Accuracy              |
| V75X6421D | IOB No Response 1                      |
| V75X6422D | IOB1 Input Data Invalid                |
| V75X6423D | IOB No Response 2                      |
| V75X6424D | IOB2 Input Data Invalid                |
| V75X6425D | IOB No Response 3                      |
| V75X6426D | IOB3 Input Data Invalid                |
| V75X6427D | Toggle Buffer Parity                   |

|           |                 |
|-----------|-----------------|
| V75X6428D | Data RAM Parity |
| V75X6429D | FPM Parity      |
| V75X6430D | Decom 1 Parity  |
| V75X6431D | Decom 2 Parity  |
| V75X6432D | Decom 3 Parity  |
| V75X6433D | Decom 4 Parity  |
| V75X6434D | MTU IRIG        |
| V75X6435D | PCM 1.152 MHz   |
| V75X6436D | PDI Power       |
| V76X4376E | PDI RPC A ON    |
| V76X4378E | PDI RPC C ON    |

### 33.5.2 SM

|            |                      |
|------------|----------------------|
| V92J0078CY | FPM ID               |
| V92J0106CY | Decom 1 Source       |
| V92J0107CY | Decom 2 Source       |
| V92J0108CY | Decom 3 Source       |
| V92J0109CY | Decom 4 Source       |
| V92J0110CY | PDI Load (Status)    |
| V92J0111CY | Decom 1 DFL          |
| V92J0112CY | Decom 2 DFL          |
| V92J0113CY | Decom 3 DFL          |
| V92J0114CY | Decom 4 DFL          |
| V92X0908X  | Switch Matrix Bypass |
| V93X5576X  | Decom 1 FDA Enable   |
| V93X5577X  | Decom 2 FDA Enable   |
| V93X5578X  | Decom 3 FDA Enable   |
| V93X5579X  | Decom 4 FDA Enable   |

### 33.5.3 Special COMPs

|           |                  |
|-----------|------------------|
| M11J1500E | PDI WRAP (MOC)   |
| PDI_WRAP  | PDI WRAP (oimon) |

## 33.6 OPERATIONAL NOTES

### 33.6.1 Idiosyncrasies

If the PDI is powered off, an "M" is displayed on SPEC 62 next to ITEM 5 I/O RESET (PCMMU) because the GPC is still attempting to acquire PDI switch matrix status. Executing an item 5 momentarily clears the "M," but it will return. Use the FAULT

SUMMARY display to determine if there is any other PCMMU read element bypass causing the "M." (DR 55003)

If the PDI is not locked onto a data stream which supplies parameters for FDA, there may be occasional spurious FDA alarms. (DR 55332)

During a PDI load it is important to proceed from item 9 through item 13 on SPEC 62 in sequential order. If you select a decom and format to be loaded and then select an FPM prior to executing the decom load, the FPM load request results in the decom being loaded. (DR 52750)

Do not stack the decom select and format select items on SPEC 62 in one keyboard entry (e.g., item 9+1+4). This results in an illegal entry when you attempt to load the format with an item 11. Selecting items 9 and 10 independently avoids this problem. (DR 48499-F)

Problems with or losing the PL 1 bus does not mean DFLs, FPLs, and switch matrix elements cannot be loaded/configured. In addition, the PL MDM 1 may still be available. Talk with DPS to fully understand the bus problem.

For payloads with low command rates watch the "buffer busy" and "buffer available" telemetry.

For Smart Flex MDM (SFMDM) warm starts and PDI false lock indications, see Section 33.8.

### **33.6.2 Decom Format Constraints**

Decom formats are generated based on PL requirements defined by a Command and Data Annex to a Payload Integration Plan (PIP) for each specific flight. The Command and Data Annex is incorporated along with already defined orbiter data requirements into the MAST and PDI compiler for a specific flight. The PDI compiler is then used as the source for generating the PCMMU TFLs and PDI DFL/FPLs. A peculiarity of the compiler is that, for each set of PDI decom formats that are to be loaded and used simultaneously, the PCMMU is required to have a specific TFL set. A TFL set is defined here as a 128-kbps format and its companion, a 64-kbps format. It can now be deduced from this constraint that anytime a decom format is changed or moved to another decom, a new TFL or a new FPM set must be used by the PCMMU or PDI, respectively. Most 64-kbps formats have been deleted; only a few flight-specific TFL sets are required. Thus, only the 128-kbps format needs to be changed in most cases.

### **33.6.3 Payloads**

#### **33.6.3.1 Orbiter Interface Unit**

SPEC 212 parameters are fetched from the PCMMU when the OIU telemetry is being processed via the orbiter Payload Data Interleaver.

### 33.6.3.2 Spacehab

SPEC 206 (BFS), SPEC 210, and SPEC 215 parameters are fetched from the PCMMU during all phases of a Spacehab flight.

## 33.7 ANOMALIES

### 33.7.1 SFMDM Warm Starts and PDI False Lock Indications (IFA INCO-04)

LITE, TCS and ROMPS all received data via the PDI. Decoms 1 and 4 were programmed to process LITE HRD and LRD, respectively. LITE data were collected and formatted by an SFMDM. The SFMDM output consists of either high rate data or low rate data. At least 12 times during the mission, the SFMDM experienced a "warm start." This anomalous condition causes the SFMDM output to the PDI to revert from the normal high rate data (decom 1) to the low rate data stream. Warm starts were identified by telltale SM fault messages, the loss of decom 1 lock, and the acquisition of lock on decom 4.

Both the crew and MCC exercised the capability to restart the SFMDM. Once returned to the normal mode of operation, decom 1 indicates B/W/MF lock to the high rate stream and decom 4 indicates a loss of lock. This routine of trading lock indications between decoms 1 and 4 dominated, with one exception. As documented in INCO IFA-04, at GMT 256/13:53:00 after recovery from a warm start, decom 4 continued to show B/W/F lock. This single occurrence (1/17) motivated the anomaly and the request for noninterference troubleshooting at Kennedy Space Center (KSC). To this date, the "sticky" decom 4 indication has not repeated (in three attempts at KSC). Because of the low rate of incidence (1/20), the lack of impact to payload data processing, and the existence of an easy workaround (cycle source to 0), the anomaly has been closed as unexplained.

### 33.7.2 I/O Buffer Babble

Babble, which is characterized by continuous transmission of an I/O buffer, can occur when the I/O buffer receives a command word, followed by a signal similar to a command sync within 6  $\mu$ sec. In this instance, an illegal logic state is induced in the I/O buffer timing and control circuitry which generates an improper DECODE 15 pulse. This improper timing pulse fails to reset the LOAD counter, resulting in the generation of several LOAD signals, which load the WORD ALL 1s counter with all ones, and since it cannot increment, this sequence will continue until the unit is power cycled. A timing diagram of this mode of operations is shown in the PCMMU Theory of Operations Maintenance Manual, Section 1.4.5.4.1.

## 33.8 REFERENCES

- A. PDI Spec, MC476-0136, 9-25-79.
- B. DI Critical Design Review, 6-20-78.

- C. Software Design Specification, Part II - Detailed Design Specification, Volume III - Applications, Part 2 - Systems Management, NAS 9-16920.
- D. Systems Management, Level C, Flight Software Requirements (FSR), JSC-19590-27.
- E. Intermediate and Depot Maintenance Manual, PDI Theory of Operations, SFOC-LO 0009.



THIS PAGE INTENTIONALLY BLANK

## SECTION 35 - MODULAR AUXILIARY DATA SYSTEM

### CONTENTS

| Section |                                | Page  |
|---------|--------------------------------|-------|
| 35.1    | GENERAL DESCRIPTION .....      | 35-1  |
| 35.2    | INTERFACES .....               | 35-1  |
| 35.2.1  | Controls and Displays .....    | 35-1  |
| 35.2.2  | Sensors.....                   | 35-5  |
| 35.3    | DESCRIPTION .....              | 35-5  |
| 35.3.1  | Electrical .....               | 35-5  |
| 35.3.2  | Mechanical.....                | 35-23 |
| 35.3.3  | Software.....                  | 35-23 |
| 35.3.4  | Location .....                 | 35-24 |
| 35.3.5  | Temperature Control.....       | 35-27 |
| 35.4    | DESCRIPTION OF OPERATION ..... | 35-27 |
| 35.4.1  | Crew Control.....              | 35-27 |
| 35.4.2  | Ground Commands .....          | 35-27 |
| 35.4.3  | Telemetry.....                 | 35-28 |
| 35.4.4  | Operational Instructions ..... | 35-29 |
| 35.5    | SUMMARY DATA.....              | 35-30 |
| 35.6    | OPERATIONAL NOTES .....        | 35-31 |
| 35.7    | REFERENCES .....               | 35-32 |

## TABLES

| Table |  | Page  |
|-------|--|-------|
| 35-1  | MADS component power usage.....  | 35-6  |
| 35-2  | MADS power for each orbiter.....   | 35-6  |
| 35-3  | FDM VCO for loss of any single oscillator.....                                 | 35-7  |
| 35-4  | FDM composite BITE status levels.....  | 35-7  |
| 35-5  | Conditions for FDM Mux BITE.....   | 35-8  |
| 35-6  | Recorder main operating SPECS.....   | 35-10 |
| 35-7  | MADS data recorder ranges for tape speed.....                                  | 35-11 |
| 35-8  | MADS uplink commands.....  | 35-17 |
| 35-9  | Typical track assignments.....   | 35-21 |
| 35-10 | PNL A6L switch effects.....  | 35-27 |
| 35-11 | MADS measurements transmitted via<br>operational instrumentation downlink..... | 35-29 |
| 35-12 | MADS component operating temperature limits.....                               | 35-30 |
| 35-13 | Recorder data rates.....   | 35-30 |

## FIGURES

| Figure |   |       |
|--------|---|-------|
| 35-1   | OV-103 overview.....                        | 35-2  |
| 35-2   | OV-104 overview.....                        | 35-3  |
| 35-3   | OV-105 overview.....                        | 35-4  |
| 35-4   | PNL C3.....                                 | 35-5  |
| 35-5   | PNL A6L.....                                | 35-5  |
| 35-6   | FASCOS.....                                 | 35-23 |
| 35-7   | MCM and recorder location (OV-103/104)..... | 35-24 |
| 35-8   | MCM and recorder location (OV-105).....     | 35-25 |
| 35-9   | MADS shelf 8 location.....                  | 35-26 |
| 35-10  | Generic MADS overview.....                  | 35-31 |

## SECTION 35 MODULAR AUXILIARY DATA SYSTEM

### 35.1 GENERAL DESCRIPTION

The Modular Auxiliary Data System (MADS) is a nonredundant instrumentation system onboard that measures and records selected pressure, temperature, strain, vibration, and event data during flight. MADS supplements the Operational Instrumentation (OI).

The purpose of the MADS system is to collect detailed data during all flight phases for later analysis on the ground. Data collected by the MADS system is recorded onboard and is not available until after landing.

The MADS system is controlled primarily from the ground.

### 35.2 INTERFACES

Figures 35-1, 35-2, and 35-3 show the system and its interfaces for each orbiter.

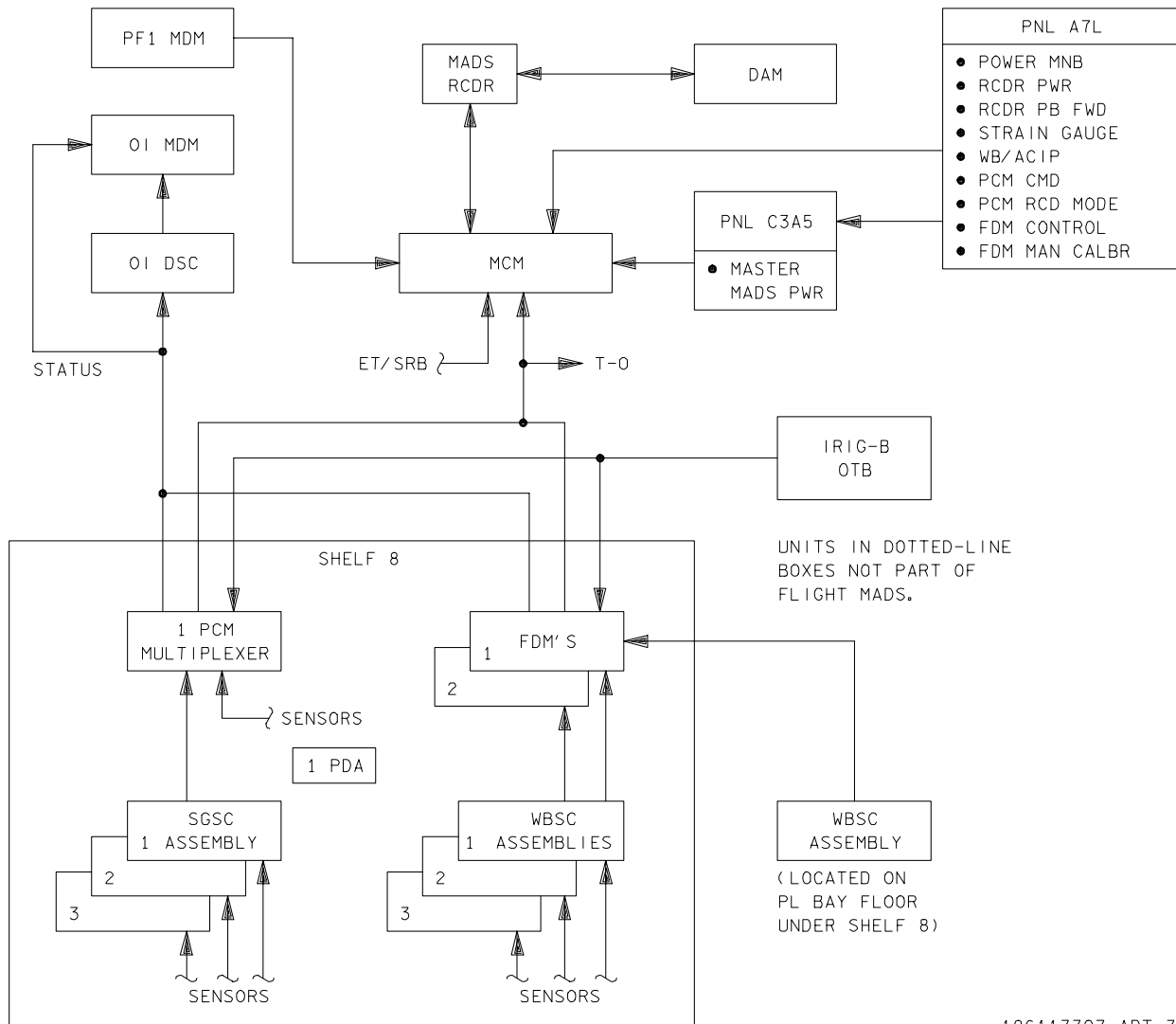
The MADS will record approximately 314 measurements throughout the orbiter for OV-105, 300 for OV-104, 620 for OV-103. There are 21 OI status measurements via Multiplexer/Demultiplexer (MDM) OA3, OA2, OF2, and OF1. There are 11 uplink commands via MDM PF1. The system is intended to be controlled primarily from the ground. An interface with the orbiter timing buffer exists to allow inclusion of IRIG-B timing. A master power switch is located on panel C3, and component power and other controls are on aft flight deck panel A6L. Additionally, a Driver Amplifier Module (DAM), carry-on ground support equipment, is used to dump the recorder after landing.

#### 35.2.1 Controls and Displays

Uplink commands are intended to be the primary method of systems control with the crew acting in a backup role. Although controls are available to the crew, they are intended primarily for preflight checkout and postflight data recovery.

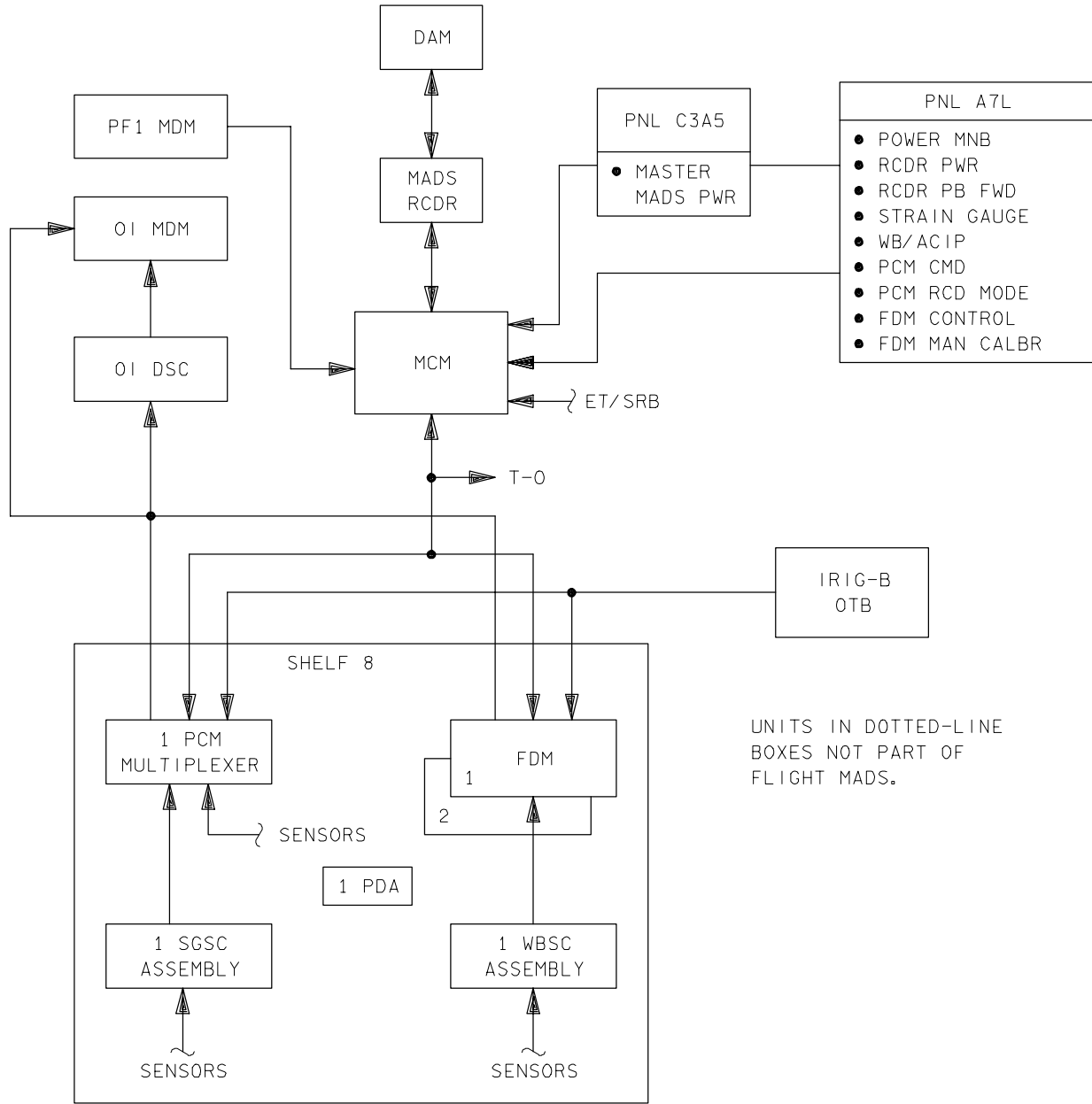
The control panel C3 and A6L for all orbiters are shown in Figure 35-4 & Figure 35-5.

There are no crew displays other than these switches.



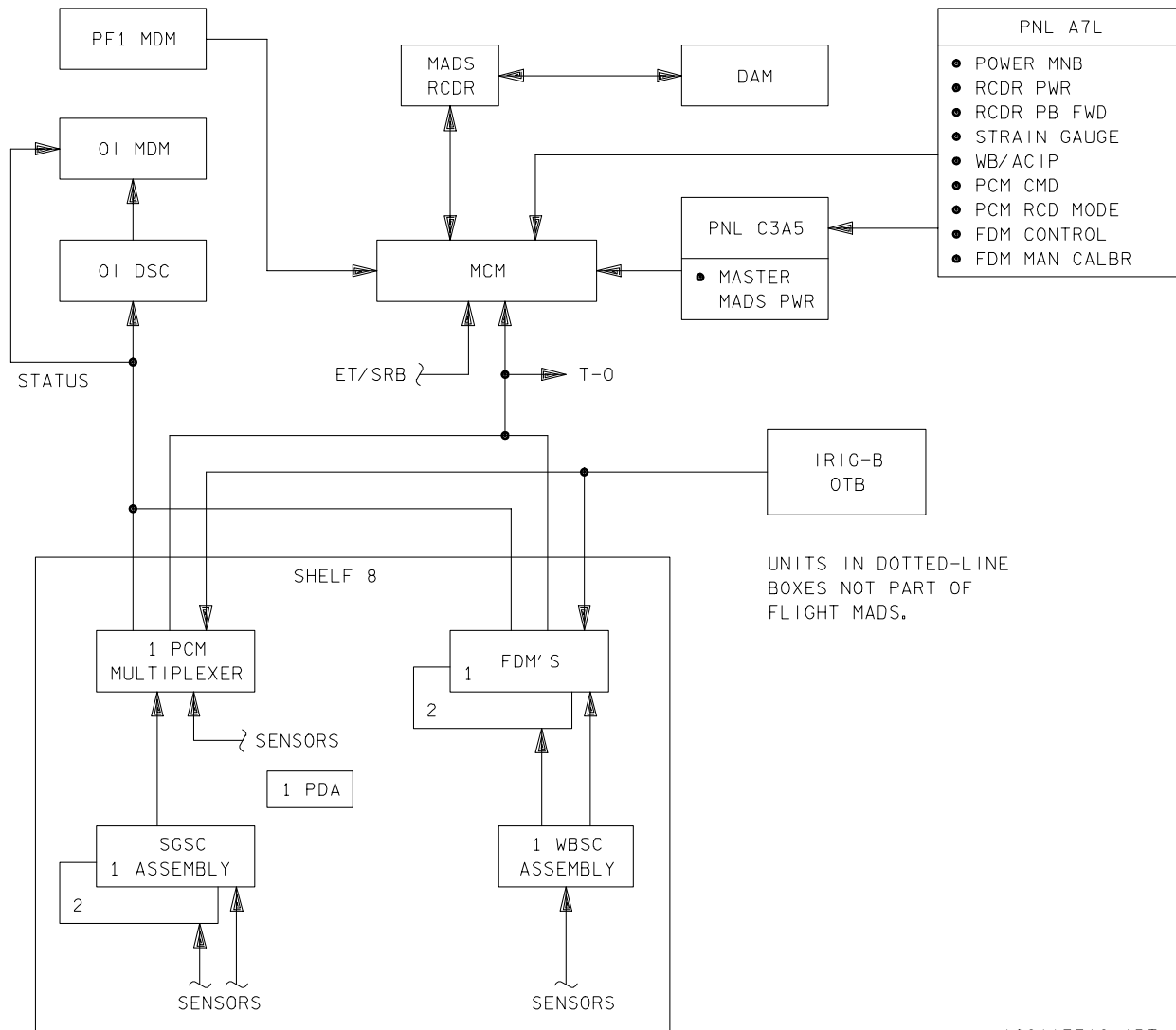
186113307. ART 3

Figure 35-1. OV-103 overview



186113308. ART 3

Figure 35-2. OV-104 overview



186113312. ART 1

Figure 35-3. OV-105 overview

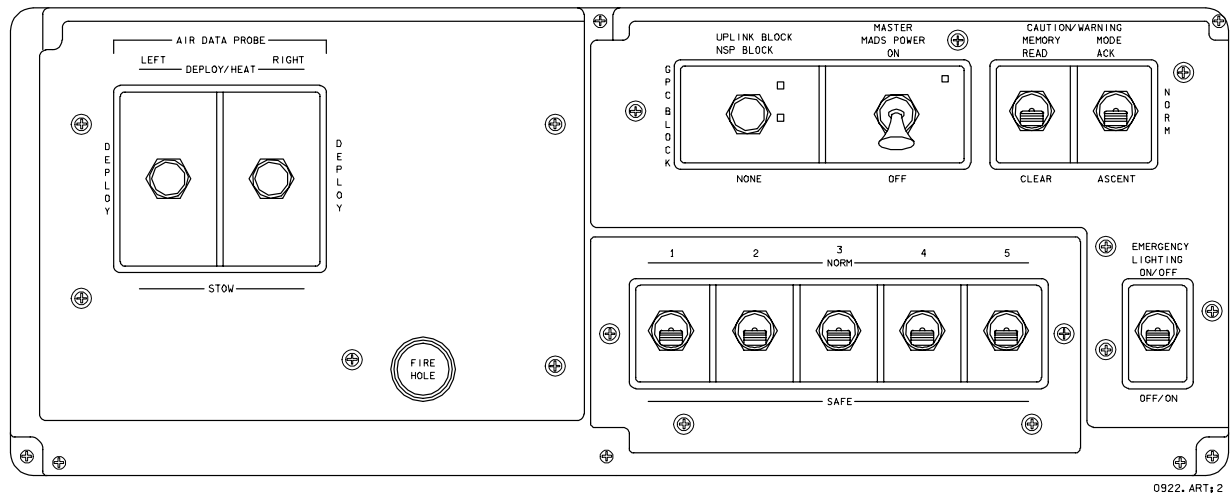


Figure 35-4. PNL C3

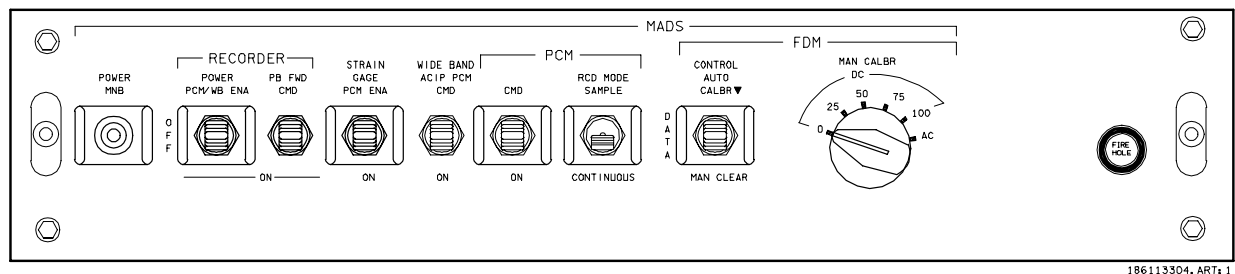


Figure 35-5. PNL A6L

### 35.2.2 Sensors

MADS uses temperature sensors, pressure sensors, strain sensors, accelerometers, vibration sensors, and acoustic pickups.

### 35.3 DESCRIPTION

#### 35.3.1 Electrical

All units are fused within the Power Distribution Assembly (PDA) by either 3- or 5-amp fuses. Each MADS bus is controlled by 15-amp Remote Power Controllers (RPCs).

MADS Wide-Band Signal Conditioner (WBSC), Strain Gauge Signal Conditioner (SGSC), and Frequency Division Multiplexer (FDM) power comes from MNA through MPC-1 (SGSC through RPC-13, WBSC and FDM through RPC-14), while Pulse Code Modulation (PCM) power comes from MNB through MPC-2, RPC-14. Recorder power comes from MNB, through FPC-2, RPC-49 (which is enabled by the RECORDER POWER switch on A6L). The AUTOCAL command comes from MDM PF1 and goes through forward load control assembly 1 (FLCA-1) to allow MNA power for calibration.

See Table 35-9 for switch/command relationships.



Table 35-1 shows the amount of power that will be consumed by each component. Table 35-2 shows how much power is consumed by each vehicle MADS installation.

**Table 35-1. MADS component power usage**

| Unit               | Power total in watts            |
|--------------------|---------------------------------|
| FDM                | 50                              |
| PCM                | 68                              |
| MADS recorder      | 140 (max, 59 stby, 110 nominal) |
| MCM                | 20.7                            |
| WBSC               | 0.6 each                        |
| SGSC               | 6, 3.7, or 6.7 each             |
| Sensors (pressure) | 2.0 or 0.3 each                 |
| Sensors (accel.)   | 0                               |
| PDA                | 0                               |

**Table 35-2. MADS power for each orbiter**

| Vehicle:          | OV-103    | OV-104    | OV-105    |
|-------------------|-----------|-----------|-----------|
| Unit #            | #/total W | #/total W | #/total W |
| FDM #             | 2/100     | 2/100     | 2/100     |
| PCM               | 1/68      | 1/68      | 1/68      |
| MADS recorder     | 1/110     | 1/110     | 1/110     |
| MCM               | 1/20.7    | 1/20.7    | 1/20.7    |
| WBSC              | 35/21     | 27/16.2   | 25/15     |
| SGSC              | 57/257.9  | 7/33.9    | 43/186.1  |
| Sensor (pressure) | 12/24     | -----     | -----     |
| Total             | 601.6 W   | 348.8 W   | 499.8 W   |

Note: 1. This is as up-to-date as possible as of 7/1/93. Since MADS changes configuration on every vehicle between every flight, it is a close estimate, and probably does not vary much.

Note: 2. Some numbers do not seem to work out because not all WBSC and SGSC consume the same amount of power.

### 35.3.1.1 FDM

The FDM is an analog data modulation package that contains four multiplexers (mux). Each mux contains 15 channels, and each channel has its own Voltage Controlled Oscillator (VCO); therefore, up to 60 measurements may be multiplexed together by each FDM.

A. FDM Output

The 15 VCOs are summed together into a composite mux output and fed to the MCM (for routing to a single track of the MADS recorder) and also to the T-0 umbilical. Each VCO has a constant bandwidth with separate center frequencies. A 240-kHz reference signal is mixed with each composite for the purpose of the tape speed compensation (WOW and flutter correction).

B. Built-In Test Equipment (BITE)

The nominal (RMS) voltage level of each of the four composite outputs is 0.9995 volt. This output level is sensed by the FDM BITE circuitry. When the level is nominal, the mux BITE output is high ( $5 \pm 1$  V dc). Should the output level increase or decrease ( $3 \pm 1$  dB), the BITE output is low ( $0 \pm .5$  V dc). A failed condition must be evaluated as to cause and effect. Table 35-3 lists the resultant signal level in case of the loss of a single VCO. You can see that the failure of just one VCO will not cause a BITE fail but that the failure of the 240 kHz reference channel could (but also could not) and the failure of multiple VCOs could (but also could not). The uncertainty is due to the plus or minus one dB tolerance in the BITE circuitry level detection. Table 35-4 lists the FDM composite Root Mean Square (RMS) voltage levels and percentage levels and shows the chances of having a BITE fail. Table 35-5 summarizes the conditions that could cause a failed BITE.

**Table 35-3. FDM VCO for loss of any single oscillator**

| FDM input channel | VCO center frequency kHz | VCO deviations $\pm$ kHz | Nominal data frequency Hz | VCO output (Vrms)            | VCO output (Vrms) <sup>2</sup> | Loss of single VCO | Resultant sum of squares | Resultant composite level (Vrms) | BITE status |
|-------------------|--------------------------|--------------------------|---------------------------|------------------------------|--------------------------------|--------------------|--------------------------|----------------------------------|-------------|
| 1                 | 12                       | 1                        | 500                       | 0.070                        | 0.0049                         | 1                  | 0.99427                  | 0.9971                           | No BITE     |
| 2                 | 16                       | 1                        | 500                       | .070                         | .0049                          | 2                  | .99427                   | .9971                            | No BITE     |
| 3                 | 20                       | 1                        | 500                       | .070                         | .0049                          | 3                  | .99427                   | .9971                            | No BITE     |
| 4                 | 24                       | 1                        | 500                       | .070                         | .0049                          | 4                  | .99427                   | .9971                            | No BITE     |
| 5                 | 28                       | 1                        | 500                       | .070                         | .0049                          | 5                  | .99427                   | .9971                            | No BITE     |
| 6                 | 32                       | 1                        | 500                       | .070                         | .0049                          | 6                  | .99427                   | .9971                            | No BITE     |
| 7                 | 36                       | 1                        | 500                       | .070                         | .0049                          | 7                  | .99427                   | .9971                            | No BITE     |
| 8                 | 48                       | 4                        | 2000                      | .417                         | .013689                        | 8                  | .98548                   | .9927                            | No BITE     |
| 9                 | 64                       | 4                        | 2000                      | .417                         | .013689                        | 9                  | .98548                   | .9927                            | No BITE     |
| 10                | 80                       | 4                        | 2000                      | .417                         | .013689                        | 10                 | .98548                   | .9927                            | No BITE     |
| 11                | 96                       | 4                        | 2000                      | .417                         | .013689                        | 11                 | .98548                   | .9927                            | No BITE     |
| 12                | 112                      | 4                        | 2000                      | .417                         | .013689                        | 12                 | .98548                   | .9927                            | No BITE     |
| 13                | 128                      | 4                        | 2000                      | .417                         | .013689                        | 13                 | .98548                   | .9927                            | No BITE     |
| 14                | 144                      | 4                        | 2000                      | .417                         | .013689                        | 14                 | .98548                   | .9927                            | No BITE     |
| 15                | 184                      | 16                       | 8000                      | .523                         | .273529                        | 15                 | .72564                   | .8519                            | No BITE     |
| REF               | 240                      | NA                       | NA                        | .744                         | .553536                        | REF                | .44564                   | .6696                            | May BITE    |
|                   |                          |                          |                           | Sum of squares               | 0.999171                       |                    |                          |                                  |             |
|                   |                          |                          |                           | RMS level ( $\sqrt{\quad}$ ) | .9995                          |                    |                          |                                  |             |

**Table 35-4. FDM composite BITE status levels**

| Level V RMS       | BITE indication | Level percent     |
|-------------------|-----------------|-------------------|
| 1.585 to $\infty$ | Fail (0)        | 158.5 to $\infty$ |
| 1.259 to 1.585    | ? (1 or 0)      | 125.9 to 158.5    |
| 0.794 to 1.259    | Good (1)        | 79.4 to 125.9     |
| 0.631 to 0.794    | (1 or 0)        | 63.1 to 79.4      |
| 0 to 0.631        | Fail (0)        | 0 to 63.1         |

**Table 35-5. Conditions for FDM Mux BITE**

| Failure mode                             | Mux 1-4 BITE indication |
|--|-------------------------|
| BITE circuit failure                     | Fail (0)                |
| Loss of composite signal                 | Fail (0)                |
| Loss of any single channel, 1 through 15 | Good (1)                |
| Loss of reference channel (240 kHz)      | ? (0 or 1)              |
| Loss of reference channel and channel 15 | Fail (0)                |
| Loss of channels 1 through 15            | ? (0 or 1)              |
| Mux output cable short                   | ? (0 or 1)              |

C. Calibration

Note: The FDM must be powered on at least 10 seconds prior to calibration to ensure proper calibration.

Calibrating the FDM can be done manually by the two calibration switches on panel A6L or be done automatically by uplink command or crew switch.

Manually, the FDM CONTROL switch must be put into the MAN CALBR position, and the FDM MAN CALBR rotary switch must be rotated through each of the six positions, pausing for at least a second at each. When finished, turn the FDM CONTROL switch to DATA and return the MAN CALBR rotary to 0.

Automatic calibration is initiated by either uplink command or by putting the control switch on A6L to AUTO CALBR. Both must be present for at least 2 seconds. Note that, in order to get the FDM to calibrate itself again after uplinking the AUTOCAL command once, the MADS AUTO FDM CAL-OFF command must be sent. The automatic sequence applies each of the six calibration signals in sequence for approximately 1 second each. The mode is then automatically

returned to DATA. The FDM provides a “high” status signal when the FDM calibration switching circuitry is in the DATA mode and a “low” signal when in the CAL mode. A calibration status signal may be generated by the following conditions:

- MADS powered down or put in OFF/STBY.
- FDM being calibrated.
- Calibrator failure.
- Power supply number 1 failure (see note below).
- Power turned off to power supply number 1 (see note below).
- Output cable shorted to ground.

Note: This condition would also generate MUX1 and MUX2 BITE indications simultaneously. A power supply number 2 failure would generate MUX 3 and MUX 4 BITE indications.

#### **35.3.1.2 PDA**

The MADS PDA provides power distribution and circuit protection for each of the MADS Line Replaceable Units (LRUs) in the payload bay. This unit receives source power from the switches on panel A6L or uplink command via the MADS Control Module (MCM). The PDA contains three power buses. Bus 1 powers the PCM multiplexers. Bus 2 powers the SGSC chassis. Bus 3 powers the FDMs, the WBSC chassis, and the pressure sensors. All units are fused within the PDA by either 3- or 5-amp fuses. Each bus is controlled by 15-amp RPCs.

#### **35.3.1.3 Signal Conditioners (SGSC/WBSC)**

The signal conditioners located on shelf 8 consists of the WBSC and the SGSC.

- A. WBSC is a charge amplifier that conditions vibration, acoustic, and POGO measurements from piezoelectric transducers. The WBSC chassis has the capability to condition 28 measurements. Each measurement is routed to its particular charge amplifier and conditioned. The output of the charge amplifier will be biased at 2.50 V dc and will be routed to the MADS FDM for frequency multiplexing.
- B. SGSC is a four-channel device capable of exciting a half or full strain gauge bridge and conditioning bridge output from 0 to 5 V dc. Since each of the four channels is independent of each other, each unit has the capability of adjusting the bias, balance, and gain for each channel. The output of each SGSC is routed to the Pulse-Code Modulation Unit (PCMU) for processing before it is recorded on the MADS data recorder. There can be up to 19 SGSCs per chassis.

### 35.3.1.4 MADS Recorder

#### A. General Description

The MADS recorders are basically off-the-shelf Bell and Howell Modular Recording System (MARS) recorders. The MARS recorder is a coaxial, reel-to-reel, 28-track, wideband recorder employing dual differential capstan drive and servo-controlled capstan/reel motors. The tape length of 9000 feet allows for 2 hours of recording per track at a speed of 15 inches per second. Playback heads are provided, but no playback electronics are incorporated into the MARS recorder. Carry-on playback amplifiers contained in a Driver Amplifier Module (DAM) are used to dump the recorded data to Ground Support Equipment (GSE) after landing. The main operating SPECs are summarized in Table 35-6.

#### 1. Tape motion

The tape motion signal is generated by a dual one-shot circuit, which gives a relay closure when the rotation frequency of one of the guide rollers (as sensed by an optical sensor) is above approximately 0.8 Hz. At a speed of 1-7/8 ips, motion telemetry may not be high, since the required rotational frequency may not exist, but this speed is not used.

**Table 35-6. Recorder main operating SPECs**

#### COOLING - AIR INPUT PWR

dc voltage 25 to 31 V dc (28 V nom)  
dc current 15 amps (max)  
dc power

| Mode        | Power (Watts) |
|-------------|---------------|
| STBY        | 58            |
| RCD         | 96.3          |
| PB (15 ips) | 59            |
| PP (60 ips) | 67            |

#### ENVIRONMENTAL LIMITS

Temp - 35° to 120° F  
Pressure - 12.7 - 18 psia

**Table 35-7. Recorder main operating SPECs (concluded)**

PERFORMANCE

Modes - Forward  
Reverse  
Record  
Stop

Speed - 1-7/8, 3-3/4, 7-1/2, 15, 30, 60 ips  
Start and stop times - 5 sec max to 60 ips  
Crosstalk - 30 dB min at 15 ips  
Freq response at 15 ips - 400 Hz - 250 Hz  $\pm$  6 dB on any channel

PWR sensing circuit limits - Upper - 37.0  $\pm$  2 V  
Reset - 33.0  $\pm$  2 V  
  
Lower - 22  $\pm$  2 V  
Reset - 24  $\pm$  2 V

DIMENSIONS H x W x L = 7-1/2 x 16.12 x 24 in.

**Table 35-8. MADS data recorder ranges for tape speed**

| Tape speed (ips) | Analog frequency range | Digital biphas-L bit rate (kbps) |
|------------------|------------------------|----------------------------------|
| 60               | 400 Hz to 1 MHz        | 32 to 512                        |
| 30               | 400 Hz to 500 kHz      | 16 to 256                        |
| 15               | 400 Hz to 250 kHz      | 8 to 128                         |
| 7-1/2            | 400 Hz to 125 kHz      | 4 to 64                          |
| 3-3/4            | 400 Hz to 625 kHz      | 2 to 32                          |
| 1-7/8            | 400 Hz to 31.25 kHz    | 1 to 16                          |

2. Protection circuit (BITE no. 1)

The protection circuit of the MARS recorder will not shut down power to all recorder circuitry if trouble is indicated. The BITE is low in the MADS recorder whenever trouble is indicated by the protection circuit. The BITE 1 signal is set for any of the following reasons.

- a. Input voltage above 37  $\pm$  2 V. Reset at 33  $\pm$  2 V.  
Input voltage below 22  $\pm$  2 V. Reset at 24  $\pm$  2 V.
- b. Any of the sensor lights in the tension sensor arm burn out.

In the case of over or under voltage, the BITE is reset when the problem is corrected (reset levels listed above), but for sensor lights out, power must be removed from the recorder and reapplied to reset the BITE circuit. (If the fault still exists, the recorder will indicate the BITE again.)

3. Record telemetry (BITE no. 2)

The record telemetry indicates that the record function is in progress, and is high when:

- c. The record amps have power present.
- d. The bias oscillator has power present.
- e. The servo indicates phase lock (up to speed).

4. Percent tape (analog)

The recorder outputs an analog voltage to indicate the amount of tape on the supply reel. A +10 V indicates a full BOT condition and 0 V indicates an empty (EOT) condition of the supply reel. This voltage is provided by a 1-K $\Omega$  (1850 turn) potentiometer, of which only 50 $\Omega$  (92 turns) is used to represent 0 to 100 percent.

5. Power

The recorder uses 28 V (nominal) power provided to the MARS recorder protection circuit. From the protection circuits, power is delivered to the transport Voltage Regulator (VR). The transport VR supplies power for all electronics, except the record amps, bias oscillator, and erase amp, which are supplied by the record VR and the bias amp, which is powered from the protection circuits. The record VR is on only for the record and erase modes.

6. Operation

The recorder will run whenever a speed is selected by grounding one of the speed select inputs. There are no stop or start commands; the recorder stops if no speed is selected. Record becomes active on the recorder whenever power (28 V) is applied to the record power input, but the tracks to be recorded are selected separately.

The recorder erase mode is remotely controlled by the GSE. The recorder will operate in the reverse direction whenever 28 V is applied to the reverse replay input. This reverses polarity to the capstan motor and reverses the operation of the tension switches (used to remove tape slack).

7. EOT/BOT

EOT/BOT is indicated by an optical sensor "seeing" a window approximately 15 feet from the end where the ferric oxide compound was chemically

removed. This causes the speed select relays to drop out (no speed selected) and the recorder will stop. If the opposite direction is selected, the recorder will change direction and continue in the record mode. However, all other circuits are still powered up. (There is no power shutdown.)

#### B. MADS recorder

A MARS recorder will be used to record MADS wideband and MADS PCM data. The recorder will be located in volume D of the crew compartment and will be controlled by either uplink command through MDM PF1 or crew switches on panel A6L. This control will be via a MADS Control Module (MCM) also located in volume D of the crew compartment. Basically the MCM allows the recorder to be rewound to BOT at 60 ips or to EOT at 15 ips. The MCM selects tracks to be recorded, speeds, controls power to the various MADS components, and will control a sample mode for PCM data. The MADS recorder has individual track selection relays (28) which are grouped in the MCM into three "passes".

Corrective Action Report (CAR) KB2089-010 documented a recorder failure on OV-103 prior to the STS-42 mission that is attributed to reel brake contamination and degradation which allowed tape slack and looping after an abrupt power cutoff while in the OPF. The abrupt power cutoff occurred while the tape was still in motion. The STS-53 prelaunch anomaly showed that damage can occur to the tape recorder when it is in the flight configuration. To avoid damaging the tape, the recorder motion must be stopped before removing power from the recorder. This has been corrected procedurally by having the recorder power switch on panel A6L in the ON position during MADS operations. The crew then takes the MADS recorder power to PCM/WB ENA on MCC go after the MCC has commanded MADS WB OFF and MADS PCM OFF. This action ensures the tape motion is stopped before removing recorder power. STS-59 (OV-105), STS-63 (OV-103), and OV-104 OMDP-1 and subsequent flights will include a hardware modification that will allow the MCC to command the recorder power on and off.

The CAR sums up the investigation by stating that the tape operating procedures at the time of failure could have contributed to the failure by wearing the brake prematurely. In addition, the change in orientation when the recorder was moved from the OPF to the VAB with slack in the tape path could have caused the tape to fall out of the correct tape path causing breakage. However, the most probable cause of tape breakage was attributed to contamination of the supply reel brake band.

#### 35.3.1.5 PCM Multiplexer

The PCM multiplexer operates under control of internally generated clock and sync signals to accept and condition 5 V and 28 V discretes, high and low level analogs, bipolar analogs, and bridge completion data. These data are multiplexed, encoded, and formatted into either a 32-kbps or 64-kbps serial bit stream for output to the MCM or T-0 umbilical. An IRIG-B Greenwich Mean Time (GMT) timing input is received from the Orbital Timing Buffer (OTB) for time correlation purposes.



A. PCM input

The capacity of signals by input type is as follows.

| <u>Type</u>  | <u>No.</u> |
|--|------------|
| High level analog (SGSC chassis and pressure transducers):<br>(0 - 5 V dc) | 128        |
| Low level analog (thermocouples and radiometers):                          |            |
| 10 mV  | 35         |
| 20 mV  | 40         |
| 30 mV  | 29         |
| 40 mV  | 16         |
| 60 mV  | 4          |
| 15 mV w/PPS(a)   | 48         |
| 15 mV w/o PPS(a)   | 16         |
| Bipolar analog:  |            |
| Plus or minus 5 V dc   | 16         |
| Bridge completion:   |            |
| N/A  | 168        |
| Low level discrete (5 V dc):   |            |
| 1 = 2.5 to 5 V dc  | 14         |
| 0 = 0 to 0.5 V dc  |            |
| High level discrete (28 V dc):   |            |
| 1 = 10 to 28 V dc  | 16         |
| 0 = 0 to 4 V dc  |            |

Precision power supply excitation supplied by the PCMU.

B. PCM output

The serial PCM output signal is a nominal 5 volts Manchester II biphasic L. A frame sync pattern is generated and appears at the beginning of each minor frame.

|             |      |      |
|-------------|------|------|
| Sync word 1 | 1111 | 1010 |
| Sync word 2 | 1111 | 0011 |
| Sync word 3 | 0010 | 0000 |

Minor frame identification is generated and appears in the fourth word of each minor frame. The first minor frame is identified by the binary count of "0000 0000" and is incremented by 1 until the full complement of minor frames are counted in each master frame and then reset. Each data word is eight bits transmitted MSB first.

C. PCM formats

Minor frame length, master frame length, and data sequencing and sampling rate is programmable by the use of a PROM. The capability for up to four formats is provided, but only two are planned to be used.

| Format                        | <u>1</u> | <u>2</u> |
|-------------------------------|----------|----------|
| Bits per word                 | 8        | 8        |
| Words per minor frame         | 80       | 160      |
| Minor frames per master frame | 50       | 50       |
| Data rate                     | 32 kbps  | 64 kbps  |

The signal for switching between formats originates in the MCM. The 64 kbps are selected automatically whenever wideband data are recorded.

The 32 kbps format is selected whenever you are not in wideband mode (send 4602 MADS WB/ACIP OFF to go from 64 to 32 kbps format).

D. PCMU BITE

The PCMU contains BITE circuitry to verify operational status. Reference voltages are generated and used to check out the encoding process for most types of signal inputs. All the individual comparisons will be OR'ed together into a single discrete and sent to OI as a GO/NO-GO output. This composite BITE is reset to a logic 1 (normal operation) after being read by the format.

The BITE circuitry verifies the correct operation of the low level discrete (5 V dc) group module, the high level analog group module, and each gain step in the low level analog group module. Bipolar analogs and high level discrettes are not checked.

- Low level discrete module verification
- To verify correct encoding, a threshold voltage  $V_{th}$  is generated between 0.5 and 2.5 V dc which are the "guaranteed" levels for determining a "0" or "1," respectively. Then two other signals are generated: one between  $V_{th}$  and 2.5 V dc and the other between 0.5 V dc and  $V_{th}$ . The outputs should result in a "1" and a "0," respectively, which in effect provides a tighter tolerance on the bilevel group than that required by the specification. Correct operation results in a BITE normal.
- High level analog module verification
- Two reference voltages are generated: one at 20 percent of full scale and the other at 80 percent of full scale. Each voltage is sampled, converted by the Analog-to-Digital (A/D) converter, and inserted into the output format. The output of each is then checked against a specified tolerance. If within

tolerance, the group module and the A/D converter are assumed to be operating correctly, and the BITE output is normal.

- Low level analog module verification
- Verification of these modules is accomplished using reference voltages as described for the high level analog signals. Most reference voltages are included in the output format for recording and postflight analysis. If a BITE fail indication occurs in flight, the only action is likely to be an attempted power cycle.

### 35.3.1.6 IRIG-B Decoder

The decoder decodes IRIG-B time received from the orbiter timing buffer to 10 ms resolution and provides this into the output format as follows:

| <u>Bits</u> |                   | <u>Content</u>   |
|-------------|-------------------|------------------|
| 1-10        | Days 1-365        | BCD MSB first    |
| 11-16       | Hours 0-23        | BCD MSB first    |
| 17-23       | Minutes 0-59      | BCD MSB first    |
| 24-30       | Seconds 0-59      | BCD MSB first    |
| 31-38       | Milliseconds 0-99 | Binary MSB first |

### 35.3.1.7 Protection - Overvoltage/Short Circuit

No signal conditioning circuit (analog or digital) will be damaged whenever any input is shorted to ground. No damage will occur when an overvoltage (+15 V dc maximum for all inputs of 60 mV or less and +40 V dc for all other channels) is applied indefinitely. During these conditions, the PCMU operation is not degraded. Due to isolation, the failure of any signal conditioner has no effect on the operation of any other signal conditioner or channel.

### 35.3.1.8 MCM

The MCM has been designed and fabricated to control MADS equipment.

#### A. MCM description

The MCM is basically a hardwired logic controller consisting of relays, semiconductor logic, and a sample mode timer. The system is controlled by switches on panels A6L and C3 or ground uplink commands. These switches provide power to the MCM and crew control of all functions except playback reverse. The ground will be prime for MADS operations with the exception of PCM mode (sample/continuous) which is a crew-only function.

#### B. MCM command and control

Eleven uplink commands are available to operate the MADS. Nine commands control the MCM and two separate commands control Frequency Data Multiplexer

(FDM) auto calibration. All eleven commands are listed in Table 35-9, along with additional information. Explanations of the nine MCM commands are as follows:

**Table 35-9. MADS uplink commands**

| DSM  | MSID      | OPS nomenclature        | MDM | Reset    | Set      |
|------|-----------|-------------------------|-----|----------|----------|
| 4600 | V78K9658U | MADS OFF/STBY           | PF1 | E1093C00 | E9090000 |
| 4601 | V78K9621U | MADS WB/ACIP ON         | PF1 | E1090000 | E9092000 |
| 4602 | V78K9661U | MADS WB/ACIP OFF        | PF1 | E1092000 | E9090000 |
| 4603 | V78K9622U | MADS PCM ON             | PF1 | E1090000 | E9091000 |
| 4604 | V78K9662U | MADS PCM OFF            | PF1 | E1091000 | E9090000 |
| 4605 | V78K9623U | MADS RCDR REWIND BOT    | PF1 | E1093C00 | E9090800 |
| 4606 | V78K9624U | MADS RCDR REWIND EOT    | PF1 | E1093C00 | E9090400 |
| 4607 | V78K9091U | MADS AUTO FDM CAL - ON  | PF1 | 70890000 | 78890200 |
| 4608 | V78K9100U | MADS AUTO FDM CAL - OFF | PF1 | 70890200 | 78890000 |
| 4609 | V78K9626U | MADS TRACK SEQ 3 ON     | PF1 | 70890000 | 78890100 |
| 4610 | V78K9666U | MADS TRACK SEQ 3 OFF    | PF1 | 70890100 | 78890000 |

- WB/ACIP ON and WB/ACIP OFF

These commands enter through the WB/ACIP PCM switch on A6L when it is in the CMD position. If RECORDER POWER switch is in PCM/WB ENABLE, sending WB/ACIP ON will send power to recorder. It is called WB/ACIP because in OV-099 the WB bus (bus 2) also powered the ACIP PCMs. PF1 Card 14 Channel 2 Bit 3 will be the actual switch to turn on and off Wide Band Strain Gages.

- PCM ON and PCM OFF

These commands enter through the PCM switch on A6L when it is in the CMD position, turning on and off the MADS PCMs. See Table 35-9 to see how else this will affect system status. PF1 Card 14 Channel 2 Bit 4 will be the actual switch to turn on and off Wide Band Strain Gages.

- RECORDER REWIND BOT

This commands the MCM directly through the hardwired logic to go to BOT at 60 ips. It also sends the equivalent of WB/ACIP OFF, PCM OFF and disables RCDR REWIND EOT. PF1 Card 14 Channel 2 Bit 6 will be the actual switch to turn on and off Wide Band Strain Gages.

- RECORDER REWIND EOT

This commands through the RCDR PB FWD switch when it is in the CMD position. It causes the recorder to go to EOT at 15 ips. It also sends the equivalent of WB/ACIP OFF, PCM OFF and disables RCDR REWIND BOT. PF1 Card 14 Channel 2 Bit 5 will be the actual switch to turn on and off Wide Band Strain Gages.

- RECORDER TRACK SEQ 3 ON

Selects the third set of tracks and puts recorder into forward direction.

- RECORDER TRACK SEQ 3 OFF

Returns recorder to track sequence 1 at the same percent tape and the same direction.

- MADS OFF/STBY

Sends the equivalent of WB/ACIP OFF, PCM OFF, and disables RCDR REWIND BOT and RCDR REWIND EOT. This will turn off recorder only if the RECORDER POWER switch is set to PCM/WB ENA.

**CAUTION**

Uplink of DSM 4600 MADS OFF/STBY while the recorder power switch is in WB/PCM ENA may cause loss of the MADS recorder. STS-53 postflight investigation revealed an inadvertent MADS OFF/STBY command contributed to the unrecoverable loss of tape tension.

Note: The switches must be configured to their command or enable position to allow uplink control.

Note: The crew has the capability to take manual control of the system operation by switch actions (Figure 35-4 and Figure 35-5).

The current MADS OFF/STBY command reset/set bits are as follows: (Card 14 channel 2)

|                          |                            |                            |
|--------------------------|----------------------------|----------------------------|
| MADS OFF/STBY            | E109 3C00                  | E909 0000                  |
| Bits 1 - 8 of the        | <b>1234 5678</b> 9012 3456 | <b>1234 5678</b> 9012 3456 |
| 2nd Hex Words --> Binary | <b>0011 1100</b> 0000 0000 | <b>0000 0000</b> 0000 0000 |

**Bit 3** Turns Wide Band On and Off

**Bit 4** Turns PCM On and Off

**Bit 5** Fast Forward to EOT On and Off

**Bit 6** Rewind to BOT On and Off

Bit 2 Turns MADS Recorder On and Off (notice that MADS OFF/STBY doesn't affect the power to the MADS Recorder)

C. MCM recorder control

The MCM has the capability to select three recorder speeds (3-3/4 ips, 15 ips, 60 ips), enable the record function, select tape direction, and enable tracks for recording. The MCM can select one of three track groups for recording:

- TRACK SEQ number 1 selects the forward direction for tape motion and enables seven tracks for recording. Up to seven additional tracks are normally selected for record during SEQ number 1. These tracks are not part of this SEQ but are controlled by the Master Events Controller (MEC) for External Task (ET) and Solid Rocket Booster (SRB) data.
- TRACK SEQ number 2 only is automatically selected by the End of Tape (EOT) signal from the recorder as long as the track SEQ number 3 command is not present. This sequence selects the reverse tape direction and enables a second set of seven tracks. When the recorder reaches Beginning-of-Tape (BOT) in this mode it will stop.
- TRACK SEQ number 3 is initiated by uplink command only. This sequence selects the forward tape direction and enables a third set of seven tracks for recording.

D. FDM and PCM control

The MCM controls power to the MADS wideband equipment and PCM equipment (SGSC and PCMU). The PCMU format/data rate is selected with the recorder tape speed; that is, 64 kbps with a 15-in/s recorder speed and 32 kbps with the 3-3/4-in/s speed.

E. ET and SRB

The ET and SRB MADS equipment is controlled by MEC number 2 when the MCM has module power applied. The MEC will command the ET MADS equipment off and deselect the recorder tracks used for ET data just prior to ET separation. It should be noted that this signal from the MEC is the only control over the track selection for these data. If for some reason the recorder should reach EOT for track pass number 1, before the MEC commanded the equipment off, it will automatically switch to pass number 2 (which records in the reverse direction). However, the tracks selected for ET data which are not switchable would remain energized and the data would be destroyed.

This feature was originally intended to allow heavily instrumented ETs ("heavyweight" ETs) and SRBs to deposit seven tracks of data on the recorder. The heavyweight ETs were used up, however; and current ETs and SRBs have less instrumentation on them.

OV-103 can record four tracks - one wideband track for each SRB, a wideband track, and a PCM track for the ET. The orbiter interfaces for both ET and SRB are still in place but are presently not being used (no data). See Table 35-9 for typical track assignments.

OV-104 and OV-105 MADS record no ET or SRB data. See 35-9 for typical track assignments. The orbiter interfaces for the ET and SRB do not exist. The inputs are just reserved only.

F. MCM operating modes

1. Wideband mode

In this mode, the recorder is commanded to record at 15 ips, the wideband equipment is powered up, the PCM and SGSC will remain on if previously on, and the PCMU 64-kbps format is selected. This mode will inhibit the 60 ips speed select.

2. PCM mode

In this mode, the MCM commands the recorder to record at 3<sub>3</sub>/<sub>4</sub> ips, powers the PCM equipment, and, if the strain gauge switch is in the PCM ENA position, provides power to the SGSC. This mode will inhibit the 60 ips speed select.

3. Playback forward mode

This mode commands the recorder to speed 15 ips and the tape direction to forward. This mode inhibits the playback reverse command. Caution must be exercised when using this mode. If playback forward (REWIND EOT) is commanded while the recorder is on track sequence number 2, the recorder will reset to sequence number 1. To reestablish sequence number 2, the recorder must reach EOT and then be rewound to the desired percent tape.

4. Playback reverse mode

This mode commands the recorder to run at 60 in/s in the reverse direction.

**Table 35-10. Typical track assignments**

[Note: 1/A = FDM1/FMMA]

| OV-103 <sup>a</sup> |          |          |          | OV-104 AND OV-105 <sup>b</sup> |          |          |          |
|---------------------|----------|----------|----------|--------------------------------|----------|----------|----------|
| Track number        | Pass     |          |          | Track number                   | Pass     |          |          |
|                     | 1        | 2        | 3        |                                | 1        | 2        | 3        |
| 1                   | ET-PCM   |          |          | 1                              | ET-PCM   |          |          |
| 2                   |          | 2/A      |          | 2                              |          | 2/A      |          |
| 3                   | ET-WB    |          |          | 3                              | ET-WB    |          |          |
| 4                   |          | 2/B      |          | 4                              |          | 2/B      |          |
| 5                   | 1/D      |          |          | 5                              | 1/D      |          |          |
| 6                   |          | 2/C      |          | 6                              |          | 2/C      |          |
| 7                   |          | MADS PCM |          | 7                              | 1/C      |          |          |
| 8                   |          | 2/D      |          | 8                              |          | 2/D      |          |
| 9                   | 1/B      |          |          | 9                              | 1/B      |          |          |
| 10                  |          | 1/A      |          | 10                             |          | 1/A      |          |
| 11                  | SRB L-WB |          |          | 11                             | SRB L-WB |          |          |
| 12                  |          | 1/C      |          | 12                             |          | SPARE    |          |
| 13                  | SRB R-WB |          |          | 13                             | SRB R-WB |          |          |
| 14                  | SPARE    |          |          | 14                             |          | MADS PCM |          |
| 15                  | 2/A      |          |          | 15                             | 2/A      |          |          |
| 16                  |          |          | 2/A      | 16                             |          |          | 2/A      |
| 17                  | 2/B      |          |          | 17                             | 2/B      |          |          |
| 18                  |          |          | 2/B      | 18                             |          |          | 2/B      |
| 19                  | 2/C      |          |          | 19                             | 2/C      |          |          |
| 20                  |          |          | 2/C      | 20                             |          |          | 2/C      |
| 21                  | 2/D      |          |          | 21                             | 2/D      |          |          |
| 22                  |          |          | 2/D      | 22                             |          |          | 2/D      |
| 23                  | 1/A      |          |          | 23                             | 1/A      |          |          |
| 24                  |          |          | 1/A      | 24                             |          |          | 1/A      |
| 25                  | 1/C      |          |          | 25                             | SPARE    |          |          |
| 26                  | MADS PCM |          | 1/C      | 26                             |          |          | SPARE    |
| 27                  |          |          | MADS PCM | 27                             | MADS PCM |          |          |
| 28                  |          |          |          | 28                             |          |          | MADS PCM |

<sup>a</sup> The orbiter interfaces for both ET and SRB are still in place but are presently not being used.

<sup>b</sup> The orbiter interfaces for the ET and SRB do not exist. The inputs are reserved only.

### 5. Sample mode

In the PCM mode, the recorder and equipment may be operated in either a continuous or a sample mode. In the sample mode, the PCM will power on the equipment (including the recorder), wait 10 seconds, record 10 seconds, then wait 10 seconds to power off the equipment. This sequence is repeated after a 10-minute powered-off period.

The MADS control module timer (for PCM sample mode) is not reinitialized by mode changes. Timer will cycle whenever the MCM is powered.

Note: The wideband mode will override the sample mode and command continuous record at 15 in/s.



6. Standby/off mode

In this mode, the MCM is in standby and all other MADS equipment is powered off.

**35.3.1.9 Other Interfaces**

- Main engine Flight Accelerometer Safety Cutoff System (FASCOS)

The MADS interfaces with the FASCOS experiment. The 64 kbps of PCM data from MADS and FASCOS is recorded on the MADS recorder during ascent and entry. The FASCOS, located on shelf 7, directly above the MADS shelf 8, feeds 12 vibration measurements into FDM 1 mux 3 and 4. See Figure 35-6. FASCOS has a temperature sensor on its heat sink.

- POGO

OV-104 has one non-MADS WBSC mounted on shelf 8. This WBSC is used to record POGO. Nine measurements are taken out of the main engines, conditioned, and fed into FDM FMM1.

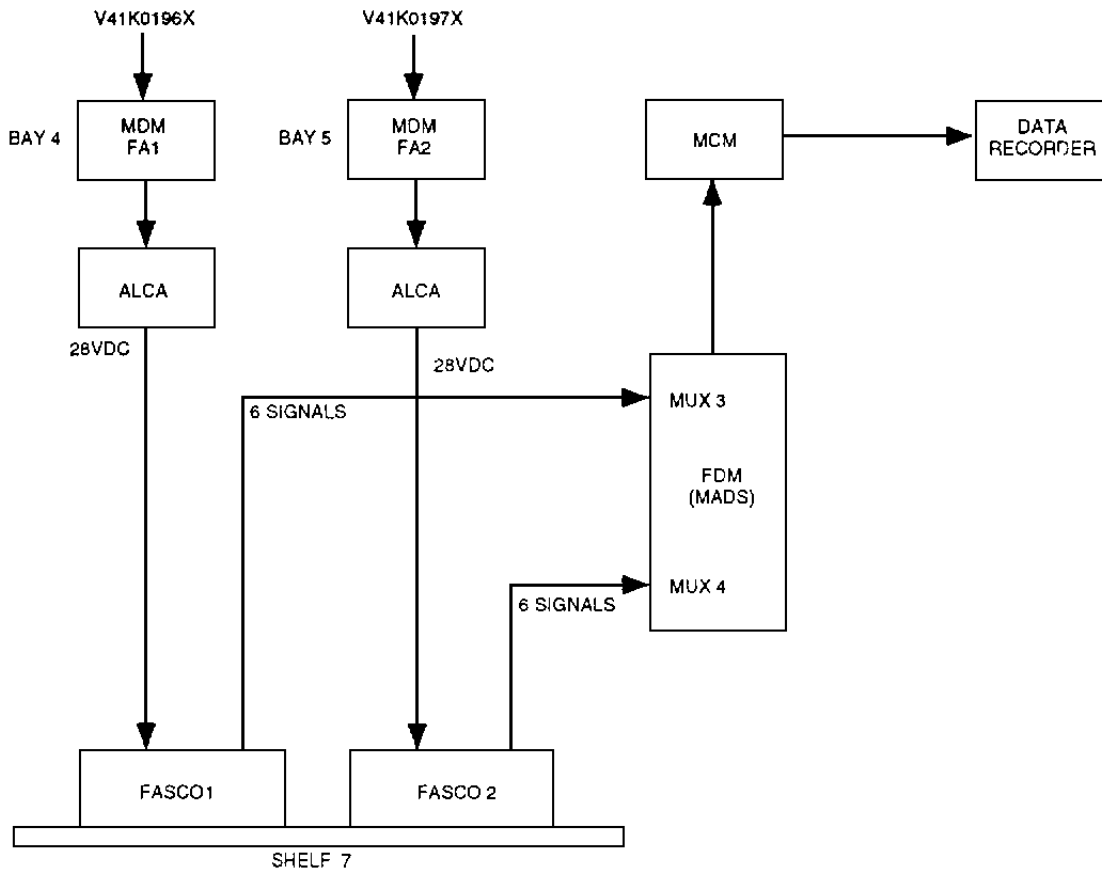


Figure 35-6. FASCOS

### 35.3.2 Mechanical

#### 35.3.2.1 Weight

See table below for weights of components.

| Component     | Weight      |
|---------------|-------------|
| FDM           | 17 lb       |
| PCM           | 28 lb       |
| MADS recorder | 58 lb       |
| MCM           | 10 lb       |
| WBSC          | 0.5 lb each |
| SGSC          | 1 lb each   |

#### 35.3.3 Software

There is no software in the MADS, except for what you see in the FDM section above. The MCM is just a relay box.

### 35.3.4 Location

OV-103/104 - Volume D of crew compartment under middeck floor, directly aft of the lockers.

OV-105 - Volume G of the ECLSS bay.

OV-103/104: MCM and MADS recorder. See Figure 35-7.

OV-105: MCM and MADS recorder. See Figure 35-8.

#### Shelf 8

OV-103 2 FDM, 1 PCM, 3 SGSC chassis, 3 WBSC chassis, 1 PDA

OV-104 2 FDM, 1 PCM, 1 SGSC chassis, 1 WBSC chassis, 1 PDA

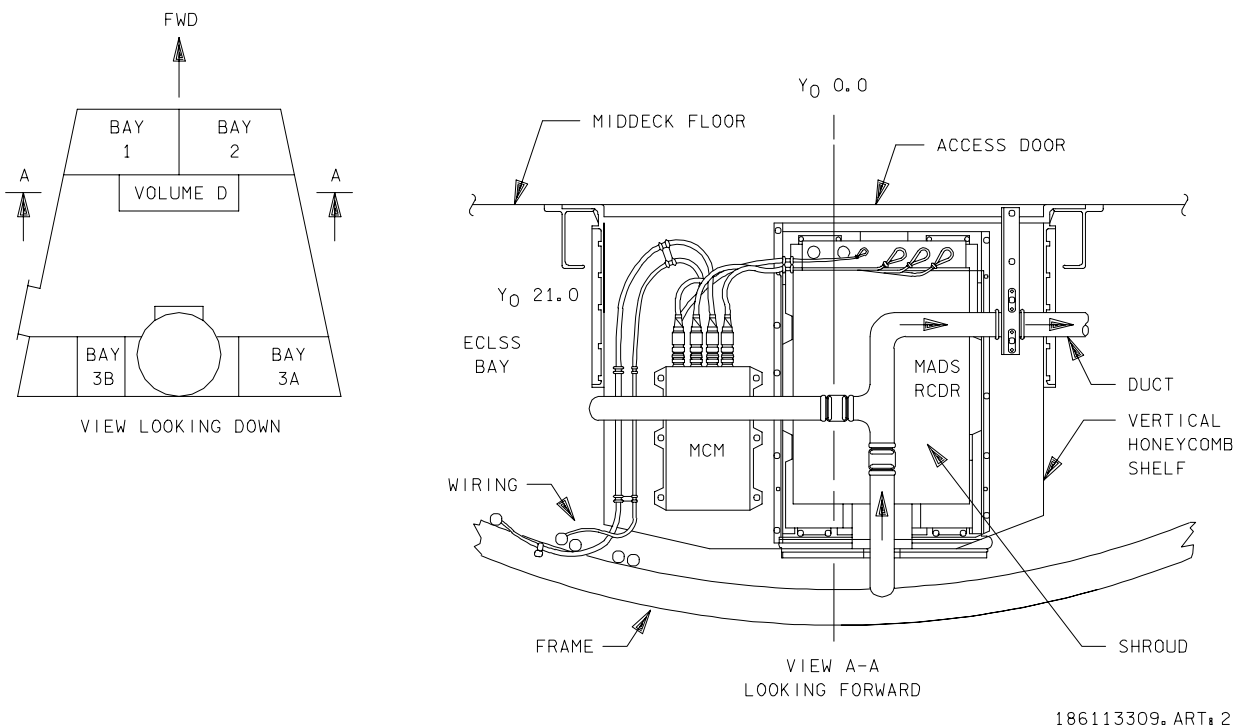
OV-105 2 FDM, 1 PCM, 2 SGSC chassis, 1 WBSC chassis, 1 PDA

See Figure 35-9 for a picture of shelf 8.

- Payload bay floor

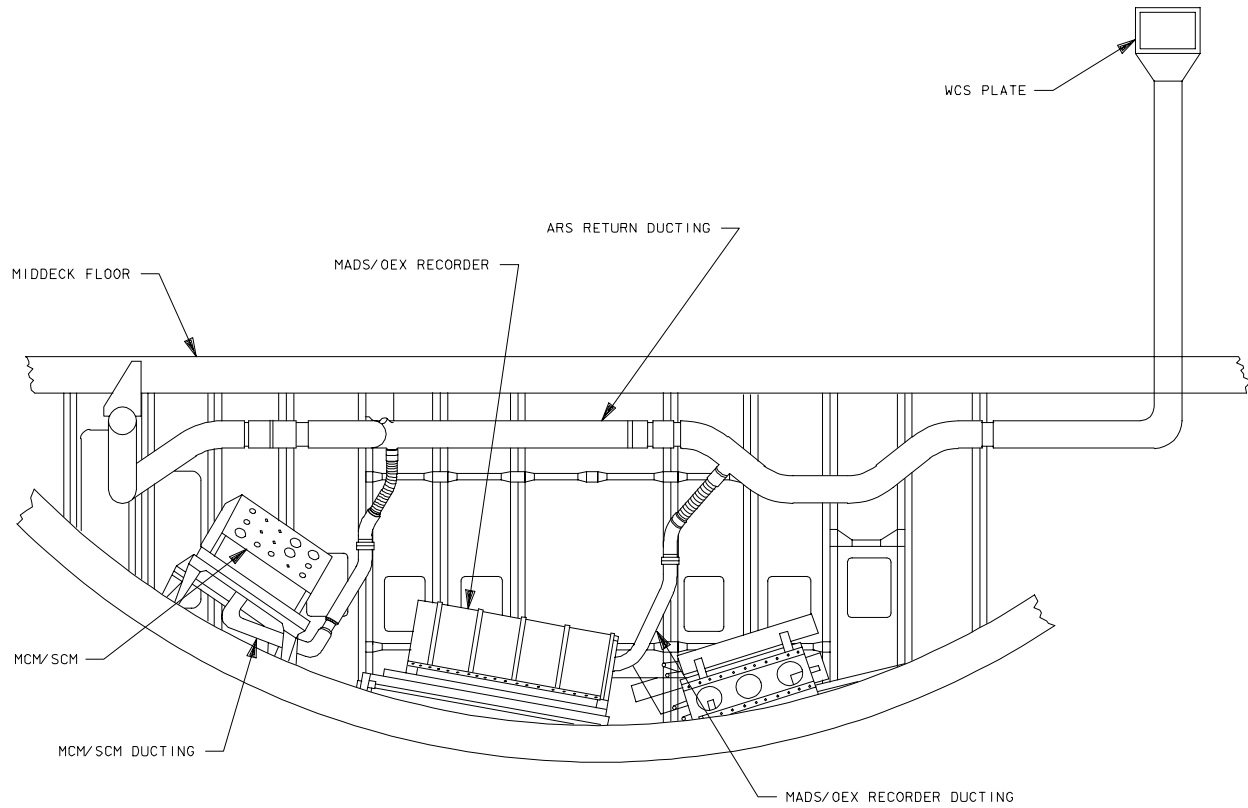
OV-103 has a third WBSC chassis bolted to the payload bay floor directly below shelf 8.

- The Orbiter Vehicles use only shelf 8 for MADS. SGSC use for OI tire pressure is installed below shelf 8 on shelf 6.



186113309. ART. 2

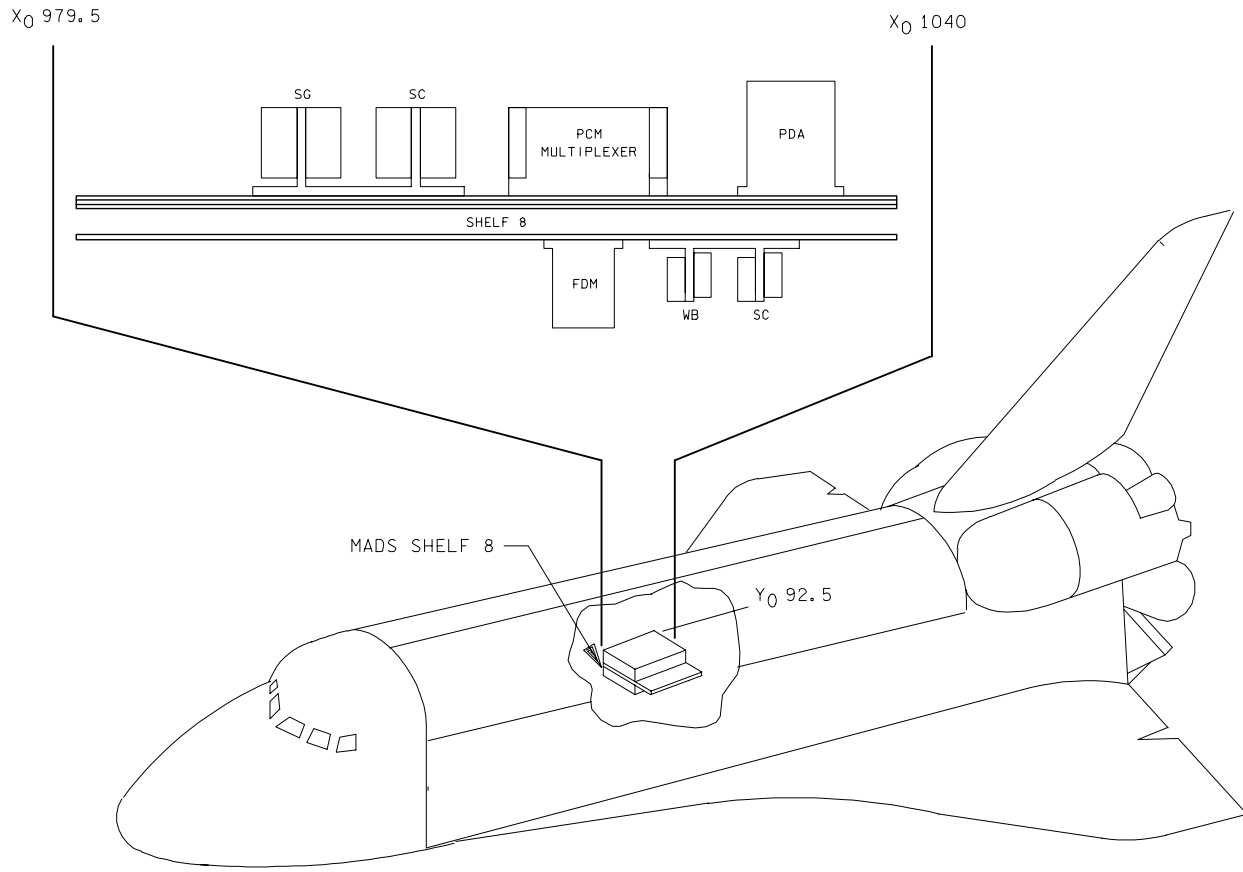
**Figure 35-7. MCM and recorder location (OV-103/104)**



LOOKING AFT LOWER EQUIPMENT BAY

186113315. ART, 1

**Figure 35-8. MCM and recorder location (OV-105)**



1055. ART 2

**Figure 35-9. MADS shelf 8 location**

### 35.3.5 Temperature Control

MCM and MADS recorder: cabin air is drawn through them.

Shelf 8: passive cooling (in the payload bay). They are under the payload bay liner, but still affected by direct sunlight or shadow. The equipment mounted on shelf 8 generally cools off during a mission. To increase the MADS equipment temperature, turn on the SGSCs. These generate a lot of heat and warm up all the equipment. The only way to cool the equipment mounted on shelf 8 is to turn off the equipment and, if necessary, orient the orbiter to put the payload bay in shadow.

## 35.4 DESCRIPTION OF OPERATION

### 35.4.1 Crew Control

PCM mode (sample/continuous) is selectable by panel switch on A6L panel.

Panel A6L switches, shown on Table 35-11, are interconnected. Refer to Table 35-9 to see what has to be thrown to have what effect.

### 35.4.2 Ground Commands

Refer to Table 35-9, MADS Uplink Commands.

**Table 35-11. PNL A6L switch effects**

Switch position

| WB/ACIP<br>PCM | PCM | Internal<br>timer                 | MADS<br>BUS1<br>(PCMs) | MADS<br>BUS2<br>(SGSC)                                   | MADS<br>BUS3<br>(WB/AIP<br>FDMs) | RCDR<br>SPEED<br>(when<br>recording) | RCDR<br>POWERED<br>(PCM/WB)      |
|----------------|-----|-----------------------------------|------------------------|--|----------------------------------|--------------------------------------|----------------------------------|
| OFF            | OFF | OFF                               | OFF                    | SGSC will be on <u>only</u> if STRAIN GAUGE is set to ON | OFF                              | 0                                    | On only when RCDR POWER SW is ON |
| OFF            | ON  | ON if PCM RCD MODE is in "sample" | ON                     | ON   | OFF                              | 3-3/4 ips                            | ON                               |
| ON             | OFF | OFF                               | OFF                    | SGSC will be on <u>only</u> if STRAIN GAUGE is set to ON | ON                               | 15 ips                               | ON                               |
| ON             | ON  | OFF                               | ON                     | ON   | ON                               | 15 ips                               | ON                               |

Note: OFF: When switch is in OFF position or in cmd (or enable) with no command present.

ON: When switch is in ON position or in cmd (or enable) with command present.

### 35.4.3 Telemetry

MADS telemetry is the same for all vehicles. See Table 35-12.

Two bits are provided for track sequence status in the OI downlink. One bit is an indication of either Sequence 2 or Master MADS OFF. Two ways to cancel the SEQ 2 command are to command REW EOT or SEQ 3 ON. This parameter V78X9612E is high FWD (1) during sequences 1 and 3. The parameter V78X9613E indicates that track sequence 3 has been commanded. This parameter is high for track sequence 3 indicating that relay K5 is energized.

Shelf 8 temperature is available in OI for monitoring, V78T9607A next to the FDM on the lower part of shelf 8 downlinked at 1 s/s. Sensor ranges are from -75° to +175° F. Restricted duty cycles will be required for payload bay mounted equipment. The minimum and maximum operating temperatures of the MADS components are given in Table 35-13.

Note that when the FDM is on and in the DATA mode, DATA MODE shows DATA. When the FDM is off or calibrating, however, it reads as CAL.

*Table 35-12. MADS measurements transmitted via operational instrumentation downlink*

| Status  | Measurement no. | MDM | DSC |
|---|-----------------|-----|-----|
| FDM 1 MUX 1 BITE  | V78X9380E       | OA3 | --  |
| FDM 1 MUX 2 BITE  | V78X9381E       | OA3 | --  |
| FDM 1 MUX 3 BITE  | V78X9382E       | OA3 | --  |
| FDM 1 MUX 4 BITE  | V78X9383E       | OA3 | --  |
| FDM 2 MUX 1 BITE  | V78X9390E       | OA3 | --  |
| FDM 2 MUX 2 BITE  | V78X9391E       | OA3 | --  |
| FDM 2 MUX 3 BITE  | V78X9392E       | OA3 | --  |
| FDM 2 MUX 4 BITE  | V78X9393E       | OA3 | --  |
| Recorder - percent tape used                                    | V78Q9602A       | OF1 | OF1 |
| Recorder - BITE   | V78X9603E       | OF1 | --  |
| Recorder - recording  | V78X9604E       | OF1 | --  |
| Recorder - tape motion on                                       | V78X9605E       | OF1 | OF1 |
| PCM 1 MUX BITE  | V78X9611E       | OA3 | --  |
| Track seq. pass 1, 2, 3 status                                  | V78X9612E       | OF1 | --  |
| Track seq. pass 3 status  | V78X9613E       | OF1 | --  |
| Shelf temp (associated with WB equipment,<br>bottom of shelf 8) | V78T9607A       | OA2 | OM2 |
| FDM 1 data mode   | V78X9309E       | OA3 | OA3 |
| FDM 2 data mode   | V78X9310E       | OA3 | OA3 |

Displays that show MADS data are

- INCO MGMT Button

#### **35.4.4 Operational Instructions**

MADS configurations and Detailed Test Objectives (DTOs) change from flight to flight and vehicle to vehicle. Therefore, operational instructions must be treated on a mission-by-mission basis.



Generally, the MADS has everything on during launch and entry, just PCMs in sample mode during orbit (or PCMs and SGSCs in sample during orbit), and PCMs only in sample mode after landing to test thermal contraction of the orbiter structure (called “thermal soakback,” this will be flight-specific).

Temperature operational limits on MADS components are listed in Table 35-13 below.

**Table 35-13. MADS component operating temperature limits**

| Component     | Minimum temp. (°F) | Maximum temp. (°F) |
|---------------|--------------------|--------------------|
| MCM           | 0                  | 125                |
| Data recorder | 35                 | 120                |
| FDM 1         | 30                 | 140                |
| SCM           | 35                 | 120                |
| PCM           | -45                | 140                |
| WBSC 1        | 20                 | 140                |
| SGSC          | 20                 | 140                |

Notes: The MADS shelf 8 temperature measurements are V789T9706A - associated with the PCM equipment and V78T9607A - associated with the WB equipment. For installation details, see document MO72-704007. Shelf 7 is V78T9608A, with FASCOS.

The MCM and SCM temperatures are not downlinked and so cannot be monitored.

### 35.5 SUMMARY DATA

The way the MADS data-gathering equipment works is the same in all orbiters. Figure 35-10 provides a generalized overview.

#### A. The MCM

MCM: Three preset unchangeable, combinable, data-gathering options (PCM, WB with SGSC, WB without SGSC) controlled by simple RTC commands. Low weight (15 lb) and power requirements (25 W).

**Table 35-14. Recorder data rates**

| Tape speed | Analog (freq range) | Digital (biphase L) |
|------------|---------------------|---------------------|
| 1-7/8      | 0.4 Hz to 31.25 kHz | 1 to 16 Kbps        |
| 3-3/4      | .4 Hz to 125.00 kHz | 2 to 32 Kbps        |
| 7-1/2      | .4 Hz to 250.00 kHz | 4 to 64 Kbps        |
| 15         | .4 Hz to 500.00 kHz | 8 to 128 Kbps       |
| 30         | .4 Hz to 625.00 kHz | 16 to 256 Kbps      |
| 60         | .4 Hz to 1.00 MHz   | 32 to 512 Kbps      |

#### B. Power

MNA MPC-1 for WBSC, SGSC, FDM, and AUTOCAL command (through FLC1).  
MNB for PCM (MPC-2) and recorder (FPC-2).

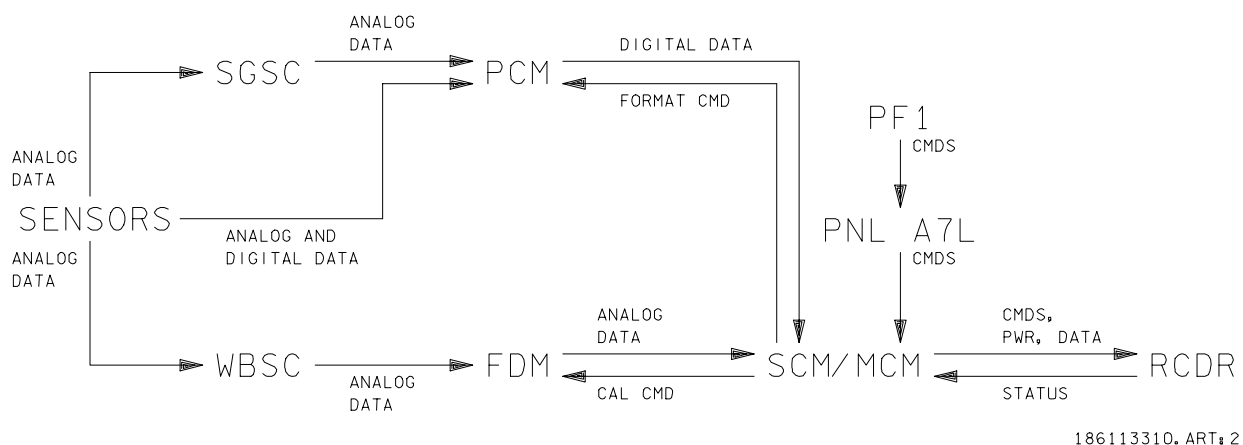
C. Cooling

Cabin air is pulled through MCM and recorder. Shelves 8 are cooled passively (out in the payload bay).

D. Location

1. OV-105: MCM and MADS recorder in volume G of ECLSS bay.
2. OV-103 and OV-104: MCM and MADS recorder in volume D of ECLSS bay below the middeck floor.

All vehicles - Everything else amidship in the payload bay on shelves 8.



186113310. ART: 2

**Figure 35-10. Generic MADS overview**

**35.6 OPERATIONAL NOTES**

- The MADS control module timer (for PCM sample mode) is not reinitialized by mode changes. Timer will cycle whenever the MCM is powered.
- At PCMU powerup, the PCMU bite will toggle while the BITE circuit is initialized. At recorder powerup, the recorder may indicate tape motion until motion circuit is fully powered.
- The REWIND EOT (or BOT) commands do not control power to the recorder. To rewind or fastforward the recorder, power must be supplied via PNL A6L RCDR power - ON.
- Note that when the FDM is on and in the DATA mode, DATA MODE shows DATA. When the FDM is off or calibrating it reads as CAL.
- If Shelf 8 temperature goes below 30° F during MADS operation, turn on the SGSC as follows to generate some heat and warm up the area. Have the crew perform the following two switch throws to warm up the Shelf 8:

(1) C3 MASTER MADS POWER - ON

(2) A6L MADS STRAIN GAGE - ON

After MADS is warmed up to ~ 34° F, the crew will need to perform the following step in De-Orbit Prep Final ENT SWITCH LIST/VER:

(1) A6L MADS STRAIN GAGE - PCM ENA.

This will allow commanding to MADS PCM

This action will turn on the half strain gage LRU which will warm up Shelf 8 ~ 5° F per hour if in an Inertial Tail toward the sun attitude. However, do not do this right before entry. You want it a little cold (less than 100° F) then so it will not overheat during entry.

During STS-112, the MADS Operator was instructed to rewind to Beginning of Tape. While rewinding, the MADS BOT Light Sensor failed to slow down and stop the rewind wheel in time, causing the tape to physically come off the reel, rendering MADS recording during entry useless. **Lessons Learned**, after ascent rewind MADS Recorder to BOT to approximately 6%.

### 35.7 REFERENCES

- A. Schematic diagram - Integrated System Schematic, MADS Instrumentation, Part 1 and 2. Drawing number VS72-978099. Rockwell International.
- B. Schematic diagram - DFI/MADS Instrumentation Integrated System Schematic. Drawing number VS72-978102. Rockwell International.
- C. Wideband Signal Conditioner Requirements (MC476-0132).
- D. Strain Gauge Signal Conditioner Requirements (MC476-0134).
- E. MADS Equipment Power Distribution (V408-780409).
- F. MADS Power Distribution Assembly (V408-780709).

**SECTION 38 - ORBITER INTERFACE UNIT**  
**CONTENTS**

| <b>Section</b> | <b>Page</b>   |
|----------------|---|
| 38.1           | SYSTEM OVERVIEW ..... 38-1                                      |
| 38.2           | INTERFACE AND INSTALLATION CONFIGURATION ..... 38-1             |
| 38.2.1         | Interfaces ..... 38-1   |
| 38.2.2         | Orbiter Installation ..... 38-2                                 |
| 38.3           | INTERNATIONAL SPACE STATION MDM TERMINOLOGY ..... 38-4          |
| 38.3.1         | Logical Devices ..... 38-5                                      |
| 38.3.2         | Physical Devices ..... 38-5                                     |
| 38.4           | MS1553B INFORMATION ..... 38-5                                  |
| 38.4.1         | Overview ..... 38-5   |
| 38.4.2         | MS1553B Bus Operation Description ..... 38-6                    |
| 38.4.3         | OIU MS1553B Bus Traffic ..... 38-8                              |
| 38.4.4         | Bus Configurations ..... 38-10                                  |
| 38.5           | OIU OPERATIONS ..... 38-11                                      |
| 38.5.1         | Command Processing Overview ..... 38-11                         |
| 38.5.2         | OIU Command Processing ..... 38-11                              |
| 38.5.3         | Command Counter ..... 38-12                                     |
| 38.5.4         | Configuration Commands (Routing Code → 00h) ..... 38-16         |
| 38.5.5         | Command Description ..... 38-18                                 |
| 38.6           | TELEMETRY PROCESSING ..... 38-21                                |
| 38.6.2         | OIU to PDI Telemetry Stream ..... 38-22                         |
| 38.6.3         | BC and RT BIAs Contributions to PDI Telemetry Build ..... 38-23 |
| 38.6.4         | OIU to PDI Telemetry Data Interruptions ..... 38-24             |
| 38.6.5         | BIA Interruptions ..... 38-25                                   |
| 38.6.6         | Data Conversions ..... 38-25                                    |
| 38.6.7         | Temperature Telemetry ..... 38-26                               |
| 38.6.8         | Health and Status Telemetry ..... 38-26                         |
| 38.7           | POWER-ON SELF-TEST AND APPLICATION INTIALIZATION ..... 38-34    |
| 38.7.1         | Power-On Self-Test ..... 38-34                                  |
| 38.7.2         | Application Initialization ..... 38-35                          |
| 38.7.3         | Time Processing ..... 38-37                                     |
| 38.7.4         | Talkback Indicator ..... 38-39                                  |
| 38.8           | ERROR LOG ..... 38-39   |
| 38.8.1         | Error Log Structure ..... 38-39                                 |
| 38.8.2         | Error Log Dump via PDI Output ..... 38-40                       |
| 38.8.3         | Error Signatures ..... 38-42                                    |
| 38.8.4         | Nonconsecutive Frame Indicator ..... 38-44                      |
| 38.9           | ACRONYMS ..... 38-44  |
| 38.10          | REFERENCES ..... 38-46  |
| 38.11          | APPENDIX ..... 38-46  |

## TABLES

| Table |  | Page  |
|-------|--|-------|
| 38-1  | Connectors.....                                | 38-4  |
| 38-2  | OIU Routing Code destinations.....             | 38-14 |
| 38-3  | Logical/Physical Device.....                   | 38-21 |
| 38-4  | OIU Serial Number Telemetry.....               | 38-27 |
| 38-5  | Block Status Word values.....                  | 38-31 |
| 38-6  | BSW representing "good" 1553 transactions..... | 38-33 |
| 38-7  | Valid time / field values.....                 | 38-38 |
| 38-8  | OIU error log EEPROM memory locations.....     | 38-40 |
| 38-9  | OCC error log data format.....                 | 38-42 |
| 38-10 | Flight/prototype pin assignments.....          | 38-46 |
| 38-11 | OIU error telemetry matrix.....                | 38-48 |

## FIGURES

### Figures

|      |   |       |
|------|---|-------|
| 38-1 | OIU Interfaces.....                     | 38-2  |
| 38-2 | OIU flight prototype unit.....          | 38-3  |
| 38-3 | ISS/OIU BUS & MDM Configuration.....    | 38-4  |
| 38-4 | MS1553B data formatting.....            | 38-6  |
| 38-5 | Example of 100-ms processing frame..... | 38-9  |
| 38-6 | OIU Bus Interface Controller (BIC)..... | 38-10 |
| 38-7 | PSP to OIU Command Word.....            | 38-13 |
| 38-8 | Configuration commands format.....      | 38-16 |
| 38-9 | OIU Telemetry Frame Description.....    | 38-23 |

## SECTION 38 ORBITER INTERFACE UNIT

### 38.1 SYSTEM OVERVIEW

The Orbiter Interface Unit (OIU) is the system that provides the communication interface between the space shuttle orbiter data system [1960's technology] and Military Standard 1553B (MS1553B) [1980's technology] communication buses. The three pertinent 1553B communication devices the Orbiter will use are the following:

- A. Space-to-Space Orbiter Radio (SSOR) to the to allow a command and telemetry interface to the International Space Station (ISS) while in proximity operations phase (rendezvous).
- B. ISS Cargo Elements located in the Space Shuttle Payload Bay, currently used with the Multi-Purpose Logistics Modules (MPLM).
- C. The International Space Station (ISS) data system ISS Command & Data Handling (C&DH).

The OIU is manifested as **Payload** and has its own Interface Control Documents (ICDs). All OIU Measurement Stimulus Identifications (MSIDs) and Commands are found in each specific Mission Integration Plan (MIP), Command and Data (C&D) Annex 4.

The OIU is a software based Line Replaceable Unit (LRU). Prior to flight, the OIU is loaded with mission specific Reconfiguration Data Tables (RDT) allowing operators (the flight crew or flight controllers) to command changes to configure the OIU to "communicate" with the three previously described 1553 components during different phases of flight.

### 38.2 INTERFACE AND INSTALLATION CONFIGURATION

#### 38.2.1 Interfaces

Payload Data Interface Panel (PDIP) connector to a Ground Support Equipment (GSE) laptop running the Ground Support Reconfiguration Application (GSRA) to support uploading of new reconfiguration data tables or flight firmware.

Standard Switch Panel (SSP) supplies **local** control to power on either OIU #1 or OIU #2. There is **no** Command to power on or off the OIU.

The Payload Timing Buffer (PTB) supplies the OIU with Inter-range Instrumentation Group B (IRIG-B) time, which is used to update the OIU internal clock.

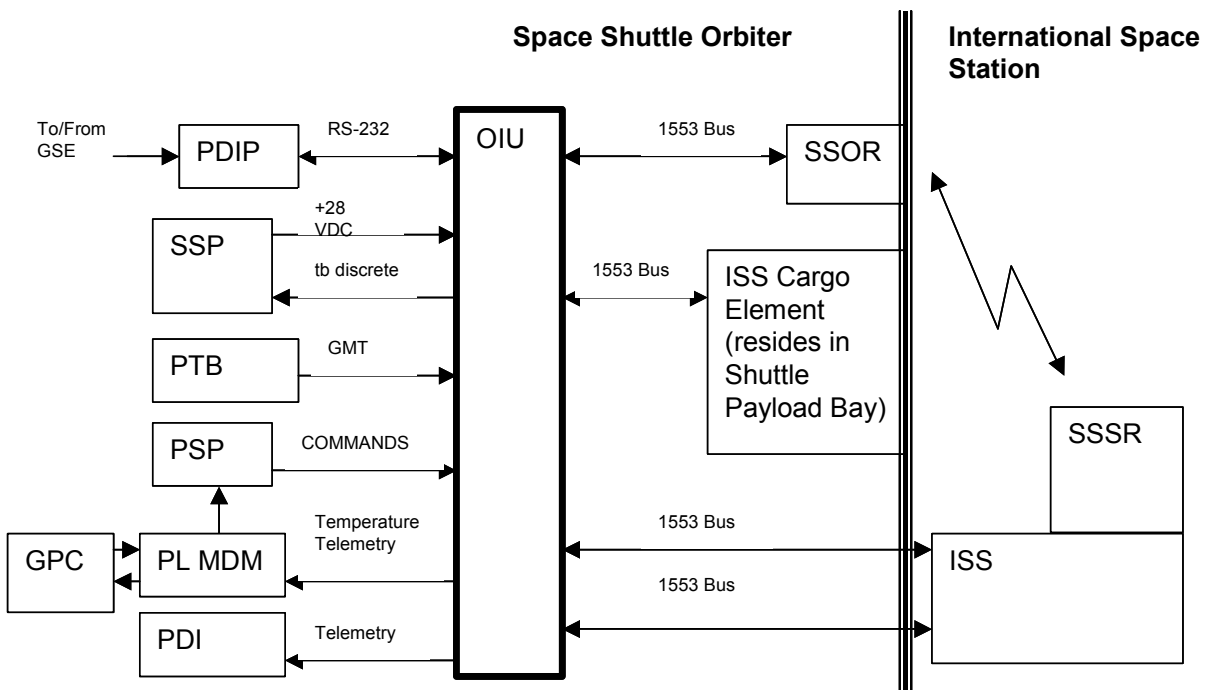
The Payload Signal Processor (PSP) properly configures the General Purpose Computer (GPC) command words to the OIU. The PSP and OIU are **non-cross-**

strapable, although an In-Flight Maintenance procedure can manually re-cable to allow PSP#1/PDI source 1 to OIU #2 and vice versa.

Payload Multiplexer DeMultiplexer (PL MDM) provides two functions:

- (a) Provides a command interface between the General Purpose Computer (GPC) and the PSP.
- (b) Receives the 4 hex word temperature telemetry from each OIU.

Payload Data Interleaver (PDI) receives OIU and, if applicable, ISS telemetry.



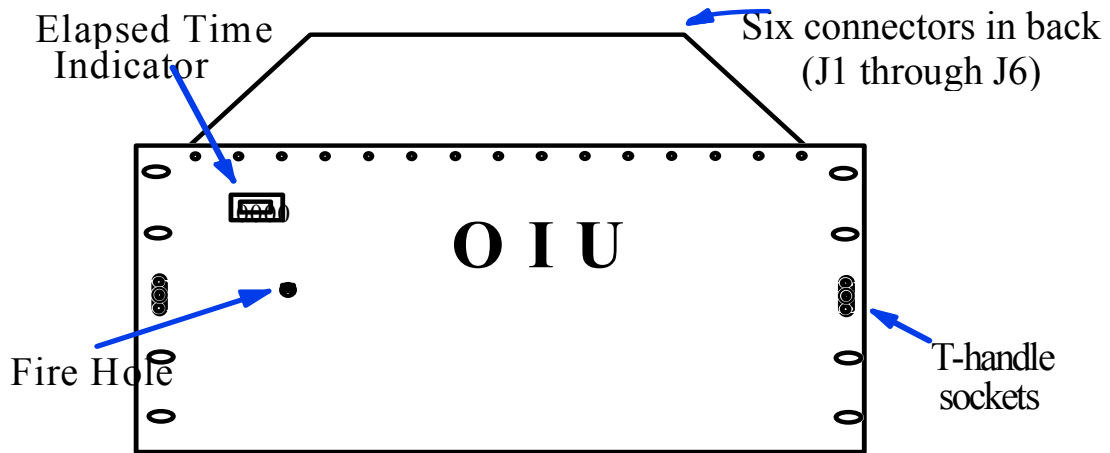
**Figure 38-1. OIU Interfaces**

Figure 38-2 depicts the OIU flight unit (front and back). The front panel of the flight/prototype unit has an Elapsed Time Indicator (ETI). This ETI represents the number of hours the OIU has been powered on.

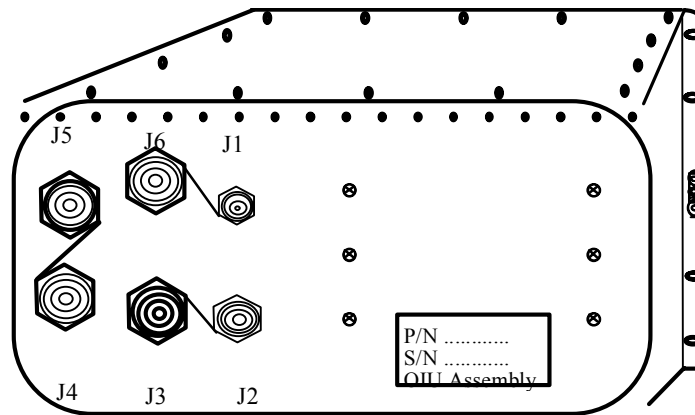
The rear panel of the flight/prototype unit has six input/output connectors, J1 to J6. The connector definitions and the pin assignments are listed in Appendix A.

### 38.2.2 Orbiter Installation

The OIU is installed in the orbiter according to specifications found in the Shuttle Orbiter/OIU Cargo Element Interfaces, ICD-A-21264. **Two** OIUs are usually mounted in panel L11.



(a) Front view



(b) Rear view

Figure 38-2. OIU flight prototype unit



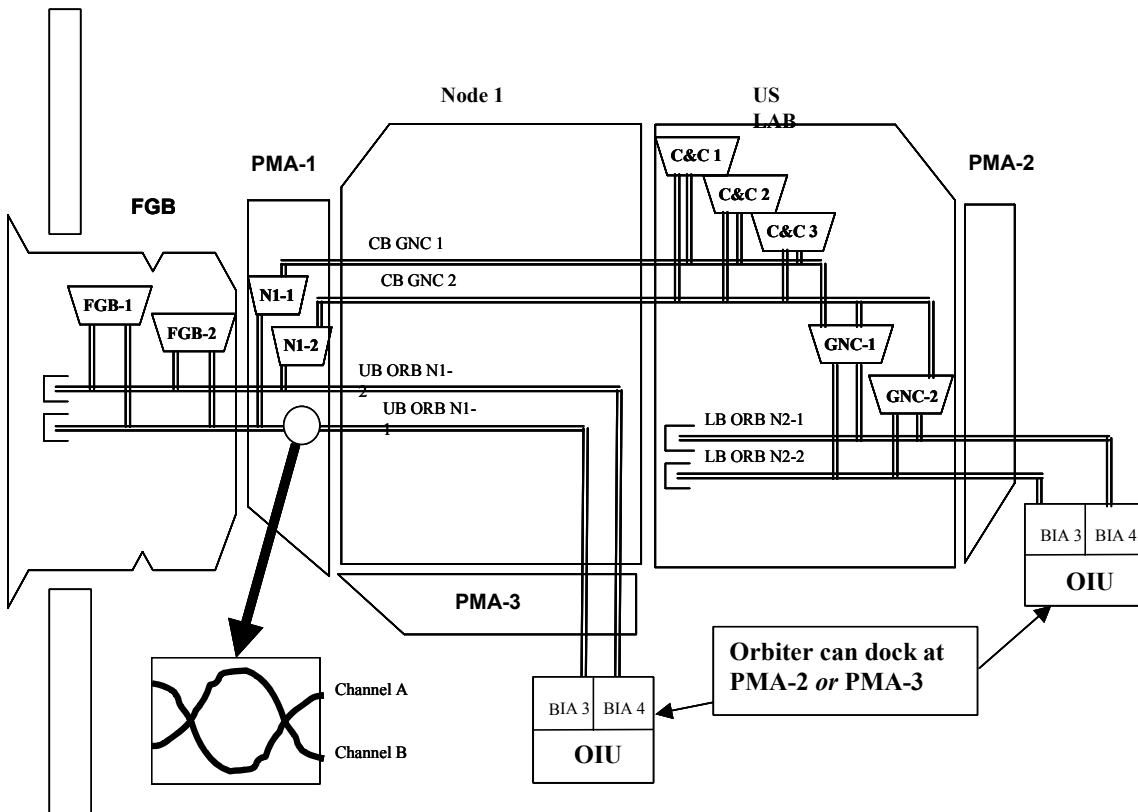
**Table 38-1. Connectors**

| Connector | Use  |
|-----------|--|
| J1        | Orbiter power (28 V) input                           |
| J2        | Orbiter standard switch panel talkback signal (28 V) |
| J3        | PDI, PSP, PTB, OIU temperature                       |
| J4        | MS1553B channel A, bus 1-4                           |
| J5        | MS1553B channel B, bus 1-4                           |
| J6        | GSE Interface  |

The OIU uses 35 Watts of Power.

### 38.3 INTERNATIONAL SPACE STATION MDM TERMINOLOGY

The OIU was designed to communicate with Line Replacement Units (LRU) and Orbiter Replacement Units (ORU) using 1553B bus architecture. Figure 38-3 provides the reader a basic communication path from either of the two OIU connections to International Space Station (ISS) data system ISS Command & Data Handling (C&DH).



**Figure 38-3. ISS/OIU BUS & MDM Configuration**

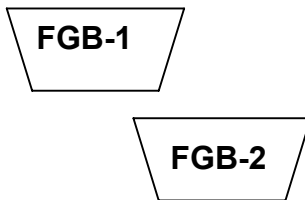
### 38.3.1 Logical Devices

A Logical Device is a type of MS1553B On-Orbit Replaceable Unit (ORU) that communicates with the OIU. The Logical Device data will determine how to extract data from the 1553B transaction and insert it into the OIU Format. The following are specific types of Logical Devices:

- A. Guidance, Navigation, and Control (GNC) MDM.
- B. Mini Pressurized Logistics Module (MPLM)
- C. Russian Functional Cargo Block (FGB) MDM
- D. Node MDM
- E. Space to Space Orbiter Radio (SSOR)

### 38.3.2 Physical Devices

The following real example is shown provide the reader what the ISS Physical Device describes. The ISS has two Functional Cargo Block (FGB) MDMs (FGB-1 and FGB-2). Each individual ISS MDM has a distinguishable Remote Terminal Address (5 bits contained within the Command and Status Words), which allows the OIU to determine which physical MDM (FGB-1 **or** FGB-2) device is mapped to the Logical Device (FGB in this example). This ensures proper communication between the BC and RT to collect telemetry and route commands to a specific ISS MDM.



Only one physical device is mapped to a logical device at one time. The OIU Configuration Commands can change the physical-to-logical device mapping and are explained in depth in Section 38.5.4.

The Reconfiguration Data Tables (RDT) specify the RT address and bus number for each physical MDM/ORU that the OIU may talk to during that flight and store mapping between the logical device and a specific physical device. The operator will send configuration commands (most of the basic flight specific commands are listed in the C&D Annex 4) to configure the OIU; these configuration commands use data listed in the RDT.

## 38.4 MS1553B INFORMATION

### 38.4.1 Overview

The MS1553B data bus provides the data flow between the OIU and ISS MDMs. The MDM contains multiple MS1553B chip sets operating as BCs, each capable of controlling up to 31 MS1553B RT ORUs. The OIU has four MS1553B chip sets (BIAs). Each BIA can be configured to operate as a BC or RT under the control of the OIU

OCC. The MS1553B data bus operates with a clock rate of 1 Mhz and is in Manchester II biphasic binary data format while on the bus.

### 38.4.2 MS1553B Bus Operation Description

#### A. Data flow description

MS1553B uses a **command response philosophy** requiring that all error free messages received by the RT, excluding broadcast commands, shall be followed by the transmission of a remote terminal MS1553B status word. All transactions, either from the BC to the RT or the RT to the BC, are initiated by the BC. The command word contains information as to which ORU RT the command is directed and is always transmitted from the BC to the RT. Figure 38-4 is a graphical representation of the MS1553B command, status, and data words structure.

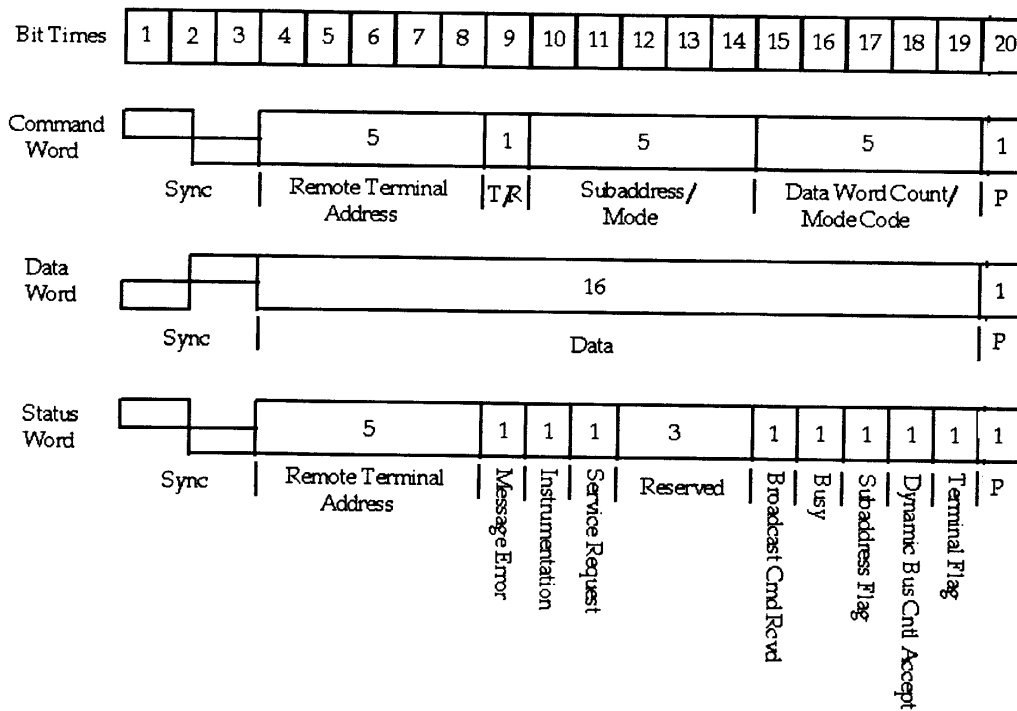


Figure 38-4. MS1553B data formatting

#### B. Definition of terms

- MS1553B command word - The command word contains information as to which RT (ORU) the command is directed and is always transmitted from the BC to the RT. Command transactions from a BC to an RT shall be spaced apart by not less than 4 microseconds. This spacing is called the minimum intermessage time gap.
- Sync - The first 3 bits of the command word.

3. RT address - Five bits, bits 4-8, following the sync signal. A total of 31 locations can be addressed with the MS1553B. Each RT has a unique address. Hex 1F (11111) is not to be assigned to a specific RT since it is reserved for broadcast mode. This mode is used for time broadcasting to all RTs on a MS1553B data bus. Note that the RTs do not respond to a broadcast time command word from the BC; i.e., they do not respond to the command with a status word as they normally would.
4. Transmit/Receive (T/R) bit - Bit 9 indicates the action required by the RT. Logic 0 indicates that the RT is to receive data into the subaddress called out in the command word. Logic 1 indicates that the RT will transmit data from the subaddress called out in the command word.
5. Subaddress/mode - Bits 10-14 are used to indicate either an RT subaddress or use of the mode (code) control. The term "subaddress" refers to a memory location in the Random Access Memory (RAM) that is shared by both the OIU BIA and the OIU OCC. This RAM is usually called the MS1553B shared RAM or shared memory. The BIA chip set is directly connected to the shared RAM address and data lines for Direct Memory Access (DMA) control over the shared RAM. The OCC is isolated from the shared RAM via isolation buffers on the address and data lines. The OCC has to "get permission" from the BIA to access shared RAM.
6. RT subaddress - Valid range is 00h-1Fh, with 00h and 1Fh reserved for mode control (see below).
7. Mode control - 1Fh or 00h in this field represents mode code commands. Mode commands generally manage the MS1553B RT BIA, not the OCC. Mode code commands can be used only with the transmission of no data words or of a single MS1553B data word.
8. Parity - Bit 20 of the command word is used for setting odd parity over the preceding 16 bits.
9. MS1553B data word - The 20-bit data word, either to or from the RT, includes the following:
  - a. Sync - The first 3 bits of the data word.
  - b. Data - Bits 4-19 are the 16 data bits, either to or from the RT, as indicated by the T/R bit.
  - c. Parity - Bit 20 of the data word is used for setting odd parity over the preceding 16 bits.
10. MS1553B Status word - The 20-bit data word, either to or from the RT, includes the following:
  - a. Sync - The first 3 bits of the data word.

- b. RT address - Bits 4-8 are the 5-bit RT address returned to the BC.
- c. Status word assignments
  - (1) Bit 9 is the message error bit that has only limited usage in MIL-STD-MS1553B specifications. The message error bit is only returned in a status word response if the RT detects an error free illegal command via the command illegalization function. This function is usually added hardware logic or detected by the host Central Processing Unit (CPU).
  - (2) Bit 10 is the instrumentation bit that is not used for ISS. In standard MS1553B, it is set low for status words and high for command words.
  - (3) Bit 11 is the service request bit that is used to signal the BC that the RT is requesting service. In the ISS program, this bit is generally used to signal the BC applications software to issue a "Transmit Vector Word Mode Code" command to fetch ORU self-test error messages. Typically, several such error messages may be queued by the ORU and a separate command is required to fetch each message, the service flag being set again until all of the messages have been transmitted.
  - (4) Bit 15 is the broadcast command received bit that is set every time an error free broadcast command is received. This bit is not used in the ISS implementation of MS1553B.
  - (5) Bit 16 is the busy bit that is set indicating the RT is unable to move data. This bit is not used in the ISS implementation of MS1553B.
  - (6) Bit 17 is the subsystem flag bit that is set indicating an MS1553B RT has experienced failure conditions and is still healthy enough to report it. The OIU does not generate or use this bit.
  - (7) Bit 18 is the dynamic bus control acceptance bit that is set indicating the RT is assuming bus controller authority over the MS1553B data bus.
  - (8) Bit 19 is the terminal flag bit that is set indicating a fault in the RT.
- d. Parity - Bit 20 of the data word is used for setting odd parity over the preceding 16 bits.

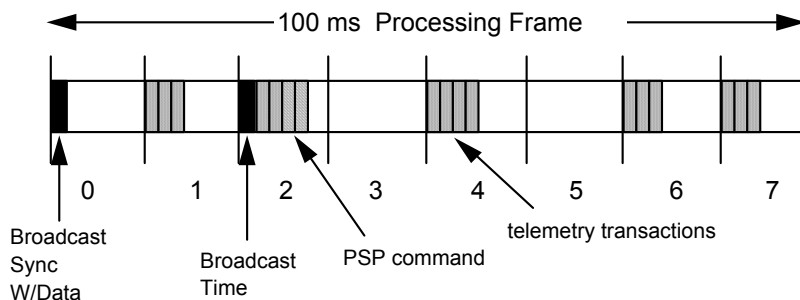
### 38.4.3 OIU MS1553B Bus Traffic

The OIU manages MS1553B bus transactions based on a 100-ms processing frame. These transactions include cyclic telemetry transactions, cyclic non-telemetry messages, such as the broadcast sync with data mode command (processing frame

number) and broadcast time, and noncyclic command transfer transactions. For buses on which the OIU is a BC, the OIU must initiate transactions to the RTs in the current OIU format. For the bus on which the OIU is an RT, the OIU processes messages received from the BC, and no processing frames are defined.

The 100-ms processing frame includes all cyclic transactions on the bus. A processing frame is defined for each bus on which the OIU is a BC and which has logical devices in the active OIU format. The processing frame defines when the broadcast sync with data mode command, the time broadcast, and the cyclic telemetry polls will occur for every device on the bus. The processing frame for each active BC bus is built during application initialization based on the active OIU format and data in the reconfiguration tables. See Figure 38-5. If the OIU is synchronized to an ISS BC, then each 100-ms processing frame is triggered by receipt of the broadcast sync with data command from the ISS BC. If the OIU is not in sync with an ISS BC or falls out of sync, the OIU internal 100-ms clock triggers the start of each processing frame. For each cyclic telemetry transaction, the data received from the RT and the associated block status word is placed into the PDI frame for telemetry. Data and block status words that are collected each 100 ms from the bus on which the OIU is RT are also placed into the PDI frame for telemetry.

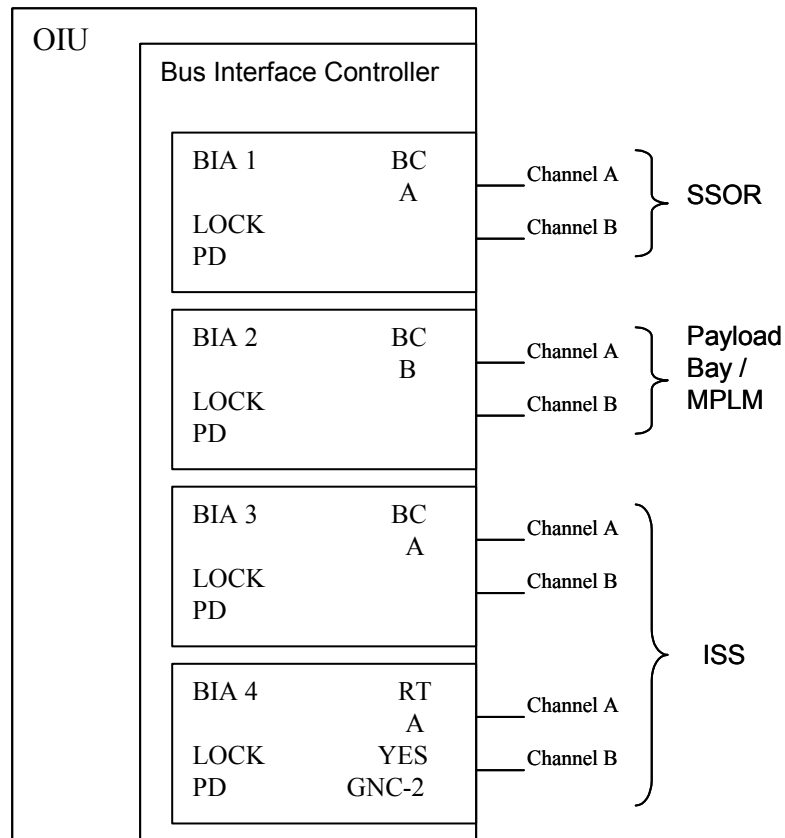
Commands are transferred to an RT as two 32-word MS1553B messages. Each processing frame specifies where and when transactions to transfer commands to RTs will occur. However, these messages are initiated only when a command is received by the OIU and needs to be routed to an RT. The OIU checks every 500 ms for a command to be routed. If a command is present, two MS1553B messages are added to the next 100-ms frame. No block status words are available in telemetry for command transactions. If no command is present, no command transfer messages occur on the bus.



**Figure 38-5. Example of 100-ms processing frame**

Note: MS1553B command transactions (PSP command) are shown in the Figure 38-5 as being transmitted in subframe 2. The actual subframe will be specified by OIU recon for that mission.

### 38.4.4 Bus Configurations



**Figure 38-6. OIU Bus Interface Controller (BIC)**

The OIU is designed to communicate on all four 1553 Bus Interface Adapters (BIAs) at the same time. **Currently**, the format limits only one BIA to send telemetry (combined with OIU status/health) to the PDI.

Each of the four BIAs can be configured so that it operates either as a BC or as a RT on that bus.

Only one of the four available BIAs can be configured as RT at a time because of limitations in the OIU to sync to more than one BC.

If the BIA is configured as Bus Controller (BC), the OIU schedules bus traffic and actively polls data from the device. In addition, if the OIU is a BC on the bus, then the bus configuration data inform the OIU which channel (A/B) to use as the primary channel for communicating with the physical devices on that bus.

If the BIA is configured as Remote Terminal (RT), the OIU waits for another device on the MS1553B bus to supply the data.

Switching OIU Formats does not effect whether a bus is RT or BC.

## 38.5 OIU OPERATIONS

The OIU is designed for two basic operations:

- (a) Receive data from devices communicating on MS1553B buses, multiplex these data with OIU health status into a single telemetry stream, and supply that telemetry stream to the PDI.
- (b) Receive commands from the PSP, and route to applicable devices on the MS1553B buses.

### 38.5.1 Command Processing Overview

The OIU is a Payload, thus all Payload Thru put commands, which either configure the OIU or are processed by the OIU to go to one of the four 1553B interfaces are listed in **Orbiter Command & Data Annex 4 (C&D Annex 4)**, Table 15-Uplink Load Commands. OIU Configuration Commands are listed using **P50Kxxxxx** MSID (Occurrences). This C&D Annex is online at Payload Integration Library System (PILS).

The OIU detects a command at the PSP interface when the alternating one-zero idle pattern (AAh) changes to eight zeros (00h). The OIU immediately begins storing a command when this OIU command flag is detected.

Once a properly formatted command has been received, the byte count, command message, and routing code are processed. Commands are processed every 500 ms by the OCC firmware to provide a maximum rate of one command per second. It is possible for the OIU to receive two PSP commands back-to-back, but the OIU processes only one per second.

The OIU receives and interprets commands up to 64 words long (16 bit words) from the PSP interface. Table 38-1 illustrates the Physical Breakdown of the Command Word Received by the PSP.

### 38.5.2 OIU Command Processing

The OIU first verifies that the Routing Code (RC), Table 38-2, matches a valid code specified in the RDT. The RDT maps valid RC to the logical device that will process the command. If the RC is recognized, the OIU attempts to route the command to the active physical device assigned to the logical device mapped to the RC. The OIU **always** transmits a 64-word command message to an MS1553B device. The 62 words of the message are dedicated to the message received from the PSP. If the message is less than 62 words long, the OIU adds fill (zeros) to the command message to total 62 words. The OIU appends its command count to the end of the second MS1553B transaction for use by an ISS MDM.

The SSOR to SSSR commanding path will be encrypted prior to sending commands via this path.



A. OIU configuration Commands

These commands are used to load a new OIU format for time updates, bus configurations, command rerouting, and changes to physical device data. Each of these commands is described in detail in Section 38.5.4. Additionally, MS1553B mode code commands that go out on a particular MS1553B bus are treated by the OIU as configuration commands.

B. Routing Commands/OIU BIA as BC

As bus controller, the OIU routes commands to a device, regardless of whether the device is active in the current format. The OIU transmits commands to MS1553B RTs only when a command with a valid routing code that is mapped to an RT is received (the OIU uses the RDT to determine how to route commands to MS1553B devices). The OIU generates two 32-word MS1553B transactions to transmit the command. The first transaction contains the first 32 data words of the command. The second transaction contains the last 30 data words (62 words maximum), a fill word, and the command count in the 32nd word. The OIU will try up to three times to transmit the command if transmission failures are detected as follows:

1. Attempt 1: Transmit on primary channel (A or B).
2. Attempt 2: If no. 1 fails, transmit on primary channel (A or B).
3. Attempt 3: If no. 2 fails, transmit on backup channel (B or A).

C. Routing Commands/OIU BIA as RT

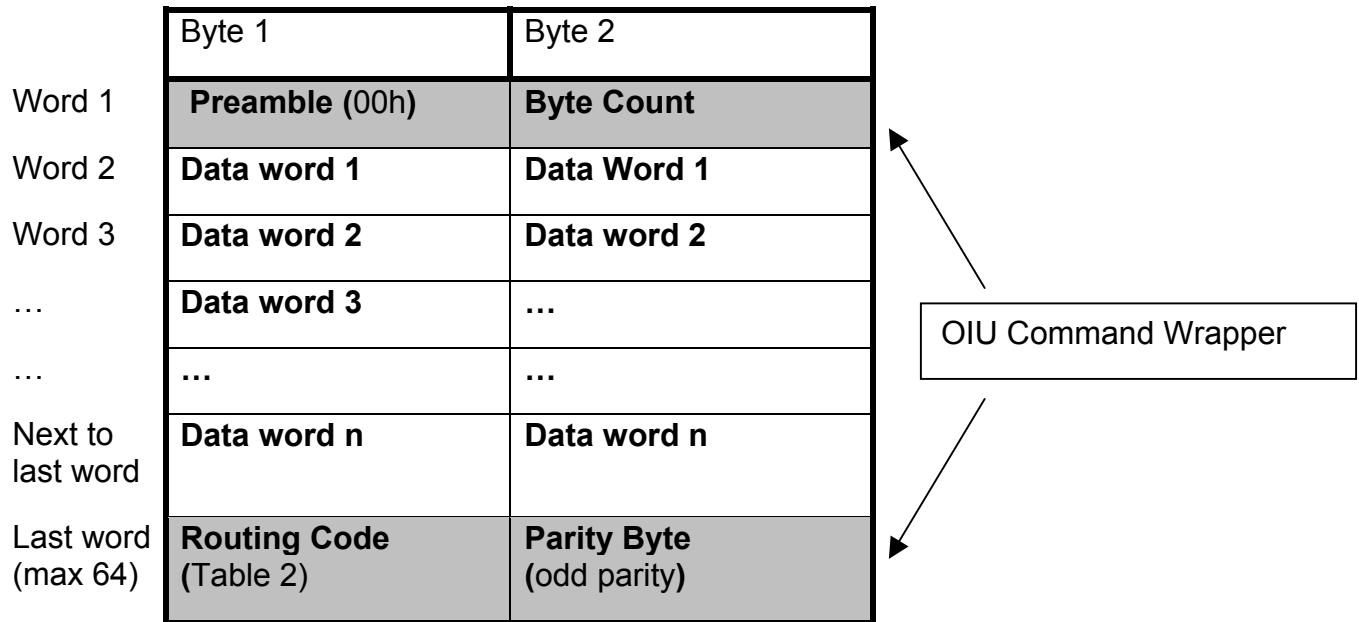
As a remote terminal, the OIU makes commands available for polling by the BC MDM. The OIU guarantees the command will be in the polling address for 1 second to allow the Bus Controller (BC) to retry failed command polls.

If the command is destined for a device on a BIA configured for RT mode (i.e., the OIU is functioning as an RT on that bus), the OIU stores the command (64 words) in the appropriate subaddresses of the BIA corresponding to that bus. An ISS BC will poll the OIU at 10 Hz for commands. When the OIU first initializes or reinitializes, each BIA command subaddress is initialized to 31 words of "FEEDh" and a 32nd word of "0000h". The ISS BC reads the 32nd word of the second subaddress to retrieve the command count. A change in the command count indicates to the BC that a new command has been polled from the OIU. A zero indicates to the ISS BC that this PSP command need not be processed. There are **no** OIU telemetry indications in case of a command problem on an MS1553B bus where the OIU is an RT.

### 38.5.3 Command Counter

When the OIU receives a valid command, the command counter parameter (P50U4132A) is incremented. This parameter indicates the number of properly formatted commands the OIU has received since initialization or reinitialization. The

command counter is used to indicate that a command was received and the OIU attempted to process the command. The command counter is also made available to the ISS MDM so that the MDM may determine when a new command is present to check, and if applicable, retrieve the RT subaddress.



**Figure 38-7. PSP to OIU Command Word**

The **OIU command wrapper** is the first 16-bit command word and the last 16-bit command word of any command sent to the OIU. The first word has two bytes: OIU Command Flag (00h) and the number of command bytes to follow. The last word also has two bytes, which are the OIU Command Routing Code (00h = OIU configuration command, all others are MS1553B bus destination devices) and an odd parity byte.

The **Preamble** of a GPC/PSP Command Word for the OIU will consist of 00h. The PSP will be configured to continually send the OIU a signal, called an Idle Pattern of alternating 1s and 0s (i.e., 1010101... or AAh). The Preamble allows the OIU to know when an actual Command to the OIU is sent (00000000 or 00h) vice the idle pattern (101010...).

The **Byte Count** of the GPC/PSP Command Word for the OIU will be a binary number representing the number of bytes for this Command word. A maximum of 64 Words can be sent at one time from the PSP to the OIU. A valid byte count number is greater than 4 (04h) and less than 126 (7Eh).

The **Data Word** is the actual Command sent to the OIU.

The **Routing Code (RC)** indicates the logical destination of the command. As per Table 38-2 a routing code of 00h designates the command as an OIU configuration

command; a nonzero routing code means the command will be routed to a device on an MS1553B bus.

**Table 38-2. OIU Routing Code destinations**

| Code      | Destination device   |
|-----------|--|
| 00h       | OIU Configuration Command                                    |
| 01h       | GNC MDM Logical Device                                       |
| 02h       | SSOR-SC (Standard Commands for an ISS MDM)                   |
| 03h       | SSOR-EK (Encryption Key commands)                            |
| 04h       | MPLM (Mini Pressurized Logistics Module ) MDM Logical Device |
| 05h       | Node 1 MDM Logical Device                                    |
| 06h       | FGB MDM Logical Device                                       |
| 07h       | AMS Logical Device   |
| 08h - F0h | Not used   |
| F1h       | MDMX-SC (MDMX Logical Device standard commands) *            |
| F2h       | MDMX-DL (MDMX Logical Device data load commands) **          |
| FFh       | LAB TEST ONLY  |

The **Parity Byte** (Vertical Odd Parity Byte) is a check on the Command Word. Calculate the vertical odd parity to place in the last command word of the OIU command wrapper as follows:

- A. Assume a command with the following command words:

1401 153F 0000

- B. Add the Wrapper first word

00h (OIU command flag) and 08h (8 bytes to follow, including the last word of the wrapper) = 0008

0008 1401 153F 0000

- C. Add the Routing Code (this example is an OIU Configuration Command):

0008 1401 153F 0000 00

- D. Break the command into bytes

00 08 14 01 15 3F 00 00 00

- E. Exclusive-OR all bytes together with an extra **FFh** (← **Exclusive OR'ing**)

00h ⊕ 08h ⊕ 14h ⊕ 01h ⊕ 15h ⊕ 3Fh ⊕ 00h ⊕ 00h ⊕ 00h ⊕ **FFh** = C8h

- F. Add the Parity Check to the last word of the command

0008 1401 153F 0000 00C8

- G. So, the command would be assembled for entry into the first five command word fields as follows:

0008  
1401  
153F  
0000  
00C8

**Example 1:**

P50K5632J - Change Bus 3 to RT

Original Command → 1401 153F 0000

Preamble and Byte Count → 00h

Byte Count → 08h

OIU Configuration Command Routing Code → 00h

Parity Check is:

$00h \oplus 08h \oplus 14h \oplus 01h \oplus 15h \oplus 3Fh \oplus 00h \oplus 00h \oplus 00h \oplus FFh = C8$

**Final OIU Command → 0008 1401 153F 0000 00C8**

**Example 2:**

U11K0258L – MPLM Cabin Fan Off:

ISS Command → 08F8 C000 000F 0000 0000 0000 0029 385E 0C0F 007F 007F 0E9B

Preamble → 00h

Byte Count → 1Ah (this is 26 byte words)

MPLM Routing Code → 04h

Parity Check is:

$00h \oplus 18h \oplus 08h \oplus F8h \oplus C0h \oplus 00h \oplus 00h \oplus 0Fh \oplus 00h \oplus 00h \oplus 00h \oplus 00h \oplus 00h \oplus 00h \oplus 00h \oplus 29h \oplus 38h \oplus 5Eh \oplus 0Ch \oplus 0Fh \oplus 00h \oplus 7Fh \oplus 00h \oplus 7Fh \oplus 0Eh \oplus 9Bh \oplus 04h \oplus FFh = 07$

**Final OIU Command → 001A 08F8 C000 000F 0000 0000 0000 0029 385E 0C0F 007F 007F 0E9B 0407**

### 38.5.4 Configuration Commands (Routing Code → 00h)

Configuration commands will cause the OIU to run the Application Initialization routine (except as noted below). Configuration commands are formatted as shown in Figure 38-8. A description of each command follows:

These Commands are listed for Flight Specific within the Payload Integration Library System (PILS) Command and Data Annex 4, Table 13

**UPDATE OIU TIME and YEAR** **0Ah**

**0Axx**

xx = cyyyyyyy  
 c = "Century" flag (1 = 20xx, 0 = 19xx)  
 yyyyyyy = year in binary form ('98 = 1100010)  
 example: Update Time, Year = 1999: 0A63

**UPDATE YEAR ONLY** **0Bh**

**0Bxx**

xx = cyyyyyyy  
 c = "Century" flag (1 = 20xx, 0 = 19xx)  
 yyyyyyy = year in binary form ('98 = 1100010)  
 example: Update Year Only, Year = 2000: 0B80  
 example: Update Year Only, Year = 1998: 0B62

**CONFIGURATION COMMAND HEADER** **14h**

**14xx**

xx = Number of OIU configuration commands to follow, in hex  
 NOTE: ONLY OIU COMMAND TYPES 15h, 16h, 17h, 18h, and 19h ALLOWED  
 example 1: Configuration Command for Bus 1 to Channel A:  
 1401 1510 F000  
 example 2: Composite Command - Configure OIU for N1-1 MDM comm:  
 Commands: N1 LD to N1-1 PD 1704 0700  
           Bus 3 to RT 153F 0000  
           Bus 4 to BC 154F 0000  
           Load Format 2 1902 0000  
 1404 1704 0700 153F 0000 154F 0000 1902 0000

**Figure 38-8. Configuration commands format**

|  |
|--|
| <p><b>CHANGE BUS CHANNEL OR BC/RT</b> <span style="float: right;"><b>15h</b></span><br/><b>15xy zuuu</b><br/>x = Bus Number (1-4)<br/>y = Channel B Flag (0 = A, 1 = B, F = no change to channel)<br/>z = BC Flag (0 = RT, 1 = BC, F = no change to BC flag)<br/>uuu = unused bits, can be anything (fill)<br/>example: Change Bus 1 to Channel A:<br/>1401 1510 F000 (note three zero hex digits of fill)<br/>example: Change Bus 3 to Channel B and RT:<br/>1401 1531 0000</p>             |
| <p><b>CHANGE PD BUS OR RT ADDRESS</b> <span style="float: right;"><b>16h</b></span><br/><b>16pp ubrr</b><br/>pp = Physical Device ID in Hex, 00-32h range see Table 38-4<br/>u = unused, fill<br/>b = Bus number, range 1-4, or F if no change<br/>rr = RT Address in Hex, 00-1Eh range, or FF if no change<br/>example: Change PD 1 to Bus 3:<br/>1401 1601 03FF<br/>example: Change PD 3 to Bus 2 and RT Address 30:<br/>1401 1603 021E</p>  |
| <p><b>ASSIGN PD TO LOGICAL DEVICE</b> <span style="float: right;"><b>17h</b></span><br/><b>17LL ppuu</b><br/>LL = Logical Device ID in hex, range 1-23h see Table 38-3<br/>pp = Physical Device ID in hex, range 1-32h see Table 38-4<br/>uu = unused hex "digits", fill data<br/>example: Change LD # 02 to PD #01:<br/>1401 1702 0100</p>  |
| <p><b>CHANGE COMMAND ROUTING</b> <span style="float: right;"><b>18h</b></span><br/><b>18xx yyuu</b><br/>xx = Command Routing Code, in hex, to be changed, range 01-FF<br/>yy = Command Routing Code, in hex, which will replace "xx", range 01-FF<br/>NOTE - If xx = yy, the OIU will reset the specified routing code to the recon<br/>table default value<br/>uu = unused, fill data<br/>example: Change routing for all commands destined for 1F to destination 8A<br/>1401 181F 8A00</p> |

**Figure 38-9. Configuration Commands (continued)**

|   |            |
|---|------------|
| <p><b>OIU FORMAT COMMAND</b><br/> <b>19xx uuuu</b><br/>                 xx = OIU Format number, in hex, range 1-FF<br/>                 uuuu = unused, fill data<br/>                 example 1: Command to load OIU Format 1:<br/>                 1401 1901 0000<br/>                 example 2: Command to load OIU Format 100:<br/>                 1401 1964 0000</p>  | <b>19h</b> |
| <p><b>SEND MS1553B MODE CODE COMMAND</b><br/> <b>1Exy nuuu wwwwww dddd dddd</b><br/>                 x = OIU Bus Number to send command out, range 1-4<br/>                 y = MS1553B Subframe Number, range 0-7<br/>                 n = Number of MS1553B Data Words in hex, range 0-1<br/>                 uuu = unused, fill data<br/>                 wwwwww wwwwww = MS1553B Command Word in hex<br/>                 dddd dddd = MS1553B Data Word in hex<br/>                 example: Send MS1553B command 1234 ABCD with data word FFFF FFFF<br/>                 out Bus 1, in Subframe 2 (not a real MS1553B command, example only):<br/>                 1E12 1000 1234 ABCD FFFF FFFF</p> | <b>1Eh</b> |

**Figure 38-10. Configuration Commands (concluded)**

### 38.5.5 Command Description

#### A. READ PTB (type 0Ah)

This command forces the OIU to read time from the PTB interface and to reinitialize. The PTB interface supplies orbiter time to the OIU in the form of ddd/hh/mm/ss/uuu, where ddd is Julian days. The time value for the current year must be specified by a command to the OIU. For a discussion on how PTB updates impact time processing, see Section 38.7. The command includes 1 bit to indicate the hundreds of years (19 or 20) and 7 bits to indicate the year. The year must be in the range from 1995 to 2099, inclusive, in order to be valid. In addition, if all 7 bits are high (logical 1), the OIU does not update the year. If the year field contains an invalid number, the INVALID CONFIG COMMAND error (P50X4287E) is set, and the Read PTB command will not be acted upon. When the hundreds of years or year is changed, the OIU recalculates the month and day and accounts for leap years.

#### B. UPDATE YEAR ONLY (type 0Bh)

This command updates the year but does not affect the hours/mins/secs of OIU time. The command includes 1 bit to indicate the hundreds of years (19 or 20) and 7 bits to indicate the year. The hundreds of years and year must be in the range from 1995 to 2099, inclusive, in order to be valid. If the year field contains an invalid value, the INVALID CONFIG COMMAND error (P50X4287E) is set and the

command is rejected. When the OIU changes the century/year, the month and day are recalculated to account for leap years. See Section 38.7 for a discussion of time management.

This command does not cause the OIU to go through Application Initialization.

C. Configuration Command Header (type 14h)

The configuration command header is used to tell the OIU how many configuration commands follow. This allows each command uplink to contain one or multiple configuration commands. This header must precede all of the following commands:

CHANGE BUS CHANNEL OR BC/RT (cmd type 15h)

CHANGE PD BUS OR RT ADDRESS (cmd type 16h)

ASSIGN PD TO LOGICAL DEVICE (cmd type 17h)

CHANGE COMMAND ROUTING (cmd type 18h)

OIU FORMAT COMMAND (cmd type 19h)

When a type 14h header is used with multiple configuration commands following, then the command is referred to as a “composite command” (something like an Multiple Real-Time Command (MRTC)). In processing a composite command, the individual commands are processed in series, and all commands are implemented before the OIU returns to normal command processing. If any command in the sequence cannot be processed, it is skipped and the next command is processed. The INVALID CONFIG COMMAND error (P50X4287E) is set if one or more of the individual commands contain errors. The command count is incremented once for each type 14h header, regardless of how many individual configuration commands are in the composite command.

D. CHANGE CHANNEL AND BC/RT FLAG (cmd type 15h)

This command is used to reconfigure the MS1553B bus interface (BIAs) of the OIU. This command designates the Primary Channel (A or B) for a bus and/or sets the associated OIU BIA to BC or RT mode. MS1553B bus traffic is affected when any changes are made to the bus configuration.

Primary channel designations and bus BC/RT mode settings are not affected by OIU format changes. Upon power cycle, the OIU uses the default channel designations and BC/RT settings in the reconfiguration table to configure the MS1553B BIAs.

Channel Changes:

The primary channel designation determines which channel is used for MS1553B traffic when the OIU is the BC on a bus. If the OIU is an RT on a bus and a



channel change command changes the primary channel designation, the OIU telemetry reflects the new designation. However, the OIU continues to respond on whichever channel the ISS BC polls.

A channel change command for a bus on which the OIU is configured as BC takes effect immediately. Upon receipt, the OIU begins using the designated channel.

Note: The OIU can only operate as an RT on one bus at a time. If a bus is already configured as an RT and a channel change command is received that would configure another bus to RT, the command is rejected and the INVALID CONFIG COMMAND error (P50X4287E) is set.

E. CHANGE PD BUS OR RT ADDRESS (cmd type 16h)

The initial map of where the physical devices are located, including bus number and RT address, and how the physical devices map to logical devices are contained in the reconfiguration table in OCC EEPROM.

This command is used to map a physical device to a new bus or new RT address that is different from the mapping specified in the reconfiguration table. These changes remain in effect until the OIU is power cycled. This command can change the bus and/or RT mapping for a device even if the device is in the active OIU format.

If a physical device ID that is not recognized (not in the current reconfiguration table) is specified, the INVALID CONFIG COMMAND error (P50X4287E) is set and the command is rejected.

F. ASSIGN PD TO LOGICAL DEVICE (cmd type 17h)

This command selects which physical device is currently assigned to a particular logical device. This command is used to switch between redundant devices such as redundant MPLM MDMs or FGB MDMs. The logical device ID must be recognized in the OIU reconfiguration table and the physical device ID must be mapped to the specified logical device in the reconfiguration table. If these constraints are met, then the specified physical device is assigned to represent the logical device.

Note: Only one device should be mapped to a bus on which the OIU is an RT, and this device should be the ISS BC. Additional ASSIGN PD TO LOGICAL DEVICE (cmd type 17h) commands should be used to move the other devices in the active OIU format to other buses. Failure to do so may make the OIU believe that one of the RTs is the ISS BC.

*Table 38-3. Logical/Physical Device*

| Logical Device | LD ID | Physical Device | PD ID |
|----------------|-------|-----------------|-------|
| GNC            | 01    | GNC -1          | 01    |
|                |       | GNC -2          | 02    |
| N1             | 04    | N1-1            | 07    |
|                |       | N1-2            | 08    |
| FGB            | 05    | FGB 1           | 09    |
|                |       | FGB 2           | 0A    |
| MDMX           | 1E    |                 |       |
|                |       |                 |       |
| Test Device    | 23    |                 |       |

G. CHANGE COMMAND ROUTING (cmd type 18h)

This command is used to change the destination of a command received by the OIU destined for a device on a MS1553B bus to another destination device. This command could, for example, cause the OIU to send commands with a routing code of FGB MDM to the N1 MDM.

Note: A routing code of zero (OIU Command) is prohibited from being included in a "Re-route PSP Commands" command, and will cause the INVALID CONFIG COMMAND error (P50X4287E) to be set.

If either of the two routing codes in this command is an invalid code, the command is rejected and the INVALID CONFIG COMMAND error (P50X4287E) is set.

H. OIU FORMAT COMMAND (cmd type 19h)

This command is used to change the OIU format.

I. SEND MS1553B MODE CODE COMMAND (cmd type 1Eh)

This command is used to have the OIU, as BC, send a MS1553B mode command to an RT. The mode command is processed as any other PSP command to an RT. This command does not cause the OIU to reinitialize.

The only check the OIU does on this command is to determine if the device the command is for is an RT to the OIU. If the OIU is RT on the bus specified in the command, the command is rejected and the INVALID CONFIG COMMAND error (P50X4287E) is set. The OIU does no other validity checking on the command.

### 38.6 TELEMETRY PROCESSING

The OIU receives data from devices communicating on MS1553B buses, multiplexes this data with OIU internally generated data (health, status, error logs) into a single

telemetry stream, and supplies that telemetry stream to the PDI. The OIU Format defines the content and structure of the OIU telemetry.

### 38.6.1 Formats

An OIU Format specifies which MS1553B device the OIU collects data from and how this data is merged with OIU Health and Status (H&S). Up to 20 formats can be defined in the RDT of the OIU, but a maximum of 10 are defined per mission per ICD-A-21264. The OIU can process only **one** OIU Format at a time. The RDT within the OIU specifies which of the 10 Formats will be active on power-up. The nominal power-up default format is 255, which contains OIU H&S telemetry only.

Each Format definition specifies **one logical device** that is active in the OIU. When the Flight Crew or Flight Controllers changes the OIU format, the OIU stops processing data from the current Logical Device and begins collecting data from the newly designated Logical Device.

- (1) When the OIU is a Bus Controller (BC) on all four MS1553B buses, the telemetry frames begin at a minor frame count equal to 0.
- (2) When the OIU Format is changed to a Logical Device being used as a Remote Terminal which is "slaved" to an ISS BC MDM and the ISS BC MDM is powered on and transmitting MS1553B transactions, the first PDI minor frame count for that format can be anywhere from 0 to 99. The ISS BC MDM must be transmitting prior to the format change for the OIU to synchronize to it; otherwise, the OIU will be on internal time and not synchronized to the ISS BC MDM; if this is the case, the OIU reinitializes and resumes operation under internal timing control. The telemetry data from the ISS BC are still placed in the telemetry frames sent to the PDI, but may move relative to the other data in the OIU PDI stream because of the loss of sync with the MDM.

Switching OIU Formats does not affect the Physical Device to Logical Device Mapping. Transactions are then set up on the buses to process telemetry for the new Logical Device.

### 38.6.2 OIU to PDI Telemetry Stream

The OIU to PDI telemetry Major Frame is 10 seconds long and is made up of 100 individual PDI minor frames. The active OIU Format specifies the content of the OIU to PDI telemetry; an example to illustrate is shown in Figure 38-11.



Figure 38-11 is for an OIU Format that includes both an ISS BC GNC MDM and a RT device such as the SSOR. The OIU Format is broken down as follows:

1. Minor frame sync pattern (C95A63h for the OIU).
2. Minor frame count.
3. OIU status words.
4. ISS BC MDM unconverted telemetry obtained from the OIU BIA “data blocks” assigned to the proper MS1553B subaddresses.
5. RT mode block status words for each of the MS1553B transactions that comprise the unconverted ISS telemetry. These block status words contain information on the success or failure of each MS1553B transaction
6. Unconverted telemetry from the RTs in the current OIU format comes next, and as can be seen from the figure, is obtained from the OIU BIA “message blocks” assigned to the respective subaddresses.
7. BC mode block status words for each of the MS1553B transactions.
8. Converted telemetry words.

Fill data are added (if required) at the end of a frame to match an allowable PDI data rate.

#### 38.6.4 OIU to PDI Telemetry Data Interruptions

When in flight mode, the OIU always outputs a data stream to the PDI, with the following exceptions:

1. The PDI telemetry stream will be interrupted when the OIU goes back through application initialization.
2. A second condition is a result of multiple asynchronous clocks used in the OIU, causing interruptions in the PDI telemetry stream. The 100-ms processing frame clock (in the OCC) is not the same clock used in the PDI transmitter circuit (in the OIC), and these clocks are not synchronized. Therefore, as the clocks drift at different rates, an **occasional PDI sync loss** from the OIU occurs. The frequency of sync loss caused by this condition is dependent on the source of the OIU 100-ms processing frame clock. If the OIU is in sync with an ISS BC, the OIU is using the ISS BC for its internal 100-ms processing frame. Based on the expected delays and the accuracy requirement for the ISS BC, an **occasional OIU-generated sync loss** is expected slightly more frequently than when the OIU generates its own 100-ms processing frame.
3. When the OIU is in sync to an ISS BC, the OIU is forced to synchronize its internal processing to the transactions from the ISS BC. The transactions

from the BC may occur at a slightly different frequency from that required for the OIU to provide data to the PDI, resulting in **an occasional PDI sync loss from the OIU**. However, PDI sync is recovered immediately without any required action from the crew or ground.

During these three nominal, but infrequent, interruptions, the OIU sends the last byte stored in the OIC SRAM prior to reentering application initialization to the PDI repeatedly instead of properly formatted frames. When this condition happens, the effect is momentary loss of PDI decom word (and, therefore, frame) sync. ***PDI decom bit sync is not affected since the OIC always generates a bit clock (even when the OCC is going through application initialization)***. When the OIU completes application initialization and returns to cyclic processing, properly formatted frames are sent to the PDI.

### 38.6.5 BIA Interruptions

If the active BIA fails, the OIU will not overwrite the last two major frames of data within its output toggle buffers. The OIU will continually send the PDI “static” data alternating between the last two 10 second Major Frames.

This was tested in the JSC engineering lab by turning off the BC to the OIU. The technician saw the static OIU data being sent to the PDI.

### 38.6.6 Data Conversions

The SM GPC payload services can display OIU telemetry parameters that are 8 bits (or less) in length on the MCDS or MEDS. The OIU provides linear data conversions for ISS parameters that exceed these limitations. Bit field extractions and floating point conversions are performed by the OIU on the telemetry collected from the devices in the mode. The converted data are placed in the same PDI frame as the raw source data. Conversions are specified within the OIU RDT. Up to 40 conversions can be processed per minor frame (only one of which can be floating point), and up to 2000 conversions can be specified per mission in the RDT.

For bit-field conversions, the OIU can extract up to 8 bits from a 16-bit MS1553B data word and store the extracted bits (right adjusted) into a designated 8-bit word in the telemetry frame. The OIU can also perform one conversion per processing frame for Institute of Electrical and Electronic Engineers (IEEE) 32-bit floating point parameters. The OIU scales between two points (start and end) on a straight line. A zero is returned for all values less than the “start,” and 255 is returned for all values greater than the “end.” The converted parameter is scaled equally between start and end in 255 equal parts and is stored in the same frame as the source floating point parameter. If errors occurred during floating point conversion, the converted parameter is set to either 0 or 255, depending on the types of errors, and the (floating point conversion err) is set in the OIU H&S. This error is cleared in the next frame.

### 38.6.7 Temperature Telemetry

The OIU is cooled by conduction of heat to the air in the rack and by conduction of heat into the orbiter structure. The OIU does not have a fan. The OIU chassis temperature has usually measured 4° F hotter than the ambient air in ground testing. The OIU power supply has usually measured 30° F hotter than the chassis in ground testing. The power supply temperature is downlinked through MDM PF 1 (OIU 1) or PF 2 (OIU 2). Note that the temperature signal is not provided on Functional Equivalent Units (FEUs) or engineering units if one of these nonflight OIU types is encountered in SAIL testing. The signal is an analog differential signal with a voltage range of +5 V dc to -5 V dc.

The MSIDs are

- OIU 1 = P50T4000V (uses PF 1 MDM)
- OIU 2 = P50T4001V (uses PF 2 MDM)

The voltage to temperature calibration curve is:

$$\text{OIU temperature (degrees F)} = V(32.029) + 140.60854$$

Note that the zero-voltage (OIU "OFF") temperature reading is 140.6° F.

The OIU temperature is sensed in the Systems Management (SM) General Purpose Computer (GPC) for Fault Detection and Annunciation (FDA) purposes.

After various discussions with the design engineers, it was agreed **to establish 150F as an operational limit** if one needed to be defined. 150F temperature (approximately) is the value that the OIU was outputting during thermal certification testing while the environment went to approximately 130F. The number seems a bit low, but 150F keeps the unit within the environmental limits that it was certified to (10F-130F). Although the power supply and parts can go to a much higher temperature, setting the operational limit at 150F keeps the unit within certification limits.

The 212F temperature was based on the power supply survivability. It was determined that the power supply could survive temperatures above 212F, but that anything that high was cause for concern.

The FDA limit is 212° F, and the message is S212 OIU TEMP HI.

### 38.6.8 Health and Status Telemetry

In each minor frame, 8 bytes (byte 5-12) are reserved for OIU Health and Status. These bytes are called the standard set of OIU H&S parameters. This portion of the OIUs PDI output contains all OIU housekeeping telemetry. From OIU output minor frames 0 to 9, these 8 bytes contain different data fields. The fields contained in these 8 bytes repeat themselves every 10 OIU output minor frames. A summary of these fields in a tabular form is provided Table 38-4.

Descriptions of these fields follow:

A. OIU format (P50U4010A)

This field consists of 1 byte and is used to identify the current OIU format associated with the data stream. Allowed values are 001-255 (01h-FFh), with 001-010 and 250-255 available as index numbers for item 1 on the OIU SPEC (SM212).

B. OIU physical box ID (P504011D)

This field consists of 1 byte. Each OIU physical box has its own unique identification number. This field provides the identification number of the OIU generating the PDI data stream. This number is not the box serial number, but can be used to determine the serial number as follows:

**Table 38-4. OIU Serial Number Telemetry**

| OIU S/N | ID (hex) | ID (decimal) | Facility    |
|---------|----------|--------------|-------------|
| 1001    | A1       | 161          | JSC OIU LAB |
| 1002    | 60       | 96           | KSC CITE    |
| 1003    | 61       | 97           | KSC CITE    |
| 1004    | 62       | 98           | JSC SAIL    |
| 1005    | 63       | 99           | JSC SAIL    |
| 1006    | A8       | 168          | FLT UNIT    |
| 1007    | A7       | 167          | FLT UNIT    |
| 1008    | A5       | 165          | FLT UNIT    |
| 1009    | 00       | 000          | FLT UNIT    |
| 1010    | A2       | 162          | FLT UNIT    |
| 1011    | A3       | 163          | FLT UNIT    |
| 1012    | A4       | 164          | FLT UNIT    |

C. BC/RT indicators (P50X4021E-P50X4024E)

This field (parent MSID, P50M4020P) consists of 1 byte (8 bits). Each bit in this field (MSIDs P50X4021E-P50X4024E) is used to indicate whether the OIU is functioning as a BC or an RT on a particular bus. For the parent MSID, the value of the Most Significant Bit (MSB) (bit 0) represents the BC/RT status for bus 1, bit 1 represents the status of bus 2, and so on down to the Least Significant Bit (LSB) (bit 7), which represents the status of bus 8. A value of 1 indicates that the OIU is the BC, and a value of 0 indicates that the OIU is an RT in both the parent and child MSIDs.

Note: The OIU has only four MS1553B buses at present; so the indicators for buses 5 to 8, which are downlinked, are ignored.



D. Channel A/B indicators (P50X4041E-P50X4044E)

The structure of this field (parent MSID P50M4040P) is similar to the BC/RT indicator field. It also has 8 bits. For each bit (parent and children), a value of 0 indicates that channel A is selected as the prime channel in the OIU for that BIA, and a value of 1 indicates that channel B is selected as the prime channel in the OIU for that BIA. This telemetry indicates only the prime selected channel of the OIU BIAs (which bus is to be used first in attempting communications with an RT), not which channel is actually in use. The block (transaction) status words actually indicate the channel currently in use for communications with an RT or BC. See Section 38.9.5.1 for further information on BSWs.

E. OCC error log latest entry no. (P50U4170D)

This is the OCC error log entry number that was last written by OCC firmware. OCC error log entry numbers range from 1 to 100. A value of 0 indicates that the error log is empty.

F. Station-generated broadcast time (P50U4110D)

This field consists of six bytes. They are used to represent the value of station-generated broadcast time (excluding microseconds) received by the OIU. Starting from the MSB (byte 0), each successive byte represents the value of years minus 1900, months, days, hours, minutes, and seconds (the LSB (byte 5)). If the active OIU format does not include an ISS BC, this field is set to zeros. When the ISS BC is in the active mode, the time received from the ISS is stored here. If the ISS BC stops communicating with the OIU, the time field is not updated and the last time received becomes static. Note that this time is in CCSDS format, not IRIG-B, and the days are not Julian days.

G. OIU-generated broadcast time (P50U4100D)

The structure of this field is the same as the station-generated broadcast time field. This field also consists of 6 bytes. However, the value in each byte represents the time field propagated by the OIU and supplied to any RTs by the OIU.

H. Station-generated broadcast time, microseconds portion of time (P50U4118D)

This field consists of 3 bytes and is used to represent the value of the microseconds portion of the station-generated broadcast time. If the active OIU format does not include an ISS BC, this field is set to zeros. When the ISS BC is in the active mode, the time received from the ISS is stored here. If the ISS BC stops communicating with the OIU, the time field is not updated and the last time received becomes static.

I. OIU-generated broadcast time, microseconds portion of time (P50U4108D)

This field consists of 3 bytes and is used to represent the value of the microseconds portion of the OIU-generated broadcast time.

J. Status bytes

There are a total of 10 status bytes (80 bits). Each bit represents the occurrence of an error. Whenever a particular bit is set to 1, it indicates that a corresponding error occurred at some time in the 10 frames prior to the beginning of this 10-frame cycle. See the OIU-generated error table in Appendix B of this systems brief for a description of the individual errors. The 10 parent MSIDs are P50M4210P, P50M4220P, P50M4230P, P50M4240P, P50M4250P, P50M4260P, P50M4270P, P50M4280P, P50M4290P, and P50M4300P, representing H&S telemetry bytes 1-10, respectively.

K. OIU-Received PSP Command Counter (P50U4132A)

This field consists of 2 bytes and is used to represent the total number of PSP commands received by the OCC (successfully passed by the OIC) since power-on. See Section 38.5.2.

L. OCC error log wrap counter (P50U4140D)

This field consists of 2 bytes and represents the number of write cycles of the EEPROM where the OCC error log resides. End of life for the EEPROM is specified as a minimum of 10,000 write cycles per byte.

M. PSP/PTB error log wrap counter (P50U4150D)

This field consists of 2 bytes and represents the number of write error log wrap cycles of the EEPROM where the OIC PSP/PTB error log resides. Endurance for the EEPROM is specified as a minimum of 10,000 write cycles per byte.

N. PDI error log wrap counter (P50U4160D)

This field consists of 2 bytes and represents the number of write error log wrap cycles of the EEPROM where the OIC PDI error log resides. Endurance for the EEPROM is specified as a minimum of 10,000 write cycles per byte.

O. Frame count bit (P50X4351E)

The MSB in PDI frame byte 11 (parent MSID P50M4350P) is the frame count bit. Whenever the value of the frame count bit is set to 1, it indicates that the frame count for this PDI minor frame was not consecutive from the previous PDI minor frame. Therefore, the data content of this PDI minor frame might not be correct. A nonconsecutive frame count occurs if the ISS BC broadcast or the SSOR sent a processing frame number that was not consecutive. This parameter is generated at a 10-Hz rate.

For each OIU format, the OIU provides three H&S parameter fields for each of the first four device format Identifications (IDs) in the mode: Dev (phys) code/sync status field (parent MSIDs P50M4050P, P50M4060P, P50M4070P, and P50M4080P for ADs 1-4, respectively), dev bus/RT number field (P50M4054P,

P50M4064P, P50M4074P, and P50M4084P), and dev data start byte/OIU RT number, bus field (P50M4057P, P50M4067P, P50M4077P, and P50M4087P).

1. Dev (phys) code/sync status - This field consists of 1 byte (8 bits). The first 6 bits represent the physical device code used for the logical device. The remaining 2 bits indicate the sync status. Note that there are no child MSIDs for the PD or sync status for any AD, other than the 8-bit parent. The MCC display decodes the parent MSIDs, and SM212 (the OIU SPEC) uses onboard display MSIDs for each bit of the parent, with a comp. Sync status values of 1, 2, and 3 represent "in sync," "out of sync," and "default," respectively. Sync codes 1 and 2 are used when the physical device is an ISS BC or the SSOR. A sync code of 1 indicates the OIU is in sync to the device and is using the frame count from this device to drive telemetry processing and MS1553B traffic on other buses. A sync code of 2 indicates the OIU has lost sync with the device and is internally generating the frame count to drive telemetry and MS1553B traffic. A sync code of 3 is assigned to all other RTs. The code does not indicate whether the RT is responding to the OIU and/or whether there are errors in the transactions with this device. Note that the MCC W/S display and SM212 both decode the sync state as 0 = NONE, 1 = YES, 2 = NO, and 3 = N/A.
2. Dev bus/RT number - This field consists of 1 byte (8 bits). The first 3 bits indicate the number of the bus that the physical device is on, and the remaining 5 bits indicate the RT number of the physical device. The first 3 bits are found in MSIDs P50U4055D (AD1), P50U4065D (AD2), P50U4075D (AD3), and P50U4085D (AD4). The last 5 bits are MSIDs P50U4056D, P50U4066D, P50U4076D, and P50U4086D.
3. Dev data start byte/OIU RT number, bus - This field consists of two bytes (16 bits). The first 10 bits represent the byte number in the PDI minor frame where the device format ID data starts. The remaining 6 bits indicate the OIU RT address if the OIU is an RT on that bus. The first 10 bits are in MSIDs P50U4058D, P50U4068D, P50U4078D, and P50U4088D for ADs 1-4, respectively. The last 6 bits are in MSIDs P50U4069D, P50U4079D, and P50U4089D.

### 38.6.8.1 BC and RT Block Status Words (Transaction Status Words)

The BC or RT mode Block Status Words (BSW) indicate the **success or failure of individual MS1553B transactions**. They are placed into the PDI stream directly after the set of unconverted transaction data for the device mode. For example, if there were four MS1553B transactions for a given device mode, the block status words would follow the set of transaction data and in the same order as the transactions. There is one special case of a block status word when the OIU is an RT. If there is an error in the MS1553B transaction so severe that it causes the OIU to not receive the transaction or communication with the ISS BC MDM ceases, the value for the block status word becomes 1553h, which indicates a severe error in MS1553B communication. Block

status word values are given in Table 38-5. For all other cases, the bits in the block status words are described in the following paragraphs. The BC mode block status words are described first, then the RT mode block status words.

**Table 38-5. Block Status Word values**

| Bit      | Value | OIU RT mode description     | OIU BC mode description     |
|----------|-------|-----------------------------|-----------------------------|
| (MSB) 15 | 8000  | EOM                         | EOM                         |
| 14       | 4000  | SOM                         | SOM                         |
| 13       | 2000  | Channel B/A*                | Channel B/A*                |
| 12       | 1000  | Error Flag                  | Error Flag                  |
| 11       | 0800  | N/A                         | Status Set                  |
| 10       | 0400  | Format Error                | Format Error                |
| 9        | 0200  | No Response Timeout         | No Response Timeout         |
| 8        | 0100  | Loop Test Fail              | Loop Test Fail              |
| 7        | 0080  | Data Stack Rollover         | N/A                         |
| 6        | 0040  | Illegal Command Word        | N/A                         |
| 5        | 0020  | Word Count Error            | N/A                         |
| 4        | 0010  | Incorrect Sync              | Good Data Block Transfer    |
| 3        | 0008  | N/A                         | Wrong Status Address/No Gap |
| 2        | 0004  | N/A                         | Word Count Error            |
| 1        | 0002  | N/A                         | Incorrect Sync Type         |
| (LSB) 0  | 0001  | Command Word Contents Error | Invalid Word                |

**38.6.8.1.1 BC mode BSW**

1. Bit 15: End of Message (EOM) - Set at the completion of the message regardless of whether or not there were any errors in the message.
2. Bit 14: Start of Message (SOM) - Set at the start of a message and cleared at the end of the message.
3. Bit 13: Channel B/A\* - Is 0 if the message was processed on channel A or 1 if it was processed on channel B.
4. Bit 12: Error Flag - Indicates there was an error in the message. See the lower bits for the exact error.
5. Bit 11: Status Set - Indicates the RT Status Word received from a responding RT contained an incorrect RT address field or one of the lower 11 bits contained an unexpected value.

6. Bit 10: Format Error - Indicates that the message contained one or more violations of the MS1553B message validation criteria (sync, encoding, parity, bit count, word count, etc.).
7. Bit 9: Response Timeout - Indicates the RT has either not responded or has responded later than the BC no response timeout time (50.5 microseconds).
8. Bit 8: Loop Test Fail - A loopback test is performed on the transmitted portion of every message in BC mode. A validity check is performed on the "received version" of every word transmitted by the OIU BIA. In addition, a bit-by-bit comparison is performed on the last word transmitted by the BC for each message. If either the received version or any transmitted word is invalid (sync, encoding, bit count, and/or parity error) and/or the received version of the last word transmitted by the OIU BIA BC does not match the transmitted version, the Loop Test fail bit is set. (This indicates there is something wrong with the OIU BIA for the bus).
9. Bit 7: N/A
10. Bit 6: N/A
11. Bit 5: N/A
12. Bit 4: Good Data Block Transfer - Set to 1 following completion of a valid (error-free) RT-to-BC transfer, or "receive mode code with data" message. This bit is always 0 for a BC-to-RT transfer or a "receive mode code without data" message.
13. Bit 3: Wrong Status Address/No Gap - Set if either or both of the following occur: (1) the RT address field of a responding RT does not match the RT address in the MS1553B command word (2) an RT responds with a response time less than 4 microseconds.
14. Bit 2: Word Count Error - Applicable for RT-to-BC transfers. If set, indicates that a responding RT did not transmit the correct number of data words (too few or too many). Is always 0 for BC-to-RT and "receive mode code" transfers.
15. Bit 1: Incorrect Sync Type - If set, indicates an RT responded with a data sync in a status word and/or a command/status sync in a data word.
16. Bit 0: Invalid Word - Indicates an RT responded with one or more words containing one or more of the following error types: sync field error, Manchester encoding error, parity error, and/or bit count error.

**Table 38-6. BSW representing “good” 1553 transactions**

|                  | Transmit | Receive  |
|------------------|----------|----------|
| <b>Channel A</b> | 8010 hex | 8000 hex |
| <b>Channel B</b> | A010 hex | A000 hex |

Note that when the OIU is BC to an ISS MDM in diagnostic mode, the block status words are usually 9800 hex (when on Channel (CH) A), or B800 hex (when on CH B), because of the ERROR bit being set by the MDM in its responses to the OIU.

### 38.6.8.1.2 RT Mode BSW

1. Bit 15: EOM - Set at the completion of the message regardless of whether or not there were any errors in the message.
2. Bit 14: SOM - Set at the start of a message and cleared at the end of the message.
3. Bit 13: Channel B/A\* - Is 0 if the message was processed on channel A or 1 if it was processed on channel B.
4. Bit 12: Error Flag - Indicates that an error was in the message. See the lower bits for the exact error.
5. Bit 11: N/A
6. Bit 10: Format Error - Indicates that the message contained one or more violations of the MS1553B message validation criteria (sync, encoding, parity, bit count, word count, etc.).
7. Bit 9: N/A
8. Bit 8: Loop Test Fail - A loopback test is performed on the transmitted portion of every message in RT mode. A validity check is performed on the “received version” of every word transmitted by the OIU BIA. In addition, a bit-by-bit comparison is performed on the last word transmitted by the RT for each message. If either the received version of any transmitted word is invalid (sync, encoding, bit count, and/or parity error) and/or the received version of the last word transmitted by the OIU BIA RT does not match the transmitted version, the loop test fail bit is set.

This indicates that something is wrong with the OIU BIA for the bus.

9. Bit 7: N/A
10. Bit 6: N/A

11. Bit 5: Word Count Error - Indicates that the ISS BC MDM did not transmit the correct number of data words, as specified in the MS1553B command word.
12. Bit 4: Incorrect Data Sync - Indicates that the ISS BC MDM transmitted a command sync in a data word.
13. Bit 3: N/A
14. Bit 2: N/A
15. Bit 1: N/A
16. Bit 0: Command Word Contents Error - Indicates that a received command word is not defined in accordance with Mil-Std-1553.

### **38.7 POWER-ON SELF-TEST AND APPLICATION INTIALIZATION**

#### **38.7.1 Power-On Self-Test**

The OIU performs the Power-On Self-Test (POST) immediately after power is applied to the unit. The POST routine runs from one to three times (depending on errors noted in each POST attempt). Any errors noted during each run are logged to the OIU error log. After all POST attempts have completed, the OIU looks for a Ground Support Equipment (GSE) signal from the Ground Support Reconfiguration Application (GSRA). This signal is present if a GSE computer is connected to the serial interface (J6) and is running GSRA. If this signal is detected, the OIU enters monitor mode and starts servicing the GSRA. If this signal is not present, the OIU enters flight mode and begins application initialization.

If any of the following errors occur during POST, they prevent the OIU from entering either monitor or flight mode:

- A. Address error
- B. Bus error
- C. Illegal instruction error
- D. Line 1010 error
- E. Line 1111 error

These errors cause the OIU to halt processing and require a power off/power-on or a system-level reset. If the only errors that occur in the last of three possible attempts at POST are PSP-related, the OIU still enters flight mode. The rationale here is that the OIU can still provide telemetry to the PDI.

POST failures that prevent the OIU from entering flight mode are the BIC POST register error, BIC POST error, BIC POST SRAM error, OCC EEPROM error, OCC register error, OCC SRAM error, Orbiter Interface Card (OIC) PDI CSI error, OIC PDI EEPROM

error, OIC PDI POST incomplete error, OIC PDIU SRAM error, and PDI SRAM access error, but they still provide access to monitor mode. Appendix B of this systems brief provides more details for each error generated during POST, as well as all OIU error telemetry.

### 38.7.2 Application Initialization

Application initialization occurs:

1. Immediately after POST
2. After an OIU configuration command is processed,
3. When the OIU loses sync with an ISS BC or the SSOR.

The flight firmware temporarily halts any ongoing PDI and MS1553B processing to initialize firmware parameters and establish the operating configuration of the OIU. Application initialization includes the following steps:

- A. Reading the reconfiguration data
- B. Initializing the OIU BIAs
- C. Constructing the 100-ms BC frame table for each BC bus
- D. OIU time initialization
- E. OIU and ISS synchronization

These are described in detail in the following sections.

#### 38.7.2.1 Reading the Reconfiguration Data Tables (RDT)

On power up, the Reconfiguration Data Tables are read to obtain basic OIU mission information or default data that apply to all OIU formats, such as how many OIU formats there are for the mission, the default BC/RT assignment of the OIU for each bus, logical/physical device mapping, etc. For all occurrences of application initialization, the reconfiguration data are read to obtain information on how to build the telemetry frames. This information includes the devices the OIU communicates with, subaddresses, number of telemetry data words, parameters selected for bit field extraction or floating point conversions, the location and content of the OIU Health and Status (H&S) parameters, etc. See JSC-27594, User's Guide for the Generation of Reconfiguration Data Tables for the Orbiter Interface Unit, for more detailed information.

#### 38.7.2.2 Reconfiguration Data Tables

The initial bus configuration is defined as part of the Reconfiguration Data Tables (RDT). Upon power-on, the OIU reads the RDT and configures the OIU using these "Default" settings.



The OIU RDTs represent a component of the OIU system that resides in the OCC Electronically Erasable Programmable Read Only Memory (EEPROM). The purpose of the tables is to provide the OIU flight firmware with flight-specific information concerning the following:

- A. OIU hardware connectivity to external devices
- B. Command and data paths to external devices
- C. MS1553B transaction attributes
- D. OIU status parameter specifications
- E. Data conversion specifications
- F. OIU error log dump specifications
- G. OIU-to-PDI telemetry frame construction

The RDT are generated by software called the reconfiguration tool. The Ground Support Reconfiguration Application (at KSC) loads the Reconfiguration Data Tables into the OIU Controller Card (OCC) EEPROM for subsequent use by the OIU firmware.

### **38.7.2.3 Initializing the OIU BIAs**

The OIU BIAs are initialized for BC or RT modes. This step includes initializing configuration registers for capabilities that the OIU needs to use. For RT mode, initialization also includes mapping of the OIU RT BIAs internal data blocks to the OIUs receive, transmit, and broadcast subaddresses. For the buses the OIU is BC on, the OIU BC BIA message blocks are mapped to all RT subaddresses that the OIU will communicate with on that bus for the current OIU format.

### **38.7.2.4 Constructing the 100-ms BC Frame Table for Each BC Bus**

For each bus the OIU is BC on, a table of the cyclic 100 millisecond (ms) frame of MS1553B telemetry transactions and nontelemetry transactions (broadcast sync with data and broadcast time) is built. The BC frames are sent out at the beginning of each 100-ms frame. They are the actual MS1553B commands for telemetry data and the broadcast messages that the OIU sends to the RTs. Transactions for an RT to receive a PSP commands are added into this table on an on-event basis when a PSP command is to be transmitted to a device on the bus.

### **38.7.2.5 Time Initialization**

As part of the application initialization, the OIU firmware sets OIU initial time to PTB time if PTB time can be acquired. If not, OIU internal time either is set to its default value of January 1, 1997, 00:00:00 during power-on or continues to increment from its previous value if initialization resulted from an event other than power-on. Furthermore, jam time (see Section 5.6) and its corresponding values in CCSDS format will be calculated from OIU internal time.

### 38.7.2.6 OIU and ISS Synchronization

If the active OIU format includes an ISS BC or the SSOR, the OIU attempts to get into sync with the BC/SSOR as part of application initialization. The OIU checks for the acquisition of three consecutive frame counts from the device within ten 100-ms processing frames. If the OIU achieves sync with the BC, then the sync code for the BC Active Device (AD) (2 bits of P50M40x0P, where x = 5 for AD1, 6 for AD2, 7 for AD3, and 8 for AD4) is set to 1 (LOCK = YES on SM212 and the OIU Mission Control Center (MCC) Workstation (W/S) display) and application initialization ends. If the OIU cannot achieve sync within ten 100-ms frames, the OIU ISS LOST SYNC error (P50X4283E) is set, the sync code for that active device (2 bits of P50M40x0P, where x = 5 for AD1, 6 for AD2, 7 for AD3, and 8 for AD4) is set to 2 (LOCK=NO on SM212 and the OIU MCC W/S display), interrupts are disabled on the BIA OIU for the bus, and application initialization ends. Subsequent broadcast messages from the Command and Control Multiplexer/Demultiplexer (CCMDM) are ignored. The OIU will not try to get in sync with the BC until application initialization is run again. Note that an OIU format reload causes application initialization to be called up again.

When the OIU is in sync to an ISS BC, all 100-ms processing is driven by receipt of the broadcast sync with data command from the BC. The frame count received with the broadcast command is used by the OIU to drive transactions on other active buses and to build PDI frames. If the OIU cannot get into sync or is in a mode where there is no ISS BC, all 100-ms processing is driven by an internal 100 ms interrupt, and the OIU generates its own frame count.

### 38.7.3 Time Processing

The OIU reads time from the Payload Timing Buffer (PTB) only during application initialization. PTB provides time in the form of ddd/hh/mm/ss. No year is supplied by PTB. Based on the PTB time, the OIU maintains internal time and jam time. Both time values are in the ddd/hh/mm/ss/uuu format. See Table 38-4. Internal time is used for time-stamping error log entries and to derive the jam time. The jam time (P50U) is the same as internal time except for the seconds field and the microseconds field. These fields are calculated to maintain consistency between the time broadcast and frame count. If the OIU is synchronized to an ISS BC, the BC frame count is used. If the OIU is not synchronized to a BC, the OIU-generated frame count is used. The calculation of the values of the seconds field and microseconds field of the jam time is part of the application initialization. The jam time is part of the PDI standard set of OIU H&S parameters and is used to calculate the OIU broadcast time in CCSDS format.

**Table 38-7. Valid time / field values**

| Time field   | Valid range |
|--------------|-------------|
| Days         | 0 - 399     |
| Hours        | 0 - 59      |
| Minutes      | 0 - 59      |
| Seconds      | 0 - 59      |
| Microseconds | 0 - 999999  |

As part of the application initialization, the OIU allows 2.5 seconds to read the PTB time. If the PTB read is successful, the internal time is set to the PTB time. If PTB time cannot be acquired within 2.5 seconds, two possible actions are

- A. If the OIU is processing a power-on application initialization, OIU internal time is set to a default value (1/0/0/0/0), and the jam time is calculated from this default time.
- B. If application initialization is occurring for some reason other than a power-on (e.g., configuration commands or a sync loss), internal time retains its current value and the jam time is calculated from retained internal time.

Jam time is converted into Consultative Committee for Space Data Systems (CCSDS) format for display via OIU telemetry data and for broadcast to MS1553B RTs in active OIU format. The value of the days field is converted into the corresponding month and days, taking leap year into consideration. Since the value of the year, which is not part of the time format described above, is also needed in the CCSDS format, the OIU provides a default year value of 1997. The year value can be changed using the read PTB and year update commands (types 0Ah and 0Bh, covered in Section 38.5.4).

Several error conditions can occur that would prevent a valid time from being received at the PTB interface. These error conditions are provided in the following summary. For all error conditions that prevent a valid PTB signal from being received, the OIU maintains the current internal time and does not reset the time.

The READ PTB command forces the OIU to read time from the PTB interface and to reinitialize. The PTB interface supplies orbiter time to the OIU in the form of ddd/hh/mm/ss/uuu, where ddd is Julian days. The time value for the current year must be specified by a command to the OIU. The command includes 1 bit to indicate the century (19 or 20, actually the 100's of years and not the century) and 7 bits to indicate which year to use. The year must be in the range from 1995 to 2099, inclusive, in order to be valid. In addition, if all 7 bits are high (logical 1), the OIU does not update the year. If the year field contains an invalid number, the INVALID CONFIG COMMAND error (P50X4287E) is set, and the command is rejected.

- A. OIC PTB LOS error (P50X4296E)

This error occurs when OIC does not receive a valid PTB signal transition from the PTB interface within 16 ms. Although OIC keeps trying to sync with PTB, OCC

firmware times out waiting for PTB time from OIC in 2.5 seconds. The timeout results in the PTB time available bit not getting set by OIC, and the PTB NOT AVAILABLE error is set. This bit remains set until the condition is cleared.

B. OIC PTB SYNC error (P50X4295E)

This error condition and effect is similar to the OIC PTB LOS error. The only difference is that this error is caused by OIC not receiving a valid PTB pulse width. This bit remains set until the condition is cleared.

C. OIC PTB TIME error (P50X4282E)

This error condition and effect is also similar to the OIC PTB LOS error. The only difference is that this error is caused by OIC detection of at least one value in the PTB time field that is not valid. This bit remains set until the condition is cleared.

D. PTB NOT AVAILABLE error (P50X4308E)

For the 2.5-second period, if OCC firmware cannot verify that the PTB available bit is set by OIC, either because the bit has not been set or because OCC firmware cannot access PSP/PTB SRAM, OCC firmware set the PTB NOT AVAILABLE error bit in H&S. This bit remains set until the condition is cleared when the next command to read PTB time is successful.

#### 38.7.4 Talkback Indicator

The OIU provides a +28 V dc signal to the orbiter Standard Switch Panel (SSP) to power an SSP talkback. OIUs 1 and 2 use the same talkback, with OFF = barberpole, OIU 1 ON = UP, and OIU 2 ON = DOWN. There is a panel overlay on the SSP with the above decoder ring for crew use.

This signal is not provided on FEUs or engineering units if one of these nonflight OIU types is encountered in Shuttle Avionics Integration Laboratory (SAIL) testing.

### 38.8 ERROR LOG

#### 38.8.1 Error Log Structure

The OIU error log processing is performed at the end of every 100-ms processing frame. A comparison is made between the current internal error section of the OIU error status bytes and the internal error section of the previous 100-ms frame. These status bytes are discussed in Section 38.8 and defined in Appendix B. If there is no change, no action is taken. But if there is any change, the internal error section (the first 7 bytes) of the current error status bytes is written to the EEPROM error log with the current OIU time. This process provides logging of each occurrence of an error event or clearance of an error event and protection from continuous logging of the same event.

Table 38-8 depicts the structure of the OIU error log. A total of 100 entries are in the OIU error log. The starting address of entry number 1 is C10000h, and the starting

address of entry 100 is C10630h. Each entry consists of 16 bytes. When a Wraparound (WRAP) occurs, entry number 11 is the beginning entry of the WRAP location. Address C10640h contains the WRAP indicator. Whenever this bit is set, it means that error log WRAP has occurred. Address C10642h is the starting address of the WRAP counter. The contents of the WRAP counter represent how many times the error log has wrapped.

Each EEPROM location is limited to 10,000 writes. The value of the WRAP counter indicates the largest number of writes that have occurred at any location in the error log.

**Table 38-8. OIU error log EEPROM memory locations**

| Entry number | Starting address (hex) | Error data             | Notes   |
|--------------|------------------------|------------------------|---|
| 1            | C10000                 | 16 bytes error data    |   |
| 2            | C10010                 | 16 bytes error data    |   |
| 3            | C10020                 | 16 bytes error data    |   |
| •            | •                      | 16 bytes error data    |   |
| •            | •                      | 16 bytes error data    |   |
| •            | •                      | 16 bytes error data    |   |
| 11           | C100A0                 | 16 bytes error data    | ← Wrap location (save the first 10 errors and the last 90 errors) |
| 12           | C100B0                 | 16 bytes error data    |   |
| •            | •                      | 16 bytes error data    |   |
| •            | •                      | 16 bytes error data    |   |
| •            | •                      | 16 bytes error data    |   |
| 98           | C10610                 | 16 bytes error data    |   |
| 99           | C10620                 | 16 bytes error data    |   |
| 100          | C10630                 | 16 bytes error data    |   |
|              | C10640                 | Wrap indicator (1 bit) |   |
|              | C10642                 | Wrap counter(16 bits)  |   |

The meaning of the contents of the 16 bytes for each entry is presented in Table 38-10. The value of bit 0 of the first byte of each error log entry is used by OCC firmware to determine the starting entry for each power-on. The next 7 bytes are used for a time stamp for each entry. The days field and milliseconds field require 2 bytes each. Bytes 9 to 15 represent the internal error section of the error status bytes. The last byte is reserved.

**38.8.2 Error Log Dump via PDI Output**

The contents of the OIU error log can be dumped using either the GSRA or the PDI output. The method for dumping the error log using the GSRA is described in the User’s Guide for the Ground Support Reconfiguration Application of the Orbiter Interface Unit.

The error log can also be dumped using the PDI output. In some OIU formats, the error log is included in the OIU output stream (format 254 is one). The telemetry stream may contain only the error log dump, or it may include MS1553B device data as well, as specified by format definitions in the reconfiguration data.

Identification of the beginning of an error log dump in the PDI output stream is via a special error log sync pattern, BBCCDDEEh. Following the sync pattern, a 16-bit word contains the number of bytes in the error log dump (1612 bytes). The next 16-bit word contains the number of bytes of error log dump per OIU output frame (the size of the dump window).

The error log itself follows these overhead data. The error log dump is written in successive PDI frames. Once it is finished, the dump begins again in a new PDI frame, with the sync pattern always at the beginning of the dump window. The dump may end prior to the end of the dump window in the final frame of the dump.

The number of bytes in the error log and the size of the dump window determine the end location of the error log dump data. Note that there is no way at present to process this error log dump in the MCC, nor are any MSIDs assigned by recon to the error log bytes in the PDI stream.

*Table 38-9. OCC error log data format*

| OCC address | Bit 7  | Bit 6 | Bit 5 | Bit 4                 | Bit 3 | Bit 2 | Bit 1 | Bit 0        |
|-------------|--------|-------|-------|-----------------------|-------|-------|-------|--------------|
| C10000      |        |       |       |                       |       |       |       | Entry Search |
| C10001      | <----- | ----- | ----- | Days field (1)        | ----- | ----- | ----- | ----->       |
| C10002      | <----- | ----- | ----- | Days field (2)        | ----- | ----- | ----- | ----->       |
| C10003      | <----- | ----- | ----- | Hours                 | ----- | ----- | ----- | ----->       |
| C10004      | <----- | ----- | ----- | Minutes               | ----- | ----- | ----- | ----->       |
| C10005      | <----- | ----- | ----- | Seconds               | ----- | ----- | ----- | ----->       |
| C10006      | <----- | ----- | ----- | msecs (1)             | ----- | ----- | ----- | ----->       |
| C10007      | <----- | ----- | ----- | msecs (2)             | ----- | ----- | ----- | ----->       |
| C10008      | <----- | ----- | ----- | Error status byte (0) | ----- | ----- | ----- | ----->       |
| C10009      | <----- | ----- | ----- | Error status byte (1) | ----- | ----- | ----- | ----->       |
| C1000A      | <----- | ----- | ----- | Error status byte (2) | ----- | ----- | ----- | ----->       |
| C1000B      | <----- | ----- | ----- | Error status byte (3) | ----- | ----- | ----- | ----->       |
| C1000C      | <----- | ----- | ----- | Error status byte (4) | ----- | ----- | ----- | ----->       |
| C1000D      | <----- | ----- | ----- | Error status byte (5) | ----- | ----- | ----- | ----->       |
| C1000E      | <----- | ----- | ----- | Error status byte (6) | ----- | ----- | ----- | ----->       |
| C1000F      | <----- | ----- | ----- | Reserved              | ----- | ----- | ----- | ----->       |

### 38.8.3 Error Signatures

When PTB time is not available OIU firmware attempts to initialize or reset its internal time using PTB time. During power-on, if PTB time is not available, OIU firmware sets its internal time to a default value. When PTB time is not available during application initialization for reasons other than power-on, such as resynchronization or configuration command processing, the OIU internal time is incremented from its previous value instead of being reset to PTB time. Because the PTB not available error is defined as

an external error, it is not logged in the error log. Instead, this error is reported in the corresponding bit in the error status bytes in the PDI stream. The value of this bit remains 1 until a valid PTB time is received.

For MS1553B transaction error signatures, see Section 38.9.5.1, BC and RT Status Words. Whenever an invalid OIU configuration command is sent to the OIU, the invalid configuration command error is generated in OIU status.

If the ISS BC or SSOR loses sync with the OIU, the corresponding sync status flags in OIU status will change from 1 (YES) to 2 (NO).

A PDI decom loss of word sync is expected when the OIU is commanded to change OIU formats. If the ISS BC stops communicating with the OIU, there is a PDI decom word sync loss until the OIU reinitializes and goes to internal time.

If a PSP command is unable to reach an RT (OIU is BC), the OIU retransmits this command on the same channel (first retry). If it fails, the OIU retransmits this command again (second retry) on the alternate channel.

If the second retry also failed, the PSP retries failed error (P50X4291E) is annunciated.

If the byte count received is outside of this range, the PSP BYTE COUNT flag (P50X4303E) is set.

If the parity check fails, the PSP PARITY error (P50X4281E) is set.

If the OIU detects a loss of the PSP carrier signal, the PSP Loss of Sync (LOS) error flag (P50X4283E) is set.

If the OIU receives three PSP commands before one has been processed, a CMD CNT OB ERR (command count out of bounds error, P50X4292E) is set.

If both OIC command buffers are full when the OIC attempts to store a new command, the PSP SYNC ERROR (P50X4284E) is set and the command is lost.

The reconfiguration table maps valid routing codes to the logical device that will process the command. If the RC does not match, the UNIMPLEMENTED RC ERR (P50X4306E) is set.

**UNIMPLEMENTED RC ERROR (P50U4306E):** The command contains an unrecognized routing code. The OIU rejects the command.

**PSP RETRIES FAILED (P50X4291E):** The OIU made three attempts to transmit a command to an RT. All three attempts failed. The OIU rejects the command.

If all three attempts fail, the (PSP RETRIES FAILED) error flag is set in telemetry. This bit is cleared after 100 milliseconds; so it may not be noticed.

If, for some reason, the ISS BC MDM stops transmitting MS1553B transactions, a PDI sync loss occurs and the ISS BC NO COMM STATUS error (P50X4286E) is set.



If errors occurred during floating point conversion, the converted parameter is set to either 0 or 255, depending on the types of errors, and the (floating point conversion err) is set in the OIU H&S. This error is cleared in the next frame.

#### 38.8.4 Nonconsecutive Frame Indicator

After the OIU is in sync with the CCMDM or the SSOR, it checks the frame count in each minor frame received from the CCMDM or SSOR for consecutive frame counts. When the frame count does not increment correctly in two or more consecutive frames, the OIU declares that sync has been lost and returns to Application Initialization. In the case where there is only one frame count discontinuity, the OIU continues program execution. However, depending on the device, either an ISS frame nonconsecutive error or an SSOR frame nonconsecutive error is entered in the error status bytes. Furthermore, in the PDI frame where the nonconsecutive frame count occurred, the MSB in frame byte 11 (nonconsecutive frame indicator) is set to 1, which indicates that the contents of the frame maybe erroneous.

#### 38.9 ACRONYMS

|        |   |
|--------|---|
| AD     | Active Device   |
| AMS    | Amplifier System                                      |
| BC     | Bus Controller  |
| BIA    | Bus Interface Adapter                                 |
| BIC    | Bus Interface Controller                              |
| C&DH   | Command and Data Handling                             |
| CCMDM  | Command and Control MDM                               |
| CCSDS  | Consultative Committee for Space Data Systems         |
| COTS   | Commercial Off-The-Shelf                              |
| CPU    | Central Processing Unit                               |
| DMA    | Direct Memory Access                                  |
| EEPROM | Electronically Erasable Programmable Read-Only Memory |
| EOM    | End of Message  |
| ESD    | Electrostatic Discharge                               |
| ETI    | Elapsed Time Indicator                                |
| EU     | Engineering Unit                                      |
| FCOH   | Flight Control Operations Handbook                    |
| FDA    | Fault Detection and Annunciation                      |
| FEU    | Functional Equivalent Unit                            |
| FGB    | Russian Functional Cargo Block (first ISS element)    |

---

|        |  |
|--------|--|
| GNC    | Guidance, Navigation, and Control                |
| GPC    | General Purpose Computer                         |
| GSE    | Ground Support Equipment                         |
| GSRA   | Ground Support Configuration Application         |
| H&S    | Health and Status                                |
| ICD    | Interface Control Document                       |
| ID     | Identification                                   |
| IEEE   | Institute of Electrical and Electronic Engineers |
| IRIG-B | Interrange Instrumentation Group B               |
| ISS    | International Space Station                      |
| LOS    | Loss of Sync                                     |
| LSB    | Least Significant Bit<br>Least Significant Byte  |
| MCC    | Mission Control Center                           |
| MDM    | Multiplexer/Demultiplexer                        |
| MIP    | Mission Integration Plan                         |
| MPLM   | Mini Pressurized Logistics Module                |
| MRTC   | Multiple Real-Time Command                       |
| ms     | milliseconds                                     |
| MSB    | Most Significant Bit<br>Most Significant Byte    |
| MSID   | Measurement Stimulation Identifications          |
| OCC    | OIU Controller Card                              |
| OIC    | Orbiter Interface Card                           |
| OIU    | Orbiter Interface Unit                           |
| ORU    | Orbit Replaceable Unit                           |
| PDI    | Payload Data Interleaver                         |
| PDIP   | Payload Data Interface Panel                     |
| PF     |  |
| PL     | Payload  |
| POST   | Power-On Self-Test                               |
| PSP    | Payload Signal Processor                         |
| PTB    | Payload Timing Buffer                            |
| RAM    | Random Access Memory                             |
| RC     | Routing Code                                     |
| RT     | Remote Terminal                                  |

SM Systems Management  
 SOM Start of Message  
 SRAM Static Random Access Memory  
 SSOR Space-to-Space Orbiter Radio  
 SSP Standard Switch Panel  
  
 T/R Transmit/Receive  
  
 W/S Workstation  
 WRAP Wraparound

**38.10 REFERENCES**

- A. Shuttle Orbiter/OIU Cargo Element Interfaces, ICD-A-21264.
- B. Program Requirement Document for the Orbiter Interface Unit (OIU), JSC-26543.
- C. User’s Guide for the Ground Support Reconfiguration Application of the Orbiter Interface Unit, JSC-27270.
- D. Software Design Document for the Flight Software CSCI of the Orbiter Interface Unit, JSC-27267.
- E. The Orbiter Interface Unit (OIU) Detailed Design Specification, JSC-27293.
- F. User’s Guide for the Generation of Reconfiguration Data Tables for the Orbiter Interface Unit, JSC-27594.
- G. Shuttle Orbiter/Station IDD Cargo Element Interfaces, NSTS-21000-IDD-ISS.
- H. OIU Assembly Drawing, SED391269.

**38.11 APPENDIX**

**Table 38-10. Flight/prototype pin assignments**

| Interface             | Power<br>NB7E10-6SNT | Talkback<br>NLS7T10-35SA | PSDP I/F<br>NLST12-35SN | MS1553B CH-A<br>NLS7T14-35SA | MS1553B CH-B<br>NLS7T14-35SN | PDIP I/F<br>NLS7T12-35SA |
|-----------------------|----------------------|--------------------------|-------------------------|------------------------------|------------------------------|--------------------------|
| Insert<br>Designation | (J1)<br>(6 pin)      | (J2)<br>(13 pin)         | (J3)<br>(22 pin)        | (J4)<br>(37 pin)             | (J5)<br>(37 pin)             | (J6)<br>(22 pin)         |
| 1/A                   |                      |                          |                         | 1_BUS1A+                     | 1_BUS1B+                     | PSP_TX                   |
| 2/B                   | 28 V DC              |                          | MDM+                    |                              |                              |                          |
| 3/C                   |                      | Talkback +               |                         | 1_BUS1A-                     | 1_BUS1B-                     | PSP_RX                   |
| 4/D                   |                      |                          |                         |                              |                              |                          |
| 5/E                   | RTN                  |                          |                         |                              |                              | PSP_GND                  |

**Table 38-10. Flight/prototype pin assignments (concluded)**

| Interface | Power<br>NB7E10-6SNT | Talkback<br>NLS7T10-35SA | PSDP I/F<br>NLST12-35SN | MS1553B CH-A<br>NLS7T14-35SA | MS1553B CH-B<br>NLS7T14-35SN | PDIP I/F<br>NLS7T12-35SA |
|-----------|----------------------|--------------------------|-------------------------|------------------------------|------------------------------|--------------------------|
| 6/F       |                      |                          | PDI+                    |                              |                              | OIC_RESET                |
| 7         |                      |                          |                         |                              |                              | OCC_DEBUG                |
| 8         |                      |                          | PTB+                    |                              |                              |                          |
| 9         |                      | Talkback +               |                         |                              |                              | OCC_TXA                  |
| 10        |                      |                          | MDM-                    |                              |                              | PDI_DEBUG                |
| 11        |                      |                          |                         | 1_BUS2A+                     | 1_BUS2B+                     | OCC_RXA                  |
| 12        |                      |                          | PDI-                    |                              |                              |                          |
| 13        |                      |                          |                         | 1_BUS2A-                     | 1_BUS2B+                     | OCC_GND                  |
| 14        |                      |                          | PTB-                    |                              |                              | PSP_DEBUG                |
| 15        |                      |                          |                         |                              |                              | PDI_TX                   |
| 16        |                      |                          |                         |                              |                              |                          |
| 17        |                      |                          |                         |                              |                              | PDI_RX                   |
| 18        |                      |                          |                         |                              |                              |                          |
| 19        |                      |                          |                         |                              |                              | PDI_GND                  |
| 20        |                      |                          |                         |                              |                              |                          |
| 21        |                      |                          |                         | 1_BUS3A+                     | 1_BUS3B+                     | OIU_RESET                |
| 22        |                      |                          | PSP-                    |                              |                              |                          |
| 23        |                      |                          |                         | 1_BUS3A-                     | 1_BUS3B-                     |                          |
| 24        |                      |                          |                         |                              |                              |                          |
| 25        |                      |                          |                         |                              |                              |                          |
| 26        |                      |                          |                         |                              |                              |                          |
| 27        |                      |                          |                         |                              |                              |                          |
| 28        |                      |                          |                         |                              |                              |                          |
| 29        |                      |                          |                         |                              |                              |                          |
| 30        |                      |                          |                         |                              |                              |                          |
| 31        |                      |                          |                         | 1_BUS4A+                     | 1_BUS4B+                     |                          |
| 32        |                      |                          |                         |                              |                              |                          |
| 33        |                      |                          |                         | 1_BUS4A-                     | 1_BUS4B-                     |                          |
| 34        |                      |                          |                         |                              |                              |                          |
| 35        |                      |                          |                         |                              |                              |                          |
| 36        |                      |                          |                         |                              |                              |                          |
| 37        |                      |                          |                         |                              |                              |                          |

**Table 38-11. OIU error telemetry matrix**

| Value | Word1                    | Word2                   | Word3                   | Word4                     | Word5                     | Value |
|-------|--------------------------|-------------------------|-------------------------|---------------------------|---------------------------|-------|
|       | Byte 0 Byte 1            | Byte 2 Byte 3           | Byte 4 Byte 5           | Byte 6 Byte 7             | Byte 8 Byte 9             |       |
| 0100  | Address                  | No PSP Command          | OIC PSP Interrupt       | TRAP V                    | OIC PSP PTB Health        | 0100  |
| 0200  | BIC Post Register        | OCC EEPROM              | OIC PSP Post *          | TRAP X                    | OIC PSP Sync              | 0200  |
| 0400  | BIC Post Self-Test       | Reserved                | OIC PSP Post incomplete | Uninit interrupt vector   | OIC PTB LOS               | 0400  |
| 0800  | BIC Post SRAM            | OCC Register            | OIC PSP SRAM *          | Unused exception          | OIC PTB Sync              | 0800  |
| 1000  | Bus                      | OCC SRAM                | OIU RT on multiple bus  | Zero divide               | OIU ISS Lost Sync         | 1000  |
| 2000  | Check instruction        | OIC PDI ARB             | Reserved                | Reserved                  | OIU SSOR Lost Sync        | 2000  |
| 4000  | Frame Overrun            | OIC PDI C51 *           | PDI SRAM access         | Reserved                  | Cmd Cnt out of bounds *   | 4000  |
| 8000  | Illegal instruction      | OIC PDI EEPROM *        | PDI SRAM Read/write     | Reserved                  | CMD retries failed        | 8000  |
| 0001  | Invalid BIC1 Interrupt   | OIC PDI Interrupt *     | Privilege Violation     | Floating point conversion | PTB not available *       | 0001  |
| 0002  | Invalid BIC2 Interrupt   | OIC PDI Post *          | CMD in Wrong buffer     | Invalid config cmd *      | Unfinished BC Frame       | 0002  |
| 0004  | Invalid Duart Interrupt  | OIC PDI Post incomplete | PSP/PTB SRAM access     | ISS BC No Comm Status     | Unimplemented RC *        | 0004  |
| 0008  | Invalid GSE              | OIC PDI SRAM *          | PSP SRAM Read/write     | Reserved                  | SSOR frame nonconsecutive | 0008  |
| 0010  | Level 7 Autovector       | OIC PDI Wrap *          | Recon EEPROM faulty     | OIC PDI Sync *            | ISS frame nonconsecutive  | 0010  |
| 0020  | Line 1010                | OIC PSP ARB             | Recon # trans subframe  | OIC PSP LOS err *         | OIC PSP byte count *      | 0020  |
| 0040  | Line 1111                | OIC PSP C51 *           | Spurious interrupt      | OIC PTB time *            | PDI buffer not clear      | 0040  |
| 0080  | MAX Error Log Write Wait | OIC PSP EEPROM *        | Trace                   | OIC PSP Parity error *    | Reserved                  | 0080  |

In Error Log. \* Stays set until condition is cleared.

**Note: The MSIDs listed below are for the STS-88/2A mission and should not change from mission to mission.**

| Error name and MSID/<br>(parent MSID)             | MCC/(SPEC 212)<br>display name | How is error condition determined?   | How is error reported?   | What is error's impact?   |
|---|--------------------------------|--|--|---|
| ADDRESS ERROR<br>P50X4218E (P50M4210P)            |                                | The address error exception is generated when the processor attempts to access a word or longword operand or an instruction at an odd address (possibly due to code corruption)  | Log the error in the EEPROM error log immediately  | A STOP instruction is executed to halt the processor until the processor is reset (power cycle) because the contents of the Program Counter are indeterminate                                     |
| BIC POST REGISTER ERROR<br>P50X4217E (P50M4210P)  |                                | OIU firmware determines that BIC register contents do not equal expected values (i.e., what they should be after initialization)   | Error code is generated when it occurs, to be logged to OIU EEPROM error log   | OIU fails POST, and SC_System_Startup will issue RESET instruction and reattempt POST for all 3 cards; max 3 POST attempts, then the watchdog timer halts the OCC (power cycle required to reset) |
| BIC POST SELF TEST ERROR<br>P50X4216E (P50M4210P) |                                | OIU firmware detects a self-test failure for any one of the 4 BIAs   | Error code is generated when it occurs, to be logged to OIU EEPROM error log   | OIU fails POST, and OIU will RESET instruction and reattempt POST; max 3 POST attempts, then system halts   |
| BIC POST SRAM ERROR<br>P50X4215E (P50M4210E)      |                                | OIU firmware determines that BIC SRAM contents do not equal expected values (i.e., what they should be after initialization)   | Error code is generated when it occurs, to be logged to OIU EEPROM error log   | OIU fails POST, and SC_System_Startup will issue RESET instruction and reattempt POST for all 3 cards; max 3 POST attempts, then WDT halts system   |
| BUS ERROR<br>P50X4214E (P50M4210P)                |                                | When an external read/write times out  | The exception handler, EP_Bus_Error_SR, is invoked and it calls the Utility CSUs to generate and log the error in the EEPROM error log immediately | A STOP instruction is executed to halt the processor until the processor is reset (power cycle) because the contents of the Program Counter are indeterminate                                     |
| CHECK INSTR ERROR<br>P50X4213E (P50M4210P)        |                                | The Check Instruction exception is generated when the Check Register Against Bounds instruction fails; however, Check Instruction not used in current design, therefore possibly generated due to code corruption or rad hit | To be logged in the EEPROM error log later   | Increment System Error Counter* and normal processing resumes   |

| Error name and MSID/<br>(parent MSID)          | MCC/(SPEC 212)<br>display name | How is error condition determined?  | How is error reported?  | What is error's impact?   |
|--|--------------------------------|---|---|---|
| FRAME_OVERRUN_ERR<br>P50X4212E (P50M4210P)     |                                | The OIU firmware has detected a 100 ms processing frame overrun (i.e., it has taken OIU longer than 100 ms to get all its work done)  | To be logged later by EXE_Schedule_Modules  | OIU FSW attempts to catch up within the next 100 ms   |
| ILL_INSTR_ERR<br>P50X4211E (P50M4210P)         |                                | The Illegal Instruction exception is generated when the processor fetches an instruction that does not match any legal instruction patterns, therefore possibly generated due to code corruption or rad hit | The exception handler, EP_Illegal_Instruction_SR, is invoked and it calls the Utility CSUs to generate and log the error in the EEPROM error log immediately  | Since the processor restores the Program Counter value to point to the offending instruction, if processing were allowed to return from the exception, this exception would continuously occur; therefore, a STOP instruction is executed to halt the processor |
| INVALID_BIC1_INTR_ERR<br>P50X4228E (P50M4220P) |                                | The autovector associated with the BIC1 interrupt has been generated for an invalid reason (i.e., NOT a "Broadcast Sync With Data" 100 ms interrupt)  | EP_BIC1_Autovector_SR calls the Utility to generate the error code, to be logged later  | Increment System Error Counter*, do NOT set the run_exe_flag; otherwise, normal processing resumes  |
| INVALID_BIC2_INTR_ERR<br>P50X4227E (P50M4220P) |                                | The autovector associated with the BIC2 interrupt has been generated -<br>Note: There is no BIC2 installed in the OIU   | EP_BIC2_Autovector_SR calls the Utility to generate the error code, to be logged later  | Increment System Error Counter* and normal processing resumes   |
| INVALID_DUART_INTR_ERR<br>P504226E (P50M4220P) |                                | The DUART interrupt is associated with the level 2 autovector; however, DUART interrupts are not used in current design; therefore, possibly generated due to problem with serial port or timers            | The exception handler, EP_DUART_Autovector_SR, is invoked and it calls the Utility CSU to generate the error code, to be logged in the EEPROM error log later | Increment System Error Counter*; Disable interrupts at level 2 and below (this "disabling" good only while in same config; if rerun APP Init and enable all interrupts, this exception should be expected again); normal processing resumes                     |
| INVALID_GSE Err<br>P50X4225E (P50M4220P)       |                                | SC_GSE_Handshake detects invalid handshake, or no handshake, when GSE connection has been detected during system startup  | Error code is generated and logged to OIU EEPROM error log once for each attempt (max 3) at handshake   | OIU FSW enters flight mode, as long as POST completed successfully; if not, a STOP instruction is executed  |

| Error name and MSID/<br>(parent MSID)                 | MCC/(SPEC 212)<br>display name | How is error condition determined?   | How is error reported?   | What is error's impact?   |
|---|--------------------------------|--|--|---|
| LEVEL_7_AUTOV_ERR<br>P50X4224E (P50M4220P)            |                                | The Level 7 Auto vector interrupt is not used by the FSW (or even implemented in h/w) therefore if the Level_7_Autovector_SR is invoked, this is possibly due to code corruption or rad hit  | EP_Level_7_Autovector_SR calls the Utility CSU to generate the error code, to be logged in the EEPROM error log later                    | Increment System Error Counter* and normal processing resumes   |
| LINE_1010_ERR<br>P50X4223E (P50M4220P)                |                                | The Line 1010 Emulator exception is generated when the processor recognizes the 1010 bit pattern within the instruction; however, this instruction is not used by the FSW, therefore, possibly generated due to code corruption or rad hit | The exception handler, EP_Line_1010_Emulator_SR, is invoked and it calls the Utility CSUs to generate and log the error code immediately | Since the processor restores the Program Counter value to point to the offending instruction, if processing were allowed to return from the exception, this exception would continuously occur; therefore a STOP instruction is executed to halt the processor  |
| LINE_1111_ERR<br>P50X4222E (P50M4220P)                |                                | The Line 1111 Emulator exception is generated when the processor recognizes the 1111 bit pattern within the instruction; however, this instruction is not used by the FSW; therefore, possibly generated due to code corruption or rad hit | The exception handler, EP_Line_1111_Emulator_SR, is invoked and it calls the Utility CSUs to generate and log the error code immediately | Since the processor restores the Program Counter value to point to the offending instruction, if processing were allowed to return from the exception, this exception would continuously occur; therefore, a STOP instruction is executed to halt the processor |
| Max Error Log Write Wait Err<br>P50X4221E (P50M4220P) |                                | PSP_Modified_Recon_EEPROM or UTL_Log_Errors detects the max. time to complete EEPROM write has been exceeded   | Error code is generated, and logging to OIU EEPROM error log is attempted  | Normal processing resumes   |
| No PSP Command Err<br>P50X4238E (P50M4230P)           |                                | OCC received interrupt, but PSP_Read_PSP_Cmd sees both OIC PSP/PTB register data received bits as 0, indicating there is no PSP cmd  | Error code is generated when it occurs, to be sent in OIU status and logged to OIU EEPROM error log at the end of the 100-ms cycle       | Normal processing continues   |
| OCC_EEPROM_ERR<br>P50X4237E (P50M4230P)               |                                | SC_OCC_EEPROM_Test reads an invalid value from any one of three EEPROM banks in OCC during POST  | Error code is generated when it occurs, to be logged to OIU EEPROM error log when OIU POST attempt is complete                           | OIU fails POST, and SC_System_Startup will issue RESET instruction and reattempt POST for all 3 cards; max 3 POST attempts, then WDT halts system   |



| Error name and MSID/<br>(parent MSID)       | MCC/(SPEC 212)<br>display name | How is error condition determined?   | How is error reported?  | What is error's impact?  |
|---|--------------------------------|--|---|--|
| OCC_REGISTER_ERR<br>P50X4235E (P50M4230P)   |                                | SC_OCC_CPU_Register_Test encounters problem reading/writing to/from OCC CPU Register(s) during POST  | Error code is generated when it occurs, to be logged to OIU EEPROM error log when OIU POST attempt is complete  | OIU fails POST, and SC_System_Startup will issue RESET instruction and reattempt POST for all 3 cards; max 3 POST attempts, then WDT halts system  |
| OCC_SRAM_ERR<br>P50X4234E (P50M4230P)       |                                | SC_OCC_SRAM_Test encounters problem reading/writing to/from OCC SRAM during POST   | Error code is generated when it occurs, to be logged to OIU EEPROM error log when OIU POST attempt is complete  | OIU fails POST, and SC_System_Startup will issue RESET instruction and reattempt POST for all 3 cards; max 3 POST attempts, then WDT halts system  |
| OIC PDI ARB Err<br>P50X4233E (P50M4230P)    |                                | OIC-detected PDI ARB error (i.e., PDI SRAM)<br>Request for Request for shared SRAM not granted within 30 ms  | If during POST, error code is generated when it occurs, to be logged to OIU EEPROM error log when OIU POST attempt is complete; otherwise, UTL_Process_OIU_Health calls the Utility CSCs to generate the error code and to log the error in OIU error log at end of 100mw cycle | OIU does Not fail POST; normal processing resumes.<br>OIC PDI remains active until data run out, then a OCC SYNC ERR will occur, and the OIC will wait until SRAM access is granted to recover. Note: When access is restored, any number of frames will be lost |
| OIC_PDI_C51_ERR<br>P50X4232E (P50M4230P)    |                                | SC_Verify_OIC_POST forwards OIC_detected PDI C51 error (i.e., During independent PDI POST, a specified value is written to an internal C51 register. A read is done to verify the value is set. If the read back fails, then this error condition is flagged). | Error code is generated when detected, to be logged to OIU EEPROM error log when OIU POST attempt is complete   | OIU fails POST, and SC_System_Startup will issue RESET instruction and reattempt POST for all 3 cards; max 3 POST attempts, then WDT halts system  |
| OIC_PDI_EEPROM_ERR<br>P50X4231E (P50M4230P) |                                | SC_Verify_OIC_POST forwards OIC-detected PDI EEPROM error (i.e., During independent PDI Post, the power-on SRAM checksum does not match the checksum stored in EEPROM)   | Error code is generated when detected, to be logged to OIU EEPROM error log when OIU POST attempt is complete   | OIU fails POST, and SC_System_Startup will issue RESET instruction and reattempt POST for all 3 cards; max 3 POST attempts, then WDT halts system  |

| Error name and MSID/<br>(parent MSID)            | MCC/(SPEC 212)<br>display name | How is error condition determined?   | How is error reported?  | What is error's impact?  |
|--|--------------------------------|--|---|--|
| OIC PDI Interrupt Err<br>P50X4248E (P50M4240P)   |                                | OIC-detected PDI INTR error (i.e., an invalid PDI80C51FC interrupt has occurred; INTR service routines exist for all possible interrupts, and this is an unused INTR | If during POST, error code is generated when it occurs, to be logged to OIU EEPROM error log when OIU POST attempt is complete; otherwise, UTL_Process_OIU_Health calls the Utility CSCs to generate the error code, and to log the error in OCC error log at end of 100-ms cycle | OIU does NOT fail POST; normal processing resumes  |
| OIC_PDI_POST_ERR<br>P50X4247E (P50M4240P)        |                                | SC_Verify_OIC_POST forwards OIC-detected POST error for PDI (i.e., Occurs when any OIC PDI error happens during POST)  | Error code is generated when detected, to be logged to OIU EEPROM error log when OIU POST attempt is complete   | OIU does not fail POST; normal processing resumes  |
| OIC_PDI_POST Incomplete<br>P50X4246E (P50M4240P) |                                | SC_Verify_OIC_POST detects OIC did not complete POST for PDI (i.e., OIC PDI POST complete bit not set)   | Error code is generated when detected, to be logged to OIU EEPROM error log when OIU POST attempt is complete   | OIU fails POST, and SC_System_Startup will issue RESET instruction and reattempt POST for all 3 cards; max 3 POST attempts, then WDT halts system  |
| OIC_PDI_SRAM_ERR<br>P50X4245E (P50M4240P)        |                                | SC_Verify_OIC_POST forwards OIC-detected PDI SRAM error (i.e., POST values written to SRAM do not match values read from SRAM)                                       | Error code is generated when detected, to be logged to OIU EEPROM error log when OIU POST attempt is complete   | OIU fails POST, and SC_System_Startup will issue RESET instruction and reattempt POST for all 3 cards; max 3 POST attempts, then WDT halts system  |
| OIC PDI Wrap Err<br>P50X4244E (P50M4240P)        |                                | SC_Verify_OIC_POST and UTL_Process_OIU_Health forward OIC-detected PDI Wrap error (Test compares data read from shared SRAM and data read back from PDI data stream) | If during POST, error code is generated when it occurs, to be logged to OIU EEPROM error log when OIU POST attempt is complete; otherwise UTL_Process_OIU_Health calls the Utility CSCs to generate the error code, and to log the error in OIU error log at end of 100-ms cycle  | If during POST, OIU does NOT fail POST; normal processing resumes. Otherwise, normal processing continues except that WRAP test no longer executed |

| Error name and MSID/<br>(parent MSID)          | MCC/(SPEC 212)<br>display name | How is error condition determined?   | How is error reported?   | What is error's impact?  |
|--|--------------------------------|--|--|--|
| OIC PSP ARB Err<br>P50X4243E (P50M4240P)       |                                | SC_Verify_OIC_POST and UTL_Process_OIU_Health forward OIC-detected PSP ARB error (PSP request for shared SRAM not granted within 30 ms)  | If during POST, error code is generated when it occurs, to be logged to OIU EEPROM error log when OIU POST attempt is complete; otherwise, UTL_Process_OIU_Health calls the Utility CSCs to generate the error code and to log the error in OIU error log at end of 100-ms cycle     | If during POST, OIU does NOT fail POST; Normal processing resumes. Otherwise, OIC PSP/PTB remains inactive until SRAM occurs granted. Note: PSP/PTB time spent. Attempting to get SRAM access may result in any number of timing-related errors. |
| OIC_PSP_C51_ERR<br>P50X4242E (P50M4240P)       |                                | SC_Verify_OIC_POST forwards OIC-POST detected PSP C51 error (i.e., PSP until a specified value to C51 register and read back - IF value read back is different, this error results)                                | Error code is generated when it occurs, to be logged to OIU EEPROM error log when OIU POST attempt is complete   | If during POST, OIU fails POST, and SC_System_Startup will issue RESET instruction and reattempt POST for all 3 cards; max 3 POST attempts, then WDT halts system  |
| OIC_PSP_EEPROM_ERR<br>P50X4241E (P50M4240P)    |                                | SC_Verify_OIC_POST forwards OIC-detected PSP EEPROM error (power-on SRAM checksum does not match the checksum stored in OIC EEPROM)  | Error code is generated when detected, to be logged to OIU EEPROM error log when OIU POST attempt is complete  | If during POST, OIU fails POST, and SC_System_Startup will issue RESET instruction and reattempt POST for all 3 cards; max 3 POST attempts, then WDT halts system  |
| OIC PSP Interrupt Err<br>P50X4258E (P50M4250P) |                                | SC_Verify_OIC_POST and UTL_Process_OIU_Health forward OIC-detected PSP INTR error (an invalid 80C51 FC interrupt has occurred INTR service routines exist for all possible interrupts, and this is an unused INTR) | If during POST, error code is generated when it occurs, to be logged to OIU EEPROM error log when OIU POST attempt is complete; otherwise UTL_Process_OIU_Health calls the Utility CSCs to generate the error code, and to log the error in OIU error log at the end of 100-ms cycle | OIU does NOT fail POST; normal processing resumes. Otherwise, PSP/PTB attempts to return from interrupt and resumes normal processing. Note: PSP/PTB time, spent logging error may result in any number of timing-related errors                 |
| OIC_PSP_POST_ERR<br>P50X4257E (P50M4250P)      |                                | SC_Verify_OIC_POST forwards OIC-detected POST error for PSP (i.e., occurs when any error happens during OIC PSP/PTB POST)  | Error code is generated when detected, to be logged to OIU EEPROM error log when OIU POST attempt is complete  | If during POST, OIU does NOT fail POST; normal processing resumes  |

| Error name and MSID/<br>(parent MSID)               | MCC/(SPEC 212)<br>display name | How is error condition determined?  | How is error reported?   | What is error's impact?   |
|---|--------------------------------|---|--|---|
| OIC_PSP_POST Incomplete<br>P50X4256E (P50M4250P)    |                                | SC_Verify_OIC_POST detects OIC did not complete POST for PSP (i.e., OIC PSP POST complete bit not set)  | Error code is generated when detected, to be logged to OIU EEPROM error log when OIU POST attempt is complete  | OIU fails POST, and SC_System_Startup will issue RESET instruction and reattempt POST for all 3 cards; max 3 POST attempts, then WDT halts system   |
| OIC_PSP_SRAM_ERR<br>P50X4255E (P50M4250P)           |                                | SC_Verify_OIC_POST forwards OIC-detected PSP SRAM error (i.e., PSP POST values written to SRAM do not match values read from SRAM)                              | Error code is generated when detected, to be logged to OIU EEPROM error log when OIU POST attempt is complete  | OIU fails POST, and SC_System_Startup will issue RESET instruction and reattempt POST for all 3 cards; max 3 POST attempts, then WDT halts system   |
| OIU RT on Multiple Bus Err<br>P50X4254E (P50M4250P) |                                | API_Load_Recon_Data reads the BC/RT flag for all buses from recon data, which says the OIU is an RT on more than one bus  | Error code is generated when it occurs, to be sent in OIU status and logged to OIU EEPROM error log at the end of the first 100-ms cycle   | OIU configures first RT bus BIA as an RT with interrupts. Configures any subsequent RT buses as RT without interrupt. OIU comes up normally and ground/crew should reconfigure OIU so that it is RT on only one bus |
| PDI_SRAM_ACCESS_ERR<br>P50X4252E (P50M4250P)        |                                | OCC not granted memory request for PDI SRAM by PDI during POST; or PDI_Construct_PDI_Minor_Frame is not granted memory when it is trying to write the PDI frame | If during POST, Error code is generated when it occurs, to be logged in OIU EEPROM Error log when OIU POST attempt is sent in OIU status and logged to OIU EEPROM error log at the end of the 100-ms cycle | If during POST, Error code is generated when it occurs, to be logged in OIU EEPROM Error log when OIU POST attempt is sent in OIU status and logged to OIU EEPROM error log at the end of the 100-ms cycle          |
| PDI_SRAM_RW_ERR<br>P50X4251E (P50M4250P)            |                                | SC_Verify_OIC_POST encounters problem reading/writing to/from PDI SRAM during POST  | Error code is generated when it occurs, to be logged to OIU EEPROM error log when OIU POST attempt is complete   | OIU fails POST, and SC_System_Startup will issue RESET instruction and reattempt POST for all 3 cards; max 3 POST attempts, then WDT halts system   |

| Error name and MSID/<br>(parent MSID)               | MCC/(SPEC 212)<br>display name | How is error condition determined?   | How is error reported?  | What is error's impact?   |
|---|--------------------------------|--|---|---|
| PRIV_VIO_ERR<br>P50X4268E (P50M4260P)               |                                | The Privilege Violation exception is generated when attempting to execute a privileged instruction when in the user mode; however, user mode is not used by FSW (always in supervisor mode), therefore, possibly generated due to code corruption or rad hit | The exception handler, EP_Privilege_Violation_SR, is invoked and it calls the Utility CSU to generate the error code, to be logged in the EEPROM error log later  | Set the supervisor bit in the Status Register on the stack to force us back into supervisor mode; increment System Error Counter* and normal processing resumes   |
| PSP in Wrong Buffer Err<br>P50X4267E (P50M4260P)    |                                | i.e., PSP_Read_PSP_Cmd expects PSP command to be in buffer 1, but it is in buffer 2 (from data rec bits)   | Error code is generated when it occurs, to be sent in OIU status and logged to OIU EEPROM error log at the end of the 100 ms cycle  | PSP command is read out of the buffer it is really in and OCC resets what buffer to expect next time  |
| PSP PTB SRAM_ACCESS_ERR<br>P50X4266E (P50M4260P)    |                                | OCC is not granted memory request for PSP SRAM during POST; or PSP_Read_PSP_Cmd cannot read PSP cmd  | Error code is generated when it occurs, to be logged to OIU EEPROM error log when OIU POST attempt is complete if during POST or logged to OIU EEPROM error log at end of 100-ms cycle and sent in OIU status (telemetry) | IF during POST, OIU fails POST, and SC_System_Startup will issue RESET instruction and reattempt POST for all 3 cards; max 3 POST attempts, then WDT halts system PSP cmd will not be read, and, otherwise, cannot be processed |
| PSP_SRAM_RW_ERR<br>P50X4265E (P50M4260P)            |                                | SC_Verify_OIC_POST encounters problem reading/writing to/from PSP SRAM during POST   | Error code is generated when it occurs, to be logged to OIU EEPROM error log when OIU POST attempt is complete  | OIU fails POST, and SC_System_Startup will issue RESET instruction and reattempt POST for all 3 cards; max 3 POST attempts, then WDT halts system   |
| Recon EEPROM Faulty Err<br>P50X4264E (P50M4260P)    |                                | API_Load_Recon_Data detects a bad table tag, or checksum   | Error is generated, logged to EEPROM  | OIU halts   |
| Recon # Trans/Subframe Err<br>P50X4263E (P50M4260P) |                                | API_Setup_Cyclic_Msgs detects more than 15 MS1553B transactions in a subframe for a given bus  | Error is generated, logged to EEPROM  | OIU halts   |
| SPURIOUS_INTR_ERR<br>P50X4262E (P50M4260P)          |                                | The Spurious Interrupt exception is generated when a bus error occurs while processing an interrupt  | The exception handler, EP_Spurious_Interrupt_SR, is invoked and it calls the Utility CSU to generate the error code, to be logged in the EEPROM error log later at end of 100-ms cycle.                                   | Increment System Error Counter* and normal processing resumes   |

| Error name and MSID/<br>(parent MSID)         | MCC/(SPEC 212)<br>display name | How is error condition determined?  | How is error reported?   | What is error's impact?   |
|---|--------------------------------|---|--|---|
| TRACE_ERR<br>P50X4261E (P50M4260P)            |                                | The Trace exception is generated when tracing is enabled via the trace bit in the status register; however, tracing is not used in current design, therefore, possibly generated due to code corruption or rad hit                            | The exception handler, EP_Trace_SR, is invoked and it calls the Utility CSU to generate the error code, to be logged in the EEPROM error log later at end of 100-ms cycle.             | Clear the trace bit in the Status Register on the stack to disable tracing; increment System Error Counter* and normal processing resumes                   |
| TRAP_V_ERR<br>P50X4278E (P50M4270P)           |                                | The TRAPV exception is generated when a runtime overflow condition occurs and the TRAPV instruction has been executed; however, the TRAPV instruction is not used by the FSW, therefore, possibly generated due to code corruption or rad hit | The exception handler, EP_TRAPV_SR, is invoked and it calls the Utility CSU to generate the error code, to be logged in the EEPROM error log later at end of 100-ms cycle              | Clear the overflow bit in the Status Register on the stack to rescind the overflow condition; increment System Error Counter* and normal processing resumes |
| TRAP_X_ERR<br>P50X4277E (P50M4270P)           |                                | The TRAP exception is generated when a TRAP (numbered 0 to 15) instruction is executed; however, TRAP instructions are not used in current design; therefore, possibly generated due to code corruption or rad hit                            | The exception handler, EP_TRAP_X_SR, is invoked and it calls the Utility CSU to generate the error code, to be logged in the EEPROM error log later at end of 100-ms cycle             | Increment System Error Counter* and normal processing resumes   |
| UNINIT_INTR_VECT_ERR<br>P50X4276E (P50M4270P) |                                | The Uninitialized Interrupt Vector exception is generated when an exception occurs and the interrupting device has not initialized its appropriate vector register number; it is responsible for providing Vector 15                          | The exception handler, EP_Uninit_Intr_Vector_SR, is invoked and it calls the Utility CSU to generate the error code, to be logged in the EEPROM error log later at end of 100-ms cycle | Increment System Error Counter* and normal processing resumes   |
| UNUSED_EXCEPTION_ERR<br>P50X4275E (P50M4270P) |                                | Any exception corresponding to an unused, reserved, unassigned, or user interrupt vector is generated. Possible due to code corruption or rad hit   | The exception handler, EP_Unused_Exception_SR, is invoked and it calls the Utility CSU to generate the error code, to be logged in the EEPROM error log later at end of 100-ms cycle   | Increment System Error Counter* and normal processing resumes   |

| Error name and MSID/<br>(parent MSID)               | MCC/(SPEC 212)<br>display name                          | How is error condition determined?  | How is error reported?   | What is error's impact?  |
|---|---|---|--|--|
| ZERO_DIVIDE_ERR<br>P50X4274E (P50M4270P)            |   | The Divide by Zero exception is generated when the processor attempts a division with a divisor of zero   | The exception handler, EP_Divide_By_Zero_SR, is invoked and it calls the Utility CSU to generate the error code, to be logged in the EEPROM error log later at end of 100-ms cycle                             | Increment System Error Counter* and normal processing resumes                                      |
| Floating Pt Conversion Err<br>P50X4288E (P50M4280P) |   | UTL_Float_Conv detects a floating point conversion error when performing the conversion   | UTL_Float_Conv calls the Utility CSC to generate the error code  | Normal processing resumes. However, the content of the converted value in PDI will not be accurate |
| Invalid Config Cmd Err<br>P50X4287E (P50M4280P)     |   | When OIU receives a bad OIU config cmd  | Error indicator status for PDI is set in OIU status (telemetry)  | The command is ignored   |
| ISS BC No Comm Status err<br>P50X4286E (P50M4280P)  | ISS - BC FAIL<br>(tbd)                                  | The EP_ExecTimer_Autovector detects that it is being executed after or since the BIC has been driving the 100-ms processing interrupt; therefore, something has happened to remove the ISS BC (or to our BIA configuration) | EP_ExecTimer_Autovector_SR resets the exec timer countdown value to resume internally driven 100-ms interrupt, and calls the Utility to generate the error code, to be included in OIU status data (telemetry) | Normal processing resumes (i.e., not an OIU error - reported as status)                            |
| OIC PDI Sync Err<br>P50X4284E (P50M4280P)           |   | UTL_Process_OIU_Health forwards OIC - detected error (OIC) PDI runs out of data and OCC has not provided next data buffer to be sent)   | UTL_Process_OIU_Health calls the Utility CSC to generate the error code to be sent in OIU status (telemetry)   | Normal processing resumes  |
| OIC PSP Command LOS Err<br>P50X4283E (P50M4280P)    | OIC - PSP/PTB - PSP<br>Signal<br>(part of comp for tbd) | UTL_Process_OIU_Health forwards OIC (PSP signal loss during command reception)  | UTL_Process_OIU_Health calls the Utility CSC to generate the error code to be sent in OIU status (telemetry)   | Normal processing resumes  |
| OIC PTB Time Err<br>P50X4282E (P50M4280P)           |   | POST complete   | Log status condition to OIC EEPROM and to shared SRAM  | If OCC does not detect bit, then OIC did not complete POST and a OIU Reset is required             |
| OIC PSP Parity Err<br>P50X4281E (P50M4280P)         | OIC - PSP/PTB - CMD<br>PARITY<br>(part of comp for tbd) | UTL_Process_OIU_Health forwards OIC (the parity byte in command does not match calculated parity)   | UTL_Process_OIU_Health calls the Utility CSC to generate the error code to be sent in OIU status (telemetry)   | Normal processing resumes  |

| Error name and MSID/<br>(parent MSID)           | MCC/(SPEC 212)<br>display name | How is error condition determined?   | How is error reported?   | What is error's impact?  |
|---|--------------------------------|--|--|--|
| OIC PSP PTB Health Err<br>P50X4298E (P50M4290P) |                                | PSP_Process_PSP_Cmd detects the PSP/PTB Health & Status bit toggling has failed to occur for three consecutive checks (100-ms processing frames)   | PSP_Process_PSP_Cmd calls the Utility CSC to generate the error code to be sent in OIU status (telemetry)                        | Increment System Error Counter* and normal processing resumes  |
| OIC PSP Sync Err<br>P50X4297E (P50M4290P)       | OIC - PSP/PTB - PSP SYNC       | UTL_Process_OIU_Health forwards OIC detected error (no available buffer for new command. OCC firmware did not clear at least one of the two buffers)   | UTL_Process_OIU_Health calls the Utility CSC to generate the error code to be sent in OIU status (telemetry)                     | Normal processing resumes  |
| OIC PTB LOS Err<br>P50X4296E (P50M4290P)        | OIC - PSP/PTB - PTB SIGNAL     | UTL_Process_OIU_Health checks the appropriate bit in PSP SRAM status reg. 1 for the error indication set by OIC Firmware   | UTL_Process_OIU_Health calls the Utility CSC to generate the error code to be sent in OIU status (telemetry)                     | Normal processing resumes  |
| OIC PTB Sync Err<br>P50X4295E (P50M4290P)       | OIC - PSP/PTB - PTB SYNC       | UTL_Process_OIU_Health forwards OIC detected (invalid PTB pulse; i.e., OIC does not receive a valid PTB signal transition within 11 ms)  | UTL_Process_OIU_Health calls the Utility CSC to generate the error code to be sent in OIU status (telemetry)                     | Normal processing resumes  |
| OIU ISS Lost Sync Err<br>P50X4294E (P50M4290P)  | ISS - SYNC FAIL                | This error can be detected by two modules: 1. UTL_Maintain_Frames detects that two consecutive ISS frame count discontinuities occurred 2. API_Check_Time_Sync could not obtain three consecutive ISS frame counts in ten frames | UTL_Maintain_Frames or API_Check_Time_Sync calls the Utility CSC to generate the error code to be sent in OIU status (telemetry) | When error occurred in UTL_Maintain_Frames, it sets rerun_API flag, and program execution will start from the Application Initialization. When error occurred in API_Check_Time_Sync, the ISS bus controller will be ignored |
| OIU SSOR Lost Sync Err<br>P50X4293E (P50M4290P) | SSOR - SYNC                    | UTL_Maintain_Frames detects that two consecutive SSOR frame count discontinuities occurred   | UTL_Maintain_Frames calls the Utility CSC to generate the error code to be sent in OIU status (telemetry)                        | UTL_Maintain_Frames sets rerun_API flag. By setting this flag, after the completion of the 100-msec frame, program execution will start from the Application Initialization  |



| Error name and MSID/<br>(parent MSID)                   | MCC/(SPEC 212)<br>display name | How is error condition determined?   | How is error reported?  | What is error's impact?  |
|---|--------------------------------|--|---|--|
| PSP Cmd Count Out of Bound Err<br>P50X4292E (P50M4290P) |                                | EP_OIC_Autovector_SR increments a counter with each OIC interrupt, keeping track of incoming PSP commands within any 100-ms processing frame; if this counter is < 0 or > 2, this error is indicated | EP_OIC_Autovector_SR calls the Utility CSCU to generate the error code, to be included in OIU status data later (telemetry) | Increment System Error Counter* and normal processing resumes    |
| PSP Retries Failed Err<br>P50X4291E (P50M4290P)         | ISS - CMD FAIL                 | As BC, OIU tried three times to send out a PSP cmd to an RT and failed   | Error indicator is set in OIU to be sent in OIU status (telemetry)  | Command is not routed  |
| PTB Not Available Err<br>P50X4308E (P50M4300P)          | OIC - PSP/PTB - PTB SIGNAL     | API_Initialize_OIU_Time detects that the PTB time is still not available 2.5 seconds after it was requested  | API_Initialize_OIU_Time calls the Utility CSC to generate the error code to be sent in OIU status (telemetry)               | Normal processing resumes  |
| Unfinished BC Frame Err<br>P50X4307E (P50M4300P)        |                                | The BC frame on a bus the OIU is BC on did not finish before the BIA was told to send another  | Error indicator for PDI is set to be sent in OIU status (telemetry)   | RTs on the bus(es) may not have received all their transactions  |
| Unimplemented RC Err<br>P50X4306E (P50M4300P)           | OIC - PSP/PTB - BAD RTG CODE   | The row number for the PSP data routing table is 0, indicating the routing code is not implemented   | Error indicator is set in OIU to be sent in OIU status (telemetry)  | Command is ignored   |
| SSOR Frame Count Out Of Order<br>P50X4305E (P50M4300P)  | SSOR - FRM SEQ                 | UTL_Maintain_Frames detects that there is a single SSOR frame count discontinuity  | UTL_Maintain_Frames calls the Utility CSC to generate the error code to be sent in OIU status (telemetry)                   | Normal processing resumes  |
| ISS Frame Count Out Of Order<br>P50X4304E (P50M4300P)   | ISS - FRAME SEQ                | UTL_Maintain_Frames detects that there is a single ISS frame count discontinuity   | UTL_Maintain_Frames calls the Utility CSC to generate the error code to be sent in OIU status (telemetry)                   | Normal processing resumes  |
| OIC PSP Byte Count Err<br>P50X4303E (P50M4300P)         |                                | UTL_Process_OIU_Health checks the appropriate bit in PSP SRAM status reg. 1 for the error indication set by OIC Firmware   | UTL_Process_OIU_Health calls the Utility CSC to generate the error code to be sent in OIU status (telemetry)                | Normal processing resumes  |
| PDI Buffer Not Clear Err<br>P50X4302E (P50M4300P)       |                                | PDI_Construct_PDI_Minor_Frame determines the buffer that is to be written to is still full   | Error code is generated when it occurs, to be sent in OIU status to be sent in OIU status (telemetry)                       | Loss of PDI sync, will start over writing to buffer 1 next cycle |

## SECTION 40 - MODULAR MEMORY UNIT/ SOLID STATE RECORDER

### CONTENTS

| Section | Page   |       |
|---------|--|-------|
| 40.1    | GENERAL .....                                | 40-1  |
| 40.2    | INTERFACES .....                             | 40-1  |
| 40.3    | MMU DESCRIPTION .....                        | 40-3  |
| 40.3.1  | Power Supply .....                           | 40-4  |
| 40.3.2  | MMU Packaging .....                          | 40-5  |
| 40.3.3  | Avionics Bay Cooling .....                   | 40-5  |
| 40.3.4  | I/O Processing .....                         | 40-6  |
| 40.3.5  | Single Board Computer .....                  | 40-8  |
| 40.3.6  | Memory .....                                 | 40-10 |
| 40.3.7  | BITE .....                                   | 40-12 |
| 40.4    | MODES .....                                  | 40-12 |
| 40.4.1  | Power-On Self-Test Mode .....                | 40-14 |
| 40.4.2  | Standby Mode .....                           | 40-15 |
| 40.4.3  | Erase Mode .....                             | 40-15 |
| 40.4.4  | Comprehensive Self-Test Mode .....           | 40-15 |
| 40.4.5  | Remap Mode .....                             | 40-16 |
| 40.4.6  | Record Modes .....                           | 40-16 |
| 40.4.7  | Playback Modes .....                         | 40-18 |
| 40.5    | COMMANDS .....                               | 40-20 |
| 40.5.1  | Store/Recall Position .....                  | 40-21 |
| 40.5.2  | Define/Clear Record Auto-Stop Position ..... | 40-21 |
| 40.5.3  | Unprotect Parallel .....                     | 40-21 |
| 40.5.4  | Define/Clear PB Queue .....                  | 40-21 |
| 40.5.5  | Reset .....                                  | 40-22 |
| 40.6    | TELEMETRY .....                              | 40-24 |
| 40.6.1  | BITE Telemetry .....                         | 40-26 |
| 40.7    | REFERENCES .....                             | 40-28 |

## TABLES

| Table |   | Page  |
|-------|---|-------|
| 40-1  | Specifications .....                    | 40-4  |
| 40-2  | Input power .....                       | 40-4  |
| 40-3  | Output power.....                       | 40-5  |
| 40-4  | Time per segment .....                  | 40-10 |
| 40-5  | OST types and categories.....           | 40-12 |
| 40-6  | POST types and categories .....         | 40-14 |
| 40-7  | CST types and categories.....           | 40-15 |
| 40-8  | SSR command table .....                 | 40-22 |
| 40-9  | SSR telemetry table .....               | 40-24 |
| 40-10 | SSR mode telemetry .....                | 40-25 |
| 40-11 | OST telemetry .....                     | 40-26 |
| 40-12 | POST telemetry.....                     | 40-27 |
| 40-13 | CST telemetry .....                     | 40-27 |
| 40-14 | Valid modes per command.....            | 40-28 |
| 40-15 | Sequential commanding requirements..... | 40-28 |

## FIGURES

| Figure |  |       |
|--------|--|-------|
| 40-1   | Picture of MMU .....                       | 40-1  |
| 40-2   | MMU 1 interfaces .....                     | 40-2  |
| 40-3   | MMU 2 interfaces .....                     | 40-3  |
| 40-4   | I/O card block diagram .....               | 40-7  |
| 40-5   | SBC block diagram .....                    | 40-9  |
| 40-6   | Memory block diagram.....                  | 40-11 |
| 40-7   | High-level state transition diagram .....  | 40-13 |
| 40-8   | State diagram for record modes.....        | 40-17 |
| 40-9   | State transition diagram for PB modes..... | 40-19 |

## SECTION 40

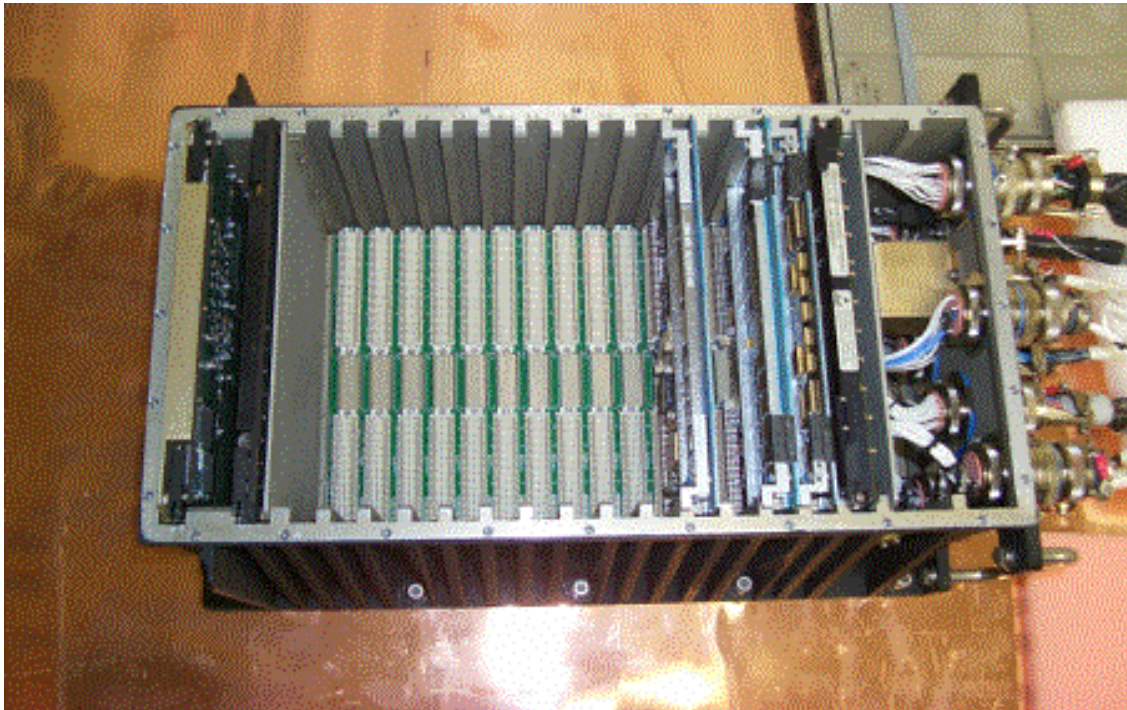
### MODULAR MEMORY UNIT/SOLID STATE RECORDER

#### 40.1 GENERAL

Boeing-North American™ (BNA) Reusable Space Systems™ (BRSS) is lead contractor for the implementation of the Modular Memory Unit (MMU) for the orbiter. The MMU replaces the function of the old Operations (OPS) recorders, payload recorder, and General Purpose Computer (GPC) Mass Memory Units. The recorder subsystem is referred to as the Solid State Recorder (SSR). The GPC mass memory subsystem is referred to as the Solid State Mass Memory (SSMM). This systems brief covers the SSR subsystem. This preliminary version of the systems brief is based on Preliminary and Critical Design reviews.

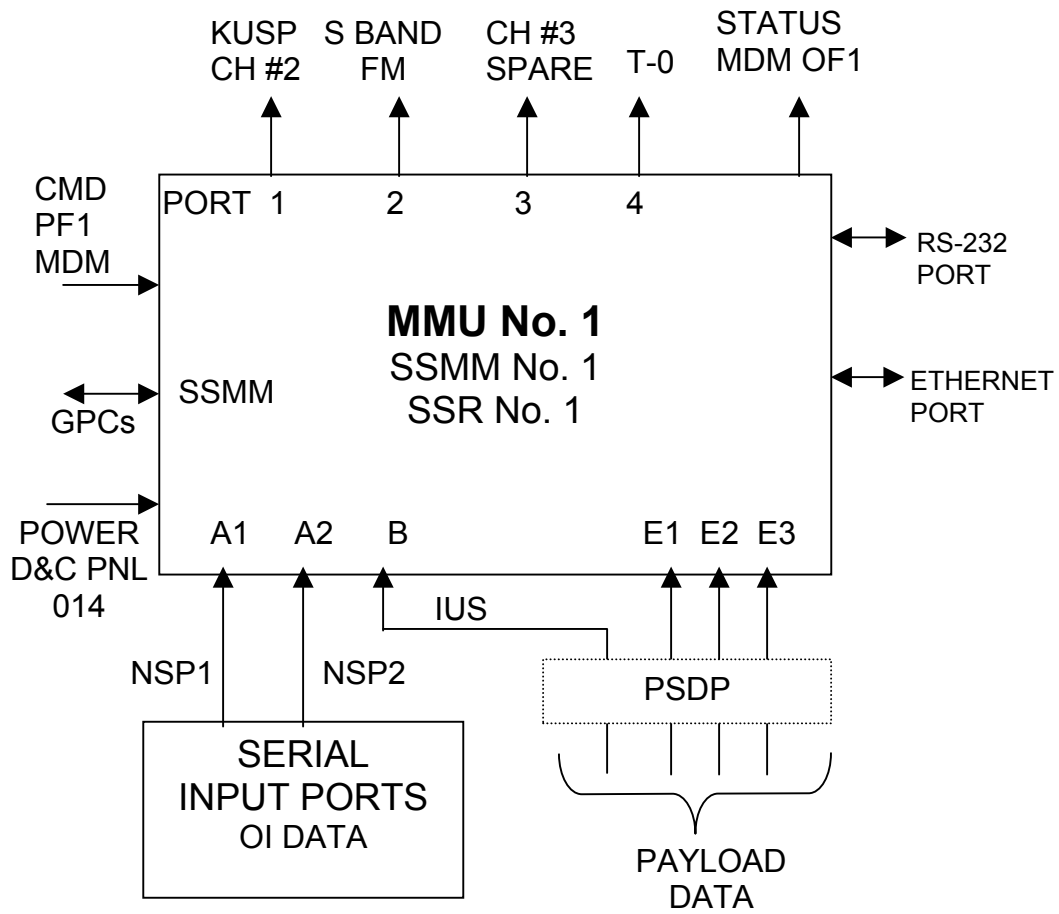
#### 40.2 INTERFACES

Figure 40-1 shows a picture of the physical MMU, Figure 40-2 shows the MMU1 interfaces, and Figure 40-3 shows the MMU2 interfaces.



*Figure 40-1. Picture of MMU*

### AVIONICS BAY 1



Operational software can be loaded via the RS-232 port

**Figure 40-2. MMU 1 interfaces**

AVIONICS BAY 2

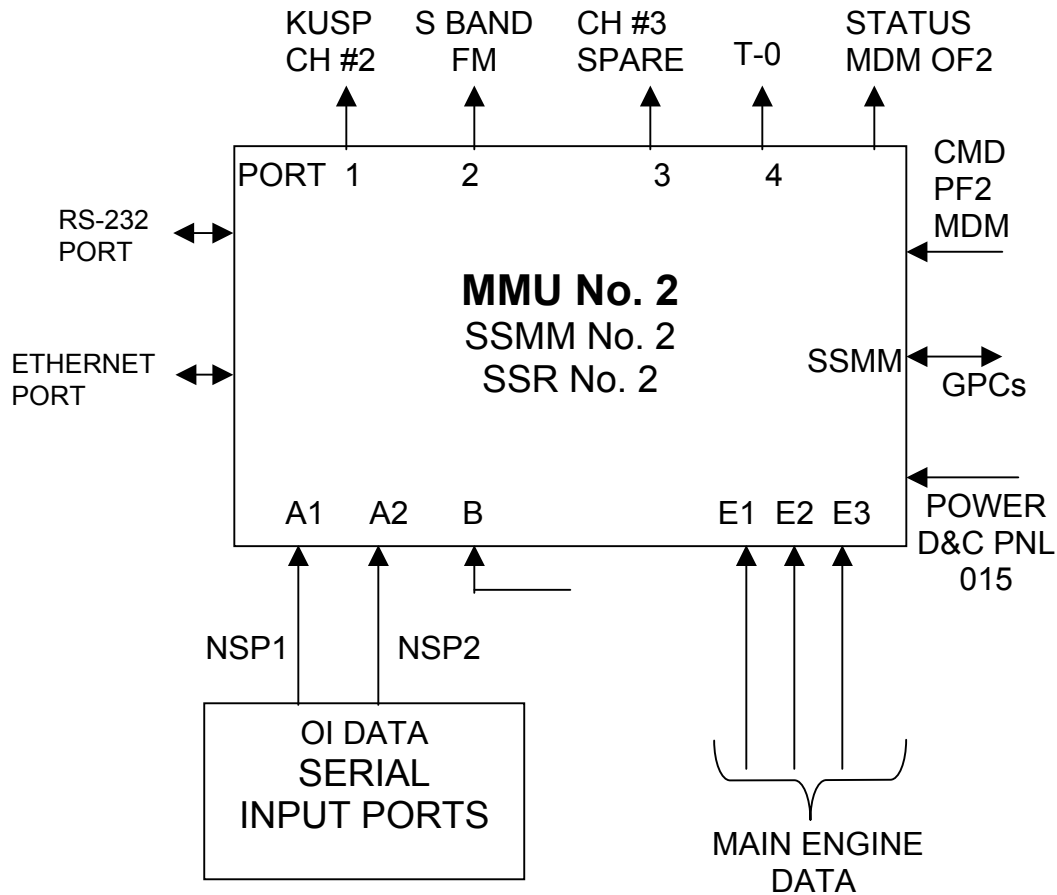


Figure 40-3. MMU 2 interfaces

40.3 MMU DESCRIPTION

Each MMU is a Line Replaceable Unit (LRU) consisting of a Versa Module Eurocard (VME) enclosure, backplane, power supply, and functional circuit card assemblies. There are two MMU LRUs on each orbiter, as well as two prototype MMUs in the

Shuttle Mission Simulator (SMS). The SSR function uses the MMU power supply and VME bus, while the SSMM uses only the power supply.

The SSMM card emulates the function of the old Mass Memory Units and was developed by SEAKR Engineering™.

The recorder Nonvolatile Memory (NVM) card uses 3.6 gigabits of flash Random Access Memory (RAM) and was developed for the SSR by SEAKR Engineering™.

The Central Processing Unit that controls the MMU operation is a Single-Board Computer (SBC) built by Aitech™ based on the PowerPC™ architecture running the WindRiver™ VxWorks™ operating system.

The SSR Input/Output (I/O) functions are performed by an I/O card developed for the SSR by SEAKR Engineering™.

Significant MMU specifications are listed in Table 40-1:

**Table 40-1. Specifications**

|             |   |
|-------------|---|
| Flash RAM   | 128 Mbit RAM chips  |
| EDAC        | Custom nonvolatile error detection and correction circuitry |
| Remap       | Memory remap to exclude bad 256 Kbyte cells                 |
| VME I/F     | 64-bit multiplexed block linear transfer                    |
| Output Freq | Accuracy 1 percent  |
| Jitter      | Bit-to-bit 1 percent  |
| Commands    | Process at least 3 per second                               |
| Power Usage | 64W ±10%  |
| Weight      | 40.2 lb   |
| Size        | 7.7 in. by 12 in. by 20 in.                                 |
| Temperature | Nominal operating range 32° to 130° F (at coldplate)        |

#### 40.3.1 Power Supply

28 V power is supplied to the MMU per Table 40-2:

**Table 40-2. Input power**

| LRU   | Panel | Switch | Control  | Power    |
|-------|-------|--------|----------|----------|
| MMU 1 | O14   | S13    | CNTL AB1 | MNA FPC1 |
| MMU 2 | O15   | S12    | CNTL AB2 | MNB FPC2 |

The MMU power supply is designed to operate from an input of 28 V dc ± 4 V dc, and maximum power output is 250 W. Table 40-3 specifies the power outputs from each LRU power supply:

**Table 40-3. Output power**

| Output (V dc) | Range (V dc) | Ripple (mV p-p) | Current min. (A) | Current max. (A) |
|---------------|--------------|-----------------|------------------|------------------|
| +5            | +0.25 –0.125 | 50              | 3.5              | 35               |
| +3.3          | +0.25 –0.125 | 50              | 1                | 10               |
| +12           | +0.6 –0.36   | 50              | 0.2              | 2                |
| -12           | +0.6 –0.36   | 50              | 0.2              | 2                |

The power supply consists of a power supply card and a capacitive energy storage card, both developed by Vista Controls™. The power supply card has five Lambda™ dc-to-dc converters, three for +5 V, one for +3.3 V, and one for ±12 V. All outputs are short-circuit protected, over-voltage protected, and over-temperature protected and automatically recover (without power cycling) when the anomaly condition is removed (SSR may lose up to 32 bits caught in the input serial to parallel converter).

The capacitor bank in the energy storage card stores 50 V dc across 19 milliFarads of capacitance, which provides 4.6 milliseconds (msec) of power for graceful shutdown of the SBC. When the input power drops below 21 V for 150 microseconds (μsec), a system reset pulse called AC Fail is generated. If the input power momentarily dips below 21 V and recovers in less than 4.6 msec, the power outputs stay within specification. During shutdown, after receipt of AC Fail, the Operational Instrumentation (OI) data buffered in the I/O card will be stored in NVM on the memory card.

The SSR Power-On Self-Test (POST) mode is described in Section 40.4.1.

If a power dropout lasts for less than 62 msec, the SSR may end up in a pre-POST state, with the mode telemetry indicating NONE. A full power cycle should recover normal functioning.

### 40.3.2 MMU Packaging

The VME enclosure consists of three pieces: a top cover, a bottom cover, and one piece with four sides, all developed by Vista Controls™. The enclosure is screwed to an adapter plate, which is mounted to a coldplate. Heat flow from the cards is through the sides of the enclosure to the coldplate. There is no fan in the box.

The 64-bit VME backplane developed by Vista Controls™ has 15 user slots, four of which are used: one for the SBC, one for the I/O card, one for the memory card, and one for the SSMM.

### 40.3.3 Avionics Bay Cooling

Both MMUs are cooled by the water distribution system. The LRUs are mounted on coldplates, which have two water loops flowing through them. Each coldplate is arranged in a sandwich fashion between the shelf and recorder. Loop 1 is next to the MMU, and loop 2 is next to the shelf. Water loop temperatures range from 32° to 122° F (usually 70° to 90° F on orbit). Without coolant water flow and allowing the cold



plate temperature to rise to 120° F, damage to the SBC could result within 33 minutes. With water flowing, the MMU can operate with Cold Plate temperature up to 130° F.

The air in the bay, nominally circulated by fans, ranges between 45° and 145° F (usually 80° to 95° F on orbit).

#### **40.3.4 I/O Processing**

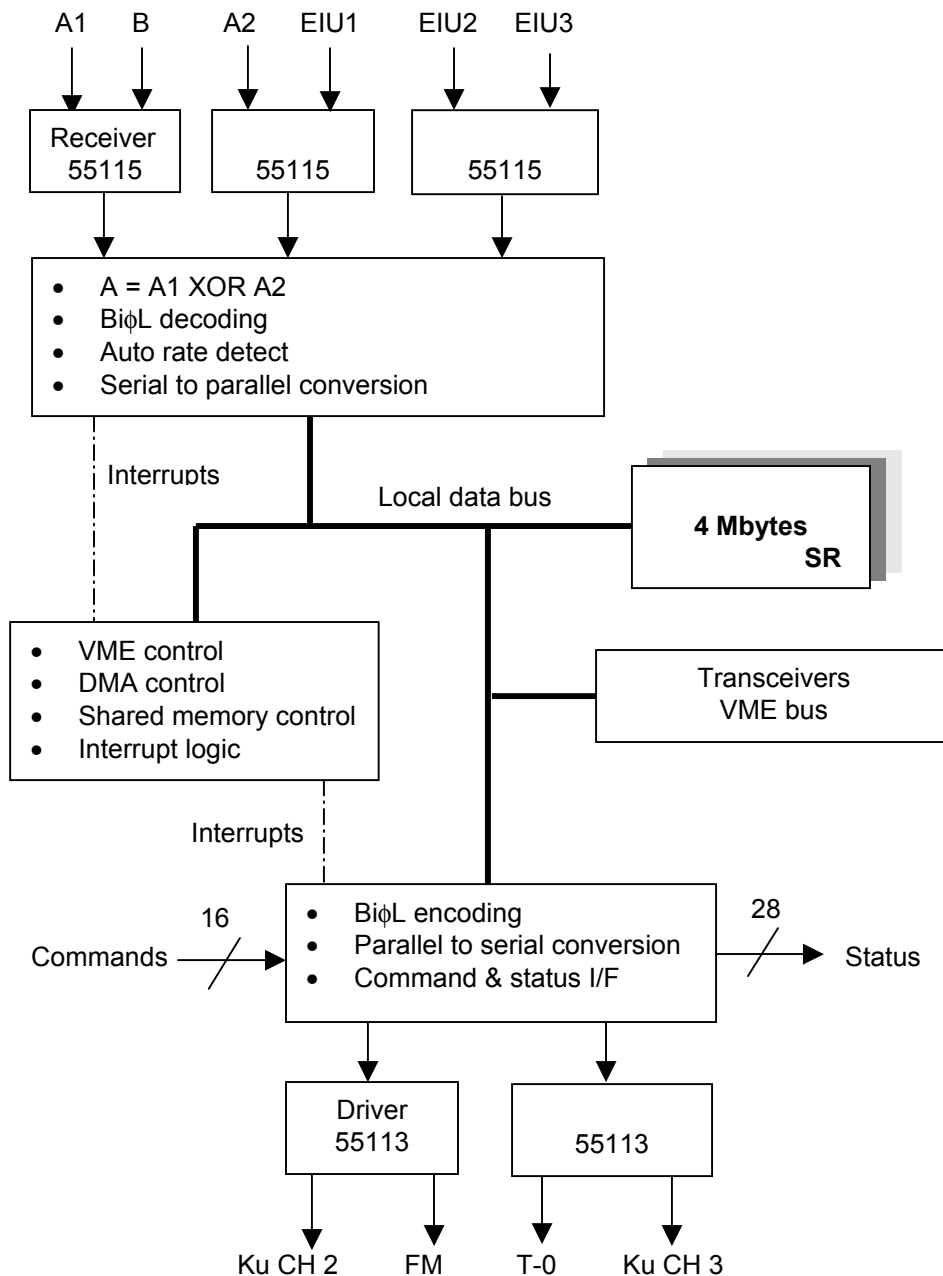
The I/O card processes the SSR commands, status, input data, and output data. Figure 40-4 shows the I/O card block diagram. There are 16 discrete command bits, 28 discrete status bits, 6 serial data inputs, and 4 serial data outputs.

##### **40.3.4.1 Command Input Detection**

When the I/O card detects a change in any input state from the Payload Forward (PF) Multiplexer/Demultiplexer (MDM), it waits for input state settling for 30  $\mu$ sec before decoding the new bit pattern. An all-zeroes reset bit pattern is required between valid commands for the command detector to output a valid command to the SBC for processing. Detailed commanding definition is covered later in this systems brief.

##### **40.3.4.2 Status Outputs**

The 28 telemetry discretes indicate Built-In Test Equipment (BITE) status, current mode, current memory position, count of Playback (PB) queue slots, auto-stop enable status, and main engine data protection status. Detailed telemetry definition is covered later in this systems brief.



XOR = exclusive OR  
 DMA = direct memory addressing  
 SRAM = static random access memory

**Figure 40-4. I/O card block diagram**

#### 40.3.4.3 Data Input Rate Detection

The I/O card detects the rate of the incoming Biphas-Level ( $Bi\phi$ -L) data by establishing the length of the long and short time durations between bit level transitions. The rate detector will remain locked on the input bit stream despite seeing up to 2 percent bit-to-bit jitter. Depending on the randomness of the data, it can lock to an input stream within four bit periods. After locking to the stream, the data is stored in NVM, if that particular recording mode has been enabled by the SBC.

#### 40.3.4.4 Dump Data Outputs

When commanded to dump stored data from a particular location in NVM, the I/O card outputs that data in  $Bi\phi$ -L format at the commanded rate to four outputs simultaneously:

- Ku Signal Processor (KuSP) channel 2
- Frequency Modulation Signal Processor (FMSP)
- Spare output for optional routing to the KuSP channel 3
- Time-Zero (T-0) lines

SSR 1 dumps via the old payload recorder paths, while SSR 2 dumps via the old OPS recorder paths.

#### 40.3.5 Single Board Computer

The SBC is designed to meet standard VME requirements and contains a BNA-developed SSR control program stored in NVM. Figure 40-5 is the SBC block diagram.

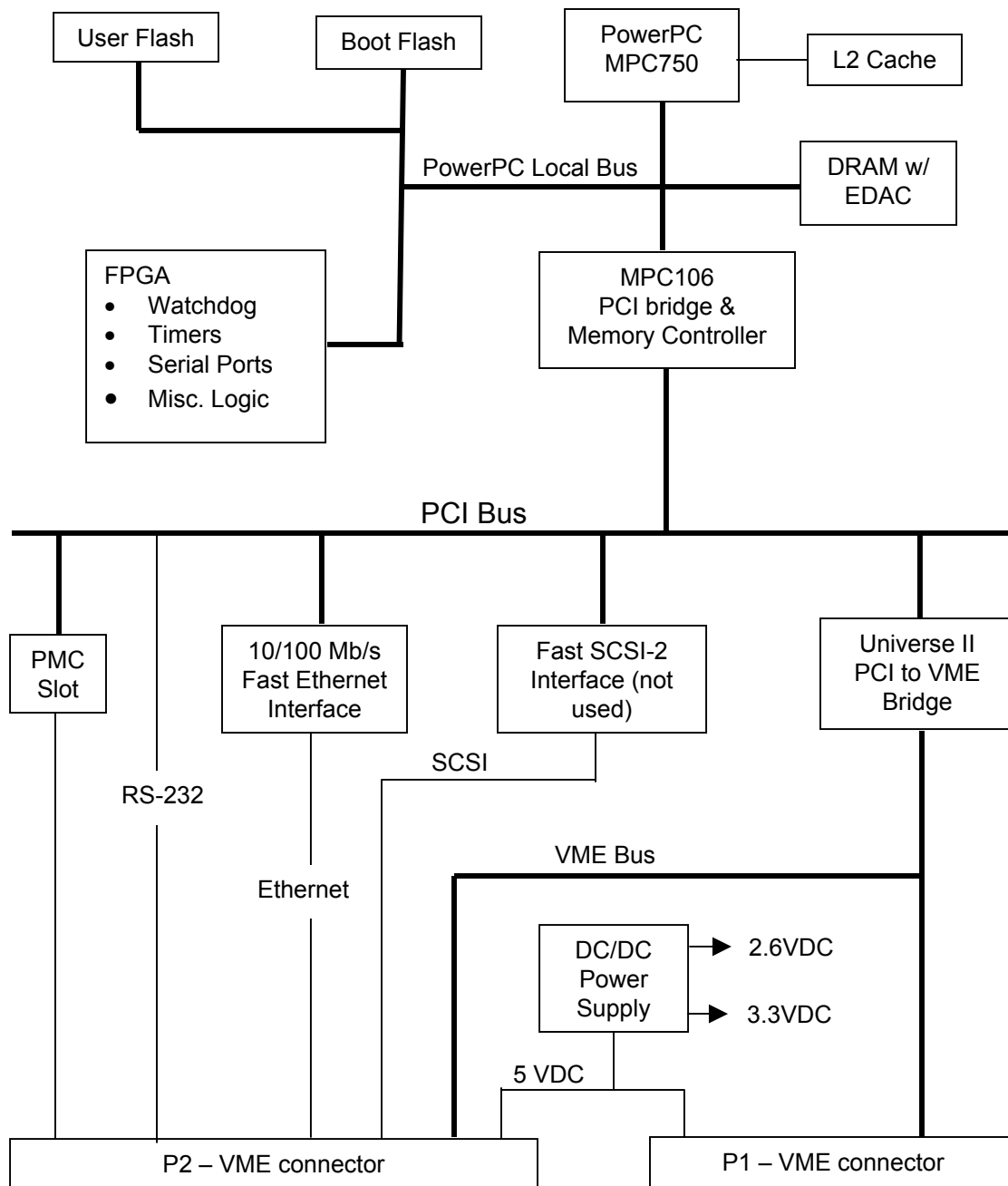
##### 40.3.5.1 SBC Functions

The SBC controls the behavior and modes of the SSR, based on commands received by the SBC. The SBC translates commands into actions and performs all the required functions of each mode. The SBC controls the initiation of maintenance functions, the recording and dumping modes, and the output status indicators.

Ethernet and RS-232 interfaces are not used operationally but can be used in the test station at KSC for diagnostics and for loading a new control program.

##### 40.3.5.2 SBC Program

The control program is stored in SBC user flash RAM. The source code is written in the Ada language. The code is structured to track the mode changes described later in this systems brief, as well as servicing the command decoder and error handling functions.



EDAC = error detection and correction  
 PMC = PCI mezzanine card  
 FPGA = field programmable gate array  
 PCI = peripheral communication interface  
 L2 = level 2

**Figure 40-5. SBC block diagram**

### 40.3.6 Memory

The nonvolatile flash RAM storage area consists of 3.6 Gbits on one card. Figure 40-6 shows the memory card block diagram. The user memory of 3.4 Gbits is mapped by the SBC into 811 segments of 512 Kbytes (811 X 512 X 1024 X 8 bits); each segment can be addressed from the Mission Control Center (MCC). The remaining 200 Mbits are available for inclusion in the user memory area during the remap process, if they pass the remap test. At the end of a remap operation, the number of memory segments available will be indicated in telemetry. If fewer than 811 segments are available following a remap, the unusable memory will be addressable at the end (position 810 and less). The unusable locations can be operationally protected from recording at the start of a mission by including the bad segments in a queue with an unusual PB rate. The mapping is specific to each memory board and is stored in the memory board NVM.

The logical memory layout is a circular buffer, with position 0 immediately following position 810 without interruption.

Table 40-4 shows the time spent on each segment for recording or PB:

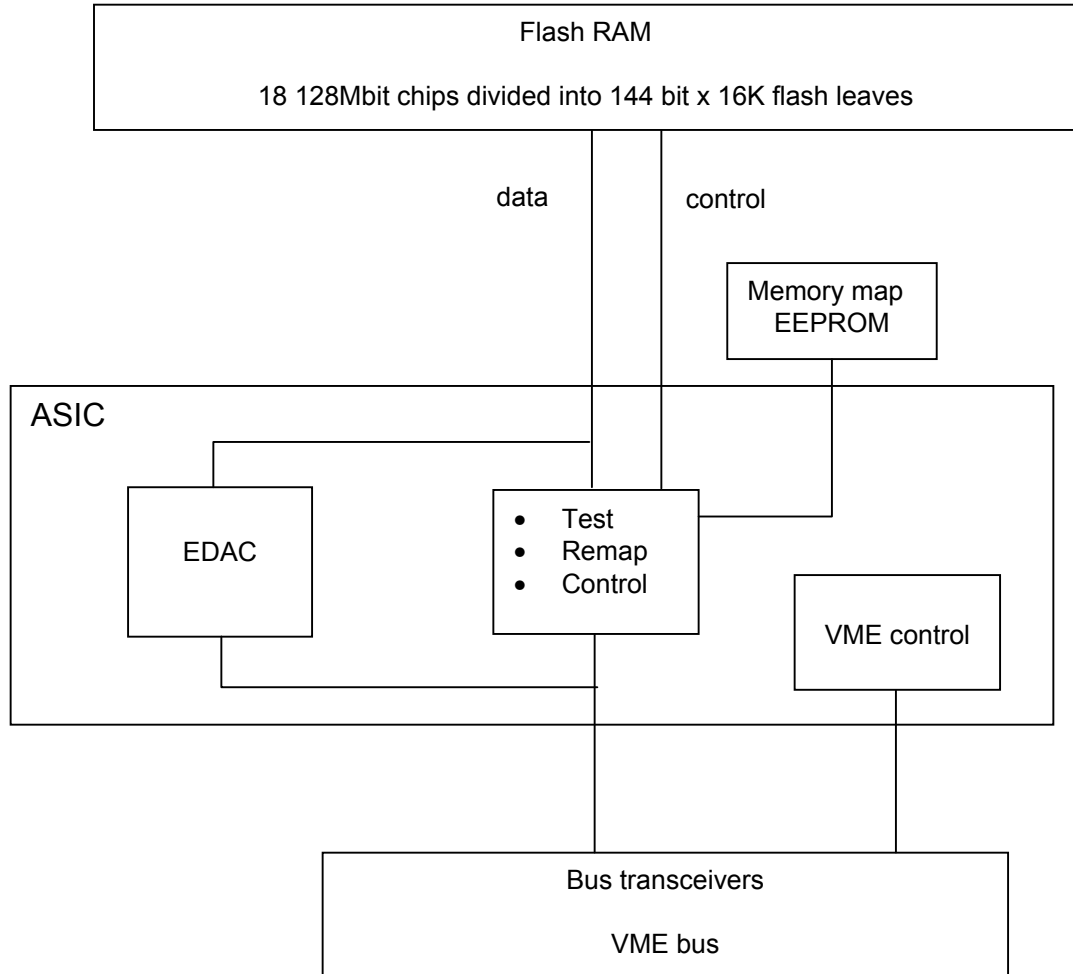
**Table 40-4. Time per segment**

| RCD rate (kbps) | Time (sec) per segment | PB rate (kbps) | Display Slot Rate Code |
|-----------------|------------------------|----------------|------------------------|
| 32              | 2 min 11 sec           | 32             |                        |
| 60              | 1 min 10 sec           |                |                        |
| 64              | 1 min 6sec             | 64             |                        |
| 96              | 44 sec                 |                |                        |
| 128             | 33 sec                 | 128            | 1                      |
| 192             | 22 sec                 | 192            | 2                      |
|                 | 4.4 sec                | 960            | 0                      |
|                 | 4 sec                  | 1024           | 4                      |
|                 | 2 sec                  | 2048           | 8                      |

Before the SSR writes data to memory, it erases ahead in 256 Kbyte blocks. When the MCC sends a command to start serial recording at a position, the SSR starts writing data at the start of that position, erasing any old data at that position. If recording parallel mode, the SSR starts recording data from the E inputs (E1, E2, and E3) at the initial E position or the position subsequent to the one last recorded, to prevent overwriting if protected. The SSR keeps track of the end of E data so that it can restart recording after the previous segment, if parallel recording was stopped and subsequently restarted. Also, the SSR will not continue dumping blank E data after dumping the last recorded segment in an E data region. If a gap is encountered during a PB, an Error Detection and Correction (EDAC) error (noncritical) will result.

When recording parallel on a clean SSR, the initial position for OI data is 162. The positions of all the different data regions in the parallel record mode is shown in the following Memory Position Allocation.

| E1   | E2     | E3      | Remainder |
|------|--------|---------|-----------|
| 0-53 | 54-107 | 108-161 | 162-810   |



EEPROM = electrically erasable programmable read-only memory  
 ASIC = application specific integrated circuit

**Figure 40-6. Memory block diagram**

### 40.3.7 BITE

The SSR performs different tests of the functional logic throughout different phases of operation and displays the results via the SSR status telemetry interface. POST is software initiated upon power-up as described in Section 40.4.1. The Operational Self-Test (OST) is cyclically initiated during operational (non-maintenance) modes, including record, PB, and standby, as described in Section 40.3.7.1. Comprehensive Self-Test (CST) is executed only upon command, as described in Section 40.4.4. BITE results are not stored by the MMU.

For category C failures, where a portion of the SSR fails but the other functions are operational, the SSR will output the BITE status and continue to operate. Category A failures are types that need correction by a reset. Category B failures prevent operation of the SSR; the SSR will immediately shut down operationally but stay powered.

#### 40.3.7.1 OST

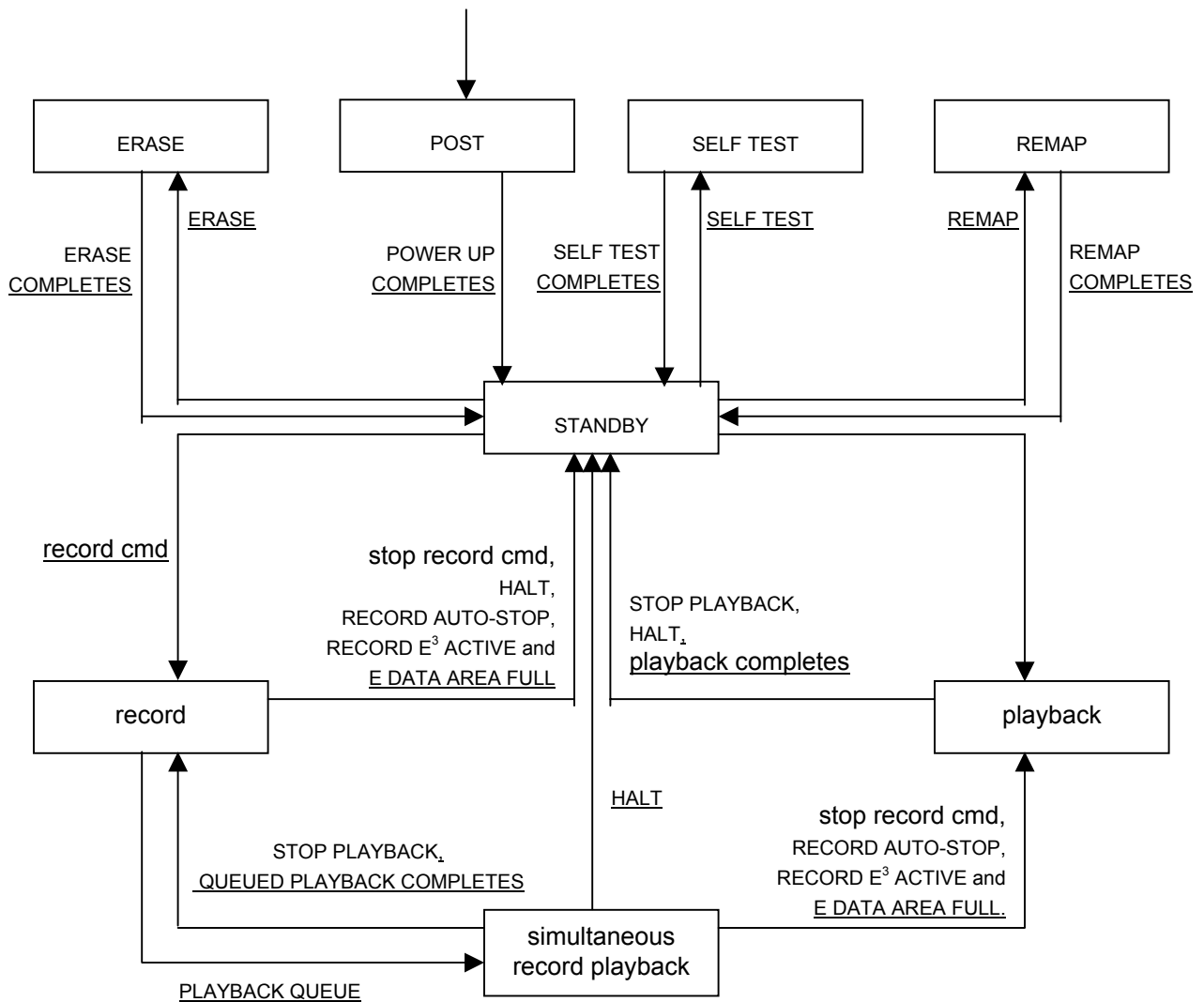
OST non-intrusively tests SBC, memory, and I/O functions. BITE telemetry is defined in the telemetry section. OST sub-test types and categories are listed in the following table:

**Table 40-5. OST types and categories**

| Test Description                   | Category | Card   |
|------------------------------------|----------|--------|
| SBC test                           | B        | SBC    |
| Tundra (PCI/VME interface) test    | C        | SBC    |
| Unexpected software exception      | A        | SBC    |
| PCI (internal SBC bus) bridge test | C        | SBC    |
| Bit errors uncorrectable by EDAC   | C        | Memory |
| I/O channel event queue overflow   | C        | I/O    |

### 40.4 MODES

The SSR subsystem behaves as a finite state machine. It shows the state transition diagram, which represents the high-level subsystem behavior.



**LEGEND:**

- A box  indicates a state.
- Uppercase state labels indicate a terminal state.
- Lowercase state labels indicate a non-terminal state (i.e., contains substates).
- A line with an arrow  indicates a transition between states.
- A line with text above it identifies the event condition(s) associated with the transition that is closest to the line.
- Uppercase transition labels indicate a terminal event condition.
- Lowercase transition labels indicate a non-terminal event condition.

**Figure 40-7. High-level state transition diagram**



#### 40.4.1 Power-On Self-Test Mode

When power is applied to the MMU, after all logic voltages are within tolerances, the POST software performs limited testing of the SBC, power supply, I/O circuitry, and memory, which takes about 70 seconds. Status outputs will be internally routed to command inputs for bit pattern testing. Dump outputs will be internally routed to record inputs for bit pattern testing. For the next 2 seconds after the end of POST, the SSR telemetry will indicate the BITE status of the SBC, SSR I/O card, and memory card, as well as the number of memory segments available. After this, the SSR will revert to the STANDBY mode. When power is cycled, all volatile memory is lost, including Playback Queue (PB QUE) slot definitions, protection definitions, and stored positions.

The BITE definitions can be found in the telemetry section of this systems brief. The following status conditions will exist following a nominal POST:

MODE = STBY      POSN = 162      SLOTS = 0      AUTO-STOP = INH  
PAR PROT = INH    BITE = GOOD

Table 40-6 lists POST subtest types and categories:

**Table 40-6. POST types and categories**

| Test description                            | Category | Card   |
|---|----------|--------|
| Tundra VME interface test                   | C        | SBC    |
| Block transfer test                         | C        | SBC    |
| Programmable timer test                     | C        | SBC    |
| Interrupt test                              | A        | SBC    |
| SBC test                                    | B        | SBC    |
| Combined timer test                         | A        | SBC    |
| RS-232 test                                 | C        | SBC    |
| PCI bridge test                             | C        | SBC    |
| SBC flash RAM checksum                      | A        | SBC    |
| Memory data test (first 5 Meg)              | C        | SBC    |
| Memory instruction test                     | C        | SBC    |
| Memory clear test (word)                    | C        | SBC    |
| Memory clear test (byte)                    | C        | SBC    |
| Memory random data test (byte, first 5 Meg) | C        | SBC    |
| Memory random data test (word, first 5 Meg) | C        | SBC    |
| Data I/O                                    | C        | I/O    |
| Status to command loop test                 | C        | I/O    |
| Registers (address/DMA/counter)             | C        | I/O    |
| Block transfer                              | C        | I/O    |
| Register read/write                         | C        | Memory |
| EDAC logic test                             | C        | Memory |
| Block transfer                              | C        | Memory |

#### 40.4.2 Standby Mode

Following POST or after being commanded to the standby mode, the SSR will not be performing any record or playback operations. The SSR must be in the standby mode in order to perform any of the following commanded actions: nonqueued PB, main engine PB, store position, recall position, erase, self-test, remap, and reset. The SSR will ignore any commands inappropriate for a current mode and set a command reject error bit. Also note that a command to a mode that already is in effect will cause a reject (see Table 40-8 for valid commands per mode).

#### 40.4.3 Erase Mode

In this mode, the SSR will erase all user non-volatile memory areas and write all ones. This action is normally done only at John F. Kennedy Space Center (KSC) between missions to remove old data from the MMUs. At the end of the erase cycle, which lasts about 3 seconds, the SSR will return to the standby mode.

#### 40.4.4 Comprehensive Self-Test Mode

In this mode, the SSR will perform self-tests of all the SSR cards. This is the most comprehensive of all tests available and will normally be done only at KSC between flights. At the end of the self-test cycle, which lasts about 175 seconds, the SSR will return to the standby mode after outputting the CST results for 10 seconds. Specific tests performed in this mode are listed in Table 40-7.

**Table 40-7. CST types and categories**

| Test description                                    | Category | Card   |
|---|----------|--------|
| Dump outputs loop to inputs (A1, A2, B, E1, E2, E3) | C        | I/O    |
| Command/status loop                                 | C        | I/O    |
| Register and block transfer                         | C        | I/O    |
| RS-232 test   | C        | SBC    |
| Ethernet interfaces                                 | C        | SBC    |
| Tundra and block transfer                           | C        | SBC    |
| User timers and combined timers                     | A        | SBC    |
| Interrupt and PCI bridge                            | C        | SBC    |
| DRAM marching address (5 Mbytes)                    | C        | SBC    |
| SBC   | B        | SBC    |
| DRAM data, memory clear & instruction               | C        | SBC    |
| DRAM walk a bit (5 Mbytes)                          | C        | SBC    |
| DRAM random data (5 Mbytes)                         | C        | SBC    |
| DRAM non-destructive marching bits                  | C        | SBC    |
| EDAC (5 Mbytes)                                     | C        | SBC    |
| EDAC fail & logic                                   | C        | Memory |
| Registers, remap, block                             | C        | Memory |

#### 40.4.5 Remap Mode

In this mode, the SSR will test each memory location by writing ones and zeroes to determine which 256 Kbyte cells to exclude. When finished, the SBC will remap the logical to physical addressing, and the mapping will be stored in NVM. Remapping could permanently decrease the recording capacity of the SSR. The remap will normally be done only at KSC. At the end of the remap cycle of about 63 minutes, the SSR will return to the standby mode. The first 162 good segments will be allocated to the E data area. The number of segments available to the user will be indicated in telemetry at the end of the remap.

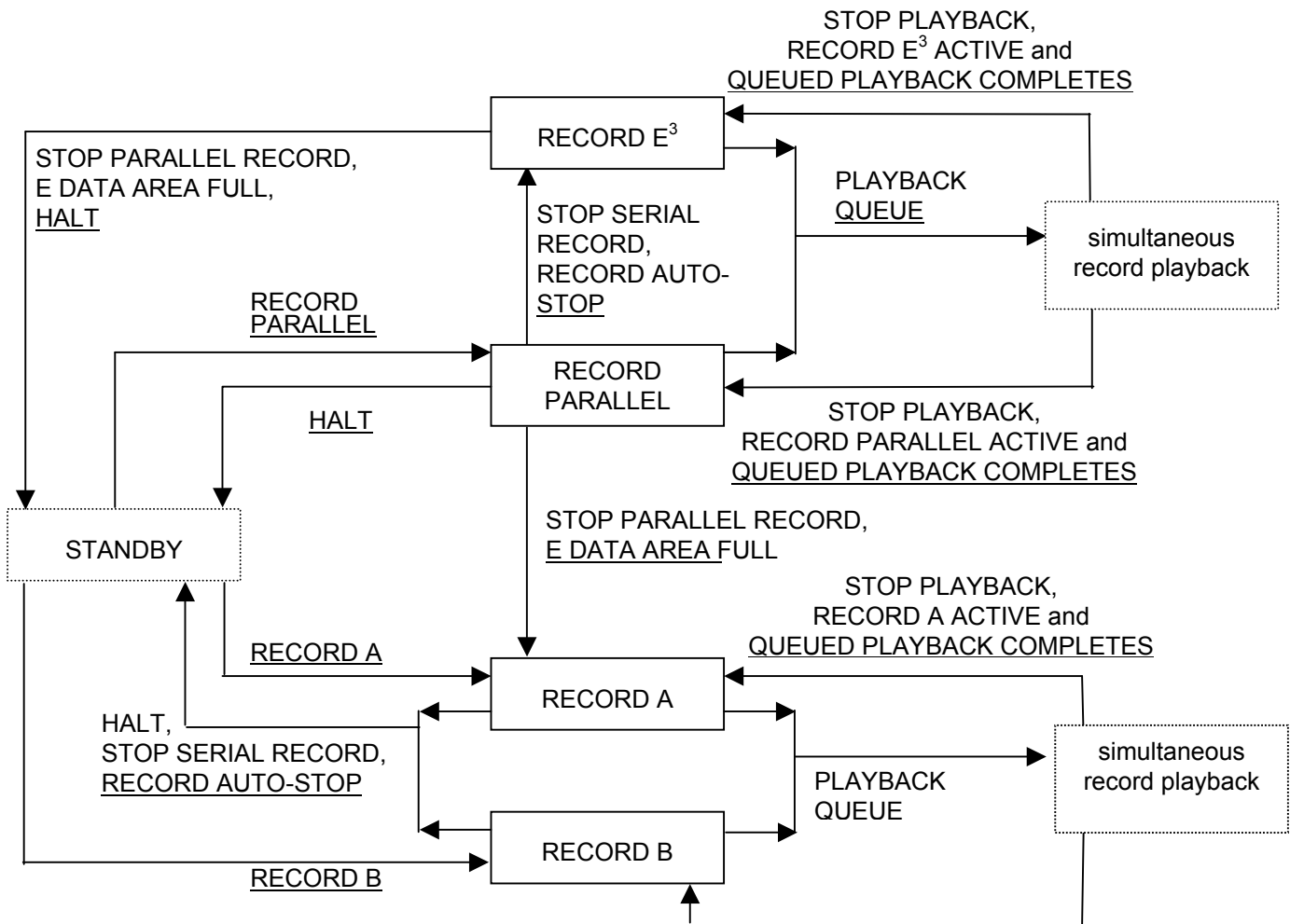
#### 40.4.6 Record Modes

The SSR can record one serial input and three parallel inputs, either alone or simultaneously, depending on which record mode is selected. It shows the state transition diagram for the record modes.

As described later, record modes can occur simultaneously with a queued PB mode. The mode indicated by the SSR will depend on which of the several recording and/or PB operations are in progress.

The SBC will monitor the I/O storage process and maintain the physical-to-logical mapping of the data. The SBC also maintains pointers for protected data (described later). If a recording operation is commanded to overwrite protected data, those protected segments will be skipped, and the recording will resume on the next available unprotected segment. The SSR erases ahead in 256 Kbyte blocks before recording data.

A halt command will terminate all recording and playback operations.



**Figure 40-8. State diagram for record modes**

#### 40.4.6.1 Serial Record Modes

The SSR can record the data appearing at either A1 (NSP1), A2 (NSP2), or B (payload) inputs. Also, the SSR can record serial A data simultaneously with parallel E type data, which is explained in Section 40.4.6.2. A command to stop parallel recording will return the SSR to the record A mode. A serial record mode can be executed while performing a queued PB, as long as the current PB location stays at least one position away from the record position.

Either the A inputs or the B input will be selected by command (both cannot be recorded simultaneously). If the A inputs are selected, the exclusive OR of the two A inputs is recorded, which means the SSR cannot record data from both A inputs simultaneously. The SBC will enable the appropriate mode to cue the I/O card to send the data to flash RAM. The data, although arriving in an unblocked serial stream, will be stored in 8-bit bytes in flash RAM.

When commanded to start recording serially, the data will be written from the beginning of the commanded segment. This ensures there are no partially empty segments to be dumped. The commanded position is either the position contained in the uplinked command or the current indicator position, which will be assumed if the commanded position is 1023 (via prebuilt Real-Time Command (RTC)).

While serially recording, the position indicator will always indicate the current logical serial recording position, regardless of any simultaneous dumping in progress. While serially recording, the position indicator will skip over protected data, along with the recording process. The serial recording will stop upon encountering the position equal to the auto-stop position, if currently enabled. When position 810 is full, the recording operation will continue uninterrupted to 0 as the next position.

#### 40.4.6.2 Parallel Record Modes

The SSR in MMU 2 can be commanded to start recording all three main Engine (E) data streams **and** one serial A input. If payload data is routed to one or more of the E data inputs on MMU 1, parallel recording will enable recording of all applied E inputs, as well as the serial A input. A command to stop recording serial input data will place the SSR in a mode with only the applicable E inputs being recorded, although this latest mode (record E<sup>3</sup>) cannot be entered from the standby mode.

When the last available E data segment is filled in one of the E data regions, the E recording will stop, returning the SSR to the serial A mode if fully parallel or to the standby mode if in the record E<sup>3</sup> mode.

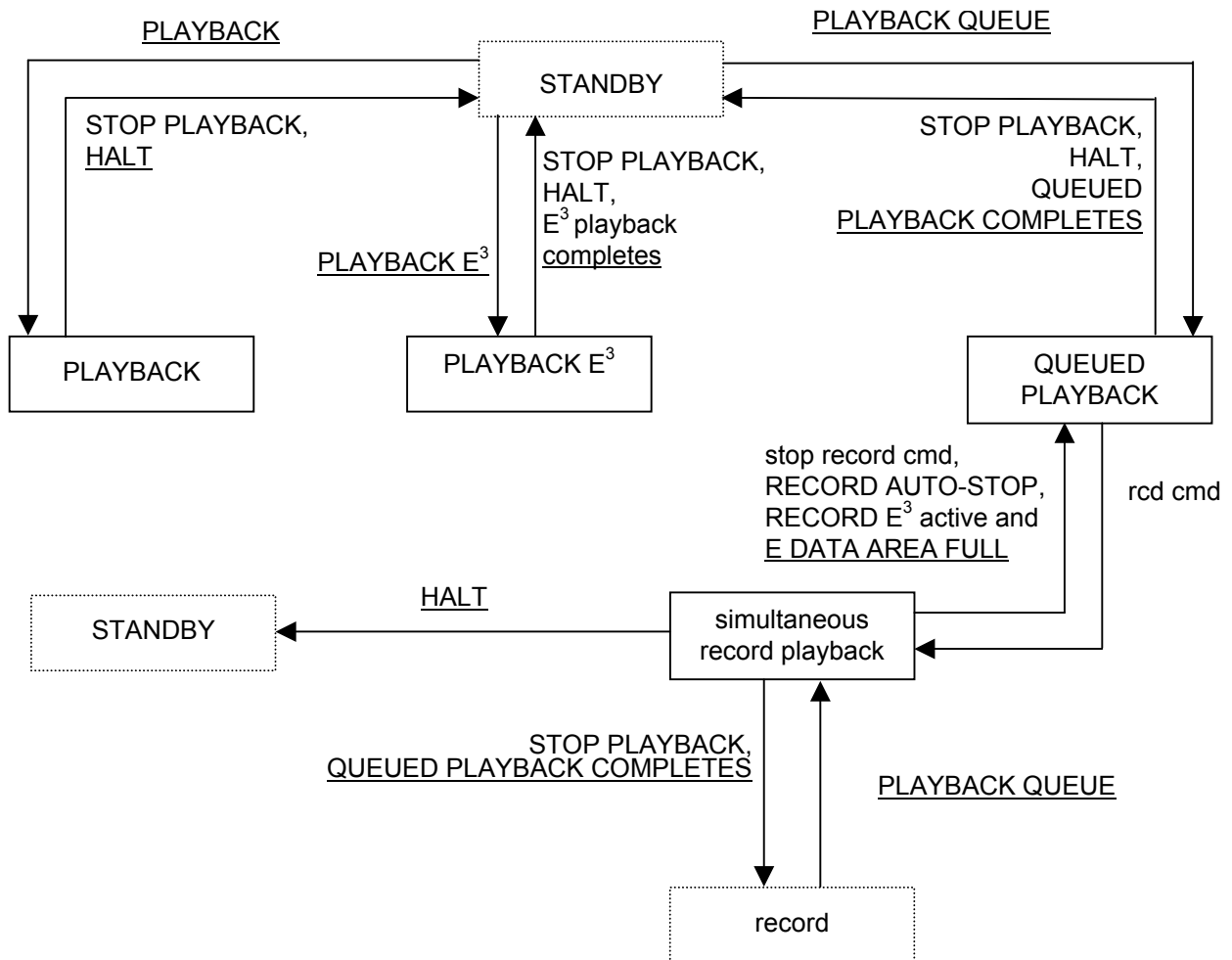
The SBC maintains a pointer to the start and end of each active E data recording segment for use later when the data is dumped. The end pointer is also used to resume recording of E data in the event of a temporary interruption either by data loss or by command. When commanded to start recording E data, the SSR will skip the last partially recorded segment to ensure no E data is overwritten.

When recording E data, if a segment that has been protected by being defined in a PB QUE is encountered, that data segment will not be overwritten by the E data.

When entering the parallel record mode, the SSR will protect the E data area from serial recording until the unprotect parallel command is sent.

#### 40.4.7 Playback Modes

The SSR will perform queued PB at a specified rate while recording simultaneously. The SSR will also perform all PB modes (in the forward direction) when not recording. Figure 40-9 shows the state transition diagram for the PB modes. If position 810 is encountered while dumping, the dump will continue uninterrupted to position 0.



**Figure 40-9. State transition diagram for PB modes**

#### 40.4.7.1 Playback (Non-queued)

If commanded in standby mode, the SSR will serially PB data at a commanded rate of 32, 64, 128, 192, 960, 1024, or 2048 Kbps, starting at the position stored in the command. If the commanded position is 1023 (via prebuilt RTC), the PB will start at the current position. All data segments will be dumped in sequence, regardless of protection status. If there is no data in a segment, the all-ones data produced by the erase function will be dumped. The PB will continue until the SSR is commanded to stop PB (or halt).

In the PB mode, there is no record operation ongoing, and the position indicator will indicate the current PB position.

#### 40.4.7.2 Queued PB

From standby or a record mode, the SSR will serially PB all data identified within queued slots of a defined rate, including 128, 192, 960, 1024, and 2048 Kbps. For example, a PBQ 1024 command will initiate the PB of all data defined in 1024 PB QUEs in sequential order of queue definition (in the forward direction). Defining commands and actions will be described later.

The queued PB will continue until all queues of that rate are dumped or until a stop PB command is sent. As previously stated, a halt command will stop all record and PB operations in the SSR. After a PB QUE is completely dumped, the queue definitions and protection will be discarded, and the SSR will decrement the queue slot count. After all PB QUEs of that data rate have been dumped, the SSR will return to the standby mode or record mode, per the state transition diagram.

#### 40.4.7.3 PB Main Engine Data

From the standby mode, the SSR will PB all three E data areas at 960 kbps or only one E data area per command at 60 kbps. Since the SSR is not recording at that time, the position indicator will indicate the current PB position.

When commanded to PB all main engine data, the SSR will begin dumping at the start of the E1 area, continue until all the E1 recorded data is dumped, and continue dumping all E2 and E3 data in the same manner. If a dump is interrupted before completion, the dump can be restarted at the beginning. Or, if the operator knows that one or two E areas have been dumped, a 960 PB can be performed from the start of the E2 or E3 data until dump sync lock goes away at the ground site. A Stop PB or Halt will stop the PB.

If the E areas are dumped individually by the special PB E1 (2,3) commands, they will be dumped at 60 kbps, and the dump will automatically stop at the end of E data recorded and protected in that particular E data area.

### 40.5 COMMANDS

The table of commands appears at the end of this section. Most of the SSR commanding functionality can be deduced by the mode description in previous sections. There are also special commands that define, unprotect, or clear definitions. Buildable SSR positional commands are built per SCP 3.22 with position data embedded in the command. Prebuilt positional commands contain 1023 for the position data, which indicates current position.

If a command is sent that is invalid for the current mode, or if sequential commands are not received by the SSR in the expected sequence, the CREJ telemetry will go low, and the display will show CREJ for BITE. Table 40-8 details the proper commanding actions that avoid triggering a CREJ.

Most SSR commands are divided into a 6-bit mode OP code and 10 position bits per this command bit example (example command is RCDA @16, HEX command = 0410):

| MSB          |   |   |   |   |   |               |   |   |   |   |   | LSB |   |   |   |
|--------------|---|---|---|---|---|---------------|---|---|---|---|---|-----|---|---|---|
| MODE OP CODE |   |   |   |   |   | POSITION BITS |   |   |   |   |   |     |   |   |   |
| 0            | 0 | 0 | 0 | 0 | 1 | 0             | 0 | 0 | 0 | 0 | 1 | 0   | 0 | 0 | 0 |
| 0            |   |   |   |   |   | 4             |   |   |   | 1 |   | 0   |   |   |   |

#### 40.5.1 Store/Recall Position

There are two positional indicator storage registers in the SSR. When the SSR is stopped, the store position 1(2) command can be used to save the current position in register 1(2). The recall position 1(2) command can be used to return a stopped SSR to the previously stored position so that a previously interrupted operation can be resumed at that position. The position number is saved in the register until overwritten by the next store position command.

#### 40.5.2 Define/Clear Record Auto-Stop Position

A serial record auto-stop position can be defined at any position on the SSR. It remains enabled until cleared via an auto-stop clear RTC. A telemetry bit is set when auto-stop is defined and cleared when auto-stop is cleared. Serial recording will stop when the recording position equals the auto-stop position.

#### 40.5.3 Unprotect Parallel

This command causes the cancellation of overwrite protection of the E data areas so that they can be used for recording serial input data. If a segment is also protected as part of a PB QUE, it will stay protected until the slot is cleared by the normal methods.

#### 40.5.4 Define/Clear PB Queue

There are 15 slots, numbered 1 through F<sub>HEX</sub>, that contain the definitions for PB QUEs. These queues are defined by pairs of commands that include start position, end position, and PB rate. When a queue is defined, the slot count being telemetered to the ground will increment by one. Slot numbers are maintained in the SSR such that the ground can uplink a command to clear slot n, at which time the slot will be cleared and the higher numbered slots will decrement position numbers by one. The ground must use the SSR program rules to keep track of queue numbers in order to clear the appropriate slot. There also is a command to clear all slots.

A queued segment is protected from overwriting by a record mode. Any string of positions can be protected by defining within a queue. If the operator does not want to dump the queue, an improbable PB rate can be defined. If the operator defines a queue that includes another queue within, the inner queue will be redumped with the latest queue. This can be avoided by defining two queues that do not include the inner queue.



**40.5.5 Reset**

The reset command will clear the user defined pointers. After reset, all volatile data will be gone, and the SSR status will appear the same as following a power cycle (Section 40.4.1). Table 40-8, the SSR pre-built command table, follows.

**Table 40-8. SSR command table**

| DSM  | COMMAND TITLE      | SAFE | MSID      | COMMAND DATA BITS   |
|------|--------------------|------|-----------|---------------------|
| 9200 | SSR1 RCDA          | U    | V75K6500U | 0009 FFFF 0809 07FF |
| 9201 | SSR1 RCDB          | U    | V75K6501U | 0009 FFFF 0809 0BFF |
| 9202 | SSR1 RCDP          | U    | V75K6502U | 0009 FFFF 0809 0FFF |
| 9203 | SSR1 PB2048        | U    | V75K6503U | 0009 FFFF 0809 13FF |
| 9204 | SSR1 PB1024        | U    | V75K6504U | 0009 FFFF 0809 17FF |
| 9205 | SSR1 PB960         | U    | V75K6505U | 0009 FFFF 0809 1BFF |
| 9206 | SSR1 PB192         | U    | V75K6506U | 0009 FFFF 0809 1FFF |
| 9207 | SSR1 PB128         | U    | V75K6507U | 0009 FFFF 0809 23FF |
| 9208 | SSR1 PB64          | U    | V75K6508U | 0009 FFFF 0809 27FF |
| 9209 | SSR1 PB32          | U    | V75K6509U | 0009 FFFF 0809 2BFF |
| 9210 | SSR1 PB ME 960     | U    | V75K6510U | 0009 FFFF 0809 2C00 |
| 9211 | SSR1 PB E1 60      | U    | V75K6511U | 0009 FFFF 0809 2C01 |
| 9212 | SSR1 PB E2 60      | U    | V75K6512U | 0009 FFFF 0809 2C02 |
| 9213 | SSR1 PB E3 60      | U    | V75K6513U | 0009 FFFF 0809 2C03 |
| 9214 | SSR1 PB QUE 2048   | U    | V75K6514U | 0009 FFFF 0809 3400 |
| 9215 | SSR1 PB QUE 1024   | U    | V75K6515U | 0009 FFFF 0809 3401 |
| 9216 | SSR1 PB QUE 960    | U    | V75K6516U | 0009 FFFF 0809 3402 |
| 9217 | SSR1 PB QUE 192    | U    | V75K6517U | 0009 FFFF 0809 3403 |
| 9218 | SSR1 PB QUE 128    | U    | V75K6518U | 0009 FFFF 0809 3404 |
| 9219 | SSR1 CLR PBQ ALL   | SAFE | V75K6519U | 0009 FFFF 0809 3810 |
| 9220 | SSR1 CLR PBQ 1     | U    | V75K6520U | 0009 FFFF 0809 3801 |
| 9221 | SSR1 CLR PBQ 2     | U    | V75K6521U | 0009 FFFF 0809 3802 |
| 9222 | SSR1 CLR PBQ 3     | U    | V75K6522U | 0009 FFFF 0809 3803 |
| 9223 | SSR1 CLR PBQ 4     | U    | V75K6523U | 0009 FFFF 0809 3804 |
| 9224 | SSR1 CLR PBQ 5     | U    | V75K6524U | 0009 FFFF 0809 3805 |
| 9225 | SSR1 CLR PBQ 6     | U    | V75K6525U | 0009 FFFF 0809 3806 |
| 9226 | SSR1 CLR PBQ 7     | U    | V75K6526U | 0009 FFFF 0809 3807 |
| 9227 | SSR1 CLR PBQ 8     | U    | V75K6527U | 0009 FFFF 0809 3808 |
| 9228 | SSR1 CLR PBQ 9     | U    | V75K6528U | 0009 FFFF 0809 3809 |
| 9229 | SSR1 CLR PBQ A     | U    | V75K6529U | 0009 FFFF 0809 380A |
| 9230 | SSR1 CLR PBQ B     | U    | V75K6530U | 0009 FFFF 0809 380B |
| 9231 | SSR1 CLR PBQ C     | U    | V75K6531U | 0009 FFFF 0809 380C |
| 9232 | SSR1 CLR PBQ D     | U    | V75K6532U | 0009 FFFF 0809 380D |
| 9233 | SSR1 CLR PBQ E     | U    | V75K6533U | 0009 FFFF 0809 380E |
| 9234 | SSR1 CLR PBQ F     | U    | V75K6534U | 0009 FFFF 0809 380F |
| 9235 | SSR1 STOP SER RCD  | U    | V75K6535U | 0009 FFFF 0809 3C00 |
| 9236 | SSR1 STOP PAR RCD  | U    | V75K6536U | 0009 FFFF 0809 4000 |
| 9237 | SSR1 CLR AUTO STOP | U    | V75K6537U | 0009 FFFF 0809 4800 |
| 9238 | SSR1 STOP PB       | U    | V75K6538U | 0009 FFFF 0809 4C00 |

**Table 40-8. SSR command table (continued)**

| DSM  | COMMAND TITLE     | SAFE | MSID      | COMMAND DATA BITS   |
|------|-------------------|------|-----------|---------------------|
| 9239 | SSR1 STORE POS1   | U    | V75K6539U | 0009 FFFF 0809 5000 |
| 9240 | SSR1 STORE POS2   | U    | V75K6540U | 0009 FFFF 0809 5001 |
| 9241 | SSR1 RECALL POS1  | U    | V75K6541U | 0009 FFFF 0809 5400 |
| 9242 | SSR1 RECALL POS2  | U    | V75K6542U | 0009 FFFF 0809 5401 |
| 9243 | SSR1 UNPROT PAR   | SAFE | V75K6543U | 0009 FFFF 0809 5800 |
| 9244 | SSR1 ERASE ENA    | SAFE | V75K6544U | 0009 FFFF 0809 5E00 |
| 9245 | SSR1 ERASE EXEC   | SAFE | V75K6545U | 0009 FFFF 0809 5E01 |
| 9246 | SSR1 RESET ENA    | SAFE | V75K6546U | 0009 FFFF 0809 6200 |
| 9247 | SSR1 RESET EXEC   | SAFE | V75K6547U | 0009 FFFF 0809 6201 |
| 9248 | SSR1 REMAP ENA    | SAFE | V75K6548U | 0009 FFFF 0809 6600 |
| 9249 | SSR1 REMAP EXEC   | SAFE | V75K6549U | 0009 FFFF 0809 6601 |
| 9250 | SSR1 SLF TST ENA  | SAFE | V75K6550U | 0009 FFFF 0809 6A00 |
| 9251 | SSR1 SLF TST EXEC | SAFE | V75K6551U | 0009 FFFF 0809 6A01 |
| 9252 | SSR1 HALT         | U    | V75K6552U | 0009 FFFF 0809 FFFF |
| 9300 | SSR2 RCDA         | U    | V75K6600U | A08A FFFF A88A 07FF |
| 9301 | SSR2 RCDB         | U    | V75K6601U | A08A FFFF A88A 0BFF |
| 9302 | SSR2 RCDP         | U    | V75K6602U | A08A FFFF A88A 0FFF |
| 9303 | SSR2 PB2048       | U    | V75K6603U | A08A FFFF A88A 13FF |
| 9304 | SSR2 PB1024       | U    | V75K6604U | A08A FFFF A88A 17FF |
| 9305 | SSR2 PB960        | U    | V75K6605U | A08A FFFF A88A 1BFF |
| 9306 | SSR2 PB192        | U    | V75K6606U | A08A FFFF A88A 1FFF |
| 9307 | SSR2 PB128        | U    | V75K6607U | A08A FFFF A88A 23FF |
| 9308 | SSR2 PB64         | U    | V75K6608U | A08A FFFF A88A 27FF |
| 9309 | SSR2 PB32         | U    | V75K6609U | A08A FFFF A88A 2BFF |
| 9310 | SSR2 PB ME 960    | U    | V75K6610U | A08A FFFF A88A 2C00 |
| 9311 | SSR2 PB E1 60     | U    | V75K6611U | A08A FFFF A88A 2C01 |
| 9312 | SSR2 PB E2 60     | U    | V75K6612U | A08A FFFF A88A 2C02 |
| 9313 | SSR2 PB E3 60     | U    | V75K6613U | A08A FFFF A88A 2C03 |
| 9314 | SSR2 PB QUE 2048  | U    | V75K6614U | A08A FFFF A88A 3400 |
| 9315 | SSR2 PB QUE 1024  | U    | V75K6615U | A08A FFFF A88A 3401 |
| 9316 | SSR2 PB QUE 960   | U    | V75K6616U | A08A FFFF A88A 3402 |
| 9317 | SSR2 PB QUE 192   | U    | V75K6617U | A08A FFFF A88A 3403 |
| 9318 | SSR2 PB QUE 128   | U    | V75K6618U | A08A FFFF A88A 3404 |
| 9319 | SSR2 CLR PBQ ALL  | SAFE | V75K6619U | A08A FFFF A88A 3810 |
| 9320 | SSR2 CLR PBQ 1    | U    | V75K6620U | A08A FFFF A88A 3801 |
| 9321 | SSR2 CLR PBQ 2    | U    | V75K6621U | A08A FFFF A88A 3802 |
| 9322 | SSR2 CLR PBQ 3    | U    | V75K6622U | A08A FFFF A88A 3803 |
| 9323 | SSR2 CLR PBQ 4    | U    | V75K6623U | A08A FFFF A88A 3804 |
| 9324 | SSR2 CLR PBQ 5    | U    | V75K6624U | A08A FFFF A88A 3805 |
| 9325 | SSR2 CLR PBQ 6    | U    | V75K6625U | A08A FFFF A88A 3806 |
| 9326 | SSR2 CLR PBQ 7    | U    | V75K6626U | A08A FFFF A88A 3807 |
| 9327 | SSR2 CLR PBQ 8    | U    | V75K6627U | A08A FFFF A88A 3808 |
| 9328 | SSR2 CLR PBQ 9    | U    | V75K6628U | A08A FFFF A88A 3809 |
| 9329 | SSR2 CLR PBQ A    | U    | V75K6629U | A08A FFFF A88A 380A |
| 9330 | SSR2 CLR PBQ B    | U    | V75K6630U | A08A FFFF A88A 380B |

**Table 40-8. SSR command table (concluded)**

| DSM  | COMMAND TITLE      | SAFE | MSID      | COMMAND DATA BITS   |
|------|--------------------|------|-----------|---------------------|
| 9331 | SSR2 CLR PBQ C     | U    | V75K6631U | A08A FFFF A88A 380C |
| 9332 | SSR2 CLR PBQ D     | U    | V75K6632U | A08A FFFF A88A 380D |
| 9333 | SSR2 CLR PBQ E     | U    | V75K6633U | A08A FFFF A88A 380E |
| 9334 | SSR2 CLR PBQ F     | U    | V75K6634U | A08A FFFF A88A 380F |
| 9335 | SSR2 STOP SER RCD  | U    | V75K6635U | A08A FFFF A88A 3C00 |
| 9336 | SSR2 STOP PAR RCD  | U    | V75K6636U | A08A FFFF A88A 4000 |
| 9337 | SSR2 CLR AUTO STOP | U    | V75K6637U | A08A FFFF A88A 4800 |
| 9338 | SSR2 STOP PB       | U    | V75K6638U | A08A FFFF A88A 4C00 |
| 9339 | SSR2 STORE POS1    | U    | V75K6639U | A08A FFFF A88A 5000 |
| 9340 | SSR2 STORE POS2    | U    | V75K6640U | A08A FFFF A88A 5001 |
| 9341 | SSR2 RECALL POS1   | U    | V75K6641U | A08A FFFF A88A 5400 |
| 9342 | SSR2 RECALL POS2   | U    | V75K6642U | A08A FFFF A88A 5401 |
| 9343 | SSR2 UNPROT PAR    | SAFE | V75K6643U | A08A FFFF A88A 5800 |
| 9344 | SSR2 ERASE ENA     | SAFE | V75K6644U | A08A FFFF A88A 5E00 |
| 9345 | SSR2 ERASE EXEC    | SAFE | V75K6645U | A08A FFFF A88A 5E01 |
| 9346 | SSR2 RESET ENA     | SAFE | V75K6646U | A08A FFFF A88A 6200 |
| 9347 | SSR2 RESET EXEC    | SAFE | V75K6647U | A08A FFFF A88A 6201 |
| 9348 | SSR2 REMAP ENA     | SAFE | V75K6648U | A08A FFFF A88A 6600 |
| 9349 | SSR2 REMAP EXEC    | SAFE | V75K6649U | A08A FFFF A88A 6601 |
| 9350 | SSR2 SLF TST ENA   | SAFE | V75K6650U | A08A FFFF A88A 6A00 |
| 9351 | SSR2 SLF TST EXEC  | SAFE | V75K6651U | A08A FFFF A88A 6A01 |
| 9352 | SSR2 HALT          | U    | V75K6652U | A08A FFFF A88A FFFF |

## 40.6 TELEMETRY

The telemetry for each SSR is divided between two cards on two OI MDMs. MDM OF1, cards 02 and 10 are used for SSR1, and MDM OF2, cards 02 and 10 are used for SSR2. The sample telemetry in Table 40-9 indicates recording serial A input at position 810, with seven slots active:

**Table 40-9. SSR telemetry table**

| Bit | SSR1 MSIDs | SSR2 MSIDs | Usage            | Sample |
|-----|------------|------------|------------------|--------|
| 28  | V75X2966E  | V75X2866E  | MODE BIT 6 MSB   | 0      |
| 27  | V75X2965E  | V75X2865E  | MODE BIT 5       | 0      |
| 26  | V75X2957E  | V75X2857E  | MODE BIT 4       | 0      |
| 25  | V75X2956E  | V75X2856E  | MODE BIT 3       | 0      |
| 24  | V75X2955E  | V75X2855E  | MODE BIT 2       | 1      |
| 23  | V75X2944E  | V75X2844E  | MODE BIT 1 LSB   | 0      |
| 22  | V75X2943E  | V75X2843E  | BITE (CBF)       | 1      |
| 21  | V75X2942E  | V75X2842E  | BITE (NCBF)      | 1      |
| 20  | V75X2941E  | V75X2841E  | SLOT COUNT MSB   | 0      |
| 19  | V75X2940E  | V75X2840E  | SLOT COUNT BIT 3 | 1      |
| 18  | V75X2931E  | V75X2831E  | SLOT COUNT BIT 2 | 1      |

**Table 40-9. SSR telemetry table (concluded)**

| Bit | SSR1 MSIDs | SSR2 MSIDs | Usage             | Sample |
|-----|------------|------------|-------------------|--------|
| 17  | V75X2929E  | V75X2829E  | SLOT COUNT LSB    | 1      |
| 16  | V75X2927E  | V75X2827E  | CST (I/O CMD)     | 1      |
| 15  | V75X2923E  | V75X2823E  | CST (I/O ADD REG) | 1      |
| 14  | V75X2922E  | V75X2822E  | CST (I/O VME REG) | 1      |
| 13  | V75X2960E  | V75X2860E  | CMD REJECT        | 1      |
| 12  | V75X2959E  | V75X2859E  | AUTO-STOP ENA     | 0      |
| 11  | V75X2950E  | V75X2850E  | PAR PROTECTED     | 0      |
| 10  | V75X2949E  | V75X2849E  | POSITION MSB      | 1      |
| 9   | V75X2948E  | V75X2848E  | POSITION BIT 9    | 1      |
| 8   | V75X2947E  | V75X2847E  | POSITION BIT 8    | 0      |
| 7   | V75X2934E  | V75X2834E  | POSITION BIT 7    | 0      |
| 6   | V75X2933E  | V75X2833E  | POSITION BIT 6    | 1      |
| 5   | V75X2921E  | V75X2821E  | POSITION BIT 5    | 0      |
| 4   | V75X2913E  | V75X2813E  | POSITION BIT 4    | 1      |
| 3   | V75X2911E  | V75X2811E  | POSITION BIT 3    | 0      |
| 2   | V75X2909E  | V75X2809E  | POSITION BIT 2    | 1      |
| 1   | V75X2905E  | V75X2805E  | POSITION LSB      | 0      |

There are 45 valid modes and up to 15 slots, and valid positions are 0 to 810. The auto-stop and parallel protect enable bits are true when a high level is transmitted.

Switch scans for power telemetry are V72S7185E for MMU1 and V72S7186E for MMU2.

This Table 40-10 provides the SSR mode telemetry.

**Table 40-10. SSR mode telemetry**

| Val | Mode    | Description  |
|-----|---------|--|
| 0   | NONE    | MMU problem or loss of mode telemetry                              |
| 1   | STBY    | Standby, no record or playback or maintenance operation in process |
| 2   | RCDA    | Recording Serial A, NSP1 (2) data or data and voice                |
| 3   | RCDB    | Recording Serial B, payload input                                  |
| 4   | RCDE    | Recording main engine or payload data at the EIU1 (2, 3) inputs    |
| 5   | RCDP    | Recording three EIU inputs and Serial A input                      |
| 6   | PB2048  | Dumping at 2048 kbps   |
| 7   | PB1024  | Dumping at 1024 kbps   |
| 8   | PB960   | Dumping at 960 kbps  |
| 9   | PB192   | Dumping at 192 kbps  |
| 10  | PB128   | Dumping at 128 kbps  |
| 11  | PB64    | Dumping at 64 kbps   |
| 12  | PB32    | Dumping at 32 kbps   |
| 13  | PBME    | Dumping all EIU data in 1,2,3 order at 960 kbps                    |
| 14  | PB E1   | Dumping EIU1 data at 60 kbps                                       |
| 15  | PB E2   | Dumping EIU2 data at 60 kbps                                       |
| 16  | PB E3   | Dumping EIU3 data at 60 kbps                                       |
| 17  | PBQ2048 | Dumping all data slots queued at 2048 kbps                         |

**Table 40-10. SSR mode telemetry (concluded)**

| Val | Mode     | Description   |
|-----|----------|---|
| 18  | PRQ1024  | Dumping all data slots queued at 1024 khns                                  |
| 19  | PBQ960   | Dumping all data slots queued at 960 kbps                                   |
| 20  | PBQ192   | Dumping all data slots queued at 192 kbps                                   |
| 21  | PBQ128   | Dumping all data slots queued at 128 kbps                                   |
| 22  | A/PB2048 | Simultaneously recording serial A data and dumping per mode 17              |
| 23  | A/PB1024 | Simultaneously recording serial A data and dumping per mode 18              |
| 24  | A/PB960  | Simultaneously recording serial A data and dumping per mode 19              |
| 25  | A/PB192  | Simultaneously recording serial A data and dumping per mode 20              |
| 26  | A/PB128  | Simultaneously recording serial A data and dumping per mode 21              |
| 27  | B/PB2048 | Simultaneously recording serial B data and dumping per mode 17              |
| 28  | B/PB1024 | Simultaneously recording serial B data and dumping per mode 18              |
| 29  | B/PB960  | Simultaneously recording serial B data and dumping per mode 19              |
| 30  | B/PB192  | Simultaneously recording serial B data and dumping per mode 20              |
| 31  | B/PB128  | Simultaneously recording serial B data and dumping per mode 21              |
| 32  | P/PB2048 | Simultaneously recording per mode 5 and dumping per mode 17                 |
| 33  | P/PB1024 | Simultaneously recording per mode 5 and dumping per mode 18                 |
| 34  | P/PB960  | Simultaneously recording per mode 5 and dumping per mode 19                 |
| 35  | P/PB192  | Simultaneously recording per mode 5 and dumping per mode 20                 |
| 36  | P/PB128  | Simultaneously recording per mode 5 and dumping per mode 21                 |
| 37  | E/PB2048 | Simultaneously recording per mode 4 and dumping per mode 17                 |
| 38  | E/PB1024 | Simultaneously recording per mode 4 and dumping per mode 18                 |
| 39  | E/PB960  | Simultaneously recording per mode 4 and dumping per mode 19                 |
| 40  | E/PB192  | Simultaneously recording per mode 4 and dumping per mode 20                 |
| 41  | E/PB128  | Simultaneously recording per mode 4 and dumping per mode 21                 |
| 42  | ERASE    | Erasing all NVM (maintenance function)                                      |
| 43  | REMAP    | Destructive remapping of NVM to exclude bad segments (maintenance function) |
| 44  | TEST     | Nondestructive in-depth self-testing (maintenance function)                 |
| 45  | POST     | Power-on self-test mode   |
| >45 | INVAL    | Values of 46 through 63 are invalid   |

#### 40.6.1 BITE Telemetry

BITE telemetry is mode dependent. POST telemetry applies to the end of the POST mode cycle, CST telemetry applies to the end of the self-test cycle, and OST telemetry applies to all other modes.

**Table 40-11. OST telemetry**

| SSR 1         | SSR 2     | FAIL = | DESCRIPTION                                   |
|---------------|-----------|--------|---|
| V75X2         | V75X2843E | 0      | Critical BITE Failure (CBF)                   |
| V75X2         | V75X2842E | 0      | Non-critical BITE Failure (NCBF)              |
| V75X2<br>960F | V75X2860E | 0      | Command Rejected by SSR (Table 40-14 & 40-15) |

**Table 40-12. POST telemetry**

| SSR 1     | SSR 2     | FAIL = | DESCRIPTION                    |
|-----------|-----------|--------|--------------------------------|
| V75X2943E | V75X2843E | 0      | SBC No-Go                      |
| V75X2942E | V75X2842E | 0      | I/O Card No-Go                 |
| V75X2941E | V75X2841E | 0      | Memory Card No-Go              |
| V75X2949E | V75X2849E | N/A    | Available Memory Positions MSB |
| V75X2948E | V75X2848E | N/A    | Available Memory Positions     |
| V75X2947E | V75X2847E | N/A    | Available Memory Positions     |
| V75X2934E | V75X2834E | N/A    | Available Memory Positions     |
| V75X2933E | V75X2833E | N/A    | Available Memory Positions     |
| V75X2921E | V75X2821E | N/A    | Available Memory Positions     |
| V75X2913E | V75X2813E | N/A    | Available Memory Positions     |
| V75X2911E | V75X2811E | N/A    | Available Memory Positions     |
| V75X2909E | V75X2809E | N/A    | Available Memory Positions     |
| V75X2905E | V75X2805E | N/A    | Available Memory Positions LSB |

**Table 40-13. CST telemetry**

| SSR 1     | SSR 2     | FAIL = | DESCRIPTION                            |
|-----------|-----------|--------|--|
| V75X2943E | V75X2843E | 0      | I/O card Engine 1 channel loop or SRAM |
| V75X2942E | V75X2842E | 0      | I/O card Engine 2 channel loop or SRAM |
| V75X2941E | V75X2841E | 0      | I/O card Engine 3 channel loop or SRAM |
| V75X2940E | V75X2840E | 0      | I/O card A1 channel loop or A/B SRAM   |
| V75X2931E | V75X2831E | 0      | I/O card A2 channel loop or A/B SRAM   |
| V75X2929E | V75X2829E | 0      | I/O card B channel loop or A/B SRAM    |
| V75X2927E | V75X2827E | 0      | I/O card MDM CMD, CMD FIFO, output     |
| V75X2923E | V75X2823E | 0      | I/O card address registers             |
| V75X2922E | V75X2822E | 0      | I/O card VME interface registers       |
| V75X2960E | V75X2860E | 0      | I/O card SRAM D64BLT, I/O D64BLT       |
| V75X2959E | V75X2859E | 0      | I/O card interrupt                     |
| V75X2950E | V75X2850E | 0      | SBC Tundra VME interface               |
| V75X2949E | V75X2849E | 0      | SBC user timers and combined timers    |
| V75X2948E | V75X2848E | 0      | SBC system DRAM memory data/address    |
| V75X2947E | V75X2847E | 0      | SBC ECC logic – long (1 Kbyte)         |
| V75X2934E | V75X2834E | 0      | SBC EEPROM check-sum                   |
| V75X2933E | V75X2833E | N/A    | Set to "1"                             |
| V75X2921E | V75X2821E | 0      | Flash memory registers                 |
| V75X2913E | V75X2813E | 0      | Flash memory remap circuit             |
| V75X2911E | V75X2811E | 0      | Flash memory block transfer D64BLT     |
| V75X2909E | V75X2809E | 0      | Flash memory EDAC logic                |
| V75X2905E | V75X2805E | 0      | Flash memory image EEPROM check-sum    |

**Table 40-14. Valid modes per command**

| COMMAND      | VALID ONLY IN THESE MODES   |
|--------------|---|
| RCD A        | STBY, PB Q modes 17-21  |
| RCD B        | STBY, PB Q modes 17-21  |
| RCD PAR      | STBY, PB Q modes 17-21  |
| PB (non QUE) | STBY  |
| PB ME        | STBY  |
| PB QUE       | STBY, RCD A, RCD B, RCD PAR, RCD E3                                 |
| DEF PB QUE   | STBY, RCD A, RCD B, RCD PAR, RCD E3, PB (non QUE) – see table 40-15 |
| CLR PB QUE   | STBY, RCD A, RCD B, RCD PAR, RCD E3, PB (non QUE)                   |
| STOP SER RCD | Any mode that includes serial A or B recording                      |

**Table 40-14. Valid modes per command (concluded)**

|              |   |
|--------------|---|
| STOP PAR     | Any mode that includes E data recording             |
| STOP PB      | Any mode that includes PB QUE or PB (non QUE)       |
| DEF AUT STOP | Any mode except ERASE, POST, REMAP, SELF TEST       |
| CLR AUT STOP | Any mode except ERASE, POST, REMAP, SELF TEST       |
| STORE POSN   | STBY  |
| RECALL POSN  | STBY  |
| UNPROT PAR   | Any mode except ERASE, POST, REMAP, SELF TEST       |
| ERASE        | STBY – see table 40-15                              |
| RESET        | STBY – see table 40-15                              |
| REMAP        | STBY – see table 40-15                              |
| SELF TEST    | STBY – see table 40-15                              |
| HALT         | Any mode except STBY, ERASE, POST, REMAP, SELF TEST |

**Table 40-15. Sequential commanding requirements**

| THIS COMMAND MUST BE  | FOLLOWED BY THIS COMMAND            |
|-----------------------|-------------------------------------|
| DEF PB QUE START @nnn | DEF PB QUE END (various rates) @nnn |
| ERASE ENABLE          | ERASE EXECUTE                       |
| RESET ENABLE          | RESET EXECUTE                       |
| REMAP ENABLE          | REMAP EXECUTE                       |
| SELF TEST ENABLE      | SELF TEST EXECUTE                   |

## 40.7 REFERENCES

MMU Theory of Operations

JSC-12829, Instrumentation and Communications Officer (INCO) Console Handbook

JSC-11174, Space Shuttle Systems Handbook

**SECTION 47 - GROUND NETWORK**  
**CONTENTS**

| <b>Section</b> |                      | <b>Page</b> |
|----------------|----------------------|-------------|
| 47.1           | GENERAL .....        | 47-1        |
| 47.2           | A/G VOICE .....      | 47-2        |
| 47.3           | S-BAND PM LINK ..... | 47-3        |
| 47.4           | MISCELLANEOUS.....   | 47-5        |



THIS PAGE INTENTIONALLY BLANK

## SECTION 47 GROUND NETWORK

### 47.1 GENERAL

The shuttle vehicle requires support services for Air-to-Ground (A/G) voice (Ultrahigh Frequency (UHF) and S-band), television, tracking data, telemetry, and command services from the Mission Control Center (MCC) and the Ground Network (GN). The purpose of this brief is to address these support operations. C-band tracking, although important, is not discussed because it is noncooperative with the vehicle; i.e., skin tracking rather than beacon tracking.

Different ground sites have different capabilities. Because of the number of stations involved and the need to respond quickly to operational problems, this can lead to confusion.

Most of the difficulty in operating with the GN can be attributed to the lack of commonality in equipment. This, in turn, is largely due to the fact that the network is actually comprised of elements of three independent networks.

#### A. Ground Spacecraft Tracking and Data Network (GSTDN)

The GSTDN is a conglomeration of sites under the administrative and, for non-shuttle flights, operational control of the Goddard Space Flight Center (GSFC). To further complicate matters, there are four special implementation sites for launch, entry, Transatlantic Abort Landing (TAL), and UHF A/G voice within the GSTDN. The GSTDN is undergoing major equipment changes in the command and data handling equipment areas. The GSTDN sites are

- ACN - Ascension Island
- AGO - Santiago, Chile
- BDA - Bermuda
- DKR - Dakar, Senegal
- GWM - Guam
- HAW - Hawaii (Kauai)
- MIL - Merritt Island Launch Area
- PDL - Ponce de Leon, Florida, extension of MIL
- VAN - Vandenburg AFB, California
- YAR - Yarragadee, Australia

#### B. Deep Space Network (DSN)

The DSN is used chiefly for deep space probes. It is owned by NASA but administered and, for non-shuttle flights, operationally controlled by the Cal Tech Jet Propulsion Laboratory (JPL) under contract to NASA. The DSN sites are

- CAN - Canberra, Australia
- GDS - Goldstone, California
- MAD - Madrid, Spain

C. Department of Defense (DOD) Remote Tracking Site (RTS)

The USAF owns and operates the DOD RTS sites. These sites are not normally a part of the GN, except in those flights where the DOD has an interest, but may be called up for support when required.

GTS - Guam  
HTS - Hawaii  
IOS - Indian Ocean Station (Seychelle Islands)  
VTS - Vandenburg AFB, California  
OTS - Oak Hangar, England  
NHS - New Hampshire  
THS - Thule, Greenland (not Shuttle compatible)

D. Dryden Flight Research Facility (DFR)

The DFR site, owned and operated by NASA's Ames Research Center, has been equipped to support shuttle S-band links for landings at Edwards Air Force Base and for limited postflight operations such as dump and playback of the orbiter operational data recorders.

E. Electronic Systems Test Laboratory (ESTL)

Although it is not a true support site, the ESTL, located at the Johnson Space Center (JSC), can be called up for inflight support of shuttle S-band systems. It is listed here only for completeness.

F. Salinas Peak (SAL), White Sands Missile Range, New Mexico

Salinas Peak is a UHF voice-only site. It will be used only for landings at the Northrup Air Strip at the White Sands Missile Range in New Mexico. This is a contingency-only landing site.

## 47.2 A/G VOICE

Three types of A/G voice are handled within the GN. One of these, Ku-band, is handled only by the MILA site, only as part of preflight testing. It is not of concern here. The other two, UHF and S-band, are essential to normal GN operations.

A. UHF voice

The UHF voice system is a simplex, Amplitude Modulated (AM), standalone system that is compatible with current aircraft and air traffic control systems. It was originally implemented in the orbiter for terminal area communications, air-to-air communications, and Extravehicular Activity (EVA) communications. It has been found to be extremely useful in A/G also. Being an analog system, it is not compatible with encrypted voice. Voice is routed to the uplink site via analog line. A 450-cps tone originated in the MCC Quindar transmitter opens and closes each transmission and causes a Quindar receiver at the remote site to key and release

the UHF transmitter. The sites having UHF capability are shown in Figure 47-1 (TBS).

B. S-band voice

The S-band voice system consists of two full duplex digital voice channels (high data rate), or one full duplex channel (low data rate), time division multiplexed with command on the uplink and interleaved in the telemetry on the downlink. In the past, all voice was routed to the uplink GSTDN sites on analog lines. The site then digitized the voice and multiplexed it with the command data for uplink. The Quindar equipment was used to cue the site as to when to accept the voice for digitizing. Since the S-band voice is a full duplex system, this was not really necessary, but the analog lines afforded little protection against unauthorized transmissions, and the Quindar served as a block. When working with the RTS sites, the voice is digitized and the link is formatted at the MCC and throughput by the DOD network and sites.

In the future it is planned to take advantage of the shuttle encrypted communications capability to provide uplink protection. Since the sites have no capability to encrypt the forward link, encryption will have to be done at the MCC. MIL/PDL are an exception as they can encrypt the data. We intend to operate all sites in the throughput mode for the uplink; that is, the voice will be digitized, multiplexed with command and Bose-Chaudhuri-Hocquenghen (BCH) error code, and the entire stream organized into 600-bit communications protocol blocks at the MCC. The remote sites will deblock the transmission and modulate the carrier with the data received. Whether or not we can operate the uplink in high or low data rate is dependent on the outgoing circuit(s) to the site. The low data rate is 24 kbps, and the high data rate is 72 kbps. Sites capable of two-channel voice uplink (high data rate) are designated as "Command Throughput - HI" on Figure 47-2 (TBS). S-band downlink voice is discussed in Section 47.3.

The GSTDN sites will retain, for the immediate future, the capability to operate in the GSTDN nonthroughput mode. This requires reloading site computer software and should be done only if there is difficulty with cryptographic equipment. Three sites, DKR, DFR, and VAN, do not have the nonthroughput capability at present and will not be modified for it.

In the past, the remote site ComTech has monitored all uplink and downlink voice transmissions for quality and crew response. If the uplink or downlink is encrypted, only two sites, MIL and PDL, will have this capability.

### 47.3 S-BAND PM LINK

The S-band PM link is a phase-locked system. The forward link (uplink) contains a serial digital bit stream comprised of one or two voice channels (24 kbps low rate, 32 kbps each high), 8 kbps of command, and BCH error protection for a total of 32 or 72 kilobits. As noted above, the number of voice channels is dependent on the circuit,

or circuits, between the MCC and the site. There are two basic modes for GN, the STDN mode and the SGLS (RTS) mode. The only difference is in the uplink frequency.

The return link (downlink) is similar to the uplink in that voice is interleaved with telemetry. The frequency is the same for STDN and SGLS modes, there are two telemetry rates, and there is no BCH error protection. Low data rate telemetry includes one 32-kbps channel of voice and 64 kbps of telemetry. High data rate telemetry has two 32-kbps channels of voice and 128 kbps of telemetry. As with the uplink, selection of high or low data rate downlink depends on the bandwidth of the lines available from the specific site.

A. GSTDN, DSN, and DFR S-band PM data handling

Selected GSTDN sites (MIL/PDL, BDA, and VAN) and DFR have 224 kbps lines to the site as well as from the site. These sites can throughput high data rate uplink as shown in Table 47-1 (TBS). The remainder of the sites, except for YAR (which has UHF A/G only), have only one 56 kbps line available for forward link data and are constrained to low rate uplink throughput. The vehicle configuration must be changed to match.

Return link data handling is similarly constrained in the throughput mode. Only those GSTDN sites with 224-kbps lines for the return link (MIL/PDL, BDA, and VAN), GDS, and DFR can throughput high data rate telemetry and voice. All others can throughput only low data rate. However, GSTDN and DSN sites will retain a modified throughput capability, when the downlink is unencrypted, to strip out voice, convert it to analog, and route it to the MCC on separate voice lines. With the voice removed, the telemetry data can be throughput on the site three 56-kbps return data lines.

At the present time the only DSN sites which can handle encrypted data are GDS and CAN.

In addition to these standard capabilities, MIL/PDL and BDA have the capability to emulate the Tracking and Data Relay Satellite System (TDRSS). This capability is used in preflight checkout and would only be used in a contingency situation otherwise.

B. Shuttle Launch Support System (SLSS)

The SLSS mode of operation enables the site to emulate a TDRSS satellite; that is, error correction coding may be used on the forward or return link. This capability is provided at only two sites, MILA/PDL and VANS. The original intent was to enable launching the shuttle with TDRSS for support, while retaining ground station backup. It is now used for S-band transponder checkout prelaunch, and coding is used on the uplink during launch to aid in overcoming launch phase circuit margin losses due to booster flame attenuation, etc.

#### 47.4 MISCELLANEOUS

##### Antenna keyholes

Restricted S-band antenna pointing regions, because of constraints against radiating into the antenna drive structure (bymbals), are called keyholes. These are located at zenith for azimuth/elevation-mounted antennas (RTS/DKR/DFR and one VAN antenna) and along the horizon on the east/west axis (GSTDN) or north/south axis (DSN) for all others. Sites with multiple antennas (MIL, BDA and GDS) have one antenna drive oriented at 90° to the other. GSTDN keyholes are semiconical, about 10° high and 6° wide. The DSN keyholes are similarly shaped, but about 15° high and 10° wide. Although radiation is prohibited, sites can frequently track the vehicle through the keyhole.

Another phenomenon related to antenna drives is a mid-pass loss of lock for direct overhead passes. This is because the antenna elevation drive does not go from horizon to horizon, but from horizon to something just over 90°. In order to track the vehicle from horizon to horizon, the antenna azimuth drive must spin the assembly so that the elevation drive can then track from overhead down. This can result in a loss of lock.

THIS PAGE INTENTIONALLY BLANK

**SECTION 48 - TRACKING AND DATA RELAY SATELLITE SYSTEM**  
**CONTENTS**

| <b>Section</b> | <b>Page</b>   |
|----------------|---|
| 48.1           | GENERAL ..... 48-1                                      |
| 48.2           | TDRSS SPACE SEGMENT ..... 48-1                          |
| 48.2.1         | General ..... 48-1                                      |
| 48.2.2         | Satellite Bent Pipe Operation ..... 48-3                |
| 48.2.3         | Radio Frequency Interference ..... 48-5                 |
| 48.2.4         | Sun Outage ..... 48-6                                   |
| 48.2.5         | High Power Mode ..... 48-6                              |
| 48.2.6         | Frequencies Available for SSA and KSA ..... 48-6        |
| 48.2.7         | TDRS Malfunctions ..... 48-6                            |
| 48.3           | TDRSS GROUND SEGMENT ..... 48-7                         |
| 48.3.1         | Rain Propagation Effects ..... 48-7                     |
| 48.3.2         | Ku-Band Autotrack ..... 48-8                            |
| 48.3.3         | Bilateration Tracking ..... 48-8                        |
| 48.3.4         | Shuttle Services ..... 48-8                             |
| 48.3.5         | Forward Link Service ..... 48-9                         |
| 48.3.6         | Return Link Service ..... 48-12                         |
| 48.3.7         | SSA Combining ..... 48-12                               |
| 48.3.8         | Tracking and Doppler Compensation ..... 48-12           |
| 48.3.9         | Simulation Services ..... 48-15                         |
| 48.3.10        | TOCC ..... 48-15  |
| 48.3.11        | Fault Detection Within WSC ..... 48-16                  |
| 48.3.12        | Logging ..... 48-16                                     |
| 48.3.13        | ADPE ..... 48-16  |
| 48.3.14        | ADPE Data Bases ..... 48-17                             |
| 48.3.15        | Data Interface System ..... 48-17                       |
| 48.3.16        | Operation Interface ..... 48-17                         |
| 48.3.17        | Data Types ..... 48-19                                  |
| 48.3.18        | Data Quality Monitoring ..... 48-19                     |
| 48.3.19        | Data Storage ..... 48-19                                |
| 48.3.20        | Shuttle TV Processing ..... 48-20                       |
| 48.3.21        | Emergency Voice ..... 48-20                             |
| 48.3.22        | Command Echo ..... 48-20                                |
| 48.3.23        | Forward and Return Link Simulation ..... 48-20          |
| 48.4           | NETWORK CONTROL CENTER ..... 48-22                      |
| 48.4.1         | Scheduling ..... 48-22                                  |
| 48.4.2         | GCMRs ..... 48-26                                       |
| 48.5           | DATA THRESHOLDS (reference EE8/Sid Novosad) ..... 48-33 |
| 48.5.1         | S-Band Forward ..... 48-33                              |
| 48.5.2         | S-Band Return ..... 48-33                               |
| 48.5.3         | Ku-Band Forward ..... 48-33                             |
| 48.5.4         | Ku-Band Return ..... 48-33                              |



| Section |                                    | Page  |
|---------|------------------------------------|-------|
| 48.6    | OTHER SYSTEM CHARACTERISTICS ..... | 48-34 |
| 48.7    | REFERENCE .....                    | 48-34 |

## TABLES

### Table

|      |  |       |
|------|--|-------|
| 48-1 | Proposed TDRS Configuration for RTF (3/05) ..... | 48-7  |
| 48-2 | SHO contents .....                               | 48-23 |
| 48-3 | GCMR message contents .....                      | 48-28 |
| 48-4 | GCM denial rejection codes .....                 | 48-32 |

## FIGURES

### Figure

|      |   |       |
|------|---|-------|
| 48-1 | TDRSS lower coverage zone, definition of coverage zone notation ..... | 48-2  |
| 48-2 | Single-access beamwidth .....   | 48-4  |
| 48-3 | SSA forward service link .....  | 48-10 |
| 48-4 | KSA forward service link .....  | 48-11 |
| 48-5 | SSA return link processing .....                                      | 48-13 |
| 48-6 | KSA return link processing .....                                      | 48-14 |
| 48-7 | NASCOM interface functional block diagram .....                       | 48-18 |
| 48-8 | TDRS network .....  | 48-21 |

## SECTION 48 TRACKING DATA AND RELAY SATELLITE SYSTEM

### 48.1 GENERAL

The Tracking and Data Relay Satellite System (TDRSS) will eventually provide all orbital support for orbiter communications. The bulk of the ground sites (Ground Spaceflight Tracking and Data Network (GSTDN)) except those required for ascent, entry, Department of Defense (DOD), supplemental TV, and contingency support will be gradually phased out and their function assumed by the TDRSS which will consist of three operational satellites, several on-orbit spares, two or three ground spares, the White Sands Ground Terminal (WSGT), the Second TDRS Ground Terminal (STGT) (which comprise the White Sands Complex [WSC]), and the Guam Remote Ground Terminal (GRGT). Both WSGT and STGT are located near Las Cruces, New Mexico. The TDRSS consists of a space segment and a ground segment.

### 48.2 TDRSS SPACE SEGMENT

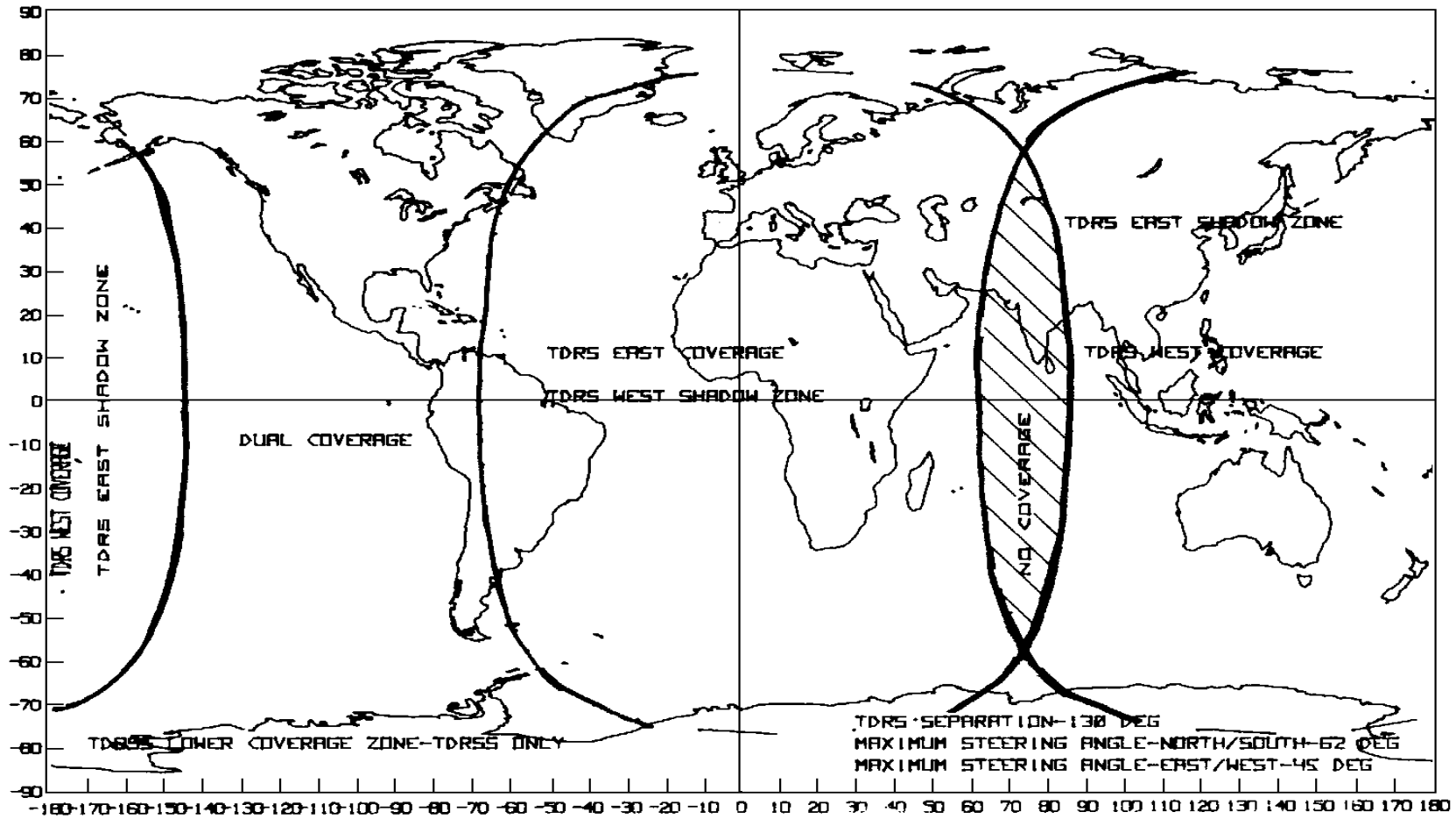
#### 48.2.1 General

Five geosynchronous satellites are available for communication with the Orbiter.

|            |         |
|------------|---------|
| TDRS West  | 174° W. |
| TDRS 171   | 171° W. |
| TDRS East  | 41° W.  |
| TDRS Spare | 46° W.  |
| TDRS Z     | 275° W. |

With these locations, a Zone of Exclusion (ZOE) exists over the Indian Ocean between 2 and 15 minutes long for spacecraft altitudes below 1200 km (no ZOE at 1200 km). At typical orbiter altitudes, the geometric orbital coverage is approximately 90 percent (55 percent with one satellite) and exceeds 94 percent at polar inclinations. Currently, TDRS Z, controlled by GRGT, is positioned to cover this ZOE. See Figure 48-1.

All nominal transmission for shuttle data relay and satellite housekeeping support between each satellite and WSC or GRGT is via Ku-band (a backup S-band capability exists but is not usable for relaying shuttle links). This Ku-band space-to-ground link using 18 m ground antennas is susceptible to attenuation because of rain and cloud cover, and the good weather at White Sands was a major criteria for the selection of both ground stations at this location.



Note

User altitude is 500 km.

Figure 48-1. TDRSS lower coverage zone, definition of coverage zone notation

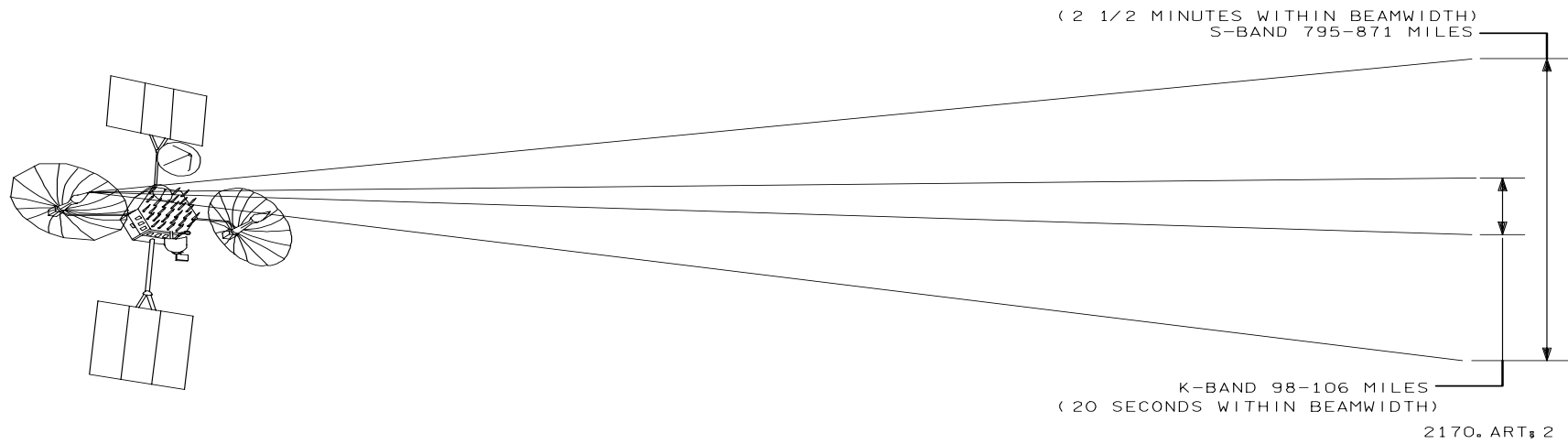
TDRS support can be divided into two types: Single Access (SA) and Multi-Access (MA). The MA service is provided for up to 20 simultaneous low data rate users (less than 50 Kbps return link and 10 Kbps forward link), involves the use of an S-band MA-phased array satellite antenna and does not interfere with SA service. Since shuttle does not use MA service, it will not be mentioned further. SA service applies to users exceeding MA data rate limits. Each satellite uses two 4.9-meter antennas to provide two Ku-band SA (KSA) and two S-band SA (SSA) services simultaneously; one KSA and one SSA from each SA antenna. Currently, only one vehicle can be supported by each antenna due to software limitations, even if colocated.

#### **48.2.1.1 KSA and SSA Services**

Although KSA and SSA services share the same 4.9-meter parabolic antenna, different antenna feeds and sets of electronics are used. Initial pointing is strictly open loop; i.e., the antenna is simply pointed at the predicted location of the shuttle based on state vectors (ICVs) provided by JSC to Goddard Space Flight Center (GSFC) usually once each hour. For S-band support (SSA), the WSC continues to send pointing angles and a program track mode is established. At the  $1.8^\circ$  SSA beamwidth, a spacecraft in low Earth orbit can be in an 800-mile area of support (which would take about 2-1/2 minutes to traverse) and still remain in the beamwidth. This implies that program track at S-band will be sufficient. The  $0.28^\circ$  KSA beamwidth, however, is designed to include an acquisition sequence involving pull-in and autotrack procedures in order to maintain the link. This beamwidth results in a 100-mile area of support in low Earth orbit which would only take 20 seconds to traverse. See Figure 48-2. All autotrack processing is done in the ground terminal using data from the onboard autotrack receiver and 5-horn feed. Known errors due to thermal distortions and other reasons are corrected and pointing commands are uplinked to maintain pointing accuracy within  $0.06^\circ$  at a maximum rate of 0.25 deg/s. There is no search capability. Once autotrack is achieved, the return link threshold can drop 3 dB without dropping out. If autotrack is used for Ku-band whenever a forward link is scheduled, a return link should also be scheduled. Experience has shown that adequate Ku-band pointing can be done without autotrack enabled (program track). This seems to provide more accurate pointing near the Earth's horizon and is now the normal mode of operation. Autotrack enable/disable has recently been implemented as a function reconfigurable by Ground Configuration Message Request (GCMR) from the GSFC Network Control Center (NCC) but not remotely from Mission Control Center (MCC) as are other reconfigurables.

#### **48.2.2 Satellite Bent Pipe Operation**

The TDRS basically acts as a bent pipe repeater relaying signals to and from WSC. Frequency conversion, amplification, multiplexing, and demultiplexing of the SA, MA, and housekeeping channels is all that the satellite can accomplish. The data processing equipment is located at WSC to increase system reliability and is described later. In brief, the satellite bent pipe operation is as follows.



**Figure 48-2. Single-access beamwidth**

A. Forward Link

WSC transmits a composite signal which is comprised of MA, SSA (1 and/or 2), KSA (1 and/or 2), and Tracking, Telemetry and Control (TT&C) (housekeeping and pilot tone) information. This composite signal is received by the spacecraft 2-meter, Ku-band Space Ground Link (SGL) antenna which is continuously pointed to the ground terminal using ground commands. The Ku-band receiver translates the uplink signal to an intermediate frequency, amplifies it and sends it to the forward processing assembly which filters and demultiplexes this composite signal into the five (or seven) separate signals originally multiplexed at the ground terminal. The MA portion of the signal (unused by shuttle) is translated to S-band and sent to the MA 30 element phased array. The SSA output from the forward processor is routed to a 26-watt Traveling Wave Tube Amplifier (TWTA) for transmission. The KSA signal is sent to a KSA upconverter to a 1.5-watt TWTA for transmission. The TT&C portion is sent to the TT&C subsystem after downconversion. The forward processor assembly sends the pilot tone signal to the spacecraft master frequency generator as a control reference for all local oscillator frequencies. Dual TWTA redundancy is provided for both SSA and KSA.

B. Return Link

Return link operation is similar to forward link operation except the flow is reversed. KSA and SSA received signals at the 4.9-meter antenna are isolated from the transmit signals by diplexers, amplified by parametric amplifiers, downconverted to intermediate frequencies, and sent to the return processor assembly. The MA return link signals are received by the phased array antenna elements, downconverted, frequency division multiplexed, and routed to the return processor assembly. The return processor assembly accepts the MA signal, TDRS housekeeping telemetry, the downlink pilot tone, the one or two SSA signals, and either one of the two KSA signals and multiplexes them into a single composite signal for Ku-band upconversion, 30-watt amplification and transmission to the ground terminal over the KSA 2 downlink channel. The remaining KSA signal (KSA 1) is filtered, amplified, and routed directly to a second dedicated downlink channel.

As backup to the K-band satellite to ground link, a fail-safe timing circuit (Emergency Timeout (ETO) timer) returns the system to S-band (originally used only during deployment) any time validated satellite commands are not received during a predetermined time interval. If this should happen, MA, SSA, and KSA transmission is automatically terminated. Encryption is bypassed and a powerdown is accomplished.

Dual redundancy is provided for the paramps, downconverters, and forward and return processing assemblies.

### 48.2.3 Radio Frequency Interference

Radio Frequency Interference (RFI) is predicted to cause a problem to SSA service whenever the shuttle is over the European, Australian, Northern Africa, and Asian

continental areas. Mutual interference from co-orbiting satellites has also been seen, especially at high frequency. Since many of these satellites use the shuttle high frequency, routine use of low frequency (assuming no other constraints from payloads) is preferred.

#### 48.2.4 Sun Outage

No SSA or KSA return link service is available when the center of the Sun is within 4° (S-band) or 1° (Ku-band) of the SA antenna boresight which occurs near Earth horizon, respectively; or within 1° of the boresight of the ground (18-meter) antenna supporting that TDRS. The MCC will be verbally advised by NCC when the 18-meter ground antenna Sun outage occurs (primarily during the equinox).

#### 48.2.5 High Power Mode

Normal forward link signal Effective Isotropic Radiated Power (EIRP) is a minimum of 43.6 dBW and 47.0 dBW for SSA and KSA links, respectively. A high power mode of operation can be scheduled by MCC to increase these figures to approximately 48.5 dBW and 49.3 dBW, respectively. Typically high power is scheduled.

#### 48.2.6 Frequencies Available for SSA and KSA

|         |  |
|---------|--|
| SSA FWD | 2025.833 to 2117.917 MHz<br>adjustable in 0.46 MHz steps |
| SSA RTN | 2200 to 2300 MHz<br>adjustable in 0.5 MHz steps          |
| KSA FWD | 13775 ± 1.6 MHz  |
| KSA RTN | 15003.4 ± 1.6 MHz  |

#### 48.2.7 TDRS Malfunctions

The current TDRS configuration contains satellite malfunctions on TDRS W-171 and TDRS-Z. On TDRS W-171, denoted TDRS-5, SA-1 Ku-Band forward is failed. Under this condition, the Shuttle and ISS cannot operate simultaneously on TDRS W-171. Therefore, the Shuttle will use TDRS-5 (171°) SA-2 while the ISS uses TDRS-8 (174°). Due to a small number of conflicts for ISS on TDRS-8, if the Shuttle launch slips, TDRS-5 becomes available to ISS.

On TDRS-Z, denoted TDRS-3, the SA-2 S-band TWTA is failed, and the SA-2 Ku-Band is restricted to Left Circular Polarization. The Shuttle requires Right Circular Polarization (RCP) while the ISS requires Left Circular Polarization (LCP). Under these conditions, the Shuttle uses SA-1 S-Band and Ku-Band while the ISS uses SA-2 S-Band (return only) and Ku-Band (forward and return). The ISS control team can still send commands to the ISS through the "Big Loop".

It is worth mention that TDRS-3 has outlived its lifespan and is currently the oldest satellite in the constellation that is still used by Shuttle and ISS.

**Table 48-1. TDRS Configuration for RTF**

| <b>Location</b> | <b>Designation</b> | <b>Relevant Malfunctions</b>   |
|-----------------|--------------------|--|
| TDW-171         | TDRS-5             | Failed SA-1 Ku-Band forward  |
| TDW             | TDRS-8             |  |
| TDE             | TDRS-10            |  |
| TDS             | TDRS-4             |  |
| TDZ             | TDRS-3             | SA-2 Ku-Band restricted to LCP (no link to Shuttle)<br>SA-2 S-band TWTA failed |

### **48.3 TDRSS GROUND SEGMENT**

Two operating ground station facilities are located at White Sands, New Mexico and Guam. The White Sands Complex consists of two terminals 3 miles apart. Each terminal includes three 18-meter, Ku-band parabolic antennas providing all normal communications with two TDRSs and one spare, an S-band telemetry and command antenna providing backup control but not data relay for all three satellites, Ku-band and S-band simulation and verification rooftop antennas providing shuttle simulation signals and TDRSS diagnostic tests, and an axial ratio measurement antenna.

Since no orbiter signal processing is done on the satellite, all hardware for modulation/demodulation of the signals to and from the orbiter is implemented at WSC. Other functions include mode and redundancy control of satellite communications equipment, gain and power level control of all channels, antenna pointing, Ku-band autotrack and acquisition processing, spectrum analysis, and providing the interface with NASA-owned equipment. Each of the two terminals (WSGT and STGT) have three Space-to-Ground Link Terminals (SGLTs), each of which supports two S-band and two Ku-band links from/to a single satellite. The three SGLTs interface with a Data Interface System (DIS), which provides the interface to the NASCOM common carrier. Each SGLT is redundant in a hot standby mode. A fiber optic Interfacility Link (IFL) connects the two terminals.

The Guam Remote Ground Terminal (GRGT) is responsible for TDRS-Z, which covers the area that is excluded from the satellites that interact with WSC.

#### **48.3.1 Rain Propagation Effects**

One of the primary reasons for the selection of White Sands was the very low rainfall frequency. Rain can cause large Radio Frequency (RF) propagation losses at Ku-band. The satellite-to-ground link is sized to meet requirements with up to 6 dB of rain loss



except for the KSA composite downlink which is sized for a 2.5-dB rain loss. Actual Electronic Systems Test Laboratory (ESTL) measurements have shown that greater than 10 dB attenuation in the Ku-band satellite-to-ground link does not significantly degrade performance.

#### **48.3.2 Ku-Band Autotrack**

Autotrack signal processing is performed on the ground using signals from the satellite Ku-band 5-horn feed. The S-band feed does not have autotracking capability; open loop pointing by the ground provides adequate pointing accuracy. Both SSA and KSA transmit and receive polarizations are GCMR-selectable; either Left-Hand Circular Polarization (LHCP) or Right-Hand Circular Polarization (RHCP). The two autotrack error signals, one for each pointing axis, are added to the data channel, sent to the ground, processed (if autotrack is enabled), and used to generate pointing commands to close the autotrack pointing loop, and keep the TDRS antenna pointed at the orbiter. In general, the 0.28° beamwidth Ku-band antenna is open loop pointed (based on GSFC-provided ephemeris data) to within 0.24° of the orbiter position. Once acquisition occurs, the TDRSS autotracks with a 0.22° accuracy and pulls in until the accuracy is maintained at less than 0.06°. Autotrack enable/disable will be configurable via GCMR, initially by voice request only from MCC to NCC. Nominally, autotrack will not be scheduled, as it seems to degrade performance near the horizon.

#### **48.3.3 Bilateral Tracking**

To provide accurate pointing data and an accurate Doppler tracking count, the satellite positions must be very accurately known. Ranging measurements are planned for 5 minutes each hour for each satellite using NASA standard transponders at White Sands, Ascension Island, Samoa, and Alice Springs, Australia. Distance measurements are calculated and used to update the WSC database. One of the satellite MA channels is typically used for these range measurements as well as for receiving housekeeping data from these unattended transponders comprising the Bilateral Tracking System (BRTS).

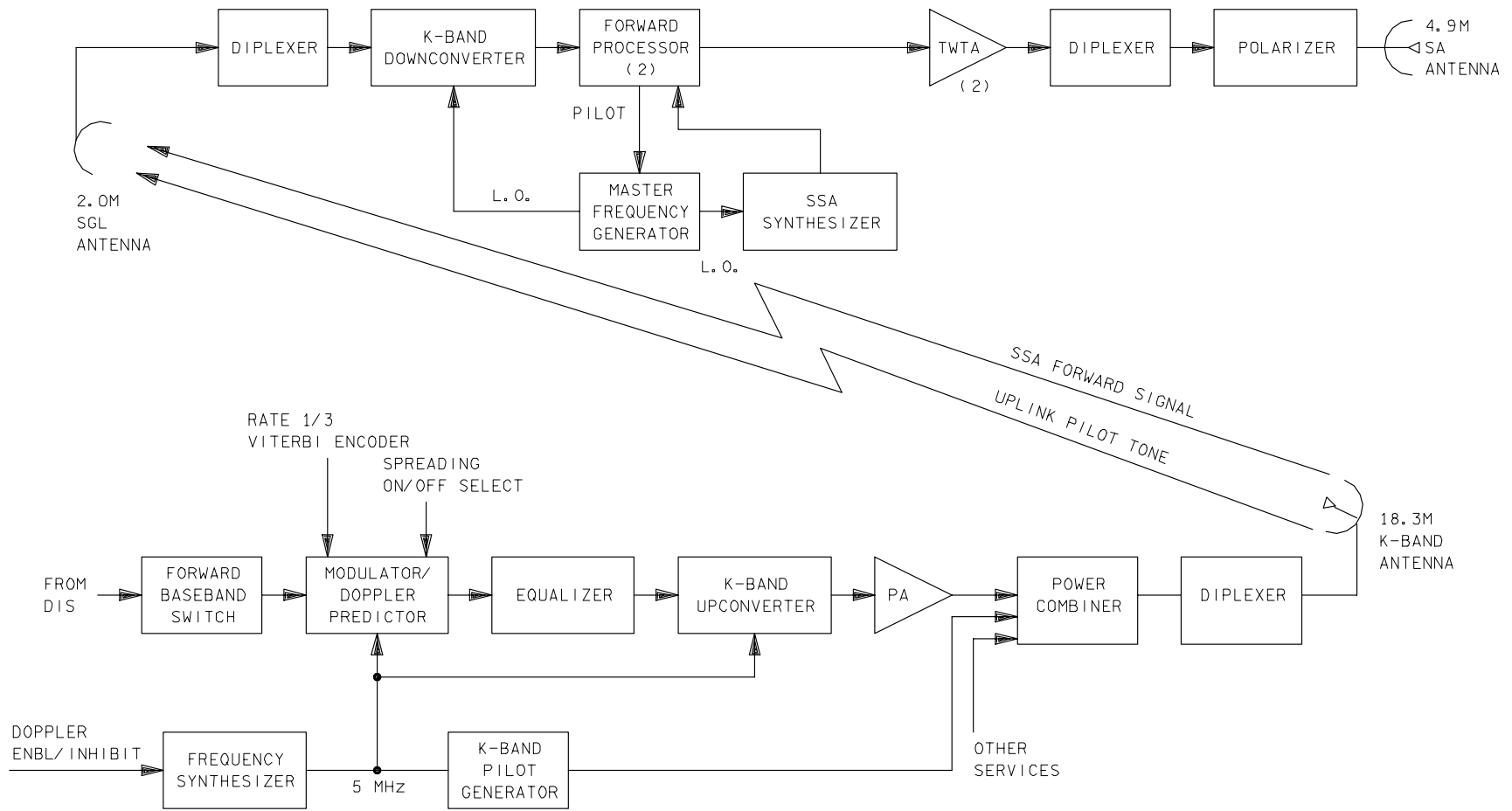
#### **48.3.4 Shuttle Services**

The basic concept of operations at WSC is to not perform data reduction - only throughput. Forward and return link services for both S- and Ku-band must be scheduled by the Network Control Center (NCC) at GSFC (with inputs from JSC and other users), and these services will begin and end exactly at the scheduled times. Scheduling is further described later in this brief. The operation of the ground station is almost entirely computer controlled by the Automatic Data Processing Equipment (ADPE) system. This system has two general processors and eight minicomputers to perform schedule conflict detection, acquisition, equipment reconfiguration, equipment failure recovery, autotrack computations, ephemeris maintenance, etc. The TDRS Operations Control Center (TOCC) is the control room at WSC that monitors and controls the satellites once on orbit and operational and are informed of all failures, conflicts, and any corrective action taken by the computer. These automatic procedures can be manually overridden by the TOCC if desired, but this is not considered normal

operation. A second control room, the TDRSS Launch and Deployment Control Center (TLDCC), is used for initial launch/deploy support. Emergency support is also available at TRW in Redondo Beach.

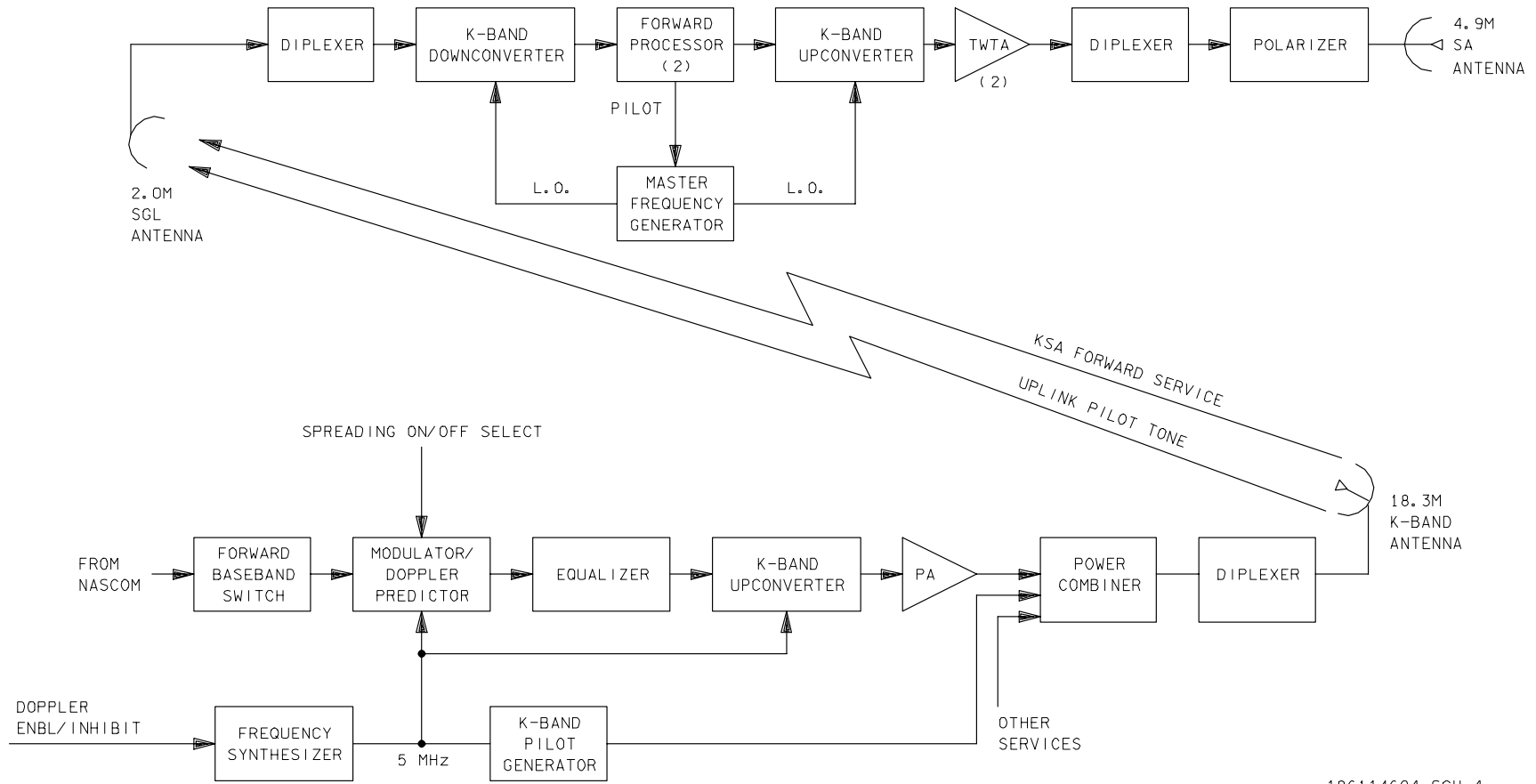
#### **48.3.5 Forward Link Service**

If SSA forward link service has been scheduled, the MCC Up-Down Link (UDL) Front End Processor (FEP) outputs a 32 kbps or 72 kbps S-band data stream to the NASCOM interface (MDM) at JSC where it is relayed via a Wide Area Network (WAN) consisting of multiple T-1 links to the NASCOM interface at White Sands. These data are then quality checked, then it is rate 1/3 encoded, spread spectrum modulated with a Pseudo Noise (PN) code (if so scheduled by MCC), combined with other SSA services and TT&C for that satellite, modulated, upconverted, uplinked, and relayed to the designated satellite antenna (1 or 2) for relay to the orbiter. Ku-band support is similar except that the input is either 72 kbps or 216 kbps and the link is NOT encoded. See Figure 48-3 and Figure 48-4.



186114603, SCH 4

Figure 48-3. SSA forward service link



186114604, SCH 4

Figure 48-4. KSA forward service link

### 48.3.6 Return Link Service

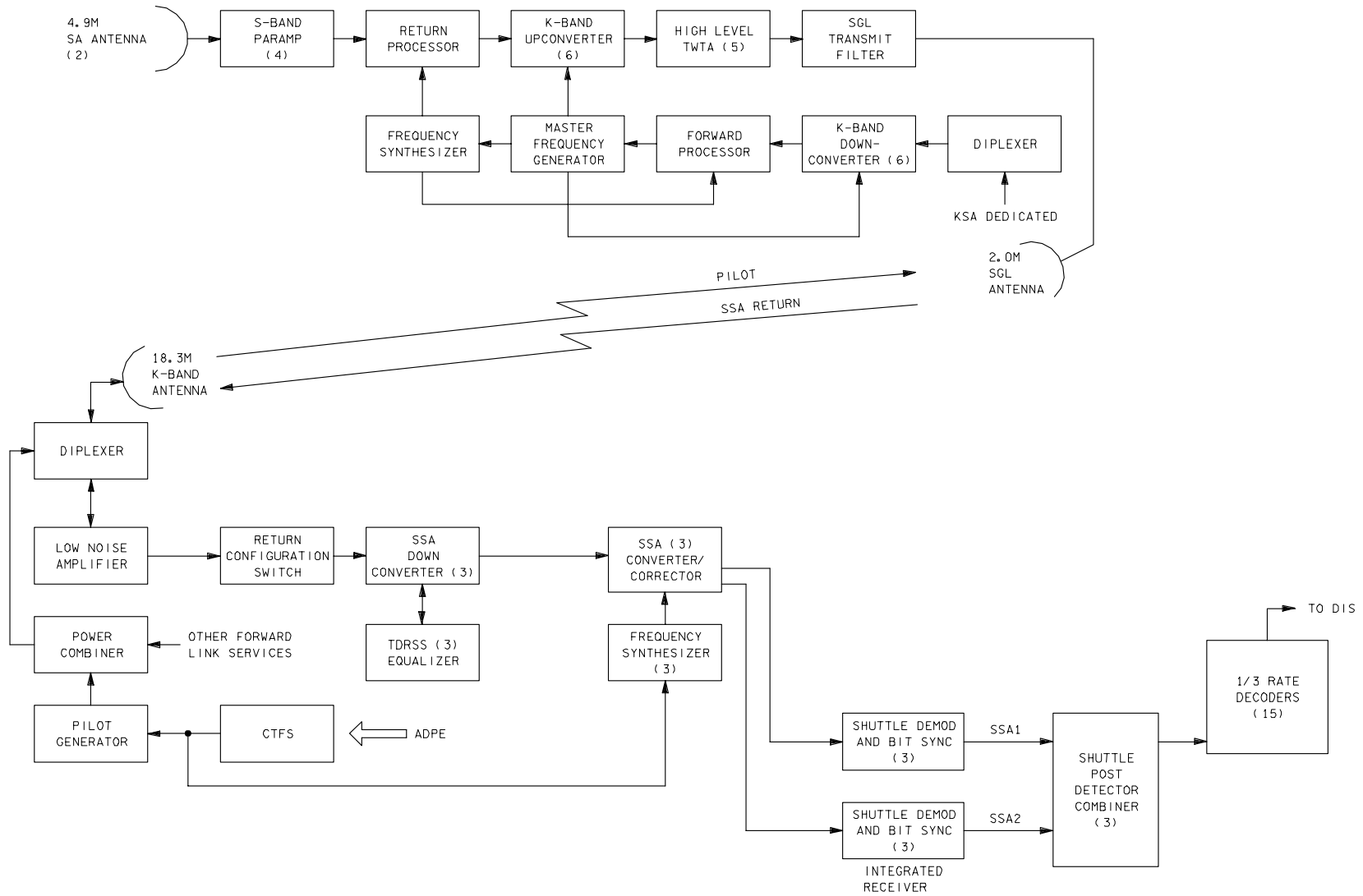
S-band return links will be received, amplified, equalized, demodulated, bit synced, 1/3 rate decoded, and shipped to the NASCOM interface as a 192-kbps or 96-kbps stream. The shuttle integrated receiver is used for this purpose. Ku-band return link service for either mode 1 Phase Modulation (PM) or mode 2 Frequency Modulation (FM), as scheduled, is similar to that for S-band. No processing is done other than to optimize data quality. WSC has dedicated KSA equipment to recover the carrier and the QPSK subcarrier. In general, the high rate demod demodulates the PM carrier, sends the 8.5 MHz subcarrier to the medium rate demod where the channel 1 and 2 bit streams are stripped out and sent to the low and medium rate bit syncs. Channel 3 PM data are sent to the high rate bit syncs and then 1/2 rate decoded. In the FM mode, the wide band demod replaces the high rate demod, and the channel 3 FM analog signal is sent directly from the wide band demod to the "wall." Channels 1 and 2 are treated the same as in the PM mode. The 192-kbps channel 1 output and the channels 2 and 3 outputs are provided to NASCOM. See Figure 48-5 and Figure 48-6. Ku-band channel 2 is not convolutionally encoded as are the S-band return link and Ku-band channel 1 and PM channel 3 (PL MAX).

### 48.3.7 SSA Combining

If the SSA combining mode is scheduled by JSC, both SSA antennas on a TDRS will point to the orbiter to increase the effective antenna gain. The two SSA return link signals are post-detection combined on the ground to yield a nominal 2.5-dB circuit margin improvement. Since both single access antennas are tied up, use of this mode must be justified. This is not a reconfigurable mode controlled by GCMR, it must be scheduled. Due to the post-detection configuration of the combiners should one of the two signals be removed (due to an antenna or other failure), reduced performance on the remaining link will require that the combining service terminate and a new service be scheduled. This capability is not normally used.

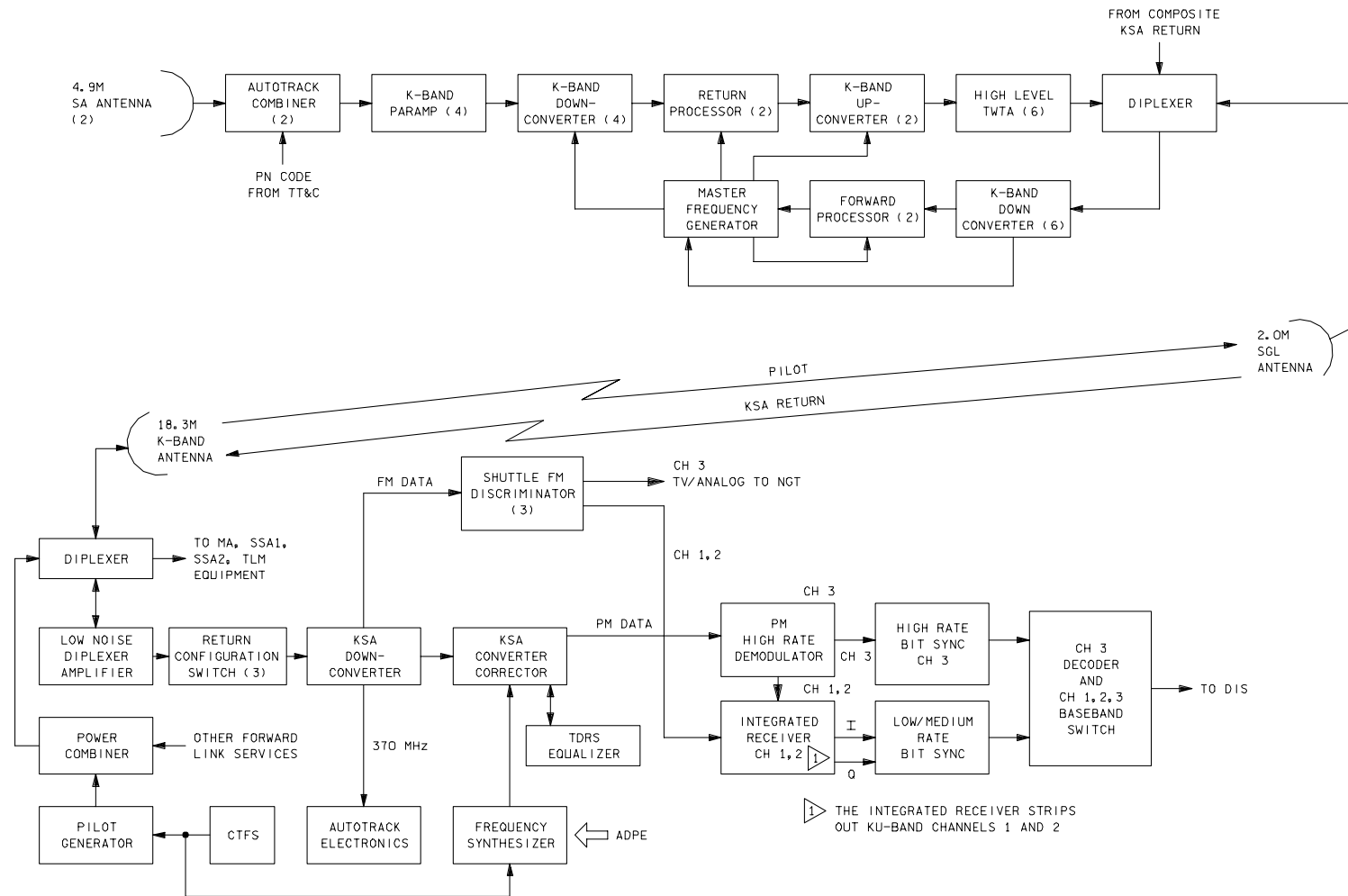
### 48.3.8 Tracking and Doppler Compensation

In addition to the data relay function, the TDRSS provides high accuracy tracking of the orbiter using two-way S-band Doppler. Corrections for ground terminal and TDRS delay are made at WSC, and GSFC corrects for other errors such as tropospheric and ionospheric delays. The delay computed by WSC and the Doppler count is sent to NASCOM and then to JSC. If JSC requests that the forward link carrier be Doppler-compensated (normal for initial acquisition) the ADPE computes the correct forward link offset using the nominal orbiter center receive frequency, the satellite ephemeris, and the orbiter ephemeris. Either the forward link carrier, the PN spreading code, or both (as requested by GCMR by JSC) can be Doppler-compensated for S-band; both carrier and PN code must be compensated or not compensated for Ku-band. Ku-band Doppler compensation is nominal. Carrier compensation must be inhibited when S-band Doppler tracking measurements are desired; if not, the tracking data will be flagged invalid by the MCC (JSC) tracking processor. This is done by JSC GCMR.



186114605, SCH, 4

Figure 48-5. SSA return link processing



186114606, ART, 6

Figure 48-6. KSA return link processing

The forward link (and then the return link) will drop lock during enabling (not inhibiting) of Doppler compensation. The return link is always Doppler-compensated for one- or two-way Doppler as required for coherent or noncoherent operating modes.

#### 48.3.9 Simulation Services

The WSC has equipment and a Ku-/S-band antenna for simulating one S-band and one Ku-band shuttle link simultaneously. (ESTL can also do this but is not always available and cannot see a satellite further west than about 171° W (marginal)). The variable parameters include:

- G/T
- EIRP
- Range and Doppler
- PN spreading and data

Simulation service must be scheduled as any other service.

#### 48.3.10 TOCC

The TOCC at each WSC terminal is the single-point control area for the TDRS satellites and WSC. It consists of eight dual-position workstations with Cathode-Ray Tube (CRT) display and manual entry devices which interface with the ADPE. The ground segment is controlled, for the most part, automatically by the ADPE. For example, the following operations are designed to be essentially automatic. Following completion of the WSC, four satellites should be available for simultaneous scheduling.

- A. Identifying and recovering from system failures
- B. Ground station configuration as requested by Ground Control Messages (GCM) received from the NCC
- C. Scheduling shuttle support service in response to Scheduling Orders (SHOs) received from NCC and detecting schedule conflicts
- D. Routine status messages (Operational Data Messages (ODMs)) transmitted to NCC and then to JSC every 5 seconds

Automatic procedures can be manually overridden if required and some operations such as satellite battery power management, stationkeeping maneuvers, simulation services, and unsuccessful ADPE attempts to recover from system failures require manual intervention. In general, TOCC operators are informed by an audible alarm of all failures as they occur, and of any automatic compensatory action taken. The TOCC (TDRS OPS) communicates with NCC by voice or Teletype (TTY) to resolve items such as schedule conflicts or equipment failures affecting spacecraft support.



### 48.3.11 Fault Detection Within WSC

Fault detection is automatic. The equipment within WSC contains equipment status indicators that are continuously monitored by the ADPE. Additionally, various TDRSS performance parameters are monitored (e.g., bit error rate, signal present, autotrack pull-in) to allow automatic acquisition/reacquisition to occur. ADPE operation is monitored and an automatic failover from prime to backup ADPE computers will be initiated when the primary fails. Generally speaking, all shuttle equipment is at least triply redundant and, when shared with other users equipment, six deep. The Automatic Link Monitoring Equipment (ALMS), a sophisticated spectrum analyzer, is available for orbiter spectrum monitoring of any forward or return link. S-band frequency/changes onboard the shuttle are not detectable with GCMR reconfiguration.

### 48.3.12 Logging

Automatic printouts within TOCC have been limited to critical information items to minimize the volume of recorded data. Automatic printouts include alarm conditions, configuration changes, operator entries, and satellite commands other than TDRS antenna pointing. However, the TOCC can always request specific printouts of specific displays. There are also magnetic tape logs for schedules, operations messages, and selected parameters but no rapid playback capability.

### 48.3.13 ADPE

The ADPE, which is divided into five function groups called Control And Display Computer Networks (CDCNs), controls and monitors the TDRSS resources by performing functions as follows.

- Displays TDRSS status and resource schedules
- Schedules resources in accordance with SHOs
- Supports automatic and TOCC-initiated satellite commanding
- Computes shuttle and satellite ephemerides from vectors supplied by GSFC
- Steers satellite antennas and predicts solar eclipses
- Collects S-band Doppler data
- Controls acquisition, reacquisition, and reconfiguration
- Processes various messages generated externally (GCMRs) and TOCC-initiated

The central computer and the other processors each have redundant units. They provide interfaces to/from NGT, TOCC, and the ground communications equipment (GCE). The ADPE operates in a "Unified Set" configuration, with 1 to 2 minutes usually required for a unit switchover. One characteristic of this configuration is that, if a unit fails less than 8 minutes from SHO end, it is not restarted and all services are lost.

All ADPEs within each CDCN interface with Subsystem Controllers (SSCLs) which provide the control and status interfaces to the operational equipment.

#### **48.3.14 ADPE Data Bases**

The ADPE maintains certain data bases used to acquire and configure for support. An example of the contents of these tables are:

- Hardware components required for a particular link (SSA FWD, KSA RTN, etc.)
- The “Hot Spare” components
- A configuration command list for each link
- An acquisition command list for each link
- An operational command list for functions such as pointing

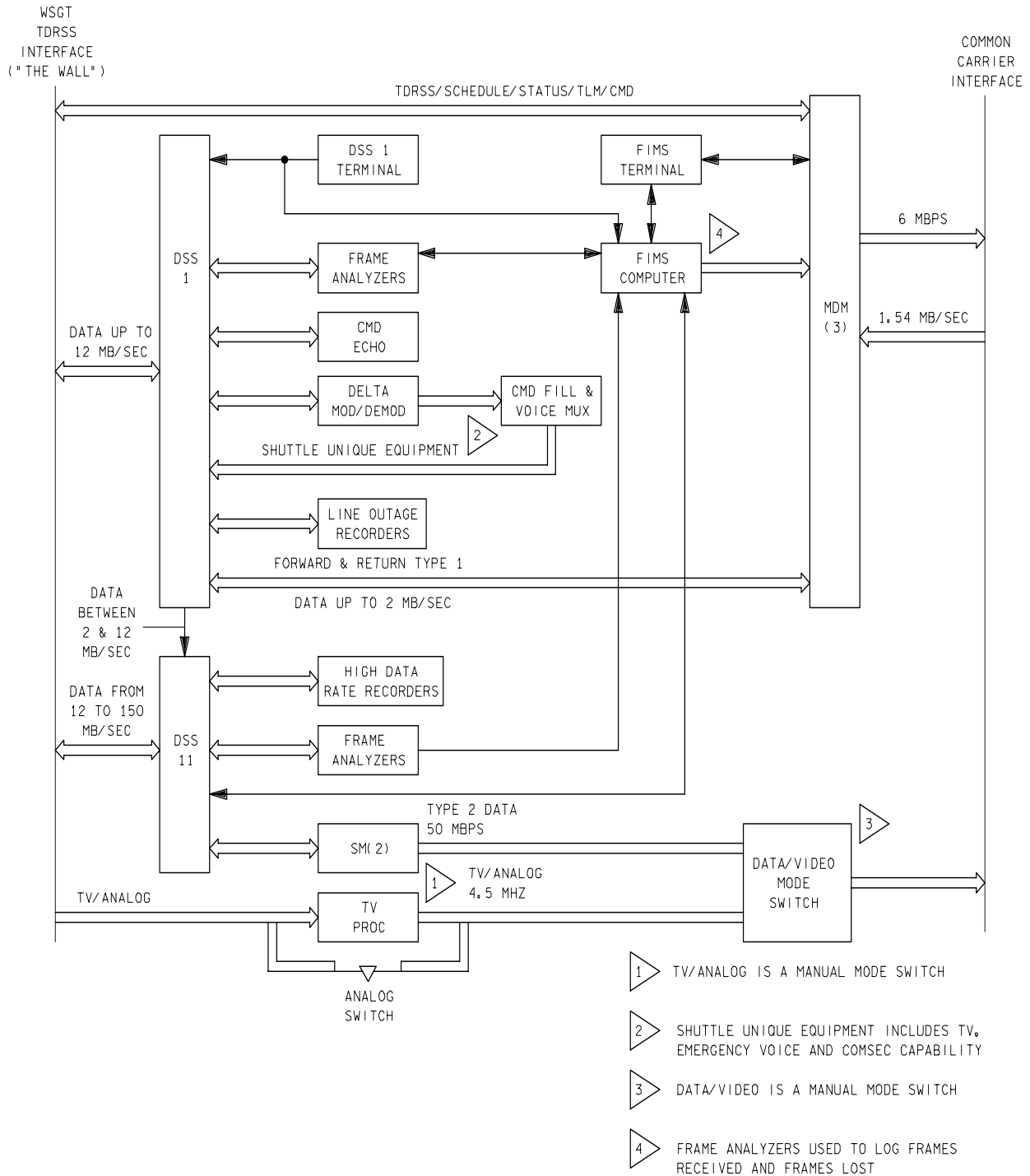
#### **48.3.15 Data Interface System**

The Data Interface System (DIS), located at WSC, performs the following functions:

- A. Provides the operational interface between WSGT and the NASCOM common carrier leased circuits for all data and voice links, scheduling messages, GCMs, and User Performance Data (UPD - site status data displayed on the TELCOM SN Status display).
- B. Data quality monitoring for all forward and return digital links (frames lost data - DQM).
- C. Data storage.
- D. Shuttle TV processing (but not color conversion).
- E. COMSEC equipment is available.
- F. Command echo check equipment (forward link data returned to MCC and logged).
- G. FWD and RTN link simulation.

#### **48.3.16 Operation Interface**

See Figure 48-7. The MDMs and SMs are configurable via GCMR using a system called the Control And Status System (CSS). Five minutes notice to NCC is desired to reconfigure via GCMR.



186114607, ART, 5

**Figure 48-7. NASCOM interface functional block diagram**

### 48.3.17 Data Types

Type 1 data extends from 100 bit/s to 7 mbps (nominally limited to 2 mbps) and these data are routed to the MDM system at W&C for real-time transmission via separate links to JSC and to GSFC. This is a two-way link and will handle all but Ku-band channel 3 high rate data. The dual WAN at JSC, WSC, and GSFC operate at continuous full redundancy, with both carrying identical data. A third MDM is used to provide playback services and for offline troubleshooting.

Type 2 data vary from 2 mbps to 50 mbps and use the Statistical Multiplexer (SM) to interface with the NASCOM. The SM (redundant) is a one-way (transmit) multiplexer that accepts a maximum of four inputs and allocates as much as 48 mbps among them (plus 2 mbps overhead). This 50-mbps output timeshares the NASCOM interface with analog/TV, using a mode switch. A mode switch configured by GCMR in the DIS allows the desired selection. The stat mux is required for Ku-band channel 3 high rate data.

The DIS MDM has the capability of routing up to 100 separate data streams into a single communications link (NASCOM limit is currently 6 mbps although the MDM limit is 10 mbps), and it can receive and distribute up to 36 forward link channels for forwarding through to WSC.

### 48.3.18 Data Quality Monitoring

WSC has responsibility for monitoring the TDRSS data quality and the services provided. This is done by the DQM. DQM consists of frame analyzers set up to monitor the presence of frame sync on all forward and return digital data links. These data are fed to the DQM computer, where statistics are compiled. Status messages with frames lost information are locally displayed and forwarded to both JSC and GSFC (DQSMs). The DQM computer also processes NCCDS scheduling messages for display. SN Status display TVCU SYNC description needs to be updated. The TVCU provides its own sync. It lacks the ability to accept the external sync signal from the RCU. External was never implemented DQM data in the MCC as they are updated every 5 seconds in real time. DQM processing does not affect actual data flow.

In order for DQM data to be useful, the frame sync pattern must be programmed into the DQM for each digital link. This has been done for standard orbiter real-time and dump links.

### 48.3.19 Data Storage

The eight High-Density Digital Recorders (HDDR) (150 mbps max) provide for data storage and retrieval resulting from line outage. Different tape transport speeds allow for various record/playback ratios. Approximate record capacity is 45 minutes per recorder. Data on the HDDRs are recorded at the output of the alternate MDM. Two analog TV recorders with 1-1/2 hour capacities are operated during scheduled TV times. Recorders recording data greater than 2 mbps are run continuously in a loop mode when high data rate services are scheduled. Data are recorded prior to SM input.

Playback capability can be scheduled as any other service. Tapes are retained for at least 30 days before degaussing.

#### **48.3.20 Shuttle TV Processing**

The signal parameters of the shuttle TV signal are not directly compatible with those of the analog NASCOM circuit and, therefore, require processing. This is part of what is called Shuttle-Unique Equipment (SUE). TV monitoring capability (unconverted) is available as well as a waveform monitor.

#### **48.3.21 Emergency Voice**

This part of the SUE allows an analog voice input from MCC (such as a black phone) to be uplinked in the event the digitized input from the MCC is inoperable. The voice is digitized and multiplexed with command fill pattern data. Return link voice is converted to analog as well and can be routinely monitored.

#### **48.3.22 Command Echo**

Although WSC provides no command verification, equipment is used to strip out the command sent from MCC via either S-band or Ku-band and return it to the MCC, where it is logged at the NOM and available for analysis if necessary.

#### **48.3.23 Forward and Return Link Simulation**

Type 1 and 2 data generators are used to provide forward and return link simulation signals to WSC and NASCOM.

#### **48.3.24 Encryption**

COMSEC gear is available in the DIS to allow use of the DQM equipment when encryption is used and when emergency voice is used. Use of this equipment does not affect data flow.

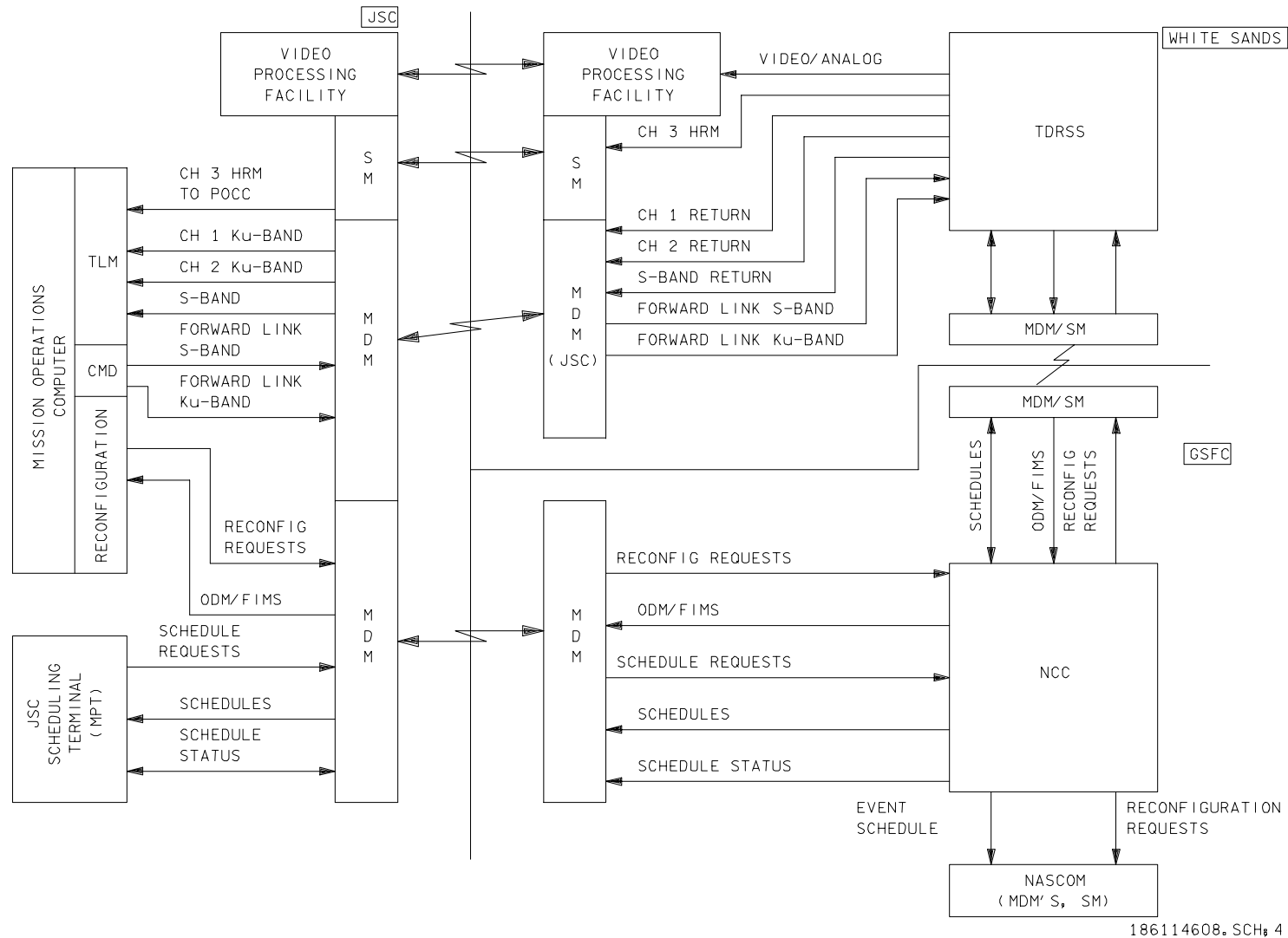


Figure 48-8. TDRS network

## 48.4 NETWORK CONTROL CENTER

The NCC is a facility at GSFC and is the focal point of operational management of the TDRSS tracking network. The NCC provides several functions as follows:

- Scheduling
- Fault isolation coordination and system testing
- Analysis of network performance

The NCC is almost completely automated although operators in the NCC control room can and will intervene when a problem occurs or a user requires assistance. It interfaces with the GSFC Flight Dynamics Facility (FDF) which generates acquisition data for TDRS based upon JSC provided vectors and maintains the TDRS ephemeris.

### 48.4.1 Scheduling

All support activities involving the TDRSS network are scheduled. This is routinely done through interactive computers using User Planning System (UPS). At the MCC, there are two UPS workstations colocated at the COMMAND console. The scheduling system operates on a nonpriority basis; i.e., there is no explicit prioritization made between requests being serviced. However, priority judgments can be applied manually by the NCC scheduling console operator. For example, a spacecraft emergency or launch and insertion support would normally receive priority over routine on-orbit operations. Shuttle single access support is usually conflict free, although conflicts are routinely worked each mission. A summary of the scheduling process is described below.

MCC transmits the initial Schedule Add Request (SAR) for an upcoming flight to NCC, who (assuming no conflicts) adds this to the NCC data base active schedule file. This is accomplished between T - 21 days to T - 7 days. NCC provides WSC and NASCOM with a Schedule Order (SHO) approximately 24 hours before the start of support. This SHO is very specific and must include the type of support required (e.g., SSA FWD, tracking, KSA RTN, etc.), support start, and end times to the second, and must also include an initial set of link parameters some of which are reconfigurable and may be difficult to predict in advance. Parameters in the SHO are defined in Table 48-1. A series of configuration codes will be defined premission and will be used to define the most commonly used SHO configurations.

It is considered routine to request schedule changes for an upcoming AOS period up to 90 minutes in advance. For example, if the premission schedule had TDRS east configured for Ku-band return link in the FM mode for a particular AOS and the orbiter will actually be in PM, then a routine SHO can be issued up to 45 minutes in advance of event start (AOS) to change the upcoming configuration. WSC requires 2 minutes (for angles up to 26°) or up to 5 minutes (for angles exceeding 26°) for antenna repointing. No changes can be made from this point until schedule start time (AOS) when reconfigurable parameters (only) can then be changed by GCMR. If a non-

reconfigurable parameter must be changed, then the current SHO must be canceled and a new one built and transmitted. This can take approximately 20 minutes with NO services available. Since changing the TDRS handover time affects both west and east SHOs, this request should be initiated 45 minutes before the west pass is affected.

Before the first service start time, TDRSS sends slewing commands to the selected antenna (requiring 2 to 5 minutes) as specified in the SHO and the ADPE performs the following according to the SHO.

- Commands the polarization
- Commands the S-band frequency (Ku-band frequency is fixed)
- Commands the forward link EIRP
- Commands the antenna to program track the orbiter
- Sets up the total chain of equipment between the ground 60-foot antenna and the “hole in the wall” data port by T-0
- Configures this equipment
- Performs an automatic acquisition
- Performs data relay until service termination time
- Generates ODMs every 5 seconds (site status data) until service termination time

**Table 48-2. SHO contents**

GENERAL

Message ID

Message type - Scheduling

User support identification code, vehicle identification code (SUPIDEN)

User despun antenna - Type 1, Type 2, or not applicable (N/A for shuttle)

Message class - Normal, emergency, simulation, routine verification, emergency routine verification, or other

TDRS ID (east, west, or spare)

PN code assignment for shuttle

Event start time (YYDDHHMMSS)



*Table 48-2. SHO contents (continued)*

FORWARD LINK SERVICES

SSA

Support start/stop time (resolved to 1 second)  
Service configuration - SSA, shuttle, nonlinear IF interface, MA, linear mode  
IF interface  
Service link ID - antenna 1 or 2  
Shuttle receive frequency (resolved to 10 Hz)  
Shuttle PN rate (resolved to 1 chip/sec)  
Power mode - Normal or high  
Polarization - LCP or RCP  
Command channel PN modulation - Yes or no (spread spectrum)  
Shuttle carrier Doppler compensation - Yes or no  
Shuttle PN rate Doppler compensation - Yes or no  
Shuttle data configuration - Mode 1 or 2 (32 or 72 kbps)  
Maximum data rate (resolved to 1 bps)  
User interface channel ID  
TDRSS interface channel ID  
Antenna slew interval - 2 or 5 minutes  
Configuration code ID

KSA

Support start/stop time (resolved to 1 second)  
Service configuration - KSA, shuttle, nonlinear IF interface, linear mode IF interface  
Service link ID - Antenna 1 or 2  
User receiver frequency (resolved to 10 Hz)  
Power mode - Normal or high  
Polarization - LCP or RCP  
Doppler compensation required - Yes or no  
Command channel PN modulation - Yes or no (spread spectrum)  
Maximum data rate (resolved to 1 bps)  
User interface channel ID

FORWARD LINK SERVICES

Initial data rate (resolved to 1 bps)  
TDRSS interface channel ID  
Antenna slew interval - 2 or 5 minutes  
Configuration code ID

*Table 48-2. SHO contents (continued)*

RETURN LINK SERVICES

SSA

Maximum user EIRP (Difference will not exceed 12 dB)  
Minimum user EIRP  
Service link ID - Antenna 1, 2, or both  
SSA combining - Yes or no  
Polarization - LCP or RCP  
Receiver configuration - Noncoherent, coherent, cross support (uses both SA and MA),  
or hybrid (uses two satellites simultaneously)  
Maximum data rate (resolved to 1 bps)  
Data stream ID (1 to 377)  
Return channel time delay measurement - Yes or no  
Shuttle transmit frequency if noncoherent (resolved to 10 Hz)  
Support start/stop time (resolved to 1 second)  
Service configuration - SSA, shuttle, nonlinear IF interface, MA, linear mode  
IF interface  
Shuttle configuration - Mode 1, 2, or 3 (96 kbps, 192 kbps, carrier only)  
Data bit jitter for shuttle (0.0 percent, 0.01 percent, 0.1 percent, 0.5 percent, 1 percent,  
2 percent)  
User interface channel ID  
TDRSS interface channel ID  
Antenna slew interval - 2 or 5 minutes  
Configuration code ID

KSA

Maximum user EIRP (difference will not exceed 12 dB)  
Minimum user EIRP  
Service link ID - Antenna 1 or 2  
Polarization - LCP or RCP  
Receiver configuration - Coherent or noncoherent (always noncoherent for shuttle)  
Shuttle transmit frequency if noncoherent (resolved to 10 Hz)  
Support start/stop time (resolved to 1 second)  
Service configuration - KSA, shuttle, nonlinear IF interface, linear mode IF interface  
Shuttle Mode - 1 or 2 (PM or FM)  
Data format, Channel 1, NRZ-L, M, S; BiØ-L, M, S (always BiØ-L for shuttle)

**Table 48-2. SHO contents (concluded)**

Data format, channel 2, NRZ-L, M, S; BiØ-L, M, S  
Initial data rate, channel 2, (resolved to 1 bps)  
Data format, channel 3, mode 1 - NRZ-L, M, S; BiØ-L, M, S (always NRZ-L for shuttle)  
Initial data rate, channel 3, mode 1 (resolved to 1 bps)  
Data bit jitter (0.0 percent, 0.01 percent, 0.1 percent, 0.5 percent, 1 percent, 2 percent)  
channels 1, 2, and 3  
User interface channel ID, mode 1 or 2 - For channels 1, 2, and 3  
Return channel time delay measurement - Yes or no  
Maximum data rate channel 2  
Maximum data rate channel 3  
Data stream ID channels 1, 2, and 3 (1 to 377)  
TDRSS interface channel ID  
Antenna slew interval - 2 or 5 minutes  
Configuration code ID

### TRACKING

Service configuration - Normal or cross support (MA and SA) and/or hybrid (two satellites) cross-support and hybrid are N/A for shuttle  
Normal tracking - MA, SSA, KSA, shuttle S-band, or shuttle Ku-band (not used by MCC)  
Range tracking required - Yes or no (N/A for shuttle)  
Doppler tracking required - No, one-way, two-way  
Support start/stop time (resolved to 1 second)  
Sample rate - 1, 0.2, 0.1, 1/60, or 1/300 S/S  
Configuration code ID  
User interface ID  
TDRSS interface ID

### **48.4.2 GCMRs**

Once the service has started (SHO start) MCC can make changes to many predefined reconfigurable parameters contained in the SHO for that particular pass. This is accomplished by a computer-to-computer interface between MCC, NCC, and WSC. The TDRS Configuration Controller (COMMAND) at MCC issues a GCMR to NCC, where it is validated and checked for conflicts, after which it is forwarded (as a GCM) to WSC, where it is again checked for conflicts. Then it is executed by the ADPE after a 15- or 20-second dropout in that service (SSA RTN, KSA FWD, etc.). This is how orbiter bit rate changes, S-band frequency changes, Ku-band PM/FM and channels 2 and 3 data format changes are accomplished. A single Ku-band return link channel can be reconfigured alone. However, a PM/FM change results in the entire return link being interrupted for 30 seconds. INCO must supply COMMAND with the required information. The parameters included in a GCMR are listed in Table 48-2. Bit rate changes at the NASCOM are now reconfigurable via GCMR since the NASCOM control and switching system (CSS) has been implemented. DQM setup is still manual. MCC

has implemented other types of GCMRs which are available for use by COMMAND as follows. All GCMRs are addressed to a particular satellite antenna (i.e., SSA1, KSA1) and for either a forward or return link. Changing antennas requires a schedule change.

A. Reacquisition Request

This GCMR is addressed to a particular service (e.g., SSA FWD) and reinitiates the acquisition sequence, necessitating a dropout of approximately 15 to 20 seconds. Reacquisitions are often required when operating TDRS, especially for return link.

B. Forward Link Sweep Request

For SSA links this will result in the forward link being swept from  $F_o$  minus 3 kHz linearly to  $F_o$  + 3 kHz in 120 seconds and held at  $F_o$  + 3 kHz thereafter. For KSA, forward link sweep is to be initiated at  $F_o$  minus 30 kHz linearly to  $F_o$  + 30 kHz in 120 seconds and held at  $F_o$  + 30 kHz thereafter. Forward link sweep requests should not be sent when Doppler compensation has been inhibited (if scheduled) and is initiated within 15 seconds of message receipt at WSC. A 15-second forward link dropout can be expected. This GCMR should not normally be required for orbiter as the center frequencies are well known.

C. Forward Link EIRP Reconfiguration

The SSA and KSA forward links can be configured for normal or high power modes within 15 seconds with this request. SSA normal and high power outputs are approximately 43.6 dBW and 46.1 dBW, respectively. KSA normal and high power outputs are approximately 46.5 dBW and 48.5 dBW, respectively. These levels are set in a table in the ADPE. Normally, the orbiter is expected to use high power for all SSA FWD and KSA FWD services.

D. Expanded User Frequency Uncertainty Request

In the event the orbiter S-band or Ku-band transmit frequency becomes unpredictable, COMMAND can transmit this message to WSC which (within 15 seconds) will accommodate a  $\pm 3$ -kHz (SSA) or a  $\pm 20$ -kHz (KSA) transmit frequency uncertainty. This message should only be required in contingency situations for shuttle.

E. Doppler Compensation Inhibit Request

Normally, forward link Doppler compensation will be automatically used especially at acquisition. However, carrier-only Doppler compensation must be inhibited during periods of two-way Doppler tracking via S-band. This message allows Doppler compensation to be inhibited for Ku-band, S-band carrier only, S-band PN (spreading) code only, or both S-band carrier and PN code. It is expected that the nominal mode during scheduled tracking periods will be S-band carrier-only Doppler inhibited. Ku-band and S-band PN code should always be Doppler compensated. Compensation inhibit is initiated within 15 seconds of message receipt and completed within 25 seconds.

*Table 48-3. GCMR message contents*

HEADER

| <u>Data item</u> | <u>Range of values</u>   |
|------------------|--|
| Message type     | 98 = GCM control   |
| Message ID       | A 7-character identifier used to reference this message            |
| Message class    | 04 = User reconfiguration request                                  |
| SUPIDEN          | Identifies the spacecraft for which a reconfiguration is requested |
| User ID          | Requester ID (4 ASCII characters)                                  |
| Password         | Alphanumeric code  |
| Station          | Identifies the satellite to be reconfigured (TDE, TDW, TDS)        |

SSA FORWARD

|   |                        |
|---|------------------------|
| Link                                    | 01 = SSA1<br>02 = SSA2 |
| Service support type                    | 0 = Forward            |
| Receive frequency, shuttle              | LSD = 10 Hz            |
| Polarization, shuttle                   | 0 = LCP<br>1 = RCP     |
| Shuttle carrier Doppler compensation    | 0 = No<br>1 = Yes      |
| Shuttle PN rate Doppler compensation    | 0 = No<br>1 = Yes      |
| Shuttle PN modulation (spread spectrum) | 0 = No<br>1 = Yes      |

**Table 48-3. GCMR message contents (continued)**

| <u>Data item</u>                       | <u>Range of values</u>   |
|--|--|
| Shuttle configuration                  | 1 = Mode 1 (32K)<br>2 = Mode 2 (72K)   |
| <u>KSA FORWARD</u>                     |  |
| Link                                   | 03 = KSA1<br>04 = KSA2   |
| Service support type                   | 0 = Forward  |
| Polarization, shuttle                  | 0 = LCP<br>1 = RCP   |
| Command channel                        | 0 = No   |
| PN modulation (spread spectrum)        | 1 = Yes  |
| Doppler compensation required, shuttle | 1 = Yes<br>0 = No  |
| Receive frequency, shuttle             | LSD = 10 Hz  |
| Data rate, shuttle                     | LSD = 1 B/S  |
| <u>SSA RETURN</u>                      |  |
| Link                                   | 01 = SSA1<br>02 = SSA2   |
| Service support type                   | 1 = Return   |
| Polarization, shuttle                  | 0 = LCP<br>1 = RCP   |
| Maximum EIRP, shuttle                  | Sign, 3 digits; LSD = 0.1 dBW  |
| Minimum EIRP, shuttle                  | Sign, 3 digits; LSD = 0.1 dBW  |
| Data stream ID shuttle                 | Numerical  |
| Data bit jitter for shuttle            | 0 = None<br>1 = 0.01 percent<br>2 = 0.1 percent<br>3 = 0.5 percent<br>4 = 1.0 percent<br>5 = 2.0 percent |
|  | N/A for shuttle  |

**Table 48-3. GCMR message contents (continued)**

| <u>Data item</u>                          | <u>Range of values</u>   |
|---|--|
| Shuttle transmit frequency if noncoherent | LSD = 10 Hz; must have zero value if transmit frequency is coherent  |
| Shuttle configuration                     | 1 = Mode 1 (96 kb)<br>2 = Mode 2 (192 kb)<br>3 = Mode 3 (carrier only)   |
| <u>KSA RETURN</u>                         |  |
| Link                                      | 03 = KSA1<br>04 = KSA2   |
| Service support type                      | 1 = Return   |
| Polarization, shuttle                     | 0 = LCP<br>1 = RCP   |
| Maximum EIRP, shuttle                     | Sign, 3 digits; LSD = 0.1 dBW  |
| Minimum EIRP, shuttle                     | Sign, 3 digits; LSD = 0.1 dBW  |
| Shuttle mode                              | 1 = Mode 1 (PM)<br>2 = Mode 2 FM digital<br>3 = Mode 2 FM analog<br>4 = Mode 2 FM TV   |
| Data format, channel 1, mode 1 or 2       | 0 = NRZ-L<br>1 = NRZ-M<br>2 = NRZ-S<br>3 = BiØ-L<br>4 = BiØ-M<br>5 = BiØ-S<br>Only BiØ-L for shuttle   |
| Data bit jitter, channel 1, mode 1 or 2   | 0 = None<br>1 = 0.01 percent<br>2 = 0.1 percent<br>3 = 0.5 percent<br>4 = 1.0 percent<br>5 = 2.0 percent<br>Only 0.5, 1.0, and 2.0 percent are implemented |
| Data stream ID, mode 1 or 2, channel 1    | Numerical (0 to 377)   |
| Data stream ID, mode 1 or 2, channel 2    | Numerical (1 to 377)   |

**Table 48-3. GCMR message contents (concluded)**

| <u>Data item</u>                          | <u>Range of values</u>   |   |
|---|--|---|
| Data stream ID, mode 1, channel 3         | Numerical (1 to 377)   |   |
| Shuttle transmit frequency if noncoherent | LSD = 10 Hz  |   |
| Data format, channel 2 mode 1 or 2        | 0 = NRZ-L<br>1 = NRZ-M<br>2 = NRZ-S<br>3 = BiØ-L<br>4 = BiØ-M<br>5 = BiØ-S                               | Only BiØ-L for Ops and payload recorder dumps. Spacelab HRM downlink are always NRZ-L |
| Data bit jitter, channel 2, mode 1 or 2   | 0 = None<br>1 = 0.01 percent<br>2 = 0.1 percent<br>3 = 0.5 percent<br>4 = 1.0 percent<br>5 = 2.0 percent | Only 0.5, 1.0, and 2.0 percent are implemented  |
| Data rate, channel 2, mode 1 or 2         | LSD = 1 b/s  |   |
| Data format, channel 3, mode 1            | 0 = NRZ-L<br>1 = NRZ-M<br>2 = NRZ-S  | NRZ-L for Spacelab HRM  |
| Data bit jitter, channel 3, mode 1        | 0 = None<br>1 = 0.01 percent<br>2 = 0.1 percent<br>3 = 0.5 percent<br>4 = 1.0 percent<br>5 = 2.0 percent | N/A for shuttle   |
| Data Rate, channel 3, mode 1              | LSD = 1 b/s  |   |

F. GCM Denials and GCM Dispositions

A GCM denial is a message from NCC to MCC either on receipt of an invalid GCMR from MCC or on receipt of a GCM reject from TDRSS. The reasons for rejection are listed in Table 48-4 and are displayed to COMMAND. A GCM disposition is a message from NCC to MCC indicating whether or not an acknowledgment was received from TDRSS (message received). COMMAND tracks these messages on TDRSS RT Management (TRM).



**Table 48-4. GCM denial rejection codes**

|                      |   |
|----------------------|---|
| Reason for rejection | 01 = Syntax error at TDRSS<br>02 = Specified SHO ID not found at TDRSS<br>03 = Specified service not found at TDRSS<br>04 = Specified service not in operation (TDRSS)<br>05 = Parameter out of range (TDRSS)<br>06 = Equipment unavailable (TDRSS)<br>07 = User spacecraft not recognized by TDRSS<br>08 = OPM not legal for service designated (TDRSS)<br>09 = Schedule conflict caused by equipment needed<br>for requested reconfiguration being unavailable<br>(TDRSS)<br>10 = Service request table overflow (TDRSS)<br>11 = Equipment reservation table overflow<br>12 = Corresponding forward service not in operation<br>(TDRSS)<br>13 = Connectivity table error (no TDRS/ground<br>antenna match) (TDRSS)<br>21 = Invalid parameter in request (NCC)<br>22 = SUPIDEN conflicts with scheduled SUPIDEN<br>(NCC)<br>23 = Service not scheduled (NCC)<br>24 = Data rate exceeds line capacity (NCC)<br>25 = Requester not authorized for this spacecraft<br>(NCC)<br>26 = Interface channel not available (NCC)<br>28 = GCM class inappropriate to service type or<br>configuration (NCC)<br>29 = Doppler compensation inhibit code inappropriate<br>for configuration<br>30 = TDRSS is down (NCC)<br>31 = Pending request for same service (NCC) |
|----------------------|---|

G. ODMs

ODMs are transmitted every 5 seconds from WSC via NCC to JSC. This is the equivalent of our current site status data. They are transmitted only when a service is active (i.e., within AOS). The data are transmitted in five packets as follows and displayed on SN Status:

|         |         |
|---------|---------|
| SSA FWD | KSA FWD |
| SSA RTN | KSA RTN |
| DQM     |         |

Each satellite is associated with a separate ODM. Note that the network is not responsible for recording ODMs or any data links and cannot perform post-pass

data analysis. Signal strength data received in ODMs are uncalibrated and may not be very usable. Also some of the Ku-band return link lock statuses have been unreliable (false locks).

#### **48.5 DATA THRESHOLDS (REFERENCE EE8/SID NOVOSAD)**

##### **48.5.1 S-Band Forward**

|                              |            |
|------------------------------|------------|
| LDR                          | -120.5 dBm |
| HDR                          | -117.0 dBm |
| Carrier only (xpndr in wide) | -122.5 dBm |
| (xpndr in narrow)            | -125.5 dBm |

##### **48.5.2 S-Band Return**

|              |            |
|--------------|------------|
| LDR          | -114.7 dBm |
| HDR          | -111.7 dBm |
| Carrier only | -131.2 dBm |

##### **48.5.3 Ku-Band Forward**

|          |            |
|----------|------------|
| 72 kbps  | -108.4 dBm |
| 216 kbps | -104.2 dBm |
| ACQ      | -105.6 dBm |

##### **48.5.4 Ku-Band Return**

###### **A. Mode 1 (PM)**

|                 |           |
|-----------------|-----------|
| CH 1 - 192 kbps | -87.4 dBm |
| CH 2 - 2 MBPS   | -81.3 dBm |
| CH 3 - 50 MBPS  | -78.3 dBm |

###### **B. Mode 2 (FM)**

|                 |           |
|-----------------|-----------|
| CH 1 - 192 kbps | -80.1 dBm |
| CH 2 - 2 MBPS   | -80.1 dBm |
| CH 3 - TV       | -80.1 dBm |

## 48.6 OTHER SYSTEM CHARACTERISTICS

- SSA combining is expected to be a contingency mode for shuttle support. This is not a reconfigurable item; i.e., it must be scheduled in advance or a schedule change made in real time. A real-time schedule (SHO) change would take down all (S-band and Ku-band) support for about 20 minutes and should be avoided.
- A problem exists with the Ku-band subcarrier lock indication for Ku-band return link support as derived from the medium rate DEMOD. Once acquisition occurs, the lock/no-lock circuitry is polled only every 30 seconds. Therefore, if subcarrier lock is lost, it may not be evident by this for this parameter length of time. ODM data should reflect the situation. Also, subcarrier signal strength always reads zero.
- WSC has the capability to monitor forward link power fluctuations, commanded and actual pointing angles, and the forward or return link spectrum on each link (using the Automated Link Monitoring System (ALMS)). All this is available to us for troubleshooting.
- When two TDRS satellites are available, it should be noted that S-band and Ku-band services are not usually scheduled simultaneously from both satellites. S-band and Ku-band services can, however, start and stop at different times; e.g., east satellite Ku-band could begin before east satellite S-band. If an emergency SHO is transmitted to WSC, then the services cannot be staggered; i.e., both S-band and Ku-band must be scheduled concurrently. However, during some high inclination ascending entries to KSC, S-band services are simultaneously scheduled from both satellites.
- Command echo can only be scheduled for either S-band or Ku-band but not both simultaneously. Normally, S-band echo will be scheduled.

## 48.7 REFERENCE

<http://msc-docsrv.gsfc.nasa.gov/cmdata/400/450/452/ICD/452-ICD-SN-CSM/452-ICD-SN-CSM.pdf>

[http://msp.gsfc.nasa.gov/tdrss/snug\\_main.pdf](http://msp.gsfc.nasa.gov/tdrss/snug_main.pdf)

## SECTION 49 - TELEMETRY PROCESSING IN THE MCC

### CONTENTS

| <b>Section</b>  | <b>Page</b> |
|---|-------------|
| 49.1 GENERAL .....  | 49-1        |
| 49.2 GENERAL DESCRIPTION.....                             | 49-2        |
| 49.2.1 Shuttle Telemetry Overview .....                   | 49-2        |
| 49.2.2 Data Types.....                                    | 49-8        |
| 49.2.3 Telemetry Formats.....                             | 49-8        |
| 49.3 MCC TELEMETRY PROCESSING FUNCTIONAL DESCRIPTION..... | 49-10       |
| 49.3.1 MCC Telemetry Processing Overview .....            | 49-10       |
| 49.3.2 Network Telemetry Flow.....                        | 49-10       |
| 49.3.3 MCC Telemetry Routing.....                         | 49-11       |
| 49.3.4 Reconfiguration Processing .....                   | 49-12       |
| 49.3.5 Front End Processing.....                          | 49-14       |
| 49.3.6 Workstation Processing.....                        | 49-16       |
| 49.3.7 Dump Processing and Archiving .....                | 49-18       |
| 49.4 REFERENCE .....                                      | 49-19       |

### TABLES

| <b>Table</b>   |       |
|--|-------|
| 49-1 DSC Reference Designators .....                                       | 49-3  |
| 49-2 Interpretation of IPCL (three volumes) for V45V0100A .....            | 49-4  |
| 49-3 SM CAL vs. MCC CAL for V45V0100A, all vehicles<br>(standard CAL)..... | 49-14 |

### FIGURES

| <b>Figure</b>  |       |
|--|-------|
| 49-1 Master DNAV menu selections for MIS query ..... | 49-5  |
| 49-2 Selecting query format .....                    | 49-5  |
| 49-3 Channelization schematic for V45V0100A .....    | 49-6  |
| 49-4 HDR standard telemetry structure.....           | 49-9  |
| 49-5 Bi $\phi$ -L telemetry format .....             | 49-9  |
| 49-6 TDRS mode telemetry .....                       | 49-11 |
| 49-7 STDN mode telemetry .....                       | 49-11 |
| 49-8 SGLS mode telemetry .....                       | 49-11 |
| 49-9 MCC telemetry routing .....                     | 49-12 |
| 49-10 Workstation telemetry processing .....         | 49-16 |

THIS PAGE INTENTIONALLY BLANK

## SECTION 49 TELEMETRY PROCESSING IN THE MCC

### 49.1 GENERAL

Telemetry is a combination of techniques from several engineering disciplines, including instrumentation, digital electronics, data communications, Radio Frequency (RF) communications, and computer science. On the orbiter, thousands of physical measurements are converted into electrical signals and telemetered via either 128 kilobits per second (kbps) or 64 kbps streams to the Mission Control Center (MCC).

Orbiter telemetry streams, which are built using the shuttle Operational Instrumentation (OI) and General Purpose Computer (GPC) systems, must be processed by the MCC in order to present to the flight controller the proper measurements, as expressed in commonly recognized physical units. The orbiter telemetry system is not an “open” system, which means that it uses a limited number of fixed, strictly defined formats, within which the telemetry is downlinked to the MCC. Thus, in order for the MCC to process the telemetry streams properly, there must be an understanding of the characteristics of the telemetry stream, which is defined by the designs of the OI system, the operational integration (OI) software releases, and the Telemetry Format Loads (TFLs). Payload telemetry formats are covered in Systems Brief (SB) 33, Payload Data Interleaver (PDI).

The TFLs are designed for each flight, based on templates for those parameters that do not vary between flights, with most of the changes being payload dependent. Guidance, Navigation and Control (GNC), Systems Management (SM), and Backup Flight System (BFS) GPC downlist formats and OI telemetry formats are fairly mature but can be changed with major firmware and software releases. The definitions of these formats are stored on the Shuttle Data Tape (SDT), which is built at the Johnson Space Center (JSC) per vendor inputs.

Operational integration, not to be confused with operational instrumentation, software releases are generated per approved requirements changes at a rate of less than one release per year. Some of these OI releases will drive changes to the GPC downlist “windows” of the TFL, and MCC telemetry processing must be updated to reflect these changes through a “reconfiguration” process, which is described later in this brief.

Operational instrumentation systems onboard also vary to a small degree from vehicle to vehicle, and some parameters must be calibrated differently for different serial numbered units, as well as for different operational modes, to yield the proper unit measurements at the MCC. These OI variations are also handled by the MCC reconfiguration system.

The following Systems Briefs provide more details on the onboard telemetry systems:

- A. SB 26 - Orbiter Operational Instrumentation Overview
- B. SB 27 - OI Dedicated Signal Conditioners

- C. SB 28 - Multiplexer/Demultiplexer
- D. SB 29 - Pulse Code Modulation Master Unit
- E. SB 12 - Network Signal Processor

## 49.2 GENERAL DESCRIPTION

### 49.2.1 Shuttle Telemetry Overview

This section discusses orbiter telemetry systems at a high level to provide understanding of how the overall telemetry system works and why the MCC performs certain functions in processing the telemetry.

#### 49.2.1.1 Sensors

There are at least nine sensors types used on the orbiter:

- A. Bridge application transducer (e.g., temperature, pressure, strain gauge)
- B. Potentiometric resistance (low frequency, <30 Hz)
- C. Differential transformer device (external excitation power)
- D. Variable reluctance device
- E. Self-generating transducer
- F. Thermoelectric transducer (thermocouple, high temperature)
- G. Piezoelectric transducer (high/low frequency accelerometer, acoustic)
- H. Electromagnetic (magnetic flux)
- I. Resistance Temperature Device (RTD)

Sensors and transducers convert physical conditions and forces, such as temperature, pressure, strain, acceleration, and light into electrical signals, which, in turn, can be processed into a form suitable for displaying to humans or telemetered to a remote monitoring system. In the orbiter, the outputs of all sensors are converted into electrical voltages (0 to 5 vdc) that are subsequently scaled for common processing subassemblies and digitized, via analog to digital converters for processing in digital computers onboard and on the ground.

These voltages are generally nonlinear and offset, such that  $n^{\text{th}}$  order polynomial transformations, in the form of

$$a_0 + a_1x^1 + \dots + a_nx^n$$

where  $x$  = current parameter value  
and  $a_0 \dots a_n$  = calibration coefficients

are required to convert the digitized voltage reading back to the original physical measurement units for monitoring. This transformation is referred to as a calibration process in the MCC, and the order (n) can range from raw data (no conversion) to 5<sup>th</sup> order for nonlinear parameters.

Sensor components are made from special materials and alloys that exploit physical phenomena related to a particular material, such as temperature coefficient, electromagnetic, and piezoelectric effects, to produce the voltage changes required for instrumentation. These components are commonly referred to as thermistors, hall effect sensors, pressure transducers, accelerometers, and strain gauges, depending on the physical attribute being measured. Switch terminals, logic outputs, and voltage comparators are also sensed to produce discrete outputs. Other types of sensors detect capacitance, light, and radiation, including RF, atomic, or cosmic radiation.

Boeing maintains a website known as the Master Measurement List, otherwise known as the MML Electronic Notebook or P51 (<http://p51.ksc.nasa.gov/aps/mml/>). Once a login name is obtained, the user can search for shuttle measurements that are routed through the orbiter OI system. P51 allows the user to search by MSID, DSC, MDM, format, or DSC/MDM card. Note that DSC searches can be difficult because they use the reference designators on Table 49-1 to refer to a DSC.

**Table 49-1.** DSC Reference Designators

|                   |                   |                   |                   |
|-------------------|-------------------|-------------------|-------------------|
| DSC OF1: 81V75A16 | DSC OA1: 54V75A19 | DSC OM1: 40V75A23 | DSC OL1: 51V75A25 |
| DSC OF2: 82V75A17 | DSC OA2: 55V75A20 | DSC OM2: 40V75A74 | DSC OL2: 51V75A77 |
| DSC OF3: 83V75A18 | DSC OA3: 56V75A21 | DSC OM3: 40V75A80 | DSC OR1: 52V75A24 |
| DSC OF4: 22V75A22 |                   |                   | DSC OR2: 52V75A78 |

Note that the P51 website does not list sensor measurements routed through the shuttle flight critical MDM's. Instead, the DPS Flight Specific Load CDs list these flight critical parameters. Both DPS and the Lead Instrumentation Officer have access to these software discs.

Additionally, the orbiter Instrumentation Program and Components List (IPCL) lists each orbiter OI Measurement Stimulus Identifier (MSID) and the sensor part number, installation drawing number, channelization, and telemetry formats. Rockwell or Boeing drawings and procurement specifications for sensors can be found in the DF reference library.

The following explanation of V45V0100A, Fuel Cell No 1 Voltage is given as an example of how to interpret the IPCL in Table 49-2.



**Table 49-2. Interpretation of IPCL (three volumes) for V45V0100A**

**IPCL Volume I**

|   |                           |
|---|---------------------------|
| Valid data range and units                              | 0-40 Volts DC             |
| Sensor part number (part of recorder assembly)          | V070-764200               |
| Sensor ref designator (part of recorder assembly)       | 40V76A31                  |
| Sensor responsibility                                   | 76: Electrical Power      |
| Sensor installation drawing (part of recorder assembly) | V070-704005               |
| Sensor/transducer provider                              | C: Rockwell International |
| DSC part number   | MC473-0110-0020           |
| DSC responsibility                                      | 75: Instrumentation group |
| DSC installation drawing                                | V070-754161               |

**IPCL Volume II**

|  |                           |
|--|---------------------------|
| DSC package ref designator                                 | 40V75A23 (DSC OM1)        |
| DSC package module (channel/card/type/dwg dash no.)        | A01DA20 (chnl A, card 01) |
| DSC input plug-pins  | J4-001,002                |
| DSC output plug-pin  | J8-01,10                  |
| Bus Terminal Unit (BTU), which is an MDM ref designator    | 81V75A10                  |
| MDM input plug-pin   | J06-006,005               |
| MDM name   | OF01                      |
| Response rate fetched by PCMMU (samples per second)        | 10                        |
| Data recorded (M = on maintenance loop recorder)           | M                         |
| MDM card, (channels)                                       | 07, (05)                  |
| PCMMU input bus (06)                                       | OI                        |
| Actual data start bit in MDM data field 00-15, MIA address | 00,12                     |
| Signal type  | S: 0-5V unipolar          |

**IPCL Volume III**

|  |                        |
|--|------------------------|
| PCM downlink rate/frame/word for TFL 164 (TFL 171)   | 10/09/12 (01/94/79)    |
| (msec delay--MDM fetch to D/L) for TFL 164 (TFL 171) | 15.5 (69.7)            |
| MDM analog to digital converter card type            | AIS - 0-5 Vdc          |
| Telemetry type                                       | 1: Flight 128 kbps D/L |
| BTU name   | MDM OF01               |
| PCM downlink rate/frame/word for TFL 129 (TFL 161)   | 10/02/49 (10/09/10)    |
| (msec delay--MDM fetch to D/L) for TFL 129 (TFL 161) | 47.8 (15.4)            |
| Actual data start bit in PCMMU data RAM field 00-15  | 0                      |
| PCMMU data RAM address                               | 0685 (2569)            |

**49.2.1.2 OI Dedicated Signal Conditioners**

While the voltages produced by sensors can vary according to sensor type, the Multiplexer/Demultiplexers (MDM) that convert analog voltages to digital signals only cover specific ranges, such as from -5.12 to +5.11 volts. The Dedicated Signal


Conditioners (DSC) is essentially an amplifier (attenuator) that boosts (pads) the sensor output to be MDM compatible. Without signal conditioners, a sensor range that is too low would not provide the digital computing systems with ample resolution or noise margin for adequate measurement, and a too high sensor range would result in clipping or ignoring of the upper range of the sensor output. However, some signals (mostly discretely) that do not need conditioning go directly from the source to the MDM.

DSCs also provide a reference voltage for certain types of sensors, such as thermistors, that do not supply a calibrated output voltage without excitation. Although not all DSC types are included in the description above, all DSC types and characteristics are described in SB 27 and Space Shuttle Systems Handbook (SSSH) drawing 17.1, sheet 2, while SB 26 and SSSH drawing 17.1, sheet 1, provide an overview of the orbiter OI system, with high level (block diagram) connections between MDM and DSC.

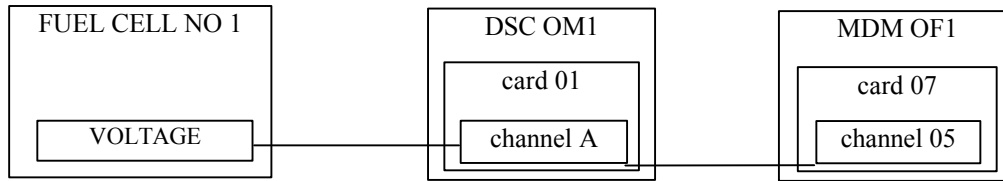
The Shuttle Configuration Analysis Program (SCAP) database found in the Mission Information System (MIS) gives the specific channelization of each measurement, including DSC card and channel and MDM card and channel. To find the MDM and DSC path of a given signal, call up **Master Display Navigation (DNAV), Global APPS, MIS, Query** (per Figure 49-1), deselect **inco** under Disciplines, click on **SCAP1-Orbiter-Channelization** (Channelization Parameters for a Single Orbiter MSID), click on **View** (with the glasses icon, per Figure 49-2), put the MSID number in the blank provided on the next popup window, click on **OK**, and a data viewer will popup with the requested information. Figure 49-3 is a channelization schematic.

|               |         |         |                    |                 |                 |
|---------------|---------|---------|--------------------|-----------------|-----------------|
| <b>Master</b> | Shuttle | Station | <b>Global APPS</b> | Tools           | (Other options) |
|               |         |         | (other options)    |                 |                 |
|               |         |         | <b>MIS</b> ----->  | <b>Query</b>    |                 |
|               |         |         | (other options)    | (other options) |                 |

**Figure 49-1. Master DNAV menu selections for MIS query**

| Disciplines                                 | Users   | File Name  | Description  |
|---|---------|--|--|
| inco<br>(un-highlighted)<br>(other options) | (blank) | <b>SCAP1-Orbiter-Channelization</b><br>(other options) | Channelization Parameter   |
| Search                                      | Plot    | Print  | ODRC   |
|   |         |  | <b>View</b><br> |

**Figure 49-2. Selecting query format**



**Figure 49-3. Channelization schematic for V45V0100A**

### 49.2.1.3 OI MDM

An OI MDM receives analog and discrete data from the orbiter systems, and provides the Analog to Digital (A/D) converters needed to convert the conditioned analog inputs to a 10 bit Pulse Coded Modulation (PCM) for output to the PCMMU, along with six (spare) zeros, to fill out the 16-bit data word. The 10 bits consist of the Most Significant Bit (MSB) polarity bit (0 = positive) and 9 magnitude bits. The A/D converter always converts at the rate of 10 mV per PCM count. Negative values are expressed in two's complement, with the MSB as the sign bit (1 = negative) that causes a conversion of -0.01V to 1023 PCM counts, counting the sign bit (which is not really counted as magnitude). The GPC processes all 10 bits from the PCMMU and is programmed to deal with the sign convention discussed above; thus, 1023 PCM counts is correctly interpreted (essentially -1 PCM count).

Physically, the MDM hybrid A/D Converter is a simple 10-bit linear converter ranging from -5.12V (0000000000) to +5.11V (1111111111). The MSB is always inverted after conversion, which is a clever device to produce 2's complement negative values. An example of this process is shown below for -2.57 Vdc.

Convert -2.57V to a 16-bit digital word:

- A. The A/D Converter starts at an all zero state (0000000000)
- B. Since -2.57 equals -5.12 +2.55, the raw conversion will produce a binary value of 255 (0011111111)
- C. The MDM always inverts the MSB (1011111111) 2's complement of the 9 magnitude bits 011111111 = 100000001 = 257 (2's complement is the simple complement plus 1 with no carry)
- D. Finally, six fill zeros are appended to the word (1011111111000000) before being placed in the PCMMU response word.

Some values are listed below without the six fill zeros.

|                     |                     |                     |
|---------------------|---------------------|---------------------|
| -5.12V = 1000000000 | -5.11V = 1000000001 | -2.57V = 1011111111 |
| -2.56V = 1100000000 | -0.01V = 1111111111 | 0.00V = 0000000000  |
| +0.01V = 0000000001 | +2.56V = 0100000000 | +5.11V = 0111111111 |

Although the discussion above deals mainly with the "high level" analog measurement type, there are other measurement types, including low level analog measurement, and

three discrete types, 28 V dc bi-level, switch closure isolated bi-level, and 5 V dc bi-level. MDM instrumentation details are covered in SB 28 and SSSH drawing 17.1, sheet 3, while SSSH drawing 8.8 and 8.13 cover the internal design of the MDM.

#### 49.2.1.4 PCMMU

The PCMMU receives the 16-bit (1 sign bit, 9 magnitude bits, and 6 zeros) data words from the MDM and stores them in its data Random Access Memory (RAM). The GPC uses and even downlists 10 bit data. However, only 8 bits are telemetered to the ground by the PCMMU telemetry data formatter. For bipolar measurements, the PCMMU telemetry data formatter drops the two Least Significant Bit (LSB) magnitude bits (decimal range of 255, PCM count of -128 to +127). The downlinked 8-bit bipolar words consist of the sign bit and the 7 most significant magnitude bits. The 7 magnitude bits for bipolar measurements with a negative polarity sign (MSB = 1) are downlinked in two's complement form.

For unipolar measurements, the PCMMU telemetry data formatter drops the MSB (sign bit) and the LSB (decimal range of 255, PCM count of 0 to +255). If a unipolar measurement somehow drops below zero volts and is uncorrected, it reads offscale high on the ground since

$$00000000 - 1 = 11111111$$

in binary subtraction; however, the PCMMU zeros out any unipolar measurement if the sign bit is 1, yielding a count of zero for all negative values. MCC processing treats unipolar measurements of zero as offscale low since all negative unipolar values are considered invalid.

The process of combining thousands of parameters in a telemetry formatter for single stream serial downlink is commonly referred to as commutation, which is really a specialized form of time division multiplexing. The process of retrieving parameters from a commutated data stream is commonly referred to as decommutation (decom).

Details of the PCMMU are discussed in SB 29 and SSSH drawing 17.2.

#### 49.2.1.5 GPC Downlist

The GPC major functions provide a downlist to the PCMMU toggle buffers for downlink in GPC downlist windows, whose locations in the Operational Downlink (OD) are determined by the TFL. Parameters included in the GPC downlist are flight-critical data bus transactions, OI measurements, which may or may not be duplicated in the OI downlist, and special GPC values that are generated in the GPC via computation. GPC downlist parameters that are duplicated in the OI downlist are generally found in the GPC downlist because of the need to know what data the GPC are seeing directly from the system or because the full 10-bit word is needed on the ground. The SM GPC can also downlist some payload parameters it acquires from a payload MDM.

#### 49.2.1.6 NSP

The Network Signal Processor (NSP) receives 128-kbps High Data Rate (HDR) and 64-kbps Low Data Rate (LDR) telemetry formats from the PCMMU and selects either HDR or LDR for downlink. When HDR is selected, 128 kbps is multiplexed with Air to Ground (A/G) 1 and A/G 2, for a total of 192 kbps. When LDR is selected, the NSP multiplexes 64 kbps with A/G 1 for a total of 96 kbps. The NSP outputs the HDR or LDR stream to the S-band transponder and Ku signal processor for RF transmission to the ground.

When the NSP loses its input data from the PCMMU, the MCC experiences a condition called "static frame" where the frame synchronizers are seeing minor frame synchronization patterns but the frame counters are no longer updating; therefore, the FEP does not validate the data and send them to the workstations. In this case, the NSP is cyclically sending an idle pattern in lieu of PCM.

When the S-band transponder loses its data input from the NSP, the ground receivers see unmodulated RF carrier, and the call coming to the MCC is "carrier no mod."

For more details on the NSP, see SB 12.

#### 49.2.2 Data Types

Each measurement has an MSID that is unique to that measurement throughout the shuttle program. The MSID consists of six fields, which are documented in each IPCL (report no. 862). As an example, the MSID V45V0100A (Fuel Cell No 1 Voltage) can be broken down as follows:

|       |   |  |           |
|-------|---|--|-----------|
| V     | = | Orbiter vehicle                              | (field 1) |
| 45    | = | Electrical Power and Distribution            | (field 2) |
| V     | = | Voltage Level                                | (field 3) |
| 0100  | = | Number assigned to this switch scan          | (field 4) |
| A     | = | Analog Signal 0-5 Vdc                        | (field 5) |
| blank | = | Used only for measurements with dual routing | (field 6) |

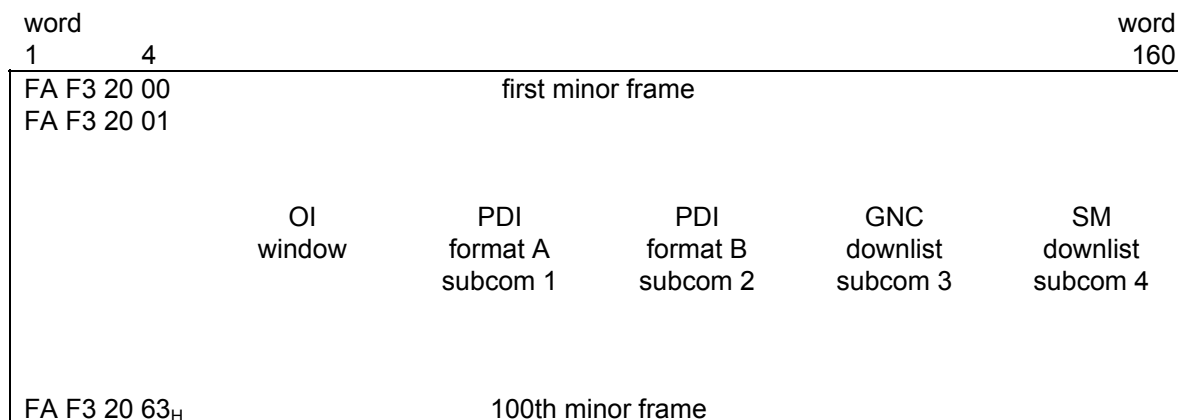
Additional data descriptions are located in the front of each IPCL (volume I).

#### 49.2.3 Telemetry Formats

Telemetry formats are built in the PCMMU telemetry formatter and are determined by the Telemetry Format Load (TFL) that is supplied to the PCMMU by the SM application, which, in turn, retrieves the TFL from the Mass Memory Unit (MMU) during the TFL load process. The TFL is basically a set of instructions for storing each telemetry parameter in a specific location in the formatter RAM. There are standard characteristics of the format that do not change between flights, as well as flight-specific format characteristics.

### 49.2.3.1 Standard Telemetry Format Characteristics

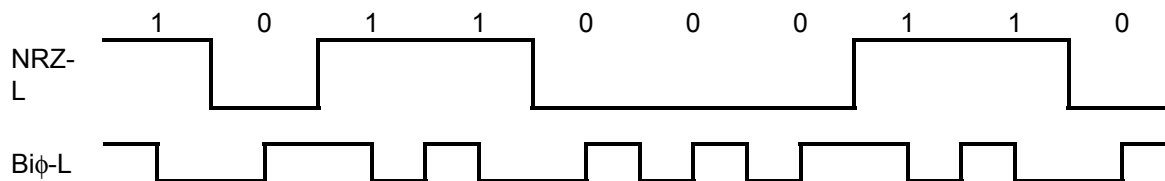
Each format is made up of 100 minor frames, each of which is made up of 160 8-bit words (80 words for LDR formats). Each minor frame consists of headers and from two to seven subcommutated windows. The headers contain three synchronization words and a frame number word (0-63<sub>H</sub>). The windows contain exactly one OI format, zero to four PDI formats, and one to five GPC formats. Figure 49-4 shows a typical minor frame structure within an HDR major frame format for a 1-second data cycle. Note that minor frames 1-3 typically contain standard information, such as TFL ID, GMT, MET, and DFL ID, in words 5-12.



**Figure 49-4. HDR standard telemetry structure**

Refer to the Space Shuttle Telemetry and Command Data Characteristics Handbook, Volume I, for detailed information on the standard telemetry characteristics. Also, the NSTS Computer Program Development Specification (CPDS) Downlist/Uplink Software Requirements describes the GPC downlist format in detail.

Data are downlinked serially from the orbiter in Bi $\phi$ -L (bi-phase-level) format. Figure 49-5 shows an example of conversion from Non-Return-Zero-Level (NRZ-L) to Bi $\phi$ -L.



**Figure 49-5. Bi $\phi$ -L telemetry format**

### 49.2.3.2 Flight Specific Telemetry Format Characteristics

The generic and flight-related requirements and planned usage for all TFLs can be found in Space Shuttle Telemetered and Recorded Data Format Requirements. TFL requirements are summarized in Section 5 of the Payload Management (PM) Flight

Software Requirements (FSR) for each flight. The presence of an MSID within a TFL can be determined by an MIS query as described in Section 49.2.1.2, but selecting **SCAP1-Orbiter-Telemetry** instead of SCAP1-Orbiter-Channelization. The exact location of an MSID in a major frame of a TFL is defined in the SDT and is used in the reconfiguration process to build decommutation tables for the MCC Front End Processors (FEPs). Additional data on MSID, TFL, and MDM channelization can be found in the MML Electronic Notebook, located at <http://p51.ksc.nasa.gov/aps/mml/>.

### **49.3 MCC TELEMETRY PROCESSING FUNCTIONAL DESCRIPTION**

#### **49.3.1 MCC Telemetry Processing Overview**

Orbiter telemetry is downlinked via the S-Band and/or Ku-band systems onboard the shuttle. This data is transmitted to a TDRS satellite, a RTS site, or a GSTDN site, where it is then routed to MCC. Note that RTS sites route orbiter downlink to Shriver Air Force Base for routing to MCC, while GSTDN sites route shuttle downlink through Goddard Space Flight Center to MCC. All TDRS S-Band or Ku-Band downlink is forwarded to MCC from the White Sands Complex.

The MCC routes the telemetry stream from the Internet Protocol (IP) router to the Downlink (D/L) FEP. The D/L FEP decommutates and calibrates the telemetry and then multicasts the processed data, via can networking to all Workstations (W/Ss) logged into the applicable activity. The W/S may perform further computations (comps), processing, and presentation formatting on the data, before they are displayed on the user's monitor screen.

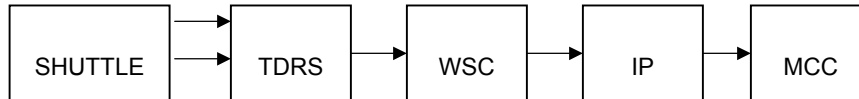
#### **49.3.2 Network Telemetry Flow**

##### **49.3.2.1 Nascom**

Nascom (an abbreviated name for the NASA communications organization) provides communications links, scheduling, and restoration services for the operation of NASA spacecraft programs, including the Space Shuttle Program (SSP). Communications links include the Tracking and Data Relay Satellite (TDRS) system or Space Network (SN), the Ground Network (GN) system, and the major operational communications trunks between centers involved in the operations of these programs. The primary system supporting the SSP is the IP system connecting the Goddard Space Flight Center (GSFC), JSC, and WSC.

##### **49.3.2.2 TDRS Flow**

See Figure 49-6 for simultaneous TDRS return links via shuttle S-band and Ku-band systems.



**Figure 49-6. TDRS mode telemetry**

The MCC D/L FEP can be set up to look for more than one good D/L stream. When one stream experiences a loss of D/L minor frame synchronization for 500 consecutive milliseconds, the D/L FEP can start processing the alternate stream. When the S-band return link is affected by radio frequency interference, this capability can result in a cleaner telemetry stream via the Ku return link, when available. The same capability may be used to auto-select ground stations when in a Spacecraft Tracking and Data Network (STDN) mode.

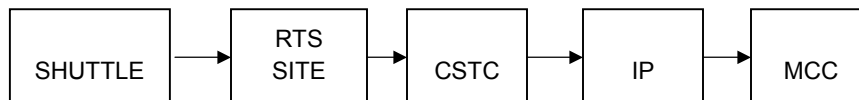
### 49.3.2.3 Ground Station Flow

When the S-band system is in a STDN mode, the flow will be through NASA sites and GSFC, whether STDN (GN) or Deep Space Network (DSN) stations (see Figure 49-7).



**Figure 49-7. STDN mode telemetry**

When the S-band system is in the space to Ground Link System (SGLS) mode, the flow will be through Remote Tracking Sites (RTS) and the Consolidated Satellite Test Center (CSTC), operated by the U.S. Air Force (see Figure 49-8).

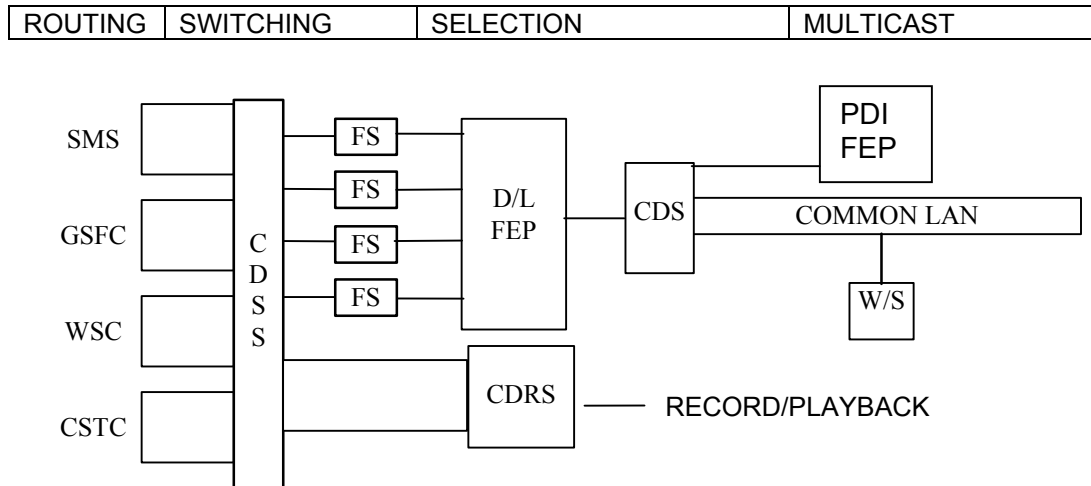


**Figure 49-8. SGLS mode telemetry**

### 49.3.3 MCC Telemetry Routing

Figure 49-9 is the MCC telemetry routing.





**Figure 49-9. MCC telemetry routing**

Telemetry streams are captured from the IP router for the applicable operational downlink and are switched to the appropriate Frame Synchronizer (FS) via the Consolidated Data Select Switch (CDSS). The D/L FEP then selects the stream to process as discussed in Section 49.3.2. After processing, the FEP outputs the telemetry in “multicast” messages; i.e., every workstation connected to the MCC common Local Area Network (LAN) that is logged onto the applicable activity will have the data addressed to it. The FEP interfaces to the common LAN via the Consolidated Distribution System (CDS), which is essentially a high-speed Fiber Optic Data Distribution Interface (FDDI) switch. The CDSS is also used to route the incoming streams to the Consolidated Data Recording Subsystem (CDRS), such that all telemetry data are backed up in the front end to allow restoration of data that are lost because of any MCC failure.

#### 49.3.4 Reconfiguration Processing

Originally designed for Telemetry Preprocessing Computer (TPC) and Mission Operation Computer (MOC) reconfiguration in the 1980’s, the MCC reconfiguration system has been adapted to help perform workstation and FEP reconfiguration also.

##### 49.3.4.1 Measurement and Stimulus (MAST II) System

Measurement and Stimulus (MAST) II is located in the JSC Software Production Facility (SPF). Specific telemetry characteristics for all TFLs and flights are maintained in the MAST II database. Data initialization and changes are input to MAST II via engineering forms and letters, vendor data packs, board directives, and Discrepancy Reports (DRs). Orbiter systems and payload control data are maintained in the MAST II Space Transportation Automated Reconfiguration (STAR) database.

#### 49.3.4.2 Shuttle Data Tape

MAST II produces the SDT, both engineering cycle and flight cycle versions, which are distributed to the major shuttle operations centers and contain the program-approved control data for all telemetry formats and calibrations (CALs). The SDT is used to build specific computer tables needed to decommutate and calibrate shuttle telemetry data.

Because of the sheer number of telemetry parameters in the SSP, most CALs are standard CALs, which are an average of actual CALs applicable to all vehicles. Actual CALs are required only when conditions such as communications transmission path variations are divergent enough to render standard CALs unusable. Multiple CALs are required only when operational phase or mode changes create these highly divergent conditions. The SDT contains both standard and actual calibration values, as well as curve 1 (default) for multiple calibration (multical) curves.

#### 49.3.4.3 Calibration Modification Dataset

MAST II also produces the CAL Modification (MOD) dataset, which contains updated actual CALs from late Line Replaceable Unit (LRU) changeouts, multiple sets for actual CALs required for onboard mode changes, unit conversions (such as metric to imperial), and other miscellaneous data not included on the SDT. One such type of data is for “piecewise” CAL conversions, in which a simulated CAL curve is produced using multiple straight lines. The CAL MOD dataset is vehicle specific and can change flight to flight if required by LRU changes or DRs. The SDT CAL is overridden in the MCC by the CAL MOD value if it exists for that MSID.

#### 49.3.4.4 CAL Data

CAL coefficients for SM GPC processing are found in the SM FSR Level C OI baseline document and are based on 10-bit processing, which means the coefficients will not be the same as used in the ground systems; however, the values viewed on a shuttle Cathode Ray Tube (CRT) should be practically identical to the values viewed at the same time on the ground. INCO/COMM Console Handbook Standard Console Procedure (SCP) 5.10 describes how to view and manipulate CAL coefficients used in the MCC.

MAST II also produces a CAL data book for each vehicle with all the CAL coefficients used in the MCC. Table 49-3 shows the difference between SM and ground CAL coefficients; notice that they are “proportional to each other” by the following equation.

$$(a_{n(\text{MCC})} / 2^n) = a_{n(\text{SM GPC})} \quad \text{example using } a_1 \text{ coefficient for V45V0100A}$$

$$1.6\text{E-}01 / 2^1 = 7.9999998\text{E-}02$$

**Table 49-3. SM CAL vs. MCC CAL for V45V0100A, all vehicles (standard CAL)**

|                        |                       |             |             |
|------------------------|-----------------------|-------------|-------------|
| SM CAL                 |                       |             |             |
| $a_0 = +4.9260014E-15$ | $a_1 = 7.9999983E-02$ | $a_2 = 0.0$ | $a_3 = 0.0$ |
| MCC CAL                |                       |             |             |
| $a_0 = 0.0$            | $a_1 = 1.600000E-01$  | $a_2 = 0.0$ | $a_3 = 0.0$ |

### 49.3.5 Front End Processing

#### 49.3.5.1 MCC FEP History

This section discusses only the D/L FEP function. Other FEP functions not covered here include uplink, ground to ground, dump, playback, and PDI.

The purpose of a D/L FEP is to provide specialized, repetitive processing services to off-load this processing from the rest of the control center. In the original shuttle MCC design, the decommutation was done by the Telemetry Preprocessing Computer (TPC), and the calibration was done by the MOC since calibration was more software intensive and the old TPC lacked the processing power for the additional CAL tasks. In an early modification to the MCC, there was a project to provide Calibrated Ancillary System (CAS) data to GSFC using a Masscomp workstation to decommutation and calibrate a few parameters. This idea was expanded later to include decommutation and CAL of the full shuttle telemetry stream using a more powerful Masscomp computer, called the Network Data Driver (NDD). This NDD software has been ported to the new FEP, which explains why decommutation and CAL are performed in software instead of the FEP Loral hardware (which is capable of running algorithms more efficiently). This evolution also dictated the FEP software architecture and processing flow.

#### 49.3.5.2 Frame Synchronization

Unblocked serial telemetry (either 96 or 192 kbps) is routed to four hardware frame sync units. The FS is programmed to accept a minor frame only if the shuttle sync pattern (FAF320<sub>H</sub>) is present in the current and previous minor frame received. Since the data may be coming inverted from the networks, the FS is programmed to invert the input from the CDSS when it detects an inverted Synchronization (sync) pattern in the incoming stream. The FS search, check, and lock criteria are all selectable.

The hardware FS sends accepted minor frames to the FEP validation function, which performs a software FS check before further processing. Operational Downlink Blocks (ODB) are sent to the Operational Data Reduction Complex (ODRC) because the ODRC needs to collect as much data as possible before invalidated data are filtered out.

#### 49.3.5.3 Validation

FEP software sets major frame validation status per the following criteria:

- A. The major frame contains 100 minor frames.
- B. All minor frames contain the full sync pattern.
- C. Minor frame counters are sequenced properly.

The validation function sends all minor frames to the next process, whether or not they passed validation checks.

#### 49.3.5.4 Data Cycle Packet

The FEP software then builds Data Cycle Packets (DCP) based on the following requirements:

- A. All OI in a DCP is from a 1-second OI cycle (to provide time homogeneity).
- B. One DCP contains about half of a 2-second GPC downlist cycle.
- C. The DCP contains OI, PDI, and GPC downlist.
- D. The DCP contains all minor frames (valid or invalid).

#### 49.3.5.5 Network Data Message

When the Network Data Message (NDM) function receives the DCP, it looks for the TFL ID so it can select the proper decom tables. Next, the DCPs are converted to NDMs, which means that the raw (uncalibrated PCM) OI parameter values in the validated major frames are placed into an order and format determined by the decom tables for an OI NDM; and the GPC downlist parameters from the current half-cycle are placed into a GPC NDM (one each per second). Each PDI format has its own PDI NDM structure, which is built to vary from 1 to 16 seconds for each NDM, depending on the payload telemetry format cycle.

#### 49.3.5.6 Processed Telemetry Message

Using current FEP CAL tables (including overridden CAL curves), the FEP calibrates applicable OI and GPC parameters from their respective NDMs and places them into an OI Processed Telemetry Message (PTM) and a GPC PTM, both of which are output to the common LAN once per second. The FEP has algorithms using mode, frequency, etc., to select the proper CAL curve number from a multiple set.

#### 49.3.5.7 Processed Payload Message

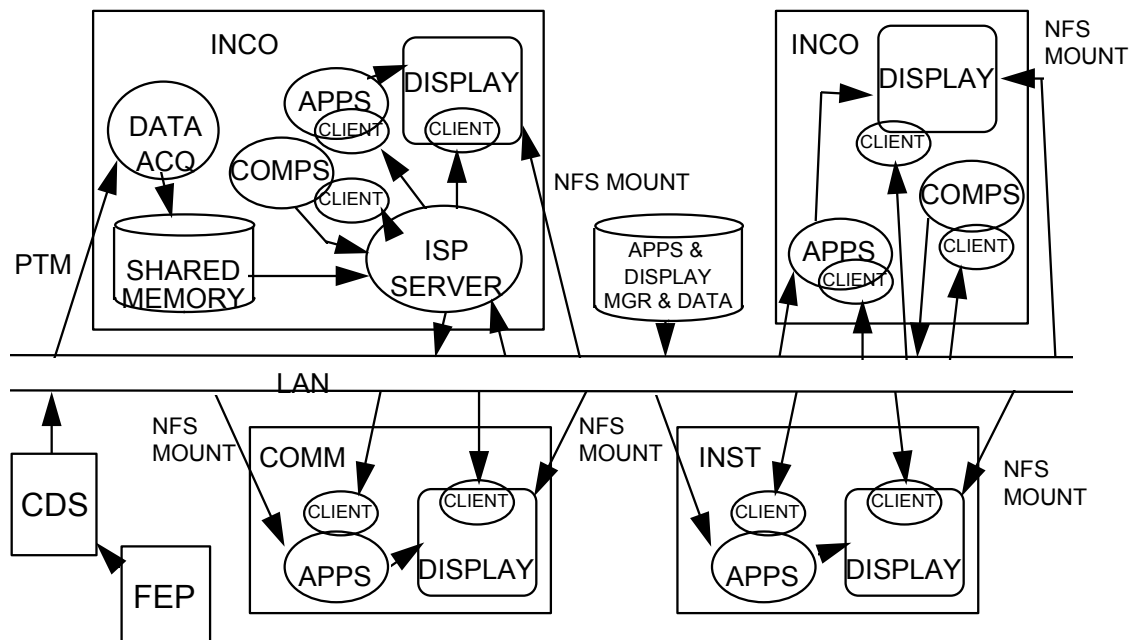
Using current FEP CAL tables, the FEP calibrates applicable parameters from the PDI NDM and places them into a Processed Payload Message (PPM) corresponding to the

data cycle defined for the NDM and outputs the PPM to the common LAN; these can be received and further processed by the PDI FEP. Built-in security features prevent proprietary payload data from being multicast to the general user.

#### 49.3.5.8 Multicast

PTMs are multicast to all W/S that are on the common LAN system and are logged into the proper activity. The W/S does not Acknowledge (ACK) receipt of the multicast PTM because retransmissions following no ACKs would increase PTM overhead and an occasional loss of a PTM is acceptable since the data are cyclic. A Data Acquisition (DACQ) application in the FEP sends the PTM to the DACQ in the W/S.

#### 49.3.6 Workstation Processing



**Figure 49-10. Workstation telemetry processing**

Workstation applications (apps), display managers, and display data are stored on a central, configuration-managed server. A Network File System (NFS) mount technique is used to run apps and displays in a virtual on-line mode, where the code is downloaded only when needed while running in real time.

##### 49.3.6.1 PTM DACQ

DACQ was developed as a means of cyclically multicasting real-time data to a virtually unlimited number of users on a high-speed LAN. W/S DACQ acquires the full-rate data stream (PTM) and places it into W/S shared memory, where other apps may acquire the data for further processing.

In the INCO area, the FCR W/S runs DACQ under control of Network Autopilot (NAP), which looks for an Information Sharing Protocol (ISP) server and starts another one if the active server fails.

#### 49.3.6.2 ISP

ISP is an application for distributing change-only parameter values to all users, based on client/server relationships. One FCR W/S will run the server, and all W/S apps and comps that use INCO ISP data will run clients.

NAP monitors the ISP server and comps, and if a server or a comp fails, NAP will try to restart it on another W/S that is running DACQ, which is normally the alternate INCO W/S. In case INCO is unable to run ISP on either W/S, a back room user has to select **Start Data** on the **INCO Data ACQ** menu to allow NAP to move the program execution to that W/S. **Show Connections** under **INCO Data ACQ** will show which INCO comps are running on which workstations.

#### 49.3.6.3 Comps

Comps are used either to combine several parameters in order to present a consolidated snapshot of a set of conditions or to convert the data into a more user-friendly symbol or unit of measurement. For example, three discrettes are sampled in a comp to determine SSR mode (comp output = STBY, RCDA, PBQ1024, etc.). This comp allows the DataCOMM officer to determine what mode their SSR is without having to decipher three separate discrettes. The INCO telemetry comp certification folder contains the description and code for the INCO comps.

#### 49.3.6.4 Displays and Apps

INCO displays and apps display telemetry data to the flight controller in a more convenient manner. Displays are built using data files that run in real time, using predefined display managers to present the data to the user. The data files contain the definitions of parameter types, output colors, and location.

Apps are used when the standard display does not possess the flexibility to present the data to the user in the desired manner, or to allow proper user interaction with the display. For example, the SSR Management was designed as an application because there were no standard display builders/managers that allowed the desired user interaction and telemetry information for the solid-state recorders. INCO displays are described in Section 7 of the Console Handbook, while apps are described in Section 7 or 9 of the Console Handbook.

### **49.3.7 Dump Processing and Archiving**

#### **49.3.7.1 Dump FEP**

Telemetry data stored onboard in the solid-state recorders are dumped through TDRS satellites, RTS sites, or GSTDN sites throughout a mission. These playbacks are captured in the dump FEP in MCC at an 8:1 ratio (data only), or a 5:1 ratio (data + voice). The dump FEP buffers all the playback data from a dump, and sorts it in order of onboard time occurrence. This dump FEP buffer is then played to a Playback (PB) FEP, where it is formatted for transmission to the ODRC at a 1:1 ratio.

Occasionally a buffer overflow condition in the dump FEP occurs. This takes place when the playback from the orbiter or ground site contains more data than the buffer in the dump FEP can hold. DFE can remedy the situation by reconfiguring the buffer to accept larger playbacks, but the overflow data must be re-dumped into the dump FEP by the DataCOMM officer.

#### **49.3.7.2 ODRC Functional Description**

The ODRC receives raw (uncalibrated) telemetry from the D/L and PB FEPs and stores the raw data in memory and on optical disks for archival. The ODRC has the ability to retrieve raw data and send them to the user as uncalibrated, calibrated per the SDT, or calibrated per MCC CAL. The ODRC determines frequently requested data per algorithms and stores them locally in memory or hard drive. During a flight, for example, the past few real-time hours of the current flight are stored locally. In order to reduce the amount of data traffic, the ODRC sends out change-only data. The user may request dump data only, real-time data only, or the best of the two. The most frequently used application for retrieving ODRC data is the Mission Evaluation Workstation System (MEWS), which is found under Global APPS on the Master DNAV menu.

The ODRC is required to support shuttle telemetry, Shuttle Avionics Integration Laboratory (SAIL) test data, shuttle PDI data, on-orbit simulation data, main engine data, Launch Processing System (LPS) data, and space station telemetry.

#### **49.3.7.3 GPC Dumps**

When GPC dumps are performed, there is a Data Processing System (DPS) application that is used to process the dumped data in real time. GPC dump data cannot be retrieved from ODRC since it does not have an MSID for decom and retrieval. If the GPC dump is re-dumped from an SSR, the dump FEP can play it back to the PB FEP as with any dump, and the PB FEP outputs the GPC dump data on the common LAN to the DPS application for processing. Real-time GPC dumps are also output to the SPF via the CDS for further processing.

#### 49.4 REFERENCE

- A. Integrated Communications Officer/Communications Console Handbook, JSC-12829.
- B. Orbiter Instrument Program and Components List (IPCL), SSD96D0056.
- C. Space Shuttle Systems Handbook, JSC-11174.
- D. NSTS Computer Program Development Specification (CPDS) Downlist/Uplink Software Requirements, SS-P-0002-140.
- E. Space Shuttle Telemetered and Recorded Data Format Requirements, NSTS-10874.
- F. Payload Management Level C Flight Software Requirements, JSC-19478.
- G. Systems Management Level C Flight Software Requirements, JSC-19590.
- H. Consolidated Communications Facility (CCF) Systems Specification, JSC-13500.



THIS PAGE INTENTIONALLY BLANK

## SECTION 70 - CLOSED CIRCUIT TELEVISION

### CONTENTS

| Section |   | Page  |
|---------|---|-------|
| 70.1    | CLOSED CIRCUIT TELEVISION OVERVIEW.....                         | 70-1  |
| 70.1.1  | Video Control Unit .....  | 70-1  |
| 70.1.2  | Electrical Description of RCU and VSU.....                      | 70-8  |
| 70.1.3  | RCU, VCU Installation.....                                      | 70-12 |
| 70.2    | TELEVISION CAMERA.....  | 70-12 |
| 70.2.1  | Camera Location Code .....                                      | 70-14 |
| 70.2.2  | Power Switching.....  | 70-14 |
| 70.2.3  | Automatic Light Control .....                                   | 70-14 |
| 70.2.4  | Gain Settings.....  | 70-15 |
| 70.2.5  | Pan/Tilt Unit Description.....                                  | 70-15 |
| 70.2.6  | Stepper Motors.....   | 70-15 |
| 70.2.7  | CCTV Camera and PTU Heaters .....                               | 70-15 |
| 70.2.8  | Remote Video Switcher Description .....                         | 70-16 |
| 70.2.9  | External Switches.....  | 70-16 |
| 70.3    | CCTV SYSTEM OPERATION.....                                      | 70-16 |
| 70.3.1  | Command.....  | 70-16 |
| 70.3.2  | Telemetry .....   | 70-25 |
| 70.3.3  | Camera Powerup .....  | 70-26 |
| 70.3.4  | Ground Camera Selection.....                                    | 70-26 |
| 70.3.5  | Onboard Camera Selection.....                                   | 70-28 |
| 70.3.6  | Conflict Resolution Between Ground and Onboard Commanding ..... | 70-30 |
| 70.3.7  | Voice Interleaver and Asynchronous Mode (Ground Only) .....     | 70-31 |
| 70.3.8  | Suggested Techniques for TV Ops .....                           | 70-33 |
| 70.3.9  | Telemetry .....   | 70-34 |
| 70.4    | SPECIAL TM COMPS.....   | 70-36 |
| 70.5    | CCTV OPERATIONAL IDIOSYNCRASIES.....                            | 70-37 |
| 70.6    | CAMERA LENS CAPABILITIES .....                                  | 70-39 |

## TABLES

| Table |   | Page  |
|-------|---|-------|
| 70-1  | CCTV commands .....                     | 70-4  |
| 70-2  | CCTV power consumption .....            | 70-11 |
| 70-3  | Telemetry .....                         | 70-35 |
| 70-4  | CCTV lenses field-of-view ranges .....  | 70-39 |
| 70-5  | General mechanical specifications ..... | 70-40 |

## FIGURES

| Figure |   |       |
|--------|---|-------|
| 70-1   | Remote control unit overview .....                  | 70-3  |
| 70-2   | Video switching unit .....                          | 70-9  |
| 70-3   | CCTV camera locations .....                         | 70-13 |
| 70-4   | CTVC camera with local controls .....               | 70-17 |
| 70-5   | CCTV command structure .....                        | 70-18 |
| 70-6   | RCU flowchart .....                                 | 70-19 |
| 70-7   | Uplink command interface sampling .....             | 70-21 |
| 70-8   | Camera command detection/execution .....            | 70-22 |
| 70-9   | Vertical interval data (sheet 1 of 2) .....         | 70-23 |
| 70-10  | PNL A7 Camera controls .....                        | 70-28 |
| 70-11  | Output of the MUX when one source is inactive ..... | 70-33 |
| 70-12  | CCTV component locations (cabin) .....              | 70-40 |

## SECTION 70 CLOSED CIRCUIT TELEVISION

### 70.1 CLOSED CIRCUIT TELEVISION OVERVIEW

The Closed Circuit Television (CCTV) system provides U.S. analog broadcast standard television (RS-170) to support orbiter and payload activities. The CCTV system is fully compatible with National Television System Committee (NTSC) color, with the exception of the split-screen Multiplexer (MUX). All CCTV cameras operate in master sync with all switching and motor movement done during the vertical interval to avoid any interference problem. Some video sources on the orbiter do not use the master sync because of Commercial Off The Shelf (COTS) design or because they use a Radio Frequency (RF) transmission path.

The Color Television Monitors (CTVMs), Video Tape Recorder (VTR), camcorders, Color Television Camera (CTVC), Intensified Television Camera (ITVC), Video Processing Unit (VPU), Television Controller Unit (TVCU), and Wireless Video System (WVS) are discussed in other sections. This brief analyzes the Remote Control Unit (RCU), Video Switching Unit (VSU), Pan/Tilt Unit (PTU), and basic camera interfaces.

This brief addresses the operation of the CCTV from a ground point of view. For thoroughness, some onboard operation is included. Reference should be made to Space Shuttle Systems Handbook (SSSH) drawings 16.1-5 (CCTV OV), 16.12 (CCTV Control), 16.12-2 (VPU), and 16.13 (CCTV Camera and Monitor).

#### 70.1.1 Video Control Unit

The Video Control Unit (VCU) is the heart of the CCTV system. It consists of two separate Line Replaceable Units (LRUs), the RCU, and the VSU.

##### 70.1.1.1 RCU Overview

The RCU performs the following functions:

- A. Receives and processes commands from the crew switch panel (panel A7U) and from the Payload Forward 2 (PF 2) Multiplexer/Demultiplexer (MDM) (commands from the Mission Control Center (MCC) or the Orbiter Space Vision System (OSVS))
- B. Turns on power to the cameras by furnishing a poweron discrete to each camera
- C. Sends camera configuration commands issued by the crew or by the ground out to the camera as part of the sync signal

- D. Generates the test pattern, which is used to check out the system or adjust a crew monitor, and the sync signal, which is sent out to each camera. This sync signal carries commands to the camera and allows the camera video to be synched to the VCUs.
- E. Drives the talkbacks on the crew switch panel (A7)
- F. Sends outputs to the Orbiter Instrumentation (OI) MDM OF 4 for downlink to the MCC and use by the Systems Management (SM) computer (the camera overtemperature (overtemp) alert).

### 70.1.1.2 Interfaces and Block Diagram

The interfaces are summarized in Figure 70-1.

#### A. RCU inputs

##### 1. Panel A7 switch inputs

The switches on panel A7U are all wired to the RCU. When a switch is pressed, the state of the switch is latched in a flip-flop and stored until the RCU microprocessor reads the flip-flop. The switches are shown on the SSSH drawing.

##### 2. MDM commands

Commands are received from the PF 2 MDM, card 7, and channel 1 as 14 parallel inputs. (The bits are described in Figure 70-6.) The commands are listed in Table 70-1.

##### 3. MDM command enable

A single line from the Ground Control Interface Logic (GCIL) TV control switch (the MNC side) on panel A7U is routed to the RCU and used to enable the MDM commands. If this discrete is low (switch in PANEL position), the RCU will not process any MDM commands. The TV control switch affects uplink commands as well as those from the OSVS.

##### 4. Power

Power is received from Main A R14 and Main B R14. Circuit breakers for each power source are on panel R14. The RCU switches the power on based on GCIL power control discretetes. The Space Shuttle Program (SSP) still refers to this panel as R15 in order to avoid the cost of changing all references to this panel in all the SSP documentation.

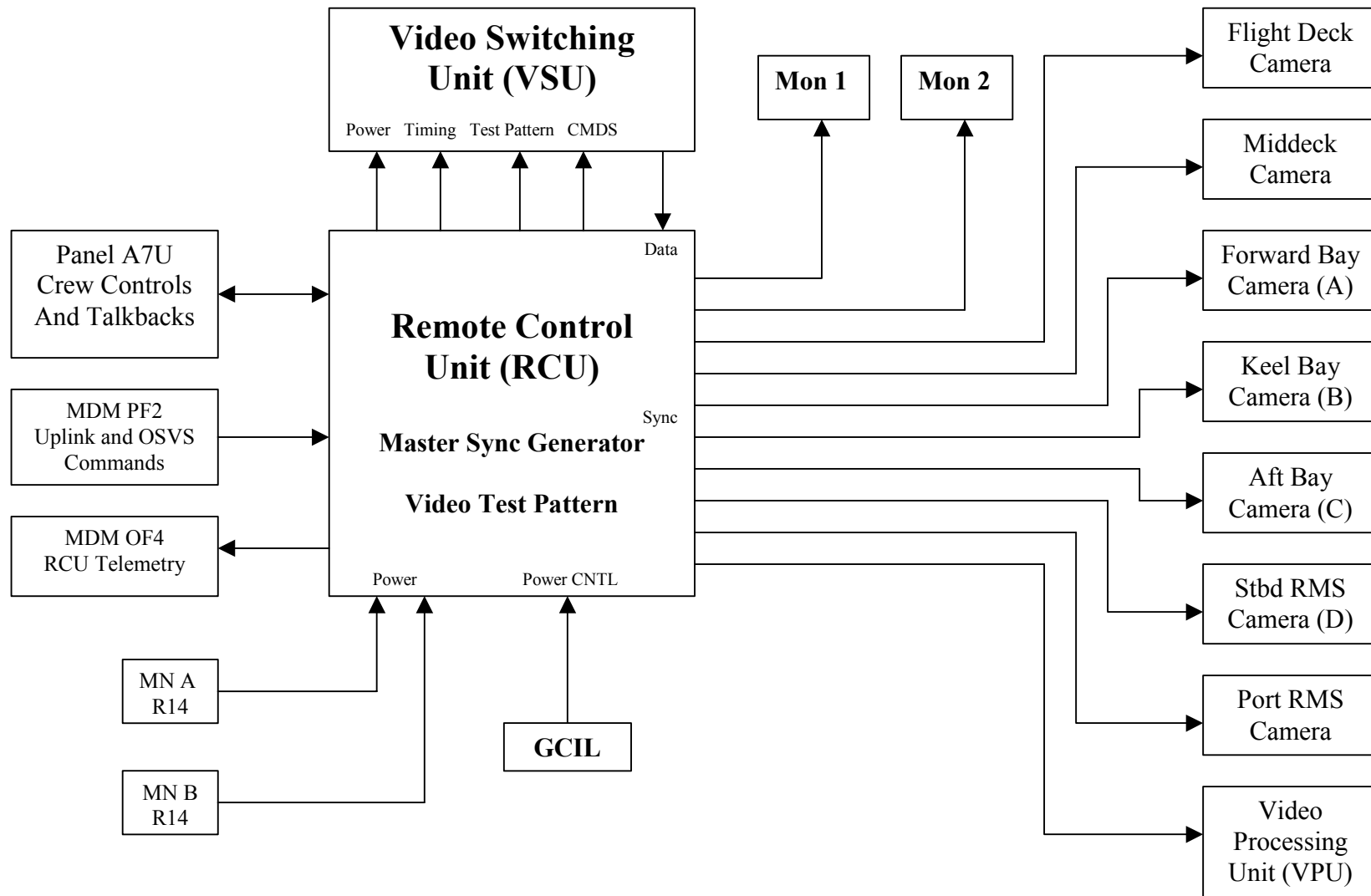


Figure 70-1. Remote control unit overview

There are four basic CCTV command types, as listed in Table 70-1.

**Table 70-1. CCTV commands**

A. GCIL Commands

4200 VCU MAIN A ON  
4201 VCU OFF  
4202 VCU MAIN B ON

B. STANDALONE Commands

These commands are STANDALONE. They set bits 7-13 on the RCU command interface but do not depend on bits 2-6.

| <u>Standalone commands</u>   | <u>Bits 7-13</u> |
|------------------------------|------------------|
| 4207 Audio Interleaver A ON  | 0010101          |
| 4208 Audio Interleaver B ON  | 0010110          |
| 4209 Audio Interleaver AB ON | 0010111          |
| 4210 Audio Interleaver OFF   | 0010100          |
| 4286 VSU ASYNC               | 0010011          |
| 4287 VSU SYNC                | 0010010          |

C. SOURCE Commands

These are SOURCE commands. They set bits 2-6 on the RCU interface, but the RCU takes no actions until all zeros in bits 7-13 are seen. Then the combined command (all 14 bits) is executed.

| <u>Source commands</u>   | <u>Bits 2-6</u> |
|--------------------------|-----------------|
| 4230 TV FLT DECK SEL     | 00000           |
| 4231 TV Mid Deck Sel     | 01000           |
| 4232 TV FWD BAY (A) Sel  | 00001           |
| 4233 TV KEEL (B) Sel     | 00101           |
| 4234 TV Aft Bay (C) Sel  | 00010           |
| 4235 TV Port RMS Sel     | 00110           |
| 4236 TV STBD RMS (D) Sel | 00111           |
| 4240 TV Port RMS Sel     | 01010           |
| 4241 TV Mux 2 Sel        | 01011           |
| 4242 TV PL 1 Sel         | 01101           |
| 4243 TV PL 2 Sel         | 01110           |
| 4244 TV PL 3 Sel         | 01111           |
| 4215 TV SPR INP (VTR PB) | 00011           |
| 4251 TV Test Pattern Sel | 01001           |
| 4221 TV CAM ADD 17       | 10001           |
| 4222 TV CAM ADD 18       | 10010           |

*Table 70-1. CCTV commands (continued)*

|                    |       |
|--------------------|-------|
| 4223 TV CAM ADD 19 | 10011 |
| 4224 TV CAM ADD 20 | 10100 |
| 4225 TV CAM ADD 21 | 10101 |
| 4226 TV CAM ADD 22 | 10110 |
| 4227 TV CAM ADD 23 | 10111 |
| 4228 TV CAM ADD 24 | 11000 |
| 4229 TV CAM ADD 25 | 11001 |
| 4288 TV CAM ADD 26 | 11010 |
| 4289 TV CAM ADD 27 | 11011 |
| 4290 TV CAM ADD 28 | 11100 |
| 4291 TV CAM ADD 29 | 11101 |
| 4292 TV CAM ADD 30 | 11110 |
| 4293 TV CAM ADD 31 | 11111 |

D. OUTPUT/FUNCTION Commands

The OUTPUT/FUNCTION commands affect bits 7-13 and thus cause command execution. The camera address that is sent along with these commands is specified by bits 2-6. The command is sent to the camera by setting a bit in the 32-bit camera command field to a 1. The OUTPUT/FUNCTION commands are split into four groups.

Group 1

These commands are acted on by the RCU and are **not** issued to the cameras.

| <u>Output/function commands</u> | <u>Bits 7-13</u> | <u>CAM CMD BIT (0-31)</u> |
|---------------------------------|------------------|---------------------------|
| 4204 TV CAM PWR ON              | 0010000          | --                        |
| 4205 TV CAM PWR OFF             | 0010001          | --                        |
| 4216 SPR OUT (VTR)              | 0000101          | --                        |
| 4217 SPR 1 OUTPUT               | 0000110          | --                        |
| 4218 SPR 2 OUTPUT               | 0000111          | --                        |
| 4245 TV MUX 1 LEFT              | 0001000          | --                        |
| 4246 TV MUX 1 RIGHT             | 0001001          | --                        |
| 4247 TV MUX 2 LEFT              | 0001010          | --                        |
| 4248 TV MUX 2 RIGHT             | 0001011          | --                        |
| 4249 TV DOWNLINK                | 0000011          | --                        |
| 4250 TV PAYLOAD                 | 0000100          | --                        |
| 4262 TV FOCUS STOP              | 0011101          | --                        |
| 4265 TV ZOOM STOP               | 0011110          | --                        |
| 4268 TV IRIS STOP               | 0011100          | --                        |
| 4272 TV TILT STOP               | 0011001          | --                        |
| 4275 TV PAN STOP                | 0011000          | --                        |



**Table 70-1. CCTV commands (continued)**

Group 2

These commands are transmitted to the cameras and repeated every field until stopped.

| <u>Output/function commands</u> | <u>Bits 7-13</u> | <u>CAM CMD BIT (0-31)</u> |
|---------------------------------|------------------|---------------------------|
| 4260 TV FOCUS NEAR              | 0111011          | 27                        |
| 4261 TV FOCUS FAR               | 0111010          | 26                        |
| 4263 TV ZOOM IN                 | 0111101          | 29                        |
| 4264 TV ZOOM OUT                | 0111100          | 28                        |
| 4266 TV IRIS OPEN               | 0111001          | 25                        |
| 4267 IRIS CLOSE                 | 0111000          | 24                        |
| 4270 TV TILT UP                 | 0110110          | 22                        |
| 4271 TV TILT DOWN               | 0110111          | 23                        |
| 4273 TV PAN LEFT                | 0110101          | 21                        |
| 4274 TV PAN RIGHT               | 0110100          | 20                        |

Group 3

These commands are transmitted to the cameras but only once for every reception of the command.

| <u>Output/function commands</u> | <u>Bits 7-13</u> | <u>CAM CMD BIT (0-31)</u> |
|---------------------------------|------------------|---------------------------|
| 4212 CAM AUX ON                 | 0101111          | 15                        |
| 4213 CAM AUX OFF                | 0101110          | 14                        |
| 4278 TV PAN/TILT RESET          | 0110001          | 17                        |
| 4280 Select ALC MENU            | 0101000          | 8                         |
| 4281 Select MAN GAIN MENU       | 0101001          | 9                         |
| 4282 Select BAL MENU            | 0101010          | 1                         |
| 4283 PEAK/0db/BAY or Night      | 0101011          | 11                        |
| 4284 NORM/12db/CABIN or<br>Day  | 0101100          | 12                        |
| 4285 AVG/24db/SUN or Night      | 0101101          | 13                        |

Group 4

These commands are sent to every field that a pan or tilt is commanded. One of them will always be on for a pan or tilt.

| <u>Output/function commands</u> | <u>Bits 7-13</u> | <u>CAM CMD BIT (0-31)</u> |
|---------------------------------|------------------|---------------------------|
| 4276 TV PAN/TILT FAST           | 0110011          | 19                        |
| 4277 TV PAN/TILT SLOW           | 0110010          | 18                        |

Camera command bit positions 0 through 7, 16, 30, and 31 are spare.

5. GCIL power control discretetes

The GCIL furnishes power control discretetes to the RCU for power on/off. The two discretetes are for MNA power on and MNB power on. The GCIL interlocks the two so that both cannot be on at the same time (the RCU also interlocks the two). Control buses AB1 and BC1 provide GCIL control power for MNA and MNB, respectively.

B. RCU outputs

1. Sync/command lines

This is a standard TV signal with the video scene "black" and commands encoded on lines 11 or 13. This is routed to all cameras and to the payload interface so that the cameras can run in sync with the RCU and receive commands from the RCU. The commands are summarized in Table 70-1. The same signal (minus the commands) is also sent to the two television monitors installed in the A3 location of the aft flight deck. The color monitors use this signal for displaying the user-interface menu, alphanumeric, and graphics when video is not received from the VSU.

2. Clock

This is a 2.045-MHz clock routed to the VSU for timing. There is also an oddframe start pulse sent to the VSU for timing.

3. Panel A7 talkbacks

The RCU furnishes 28-V discretetes for all panel A7U talkbacks. Some of these discretetes run to the Annunciator Control Assembly (ACA) that controls the brightness of the indicator lights, and some other discretetes are routed directly to the panel. The ACA control is on panel A6U. See SSSH Drawing 16.12-1.

4. Camera power ON discretetes

The RCU furnishes 28-V discretetes to all cameras for camera power on control. The camera senses the state of its control discrete and turns itself on when the discrete is high. No positive feedback tells the RCU that the camera is powered. Thus, the camera power talkbacks on panel A7 and telemetry actually indicate that the RCU has set the camera power on discrete high.

5. MDM telemetry

The RCU furnishes 28-V discretetes to MDM OF 4 for ground telemetry and crew alert for camera overtemp. The telemetry is summarized in Section 70.3.2. With the proliferation of asynchronous video sources on the orbiter, the overtemp alert is generally inhibited onboard to avoid nuisance alarms via uplink command.

### 70.1.1.3 VSU

The VSU performs the following functions:

- A. Receives video from all cameras, VTRs, and payload sources and routes it to crew monitors and the downlink (S-band FM and Ku-band systems). The instructions on what to send and where to send it are received from the RCU (which receives them from the crew panel or the PF 2 MDM).
- B. Adds timetags to the video signal received from the cameras. The time information is received from the master timing unit.
- C. Provides two split-screen MUXs. These allow two scenes to be viewed together, one on the left and one on the right.
- D. Decodes telemetry received from the cameras, displays the data on the crew television monitors, and sends the data to the RCU for display on the A7 panel and for downlink to the MCC. Each CCTV monitor can enable the VSU to overlay camera telemetry (camera ID, pan/tilt angles, and temperature - when overtemp condition is sensed) and crosshairs on the video routed from the VSU to each monitor.
- E. Limit-senses the temperature of each camera (the temperature is encoded in the video by each camera) and alerts the crew and the ground if an overtemp is sensed. This is done by displaying the temperature on the crew monitor, sending a signal to the RCU, which sets a discrete to an OI MDM (which is downlinked to the MCC and used to set off an alert by the SM computer), and inserting a flag into the downlink video, which causes the temperature data on the Instrumentation and Communications Officer (INCO) ground monitor to flash.

### 70.1.1.4 Interfaces

The interfaces for the VSU are shown in Table 70-2.

## 70.1.2 Electrical Description of RCU and VSU

### 70.1.2.1 RCU

The RCU consists of four major components.

#### 70.1.2.1.1 Power supply

The power supply switches at the horizontal line rate to avoid interference and supplies power to all RCU and VSU circuits. Power is delivered to the RCU power supply from MNA or MNB, but not both. There is GCIL control over the main bus selection. There is no automatic switchover in case of power loss.

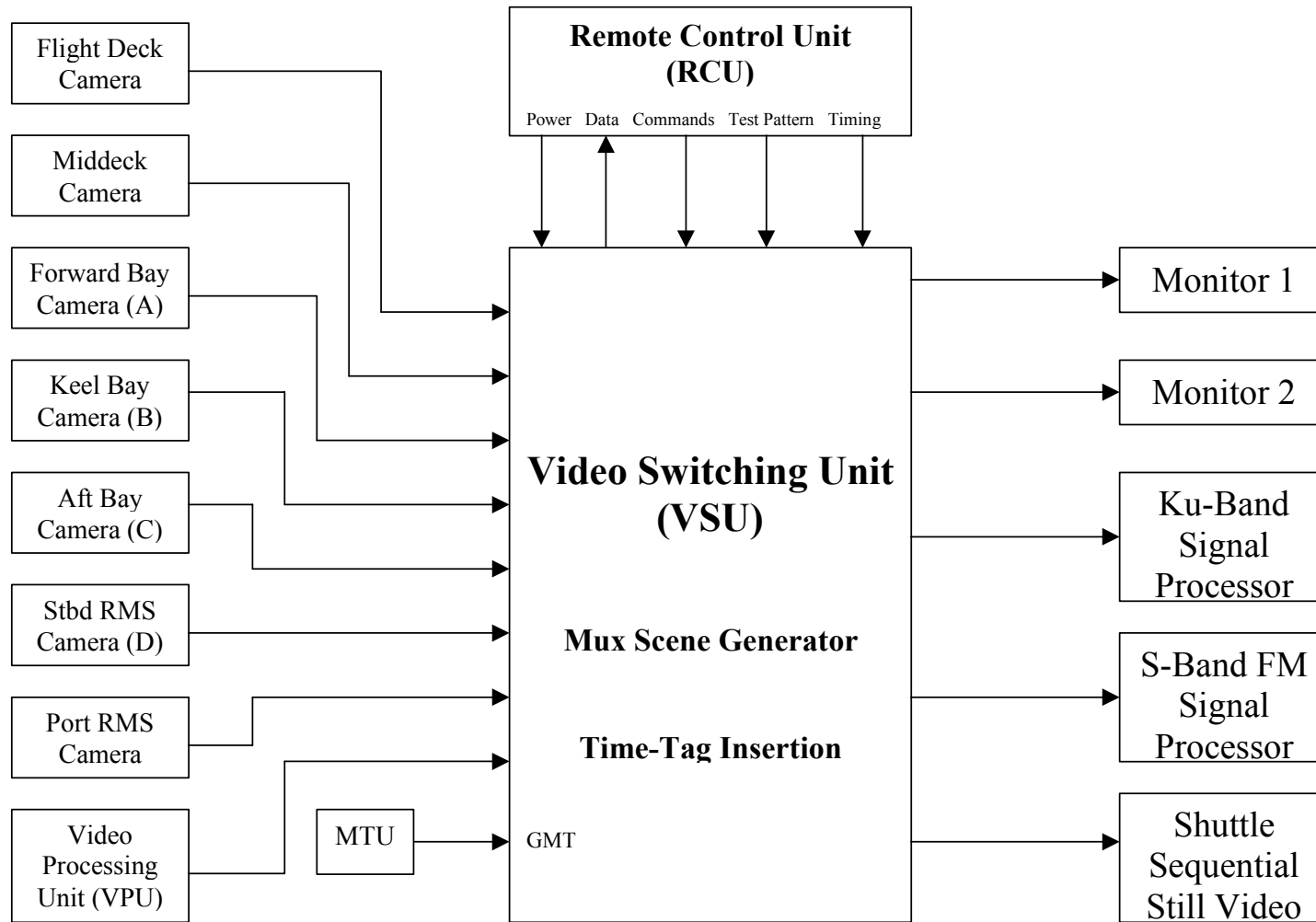


Figure 70-2. Video switching unit

#### **70.1.2.1.2 Sync generator and timing circuits**

The sync generator has redundant 14.318180-MHz oscillators. There is no automatic failover. Oscillator A runs when MNA is powering the RCU, and oscillator B runs when MNB is powering the RCU. The crew can reverse this with the TV SYNC switch located on crew panel A7U (oscillator A with MNB, etc.). The timing circuits generate the line count and subline count, which control data clocking to cameras and to and from the VSU. During lines 11 and 13, command data are clocked from data buffers (where the microprocessor stored it) and multiplexed on the composite sync routed to all cameras. Also during line 11, data are clocked from the RCU to the VSU. The timing circuits furnish a 2.045-MHz timing signal and an odd field start signal to the VSU so that the VSU can sync with the RCU. The timing circuits also generate the Vertical Interval Test Signal (VITS) and the Full Field Test Signal (FFTS). The signature for a failed sync generator includes loss of almost all commanding to the CCTV system. Power control of the RCU/VSU via GCIL (crew or MCC) as well as sync generator select (crew only) are the only configuration changes possible if the operating sync generator fails.

#### **70.1.2.1.3 Microprocessor**

The RCU is controlled by an RCA 1802 CMOS microprocessor with 4k bytes of Programmable Read-Only Memory (PROM) and 256 bytes of Random Access Memory (RAM). The microprocessor runs through its program and idles until a line 1 interrupt is issued by the timing circuits. It then runs through the same program again. This is discussed further in Section 70.3

#### **70.1.2.1.4 Input/output storage buffers**

There are several buffers that store data until the timing circuits clock the data out (as is the case for camera commands) or until the microprocessor reads the contents (via an 8-bit data bus). The output buffers are loaded by the microprocessor or by a direct memory addressing scheme. Many of the output buffers have relays associated with them to furnish 28-V discretes to the OI MDM or to the A7U panel talkbacks.

#### **70.1.2.1.5 Power use**

The RCU draws 46 watts of power. This includes the power supplied to the VSU. Power for all elements of the CCTV system is shown in Table 70-2.

#### **70.1.2.2 VSU**

The VSU is also microprocessor-based. It can be split into three major parts.

**Table 70-2. CCTV power consumption**

| LRU   | Current               | Power (at 28 V)                  |
|---|-----------------------|----------------------------------|
| RVS <sup>a</sup>                              | .34 mA                | .00952 W .01 W                   |
| RCU/VSU <sup>b</sup>                          | 1.25A VSU loads low   | 35.0 W                           |
|   | 1.65A VSU loads high  | 46.2 W                           |
| PTU <sup>b</sup>                              | 6.9 mA - IDLE         | .19 W                            |
|   | 92.9 mA - PAN         | 2.60 W                           |
|   | 98.6 mA - TILT        | 2.76 W                           |
|   |                       | .19 W - 1 DLE (2.49 W per MTR)   |
|   |                       | 2.68 W - 1 MTR                   |
|   |                       | 5.17 W - 2 MTR                   |
| TVC (508) <sup>a</sup> w/<br>MLA <sup>a</sup> | 687 mA                | 19.24 W                          |
|   | +80 mA per lens MTR   | 2.24 W - focus, zoom or iris     |
| CTVC <sup>d</sup>                             | 764 mA - IDLE         | 21.40 W - IDLE                   |
|   | +116 mA shutter       | 3.25 W - shutter                 |
|   | +75 mA per motor      | 2.10 W - focus, zoom, or iris    |
| ITVC <sup>e</sup>                             | 617 mA – IDLE         | 17.28 W - IDLE                   |
|   | +125 mA focus or iris | 3.50 W - focus or iris           |
|   | +252 mA zoom          | 7.06 W - zoom                    |
| VFM <sup>a</sup>                              | 185 mA                | 5.18 W                           |
| CTVM <sup>f</sup>                             | 1.94 A                | 54.40 W                          |
| PTU HTR <sup>c</sup>                          | 293 mA                | 8.20 W                           |
| CAMR HTR                                      | 711 mA                | 19.90 W – TVC (508) <sup>c</sup> |
|   | 849 mA                | 23.76 W – CTVC <sup>g</sup>      |
|   | 982 mA                | 27.50 W – ITVC <sup>e</sup>      |

<sup>a</sup> Refer to V. FRY 6/23/80 ACCEPTANCE TEST DATA.

<sup>b</sup> Refer to Will Fraley 6/24/80.

<sup>c</sup> Refer to EEL 1/14/80.

<sup>d</sup> Refer to CTVC Critical Design Review Viewgraph Package no.1, 1989, p. 2-008.

<sup>e</sup> Refer to ITVC Critical Design Review Viewgraph Package, 1992, p. 275.

<sup>f</sup> Refer to CTVM Critical Design Review Viewgraph Package no.1, 1988, p. LJW-4.

<sup>g</sup> Refer to CTVC Critical Design Review Viewgraph Package no.2, 1989, p. 6-057.

#### **70.1.2.2.1 Microprocessor**

The microprocessor uses 2k bytes of PROM and 256 bytes of RAM. The VSU microprocessor program also runs once every video field. The microprocessor interfaces with two 32-byte RAMs used for control of the alphanumeric/character generators, also. The alphanumeric characters are displayed on the CTVMs when enabled by the monitor C-DATA and X-HAIR menus (see Section 74 for details). The character generators are driven by the timing circuits and use data stored by the microprocessor in the 32-byte RAM.

#### **70.1.2.2.2 Timing circuits**

These circuits use the 2.045-MHz clock and the odd field signal from the RCU to generate line counts and subline counts. They are used to clock in the RCU data (commands), clock out the camera data to the RCU, and control data acquisition from the cameras. The logic sequences through the 12 possible cameras, sampling each camera for 3 fields to wait on a field sequential color sync signal (on a "green" field) so that temperature can be read. Thus, any camera is sampled every 39 fields or 650 msec. Although the Field Sequential Color (FSC) cameras are no longer flown, this design can create a usual signature with the ITVC. The ITVCs insert temperature on two of three fields (the 508/FSC cameras inserted temperature on one of three fields (the "green" field), and the CTVC inserts temperature on every field). Since the ITVC was not designed to insert temperature on any two specific fields (out of three), the ITVC occasionally powers up such that temperature is not located on the VSU green field and thus the temperature is not sensed by the VSU. If temperature is not detected by the VSU, it will not output camera telemetry to the RCU for display as feedback on the crew panel A7U Pushbutton Indicators (PBIs), nor is the telemetry available for downlink through OF 4 MDM. The VSU must detect a temperature pulse on line 18 of a green field from a CCTV camera before providing camera mode status to the RCU for driving the panel A7U PBIs as well as the MDM OF 4 camera status telemetry.

#### **70.1.2.2.3 Video matrix**

This is simply a matrix of Field Effect Transistor (FET) switches that allow any input to be connected to any output (also called a crossbar). The matrix is controlled from the input shift register. The microprocessor does not control the matrix.

#### **70.1.3 RCU, VCU Installation**

The RCU and VCU are installed in the crew cabin on the starboard side of the flight deck. They are both forced-air cooled by cabin air.

### **70.2 TELEVISION CAMERA**

All CCTV cameras can be mounted in any designated location in the payload bay. Commands and synchronization are received from the RCU, and video is output to the Viewfinder Monitor (VFM) port and to the VSU. External (local) controls are located on the side of the cameras. Currently, the SSP manifests the CTVCs and ITVCs for

missions (with or without illuminators). Figure 70-2 shows camera locations in the payload bay.

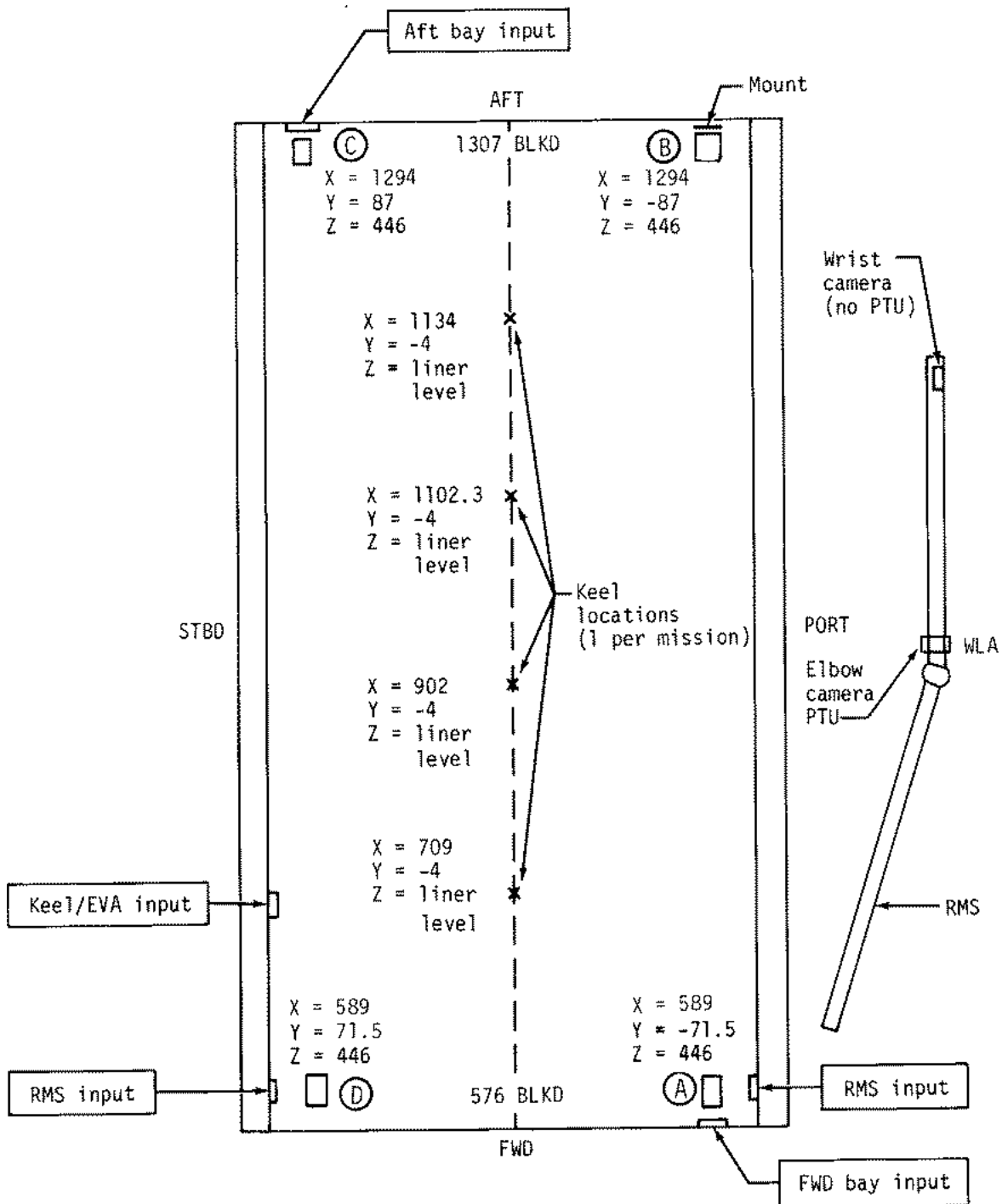


Figure 70-3. CCTV camera locations



### 70.2.1 Camera Location Code

Each camera commanded by the RCU must have a unique address. The address is determined by the location where the camera is connected (i.e., FWD BAY). This is accomplished by a hardwired 5-bit code in the bulkhead connector (selected pins are shorted to common). Thus, any camera can be connected by any input and respond to the location address. Note, it is possible for more than one connection to have the same location address. For example, the Orbiter Docking System (ODS) television ports 1 and 2 are both addressed as PL2.

### 70.2.2 Power Switching

All dc power required by the CTVC/ITVC, VFM, and PTU is located in the power supply module of the camera. A power ON/OFF enable command, which is a voltage level change to +28 V, is received from the RCU. The circuit is configured to be initially OFF when +28 V main bus is applied. The CCTV camera illuminator (when flown) is powered by the camera heater power source (circuit breaker on panel R14).

### 70.2.3 Automatic Light Control

The CTVCs and ITVCs are normally operated in an Automatic Light Control (ALC) mode. ALC circuits provide automatic feedback to limit the amount of light penetrating the lens and exciting the Charge-Coupled Devices (CCDs) that convert the light energy into an electric signal. Each camera type has the common settings of peak, normal, and average. What differentiates each setting is the area of the video picture in which the amplitude of the video signal from adjacent picture elements (pixels) must exceed a defined limit before the ALC circuit senses a video signal amplitude violation. The purpose of an ALC circuit is to maintain consistent illumination for maintaining picture quality.

The ALC circuit commands motor control logic to drive a stepper motor to open/close the iris to increase/decrease the amount of light to maintain a defined picture quality. The peak setting is most sensitive to area lighting; about 0.01 percent of the picture area (cluster of 36 or more pixels) must change before the ALC circuit senses this change and commands the iris to compensate. Because of its sensitivity to light, this mode provides a dimmer image than the other two settings. The peak mode can also fail to keep up with changing or dynamic lighting conditions. The iris opens and closes frequently, generating an image that gets bright, then dim, then bright again as the iris tries to keep up the ALC circuit commands. The ALC-average mode requires the largest video picture area of the three settings before commanding the iris to adjust the light entering the camera. ALC-average requires 5 percent or more picture area (a cluster of at least 18000 pixels) to change before adjusting the iris. ALC-norm uses a midrange value of 1 percent of the picture area, or 3600 pixels, before adjusting the iris.

The cameras also employ an Auto-Gain Circuit (AGC) to achieve the desired 1-V peak-to-peak RS-170 video signal standard. The AGC can vary between 0 dB and +24 dB of gain.

#### 70.2.4 Gain Settings

Both the CTVC and ITVC provide manual gain and iris settings in case the automatic settings do not provide the desired output. Both types of cameras can provide manually selected gain settings of 0db, +12db, and +24dB gain settings. Whenever a manual gain setting is selected, the ALC circuit is bypassed, enabling the users to fully control the amount of light entering the camera by commanding the iris themselves. The ITVCs also provide an additional gain option that can be used with either manual or ALC mode. The NITE setting provides approximately 16dB more gain at low light levels than the DAY setting, but does this at the expense of Signal/Noise Ratio (SNR). The SNR for DAY at higher light levels is around 56dB, whereas the SNR for NITE mode is, at best, 40dB. NITE setting also amplifies the fixed-pattern noise (inherent to the image intensifier) in addition to the random white noise in the video signal. Generally speaking, reducing the gain in the ITVC provides a less noisy picture.

#### 70.2.5 Pan/Tilt Unit Description

The PTU is a remotely controlled azimuth/elevation mount for CCTV cameras located on the forward and aft bulkheads and on the Remote Manipulator System (RMS) elbow of the orbiter. The power supply cable routing is from bulkhead to PTU and from PTU to TVC. Pan and tilt motions are provided upon TVC command at 1.2° per second (slow command) or 12° per second (fast command) over a total range of 340° (+170° from nominal zero position).

Pan/tilt limit indicators are incorporated into the drive mechanism in the clutch housing area to interrupt electrical power to the motor drives, thereby limiting the motion to a preset panning and tilting range. The limit range is preflight adjustable. In case of failure of the indicators, the unit pans/tilts 3° until it reaches a mechanical hardstop to prevent further motion. The clutch slips to prevent damage to the motor and gear train.

#### 70.2.6 Stepper Motors

The PTU uses two identical stepper drive circuits (pan and tilt), while the CTVC and ITVC use three (focus, zoom, and iris). The iris clock has two rates: 60 Hz is the manual rate and 120 Hz is the auto rate. The PTU has two rates: 6 Hz for slow and 60 Hz for fast. The stepper logic receives the command and generates the two-phase drive for the stepper motors.

#### 70.2.7 CCTV Camera and PTU Heaters

Each CCTV camera and PTU assembly include heater circuits that are thermostatically controlled. Each camera type has different thermostat limits, but the pan/tilt unit heaters activate at -8° C and turn off at 0° C. The VSU issues an alert to the RCU and a flag (short duration pulse) in the downlink video if a camera temperature exceeds 45° C and the VSU is operating in the "sync" mode. The VSU ignores temperature data when commanded to the "async" mode. The 45° C limit originates to the design of the vidicon-based 506/508 series of CCTV cameras. The newer solid state cameras

(CTVC/ITVC) can operate up to 55° with normal performance. The CTVC and ITVC should be powered off prior to reaching 60° C in order to avoid damage to the cameras.

Each camera heater circuit is activated by enabling individual circuit breakers located on panel R14. The same holds true for the pan/tilt unit heater circuit breaker. The camera heater circuit breaker also enables the logic for activating the Light Emitting Diode (LED) illuminators when flown. There are no temperature sensors on the PTU. Each CCTV camera inserts a temperature signal on line 18 of the video that can be read in real time from the onboard monitors as well as the Vertical Interval Data Detector (VIDD) in the MCC.

### **70.2.8 Remote Video Switcher Description**

The Remote Video Switcher (RVS) unit is mounted on the RMS elbow PTU. It selects either the elbow or wrist RMS camera as a video source by using three Delta Pressure/Delta Time (DP/DT) latching relays to switch camera ON, SYNC, and VIDEO signals. Note that, although the +28 V camera power is routed through the RVS, it is not switched in that unit.

The RMS was designed for installation on either the port or starboard side of the orbiter; therefore, a toggle switch is included on the RVS to allow selection of the proper camera location code.

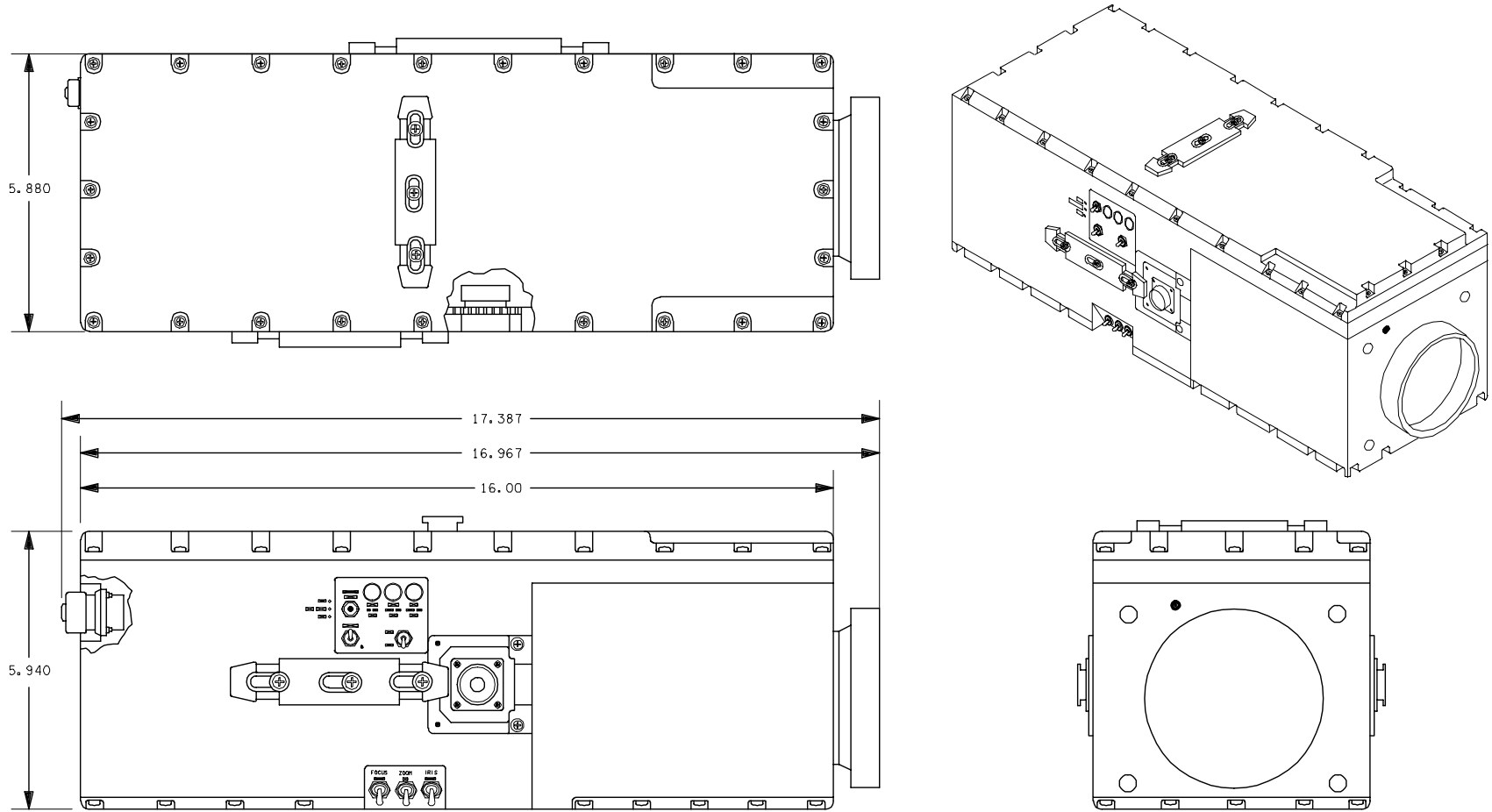
### **70.2.9 External Switches**

Both CTVC and ITVC provide local controls on the right side housing of the cameras. These controls provide access to most functions of the camera. Momentary switches provide control over zoom, focus, and iris settings. A three-position switch is provided to select between ALC, manual gain, and color balance (Day/Nite if ITVC) modes. A pushbutton is provided to toggle through the available settings. A two-position switch is provided to select between shuttle and Space Station command addressing, while the ITVC includes this switch for selecting linear or black stretch gamma. Figure 70-3 shows the location of the local controls.

## **70.3 CCTV SYSTEM OPERATION**

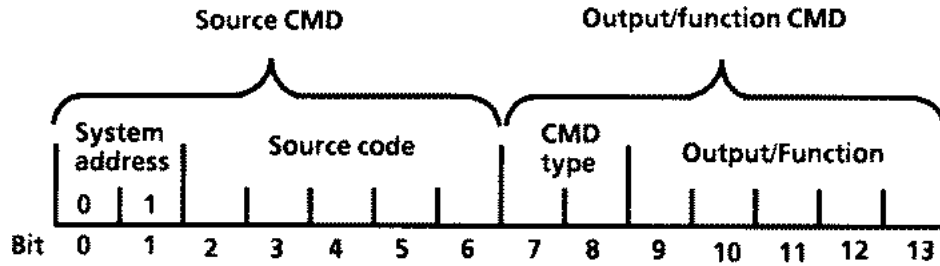
### **70.3.1 Command**

The CCTV command structure is illustrated in Figure 70-4. Commands are received by the RCU from the A7 panel and the PF 2 MDM. The RCU is controlled by an RCA 1802 microprocessor, which is running a cyclic program. RCU processing starts at the beginning of a video field and is completed by the end of the field (Figure 70-5).



186111617.ORT; 1

**Figure 70-4. CTV camera with local controls**



System address - 01 = CCTV

CMD type 01 Camera control command  
(output on sync line)

00 VCU command  
(not output on sync line)

Each command must be preceded by all zeros in bits 7 to 13. Bits 0 to 6 may remain static for many commands.

NOTE: Bits 14 and 15 on the MDM card are assigned to a different (non-comm) system.

18611\*013

Figure 70-5. CCTV command structure

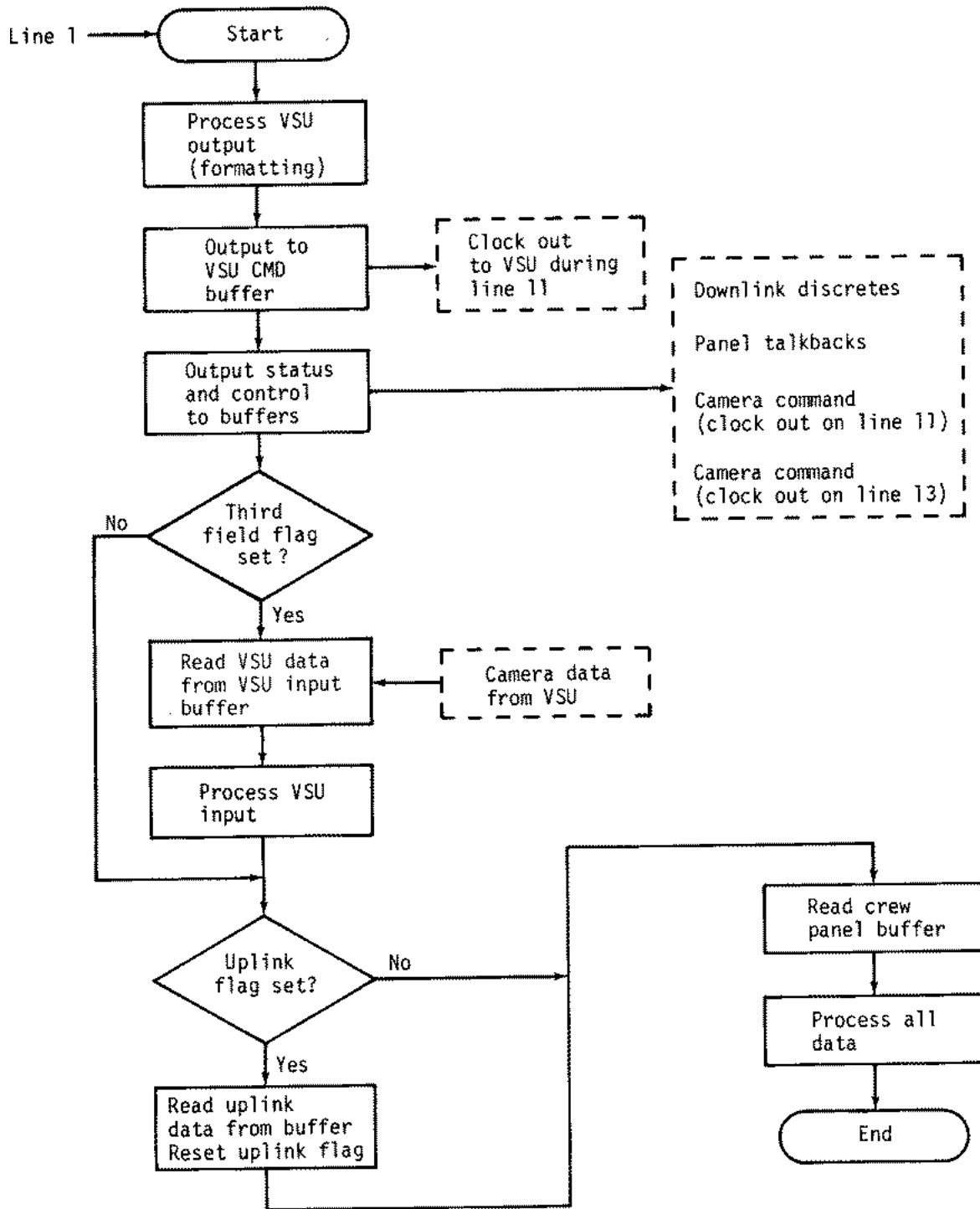


Figure 70-6. RCU flowchart

The crew switches are momentary and are sampled every vertical field. The inputs are processed and commands sent to the cameras via the sync lines or to the VSU via a dedicated line. Commands from the MDM are sampled only once. For a command to be read, all zeros must be present on bits 7 to 13 of the command word (Figure 70-6). When any bits 7 to 13 go high, the RCU waits 200  $\mu$ sec, then loads the input register and sets a flag telling the microprocessor that an uplink command is present. Another command will not be read from the MDM until the microprocessor reads the present command and resets the flag. Thus, commands are processed only once and can be received no faster than the processor cycle, which is 59.99 times per second or every 16 msec. Commands addressed to the VSU are issued to the VSU. Commands addressed to a camera are transmitted to all cameras, and only the camera wired to accept that address will execute the commands (Figure 70-7).

Camera motion commands (PAN, TILT, FOCUS, ZOOM, IRIS) are latched in the RCU and sent every field until any one of the following occurs:

- A stop command is received.
- An uplink command with a different camera address is processed.
- The crew issues a motion command which conflicts with the uplink motion command.
- The uplink commands motion in the opposite direction.
- The TV POWER CONTROL switch is placed in PNL.

Commands are sent to the cameras on lines 11 and 13 of the composite sync. Line 11 is used for crew commands and line 13 for uplink commands; thus, both can operate independently. If the crew and uplink commands conflict, a single command is output on line 11. The formats of the camera command are shown in Figure 70-8, and all commands are listed in Table 70-1. The bit length is two periods of the 2.045-MHz clock (130 times the horizontal line rate). The first 8 bits are a 11110000 sync pattern. The sync pattern is always present even if no command is present. The next 8 bits consist of a camera address with a single bit for odd parity. The final 32 bits are the function code. All camera commanding is done over the sync lines, except camera power on/off, which is commanded by a 28-V discrete signal (one for each camera). Although the camera power on/off commands do not travel via the sync lines to the cameras, RCU sync generator signals are still required for operation of all RCU-generated commands, including camera power (with the exception of flight deck, middeck, and standard switch panel enabled cameras).

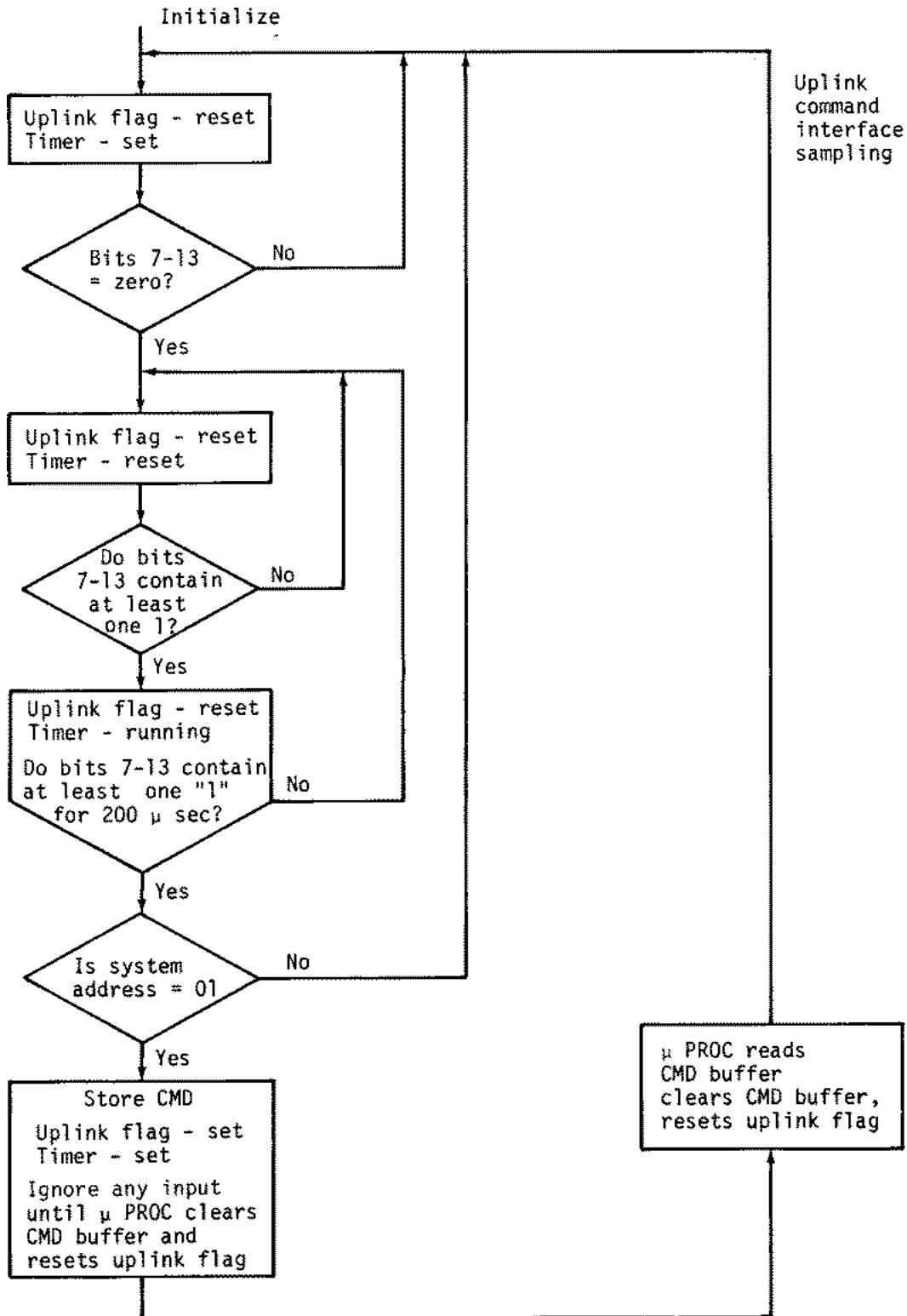


Figure 70-7. Uplink command interface sampling



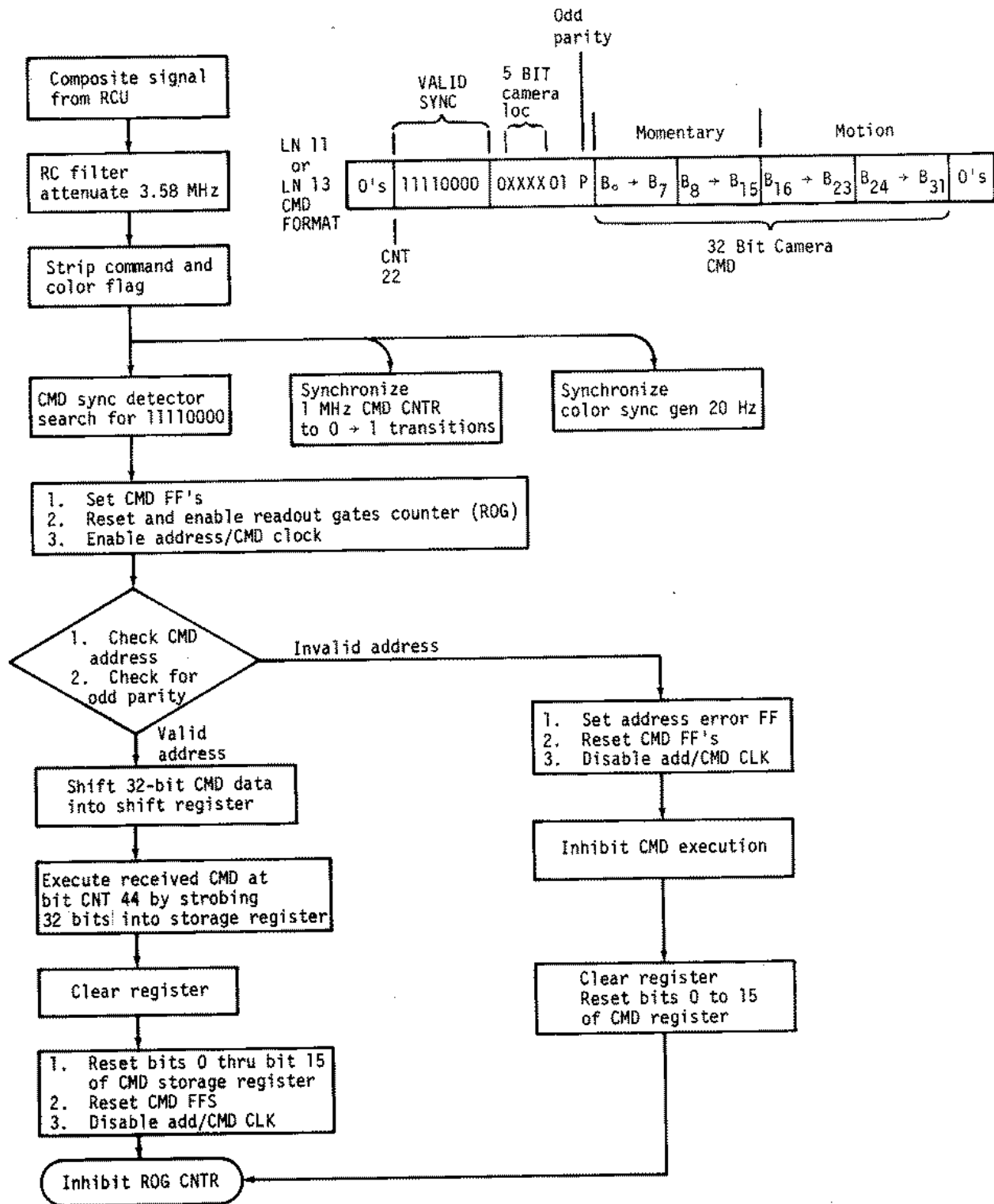


Figure 70-8. Camera command detection/execution

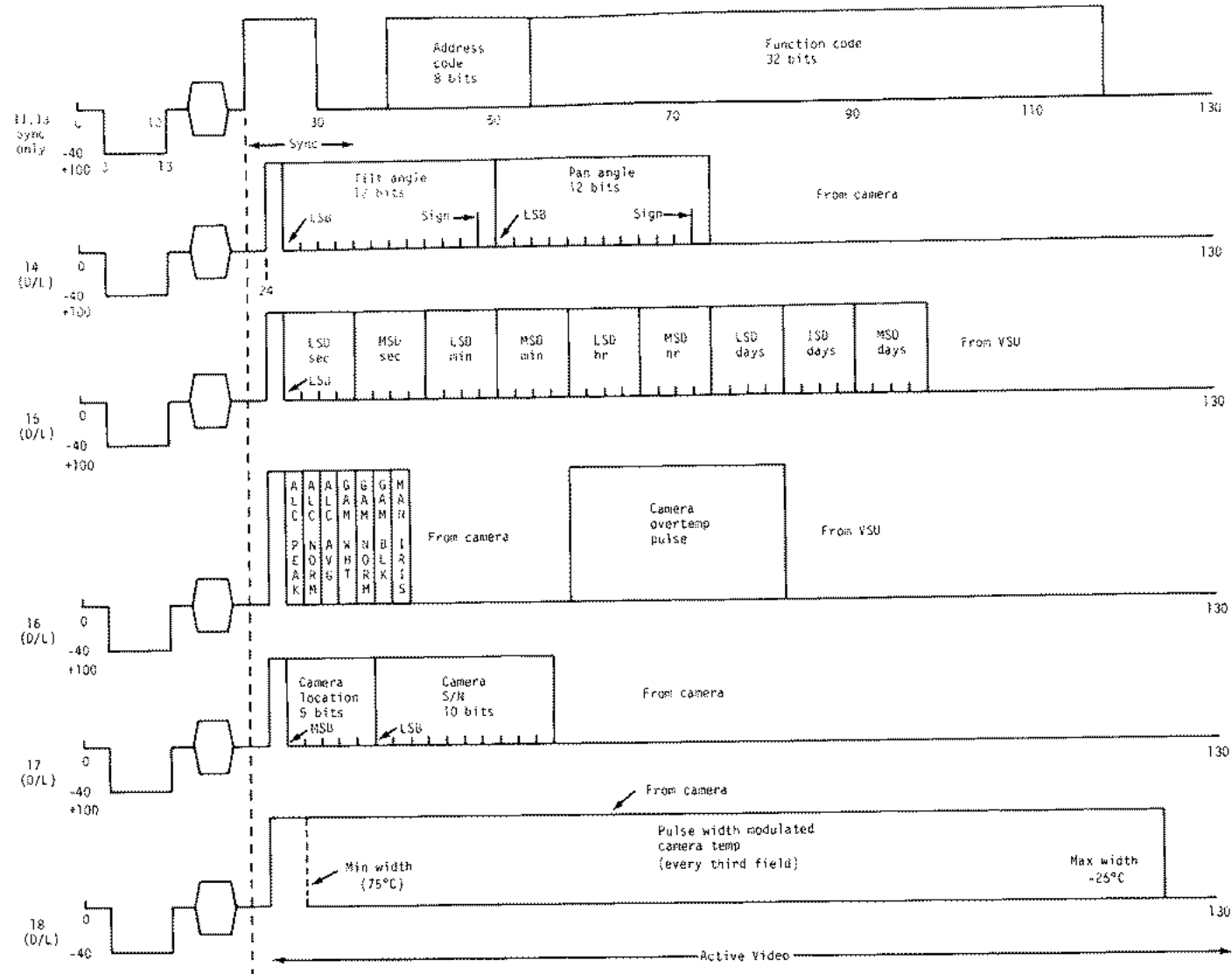


Figure 70-9. Vertical interval data (sheet 1 of 2)

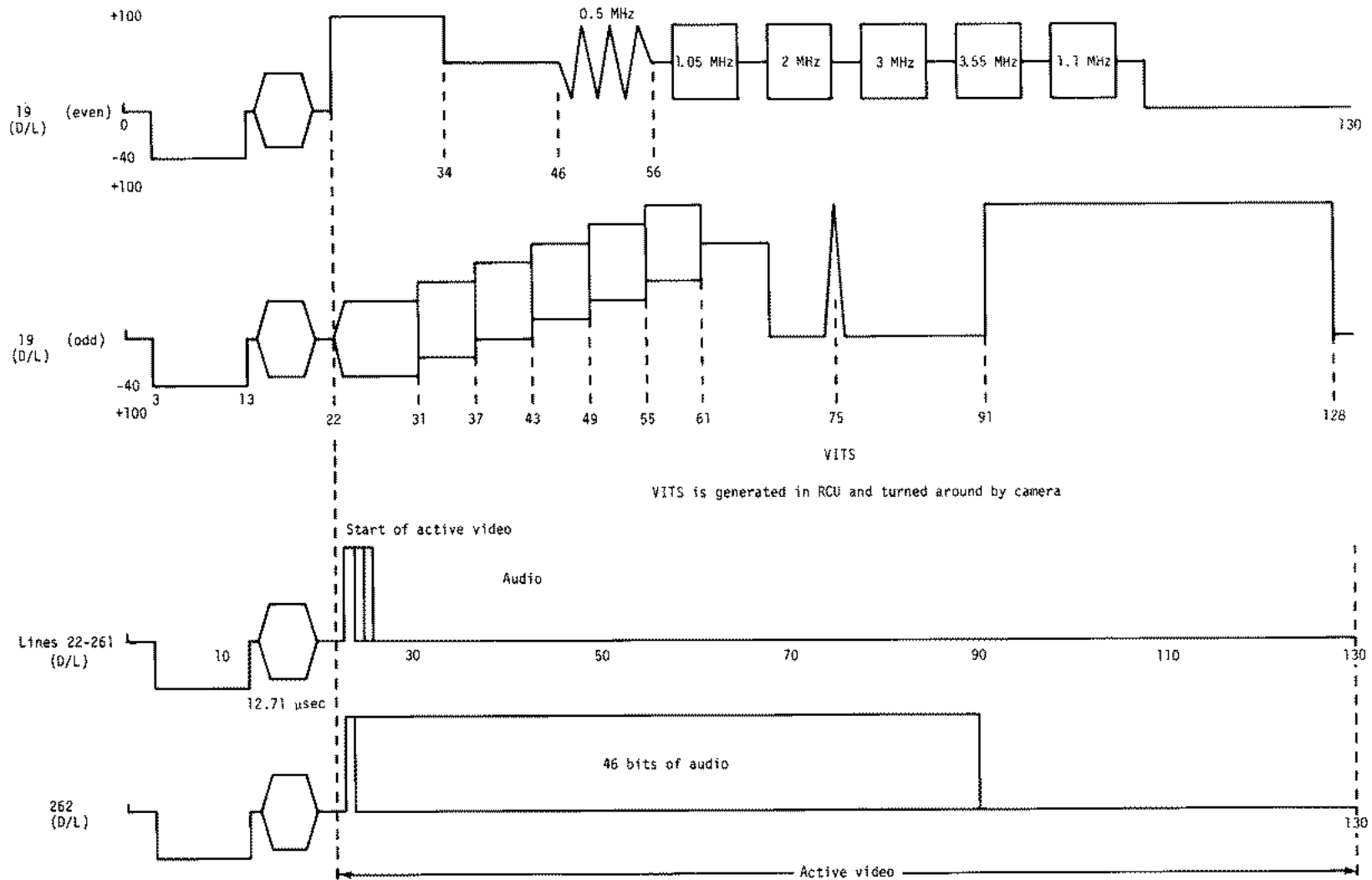


Figure 70-9. Vertical interval data (sheet 2 of 2)

### 70.3.2 Telemetry

The RCU drives 28-V discrete signals for talkbacks on the A7 panel and telemetry to MDM OF 4. The telemetry and talkback parameters, with the exception of camera data and camera overtemp, are from the RCU command logic. The VSU provides camera data and overtemp alert to the RCU. All camera telemetry is interleaved in the video by the camera and can be detected on the ground (VIDD). The VSU samples a camera every third field; thus, data are updated every 39th field (12 video inputs) or every 650 msec. Temperature is limit-sensed by the VSU from a pulse width modulated signal found on line 18 of each camera video. When the temperature of a camera reads 45° C or greater,

- An overtemp flag is inserted on line 16 of the downlink video.
- A camera overtemp discrete is set to OI MDM OF 4. This bit is limit-sensed by the General Purpose Computer (GPC) (SM OPS 2) and results in an SM ALERT, as long as the SM is enabled to annunciate the S76 COMM CAM TEMP message.
- The VSU enables display of temperature on the onboard monitors (white camera data). Normally, camera temperature is not part of the white alphanumeric; it is present only when the temperature of at least one camera exceeds 45° C.

When the overtemp condition goes away, all the above are reset. A false reading could result in the overtemp condition being present for one sampling cycle or 650 msec. SM Fault Detection and Annunciation (FDA) has an N count (filter) of 15 (seconds) before an SM alert is sounded.

The formats of the camera and VSU data inserted in the downlink video are illustrated in Figure 70-8. The camera command on lines 11 and 13 is present only on the sync line (and on the FFTS). All other information is present in the downlinked video.

| Vertical interval line number | Field                                       | Signal information  |
|-------------------------------|---|---|
| 11                            | All   | Camera control commands (crew)  |
| 12                            | All   | Lens data (focus, zoom, iris)   |
| 13                            | All   | Camera control commands (PF 2)  |
| 14                            | All   | Pan/tilt angles   |
| 15                            | All   | GMT insertion by VSU  |
| 16                            | All   | Camera data and overtemp flag (if set)  |
| 17                            | All   | Camera location and serial number   |
| 18                            | CTVC (all)<br>ITVC (2 of 3)<br>508 (1 of 3) | Camera temperature (-25° to +75° C) must be detected on a designated green field for the VSU to monitor lines 14 and 16 |
| 19                            | Odd   | VITS modulated staircase, 2T pulse, bar window  |
| 19                            | Even  | VITS multiburst   |

### 70.3.3 Camera Powerup

When a CTVC or ITVC is initially powered, the cameras default to specific mode settings. Here are the default settings for the CTVC and ITVC:

| Mode                | CTVC      | ITVC      |
|---------------------|-----------|-----------|
| Camera iris         | CLOSED    | CLOSED    |
| ALC                 | OFF       | OFF       |
| Manual gain         | 0 dB      | 0 dB      |
| Color balance       | SUN       | N/A       |
| Day/Nite            | N/A       | NITE      |
| Shutter             | OFF       | N/A       |
| Aperture correction | N/A       | OFF       |
| Color bars          | OFF       | N/A       |
| Gamma               | BLACK STR | BLACK STR |

Since the iris is closed, no picture is received. Sending an ALC command sequence places the camera in automatic iris mode, and the iris opens to the proper setting. For a payload bay camera, plans are to use ALC AVG on the initial setting. When a camera is powered down, there is a 4-second delay before power is actually removed to allow the iris to fully close (this is done automatically). This is important because the Sun can damage the camera even when the camera is turned off. In the case of a cabin camera and a centerline camera, the iris does not automatically close if the camera is turned off via crew switches on panels O19/M058F or standard switch panel. Since these cameras are in the cabin, it normally causes no problem (centerline camera is looking through a window up -Z axis). The crew is instructed to close the iris of the centerline camera prior to powerdown. However, if a cabin camera is to be used for Extravehicular Activity (EVA), the iris should be fully closed before the camera is taken EVA. Generally speaking, the crew uses camcorders in the cabin instead of CTVC or other CCTV cameras.

### 70.3.4 Ground Camera Selection

Ground commanding is accomplished via a 14-bit parallel word set on MDM PF 2. The 14-bit command word is partitioned as shown in Figure 70-6. As explained earlier, the RCU responds to a command after a reset/set mask is sent to bits 7 to 13. Commands affecting bits 0 to 6 do not cause any RCU response. Commands are split into two basic categories, source commands (affecting bits 0 to 6) and output/function commands (affecting bits 7 to 13). In effect, a ground operator builds a command onboard using this feature; the source is loaded and an output/function causes the RCU to execute the command. A third type of command, called a standalone command, does not require a source command because all required information is contained in the standalone command. The source, output/function, and standalone commands are listed in Table 70-1. A source command may be followed by as many output/function

commands as required. Since bit 1 must be one for the proper system address, if the set mask of a source command was not received, the RCU does not respond to any output/function command. If the reset mask was not received, the RCU responds to the OR'd combination of two source commands. There is no way to confirm that a source command was received except by sending an output/function command and looking for the correct response.

The PAN/TILT FAST/SLOW commands (4276/4277) control the pan/tilt rate for the currently selected source (camera). Whenever the source is changed and any output/function command is received, the pan/tilt rate reverts to FAST. When panning or tilting in SLOW and it becomes desirable to change cameras with pan or tilt in SLOW, the PAN/TILT SLOW command must precede the PAN or TILT command.

The following series of commands assigns the forward bay camera to the downlink and zoom it:

- 4232 TV FWD BAY CAM-SEL
- 4249 TV DOWNLINK
- 4264 TV ZOOM OUT
- 4255 TV ZOOM STOP

Since the ground has to issue a single RTC, all motion commands (FOCUS, IRIS, ZOOM, PAN, TILT) start when the command is received and continue to move until a STOP command is received, a command with a different camera address is processed, a conflict occurs, or the TV POWER CONTR switch is placed in PNL. End of travel does not cancel the motion command. No damage results, but a STOP should be sent as soon as possible.

A split-screen MUX is programmed in the same fashion as a single source. Note that the left or right sides of a MUX are outputs, and the MUX itself is an input. The following command sequence assigns the forward and aft bay cameras to the left and right sides of MUX 1 and downlinks them (both cameras must be on):

- 4232 TV FWD BAY CAM - SEL
- 4245 TV MUX 1 LEFT
- 4234 TV AFT BAY CAM - SEL
- 4246 TV MUX 1 RIGHT
- 4240 TV MUX 1 - SEL
- 4249 TV DOWNLINK

### 70.3.5 Onboard Camera Selection

The CCTV system is operated onboard from the switches on panel A7 (Figure 70-9), and switches on the cameras themselves. A few switches on panel A7 require some explanation. The TV POWER CONTROL switch does not operate the same as the other GCIL control switches. The only GCIL function in the CCTV is the power on/off.



**Figure 70-10. PNL A7 Camera controls**

In the PANEL position, the control switch activates panel drivers, thus giving the crew control over power on/off. The PANEL configuration of the control switch also disables the RCU from accepting commands from the PF2 MDM. Therefore, in the PANEL position, only the crew has control over any aspect of the CCTV. When the switch is placed in the COMMAND position, the GCIL command drivers become active, giving the ground control over CCTV power on/off. In addition, the RCU is enabled to receive commands from the MDM. Therefore, in the COMMAND position, the ground has

control over power on/off, but both ground and crew can command the rest of the CCTV system.

The TV SYNC switch has two positions, NORMAL and REVERSE. In NORMAL, sync generator A operates when the VCU is powered from MNA, and sync generator B operates when the VCU is powered from MNB. In the REVERSE position, sync generators A and B are reversed with regard to main bus ties (sync gen A with MNB, etc.). The crew can thus easily and quickly change sync generators. The ground does not have this command and must change power buses to change sync generators.

The functioning of the VIDEO OUTPUT, VIDEO INPUT, and CAMERA COMMAND switches is explained in the following sections. The VIDEO OUTPUT, VIDEO INPUT, and the ALC and GAMMA switches are PBIs that illuminate to display certain status information during operation. The function of each is explained, and then an operational example is given.

#### **70.3.5.1 Video Output**

When a VIDEO OUTPUT PBI is depressed, it illuminates and all other VIDEO OUTPUT PBIs are extinguished. Only one VIDEO OUTPUT PBI can be illuminated at a time. Also, the VIDEO INPUT PBI corresponding to the video input connected to the selected video output illuminates. If no input was previously connected to the selected video output, no VIDEO INPUT PBI illuminates. If the previous video input was a CCTV camera, the ALC and GAMMA PBIs illuminate to indicate the current modes of the camera ALC and GAMMA circuits. Depressing a VIDEO OUTPUT PBI does not change the VSU configuration or issue any camera command. It only reads out status and prepares the system for the next command.

#### **70.3.5.2 Video Input**

When a VIDEO INPUT PBI is depressed it illuminates, and a command is issued to the VSU to assign the selected input to the output represented by the illuminated VIDEO OUTPUT PBI. Any other VIDEO INPUT PBI that was illuminated goes out. Also, if the selected input is CTVC or ITVC, the ALC and GAMMA PBIs indicate the current camera ALC and GAMMA modes (assuming RCU is in "sync" mode). The only time depressing a VIDEO INPUT PBI does not send a VSU command is when no VIDEO OUTPUT PBI is illuminated. This occurs only after VCU powerup initialization.

#### **70.3.5.3 Camera Command**

The CAMERA COMMAND PBIs and toggle switches issue commands to the video input (camera) represented by the illuminated VIDEO INPUT PBI. The ALC and GAMMA PBIs allow selection of the appropriate mode and function as talkbacks. The ALC PBIs indicate the ALC mode and manual/auto iris mode. In the auto iris mode (iris controlled by ALC circuits), the ALC mode is indicated by the single PBI that is illuminated. In the manual iris mode (iris not controlled by ALC circuits, but set by command), the ALC mode is indicated by the PBI that is not illuminated (two will be on, one off). The auto



iris mode is entered when an ALC command is sent. The manual iris mode is entered when an iris command (open or close) is sent.

The typical command sequence is VIDEO OUTPUT, VIDEO INPUT, CAMERA COMMAND. As an example, to assign the forward bay camera to monitor 1 and zoom it out:

- A7 VIDEO OUTPUT - MON 1
- VIDEO INPUT - FWD BAY
- CAMR CMD ZOOM - OUT

The MUXs are programmed in the same fashion as single cameras. Each side of the MUX is an output, and the MUX as a whole is an input to the VCU. The following is an example with the forward bay camera and the aft bay camera assigned to the left and right sides of MUX 1 and displayed on monitor 1:

- VIDEO OUTPUT - MON 1
- VIDEO INPUT - MUX 1
- VIDEO OUTPUT - MUX 1 L
- VIDEO INPUT - FWD BAY
- VIDEO OUTPUT - MUX 1 R
- VIDEO INPUT - AFT BAY

Note that since the MUX was assigned to the monitor first, each camera could be viewed and camera commands sent to it as it was assigned to the MUX. (This works because the monitor gets sync from the RCU.) If the monitor sync switch is in INTERNAL, the problem described in 70.3.8 (loss of sync) occurs.

### 70.3.6 Conflict Resolution Between Ground and Onboard Commanding

When in command mode, onboard camera motion commands are acted on only when the camera motion switches change. Onboard commands have the same priority as ground commands. The VCU responds to the last command change, either from the ground or onboard.

| <u>Action</u>  | <u>Response</u>   |
|--|-------------------|
| Crewmember presses and holds the PAN switch in left position | Camera pans left  |
| Ground sends PAN RIGHT                                       | Camera pans right |
| Crewmember releases the PAN switch                           | Camera stops      |

It is changes that are sensed, not the actual switch positions. Camera functions subject to these limits are PAN, TILT, ZOOM, FOCUS, and IRIS.

In the above case, the pan or tilt rate could have been different. Another conflict can arise when the ground commands pan at one rate and the onboard commands tilt at the other rate (to the same camera). In this case, both PAN and TILT will be at the rate selected by the last command received. For instance, if the crewmember was panning at the slow rate when an uplink command to TILT fast was received for the same camera, both PAN and TILT would run in fast. If the crewmember released his pan, the PAN would stop and the TILT would continue at the fast rate. If the crewmember pushed the onboard PAN switch again, the PAN and TILT would both run at the slow rate.

When command changes from both ground and onboard are sampled together (in commands in the same vertical field interval), the onboard overrides the ground.

Note: Since the RCU responds to switch changes when in the CMD mode (POWER CONTR switch in CMD), the PAN/TILT rate switch is ineffective until a camera motion switch is changed; i.e., if a PAN is in progress and the rate switch is moved, no rate change occurs until the PAN is stopped and restarted or some other PAN/TILT motion is started.

Nonsimultaneous commands (occurring during different video fields) are executed independently.

### **70.3.7 Voice Interleaver and Asynchronous Mode (Ground Only)**

The standalone commands control the operation of the voice interleaver and the asynchronous video mode. These commands operate in a straightforward fashion. Whenever an asynchronous source is being downlinked (i.e., a VTR dump), the asynchronous mode must be entered, and the voice interleaver must be turned off.

Note that there are no crew switches for these functions. However, if the voice interleaver is enabled, the crew can select ICOM A and/or ICOM B via two switches located on Panel A1R, labeled PL BAY OUTLETS.

#### **70.3.7.1 Asynchronous Mode**

The VSU samples camera video synchronously. Therefore, a nonsynchronous source may result in false readings. In addition, the VSU inserts a Greenwich Mean Time (GMT) time code on line 15 of all video inputs; if a camera is sensed, an overtemp flag is inserted on line 16 of the downlink. This is also done synchronously, so an asynchronous source would have the time code and/or overtemp flag (and interleaved audio, if that is turned on) inserted in the wrong places. A more serious problem is that a false temperature reading (from the asynchronous source) could result in a false SM ALERT. To prevent this, the asynchronous mode (async mode) is entered via MDM command. In the async mode, the VSU is inhibited from all camera sampling except pan/tilt angles. This is a hardware inhibit, and the VSU microprocessor does not know it

is inhibited; so it reads zeros for all parameters. Also, GMT insertion is inhibited. The audio interleaver is not inhibited. This causes the ALC and GAMMA telemetry on panel A7 and on downlink to freeze, possibly in a random configuration. No camera temperatures are sensed; so an overtemp alert does not occur although the overtemp flag might be latched on the async command that was issued when the VSU detected a camera temperature over 45°.

#### **70.3.7.2 Onboard Effects of Async Mode**

Since the async mode inhibits VSU sampling of camera temperature, the VSU limit-sensing of camera temperature is disabled, the SM alert for camera overtemp is disabled, and camera temperatures are not available to the crew. Pan and tilt angles are sensed by the monitor; so the green crew alphanumeric display (on the TV monitors) reads correctly. ALC and GAMMA settings are not sensed by the VSU, so the ALC and GAMMA PBIs on panel A7 freeze (possibly in a random state). The crew can still command ALC and GAMMA and the camera does respond, but the talkbacks do not work. Note that this applies to all cameras, not just the asynchronous source.

#### **70.3.7.3 Ground Effects of Async Mode**

The only effect on ground operations is that the OI telemetry parameters for ALC and GAMMA are static (possibly in a random state), and the GMT is not inserted in the video. If a real-time source is being downlinked, the GMT readout on the TV monitor is static. If a VTR is being dumped, the TV monitor display shows the data of the recorded source; i.e., the GMT when the recording was made. Thus, when the VTR is downlinked in the async mode, our operations are not impacted.

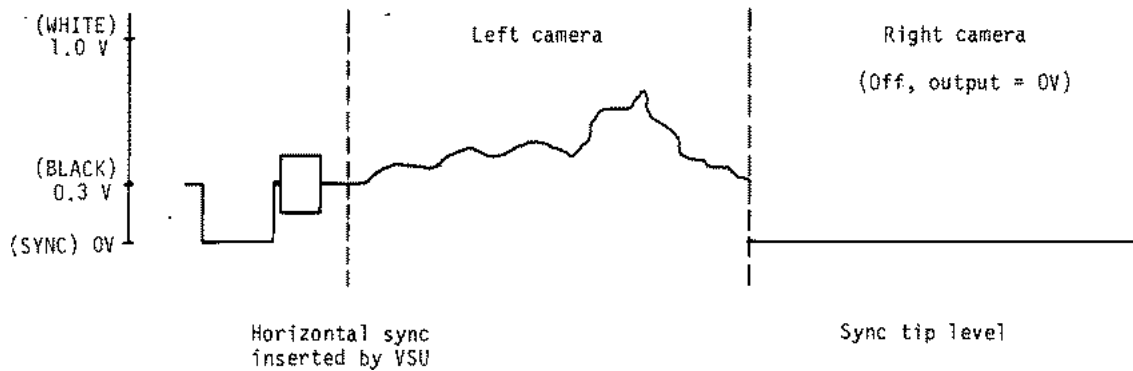
#### **70.3.7.4 Audio Interleaving**

The VSU has the capability to interleave a single delta modulated voice channel in the downlink video. The channel can be either ICOM A, ICOM B, or both mixed together. The audio is routed from the payload bay intercom channels. The format of the bits is shown in Figure 70-10. Lines 22 to 261 contain a leading “one” for sync and 2 data bits. Line 262 contains 46 bits. The voice is delta modulated in the VSU at a 31.6-kHz rate (2x horizontal line rate). Note that the interleaved audio goes only to the downlink channel. The interleaved audio was used on some Spacelab flights; however, on non-Spacelab flights it is not used because of lip sync problems when retrieving the video for playback by the ground. Since the voice bits cannot be removed from the video, any downlink video with voice interleaver enabled no longer conforms to the broadcast NTSC standard. The Federal Communications Commission (FCC) prefers that NASA not use this feature unless critical to science operations.

#### **70.3.7.5 Limit on Split-Screen Operations**

Split-screen operation with a nonoperating (off or failed) or nonexistent camera causes loss of video synchronization on the ground. This loss propagates throughout the video system (and to commercial broadcasters if they are broadcasting our video). It occurs because a nonoperating or nonexistent camera outputs zero volts, sync tip level

(Figure 70-11). When commanding a split screen, make sure that both cameras are on before the split screen is downlinked.



**Figure 70-11. Output of the MUX when one source is inactive**

### 70.3.8 Suggested Techniques for TV Ops

Note: Get permission from the crew before using any cameras. This is especially important for cabin and payload bay cameras when the crew is doing some sort of payload bay ops. The OSVS requires calibration of the cameras. Since the calibration takes time, INCO should not command cameras during these tasks.

#### A. Payload bay ops

1. Lighting is the big problem. The CTVC is very tolerant of bright light, but the ITVC is not. Try minimizing the gain with the ITVC (ALC Norm, Gamma Linear). The best technique is to pan and tilt to get the bright spots out of the view.
2. When trying to see detail with a small bright object against a dark background (like space), the best approach is to minimize the gain (reduce the bloom). Go to GAMMA linear and use the manual gain and iris to get good contrast on the object. Remember not to leave the camera this way unattended. Both CTVCs and ITVCs are susceptible to solar damage when using a manual gain setting.
3. Zoom out before panning or tilting. Otherwise, it is easy to get lost in the payload bay.
4. Use pan tilt in the slow rate. The fast rate is usually too fast for operation from the ground because of the delay in Tracking and Data Relay Satellite (TDRS) transmission.

Use fast only when you have a long way to go and not much time to get there.

5. Use the zoom selectively. When shooting Public Affairs Office (PAO) shots, start wide, zoom in on an area of interest, then go back out wide. Try to make

smooth transitions from one zoom setting to another. Do not “step” the zoom setting. Get a good idea of the shot wanted and go after it.

B. Inside the cabin TV ops

1. Lighting is still the big item. Try to get bright lights out of view by using the zoom.
2. Coordinate with the crew when to command to asynchronous mode. The crew may have to remove power from the camcorder to avoid a false overtemp flag.

### 70.3.9 Telemetry

The OI telemetry is listed in Table 70-3. There are some additional data presented to the crew.

A set of alphanumerics can be displayed on either of the onboard monitors. Electronically generated crosshairs are also available. These graphics can be generated by the VSU (white) or by the monitor (green). The white alphanumerics show camera location, pan and tilt angles and, if any camera temperature is 45° C or greater as detected by the VSU, the temperature of the displayed camera also appears.

The MCC also has a unit, called the VIDD, that decodes data from the video. All data interleaved in the downlink video are viewable from an overlay generated by the VIDD.

**Table 70-3. Telemetry**

| <b>MSID</b> | <b>Description</b>      | <b>Function</b>  |
|-------------|-------------------------|--|
| V74X0830E   | FLT DECK CAM SELECTED   | RCU discretes indicating which camera is selected for downlink   |
| X0798E      | MIDDECK CAM SELECTED    |  |
| X0799E      | CABIN CAM 3 SELECTED    |  |
| X0825E      | FWD BAY CAM SELECTED    |  |
| X0827E      | AFT BAY CAM SELECTED    |  |
| X0826E      | KEEL - EVA CAM SELECTED |  |
| X0829E      | PORT RMS CAM SELECTED   | Cannot differentiate elbow and wrist   |
| X0828E      | STBD RMS CAM SELECTED   |  |
| x0795E      | PAYLOAD 1 SELECTED      |  |
| X0796E      | PAYLOAD 2 SELECTED      |  |
| X0797E      | PAYLOAD 3 SELECTED      |  |
| x0847E      | CAMERA OVERTEMP         | RCU discrete, indicates VSU detected a camera temperature at least 45° C. RCU discretes. If the VSU detects camera temperature on the "green" field, these discretes are enabled. These discretes provide insight into the currently selected setting of the camera. Use VIDD to ascertain all camera settings of downlinked camera. |
| X0843E      | ALC PEAK                |  |
| X0844E      | ALC NORM                |  |
| X0845E      | ALC AVG                 |  |
| X0846E      | GAM WHITE               |  |
| X0848E      | GAM BLACK               |  |
|             |                         |  |
| X4880E      | VCU PWR MNA             | GCIL discretes, indicating which bus is powering the VCU. Mutually exclusive.  |
| X4881E      | VCU PWR MNB             |  |
| X0782E      | VCU SYNC GEN            | RCU discrete. 1 = sync gen A   |
| S0790E      | SYNC NORM               | Switch scan. Position of onboard SYNCH switch.   |
| S0791E      | SYNC REVERSE            |  |
| S0793E      | GCIL                    | Switch scan. 1 = CMD on GCIL mode switch.  |
| S0781E      | DOWNLINK                | Switch scan downlink enable/inhibit switch. 1 = inhibit.   |



## 70.5 CCTV OPERATIONAL IDIOSYNCRASIES

The following is a list of idiosyncrasies found in the CCTV system. There are probably others, but these are the ones we know about.

- A. The cue light on the CTVC for cabin-located cameras is turned on by the RCU when that camera is selected for downlink either alone or as part of a MUX. However, the camera does not have to be turned on for the cue light to work (it does have to be plugged in). In order to get cue light on the flight deck or middeck camera, the downlink switch must be in the enable position.
- B. In order to power on a camera via command, an input/output select function must be sent first. The input command puts the camera address on MDM lines to RCU so that the RCU knows which camera to power on. The poweron talkbacks for the payload bay cameras are driven when the RCU commands the camera ON. It does not prove the camera came on or even if the camera is really there. It only indicates that the RCU set the camera on discrete high. Thus, one could (by the talkbacks anyway) turn on a nonexistent camera.
- C. All telemetry, panel talkbacks, and camera ON command discrettes are driven by latching relays in the RCU. When the RCU is turned off, power is removed so that all the discrettes go low, but the relays stay where they are. When power is reapplied to the RCU, the microprocessor runs an initialization routine and resets all the relays. However, this process takes 8 to 10 seconds; so all telemetry points, panel talkbacks, and camera ON commands go back to their last state for 8 to 10 seconds. This causes no damage, but it is good practice to avoid having cameras turn on briefly by turning the cameras off before turning the VCU off. The VCU does not respond to any commands (MDM or A7) during the initialization period. Please note that if a camera comes on during initialization, wait 4 more seconds before turning the camera on (see paragraph E). To be safe, wait 15 seconds from VCU powerup to the first command.
- D. The pan/tilt readouts are not true pan/tilt unit telemetry. They are maintained by the camera and indicate where the camera "thinks" that it is pointed. If the PTU hangs up, fails, or is nonexistent, the camera does not know and indicates pan/tilt angles as if it were really panning or tilting. The pan/tilt counter is 11 bits; so the angles could go as high as  $409.4^\circ$ , then reset to zero and continue.
- E. A camera should not be powered up within 4 seconds of being powered down. This recommendation is a result of the auto iris close function. When a camera is turned off, it remains powered for 4 seconds while the iris closes. If it turned on before 4 seconds, the iris close command can be latched in the camera, and the iris has a continuous close command that cannot be overridden by an iris open command or the ALC circuits. To recover, the camera must be turned off (wait 4 seconds) and then turned back on. Also, switching from main bus A to main bus B or vice versa must have at least a 5-second pause to ensure that the operation between the GCIL and the RCU functions properly. There has been a history of



some RCUs not operating properly when a GCIL command was transmitted. The RCU hangs up because Poweron Reset (POR) is not performed. If this occurs, the RCU should be powered OFF and ON to clear.

- F. Asynchronous video sources can cause unusual flickering of the ALC/gamma talkbacks as well as video processing mode changes in the color monitors. These events are caused by GMT insertion on the wrong line by the VSU (sync mode) or if the video source is replaying CCTV cameras from the payload bay.
- G. There are two signals that can be inserted onto downlink video by the VSU. When in the sync mode, the VSU inserts GMT on line 15. If the VSU senses a temperature violation in sync mode, an overtemp flag is inserted on line 16 of the downlink video sent to the S-band FM and Ku-band systems. If the VSU is commanded to async mode when the overtemp flag is set, the overtemp flag remains latched until the VSU is commanded to sync mode and the temperature violation is no longer detected. INCO can “freeze” the visible overtemp flag in an asynchronous video source (effectively making the flag disappear from the video) by commanding the VSU from sync mode to async mode when the scrolling overtemp flag reaches the right edge of the screen. The best way to avoid this situation is to coordinate with the crew prior to the asynchronous downlink. All asynchronous sources to the VSU should be powered off, the async command uplinked, and then the asynchronous sources activated.

**70.6 CAMERA LENS CAPABILITIES**

Table 70-4 gives CCTV lenses field-of-view ranges.

**Table 70-4. CCTV lenses field-of-view ranges**

**(a) Monochrome lens assembly (decommissioned)**

| Parameter |            | Horizontal, deg | Vertical, deg | Diagonal, deg |
|-----------|------------|-----------------|---------------|---------------|
| Zoom out  | Focus far  | 40.9            | 30.6          | 51.5          |
|           | Focus near | 33.0            | 24.7          | 41.25         |
| Zoom in   | Focus far  | 6.6             | 4.9           | 8.25          |
|           | Focus near | 5.8             | 4.3           | 7.2           |

**(b) Color television camera**

| Parameter | Horizontal, deg | Vertical, deg | Diagonal, deg |
|-----------|-----------------|---------------|---------------|
| Zoom out  | 72.0            | 54.0          | 90.0          |
| Zoom in   | 10.6            | 7.98          | 13.3          |

Note: CTVC specifications are based on diagonal values, ± 5 percent (CTVC Critical Design Review, Viewgraph Package no.2, 1989, p. 3-005)

**(c) Intensified television camera**

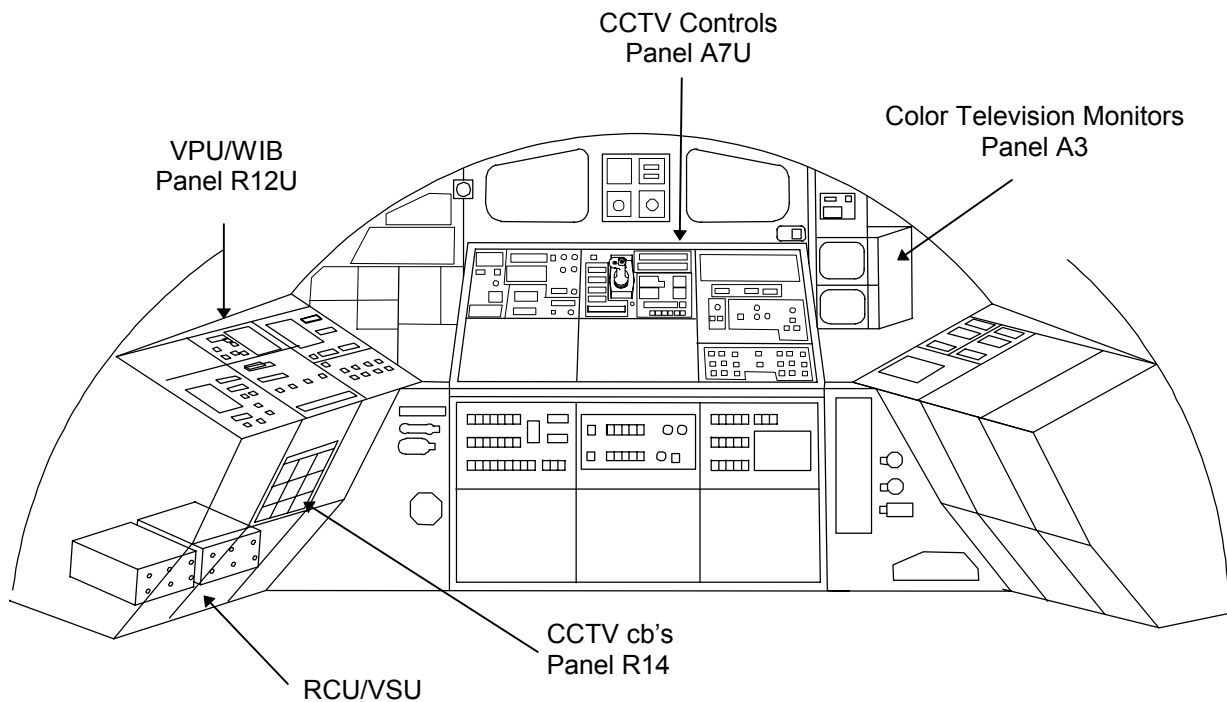
| Parameter | Horizontal, deg | Vertical, deg | Diagonal, deg |
|-----------|-----------------|---------------|---------------|
| Zoom out  | 54.7            | 41.0          | 68.4          |
| Zoom in   | 4.0             | 3.0           | 5.0           |

Note: ITVC specifications are based on horizontal values (ITVC Critical Design Review, Viewgraph Package, 1992, p. 50)

| Lens    | Focal length (zoom), mm | Zoom ratio | Focus distance, ft | F-stop (iris) |
|---------|-------------------------|------------|--------------------|---------------|
| 508/MLA | 18 to 108               | 6:1        | 2.5 to ∞           | f1.6 to f16   |
| CTVC    | 5.5 to 47               | 8.5:1      | 1.0 to ∞           | f1.7 to f16   |
| ITVC    | 8.5 to 127.5            | 15:1       | 3.28 to ∞          | f1.7 to f16   |

**Table 70-5. General mechanical specifications**

| Item                  | Size, in.             | Weight, lb |
|-----------------------|-----------------------|------------|
| Color TV camera       | 17.39 by 5.88 by 5.94 | 18.1       |
| Intensified TV camera | 16.87 by 5.88 by 5.94 | 17.2       |
| Viewfinder monitor    | 8 by 4.3 by 3.6       | 4.0        |
| Pan/tilt unit         | 16 by 11 by 11        | 9.0        |
| Video switching unit  | 13 by 10.5 by 7.8     | 39.0       |
| Remote control unit   | 10 by 10 by 7.7       | 39.0       |
| TV monitor            | 12.5 by 10 by 7       | 21.0       |



**Figure 70-12. CCTV component locations (cabin)**

## SECTION 71 - SOLID STATE COLOR TELEVISION CAMERA (CTVC)

### CONTENTS

| Section |  | Page  |
|---------|--|-------|
| 71.1    | BACKGROUND .....   | 71-1  |
| 71.2    | PHYSICAL AND MECHANICAL DESCRIPTION .....                          | 71-1  |
| 71.3    | ELECTRICAL DESCRIPTION.....  | 71-1  |
| 71.3.1  | Camera Location Code .....   | 71-2  |
| 71.3.2  | Power Switching.....   | 71-2  |
| 71.3.3  | Power Consumption .....  | 71-2  |
| 71.3.4  | Video Detection .....  | 71-7  |
| 71.3.5  | Automatic Gain/Light Control .....                                 | 71-7  |
| 71.3.6  | Command/Telemetry Processor.....                                   | 71-9  |
| 71.3.7  | INCO Uplink Commands.....  | 71-11 |
| 71.4    | POWER ON RESET .....   | 71-27 |
| 71.5    | SYNCHRONIZATION.....   | 71-27 |
| 71.6    | RGB VIDEO PROCESSING .....   | 71-29 |
| 71.6.1  | NTSC Color Encoder.....  | 71-29 |
| 71.6.2  | Differences in the ITVC Telemetry .....                            | 71-30 |
| 71.6.3  | Vertical Interval Data Detector (VIDD) Display Interpretation..... | 71-31 |
| 71.7    | CAMERA ILLUMINATORS .....  | 71-36 |
| 71.7.1  | General Description .....  | 71-36 |
| 71.7.2  | Camera LEDs.....   | 71-37 |
| 71.7.3  | Power to the Illuminator Assemblies .....                          | 71-37 |
| 71.7.4  | Control to the Illuminator Assemblies .....                        | 71-38 |

## TABLES

| Table |                            | Page  |
|-------|----------------------------|-------|
| 71-1  | Power Consumption.....     | 71-2  |
| 71-2  | MCC Command Breakdown..... | 71-11 |
| 71-3  | ITVC Differences.....      | 71-30 |

## FIGURES

| Figure |   |       |
|--------|---|-------|
| 71-1   | Camera configuration.....                                 | 71-3  |
| 71-2   | Camera electronics internal configuration.....            | 71-4  |
| 71-3   | CTVC simplified block diagram.....                        | 71-5  |
| 71-4   | CVTC LVPS block diagram.....                              | 71-6  |
| 71-5   | ALC/AGC block diagram.....                                | 71-8  |
| 71-6   | Local commanding.....                                     | 71-9  |
| 71-7   | Telemetry generation.....                                 | 71-10 |
| 71-8   | Composite sync/command line format (lines 11 and 13)..... | 71-13 |
| 71-9   | Panel A7 switches/labeling with CTVC decal.....           | 71-14 |
| 71-10  | External switch orientation.....                          | 71-16 |
| 71-11  | Line 12 lens data format.....                             | 71-18 |
| 71-12  | Line 14 pan/tilt data format.....                         | 71-19 |
| 71-13  | Line 16 camera command status data format.....            | 71-20 |
| 71-14  | Line 17 camera ID data format.....                        | 71-21 |
| 71-15  | Line 18 camera temperature.....                           | 71-22 |
| 71-16  | Camera Lens.....  | 71-24 |
| 71-17  | Shutter servo.....  | 71-25 |
| 71-18  | SMPTE color bar pattern.....                              | 71-26 |
| 71-19  | Synchronization.....                                      | 71-28 |
| 71-20  | NTSC/green video output.....                              | 71-29 |
| 71-21  | Camera lens capability.....                               | 71-30 |
| 71-22  | Illuminator Subassemblies.....                            | 71-37 |
| 71-23  | PTU to Camera Cable.....                                  | 71-38 |
| 71-24  | Illuminator Internal Views.....                           | 71-39 |
| 71-25  | PTU to CTVC Cable Schematic.....                          | 71-41 |

## SECTION 71 SOLID STATE COLOR TELEVISION CAMERA (CTVC)

### 71.1 BACKGROUND

The color television camera (CTVC) features solid state sensor technology, increased zoom range, no image retention, no Sun blooming problem, low maintenance plug-in modules, low power consumption, longer lifetime, and generates true NTSC color.

### 71.2 PHYSICAL AND MECHANICAL DESCRIPTION

The CTVC overall size is 16.0 inches long, 5.88 inches wide, and 5.94 inches high. The estimated weight is 18.7 pounds. Power consumption is approximately 34 watts average. The CTVC assembly consists of a lens assembly and an electronics assembly. The two subassemblies are separable enclosures that are secured and connected inside the camera housing. The lens assembly contains a 2/3-inch format wide-angle zoom lens and lens drive motors and electronics in an aluminum housing. Three motors on pivoting mounts engage the lens function ring gears on the barrel of the lens. Stepper motors fitted with integral gear head assemblies, together with the spur gear drive to the lens, magnify the output torque and provide the necessary rates for the iris, zoom, and focus functions. Three single turns, high resolution potentiometers are mounted similarly to the stepper motors and provide discrete position information for iris, zoom, and focus functions. Switches and LED's for all camera and lens functions are located on the side of the camera. Figures 71-1 and 71-2 provide external and internal detail of the camera assembly.

The prism/CCD assembly is part of the lens housing and maintains optical alignment. The prism/CCD assembly consists of a three-piece prism; several planar glass elements, which are use for filtering, polarizing, and path extension; and three CCD imagers mounted on an adapter plate. The three CCD imagers are permanently positioned and attached to the prism using a Fujinon lens. The photo-sensitive area of the green CCD is positioned so that the center pixel coincides with the optical axis of the lens and prism system. The blue and red CCD's are registered with respect to the green CCD so that the center pixels coincide. The lens, prism, and CCD are aligned to place the center of an optical target less than +30 microns at the image plane over the full zoom range of the lens. The prism assembly allows for enclosure of a two-blade, "bow-tie" shutter wheel to provide optical blanking during vertical image transfer. The shutter wheel is 3.0 inches in diameter and is made of 0.02-inch thick spring steel. A light shield is provided to prevent dust contamination and limit electrical crosstalk.

### 71.3 ELECTRICAL DESCRIPTION

Figure 71-3 provides a block diagram depicting signal flow through the CTVC.

### 71.3.1 Camera Location Code

The CTVC has been modified to support either space station or orbiter missions. On the right side of the camera a switch toggles between the 5-bit orbiter location or the 7-bit space station location.

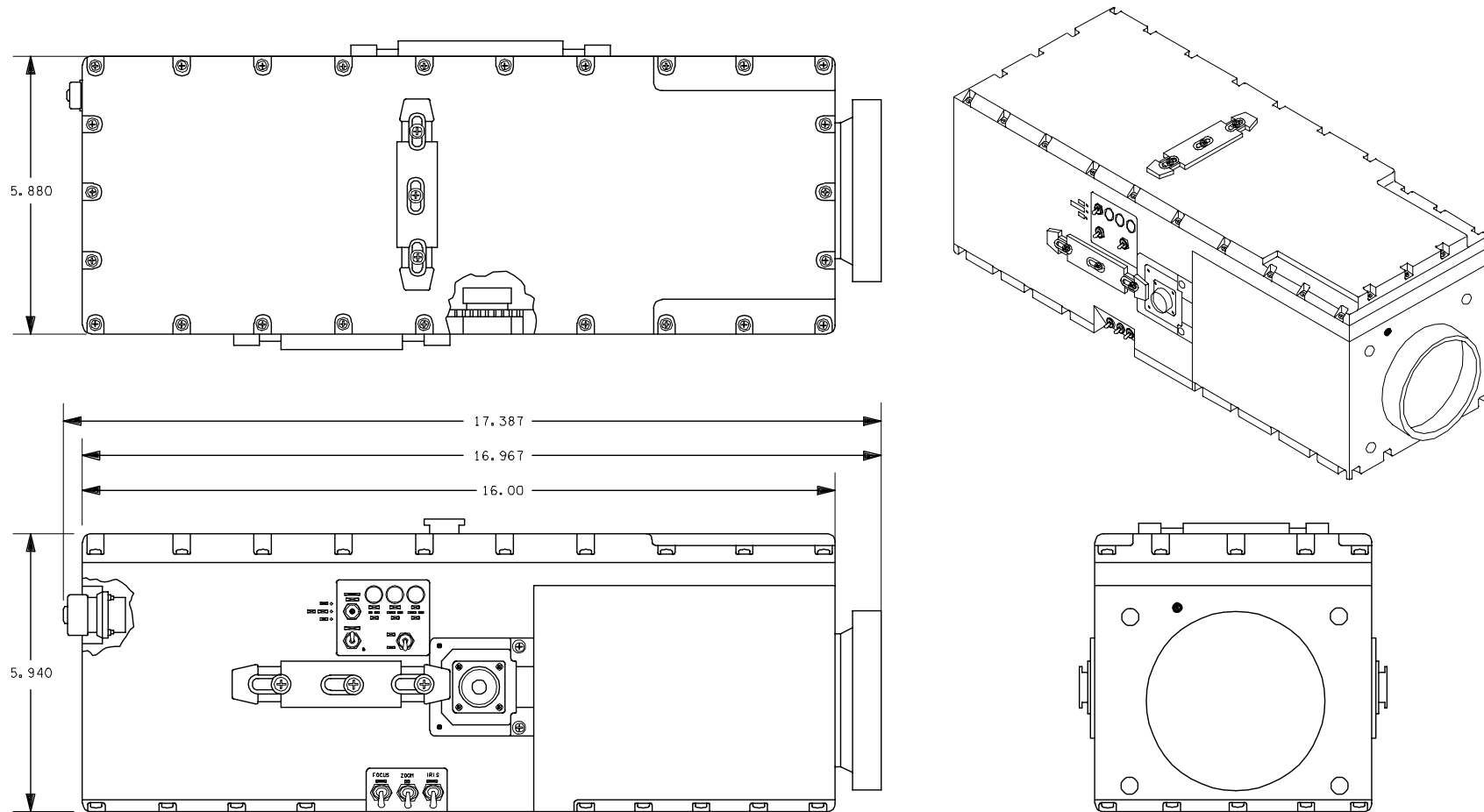
### 71.3.2 Power Switching

The CTVC power supply is managed by a power controller that receives +28 VDC power from the Orbiter. It is triggered by the ON/OFF command to switch power to the LVPS, pan/tilt unit (PTU), and viewfinder module (VFM). The ON/OFF control circuitry activates the iris close timer, iris close pulse, pulse width modulator shutdown, and relay drivers. The circuitry receives the outputs of the protection circuit comparators for fault action. The iris close timer provides a 3-second delay to LVPS turnoff to allow the iris mechanism to close. An OFF command causes the iris pulse signal to be sent and starts a 3-second delay after which the supply turns off. Fault-induced shutdowns are not delayed. Sensing circuits for under- and overvoltage conditions are combined with the iris close timer output to form a common trip signal for the power controller. See Figure 71-4 for further detail.

### 71.3.3 Power Consumption

**Table 71-1. Power Consumption**

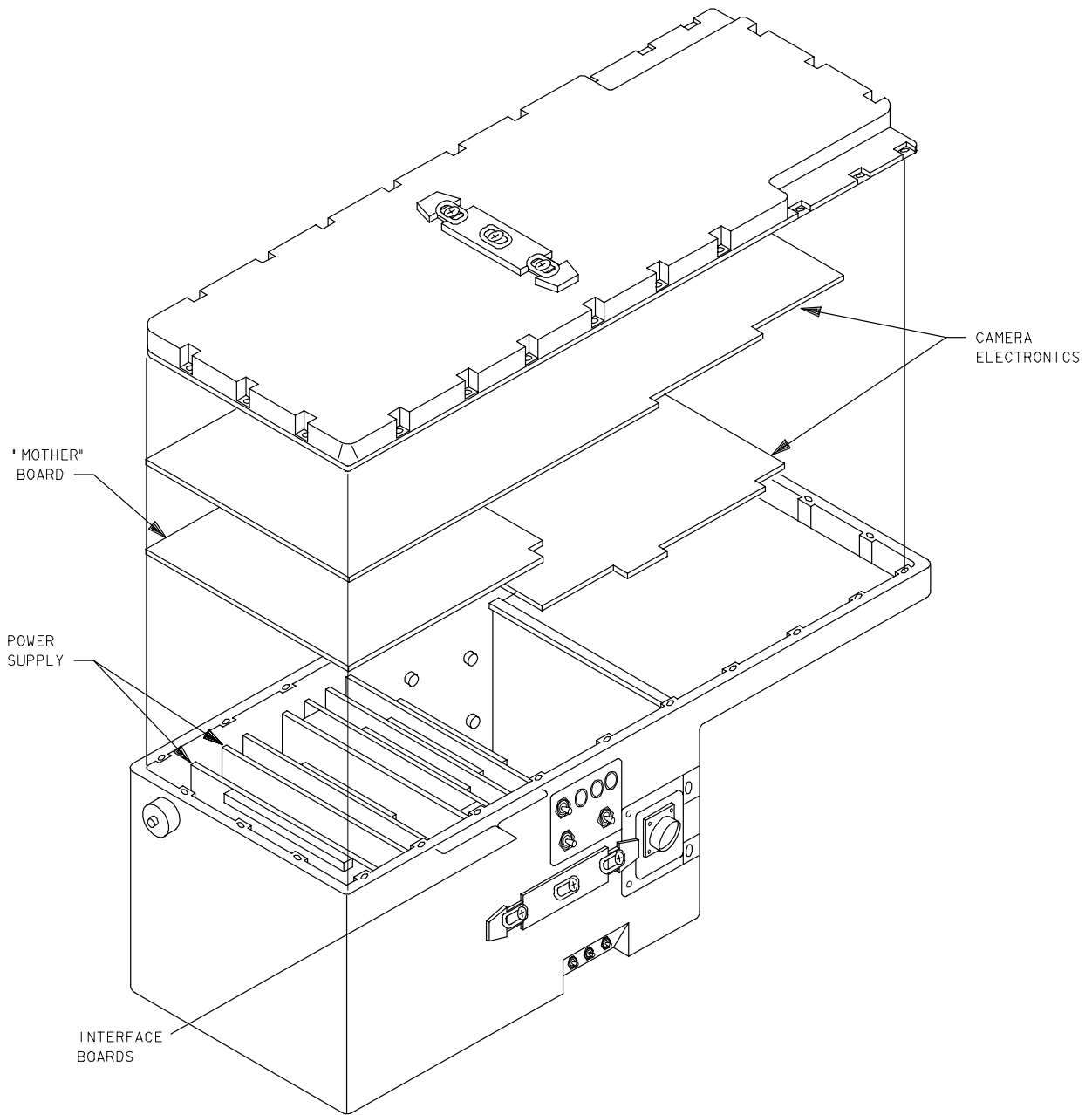
| <b>Equipment</b>        | <b>Power (W)</b> | <b>Equipment</b> | <b>Power (W)</b> |
|-------------------------|------------------|------------------|------------------|
| RCU/VSU                 | 44.8             | AVIU w/ V-10     | 17               |
| Color Monitor           | 56               | AVIU w/ PD100A   | 10.8             |
| Pan/Tilt Unit           | 2                | AVIU w/ Mini-cam | 6.5              |
| Pan/Tilt Unit Htr       | 12.5             | AVIU             | 2.6              |
| CTVC                    | 25.5             | V-10             | 11.5             |
| CTVC Heaters            | 32.8             | DTV (ascent)     | 30.8             |
| ITVC                    | 12.7             | DTV (orbit)      | 67.88            |
| ITVC Heaters            | 21.5             | DTV (crew sleep) | 52.2             |
| Videospection Cam       | 8.6              | DTV (entry)      | 37.64            |
| Videospection Htr       | 8                | SSV              | 11.52            |
| 180 LED Illuminator OFF | 1.5              | TVCU             | 4.9              |
| 180 LED Illuminator ON  | 21.9             | VPU              | 2.7              |
| 180 LED Illuminator Htr | 11.7             | WVS Transponders | 120              |
| 40 LED Illuminator OFF  | 1.2              | WVS Antenna Htr  | 350              |
| 40 LED Illuminator ON   | 5.9              | WVS Antenna      | 35               |
| 40 LED Illuminator Htr  | 11.7             | PD100A Camcorder | 6.5              |



186111617.ORT; 1

**Figure 71-1. Camera configuration**





186111618. ISO 1

**Figure 71-2. Camera electronics internal configuration**

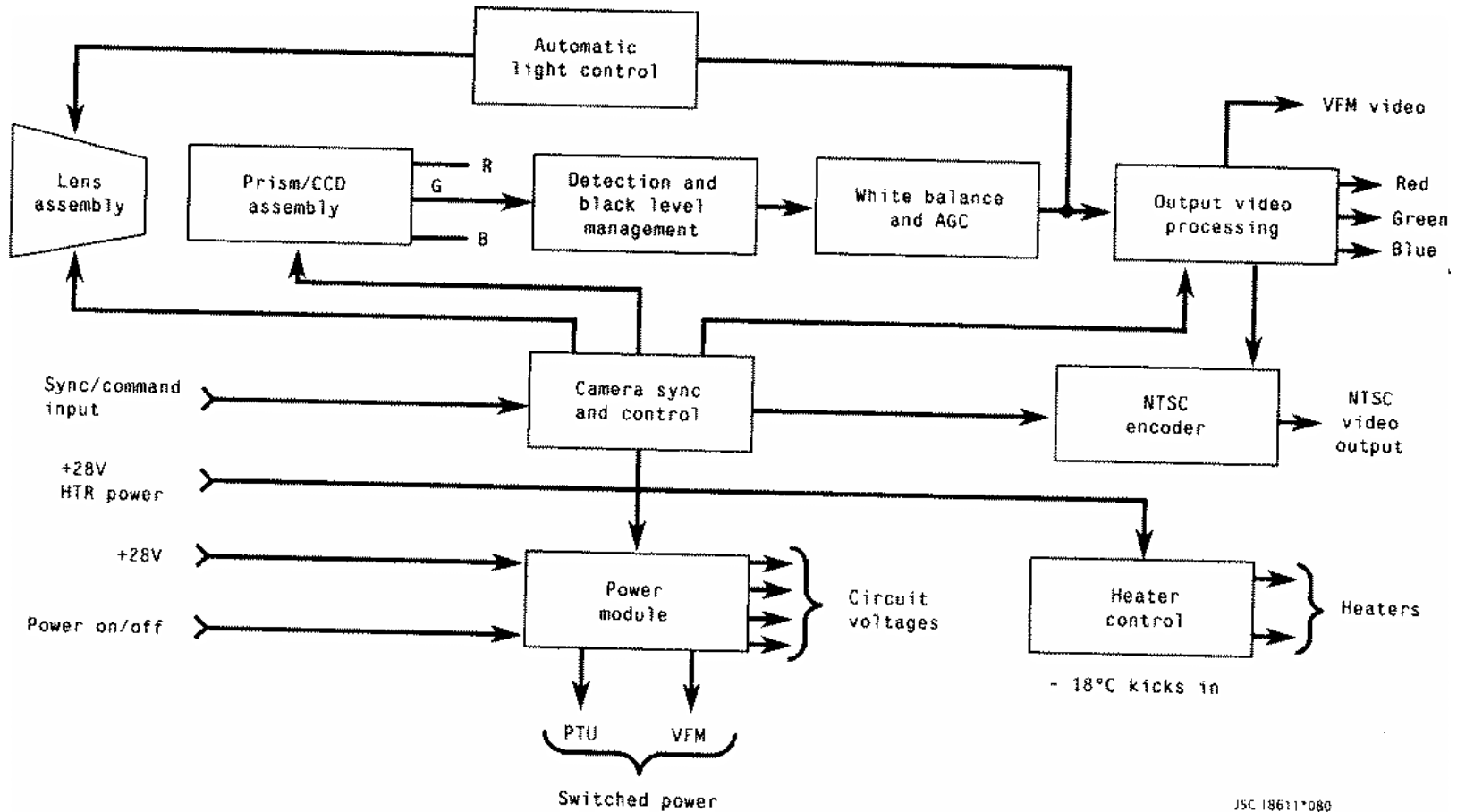
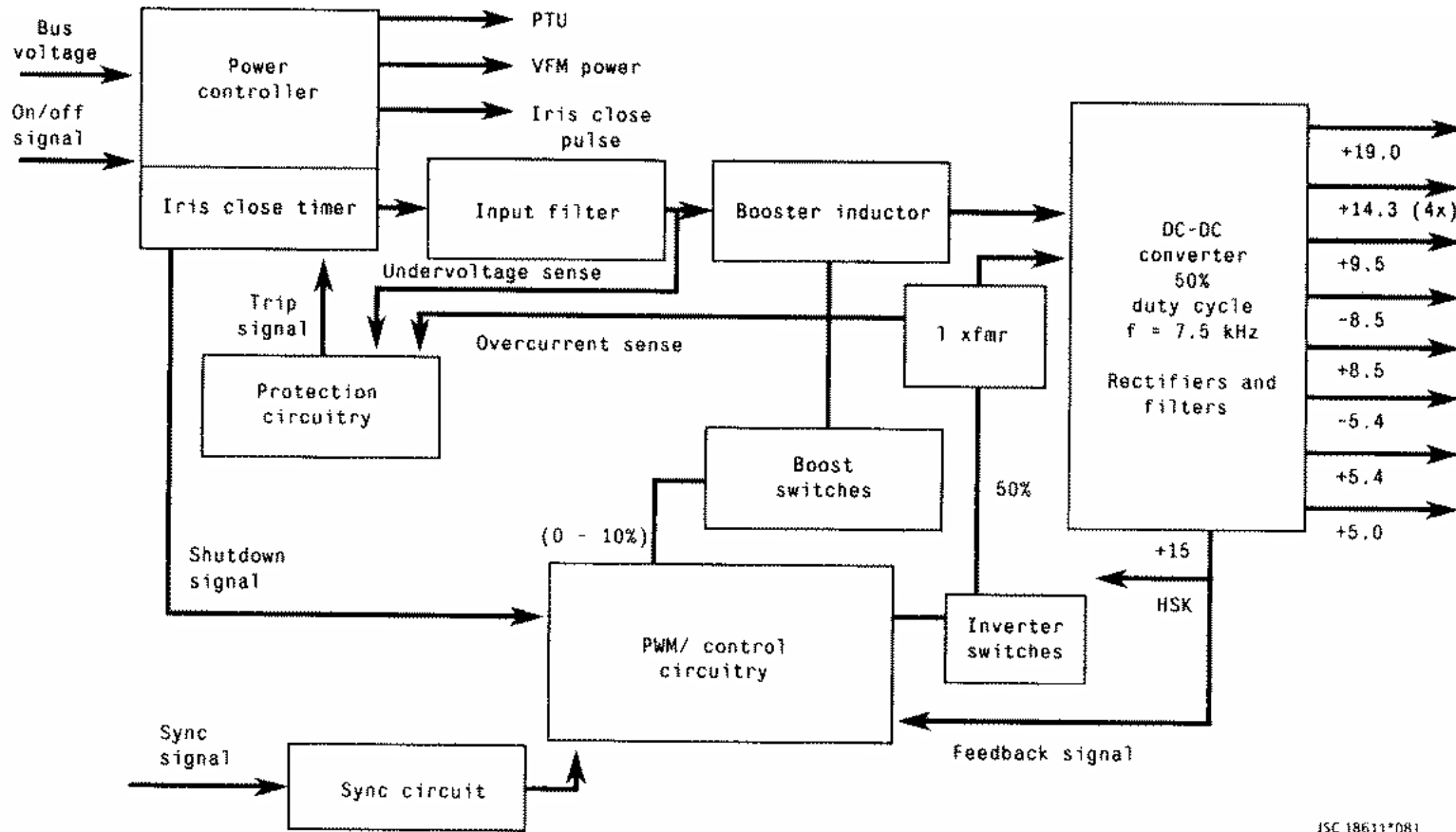


Figure 71-3. CTVC simplified block diagram



JSC 18611\*081

Figure 71-4. CVTC LVPS block diagram

#### 71.3.4 Video Detection

Photoelectronically and thermally generated electrons are integrated by three (green, red, blue) CCD's. The pixel video detector outputs a frame transfer that can be thought of as an amplitude modulated carrier. The thermal electrons known as dark current are corrected and integrated to establish a black level reference. The video is then driven by process blanking to remove unwanted signals present due to imager clocking. After blanking, the video is amplified and corrected for black level shading. A feedback clamp looped around the video amplifier maintains black level reference. The signal is then sent to the automatic gain control circuitry.

#### 71.3.5 Automatic Gain/Light Control

The color balance amplifiers (CBA) and automatic light control/automatic gain control (ALC/AGC) circuitry accept red, green, and blue video outputs from the video detection and provide color-balanced video of fixed amplitude to the video processing circuitry. The CTVC provides three preset color balance settings which are manually selected by uplink or off the side panel. The red and blue channels are provided with adjustment potentiometers which are used to compensate for variations in the response of the prism, CCD imagers, and video preprocessing circuitry. The potentiometers are set during camera test and then staked to prevent subsequent adjustment. The settings are daylight, fluorescent, and tungsten. The ALC/AGC circuit maintains the video signal at a predetermined level by controlling the lens aperture and the gain of an AGC amplifier. Automatic feedback control in conjunction with three detector settings (5 percent, 1 percent, and peak) maintains the correct video output level. The area detector circuit, which is part of the control loop, keeps a commanded fraction of the picture raster at a predetermined signal level. On the side of the camera the functions for ALC, gain, and balance are selectable via switches. The FUNCTION SELECT switch is a three-position toggle switch. Its purpose is to enable the SELECT switch to command (in a sequencing fashion) either the ALC, MANUAL GAIN, or BALANCE functions, and at the same time assign the three associated indicators to display either ALC, MANUAL GAIN, or BALANCE status. (If the FUNCTION SELECT switch is in the ALC position, the ALC status will be indicated by an illuminated PEAK, NORM, or AVG lamp. The ALC status may be changed by momentarily depressing the SELECT switch.) SELECT is a two-position momentary switch which is spring loaded to the UP position. It works in conjunction with the FUNCTION SELECT switch to command the ALC, MANUAL GAIN, and BALANCE functions. See Figure 71-5.

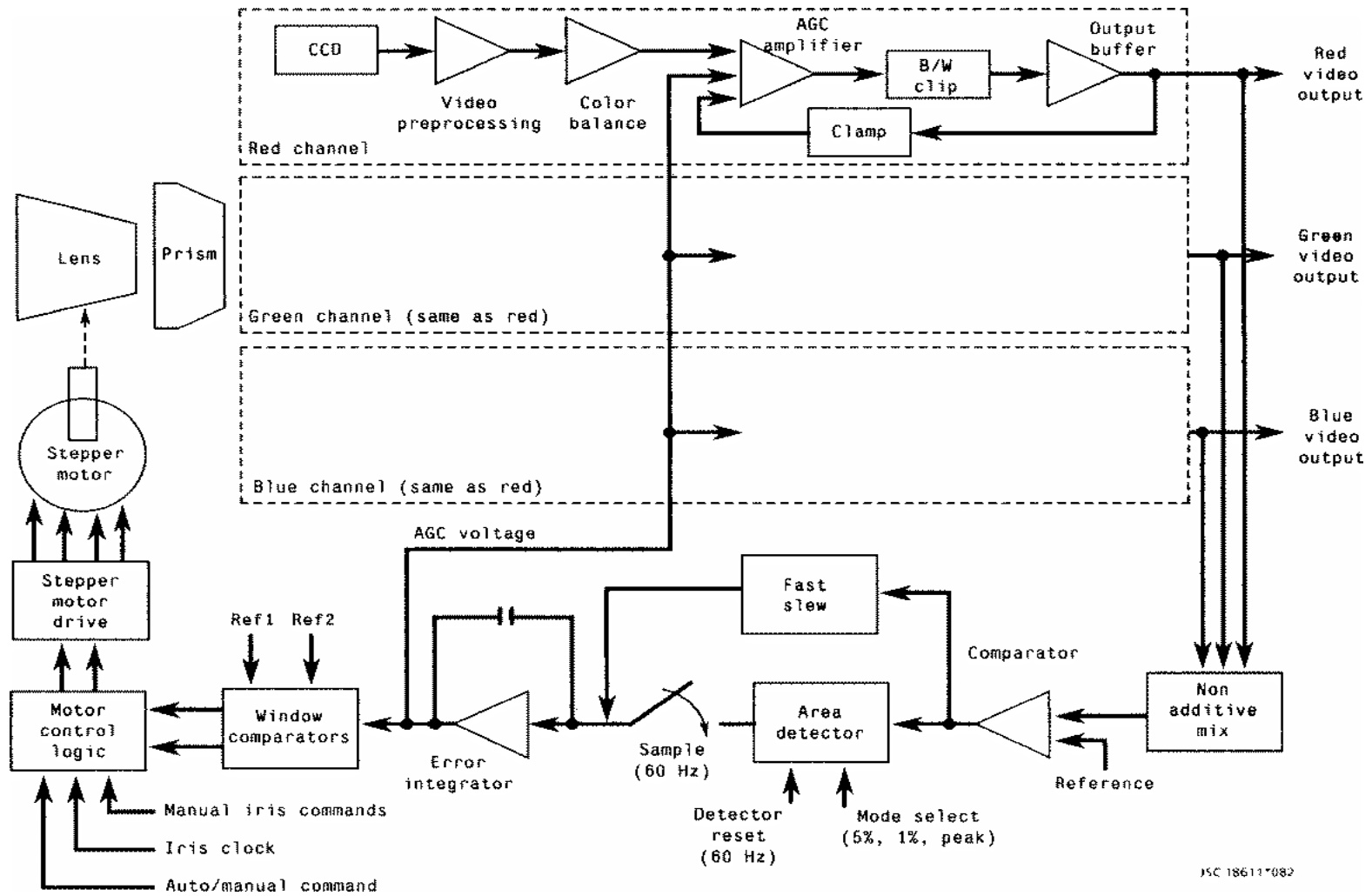


Figure 71-5. ALC/AGC block diagram

### 71.3.6 Command/Telemetry Processor

Functions performed by the command/telemetry (CMD/TLM) processor include local remote command reception, command decoding, encoding of camera status of insertion during the vertical interval and display by the local light emitting diodes (LED's), generation of pan/tilt control commands and position data, generation of motor control signals for the lens assembly, and generation of the SMPTE color bar pattern. Also provided are specialized timing signals required by other circuits in the camera that include sample and hold signals for the ALC/AGC control, modified blanking signals for video processing, triggers to enable the temperature pulse width modulator and lens data analog to digital converter, and a half field gate used for dark current sampling.

- |  |
|--|
| <p>14 COMMAND FUNCTIONS AVAILABLE</p> <ul style="list-style-type: none"><li>• FOCUS NEAR/FAR CONTROL</li><li>• ZOOM IN/OUT CONTROL</li><li>• IRIS OPEN/CLOSE CONTROL</li><li>• GAMMA LINEAR/BLACK STRETCH SELECT</li><li>• COLOR BALANCE - SUN SELECT</li><li>• COLOR BALANCE - CAB SELECT</li><li>• COLOR BALANCE - BAY SELECT</li><li>• ALC PEAK MODE SELECT</li><li>• ALC NORM MODE SELECT</li><li>• ALC AVG MODE SELECT</li><li>• MAN GAIN - 0 dB SELECT</li><li>• MAN GAIN - 12 dB SELECT</li><li>• MAN GAIN - 24 dB SELECT</li></ul> |
|--|

**Figure 71-6. Local commanding**

Generates 2-Mhz Vertical Interval Data (VID) clock  
Generates control signals required for insertion of downlink VID on the following lines:

- Line 12 - Lens data (zoom, focus, iris)
- Line 14 - Pan/tilt data
  - Generates pan/tilt angle magnitude and sign data
- Line 16 - Gamma/camera mode data
  - In addition to existing 7 bits of A7 control panel status, generates 13 bits of camera status unique to the CTVC. Encodes existing status to provide proper control of the A7 panel status indicators
- Line 17 - Camera ID data (serial number, location)
  - Location code data may be increased from 5 bits to 7 bits for use with future systems
- Line 18 - Camera temperature data
  - Generates control signals for temperature pulse width modulator
- Line 19 - Vertical Interval Test Signal (VITS)
  - Generates control signals for insertion of VITS data

**Figure 71-7. Telemetry generation**

#### **71.3.6.1 Command Reception and Decoding**

Remote control of gamma, gain, ALC mode, color bar mode, color balance, shutter mode, and lens assembly functions are generated by the CCTV system RCU and distributed to each camera location. Commands may appear on lines 11 and 13 of both fields and consist of an 8-bit sync word, an 8-bit address field, and a 32-bit command field. The leading sync bit of the command is detected and used to synchronize the command receiver clock with the clock of the RCU. The 8 sync bits are then shifted into the sync shift register and compared to the hard-wired sync code. If the sync word is OK, the command bit counter is enabled and the address word is shifted into the address shift register (counts 0-7). The command address is compared with the destination camera address. If the correct address has been received, the command bit counter continues counting. During counts 7-39, the input command clock is enabled and the entire command word is shifted into the input command shift register. At count 44, the command is latched into the command decoder. Finally, at count 48, the command receiver is reset and waits for the next sync word. If, during counts 0-7, an address error is found, the system will reset. The command decoder decodes and executes all gamma, gain, ALC mode, color bar mode, color balance, and shutter mode commands encoded in the 32-bit uplink command. Motor control commands in the uplink are decoded by the pan command decoder, tilt command decoder, zoom motor controller, focus motor controller, and iris motor controller. The command decoder also decodes commands controlled by the local camera switch panel. These commands are GAIN, ALC mode, color balance, and shutter mode. All of the above logic for the CMD/TLM processor is accomplished using 10 erasable programmable logic devices

(EPLD's). The EPLD encodes the command status data for insertion on line 16 of the VID and provides the drivers for the three local camera status LED's.

### 71.3.7 INCO Uplink Commands

When the CTVC is first powered up, the camera defaults to manual gain (MAN GAIN) menu. The first uplink command sent should be to command the CTVC to ALC MENU and select an ALC mode (typically NORM or AVG). To command the CTVC to the ALC MENU from the MAN GAIN menu, send function code 01000 (same as TVC ALC PEAK command). ALC NORM can then be selected by sending 01100 (same as TVC GAMMA NORM).

**Table 71-2. MCC Command Breakdown**

| COMMAND DESCRIPTION<br>(command title using CAMERA menu on CCUD)<br>(command title using CTVC menu on CCUD) | Function code                             |     |     |     |     |
|---|---|-----|-----|-----|-----|
|   | A9  | A10 | A11 | A12 | A13 |
| <b>All OFF MENU*</b>  |   |     |     |     |     |
| SHUTTER ON<br>(GAM WHITE)<br>(SHUTR ON/OFF)**   | 0   | 1   | 0   | 1   | 1   |
|   | (Same as TVC GAMMA WHITE STRETCH command) |     |     |     |     |
| SHUTTER OFF<br>(GAM WHITE)<br>(SHUTR ON/OFF)**  | 0   | 1   | 0   | 1   | 1   |
|   | (Same as TVC GAMMA WHITE STRETCH command) |     |     |     |     |
| BARS ON<br>(GAM NORM)<br>(TST PAT ON/OFF)**   | 0   | 1   | 1   | 0   | 0   |
|   | (Same as TVC GAMMA NORMAL command)        |     |     |     |     |
| BARS OFF<br>(GAM NORM)<br>(TST PAT ON/OFF)**  | 0   | 1   | 1   | 0   | 0   |
|   | (Same as TVC GAMMA NORMAL command)        |     |     |     |     |
| GAMMA LINEAR<br>(GAM BLACK)<br>(LINEAR ON/OFF)**  | 0   | 1   | 1   | 0   | 1   |
|   | (Same as TVC GAMMA BLACK STRETCH command) |     |     |     |     |
| GAMMA BLACK STRETCH<br>(GAM BLACK)<br>(LINEAR ON/OFF)**   | 0   | 1   | 1   | 0   | 1   |
|   | (Same as TVC GAMMA BLACK STRETCH command) |     |     |     |     |
| <b>ALC menu select</b>  |   |     |     |     |     |
| (ALC PEAK)<br>(ALC MENU)  | 0   | 1   | 0   | 0   | 0   |
|   | (Same as TVC ALC PEAK command)            |     |     |     |     |
| Mode selections within menu   |   |     |     |     |     |
| ALC PEAK<br>(GAM WHITE)<br>(PEAK)**   | 0   | 1   | 0   | 1   | 1   |
|   | (Same as TVC GAMMA WHITE STRETCH command) |     |     |     |     |
| ALC NORMAL<br>(GAM NORM)<br>(NORMAL)**  | 0   | 1   | 1   | 0   | 0   |
|   | (Same as TVC GAMMA NORMAL command)        |     |     |     |     |



**Table 71-2. MCC Command Breakdown (concluded)**

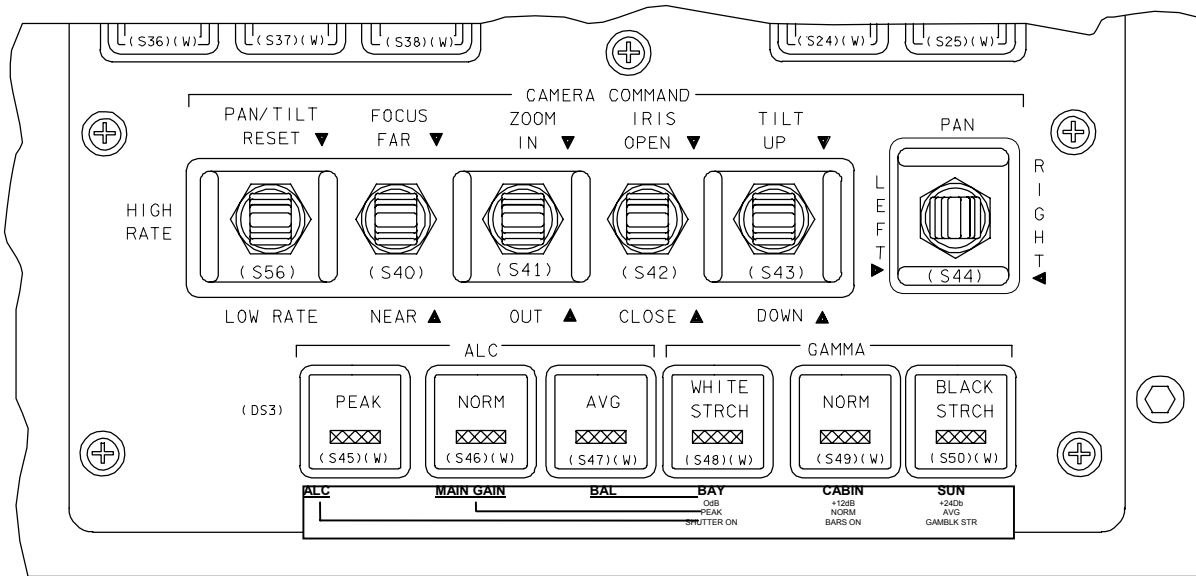
|   |  |
|---|--|
| ALC AVERAGE<br>(GAM BLACK)<br>(AVERG)**                 | 0 1 1 0 1<br>(Same as TVC GAMMA BLACK STRETCH command) |
| RETURN TO (ALL OFF) MENU<br>(ALC PEAK)<br>(ALC MENU)    | 0 1 1 0 0<br>(Same as TVC ALC PEAK command)            |
| <b>Manual gain menu select</b>                          |  |
| (ALC NORM)<br>(MAN GN MENU)                             | 0 1 0 0 1<br>(Same as TVC ALC NORM command)            |
| Mode selections within menu                             |  |
| 0 dB GAIN<br>(GAM WHITE)<br>(0 dB GAIN)**               | 0 1 0 1 1<br>(Same as TVC GAMMA WHITE STRETCH command) |
| +12 dB GAIN<br>(GAM NORM)<br>(12 dB GAIN)**             | 0 1 1 0 0<br>(Same as TVC GAMMA NORMAL command)        |
| +24 dB GAIN<br>(GAM BLACK)<br>(24 dB GAIN)**            | 0 1 1 0 1<br>(Same as TVC GAMMA BLACK STRETCH command) |
| RETURN TO (ALL OFF) MENU<br>(ALC NORM)<br>(MAN GN MENU) | 0 1 0 0 1<br>(Same as TVC ALC NORM command)            |
| <b>White balance menu select</b>                        |  |
| (ALC AVG)<br>(BAL MENU)                                 | 0 1 0 1 0<br>(Same as TVC ALC AVG command)             |
| Mode selections within menu                             |  |
| BAY(CCTV)/NIGHT(ITVC)<br>(GAM WHITE)<br>(BAY/NIGHT)**   | 0 1 0 1 1<br>(Same as TVC GAMMA WHITE STRETCH command) |
| CABIN(CCTV)/DAY(ITVC)<br>(GAM NORM)<br>(CABIN/DAY)**    | 0 1 1 0 0<br>(Same as TVC GAMMA NORMAL command)        |
| SUN(CCTV)/NIGHT(ITVC)<br>(GAM BLACK)<br>(SUN/NIGHT)**   | 0 1 1 0 1<br>(Same as TVC GAMMA BLACK STRETCH command) |
| RETURN TO (ALL OFF) MENU<br>(ALC AVG)<br>(BAL MENU)     | 0 1 0 1 0<br>(Same as TVC ALC AVG command)             |

\*To reach the "all off menu", send the command for the current menu.

\*\*PEAK, 0 dB GAIN, BAY/NIGHT, and SHUTR ON/OFF are the same command; NORMAL, 12dB GAIN, CABIN/DAY, TST PAT ON/OFF are the same command; and AVERG, 24 dB GAIN, SUN/NIGHT, and LINEAR ON/OFF are the same command. They are given different titles to reflect the action that will occur I the correct menu is selected.



A7 PANEL WITH CTVC DECAL



186111626. PNL 1

Orbiter panel switch functions

The shuttle color television camera decal was designed to assist crewmembers in the operation of the new shuttle solid-state color television cameras. The decal is located on the A7 panel and is used in conjunction with the switch S45 through S50 pushbutton indicators to provide crewmembers with a reference to indicate CTVC menu and mode selections. There are four menus and three mode selections per menu, as follows:

| MENUS        | MODE SELECTIONS |             |                    |
|--------------|-----------------|-------------|--------------------|
|              | 1.              | 2.          | 3.                 |
| 1. BAL       | BAY             | CABIN       | SUN                |
| 2. MAN GAIN  | 0dB             | +12dB       | +24dB              |
| 3. ALC       | PEAK            | NORM        | AVG                |
| 4. (ALL OFF) | SHUTTER ON/OFF  | BARS ON/OFF | GAM BLK STR/Linear |

The CTVC menu selections ALC, MAN GAIN, and BAL can be accessed by pressing either switch S45, S46, or S47 is illuminated. The ALL OFF menu is used as a starting point for ground controllers to implement uplink commands. After mode selection is completed, the menu switches should be returned to the ALL OFF menu. The previously selected modes are still active. ALL OFF means that all three menu select pushbutton indicator lamps (ALC, MAN GAIN, BAL) are off.

**Figure 71-9. Panel A7 switches/labeling with CTVC decal**

Menu Selection Example

Commanding the CTVC into an automatic light control (ALC) menu can be accomplished by pressing switch S45 (the pushbutton indicator will illuminate). At this point the crewmember can select one of three ALC mode selections PEAK, NORM, or AVG by pressing switch S48, S49, or S50, respectively, which will then illuminate indicating the mode selected.

| MENU     | MODE SELECTIONS |      |     |
|----------|-----------------|------|-----|
|          | 1.              | 2.   | 3.  |
| ALC (on) | PEAK            | NORM | AVG |

Exiting the above ALC menu can be accomplished by either pressing switch S46 (MAN GAIN menu select) or switch S47 (BAL menu select). Prior to selecting either the MAIN GAIN or BAL menu, exiting the ALC menu can also be accomplished by pressing switch S45 a second time. Pressing switch S45 a second time causes the pushbutton indicator lamp to extinguish and returns the CTVC to the ALL OFF menu.

The MAIN GAIN and BAL menus are selected and deselected in the similar manner as in the above example.

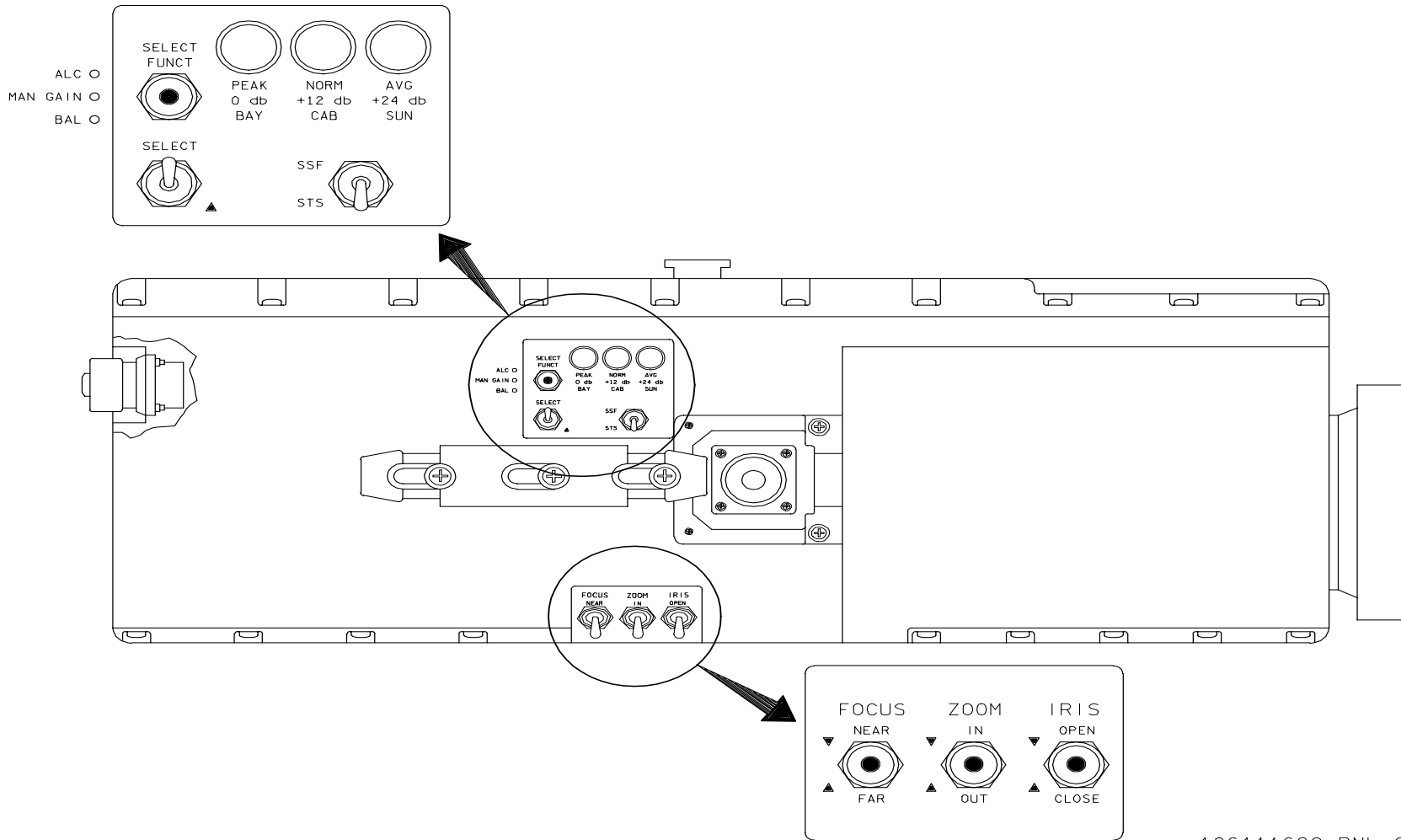
After menu and mode selections have been made, always return the menu selection to the ALL OFF menu.

ALL OFF MENU

To enter this menu, the crewmember deselects ALC, MAN GAIN, or the BAL menu. When none of these three switches are illuminated, the crewmember has entered the ALL OFF menu. At this point three additional modes can be selected.

- Pressing switch S48 turns on the anti-vertical smearing SHUTTER wheel. Switch S48 will illuminate. The SHUTTER can be turned off by pressing switch S48 a second time. This Switch does not control any active function of the ITVC from the ALL OFF MENU.
- The color BARS ON test pattern can be turned on by pressing switch S49. The switch S49 will become illuminated. Pressing switch S49 a second time extinguishes the indicator lamp, turns the color bars off, and reselects the CTVC video picture output. This switch controls the aperture (AP) in the ITVC from the ALL OFF Menu.
- The last mode available in the ALL OFF menu is the selection between GAM BLK STR (gamma black stretch) and linear (this also applies to ITVC). GAM Linear is the normal operating mode which is indicated when switch S50 is extinguished. Pressing switch S50 illuminates its indicator lamp and the camera enters BLK STRCH mode. To exit BLK STRCH mode and return to the LINEAR mode, press switch S50 a second time. This causes switch S50 to extinguish and places the camera back into normal operating LINEAR mode.

**Figure 71-9. Panel A7 switches/labeling with CTVC decal (concluded)**



186111622, PNL 2

**Figure 71-10. External switch orientation**

Camera switch functions

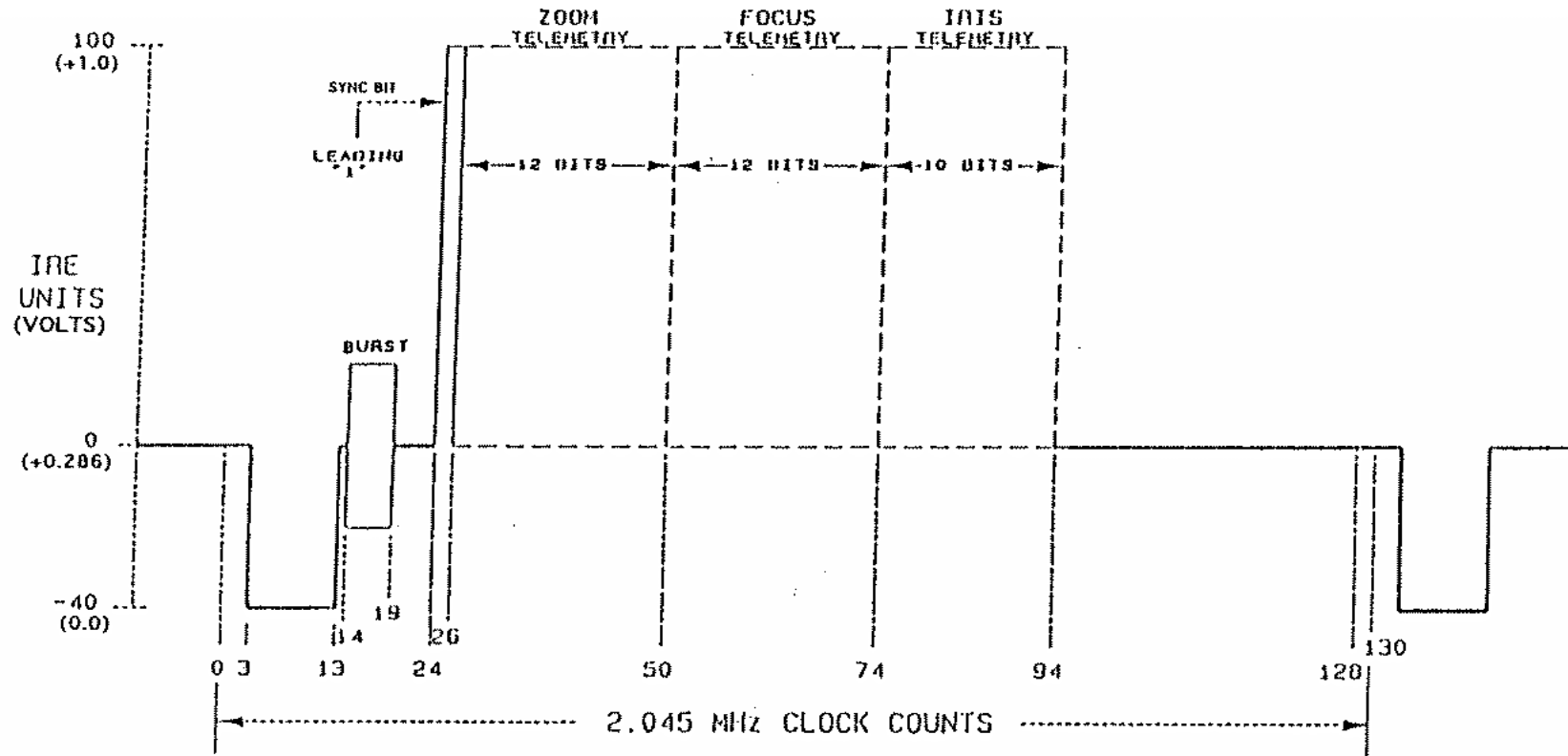
|             |   |   |
|-------------|---|---|
| FOCUS       | - | This is a three-position momentary switch that is spring-loaded to the center position. Holding the switch in either the NEAR or FAR position produces position continuous driving (in the appropriate direction) of the focus drive motor until a stop is reached or the switch is released.   |
| ZOOM        | - | Operates similarly to FOCUS switch.   |
| IRIS        | - | Operates similarly to FOCUS switch.   |
| SELECT FUNC | - | This is a three-position toggle switch. Its purpose is to enable the SELECT switch to command (in a sequencing fashion) either the ALC, MANUAL GAIN, or BALANCE functions, and at the same time assign the three associated indicators to display either ALC, MANUAL GAIN, or BALANCE status. (If the FUNCTION SELECT switch is in ALC position, the ALC status is indicated by an illuminated PEAK, NORM, or AVG lamp. The ALC status may be changed by momentarily depressing the SELECT switch.) |
| SELECT      | - | This is a two-position momentary switch that is spring loaded to the UP position. It works in conjunction with the FUNCTION SELECT switch to command ALC, MANUAL GAIN, and BALANCE functions.   |
| SSF/STS     | - | This is a two-position toggle switch.<br>STS - 5 bit location code (shuttle)<br>SSF - 7 bit location code (station)   |

**Figure 71-10. External switch orientation (concluded)**

**71.3.7.1 VID Telemetry**

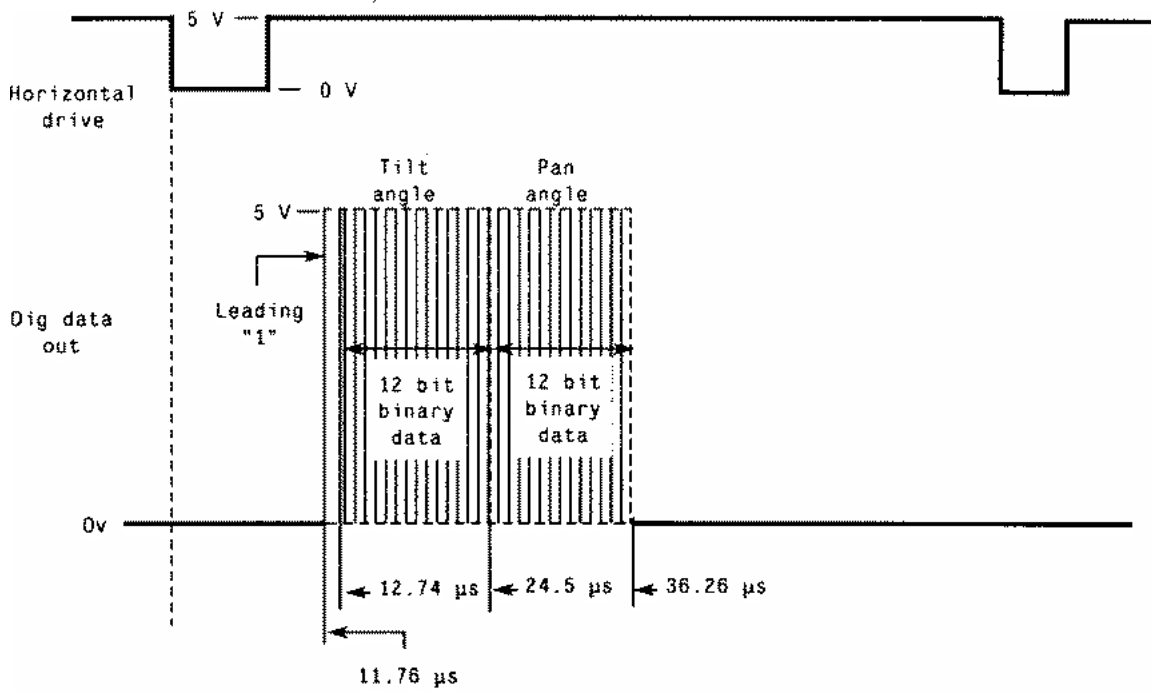
Camera telemetry is inserted into the vertical interval during lines 12, 14, 16, 17, and 18. The TLM associated with each of these lines is lens data, pan/tilt data, camera operating mode data, camera address and serial number data, and temperature data, respectively.

In line 16 of the VID, the data seen in clock periods (CP) 26-38 is status feedback of the ALC/GAM commands sent to the selected camera by the RCU and reflected on panel A7U as well as OI Telemetry. This was old camera ALC and Gamma data but it still used with the CTVC/ITVC cameras to provide telemetry to the VCU; this data is decoded as DB1-DB6 in the MCC VID Detector (VIDD). The data in CP 102-128 represents the actual status of the CTVC/ITVC camera functions, which are decoded as DB7-DB19 in the VIDD. Full VIDD interpretation is covered in section 71.6.3.



CTVC line 12 lens assembly telemetry.  
Vertical interval data (VID) format.  
Output from camera.

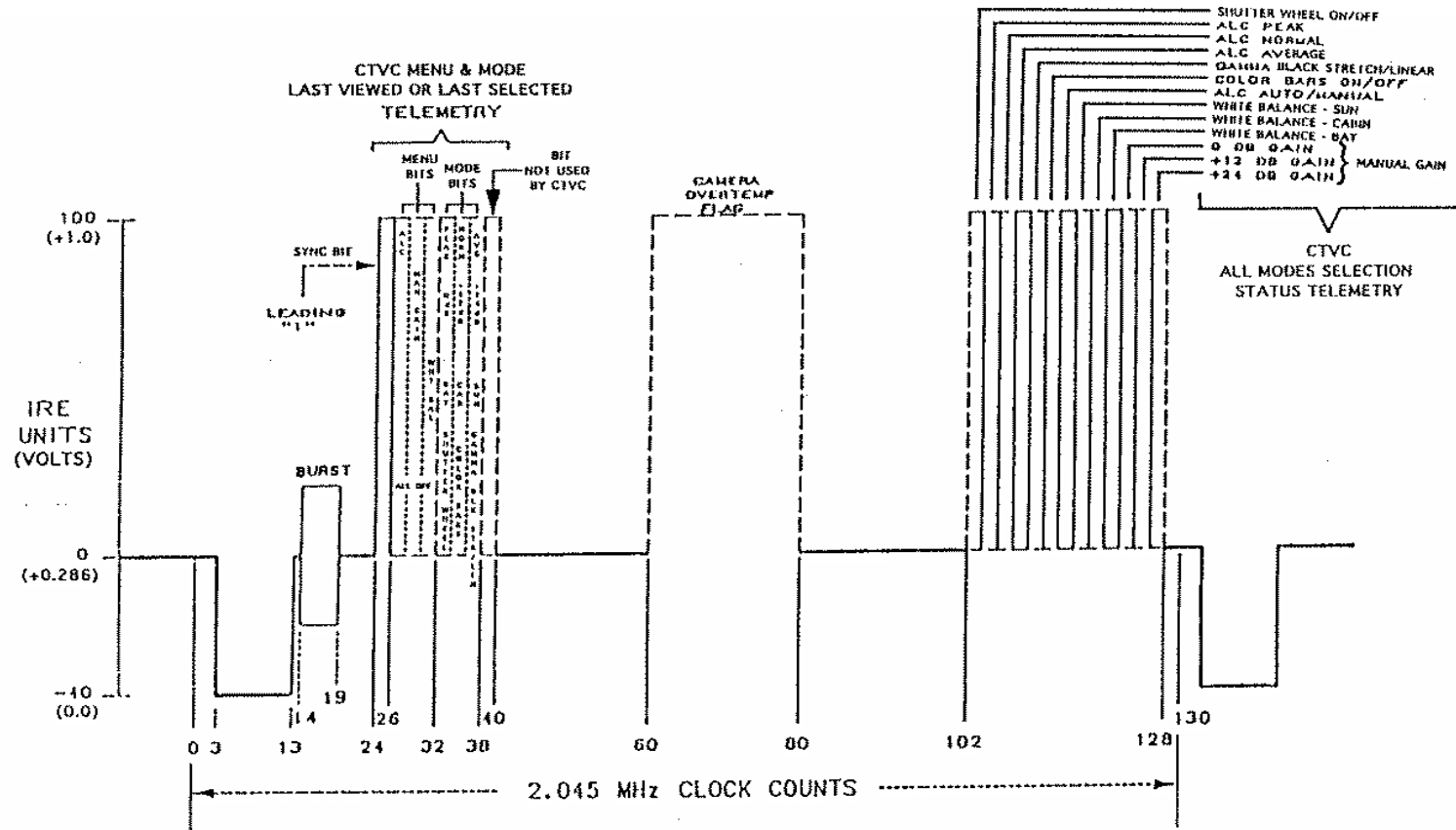
Figure 71-11. Line 12 lens data format



JSC 18611\*091:16

Figure 71-12. Line 14 pan/tilt data format

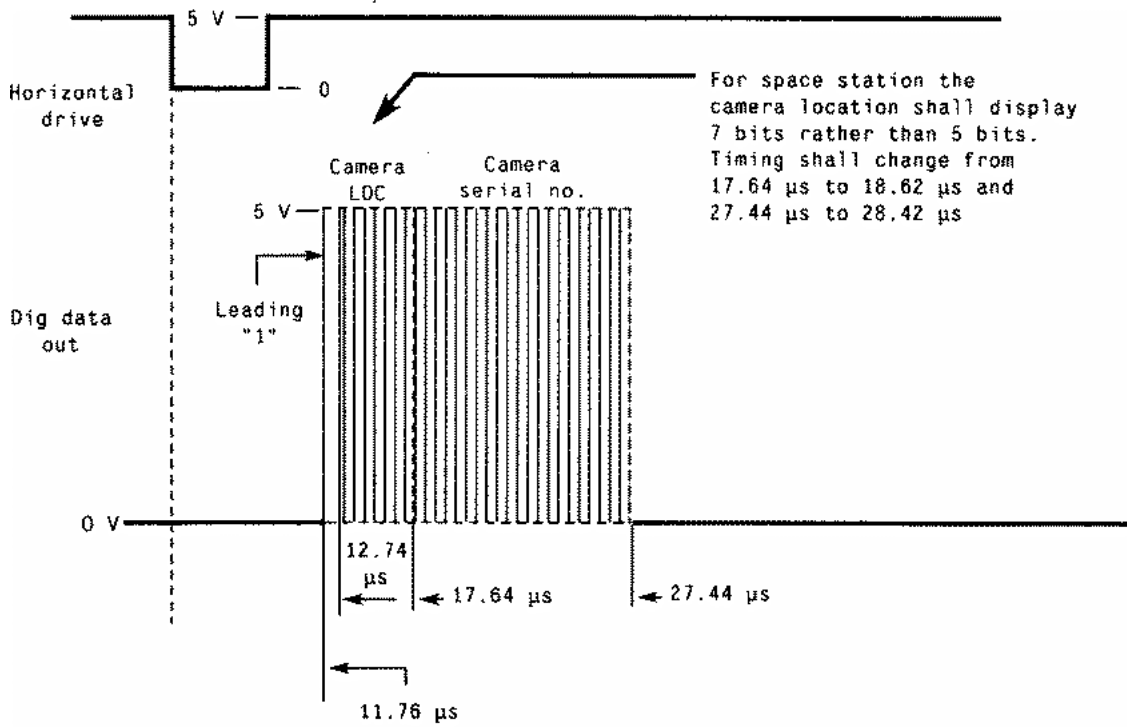




CTVC line 16 camera modes status telemetry vertical interval data (VID) format with VSU inserted camera overtemp flag (output from VSU).

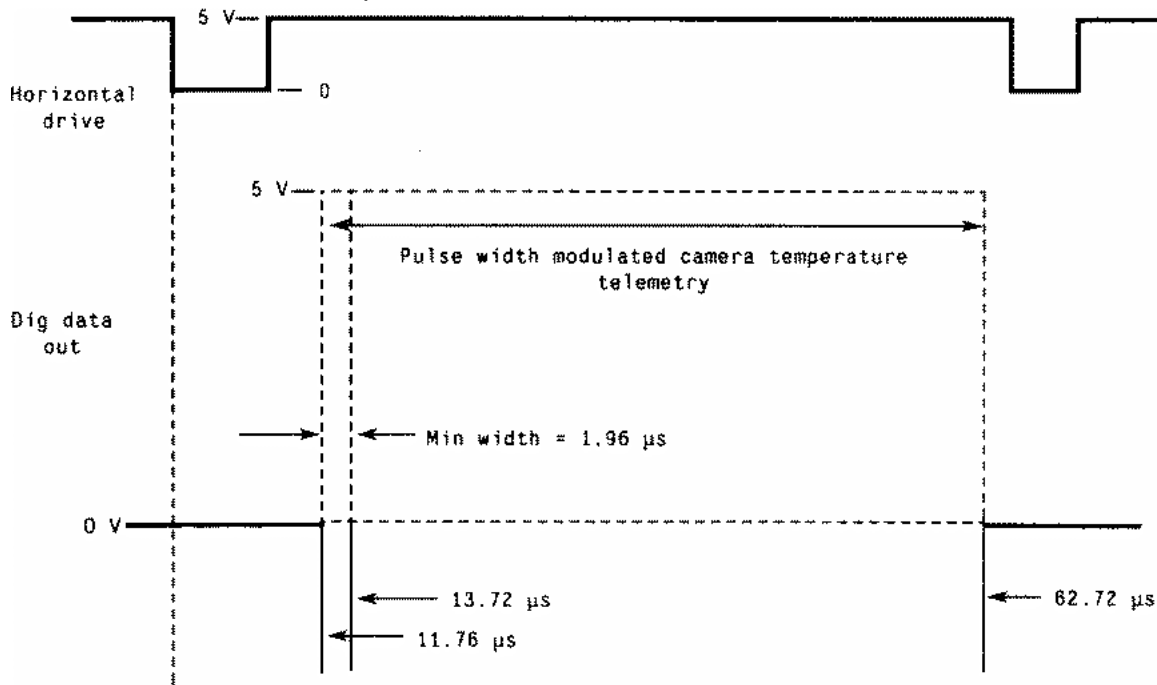
- NOTES:
1. The camera overtemp pulse width is approximate.
  2. The camera overtemperature flag is inserted onto the downlink video line 16 at the VSU, when any powered-on CCTV camera temperature exceeds +45° C.

**Figure 71-13. Line 16 camera command status data format**



JSC 18611\*089.16

Figure 71-14. Line 17 camera ID data format



JSC 18611\*088:16

**Figure 71-15. Line 18 camera temperature**

### 71.3.7.2 Pan/Tilt Control

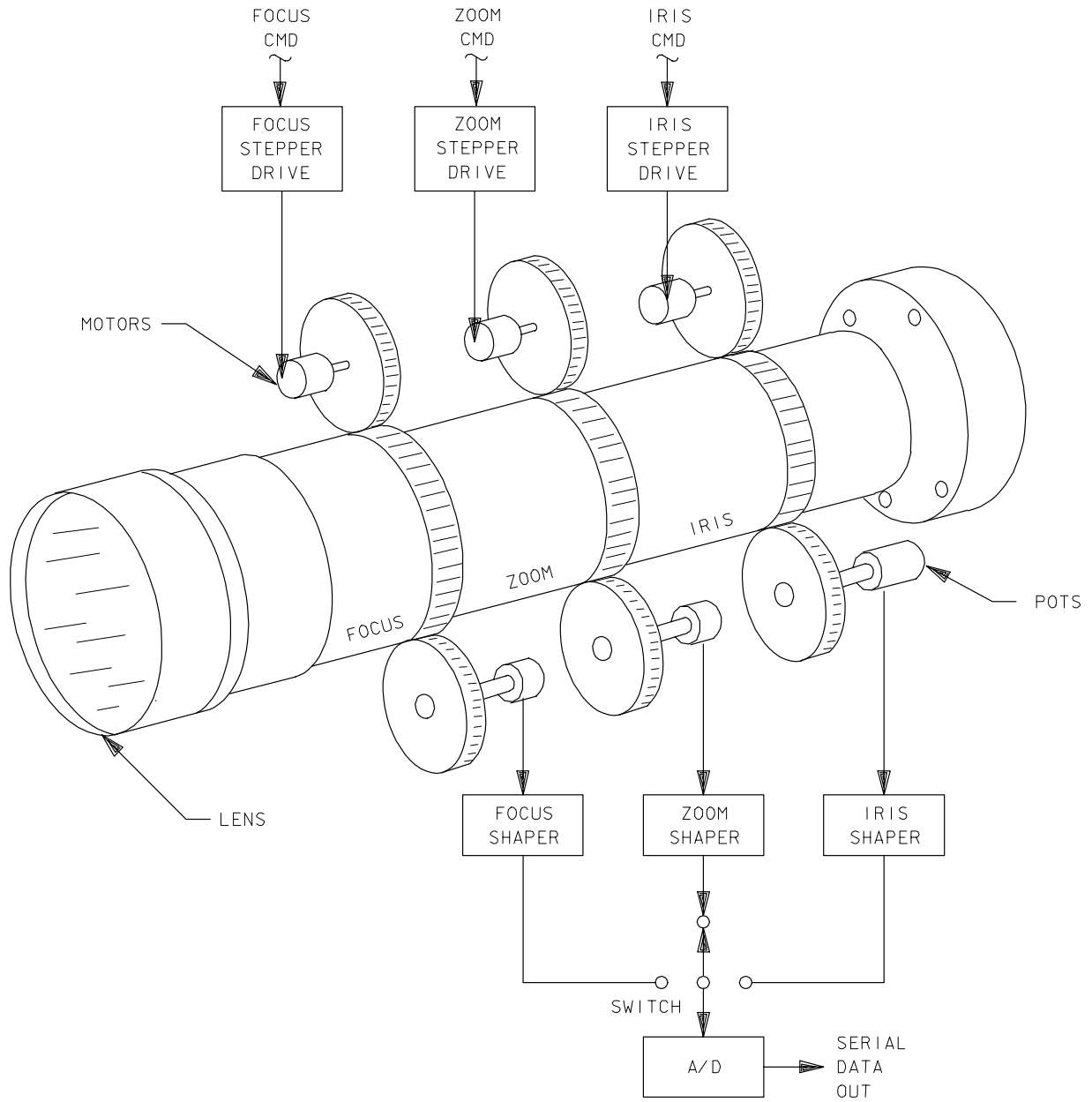
The CMD/TLM provides the circuitry to decode the remote pan/tilt (P/T) commands and to generate the pan/tilt control clocks (fast and slow) and resettable counters that derive relative pan and tilt angles for insertion on line 14. The remote commands consist of P/T fast, P/T slow, P/T reset, pan right, pan left, tilt up, and tilt down. Limit switch closures associated with the PTU are also accepted by the CMD/TLM processor. These are the right and left limit switches and the up and down limit switches. If a limit switch is enabled, the P/T control clock will be inhibited and the position counter will stop counting. The P/T control provides an 11-bit counter to monitor pan and tilt position. It also generates a sign bit for the counter to determine the direction of motion away from zero. A P/T reset command resets the counter to zero.

### 71.3.7.3 Lens Motor Control

The CMD/TLM processor also provides the necessary circuitry to decode and enact local and remote lens motor commands. These commands are iris open and close, focus near and far, and zoom in and out. As in the P/T commands, there are end-of-motion limit switches associated with each of these commands. The CMD/TLM processor responds to these commands and generates the necessary motor drive clocking signals. Each motor requires four separate clocks, each a different phase. The relationship of the clock phases determines the direction in which the motor will turn. The focus and zoom motor controllers run at 120 Hz. The iris motor controller on the other hand operates at two rates, 120 Hz and 60 Hz. Unlike the focus and zoom

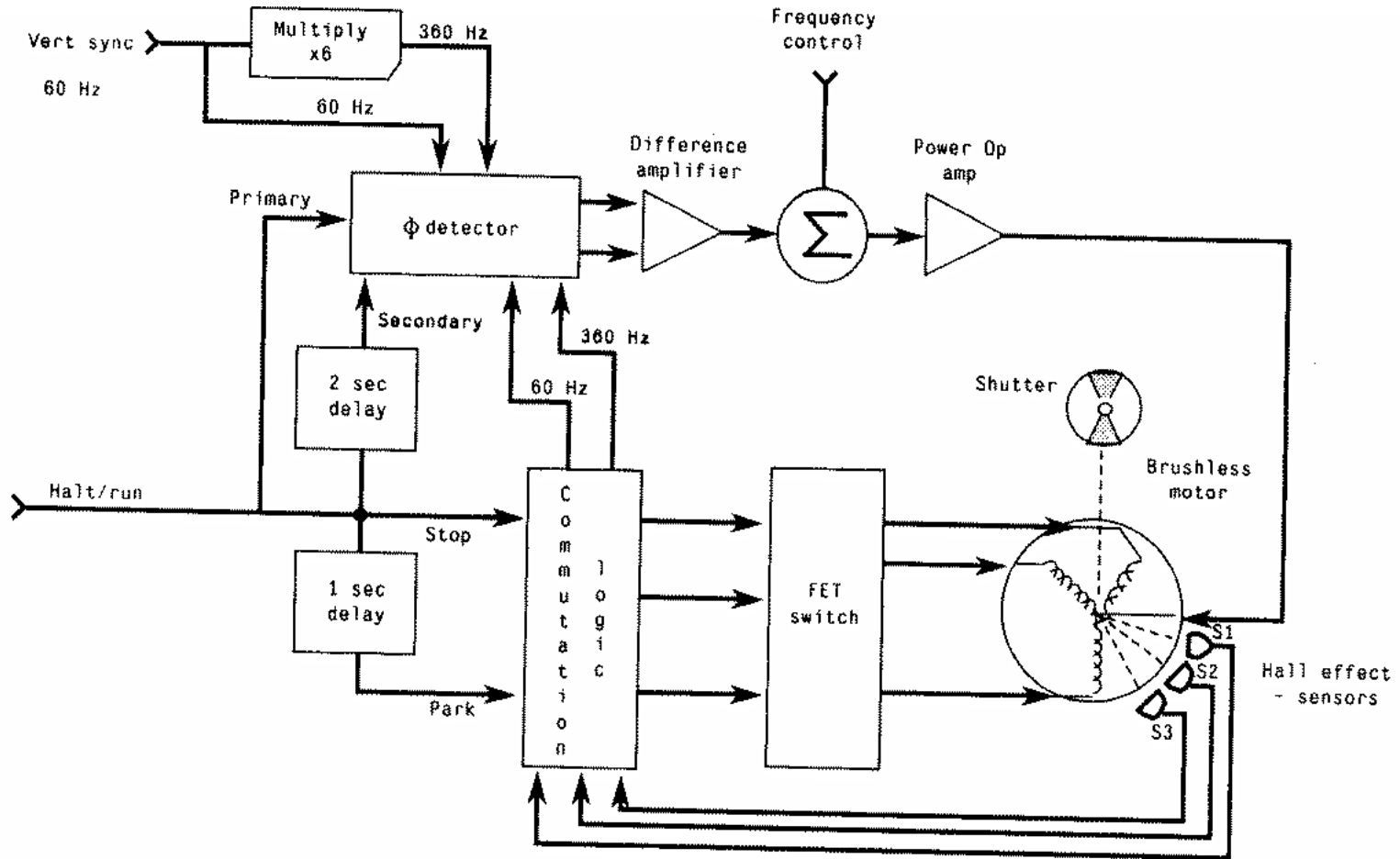
controls, the iris controller also responds to open and close commands from the ALC/AGC control. Commands from ALC automatically select the 120-Hz clock. Local or remote commands automatically select the 60-Hz clock. In addition, the remote or local commands cause a command to be transmitted to the command decoder that forces the camera into the manual gain 0-dB mode. Finally, the iris controller responds to a pulse transmitted just prior to powerdown. This command, POWER OFF PRESET, is latched and forces the iris to close at the 120-Hz rate. Enough time is allowed for the iris to close fully from a fully open position before power is lost. The focus, zoom, iris, and shutter interface to the lens assembly is made via gear-driven stepper motors. One motor is dedicated to each function of focus, zoom, and iris. A second series of three gears attaches to three potentiometers to read a voltage indicative of position of focus, zoom, and iris. The voltages are shaped, selected via analog switches, routed to the A-D, and eventually output as a serial data stream. A rotating shutter wheel (not shown in Figure 3-32) is located between the lens assembly and CCD sensor. The servo drives the shutter wheel in synchronism with an externally furnished horizontal sync pulse.

The shutter wheel is driven under instruction of its Hall effect sensors via the commutation logic and FET switches. One of the Hall effect sensors is used as a phase generator. The output of the phase detector is looped around via a differential amplifier, a power op amp, to control the speed of the motor as shown in Figure 71-17.



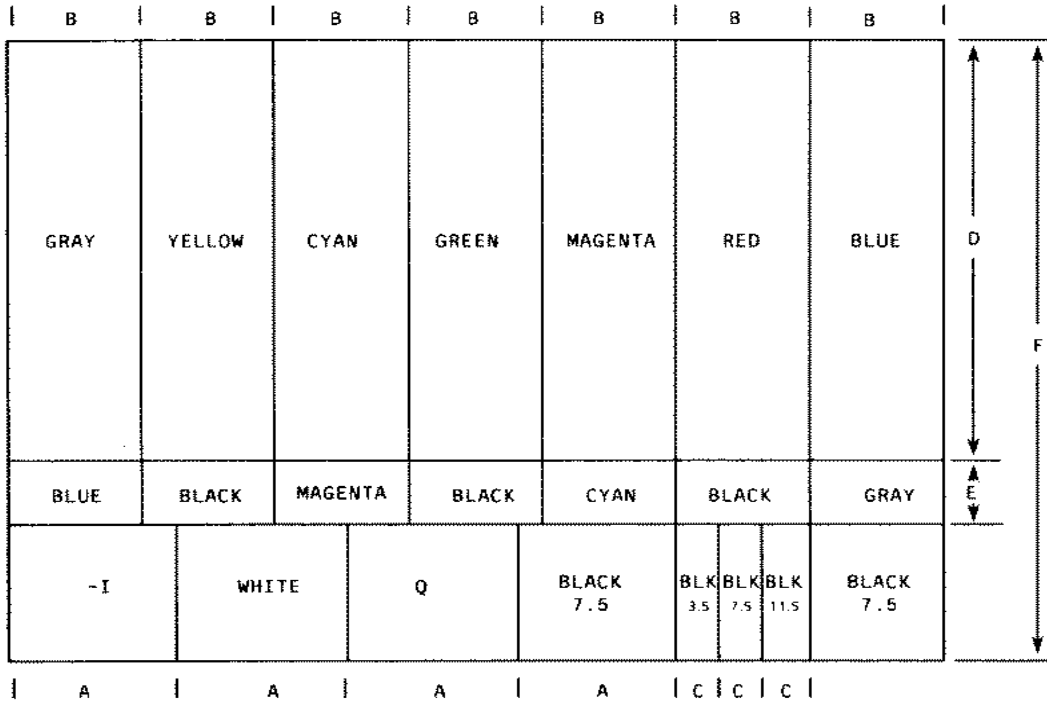
186111635. ISO; 1

**Figure 71-16. Camera Lens**



JSC 18611\*085

Figure 71-17. Shutter servo



A - 9.40  $\mu$ s      D - 10.30 ms  
 B - 7.52  $\mu$ s      E - 1.21 ms  
 C - 2.51  $\mu$ s      F - 15.41 ms

NOTES: 1. Vertical blanking period = 20 H (1.271 ms)  
 2. Horizontal blanking period = 10.9  $\mu$ s

JSC 18611\*086:16

**Figure 71-18. SMPTE color bar pattern**

#### 71.4 POWER ON RESET

During powerup, a POWER ON RESET signal is received by the CMD/TLM processor. In addition to initializing the CMD/TLM for proper operation, the signal also configures the operating modes of the camera to an initial known condition. The CMD/TLM will reset the camera as follows:

- Manual gain mode selected
- 0-dB mode selected
- Color balance - Daylight selected
- Shutter - Disabled
- Gamma - Linear
- Color bars - Disabled
- Pan/tilt control clock - Disabled
- Pan/tilt position counters - Disabled
- Iris, focus, and zoom motors - Disabled
- Command receiver counters and shift registers - Cleared

#### 71.5 SYNCHRONIZATION

The CTVC composite video output may be synchronized in frequency to the master composite sync signal distributed throughout the orbiter by the RCU. This signal also provides camera command data from both ground and crew. In the event of loss of master sync, the CTVC will continue to provide an NTSC composite video signal that conforms to EIA STD RS-170A but is asynchronous with the balance of the orbiter video system. See Figure 71-19.



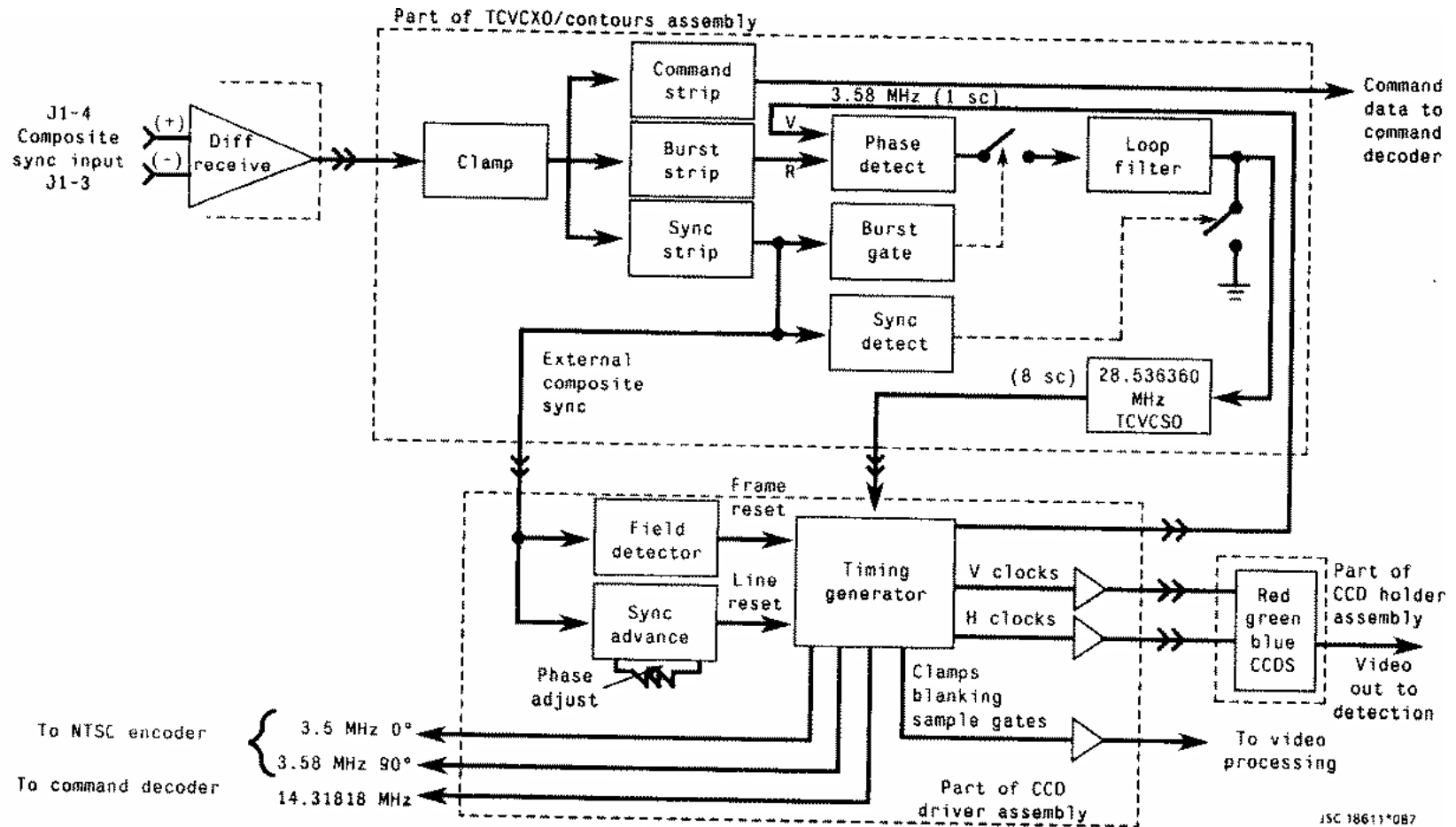


Figure 71-19. Synchronization

## 71.6 RGB VIDEO PROCESSING

The video from the green channel generated from the ALC/AGC first undergoes a one-line delay to place it in phase with the red and blue channels; the green channel CCD has been mechanically displaced by one line to permit development of the vertical contour signal. From this point, all three component channels (RGB) undergo identical processing and provide the following functions:

- Aperture compensation
- Gamma compensation
- Black level restoration
- Black/white clipping
- SMPTE color bar generation
- Video/color bar switching
- Sync, VITS, and digital data insertion
- Sync and command line receiver
- NTSC and RGB line drivers
- Vertical contour generation

### 71.6.1 NTSC Color Encoder

This is used to convert red, green, and blue component video signals to a composite video signal encoded in NTSC format. The encoder consists of two major paths, the luminance channel and the chrominance channel. Both channels require individual matrixes, low pass filters, and modulators. The modulators are used to generate chrominance signal (color information). Following blanking, the chrominance signal is summed to the delayed luminance signal to form the NTSC composite video signal. The NTSC signal is sent to the RGB video processor where it is output from the camera through the NTSC output driver circuitry.

Composite picture signal, nominal 1V P-P into 75-ohm load impedance, black negative, multiplexed with following vertical interval telemetry information.

| Vertical interval line number | Field number | Signal information                            |
|-------------------------------|--------------|---|
| 11                            | 1/2          | Camera control commands                       |
| 12                            | 1/2          | Lens function status                          |
| 13                            | 1/2          | Camera control commands                       |
| 14                            | 1/2          | Pan/tilt angle status                         |
| 16                            | 1/2          | Camera status                                 |
| 17                            | 1/2          | Camera location - S/N identification          |
| 18                            | 1/2          | Camera temperature via PWM signal             |
| 19                            | 1            | VITS-mod. staircase, 2T pulse, and bar window |
|                               | 2            | VITS-multiburst                               |

**Figure 71-20. NTSC/green video output**

| Parameter      | Horizontal<br>(deg) | Vertical<br>(deg) |
|----------------|---------------------|-------------------|
| ZOOM IN        | 10.6                | 8.0               |
| ZOOM OUT       | 77.0                | 61.0              |
| FOCUS DISTANCE | 1 ft to infinity    |                   |
| F-STOP         | F1.7 to F16         |                   |
| FOCAL LENGTH   | 5.5mm to 47mm       |                   |
| ZOOM           | 8.5 to 1            |                   |

**Figure 71-21. Camera lens capability**

### 71.6.2 Differences in the ITVC Telemetry

The ITVC was designed to insert its temperature telemetry pulse on only two out of three fields (CTVC is three out of three fields) to give the CTV Monitor something different allowing it automatically to shift to Black and White. The drawback to this function is, when the ITVC powers and syncs up, it ships its telemetry to the VSU. The VSU is designed to only look on only one out of three of the old FSC fields (the “third”, or “green” field, using the RCU sync signal as the “third field reference”).

Because the ITVC was designed to put the temperature pulse in two out of three fields, there is a 1 in 3 possibility of the ITVC inserting the temp pulse in the wrong fields (“red” and “blue”, but not “green” or, “first” and “second”, but not “third”). When in this condition, the A7 lights and the VSU OI telemetry go static. The VIDD overlay data is still good, since the VIDD does not use the presence or absence of data on the “third” field for anything. Also note that the CTVM, when on internal sync, can decode the ITVC PTU data, lens data, and temp without problems.

If the VSU randomly comes up in this 1 in 3 possibility by analyzing the “green” field of the ITVC and the A7 lights are off (crew) and OI telemetry (INCO) shows default ITVC State(ALC=NORM, GAMMA =WHITE, or MAN GAIN=0db), power cycle the ITVC (normal sequence – off, wait at least 5 seconds, on). Eventually, the odds will put the ITVC pulse out in the “green” field, allowing the VSU/RCU units to show the A7 lights and OI telemetry.

**Table 71-3. ITVC Differences**

|                      | CTVC                   | ITVC       |
|----------------------|------------------------|------------|
| <b>BAL Telemetry</b> | Bay, Cabin, Sun        | Night, Day |
| <b>ALL OFF menu</b>  | Shutter and Color Bars | Aperture   |

### 71.6.3 Vertical Interval Data Detector (VIDD) Display Interpretation

#### 71.6.3.1 VID Line 12

|     |              |      |      |        |             |              |               |
|-----|--------------|------|------|--------|-------------|--------------|---------------|
| XXX | ALC          | YYY  | PAN  | +000.0 | <b>FOC</b>  | <b>000.0</b> | +00C          |
| TTT | GAM          | ZZZ  | TLT  | -000.0 | <b>ZOOM</b> | <b>000.0</b> | <b>T/0000</b> |
| GMT | 000:00:00:00 | AAAA | MMMM | SSSS   | WWW         | GGGG         |               |

- FOCUS (FOC), ZOOM, T (IRIS Sensitivity)

#### 71.6.3.2 VID Line 14

|     |              |      |            |               |      |       |        |
|-----|--------------|------|------------|---------------|------|-------|--------|
| XXX | ALC          | YYY  | <b>PAN</b> | <b>+000.0</b> | FOC  | 000.0 | +00C   |
| TTT | GAM          | ZZZ  | <b>TLT</b> | <b>-000.0</b> | ZOOM | 000.0 | T/0000 |
| GMT | 000:00:00:00 | AAAA | MMMM       | SSSS          | WWW  | GGGG  |        |

- PAN, TILT Relative Angles

#### 71.6.3.3 VID Line 15

|            |                     |      |      |        |      |       |        |
|------------|---------------------|------|------|--------|------|-------|--------|
| XXX        | ALC                 | YYY  | PAN  | +000.0 | FOC  | 000.0 | +00C   |
| TTT        | GAM                 | ZZZ  | TLT  | -000.0 | ZOOM | 000.0 | T/0000 |
| <b>GMT</b> | <b>000:00:00:00</b> | AAAA | MMMM | SSSS   | WWW  | GGGG  |        |

- GMT Greenwich Mean Time

71.6.3.4 VID Line 16

|     |              |            |      |        |      |       |        |
|-----|--------------|------------|------|--------|------|-------|--------|
| XXX | <b>ALC</b>   | <b>YYY</b> | PAN  | +000.0 | FOC  | 000.0 | +00C   |
| TTT | GAM          | ZZZ        | TLT  | -000.0 | ZOOM | 000.0 | T/0000 |
| GMT | 000:00:00:00 | AAAA       | MMMM | SSSS   | WWW  | GGGG  |        |

- YYY ALC Setting

|                |                |
|----------------|----------------|
| -506 and -508: | PK, NOR or AVG |
| CTVC:          | PK, NOR or AVG |
| ITVC:          | PK, NO or AVG  |

|     |              |            |      |        |      |       |        |
|-----|--------------|------------|------|--------|------|-------|--------|
| XXX | ALC          | YYY        | PAN  | +000.0 | FOC  | 000.0 | +00C   |
| TTT | <b>GAM</b>   | <b>ZZZ</b> | TLT  | -000.0 | ZOOM | 000.0 | T/0000 |
| GMT | 000:00:00:00 | AAAA       | MMMM | SSSS   | WWW  | GGGG  |        |

- ZZZ Gamma Setting

|                |                 |
|----------------|-----------------|
| -506 and -508: | WHT,NOR, or BLK |
| CTVC or ITVC   | LIN or NOR      |

|     |              |             |      |        |      |       |        |
|-----|--------------|-------------|------|--------|------|-------|--------|
| XXX | ALC          | YYY         | PAN  | +000.0 | FOC  | 000.0 | +00C   |
| TTT | GAM          | ZZZ         | TLT  | -000.0 | ZOOM | 000.0 | T/0000 |
| GMT | 000:00:00:00 | <b>AAAA</b> | MMMM | SSSS   | WWW  | GGGG  |        |

- AAAA = ALC Mode
  - Old Cameras data is in clock period 38-40 after DB6
  - CTVC/ITVC data is in DB13

|           |     |
|-----------|-----|
| Automatic | AUT |
| Manual    | MAN |

|     |              |      |             |        |      |       |        |
|-----|--------------|------|-------------|--------|------|-------|--------|
| XXX | ALC          | YYY  | PAN         | +000.0 | FOC  | 000.0 | +00C   |
| TTT | GAM          | ZZZ  | TLT         | -000.0 | ZOOM | 000.0 | T/0000 |
| GMT | 000:00:00:00 | AAAA | <b>MMMM</b> | SSSS   | WWW  | GGGG  |        |

- MMMM = Menu Mode
  - CTVC/ITVC menus decoded from DB1-DB3
  - ALC = ALC Menu
  - GAIN = Manual Gain Control Menu
  - WBAL = White Balance Menu
  - LLVL = Light Level Control Menu
  - AOFF = All OFF Menu

|            |                       |
|------------|-----------------------|
| 506 or 508 | (Blank)               |
| CTVC       | ALC, GAIN, WBAL, AOFF |
| ITVC       | ALC, GAIN, LLVL, AOFF |

|     |              |      |      |             |      |       |        |
|-----|--------------|------|------|-------------|------|-------|--------|
| XXX | ALC          | YYY  | PAN  | +000.0      | FOC  | 000.0 | +00C   |
| TTT | GAM          | ZZZ  | TLT  | -000.0      | ZOOM | 000.0 | T/0000 |
| GMT | 000:00:00:00 | AAAA | MMMM | <b>SSSS</b> | WWW  | GGGG  |        |

- SSSS = Shutter or Aperture Correction Status
  - CTVC/ITVC camera data is in DB7

|            |              |
|------------|--------------|
| 506 or 508 | (Blank)      |
| CTVC       | SHON or SHOF |
| ITVC       | APON or APOF |

|     |              |      |      |        |            |       |        |
|-----|--------------|------|------|--------|------------|-------|--------|
| XXX | ALC          | YYY  | PAN  | +000.0 | FOC        | 000.0 | +00C   |
| TTT | GAM          | ZZZ  | TLT  | -000.0 | ZOOM       | 000.0 | T/0000 |
| GMT | 000:00:00:00 | AAAA | MMMM | SSSS   | <b>WWW</b> | GGGG  |        |

- WWW = White Balance or Light Level Status
  - CTVC/ITVC camera data is in DB14 - DB 16
  - SUN = Sun white balance
  - BAY = PLB Floodlight White Balance
  - CAB = Cabin White Balance
  - DAY = Day Light Levels
  - NIT = Night Light Levels

|            |                  |
|------------|------------------|
| 506 or 508 | (Blank)          |
| CTVC       | SUN, BAY, or CAB |
| ITVC       | DAY, NIT         |

|     |              |      |      |        |      |             |        |
|-----|--------------|------|------|--------|------|-------------|--------|
| XXX | ALC          | YYY  | PAN  | +000.0 | FOC  | 000.0       | +00C   |
| TTT | GAM          | ZZZ  | TLT  | -000.0 | ZOOM | 000.0       | T/0000 |
| GMT | 000:00:00:00 | AAAA | MMMM | SSSS   | WWW  | <b>GGGG</b> |        |

- GGGG = Manual Gain Setting (valid only in MAN Mode)
  - CTVC/ITVC camera data is in DB17 - DB19

|            |                 |
|------------|-----------------|
| 506 or 508 | (Blank)         |
| CTVC       | 0db, 12db, 24db |
| ITVC       | 0db, 12db,24db  |

71.6.3.5 VID Line 17

|            |              |      |      |        |      |       |        |
|------------|--------------|------|------|--------|------|-------|--------|
| XXX        | ALC          | YYY  | PAN  | +000.0 | FOC  | 000.0 | +00C   |
| <b>TTT</b> | GAM          | ZZZ  | TLT  | -000.0 | ZOOM | 000.0 | T/0000 |
| GMT        | 000:00:00:00 | AAAA | MMMM | SSSS   | WWW  | GGGG  |        |

- TVC Type
  - The TVC Serial Number in the VID is used to determine the TVC type.

| TYPE    | Displayed | Serial Number ID |
|---------|-----------|------------------|
| 506,508 | OLD       | 0XX              |
| CTVC    | CTV       | 2xx or 4xx       |
| ITVC    | ITV       | 8xx              |
| OTHER   | OTH       |                  |

|            |              |      |      |        |      |       |        |
|------------|--------------|------|------|--------|------|-------|--------|
| <b>XXX</b> | ALC          | YYY  | PAN  | +000.0 | FOC  | 000.0 | +00C   |
| TTT        | GAM          | ZZZ  | TLT  | -000.0 | ZOOM | 000.0 | T/0000 |
| GMT        | 000:00:00:00 | AAAA | MMMM | SSSS   | WWW  | GGGG  |        |

- TVC Location Identification

|          |            |          |            |
|----------|------------|----------|------------|
| <b>0</b> | <b>FLT</b> | <b>8</b> | <b>MID</b> |
| 1        | -A-        | 9        | #9         |
| 2        | -C-        | 10       | #10        |
| 3        | #3         | 11       | #11        |
| 4        | #4         | 12       | #12        |
| 5        | -B-        | 13       | PL1        |
| 6        | RMS        | 14       | PL2        |
| 7        | -D-        | 15       | PL3        |
|          |            | 16-31    | #16-#31    |



### 71.6.3.6 VID Line 18

|     |              |      |      |        |      |       |             |
|-----|--------------|------|------|--------|------|-------|-------------|
| XXX | ALC          | YYY  | PAN  | +000.0 | FOC  | 000.0 | <b>+00C</b> |
| TTT | GAM          | ZZZ  | TLT  | -000.0 | ZOOM | 000.0 | T/0000      |
| GMT | 000:00:00:00 | AAAA | MMMM | SSSS   | WWW  | GGGG  |             |

- Camera Temperature (Celsius)

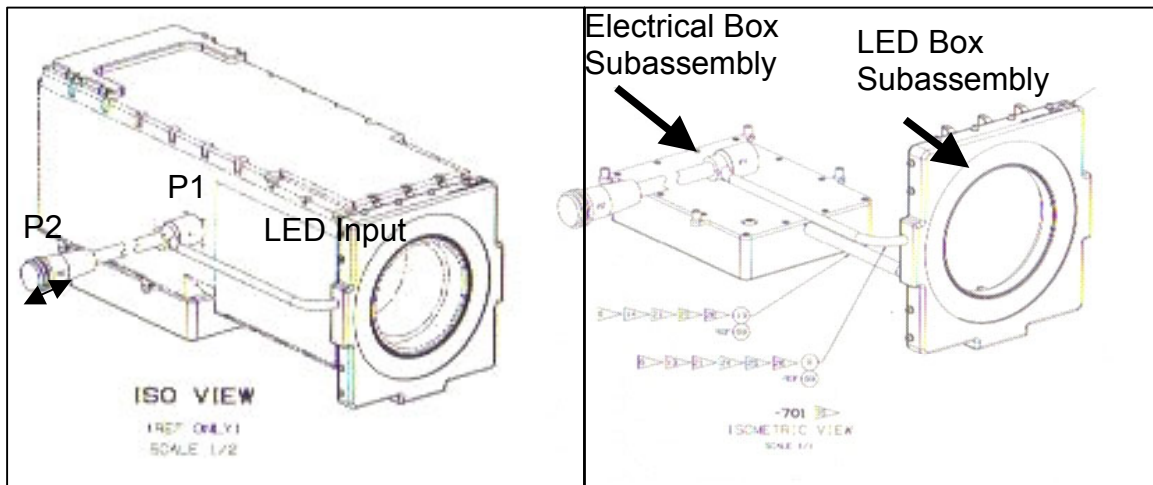
### 71.6.3.7 VID Display Colors

| COLOR  | USED FOR:                              | Abbreviation |
|--------|--|--------------|
| Black  | Background                             | BLK          |
| GREEN  | Data (Good)                            | GRN          |
| CYAN   | Data (no video coming into the VID)    | CYN          |
| VIOLET | Data (parameter missing or overridden) | VIO          |
| RED    | Data (parameter out of range)          | RED          |
| BROWN  | Titles                                 | BRN          |
| YEL    | Data (Off-Nominal)                     | YEL          |
| WHITE  | All Else                               | WHT          |

## 71.7 CAMERA ILLUMINATORS

### 71.7.1 General Description

The Illuminator Units are separate housed assemblies fit to the Camera as shown in Figures 71-22. Figure 71-22 details the Illuminator System (with the actual Camera removed) as two separate box assemblies, the Electrical Box Assembly and the Illuminator Box.



**Figure 71-22. Illuminator Subassemblies**

### 71.7.2 Camera LEDs

The CTVC has 180 white 20 degree (°) Illuminators.

As of STS-113, the ITVC use 180 white 20 degree (°) Illuminators.

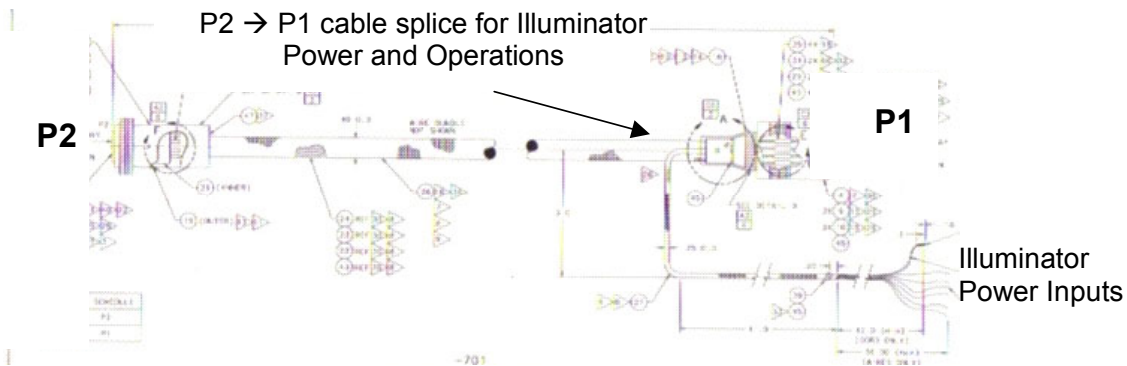
The RMS WRIST CTVC has 40 white 40° illuminators

### 71.7.3 Power to the Illuminator Assemblies

The Pan/Tilt Units, Cameras, and Illuminator Assemblies will receive power from combinations of the three different Power Inputs from Panel R14 circuit breakers (cb)

- CAMR/PAN-TILT cb
- CAMR HTR cb
- PAN-TILT HTR cb

All three Power Supplies are routed first into the Pan/Tilt Units which are located under the CCTV cameras; the three Power sources exit the Pan/Tilt Units through Port P2, see Figure 71-23, and become spliced prior to entering the P1 port, connected to the camera. The Illuminator Type determines “which” of the three Power Sources are spliced into for Illuminator Power (and Operation). Figure 71-25 is a detailed drawing of this cable inputs and outputs.



**Figure 71-23. PTU to Camera Cable**

The CTVC and ITVC which contain 180 white 20 degree (°) Illuminators spliced into the Power Supply from the following two circuit breakers for Illuminator Power and Operations:

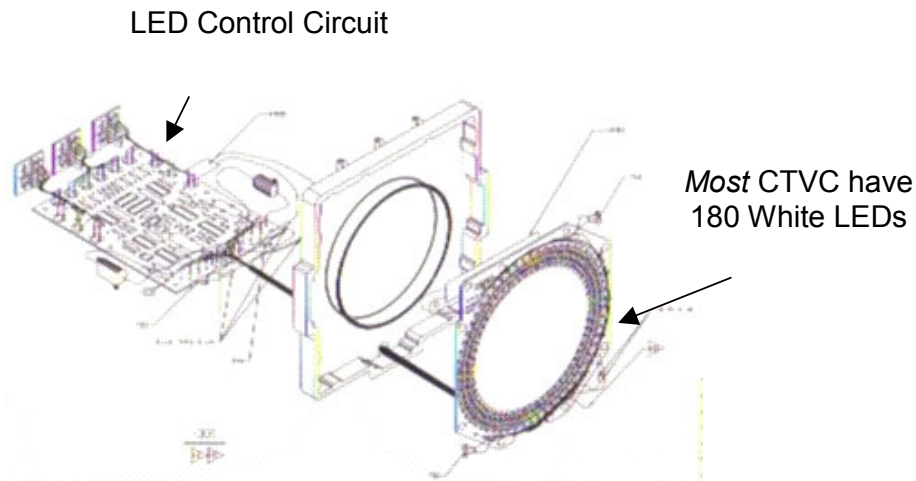
|               |           |
|---------------|-----------|
| CAMR/PAN-TILT | (Power)   |
| PAN-TILT HTR  | (Control) |

The other Illuminators spliced into the Power Supply from the following two circuit breakers for Illuminator Power and Operations:

|               |           |
|---------------|-----------|
| CAMR/PAN-TILT | (Power)   |
| CAMR HTR      | (Control) |

#### 71.7.4 Control to the Illuminator Assemblies

These two power supplies enter the Illuminator System through the LED Box Subassembly, and are immediately routed back to the LED Control Circuit. The LED Control Circuit contains the logic to turn on and off the LEDs. Figure 71-24 shows the internal views of the cable runs between the two assemblies.



**Figure 71-24. Illuminator Internal Views**

#### 71.7.4.1 Turning On and Off the 180 white 20 degree (°) Illuminators

The LED Control Circuit will turn ON and OFF the 180 white 20 degree (°) Illuminators with the use of two circuit breaker inputs as follows:

- CAMR/PAN-TILT cb power
- PAN-TILT HTR cb power

In General, the Illuminator System is powered by the CAMR/PAN-TILT cb and the crew will manually cycle PAN-TILT HTR cb power to turn the Illuminators ON/OFF.

The Crew will manually shut both circuit breakers (CAMR/PAN-TILT cb closed first then PAN-TILT HTR), Illuminators will initially not come on.

From then on cycling the PAN-TILT HTR ( off then on ) will turn **on** the Illuminators, the next cycling of the PAN-TILT HTR off/on will turn **off** the Illuminators.

If PAN-TILT HTR is erroneously closed first, then CAMR/PAN TILT cb is closed, it will require two additional cycles of the heater cb to get the Illuminator on for the first time.

#### 71.7.4.2 Turning On and Off other Illuminators

The major difference between the other Illuminators vs. the 180 white 20 degree (°) Illuminators is the P1 to P2 Cable spliced into the CAMR HTR cb, not the PAN - TILT HTR cb. With this stated, the operations of the other illuminators are similar to the 180 white 20 degree (°) Illuminators, except the crew is going to cycle the CAMR HTR cb, verse the PAN-TILT HTR cb, as follows:

The Illuminator System for other Illuminators are powered by the CAMR/PAN-TILT cb and the crew will manually cycle CAMR HTR cb power to turn the Illuminators ON/OFF.

The Crew will manually shut both circuit breakers (CAMR/PAN-TILT cb closed first then CAMR HTR), Illuminators will initially not come on.

From then on cycling the CAMR HTR ( off then on ) will turn **on** the Illuminators, the next cycling of the CAMR HTR off/on will turn **off** the Illuminators.

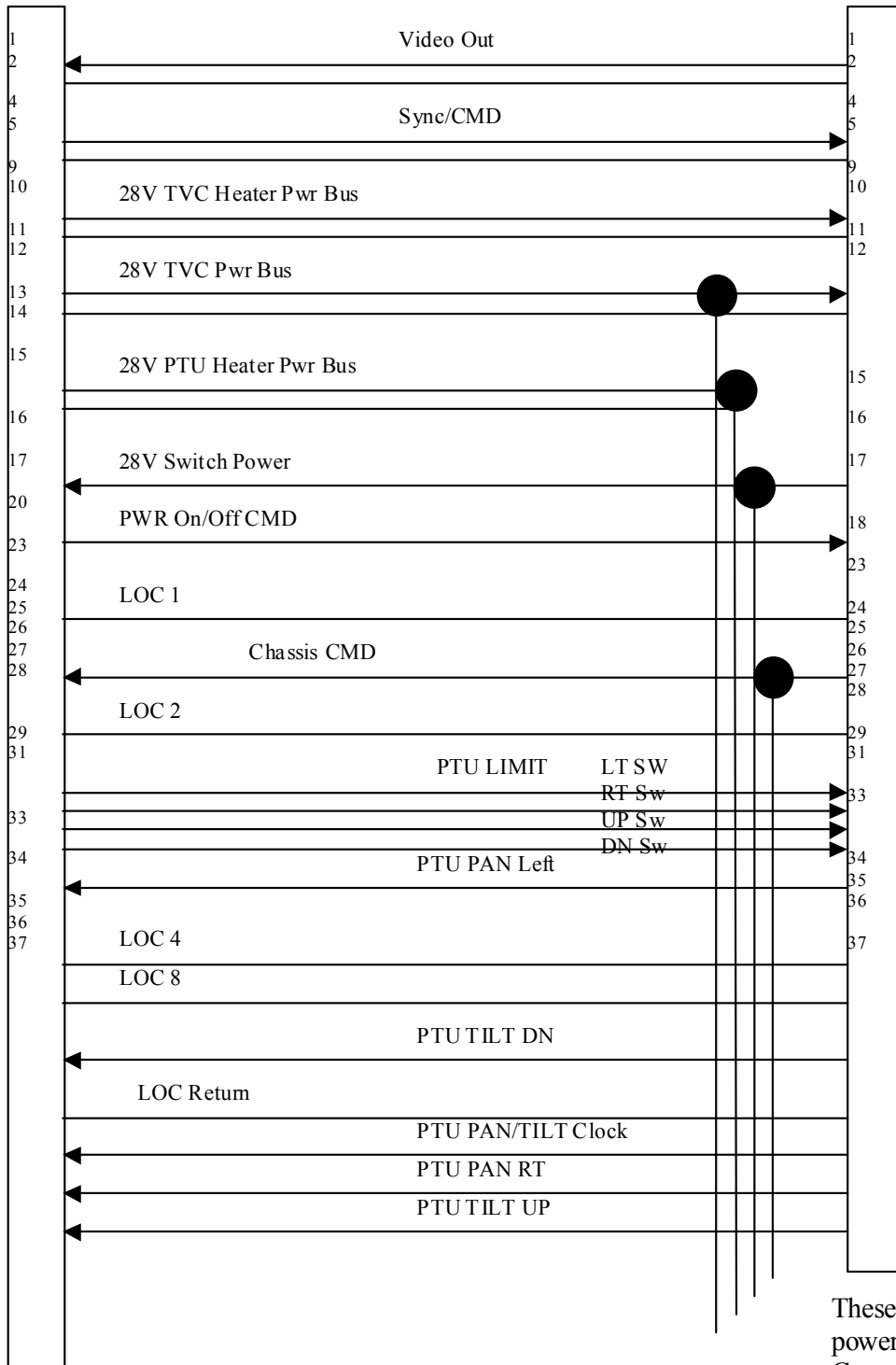
If CAMR HTR is erroneously closed first, then CAMR/PAN TILT cb is closed, it will require two additional cycles of the heater cb to get the Illuminator on for the first time.

#### **71.7.4.3 LED Control Circuit Flip-Flop Chain**

The LED Control Circuit, only taking two circuit breaker inputs, is designed using a chain of Flip-Flops to turn on and off the LEDs. The HTR circuit breaker is used as the input clock into the Chain of 6 Flip-Flops Logic. The Flip-Flop designed to input and store the circuit breaker opening and closing “events” and executing the inverse of the last stored output.

P2 (PTU)

P1 (CTVC/ITVC)



These signals are used to power and control the Camera Illuminators

Figure 71-25. PTU to CTVC Cable Schematic

- (a) The Video Out Signal is the Camera's NTSC Generated video signal which gets routed to the Video Switching Unit.
- (b) The Remote Control Unit (RCU) generates the Sync/CMD signal which is routed to the camera. When the crew (or MCC) sends a command to either the Camera or Pan/Tilt Unit (PTU) line 11 (or line 13), the RCU will embed the command into the Sync lines of the input camera signal.
- (c) All Heater Bus power comes directly from circuit breakers on R14. Notice that one of these inputs is redirected to supply both control and heat to the camera's illuminator control box.
- (d) 28 Volt Switch Power comes directly off the cameras.
- (e) The Remote Control Unit (RCU) processes the PWR On/Off CMD and routes it in parallel with the Sync/CMD Signal.
- (f) Each Camera uses a four bit pin location reference when in the payload bay.
- (g) Each Camera will take the Sync/CMD signal in from the RCU. If the command contains a PTU Pan or Tilt command, the camera sends the signal back through the cable to command the PTU motors.
- (h) If the PTU hits a 'hard stop' limit while either panning or tilting, the PTU sends one of four "limit" signals back to the camera.
- (i) The camera also sends a clock signal to the PTU.

## SECTION 72 - WIRELESS VIDEO SYSTEM

### CONTENTS

| Section |  | Page  |
|---------|--|-------|
| 72.1    | OVERVIEW.....  | 72-1  |
| 72.1.1  | Purpose.....   | 72-1  |
| 72.1.2  | General .....  | 72-1  |
| 72.1.3  | Components.....  | 72-1  |
| 72.1.4  | Power and Thermal.....   | 72-3  |
| 72.1.5  | Electrical Characteristics and Performance.....                              | 72-4  |
| 72.2    | PAYLOAD BAY ASSEMBLY.....  | 72-5  |
| 72.2.1  | Purpose.....   | 72-5  |
| 72.2.2  | General .....  | 72-5  |
| 72.2.3  | Components.....  | 72-6  |
| 72.3    | CREW COMPARTMENT ASSEMBLY .....  | 72-9  |
| 72.3.1  | Purpose.....   | 72-9  |
| 72.3.2  | General .....  | 72-9  |
| 72.3.3  | Components.....  | 72-10 |
| 72.4    | EXTRAVEHICULAR MOBILITY UNIT RADIO FREQUENCY<br>CAMERA ASSEMBLY (ERCA) ..... | 72-19 |
| 72.4.1  | Purpose.....   | 72-19 |
| 72.4.2  | General .....  | 72-19 |
| 72.4.3  | Components.....  | 72-21 |
| 72.5    | ANOMALIES AND IDIOSYNCRACIES.....  | 72-25 |
| 72.6    | REFERENCES.....  | 72-25 |



## TABLES

| Table |   | Page  |
|-------|---|-------|
| 72-1  | Temperature Design Limits for WVS Payload Bay Components..... | 72-3  |
| 72-2  | WVS Power Usage .....   | 72-4  |
| 72-3  | WVS Command Processing Requirements.....                      | 72-17 |
| 72-4  | Commanded Configuration .....                                 | 72-18 |
| 72-5  | WVS Telemetry .....   | 72-18 |

## FIGURES

| Figure |  |       |
|--------|--|-------|
| 72-1   | Overview Block Diagram of the Wireless Video System .....            | 72-2  |
| 72-2   | Panel A7U-WVS Power and Heater Control .....                         | 72-4  |
| 72-3   | Payload Bay Assembly, Antennas .....                                 | 72-6  |
| 72-4   | Block Diagram of the Payload Assembly .....                          | 72-7  |
| 72-5   | Wireless Video System Interface Box .....                            | 72-9  |
| 72-6   | PGSC RF Camera Page .....  | 72-13 |
| 72-7   | PGSC WVS Transceiver Page.....                                       | 72-14 |
| 72-8   | PGSC Telemetry Page.....   | 72-15 |
| 72-9   | Block Diagram of the WVS Interface Box.....                          | 72-16 |
| 72-10  | Isometric View of ERCA .....   | 72-19 |
| 72-11  | ERCA Component Location .....  | 72-20 |
| 72-12  | ERCA Camera and Command Processor.....                               | 72-20 |
| 72-13  | ERCA Cameras - Isometric Views .....                                 | 72-21 |
| 72-14  | Extravehicular Mobility Unit Radio Frequency<br>Camera Assembly..... | 72-22 |

## SECTION 72 WIRELESS VIDEO SYSTEM

### 72.1 OVERVIEW

The Wireless Video System (WVS) consists of three general sets of components:

- (1) Payload bay transceivers and antennas
- (2) Extravehicular Mobility Unit (EMU) mounted cameras including a radio frequency (RF) transceiver with antennas
- (3) A crew panel interface with RS422 ports and video routing capability together with a portable computer (including configuration and monitoring software and RS422 communications interfaces).

In General, there are three cameras on the EVA member's Helmet. Camera configurations and video image selection from each EVA helmet is done via a Payload General Support Computer (PGSC) on the flight deck. The Intra-vehicle Activity (IVA) member on the flight deck is reviewing video images and sending helmet camera commands trying to select the best image to observe and help the EVA member during his/her activity.

#### 72.1.1 Purpose

WVS provides video during EVA from the perspective of the EVA crewmember. The WVS allows the ground and orbiter on-board crew to monitor EVA crewmember activity and to assist, as needed, with operations and potential problems that may occur. The WVS will also be used for close-out photo documentation.

#### 72.1.2 General

The WVS is designed to send two separate simultaneous, non-synchronized National Television Standards Committee (NTSC) video signals (each coming from 1 EVA Helmet) to the Orbiter cabin for recording, real-time viewing, or routing of video. The WVS also provides telemetry and status to the orbiter on-board crew and crew control of camera selection and operations. Figure 72-1 is a block diagram representation of the WVS.

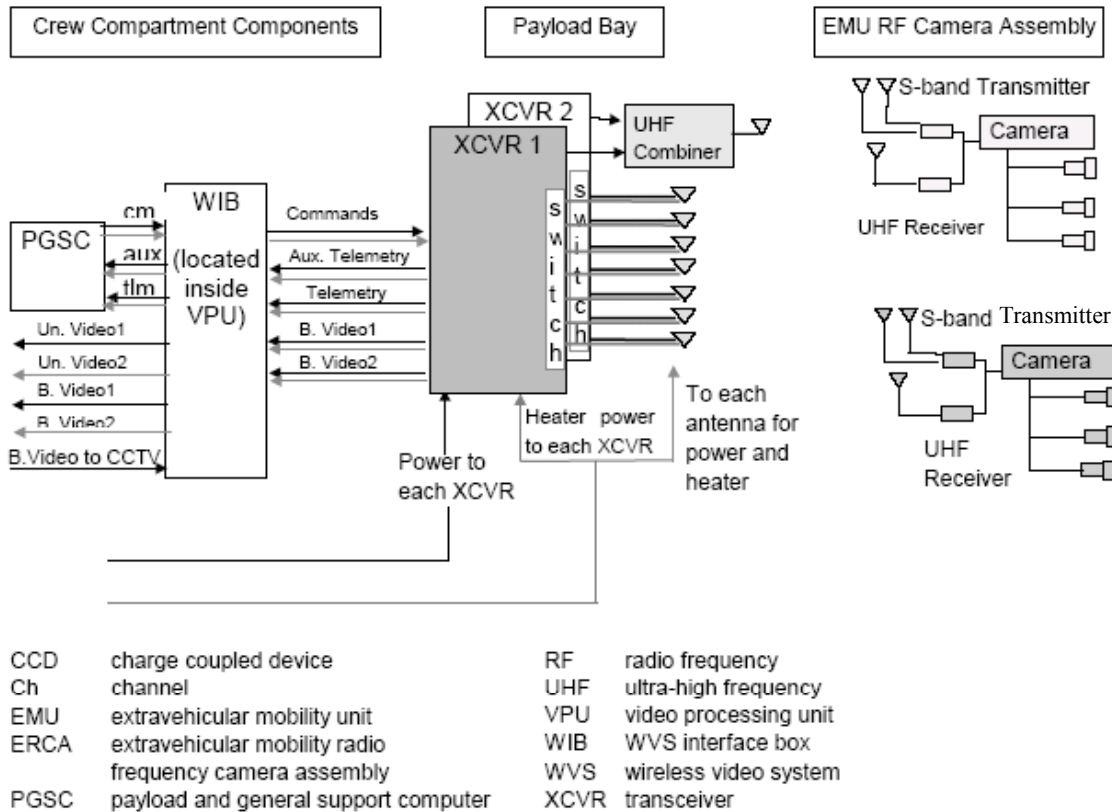
#### 72.1.3 Components

The WVS includes the components described below, and these components are grouped by the following three locations:

- Payload Bay Assembly located in the Payload Bay
- Crew Compartment Assembly located on the Flight Deck
- Extravehicular Mobility Unit Radio Frequency Camera Assembly (ERCA) located on the helmet of the EVA Astronaut

### 72.1.3.1 Payload Bay Assembly

The payload bay assembly serves as the hub of the WVS and is used for all signal routing, i.e., video, command and telemetry. It consists of radio transceivers and antennas.



**Figure 72-1. Overview Block Diagram of the Wireless Video System**

### 72.1.3.2 Crew Compartment Assembly

The crew compartment assembly provides control and monitoring of the performance of the WVS. This assembly is composed of two separate components:

- (1) Wireless Interface Box (WIB)
- (2) PGSC

The WIB is used by the crew for providing control inputs to and receiving video, telemetry, and status from both the payload bay assembly and the ERCA. The PGSC contains the software used for configuration control of the WVS and monitoring of WVS status and telemetry data.

### 72.1.3.3 Extravehicular Mobility Unit Radio Frequency Camera Assembly

The ERCA provides the video input signal for the WVS and accepts commands from the crew compartment assembly. It contains a transmitter/receiver, 3 cameras, an antenna electronics box, and antennas that attach to the EVA Helmet Interchangeable Portable Light assembly (EHIP).

### 72.1.4 Power and Thermal

The transceivers, supported Payload Assembly electronics, and heaters for all seven S-band antennas are powered by MNC MPC3. Control power is CNTL BC1. Note that the WVS transceivers, antennas 1, 2, 3, and 4 (see SSSH 16.12-3 for locations), and antennas 5, 6, and 7 each use a separate Remote Power Controller (RPC). The WIRELESS VIDEO POWER switch on panel A7 controls power to both transceivers (See Figure 72-2). The WIB does not require power since it simply routes signals.

The WIRELESS VIDEO HEATER switch on panel A7 controls power to the transceiver heaters and the S-Band antenna electronics and heaters, which draw a total of 335 Watts. The heater switch will nominally be turned on four hours prior to an EVA and turned off when the EVA is complete. Engineering analysis has shown that 4 hours is sufficient to get the WVS payload bay equipment above operating temperatures. Since the payload bay frequently drops below the antenna minimum non-operating temperature of -85°F, the heaters are required. The heaters are thermostatically controlled thermistors which come on at 70°F and turn off at 81°F. Temperature sensor accuracy is ±5° Celsius [C]. Temperature sensor range is -58° Fahrenheit (F) to 248° F (-50° C to +120° C).

**Table 72-1. Temperature Design Limits for WVS Payload Bay Components**

| Component               | Operating Temperatures                | Non-Operating Temperatures            |
|-------------------------|---------------------------------------|---------------------------------------|
| Payload Bay Transceiver | -31°F to +185°F<br>(-35°C to +85°C)   | -85°F to +257°F<br>(-65°C to +125°C)  |
| S-Band Antenna Array    | -31°F to +185°F<br>(-35°C to +85°C)   | -85°F to +257°F<br>(-65°C to +125°C)  |
| UHF Antenna             | -190°F to +210°F<br>(-123°C to +99°C) | -190°F to +210°F<br>(-123°C to +99°C) |
| UHF Power Combiner      | -75°F to +185°F<br>(-59°C to +85°C)   | -75°F to +220°F<br>(-59°C to +104°C)  |

Table 72-2. WVS Power Usage

| Component             | Power Usage (Watts) |
|-----------------------|---------------------|
| transceiver(2)        | 80 (40 each)        |
| transceiver heater(2) | 90 (45 each)        |
| antenna heaters(7)    | 245 (35 each)       |
| antenna electronics   | 35 (5 each)         |

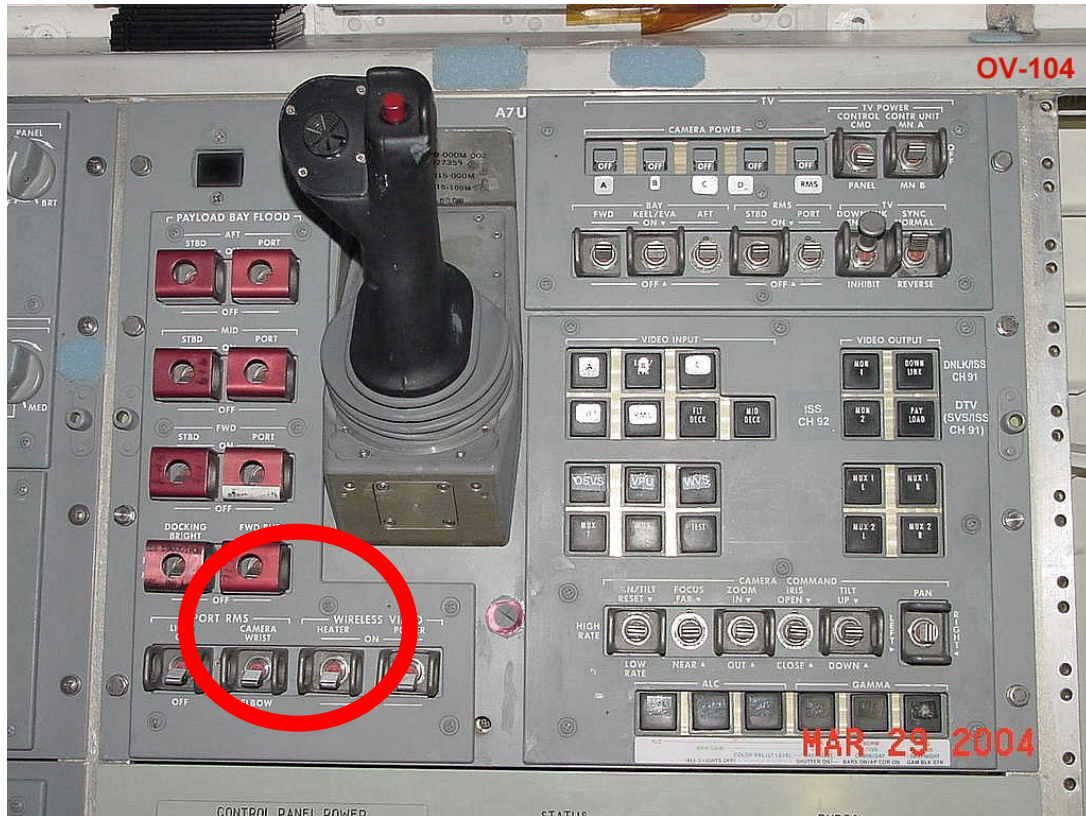


Figure 72-2. Panel A7U-WVS Power and Heater Control

## 72.1.5 Electrical Characteristics and Performance

### 72.1.5.1 Operational Frequencies

The WVS center frequency for S-band video and telemetry transmission is commandable to one of two frequencies. High frequency is 2.47 GHz and low frequency is 2.41 GHz, ±16 MHz. The frequency for UHF command transmission is 400.2 MHz, ±100 kHz.

### 72.1.5.2 Video

The WVS provides two simultaneous asynchronous video signals to the WIB for display and routing purposes.

#### **72.1.5.2.1 Video Range and Link Margin**

The WVS supports RF video between the orbiter and up to two simultaneous ERCA units out to a range of 300 feet, direct line of sight. The link margin of the WVS RF video at the range of 300 feet is at least 3 dB, direct line of sight.

#### **72.1.5.2.2 Data Latency–Acquisition and Reacquisition**

Command data latency added by the WVS does not exceed 3 seconds including the range delay at the maximum range specified. The WVS acquisition and reacquisition time is less than 10 seconds excluding effects of RF interference, blockage, and multi-path. A phased loop lock (PLL) acquisition circuit is used.

#### **72.1.5.3 Command**

The WVS accepts configuration commands from the PGSC for control of both the payload bay assembly and ERCAs. The commands to the ERCAs are transmitted via the UHF communications link. See Table 72-2 for a list of commands. The data rate of the command link is 9600 bps.

The WVS can support an RF command link out to a range of 300 feet, direct line of sight. The link margin of the WVS RF command link at the range of 300 feet is at least 3 dB, direct line of sight.

#### **72.1.5.4 Telemetry**

The WVS provides operational telemetry data via PGSC to the crew for display and monitoring.

The WVS telemetry (TLM) link consists of four separate channels. There are two channels from each payload bay assembly transceiver. The two telemetry channels from each payload bay assembly transceiver consist of one channel for WVS telemetry and the other for auxiliary data. The channel data rate of each of the four telemetry links is 9600 bps.

### **72.2 PAYLOAD BAY ASSEMBLY**

#### **72.2.1 Purpose**

The Payload Bay Assembly acts as the hub of the WVS system. All video, command, telemetry routing, and signal conditioning are provided by this assembly.

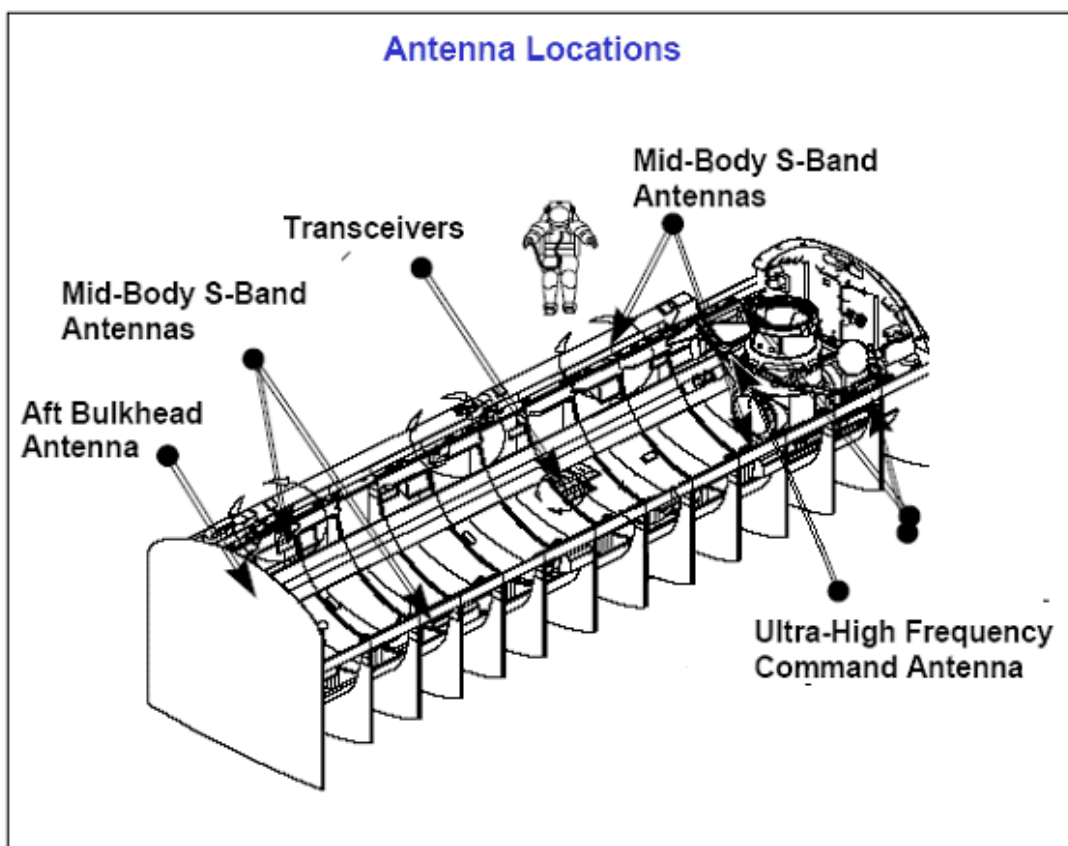
#### **72.2.2 General**

The Payload Bay Assembly receives ERCA video and telemetry from an antenna array. It processes the telemetry for display on the PGSC. The payload bay assembly also receives commands from the PGSCs and routes them to the ERCA for configuration control and processes telemetry for use by the crew on-board the orbiter. Figure 72-3 shows the standard locations of the antennas and 72-4 is a high level representation of the interfaces to the transceivers.

### 72.2.3 Components

The Payload Bay Assembly consists of the following components:

- Payload Bay Transceiver
  - S-Band Receiver
  - Antenna Selection Processor
  - Command Processor
  - UHF Transmitter
- S-Band Antenna Array
- UHF Antenna
- UHF Power Combiner



**Figure 72-3. Payload Bay Assembly, Antennas**

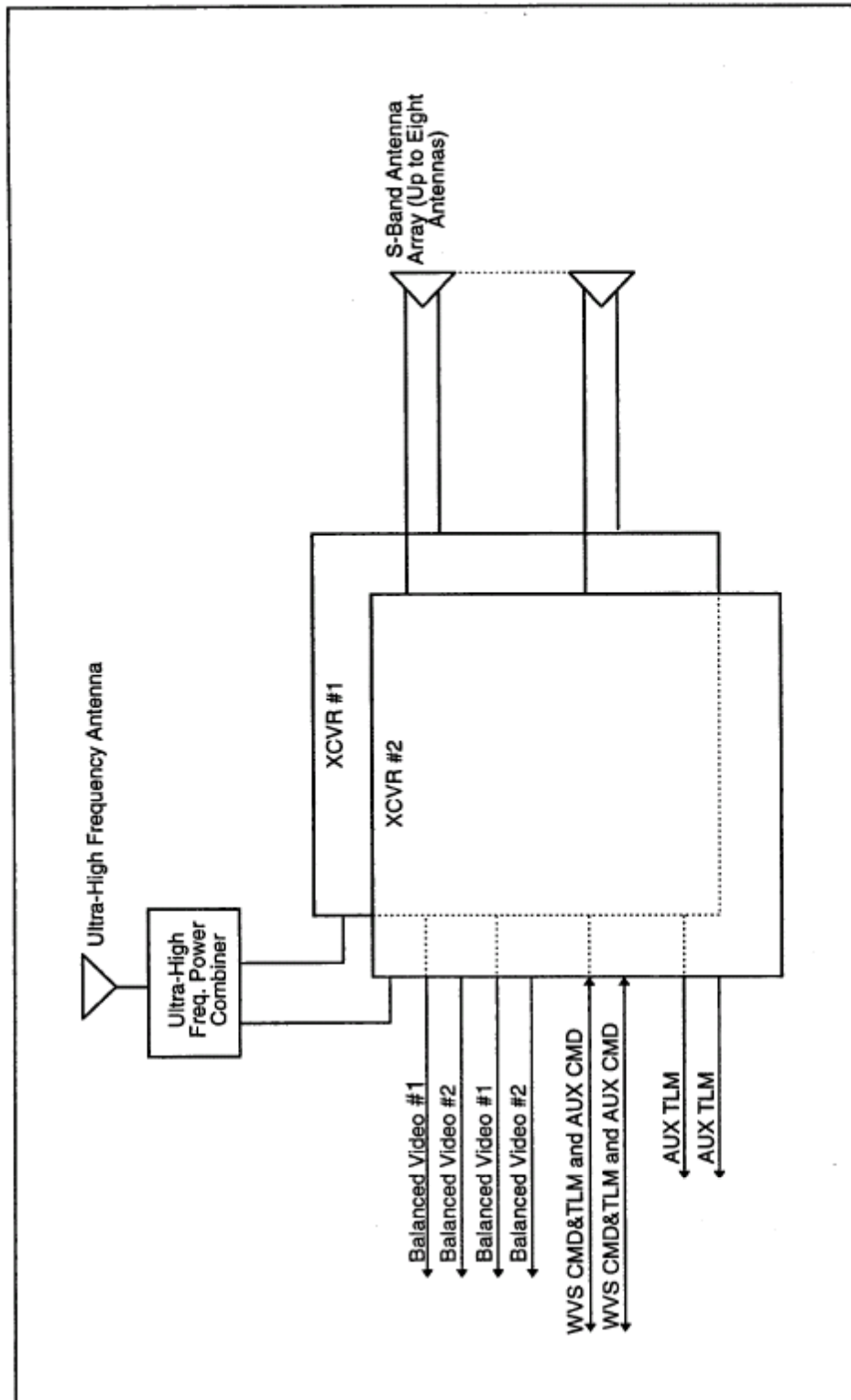


Figure 72-4. Block Diagram of the Payload Assembly



### **72.2.3.1 S-Band Antenna Array**

The S-band antenna array receives video and telemetry from the ERCAs. A 2 MHz switching pulse is provided to the S-band antenna array on the coaxial cable from the antenna selection processor. All antennas are calibrated to have the same signal losses over the connecting cable as the one with the longest cable to avoid attenuation problems. Nominally, seven S-Band antennas are installed, although up to eight can be. Each antenna is comprised of four patch antennas.

### **72.2.3.2 Payload Bay Transceiver**

#### **72.2.3.2.1 S-Band Receiver**

The S-band receiver receives and demodulates video and telemetry received from the ERCA via the S-band antennas. The S-band receiver also executes commands received from the command processor. It is commandable to high frequency or low frequency. The S-band receiver outputs two asynchronous balanced NTSC video signals that are compatible with the Space Shuttle's closed circuit television (CCTV) system as defined in Revision B of the Shuttle Orbiter CCTV System Interface Control Document (ICD-3-00050-01). When no RF TV signal is detected, the receiver will output a "blue screen".

#### **72.2.3.2.2 Antenna Selection Processor**

During the video blanking interval, the antenna selection algorithm seeks the strongest RF signal from all 32 patch antennas (only 28 actually installed). The antenna selection algorithm has auto and manual modes. The auto mode allows automatic switching between each element of each of the antenna quads, and selects the antenna with the strongest RF signal. The MANUAL mode causes the system to select a quad antenna, as commanded, around the eight quad units. AUTO mode is the default mode of operation. The PGSC can show all 64 antenna paths (8 antennas x 4 patches x 2 transceivers).

#### **72.2.3.2.3 Command Processor**

The command processor receives telemetry data from the S-band receiver, antenna selection processor, and the UHF transmitter. The command processor extracts embedded telemetry from the ERCA video link. It combines the two signals and transmits them via RS422 serial data link to the WIB. It also accepts commands from the WIB via an RS422 serial communications link. The command processor routes received commands to the S-band receiver, antenna selection processor, and UHF transmitter. It controls the ON-OFF power to the UHF transmitter.

#### 72.2.3.2.4 Ultra-High Frequency Transmitter

The UHF transmitter receives commands from the command processor and transmits them to the ERCA. The UHF system uses Gaussian Minimum Shift Keying (GMSK) modulation. The transmitter power is 500 mW and it operates at 400.2 MHz at a data rate of 9600 bps with an 11.34kHz bandwidth.

#### 72.2.3.3 Ultra-High Frequency Antenna and Frequency Power Combiner

There is a single UHF antenna which transmits commands to the ERCA.

The UHF power combiner combines the signals from the two coaxial cables connected to the UHF transmitters into a single cable to be connected to the UHF antenna.

### 72.3 CREW COMPARTMENT ASSEMBLY

#### 72.3.1 Purpose

The crew compartment assembly provides for configuration control, performance monitoring, and signal routing for the payload bay assembly.

#### 72.3.2 General

The crew compartment assembly consists the WIB and a PGSC. RS422 cables are used to connect the PGSC to the WIB. The WIB provides a common interface between the payload bay assembly, the CCTV system, and the PGSC. The PGSC collects telemetry from and routes commands to the payload bay assembly. Figure 72-5 is a line drawing of the WIB.



**Figure 72-5. Wireless Video System Interface Box**

### 72.3.3 Components

The crew compartment assembly consists of the following components:

- WIB integrated into the VPU
- PGSC with WVS control and monitoring software installed
- RS422 interconnecting cables
- Cables to route transceiver video to the CCTV system

#### 72.3.3.1 Wireless Video System Interface Box

The WIB provides routing of four separate video signals from the payload bay assembly (refer to Figure 72-5). The WIB can convert one balanced video signal per transceiver into an unbalanced NTSC video signal. The WIB provides two RS422 communications ports for routing telemetry and commands between the payload bay assembly and the PGSC. It also provides routing for two RS422 communications ports for auxiliary telemetry data from the payload bay assembly. The WIB provides an interface for routing WVS video signals to the orbiter CCTV system via the VPU.

#### 72.3.3.2 Software

The WVS control and monitoring software can be loaded on a PGSC with two RS422 full duplex communications ports. The software has a graphical user interface (GUI). The crew can use the GUI to configure all WVS components via the RS422 command communications link. The GUI sends commands to the active transceiver's RS422 communications port. The GUI will only allow one transceiver to be on at a time. The GUI receives telemetry from both payload bay assembly transceivers and displays the data for crew use in accordance with the *Wireless Video System Software Requirements Document* (JSC28411) or the web address:

[http://www4.jsc.nasa.gov/eaprojects/ea-projects/flightgfe/WVS\\_Shuttle/Documents/Pre-Released/JSC28446.doc](http://www4.jsc.nasa.gov/eaprojects/ea-projects/flightgfe/WVS_Shuttle/Documents/Pre-Released/JSC28446.doc)

The displays available are:

- Top Status area (available at the top of each page)
- EMU Page (Figure 72-6)
- Transceiver Page (Figure 72-7)
- Telemetry Page (Figure 72-8)

These displays allow the crewmember to send the commands listed in Table 72-1 and to observe telemetry on the WVS system.

### 72.3.3.2.1 Top Status Area (Figures 72-6, 72-7, and 72-8)

The top status area is available at the top of the EMU, transceiver, and telemetry pages. It shows the following:

**RF Camera Status** (ON (green), OFF (black)) - RF camera power status changes to ON when a camera is selected in the pull down menu.

**RF Camera Pull Down Menu** - Assigns an ERCA to the respective transceiver. This will send a command to turn the camera electronics and the selected lens on. If an ERCA is selected to a transceiver when it is already assigned to the other transceiver, then the assignments will be swapped.

**Command Power: Level Status** (ON/OFF) - Denotes which transceiver is configured to process commands and the command level (min/max)

**Frequency Status/Command** (high/low) - Displays the frequency selected to each transceiver. Since the transceivers will always operate on different frequencies, swapping frequency assignment to one transceiver will also assign the alternate frequency to the other transceiver. Selecting this button will send a command to swap the frequency assignments. This is the easiest way to swap video coming out of the WIB connectors.

**Lens Select Command** (L/C/R) - Displays which camera is selected for each ERCA. Selecting a different one will send a command to change the camera assignment. Default is center.

**Alert Message Display** - Displays error messages. New messages will flash in blue until the button is pressed to acknowledge it. The "Temp Caution" message will flash in yellow. The messages will disappear when the problem is fixed. Highest priority messages are displayed first. If more than one message occurs, clicking the button will cycle through the messages. Once they are all acknowledged only the highest priority message can be viewed. Possible messages are:

- Static XCVR - Loss of comm between the PGSC and transceiver
- Static RF Camera - Loss of comm between the transceiver and camera
- Bad Camera ID - Mismatch between camera selected and transmitting camera
- Temp Alert - Camera or transceiver is within 5° of its caution range (ERCA = -35° to -30°C or 80° to 85°C, XCVR = -40° to -35°C or 80° to 85°C)
- Temp Caution - Camera or Transceiver has gone out of limits (ERCA < -35° or > 85°C, XCVR < -40° or > 85°C)

**Select Page** - Selects which display to show in the lower portion of the screen (RF Camera, Telemetry, and XCVR)

### 72.3.3.2.2 RF Camera Display (Figure 72-6)

**Lens Iris Control** - Opens or closes the iris for the selected lens. There is no telemetry other than the video.

**Electronic Shutter Control** (Auto/Manual) - Selects auto or manual shutter control. If manual is selected, brightness control buttons enable the user to increase or decrease the electronic shutter speed (1 to 100) for a darker or brighter image. Initial value is 50.

**White Balance Control** (auto, 6100K, 2800K, and variable) - Sets white balance for the selected camera. If variable is selected, the user can increase or decrease the blue or red gain on a scale from 1 to 100 (initial values are 50).

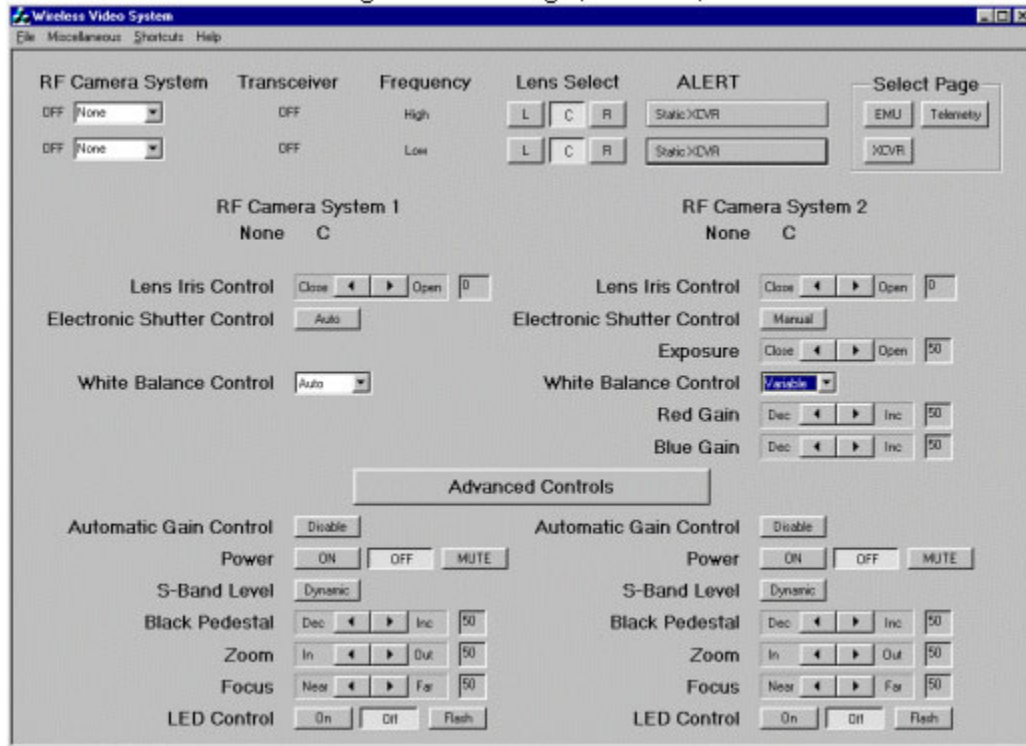
**Automatic Gain Control** (Enabled/Disabled) - Enables or Disables AGC. Default is disabled. It may need to be enabled for dark subjects. It must be selected for viewing in advanced controls.

**Power Status** (ON/OFF/MUTE) - Shows the status of the ERCA transmitter. Selected one of the buttons will send a command. The ERCA transmitter can also be turned on and off with the RF Camera pull down menu. Mute leaves the ERCA powered, but inhibits video transmission. It must be selected for viewing in advanced controls.

**S-Band Level** (Dynamic/Maximum) - Dynamic mode (default) will adjust the S-Band power level per the received signal strength (adjusted to be received at -40dB). Maximum mode will set the power level at the maximum regardless of signal strength. It must be selected for viewing in advanced controls.

**Black Pedestal** - Not Used. Adjusts brightness control from 0 to 100. It must be selected for viewing in advanced controls.

**Zoom, Focus, LED Control** - Not used; capabilities do not exist. It must be selected for viewing in advanced controls.



**Figure 72-6. PGSC RF Camera Page**

### 72.3.3.2.3 Transceiver Page (Figure 72-7)

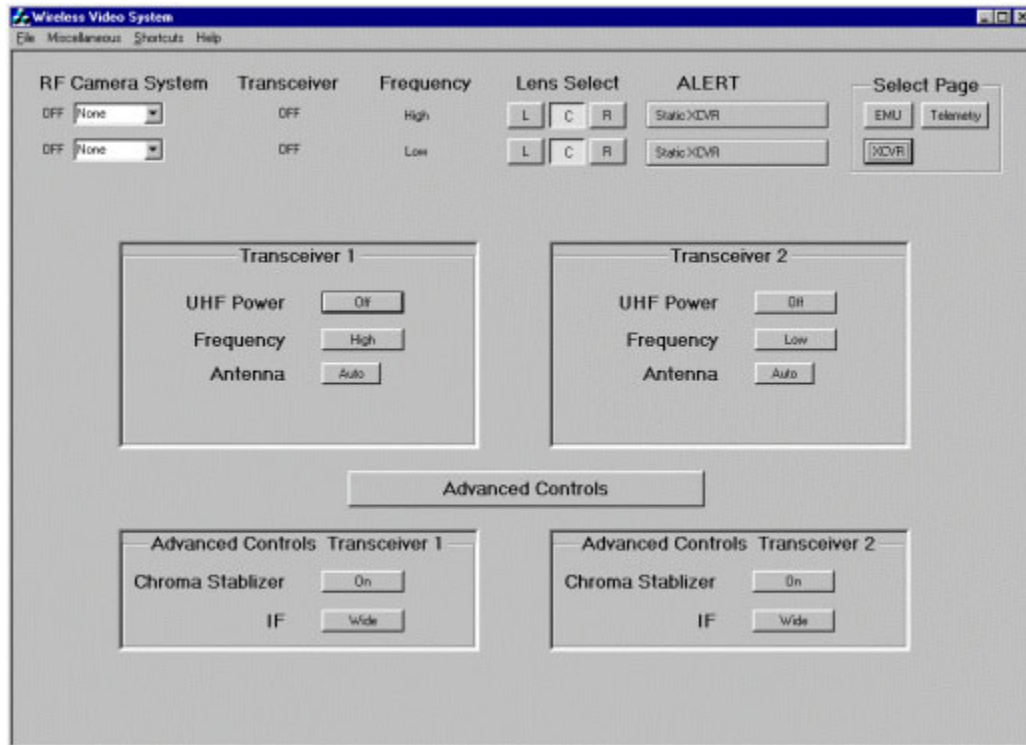
**CMD Power** (Off/On) - Clicking this button will turn on or off the associated transceiver command processor. Transceiver 1 and 2 selections are mutually exclusive and an On command will automatically turn the other Off. The status is also shown in the top status area under CMD PWR:LVL

**Antenna** (Auto/Manual) - Selects the antenna selection method. Auto (default) will automatically select the best antenna based on signal strength. In Manual, a drop down menu will appear that allows the user to select one of eight antennas. The antenna numbering sequence is shown on the WVS cue card.

**Chroma Stabilizer** - Not used. It must be selected for viewing in advanced controls.

**Intermediate Frequency (IF)** (Wide/Narrow) - Controls the bandwidth sampled for the RF Camera return signal. Typically changed to narrow for signal strength troubleshooting. It must be selected for viewing in advanced controls.

**CMD Level** (Max/Min) - Not used with the new spread spectrum transceivers. The status is shown in the top status area under CMD PWR:LVL. It must be selected for viewing in advanced controls.



**Figure 72-7. PGSC WVS Transceiver Page**

#### 72.3.3.2.4 Telemetry Page (Figure 72-8)

**RF Camera** (user defined) - Displays the current RF Camera title

**Lens** (L,C,R) - Displays the currently selected lens

**UHF Signal Strength** (nominally -120 to -59) - Displays command link signal in dB seen at the selected camera.

**UHF RX Good** - Not used

**Pwr Voltage** (nominally 12.8) - Displays RF camera system voltage

**Pwr Amperes** (nominally 0.40) - Displays RF camera system current

**Temperature Electronics** (nominally 13 to 30) - Displays the temperature of the RF camera electronics in deg C.

**Temperature L,C,R** (nominally 0 to 33) - Displays the temperature of each lens in deg C.

**XCVR 1,2 Temperature** (nominally 18 to 37) - Displays the transceiver temperature in deg C.

**S-Band Signal Strength** (nominally 97.5 to -10.5) - Displays the return signal strength seen at the transceiver in dB.

**S-Band Antenna Select** - Displays which S-Band antenna the transceiver is using to get a video signal.

**S-Band Antenna Mode** (Auto, Manual) - Displays transceiver antenna selection mode.

**Power Voltage** (nominally 12.42) - Displays transceiver system voltage.

**Power Amperes** (nominally 1.10) - Displays transceiver system current.

**Quads 1,2** - Displays the current signal strength of the strongest antenna quad for each antenna at each transceiver in dB.

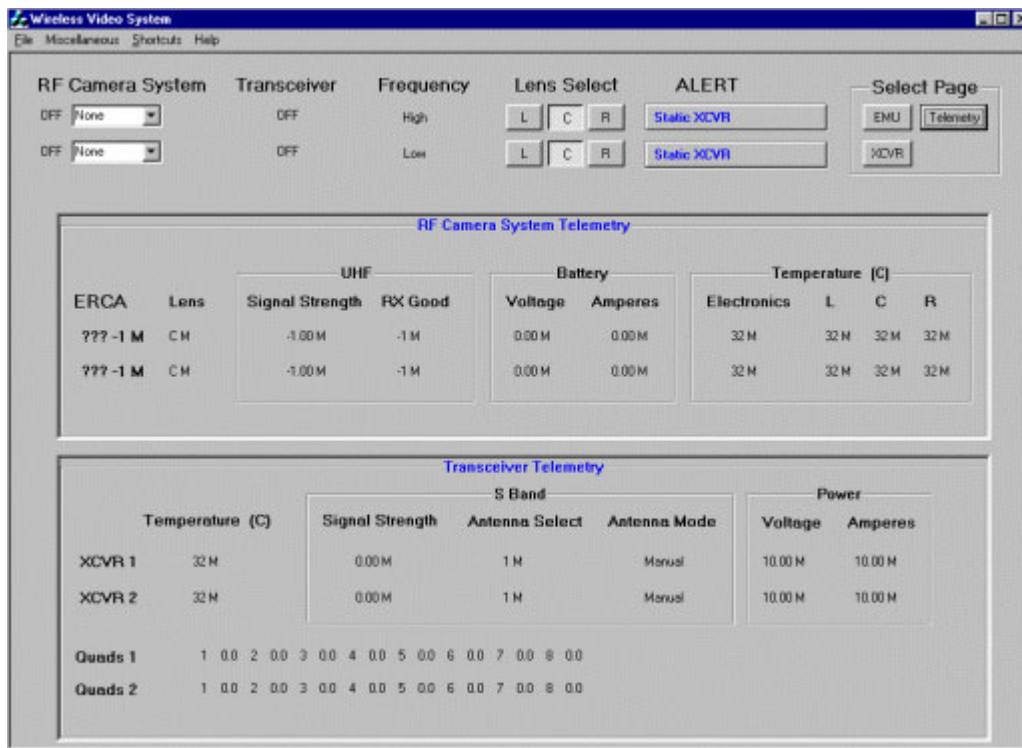


Figure 72-8. PGSC Telemetry Page

### 72.3.3.3 Command

The Crew Compartment Assembly provides control via command to the Payload Bay Assembly and ERCA over an RS422 command link. The RS422 command link includes commands defined in Table 72-2. Table 72-2 provides a complete list of the Payload Bay Assembly and ERCA commands.



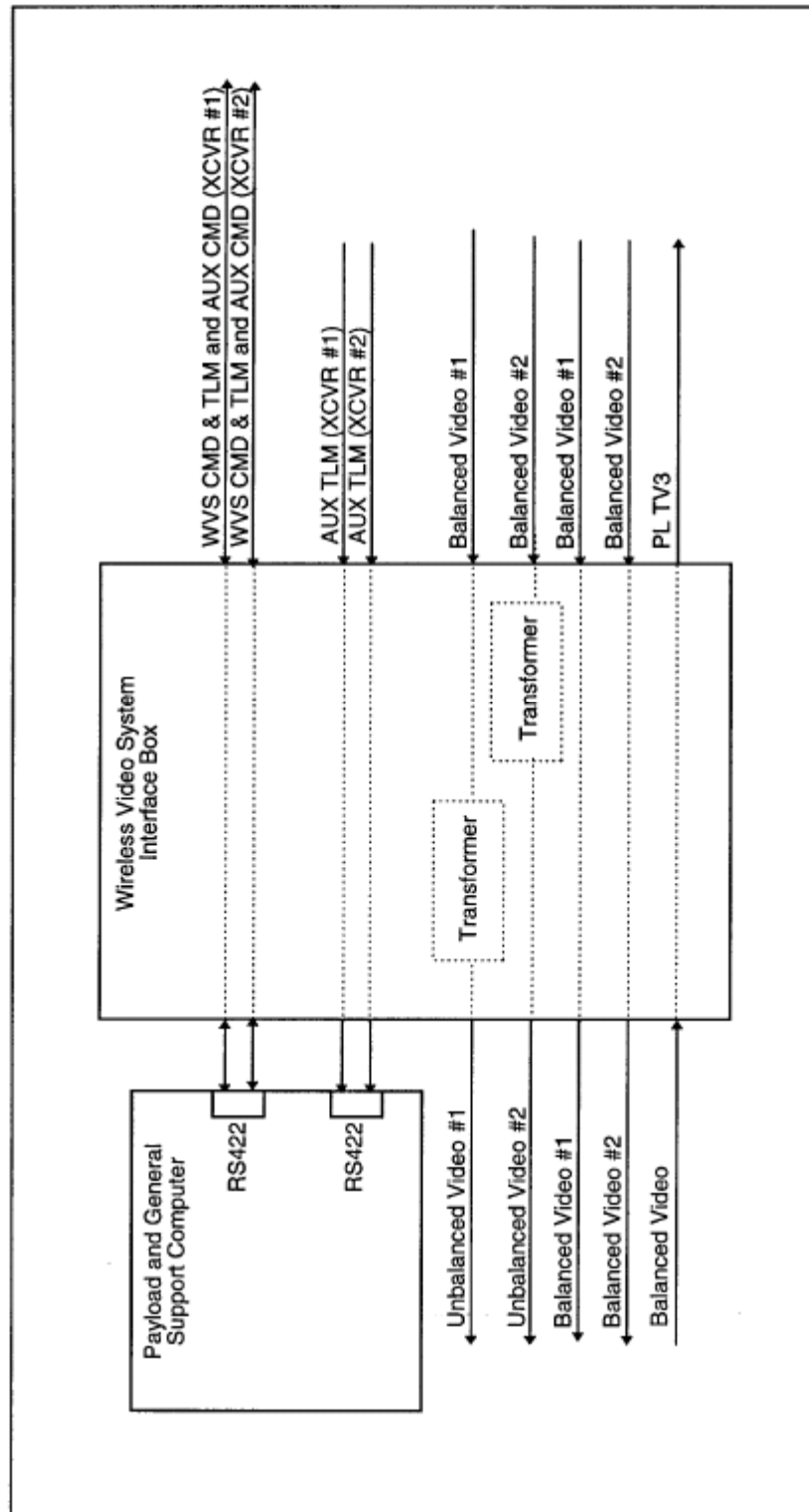


Figure 72-9. Block Diagram of the WVS Interface Box

**Table 72-3. WVS Command Processing Requirements**

| Component Module     | Command   |
|----------------------|---|
| Payload Bay Assembly | S-Band Receiver 1 Frequency Select (HIGH-LOW)                                     |
|                      | S-Band Receiver 2 Frequency Select (HIGH-LOW)                                     |
|                      | S-Band Receiver 1 Antenna Selection Processor Control (AUTO-MANUAL)               |
|                      | S-Band Receiver 2 Antenna Selection Processor Control (AUTO-MANUAL)               |
|                      | S-Band Quad Antenna Select (1,2,3,4,5,6,7,8)                                      |
|                      | UHF Transmitter 1 (ON-OFF)  |
|                      | UHF Transmitter 2 (ON-OFF)  |
| ERCA*                | S-Band Transmitter (ON-OFF)   |
|                      | S-Band Transmitter Frequency Select (HIGH-LOW)                                    |
|                      | Lens Select (Modes: 1, 2, 3)  |
|                      | Lens Mechanical Iris Control (Modes: OPEN, CLOSE)                                 |
|                      | Light-Emitting Diode (LED) Assembly Control (Modes: ON, OFF, FLASH) (not used)    |
|                      | White Balance Control (Modes: 2800K, 6100K, and Auto Tracing White Balance [ATW]) |
|                      | Electronic Shutter Control (Modes: AUTOMATIC, MANUAL [OPEN, CLOSE])               |
|                      | Focus (not used)  |
|                      | Zoom (not used)   |
|                      | Auxiliary (AUX) Commands  |

\* ERCA commands include a camera identification. The camera identification is used for command authentication.

**72.3.3.4 Commanded Configuration and Telemetry**

The Crew Compartment Assembly displays the commanded configuration and receives and display telemetry from the Payload Bay Assembly and ERCA via an RS422 telemetry link as defined in Tables 72-2 and 72-3.

**Table 72-4. Commanded Configuration**

| <b>Component Module</b>          | <b>Commanded Configuration</b>                 |
|----------------------------------|--|
| Payload Bay Assembly (COMMANDED) | S-Band Receiver Frequency (1,2)                |
|                                  | (HIGH, LOW)                                    |
| ERCA (COMMANDED)                 | S-Band Transmitter (1,2) (ON, OFF)             |
|                                  | S-Band Transmitter Frequency (1,2) (HIGH, LOW) |

\* The commanded configuration is simply a loop back internal to the PGSC that displays the latest configuration (for example, the frequency displayed is just the last commanded frequency).

**Table 72-5. WVS Telemetry**

| <b>Component Module</b>          | <b>Commanded Configuration</b>   |
|----------------------------------|--|
| Payload Bay Assembly (TELEMETRY) | Antenna Selection Processor Mode (1,2) (AUTO, MANUAL)  |
|                                  | UHF Transmitter (1, 2) (ON,OFF)  |
|                                  | Payload Bay Transceiver (1, 2) (Temperature)   |
|                                  | S-Band Receiver (1, 2) (Signal Strength), -80 to 0.0 dB referenced to one milliwatt, ±0.5 dB |
|                                  | S-Band Selected Quad Antenna (1, 2, 3, 4, 5, 6, 7, 8)  |
| ERCA (TELEMETRY)                 | Camera Identification (Numbers 0-256)  |
|                                  | Lens Select (1, 2) (1, 2, 3)   |
|                                  | White Balance (1,2) (2800K, 6100K, ATW)  |
|                                  | Electronic Shutter (1,2) (AUTO, MANUAL)  |
|                                  | ERCA Temperatures (1,2) (Three Temperature Readings)   |
|                                  | Auxiliary Data Port Telemetry (1,2)  |

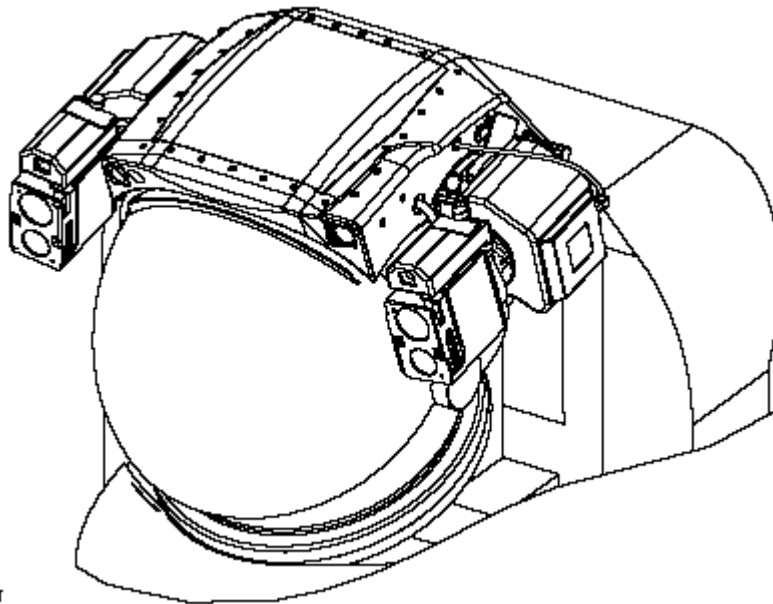
## 72.4 EXTRAVEHICULAR MOBILITY UNIT RADIO FREQUENCY CAMERA ASSEMBLY (ERCA)

### 72.4.1 Purpose

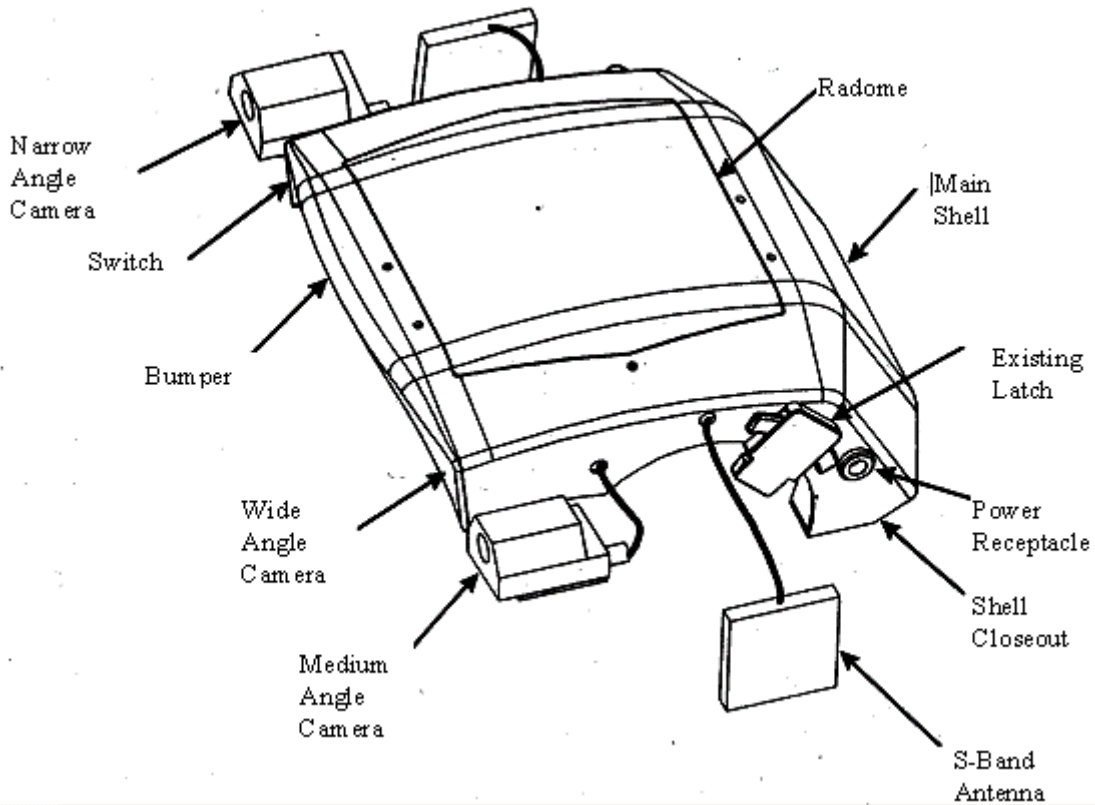
The ERCA provides a source of NTSC video, from the EVA member's point-of-view, to the orbiter during EVA operations.

### 72.4.2 General

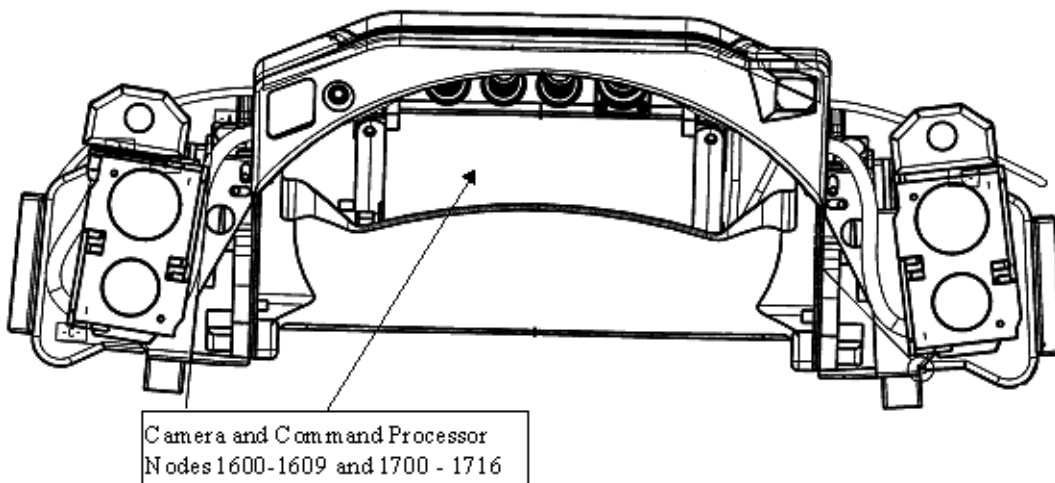
The ERCA components are integrated onto the EHIP assembly and are used to capture video images which are transmitted to the payload bay assembly. The ERCA also receives and processes commands from the Space Shuttle payload bay assembly. Figure 72-14 is a block diagram of the ERCA. The ERCA is based on the commercially available Sony model XC-999 video camera. Each ERCA system has its own unique address. The ERCA provides a single video signal with associated telemetry to the S-band transmitter and a single baseband unbalanced video signal of selected CCD and lens assembly to the video port. It accepts and processes configuration commands. The ERCA is powered by the Rechargeable EVA Battery Assembly.



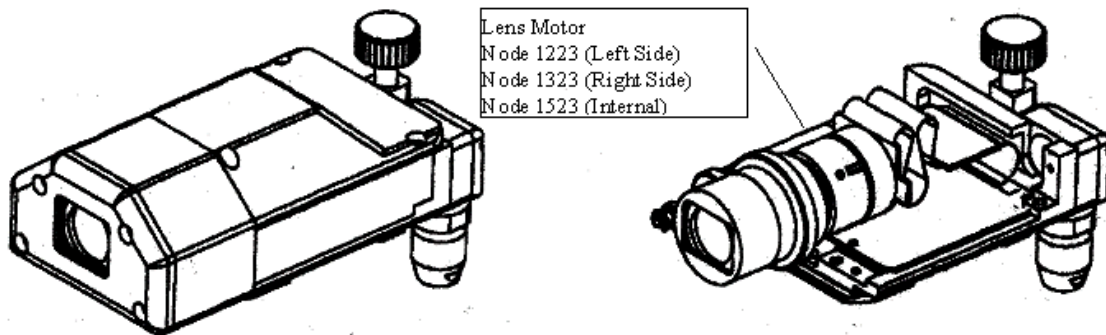
*Figure 72-10. Isometric View of ERCA*



**Figure 72-11. ERCA Component Location**



**Figure 72-12. ERCA Camera and Command Processor**



*Figure 72-13. ERCA Cameras - Isometric Views*

### 72.4.3 Components

The ERCA consists of the following components:

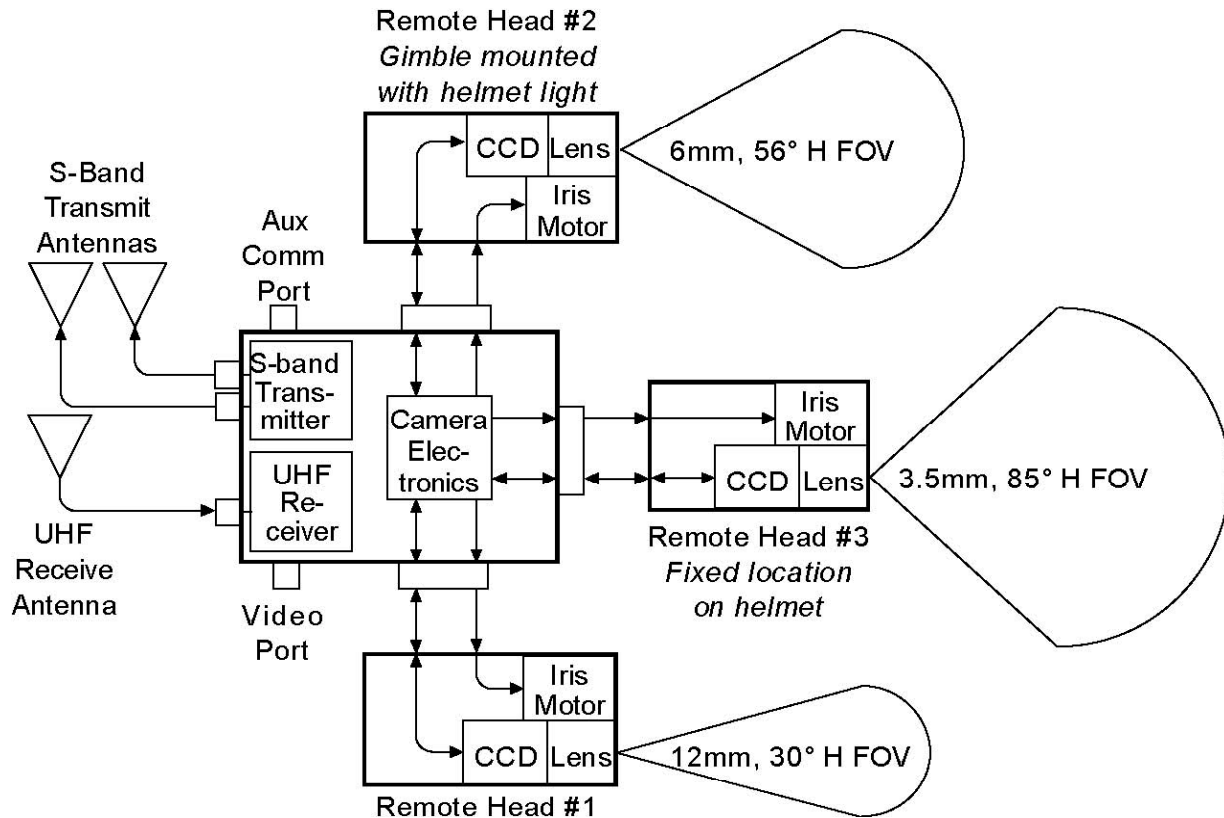
- RF Camera Electronics
  - Camera Electronics
  - S-Band Transmitter
  - UHF Receiver
- CCD and Lens Assemblies (3)
- S-Band Antennas (2)
- UHF Antenna
- Housing
- Mounting Hardware
- Cables

#### 72.4.3.1 Radio Frequency Camera Electronics

The RF camera electronics distributes power to the other ERCA subsystems as well as routing commands and telemetry

##### 72.4.3.1.1 Camera Electronics (Command Definition)

The camera electronics will route commands to the CCD and lens assembly, the S-band transmitter, the auxiliary communications port, and the external power subsystems. The camera electronics will receive commands from the UHF receiver. The following definitions are for user interface commands.



CCD charge coupled device  
H FOV horizontal field of view  
mm millimeter  
UHF ultra-high frequency

**Figure 72-14. Extravehicular Mobility Unit Radio Frequency Camera Assembly**

#### 72.4.3.1.1.1 Camera System Standby Mode

The camera system standby mode powers off the S-band transmitter. The UHF receiver and camera electronics will continue to accept and process commands while in standby mode.

#### 72.4.3.1.1.2 Camera Electronic Shutter Control

The camera electronic shutter control system receives commands to control the camera's electronic shutter speed and mode of operation. The camera electronic shutter control system operates in, automatic or manual mode. In automatic mode the camera electronic shutter control will automatically adjust the electronic shutter speed based on its internal sensing of the lighting conditions in the scene. In manual mode it will specify a percentage of maximum electronic shutter speed. In the manual mode the two electronic shutter control commands are open and close. Automatic is the default mode of operation.

#### **72.4.3.1.1.3 Lens Mechanical Iris Control**

The lens mechanical iris control system receives commands to control the motor that opens and closes the diaphragm of the lens' iris. The lens mechanical iris control command specifies a direction and percentage of maximum iris motor speed. The iris motor runs at the specified percentage speed for up to 150 msec. The motor stops if either 150 msec. has elapsed since the last lens mechanical iris control command or the mechanical iris is fully opened (or closed). The mechanical lens iris control commands are open and close. There is no automatic iris control, it must be manually commanded.

#### **72.4.3.1.1.4 White Balance Control**

The white balance control system receives commands to control four modes for white balance, 2800K, 6100K, ATW, and variable. 2800K is meant for night operations with the payload bay lights, 6100K is meant for sunlight operations. ATW mode will automatically adjust the white balance according to lighting conditions. Variable mode allows manual adjusting of the red and blue gain.

#### **72.4.3.1.1.5 Auxiliary Port Commands**

The auxiliary port receives commands to control the device attached to the auxiliary port. This port is meant to provide telemetry on a second subcarrier from a different type of camera. It is not used.

#### **72.4.3.1.1.6 Sleep Mode**

The sleep circuit is a feature that is enabled by use of the jumper or the dual in-line package switch. The sleep circuit exists to conserve battery power. It is a low power consumption circuit that consists of a timer that will periodically power up the camera's UHF data receiver and associated electronics for one (1) second in an attempt to detect the presence of the UHF command link from the transceiver. If the command link is detected, the microprocessor will also be powered up and the UHF receiver will remain active until the camera is remotely commanded off or the loss of the command link is detected. Loss of the command link is defined as a drop in the carrier level below a threshold level of valid command data packets. After carrier loss, the UHF receiver will remain powered on for a period of ten minutes, then the receiver will be powered off. If the command link is not present at wake-up, the unit will remain powered down for sixty seconds after which time the cycle repeats. Upon receipt of a camera power-up command with the appropriate address, the control subsystem will power-on the camera subsystems. The sleep mode is disabled for the ERCA and it is not used.

#### **72.4.3.1.1.7 Transmitter Control**

Upon receipt of a transmitter OFF command, the S-band transmitter will transition to the standby state. Upon receipt of a transmitter ON command, the S-band transmitter will transition to the active state.



#### **72.4.3.1.1.8 Lens Select**

Video sources from the 3 CCD and lens assemblies are selectable via command. The commands are left, right, or center.

#### **72.4.3.1.2 Camera Electronics (Telemetry Definition)**

The camera electronics receives telemetry from temperature sensors. There are provisions for at least three temperature sensors. One sensor is located in the camera's main electronics housing. The other sensors are remotely mounted. Temperature sensor accuracy is be  $\pm 5^{\circ}$  C. Temperature sensor range is  $-67^{\circ}$  F to  $+257^{\circ}$  F ( $-55^{\circ}$  C to  $+125^{\circ}$  C) for camera electronics. A unique camera identification is transmitted as part of the camera's telemetry data stream. Data or telemetry received from the auxiliary communications port is routed to the camera electronics. The camera electronics routes received telemetry data and camera identification to the S-band transmitter. The auxiliary port connection to the camera electronics is RS-422 compatible.

#### **72.4.3.1.3 S-Band Transmitter**

The S-band transmitter receives video from the camera electronics and telemetry and auxiliary data from the camera electronics. The S-band transmitter creates and transmits a composite video and telemetry signal where the telemetry signals are in two sub-carriers. Sub-carrier #1 contains ERCA telemetry and sub-carrier #2 contains auxiliary telemetry (not used). The subcarrier frequencies are 5.8 and 6.2 MHz respectively and have a data rate of 9.6 kbps. The power output is 250 mW (125 mW for each antenna).

#### **72.4.3.1.4 Ultra-High Frequency Receiver**

The UHF receiver receives commands via the UHF RF command link and routes these commands to the camera electronics system.

#### **72.4.3.2 Charge Coupled Device Lens Assembly**

The RF camera includes three CCD and lens assemblies that interface with the camera electronics. The 3.5 mm CCD and lens assembly is installed in the ERCA housing. One CCD and lens assembly (6 mm or 12 mm) is mounted on each of the two EHIP lights. Each CCD and lens assembly are separately packaged and remotely attached to the remainder of the video camera electronics. Each CCD and lens assembly includes a motor drive to allow remote control of the lens iris diaphragm. The CCD and lens assembly iris motor are compatible for use in high oxygen, low pressure as well as vacuum environments. The CCD and lens assembly provide a minimum field of view of 30 degrees horizontal, 23 degrees vertical and 37 degrees diagonal. It provides viewing capability where objects are in focus for a minimum range of 12.0 inches to 25 feet away from the camera in sunlight and dark environments. The CCD lens assembly is capable of utilizing future lenses developed for the Sony XC-999 camera.

### **72.4.3.3 S-Band Antennas**

The S-band antennas are usable over at least  $\pm 90$  degrees when attached to the ERCA. Axial ratio for the S-band antennas is less than or equal to 10 dB. There are two S-band antennas attached to the ERCA. They are attached to either side of the EVA helmet just behind the side mounted cameras. Both antennas continuously transmit when powered on.

### **72.4.3.4 Ultra-High Frequency Antenna**

The UHF antenna is usable over at least  $\pm 100$  degrees when attached to the ERCA. Axial ratio for the UHF antenna is less than or equal to 10 dB. There is a single UHF patch antenna located on the top forward section of the EVA helmet.

### **72.4.3.5 ERCA Housing**

The ERCA housing is a single assembly that contains the RF camera, one CCD and lens assembly, and the S-band and UHF antennas. The ERCA housing and CCD and lens assemblies can be attached or removed from the EHIP lights during intravehicular activity. Power to the ERCA is provided via an interface to the EMU power harness. The ERCA provides an EVA single-gloved hand operable on-off power switch which is accessible to the EVA crew member who is carrying the ERCA. The ERCA provides a capability for single-gloved hand manual pointing on the cameras mounted on the EHIP lights by the EVA crew member who is carrying the ERCA. The ERCA meets requirements for stowage in a middeck locker. It can recover from single-event, non-fatal interrupts by cycling power.

## **72.5 ANOMALIES AND IDIOSYNCRASIES**

- During radiation testing, transceivers have experienced single-event upsets. In each case, a soft reset (turning the transceiver off and then on by command from the PGSC) or a hard reset (actually cycling power using the circuit breaker) recovered.
- An older version of the transceivers would occasionally stop communicating with the PGSC. The problem has not occurred on the current transceivers.

## **72.6 REFERENCES**

Wireless Video System Design Requirements Document, October 2000

STS-114 Photo/TV Checklist, Basis, August 2004

WVS PGSC display, version 1.3

THIS PAGE INTENTIONALLY BLANK

## SECTION 73 - SHUTTLE IN-CABIN VIDEO EQUIPMENT

### CONTENTS

| Section | Page   |
|---------|--|
| 73.1    | INTRODUCTION..... 73-1                                       |
| 73.2    | GENERAL USE CABLES..... 73-1                                 |
| 73.2.1  | TV Power Cable ..... 73-1                                    |
| 73.2.2  | Pigmy Cable..... 73-6  |
| 73.2.3  | Monitor-to-VIU/CM Cable ..... 73-7                           |
| 73.2.4  | BNC Video Cable ..... 73-9                                   |
| 73.2.5  | Balanced Video Cable..... 73-9                               |
| 73.3    | CAMCORDER SYSTEM..... 73-9                                   |
| 73.3.1  | Camcorder Video/Power Cable..... 73-9                        |
| 73.3.2  | Advanced Video Interface Unit (AVIU) ..... 73-12             |
| 73.3.3  | AVIU-CM-Camcorder Video Cable..... 73-15                     |
| 73.3.4  | Camcorder/Compact Portable Light Power Interface ..... 73-17 |
| 73.3.5  | CCPI/DC Power Interface Cable ..... 73-21                    |
| 73.3.6  | CCPI Fuse Kit ..... 73-23                                    |
| 73.3.7  | Compact Portable Light Power Cable ..... 73-23               |
| 73.4    | MINI-CAM SYSTEM..... 73-25                                   |
| 73.4.1  | Mini-Cam and Lens ..... 73-25                                |
| 73.4.2  | Mini-Cam Brackets..... 73-27                                 |
| 73.4.3  | Mini-Cam Extension Cable..... 73-28                          |
| 73.4.4  | Mini-Cam ASC/ENT Cable ..... 73-28                           |
| 73.4.5  | Mini-Cam Downlink Cable ..... 73-29                          |
| 73.4.6  | Bottom-of-Locker Cable ..... 73-29                           |
| 73.4.7  | Mini-Cam On-Orbit Cable..... 73-29                           |
| 73.4.8  | Mini-Cam Sync Cable ..... 73-30                              |
| 73.4.9  | ProShare Video/Power Cable ..... 73-30                       |
| 73.5    | TV CONTROLLER UNIT..... 73-30                                |
| 73.5.1  | TVCU Centerline Mode ..... 73-31                             |
| 73.5.2  | TVCU Camcorder Mode..... 73-31                               |
| 73.6    | MISCELLANEOUS EQUIPMENT ..... 73-33                          |
| 73.6.1  | Bal/Unbal Transformer ..... 73-33                            |
| 73.6.2  | RCA-RCA Cable ..... 73-33                                    |
| 73.6.3  | Y-C Cable..... 73-33   |
| 73.6.4  | Adapters..... 73-33  |
| 73.6.5  | Portable Digital Cameras ..... 73-33                         |

**TABLES**

| <b>Table</b> |  | <b>Page</b> |
|--------------|--|-------------|
| 73-1         | Specifications for TV power cables .....               | 73-2        |
| 73-2         | Monitor-to-VIU/CM video cable .....                    | 73-7        |
| 73-3         | Specifications for BNC video cable .....               | 73-9        |
| 73-4         | Specifications for balanced video cable .....          | 73-9        |
| 73-5         | Camcorder video/power cable.....                       | 73-10       |
| 73-6         | AVIU Port Functions.....                               | 73-14       |
| 73-7         | AVIU/CM camcorder cable.....                           | 73-15       |
| 73-8         | Camcorder/compact portable light power interface ..... | 73-17       |
| 73-9         | CCPI connector and fuse data .....                     | 73-19       |
| 73-10        | CCPI/dc power I/F cable .....                          | 73-21       |
| 73-11        | CCPI fuse kit .....                                    | 73-23       |
| 73-12        | CPL I/F power cable.....                               | 73-23       |
| 73-13        | Mini-Cam.....  | 73-27       |
| 73-14        | Lens assemblies .....                                  | 73-27       |
| 73-15        | Bracket data .....                                     | 73-28       |
| 73-16        | Mini-Cam extension cable .....                         | 73-28       |
| 73-17        | Mini-Cam ASC/ENT cable.....                            | 73-29       |
| 73-18        | Mini-Cam downlink cable .....                          | 73-29       |
| 73-19        | Mini Cam On-Orbit Cable.....                           | 73-30       |
| 73-20        | Mini-Cam sync cable .....                              | 73-30       |
| 73-21        | ProShare video/power cable .....                       | 73-30       |

**FIGURES**

**Figure**

|       |   |       |
|-------|---|-------|
| 73-1  | TV power cables (10- and 20-foot) schematic diagram ..... | 73-2  |
| 73-2  | TV power cables (10- and 20-foot).....                    | 73-3  |
| 73-3  | TV power cable (6-foot) schematic diagram.....            | 73-4  |
| 73-4  | TV power cable (6-foot).....                              | 73-5  |
| 73-5  | Pigmy cable.....  | 73-6  |
| 73-6  | Flight Deck Connection .....                              | 73-6  |
| 73-7  | Monitor-to-VIU/CM video cable .....                       | 73-8  |
| 73-8  | Camcorder video/power cable.....                          | 73-11 |
| 73-9  | AVIU Functional Diagram.....                              | 73-13 |
| 73-10 | AVIU/CM-camcorder video cable .....                       | 73-16 |
| 73-11 | CCPI connector and fuses .....                            | 73-18 |
| 73-12 | CPI schematic diagram .....                               | 73-20 |
| 73-13 | CCPI/dc power interface cable schematic diagram.....      | 73-22 |
| 73-14 | CPL power cable.....                                      | 73-24 |
| 73-15 | Mini-Cam and lens assemblies .....                        | 73-26 |
| 73-16 | TVCU Functional Diagram .....                             | 73-32 |

## SECTION 73 SHUTTLE IN-CABIN VIDEO EQUIPMENT

### 73.1 INTRODUCTION

The Space Shuttle Program requires video documentation of crew activities, experiments, payload deploys, etc. from within the crew module. The documentation is accomplished through the use of NASA-developed equipment as well as off-the shelf equipment. The NASA-developed equipment includes various general use cables, a Mini-Cam system, a camcorder system, and video monitoring equipment. The miscellaneous cables are used as required to route video, power, and sync. The Mini-Cam can obtain real-time video, but must be connected to a Video Tape Recorder (VTR) to record its video. The off-the-shelf equipment includes camcorders and their associated hardware as well as video monitoring equipment. The camcorders can record video captured through the lens or received from other sources. The camcorders can also record audio. The actual hardware manifested for a mission is dependent on the Space Shuttle Program and payload customer requirements.

### 73.2 GENERAL USE CABLES

Various cables can be manifested on the space shuttle to route video, power, and sync for video systems. This cable list includes the following: Television (TV) power cable (10- or 20-foot), pigmy cable, monitor to Video Interface Unit Model CM (VIU/CM) cable, Payload Data Interface Panel (PDIP) video cable, TV Interface Panel (TVIP) cable, BNC video cable, and balanced video cable. Each cable is described in the following sections. For more details on how these cables are used, refer to the generic and flight-specific Photo/TV Checklist Flight Data File (FDF).

#### 73.2.1 TV Power Cable

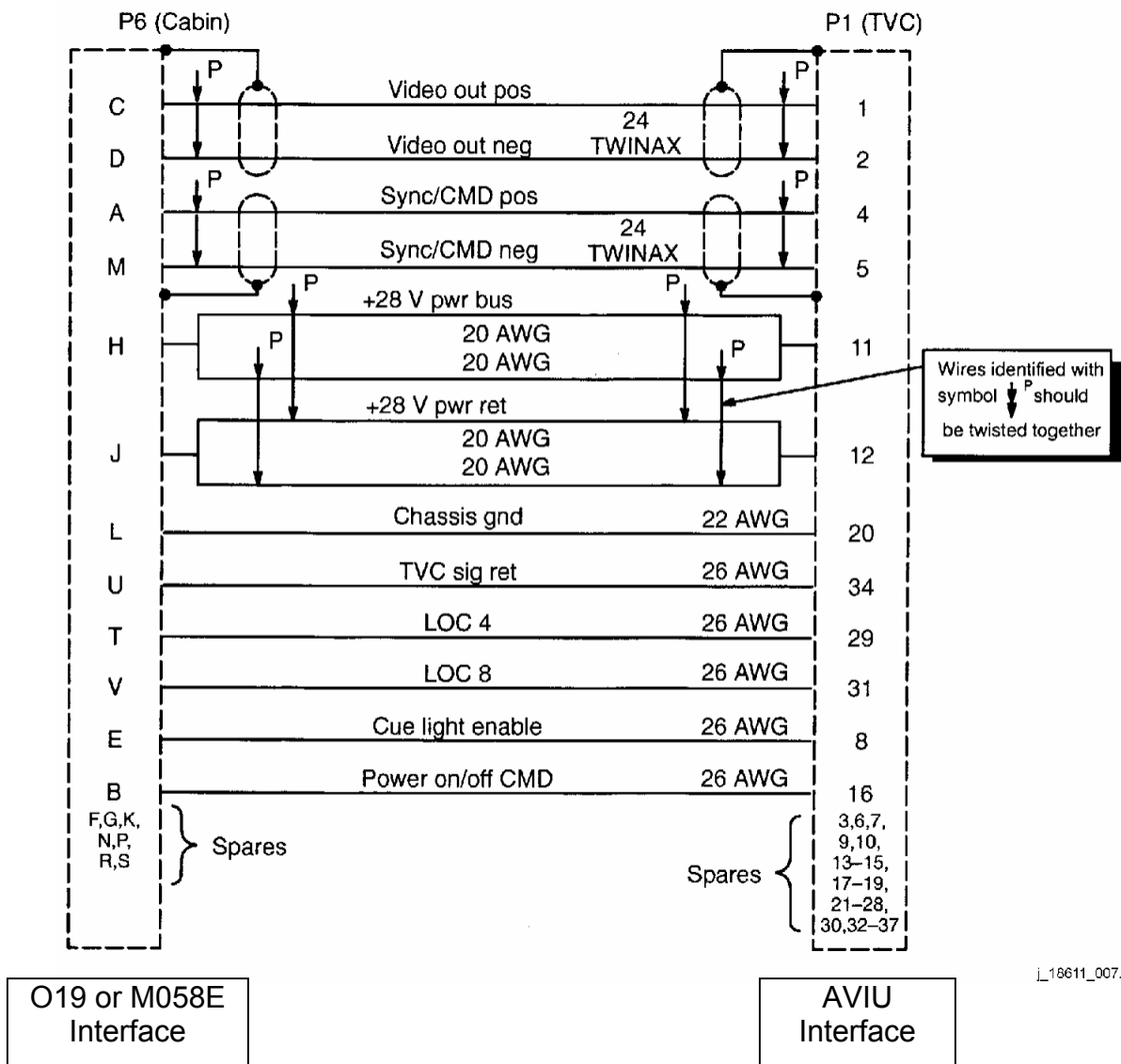
Currently, there are three TV power cables that can be used in the orbiter: a 10-foot cable, a 20-foot cable, and a 6-foot cable. The specifications for these cables are listed in Table 73-1.

##### 73.2.1.1 10- and 20-Foot TV Power Cables

The 10- or 20-foot TV power cable can be used to route video from external video sources to the orbiter Closed Circuit Television (CCTV) system, to route power from the orbiter to video devices, and to route a synchronization/command signal from the orbiter CCTV system to synchronous video sources. The external video sources include the camcorder system, the Mini-Cam system, and flight-specific payload systems. The TV power cable interfaces with the orbiter CCTV system directly through the TV power connections on O19 and MO58F or through the pigmy cable, which can be connected at O19 or MO58F. Figure 73-1 is the schematic diagram of the 10- and 20-foot TV power cables. The cables are also shown in Figure 73-2.

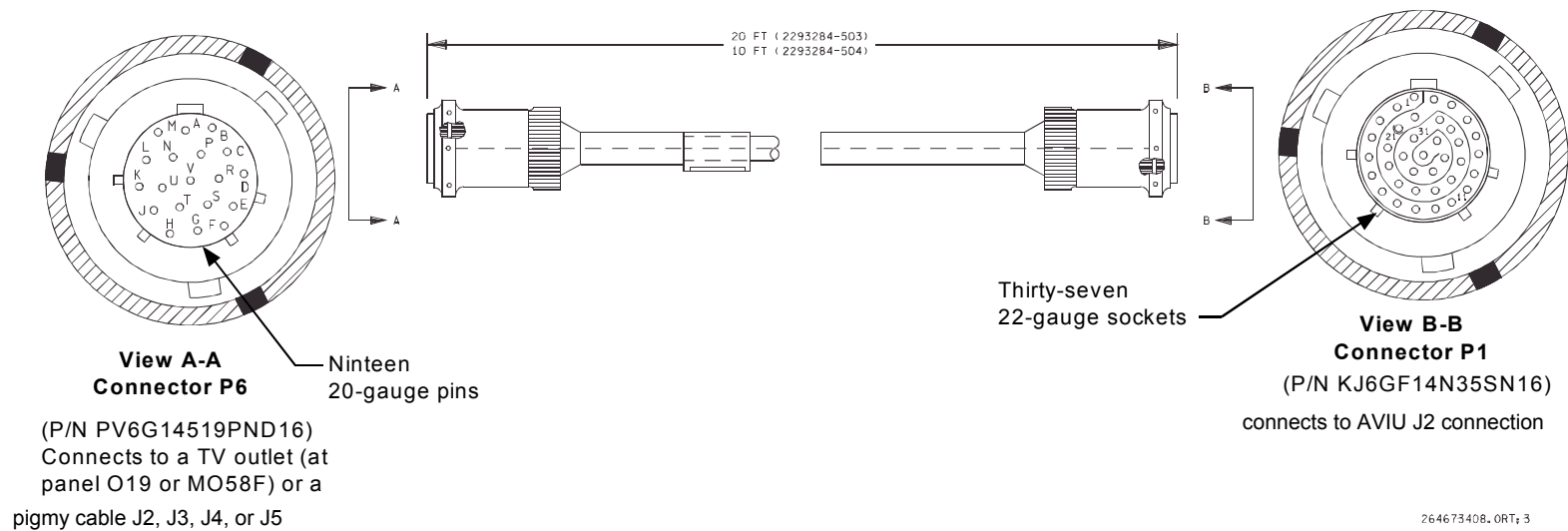
Table 73-1. Specifications for TV power cables

| Item         | Specification |             |   |
|--------------|---------------|-------------|---|
|              | 10 ft         | 20 ft       | 6 ft ± 3 in   |
| Part no.     | 2293284-504   | 2293284-503 | SED39122650-301   |
| Drawing no.  | RCA 2293284   | RCA 2293284 | SED39122650 (VIU to orbiter cable - camcorder cable assy) |
| Manufacturer | RCA           | RCA         | NASA  |
| Weight       | 1.08 lb       | 1.72 lb     | 0.61 lb   |



I\_18611\_007.tif

Figure 73-1. TV power cables (10- and 20-foot) schematic diagram



264673408.ORT; 3  
j\_18611\_046.cv5

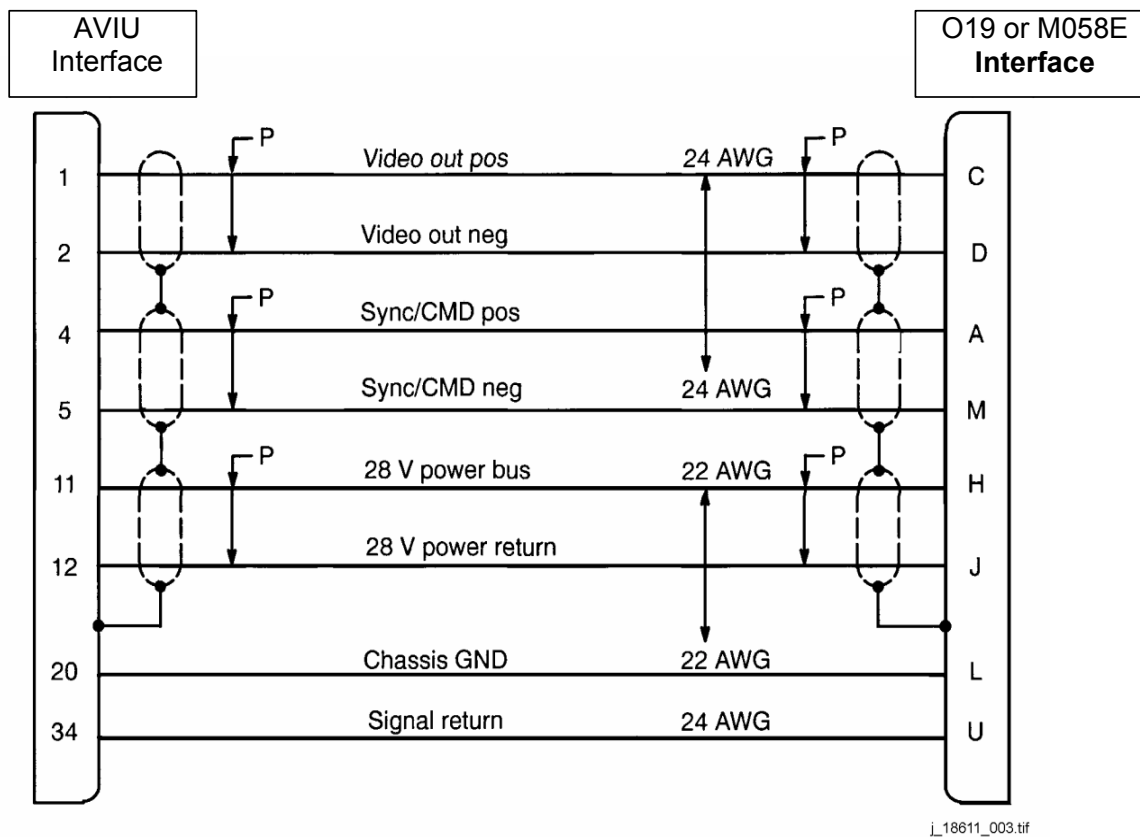
**Figure 73-2. TV power cables (10- and 20-foot)**



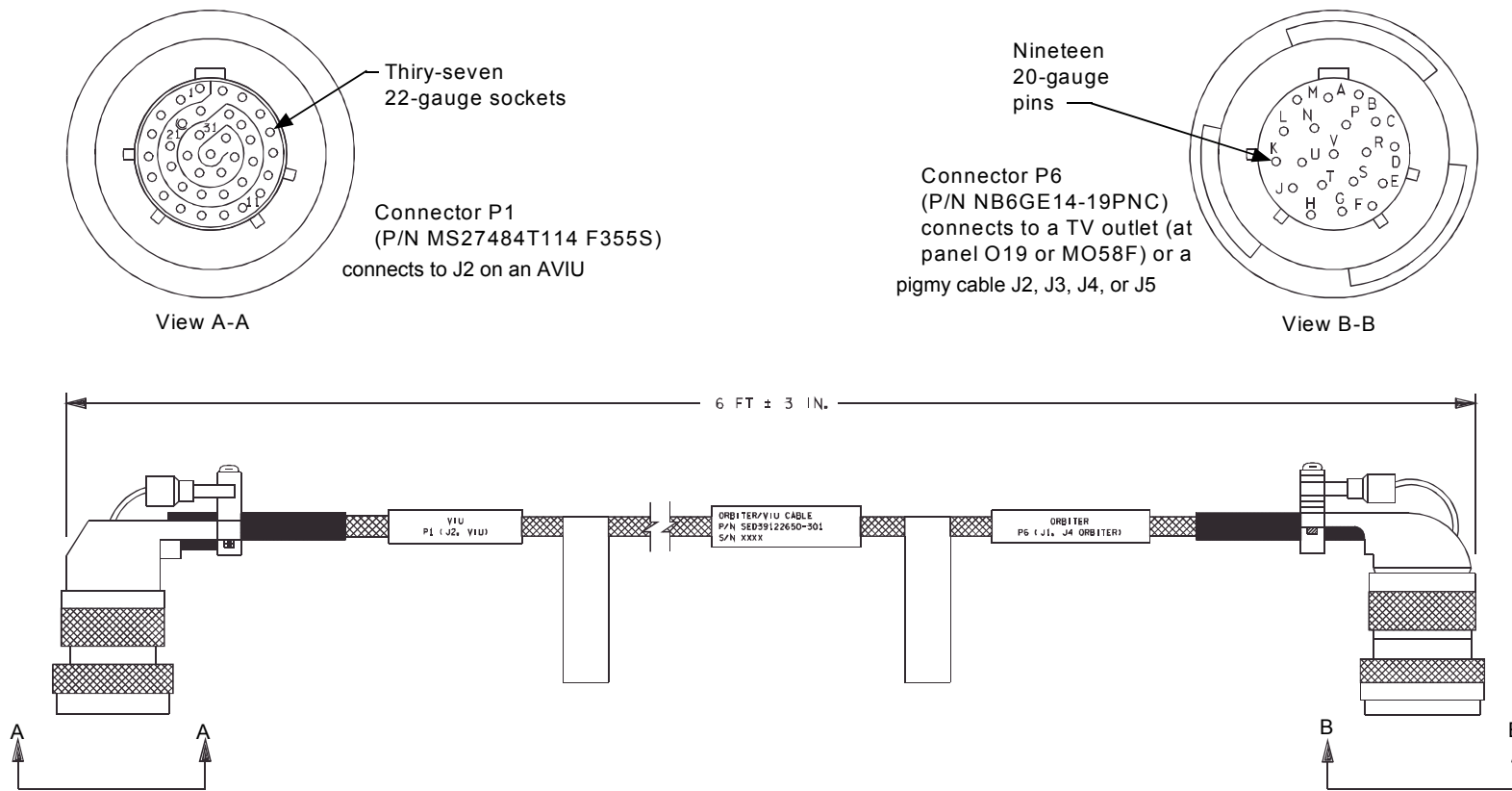
### 73.2.1.2 6-Foot TV Power Cable

The 6-foot TV power cable is currently only manifested for SPACEHAB flights and was designed to work with the camcorder. The cable is essentially the same as the 10- and 20-foot TV power cables as far as providing power to the camera and allowing video to flow back to the Video Switching Unit (VSU), however, the 6-foot TV power cable does not have sync or command lines.

Sync is required by the Color Television Camera (CTVC) and the Intensified Television Camera (ITVC) for panel A7 or Mission Control Center (MCC) commands to work, since the commands are imbedded in the sync signal. Therefore, this cable cannot be used with the CTVC or the ITVC if remote commanding is desired. However, both cameras do have switches to allow local control by the crew. Figure 73-3 is a schematic diagram of the cable. The cable is shown Figure 73-4.



**Figure 73-3. TV power cable (6-foot) schematic diagram**



264673406.ORT: 3  
j\_18611\_047.cv5

Figure 73-4. TV power cable (6-foot)

### 73.2.2 Pigmy Cable

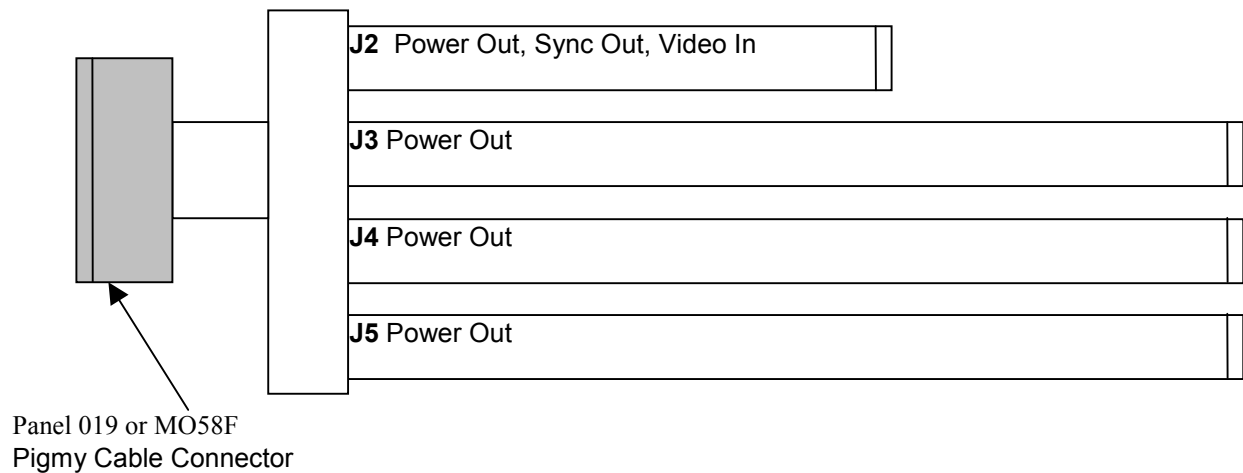
The pigmy cable is designed to connect to either orbiter TV Outlet Panel O19 or MO58F; it contains four umbilicals (J2, J3, J4, & J5).

- The J2 connector supplies 28Vdc Power Out, Sync Out, and Video In.
- The J3 J4, and J5 connectors only supplies 28Vdc Power Out

The four Pigmy Cables route 28 V dc power from the TV Outlet Panels to the Audio Video Interface Unit (AVIU), Camcorder/Compact Portable Light Power Interface (CCPI) or Payload Data Interface Panel (PDIP) input for a specialized payload.

The Video sourced from either Flight Deck or Mid Deck will be routed only thru the J2 Pigmy Cable Umbilical to the Video Switching Unit (VSU).

The pigmy cable is shown in Figure 73-5.



**Figure 73-5. Pigmy cable**



**Figure 73-6. Flight Deck Connection**

**73.2.3 Monitor-to-VIU/CM Cable**

The monitor-to-VIU/CM video cable is used to route video from a flight deck monitor to the AVIU (unbalanced connector) J4 input for eventually recording. The AVIU J7 output can then be connected via different cable to either.

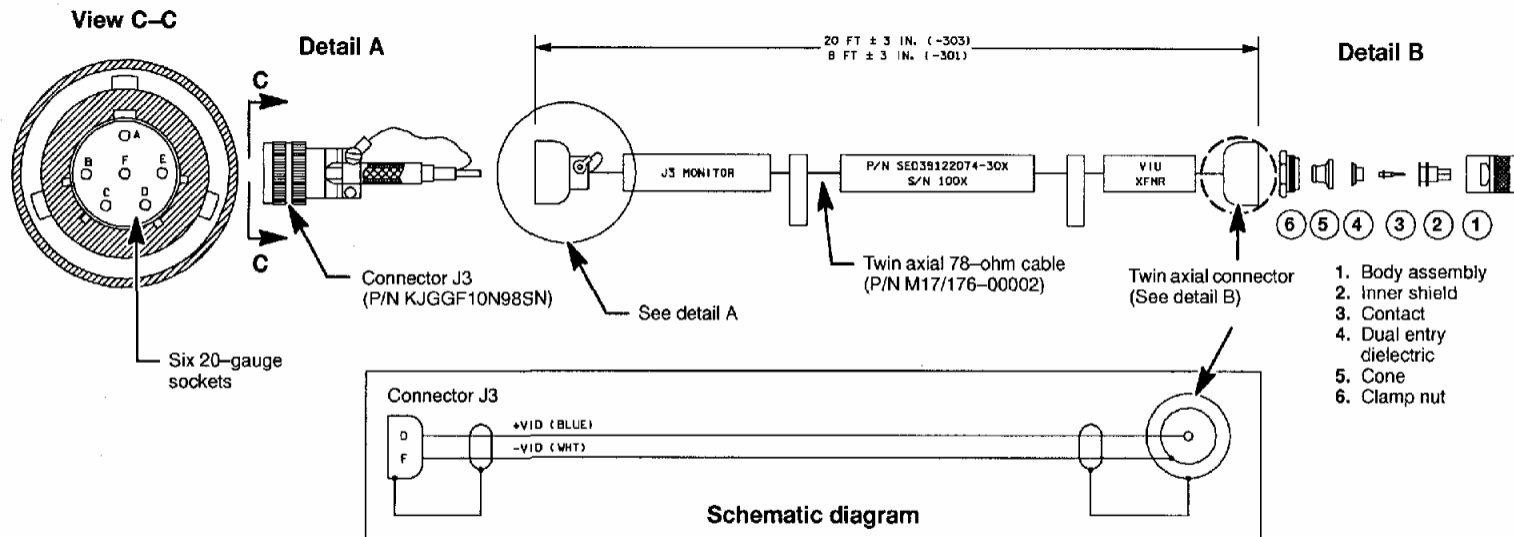
- A. V10 VTR Recorder
- B. PD100 Sony Camcorder

The Monitor-to-VIU/CM Cable can also be used directly (no AVIU interface) to connect to Monitor 2(1) to ISS (CH92) connector of the VPU.

The specifications for this cable are listed in Table 73-2.

**Table 73-2. Monitor-to-VIU/CM video cable**

| Item         | Specification   |                 |
|--------------|-----------------|-----------------|
|              | 8 ft ± 3 in     | 20 ft ± 3 in    |
| Part no.     | SED39122074-301 | SED39122074-303 |
| Drawing no.  | SED39122074     | SED39122074     |
| Manufacturer | NASA            | NASA            |
| Weight       | 0.13 lb         | 0.39 lb         |



i\_18611\_055.tif

Figure 73-7. Monitor-to-VIU/CM video cable

### 73.2.4 BNC Video Cable

The specifications for this cable are listed Table 73-3.

**Table 73-3. Specifications for BNC video cable**

| Item         | Specification   |
|--------------|-----------------|
| Part no.     | SED33105779-301 |
| Drawing no.  |                 |
| Manufacturer |                 |
| Weight       | 0.20 lb         |
| Length       |                 |

### 73.2.5 Balanced Video Cable

The specifications for this cable are listed in Table 73-4.

**Table 73-4. Specifications for balanced video cable**

| Item         | Specification   |
|--------------|-----------------|
| Part no.     | SED33105778-301 |
| Drawing no.  |                 |
| Manufacturer |                 |
| Weight       | 0.22 lb         |
| Length       |                 |

## 73.3 CAMCORDER SYSTEM

The Sony PD-100 camcorder is used to record and play back high quality video and audio. The camcorder can record up to 40-minute digital tapes. The camcorder can be used in cabin for Public Affairs Office (PAO) events, crew conferences, etc. or out the window for deploys, retrieves, external tank video, etc.

The features, specifications, and operations of these camcorders are described in their respective instruction manuals, as PDF documents, saved on the DF24 hard drive at:

S:\Divisions\DF\Private\DF24\INFO\_LRU\COMMSYS\CCTV

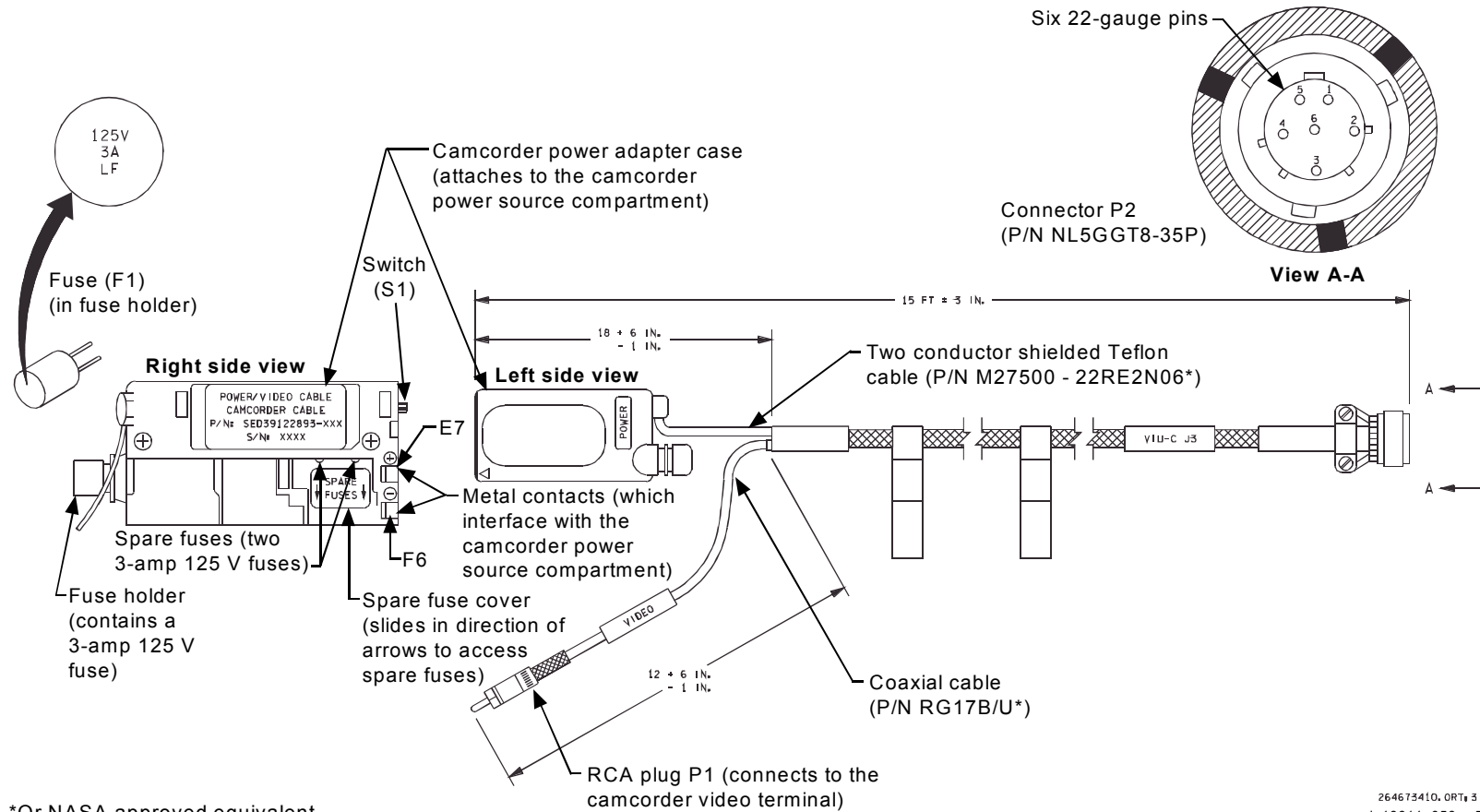
The orbiter interface equipment is described in the following sections.

### 73.3.1 Camcorder Video/Power Cable

This 15-foot camcorder video/power cable transmits video and 8.4 V dc power between the AVIU to the SONY PD-100 Camcorder. The specifications for this cable are listed Table 73-5. Figure 73-8 shows the basic cable configuration.

*Table 73-5. Camcorder video/power cable*

| Item     | Specification    |
|----------|------------------|
| Part no. | SED 33111490-303 |
| Weight   | 0.77 lb          |
| Length   | 15.0 ft          |



**Figure 73-8. Camcorder video/power cable**



### 73.3.2 Advanced Video Interface Unit (AVIU)

The AVIU is Government-furnished equipment. It was designed and built to provide a necessary interface between the orbiter power, the CCTV system, and Commercial off-the-shelf equipment (such as PD-100 camcorders and V10 digital recorders). The AVIU is shown in Figure 73-9.

The AVIU is powered by 28 V dc from panel O19 or MO58F. The orbiter 28 V dc is applied to a dc-to-dc converter that outputs 8.4 Vdc power source for the camcorder; thus allowing the crew to charge the Camcorder Battery or use orbiter power to operate the Camcorder. The unbalanced video from the camcorder is routed to a bal/unbal transformer for coupling into an orbiter-balanced video interface circuit board. The bal/unbal transformer transforms the camcorder unbalanced video to balanced video compatible with the orbiter CCTV system. The video is input to the VSU through the same pigmy legs that provide the 28 V dc.

Table 73-6 contains information on the AVIU J port connections switches.

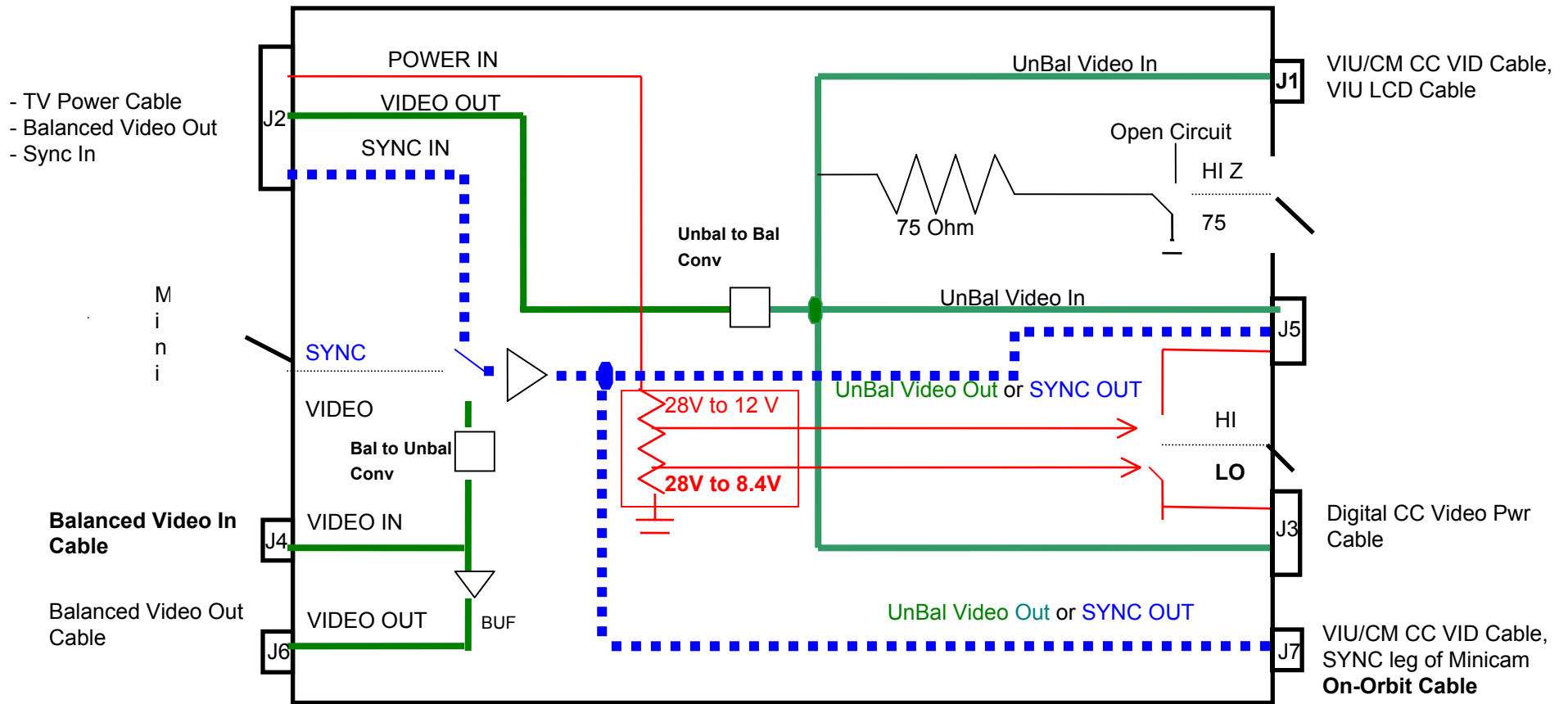


Figure 73-9. AVIU Functional Diagram

**Table 73-6. AVIU Port Functions**

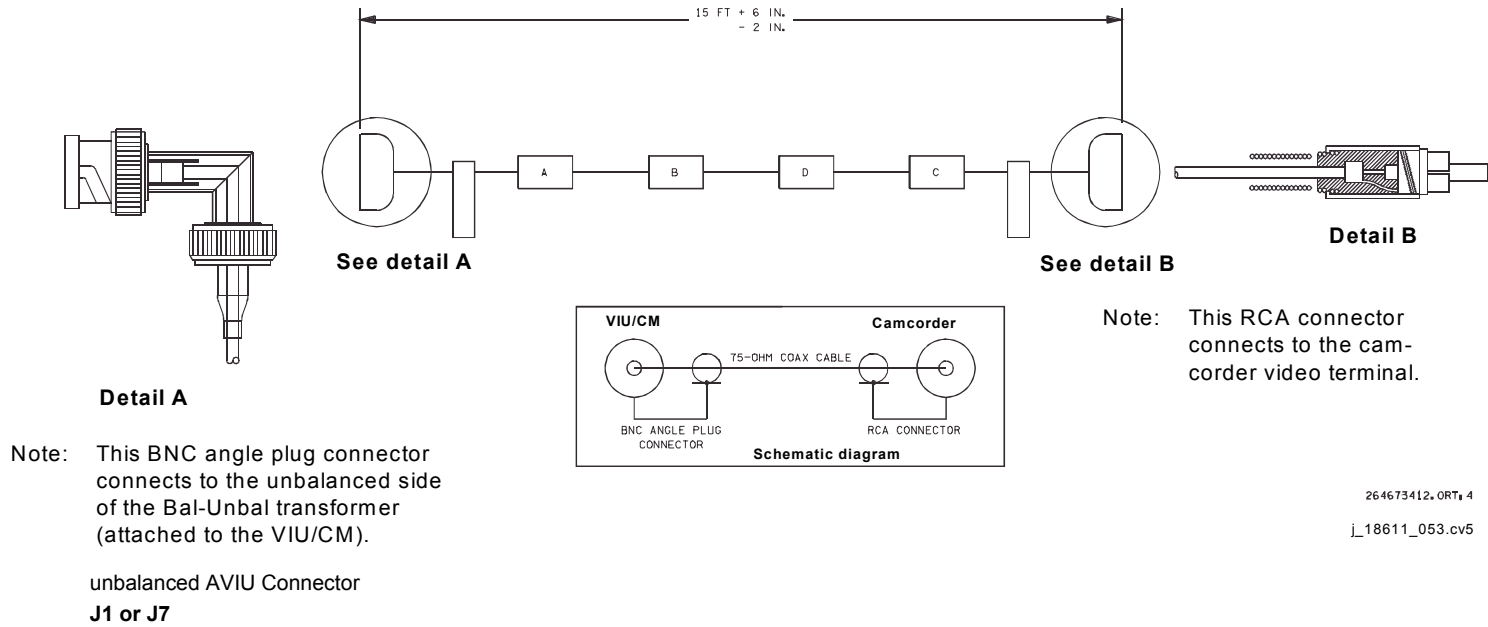
|  |   |
|--|---|
| <p><b>J2 Port</b></p> <ul style="list-style-type: none"> <li>• Balanced Video Output (Normally to CTVC System)</li> <li>• 28 Volt Input</li> <li>• SYNC Signal Input</li> </ul>        | <p><b>J1 Port</b></p> <ul style="list-style-type: none"> <li>• Unbalanced Video Input or Output</li> </ul>  |
| <p><b>SYNC/VIDEO Switch</b></p> <ul style="list-style-type: none"> <li>• VIDEO - Unbalanced Video output to PD100 or V10 from J4 Input</li> <li>• SYNC - SYNC signal output</li> </ul> | <p><b>HI Z/75 Switch</b></p> <ul style="list-style-type: none"> <li>• 75 - for normal ops</li> <li>• HI Z – if J1 video going to PGSC or a terminated source (i.e., PD100 or V10).</li> </ul>   |
| <p><b>J4 Port</b></p> <ul style="list-style-type: none"> <li>• Balanced Video Input (Video from the back of the Monitor via the Monitor to VIU/CM Cable)</li> </ul>                    | <p><b>J3 Port</b></p> <ul style="list-style-type: none"> <li>• Unbalanced Video Input or Output</li> <li>• 8.4 Volt Power out</li> </ul>  |
| <p><b>J6 Port</b></p> <ul style="list-style-type: none"> <li>• Balanced Video Signal output</li> </ul>   | <p><b>HI/LO Switch</b></p> <ul style="list-style-type: none"> <li>• HI – 12 volt (Minicam) sw pos near J5</li> <li>• LO – 8.4 volt (PD100 or V10) sw pos near J3</li> </ul>   |
|  | <p><b>J7 Port</b></p> <ul style="list-style-type: none"> <li>• SYNC/VIDEO sw - VIDEO Unbalanced Video output to PD100 or V10 from J4 Input</li> <li>• SYNC/VIDEO sw - SYNC signal output to Minicam via Minicam On-Orbit Cable</li> </ul> |

### 73.3.3 AVIU-CM-Camcorder Video Cable

The AVIU/CM-camcorder cable can be used with a bal/unbal transformer and a monitor to AVIU/CM cable (SED39122074-301, -303) to record video from a flight deck color TV monitor onto a camcorder. This cable connects the unbalanced side of the bal/unbal transformer and the camcorder. The specifications for the VIU/CM-camcorder cable are listed in Table 73-7. The cable is shown in Figure 73-10.

**Table 73-7. AVIU/CM camcorder cable**

| Item         | Specification                                |
|--------------|--|
| Part no.     | SED39122269-301                              |
| Drawing no.  | SED39122269 (cable assy, camcorder - VIU/CM) |
| Manufacturer | NASA   |
| Weight       | 1.24 lb                                      |
| Length       | 15 ft 6 ± 2 in.                              |



264673412.ORT1.4  
j\_18611\_053.cv5

**Figure 73-10. AVIU/CM-camcorder video cable**

**73.3.4 Camcorder/Compact Portable Light Power Interface**

The CCPI is used solely for a multiple power source; there is no video routing capability. It can provide power to two camcorders and one compact portable light simultaneously, thus freeing up the TV PWR ports. The CCPI draws 25 V current directly from any orbiter dc outlet and steps it down to a 6 V so the power can be used with the camcorder and Compact Portable Light (CPL). When using the CCPI, the CCPI/dc power/Interface (I/F), the camcorder video power, and the CPL I/F cables are used. The CCPI has four fuses (two 2A, one 8A, and one 4A). Spares are located in the CCPI fuse kit.

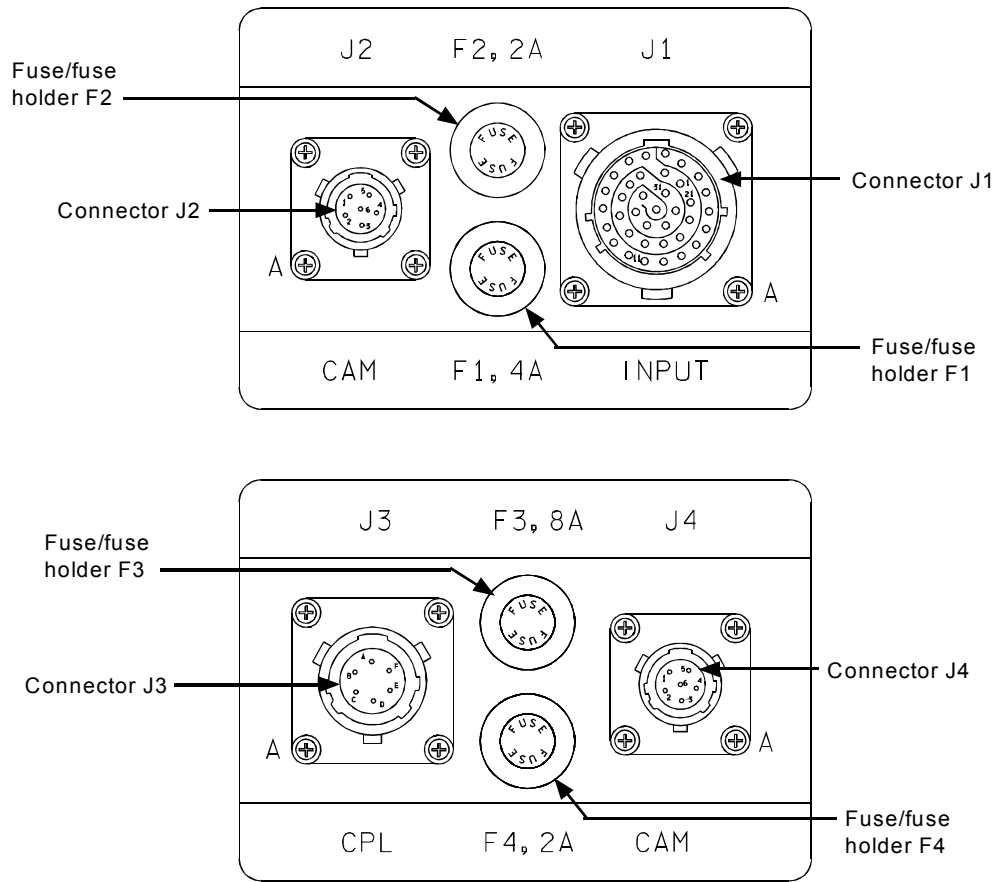
The decal on the CCPI states the following:

OPERATING LIMITS  
CAMCORDERS ONLY - UNLIMITED  
CPL ONLY - 19 MIN.  
CPL + ONE CAMCORDER - 14 MIN.  
CPL + TWO CAMCORDERS - 11 MIN.

The specifications for the CCPI are listed Table 73-8. The CCPI connector and fuses are shown in Figure 73-11. Table 73-9 provides more data on each connector and fuse. Figure 73-12 is the CCPI schematic diagram.

**Table 73-8. Camcorder/compact portable light power interface**

| Item         | Specification   |
|--------------|---|
| Part no.     | SED33104920-301   |
| Drawing no.  | SED33104920 (assy, camcorder/CPL power interface)<br>SED33104950 (schematic diagram, camcorder/CPL power interface) |
| Manufacturer | NASA  |
| Weight       | 2.36 lb   |
| Dimensions   |   |
| Height       | 2.25 in.  |
| Width        | 3.25 in.  |
| Length       | 6.75 in.  |
| Overall      | 8.25 in. (including connector caps)   |



Back side

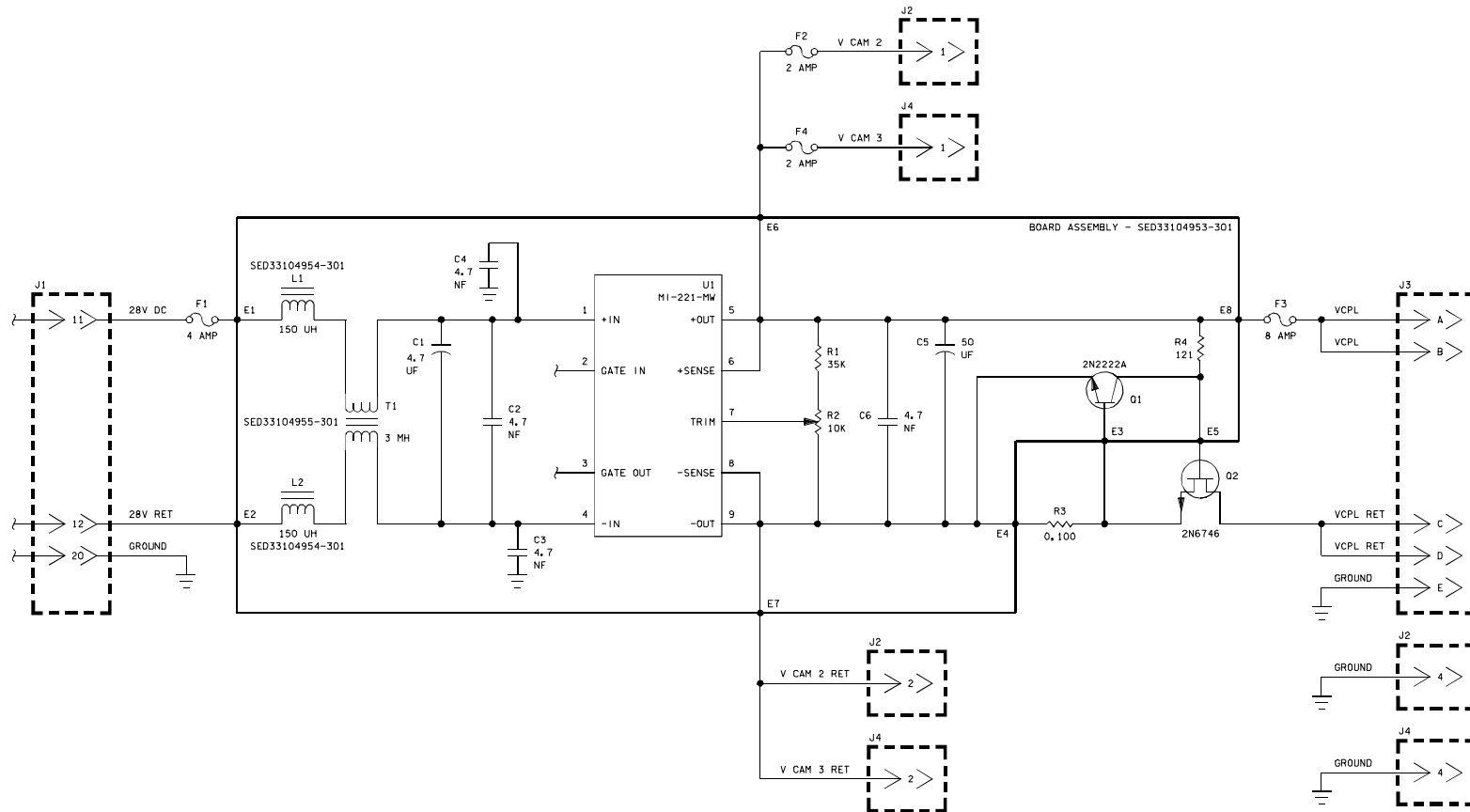
264673415, PNL+ I  
j\_18611\_187.cv5

**Figure 73-11. CCPI connector and fuses**

**Table 73-9. CCPI connector and fuse data**

| CCPI location | Item         | CCPI label | Description                                  | Part number    | Equipment                   |
|---------------|--------------|------------|--|----------------|-----------------------------|
| Front side    | Connector J1 | J1, INPUT  | Circular connector with 37 22-gauge pins     | NLSOE14-35P    | TV power cable              |
| Front side    | Fuse F1      | F1, 4A     | Fast-acting, 4 amp, 2AG cartridge fuse       | 225-004        | N/A                         |
| Front side    | Connector J2 | J2, CAM    | Circular connector with six 22-gauge sockets | MS27472E8F35 S | Camcorder/video power cable |
| Front side    | Fuse F2      | F2, 2A     | Fast-acting, 2 amp, 2AG cartridge fuse       | 225-002        | N/A                         |
| Back side     | Connector J3 | J3, CPL    | Circular connector with six 20-gauge sockets | MS3470L10-6S   | CPL power cable             |
| Back side     | Fuse F3      | F3, 8A     | Fast-acting, 8 amp, 2AG cartridge fuse       | 225-008        | N/A                         |
| Back side     | Connector J4 | J4, CAM    | Circular connector with six 22-gauge sockets | MS27472E8F35 S | Camcorder/video power cable |
| Back side     | Fuse F4      | F4, 2A     | Fast-acting, 2 amp, 2AG cartridge fuse       | 225-002        | N/A                         |





264673418, SCH 1  
3418.cv5

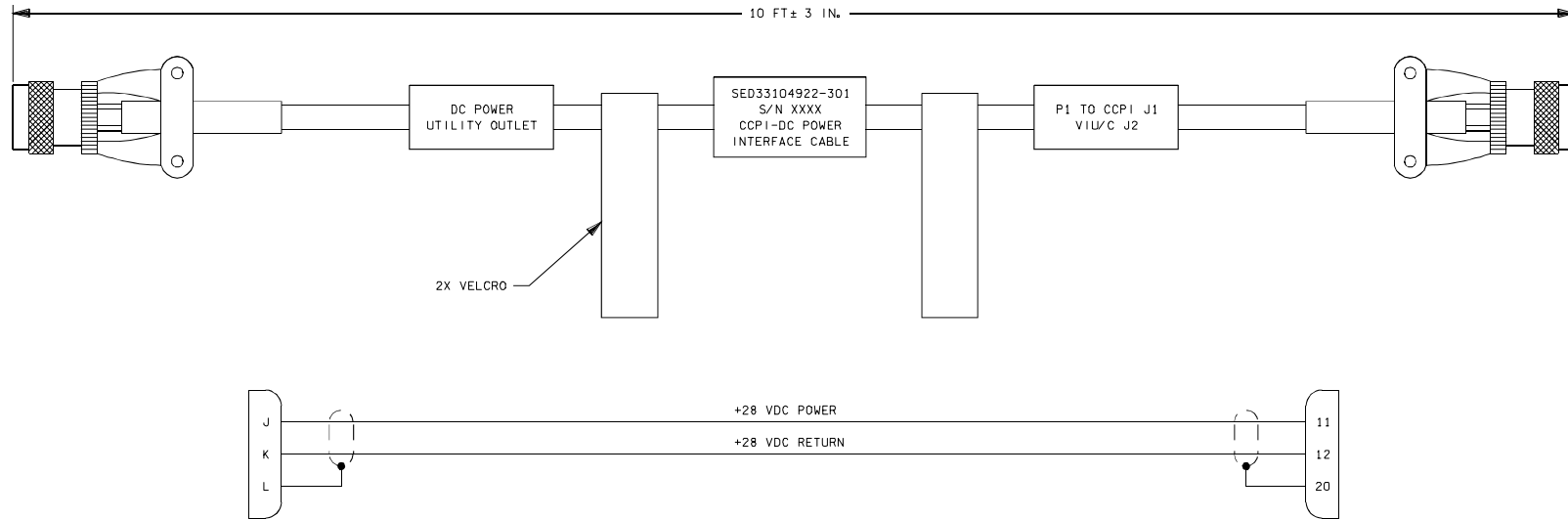
Figure 73-12. CPI schematic diagram

### 73.3.5 CCPI/DC Power Interface Cable

This cable is used to power the CCPI from an orbiter +28 V dc utility outlet. The specifications for the CCPI/dc power interface cable are listed in Table 73-10. Figure 73-13 shows the schematic diagram.

**Table 73-10. CCPI/dc power I/F cable**

| Item         | Specification                               |
|--------------|---|
| Part no.     | SED33104922-301                             |
| Drawing no.  | SED33104922 (CCPI/dc power interface cable) |
| Manufacturer | NASA  |
| Weight       | 0.36 lb                                     |
| Length       | 10 ft ± 3 in.                               |



264673421. ART 1  
3421.cv5

**Figure 73-13. CCPI/dc power interface cable schematic diagram**

### 73.3.6 CCPI Fuse Kit

The CCPI fuse specifications, including contents, are given in Table 73-11. Each fuse is contained in a small Ziploc bag and labeled.

**Table 73-11. CCPI fuse kit**

| Item         | Specification                    |                 |           |
|--------------|----------------------------------|-----------------|-----------|
| Part no.     | SED33105384-301                  |                 |           |
| Drawing no.  | SED33105384 (CCPI fuse kit assy) |                 |           |
| Manufacturer | NASA                             |                 |           |
| Weight       | 0.03 lb                          |                 |           |
| Contents     | Fuse label                       | Ratings (PM DS) | Quantity* |
|              | CCPI CCPI-CPL OUT 8A             | 8               | 1         |
|              | CCPI input 4A                    | 4               | 1         |
|              | CCPI CC OUT 2A                   | 2               | 1         |
|              | VIU VIU-TEAC 2A                  | 2               | 1         |
|              | VIU VIU/C/CM 1A                  | 1               | 1         |

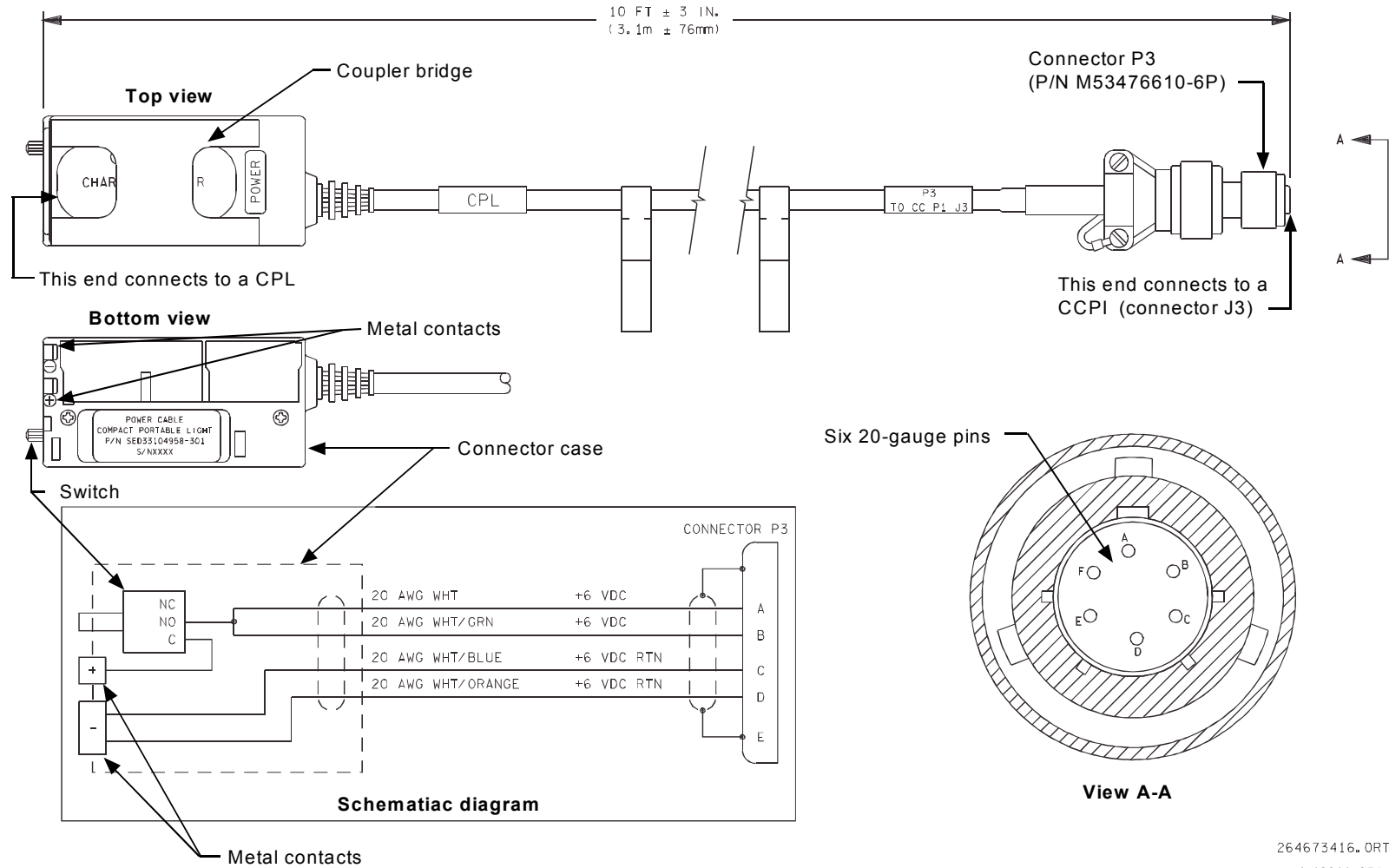
\*The quantity is 1 unless specified by assembly TPS to meet flight-specific requirements.

### 73.3.7 Compact Portable Light Power Cable

The CPL power cable routes 6 V dc power from the CCPI to the CPL. The specifications for the CPL power cable are given in Table 73-12. The cable is shown in Figure 73-14.

**Table 73-12. CPL I/F power cable**

| Item         | Specification   |
|--------------|---|
| Part no.     | SED33104958-301   |
| Drawing no.  | SED33104958 (connector/cable assy, power cable-camcorder/CPL power interface) |
| Manufacturer | NASA  |
| Weight       | 0.62 lb   |
| Length       |   |



264673416.ORT: 3  
j\_18611\_054.cv5

Figure 73-14. CPL power cable

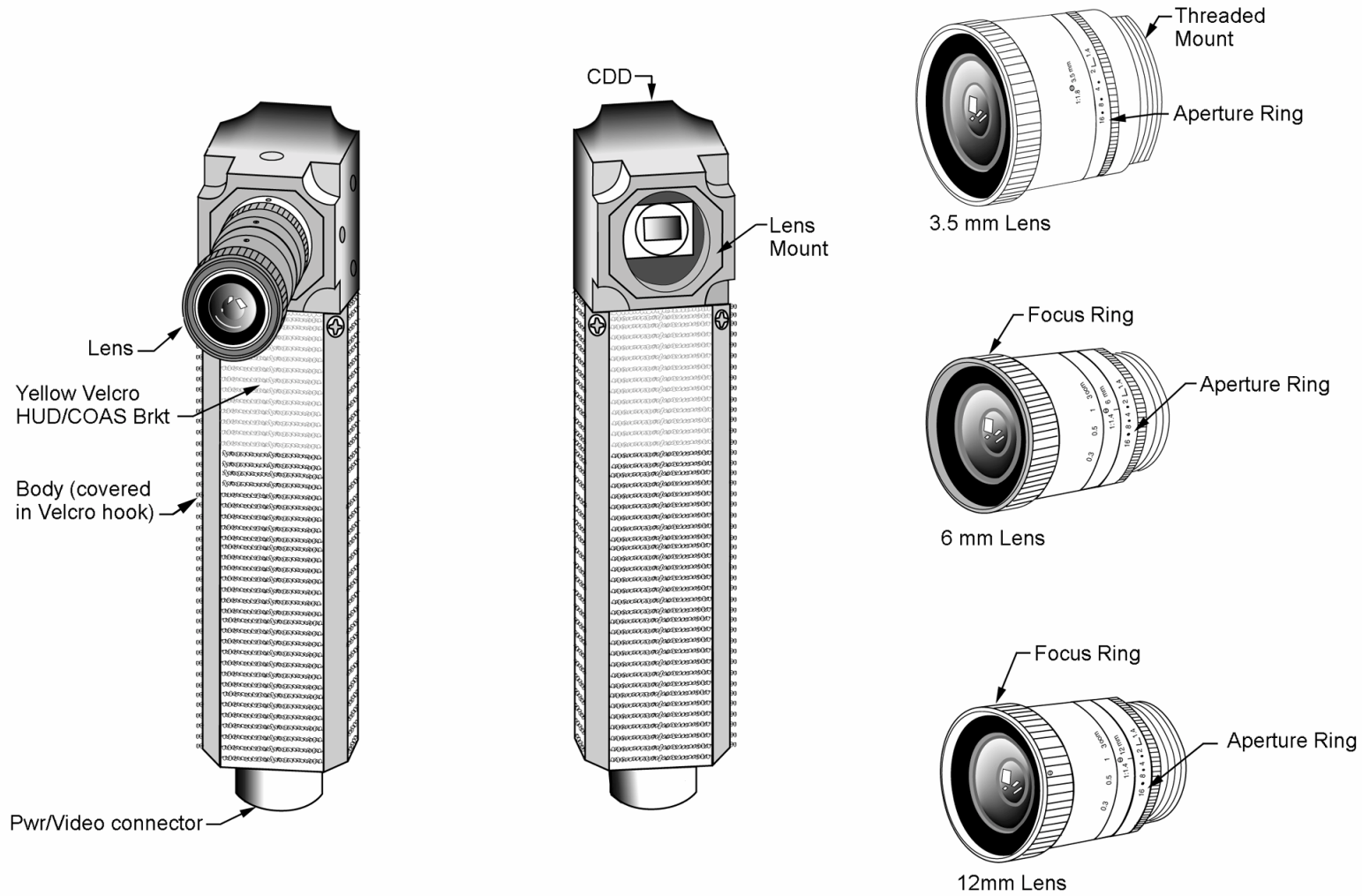
## 73.4 MINI-CAM SYSTEM

The Mini-Cam may be used to capture video during all phases of flight. During ascent and entry, the Mini-Cam has three possible configurations: (1) mounted on a glareshield bracket looking back at the crew, (2) mounted on an aft bracket looking forward at the crew, or (3) mounted on an overhead bracket looking out the overhead window. During entry, the Mini-Cam has two additional possible configurations: (1) mounted on a Heads-Up Display (HUD) bracket looking through the HUD out the pilot's window or (2) mounted on the Pilot's Point of View (PPOV) camera bracket looking out the pilot's window. The PPOV configuration is available only on OV-102 and requires the SED-39127622-301 camera. During ascent and entry, the Mini-Cam video may be recorded on an 8mm VTR along with audio. During entry, video of the approach and landing may be downlinked real time through ground sites. On orbit, the main function of the Mini-Cam is to capture video for video teleconferencing. The Mini-Cam is connected to the Payload General Support Computer (PGSC) that has the ProShare/OCA capabilities. The Mini-Cam may also be used as a video camera on orbit, but typically the camcorder is used.

The Mini-Cam system requires the following Mini-Cam system-specific components: Mini-Cam with lens, Mini-Cam extension cable (extension cable PPOV/Mini-Cam), Mini-Cam Ascent/Entry (ASC/ENT) cable (pwr cable Ascent TV Cam), Mini-Cam downlink cable (PPOV TEAC Wye cable), 12 V dc VIU/CM, the bottom of locker cable, and brackets. The Mini-Cam system also uses other video equipment discussed in this brief. Flight-specific configurations may also include the following Mini-Cam components: Mini-Cam on-orbit cable (pwr/video cable Mini-Cam), Mini-Cam sync cable (pigmy sync to XFMR cable), or ProShare video/pwr cable. Mini-Cam configurations are described in the generic and flight-specific photo/TV checklists. The Mini-Cam system-specific components are discussed in the following sections.

### 73.4.1 Mini-Cam and Lens

The Mini-Cam can be used with one of three lens assemblies. The lens is at a 90° angle with the camera body. The PPOV camera is the same as the Mini-Cam except the lens is in line with the camera body. The PPOV camera has not been used since the HUD bracket was developed for Mini-Cam entry video. A diagram of the Mini-Cam and lens assemblies is given in Figure 73-15. The specifications for the Mini-Cam and lens assemblies are given in Table 73-13 and Table 73-14, respectively.



j\_18611\_123.tif

Figure 73-15. Mini-Cam and lens assemblies

**Table 73-13. Mini-Cam**

| Item                  | Specification                                       |
|-----------------------|---|
| Part no.              | SED39127620-302                                     |
| Drawing no.           |   |
| Manufacturer          |   |
| Weight                | 0.40 lb   |
| Dimensions            |   |
| Depth                 | 1-3/16 in.  |
| Width                 | 1 in.   |
| Length                | 5-1/4 in.   |
| Imager                |   |
| Model                 | XC-999  |
| Horizontal resolution | 470 lines   |
| Pixel count           | 768 horizontal, 494 vertical                        |
| Sensing area          | 6.4 mm horizontal, 4.8 mm vertical, 8.0 mm diagonal |

**Table 73-14. Lens assemblies**

| Item                            | Specification |                                 |            |
|---------------------------------|---------------|---------------------------------|------------|
|                                 | 3.5 mm        | 6.0 mm                          | 12.0 mm    |
| Part no.                        |               |                                 |            |
| Drawing no.                     |               |                                 |            |
| Manufacturer                    |               |                                 |            |
| Weight                          | 0.10 lb       | 0.10 lb                         | 0.10 lb    |
| Aperture range (f/stop)         | f/1.8-f/16    | f/1.4-f/16                      | f/1.4-f/16 |
| Approximate Field of View (FOV) | 84.87°        | 56.15°                          | 29.86°     |
| Minimum focus distance (ft)     | Fixed         | 0.3 m                           | 0.5 m      |
| Configurations used             | Glareshield   | Aft window, COAS, video telecon | HUD        |

**73.4.2 Mini-Cam Brackets**

Several brackets have been designed for mounting the Mini-Cam. Bracket data are provided in Figure 73-15.



**Table 73-15. Bracket data**

| Item         | Specification          |             |                                    |   |
|--------------|------------------------|-------------|------------------------------------|---|
|              | Glareshield            | Rear window | COAS                               | HUD   |
| Part no.     |                        |             |                                    |   |
| Drawing no.  |                        |             |                                    |   |
| Manufacturer |                        |             |                                    |   |
| Weight       |                        |             |                                    |   |
| Dimensions   |                        |             |                                    |   |
| Width        | 2 in.                  | 2 in.       | N/A                                | N/A   |
| Length       | 9.5-10.5 in.           | 12-20 in.   | 5.75-in. base<br>3.5-in. extension | 4.5-in. base<br>1.5-in. extension<br>2-in. rise |
| Mount type   | Velcro with FDF tether | Velcro      | Thumbscrew                         | Thumbscrew with tie wrap                        |

**73.4.3 Mini-Cam Extension Cable**

The Mini-Cam extension cable is used to provide additional length between the Mini-Cam and the Mini-Cam ASC/ENT cable or Mini-Cam on-orbit cable. The specifications for the Mini-Cam extension cable are provided in Table 73-16.

**Table 73-16. Mini-Cam extension cable**

| Item         | Specification                               |
|--------------|---|
| Part no.     | SED39127626-303                             |
| Drawing no.  | SED39127626 (extension cable PPOV/Mini-Cam) |
| Manufacturer |   |
| Weight       | 0.50 lb                                     |
| Length       |   |

**73.4.4 Mini-Cam ASC/ENT Cable**

The Mini-Cam ASC/ENT cable is used only during ascent or entry to connect the Mini-Cam or Mini-Cam extension cable to the 12 V dc VIU/CM and the 8mm VTR. The specifications for the cable are provided in Table 73-17.

**Table 73-17. Mini-Cam ASC/ENT cable**

| Item         | Specification                         |
|--------------|---------------------------------------|
| Part no.     | SED39125366-301                       |
| Drawing no.  | SED39125366 (pwr cable ascent TV cam) |
| Manufacturer |                                       |
| Weight       | 0.50 lb                               |
| Length       |                                       |

#### **73.4.5 Mini-Cam Downlink Cable**

The Mini-Cam downlink cable is used during entry to route Mini-Cam video from the 8mm VTR to the PPOV VSU T-cable so the video can be downlinked real time via the S-band FM system. The specifications for the Mini-Cam downlink cable are given in Table 73-18.

**Table 73-18. Mini-Cam downlink cable**

| Item         | Specification                     |
|--------------|-----------------------------------|
| Part no.     | SED39127625-301                   |
| Drawing no.  | SED39127625 (PPOV TEAC Wye cable) |
| Manufacturer |                                   |
| Weight       | 0.50 lb                           |
| Length       |                                   |

#### **73.4.6 Bottom-of-Locker Cable**

The bottom-of-locker cable is connected to the S-band FM PL ANLG input behind the orbiter panels. One end of the cable is routed through a hole in the bottom of the 8mm VTR aft deck storage container. For entry, this cable is connected to the Mini-Cam downlink cable so that video can be downlinked via the S-band FM system.

#### **73.4.7 Mini-Cam On-Orbit Cable**

The Mini-Cam on-orbit cable can be used to route Mini-Cam video to the CCTV system. For unsynchronized Mini-Cam video, the cable is connected to the Mini-Cam or Mini-Cam extension cable and the 12 V dc VIU/CM. For synchronized video, the cable is also connected to a bal/unbal transformer. The other side of the bal/unbal transformer is connected to the Mini-Cam sync cable, which receives a sync signal from the CCTV system. The specifications for the Mini-Cam on-orbit cable are provided in Table 73-19.

**Table 73-19. Mini Cam On-Orbit Cable**

| Item         | Specification                          |
|--------------|--|
| Part no.     | SED39127626-301                        |
| Drawing no.  | SED39127626 (pwr/video cable Mini-Cam) |
| Manufacturer |  |
| Weight       | 0.50 lb                                |
| Length       |  |

#### 73.4.8 Mini-Cam Sync Cable

The Mini-Cam sync cable is used if the crew wants to route synchronous Mini-Cam video to the CCTV system. The cable connects between the bal/unbal transformer and the TV power port or the J3 SYNC/POWER connector on the pigmy cable. The specifications for the Mini-Cam sync cable are provided in Table 73-20.

**Table 73-20. Mini-Cam sync cable**

| Item         | Specification                          |
|--------------|--|
| Part no.     | SED39124816-307                        |
| Drawing no.  | SED39124816 (pigmy sync to XFMR cable) |
| Manufacturer |  |
| Weight       | 0.50 lb                                |
| Length       |  |

#### 73.4.9 ProShare Video/Power Cable

**Table 73-21. ProShare video/power cable**

| Item         | Specification   |
|--------------|-----------------|
| Part no.     | SED33109713-301 |
| Drawing no.  | SED33109713     |
| Manufacturer |                 |
| Weight       |                 |
| Length       |                 |

### 73.5 TV CONTROLLER UNIT

The TVCU is designed by Johnson Space Center Engineering. It is flown on the shuttle for basically two different purposes. Figure 73-16 provides a functional diagram.

1. In case of a RCU/VSU failure, to provide a means of independently controlling a CTVC Camera using a connected PGSC.

2. To provide amplification of either an Unbalanced Video Signal (PD-100 Camcorder) or a Balanced Video Signal prior to being input into the CCTV system.

The TV Controller Unit (TVCU) has two different modes:

1. Centerline Mode
2. Camcorder Mode

Switch S1 determines the TVCU Mode.

### **73.5.1 TVCU Centerline Mode**

TVCU Centerline Mode was designed to provide an independent means of controlling the Centerline Camera, if there is a RCU/VSU failure in the CTVC system.

The TVCU with installed PGSC will provide a means for the crew members to send centerline camera sync signals (iris, focus, etc) while viewing an image on a Flight Deck Monitor.

The Centerline Camera Balanced Video Signal enters the J4 port, gets amplified, and can be sent through any of the J3, J1, or J2 port.

A sync pulse which emulates the RCU sync pulse is generated by the internal 14.31 Mhz clock. The sync signal enters the Input/Output (I/O) Processor parallel with the incoming Centerline Camera Balanced Video Signal. The Crew will use the PGSC "TV CONTROLLER" program allowing them to use the computer to send commands such as "ALC", "AVG", "Zoom", and/or "Focus". The PGSC sends these commands via a RS-232 port to the I/O Processor. The I/O Processor will insert these codes into the "CTVC Synch Out" to control the CTVC.

### **73.5.2 TVCU Camcorder Mode**

TVCU Camcorder Mode is normally used during ISS/Shuttle docking configurations. Due to the physical distance this video signal needs to travel, the TVCU is used to amplify the unbalanced video signal from the PD-100 Camcorder located in the ISS and route it to the shuttle CCTV VPU → VSU as a video input.

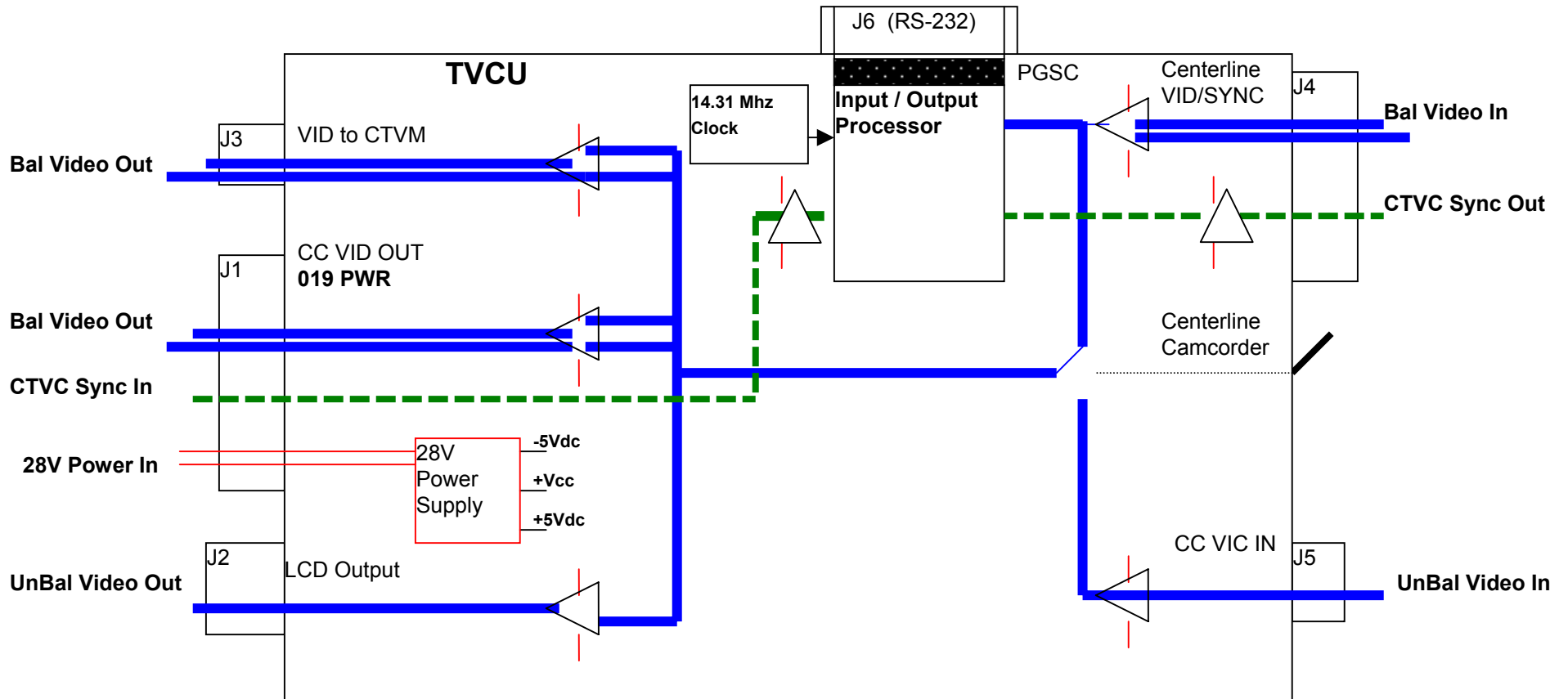


Figure 73-16. TVCU Functional Diagram

## **73.6 MISCELLANEOUS EQUIPMENT**

### **73.6.1 Bal/Unbal Transformer**

The bal/unbal transformer (SED39124190-301) has been previously mentioned. A bal/unbal transformer can also be flown separately for flight-specific requirements. This transformer converts balanced orbiter video to unbalanced video or vice versa.

### **73.6.2 RCA-RCA Cable**

The RCA-RCA cable is used to connect two video components that have RCA ports. This cable is primarily used to meet flight-specific requirements.

### **73.6.3 Y-C Cable**

The Y-C cable can be used by the crew when editing video between two camcorders. This cable provides better quality video for editing than the RCA-RCA cable.

### **73.6.4 Adapters**

Several adapters are available for interfacing video cables and components: the RCA-BNC adapter (SED33106400-301); BNC-RCA phono adapter (SED39122368-001); and the BNC T-adapter (SED39122270-003). These adapters are primarily used for flight-specific requirements.

### **73.6.5 Portable Digital Cameras**

The crew members take still pictures using portable digital cameras with digital memory sticks (1GB PCMCIA microdrives). It is possible to put two PCMCIA microdrives in one camera, but we train the crew to use one at a time. Depending on the complexity of the image, one microdrive can hold between 135 and 140 images. Images are typically 6 to 7 MB in size in a raw Kodak proprietary .dcr format.

THIS PAGE INTENTIONALLY BLANK

**SECTION 74 - COLOR TELEVISION MONITOR**  
**CONTENTS**

| <b>Section</b> |  | <b>Page</b> |
|----------------|--|-------------|
| 74.1           | GENERAL DESCRIPTION.....               | 74-1        |
| 74.1.1         | Use/Function.....                      | 74-1        |
| 74.1.2         | Interfaces.....                        | 74-1        |
| 74.1.3         | Block Diagram.....                     | 74-2        |
| 74.2           | DESCRIPTION.....                       | 74-3        |
| 74.2.1         | Electrical.....                        | 74-3        |
| 74.2.2         | Mechanical.....                        | 74-4        |
| 74.2.3         | Onscreen Graphics.....                 | 74-5        |
| 74.2.4         | Controls.....                          | 74-12       |
| 74.2.5         | Signal Processing.....                 | 74-13       |
| 74.3           | INSTALLATION.....                      | 74-18       |
| 74.3.1         | Location.....                          | 74-18       |
| 74.3.2         | Cooling.....                           | 74-18       |
| 74.4           | DESCRIPTION OF OPERATION.....          | 74-18       |
| 74.5           | TELEMETRY.....                         | 74-18       |
| 74.6           | OPERATING INSTRUCTIONS.....            | 74-18       |
| 74.7           | CONNECTOR PINOUTS.....                 | 74-19       |
| 74.8           | REFERENCES.....                        | 74-22       |
| 74.8.1         | Narrative.....                         | 74-22       |
| 74.8.2         | Drawings.....                          | 74-22       |
| 74.9           | COLOR TV MONITOR FLIGHT ANOMALIES..... | 74-22       |



## TABLES

| Table |  | Page  |
|-------|--|-------|
| 74-1  | Electrical specifications .....                                  | 74-3  |
| 74-2  | Optical and mechanical specifications.....                       | 74-4  |
| 74-3  | VSU-generated onscreen data graphics .....                       | 74-10 |
| 74-4  | CTVM-generated onscreen data graphics.....                       | 74-11 |
| 74-5  | Connector designator functions, part numbers, and locations..... | 74-19 |
| 74-6  | Connector designator pin numbers and functions .....             | 74-20 |

## FIGURES

| Figure |                                    | Page  |
|--------|------------------------------------|-------|
| 74-1   | Block diagram of CTVM .....        | 74-2  |
| 74-2   | Onscreen menu graphics .....       | 74-5  |
| 74-3   | Onscreen VSU-generated data .....  | 74-9  |
| 74-4   | Onscreen CTVM-generated data ..... | 74-9  |
| 74-5   | CTVM front panel .....             | 74-13 |
| 74-6   | CTVM front view.....               | 74-21 |
| 74-7   | CTVM rear view .....               | 74-21 |
| 74-8   | CTVM side view .....               | 74-22 |

## SECTION 74 COLOR TELEVISION MONITOR

### 74.1 GENERAL DESCRIPTION

The Color Television Monitor (CTVM) is a replacement for the existing orbiter monochrome monitors. The CTVM was built by GE AstroSpace Systems (formerly RCA AstroSpace Systems) of Hightstown, NJ, with design inputs for the Field Sequential Color (FSC) converter from NASA/JSC, EE26. The CTVM replaces the existing monitors one for one, duplicating all current functions while adding new capabilities. A pair of CTVMs mount at panel location A3, above the Remote Manipulator System (RMS) hand controller in the aft flight deck. The CTVM can display National Television System Committee (NTSC) standard broadcast color, orbiter FSC, and monochrome (black and white) signals. The new monitor design also includes three inputs not present on the old monitors ("C" and "D" on the front and rear panels and RGB on the rear panel) and an internal split screen capability (inputs "C" and "D" only). Functions are selected by an onscreen menu described herein.

#### 74.1.1 Use/Function

The CTVM is used to display video signals (television pictures) from the orbiter Closed Circuit Television (CCTV) system or from directly connected video generating devices. The CTVM also displays crosshair and camera data to aid in CCTV system use.

#### 74.1.2 Interfaces

The CTVM interfaces with the following orbiter systems.

- Electrical Power Distribution System (EPDS)
- Environmental Control and Life Support System (ECLSS)
- Orbiter CCTV system

##### A. EPDS

Each CTVM is supplied with 28 volts direct current (V dc) from a main bus through a 5-amp circuit breaker (cb). Monitor 1 (upper monitor) is supplied from VmnA, R14, and monitor 2 from VmnB, R14. Both cb's are on panel R14, row D, and are labeled MN A(B), TV, MON 1(2), cb 38(43).

##### B. ECLSS

Each CTVM is connected to the avionics forced air system through a duct connector on the rear of the CTVM.

C. Orbiter CCTV System

The CCTV system sends each CTVM composite sync and two video lines (panel and downlink) using connector J1 on the rear of each monitor.

74.1.3 Block Diagram

Figure 74-1 is a simplified block diagram of the CTVM. See SSSH drawing 16.13 for more information.

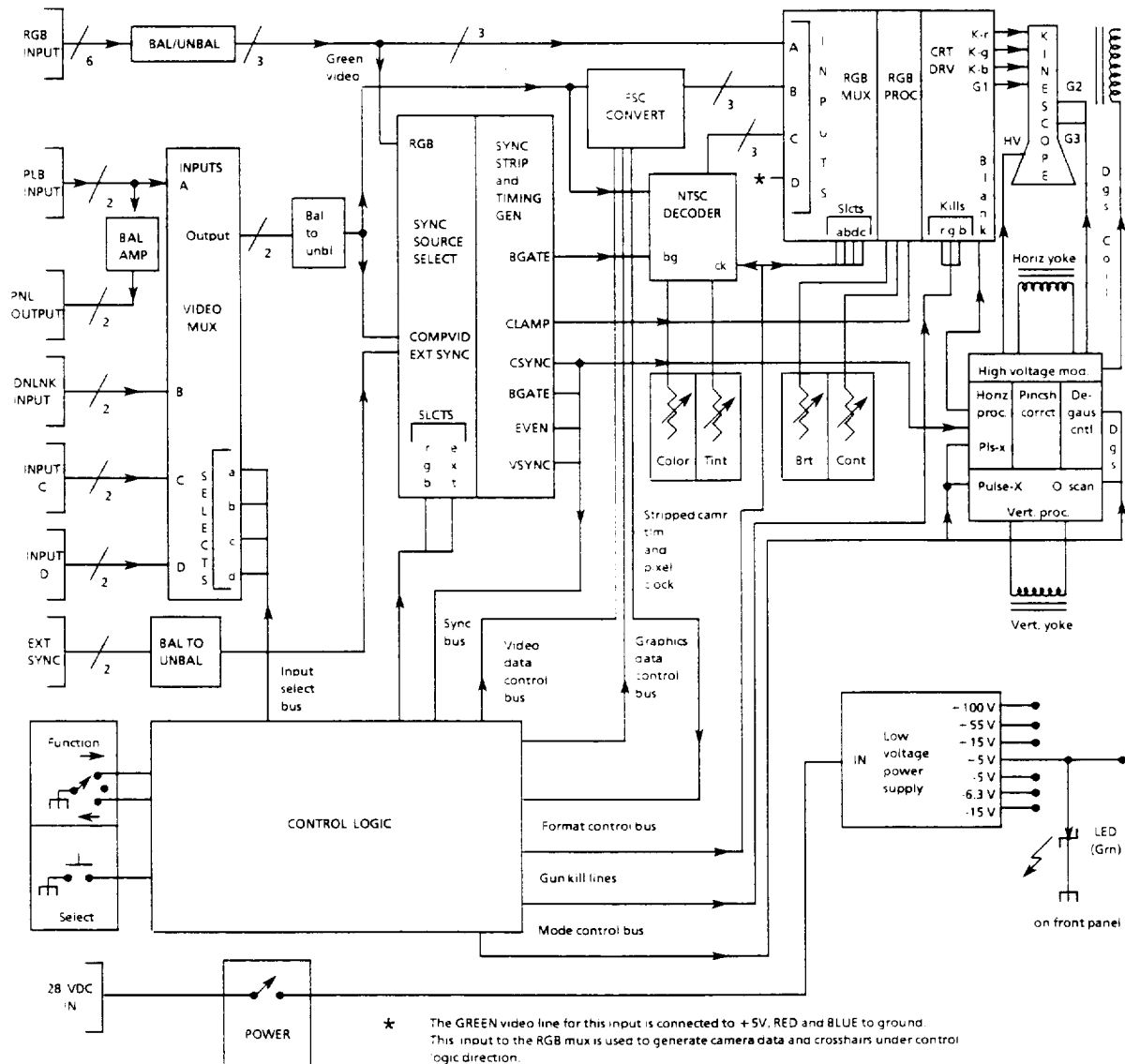


Figure 74-1. Block diagram of CTVM

## 74.2 DESCRIPTION

The following is a summary of the mechanical and electrical characteristics of the CTVM.

### 74.2.1 Electrical

Table 74-1 gives the electrical specifications for each CTVM.

**Table 74-1. Electrical specifications**

|                            |  |
|----------------------------|--|
| Supply voltage             | 24-32 V dc, steady stream  |
| Low voltage trip point     | 21.5 V dc $\pm$ 0.5 V dc   |
| Input current (nominal)    | 2.00 A   |
| Input current (maximum)    | 3.07 A   |
| LVPS protection trip point | 5.00 A nominal   |
| Video input: Type          | Balanced composite video   |
| Format                     | RS-170 compatible  |
| Level                      | 1 volt peak to peak  |
| Sync tip                   | At ground (0 volt) reference   |
| Polarity                   | Black is negative  |
| Impedance                  | 75 $\Omega$  |
| Blanking level             | +0.714 V from blanking to reference<br>white level (100 IRE units)     |
| Sync level                 | -0.286 V from blanking level<br>0 V reference to ground (40 IRE units) |
| External sync input: Type  | Balanced composite sync  |
| Level                      | 1 volt peak to peak  |
| Sync tip                   | At (0 volt) reference  |

**74.2.2 Mechanical**

Table 74-2 gives the mechanical and optical (kinescope) specifications for the CTVM.

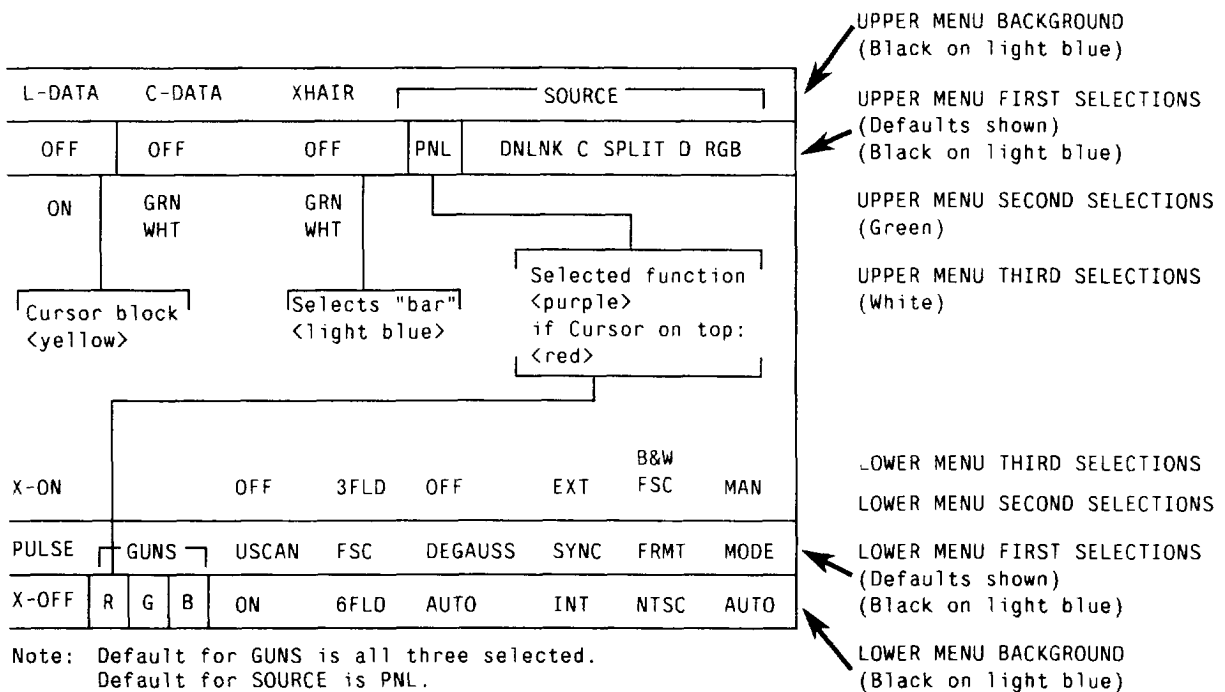
**Table 74-2. Optical and mechanical specifications**

|  |   |   |
|--|---|---|
| Dimensions (L by W by H)<br>- Each monitor<br>- Both monitors in mounting brackets   | 16 by 11.5 by 7 inches<br><br>16 by 13.86 by 15.25 inches   |   |
| Weight<br>- Each monitor<br>- Both monitors in mounting brackets   | 31.6 lb<br><br>66.7 lb  |   |
| Kinescope specifications<br>- Screen diagonal<br>- Viewable area<br>- Dot pitch<br>- Aspect ratio<br>- Contrast ratio<br>- Center resolution<br>- Deflection angle | 10 inches<br>37.7 in <sup>2</sup><br>0.28mm<br>4:3<br>45 ft-Lambert<br>32:1 (with 25 ft-candle ambient)<br>90° horizontal |   |
| Thermal<br>- Air flow required<br>- Pressure drop across CTVM<br>- Total power dissipated  | 16 CFM<br>0.65 in Hg<br>65.8 W  | - Cabin pressure<br>15.23 to 3.28 psia<br>- Cabin air temp<br>60°F to 120°F (Op)<br>-10°F to 120°F (Non-Op) |

### 74.2.3 Onscreen Graphics

#### 74.2.3.1 Onscreen Menu

The CTVM has an onscreen menu for selection of many monitor functions. See Figure 74-2 for a view of the menu graphics.



**Figure 74-2. Onscreen menu graphics**

The onscreen menu has two sets of graphics: upper and lower. Each set contains a background field at the top or bottom of the screen and a selections field, located below the upper foreground field or above the lower foreground field. The menu is brought up automatically on monitor powerup and may be brought up by pressing the SELECT or FUNCTION switches on the monitor panel. On powerup and/or the activation of either FUNCTION or SELECT switches, both the upper and lower CTVM status/menu bars temporarily appear at the top and bottom of the CRT screen for about 12 seconds. On powerup, the upper and lower menu select fields appear with the data shown as UPPER(LOWER) MENU FIRST SELECTS (defaults), and the menu cursor is over the first block (called L-DATA OFF). To move the cursor, push the FUNCTION switch in the direction of desired cursor movement. Pushing the FUNCTION switch once moves the cursor once, and holding the switch down cycles the cursor through all selections on the screen (at a rate of about two blocks every second) until the switch is released. When the cursor reaches the end of a menu "bar," it will jump to the opposite end of the other menu bar (i.e., the FUNCTION switch arrows always show the direction of cursor movement on either the upper or lower menu bars).

The selected function appears as either a legend (OFF, 3FLD, etc.) or a block similar to the cursor block, but is a different color. The SOURCE and GUNS functions are the only two which appear as a block of different color; all others appear as a legend.

A description of the CTVM menu functions follows.

| Function | Selectable states<br>(default first)          | Description  |
|----------|---|--|
| L-DATA   | OFF (ON)                                      | Disables (enables) onscreen display of solid state camera (CTVC, ITVC) lens data such as field-of-view, T-stop, etc. Provides no meaningful data on orbiter SIT Government-Furnished Equipment (GFE) cameras. See Figure 74-3 for a view of the onscreen video switching unit (VSU)-generated data graphics, and Figure 74-4 for CTVM-generated data graphics. |
| C-DATA   | OFF (GRN) (WHT)                               | Disables (enables) onscreen display of camera data (temperature, etc.) generated by the CTVM (GRN) or the VSU (WHT). GRN data are displayed in green, and WHT data are displayed in white. See Figure 74-3 for a view of the onscreen VSU generated data graphics, and Figure 74-4 for CTVM generated data graphics.   |
| XHAIR    | OFF (GRN) (WHT)                               | Disables (enables) onscreen display of the middle-of-the-screen crosshairs in green (CTVM generated) or white (VSU generated).   |
| SOURCE   | PNL (DNLNK)<br>(C)<br>(D)<br>(SPLIT)<br>(RGB) | Switches the designated video input (source) to the CTVM processing section. PNL is the VSU output for CTVM 1 or 2, DNLNK is the VSU downlink output, C and D are two spare CTVM inputs, SPLIT is a split screen multiplexer (mux) of inputs C and D, and RGB is the back panel Red, Green, Blue (RGB) input.  |
| PULSE    | X-OFF (X-ON)                                  | Disables (enables) the CTVM pulse-cross (pulse-x) function. This function shifts the display horizontally and vertically and expands the image so that the vertical and horizontal blanking and retrace interval visible. Used primarily for ground checkout.  |

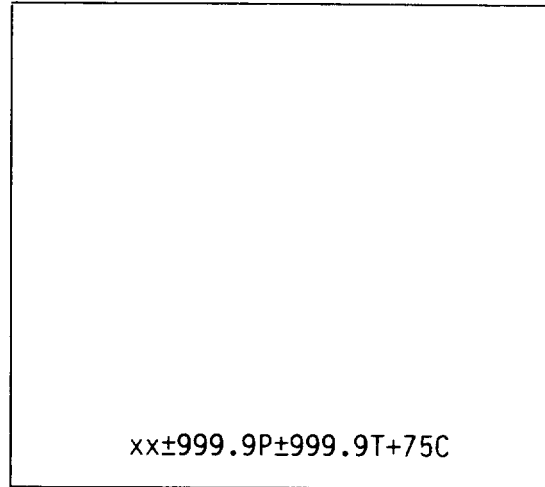
| Function | Selectable states<br>(default first) | Description  |
|----------|--------------------------------------|--|
| GUNS     | R,G,B (enabled)<br>R,G,B (disabled)  | Enables (disables) one or two of the three kinescope electron guns. The CTVM logic will not allow all three guns to be turned off at once since this would blank the display entirely. If red is off, white areas of the picture appear cyan; if green is off, white areas appear magenta; and if blue is off, white areas appear yellow. If two guns are off, white areas are in the color not disabled. Used for ground checkout of the CTVM.  |
| USCAN    | ON (OFF)                             | Enables (disables) the CTVM underscan feature. Underscan allows viewing the video frame from edge to edge with no lost image data. When in overscan mode (USCAN-OFF), about 5 percent of the total frame is lost from the four sides of the screen.  |
| FSC      | 6FLD (3FLD)                          | Selects either 6-field or 3-field conversion for FSC video signals. The 6-field conversion gives best detail resolution, while 3-field gives best motion resolution. The 6-field is fine for most uses except when rapid motion is involved.   |
| DEGAUSS  | AUTO (OFF)                           | Enables (disables) automatic degaussing of the kinescope and supporting ferrous metal structure. Degaussing is required to cancel magnetism built up in the kinescope because of orbiter attitude changes within the Earth's magnetic field. AUTO fires the degaussing circuitry once every 10 minutes, and OFF disables all degaussing. When operating, the degaussing effect may be seen as a slight disturbance in the picture, lasting about 150 milliseconds. When AUTO is selected, the circuit is immediately fired once. |



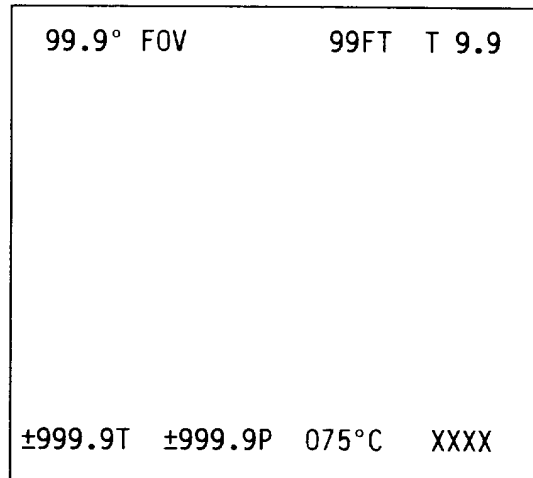
| Function | Selectable states<br>(default first) | Description   |
|----------|--------------------------------------|---|
| SYNC     | INT (EXT)                            | <p>Selects either CTVM stripped sync (internal), or Remote Control Unit (RCU)-generated sync (external). The internal sync is stripped out of the video from the selected SOURCE. If on internal sync and either the incoming video or the sync on the incoming video goes away (such as when powering down a GFE camera), the CTVM goes to external sync. Internal sync may be reselected when it returns. This is done to allow display of the menu in the absence of incoming video since the menu logic needs sync to place the menu graphics on screen. Since the camcorder is not in sync with the RCU, the CTVM should be in INT mode for camcorder video viewing.</p> |
| FRMT     | NTSC (FSC) (B&W)                     | <p>Selects one of three color processing modes if MAN is selected (see next item). NTSC allows displays of NTSC signals, FSC allows display of FSC signals, and Black and White (B&amp;W) disables color processing entirely. Always displays the current processing mode.</p>  |
| MODE     | AUTO (MAN)                           | <p>Selects either automatic or manual selection of the color processing mode. To change a FRMT (see above item), MODE must be in manual (MAN). Auto defaults to NTSC in the absence of the GFE camera "green field flag" and selects FSC when it sees a flag on every third field. Since orbiter FSC (Color Lens Assembly (CLA) and Wide Lens Assembly (WLA)) cameras and B&amp;W (Monochrome Lens Assembly (MLA)) cameras both generate the flag every third field, CTVM AUTO selects FSC for both types of camera. If the flicker caused by FSC conversion of a B&amp;W signal is objectionable, then MAN B&amp;W may be selected.</p>                                      |

### 74.2.3.2 VSU and CTVM Camera Data Graphics

The VSU and the CTVM generate onscreen data graphics using measurements derived from the camera Vertical Interval Data (VID). These graphics are described in Figure 74-3 and Figure 74-4.



**Figure 74-3. Onscreen VSU-generated data**



**Figure 74-4. Onscreen CTVM-generated data**

99.9° FOV = Field-of-view measurement from new cameras (CTVC, ITVC). Not valid for current orbiter GFE SIT cameras.

99FT = Focus distance measurement from new cameras (CTVC, ITVC). Not valid for current orbiter GFE SIT cameras.

T 9.9 = T-stop measurement from new cameras (CTVC, ITVC). Not valid for current orbiter GFE SIT cameras.

±999.9P = Pan angle. Display limits -999.9° to +999.9°.

±999.9T = Tilt angle. Display limits -999.9° to +999.9°.

075°C = Camera temperature in °C. Always visible. Camera temperature telemetry limits -25° C to +75° C.

XX = Camera location Identification (ID), derived as follows.

**Table 74-3. VSU-generated onscreen data graphics**

| Location code             | Camera station ID | Common name       | Camera location ID |
|---------------------------|-------------------|-------------------|--------------------|
| 0 00000                   | Flight deck       | Flight deck       | C1                 |
| 1 00001                   | Forward bay       | Camera A          | FB                 |
| 2 00010                   | Aft bay           | Camera C          | AB                 |
| 3 00011                   | None (spare)      | None              | (Blank)            |
| 4 00100                   | None (CAB CAM 3)  | None              | (Blank)            |
| 5 00101                   | Keel              | Camera B          | KB                 |
| 6 00110                   | Port RMS          | RMS               | RP                 |
| 7 00111                   | Starboard RMS     | Camera D          | RS                 |
| 8 01000                   | Middeck           | Middeck           | C2                 |
| 9 01001                   | None (FFTS)       | Test pattern      | (Blank)            |
| 10 01010                  | None (MUX 1)      | None              | (Blank)            |
| 11 01011                  | None (MUX 2)      | None              | (Blank)            |
| 12 01100                  | None (CAB CAMR 4) | None              | (Blank)            |
| 13 01101                  | Payload 1         | (Flight Specific) | P1                 |
| 14 01110                  | Payload 2         | (Flight Specific) | P2                 |
| 15 01111                  | Payload 3         | (Flight Specific) | P3                 |
| 16 to 31<br>10000 - 11111 | Unassigned        | None              | (Blank)            |

Table 74-4 is a description of the CTVM-generated onscreen data graphics.

XXXX = Camera location ID, derived as follows.

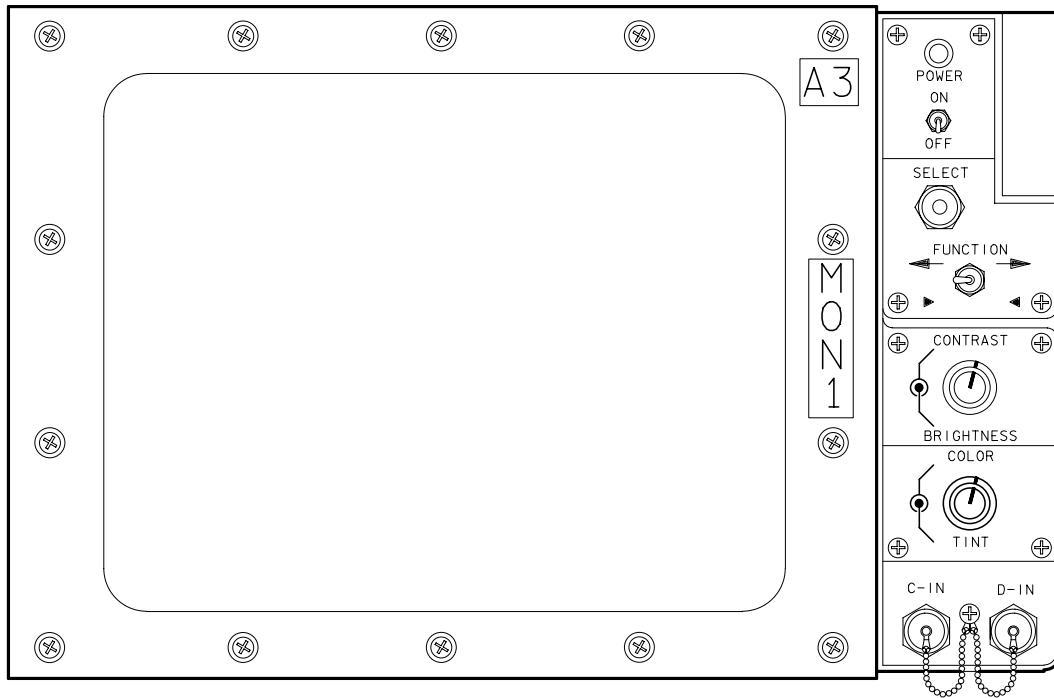
**Table 74-4. CTVM-generated onscreen data graphics**

| Location code             | Camera station ID | Common name       | Camera location ID |
|---------------------------|-------------------|-------------------|--------------------|
| 0 0000                    | Flight deck       | Flight deck       | FLT                |
| 1 0001                    | Forward bay       | Camera A          | CAMA               |
| 2 0010                    | Aft bay           | Camera C          | CAMC               |
| 3 0011                    | None (spare)      | None              | (Blank)            |
| 4 00100                   | None (CAB CAM 3)  | None              | (Blank)            |
| 5 00101                   | Keel              | Camera B          | CAMB               |
| 6 00110                   | Port RMS          | RMS               | RMS                |
| 7 00111                   | Starboard RMS     | Camera D          | CAMD               |
| 8 01000                   | Middeck           | Middeck           | MID                |
| 9 01001                   | None (FFTS)       | Test pattern      | (Blank)            |
| 10 01010                  | None (MUX 1)      | None              | (Blank)            |
| 11 01011                  | None (MUX 2)      | None              | (Blank)            |
| 12 01100                  | None (CAB CAMR 4) | None              | (Blank)            |
| 13 01101                  | Payload 1         | (Flight Specific) | P1                 |
| 14 01110                  | Payload 2         | (Flight Specific) | P2                 |
| 15 01111                  | Payload 3         | (Flight Specific) | P3                 |
| 16 to 31<br>10000 - 11111 | Unassigned        | None              | (Blank)            |

#### 74.2.4 Controls

A description of the crew-accessible controls (see Figure 74-5) follows.

| Control                 | Positions                     | Description  |
|-------------------------|-------------------------------|--|
| (LED)                   | None                          | Green power on Light-Emitting Diode (LED) indicator. When the Low Voltage Power Supply (LVPS) 5-volt output is active, this LED is on. If the LVPS has tripped off, this LED is off.   |
| POWER                   | ON (OFF)                      | Applies (removes) 28-volt main bus power to (from) the LVPS. A power cycle will reset the LVPS protection circuit.   |
| SELECT                  | (pb)                          | Pushing this pushbutton (pb) changes the menu function upon which the cursor rests.  |
| FUNCTION                | (left arrow)<br>(right arrow) | This is a center return (spring-loaded) toggle switch. When the handle is pushed to the right, the menu cursor moves to the right; and when pushed to the left, the cursor moves to the left.  |
| CONTRAST/<br>BRIGHTNESS | (rotary)                      | Dual potentiometers on concentric shafts for control of contrast/brightness. The controls have detent (semi-locking) positions in the center of their adjustment range (white line on knob faces up toward the 12 o'clock position). The detent positions are anticipated to be the normal operating positions.  |
| COLOR/<br>TINT          | (rotary)                      | Dual potentiometers on concentric shafts for control of color/tint. The controls have detent (semi-locking) positions in the center of their adjustment range (white line on knob faces up toward the 12 o'clock position). The detent positions are anticipated to be the normal operating positions. When either SOURCE=RGB or FRMT=FSC is selected, the COLOR and TINT controls do not affect the color or the tint in the display. |



186117405, PNL 1

**Figure 74-5. CTVM front panel**

## 74.2.5 Signal Processing

Refer to section 74.1.3, Block Diagram.

### 74.2.5.1 Video Input Processing

All video inputs to the CTVM are balanced, 75Ω orbiter standard. The RGB input consists of three balanced lines (red, green, and blue), with the composite sync signal interleaved into the green video. This line is available on the rear panel only. There are four composite video input lines (A, B, C, and D, also called PANEL, DOWNLINK, C, and D, respectively). Any of the three may be used for monochrome, NTSC, or FSC video. The PANEL (A) input also has a buffered output available on the rear panel. The A and B lines are available on the rear panel only, and the C and D inputs are available on both the front and rear panels. Any one of the four inputs is sent from the video input to a balanced-to-unbalanced converter and then to the sync selector, FSC converter, and the NTSC converter. Note that the control logic controls the input selection and can form a split-screen display of the C and D inputs by rapidly switching from one to the other. If split screen is used, C will be on the left, and D on the right with the sync signal being derived from the C input, and the color burst (for NTSC signals) derived from the D input. External sync may be selected during split operations but is not recommended unless both video generating devices hooked to inputs C and D are in sync with the RCU.

Note: Both C and D must be in sync with each other, so that a good split screen image may be displayed. Color (if present) will not be displayed correctly on either image because of transitional delays in the switching process.

#### 74.2.5.2 Synchronization Signal Processing

The sync source selector chooses its input based on the following:

INPUT = RGB green video line if (RGB mode • INTernal sync)

INPUT = A, B, C, or D as selected by the input selector if (A+B+C+D) • (INT)

INPUT = C if (SPLIT mode • INT)

INPUT = RCU Sync Line if (EXTernal sync) + (INT • no video coming in on selected line)

The sync source selector passes the composite video with sync to the sync stripper and timing generator for further processing.

The sync stripper removes the composite sync from the composite video and passes it to the timing generator. The timing generator produces the internal sync and timing signals needed to process and display the incoming video. The timing generator also provides composite sync for the use of the horizontal and vertical deflection systems.

Note: The timing signals needed to produce the onscreen menu graphics are produced in this section, and if there is no sync coming in, the menu cannot be displayed. This is a problem only if the RCU sync signal is not available because, on loss of incoming video (INTernal) sync, the CTVM defaults to EXTernal sync.

#### 74.2.5.3 FSC and NTSC Converters

The FSC converter digitizes the incoming video, stores it in three RAM areas (as RGB video), reads it out, and converts it back to analog. The onscreen menu graphics are also generated in the FSC converter under control of the control logic. The FSC converter output RGB video is sent to the RGB mux. The NTSC converter strips the NTSC 3.579545 MHz color subcarrier off the incoming video, demodulates the color difference signals (RED-luminance, GREEN-luminance, and BLUE-luminance), and combines these signals with delayed luminance video to produce an RGB output.

Note: The color and tint control inputs are applied to the NTSC converter and affect only NTSC color signals. The NTSC converter output is sent to the RGB mux.

#### 74.2.5.4 RGB Mux

The RGB mux receives RGB video from the FSC converter, the NTSC converter, the RGB input buffers, and a fixed-level green graphics input. The green graphics input is selected by the control logic to produce the green camera data and crosshairs. The RGB input is selected whenever the RGB input is selected on the menu. The FSC converter output is selected for display of the onscreen menu data and when FSC mode

is selected on the menu. The NTSC converter output is selected when either NTSC or B&W mode is selected on the menu. The selected input is sent to the RGB processor section.

#### **74.2.5.5 RGB Processor**

The RGB processor receives the RGB mux output and clamps the video levels to provide dc-restored RGB drive signals for the kinescope drivers. The contrast and brightness controls are applied to this section and are active in all modes. The RGB processor sends its output to the kinescope drivers.

#### **74.2.5.6 Cathode-Ray Tube (Kinescope) Drivers**

The Cathode-Ray Tube (CRT) kinescope drivers receive the output of the RGB processor and convert the voltage and current levels to those required by the kinescope cathodes. Raster blanking from the high voltage module (needed to prevent retrace lines from becoming visible) is applied to this section. The control logic sends its gun kill signals to this section. The kinescope driver section also provides grid 1 voltages for the kinescope.

#### **74.2.5.7 High Voltage Module**

The high voltage module provides three levels of high voltage for the kinescope: ultor voltage ( $\approx 20$  kV), focus grid (G3) voltage ( $\approx 7$  kV), and screen grid (G2) voltage ( $\approx 800$  V). These voltages are produced in the Integrated High Voltage Transformer (IHVT) and focus divider assembly, which receives its input from the horizontal deflection output stage. The horizontal deflection output stage is also contained in the high voltage module and drives the horizontal deflection yoke coils (located in the CRT assembly around the kinescope neck) in addition to the IHVT. The high voltage module also provides a degaussing voltage pulse to the degaussing coil (located in the CRT assembly, around the kinescope faceplate) under control of the degaussing control section.

#### **74.2.5.8 Horizontal Processor**

The horizontal processor converts the composite sync signal into horizontal and vertical drive signals. The vertical drive signal is sent to the vertical processor, and the horizontal drive signal is sent to the horizontal deflection output stage in the high voltage module. When the control logic calls for a pulse-cross (pulse-x) display, the horizontal processor alters its output to provide a horizontally shifted raster so that the horizontal blanking interval is visible.

#### **74.2.5.9 Vertical Processor**

The vertical processor receives the vertical drive signal, amplifies it, and sends it to the vertical deflection yoke coils (located in the CRT assembly around the kinescope neck). This section also sends a sample of the vertical deflection voltage to the pincushion



corrector. The vertical processor alters its operations on selection of overscan mode and pulse-x to provide either a shifted raster (pulse-x) or a taller raster (overscan).

#### 74.2.5.10 Pincushion Corrector

The pincushion corrector provides a correcting voltage to the high voltage module for elimination of pincushion distortion of the raster. Pincushion distortion results from the shape of the kinescope faceplate and shadowmask, and is corrected by changing the raster width based on the vertical position of the scan line within the raster. The pincushion corrector alters its operations in the overscan mode to that its corrections are adequate for the increased raster width.

#### 74.2.5.11 Degaussing Control

The degaussing control section sends a signal to the high voltage module which triggers a degauss cycle. The degaussing controller sends this signal based on inputs from the vertical and horizontal processor and a degauss command from the control logic, as follows:

DEGAUSS PULSE OUTPUT IF (IN VERTICAL BLANKING INTERVAL) •  
(IN HORIZONTAL BLANKING INTERVAL) •  
(CONTROL LOGIC REQUESTING DEGAUSSING)

#### 74.2.5.12 Low Voltage Power Supply

The Low Voltage Power Supply (LVPS) receives the 28 V dc input from the appropriate Vmn bus and converts it to the voltages used in the CTVM, as follows:

|          |  |
|----------|--|
| +100 VDC | CRT Drvrs  |
| +55 VDC  | High Voltage Power Supply (HVPS)                           |
| +15 VDC  | CRT Drvrs, FSC and NTSC Conv, Vert Defl, Vid Proc, Degauss |
| +5 VDC   | FSC and NTSC Conv, Vid Proc, Control Logic                 |
| -5 VDC   | Vid Proc   |
| -6.3 VDC | Kinescope heater   |
| -15 VDC  | FSC and NTSC Conv, Vert Delf, Vid Proc                     |

Note: The +100 V dc bus has a series-pass type regulator, with foldback-type overcurrent protection. The other buses have no individual regulation since the switching converter's built-in regulation is adequate for all other outputs. The LVPS has an overcurrent protection circuit which will shut the entire CTVM down when an overcurrent condition is sensed in the hexfet switch section of the LVPS. Once the overcurrent circuit trips off, power must be removed to reset the circuit. Note that the power-on LED is driven from the +5 V dc bus, so if the overcurrent protection circuit trips, the LED will not be illuminated.

#### 74.2.5.13 Control Logic

The control logic generates and controls the onscreen menu and provides logic control signals for the rest of the CTVM. The control logic is not a module or a section as such;

rather, it is integrated into the FSC converter section. The control logic (and the FSC converter) are implemented in Programmable Array Logic (PAL) devices. The internal control logic lines are controlled as follows.

SYNC SELECTS:

RGB (SYNC) SLCT = (RGB mode on menu)  
EXT (SYNC) SLCT = (EXT SYNC mode on menu)

FORMAT CONTROL BUS:

RGB MUX SLCT A = (RGB mode on menu) • (no green data pixel required)  
RGB MUX SLCT B = [(FSC mode on menu) + (menu graphics required on screen)]  
• (no green data pixel required on screen)  
RGB MUX SLCT C = [(NTSC mode on menu) + (B&W mode on menu)] • (no green  
data pixel required on screen)  
RGB MUX SLCT D = (green camera data or crosshair pixel required on screen)  
NTSC DECODER CK (color kill) = (B&W mode on menu)

GUN KILL LINES:

CRT DRV KILL R = (RED GUN KILL selected on menu)  
CRT DRV KILL G = (GREEN GUN KILL selected on menu)  
CRT DRV KILL B = (BLUE GUN KILL selected on menu)

INPUT SELECT BUS:

VIDEO MUX SELECT A = (PNL selected on menu)  
VIDEO MUX SELECT B = (DNLNK selected on menu)  
VIDEO MUX SELECT C = (C selected on menu) + [(left half of split screen required for  
display) • (SPLIT mode on menu)]  
VIDEO MUX SELECT D = (D selected on menu) + [(right half of split screen required for  
display) • (SPLIT mode on menu)]

MODE CONTROL BUS:

PULSE-X = (PULSE-X selected on menu)  
O.SCAN = (OVERSCAN selected on menu)  
DEGAUSS = (DEGAUSS AUTO selected on menu) • [(previous degauss mode was  
OFF) + (degauss timer in control logic calling for a degauss cycle)]

#### 74.2.5.14 CRT Assembly

The CRT assembly consists of the kinescope (CRT), the deflection yoke, the degaussing coil, purity and convergence magnets, a magnetic shield assembly, and the faceplate assembly. The CRT assembly mounts to the rest of the CTVM using 16 no. 6-32 cap screws through the faceplate assembly (not visible from the front of the CTVM). The faceplate assembly also contains a Lexan implosion shield, through which the kinescope face may be seen. The kinescope is a modified Toshiba E8223B22.

## 74.3 INSTALLATION

### 74.3.1 Location

The CTVMs are mounted above the RMS hand controller on the port side of the aft flight deck in panel location A3. Monitor 1 is on top, and Monitor 2 is on the bottom of the two-monitor stack.

### 74.3.2 Cooling

The CTVMs are cooled by avionics suction (forced air). Air is drawn in through four sintered bronze filters with an area of approximately 20 in<sup>2</sup>. One filter is located on the bottom cover (5.3 in<sup>2</sup>), and three on the top cover (2 in<sup>2</sup>, 7.1 in<sup>2</sup>, and 5.6 in<sup>2</sup>). The required airflow rate for each CTVM is 16 cfm at 0.65 inch of water pressure drop.

## 74.4 DESCRIPTION OF OPERATION

The CTVM has no ground commandable functions and is totally under crew control. Primary CTVM operations consist of input selection, power control, and image setup functions (brightness, contrast, color level, and tint). If needed, secondary CTVM operations consist of manual degaussing, FSC processing mode changes (3 field (FLD)/ 6 FLD), data and crosshair selection, and manual video mode selection.

## 74.5 TELEMETRY

The CTVM has no telemetry. The CTVM will, however, display camera and lens telemetry (if available in the video).

## 74.6 OPERATING INSTRUCTIONS

### A. Activation

✓cb R14:D MN A(B) TV MON 1(2) - cl  
pnl A3 MON 1(2) POWER - ON

✓LED - lit

✓Menu - on screen after kinescope warmup (about 20 seconds)

### B. Operation

Menu - Select desired input

If PNL or DNLNK:

Ensure that VSU is sending desired video to MON 1 (2) on PNL line, or downlink has active video coming down

Select FSC conversion mode (6 FLD/3 FLD) as required (6 FLD for fine detail, 3 FLD for rapid motion with less streaking)

If colors are off (out of purity):

Menu - DEGAUSS OFF, then AUTO

May be repeated at 10-minute intervals, are required to remove all residual magnetism from kinescope and shields.

If viewing video from an orbiter GFE monochrome camera:

Menu - MODE - MAN  
FRMT - B&W

Note: Selecting B&W reroutes the monochrome video to the NTSC converter, eliminating the flicker and color streaking introduced by the FSC converter. Also, the AUTO mode cannot tell the difference between orbiter FSC and orbiter B&W and defaults to FSC for GFE cameras.

## 74.7 CONNECTOR PINOUTS

See Figure 74-5, Figure 74-6, Figure 74-7, and Figure 74-8 for front, rear, and side views of the CTVM.

More data are given in Table 74-5 and Table 74-6.

**Table 74-5. Connector designator functions, part numbers, and locations**

| Connector designator | Function  | Part number    | Location            |
|----------------------|---|----------------|---------------------|
| J1                   | Video input (A&B), external sync input, power input | NLSOE12-35P*   | Rear <sup>+</sup>   |
| J2                   | Video C input                                       | KJ5E10N98PN16* | Rear <sup>++</sup>  |
| J3                   | Video A output                                      | KJ5E10N98PN16* | Rear <sup>++</sup>  |
| J4                   | Video C input                                       | BJ154AC-47**   | Rear                |
| J5                   | Video D input                                       | BJ154AC-47**   | Front               |
| J6                   | Video C input                                       | BJ154AC-47**   | Front               |
| J7                   | RGB input   | NLS0E10-35P*   | Rear <sup>+++</sup> |
| J8                   | Video D input                                       | BJ154AC-47**   | Front               |

\*MSFC specs per documents 40M38277, rev B, and 40M3956, rev E.

\*\*Trompeter Triax connectors, MIL-C 3655 spec.

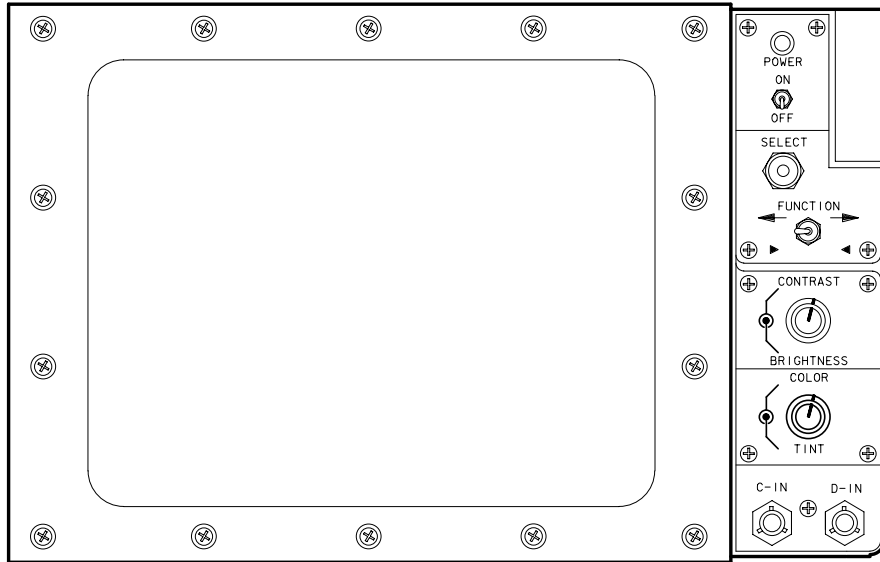
<sup>+</sup>Mating connector NLS6GT12-35S.

<sup>++</sup>Mating connector KJG6F10N98SN.

<sup>+++</sup>Mating connector TBD.

**Table 74-6. Connector designator pin numbers and functions**

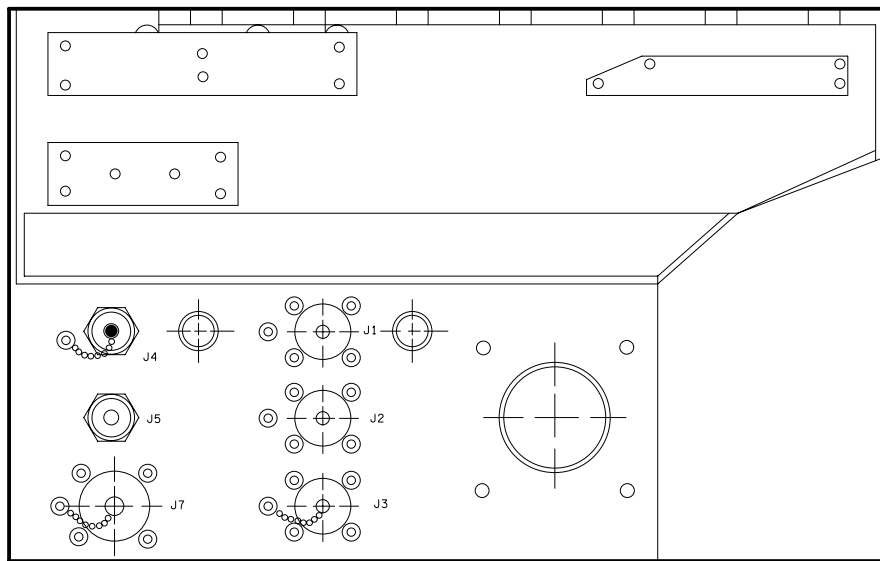
| Connector designator | Pin no.          | Function                      |
|----------------------|------------------|-------------------------------|
| J1                   | 1                | +28 V dc IN from R14 cb       |
|                      | 2                | Data/Xhair return line to VSU |
|                      | 4                | 28 V dc return (ground)       |
|                      | 5                | Data disable line to VSU      |
|                      | 6                | Xhair disable line to VSU     |
|                      | 16               | Video A in + from VSU         |
|                      | 17               | Video A in - from VSU         |
|                      | 18               | Sync + from RCU               |
|                      | 19               | Sync - from RCU               |
|                      | 20               | Video B in + from VSU (DNLNK) |
|                      | 21               | Video B in - from VSU (DNLNK) |
|                      | All others spare |                               |
| J2                   | A                | Video C in +                  |
|                      | C                | Video C in -                  |
|                      | All others spare |                               |
| J3                   | D                | Video A out +                 |
|                      | F                | Video A out -                 |
|                      | All others spare |                               |
| J4                   | 1                | Video C in +                  |
|                      | 2                | Video C in -                  |
| J5                   | 1                | Video D in +                  |
|                      | 2                | Video D in -                  |
| J6                   | 1                | Video C in +                  |
|                      | 2                | Video C in -                  |
| J7                   | 1                | RGB red video in +            |
|                      | 2                | RGB red video in -            |
|                      | 3                | Spare                         |
|                      | 4                | RGB green video in +          |
|                      | 5                | RGB green video in -          |
|                      | 6                | Spare                         |
|                      | 7                | RGB blue video in +           |
|                      | 8                | RGB blue video in -           |
|                      | 9                | TEST FUNCTION - DO NOT USE    |
|                      | 10               | TEST FUNCTION - DO NOT USE    |
|                      | 11               | TEST FUNCTION - DO NOT USE    |
|                      | 12               | TEST FUNCTION - DO NOT USE    |
|                      | 13               | Spare                         |



FRONT VIEW

186117406, PNL 1

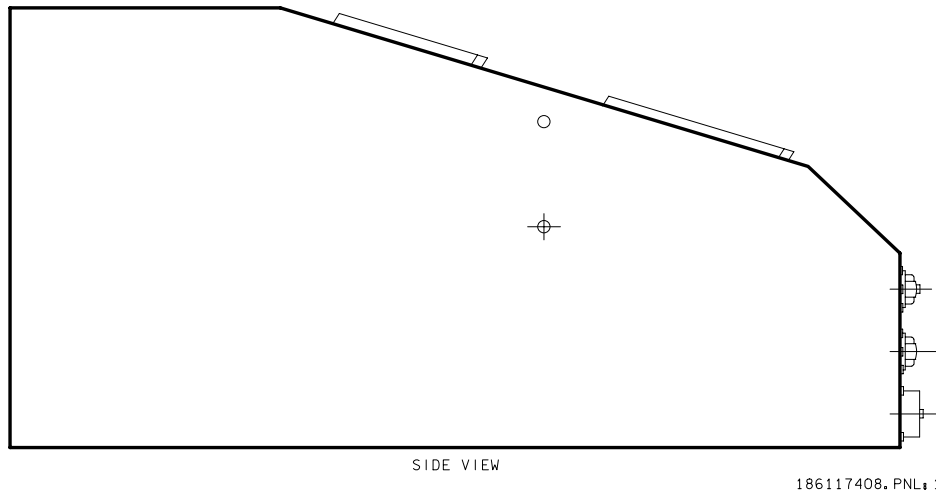
**Figure 74-6. CTVM front view**



BACK VIEW

186117407, PNL 1

**Figure 74-7. CTVM rear view**



**Figure 74-8. CTVM side view**

## 74.8 REFERENCES

### 74.8.1 Narrative

CCTV Color TV Monitors Critical Design Review, March 1988

### 74.8.2 Drawings

Color Television Monitor (CTVM) – Vendor drawing no. 3265082-50x

## 74.9 COLOR TV MONITOR FLIGHT ANOMALIES

This section summarizes anomalies that have occurred on the Color TV monitors during past missions.

Currently, the only Color TV monitor failures that have occurred have been related to a lack of cooling caused by dirty filters. In one case, a sock was found blocking the filters. The filters should be cleaned as part of scheduled maintenance.

## SECTION 75 - SEQUENTIAL STILL VIDEO

### CONTENTS

| Section |                             | Page |
|---------|-----------------------------|------|
| 75.1    | GENERAL .....               | 75-1 |
| 75.2    | DESCRIPTION .....           | 75-1 |
| 75.2.1  | Encoder .....               | 75-1 |
| 75.2.2  | SSV Ground Terminal .....   | 75-5 |
| 75.3    | PERFORMANCE .....           | 75-6 |
| 75.4    | DATA DOWNLINK .....         | 75-6 |
| 75.5    | ENCODER OPERATIONS .....    | 75-6 |
| 75.6    | MCC Ground operations ..... | 75-7 |
| 75.7    | SSV VIDEO Telemetry .....   | 75-8 |

### TABLES

| Table |   |      |
|-------|---|------|
| 75-1  | Encoder Specifications .....                                | 75-2 |
| 75-2  | Video "IN_SEL" Switch Positions. ....                       | 75-4 |
| 75-3  | Standard Program Data Output Rate Switch Positions. ....    | 75-4 |
| 75-4  | Standard Program Quality Output Rate Switch Positions. .... | 75-5 |
| 75-5  | Ground Terminal Equipment .....                             | 75-5 |
| 75-6  | Ground Terminal Boot-up Actions .....                       | 75-7 |
| 75-7  | Ground Terminal Status, Good Video Data Received .....      | 75-8 |
| 75-8  | Ground Terminal Statusing, No Video Data Received .....     | 75-8 |
| 75-9  | Ground Terminal Power Down .....                            | 75-8 |

### FIGURES

| Figure |                           |      |
|--------|---------------------------|------|
| 75-1   | SSV Flight Hardware ..... | 75-2 |
| 75-2   | Encoder Front Panel ..... | 75-3 |



THIS PAGE INTENTIONALLY BLANK

## SECTION 75 SEQUENTIAL STILL VIDEO

### 75.1 GENERAL

Johnson Space Center (JSC) NASA EV2 Division is the engineering developer of the Sequential Still Video (SSV) System. The SSV system is used to process orbiter video into a still frame or picture-in-picture format for low data bandwidth transfer to the ground. The SSV receives an analog NTSC picture, converts it to a digital signal, ships it to the Payload Data Interleaver (PDI) for downlink formatting to the ground via the S-Band – PM System. The SSV Output can provide several different still frame data rates, ranging from 1 Kbps to 8Mbps. The system will receive video input from any standard onboard NTSC composite or Y/C component video system.

### 75.2 DESCRIPTION

SSV through low data rate snap shot transfer provides a means transferring sequential still video to the ground, anytime the orbiter has downlink communication path. The quality and transfer rate of the still sequential pictures is dependent on the SSV Encoder, Orbiter TFL/DFL, and ground network configuration.

The SSV allows a less robust alternative to the current shuttle Closed Circuit Television (CCTV) system, which only allows for NTSC analog video to be downlinked via the Ku-Band Channel 3 System.

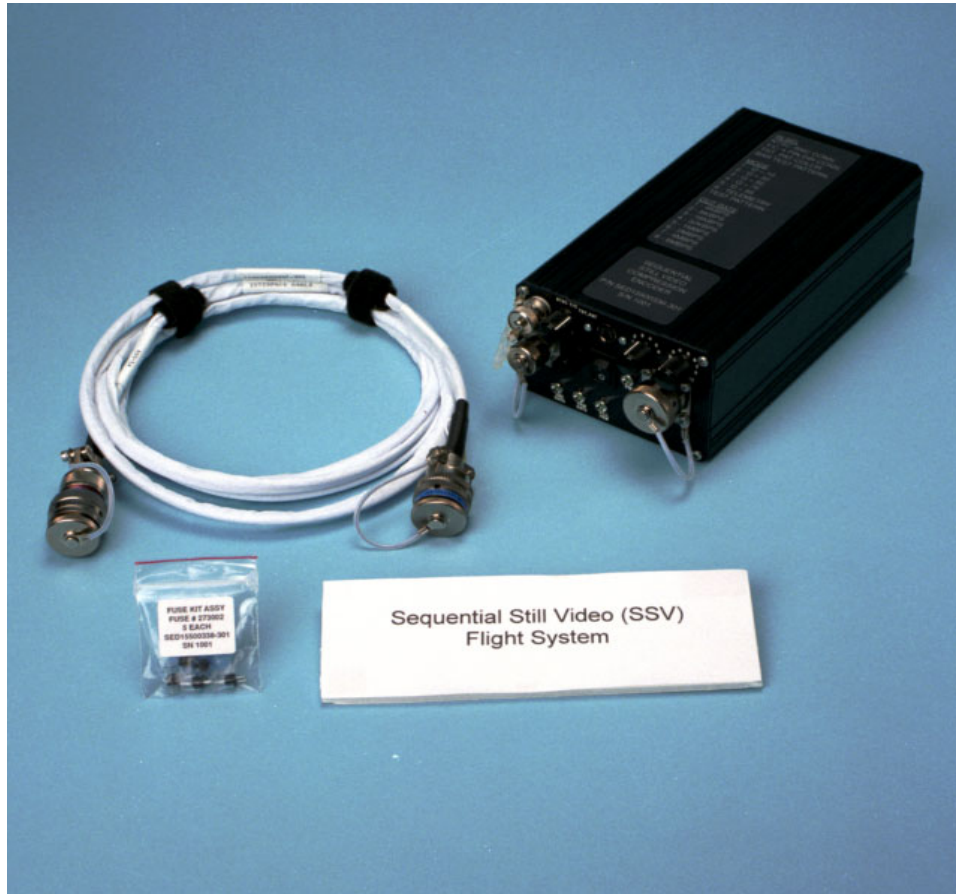
The SSV System is divided into two major parts, the SSV Encoder (onboard equipment) and the SSV Ground Terminal. The SSV Encoder processes video into a digital data stream for downlink data transfer. The Ground Terminal processes the encoder data back into a usable video signal for ground distribution. These two major components will be discussed in independent sections.

#### 75.2.1 Encoder

Figure 75-1 shows a picture of the physical SSV Flight Hardware with SSV Encoder, cables, and video balance/unbalance transformer.

SSV Encoder and associated components are usually stowed during ascent and entry phases of flight, in crew storage compartments. On orbit, the encoder is usually cabled, front panel configured, and mounted behind the onboard CCTV Monitors with Velcro.

Significant SSV Encoder specifications are listed in Table 75-1.



**Figure 75-1. SSV Flight Hardware**

**Table 75-1. Encoder Specifications**

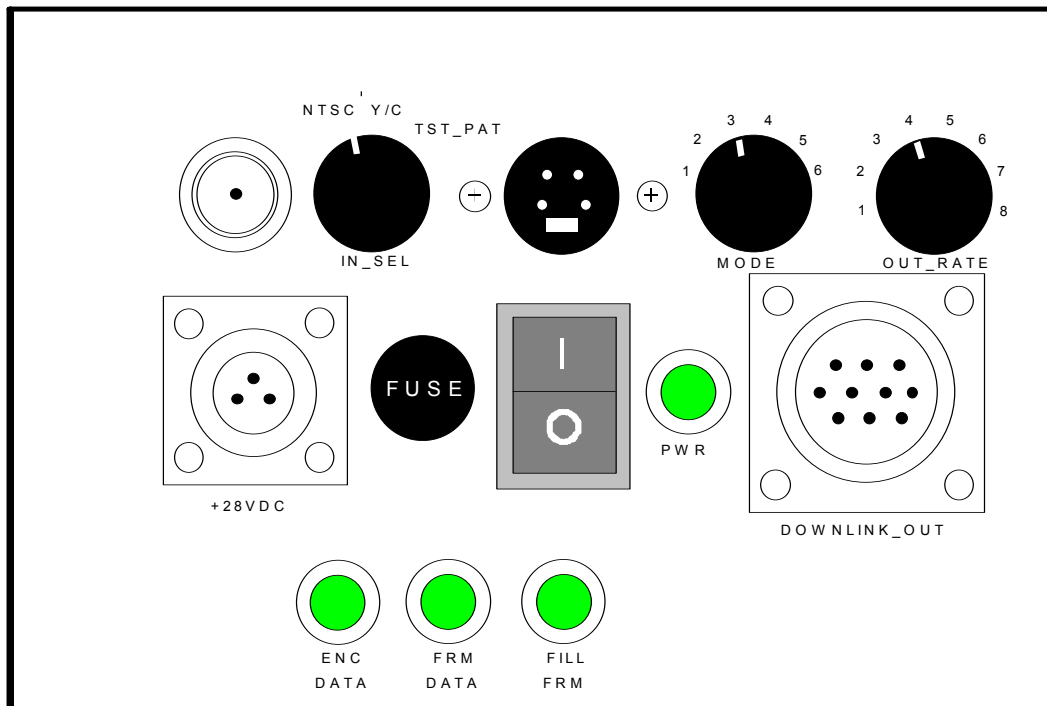
| ITEM              | Description                       |
|-------------------|-----------------------------------|
| Weight            | 7 lbs                             |
| Size              | 2.72" (H) x 4.25"(w) x 8.50" (L)  |
| Power Usage       | +28Vdc @ approximately 11.2 Watts |
| Cooling           | Free Air                          |
| Operational Temp. | 32 °F to 120 °F                   |

**75.2.1.1 Power**

SSV Encoder Unit uses +28 Volts dc from the orbiter +28V dc Utility Outlets. The unit draws between 0.4 and 0.7 Amps of current. Nominal unit power usage is approximately 11.2 watts.

The power cable used with the unit is of the same type as that used with the PGSCs. The power cable connects to the unit front panel, where all the display and controls are. See Figure 75-2 for front panel view.

The SSV Encoder front panel has a power switch, green power indicator, and an accessible 2 Amp fuse. A Fuse Kit (SED 15500338-301) is usually flown with the unit and carries 5 Littlefuse 273002 plastic miniature fuses.



**Figure 75-2. Encoder Front Panel**

### 75.2.1.2 Encoder Input

The SSV Encoder has three video input sources; NTSC composite video via a BNC connector, Y/C component video via a 4 pin DIN connector, and an internal color bar test pattern. The video source to be processed is selected by use of the “IN\_SEL” rotary switch. Normally in flight, the “IN\_SEL” configuration is NTSC.

See Figure 75-2 for switch location. Table 75-2 provides the video “IN\_SEL” positions.

**Table 75-2. Video “IN\_SEL” Switch Positions.**

| Position | Device selected                         |
|----------|---|
| NTSC     | BNC connector for composite video       |
| Y/C      | 4 pin DIN connector for component video |
| TST_PAT  | Internal color bar test pattern         |

### 75.2.1.3 Encoder Output

The SSV clock and data output is NRZ-L with a 0 degree clock, a frame size of 1024 bytes, and frame sync of 1ACFFC1D. Up to 8 data rates are pre-mission programmable from 1 Kbps to 8 Mbps. See the Table 75-3 for the standard programmed rates. The internally generated color bar test pattern is a 1024 fill frame.

**Table 75-3. Standard Program Data Output Rate Switch Positions.**

| Position | Output Rate |
|----------|-------------|
| 1        | 4 Kbps      |
| 2        | 8 Kbps      |
| 3        | 16 Kbps     |
| 4        | 25 Kbps     |
| 5        | 32 Kbps     |
| 6        | 64 Kbps     |
| 7        | 2 Mbps      |
| 8        | 4 Mbps      |

### 75.2.1.4 Video Compression

The image quality output can be selected via the “Mode” rotary switch. Quality mode switch selections are programmable and can be pre-mission programmed. A “Q” is a scaling factor applied to quantization levels of the discrete cosine transform coefficients. A large Q means that these coefficients are quantized finely, producing a better picture. Likewise if the Q value is small, then the coefficients have been quantized roughly, and will produce a poor picture. Thus Q relates to image quality with 100 being the best image quality and 1 being the worst image quality. Table 75-4 shows the standard pre-programmed “Q” positions for the “Mode” rotary switch. Normally in flight, the “MODE” switch is in the “3” position, which allows a Q value of “50”.

The Telemetry Test Pattern position of the quality switch provides a ones and zero field test pattern on the encoder output. Field test pattern position is not typically used.

**Table 75-4. Standard Program  
Quality Output Rate Switch Positions**

| Mode | Selected quality (Q)   |
|------|------------------------|
| 1    | Q=10                   |
| 2    | Q=30                   |
| 3    | Q=50                   |
| 4    | Q=70                   |
| 5    | Q=85                   |
| 6    | Telemetry Test pattern |

#### 75.2.1.5 Status Indicators

SSV Encoder has three green status indicators located on the front panel. These indicators will flash when video is being received and processed by the encoder unit. Static indication of the Frame Data or Fill Frame indicators could indicate improper front panel configuration or internal component failure. Encoded Data indicator will flash to fast for the human eye to see, when encoder is processing a good video signal. No light on the Encoded Data indicator could suggest no video being received for processing, panel "IN\_SEL" not configured properly, or front end failure of encoder.

#### 75.2.2 SSV Ground Terminal

The SSV Ground Terminal processes data received from the SSV Encoder, and returns it as video snap-shots. The video is then made available for the user community in Y/C Component and NTSC Composite Video. Table 75-5 list the equipment used to make-up the ground terminal system.

**Table 75-5. Ground Terminal Equipment**

| ITEM                   | Description  |
|------------------------|--|
| Console Terminal       | 33mhz 486 Processor w/ Keyboard and Monochrome Monitor |
| Distribution Amplifier | For NTSC Composite Video Distribution                  |
| Video Converter        | For Conversion of Y/C to NTSC Video                    |
| Color Monitor          | NTSC Video Base-band Monitor                           |
| A/B Video Switch.      | Video Control Switch user Community                    |

Ground terminal equipment is located in the INCO MSPR on a table, between the INST and RF COMM Consoles.

##### 75.2.2.1 Ground Terminal Description

The SSV Ground terminal consist of a 33mhz 486 processor, with an SSV two card set for processing SSV Data, DOS 5.0 Operating System, and special SSV Software. The terminal looks and operates like a standard PC, but has no user applications installed.

The SSV cards inside process the SSV data provided from the encoder, and outputs it as Y/C Component and NTSC Composite Video formats. The SSV card set and software can sync with any incoming data rate and quality from the SSV Encoder, and will update the user video output as required.

### 75.3 PERFORMANCE

The SSV samples video at 640 (H) x 480 (V) square pixels (deinterlaced to 240) or at 12.27272 MHz. The SSV digitizes to 8 bits per colorplane, (i.e., 8 bits per component sample), resulting in 24 bits per pixel. A YCBCR colorspace is used with 4:2:2 sampling, with component samples either luminance (Y), Color blue (Cb), or Color red (Cr). Thus, an average scene will require 320 Kbits per frame.

### 75.4 DATA DOWNLINK

The SSV data is normally downlinked using the Payload Data Interleaver (PDI). The data rates are pre-mission configured and agreed upon. The time it takes to downlink one still frame image is dependent on the downlink Frame Rate and the Image Quality selected. This time can typically be calculated by use of the following formula:

$$320\text{Kbits (Average Scene per Frame) / PDI data rate} = X \text{ (Time in Seconds)*}$$

(\*Typical Reference for frame update rate = 10 sec. per frame at 32Kbps)

Note: It takes 2 complete images for the ground processors to process a new scene. Time for the first frame should always be expected to take twice the amount of time for an average update.

The SSV is normally only cable connected to the PDI, but there is the pre-flight option to cable SSV output to the Ku-band payload digital input, if a much higher data rate downlink is required.

### 75.5 ENCODER OPERATIONS

Current flight configuration requires crew member unstow and configure the SSV per the mission specific Photo TV Flight Data File. The crewmember is required to connect the encoder to a video source, connect power and PDI data cables, and place it in the appropriate onboard location for proper cooling. A crewman is also required to configure the IN\_SEL, MODE, and OUT\_RATE rotary switches.

When a different configuration is desired, the rotary switches must be moved to the new desired configuration, and a unit power cycle must be performed for the encoder to recognize and implement the new configuration changes. The crew can tell when power is applied to the encoder via the green PWR indicator on the front of the unit. The crewman can also tell if the encoder is processing video by the data status indicators.

The orbiter Telemetry Format Load (TFL) and DECOM Format Load (DFL) must be properly configured onboard and matched to the SSV Encoder data rate output, in order for the SSV data to be developed on the ground. The Instrumentation Officer is usually responsible for making these changes per flight plan timeline.

## 75.6 MCC GROUND OPERATIONS

Prior to the SSV data transfers, the Instrumentation Officer will power on all SSV Ground Terminal Equipment, and have the Video “Blank” Switch in the “Off” state, to avoid unwanted crew screens to be released to the user community. The Instrumentation Officer will then take the appropriate actions to start the Ground Terminal processing of the SSV Data. See Table 75-6 for ground terminal operation actions.

**Table 75-6. Ground Terminal Boot-up Actions**

| <b>SSV Ground Equipment - Power Up</b>  |
|---|
| Base Band (BB) Monitor Power - ON<br>CPU/Monitor Power - ON<br>Verify 'Kill' Switch Position – A or “OFF” State<br>At prompt, type (not case sensitive):<br>C<br>RTN key<br>SBYT1<br>RTN key<br>RTN key<br><br>Verify that program initialized correctly<br>Ck: Computer monitor display (see next table) |

Once all TFL/DFL, crew, and ground console actions are complete, video should appear on the BB Monitor, after the proper allotted time for building video frames has occurred. The Ground Terminal status display should look similar to Table 75-7. If the ground terminal is not receiving SSV Data, the Ground Terminal status will appear similar to the information seen in Table 75-8.

When all appears well with the SSV ground data, and the SSV Video is not displaying unwanted crew scenes, the “On/OFF” or A/B video switch can be placed in the “ON” state for the User Community to receive SSV video.

At the completion of SSV Operations, the Instrumentation Officer will power-down the ground terminal equipment, as described in Table 75-9.



## 75.7 SSV VIDEO TELEMETRY

SSV Telemetry is embedded within the video image. The only SSV video telemetry is shown on the CPU display in Table 75-5. Information on Clock, Data Frame, Rate, and Mode information is displayed on the Ground Processing Display.

**Table 75-7. Ground Terminal Status, Good Video Data Received**

```

*** De-framer Status ***
Reset done:      Received
Clock:          Clk/Data Locked
Frame:          Locked
Dfail:          Received
Start of frame: Received
Data polarity:  Inverted
Fill Frame:     Not Receiving

*** De-framer telemetry ***
Status byte 1 = 10 Status byte 2 = ff8c
Status byte 3 = 0  Status byte 4 = 64
VCID = 38 Output Rate Select: 4

*** Video Digitizer and Encoder Telemetry ***
Video input:    Composite
Compression Mode: 3  Q value: 50

Re-writing Q tables before each frame
Hit Enter to exit....
End of Bt858 / Display Init (brkinnt1)
    
```

**Table 75-8. Ground Terminal Statusing, No Video Data Received**

```

*** De-framer Status ***
Reset done:      Received
Clock:          No Clock  Clock Search:  Searching
    
```

**Table 75-9. Ground Terminal Power Down**

| <b>SSV Ground Equipment - Power Down</b> |
|--|
| BB Monitor Power - OFF                   |
| CPU/Monitor Power - OFF                  |

**SECTION 76 - DIGITAL TELEVISION**

**CONTENTS**

| <b>Section</b> |  | <b>Page</b> |
|----------------|--|-------------|
| 76.1           | DIGITAL TELEVISION .....                           | 76-1        |
| 76.1.1         | Background .....                                   | 76-1        |
| 76.2           | VERTICAL INTERVAL PROCESSOR (VIP) .....            | 76-4        |
| 76.2.1         | Background .....                                   | 76-4        |
| 76.2.2         | VIP Inputs and Outputs .....                       | 76-4        |
| 76.2.3         | VIP Signal Process .....                           | 76-4        |
| 76.2.4         | VIP Requirements .....                             | 76-5        |
| 76.2.5         | VIP Telemetry .....                                | 76-6        |
| 76.2.6         | VIP Power .....                                    | 76-6        |
| 76.2.7         | VIP Switches .....                                 | 76-7        |
| 76.2.8         | VIP LEDs.....                                      | 76-7        |
| 76.2.9         | VIP FUSES .....                                    | 76-7        |
| 76.3           | VIP PATCH PANEL .....                              | 76-8        |
| 76.3.1         | Background .....                                   | 76-8        |
| 76.3.2         | VIP Patch Panel Connection Description .....       | 76-8        |
| 76.3.3         | Panel L10 VIP Patch Panel Back Cable Routing ..... | 76-9        |
| 76.4           | DIGITAL RECORDER (DSR-20).....                     | 76-10       |
| 76.4.1         | Background .....                                   | 76-10       |
| 76.4.2         | Digital Recorder (DSR-20) Telemetry .....          | 76-11       |
| 76.4.3         | Digital Recorder (DSR-20) Power .....              | 76-11       |
| 76.4.4         | DSR-20 Operations.....                             | 76-11       |
| 76.4.5         | VTR Requirements.....                              | 76-11       |
| 76.5           | DIGITAL MUX .....                                  | 76-12       |
| 76.5.1         | Background .....                                   | 76-12       |
| 76.5.2         | Digital MUX Power .....                            | 76-14       |
| 76.5.3         | Digital MUX Switches and LEDs .....                | 76-15       |
| 76.5.4         | DTV MUX MAIN BOARD Requirements .....              | 76-16       |
| 76.5.5         | Optical Channel Troubleshooting .....              | 76-16       |
| 76.5.6         | Fiber Optic Indicators .....                       | 76-17       |
| 76.5.7         | IEEE 1394 Indicator .....                          | 76-18       |
| 76.5.8         | Output Relay Select .....                          | 76-19       |
| 76.5.9         | Digital MUX Main Board.....                        | 76-21       |
| 76.5.10        | DTV Flight Deck Location.....                      | 76-28       |
| 76.5.11        | DTV Shuttle Interfaces .....                       | 76-28       |

## TABLES

| Table |                                   | Page  |
|-------|-----------------------------------|-------|
| 76-1  | Rate Select Switch .....          | 76-15 |
| 76-2  | Rate Switch Troubleshooting ..... | 76-17 |

## FIGURES

| Figure |  |       |
|--------|--|-------|
| 76-1   | DTV .....  | 76-3  |
| 76-2   | VIP .....  | 76-6  |
| 76-3   | VIP Patch Panel .....                                | 76-8  |
| 76-4   | VIP Patch Panel Rear Cabling to VIP and DSR-20 ..... | 76-9  |
| 76-5   | DSR-20 .....   | 76-10 |
| 76-6   | Digital MUX .....                                    | 76-13 |
| 76-7   | Panel R1 .....                                       | 76-14 |
| 76-8   | Digital MUX Front Panel Label .....                  | 76-16 |
| 76-9   | Optical Channel (1 of 3) Front Panel Display .....   | 76-18 |
| 76-10  | IEEE 1394 Front Panel Display .....                  | 76-18 |
| 76-11  | Rate Switch .....                                    | 76-19 |
| 76-12  | Digital Mux Front and Back Panel Ports .....         | 76-20 |
| 76-13  | EPLD to 1805 Micro Processor Protocol .....          | 76-21 |
| 76-14  | DMUX Telemetry Format .....                          | 76-25 |
| 76-15  | DTV Flight Deck Location .....                       | 76-28 |
| 76-16  | DTV Shuttle Interface .....                          | 76-29 |

## SECTION 76 DIGITAL TELEVISION

### 76.1 DIGITAL TELEVISION

#### 76.1.1 Background

The United States (U.S.) television standard is in the process of transitioning from the current analog National Television Systems Committee (NTSC) format to the digital television (DTV) Advanced Television Systems Committee (ATSC) format as adopted by the Federal Communications Commission (FCC). The Space Shuttle Program will take an incremental approach to DTV implementation. Multiple DTV configurations will be phased in with each configuration providing a fully functional system that is compatible with the U.S. DTV standard. The initial operational system described in this document will be a standard definition television (SDTV) system, designated as DTV System Configuration 1. This initial operational DTV system will be integrated into the Space Shuttle Orbiter as a first step toward the complete transition of the Space Shuttle Orbiter video systems from analog NTSC to DTV. The system will be designed and built to facilitate meeting the following objectives:

- 1) Provide a fully functional DTV system made up of components that are fully compatible with each other and with the U.S. DTV standard.
- 2) Provide a means to digitize and compress the current closed circuit television (CCTV) system analog video signals for digital recording, playback, and downlink.
- 3) Provide a digital video tape recorder (VTR) replacement for the current Orbiter analog VTRs.
- 4) Provide a digital camcorder for origination and recording of Orbiter digital video as a replacement for the current analog camcorder.
- 5) Provide for digital downlink of all Orbiter video.
- 6) Provide improved on-orbit video editing capabilities.
- 7) Utilize an improved videotape format for enhanced videotape archiving and duplication quality.
- 8) Improve reliability and performance of flight video systems.
- 9) Provide infrastructure required for equipment upgrades, including interfaces required for integration of both high definition television (HDTV) and additional SDTV capabilities in future configurations of the DTV system.
- 10) Provide for commonality of flight equipment between the Space Shuttle and International Space Station (ISS) Programs, where possible. Utilize industry standards for signal interfaces, where possible.

The Digital Television System (DTS) Configuration 1 includes the following four components:

- **Vertical Interval Processor (VIP):** Component which copies the Vertical Interval from the CTVC Signal.
- **VIP Patch Panel:** Component which allows the crew to receive the Video and Audio Signals.
- **Digital Recorder (DSR-20):** Component which allows the crew to Digitally Tape Video Signal.
- **Digital Multiplexer (DMUX):** Component which receives a Digital Video Signal and ships it to the Ku-Band Signal Processor Assembly.

Figure 76-1 shows these components on Panel L10.

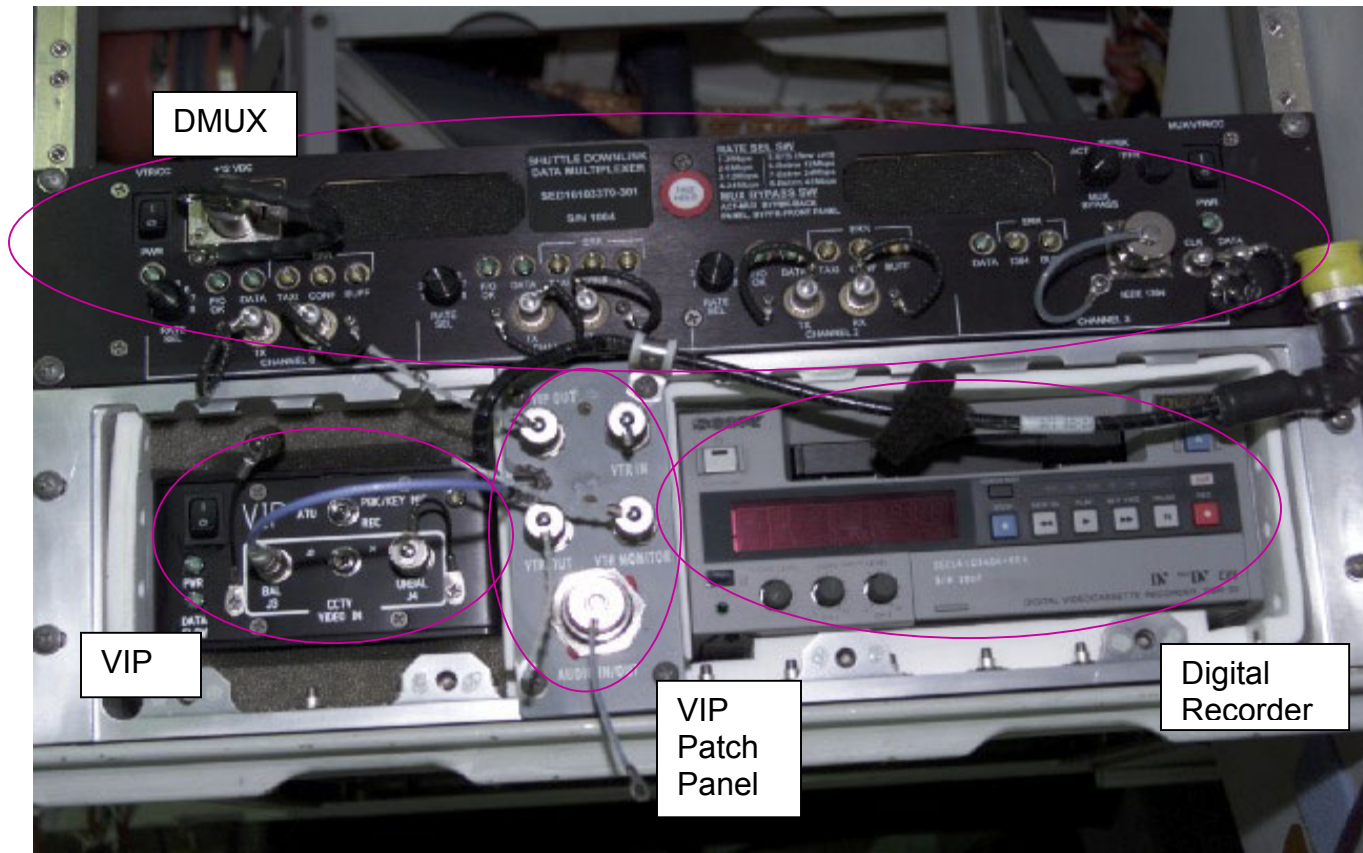


Figure 76-1. DTV

## 76.2 VERTICAL INTERVAL PROCESSOR (VIP)

### 76.2.1 Background

With the implementation of the Digital Television (DTV) system starting on STS-110, a new method of downlinking and storing the CCTV telemetry has been developed. Because the DTV system employs some Commercial off-the-shelf technology (COTS), which does not process the Shuttle CCTV vertical interval blanking area contained within CCTV video signal, the NASA engineers developed a work-around to allow the preservation of the CCTV telemetry that is contained in the vertical interval. To accomplish this, a piece of hardware called the Vertical Interval Processor (VIP) was developed by the Avionics Division at the Johnson Space Center.

The VIP encoder is located in panel L10, inserted in a Styrofoam container. It is covered during ascent/entry to ensure the VIP does not slip out. The VIP extracts the CCTV telemetry from the Orbiter Video signal. It then reprocesses it and feeds it to the audio channel 2 of the on-board VTR. The live digital downlink has the CCTV telemetry inserted on audio channel 2 and real audio on channel 1. This is also true if the downlink is coming from the on-board VTR playback. Once on the ground, the original analog video format is reconstructed with the telemetry reinserted into the vertical interval using the VIP Decoder. The VIP decoder also provides the CCTV telemetry for display on a personal computer via a RS-232 serial port.

### 76.2.2 VIP Inputs and Outputs

The VIP receives:

1. 120 Vac, 400hz, Power
2. A balanced or unbalanced input NTSC Analog Video Signal
3. Playback Audio from the Digital VTR (DSR-20)
4. Record Audio from a standard CCU connection

The VIP outputs:

1. 120 Vac, 400hz Power (currently no output uses this Alt Power)
2. A balanced or unbalanced output NTSC Analog Video Signal
3. Record Audio to the Digital VTR (DSR-20) on Audio Channel # 1
4. The CCTV Vertical Interval converted to a digital signal on Audio Channel # 2

### 76.2.3 VIP Signal Process

Primarily, the NTSC Analog video signal is sent by Video Switching Unit (VSU), column 4, J1 output pins 7-8 to the VIP. The VIP receives the VSU Analog Signal thru

the front panel's balanced input. The VIP then converts the signal to unbalanced video using a balance/unbalance transformer before processing it.

The VIP's Video Telemetry Extractor determines where in the NTSC signal the Vertical Interval Information is located and converts the Vertical Interval Information to a digital signal. From this single Analog NTSC input, the VIP outputs two separate signals to the Digital Recorder (DSR-20):

1. An Amplified Analog NTSC signal of the original video input.
2. The video's Vertical Interval converted to a digital signal on Audio Channel # 2

Secondary, the VIP was designed to "precondition" audio signals to be recorded on the Digital VTR (DSR-20) or amplify playback audio from the Digital VTR (DSR-20) to be heard on the Audio Distribution System.

#### 76.2.4 VIP Requirements

The VIP shall:

- 1) Be stowed in an AFD mounted stowage container with the VTR.
- 2) Operate on single-phase 400Hz 115VAC Orbiter power.
- 3) Provide a conditioned single-phase 400Hz 115VAC power output.
- 4) Also be capable of operating on 120VDC ISS power and providing a filtered 120VDC power output.
- 5) Process a balanced video signal output from the Orbiter CCTV system to produce an unbalanced, electrically isolated, DC restored, NTSC composite analog video signal and provide it to the VTR video input for the purpose of recording or downlink. (Video signal selection is a function of the CCTV system.)
- 6) Encode the vertical interval telemetry from a received Orbiter CCTV signal as an audio signal and provide the encoded signal to one VTR audio input channel.
- 7) Interface with an Orbiter audio terminal unit (ATU) and provide the necessary audio signal interfaces between the VTR and the Orbiter ADS for recording and playback.
- 8) Interface with a dedicated Orbiter CCTV video signal.
- 9) Be designed to allow disconnection from the dedicated Orbiter CCTV signal and re-connection to an alternate Orbiter video signal. (Another system may interface directly to the CCTV signal when disconnected from the VIP.)

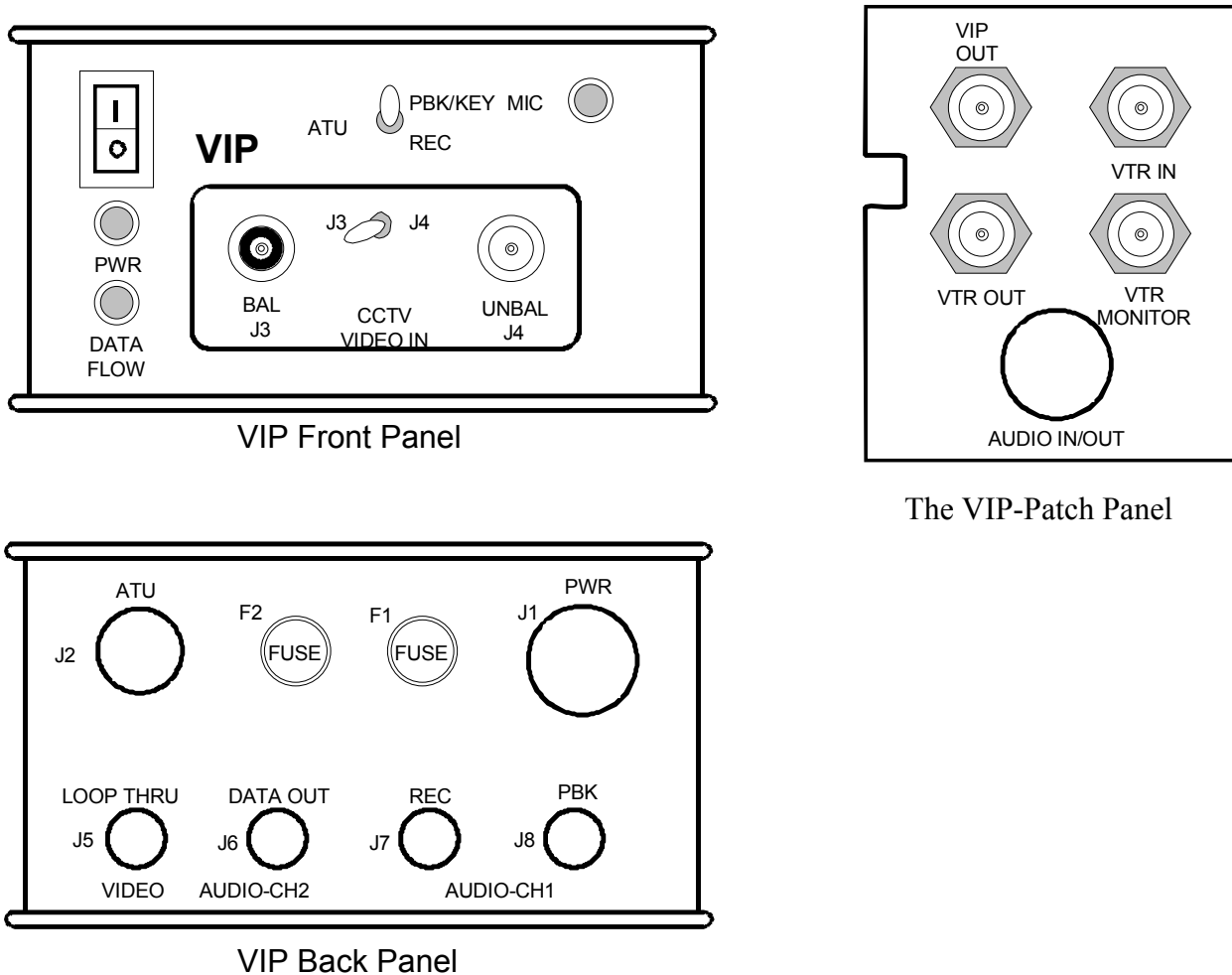


**76.2.5 VIP Telemetry**

None

**76.2.6 VIP Power**

The VIP is powered by AC2, 400hz, Panel MA73C, thru CB15. When powered on, the VIP performs a self-test. Upon successful completion of the self-test, the data flow LED should blink twice, indicating that components in the video telemetry extractor are working properly.



**Figure 76-2. VIP**

### 76.2.7 VIP Switches

**S1 Balanced Video or Unbalanced Video** - Switch determines which Analog NTSC input is processed into the Video Telemetry Extractor.

BAL - Receive the Balanced Video analog NTSC and process it.

UNBAL - Receive the UnBalanced Video analog NTSC and process it.

**S2 PBK/KEY or REC** - Switch determines audio routing from Digital Recorder (DSR-20) to the AUDIO IN/OUT CCU connection:

PBK/KEY - Amplify playback audio from the Digital VTR (DSR-20) to be heard on the Audio Distribution System

REC - "Precondition" audio signals to be recorded on the Digital VTR (DSR-20)

### 76.2.8 VIP LEDs

PWR LED – Indicates the VIP Power Supply is working.

PBK/KEY – Indicates the VIP Power Supply is working and S2 is in PBK/KEY position.

DATA FLOW LED – Indicates that the microprocessor within the video telemetry extractor is receiving vertical interval data.

### 76.2.9 VIP FUSES

Both Fuse 1 (F1) and Fuse 2 (F2) are located on the back of the VIP. The VIP would have to be physically pulled from the Styrofoam sleeve to replace these fuses.

F1 – 5 Amp Fuse electrically located prior to the VIP power switch.

F2 – 2 Amp Fuse electrically located after the VIP power switch.

### 76.3 VIP PATCH PANEL

#### 76.3.1 Background

The VIP Patch Panel was designed to allow interfacing between VIP, Audio System, the Digital VTR (DSR-20), and the Crew Members. It is located on panel L10 between the VIP and VTR.

The VIP was designed at NASA engineering while the Digital VTR (DSR-20) was bought Commercial of the Shelf (COTS). Just like a lot of home stereo/computer equipment, the VIP and Digital VTR (DSR-20) have cable connections off the back of each separate component; video out/in cables are physically located in the back of the DSR-20. The VIP Patch Panel was designed to allow crew member ergonomic ease in routing complicated video sources to the front of panel L10.

#### 76.3.2 VIP Patch Panel Connection Description

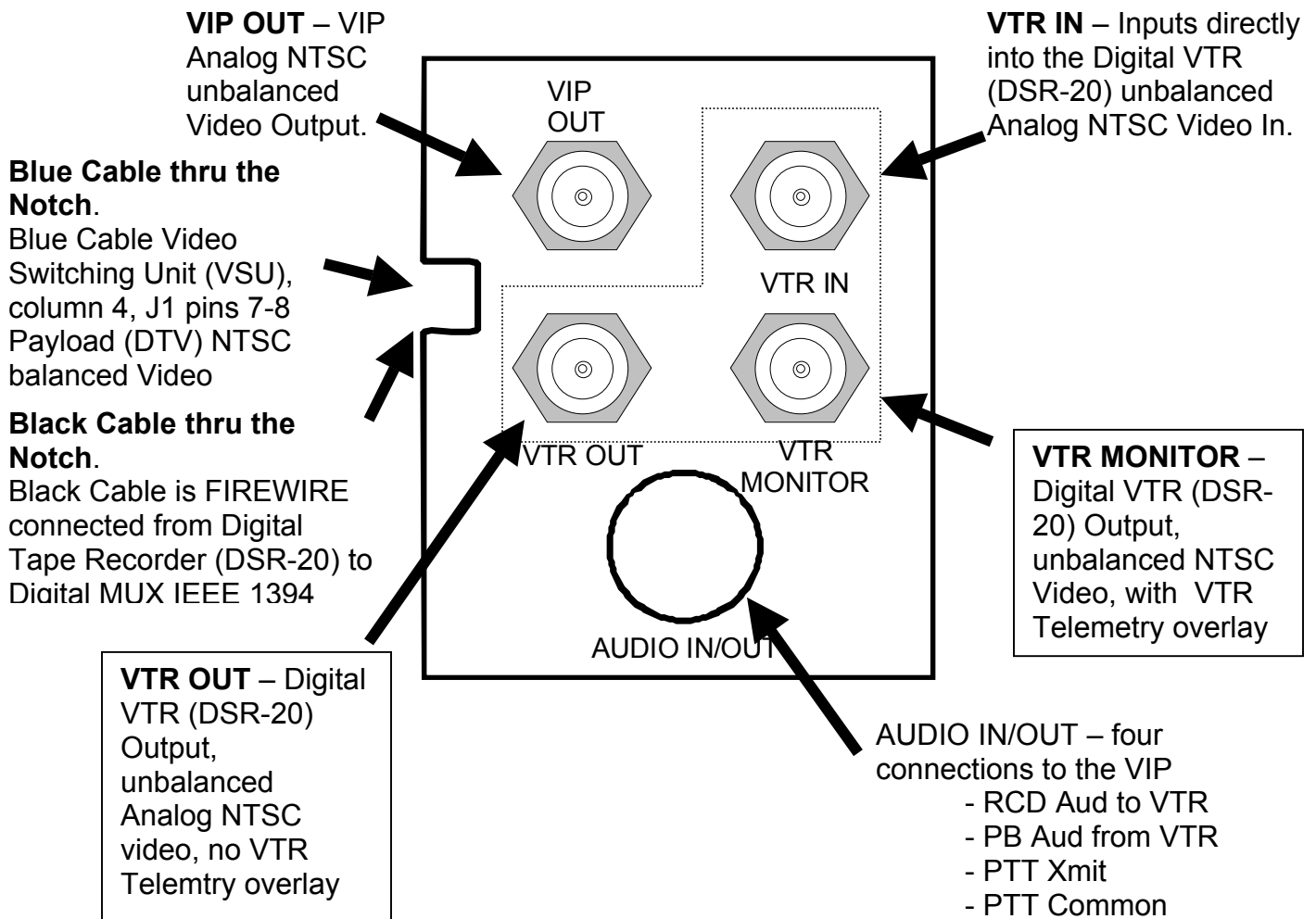


Figure 76-3. VIP Patch Panel

76.3.3 Panel L10 VIP Patch Panel Back Cable Routing

Figure 76-4 shows the permanent cable routing from the VIP Back Face, VIP Patch Panel Back Face, and the Digital Recorder (DSR-20) Back Face.

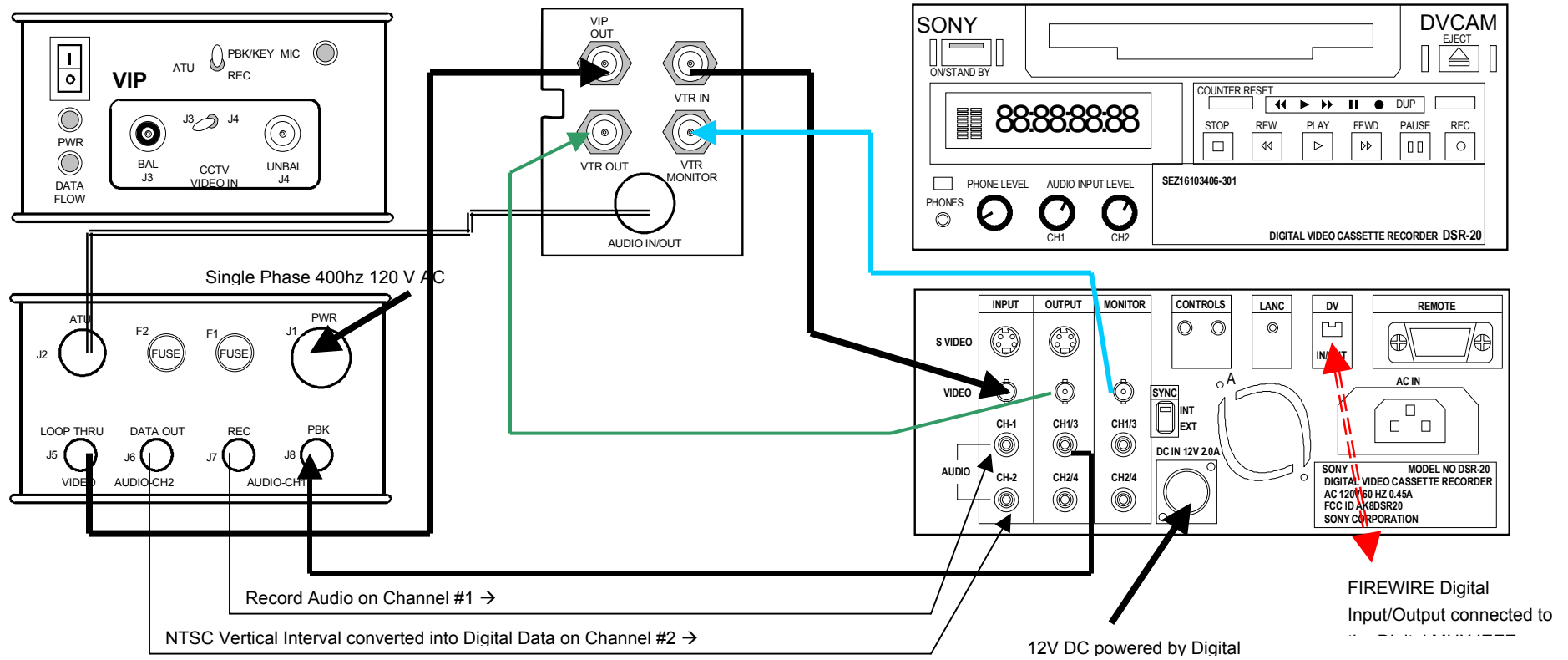


Figure 76-4. VIP Patch Panel Rear Cabling to VIP and DSR-20

## 76.4 DIGITAL RECORDER (DSR-20)

### 76.4.1 Background

The Digital Recorder VTR is a Sony DSR-20 Commercial Off the Shelf (COTS) Digital Tape Recorder. The VTR is located in panel L10, inserted in a Styrofoam container. It is covered during ascent/entry to ensure the VIP does not slip out. The DSR-20 will record digital data on either 3-hr or 40-min tape.

Primarily, The Digital Recorder will take the following three inputs, NTSC Analog unbalanced input from the VIP Patch Panel, VIP Record Audio received on Audio Channel #1, and NTSC Analog Vertical Interval digitally converted signal on Audio Channel #2. These 3 inputs are processed through an Analog to Digital converter. After all three signals are converted to a digital format that can be recorded digitally on tape and/or outputted to the Digital MUX through the DTV MUX IEEE 1394 FIREWIRE. To ensure proper digital muxing it is important that the crew is trained to have the DSR-20 Audio Input Levels set for **Ch1 level of 4** and **Ch2 level of 6** on the DSR-20 front panel. See Figure 76-5 for the DSR-20 Front Panel.

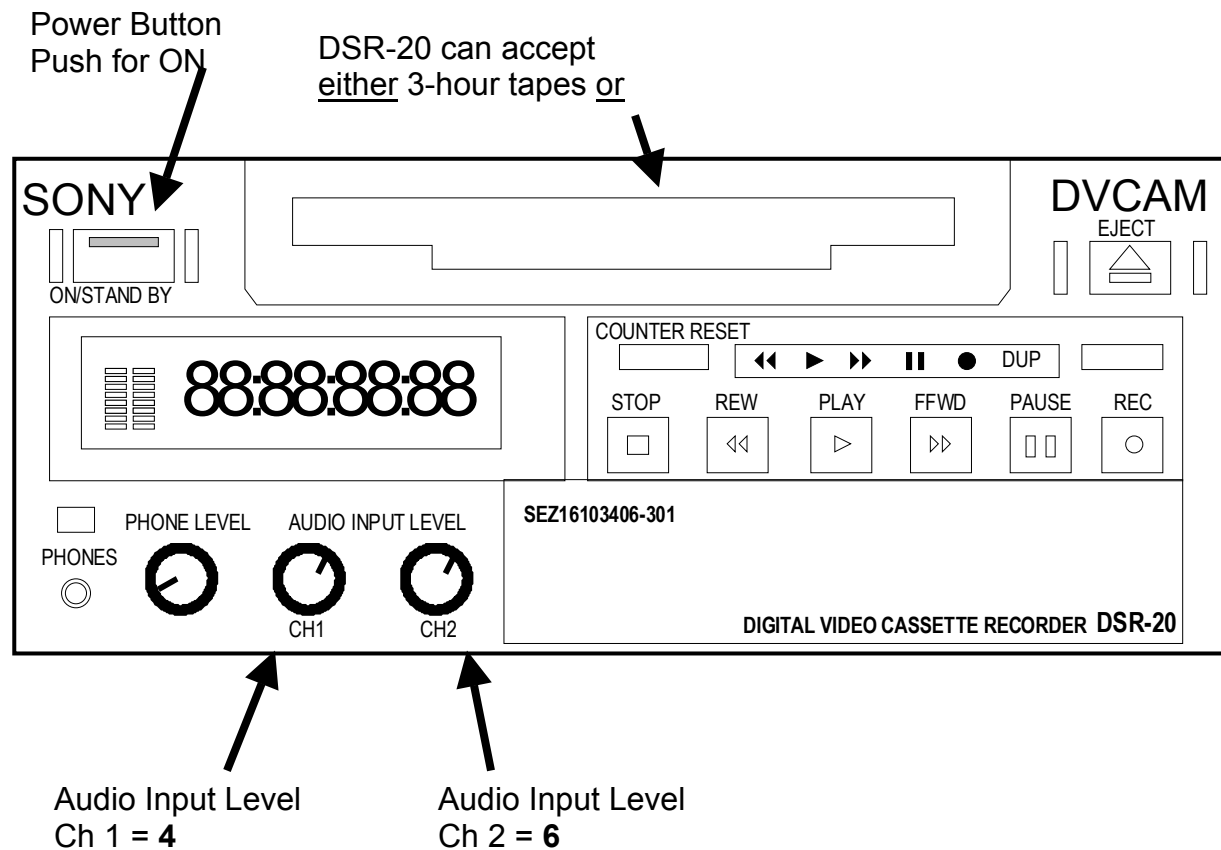


Figure 76-5. DSR-20

#### 76.4.2 Digital Recorder (DSR-20) Telemetry

None

#### 76.4.3 Digital Recorder (DSR-20) Power

The Digital Recorder (DSR-20) receives a 12 volt dc power supply thru the Digital MUX. The DSR-20 is designed to take either a 12 volt DC input or 120 volt AC input; the current configuration is wired for only the 12 volt dc input.

#### 76.4.4 DSR-20 Operations

The DSR-20, being a commercial product Video Tape Recorder, uses similar operations as your home VCR. There is no commanding to any of the DTV system so the crews are trained to use the play, rec, pause buttons to operate the system

#### 76.4.5 VTR Requirements

- 1) Be a commercial DVCAM format VTR, modified as required by this document. (The initial model will be a Sony DSR-20.)
- 2) Be capable of recording and playing back either analog or digital video.
- 3) Be capable of recording and playing back two separate analog audio channels.
- 4) Be stowed in an AFD mounted stowage container with the VIP.
- 5) Be capable of operating on single-phase 400Hz 115VAC power or 120VDC power.
- 6) Also be capable of operating on +13.2VDC power from the DTV Mux or other power source.
- 7) Include a DVCAM IEEE 1394 digital I/O (i.Link) interface.
- 8) Include an integral tape position counter display, built into its display and control panel.
- 9) Interface with the VIP for the purpose of: a) receiving encoded CCTV vertical interval telemetry on one VTR audio channel, b) recording and playback of the Orbiter audio distribution system (ADS) signals, and c) recording and playback of the Orbiter CCTV system video signals.
- 10) Operate as a transcoder for the purpose of digitizing and compressing CCTV signals for downlink.
- 11) Interface with the Mux for the purpose of: a) receiving +13.2VDC power, and b) providing recorded or transcoded signals for downlink, by way of the i.Link interface.

- 12) Provide NTSC composite analog video I/Os, including an output for monitoring the video input signal being recorded or transcoded.
- 13) Provide the video signal input from the VIP as a loop-through output signal. (The VTR is required to be turned on for this signal to be available.)
- 14) Provide for a continuous recording time of at least 184 minutes, utilizing standard size DVCAM format tape cassettes also function with the mini size DVCAM tape cassettes utilized by the camcorder.

## **76.5 DIGITAL MUX**

### **76.5.1 Background**

The Digital MUX was designed by NASA Engineering. It is located on panel L10, fastened to the panel support structure. The Digital MUX is designed to take multiple digital inputs, MUX them into one serial data stream and output them to the KU-BAND Signal Processor Assembly (SPA).

The Digital MUX is divided into several key components.

- Power Supply
- MUX Main Board
- Output Relays

The Power Supply receives power and directs it thru DC/DC converters to power the DSR-20 VTR, Camcorder (CC), and/or MUX Main Board

The MUX Main Board receives four different inputs, digitally MUXes them into a specific format and outputs them to the Output Relay component.

The Output Relays component controls which one of the three inputs (MUX Main Board Output, Front Panel Payload Input, or Rear Panel Payload Input) and associated clocks are sent to the KU-Band SPA. The Output Relays are controlled by one switch (MUX BYPASS).

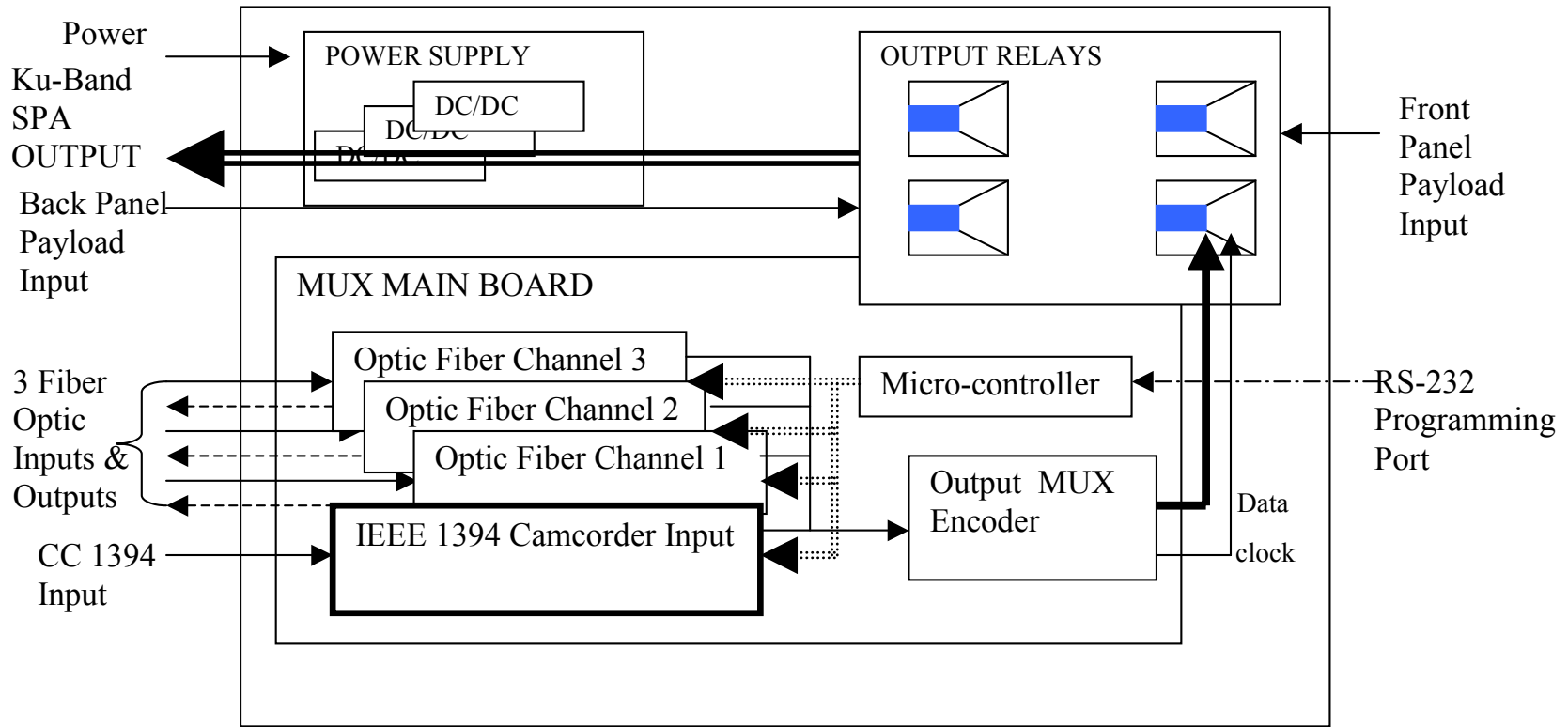


Figure 76-6. Digital MUX



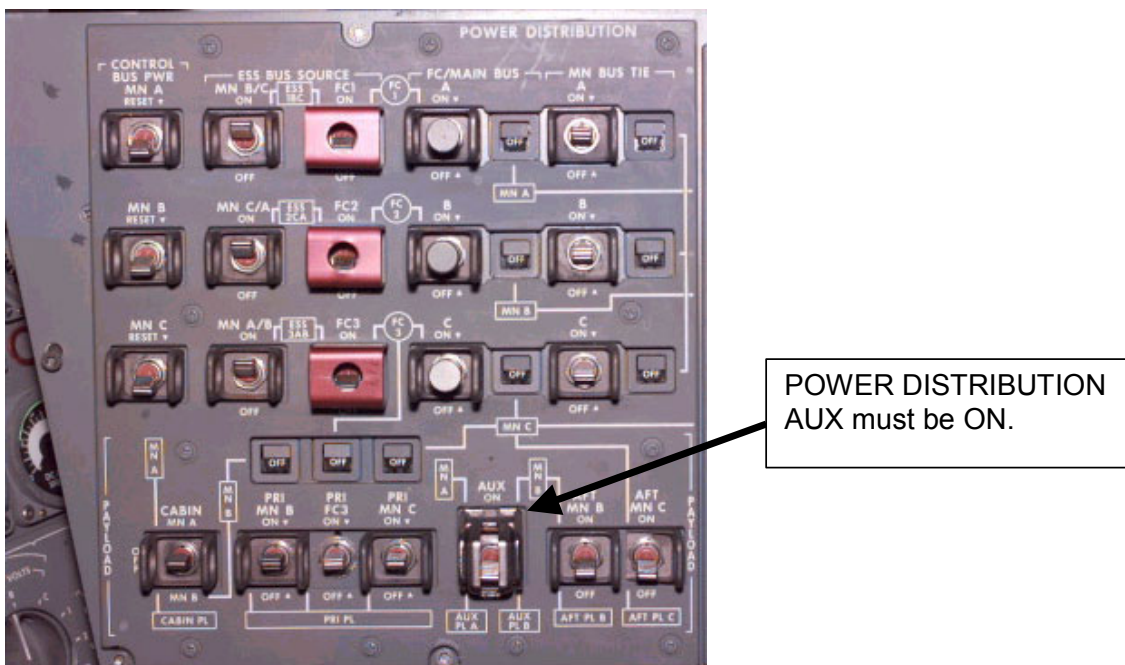
The Digital MUX has the following six inputs, of these only the **bolded** inputs are processed within the MUX MAIN BOARD.

- **Fiber Optic Channel 1**
- **Fiber Optic Channel 2**
- **Fiber Optic Channel 3**
- **IEEE 1394 Input (Normally where DSR-20 Digital VTR is connected)**
- **Front Panel PAYLOAD Input**
- **Rear Panel PAYLOAD Input**

The MAIN MUX BOARD is programmed thru a RS-232 connection.

### 76.5.2 Digital MUX Power

The Digital MUX can power several pieces of equipment. The Digital MUX receives power from Panel R1, ESS 1BC powers switch AUX, energizes a 20amp RPC directing power thru MNA MPC1, thru AUX PLA down to the Payload Station terminal J33.



**Figure 76-7. Panel R1**

The Digital MUX has two power switches **MUX/VTR/CC** and **VTR/CC**.

The **MUX/VTR/CC** switch powers all three DC/DC Converters, while the **VTR/CC** switch only powers the Digital VTR(DSR-20) and Camcorder (CC) DC/DC Converters. So if you want to use the Digital MUX Main board you need to turn on the MUX/VTR/CC switch.

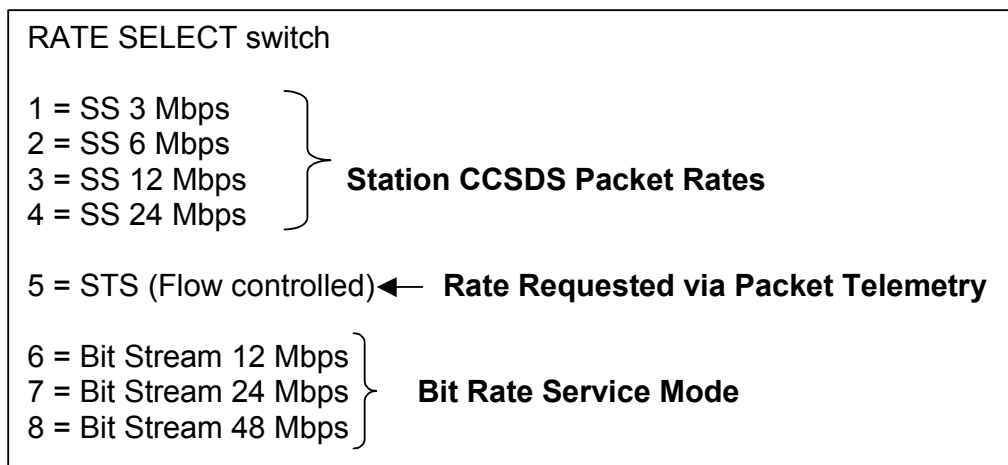
### 76.5.3 Digital MUX Switches and LEDs

An individual Optical Channel is controlled by the respective RATE SEL switch. This switch nomenclature is a misnomer and a handy front panel nameplate details the specific functions of this switch, shown in Figure 76-8.

An Optical Channel's RATE SEL switch can be divided into three distinct sections.

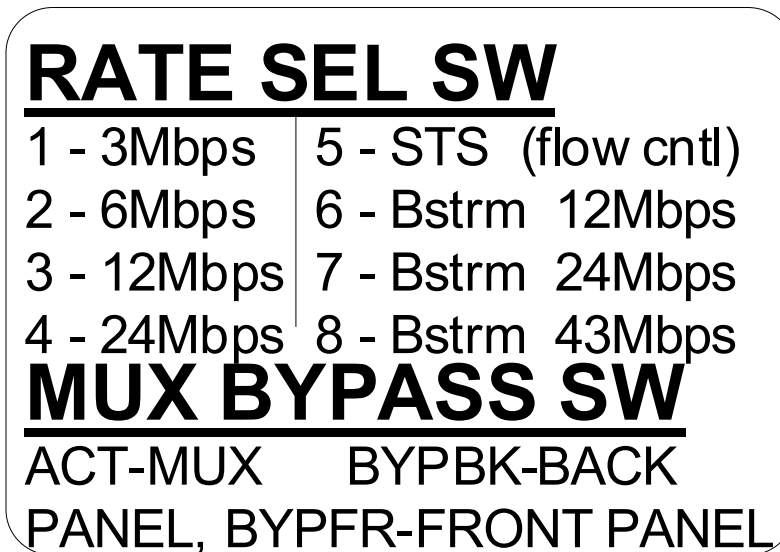
- Space Station (SS) CCSDS Packet Rates
- STS Mode
- Bit Stream Mode

**Table 76-1. Rate Select Switch**



The difference in the three modes are the following:

- In Space Station(SS) Mode, the CCSDS telemetry comes in distinct packets flown at a specific rate.
- In STS Mode, the telemetry entering the Optical Channels contains the requested bit rate.
- In Bit Rate Service Mode, the Bit Rate is standard, no distinct packets, analogous to an IRIG standard.



*Figure 76-8. Digital MUX Front Panel Label*

Station CCSDS Packet Rates - 3, 6, 12, 24 Mbps  
STS flow controlled input - rate requested via packet telemetry  
Bit Rate Service - 12, 24, 48 Mbps (minus approx 10% overhead)

#### **76.5.4 DTV MUX MAIN BOARD Requirements**

1. CCSDS minimum packet length is 233 bytes (one frame), maximum is 4096 bytes.
2. Uses similar format with OCA.
3. F/O interface -  
CCSDS packet interface - 1320nm wavelength, TAXI protocol, 125Mbps.  
Bit Stream Service - 1320nm wavelength, 125Mbps.
4. Input channel buffer sizes - 128Kbytes.
5. MUX Output - 48Mbps, 50-Ohm impedance, conforms to ICD 19001 spec for Payload Max data and clock interface.
6. Statistical MUX Algorithm - Round Robin. All channels are polled within every 256 frame cycle. Channels requesting too much bandwidth are blocked. Unused bandwidth is allocated to other channels as available. Flow-controlled channel provides at or higher bit rate compared to that requested. Station non-flow controlled channels provide up to selected bit rate. Priority channel is the 1394 channel. All available frames are sent when this channel is polled.

#### **76.5.5 Optical Channel Troubleshooting**

If any of the Digital MUX Optical Channels indicate ERRORS, odds are it is an incorrect RATE SWITCH setting. Remember the Rate Switch determines type of data (SS, STS,

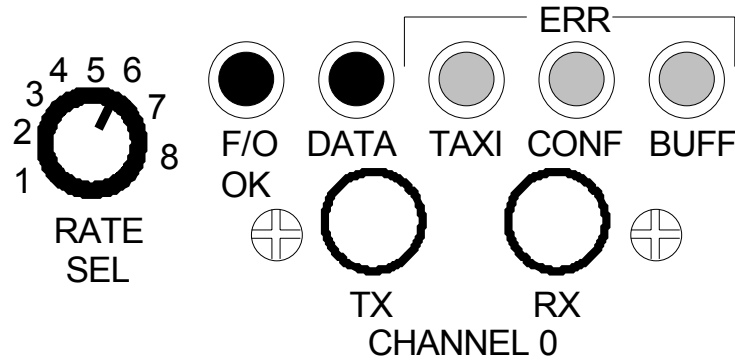
Bit Rate) and Rate of data. Table 76-2 is provided to describe some “misconfigurations” between Payloads and Front Panel Settings and necessary action taken.

**Table 76-2. Rate Switch Troubleshooting**

| <b>MUX Front Panel Settings</b> | <b>Payload</b>                                  | <b>Action Taken</b>   |
|---------------------------------|---|---|
| STS                             | Channel request accumulation is less than 48    | Operate Normally at requested   |
| STS                             | Channel request accumulation is greater than 48 | Last channels polled causing the greater than 48 receive CONFERR and data is not passed |
| STS                             | No request                                      | Set to lowest rate  |
| STS                             | SS  | CONFERR and data is not passed  |
| SS                              | STS   | CONFERR and data is not passed  |
| SS                              | Request <=SS                                    | Operate Normally at requested   |
| SS                              | Request > SS                                    | CONFERR and data is not passed  |
| SS                              | No request                                      | Set to front panel rate   |
| SS accumulated rates > 48       | Don't care                                      | Last channels causing more than 48 get CONFERR  |
| STS                             | Bit Stream                                      | CONFERR and data is not passed  |
| SS                              | Bit Stream                                      | CONFERR and data is not passed  |
| Bit Stream                      | Bit Stream <= requested rate                    | Operate Normally  |
| Bit Stream                      | Bit Stream > requested rate                     | CONFERR and data is not passed  |

### 76.5.6 Fiber Optic Indicators

Each of the Three Fiber Optic Inputs has the following Digital MUX Front Panel Indications. Figure 76-9 shows one of the three channels. The Crew can only configure the Rate Switch described.



**Figure 76-9. Optical Channel (1 of 3) Front Panel Display**

**F/O Channels:**

F/O OK = Fiber Optic signal being received

DATA = Data being received

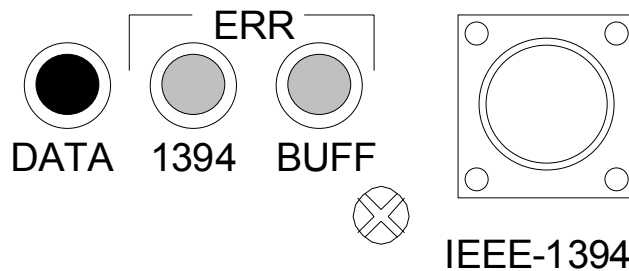
TAXI ERR = TAXI error detected

CONF ERR = Configuration error, requested bit rate too high

BUFF ERR = Channel buffer has underflowed or overflowed

**76.5.7 IEEE 1394 Indicator**

Figure 76-10 shows the LEDs used to show the “condition” of the incoming IEEE 1394 data stream. Notice there are no switches for 1394.



**CHANNEL 3**

**Figure 76-10. IEEE 1394 Front Panel Display**

**IEEE 1394 Channel:**

DATA = Data being received

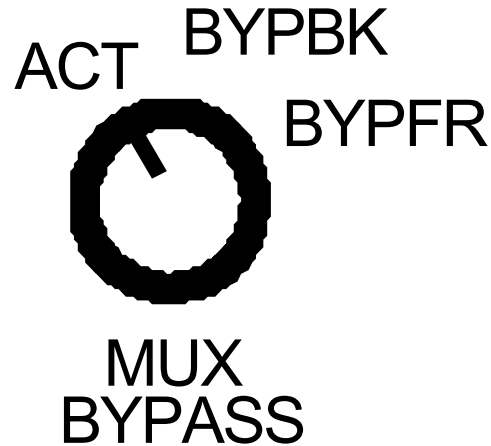
1394 ERR = 1394 format error

BUFF ERR = Channel buffer has underflowed or overflowed

### 76.5.8 Output Relay Select

The Output Relays component controls which one of the three inputs (MUX Main Board Output, Front Panel PAYLOAD Input, or Rear Panel PAYLOAD Input) and associated clocks are sent to the KU-Band SPA; this is done with one front panel switch (MUX BYPASS). Figure 76-11 displays this switch.

Technically there are four “self-latching relays”, which are electrically controlled via the MUX BYPASS switch.



*Figure 76-11. Rate Switch*

#### MUX BYPASS

**ACT Position:** Output of the MUX MAIN BOARD (1394 IEEE and/or Optic Fiber) data and clock goes to the Ku-Band System.

**BYPBK Position:** The Payload Source connected directly into the Back Panel of the Digital MUX will be routed to the Ku-Band System.

**BYPFR Position:** The Payload Source connected directly into the Front Panel of the Digital MUX will be routed to the Ku-Band System.

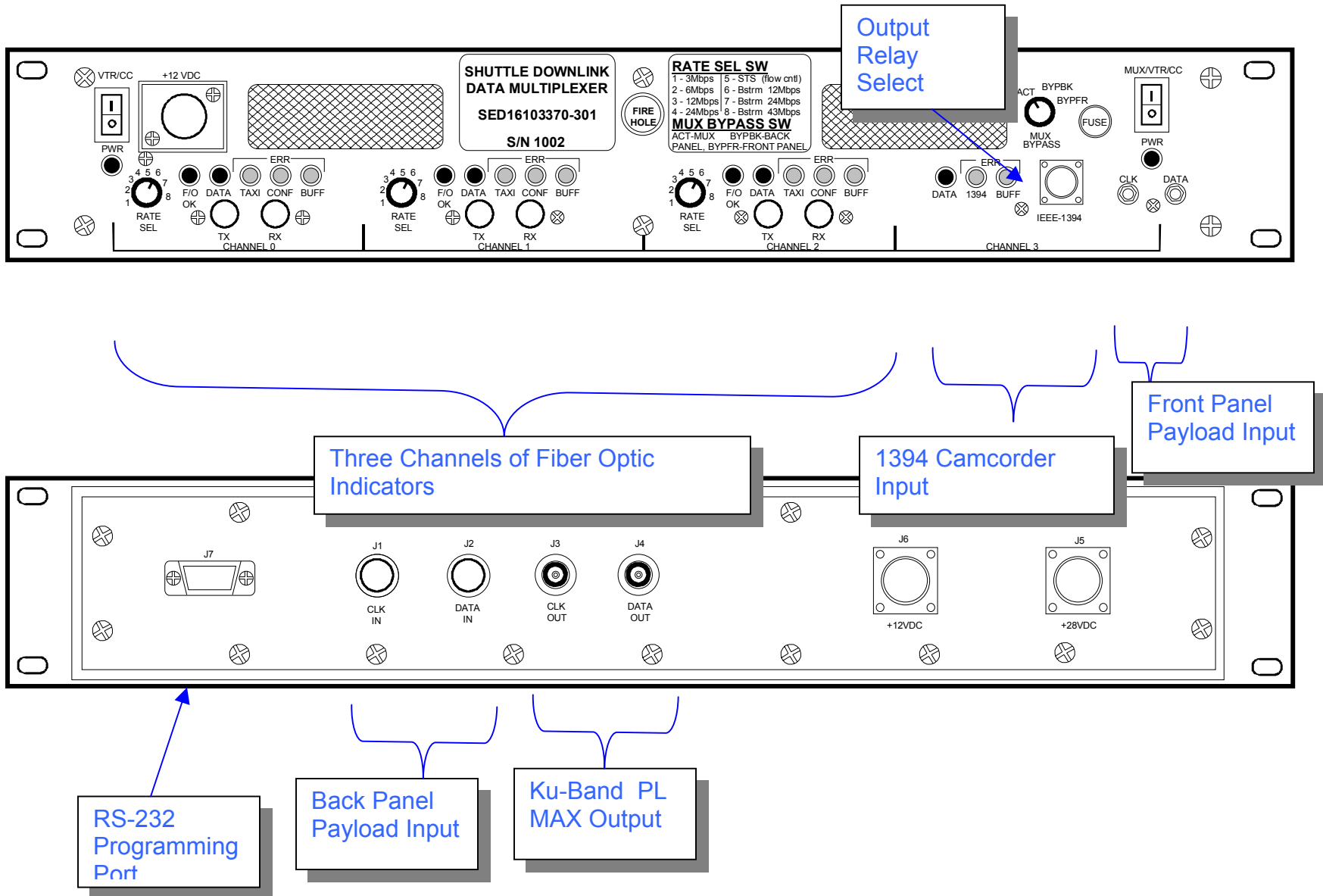


Figure 76-12. Digital Mux Front and Back Panel Ports

### 76.5.9 Digital MUX Main Board

The purpose of the Digital MUX MAIN Board is to receive four inputs, MUX all applicable telemetry into one data stream and send it to the Output Relay.

1. Data formats supported:

- 1) One 1394 Input - IEEE 1394 Isochronous Packets (conforming to IEC 61883) (DVCAM),
- 2) Three Fiber Optic Inputs - ISS compliant 1320nm fiber optic (F/O), TAXI interface, supporting both Consultative Committee for Space Data Systems (CCSDS) packet format and bit stream data. (Future DTV configurations and other users will utilize these channels.) CCSDS Packets & Bit Stream Service.

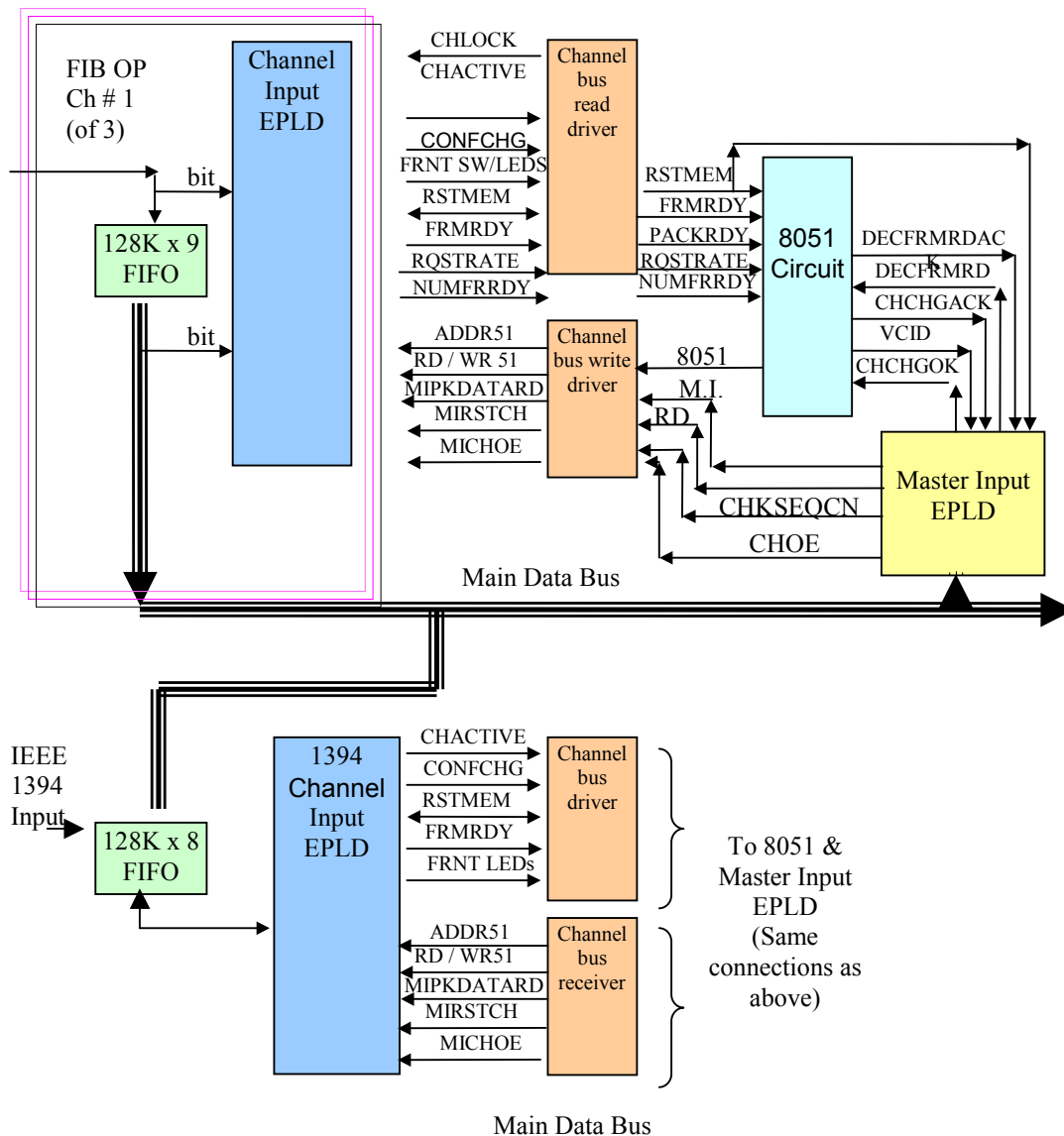


Figure 76-13. EPLD to 1805 Micro Processor Protocol



### 76.5.9.1 MUX MAIN BOARD Sequence of Events

At power up, the 8051 Micro Controller defaults to a Virtual Channel ID (VCID) of 00 to produce fill frames until packet filled frames are ready.

The 8051 determines which of the applicable four channels are active by way of Channel Input EPLD "CHACTIVE" reply. It determines the requested channel rates and builds an allocation table based on these requests. The 8051 Micro Controller determines the current channel's allocation based on current priority order:

1. Uplinked Rate (not currently implemented)
2. 1394 is active
3. Selected SS Rate or Bit Stream Rate from front Panel
4. Lowest rate when front panel is selected for STS.

If the requested rate for each channel can be accommodated, it is added to the allocation table, if not CONFERRs are sent and the channel is blocked until it request a rate that can be supported.

8051 resets all channel FIFO buffers by way of the "RSTMEM" command.

8051 then starts the following loop:

1. 8051 chooses channel (ch) by polling "FRMRDY" (Frame Ready) from each channel in sequence to find which channel has data. The sequence will be in order of 0 to 3. The "FRMRDY" signal is one of several signals that all channels have in common which are activated (read by 8051) when the 8051 addresses each specific channel. "FRMRDY" active means that at least one complete packet and one complete frame has been received.
2. 8051 determines if configuration has changed by way of CONFCHG. CONFCHG is set at power up and any time a channel's requested rate has changed.
3. 8051 determines the number of frames to be sent for current channel by: number of frames ready (decremented after each frame completely read, added to only after completed packets received; and previous over run of channel allocation from last time channel was polled.
4. 8051 Provides the Virtual Channel ID (VCID) to the Master Input EPLD for inclusion of the frame header. "CHCHGACK" sent from 8051 to Master Input EPLD.
5. The Master Input EPLD produces the Data Boundary Pointer (First Header Pointer). During the frame header creation, the Master Input EPLD determines the Data Boundary value based on the remaining packet data size for the upcoming frame. A first header pointer is sent for every packet whether

VCID changes or not. A first header pointer of 0x00 = 1<sup>st</sup> byte of frame is first byte of new packet. A first header pointer of 0x00= No new packet header in this frame.

6. The Master Input EPLD then dumps the particular Channel FIFO Buffer by way of a "MIPKDATARD" signal. This sends the channels data to the Reed-Solomon Encoder headed to the output of the MUX MAIN BOARD.
7. Allow the Channel Change if Channel Allocation Complete.

If 8051 determines that current channel is not complete, VCID remains the same, go to step 4.

If 8051 determines that current channel is complete, go to step 1.

The 8051 Micro Controller, Channel Input EPLDs and Master Input EPLDs communicate back and forth using a limited amount of standardized protocol. When the Master Input EPLDs determine when it is in the last or next to last frame (using frame counters) and will coordinate with the 8051 and the Channel Input EPLDs to send commands to change channels or input fill data.

For the VCID to change, the 8051 has to have counted down to the last frame or next to last frame of this channel allocation from the Master Input EPLD. This is required in addition to "CHCHGOK" to allow the 8051 to determine the number of packet filled frames to send by way of the statistical algorithm. The VCID remains the same otherwise. If the 8051 receives "CHCHGOK" and has determined that there are no more frames available, the VCID goes to 00. The Master Input EPLD produces frame fill to finish off the current frame and produce fill frames until frames are available again. It is common for the first header pointer to point to the start of the fill data in the middle of a frame. The corresponding VCID for that Frame will be 0x00.

#### **76.5.9.2 MUX MAIN BOARD Signal Exchange Scenario**

The minimum packet size is 233 bytes to ensure a frame boundary is always crossed for each packet. maximum packet size is 4096 bytes.

1. Powerup, VCID = 00
2. 8051 polls channels using "CHACTIVE" to determine if channel is active or not. Channel bitrate allocation is determined, allocation tables produced, CONFERRs sent as required. Channel receiving CONFERR is blocked by 8051 until acceptable channel allocation is indicated.
3. All input buffers reset by RSTMEM.
4. 8051 selects channel by way of priorities.
5. Verify current channel settings using CONFCHG. If no change go to 6. f change and channel not active, RSTMEM, go to 4. If change and channel active, if not supportable, RSTMEM, go to 4. If supportable, RSTMEM, go to 6.

6. Determine number of frames to be sent.
7. VCID from 8051 to Master Input EPLD.
8. Master Input EPLD creates Master Input Address from VCID
9. Read (MIPKDATARD) channel FIFO starting at frame location indicated by first header pointer.
10. Master Input EPLD send "DECFRMRD" at end of each frame (at start of Reed-Solomon parity time). Allow channel change at the end of packets – CHCHOK. If 8051 determines channel is not complete, VCID remains the same. Go to step 7. If 8051 determines channel is complete, go to step 4.

### 76.5.9.3 Various Data Format Process

**For CCSDS packet channels** – Packet size is loaded into Master Input EPLD and decremented until < frame data size x2, then Master Input EPLD sends CHCHGOK. CHCHGOK activated (after new packet start or fill frame, and last or next to last frame) to indicate OK for 8051 to change channels. 8051 determines whether to keep current VCID or search for next channel based on Number of Frames ready (NUMFRMRDY) received at beginning of this cycle's current channel time and channel allocation for this channel. CHCHGACK sent when VCID is ready for Master Input EPLD.

**For Bit Stream Channels** – CHCHGACK sent as normal when Bit Stream Channel is selected. CHCHGOK is asserted early into the Bit Stream downlink time period by Master Input EPLD. Number of frames loaded into 8051 and decremented until < frame data size x1. New channel determined by 8051 and CHCHGACK sent.

**For 1394 channel** – Master Input loads a constant number into its packet counter and decrements this packet counter as in the CCSDS packet case. CHCHGOK is set for the same case as CCSDS packets. This process is repeated until the 1394 FRMRDY signal is no longer active indicating the last 1394 packet is being processed. All available 1394 data is sent when this channel is selected. 8051 determines new channel and send CHCHGACK.

### 76.5.9.4 Operational Notes on the MUX MAIN BOARD

The minimum packet size is 233 bytes, maximum is 4096 bytes.

The output is always 48Mbps.

The Master Input EPLD has to receive a continuous stream of data or be told that it is responsible for generating frame fill or fill frames. It uses the VCID and its internally generated First Header Pointer to determine channel and start of packets.

Only one VCID channel change per frame allowed. Frame fill may be created from a VCID of 00, but only one channel of good data will be contained within each frame.

The allocation table given to each channel is produced by allowing 1 to 256 frames per poll per channel. The encoder or other input source can request a rate if they produce a APID for a source that doe rate selection / request. The 5 bit number is used with a lookup table in the 8051 to determine rate. For example:

$$00|010 (6Mbps) \rightarrow (6Mbps * 255 \text{ Frames per poll}) / 48Mbps = 31.8 > 32 \text{ Frames per poll}$$

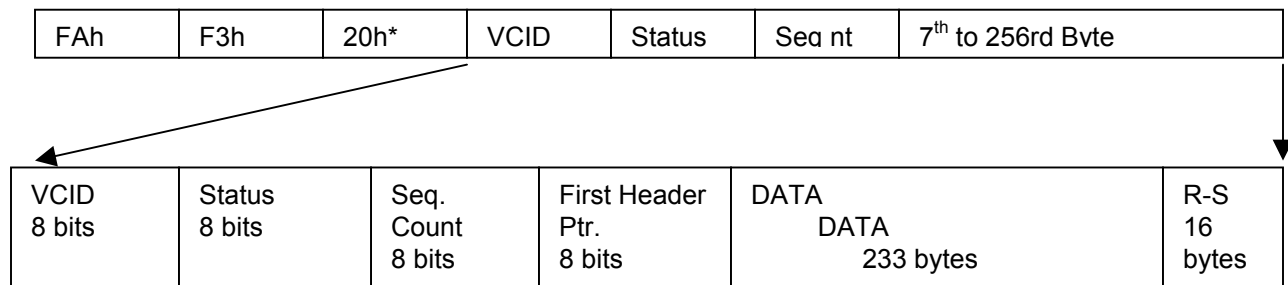
The 8051 adds up all rates and makes sure they don't exceed 256. CONFERR is used to facilitate this action.

### 76.5.9.5 DTV MUX MAIN BOARD Output Format W/O Scrambling Code

Reed Solomon Code Block Written Into Interleaver Dual Port Memory Horizontally

The DTV MUX MAIN BOARD output 256 Bytes of at a Rate of 48 Mbps.

\* A Frame Sync FAF321h occurs every 64s Frame to indicate location of the dual port memory.



**Figure 76-14. DMUX Telemetry Format**

**VCID** - Virtual Channel ID, 8 bits (ex. Ch 0 = 80h, Ch 1 = 81h, Ch 2 = 82h, Ch 3 = 83h)

**Status** – 8 bits, Status will come down as an embedded 64 byte frame (including frame sync) (one byte per MUX telemetry frame). Frame Sync = D3C6h

**Sequence Counter** – 8 bits,

**First Header Pointer** – 8 bits, 00h = first data byte in frame containing first byte of new packet

**Data** = 233 bytes, maximum per DTV MUX MAIN BOARD Frame

**R-S** = 16 bytes, Reed-Solomon Parity check.

### 76.5.9.6 MUX MAIN BOARD Requirements

1. Total number of channels. Expandable from 4 to 16 channels in increments of 4.
2. Only complete packets are sent for the CCSDS packets and IEEE 1394 packets case.

3. The MUX MAIN Board sends either valid data or fill frames or frame fill (frame partially filled with fill data).
4. The MUX is programmed to prioritize its telemetry bandwidth as follows:
  - (1) Uplinked rate (Not currently implemented)
  - (2) IEEE 1394 channel when active
  - (3) Front panel controls for SS rates,
  - (4) Requested rate for STS for inputs with identification header coding which are requesting a rate.
  - (5) Lowest rate when in STS and no correct header requested rate.

Currently when the 1394 is active; i.e., when there is either a CAMCORDER or VTR Input thru the 1394 front panel interface, it is given top priority and all frames are sent per poll. When 1394 is not active Bit Rate allocation is divided between the three other optical channels.

Provide three additional input channels, each with an include any Mux generated status and configuration telemetry in the downlink data stream.

#### 76.5.9.7 CCSDS Packet Format

The packet format is derived from the Consultative Committee for Space Data Systems (CCSDS), Recommendation for Space Data System Standards, Advanced Orbiting Systems, Networks and Data Links: Architectural Specification, CCSDS

701.00-R-3, Red Book, Issue 3, June, 1989, Page 5-27.

The Transparent Asynchronous Xmitter - Receiver Interface (TAXI) protocol is used for packet delimiting as is required for International Space Station (ISS) applications, used only in SS Mode. The following is the format employed for the packet structure:

Total packet length = 1888 bytes.

1. SR Command 0110 (TAXI) - packet delimiting
2. 48 bit CCSDS Packet Header - sent MSB first
  - 2.1 First 16 bits come from EPROM Programmable Logic Device (EPLD)  
Value  
000      Version #, 3 bits  
0 Type, 1 bit  
1 Secondary Header flag, 1 bit  
0000000001 Application Process ID (APID) or Packet Channel ID, 11 bits  
\* Note - M-JPEG CE APID = 0000000000

2.2 Next 16 bits come from the EPLD

Value

00 Sequence Flag, 2 bits (00 means continuation segment)  
XXXXXXXXXXXXXXXX Packet Sequence Count, 14 bits, Packet #s 0 to 16384

2.3 Next 16 bits come from EPLD

Value

1881D Packet Length, 16 bits (Packet length excluding the Primary Header - 1)  
See page 5-29 of Red Book, CCSDS 701.00-R-3

3. 16 bit Secondary Header from EPLD

Value

XXX Front panel switch setting (encoded), 3 bits. (000 lowest, 111 highest)  
XXXXXXXXX Front panel LED indicators, 9 bits.

- Bit 8 = F/O OK
- Bit 7 = SDI OK
- Bit 6 = Pack Lock
- Bit 5 = DVB RVS
- Bit 4 = TAXI ERR
- Bit 3 = CONF ERR
- Bit 2 = BUFF ERR
- Bit 1 = OVER TEMP
- Bit 0 = FAN OK

XXXX Transmit Speed, 4 bits

|       |      |
|-------|------|
| STS12 | 0110 |
| STS16 | 1000 |
| STS20 | 1001 |
| STS24 | 0111 |
| STS28 | 1010 |
| STS32 | 1011 |
| STS36 | 1100 |
| STS43 | 1101 |

4. Data 1880 x 8 bits, from Data FIFOs (470 32 bit words, 69.719 packets per Data FIFO [128K FIFO])

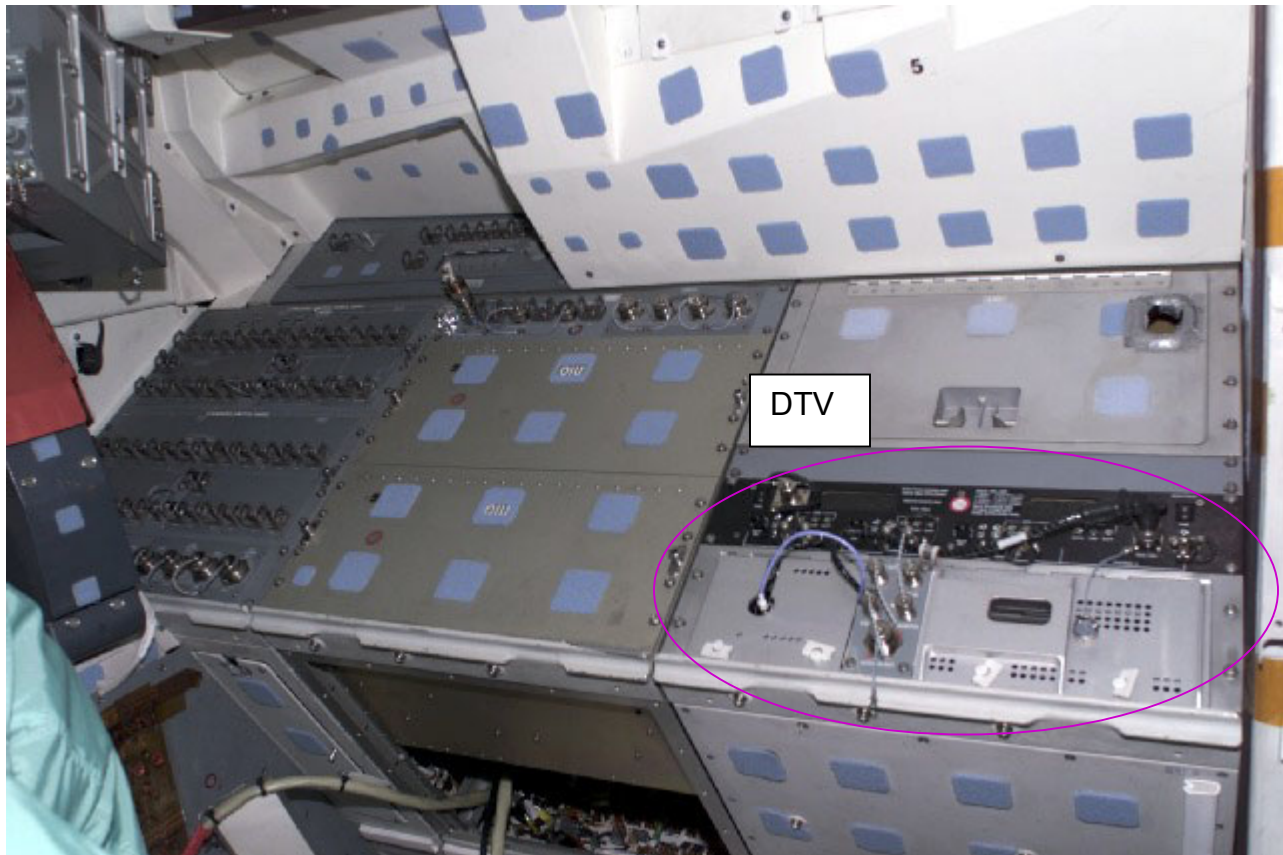
5. RS Command 1100 (TAXI) - packet delimiting

X = variable

Note - All Primary Header and Secondary Header bits are written to the FIFO read side data bus by the EPLD. The data area is read out of the FIFO.

Note - Packet Header: Originates from EPLD. Data originates from read side of FIFO.

### 76.5.10 DTV Flight Deck Location



**Figure 76-15. DTV Flight Deck Location**

### 76.5.11 DTV Shuttle Interfaces

The DTV interfaces with the Shuttle through the Payload Station Distribution Panel (PSDP). The following are “Standard” Interface Connections.

- J37 port connects 400HZ AC PWR to the VIP
- J35 port connects the VSU Payload CTVC Output
- J33 port connects 28Vdc input to the Digital MUX
- J724 port connects the Digital TV MUX Digital Video Data to Ku-Band Signal Processor
- J723 port connects the Digital TV MUX Digital Video Clock to Ku-Band Signal Processor

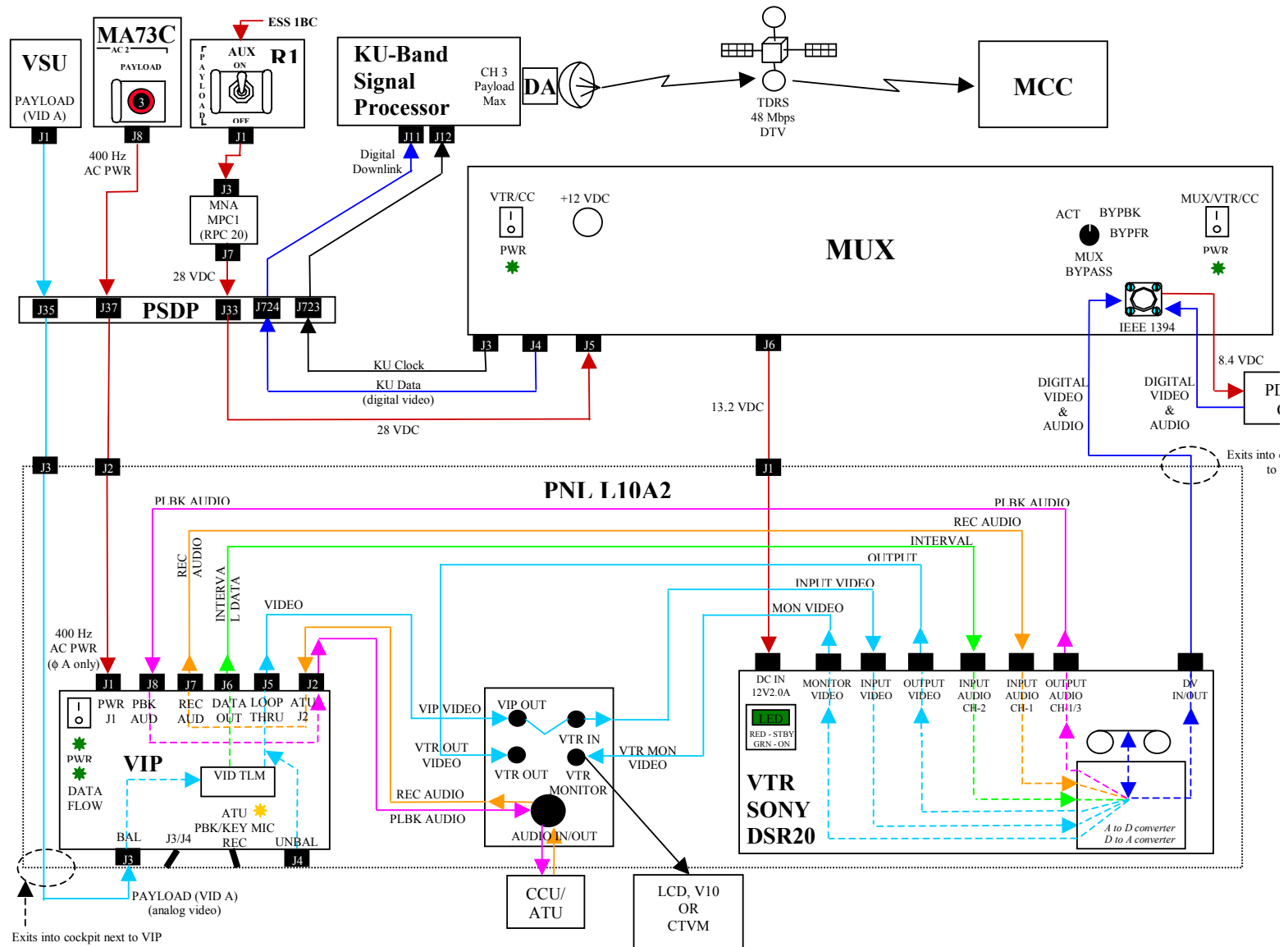


Figure 76-16. DTV Shuttle Interface



## 76.6 REFERENCES

- A. Shuttle Orbiter/DTV Cargo Elements Interface, ICD-A-21429
- B. M-JPEG Video Compression System, MSC-22744

The following references are found on the following JSC Engineering website under "DOCUMENTS".

<http://www4.jsc.nasa.gov/eaprojects/ea-projects/flightgfe/dtv/html/dtv.htm>

- A. CCTV Telemetry Reinsertion Delay Through the DTV System Baseline
- B. HDTV MPEG CE Packetizer CCSDS Packet Format
- C. DTV MUX Frame Format
- D. DTV MUX/DEMUX Features & Specifications
- E. VIP/VTR Power Cable Certification Information
- F. MUX IEEE 1394 Packet Channel Input Control
- G. MUX CCSDS Packet/Bit Stream Channel Input Control
- H. MUX Data Formatting Theory of Operations

**SECTION 77 - ORBITER BOOM SENSOR SYSTEM**  
**CONTENTS**

| <b>Section</b> |  | <b>Page</b> |
|----------------|--|-------------|
| 77.1           | GENERAL DESCRIPTION.....                                   | 77-1        |
| 77.1.1         | Interfaces .....   | 77-5        |
| 77.2           | OVERVIEW OF OBSS USAGE .....                               | 77-7        |
| 77.2.1         | Inspection.....  | 77-7        |
| 77.2.2         | Recording of Scan.....                                     | 77-8        |
| 77.2.3         | EVA Worksite .....   | 77-8        |
| 77.2.4         | Jettison.....  | 77-8        |
| 77.3           | DESCRIPTION.....   | 77-9        |
| 77.3.1         | Remote Manipulator System (RMS) Sideview Camera (RSC)..... | 77-9        |
| 77.3.2         | Intensified Video Camera (ITVC) .....                      | 77-10       |
| 77.3.3         | Laser Dynamic Range Imager (LDRI) .....                    | 77-11       |
| 77.3.4         | Laser Camera System (LCS) .....                            | 77-14       |
| 77.3.5         | ISIS Digital Camera.....                                   | 77-15       |
| 77.4           | OPERATIONS.....  | 77-18       |
| 77.4.1         | Boom Positioning .....                                     | 77-18       |
| 77.4.2         | Modes of Operation for the ITVC/LDRI Assembly.....         | 77-19       |
| 77.4.3         | Modes of Operation for the LCS Assembly .....              | 77-20       |
| 77.4.4         | Scan Types .....   | 77-21       |
| 77.4.5         | Handling of the Boom.....                                  | 77-24       |
| 77.4.6         | Ground Processing .....                                    | 77-25       |
| 77.5           | OBSS OPERATIONAL NOTES .....                               | 77-27       |
| 77.6           | ELECTRICAL .....   | 77-28       |
| 77.7           | CONTROLS .....   | 77-29       |
| 77.8           | PHYSICAL CHARACTERISTICS.....                              | 77-31       |
| 77.9           | INSTALLATION.....  | 77-32       |
| 77.10          | TELEMETRY.....   | 77-32       |
| 77.11          | REFERENCES.....  | 77-35       |

## TABLES

| Table |  | Page  |
|-------|--|-------|
| 77-1  | Inspection Requirements.....           | 77-3  |
| 77-2  | OBSS Sensor Performance .....          | 77-11 |
| 77-3  | Inspection Scenarios .....             | 77-22 |
| 77-4  | OBSS Electrical/Power Information..... | 77-28 |

## FIGURES

### Figure

|       |  |       |
|-------|--|-------|
| 77-1  | Aft End of OBSS .....                                    | 77-4  |
| 77-2  | Integrated Boom Assembly Mounted on Starboard Sill ..... | 77-5  |
| 77-3  | OBSS Overall Diagram .....                               | 77-7  |
| 77-4  | RMS Sideview Camera near the End Effector .....          | 77-9  |
| 77-5  | ITVC Image of RCC Damage (10ft) .....                    | 77-10 |
| 77-6  | LDRI Sensor Field of View .....                          | 77-11 |
| 77-7  | LDRI Sample Range Image .....                            | 77-12 |
| 77-8  | LDRI/ITVC from STS-97 DTO .....                          | 77-13 |
| 77-9  | LCS Sample Range Image.....                              | 77-14 |
| 77-10 | LCH with IDC mounted on side .....                       | 77-16 |
| 77-11 | Adimec-2000m and Pleora Converter Box.....               | 77-17 |
| 77-12 | IDC/LCH to OCA Block Diagram .....                       | 77-18 |
| 77-13 | Boom Grappled by RMS .....                               | 77-24 |
| 77-14 | PNL A8L.....   | 77-30 |
| 77-15 | OBSS Patch Panel (OPP).....                              | 77-30 |
| 77-16 | PNL A8 Keep-Alive Telemetry.....                         | 77-33 |

## SECTION 77 ORBITER BOOM SENSOR SYSTEM

### 77.1 GENERAL DESCRIPTION

The Orbiter Boom Sensor System (OBSS) was developed to meet Columbia Accident Investigation Board (CAIB) recommendation 6.4-1:

“For missions to the International Space Station, develop a practicable capability to inspect and effect emergency repairs to the widest possible range of damage to the Thermal Protection System, including both tile and Reinforced Carbon-Carbon, taking advantage of the additional capabilities available when near to or docked at the International Space Station.

For non-Station missions, develop a comprehensive autonomous (independent of Station) inspection and repair capability to cover the widest possible range of scenarios.

Accomplish an on-orbit Thermal Protection System inspection, using appropriate assets and capabilities, early in all missions.

The ultimate objective should be a fully autonomous capability for all missions to address the possibility that an International Space Station mission fails to achieve the correct orbit, fails to dock successfully, or is damaged during or after undocking.”

The OBSS consists of: a boom that mounts to the starboard sill for launch, landing, and on orbit stowage, inspection sensors, and ground based data processing. The forward end of the boom contains an interface that is mechanically and electrically compatible with the Shuttle Remote Manipulator System (SRMS). An electrical interface provides the connections to supply the boom-mounted sensors the necessary power, command, and telemetry connections. A mechanical interface provides the structural interface such that the SRMS can maneuver the boom into the required positions for Thermal Protection System (TPS) inspection. The middle portion of the boom contains an interface that is mechanically compatible with the Space Station Remote Manipulator System (SSRMS). When the Orbiter is docked to the International Space Station (ISS), it is necessary for the SSRMS to grapple and unberth the boom from the Orbiter and hand it off to the SRMS due to ISS structure blockage at the Orbiter Docking Station (ODS).

The aft end of the boom contains two sensor packages which together make up Integrated Sensor Inspection System (ISIS). One sensor package (SP-1) consists of an Intensified Television Camera (ITVC) and the Sandia Laboratories developed Laser Dynamic Range Imager (LDRI). The primary function of the ITVC is to control the Pan/Tilt Unit (PTU) during LDRI scanning. It is also possible for the ITVC to provide a 2D black and white image of the external Orbiter TPS surfaces. A mounting plate on the boom accommodates the second sensor package (SP-2) which contains the Laser Camera System (LCS), developed by Neptec, as well as a digital still camera, the ISIS

Digital Camera (IDC), by Adimec. See Figure 77-1 for a diagram of the aft end of the boom. In addition, the integrated system uses the RMS Sideview Camera (RSC), a situational awareness camera mounted on the RMS end effector.

The primary function of both the LDRI and LCS is to provide quantitative 3D information concerning the outer mold line of the Orbiter TPS surfaces. Sensors are required to detect the following:

**Table 77-1. Inspection Requirements**

Tile Damage Inspection Requirements

|  | Minimum Cross Distance of Area (in.) | Accuracy of Cross Distance Measurement (in.) | Accuracy of Depth Measurement (in.) |
|--|--------------------------------------|--|-------------------------------------|
| Nose and main landing gear door perimeter, wing leading edge carrier panel tiles, external tank door perimeter, and the elevon coves | 1                                    | ± .25  | ± .25                               |
| All other lower surface LI-900 acreage tiles and OMS pods  | 3                                    | ± .25  | ± .25                               |

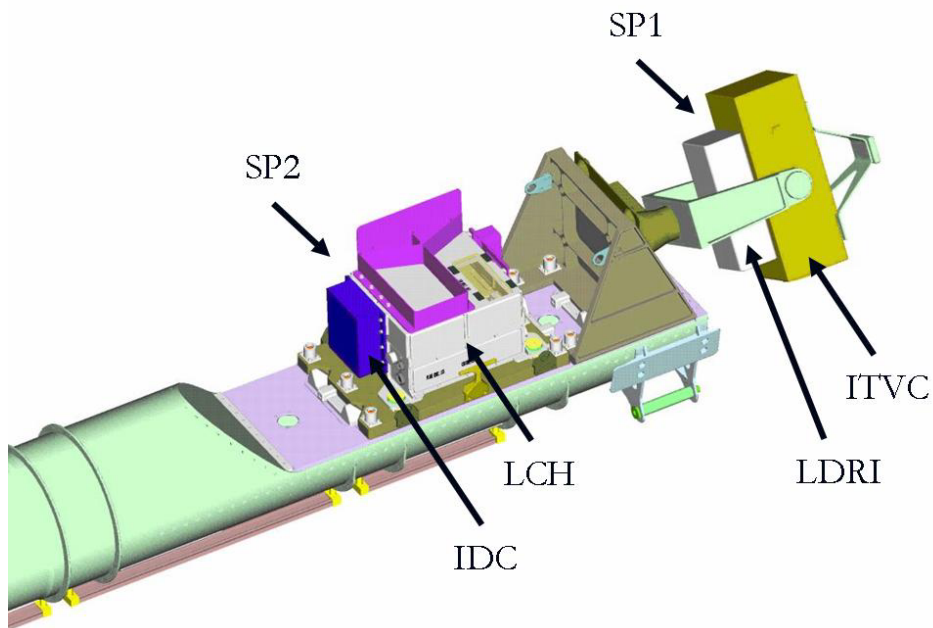
RCC Damage Inspection Requirements

|   | Through Hole Diameter <sup>(2)</sup> | RCC Exposed Substrate Diameter <sup>(3)</sup> | RCC Cracks <sup>(4)</sup> |
|---|--------------------------------------|---|---------------------------|
| RCC components  |                                      |   |                           |
| Nose Cap (Zones 1-3 and 7) and chin panel                           | TBD <sup>(1)</sup>                   | ≥ .080"                                       | ≥ .030" X 2"              |
| Nose Cap (Zones 4-6)  | TBD <sup>(1)</sup>                   | N/A   | N/A                       |
| Lower wing leading edge, Panels 1-7 and 11-22, Zones 1, 2, 3, and 4 | TBD <sup>(1)</sup>                   | ≥ .080"                                       | ≥ .030" X 2"              |
| Lower wing leading edge, Panels 8-10, Zones 2, 3, and 4             | TBD <sup>(1)</sup>                   | ≥ .080"                                       | ≥ .020" X 2"              |
| Lower wing leading edge, Panels 8-10, Zone 1                        | TBD <sup>(1)</sup>                   | ≥ .080"                                       | ≥ .030" X 2"              |
| Upper wing leading edge, Panels 1-22, Zone 5A                       | TBD <sup>(1)</sup>                   | N/A   | N/A                       |
| Upper wing leading edge, Panels 1-22, Zones 5B and 6                | ≥ 1"                                 | N/A   | N/A                       |

- NOTES: 1. Hole size to be determined from micrometeoroid and orbital debris study.
2. Holes are defined as penetrations through the outer and inner mold line of the RCC. Dimension in the table is the minimum distance between opposite sides of the penetration.

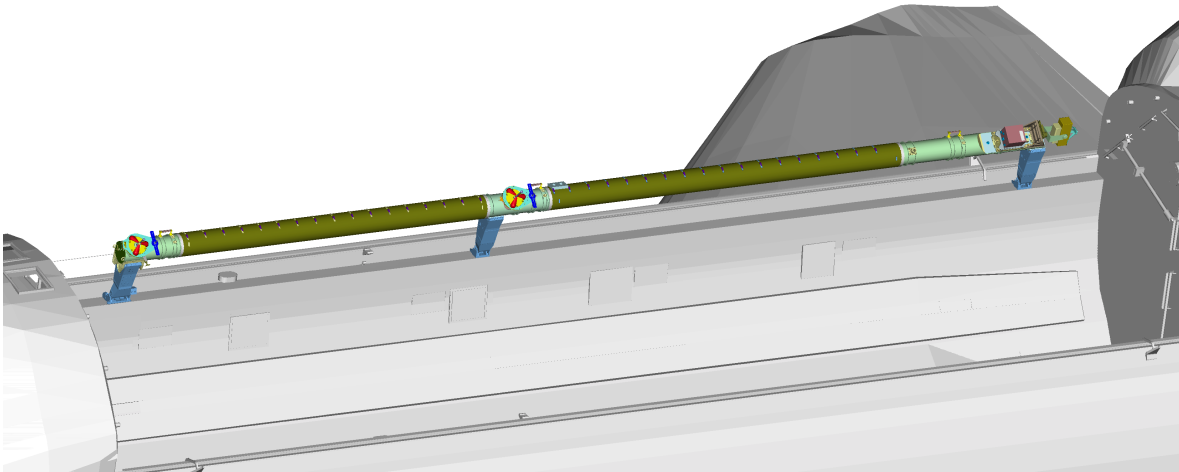
**Table 77-1. Inspection Requirements (concluded)**

3. Exposed substrate is defined as carbon-carbon weave devoid of Silicon Carbide (SiC). Dimension in the table is the minimum distance between opposite sides of the exposed substrate (does not include the area of any SiC, regardless of whether or not that SiC has been crushed or otherwise damaged).
4. Cracks are defined as highly elongated areas of exposed substrate and damaged SiC coating. The first dimension in the table is the minimum width of the exposed substrate along all portions of the crack. The second dimension is the length over which the minimum width of exposed substrate is continually present.



**Figure 77-1. Aft End of OBSS**

Note: The requirements are ever evolving. Check NSTS-60517 for the latest requirements.



**Figure 77-2. Integrated Boom Assembly Mounted on Starboard Sill**

The on-orbit components of OBSS consist of:

- An Integrated Boom Assembly (IBA) consisting of:
  - A boom assembly
  - A modified Electrical Flight Grapple Fixture (EFGF) assembly (Forward)
  - A modified Flight Releasable Grapple Fixture (FRGF) assembly (Mid)
- An Integrated Sensor Assembly (ISA) that mounts on the IBA (Aft)
- Three (3) Manipulator Positioning Mechanism (MPM) assemblies
- Wiring and support equipment (in the Orbiter Command Deck)

Lastly, the OBSS also consists of not only components internal to the Orbiter but those on the ground that support data analysis and operation of the system as well. See Figure 77-2 for the IBA as mounted on the starboard sill.

### 77.1.1 Interfaces

When stowed on the starboard sill, the boom element interfaces to the Orbiter provided MPMs via striker bars at three locations. An interface at the shoulder MPM provides keep-alive power for the sensor packages. The keep-alive power is disconnected and re-connected without EVA support. The MPMs support the boom system during ascent and landing. A limited amount of temperature telemetry is available in the SM downlist and the panel A8 light emitting diode (LED) display, while in keep-alive mode, via the Manipulator Controller Interface Unit (MCIU).

An EFGF is used for SRMS grapplings and manipulation of the IBA, as well as to provide a path for command, control, communications, and power to the sensor packages. The EFGF is electrically isolated from the structure. An FRGF is used to allow the SSRMS to grapple the boom assembly and hand it off to the SRMS.

The interface between the base boom element and the sensor package allows the sensor package to be removed and replaced by EVA crew. The interface contains electrical connectors that pass command and control signals, data outputs, and keep-



alive power from the boom assembly to the sensor package assembly. The mechanical interface also supports the attachment of an EVA worksite in addition to the sensor assembly.

The following is a general overview of crew/MCC interfaces with the OBSS:

Inputs:

- A. Panel A7: switch inputs are used to select the ITVC/LDRI images as well as control LDRI modes.
- B. Panel R12: crew inputs to the VPU, WIB, OBSS Patch Panel (OPP) (officially still named the OSVS Patch Panel), and OBSS Panel. There is a circuit breaker as well as switch controls on these panels. Also, the PDIP cable is used to connect RSC video to the PL3 input.
- C. Panel A8L (A8A2): switch inputs for keep-alive power.
- D. IBM A31P Laptop: crew control of LCS package. The laptop contains the Laser Camera Controller (LCC) software which interfaces with the Laser Camera Head (LCH). The laptop also contains DCCS software which interfaces with the IDC.
- E. Standard Switch Panel 1 (SSP1): switch input for the Assembly Power Converter Unit 2 (APCU2) which sends +124V power to the LCS. This is a flight specific configuration.

Outputs:

- A. Panel A8: LED display with limited OBSS telemetry. It is configurable with rotary switches.
- B. MCIU: limited OBSS telemetry in SM downlist, also routes some telemetry to panel A8 digital display.
- C. PGSC: output from LCH/IDC to LCC/IDC IBM A31P laptop.
- D. CCTV PL2: ITVC/LDRI video (if VPU jumper is in the LDRI/ITVC port)
- E. CCTV PL3:RSC video
- F. Panel A7: Mode lights

See Figure 77-3 below for an overall interface diagram of the OBSS.

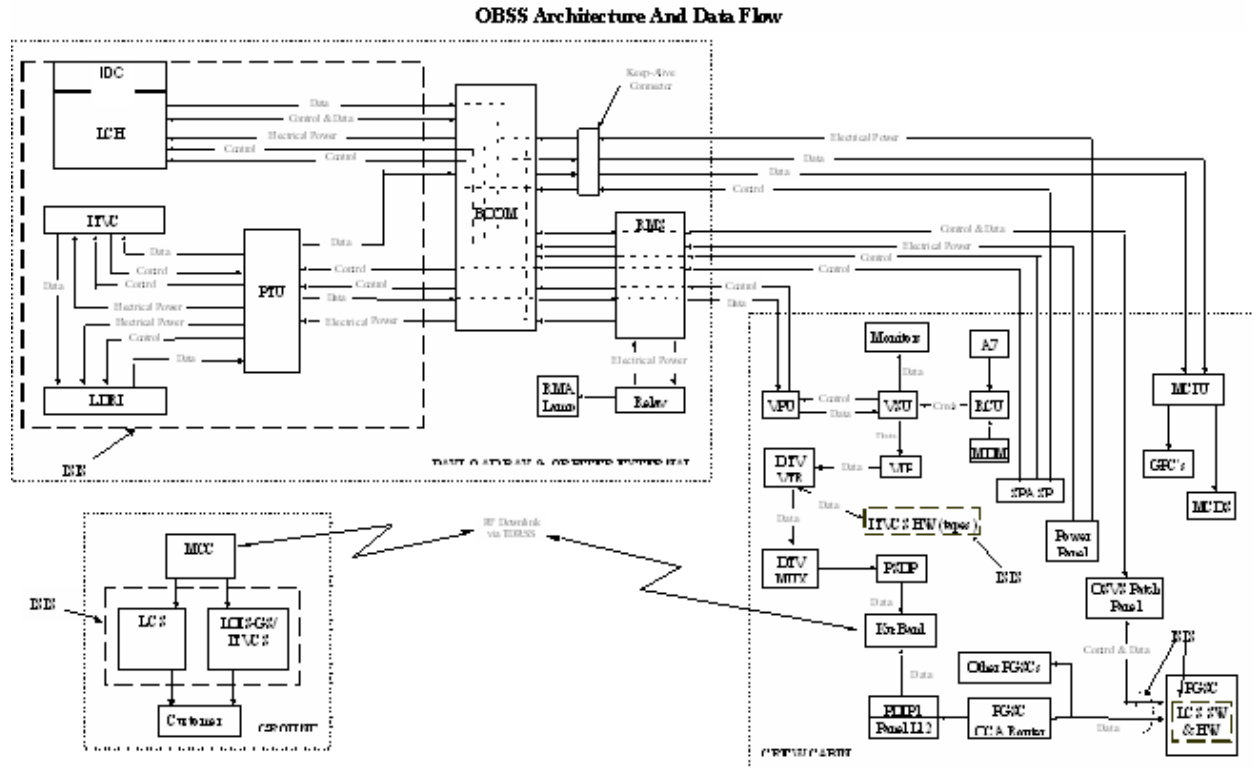


Figure 77-3. OBSS Overall Diagram

## 77.2 OVERVIEW OF OBSS USAGE

### 77.2.1 Inspection

The OBSS is used to perform inspections on RCC panels, Black High Temperature Reusable Surface Insulation (HRSI) tiles, Black Fibrous Refractory Composite Insulation (FRCI) tiles, White Low Temperature Reusable Surface Insulation (LTRSI) TPS tiles, and fillers and seals around surface penetrations.

#### 77.2.1.1 Motion

The OBSS performs inspections while the sensor package is translating along the area to be inspected at a maximum rate of 1 meter/minute.

#### 77.2.1.2 Lighting

The OBSS is capable of operating in all lighting conditions except for when the sun is directly in the sensors' field of view.

### **77.2.2 Recording of Scan**

The OBSS scan is downlinked real-time via Ku-Band and is simultaneously recorded onboard on a DSR-20. A spare DSR-20 is manifested for redundancy. In the future, the program may upgrade to a DSR-25. INCO keeps track of all LOS times during the scan so that those times can be passed on to the crew for later playback. Any LOS during the scans, larger than 1 second is included in INCO's list.

### **77.2.3 EVA Worksite**

The OBSS boom assembly is capable of having an EVA worksite mounted on it in addition to the sensor assembly. It will also be capable of having a crew member on the end of the boom while the OBSS is being maneuvered by either the SRMS or SSRMS. Potentially, this allows the boom assembly to support the EVA crewperson for repair of the TPS, if necessary. For initial Return to Flight, the boom assembly will NOT be used as a base for TPS repair due to stabilization problems which could cause the SRMS brakes to slip.

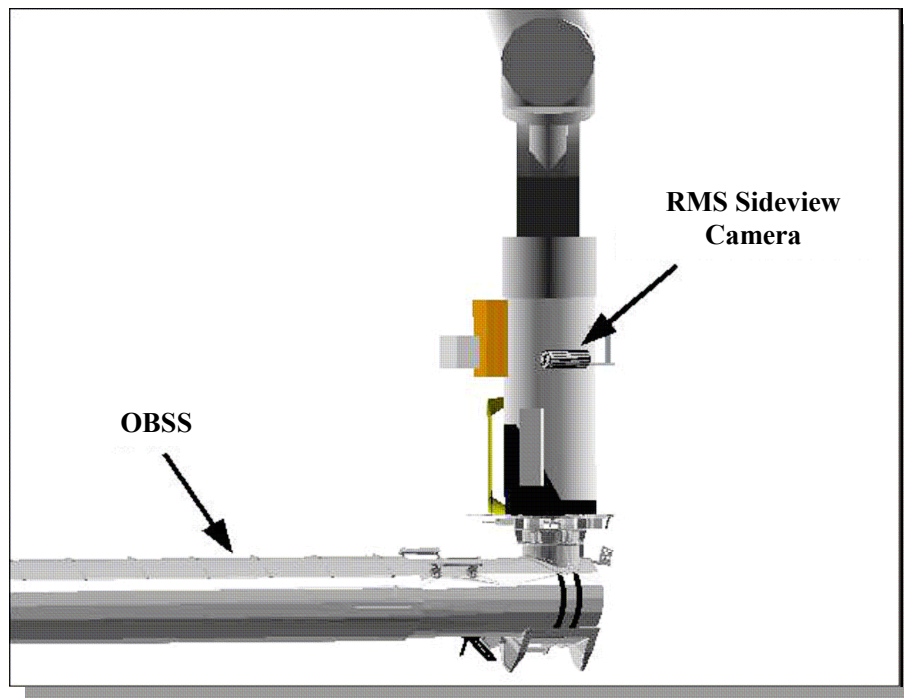
### **77.2.4 Jettison**

The OBSS equipment in the payload bay, including portions of the MPMs, is capable of being jettisoned via crew switch throw on panel A14.

## 77.3 DESCRIPTION

### 77.3.1 Remote Manipulator System (RMS) Sideview Camera (RSC)

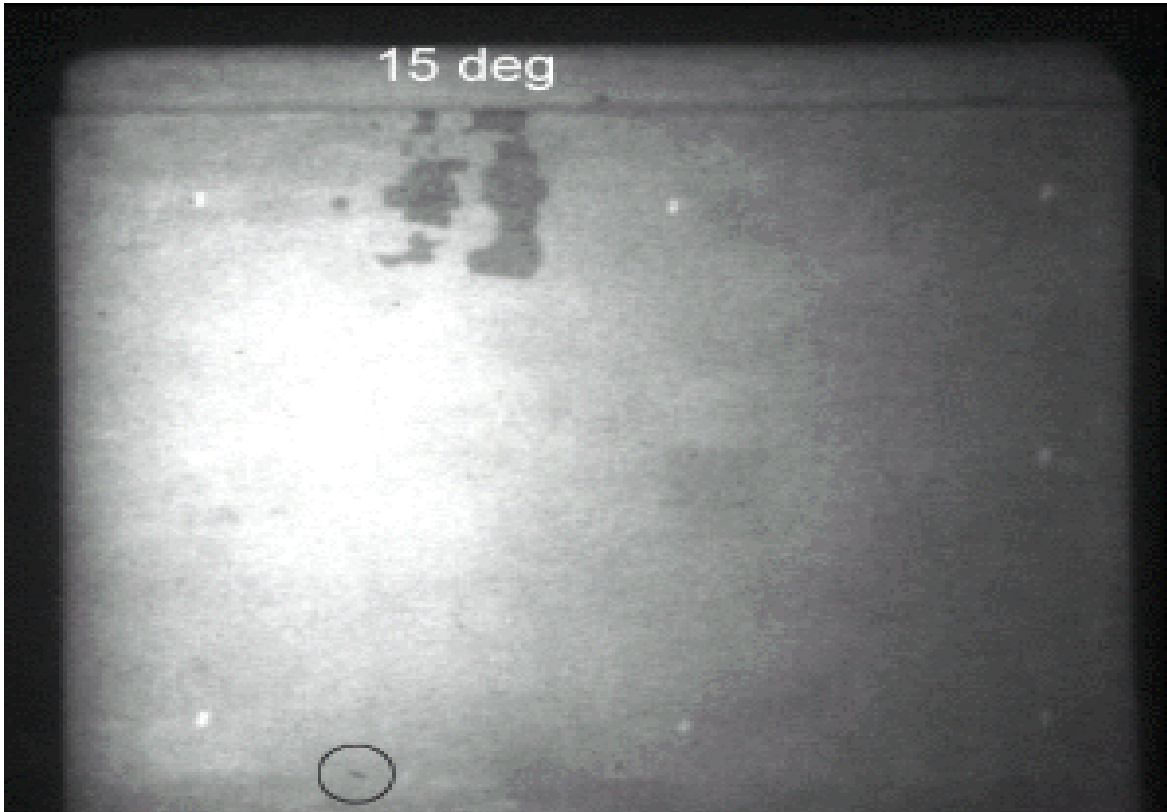
The RSC is a black & white asynchronous camera, built by Videospection Corp, which is mounted on the side of the SRMS wrist roll joint. It is used by the crew for situational awareness during boom operations. It has a fixed focal length and fixed focus determined preflight. For most flights, it will be 30 degree field of view (FOV) with a focus at 35 feet. An exception is SVS flights where it will be 22 degree FOV with focus at infinity. The exposure control is automatic with no option for manual selectability. This camera has no pan tilt unit and therefore is stationary with respect to the SRMS. The RSC also serves as an illuminator with 156 LEDs available for illumination down the length of the boom. There are 4 different illumination levels available, High-156 LEDs, Medium-84 LEDs, Low-30 LEDs, and off with no illumination. The RSC illuminator is toggled via the K1 relay which also resets the LDRI/ITVC PTU pan and tilt angles and takes the LDRI to standby. There are two internal 4 watt heaters in the RSC which activate at 9 degrees C and deactivate at 13 degrees C. The heaters receive their power from RSC camera power (S2 on the OBSS panel), not from illuminator power. Figure 77-4 shows a rendering of the RSC and its mounting on the SRMS.



**Figure 77-4. RMS Sideview Camera near the End Effector**

### 77.3.2 Intensified Video Camera (ITVC)

The ITVC manifested as part of sensor package 1 is a standard ITVC. The lens can be adjusted from a field of view (FOV) of approximately 4 degrees to approximately 50 degrees. The wide FOV is helpful for situational awareness and gross TPS surveys

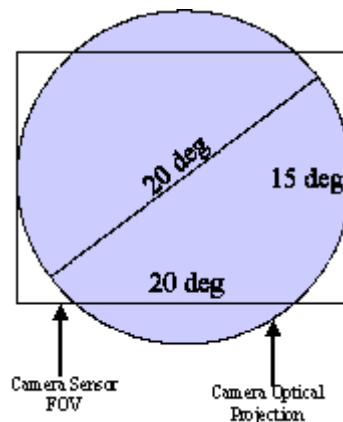


**Figure 77-5. ITVC Image of RCC Damage (10ft)**

(inspecting for large damaged areas). The narrow FOV is helpful for inspecting details of small defects. The LDRI can provide illumination for the ITVC in dark conditions. The illumination is supplied at a wavelength of 805nm, which is not in the eye's visible spectrum but is received well by the ITVC light intensifier. The resolution of the ITVC is too low for adequate 0.25" through hole detection but can be used as a backup to LDRI and LCS for 1" through hole damage. Figure 77-5 shows a sample ITVC image of RCC damage at a distance of 10 feet.

### 77.3.3 Laser Dynamic Range Imager (LDRI)

The LDRI, developed by Sandia Laboratories, is the primary sensor used for RCC inspection for Return to Flight. The LDRI provides a source of both standard 2-Dimensional video and video data that includes 3D information about the target. The LDRI is configured with a fixed 50mm lens that provides approximately a 15 x 20 degree FOV. The aspect ratio is 4:3 with rounded corners as shown in Figure 77-6.



**Figure 77-6. LDRI Sensor Field of View**

As a black and white video camera, the resolution of the LDRI is comparable to the ITVC. When configured in a mode to acquire 3D data, the LDRI modulates its illumination source and produces a video image that appears to flicker. This data can

**Table 77-2. OBSS Sensor Performance**

| Camera | 4x margin for Detectable Resolution (in.) [thru-hole dia] | Max Range (ft) | HFOV (deg) | Maximum Incidence Angle (deg) | Estimated FOV Horizontal vs. Vertical (inches) | Scan Rate (m./min.) |
|--------|---|----------------|------------|-------------------------------|--|---------------------|
| LDRI   | 0.25  | 7              | 20         | 30                            | 29" x 21" *                                    | 1                   |
| LDRI   | 1   | 10             | 20         | 30                            | 41" x 31" *                                    | 3                   |
| ITVC   | 0.25  | 5              | 8          | 35                            | 8.4" x 6.3"                                    | 0.53                |
| ITVC   | 0.95  | 10             | 15         | 35                            | 32" x 24"                                      | 2.0                 |
| LCS**  | 0.25  | 10             | 30         | 35                            | 63" x 63"                                      | 1                   |
| LCS**  | 1   | 10             | 30         | 35                            | 63" x 63"                                      | 3                   |

\*4:3 HFOV to VFOV ratio but has curved corners

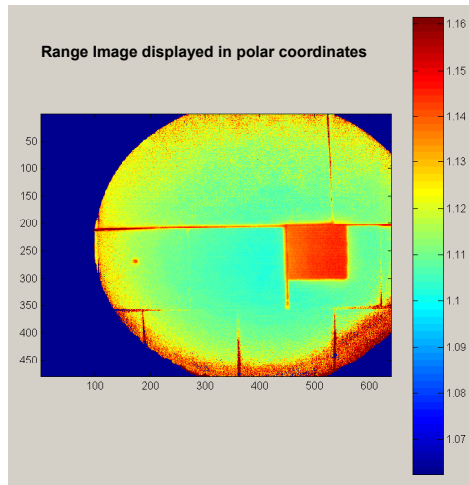
\*\* Performance details reported for environment with no unintentional boom oscillations

Reference: OBSS Sensor Performance Presentation, Jim Siekierski (EV), 1/30/04.

be processed to provide quantitative measurements of length, width, and depth of the feature being inspected. The LDRI can operate in a 2D inspection mode while stationary or in motion due to either translation of boom oscillations. Using the Continuously Scanned Image Set Data Collection Method, the LDRI can collect 3D data while the SRMS moves in a direction parallel to the surface to be measured. 3D data

can be collected using this method as long as the sensor maintains the range, angle of incidence, and scan rate criteria as defined in Table 77-2.

The LDRI can be used for 2D and 3D TPS inspection in both well-lit and dark conditions. Figure 77-7 shows a sample of the depth information provided by the LDRI sensor.



**Figure 77-7. LDRI Sample Range Image**

The LDRI sensor is mounted to the bottom of the ITVC camera, which is mounted on a standard pan/tilt unit (PTU). The LDRI sensor can be maneuvered by crewmembers using the CCTV controls on the aft flight deck. The crew can control LDRI modes and transitions between LDRI and ITVC from panel A7. Figure 77-8 shows the LDRI/ITVC along with the PTU and counterweight assembly as flown on STS-97 as a Detailed Test Objective (DTO).



*Figure 77-8. LDRI/ITVC from STS-97 DTO*



### 77.3.4 Laser Camera System (LCS)

The LCS, by Neptec, consists of the Laser Camera Head (LCH), a crew cabin IBM A31P laptop identified as the Laser Camera Controller (LCC), and data processing applications running on workstations in a laser system data analysis lab. It produces detailed 3D images of the target surface. An example of the LCS range image is provided in Figure 77-9. The LCS is a spot scanner system that collects an array of data points. The array size is operationally configurable over the following range: 2x2 array to a 1024x1024 array. This array of data points can be spaced across any FOV between 5 and 30 degrees. Combinations of these values can be set to configure the sensor for either a quick search for large damaged areas or a detailed inspection of a small defect. The sensor operates at approximately 1500nm and is unaffected by all natural lighting conditions. Accurate depth information can be attained from a scan with the sensor platform both stationary or in motion, including unknown oscillations caused by boom dynamics.

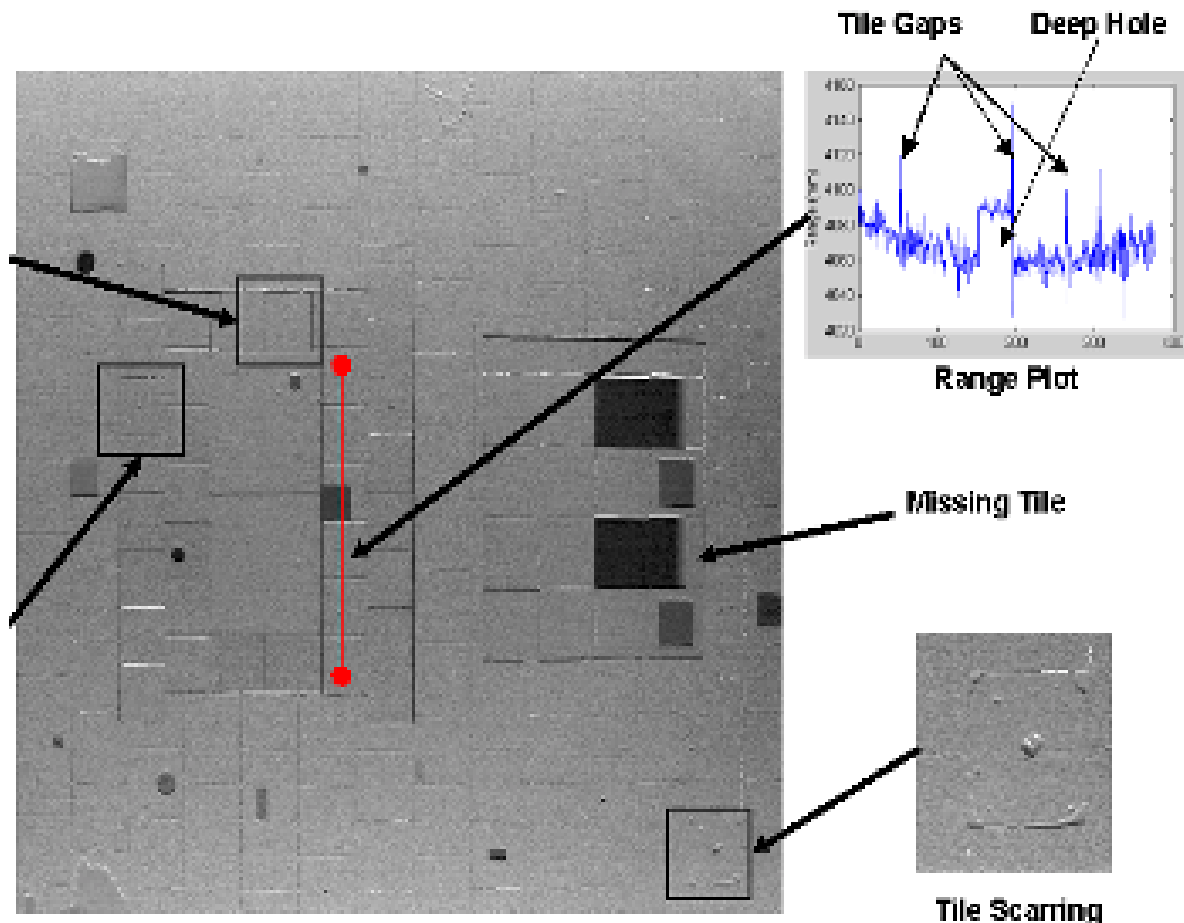


Figure 77-9. LCS Sample Range Image

In general, the best performance of the system will result from a sensor platform that is stationary. While translating, the system operates in a line scanner mode.

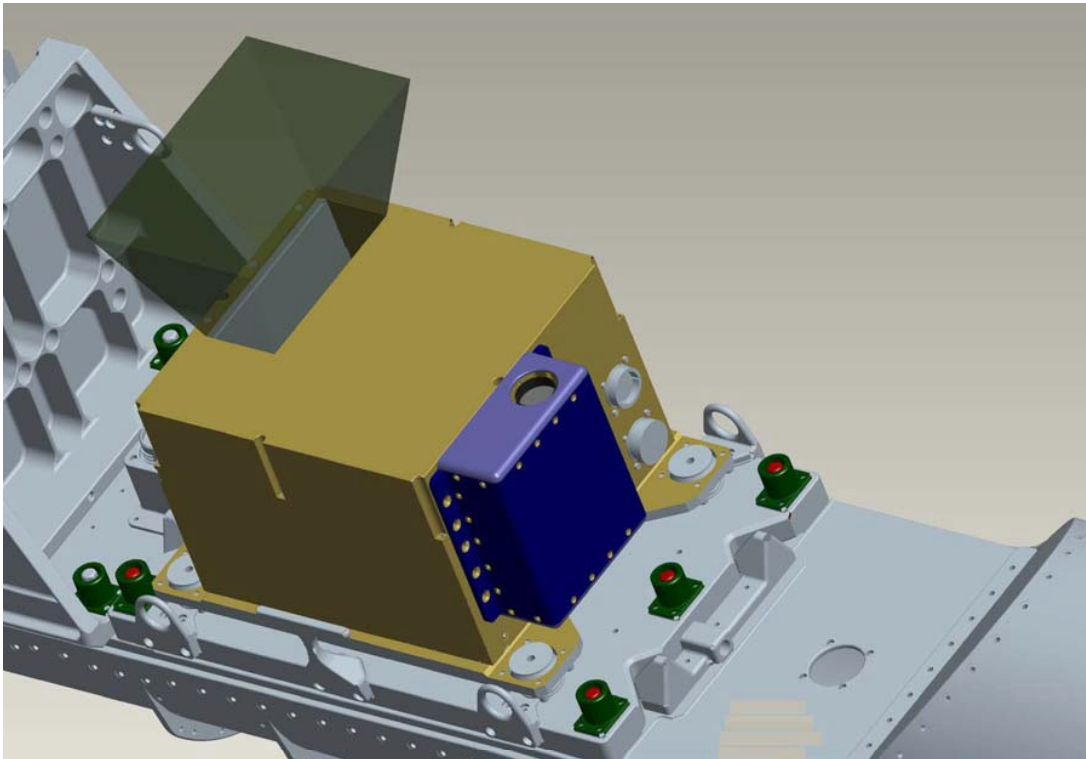
The translation of the boom can move this scan line across the target to collect depth information for the TPS surface. Unknown oscillations imparted on the sensor platform by the boom may affect the reconstruction of complete 3D models of the TPS surface, but the accuracy of the depth measurements is unaffected. The depth information is sufficient to provide the data necessary to detect surface damage, and can be used to supplement standard imagery in the damage detection process. Operating in line scanner mode also allows the effective LCS FOV to be increased to approximately 40 degrees.

LCS is fixed with no pan/tilt capabilities. However, the LCS was designed with all necessary interfaces to make mounting the LCS on a PTU possible for future consideration.

### **77.3.5 ISIS Digital Camera**

The LCS also includes electrical and mechanical provisions for the mounting of an ethernet device, a high resolution NASA-supplied digital camera, the IDC. The camera is an Adimec-2000m 1920x1080 pixel, 10-bit monochrome CCD camera. The lens is ground interchangeable at 35, 50, or 75mm. The camera is paired with the Pleora iport PT1000-CL, an ilink to ethernet converter box. The camera, converter box, and heaters collectively are called the Digital Camera Assembly (DCA)

The purpose of this camera is to capture images of damage detected by the other inspection sensors, not be a primary inspection sensor itself. The IDC is mounted to the side of the LCH as illustrated in Figure 77-10. Figure 77-11 shows the Adimec-2000m, along with the Pleora converter box.



**Figure 77-10. LCH with IDC mounted on side**

The IDC receives conditioned power directly from the LCH, +12V for the actual camera and +12V for the converter box and communicates through the LCH's ethernet switch. There exist two heaters in the DCA, one 4.1W heater used while berthed, and a 14W heater used while the OBSS is grappled by the SRMS. Both heaters are thermostatically controlled between 20 and 35° C. Note that the 14W heater is undersized and insufficient for the IDC, therefore, it requires heat from the LCH heaters as well.

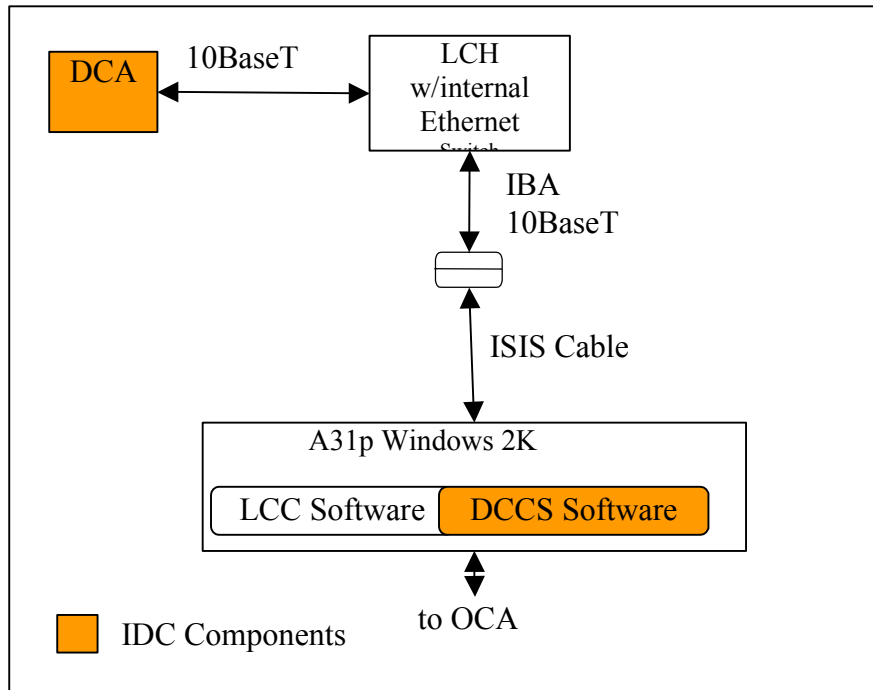
Although, LDRI can be used for illumination for the IDC, sunlight is its optimal source.

As with the LCS, the crew controls the IDC from their A31P and images are routed back to that respective A31P and onto OCA for downlink. Specifically, the IDC files are stored as uncompressed 16-bit tiff files at around 4MB per file. Only 10-bits worth of the images are OCA downlinked, and only 8-bits are displayed on the laptop. Both the LCC and Digital Camera Control Software (DCCS) software run on Win2K. A basic system diagram is shown in Figure 77-12. As seen in the figure, the LCH contains an internal ethernet switch which enables the same laptop to be used for both the LCS and IDC.

Note: LCH must be powered up before the IDC can be operated.



**Figure 77-11. Adimec-2000m and Pleora Converter Box**



**Figure 77-12. IDC/LCH to OCA Block Diagram**

## 77.4 OPERATIONS

The highest probability of damage to the TPS is during the ascent phase of flight. OBSS works in conjunction with other imaging resources such as Enhanced Launch Vehicle Imaging System (ELVIS), Wing Leading Edge (WLE) sensors, and the Flight Day 3 R-bar Pitch Maneuver (RPM) to assess possible damage caused during ascent. The inspection is not used to look for damage caused by Micro-Meteoroid Orbital Debris (MMOD).

### 77.4.1 Boom Positioning

Boom positioning for surveys is done with a combination of autosequence and manual maneuvers. Flight rule clearances differ whether in autosequence or manual mode.

#### 77.4.1.1 Autosequence

Autosequence mode allows the RMS to run a predefined sequence of motions with little crew intervention. Pause points can be programmed into the sequence or the crew can command a pause event in real-time. Camera settings such as pan, tilt, and zoom can be adjusted during these pause points. Once these adjustments are made, the autosequence can continue from the pause point. If a pause occurs and the RMS is physically moved, for example if the crew wants to move the sensor package closer to the target, the RMS must return to the predefined start/stop point and duplicate part of the autosequence before continuing.

### **77.4.1.2 Manual Mode**

The crew can manually maneuver the RMS and, therefore, the boom. This will allow real time adjustments to be made should there be any errors in the predefined inspection autosequence. Flight rules for crew operated manual RMS modes specify a minimum clearance of 2 feet between the RMS end effector and other structures. To satisfy this flight rule, the sensor package cannot be placed closer than 2 feet from any Orbiter surface during manual RMS maneuvers. Since flight rule clearance for manual mode is less restrictive than the 5 feet clearance required in autosequence, manual mode allows greater maneuver flexibility and can be used to gain additional detailed information on critical sections of the Orbiter surface. However, it should also be noted that, because the sensors are fixed focus, the boom could be maneuvered to a point that is so close to structure, that images would be too fuzzy to be of value.

### **77.4.2 Modes of Operation for the ITVC/LDRI Assembly**

There are six modes of operation for the LDRI. The modes are selected from A7 or by uplink command. Each of these modes is discussed in detail below. See CCTV System Brief 70 for ITVC operations.

#### **77.4.2.1 Mode 1: Standby**

This mode allows the nominal video signal from the ITVC to pass through the LDRI. The LDRI illumination source is off while in this mode. This mode is entered upon LDRI power-up, in the event of an LDRI overtemp condition, when the Mode 1 command is sent, or when the K1 relay is cycled. This mode of operation is used for ITVC inspections with suitable natural lighting conditions.

#### **77.4.2.2 Mode 2: Illumination**

This mode allows the nominal video signal from the ITVC to pass through the LDRI to the CCTV system, and provides laser illumination continuously. Mode 2 is also used to help keep the sensor warm as Mode 1 was deemed as insufficient in that manner. This mode also improves ITVC performance in low-light conditions by providing an 8W light source that is visible to the camera. Pulse timing of 60 cycles per second is synchronized with the CMD/SYNC input to the LDRI. The center wavelength is 806nm, which is in the infrared (IR) spectrum. As long as the LDRI internal temperature is maintained below 50° C, the optical burst duration is 4.86ms, yield around 2W of average light intensity.

#### **77.4.2.3 Mode 3: LDRI Active**

This mode provides intensified monochrome video over a fixed FOV in day or night conditions. Video output in this mode is 2D and will be similar to the illuminated ITVC output. Unlike the ITVC, the sensor incorporates a spectral filter designed to block “out-of-band” light, therefore, this mode may tend to exhibit less solar-shadowing than the ITVC, particularly at short range. This mode of operation can be used to acquire video

images of the TPS should there be an ITVC failure. Mode 3 is best suited for scenes with low contrast.

#### **77.4.2.4 Mode 4: LDRI Active with Gamma Correction**

Similar to mode 3 but with the addition of Gamma correction. This mode is best suited for scenes with high contrast.

#### **77.4.2.5 Mode 5: High Resolution**

This mode provides LDRI pulsating video images and concentrates on providing the highest level of sensitivity, with ambiguity in absolute distance. Mode 5 is required for producing high-resolution depth measurements. Modes 5 and 6 are easily distinguished from Modes 1-4 by the flicker or pulsation apparent in the video. Note that Modes 5 and 6 generate more internal heating than other modes. Mode 5 is best suited for scenes with low contrast.

#### **77.4.2.6 Mode 6: High Resolution with Gamma Correction**

Similar to mode 5 but with addition of Gamma correction. This mode is best suited for scenes with high contrast.

### **77.4.3 Modes of Operation for the LCS Assembly**

#### **77.4.3.1 Quickview**

In Quickview mode, the crew has the ability to visually verify the content of the FOV sensor prior to taking a more time consuming detailed scan. The A31P laptop running the LCS application in the Orbiter crew cabin contains the controls for this mode of operation. Once the proper command is executed, approximately 10 to 30 seconds will elapse before an image is displayed on the PGSC. The crew can then verify the sensor is pointed in the correct direction prior to continuing the detailed scan.

#### **77.4.3.2 Detailed Scan**

In Detailed Scan mode, the LCS can be used to scan an object to create a 3D high-resolution image. This data can be processed by ground software to create 3D image models, or make quantitative measurements to inspect an object. This mode of operation should be used for "stop and stare" inspections. Reducing the effective motion in the tip of the boom will increase the probability of detecting damage in this mode of operation. The LCS design also includes the accelerometers in the LCH, which could be used to alert the crew if the boom tip oscillations would affect the quality of the LCS scans.

### **77.4.3.3 Line Scan**

Line Scan mode is similar to the Imaging Mode, except that motion of the laser is varied in only 1 axis, thus producing a line of data collection. This single-axis motion may involve either one or both of the pointing mirrors internal to the sensor head (LCH), and the scan line will always pass through the optical centerline. If both mirrors are used, the effective FOV of the sensor can be increased to approximately 40 degrees. The sensor relies on the physical motion (translation) of the sensor head to provide the second axis of laser pointing. This mode of operation should be used while imaging with a constant translation motion of the inspection sensor. The angle of the scan line can be adjusted such that the LCS scans perpendicular to the axis of motion as much as possible. Unknown oscillations imparted on the sensor platform by the boom may affect the reconstruction of complete 3D models of the TPS surface, but the accuracy of depth measurements is unaffected. The depth information gathered in line scan mode is sufficient to provide the necessary data to detect surface damage, and can also be used to supplement 2D imagery when attempting to detect TPS damage. This mode of operation is not intended for use during “stop and stare” inspections but can be used if necessary.

### **77.4.3.4 SRMS-based Keep Alive Mode**

The SRMS-based Keep Alive Mode is designed to keep the LCS unit within thermal limits while attached to the SRMS. Unlike Berthed Keep-Alive Mode, the unit is receiving 124V power. To enter this mode, a command must be sent from the LCC to the LCH. The LCH responds by shutting down all electronics not associated with its heater circuits. Further communication with the LCH is not possible until the 124V power is cycled. Upon initial powerup, LCH will come up in standby.

### **77.4.3.5 Berthed Keep Alive Mode**

While berthed in the MPMs, the LCH receives 28V power from the Orbiter and uses this power for thermal management to keep the unit’s electronics within their storage temperature range. No communication with the LCH is possible in this mode.

### **77.4.3.6 Standby**

Standby mode is only available when receiving 124V power. In this mode, the electronics are fully powered and communicating with the LCC. In addition, if the LCC stops communicating with the LCH, both go to Standby.

## **77.4.4 Scan Types**

The following section outlines the different types of scans and what scenario would necessitate each respective type of scan. Table 77-3 summarizes the general assumptions and constraints given each type of scenario.



**Table 77-3. Inspection Scenarios**

| Inspection Scenario # -><br><br>Assumption/Constraint | 1<br>LDRI<br>scan | 2<br>LCS scan<br>from<br>movable<br>base | 3<br>LDRI<br>Stop<br>and<br>Stare | 4<br>LCS<br>Stop<br>and<br>Stare<br>from<br>movable<br>base | 5<br>ITVC<br>scan | 6<br>LCS<br>scan<br>from<br>fixed<br>base | 7<br>LCS<br>stop<br>and<br>stare<br>from<br>fixed<br>base | 8<br>EVA<br>redundancy |
|---|-------------------|--|-----------------------------------|---|-------------------|---|---|------------------------|
| Operates on PTU on boom                               | x                 | x  | x                                 | x   | x                 |   |   |                        |
| Sensor operations commanded from AFD                  | x                 | x  | x                                 | x   | x                 | x   | x   |                        |
| Adequate visual cues for arm and berthing ops         | x                 | x  | x                                 | x   | x                 | x   | x   | x                      |
| Autosequence for arm position                         | x                 | x  |                                   |   | x                 | x   |   |                        |
| Overlap in scanned images necessary                   | x                 | x  |                                   |   | x                 | x   |   |                        |
| RMS manually maneuvered to damage location            |                   |  | x                                 | x   |                   |   | x   |                        |
| Adequate lighting required                            |                   |  |                                   |   | x                 |   |   | x                      |
| ISS payload deployed from Orbiter                     |                   |  |                                   |   |                   |   |   | x                      |
| Fixed base limits coverage of starboard RCC           |                   |  |                                   |   |                   | x   | x   |                        |
| Positioning of EVA crew person on boom from AFD       |                   |  |                                   |   |                   |   |   | x                      |

#### **77.4.4.1 LDRI Scan**

The typical LDRI scan is the prime sensor used for damage detection and damage measurement. This is done on FD2 for initial damage detection and measurement. Future scans after docking allow follow up on areas of interest identified with the FD2 scan and FD3 DCS 760 imaging performed during the RPM. The LDRI scan is performed with autosequence trajectories covering the nose cap, starboard and port RCC.

#### **77.4.4.2 LCS Scan**

The LCS scan is the backup sensor used for damage detection and measurement. The assumption is that the LDRI is inoperable. The timeframe and the areas to be scanned are the same, however, the autosequence will be different because of the LCS's position on the boom and the fact that it is not mounted on a PTU.

#### **77.4.4.3 LDRI Stop and Stare**

LDRI stop and stare is used to gain additional imaging for more precise depth measurement on a known damage location. This will be done while docked at the ISS.

#### **77.4.4.4 LCS Stop and Stare**

Similar to the LDRI stop and stare except that LCS stop and stare is the prime sensor to gain additional 3D information on a known damage location.

#### **77.4.4.5 ITVC Scan**

The ITVC scan is a contingency scan for initial damage detection. It is assumed that both the LCS and LDRI are inoperable. The scan is performed in a similar manner to the LDRI scan but at a much closer range to the target.

#### **77.4.4.6 IDC Imaging**

Like the LCS Stop and Stare, the IDC will be one of the prime focused inspection sensors but for 2D vice 3D.

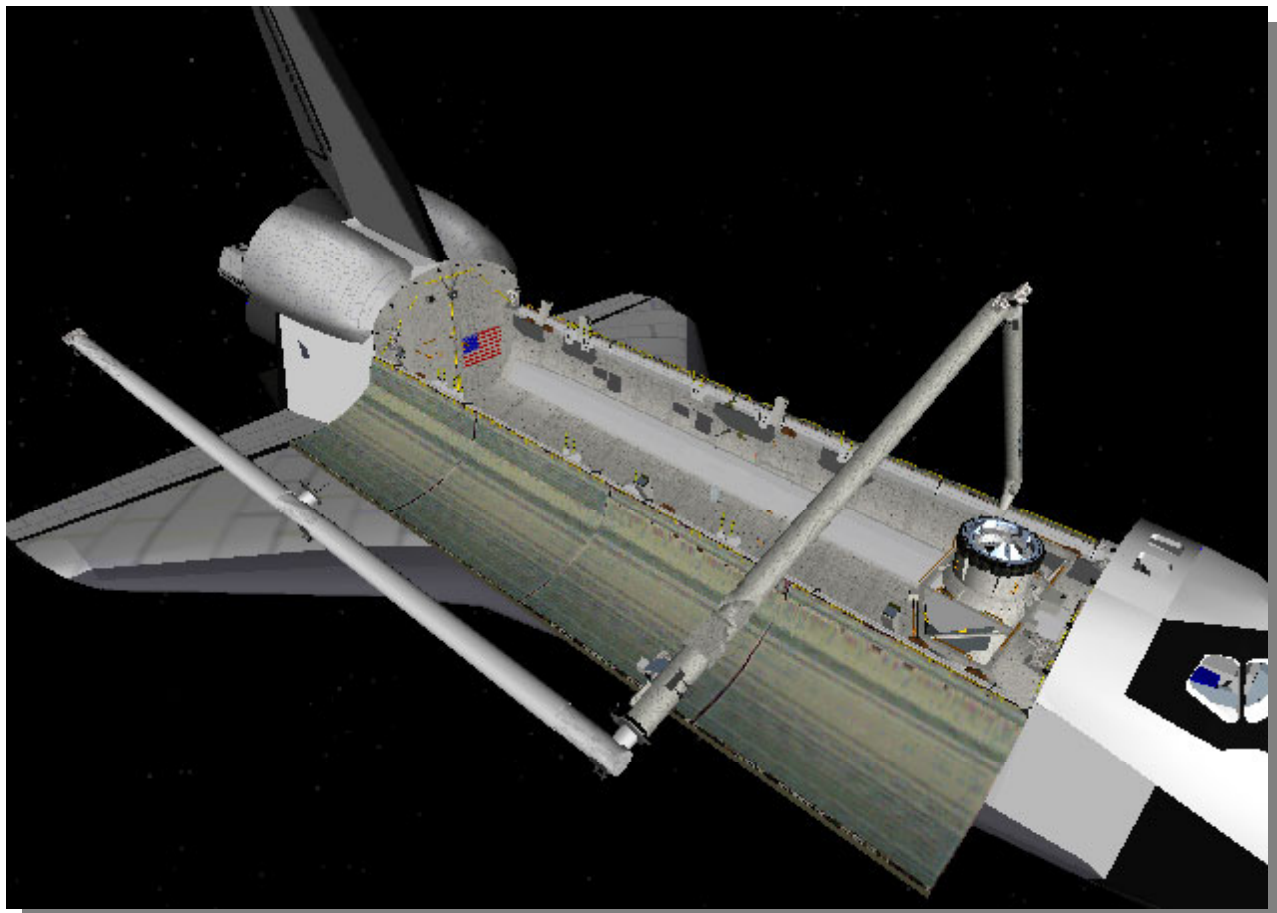
#### **77.4.4.7 EVA Crewmember with Handheld Digital Camera**

This is a contingency plan to the contingency plan in the case that all OBSS sensors are unusable. The EVA crewmember would either use the OBSS EVA mount to support themselves while taking digital still pictures or use a SAFER to fly to the underside of the Orbiter.

#### 77.4.5 Handling of the Boom

The boom's keep alive power is turned on in the PDRS On Orbit Init procedure performed just after Post Insertion. The sensor packages have a 90 minute survival time, when unpowered on orbit. The first component to freeze is the PTU (pan motor).

After SRMS powerup and checkout, the MPMs are rolled out, the SRMS end effector is maneuvered over the EFGF and keep alive power to the boom is removed. Next, the SRMS grapples the boom at the EFGF. Then, the Manipulator Retention Latches (MRLs) are commanded to unlatch, and the SRMS is commanded to remove the OBSS from the MPMs. The Ready-to-Latch (RTL) indicators show when the striker bars have cleared the RTL envelope. Following that, the boom sensors are powered up. After sensor checkout and characterization by the imaging team, the boom survey can begin. See Figure 77-13 for an illustration of the SRMS grappling the boom and holding it over the starboard wing.



*Figure 77-13. Boom Grappled by RMS*

#### **77.4.5.1 Undocked Survey**

All OBSS maneuvers are performed in manual mode by the crew while all surveys are performed via autosequence. The overall sequence of events in the survey are: maneuver to begin starboard survey, starboard survey, maneuver to nose cap survey, nose cap survey, maneuver to port survey, port survey.

After the survey, OBSS is reberthed, latched, ungrappled and keep alive power is reapplied.

#### **77.4.5.2 Docked Survey**

While docked to the ISS, the SSRMS is required to handoff the OBSS to the SRMS for any survey. The SRMS cannot physically grapple the OBSS as the lab is directly in the way. In addition, the clearance between the payloads in the payload bay and the OBSS is extremely small. While the OBSS is stowed on the starboard MPMs, the clearances are as small as 3" with no misalignments. This means the OBSS must be deployed before the unberthing of a payload can take place.

The SSRMS grapples the OBSS at the FRGF. Keep alive power is then removed, starting the sensor package's thermal clock. Next, the SSRMS unberths the OBSS at which time the boom will pass within 3 feet of the ISS UHF antenna. The maneuver is in the starboard direction to clear the antenna.

The SSRMS then maneuvers to handoff position which is far enough up and aft to clear both the ISS and payload bay. The SRMS grapples the OBSS at the EFGF and sensor power is applied. The handoff time is very close to and may exceed the sensor package thermal time limit. Next, the SSRMS releases the OBSS and the SRMS maneuvers the OBSS to a temporary stowage position.

For some missions, the SRMS will place the OBSS in a "park" position when not performing any scanning operations. This can allow the OBSS ITVC to gain views of the ISS unattainable by an other station or shuttle assets.

The SRMS hands the OBSS off to the SSRMS for reberth operations prior to undock. The general flow is a reverse sequence. However, the operation takes additional time due to nominal temperature induced deformation of the orbiter sill. Past flight experience shows that the SRMS cradle routinely takes additional time to achieve 3 RTL indicators and the same is expected of OBSS.

#### **77.4.6 Ground Processing**

Sensor data collection during the on-orbit TPS inspection is relayed to the ground where three sensor data processing laboratories, KX (JSC imaging experts), Sandia, and Neptec, analyze the data in detail. The output products are integrated by KX into a report identifying and presenting measurements for any observed orbiter TPS damage. The report is provided to the MER, Mission Management Team (MMT), and the System Engineering and Integration (SE&I) organization.

#### **77.4.6.1 ITVC Video Data**

KX has the prime responsibility of analyzing ITVC data on the ground. Sandia may assist in the analysis but has no official responsibility for this task.

#### **77.4.6.2 Neptec LCS Data**

Neptec has the prime responsibility for processing and analyzing all LCS data for the first two missions in which it flies. The analysis includes detecting any suspect areas during “line scan” translation and “stop and stare” modes of operation. Neptec presents their findings, results of measurements, and level of certainty, including pictures and analysis, to KX. KX then correlates Neptec’s findings with their own and passes it on to the appropriate channels. Any LCS data which cannot be integrated with the ITVC results is passed to management as-is. After the first two LCS missions, KX personnel will be trained by Neptec to analyze the LCS 3D data.

#### **77.4.6.3 Sandia LDRI/LOIS**

Sandia and KX have a dual responsibility of reviewing LDRI data for the first two RTF missions. KX reviews the images as though the data is 2D ITVC data. Sandia analyzes the 2D intensity images as well as the processed 3D ranges images. Sandia presents their findings to KX who then correlates those findings with their own and channels the information to the proper management. Any LDRI data which cannot be integrated with other sensor data is forwarded to management as-is. For subsequent missions, KX personnel will be trained by Sandia to analyze LDRI 3D data.

#### **77.4.6.4 Imagery Management**

The TPS Imagery Coordinator (TIC) is the responsible KX party for all mission related activity associated with TPS on-orbit surveys and subsequent tracking of imagery products. TIC provides the interface between the sensor teams and the Flight Control Team.

A web based interface consisting of status and control functions will be maintained in real-time by the TIC. The web display will include information linking on orbit imagery requirements derived from FDF checklists as well as planned acquisition times per the Flight Plan. The system also allows users to access views of previously downlinked imagery and links to Orbiter models indicating areas already scanned.

## 77.5 OBSS OPERATIONAL NOTES

Each time the K1 relay (SPEE PWR sw on OBSS panel) is cycled, the RSC illuminator LEDs toggle from HIGH (all 156 LEDs), to MED (84 LEDs) to LOW (30 LEDs) to OFF (0 LEDs). The RSC illuminator initializes with all LEDs off. In addition to changing the amount of illumination, cycling the K1 relay also resets the Boom PTUs pan/tilt angles and takes LDRI to its Standby mode.

There is an auto shutdown feature with the LDRI so that it will shutdown when the sun or very high spectral reflection is in the FOV. The LDRI will attempt to return to the last commanded mode after 10 seconds. If viewing LDRI images at this time, the image will go to black.

When a Video Output pb and PL2 pb are selected on A7, the PTU/ITVC can be commanded since the ITVC is coded to accept commands addressed to PL2.

Since the LDRI is coded to accept commands addressed to MIDDECK, the LDRI can be commanded when a Video Output pb (the crew will be using MUX 1L) is selected in conjunction with the MIDDECK pb on A7. The 6 different LDRI modes are selected via the 6 exposure control pushbuttons at the bottom of A7. Note, the pb lights will not illuminate when a LDRI mode is selected except as described below.

If in modes 1 or 2 (ITVC modes of LDRI) and PL2 selected, the exposure control lights reflect the ITVC exposure control and not LDRI mode setting.

If in modes 3 through 6 (LDRI active modes) and PL2 selected, the exposure control lights reflect which LDRI mode is selected.

When in modes 3 through 6, gain can be adjusted with the IRIS switch if the LDRI MIDDECK command path is selected. The maximum gain allowed is T70 which corresponds to the brightest picture. The minimum and default gain is T280 which is the darkest and is suitable for most scenes. T280 corresponds to 32 pixels averaged every 8 frames at 90 IRE (light intensity reading where 100 IRE is white).

The LDRI gain adjustment, when made in one LDRI mode, is applied to the other 3 active LDRI modes (3, 4, 5, 6).

The LDRI gain is reset when taken to Mode 1.

The PTU pan angles range from  $-168.2^{\circ}$  to  $+168.2^{\circ}$ . The PTU tilt angles range from  $-130^{\circ}$  to  $+175^{\circ}$ . The negative tilt range is limited by the LDRI's EVA releasable cable (ISA1 cable W601).

To adjust pan/tilt, the PTU/ITVC command path must be selected by selecting a video output and PL2 on panel A7. It is possible to adjust pan/tilt angles when in an LDRI mode but when doing so, all ITVC commands can still be sent in the blind since LDRI and ITVC share the PL2 video output. To safeguard against ITVC damage, it is recommended to adjust pan/tilt when in an ITVC mode.

It is possible to command the LDRI in the blind if the LDRI command path is selected but PL2 is not selected to a monitor, since the command path is MIDDECK and the videopath is PL2.

It is possible to see a pulsing view when you initially go to modes 3 or 4 that will quickly dissipate, settling in about 5 seconds. This is the system's auto gain adjusting to the scene. Do not confuse this with modes 5 and 6.

**77.6 ELECTRICAL**

**Table 77-4. OBSS Electrical/Power Information**

| COMPONENT  | BUS  | WATTAGE   |
|--|--|---|
| Berthed Keep Alive power<br>(both LDRI & LCS)<br>Arm-Based Keep Alive (see 77.4.3.4) | MNA MPC1 &<br>MNB MPC2   | SP1- 73.8 W<br>SP2- 100.6 W   |
| LCH  | PRI PL   | 62.0 W*   |
| DCA  | PRI PL   | 48.9 W*   |
| +124V LCS*   | PRI PL<br>(APCU 1 enab via CABPL1)<br>(APCU 2 enab via AUXPLB) | LCS- 23.9 W*<br>LCS htrs- 66.0 W*<br>IDC- 10.2 W*<br>DCA htrs - 38.7 W* |
| LDRI   | MNA MPC1   | 100.8 W   |
| ITVC   | MNA MPC1   | 61.6 W  |
| PTU  | MNA MPC1   | 18.1 W  |
| RSC  | CABPL3   | 18 W  |
| RSC illuminators   | MNA MPC1   | 15 W  |

\* Note: these numbers are based on 126.5v, however, the highest voltage seen at the end of the boom is 113v.

## 77.7 CONTROLS

See Figures 77-14, 77-15, and 77-16

### A. Keep Alive Power - A8L

1. STARBOARD RMS HEATER AUTO A (S7) - turns MNA berthed keep alive power on
2. STARBOARD RMS HEATER AUTO B (S9) - turns MNB berthed keep alive power on
3. RMS SEL - PORT and RMS POWER - PRIMARY in order to allow +28V MNA power to flow to the K1 relay. This is performed during RMS PWRUP.

\*Note: The RELEASE/LATCH switch located above the S9 switch has been changed to a center off Lever Lock type switch to prevent inadvertent jettison. This is not reflected in Figure 77-14.

### B. OSVS Patch Panel (OPP) - R12

1. OBSS SW PWR cb1 (3A) pushed in - allows power to OBSS SW PWR switch
2. OBSS SW PWR sw ON - performed during PDRS On Orbit Init and turned off in D/O PREP. Allows power to flow to switches on the OBSS panel.
3. LCC PGSC connects to J107 LCS CMD/TLM for interfacing with the LCH.
4. J105 connects RSC video to the VPU WIB PL3 connector.

### C. OBSS Panel - R12

1. RSC PWR (S2) - provides power to the RSC as well as the RSC heaters. Note, the RSC illuminator heaters are not wired, however, the RSC heater has been deemed sufficient.
2. ITVC ENA (S3) - allows the OBSS ITVC to accept A7 commanding.
3. SPEE PWR (S4) - enables the K1 relay in the end effector which allows +28VMNA power to flow to the PTU/ITVC/LDRI. It also provides power to the RSC illuminator. This switch is turned on AFTER unberth and turned off BEFORE reberth.

### D. VPU - R12

1. Green jumper must be placed in the old MISS CAM port now named LDRI/ITVC (far right position) to assign LDRI/ITVC video to PL2.
2. PDIP video cable to connect J105 on the OPP (RSC VIDEO) to J603 (CCTV PL3) of the WIB to send the RSC video to PL3.



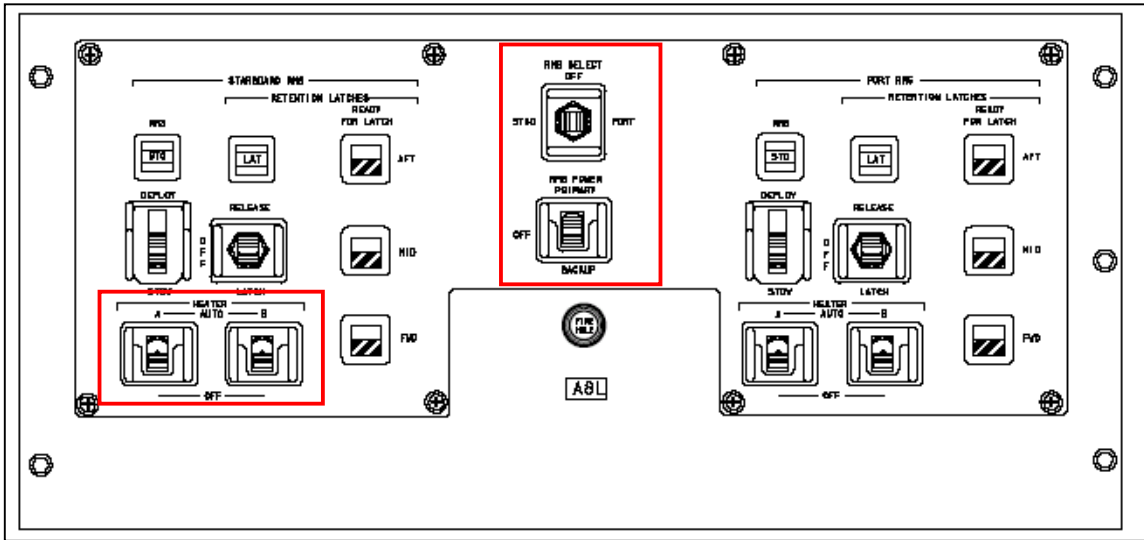


Figure 77-14. PNL A8L

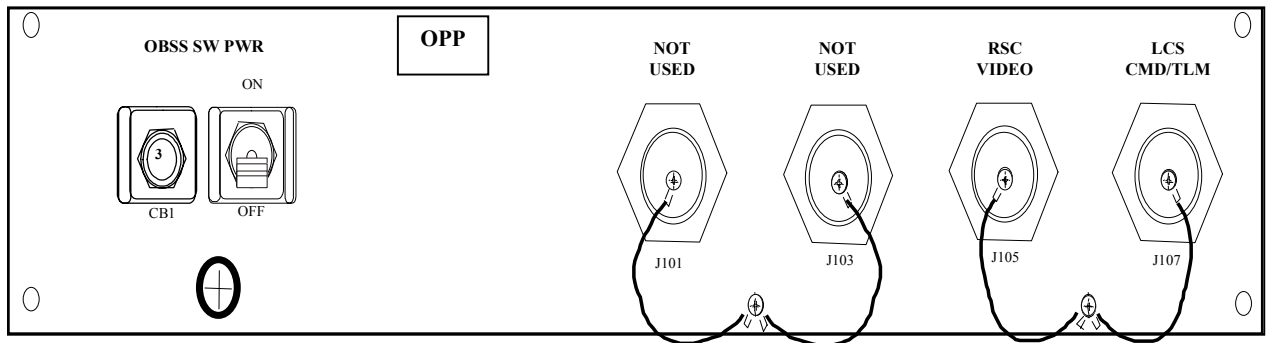
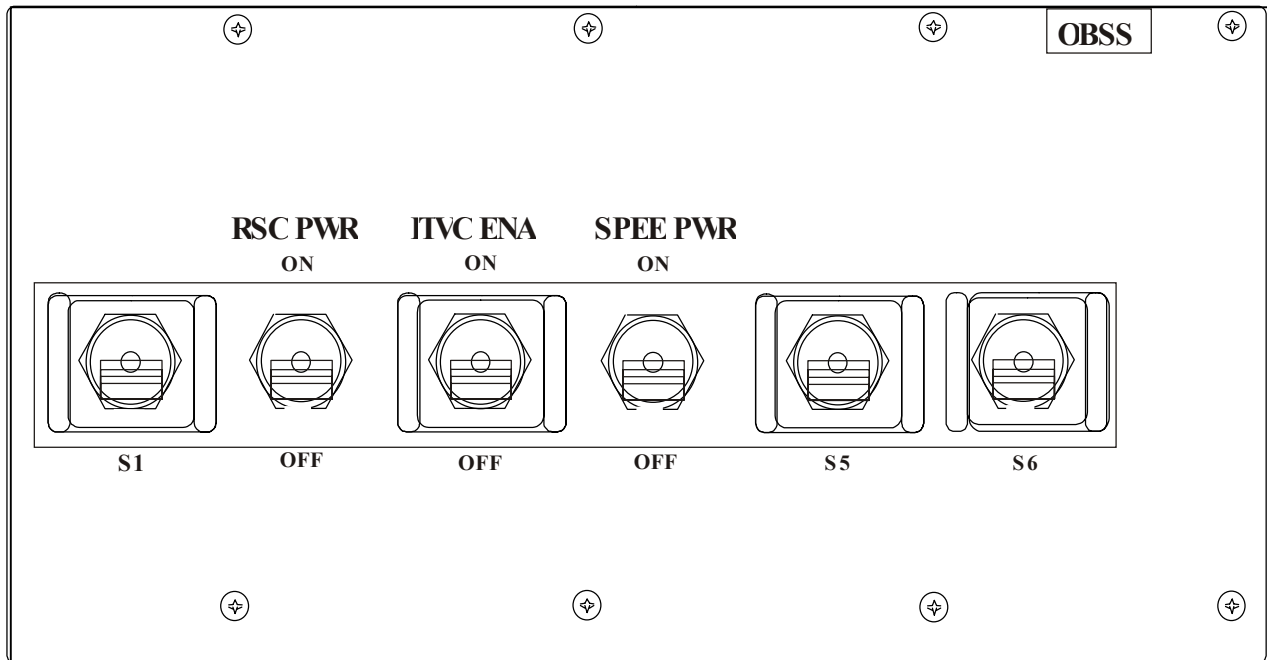


Figure 77-15. OBSS Patch Panel (OPP)



**Figure 77-16. OBSS Panel**

### 77.8 PHYSICAL CHARACTERISTICS

Manufacturer- Boom MDR  
                   LDRI Sandia Laboratories  
                   LCS Neptec  
                   RSC Videospection

Weight- Boom 410 lbs.

Both sensor packages have non-operational temperature ranges of -110° C to +50° C. See the Robotics section of the flight specific flight rules for the operating temperature limits of the sensors.

It is important to note that, in future flights, the boom may be left on the ISS without the sensor packages. The EFGF and FRGF have non-operational temperature ranges of -156° C to +121° C (±250° F). The FRGF operates within a temperature range of -76° C to +68° C (-105° F to +154° F) while the EFGF operates within -57° C to +88° C (-70° F to +190° F).

## 77.9 INSTALLATION

The following is a description of the OBSS location.

The OBSS is stowed in the starboard MPMs during ascent and entry. Keep alive power is applied when the boom is stowed during orbit to power heaters so as not to freeze the sensor packages.

## 77.10 TELEMETRY

A limited amount of Berthed Keep Alive telemetry is fed through the OBSS/MPM interface to the MCIU which in turn goes to the SM GPC via the Launch Data Bus. These temperatures share MSIDs (subcommutated) in the SM GPC:

- V54T2100J THERMISTOR\_DATA word 1
- V54T2110J THERMISTOR\_IDENT word 1
- V54T2120J THERMISTOR\_DATA word 2
- V54T2130J THERMISTOR\_IDENT word 2
- V54T2140J THERMISTOR\_DATA word 3
- V54T2150J THERMISTOR\_IDENT word 3
- V54T2160J THERMISTOR\_DATA word 4
- V54T2170J THERMISTOR\_IDENT word 4

The SM GPC has the ability to process 24 temperatures from the MCIU and RMS (not just OBSS temperatures). The MCIU ships those temperatures as a negative integer and the SM processes this information via table lookup. The parameters are then passed to the ground in the SM downlist.

Ground comps generate the following parameters:

- STBD\_LED\_WR\_TEMP for AV1
- STBD\_ABE\_WR\_TEMP for AV2
- STBD\_LED\_EP\_TEMP for PTU
- STBD\_LED\_SP\_TEMP for ITVC
- STBD\_LED\_SY\_TEMP for LDRI
- STBD\_LED\_WP\_TEMP for LCS



The LDRI iris parameter is inserted on video line 12 of the vertical interval (VI).

Pan and tilt telemetry is available for the ISIS PTU in video line 14 of the VI.

LDRI mode status is available as a 7 bit word from clock count 26 to clock count 40 in video line 16 of the VI.

LDRI temperature telemetry is available in clock counts 12 to 64 in video line 18 of the VI.

There also exist FDA limits in the SM GPC for the various sensor package temperatures which will annunciate an alarm.

## 77.11 REFERENCES

- A. Systems Requirements Document for the Orbiter Boom Sensor System, January 30, 2004. NSTS 60514
- B. Concept of Operations Document for the Orbiter Boom Sensor System, August 23, 2004. Rev. Basic. JSC 61605
- C. Project Technical Requirements Specification for the Integrated Sensor Inspection System, June 2004. Baseline, Change Package 1. JSC 49922
- D. System Design Review for the Orbiter Boom Sensor System. August 31-September 1, 2004.
- E. Integrated Sensor Inspection System (ISIS) Sensor Package 1 Critical Design Review. June 7-9, 2004.
- F. Orbiter Sensor System Laser Camera System Critical Design Review. August 10-12, 2004.
- G. Integrated Sensor Inspection System (ISIS) Electrical Power Consumption. Version 15. October, 2004.
- H. ISIS Digital Camera (IDC) System Requirements Review (SRR)
- I. ISIS Digital Camera (IDC) System Design Review (SDR)
- J. Integrated Inspection Sensor System (ISIS) Electrical Power Consumption. JSC 62726A.
- K. Program Requirements Document for the Shuttle On-Orbit Thermal Protection System (TPS) Inspection System. NSTS 60517.

**SECTION 78 - ENHANCED LAUNCH VEHICLE IMAGING SYSTEM**

**CONTENTS**

| <b>Section</b> |   | <b>Page</b> |
|----------------|---|-------------|
| 78.1           | GENERAL DESCRIPTION.....  | 78-1        |
| 78.1.1         | Interfaces .....  | 78-3        |
| 78.2           | CAMERAS .....   | 78-5        |
| 78.2.1         | ET LO2 Feedline Faring Camera System (TIR11) .....                | 78-5        |
| 78.2.2         | Orbiter Umbilical Well Still Camera (ET TPS Camera, ORU13).....   | 78-9        |
| 78.2.3         | SRB Forward Skirt ET Observation Camera (SRF11, SLF11).....       | 78-18       |
| 78.2.4         | SRB ETA-Ring Camera System (SRA11, SLA11) .....                   | 78-20       |
| 78.2.5         | SRB Forward Skirt Aft-Pointing Camera System (SRF21, SLF21) ..... | 78-22       |
| 78.2.6         | Crew Handheld Still Camera (OCM12) .....                          | 78-26       |
| 78.3           | ELECTRICAL .....  | 78-27       |
| 78.4           | TELEMETRY.....  | 78-27       |
| 78.5           | REFERENCES.....   | 78-28       |

## FIGURES

| Figure |  | Page  |
|--------|--|-------|
| 78-1   | ELVIS Cameras Overview - Part A .....                          | 78-2  |
| 78-2   | ELVIS Cameras Overview - Part B .....                          | 78-3  |
| 78-3   | ELVIS End to End Interfaces.....                               | 78-4  |
| 78-4   | Approximate Camera Imaging Times.....                          | 78-5  |
| 78-5   | ET LO2 Feedline Fairing Camera Simulated View.....             | 78-6  |
| 78-6   | Camera Installed in Feedline Fairing.....                      | 78-6  |
| 78-7   | ET LO2 Feedline Fairing Camera Real-Time Video Path.....       | 78-8  |
| 78-8   | ET LO2 Feedline Fairing Camera Recorded Video Path.....        | 78-9  |
| 78-9   | ET TPS Camera System Overview.....                             | 78-10 |
| 78-10  | ET TPS Camera System/Timing Diagram.....                       | 78-12 |
| 78-11  | ET TPS Camera State Transition Diagram .....                   | 78-13 |
| 78-12  | IVA IEEE 1394 Converter Box .....                              | 78-14 |
| 78-13  | ET TPS Camera Cable Routing .....                              | 78-15 |
| 78-14  | Kodak DCS 760 in ET TPS Assembly.....                          | 78-16 |
| 78-15  | ET Umbilical Well Image from STS-114 .....                     | 78-17 |
| 78-16  | Updated A13 Panel.....   | 78-18 |
| 78-17  | SRB Right Hand Fwd Skirt ET Obs Camera Typical View .....      | 78-19 |
| 78-18  | SRB Left Hand Fwd Skirt ET Obs Camera Typical View.....        | 78-19 |
| 78-19  | Right Hand SRB ETA-Ring Camera Typical View.....               | 78-20 |
| 78-20  | Left Hand SRB ETA-Ring Camera Typical View .....               | 78-21 |
| 78-21  | Solid State Video Recorder .....                               | 78-22 |
| 78-22  | Right Hand SRB Fwd Skirt Aft-Pointing Camera Typical View..... | 78-23 |
| 78-23  | Left Hand SRB Fwd Skirt Aft-Pointing Camera Typical View ..... | 78-23 |
| 78-24  | SSVR Mounted on the SRB Forward Skirt.....                     | 78-24 |
| 78-25  | Aft-Pointing Camera on the Forward Skirt.....                  | 78-24 |
| 78-26  | Aft-Pointing Camera in Forward Skirt Housing.....              | 78-25 |
| 78-27  | SRB Cameras .....  | 78-25 |
| 78-28  | Crew Handheld Camera Typical FOV (from STS-114) .....          | 78-26 |
| 78-29  | Kodak DCS 760 with 400mm lens.....                             | 78-27 |



## SECTION 78 ENHANCED LAUNCH VEHICLE IMAGING SYSTEM

### 78.1 GENERAL DESCRIPTION

The Enhanced Launch Vehicle Imaging System (ELVIS) is an imaging system used for observing general vehicle condition, monitoring specific component performance, and debris tracking during launch and ascent. ELVIS' primary objective is to provide imagery data Image Analysis Integration (IAI) for engineering evaluation of vehicle ascent performance and Thermal Protection System (TPS) integrity for use in determining current mission contingency requirements for on-orbit inspections or repairs.

ELVIS consists of multiple cameras mounted on the Space Shuttle Vehicle to obtain supplemental imagery to aid ground camera views. ELVIS includes cameras mounted on the Orbiter, Solid Rocket Booster (SRB), and External Tank (ET).

ELVIS consists of the following nine cameras:

|       |   |
|-------|---|
| TIR11 | ET Liquid Oxygen (LO <sub>2</sub> ) feedline fairing camera |
| SRF11 | Right Hand SRB Forward Skirt ET observation camera          |
| SLF11 | Left hand SRB Forward Skirt ET observation camera           |
| SRA11 | Right hand SRB ETA-Ring camera                              |
| SLA11 | Left hand SRB ETA-Ring camera                               |
| SRF21 | Right hand SRB Forward skirt aft-pointing camera            |
| SLF21 | Left hand SRB Forward skirt aft-pointing camera             |
| ORU13 | Orbiter umbilical well still camera (aka ET TPS camera)     |
| OCM12 | Crew handheld still camera                                  |

Figure 78-1 shows an overview of the locations of TIR11, SRF11, and SLF11. Figure 78-2 also shows the locations of SRF11 and SLF11 in addition to SRA11, SLA11, SRF21, SLF21, and ORU13.

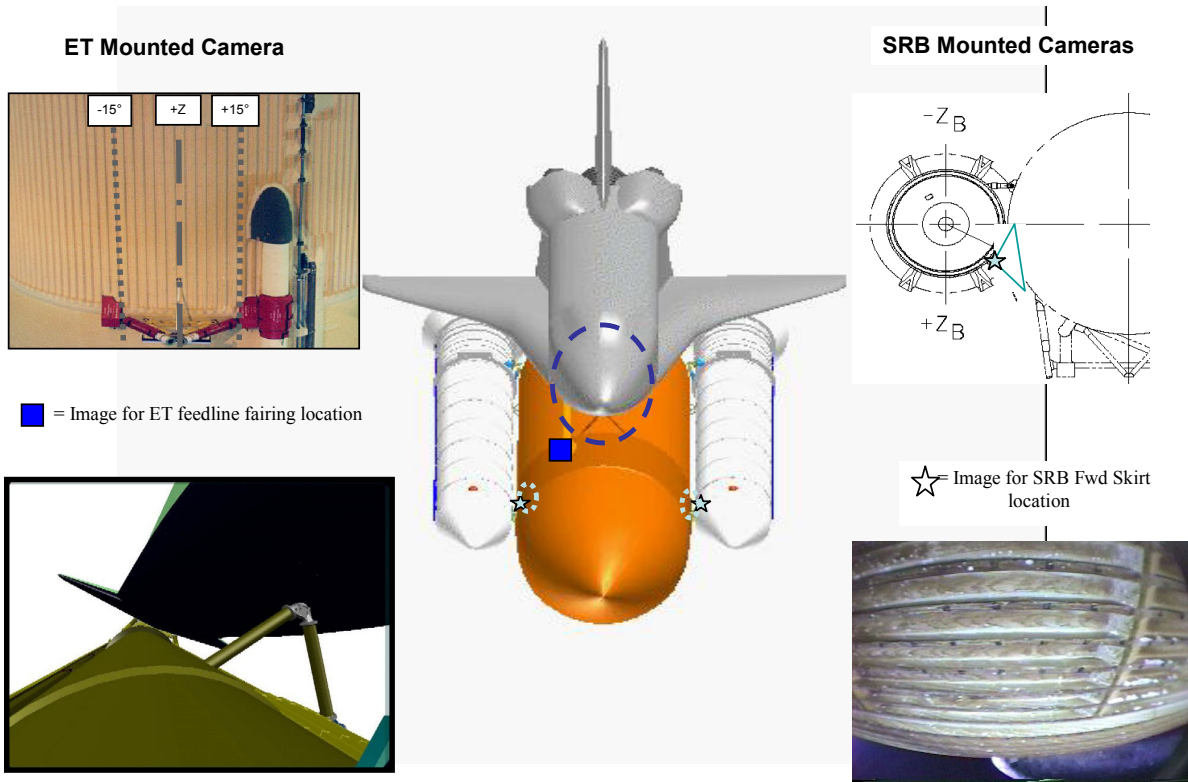
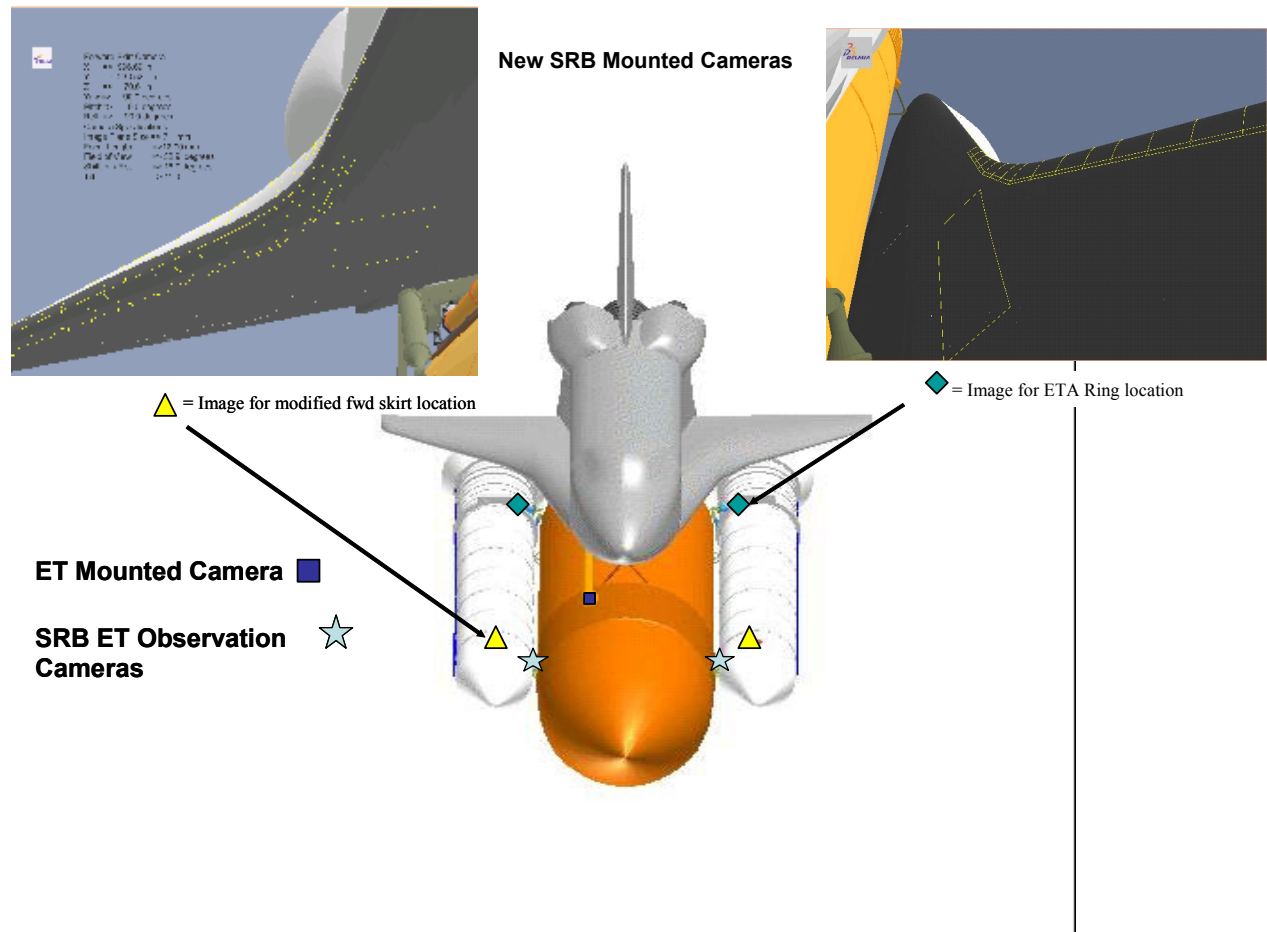


Figure 78-1. ELVIS Cameras Overview - Part A

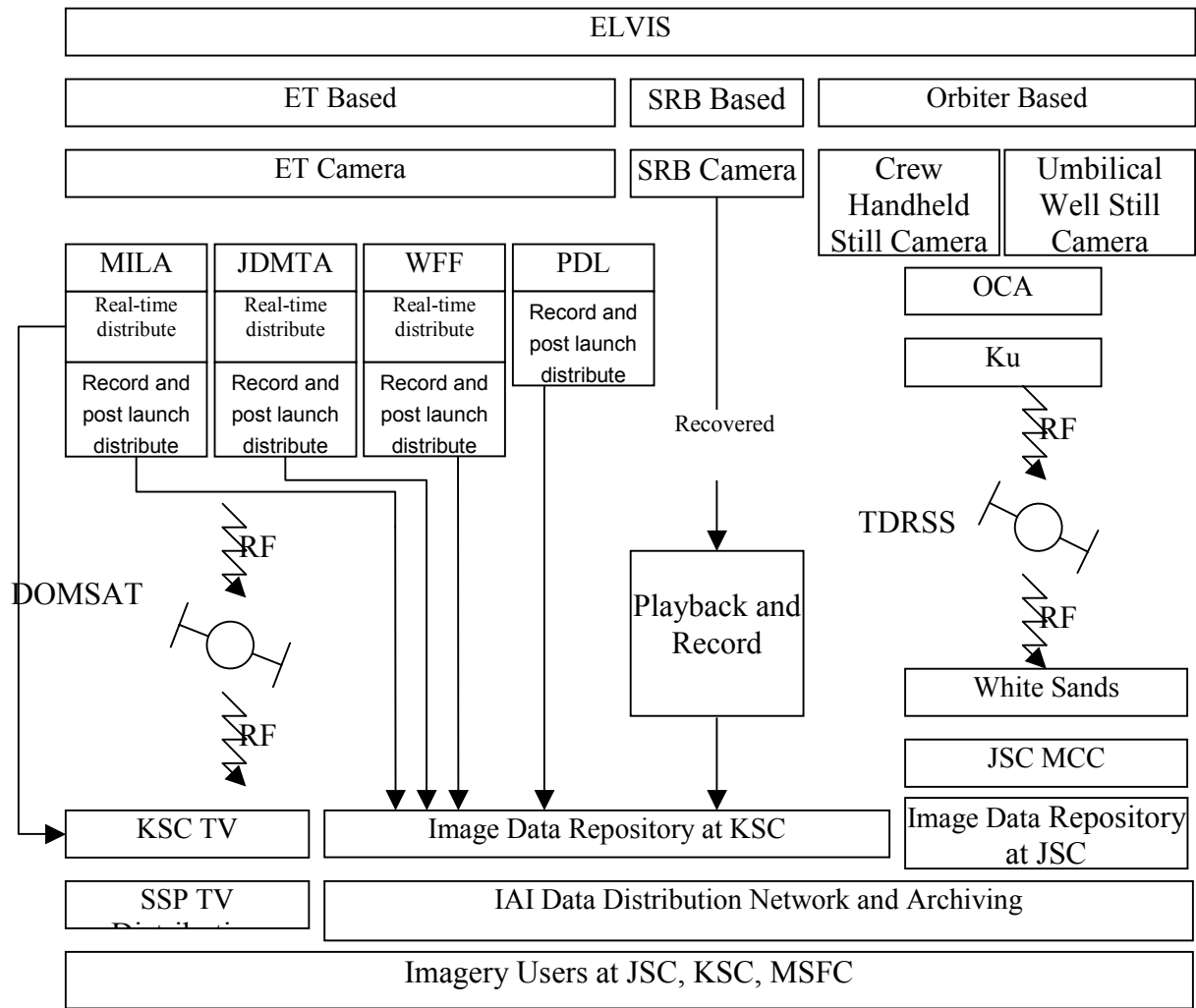


**Figure 78-2. ELVIS Cameras Overview - Part B**

### 78.1.1 Interfaces

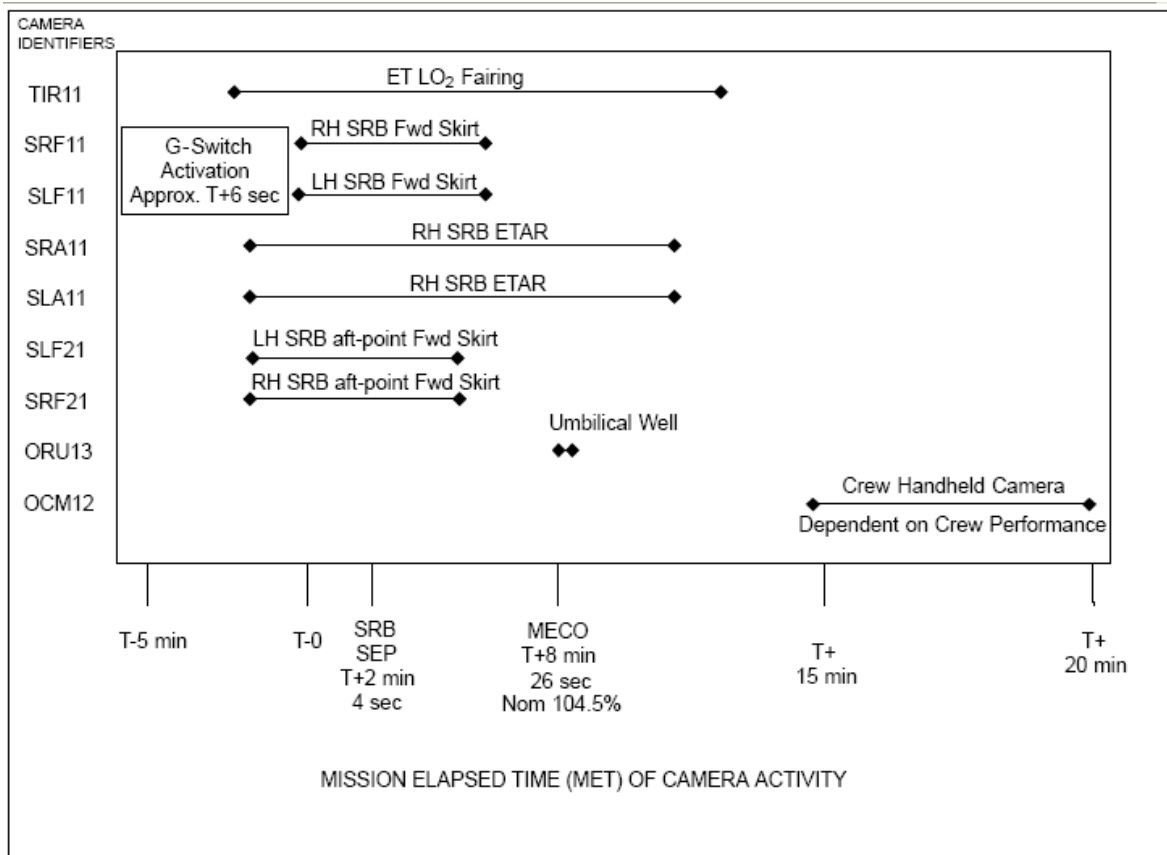
INCO has very limited interaction with ELVIS. INCO has two commands that can be sent to the ET TPS camera and the images are then downlinked via Orbiter Communications Adapter (OCA). The ET LO<sub>2</sub> Feedline Camera transmits on a 2272.5Mhz FM carrier to ground sites along the ascent path. These ground sites retransmit the images to KSC for IAI evaluation. The IAI network at KSC then broadcasts the post-launch signals to the JSC, KSC, and MSFC IAI image analysis laboratories. Lastly, the crew handheld camera's images are downlinked via OCA and its video is sent to Ku TV. This is the extent of INCO's responsibility with the cameras.

All SRB cameras are recorded onboard the SRBs and recovered later. Figure 78-3 shows a summary of the end-to-end ELVIS image transmission for all nine cameras while Figure 78-4 shows an overview of the approximate imaging times of each camera.



| LEGEND |  |       |   |        |                                      |      |                              |
|--------|--|-------|---|--------|--------------------------------------|------|------------------------------|
| ELVIS  | Enhanced launch Vehicle Imaging System | OCA   | Orbiter Communication Adapter             | Ku     | Ku-Band                              | MSFC | Marshall Space Flight Center |
| SRB    | Solid Rocket Booster                   | MILA  | Merritt Island Launch Area                | DOMSAT | Domestic Satellite                   |      |                              |
| ET     | External Tank                          | PDL   | Ponce Deleon                              | TDRSS  | Tracking data relay Satellite System |      |                              |
| GSFC   | Goddard Space Flight Center            | JDMTA | Jonathon Dickinson Missile Tracking Annex | KSC    | Kennedy Space Center                 |      |                              |
| RF     | Radio Frequency                        | WFF   | Wallops Flight Facility                   | JSC    | Johnson Space Center                 |      |                              |

Figure 78-3. ELVIS End to End Interfaces

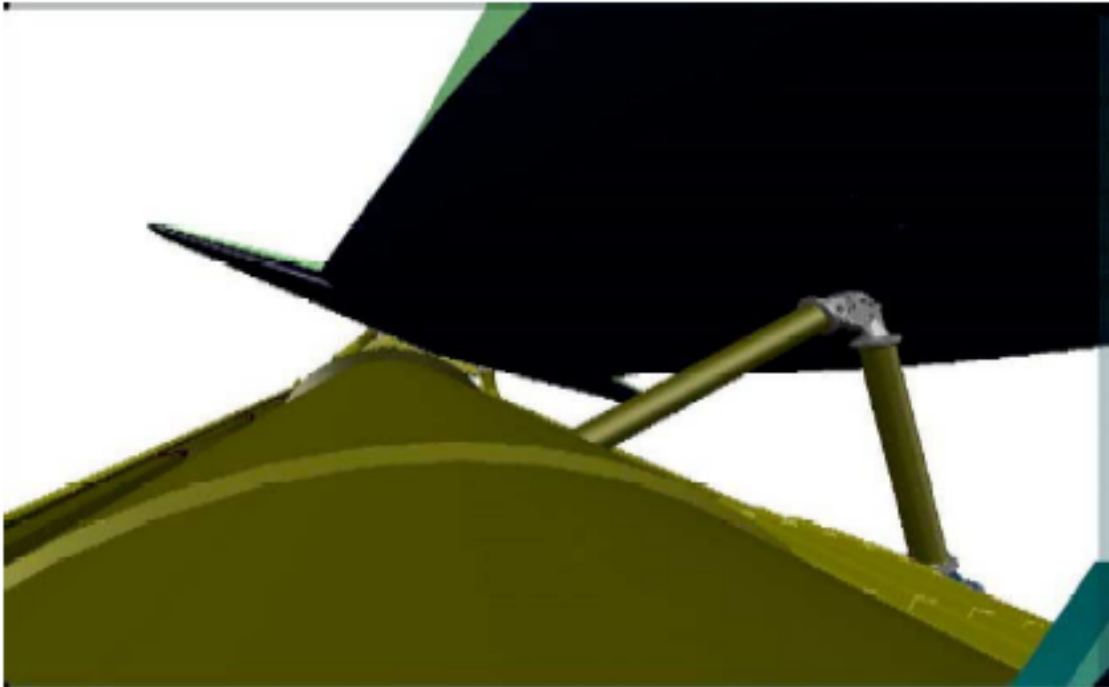


**Figure 78-4. Approximate Camera Imaging Times**

## 78.2 CAMERAS

### 78.2.1 ET LO<sub>2</sub> Feedline Faring Camera System (TIR11)

The ET LO<sub>2</sub> feedline fairing camera is a Sony XC-999 which is powered and controlled automatically from the electronics package mounted on a support beam located between the LO<sub>2</sub> and LH<sub>2</sub> tanks ( $X_t = 1034$ ,  $Y_t = +/-218$ ,  $Z_t = 470$  with antennas at  $X_t = 903 +/-47.5^\circ$  from the -Z of the tank). The camera's FOV includes the bipod assembly region, Orbiter left and right wing (except as obstructed by the bipod strut), Orbiter -Z TPS beginning 12 inches forward of the bipod fitting and continuing aft. Figure 78-5 shows a simulated view of the ET LO<sub>2</sub> camera. The camera captures images at the National Television System Committee (NTSC) frame rate of 30 frames per second (fps) and can see debris/divots that are 2.0 x 2.0 inches or larger at a distance of under 20 feet. Figure 78-6 shows the actual camera installed.



*Figure 78-5. ET LO2 Feedline Fairing Camera Simulated View*



*Figure 78-6. Camera Installed in Feedline Fairing*

### **78.2.1.1 ET LO<sub>2</sub> Feedline Fairing Camera Ground Operations**

The ET LO<sub>2</sub> feedline fairing camera is signal strength and functionality checked using Ground Support Equipment (GSE) activation and hat couplers on the ET antennas while still in the Vehicle Assembly Building (VAB). End to end checkout is done at the Pad with the MILA facility while the Rotating Service Structure (RSS) is positioned to allow an RF path to MILA. A launch processing system (LPS) ground command is used to turn the system on and off during the testing.

### **78.2.1.2 ET LO<sub>2</sub> Feedline Fairing Camera System Interfaces**

The ET LO<sub>2</sub> feedline fairing camera is powered by a battery with a 60 minute life. A full battery charge supports at least three Launch Countdown (LCD) scrubs and recycles before requiring recharge.

The camera system is activated using an LPS ground command initiated at approximately T-2 minutes and 30 seconds. This command is initiated by the Ground Launch Sequencer (GLS) automatically and is routed via the LPS to the ET. In the event of a scrub, the camera system deactivation is accomplished as soon as possible per the S0007, LCD Operations and Maintenance Instructions (OMI), scrub/safing turnaround section.

The camera system provides the capability to RF downlink the ET camera video signal to ground stations from RF activation until G-switch timer activation at MET 15 minutes, which effectively turns off the transmitter (a G-switch is a mechanical device that senses acceleration in order to close its contacts). However, the most critical portion of image gathering is prior to SRB separation, for debris transport analysis purposes, while imagery after SRB separation is only "highly desirable."

The video signal is frequency modulated on a 2272.5 MHz carrier and downlinked to ground stations. Goddard Space Flight Center (GSFC) network distributes the signal to the local station demarcation point at Merritt Island Launch Area (MILA), Jonathan Dickinson Missile Tracking Annex (JDMTA) and Wallops (WLP) for delivery to KSC-TV in real-time. The signal is then distributed to the other centers. Figure 78-7 provides a summary of the real-time distribution feedline fairing camera imagery. Note that Wallops also has the ability to transmit video files over the internet as well.

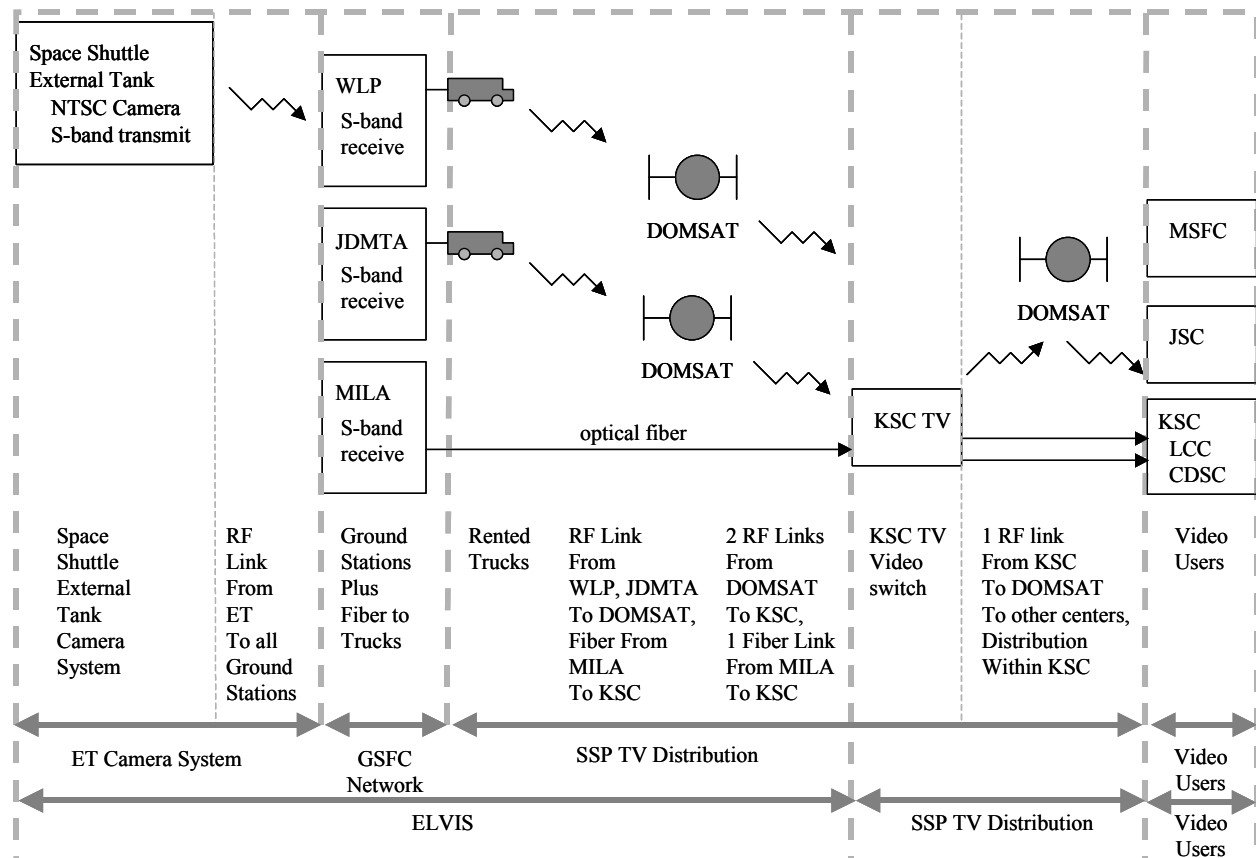
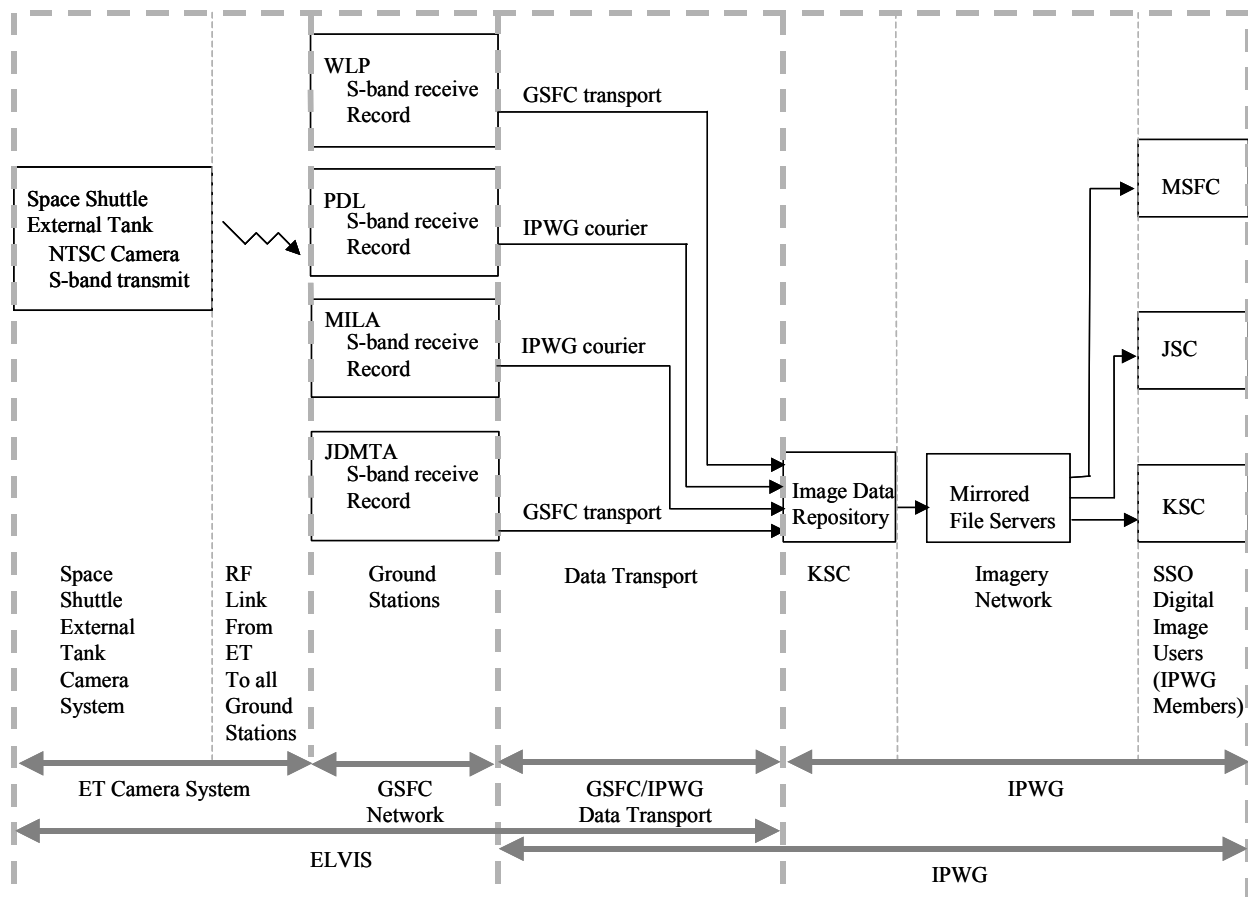


Figure 78-7. ET LO2 Feedline Fairing Camera Real-Time Video Path



The original video signal is also digitally recorded in Wavelet format at all the receiving ground stations. The GSFC network then distributes the digitally recorded camera signal to the IAW network at KSC within 24 hours of launch. Figure 78-8 provides a summary of the recorded, post launch image distribution.



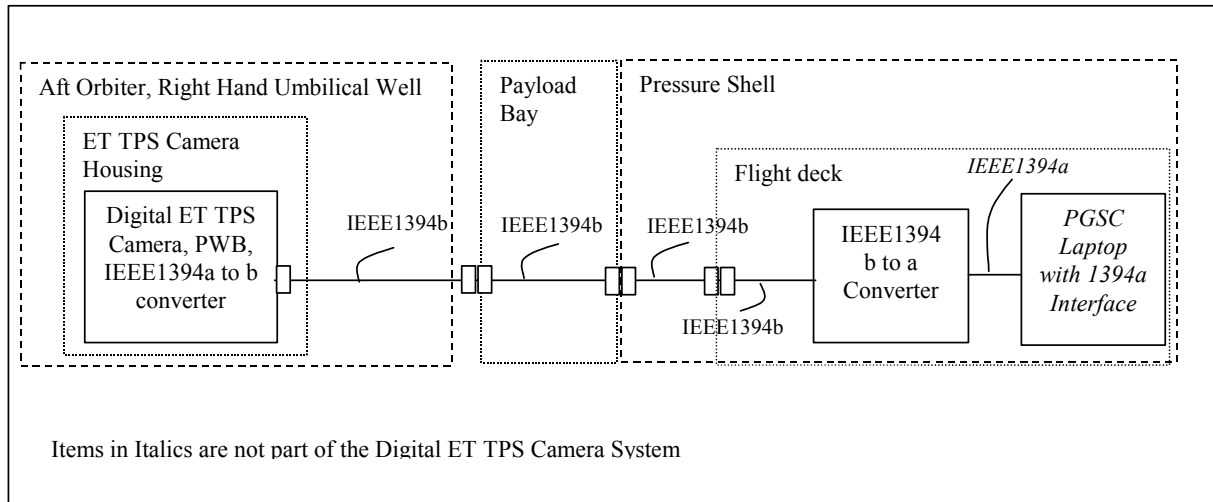
**Figure 78-8. ET LO2 Feedline Fairing Camera Recorded Video Path**

### 78.2.2 Orbiter Umbilical Well Still Camera (ET TPS Camera, ORU13)

The ET TPS Camera is a commercial off the shelf (COTS), intra-vehicular activity (IVA) certified, Kodak DCS 760 Digital Camera with a 35mm lens. The camera is installed in the starboard umbilical well at  $X_o = +1347$ ,  $Y_o = +96$ ,  $Z_o = +260$  while in the VAB. In addition, the camera is set in the following configuration: drive mode is set to “CS”, focus mode to “M”, shutter speed set to “1/250”, aperture set to “6.3”, with the lens lock to it smallest aperture and focus set to infinity.

### 78.2.2.1 ET TPS Camera System Interfaces

There are several interfaces in the ET TPS camera system as shown in Figure 78-9. These include Camera firewire 1394a to firewire 1394b (in Printed Wiring Board (PWB)), firewire 1394b to 1394a converter, firewire 1394a to the laptop computer, and 28V MNA power to the camera assembly. Lastly, the camera system interfaces with an IBM A31P Laptop for OCA downlink.



**Figure 78-9. ET TPS Camera System Overview**

### 78.2.2.2 ET TPS Camera System Operations Overview

An orbiter flight software command initiates camera photography roughly at ET separation. Images are stored on an internal camera flash memory card. After post insertion, the crew sets up an IBM A31P laptop, transfers the images to the laptop, and downlinks the images via OCA.

#### 78.2.2.2.1 ET TPS Camera System Commanding

Three ET TPS control signals exist: CAMERA POWER and CAMERA HEATER/POWER, both routed via FA MDMs, and ET/ORB SEP CAMERAS ON which is generated in the camera control board. Figure 78-10 demonstrates the timing analysis in order for the ET TPS camera to start its imaging sequence.

The command sequence is as follows: the LPS commands CAMERA HEATER/POWER ON at T-8 hours 10 minutes per the OMI which can be verified at <http://kscgrndtsk1.ksc.nasa.gov/OMIDSearch/OMIDSearch.htm>. The GNC commands CAMERA POWER ON three times: prelaunch, at SRB separation, and again at ET separation. If CAMERA POWER ON stay “high” for more than 16 seconds, then ET/ORB SEP CAMERAS ON is sent from the camera controller and the camera starts

snapping pictures at 1.5 second intervals for 45 seconds during which the crew executes a +X maneuver so that a complete view of the ET may be collected at very close range (approximately 100 feet). The GNC then commands CAMERA HEATER/POWER OFF after the Main Propulsion System (MPS) dump, which is about 2 minutes after ET separation.

In OPS 201, INCO sends a real time command (RTC), DSM 5300 UMB WELL STILL CMR ON (V56K0010U) , through MDM FA1 to repower the camera for image retrieval. Likewise, INCO uplinks a second ET TPS command, DSM 5301 UMB WELL STIL CMR OFF (V56K0011U), also via MDM FA1.

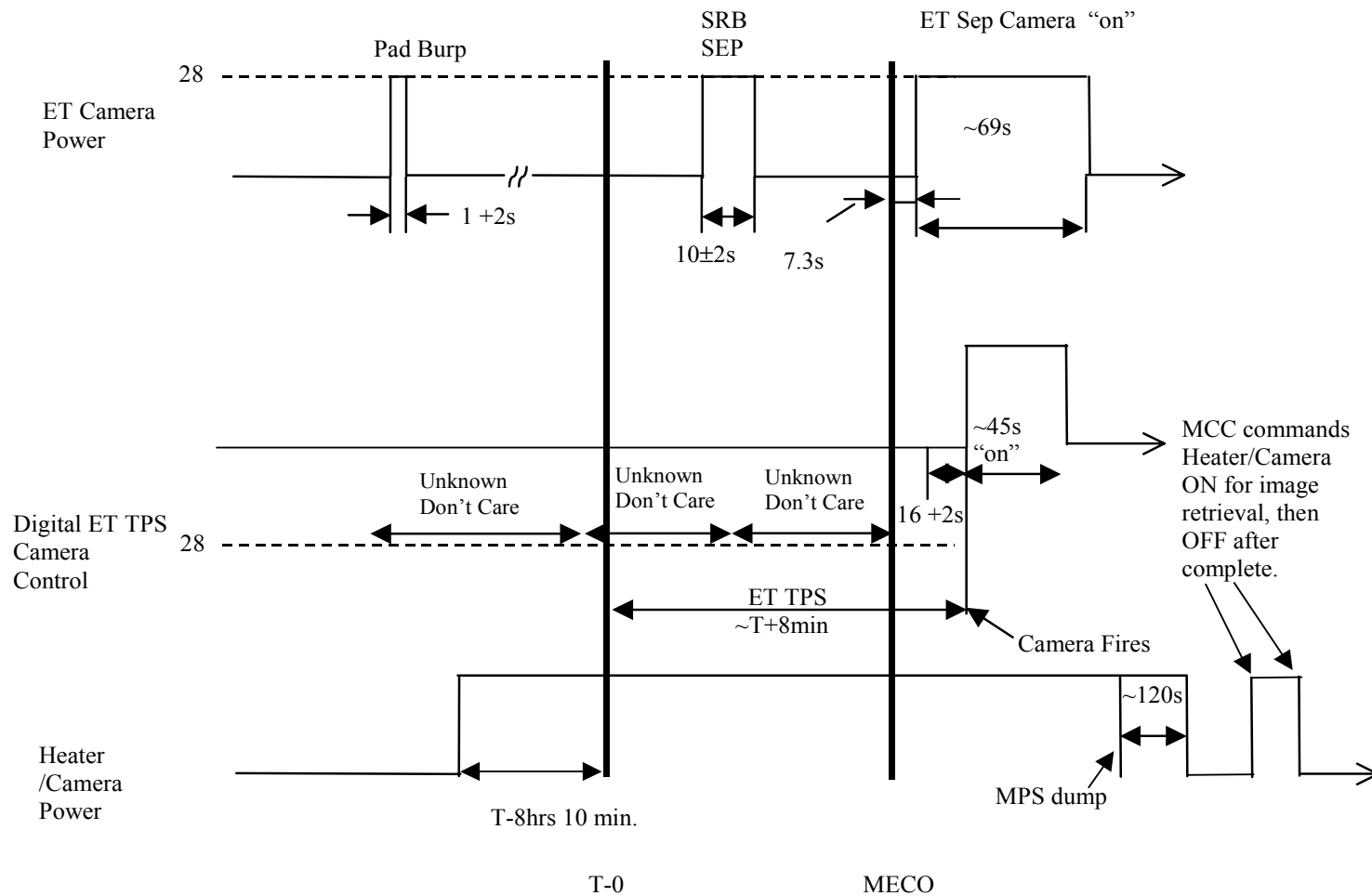


Figure 78-10. ET TPS Camera System/Timing Diagram

See Figure 78-11 for a command state transition diagram for the ET TPS camera.

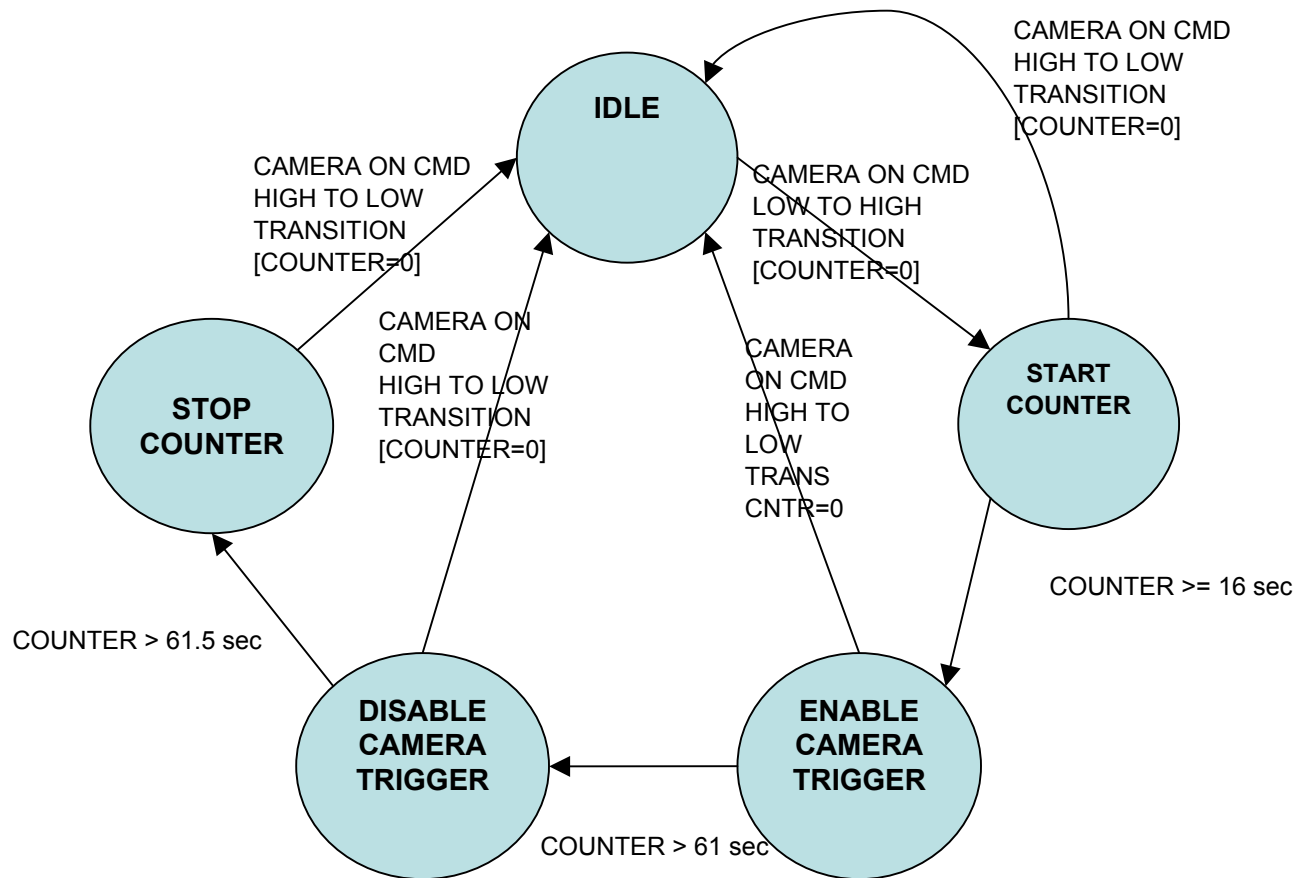


Figure 78-11. ET TPS Camera State Transition Diagram

### 78.2.2.3 ET TPS Camera System Hardware

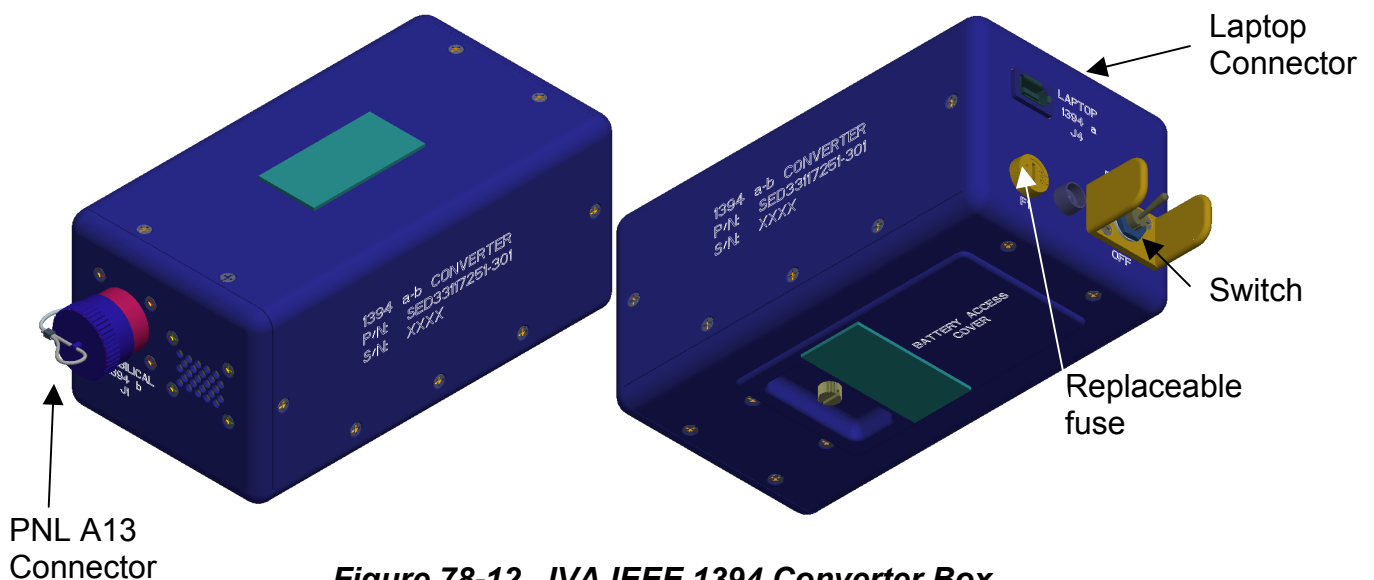
The main components of the ET TPS system are: IEEE 1394 converter box, heater assembly, timing/logic control board, power board voltage converter, and the Kodak DCS 760.

#### 78.2.2.3.1 IEEE 1394 Converter Box

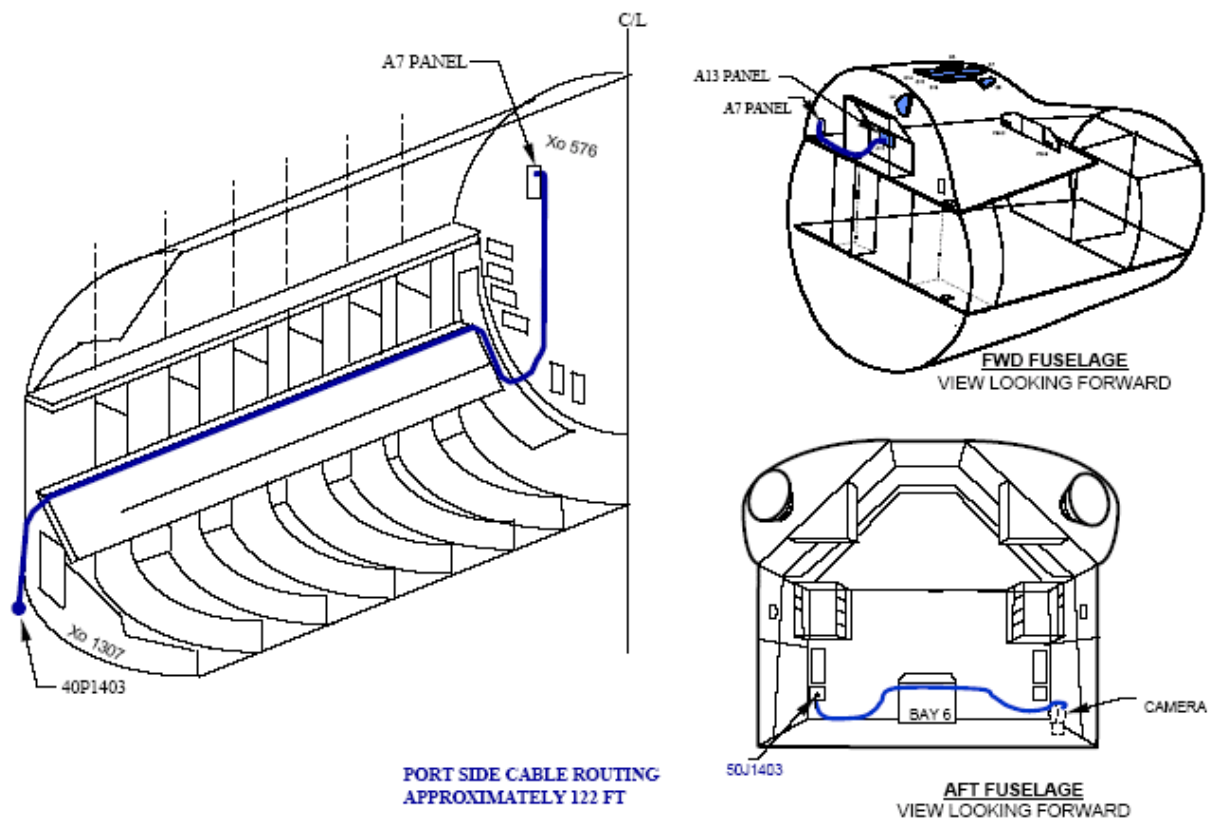
There are two IEEE converter cards onboard the Orbiter, one in the camera assembly to convert the camera signal from 1394a to 1394b and a second IVA converter housed in its own box in the crew cabin to convert from 1394b back to 1394a.

There are multiple reasons to convert to 1394b. The first reason is that 1394a is only good for about a 20' run. The total amount of cabling from camera to laptop is roughly 130'. A second reason is that 1394a is DC coupled which can lead to EMI problems, lightning hazards and electrostatic discharge (ESD). 1394b can be AC coupled to eliminate these issues.

The IVA converter board is nearly identical to the one in the camera assembly except it has a different physical layout to fit in its different housing and the 1394a connector is modified to a standard 6 pin connector to allow it to interface with the laptop via a COTS cable. In addition, the IVA board receives power from 4 AA batteries where it is converted to +3.3Vdc and +1.8Vdc, while the camera assembly board receives its +3.3Vdc and +1.8Vdc power from the Orbiter. The AA batteries have expected life of greater than 4 hours and are replaceable on orbit. Lastly, the IVA box has an on/off switch, an LED indicator, and a replaceable 2A fuse. The IVA converter box can be seen in Figure 78-12. Note the port for connecting the laptop in the picture on the left and note the switch, LED, and battery compartment in the picture on the right.



**Figure 78-12. IVA IEEE 1394 Converter Box**



**Figure 78-13. ET TPS Camera Cable Routing**

Figure 78-13 reiterates the length of the cable run as well as shows the detail of the routing from the camera to the crew cabin. Note that there exists extra cabling in the bundle which can be used as a replacement cable in the event of a prelaunch failure or to support an additional camera.

#### 78.2.2.3.2 ET TPS Heater Assembly

A total of four heaters occupy the ET TPS camera assembly, two in the electronic heater assembly, and two in the camera heater assembly. They are each 12.6W and are actively controlled between 54°F and 95°F.

The DCS 760 has an operating range between 0°F and 140°F (-19°C to 60°C) while the electronics box including the IEEE 1394 board operates from -40°F to 230°F (-40°C to 110°C). These limits are well within the expected launch, orbit, and entry environments.

Note that the heaters are turned off at the same time as the camera after ET sep. The camera will reach a steady state temperature of -65°F within 24 hours. It takes about two hours to warm the camera from -65°F to its operating temperature of 0°F. It must be at operating temperature prior to image retrieval from the A31P laptop. This is why INCO turns the camera on as soon as possible after Ops 201.

### 78.2.2.3.3 ET TPS Timing/Controller

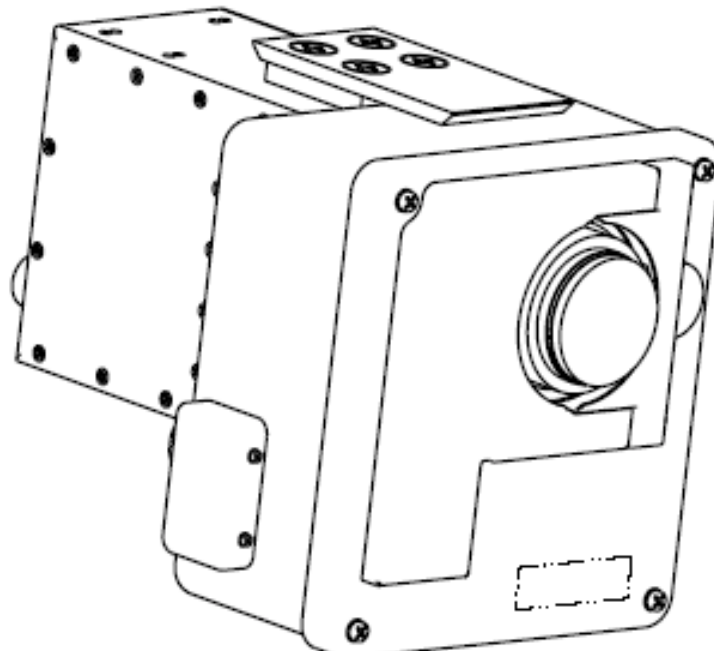
The digital ET TPS timing/controller board has multiple purposes. It takes in +28Vdc Orbiter power and provides the camera assembly isolation from that 28V discrete signal. In addition, it converts the 28V discrete to a +3.3V signal which then interfaces with the power board voltage converter. It also decodes the incoming control signal and most importantly, provides shutter release control once every 1.5 seconds for a total duration of 45 seconds.

### 78.2.2.3.4 ET TPS Power Board Voltage Converter

The ET TPS power board voltage converter provides all on board circuit protection for the ET TPS camera assembly. Through a series of fuses, DC-DC conversion, and voltage regulation, it provides the following: +28V to the electronics heaters and camera heaters, +3.3V and +1.8V to the IEEE 1394 converter, and +7.2V to both the digital camera and the control board.

### 78.2.2.3.5 Kodak DCS 760

The ET TPS camera is a COTS Kodak DCS 760 with a 35mm lens. The camera is set in the following configuration: drive mode is set to "CS" or continuous silent, focus mode to "M" or manual, shutter speed set to "1/250", aperture set to "6.3", with the lens lock to it smallest aperture and focus set to infinity.



*Figure 78-14. Kodak DCS 760 in ET TPS Assembly*



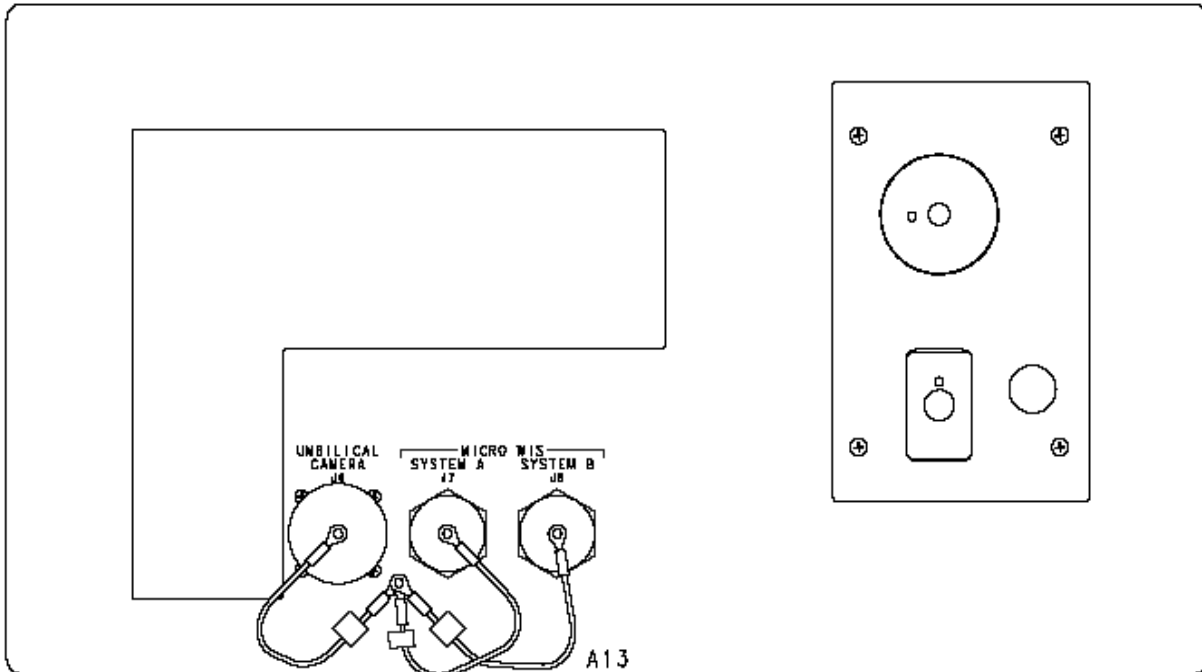


S114E5072

***Figure 78-15. ET Umbilical Well Image from STS-114***

Figure 78-14 shows the Kodak DCS 760 and Figure 78-15 is an umbilical well camera image from STS-114. The first shot is frame #5 and the second is frame #28 from a series of shots.

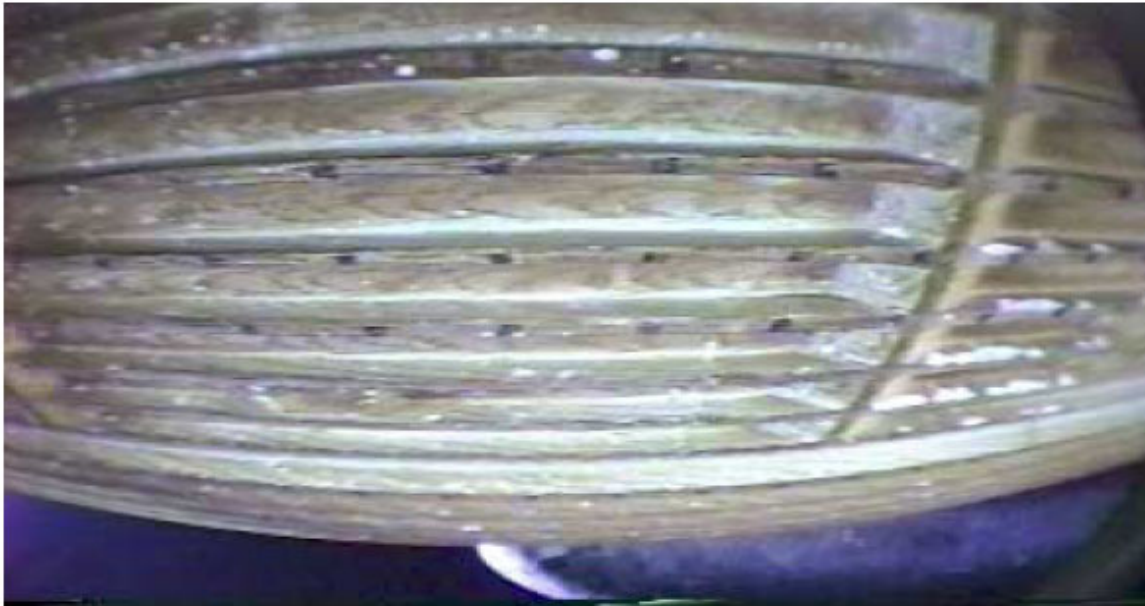
Figure 78-16 shows the new panel A13 where the A31P interfaces with the ET TPS camera system.



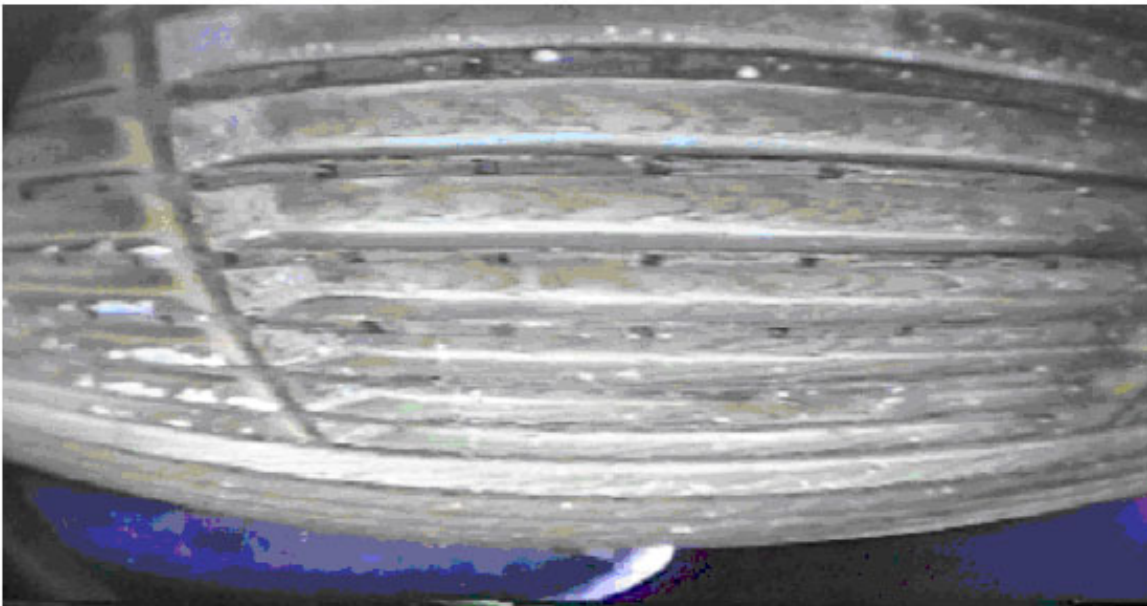
**Figure 78-16. Updated A13 Panel**

### 78.2.3 SRB Forward Skirt ET Observation Camera (SRF11, SLF11)

Each SRB forward skirt ET observation camera ( $X_t = 997$ ,  $Y_t = +/-187$ ,  $Z_t = 435$ ) is a self contained, self isolated system. There is no MCC insight or control of these cameras. These cameras provide the image analysis team with a FOV of the inter-tank region thrust panel from the left and right side SRBs. The typical fields of view are seen in Figures 78-17 and 78-18.



**Figure 78-17. SRB Right Hand Fwd Skirt ET Obs Camera Typical View**



**Figure 78-18. SRB Left Hand Fwd Skirt ET Obs Camera Typical View**

The cameras capture images at the National Television System Committee (NTSC) frame rate of 30 frames per second (fps) and can see debris/divots that are 0.1 inches or larger in diameter at a distance of 2 feet +/-6 inches.

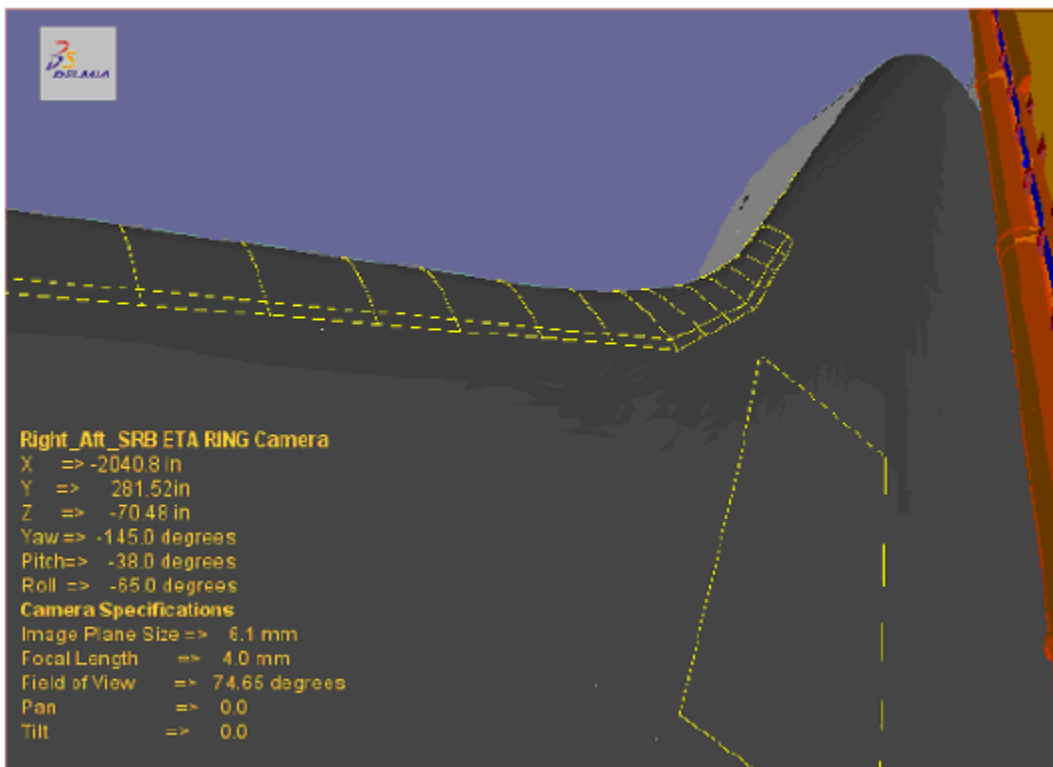
There is no prelaunch pad interface; the Splashdown Data Acquisition System (DAS), located in the SRB forward skirt dome canister, contains batteries and a video recorder.

Post SRB retrieval, images are downloaded from the DAS and the images are made available to IAI.

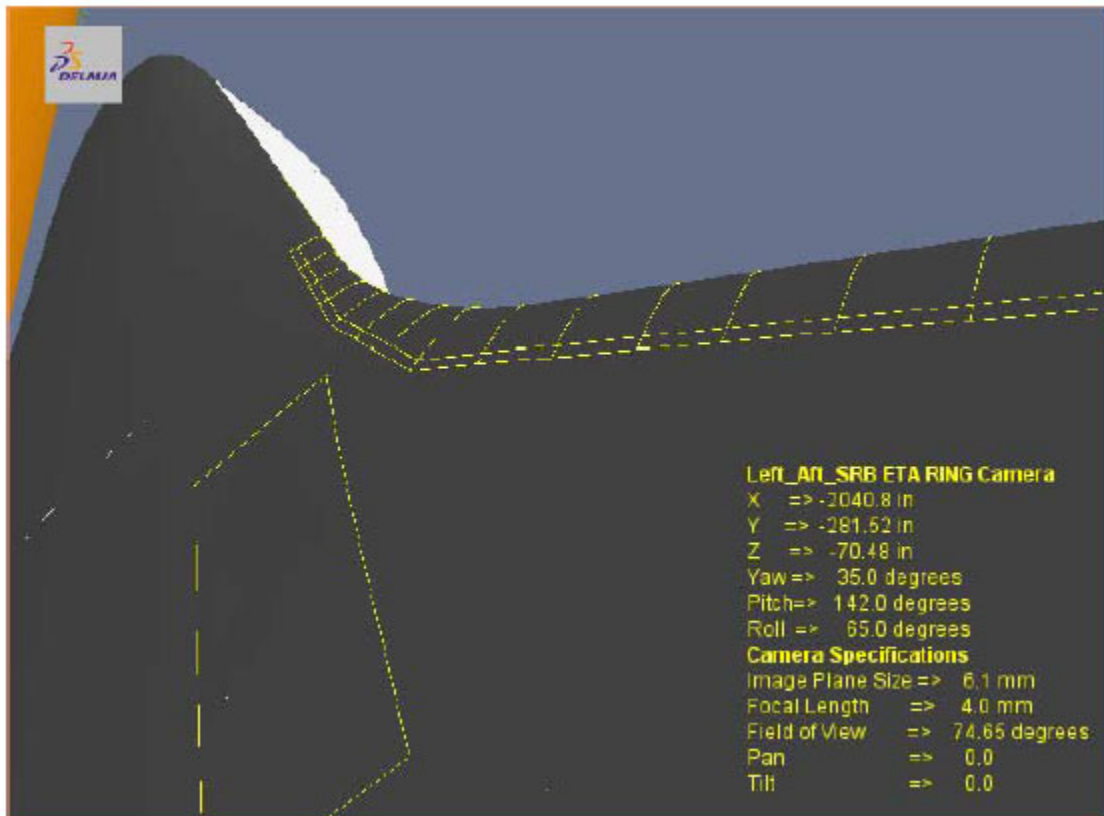
The system is turned on using a G-switch, which actuates at lift-off. The recording system is operational at about T+15 seconds and will image the ET thrust panel area until about T+300 seconds (past SRB separation) when the DAS recorder switches to record main parachute deployment images.

#### 78.2.4 SRB ETA-Ring Camera System (SRA11, SLA11)

The SRB ETA-Ring cameras ( $X_t = 2046$ ,  $Y_t = +/-218$ ,  $Z_t = 470$ ) together with their Solid State Video Recorders (SSVRs) make up the SRB ETA-Ring camera system. The cameras provide a view of the underside forward portion of the Orbiter, including the nose, a portion of the main landing gear door, and wing leading edge RCC panels 1 through 12. Figures 78-19 and 78-20 demonstrate the expected fields of view.



**Figure 78-19. Right Hand SRB ETA-Ring Camera Typical View**

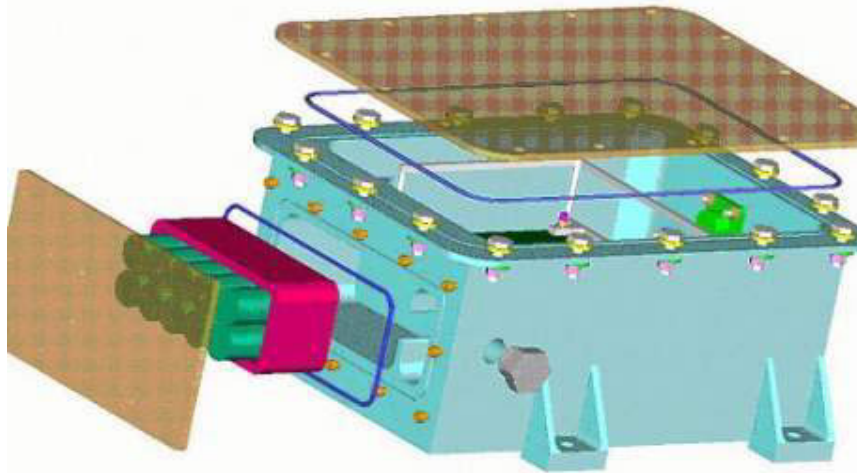


**Figure 78-20. Left Hand SRB ETA-Ring Camera Typical View**

The cameras are able to detect debris/divots of 1.2 inches x 1.2 inches at a distance of 15.0 feet and capture images at the National Television System Committee (NTSC) frame rate of 30 frames per second (fps).

The ETA Ring cameras are activated via LPS/GLS command at T-1:57 and provide imaging from system activation to after SRB separation. Imaging ceases at activation +13 minutes where it self powers down. The SRBs are then recovered and the images are retrieved from the SSVR and made available to IAI. The SSVR can be seen in Figure 78-21.





**Figure 78-21. Solid State Video Recorder**

### **78.2.5 SRB Forward Skirt Aft-Pointing Camera System (SRF21, SLF21)**

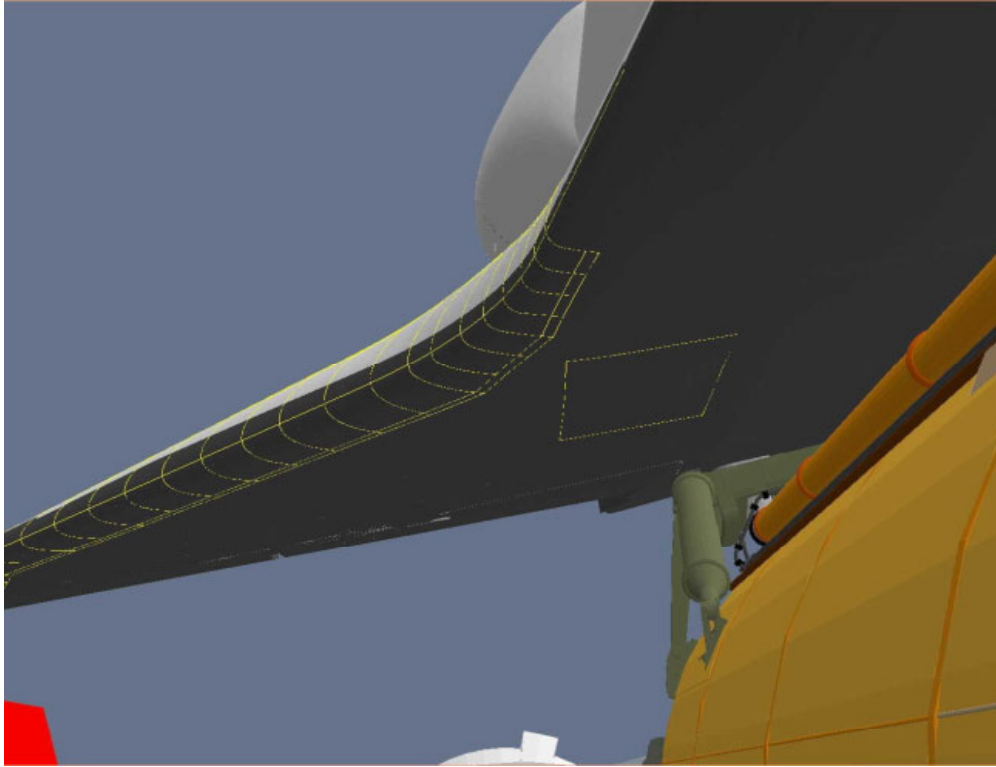
The SRB forward skirt aft-pointing cameras ( $X_t = 978$ ,  $Y_t = +/-235$ ,  $Z_t = 473$ ) are mounted to the SRB forward skirt inside a fairing. Together with the same type SSVRs the ET-Ring cameras use, these cameras provide IAI with images of the right and left wings' leading edge. Note: each camera has its own SSVR. Figures 78-22 and 78-23 illustrate a simulated FOV from these cameras.

As was the case with the ET-Ring cameras, SRF21 and SLF21 are able to detect debris/divots of 1.2 inches x 1.2 inches at a distance of 15.0 feet and capture images at the National Television System Committee (NTSC) frame rate of 30 frames per second (fps).

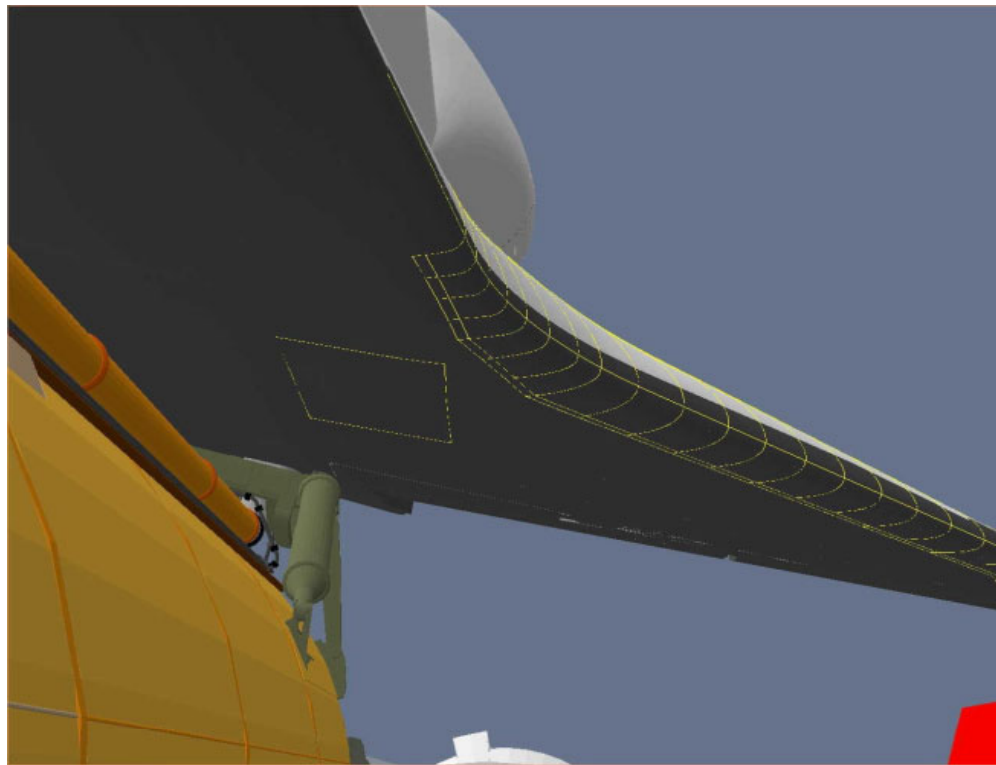
The SRB forward skirt aft-pointing cameras are, like the ET-Ring cameras, activated via LPS/GLS command at T-1:57, and provide imaging from system activation to after SRB separation. Imaging ceases at activation +13 minutes where it self powers down. The SRBs are then recovered and the images are retrieved from the SSVR and made available to IAI. The SSVR can be seen in Figure 78-21 and its mounting location can be seen in Figure 78-24. Note that for a cut-off/abort, the GLS issues camera off commands for the ETA Ring cameras and SRB Forward Skirt Aft-Pointing Cameras approximately 1 minute after safing is initiated.

Figures 78-25 and 78-26 demonstrate the mounting of the SRB forward skirt aft-pointing cameras.

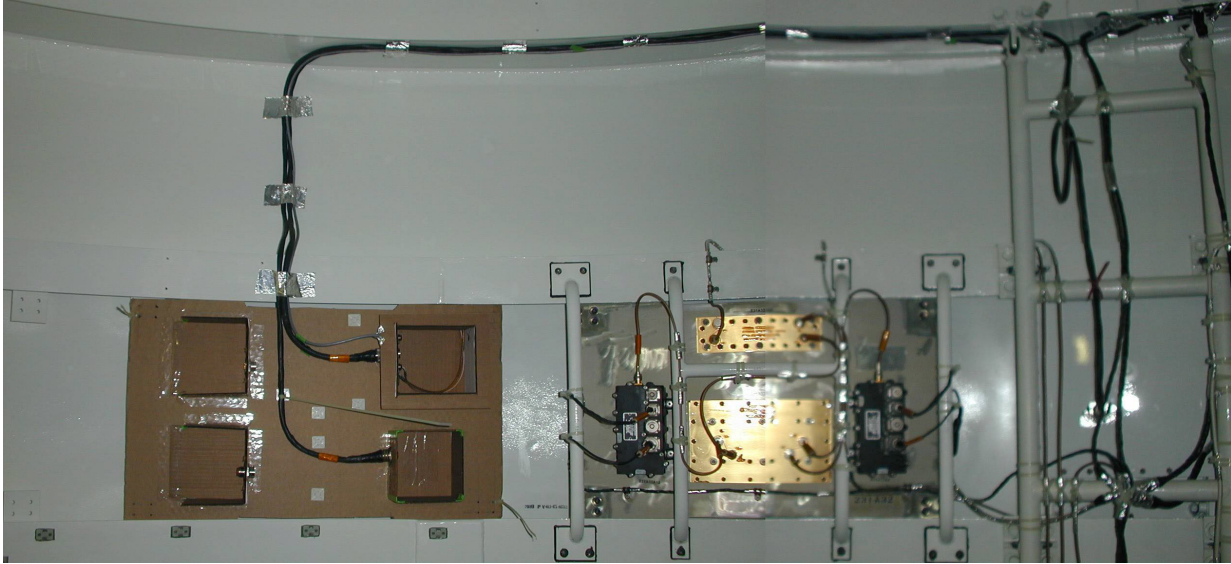
Lastly, Figure 78-27 shows a summary of the locations of the SRB cameras.



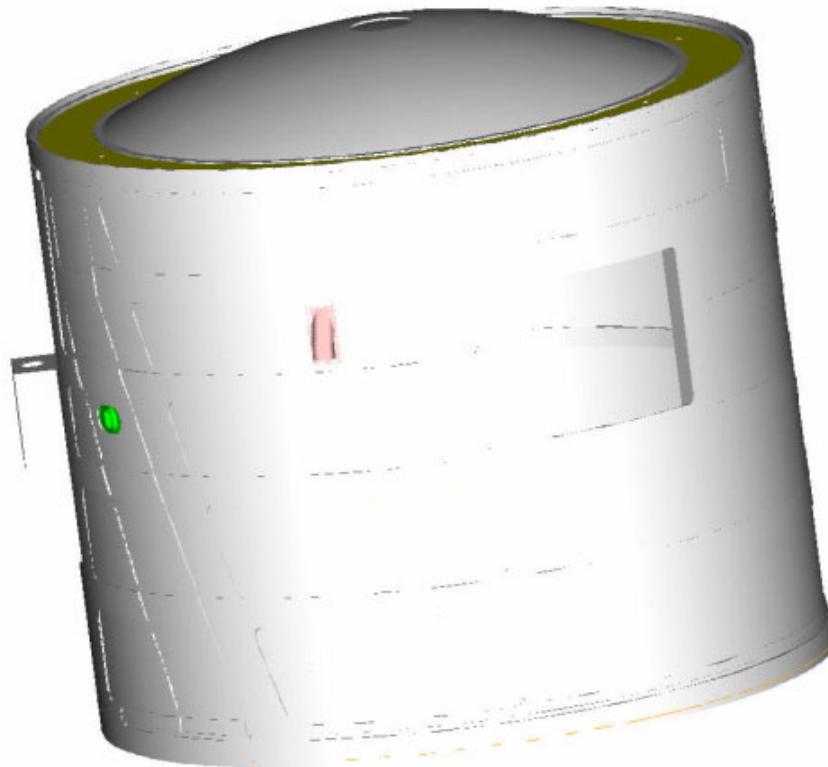
**Figure 78-22. Right Hand SRB Fwd Skirt Aft-Pointing Camera Typical View**



**Figure 78-23. Left Hand SRB Fwd Skirt Aft-Pointing Camera Typical View**

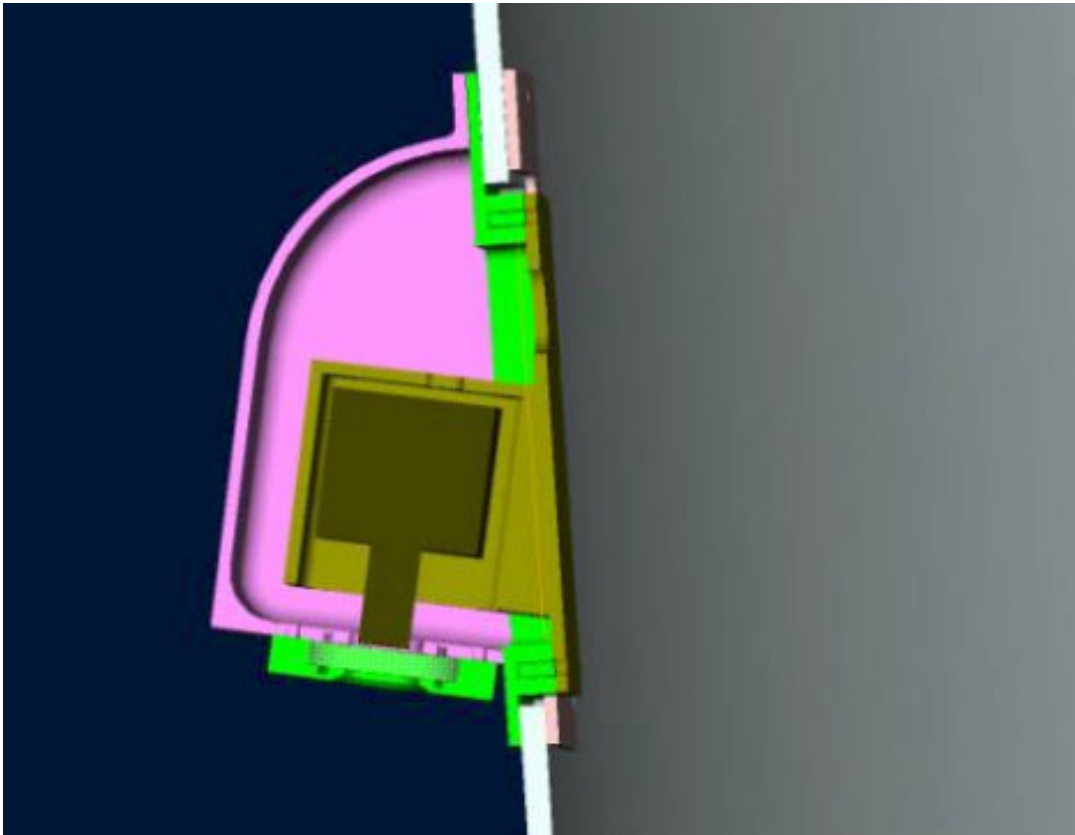


**Figure 78-24. SSVR Mounted on the SRB Forward Skirt**

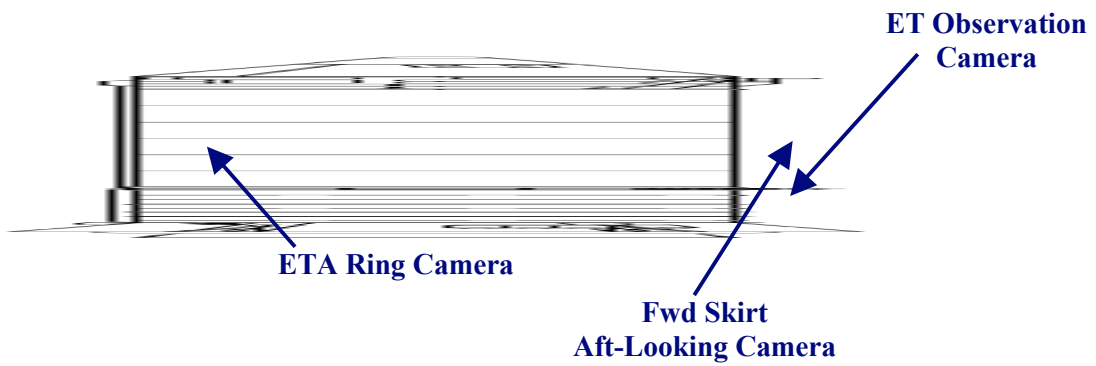


**Figure 78-25. Aft-Pointing Camera on the Forward Skirt**





*Figure 78-26. Aft-Pointing Camera in Forward Skirt Housing*



*Figure 78-27. SRB Cameras*

### 78.2.6 Crew Handheld Still Camera (OCM12)

The crew handheld still camera is a Kodak DCS 760 with 400mm lens used to image the ET through the crew module overhead windows to obtain the following images: the Orbiter facing (+Z) side of the ET, ET nose, left and right limbs of the ET (-Y and +Y ET limbs), views of the ET aft dome, and the far (-Z) side of the ET. It is a 400mm lens camera and is part of the standard photo/TV stowage allocation. Figure 78-28 shows an image from the crew handheld camera from STS-114.



S114E5009

**Figure 78-28. Crew Handheld Camera Typical FOV (from STS-114)**

The camera has the capability to capture one image every 5 seconds and can detect debris/divots 7.0 inches in diameter or larger at distances less than 5000 feet.

Images are taken from lift-off plus 14 minutes through lift-off plus 20 minutes. Those images are stored on a removable flash storage memory card which can be downlinked via OCA for distribution to IAI.

The images are further processed by the Electronic Still Camera (ESC) console operator who grabs the images off the ESC file server (which received them from the OCA server) and places them into a directory used by the Image Science & Analysis Group (IS&AG) Mission Evaluation Room (MER) team.

The crew's Kodak DCS 760 with 400mm lens can be seen in Figure 78-29.



*Figure 78-29. Kodak DCS 760 with 400mm lens*

### 78.3 ELECTRICAL

The ET TPS camera receives +28V discretes from MNA APC1 and MNC ALC3. The Camera Heater power source (MNA APC1) is enabled by activating the K7 relay with a MNA ALC1 power discrete via an MDM FA1 command as discussed previously.

In addition, a 5A RPC is enabled by a MNC ALC3 power discrete via MDM FA3 enabling MNA APC1 power to get to the ET TPS camera assembly.

It is estimated that during picture taking, the ET TPS camera assembly consumes 84W of power. During non picture taking modes, with heaters, it consumes about 42W and without heaters, about 14W.

Total power consumption of the aft IEEE 1394 converter board is practically negligible at 0.56W. Note that the crew cabin IEEE 1394 converter board is battery powered.

All other ELVIS camera systems do not receive Orbiter power.

### 78.4 TELEMETRY

ELVIS has no telemetry other than real-time video from the ET LO<sub>2</sub> feedline fairing camera.

## 78.5 REFERENCES

- A. Digital ET TPS Camera Delta System Design Review.
- B. Enhanced Launch Vehicle Imaging System Concept of Operations. October 2004 Baseline.
- C. Orbiter Umbilical Well Digital ET TPS Camera System Design Review.
- D. Systems Requirements Document For The Enhanced Launch Vehicle Imaging System. NSTS 37389. August 20, 2004
- E. Enhanced Launch Vehicle Imaging System System Design Review (SDR). February 17-20, 2004.

**SECTION 81 - SOLID ROCKET BOOSTER/EXTERNAL TANK  
RANGE SAFETY SYSTEM**

**CONTENTS**

| <b>Section</b> |  | <b>Page</b> |
|----------------|--|-------------|
| 81.1           | GENERAL .....                                  | 81-1        |
| 81.1.1         | Range Safety Profile .....                     | 81-1        |
| 81.1.2         | Space Shuttle Range Safety Profile .....       | 81-1        |
| 81.2           | SHUTTLE RANGE SAFETY SYSTEM CONFIGURATION..... | 81-7        |
| 81.2.1         | SRB RSS Description .....                      | 81-7        |
| 81.2.2         | ET RSS Description .....                       | 81-7        |
| 81.3           | RSS COMMAND MESSAGE FORMAT .....               | 81-7        |
| 81.4           | TELEMETRY.....                                 | 81-7        |
| 81.4.1         | Decoder ON/Checktone OFF.....                  | 81-8        |
| 81.4.2         | Receiver Signal Strength .....                 | 81-8        |
| 81.5           | POWER.....                                     | 81-8        |
| 81.6           | RSS HARDWARE LOCATIONS .....                   | 81-8        |
| 81.6.1         | SRB RSS Hardware Locations.....                | 81-8        |
| 81.6.2         | ET RSS Hardware Locations .....                | 81-9        |
| 81.7           | RSS CONTROL AND OPERATIONS .....               | 81-9        |
| 81.8           | OPERATIONAL NOTES .....                        | 81-9        |
| 81.9           | REFERENCES.....                                | 81-10       |

**TABLES**

| <b>Table</b> |                                  |       |
|--------------|----------------------------------|-------|
| 81-1         | SRB/ET range safety system ..... | 81-10 |

**FIGURES**

| <b>Figure</b> |   |      |
|---------------|---|------|
| 81-1          | Impact limit lines and destruct lines (for illustration purposes only)..... | 81-2 |
| 81-2          | Head-on (-X) view showing range safety command<br>antenna placements.....   | 81-4 |
| 81-3          | ET/SRB range safety systems schematic .....                                 | 81-5 |

THIS PAGE INTENTIONALLY BLANK

## SECTION 81 SOLID ROCKET BOOSTER/EXTERNAL TANK RANGE SAFETY SYSTEM

### 81.1 GENERAL

#### 81.1.1 Range Safety Profile

Launch vehicles convert vast amounts of chemical potential energy into equally vast amounts of kinetic energy to accelerate their payloads to Earth-orbital velocity. Despite the best of all planning, design, and tests, the hazards and risk of a malfunction causing a launch vehicle to lose directional control and allowing escape from its planned trajectory must be considered. Range Safety's function (Figure 81-1) is to terminate flights that are far enough out of normal bounds to endanger populated areas. In order to protect populated areas, impact limit lines are drawn around them. No lethal piece of a launch vehicle can land behind an impact limit line. Since termination would have to occur well before an impact line is reached, vehicle destruct lines are drawn inside the boundaries of the impact lines. A vehicle passing outside the boundaries of the destruct line would be subject to termination. Flight termination is accomplished by remotely detonating explosive charges aboard the errant vehicle.

#### 81.1.2 Space Shuttle Range Safety Profile

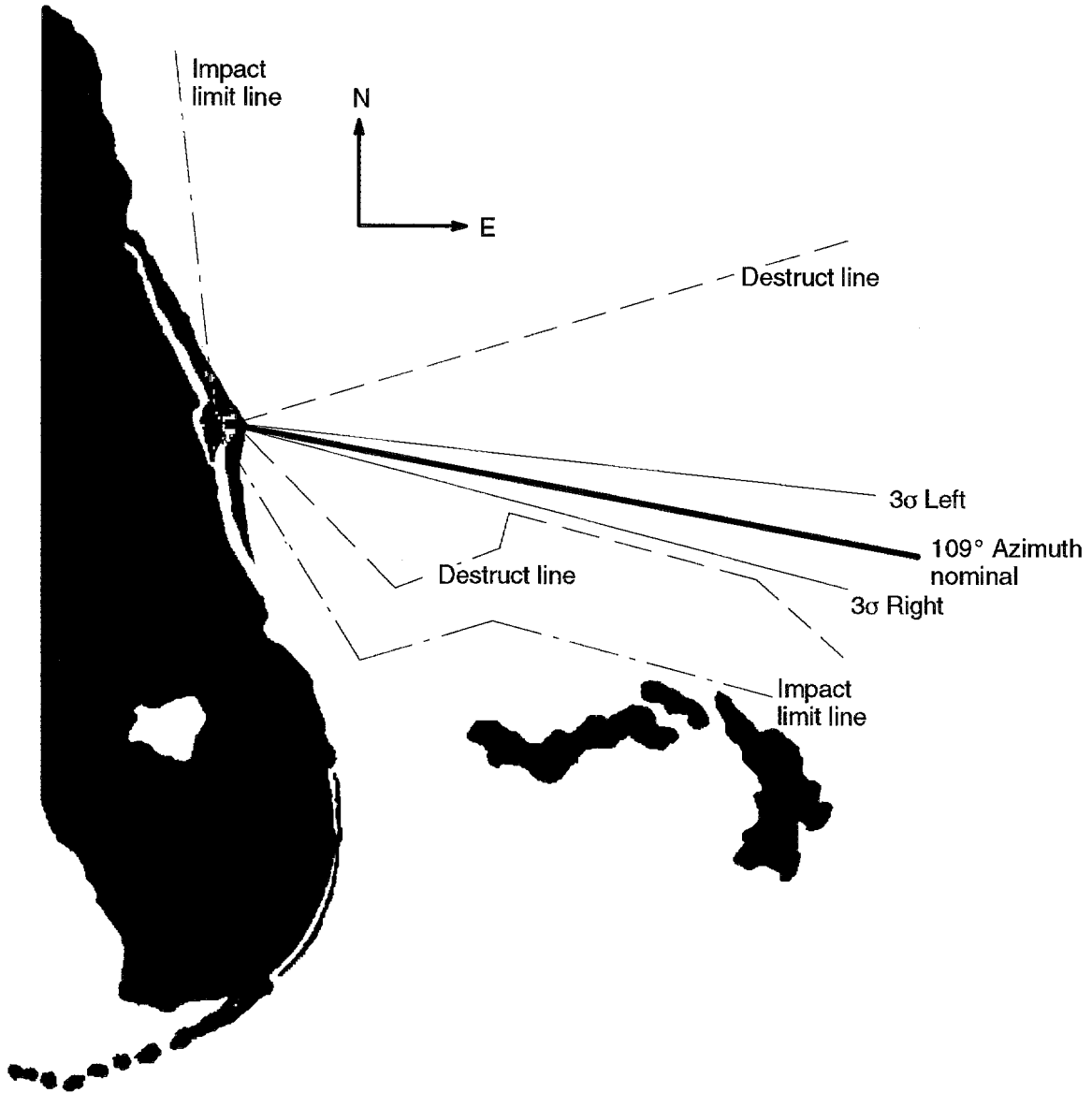
##### 81.1.2.1 Controllability

During first stage, trajectory deviations may lead to a violation of a destruct line by a shuttle that is still under control. It may be possible to return the vehicle toward its normal trajectory or to safely execute an abort. Therefore, the Flight Director (FD) and Flight Dynamics Officer (FDO) are in voice contact with the Flight Control Officer (FCO) (formerly Range Safety Officer (RSO)) during ascent. If the FCO detects a violation, the FDO and FD are immediately informed. The FD must determine whether the shuttle is controllable or uncontrollable and inform the FCO. As long as the FD declares the shuttle controllable, the FCO takes no action to terminate the flight for trajectory deviations alone (any exceptions are out of the scope of this document).

##### 81.1.2.2 Range Safety Limit Avoidance

A deviation from nominal trajectory that is large enough to warrant FCO action must be corrected. First stage options are as follows:

- A. State vector update ( $\Delta$  state)
- B. Select Control Stick Steering (CSS) (after 90 seconds Mission Elapsed Time (MET))
- C. Engage Backup Flight System (BFS)



*Figure 81-1. Impact limit lines and destruct lines  
(for illustration purposes only)*



In second stage, the options are as follows:

- A. State vector update ( $\Delta$  state)
- B. Abort to Orbit (ATO) selection
- C. Select CSS
- D. Transoceanic Abort (TAL) or Return to Launch Site (RTL) selection
- E. Engage BFS
- F. Space Shuttle Main Engine (SSME) manual cutoff. For loss of comm, the FCO will send the Range Safety System (RSS) ARM command 15 seconds from the destruct line as a cue for manual Main Engine Cutoff (MECO).

Options are listed in order of priority. The priorities are established such that higher priority options preserve the use of lower priority options and involve fewer new dangers to the crew and shuttle vehicle when possible.

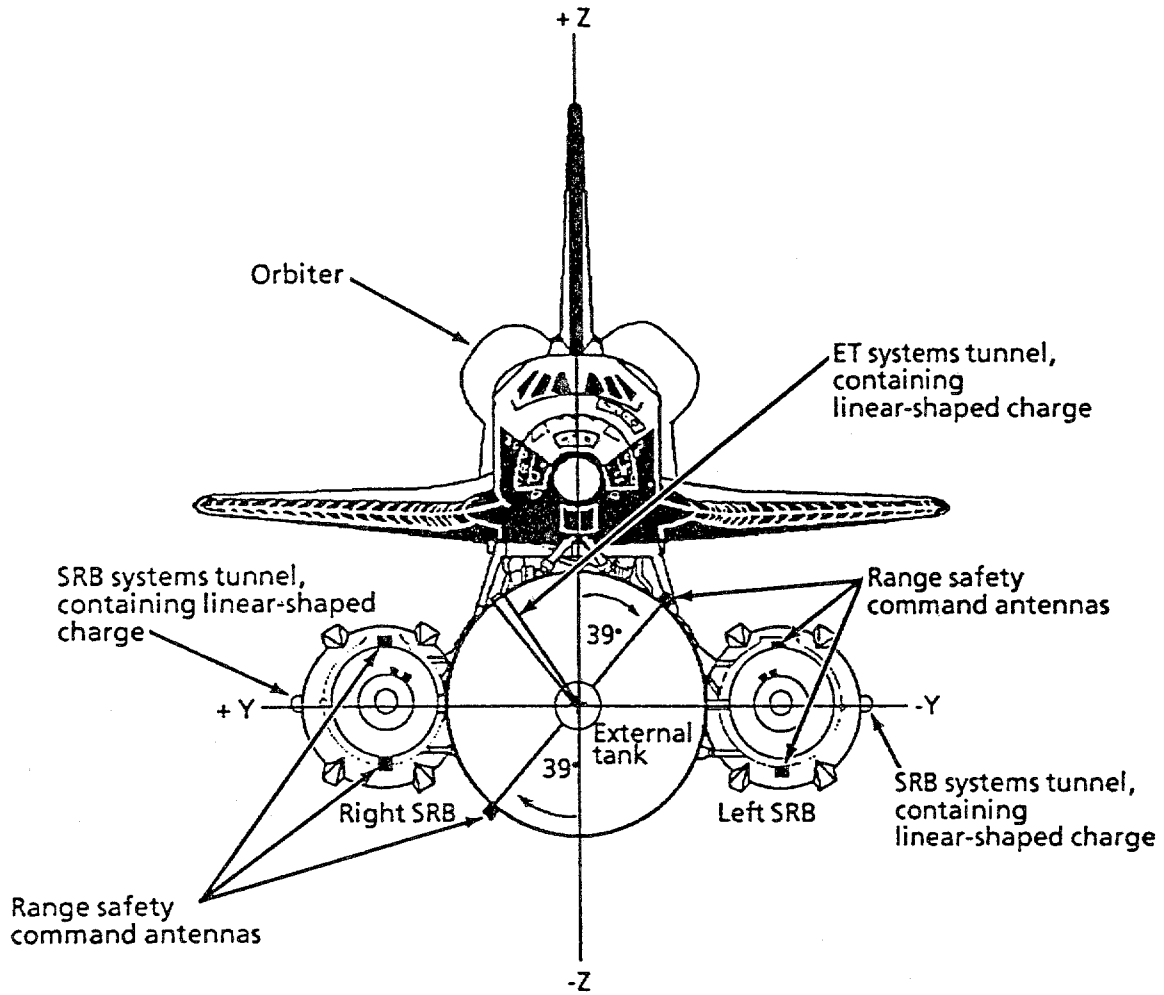
### **81.1.2.3 Space Shuttle Range Safety System Performance Summary**

The RSS consists of three autonomous subsystems (Figures 81-2 and 81-3): one in the External Tank (ET) and one in each Solid Rocket Booster (SRB). Each subsystem is capable of responding independently to RSS command transmissions. The FCO can transmit two commands to the RSS: ARM and FIRE. Each SRB subsystem can also receive a SAFE command from Ground Support Equipment (GSE) and from the onboard General Purpose Computers (GPCs) prior to SRB separation during first stage. The subsystems are cross-strapped by links in such a way that a command received by one is shared by all three. Placement of two redundant antennas on each SRB and on the ET combines with cross-strapping to provide 95 percent spherical coverage for RSS command reception.

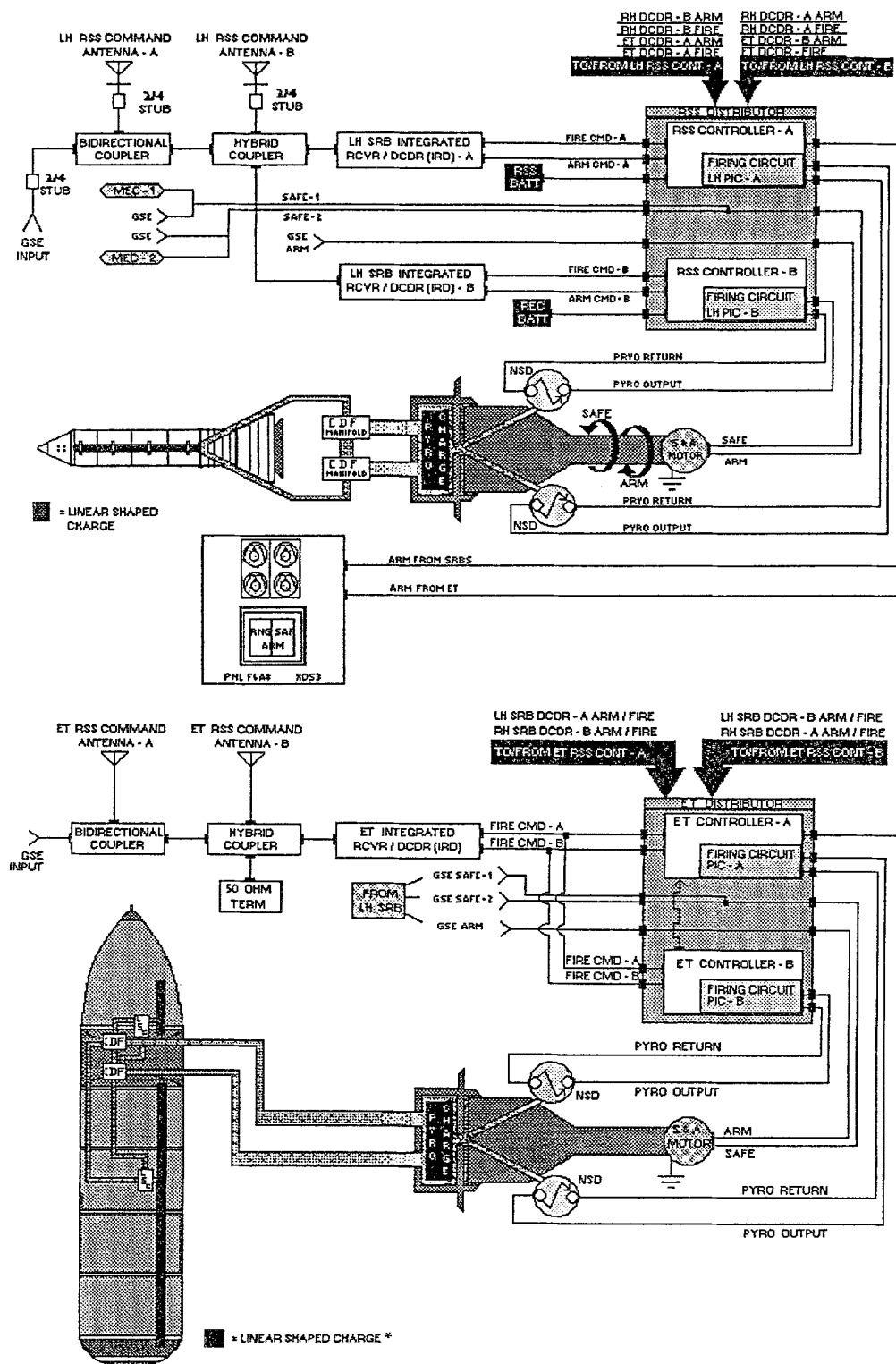
Commands passed by an SRB Integrated Receiver/Decoder (IRD) are sent to the "A" or "B" subsystem of the RSS distributor system; commands passed by the ET IRD are sent to the "B" system of the ET. Two-way dc links cross-strap the system as follows:

- A. System A of each SRB is linked to system B of the other SRB.
- B. System A of the left SRB and system B of the right SRB are linked to system A of the ET.
- C. System B of the left SRB and system A of the right SRB are linked to system B of the ET.

This action is accomplished so that any command received by any distributor subsystem is shared by all six subsystems.



**Figure 81-2. Head-on (-X) view showing range safety command antenna placements**



\*This shows a prior configuration with two linear shaped charges. Currently, there is only one, on the LO<sub>2</sub> tank.

Figure 81-3. ET/SRB range safety systems schematic

From the distributor subsystem, commands go to the Safe and Arm (S&A) device. This motor driven device is rotated to either a SAFE or ARM position. In the SAFE position, the S&A mechanically inhibits ARM and FIRE commands by physically blocking the NASA Standard Detonator (NSD) explosive path to the pyro booster charge. In the ARM position, the S&A physically opens the NSD explosive path to the pyro booster charge, which sets off the Linear Shaped Charges (LSCs) on both SRBs and the ET.

For the space shuttle, there is one LSC on each SRB and one LSC on the ET. A single explosive LSC charge-train on each SRB runs the length of the motor casing. The FIRE command detonates the LSC, causing the SRM casing to split apart, thus releasing chamber pressure to the surrounding ambient atmosphere and causing immediate thrust termination. On the ET, one LSC is placed in-line on the outer surface of the LO<sub>2</sub> tank. The FIRE command detonates the LSC, rupturing the tank and dispersing the LO<sub>2</sub>. This action, in turn, causes LH<sub>2</sub> tank rupture.

#### **81.1.2.4 Space Shuttle RSS Ground Checkout and Flight**

The following list summarizes major Shuttle Range Safety System (SRSS) events prior to launch:

A. T - 6.5 days

The SECRET classified command codes are installed in each IRD by the National Security Agency (NSA). Closed-loop tests are performed to verify functionality of the range safety and SRSS command system. (Prior to this, dummy test codes were used for open-loop test purposes before actual code installation.)

B. T - 24 hr

The NSDs are electrically mated for countdown and flight operations.

C. T - 5 min

The S&A device is rotated from SAFE to ARM position. Transmission of ARM and FIRE commands is inhibited by application of ARM INHIBIT commands from the Ground Launch Sequencer (GLS).

D. T - 10 sec

ARM INHIBIT commands are terminated from the GLS.

The shuttle lifts off with the RSS operative and ready. This action is required because a catastrophic malfunction could demand FCO action at any time between SSME start and MECO.

Prior to SRB separation, the orbiter GPCs transmit SAFE commands, which remove power from the SRB RSS systems. This action is accomplished in order to facilitate safe SRB recovery operations by recovery personnel. In the event of abnormal SRB separation, the SRB RSSs remain active to provide the FCO with a means to destroy the SRBs. The orbiter does not SAFE the ET RSS system prior to ET separation

because the ET is not recoverable. Also, the potential remains that a destruct command response may be required in order to prevent the ET from impacting land masses.

## **81.2 SHUTTLE RANGE SAFETY SYSTEM CONFIGURATION**

### **81.2.1 SRB RSS Description**

Each SRB RSS consists of two antenna couplers, two redundant IRDs, one RSS Distributor (RSD) that consists of two RSS controller/firing circuits (A/B), an S&A device with two NASA Standard Initiator (NSI) detonators (NSDs), two Confined Detonating Fuse (CDF) manifolds, seven CDF assemblies, and one LSC.

The antenna couplers (one directional and one hybrid) provide the proper impedance for radio frequency and Ground Support Equipment (GSE) commands. The command receivers are tuned to RSS command frequencies and provide the input signal to distributors when an RSS command is received. The command decoders use a code plug (P-plug) to prevent any adverse command signals from entering the distributors. The distributors contain the logic enabling valid destruct power to be applied to the RSS NSIs.

### **81.2.2 ET RSS Description**

The ET RSS consists of redundant command antennas, a directional and hybrid coupler, and an IRD. Pyrotechnic assemblies and functionalities are identical to those found within the SRB RSS.

## **81.3 RSS COMMAND MESSAGE FORMAT**

Each RSS command message is composed of 11 characters. Each character consists of two audio tones selected from a group of seven in the range 7.35 to 13.65 kHz, equally spaced 1.05 kHz apart. The same commands used in the encoder on the ground are loaded into the microprocessor in the decoder onboard the vehicle prior to flight. The first 10 characters are each about 7 msec long, with a 1.5 msec space between characters. The 11th character is about 30 msec in duration. The 11th character defines the specific command.

If the command agrees with the prestored command in the microprocessor, then the output of the decoder is enabled. If not, then the output will not be enabled, and the decoder will be reset to await the next command. If the command was valid, the decoder will output a discrete signal (28 V dc for about 45 msec), sending an ARM or FIRE discrete signal to the RSS distributor.

## **81.4 TELEMETRY**

There are 10 telemetry measurements which are monitored on the ground; 2 measurements for each receiver and decoder system.

#### **81.4.1 Decoder ON/Checktone OFF**

The event will be HI (Decoder ON/checktone OFF) when power is applied to the decoder without a pilot tone transmitting from the ground, but the FCO will be able to transmit a 15.45-Mhz pilot tone (the "checktone") to disable this event and cause it to go LO (decoder ON/checktone ON). This exercise allows the FCO to verify that all RSS receivers are receiving command transmissions.

#### **81.4.2 Receiver Signal Strength**

This is an analog measurement which is a measure of the total received RF power. The range of measured power is from about -100 dBm to -50 dBm, corresponding to a transducer range of 0.5 V dc to 5.0 V dc. Transducer-telemetry saturation occurs at -50 dBm/5.0 V dc. The measurement will nominally be in the saturation region (i.e., >-50 dBm).

### **81.5 POWER**

(Refer to SSSH drawings 5.4 and 5.5.) Each receiver/decoder receives 28 V dc power from its associated distributor. The ET uses two dedicated batteries connected in parallel for power. The SRBs use a dedicated battery for system A and the recovery battery for system B.

The dedicated battery is the primary RSS power source. This battery supplies 28 V dc, 50 AH conditioned power to the RH and LH RSS controller A units alone.

The recovery battery is a 28 V dc, 50 AH energy source used to supply power to the following recovery and RSS devices:

- A. LH/RH RSS-B controllers
- B. RF recovery beacon
- C. Flashing light assembly (white strobe)
- D. Pyrotechnic initiator controller power to: nozzle extension severance; nose cap and frustum release, and main parachute disconnect

### **81.6 RSS HARDWARE LOCATIONS**

#### **81.6.1 SRB RSS Hardware Locations**

Two RSS antennas, spaced 180° apart, are skin mounted on each SRB forward skirt. The SRB RSS decoders and associated RSS hardware are mounted within the forward skirt assemblies.

### 81.6.2 ET RSS Hardware Locations

Two RSS antennas, spaced 180° apart, are skin mounted on the intertank bulkhead of the ET. The ET RSS decoders and associated RSS hardware are mounted within the intertank bulkhead.

### 81.7 RSS CONTROL AND OPERATIONS

(Refer to drawing 5.5-2, SSSH, JSC-11174.) The received range safety RF signal is demodulated in the FM receiver to recover the baseband audio signal. The audio signal is converted from an analog signal to a 6-bit digital signal before being processed further by the decoder. The decoder samples this signal at a 33.6-kHz rate and stores the samples in the microprocessor using Direct Memory Access (DMA) techniques. In the search mode, these data samples will be continually processed through several different algorithms to determine if a signal is present. If a signal is present, then further processing will determine whether the signal is a command or a 15.45-kHz pilot tone. If a pilot tone is detected, the decoder ON/checktone OFF telemetry indicator will be set to the LO state. When the pilot tone is not present, the same telemetry indicator will be in the HI state.

If a command is detected, then additional processing will determine if the 11 characters that were transmitted were valid. If the 11 characters are valid, further processing will ensure that the received command compares exactly with 1 of the 5 commands loaded into the microprocessor prelaunch. These commands are

- A. ARM
- B. FIRE
- C. Three spare commands

If the command does not compare with a prestored command, the decoder output will be inhibited for 45 milliseconds, and then the decoder will return to search mode. If the command compares exactly with a prestored command, then that compared command will be output (28 V dc) for 45 milliseconds. After the 45 milliseconds time outs, the decoder will go back into the search mode; and, if the command is still being received, the command will be output again, etc. The ground range safety transmission system normally outputs the selected command (ARM/FIRE) in groups of 10 commands at a time. The pilot tone is transmitted in a random fashion to ensure that all range safety IRDs are locked up to the ground-transmitted 416.5-MHz carrier. This pilot tone will be inhibited at least 1/10th second before a command is transmitted to the space shuttle vehicle.

### 81.8 OPERATIONAL NOTES

At present (April 1994), the ET RSS has a CRITICAL 1 failure mode which requires a waiver for each flight. This failure mode is because of the single ET IRD, for which no redundancy exists for that unit on the ET, vice the redundant units found on the SRBs.

In addition, the ET RSS IRD redesign is necessary due to parts obsolescence of IRD components.

A proposed redesign is in work to replace the outdated ET IRD and its associated RSD with two Enhanced Receiver/Decoder (ERD) units. This task will eliminate the CRITICAL 1 failure mode and its associated waiver. Effectively for the modification is STS-90 and subsequent flights.

## 81.9 REFERENCES

### A. Narrative

1. Range Safety System Signal Control, Specification No. 16A03039, Dec. 1977.
2. Range Safety Command Destruct System Handbook, No. 10A00570, July 1977.
3. Range Safety Command Destruct System, Specification No. 30A90506, Dec. 1977.
4. Digital Command Receiver, MCR-503 (modified), Motorola Inc., Tech Manual, Dec. 1964.
5. Secure Range Safety Command Decoder Model AED-201, AVCO Corp., PN331800, Nov. 1965.
6. Integrated Receiver/Decoder Tech Manual (MSFC Contract NAS8-33440), Cincinnati Electronics Corp., Dec. 1980.
7. Range Safety System Handbook 10A00570 (MSFC Contract NAS8-32000), United Space Boosters, Inc., July 1983.

### B. Drawings

1. ET INTERCONNECT, 16A10565
2. SRB CABLE INTERCONNECT, 16A10240
3. SRB ELECTRICAL SCHEMATIC, 16A10241
4. SKETCH-RANGE SAFETY SYSTEM (ET & SRB), SK-EC-14-BN-10

**Table 81-1. SRB/ET range safety system**

#### ANTENNA

|                 |                                    |
|-----------------|------------------------------------|
| Frequency range | 406 to 420 MHz (nominal 416.5 MHz) |
| Polarization    | Left Hand Circular (LHC)           |

#### DIRECTIONAL COUPLER

|                 |        |
|-----------------|--------|
| Input impedance | 50 ohm |
|-----------------|--------|



*Table 81-1. SRB/ET range safety system (concluded)*

|                               |  |             |  |
|-------------------------------|--|-------------|--|
| Insertion loss                | 0.3 dB (max)                             |             |  |
| Coupling                      | 16 dB                                    |             |  |
| Directivity                   | 24 dB (min)                              |             |  |
| <u>HYBRID COUPLER</u>         |  |             |  |
| Input impedance               | 50 ohm                                   |             |  |
| Insertion loss                | 3.4 dB                                   |             |  |
| Isolation                     | 24 dB                                    |             |  |
| <u>RECEIVER</u>               |  |             |  |
| Input impedance               | 50 ohm                                   |             |  |
| Center frequency              | 416.5 MHz                                |             |  |
| Receiver type                 | FM                                       |             |  |
| Frequency deviation           | ±60 kHz                                  |             |  |
| Audio bandwidth               | 7 to 15.45 kHz                           |             |  |
| Input voltage                 | 28 V dc                                  |             |  |
| Input power                   | 12 W (max) at 28 V dc                    |             |  |
| <u>DECODER</u>                |  |             |  |
| Signal type                   | Dual tones (A/D converted)               |             |  |
| Input voltage                 | 24 V dc to 36 V dc                       |             |  |
| Input power                   | 12 W (max)                               |             |  |
| Functional outputs            | 5: - FIRE, ARM, and three spare commands |             |  |
| Discrete levels               | 28 V dc                                  |             |  |
| Discrete durations            | 40 ±5 msec                               |             |  |
| <u>TELEMETRY MEASUREMENTS</u> |  |             |  |
| <u>Measurement Title</u>      | <u>Vehicle</u>                           | <u>MSID</u> |  |
| RSS DCDR "X" ON/checktone OFF | LSRB A                                   | B55X1871X   |  |
| 1 = "ON"                      | LSRB B                                   | B55X1872X   |  |
|                               | ET                                       | T55X1925E   |  |
|                               | RSRB A                                   | B55X2871X   |  |
|                               | RSRB B                                   | B55X2872X   |  |
| RSS RCVR SIGNAL STRENGTH      | LSRB A                                   | B55E1100C   |  |
| 0.5 to 5 VDC                  | LSRB B                                   | B55E1101C   |  |
|                               | ET                                       | T55E1130A   |  |
|                               | RSRB A                                   | B55E2100C   |  |
|                               | LSRB B                                   | B55E2101C   |  |

THIS PAGE INTENTIONALLY BLANK

Distribution for JSC-18611 (total = 57)

**NASA/JSC**

DF2/  
DF24/Group Lead (22)  
DO56/R. P. Campbell  
DO5/J. McKenna  
DT35/J. Plumpton  
DT37 (5)  
DT37/V. K. Renfrew  
EV211/B. C. Embrey  
EV813/C. Foster  
EV4/C. Sham  
NS44/B. Goffney

**NASA/GSFC**

Greenbelt, MD 20771  
Code 531/M. Steiner

**NASA/KSC**

Kennedy Space Center, FL 32899  
PK-F1/RF COM (4)  
PH-F2/S. Green  
USK-195/P.R. Gratsch  
USK-N94/G. H. Sawasky (3)

**NASA/MSFC**

Marshall Space Flight Center, AL 35812  
EO27/A. Johnson  
EO27/D. Mann  
PD11/R. White

**Lockheed-Martin**

LMTO/Orgn 52-20/Bldg 100  
Onizuka Air Station  
1080 Lockheed Way, Box 061  
Sunnyvale, CA 94087-1237  
R.R. Fink

**Hernandez Engineering Inc.**

H10H-115/Editing

**McDonnell Douglas Aerospace**

689 Discovery Drive  
Huntsville, AL 35806  
21A1/Spacelab Library

**Boeing**

12214 Lakewood Blvd  
Downey Ca. 90241  
FB94/J. Swanson

**Boeing North American**

FB05/J. Ogle  
HZ1-10/M. May

**United Space Alliance**

USH-636L/M. Fulton  
USH-636L/T. Conkey  
USH-635K/K.Bimage

**NOTE: FOR CHANGES IN DISTRIBUTION OR ADDRESS CORRECTIONS CONTACT**

DF24/E. Wingrove  
Johnson Space Center  
Houston, Texas 77058  
281-483-7273  
eric.wingrove-1@ nasa.gov