

**GPC PRACA HISTORY RELATING TO STS-135 ANOMALY**

PRACA Report #	Vehicle	Flight/Mission	GPC S/N	Symptom	Attributed Cause
KA0096 060V-0042 UA3180112	OV-103	STS-51 Sep 1993	508	DURING STS-51 DEORBIT OPERATION, GPC #3 EXPERIENCED A FAILED TO SYNCHRONIZE DURING THE GPC OPS #3 REDUNDANT SET FORMATION PRIOR TO ENTRY.	UA-THE HISTORY OF THE GPC COUPLED WITH SUBSEQUENT PERFORMANCE OF ALL THE HARDWARE SUBSYSTEMS ON OV-103 INDICATES THAT IF THE CAUSE WERE A HARDWARE FAILURE THEN IT WAS INTERMITTENT. THERE IS NO EVIDENCE TO INDICATE THAT THE FTS WAS A RESULT OF ANY HARDWARE FAILURE. NO CAUSE OF THE FTS HAS BEEN DETERMINED AND NONE OF THE POTENTIAL AREAS OF CONCERN (PROCEDURAL, SOFTWARE, OR HARDWARE) HAVE OR CAN BE ELIMINATED. A DETERMINATION OF A MOST PROBABLE CAUSE OF THE FTS HAS NO STRAIGHTFORWARD APPROACH BECAUSE WITHOUT FURTHER DATA (OF WHICH NONE IS AVAILABLE) NONE OF THE POTENTIAL CAUSE CATEGORIES (PROCEDURAL, SOFTWARE, OR HARDWARE) CAN BE ELIMINATED. NO ADDITIONAL SPECIFIC ELEMENT TESTING CAN BE IDENTIFIED WHICH WOULD YIELD MEANINGFUL RESULTS. HOWEVER, RUNTIME CONFIDENCE TESTING TO ACQUIRE TIME EXERCISING THE INTEGRATED DPS SYSTEM IS CONSIDERED PRODUCTIVE TESTING. THE SUBSYSTEM, HARDWARE AND SOFTWARE, HAS EXECUTED FLAWLESSLY SINCE THE FTS. THERE IS NO INDICATION THAT THE FTS WAS CAUSED BY A GENERIC PROBLEM. THE FTS WAS CAUSED BY SOME TRANSIENT EFFECT AND ITS EFFECTS WERE LIMITED TO A SINGLE GPC DURING RS EXPANSION. WITHOUT A SUBSTANTIAL CAUSE, THE REMOVAL OF ANY HARDWARE WITHIN THE SUBSYSTEM IS NOT RECOMMENDED. THE MOST PROBABLE CAUSE IS THE SOFTWARE SCENARIO IN WHICH GPCS 1,2 AND 4 DID NOT DETECT GPC 3 AT THE I/O COMPLETION POINT FOR DEU POLLING. THIS IS BASED ON THE FACT THAT DEU I/O IS UNIQUE IN THAT ALL APPLICABLE DEUS ARE POLLED CONSECUTIVELY IN ONE OR MORE CYCLES AND EACH GPC HAS ITS OWN DETERMINATION OF APPLICABLE DEUS. THE GPC'S DETERMINATION OF APPLICABLE DEUS IS REFRESHED AT THE END OF THE OPS TRANSITION WITH A READ OF THE BCE RECEIVER ENABLE REGISTER. THIS SPECIFIC READ DURING AN OPS TRANSITION IS DIFFERENT FROM THE CYCLIC PROCESS USED BY OTHER TYPES OF I/O.
KB4255	OV-103	STS-103 Dec 1999	504	DURING POWER DOWN IN POST LANDING, GPC 1(S/N 504) EXPERIENCED A FAILURE INVOLVING THE TRANSITION FROM "RUN" TO "STANDBY". THE GPC's IO TALKBACK INDICATOR DID NOT TRANSITION FROM GRAY TO BARBERPOLE AS EXPECTED.	UA - THE ERROR EXPERIENCED ON OV103, GPC S/N 504, CAN BE EXPLAINED BY A SINGLE EVENT UPSET (SEU) OF THE CPU LOCAL STORE. DURING NORMAL OPERATIONS, THE CPU RELIES UPON CONSTANT VALUES LOADED IN ITS INTERNAL LOCAL STORE TO COMPLETE DIFFERENT TASKS. IN THIS INSTANCE, THE CPU LOCAL STORE CONTAINS THE HARDWARE COMMANDS NECESSARY TO LOAD THE PROGRAMMABLE TIMERS. THE NORMAL SEQUENCE OF EVENTS FOR TIMER LOADING IS AS FOLLOWS: 1) STOP THE TIMER 2) LOAD THE TIMER 3) RESTART THE TIMER A HISAM DUMP WAS PERFORMED. THE RESULTS OF THE HISAM DUMP DISCLOSED THE FOLLOWING: THE GPC TOOK A PROGRAM CHECK INTERRUPT FOR AN ILLEGAL OPCODE/ILLEGAL IO COMMAND WHILE PERFORMING AN UPDATE TO THE PROGRAMMABLE TIMER 1. THE SYNC TRACE LOG INDICATED THAT TIMER 1 DID GET UPDATED. THE CPU MICROCODE USES THE SAME MICROROUTINE TO LOAD BOTH TIMER 1 AND TIMER 2. HOWEVER, THE LOCAL STORE CONSTRAINTS USED DIFFER DEPENDING ON THE TIMER BEING LOADED. THESE CONSTRAINTS ARE THE ACTUAL HARDWARE COMMANDS SENT TO THE MEMORY MANAGEMENT UNIT (MMU) TO PERFORM THE VARIOUS FUNCTIONS. A SINGLE EVENT UPSET AT THE RIGHT LOCAL STORE, CPU SECTOR 3, REGISTER 5 WILL CAUSE THE RESTART TIMER 1 COMMAND (8802H) TO FAIL. THIS CAN RESULT IN AN ILLEGAL OPERATION CONDITION AND CAUSE A PROGRAM CHECK- ILLEGAL IO INTERRUPT. INDICATORS VIEWED IN THE SIMULATED FAILURE WERE IDENTICAL TO THE ORIGINAL FAILURE. 1) PROGRAM CHECK- ILLEGAL OPCODE/ILLEGAL IO INTERRUPT TAKEN 2) TIMER 1 STOPPED 3) TIMER 1 HIGH HALFWORD CONTAINING 1F 4) SYNC TRACE LOG INDICATING TIMER STOPPED 5) RUN DISCRETE ACTIVE 6) IO TALKBACK ACTIVE. ANOTHER INDICATION THAT CORRELATES THIS SCENARIO TO THE ACTUAL FAILURE IS THAT THE TRANSITION OF THE GPC FROM HALT TO STDBY REINITIALIZES LOCAL STORE AND CORRECTS THE ERROR. THE CPU LOCAL STORE IS SUSCEPTIBLE TO SEU's AS DOCUMENTED IN THE SPACE SHUTTLE GENERAL PURPOSE COMPUTER RADIATION EFFECTS STUDY-1991 UPDATE.FTP TESTING PERFORMED FOR 40 HRS OVER 4500 PASSES OF FTP TESTED THAT CIRCUITRY IN THE 40 HOUR TIME PERIOD. NO FURTHER ACTION IS NECESSARY. FAILURE HISTORY THERE HAVE BEEN NO FAILURES ON THIS UNIT THERE HAS BEEN ONE OTHER DOCUMENTED SEU IN THE GPC INVOLVING THE CPU LOCAL STORE. THIS OCCURRED ON STS-71 INVOLVING GPC S/N 536. THE ANOMALY IS CONSIDERED TO BE THE RESULT OF A SEU AND NOT THE RESULT OF A PHYSICAL FAILURE OF THE GPC. THE GPC IS CONSIDERED TO BE A "FLIGHT WORTHY" UNIT.

**GPC PRACA HISTORY RELATING TO STS-135 ANOMALY**

PRACA Report #	Vehicle	Flight/Mission	GPC S/N	Symptom	Attributed Cause
KB4394 102V-0018	OV-103	STS-92 Oct 2000	506	<p>SEVERAL HOURS AFTER LANDING, WHEN THE GPC MODE SWITCH WAS MOVED FROM RUN TO STANDBY IN FINAL PREPARATION FOR GPC 1 POWER DOWN, THE TALKBACK DID NOT CHANGE FROM RUN TO BARBERPOLE AS EXPECTED. SUBSEQUENTLY, GPC 1 WAS POWERED OFF WHILE STILL IN STANDBY AND THE MODE TALKBACK CHANGED TO BARBERPOLE.</p> <p>Program Check Interrupt occurred on the same instruction as the anomaly of STS-103 on 12-27-99 (IPR 92V-0005). A detailed analysis of the time recorded for the GPC Error Log entry caused by the Program Check Interrupt and the two Sync Trace Log entries which occurred after program check reveals that a very similar anomaly occurred during the CPU microcode execution of the ICR instruction for the two flights. The local store memory is implemented using 256X4 static RAM chips. This memory is the area of the GPC that is most susceptible to SEU's as it does not contain Error Detection/ Correction circuitry as does the main memory. The registers affected in this IPR (IPR 102V-0018) are not the same as those affected in IPR 92V-0005.</p>	<p>UA - MOST PROBABLE CAUSE OF THE ANOMALY EXPERIENCED IN GPC S/N 506 WAS A SINGLE EVENT UPSET OF THE GPC LOCAL STORE; SPECIFICALLY AN SEU OF THE RIGHT LOCAL STORE, SECTOR 3, REGISTER 4.</p> <p>A HISAM DUMP WAS PERFORMED &amp; ANALYZED. CONCLUSIONS: THE ERROR INDICATIONS ARE SIMILAR TO THE ANOMALY OBSERVED ON THE STS-103 MISSION INVOLVING GPC S/N 504 (CAR# KB4255). HOWEVER, THERE IS ONE DIFFERENCE; THE HARDWARE HALF OF TIMER 1 WAS NOT UPDATED IN THE CURRENT CASE. A PROGRAM CHECK INTERRUPT FOR AN ILLEGAL OPCODE OCCURRED DURING THE PCIO INSTRUCTION TO UPDATE TIMER 1. TIMER 1 WAS STOPPED AFTER EXPERIENCING THE PROGRAM CHECK INTERRUPT. THE HIGH END OF TIMER 1 WAS UPDATED TO THE EXPECTED VALUE. SEVERAL POSSIBLE CAUSES WERE CONSIDERED AND EVALUATED. CPU MICROCODE ERROR THE MICROCODE USED TO PERFORM TIMER UPDATES IS IDENTICAL FOR EITHER TIMER 1 OR TIMER 2 UPDATES. NO INDICATIONS OF ERRORS WERE OBSERVED WITH TIMER 2 UPDATES. BAD REGISTER IN THE CPU ONLY ONE REGISTER OUTPUTS DATA FROM THE CPU. A REGISTER FAILURE IS NOT A LIKELY CAUSE SINCE THE CPU APPEARED TO BE FUNCTIONAL BEFORE AND AFTER THE ERROR INDICATIONS. CORRUPTED DATA ON THE INTERNAL HIGH SPEED DATA BUS (HBUS) AN ERROR ON THE HBUS WOULD MOST LIKELY AFFECT MULTIPLE TRANSACTIONS. THE GPC APPEARED TO BE FUNCTIONAL AFTER THE PROGRAM CHECK INTERRUPT FAULTY CIRCUITRY IN THE MEMORY MANAGEMENT UNIT (MMU) ALL XIO COMMANDS ARE DECODED IN THE MMU BY AN FPLA, AND ASSOCIATED LOGIC GATES. AN ERROR WITH A FPLA IS TYPICALLY A HARD FAILURE AN ERROR IN THIS CIRCUITRY WOULD AFFECT MORE THAN ONE XIO COMMAND. A PCIO TO UPDATE EITHER TIMER 1 OR 2 WOULD EXERCISE THE FPLA IDENTICALLY. AN ERROR BEYOND THIS POINT IN THE MMU LOGIC WOULD NOT RESULT IN A PROGRAM CHECK INTERRUPT A TIMER 2 INTERRUPT WAS EXPERIENCED AFTER THE PROGRAM CHECK INTERRUPT OCCURRED. NO PROGRAM CHECK INTERRUPT WAS EXPERIENCED WHILE PERFORMING TIMER 2 INTERRUPT HANDLER. INDICATES THAT THE HARDWARE ASSOCIATED WITH THE TIMER UPDATE FUNCTIONED NOMINALLY FAILED CPU LOCAL STORE THIS WOULD RESULT IN A HARD FAILURE. THE GPC FUNCTIONED NORMALLY AFTER THE POWER CYCLE. SINGLE EVENT UPSET (SEU) LOCAL STORE IS ONLY INITIATED AT POWER ON OR UPON EXITING THE "SLEEP" MODE. GPC S/N 506 WAS INSTALLED IN SLOT 1 AND WAS POWERED UP AND IN THE "RUN" MODE FROM PRE-LAUNCH THROUGH POST LANDING. THE UPDATE OF TIMER 1 IS ONLY PERFORMED DURING TRANSITIONS TO AND FROM STANDBY. AS STATED ABOVE, THE GPC WAS POWERED UP AND IN THE "RUN" MODE FROM PRE-LAUNCH THROUGH POST LANDING. THE LOCAL STORE IS COMPOSED OF SRAM A RADIATION EFFECTS STUDY PERFORMED BY IBM IN 1991 REVEALED THAT THE SRAM USED IN THE REGISTERS (AM9122 256X4 NMOS SRAM) IS THE COMPONENT OF THE GPC THAT IS THE MOST SUSCEPTIBLE TO THE EFFECTS OF RADIATION. THE CPU LOCAL STORE CONTAINS 4 BANKS OF 4 CHIPS. IT IS BROKEN UP INTO LEFT LOCAL STORE AND RIGHT LOCAL STORE. EACH LOCAL STORE CONTAINS THE SAME INFORMATION. A REGISTER IS 16 BITS WIDE AND IS BROKEN UP OVER 4 CHIPS. LOCAL STORE IS INITIALIZED AT POWER UP BY CPU MICROCODE FROM PROM'S. LOCAL STORE CONTAINS ALL MACRO REGISTERS, INTERMEDIATE FLOATING POINT VALUES, AND CONSTANT DATA.</p>
KB4394 (continued)	OV-103	STS-92 Oct 2000	506		<p>FLIGHT SOFTWARE DOES NOT RELY ON MACRO REGISTERS TO CONTAIN INFORMATION FOR EXTENDED PERIODS OF TIME (TYPICALLY LESS THAN 40 MS). ANY DATA TO BE KEPT IS PLACED IN CPU MAINSTORE. OF THE POSSIBLE 1024 CPU LOCAL STORE REGISTERS, 400 REGISTERS ARE USED. OF THE 400 REGISTERS, 333 REGISTERS ARE CONSIDERED CONSTANT (DATA IS NOT CHANGED AFTER INITIALIZATION). OF THE 333 REGISTERS, 37 ARE USED FOR DIAGNOSTIC FUNCTIONS, AND THUS, ARE NOT USED IN FLIGHT. THE END RESULT IS, 296 REGISTERS OUT OF 1024 ARE CONSIDERED CONSTANT WHILE THE GPC IS OPERATING. CPU LOCAL STORE HAS NO PROTECTION IMPLEMENTATION. CONTRIBUTING FACTORS TO THIS DECISION ARE SPEED, REAL ESTATE, AND POWER REQUIREMENTS. CPU MAIN MEMORY IS ALSO SUSCEPTIBLE TO THE EFFECTS OF RADIATION. HOWEVER, THE MAIN MEMORY IS "SCRUBBED" ON A REGULAR BASIS, AND IS ALSO PROTECTED BY ERROR DETECTION AND CORRECTION (EDAC) ROUTINES. IOP LOCAL STORE AND DMA QUEUE BOTH HAVE PARITY HARDWARE IMPLEMENTED, HOWEVER, FLIGHT SOFTWARE CURRENTLY HAS ALL PARITY CHECKING DISABLED. THE IOP CHECKING IS DISABLED IN THE FSW SINCE IT WAS DISCOVERED DURING Jael TESTING THAT THERE ARE CERTAIN FAILURE MODES OF BTU'S THAT RESPOND TO IOP READ REQUESTS. THIS CONDITION CAN TRIGGER THE PARITY DETECTION LOGIC IN THE IOP TO DETECT A PARITY ERROR. SINCE THIS COULD BE MANIFESTED BY MULTIPLE GPC'S SIMULTANEOUSLY, THE EXPOSURE TO THE PASS RS OPERATION WAS CONSIDERED UNACCEPTABLE. THEREFORE, THE SHUTTLE PROGRAM COMMUNITY DECIDED THAT IT WAS BETTER TO DISABLE THE PARITY CHECKING THAN EXPOSE THE SYSTEM TO THE POTENTIAL FOR MULTIPLE GPC FAILURES DUE TO SOME EXTERNAL SOURCE. IT IS THE OPINION OF THE PRT THAT THE MOST PROBABLE CAUSE OF THE ANOMALY EXPERIENCED IN GPC S/N 506 WAS A SINGLE EVENT UPSET OF THE GPC LOCAL STORE; SPECIFICALLY AN SEU OF THE RIGHT LOCAL STORE, SECTOR 3, REGISTER 4. THE REGISTER AFFECTED IN THIS CASE IS NOT THE SAME REGISTER AS THAT OF CAR #KB4255. THERE IS THE DISTINCT POSSIBILITY THAT THE CHIP AFFECT IS NOT EVEN THE SAME CHIP. FAILURE HISTORY THERE HAVE BEEN NO PREVIOUS RECORDED ANOMALIES RELATED TO GPC S/N 506. THERE HAVE BEEN TWO OTHER DOCUMENTED ANOMALIES ATTRIBUTED TO SEU'S IN THE GPC INVOLVING THE CPU LOCAL STORE. THE FIRST OCCURRED ON STS-71 INVOLVING GPC S/N 536. THE SECOND ONE OCCURRED ON STS-102 INVOLVING GPC S/N 504. THE PRT CONCURS THAT THIS ANOMALY IS CONSIDERED TO BE THE RESULT OF A SEU AND NOT THE RESULT OF A PHYSICAL FAILURE OF THE GPC. THE GPC IS CONSIDERED TO BE A "FLIGHT WORTHY" UNIT.</p>

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<b>PRACA Report #</b>	<b>Vehicle</b>	<b>Flight/Mission</b>	<b>GPC S/N</b>	<b>Symptom</b>	<b>Attributed Cause</b>
KB2594 DIG-3-16-0277	OV-103	KSC Jan 1993	526	<p>AT KSC, DURING ROUTINE MONITORING IN A FOUR GPC (GPC 2 THROUGH GPC 5) REDUNDANT SET, GPC 2 (P/N MC615-0025-0202, S/N 526) LOGGED A SINGLE I/O ERROR: "HDA INPUT RDS, FA2 INPUT PROM SEQ 3,10". THE STATUS REGISTER OF 1D00 0000 INDICATED THAT THE S, V, SIGNATURE MISMATCH, AND PARITY ERROR BITS WERE SET DURING A BUS 15/FLIGHT CRITICAL 6 (FC6) TRANSACTION. FC6 WAS COMMANDED BY GPC 3. GPC'S 3, 4, AND 5 DID NOT RECEIVE AND I/O ERROR CONDITION. NO FAIL TO SYNC, I-FAIL, OR U-FAIL, VOTES WERE OBSERVED FROM ANY OF THE REDUNDANT SET GPC'S. AS PART OF PRELIMINARY TROUBLESHOOTING GPC 2 AND GPC 3 MAIN MEMORY WERE DUMPED. DATA ANALYSIS DETERMINED THAT THE DUMPED GPC'S PERFORMANCE WAS NOMINAL AND PER DESIGN SINCE ONLY ONE I/O ERROR WAS LOGGED AND GPC 2 WAS ABLE TO MAKE A PREDETERMINED SYN POINT (AT LEAST 40 MS) WITH THE OTHER GPCS. THE VENDOR HAS INDICATED THAT THIS I/OERROR OCCURRENCE IS A RECREATION OF AN EARLIER PROBLEM THAT WAS SEEN DURING THE MAY 1990 INITIAL VENDOR "SELL OFF". THE ORIGINAL PROBLEM OCCURRED ON ANOTHER GPC BUS AND WAS A SINGLE OCCURRENCE IN WHICH A PROBLEM WAS DETECTED DURING A MIA TRASACTION (GPC S/N 526).</p>	<p>THE MOST LIKELY CAUSE OF THIS UNEXPLAINED ANOMALY WAS IDENTIFIED AS THE MIA ASSOCIATED WITH BCE 15; MIA P/N A538R485-20, S/N 458, LOCATED ON MIA PAGE ASSEMBLY P/N 6966025-20, S/N 564. BCE 15 CORRESPONDS TO THE "A" SIDE OF MIA S/N 458. THE GPC WAS REMOVED AND RETURNED TO IBM/OWEGO FOR FAILURE ANALYSIS. THE UNIT WAS TESTED TO DETERMINE IF THERE WERE ANY CHARACTERISTICS ASSOCIATED WITH THE SUSPECT MIA THAT WERE DIFFERENT FROM OTHER MIA'S INSTALLED IN THE GPC. OF PRIMARY INTEREST WERE COMPARISONS OF SIGNAL TIMING AT THE MIS PAGE INTERFACE. THE COMPARISONS DISCLOSED NO SIGNIFICANT DIFFERENCES. THE COMPARISONS DISCLOSED NO SIGNIFICANT DIFFERENCES. THE FOLLOWING TESTS WERE SUBSEQUENTLY PERFORMED: -BASELINE TESTS (ROOM AMBIENT FAT) -EXAMINATION OF ALL INTERFACE SIGNALS DURING -5 TO +105 DEGREE BURN-IN -ROOM AMBIENT TESTING WHILE OPERATING ALL 24 MIA CHANNELS -MIA PAGE, S/N 564, WAS REMOVED FROM THE GPC AND SUBJECTED TO A COMPLETE VISUAL EXAMINATION. THE RESULTS OF THE ABOVE TESTING DISCLOSED NO ANOMALOUS CONDITIONS. MIA, S/N 458, WAS REMOVED FROM MIA PAGE ASSEMBLY, S/N 564, AND SENT TO GEC-MARCONI FOR FAILURE ANALYSIS. A REPLACEMENT MIA, S/N 1073, WAS INTSALLED ON MIA PAGE ASSEMBLY, S/N 564, AND THE PAGE SUCCESSFULLY COMPLETED PAGE LEVEL FUNCTIONAL TEST PRIOR TO INSTALLATION INTO GPC, S/N 526. PRIOR TO INITIAL CAT AND DELIVERY, GPC, S/N 526, EXHIBITED A ONE TIME EVENT WITH THE SAME FAILURE SYMPTOMS. THIS OCCURRED DURING BURN-IN AT +105 DEGREES F. THE INCIDENT WAS REPORTED TO RIC AND NASA. MIA PAGES AND MIA'S WERE MOVED AROUND WITHIN THE SRU'S AND LRU TO PERMIT POSITIVE IDENTIFICATION OF THE FAULTY HARDWARE IF THE INCIDENT SHOULD REPEAT. NASA, RIC, AND IBM JOINTLY AGREED TO COMPLETE THE INITIAL DELIVERY SEQUENCE. THE ENSUING INVESTIGATION DISCLOSED THE FOLLOWING CONDITIONS: -FAILED FTP SPECIAL CONCURRENCY TEST 21 WHILE AT 105 DEGREES F. THE TEST SENDS TWO GROUPS OF THREE WORDS FROM ONE CHANNEL THROUGH AN EXTERNAL WRAP CIRCUIT TO A RECEIVER IN A SECOND CHANNEL OF THE GPC -RECEIVED DATA EXHIBITED BAD IUA, PARITY AND SEV. EXTENSIVE TESTING FAILED TO CAUSE THE ANOMALY TO REPEAT. THEREFORE, THE PROBLEM COULD NOT BE ISOLATED TO EITHER TRANSMITTER OR RECEIVER. GIVEN THE SITUATION AT THE TIME, THE FOLLOWING ACTIONS WERE TAKEN PRIOR TO DELIVERY; -DETAILED VISUAL INSPECTION OF THE PAGE ASSEMBLY AND ASSOCIATED MIA'S -IN ORDER TO ISOLATE THE FAILURE, MIA PAGE AND MIS LOCATIONS WERE CHANGED WITHIN THE GPC -FULL FAT VIBRATION TEST (50 SECONDS AT FULL LEVEL IN EACH AXIS) -COMPLETED 8 NORMAL (-5 TO +105 DEG. F) BURN-IN CYCLES -COMPLETED 12 NORMAL BURN-IN CYCLES -COMPLETED 5 EXTENDED BURN-IN CYCLES (-65 TO +120 DEG. F) - COMPLETED FULL ATP AND SHIPPED TO HOUSTON FOR 1000 HOURS OF OPERATION. AFTER INITIAL DELIVERY, THE GPC SUCCESSFULLY COMPLETED 3000 HOURS OF OPERATION PRIOR TO THE REPORTED FAILURE. THE COMBINATION OF BOTH THE INITIAL AND THE FIELD FAILURES PERMITTED ISOLATION OF THE PROBLEM TO MIA, S/N 458. THE MIA HAS BEEN REMOVED AND RETURNED TO GEC-MARCONI FOR FAILURE ANALYSIS.</p>

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PRACA Report #	Vehicle	Flight/Mission	GPC S/N	Symptom	Attributed Cause
AD9959	FSW	Mar 1994		DATA ANOMALY OF FTS THAT OCCURRED IN SMS DISCLOSED INCORRECT CODES BEING CLEARED/SET IN THE GPC PSW.	<p>WHEN ANY OF 9 CPU CRASH INTERRUPTS ARE TAKEN THE CONDITION CODE (CC) IS SET TO 10 (AN INVALID VALUE) AND THE CARRY BIT AND OVERFLOW BIT ARE CLEARED. FOR UNMASKED INTERRUPTS A PSW SWAP WILL OCCUR AND THE INCORRECT CONDITION CODE, CLEARED CARRY BIT, AND CLEARED OVERFLOW BIT WILL BE STORED IN THE OLD PSW. THIS CAN RESULT IN ERRONEOUS GPC OPERATION ONLY IF SUBSEQUENT PROCESSING UTILIZES THE OLD PSW'S CC, CARRY BIT, OR OVERFLOW BIT. A MASKED DMA STORE PROTECT INTERRUPT WILL SET THE CONDITION CODE (CC) TO 10 (AN INVALID VALUE) AND CLEAR THE CARRY AND OVERFLOW BITS ALL IN THE CURRENT PSW. THIS CAN RESULT IN ERRONEOUS GPC OPERATION IF AN INSTRUCTION TRIES TO UTILIZE THE CC, CARRY BIT, OR OVERFLOW BIT BEFORE THEY ARE SET BY ANOTHER GPC INSTRUCTION. FOR EXAMPLE, IF A MASKED DMA STORE PROTECT INTERRUPT OCCURS BETWEEN A LOAD INSTRUCTION THAT SETS THE CC AND A BRANCH INSTRUCTION THAT BRANCHES ON THE CC THE BRANCH WILL NEVER BE TAKEN REGARDLESS OF THE VALUE THAT THE CC WAS SET TO BY THE LOAD INSTRUCTION. ADDITIONALLY A MASKED DMA STORE PROTECT INTERRUPT CLEARS THE FIXED POINT OVERFLOW, FLOATING POINT UNDERFLOW, AND FLOATING POINT OVERFLOW BITS IN THE CURRENT PSW. THIS CAN RESULT IN A LOST INTERRUPT IF A MASKED DMA STORE PROTECT INTERRUPT OCCURS AND A SUBSEQUENT INSTRUCTION ISSUES ONE OF THESE ARITHMETIC INTERRUPTS. THE FOLLOWING IS A LIST OF ALL THE CPU CRASH INTERRUPTS: 1) CPU STORE PROTECT (CPU TRIES TO STORE TO A MEMORY LOCATION THAT IS STORE PROTECTED-PROGRAM CHECK INTERRUPT); 2) DMA STORE PROTECT (IOP TRIES TO STORE TO A MEMORY LOCATION THAT IS STORE PROTECTED-EXTERNAL 1 (OR LEVEL B) INTERRUPT); 3) POWER ON; 4) SYSTEM RESET; 5) IPL; 6) CPU MICROSTORE PARITY ERROR (MACHINE CHECK INTERRUPT); 7) INTERRUPT PAGE FAULT (MACHINE CHECK INTERRUPT); 8) CPU MULTI-BIT ERROR (MACHINE CHECK INTERRUPT); 9) DMA MULTI-BIT ERROR (MACHINE CHECK INTERRUPT); 10) EA FAULT (MACHINE CHECK INTERRUPT); 11) ENDOP TIME-OUT (MACHINE CHECK INTERRUPT); 12) CPU CANNOT CONTINUE (MACHINE CHECK INTERRUPT). POWER ON, SYSTEM RESET, AND IPL INTERRUPTS ARE NOT EXPOSED TO THIS PROBLEM. THESE INTERRUPTS DO ASSERT THE CPU CRASH SIGNAL THAT SETS THE CONDITION CODE TO 10 AND CLEARS THE CARRY BIT AND OVERFLOW BIT. HOWEVER EACH OF THESE INTERRUPTS RELOADS THE CC AND CARRY AND OVERFLOW BITS WHEN THEY PICK UP THE NEW PSW AND THEY DO NOT STORE CORRUPTED FIELDS INTO THE OLD PSW. CPU STORE PROTECT, ENDOP TIME-OUT, AND CPU CANNOT CONTINUE INTERRUPTS CANNOT BE MASKED. WHEN ONE OF THESE INTERRUPTS OCCUR THE CONDITION CODE (CC) IS SET TO 10 (AN INVALID VALUE) AND THE CARRY BIT AND OVERFLOW BIT ARE CLEARED. SINCE THE INTERRUPT IS UNMASKED, A PSW SWAP WILL OCCUR AND THE INCORRECT CONDITION CODE AND CLEARED CARRY BIT AND OVERFLOW BIT WILL BE STORED IN THE OLD PSW. THIS CAN RESULT IN ERRONEOUS GPC OPERATION ONLY IF SUBSEQUENT PROCESSING UTILIZES THE OLD PSW'S CC, CARRY BIT, OR OVERFLOW BIT. CPU MICROSTORE PARITY ERROR, INTERRUPT PAGE FAULT, CPU MULTI-BIT ERROR, DMA MULTI-BIT ERROR, AND EA FAULT INTERRUPTS CAN BE MASKED. WHEN THIS GROUP OF MACHINE CHECK INTERRUPTS IS MASKED THERE IS NO EXPOSURE TO THIS PROBLEM SINCE THE CPU CRASH SIGNAL IS NOT ASSERTED.</p>

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AD9959 (continued)	FSW	Mar 1994			<p>THIS IS BECAUSE THE INTERRUPT MICROCODE CHECKS TO SEE IF MACHINE CHECK INTERRUPTS ARE MASKED BEFORE BRANCHING DOWN THE CODE PATH THAT ASSERTS CPU CRASH. IF MACHINE CHECK INTERRUPTS ARE NOT MASKED AND ONE OF THESE INTERRUPTS OCCURS, THE CONDITION CODE (CC) IS SET TO 10 (AN INVALID VALUE) AND THE CARRY BIT AND OVERFLOW BIT ARE CLEARED. SINCE THE INTERRUPT IS UNMASKED A PSW SWAP WILL OCCUR AND THE INCORRECT CONDITION CODE AND CLEARED CARRY BIT AND OVERFLOW BIT WILL BE STORED IN THE OLD PSW. THIS CAN RESULT IN ERRONEOUS GPC OPERATION ONLY IF SUBSEQUENT PROCESSING UTILIZES THE OLD PSW'S CC, CARRY BIT, OR OVERFLOW BIT. WHEN A DMA STORE PROTECT INTERRUPT OCCURS THE CARRY BIT AND OVERFLOW BITS ARE CLEARED AND THE CC IS SET WHEN DMA STORE PROTECT INTERRUPTS ARE MASKED (SET IN THE CURRENT PSW) AND UNMASKED (SET IN THE OLD PSW DUE TO A PSW SWAP OCCURS). IF THE DMA STORE PROTECT INTERRUPT IS MASKED, THEN CPU CODE WILL CONTINUE TO EXECUTE AND EXPOSURE TO A PROBLEM WILL ONLY OCCUR IF AN INSTRUCTION THAT UTILIZES THE CC, CARRY BIT, OR OVERFLOW BIT IS EXECUTED BEFORE THESE STATUS BITS ARE SET BY ANOTHER INSTRUCTION. IF DMA STORE PROTECT INTERRUPTS ARE UNMASKED THEN A PSW SWAP WILL OCCUR AND THE INCORRECT CONDITION CODE AND CLEARED CARRY BIT AND OVERFLOW BIT WILL BE STORED IN THE OLD PSW. THIS WILL RESULT IN EXPOSURE TO THE PROBLEM IF SUBSEQUENT PROCESSING UTILIZES THE OLD PSW'S CC, CARRY BIT, OR OVERFLOW BIT. ADDITIONALLY A MASKED DMA STORE PROTECT CLEARS THE FIXED POINT OVERFLOW, FLOATING POINT UNDERFLOW, AND FLOATING POINT OVERFLOW BITS IN THE CURRENT PSW. THIS CAN RESULT IN A LOST INTERRUPT IF A MASKED DMA STORE PROTECT INTERRUPT OCCURS AND A SUBSEQUENT INSTRUCTION ISSUES ONE OF THESE ARITHMETIC INTERRUPTS. WHEN THE CPU CRASH SIGNAL IS ASSERTED THE CONDITION STATUS CONTROL REGISTER IS CLEARED. THIS REGISTER HOLDS 4 STATUS BITS THAT ARE CONVERTED INTO THE CARRY BIT AND CONDITION CODE BITS IN THE PSW. WHEN THIS REGISTER IS CLEARED THE CARRY BIT IS SET TO ZERO AND THE CONDITION CODE IS SET TO 10 (THIS IS NOT A VALID VALUE FOR THE CONDITION CODE). THE OVERFLOW BIT IS STORED IN ANOTHER LATCH THAT IS CLEARED WHEN CPU CRASH IS ASSERTED. EFFECTS ON GPC CODE EXECUTION BRANCHES NOT AFFECTED: BRANCH AND LINK; BRANCH AND INDEX; BRANCH ON COUNT; BRANCH ON COUNT BACKWARD. BRANCHES THAT DO NOT USE THE CC, CARRY BIT, OR OVERFLOW BIT ARE NOT AFFECTED BY THIS ISSUE. THE BRANCH AND LINK INSTRUCTION EXECUTES CORRECTLY BUT IF THE PROBLEM OCCURS THEN WHEN THE CURRENT PSW IS STORED INTO GENERAL REGISTER R1 IT WILL HAVE A CC EQUAL TO 10 AND CLEARED CARRY AND OVERFLOW BITS. BRANCHES THAT USE THE CC: BRANCH ON CONDITION; BRANCH ON CONDITION BACKWARD; BRANCH ON CONDITION (EXTENDED); BRANCH ON CONDITION FORWARD. SINCE THE CC IS SET TO THE INVALID VALUE OF 10 WHEN THIS PROBLEM OCCURS ANY BRANCHES THAT BRANCH ON THE CONDITION CODE WILL ALWAYS NOT BE TAKEN EXCEPT FOR UNCONDITIONAL BRANCHES WHICH WILL WORK CORRECTLY SINCE THEY DO NOT CHECK THE VALUE OF THE CC. BRANCHES THAT USE THE OVERFLOW AND CARRY BITS: BRANCH ON OVERFLOW AND CARRY; BRANCH ON OVERFLOW AND CARRY FORWARD.</p>

**GPC PRACA HISTORY RELATING TO STS-135 ANOMALY**

PRACA Report #	Vehicle	Flight/Mission	GPC S/N	Symptom	Attributed Cause
AD9959 (continued)	FSW	Mar 1994			SINCE THE CARRY BIT AND OVERFLOW BIT ARE CLEARED WHEN THIS PROBLEM OCCURS ANY BRANCH THAT BRANCHES ON THE OVERFLOW AND/OR CARRY BIT WILL MAKE THE BRANCH DETERMINATION BASED ON BOTH THE CARRY BIT AND OVERFLOW BIT BEING SET TO ZERO. THIS CLASS OF BRANCHES CAN BE CODED TO BRANCH ON VARIOUS COMBINATIONS OF THE OVERFLOW AND CARRY BITS BEING SET OR RESET. THEREFORE IF THE FAILURE OCCURS THE BRANCH MAY BE ERRONEOUSLY TAKEN OR NOT TAKEN DEPENDING ON HOW THE BRANCH INSTRUCTION WAS CODED. PASS NEVER INTENTIONALLY ISSUES THESE TYPES OF INTERRUPTS. THEY ARE EITHER THE RESULT OF A HARDWARE FAILURE OF A SOFTWARE CODING ERROR. FOR ALL OF THESE TYPES OF INTERRUPTS, WITH THE EXCEPTION OF A DMA STORE PROTECT INTERRUPT, THE PASS SOFTWARE RESPONSE IS TO IMMEDIATELY ENTER THE WAIT STATE OR TO IMMEDIATELY PASS CONTROL TO AN APPROPRIATE INTERRUPT HANDLER WITH NO ATTEMPT EVER BEING MADE TO RETURN CONTROL TO THE PSW ACTIVE AT THE TIME THE INTERRUPT OCCURRED. AS A RESULT, THERE IS NO POSSIBLE ADDITIONAL ADVERSE SIDE EFFECT FROM THE HARDWARE OPERATION IN THESE CASES. SOME PASS CODE DOES MASK THE DMA STORE PROTECT INTERRUPT AND IS THEREFORE EXPOSED TO THE HARDWARE DESIGN ERROR. THE EFFECTS WOULD BE DEPENDENT UPON THE INSTRUCTION SEQUENCE ACTIVE AT THE TIME THE INTERRUPT OCCURRED. WITH THE EXCEPTION OF A SOFTWARE CODING ERROR THE EFFECTS WOULD MOST LIKELY BE LIMITED TO A SINGLE GPC FAILING OUT OF THE SET. IT SHOULD BE NOTED THAT WHENEVER AN APPLICATIONS PROCESS IS EXITED PREMATURELY, THE REMAINING CODE IN THAT PROCESS WILL NOT BE EXECUTED, POSSIBLY RESULTING IN ERRONEOUS DOWNSTREAM PROCESSING AND/OR A FAIL TO SYNC WITH OR WITHOUT THIS HARDWARE ERROR. ANALYSIS OF THE BFS HAS CONCLUDED THAT THIS PROBLEM HAS NO ADVERSE EFFECTS ON THE PERFORMANCE OF THE BFS. BFS DOES INTENTIONALLY CAUSE SOME OF THESE INTERRUPTS. IN THESE CASES THE INTERRUPTS ARE ALWAYS UNMASKED AND THE OLD PSW IS NEVER USED, THEREFORE, THERE IS NO EXPOSURE TO THE HARDWARE DESIGN ERROR. GIVEN THE SPECIFIC INSTANCE OF AN INTERRUPT BEING CAUSED BY A FAILURE (EITHER HARDWARE OR SOFTWARE) THERE IS A MINUTELY INCREASED POSSIBILITY THAT BFS WILL NOT BE SUCCESSFUL IN THE RECOVERY (BSF RESTART) AT THIS POINT REGARDLESS OF THIS DESIGN ERROR BECAUSE BFD FAULT TOLERANCE REQUIREMENTS HAVE BEEN EXCEEDED. LESS THAN 1% OF THE BFS SOFTWARE IS EXPOSED TO A HARDWARE PROBLEM OF AN UNDEFINED (VERY REMOTE) PROBABILITY. THIS IM WAS DISCUSSED AT THE PRT HELD ON MARCH 17, 1994, AND THE DECISION WAS MADE TO CLOSE THIS AT THE "IM" LEVEL WITH NO FURTHER ACTION REQUIRED.
66RF21 STS-66-V-09	OV-104	STS-66 Nov 1994	524	DURING THE SM CHECKPOINT FROM GPC 4 TO MMU 1, I/O ERROR MMU 1 AND S60 CHECKPOINT FAIL ERROR MESSAGES WERE ANNUNCIATED. SUCCESSFUL TRANSACTIONS WERE PERFORMED BETWEEN GPC 1 AND MMU 1. ALL OPERATIONS WITH MMU 2 WERE NOMINAL	DEFECTIVE MIA PAGE, S/N 568, CONTAINING DEFECTIVE MDMIA, S/N 469. IT WAS DETERMINED THAT TRANSFORMER T2 OF MDMIA S/N 469 HAD AN OPEN AT PINS 1 & 2.
78RF03 STS-78-V-01	OV-102	STS-78 June 1996	533	AT 172:15:18:30 GMT. (GPC) 5 INPUT/OUTPUT (I/O) TERMINATE B DISCRETE BEGAN BEHAVING ERRACTICALLY.	UA - RESULTS OF THE FAILURE ANALYSIS INDICATE THAT THE "MOST PROBABLE" WOULD BE THE ASSOCIATED WIRE HARNESS OR CONNECTOR.
AD6739	SAIL	Feb 1990	005 Non-flt	GPC IN #1 SLOT FAILED TO SYNC IN SAIL/GTS. GPC FAILED SYNC WHEN BROUGHT BACK TO OPS 901 REDUNDANT SET.	IBM, AT HOUSTON, VERIFIED THE FAILURE & ISOLATED IT TO A RAM IC, P/N 6135011-2, WHICH WAS REMOVED FROM THE CPU A (CA) PAGE, P/N 6966064. IBM VERIFIED THAT THE GPC WAS SPENDING AN ABNORMALLY LONG PERIOD OF TIME EXECUTING A LOOP OF CODE, THEREBY CAUSING IT TO FAIL TO SYNC, SEE ATTACHED DR CLOSEOUT STATEMENT. FAILURE ANALYSIS WAS NOT PERFORMED ON THIS IC SINCE IT WAS BOUGHT TO AVIONICS SPEC & NOT TO THE HIGH-REL STDS OF OTHER PARTS BOUGHT FOR PRODUCTION UNITS. NASA, BELIEVED THAT THE IC WOULD BE HELD IN BONDED STORAGE FOR FUTURE ANALYSIS, SHOULD A TREND BE INDICATED, HOWEVER DUE TO A MISUNDERSTANDING THE BAD PART WAS INADVERTENTLY DISCARDED. THE TEST ENGINEER CONFIRMED THAT THE PART OUTPUT WAS INCORRECT WITH A PROPER INPUT SIGNAL ON THE BOARD. THIS PARTICULAR IC FAILURE MECHANISM MAY NOT HAVE BEEN CAUGHT DURING ATP SINCE THIS FAILURE MODE WOULD ONLY SHOW UP DURING TESTING OF THE GPC IN A REDUNDANT SET.

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AE2723		May 2004	519	During incoming functional testing, an error occurred while running the room temperature portion of Functional Test Procedure (FTP), the error observed was a failed Memory Test 9, Part 2, with Single Bit ECC errors indicated. The failure was isolated to a discrepant 4-bit counter (IC U44 Pin 11, P/N 102A450-1, lot date code 8622) on the A21 CMOS Page Assembly (Lower memory - P/N 6966070-23, S/N 539).	When the EDAC encounters a single bit error it will correct the error and increment the Single Event Upset (SEU) counter. The FTP then verifies that SEU counter has incremented properly (equal to the number of injected single bit errors). The Single Bit ECC errors indicated that the GPC was not passing this FTP memory test. The error data indicated that the single bit errors injected in the even and odd addresses of sector 2 (address range 1000016 ? 17FFF16) were all failing to scrub properly. The failure was then further isolated to a defective output of a 4 bit counter (IC U44 Pin 11, p/n 102A450-1, date code 8622) on the A21 CMOS Page Assy. (lower memory), P/N 6966070-23, S/N 539. When this 4 bit counter failed, it resulted in a defective Scrub Counter Address and caused the EDAC to skip addresses in sector 2 (1000016 ? 17FFF16). Since the EDAC was skipping these addresses, it was not able to detect and correct bit errors in this sector and hence the SEU counter was not incremented to the expected value. The 4 bit counter IC was replaced and successfully retested, confirming that it was the root cause of the FTP Single Bit ECC errors.