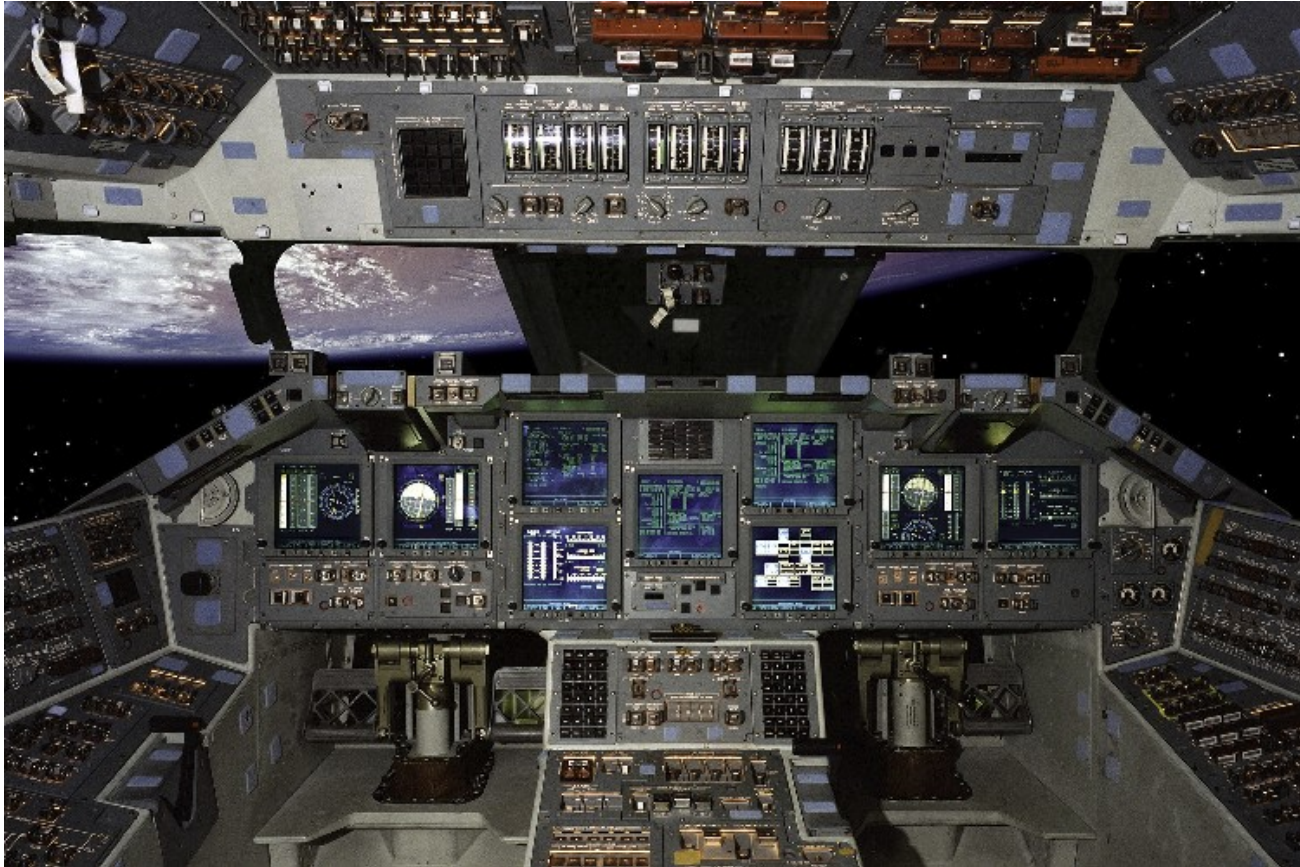


Space Shuttle Cockpit Avionics Upgrade

COTS Content in a Critical Manned Space Application



September 08, 2004

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United Space Alliance LLC**

CAU Operational Objective



To increase situational awareness and reduce cockpit workload resulting in the execution of more accurate and timely decisions

note: crew error reportedly responsible for the majority of civil and military aeronautical accidents

CAU Project Background

The Shuttle has complex flight regimes:

- Launch rocket for approximately 9 minutes
- Orbital spacecraft for 10-14 days
- Hypersonic plane for an hour
- Subsonic glider about 5 minutes

Large operational flight envelope is further complicated by an extremely large set of monitoring tasks and procedures over 10 major subsystems

- Propulsion, Guidance & Navigation, Flight Control, Hydraulics
- Power, Thermal, Environmental
- Data Processing, Communications
- Payloads

NASA chooses the “Best of the Best” for its astronauts

- Experienced test pilots with thousands of hours in 40+ aircraft

Minimum time required to train a shuttle pilot is 2-3 years!

- See backup charts pp. 36, 37 for overview of Shuttle workload & task complexity

Need for Improved Situational Awareness

- Situational Awareness (SA) is an understanding of the state of the environment
 - It provides the PRIMARY basis for subsequent decision making and performance in the operation of complex, dynamic systems

- What detracts from situational awareness?
 - Too much data
 - Too little time
 - Lack of information
 - High workload
 - Malfunctions
 - Environmental distractions (noise, vibration, visibility, etc.)

- What are the consequences when these come together?

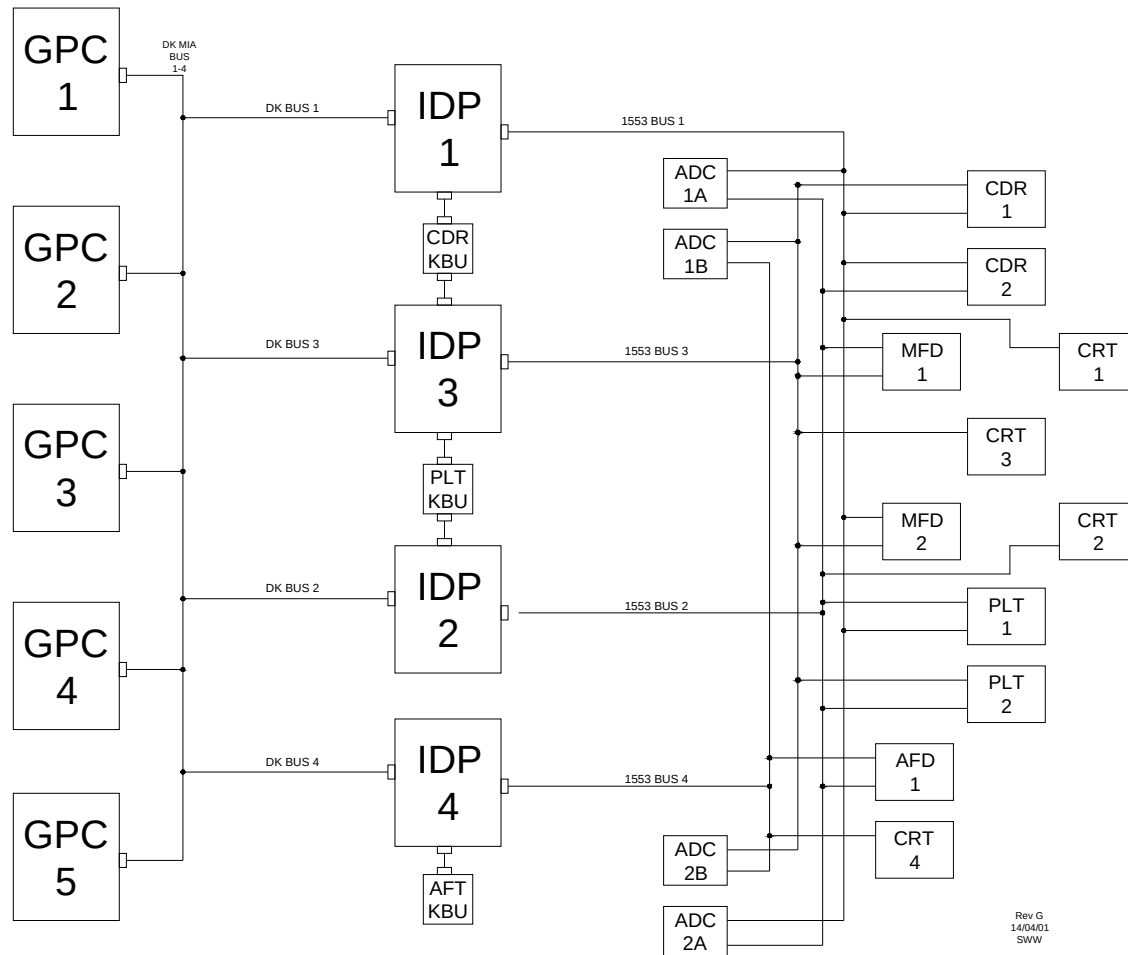
Errors can be, and are, made

- Display navigation/command inputs
- Problem diagnosis and resolution

Current Shuttle Display Architecture

- 5X legacy General Purpose Computers (GPCs) perform redundant flight control, systems management, and display processing
- 4X legacy Integrated Display Processors (IDPs) perform text & graphics generation out to MDUs, keyboard I/O back to GPCs
 - IDPs operate 100% independently from each other
 - Each IDP's span to cockpit displays is limited by bus architecture
- 11X legacy Multi-Function Display Units (MDUs) are 7-inch backlit LCD displays
 - 7 MDUs have 2X 1553 ports, mapped to two different IDPs
 - An IDP failure allows any of these 7 MDUs to switch to another IDP, but display continuity is lost as a result
 - Remaining 4 MDUs are “dedicated” to an IDP, and do not have redundant ports
- 4X legacy Analog-to-Digital Converters (ADCs) gather legacy sensor data for display

Current Shuttle Display Architecture



Key CAU Design Requirements

- New displays shall provide both information and command path required to affect necessary change
 - Composite displays shall present information from multiple data sources and multiple subsystems
 - Logically arranged on single displays for streamlined cockpit operation
 - Crew shall not be required to toggle between displays to gather information and take action
- Graphics performance (detail, rate, human factors) shall meet or exceed existing MEDS capabilities
- System shall be symmetric and modeless for critical operations
 - Any display image is available on any of eleven (nine forward) physical displays
 - Any keyboard is assignable to any display
- System shall remain symmetric and modeless after 1st failure
 - After any single failure, cockpit looks and works the same as in normal operation
 - Cockpit is fully functional after any two failures, with minor manual reconfiguration
- See backup charts pp. 38-47 for examples & summary of CAU human factors improvements

Design / Implementation Approach

- Use COTS hardware and software to provide required system performance and development efficiency
 - Survey of MIL & Space processor hardware showed a performance shortfall of 1 to 2 orders of magnitude
- Employ COTS hardware technology where feasible
 - Processor, RAM, Flash, backplane standards, non-critical interfaces, test interfaces
- Employ MIL / MOTS / Custom / Radiation-Hardened technology where necessary
 - Critical I/O interfaces, Gate Arrays (majority of custom logic)
- Use sound design mitigation techniques to select and adapt COTS to space environment
 - Hardware-based error detection & correction
 - Software-based correction (i-cache) or trapping (d-cache) of COTS processor cache upsets
 - Exhaustive radiation test of COTS components, with strict pass / fail criteria
- Use & Enhance legacy Shuttle FDIR (Fault Detection Isolation and Recovery) capabilities
 - GPC rejection of erroneous command inputs (syntax and content vs. current ops mode)
 - GPC-generated test patterns for interface health monitoring
- Modify legacy architecture as necessary to meet unique user requirements
 - Cross-Strapping of Command (DK Bus) and Display (1553 Bus) interfaces
- Ensure FO / FS (Fail OP / Fail Safe) Guidelines in effect at all stages of design
 - System redundancy, power distribution, nominal command & display bus distribution vs. nominal cockpit operations, rigorous analysis of failure scenarios
- See backup charts pp. 33-35 for Data Pollution Prevention overview

FPGA Specific Implementation Approach

- Xilinx for prototyping, convergence of requirements & design
 - Note that the MIL hardware which is the design basis for much of CAU flies with Xilinx, so large portions of our prototype hardware was truly “off the shelf”
- Actel Commercial for Ground-use avionics hardware
 - NASA manned space programs have non-flight hardware for verification & training labs that outnumbered flight hardware boxes ~2:1
 - Majority of run time (~100:1) is accumulated on ground hardware, so “design similarity” to flight hardware (functional & performance @ bit level) is critical for accumulation of valid hardware design shelf life, software development & formal verification credit
- Actel Rad Tolerant for Flight avionics hardware
 - Reserve highest cost components for actual flight hardware
 - Based on the assumption (with proof required !) that the Rad Tolerant implementation is easily ported from, and “works like” the Commercial equivalent parts
 - Design similarity of ground vs. flight hardware is ensured by screening logic designs against Commercial and Rad Tolerant FPGA timing constraints at each design iteration

CAU System Content

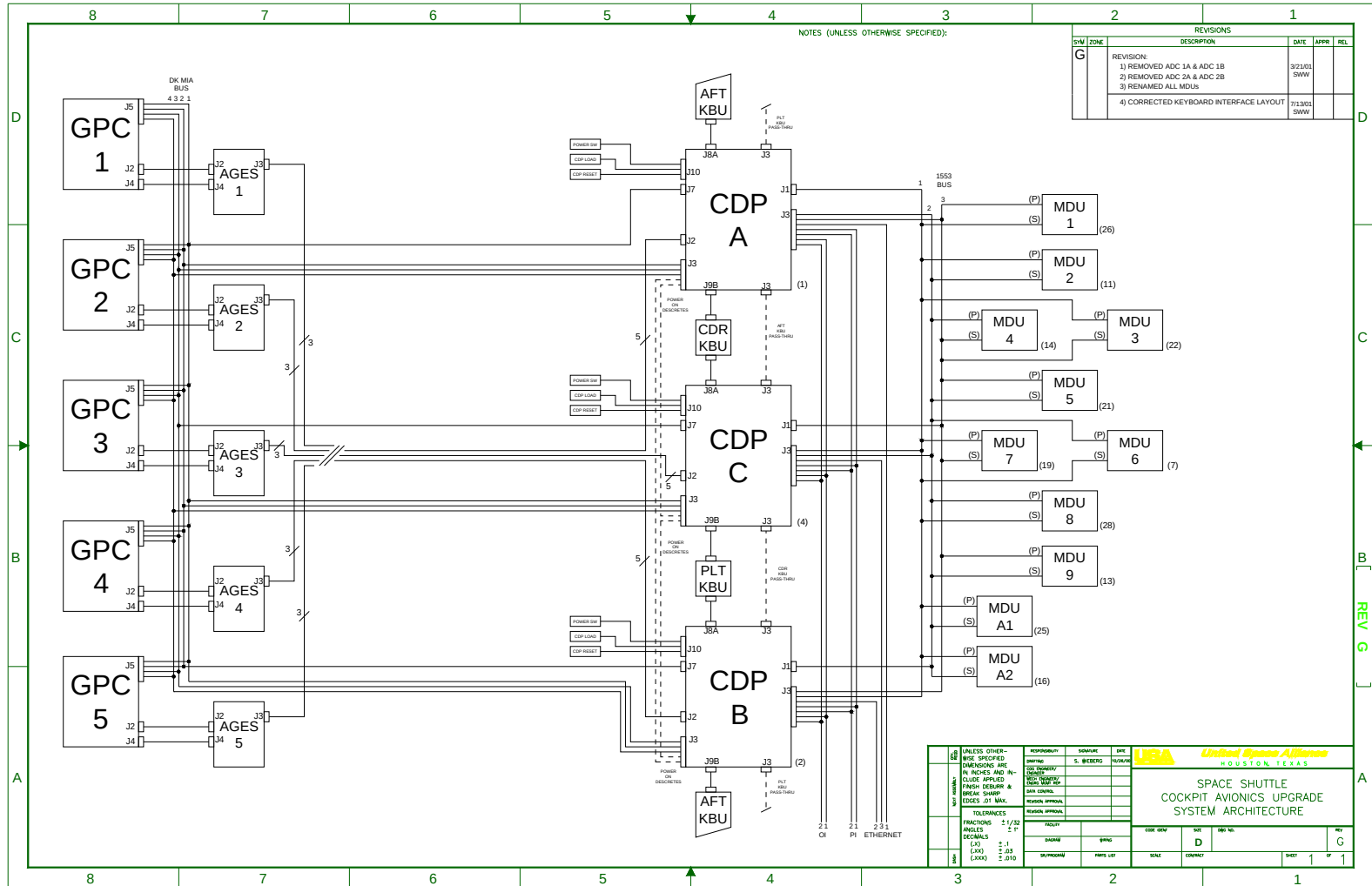


- **New CAU Software Applications Enable Cockpit Safety Goals**
 - Shuttle Abort Flight Management (SAFM)
 - Graphically shows Abort Opportunities based on current vehicle energy and configuration during Critical Mission Phases
 - New Display layout and navigation scheme
 - Enhanced Caution & Warning (ECW) (Full ECW not currently funded, but baseline system achieves many of the ECW objectives)
 - Uses graphics and text to show Configuration, Faults and Fault History of Shuttle Systems
 - Onboard Systems & Flight Dynamics Monitoring equal or superior to Mission Control
- **New CAU Hardware hosts New CAU Software Applications**
 - Command & Display Processor (CDP)
 - Three new CDP boxes replace four existing MEDS Integrated Display Processors (IDPs), with significantly more processing power and enhanced connectivity to Shuttle Vehicle Data
 - ~1000 X as powerful as Shuttle flight control General Purpose Computers (GPCs)
 - General Purpose Computer (GPC) Avionics Ground Equipment interface Serializer (AGES)
 - Five new AGES boxes capture all memory data from the five existing GPCs, and forward that data to the CDPs, giving the CAU system full insight into existing Flight Software data and processes
- **The CAU project will use pieces of the Multi-Functional Electronics Display System (MEDS)**
 - Integrated Data Processors will be replaced with Command and Display Processors (CDPs)
 - Multi-function Display Units (MDUs) will be retained

Cockpit Avionics Upgrade Architecture

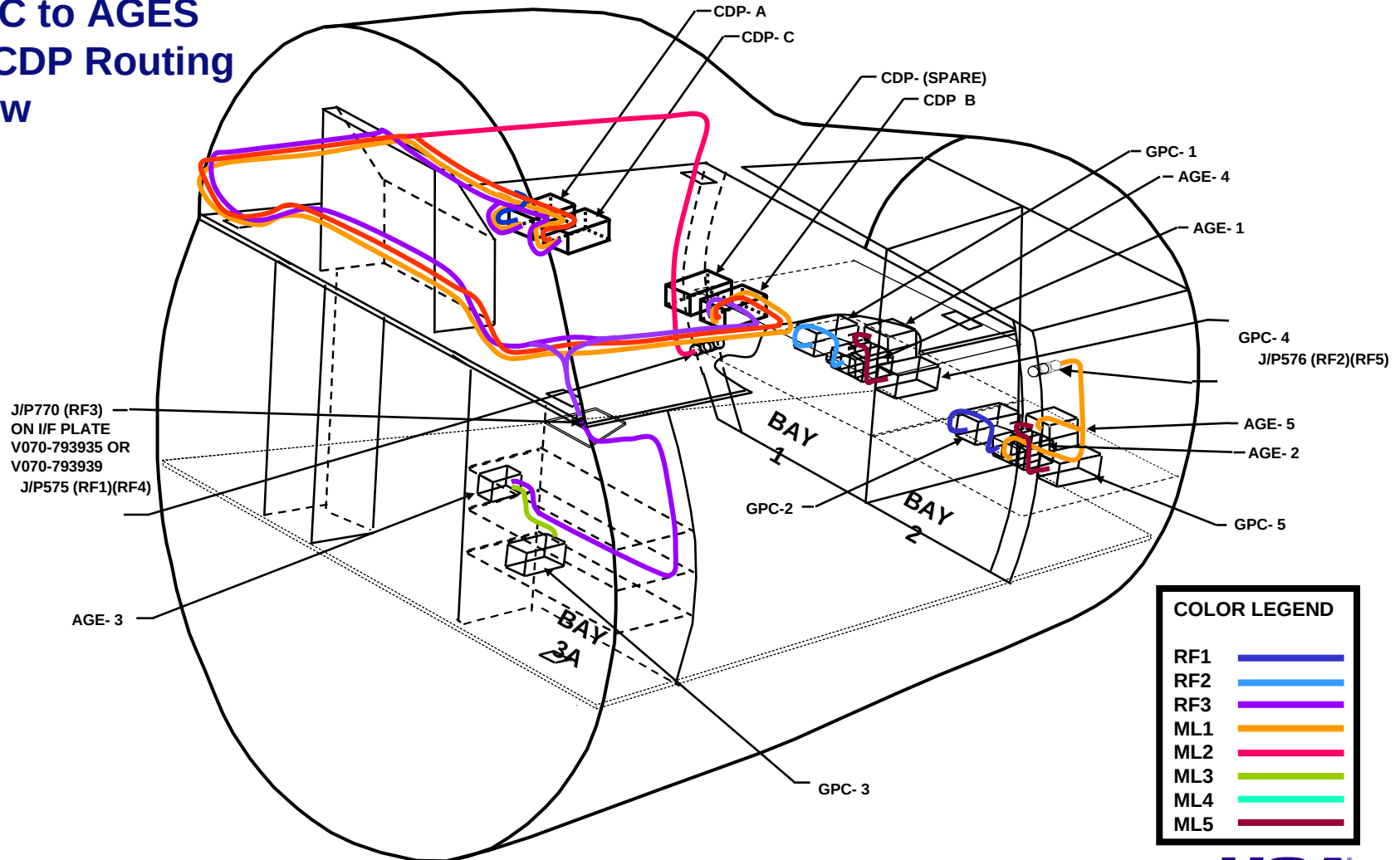
- 5X legacy General Purpose Computers (GPCs) perform redundant flight control, systems management (*but not display processing*)
 - Display processing software has been excised from GPC Flight Software
- 5X new Avionics Ground Equipment Interface Serializers (AGES) units act as Reflective Memory encoders & transmitters per GPC
 - Xceivers plus one FPGA – no RAM, no software, no firmware
- 3X new Command and Display Processors (CDPs) perform graphics generation out to MDUs, keyboard I/O back to GPCs
 - CDPs operate *cooperatively and redundantly*, and are “aware” of each other’s tasks
 - Each CDP’s span to cockpit displays is *not* limited by bus architecture
- 11X legacy Multi-Function Display Units (MDUs) are 7-inch backlit LCD displays
 - *All* MDUs have 2X 1553 ports, mapped to all CDPs
 - A CDP failure allows *any* of the 11 MDUs to switch to another CDP, and display continuity is *maintained*

CAU Hardware Architecture

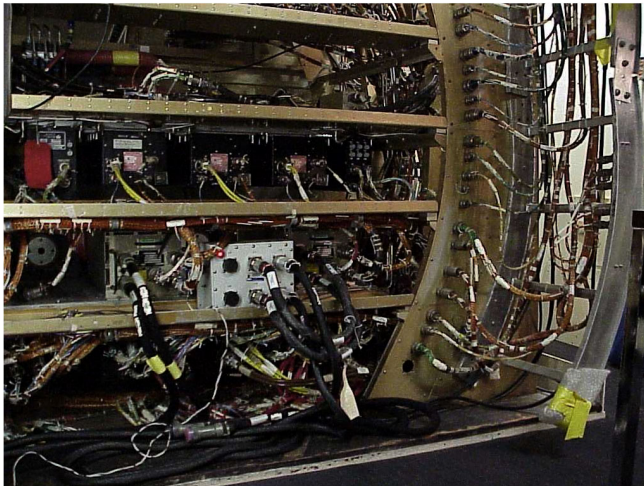
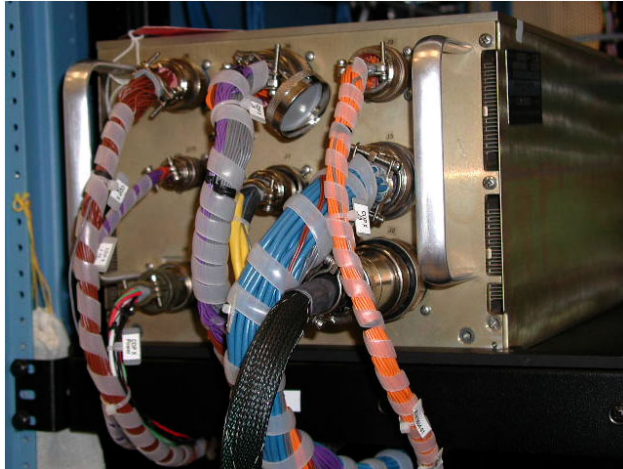


Vehicle Modification Kit

GPC to AGES to CDP Routing View



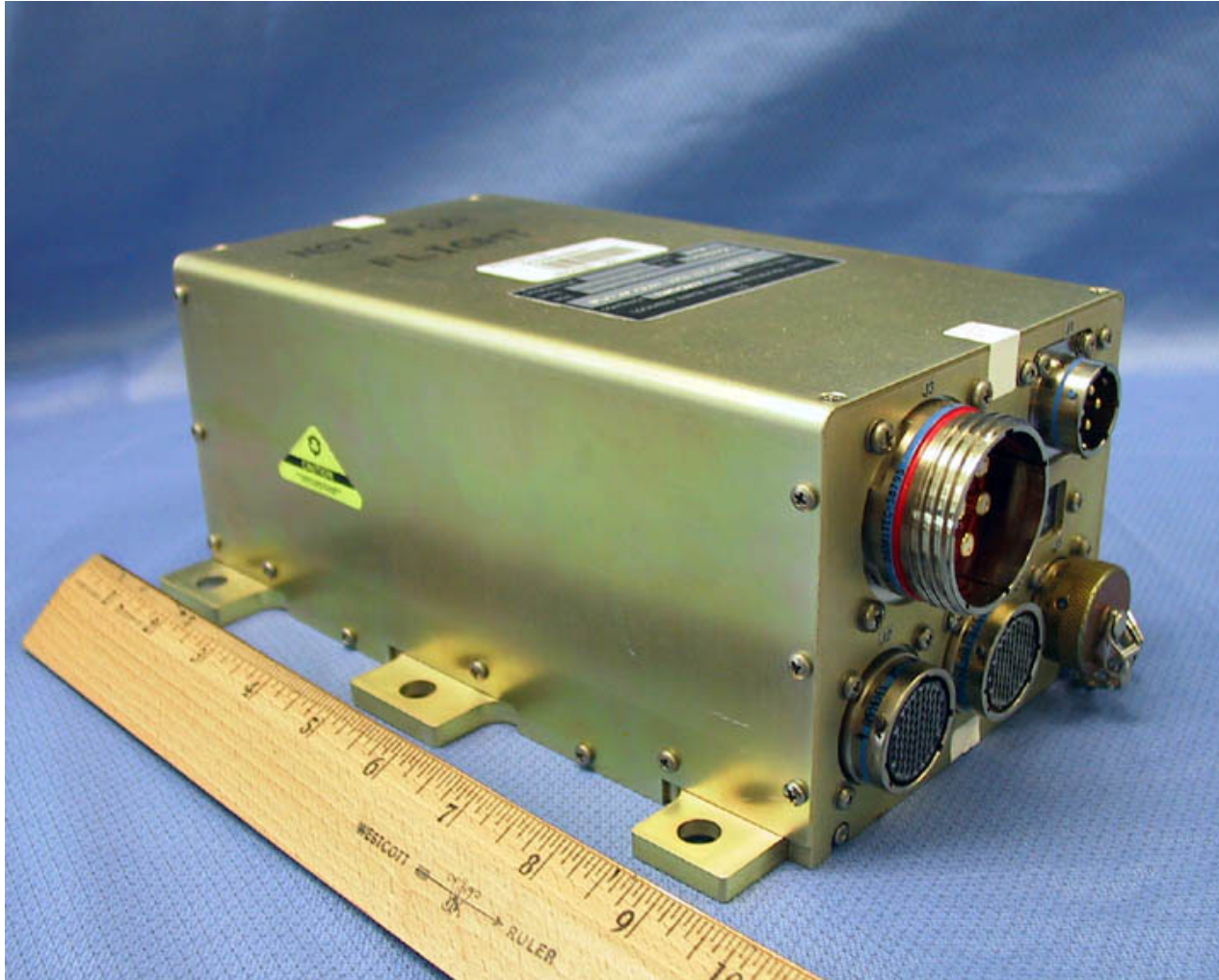
Representative Installation Views



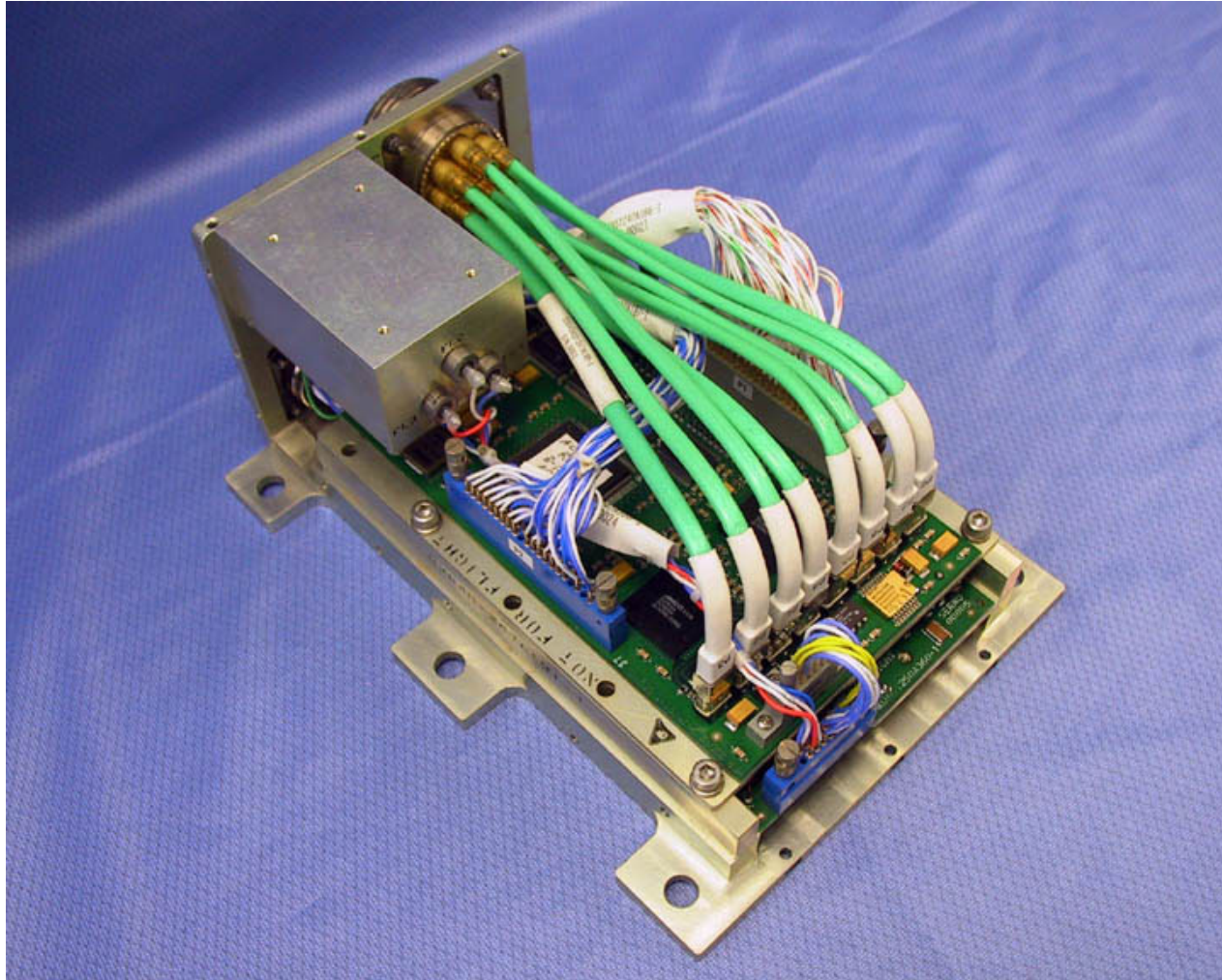
New CAU Hardware – AGES

- **AGES – Avionics Ground Equipment Serializer – custom reflective memory adapter**
 - AGES ties legacy Flight Control and Systems Management GPCs to new CAU System by duplicating memory contents of the 5 GPCs in EACH of the three CDPs, in real time
 - AGES implemented (one per GPC) as a small, lightweight, low power (<10W) data serializer, to eliminate long, heavy runs of parallel data cable
- **AGES tracks parallel data on GPC memory bus via a GPC factory diagnostic interface (currently unused in flight)**
 - AGES error-checks GPC interface, then streams each GPC memory transaction via Fibre Channel (FC physical level, custom 10 character protocol) serial bus to each of three CDPs, where GPC memory images are reconstructed in real time
 - AGES sends GPC data @ 531 Mbps over 60' twinax copper FC media, Bit Error Rate requirement allocation < 1E-19 (FC BER spec is < 1E-12), open loop, no retry on error
 - Ultra high quality wiring & connectors, custom Reed-Solomon forward error correction encoding / decoding hardware to meet E-19 BER requirement using a 1E-12 BER (COTS) physical link
- **CDP Software can now read all legacy GPC parameters directly from reconstructed GPC memory images sent by AGES, with ZERO GPC overhead**
- **AGES can be considered as an extension of the GPC for both operations and fault-management purposes**

AGES Photo



AGES Photo – Cover Removed



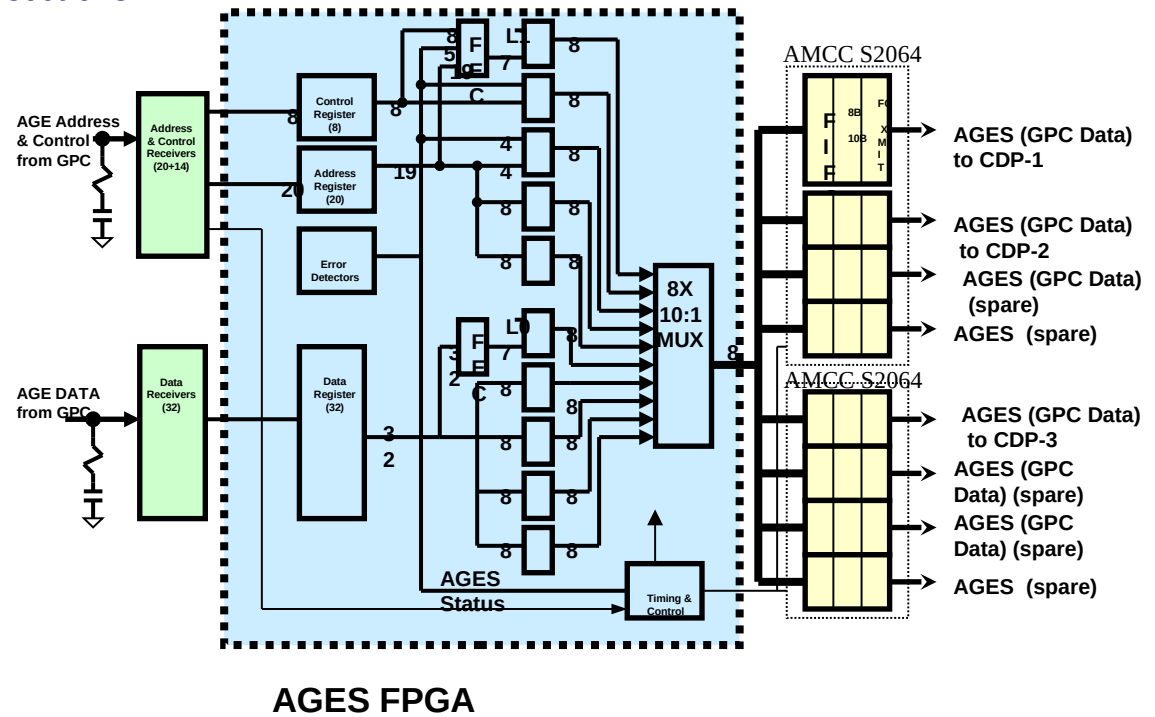
AGES AGE Capture Module (ACM)

■ The AGES AGE Capture Module:

- Captures information appearing on the GPC parallel AGE interface
- Interprets this information for valid or abnormal operations and status conditions
- Transmits this information to the CDP via a serial Fibre Channel interface

■ The ACM has three major logic sections:

- AGE interface receivers
- An FPGA for data capture, timing and control
- Fibre Channel transmitters



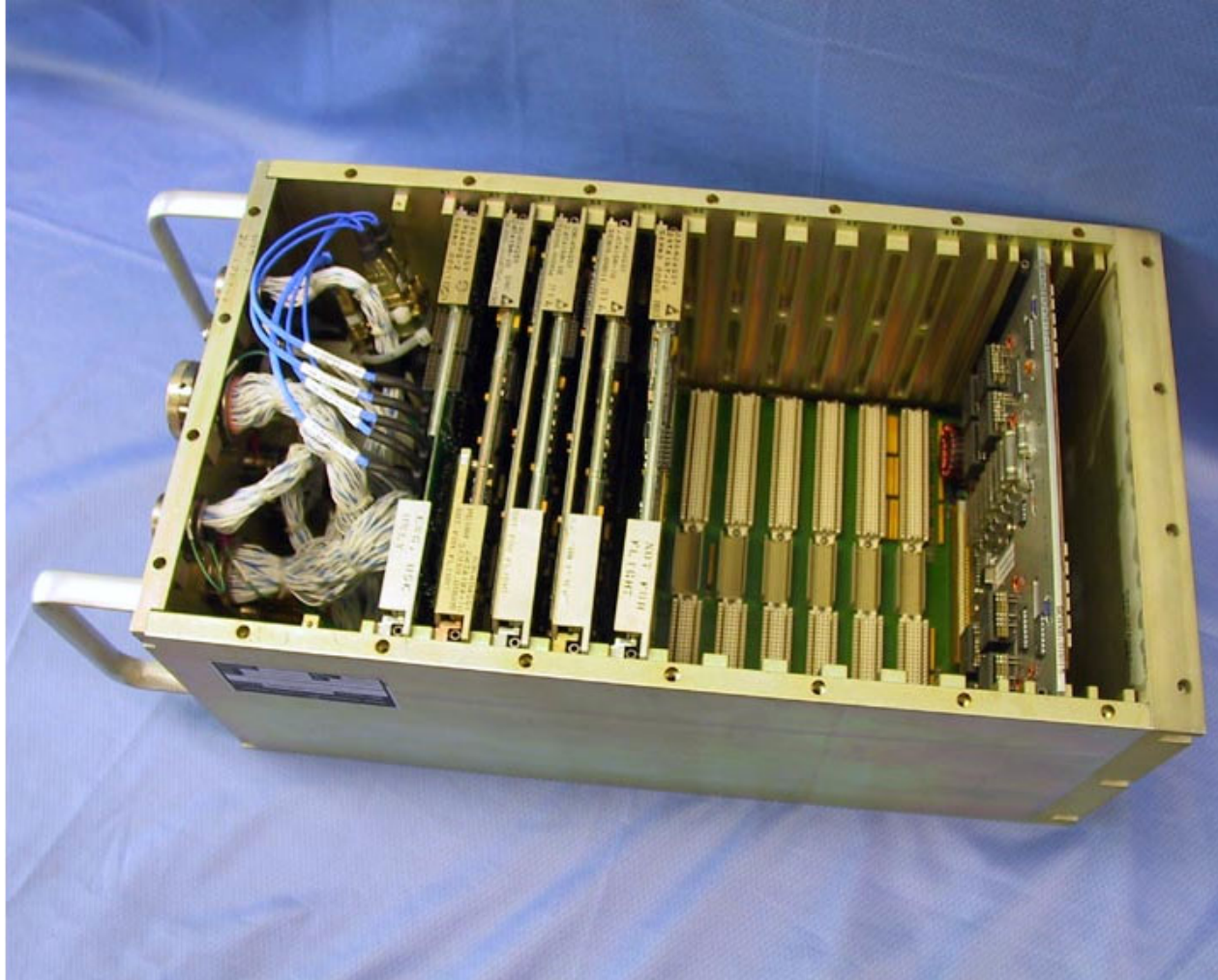
New CAU Hardware – CDP

- **CDP – Command and Display Processor**
 - CDP (CAU) replaces legacy DEU (MCDS) or IDP (MEDS)
 - General Purpose CPU (Motorola 7455) for OS and Apps (Displays, Commanding, SAFM, ECW)
 - Dedicated radiation-tolerant channel processors for 1553 (COTS) and MIA (Custom) interfaces
 - Discrete I/O for Power, Reset, Mode and Panel Indicator control
- **Receives, checks and processes GPC memory contents from 5 AGES units**
 - CDP Software can now read all legacy GPC parameters directly from reconstructed GPC memory images sent by AGES, with ZERO GPC overhead
- **Receives Crew Keyboard inputs**
- **Sends MDU Display Outputs, GPC Command Outputs**

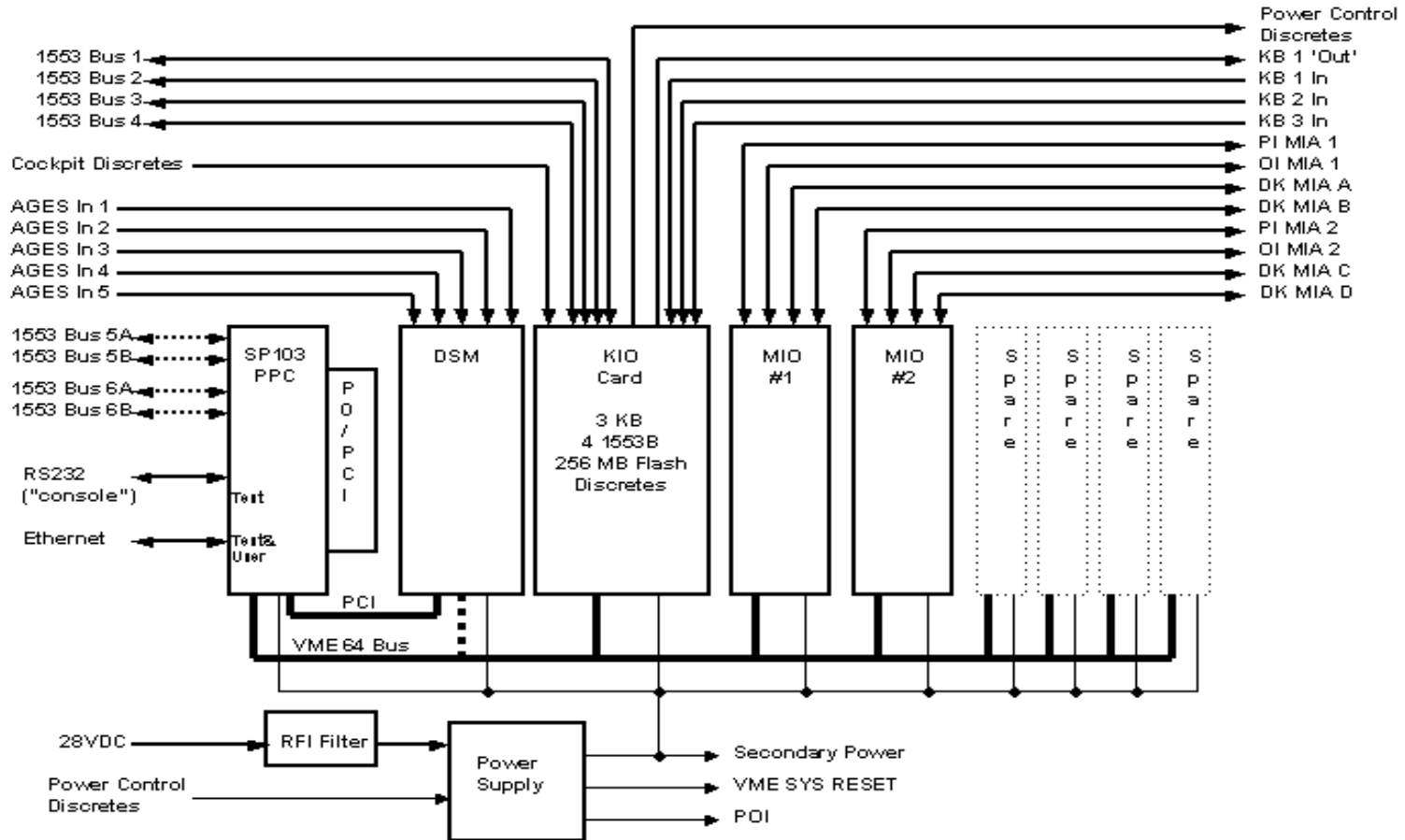
CDP Photo



CDP Photo – Cover Removed



CDP Internal Design



CDP Deserializer Module – DSM

■ AGES Interface

- 531 Mbaud interface
- Modified Reed-Solomon Forward Error Correction

■ FIFO Interface

- Original design used 128K deep FIFO (≈ 28 msec @ 250 ns max GPC data rate)
- 32K deep FIFO adopted to replace 128K deep FIFO due to more favorable radiation characteristics, still with adequate performance margin
- ECC (“Modified Hamming Code”) – correct any one, detect any two bits in error

■ SRAM Interface

- ARM 512K x 16 bits x 5 channels
 - Holds real-time contents of memories of all 5 GPCs
- Event RAM 512K x 16 bits x 5 channels
 - Holds programmable triggers that signal CDP of selected GPC software events
 - Used to synchronize the CDP software with GPC software
- Both with ECC (“Modified Hamming Code”) – correct any one, detect any two bits in error

■ PCI Bus Interface

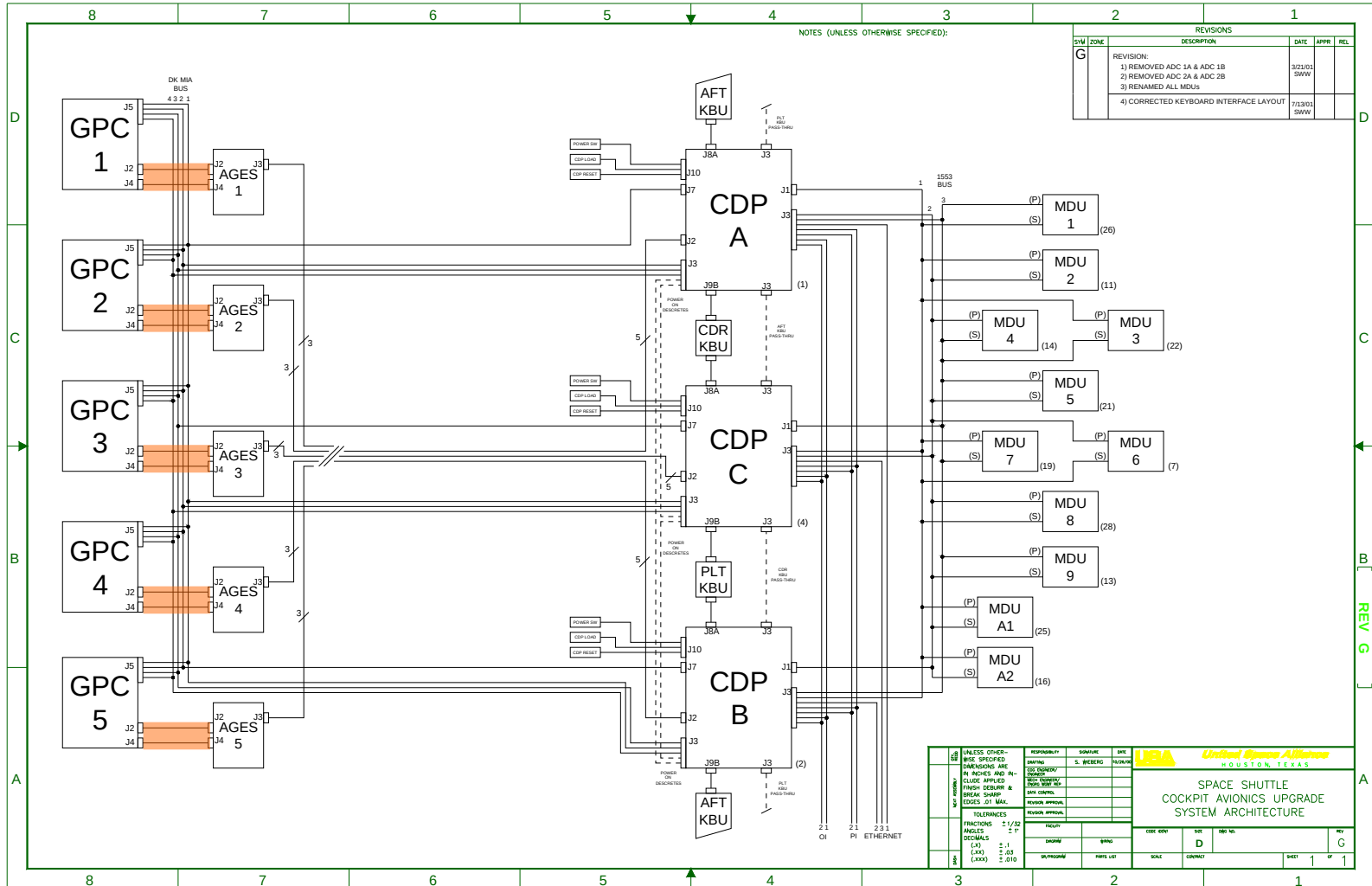
■ Built In Test (BIT) Features

- Data Wrap
- Forced Single Bit Error / Multi Bit Error at every stage
- BIT features enabled only via two or more dissimilar software actions, to prevent inadvertent activation during normal operation

Memory Technologies & Mitigations

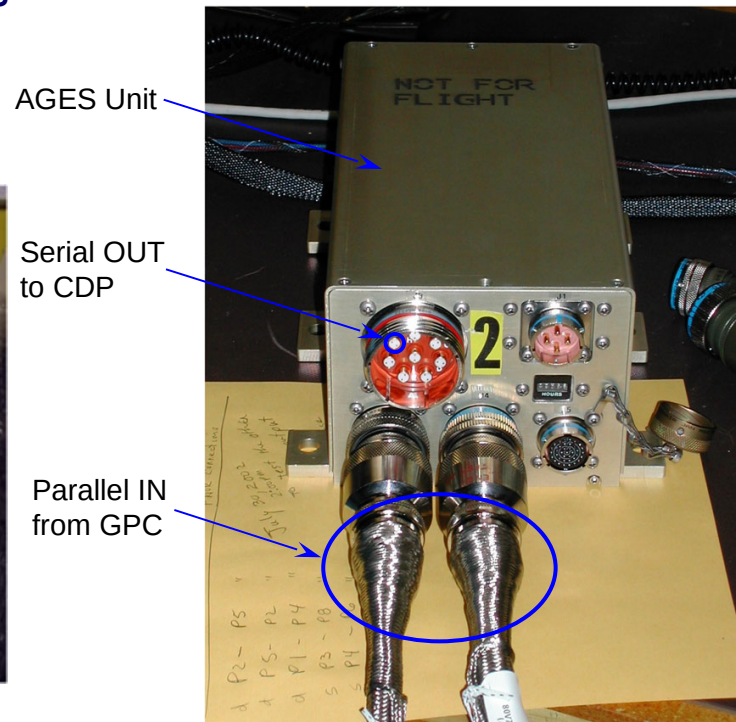
- EEPROM – holds boot configuration parameters & hardware error logs
 - Controlled by FPGA outputs (potential glitch issue), but device has write-protect “cipher” mechanism (managed in device driver software) to prevent stray writes during transients
 - Minor exposure to corruption if in writable mode during power failure
 - Exposure exists for a few tens or hundreds of milliseconds per Shuttle Mission
- Flash – holds boot code on processor card and I/O channel cards, holds applications and logs on secondary VME card operating under True Flash File System (TFFS)
 - Redundant Kernel images, redundant application file partitions
 - but non-redundant COTS boot loader – at least it’s small...
 - Radiation testing led to selection of a different component, and the addition of a software-managed RESET function
 - Software RESET is OR’d with Power-On / Off Reset at each Flash component
 - 7X improvement in radiation performance while held reset
- SDRAM – main processor memory
 - 512M x 4 bit, 4-bit error detection, 1-bit error correction, via COTS memory controller
 - Hardware-initiated background cyclic scrub (rewrite) of single bits in error

Legacy GPC Test Port (Mem Addr, Data, Cntl)

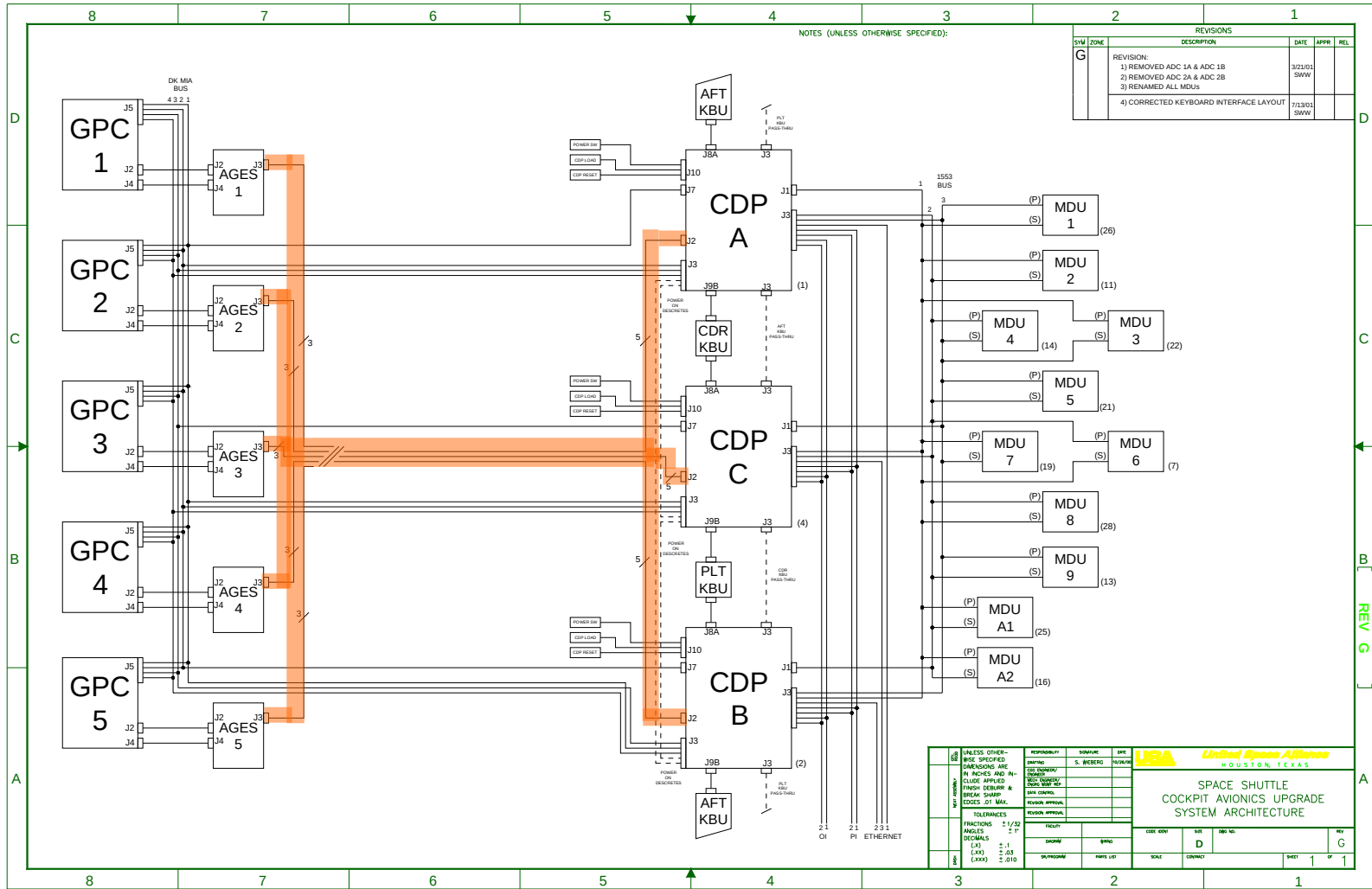


CAU Interfaces – External – GPC AGE

- GPC AGE to AGES cables are short (<3 ft.) high conductor count (parallel bus), internally shielded, with outer overbraid
- 2 cables connect each GPC to the associated AGES
- 10 cables total per vehicle - 2 per GPC / AGES
- Cable design is very robust against EMI / RFI
- GPC interface design, conductor count and resulting bulk of the cables makes them unsuitable for long, multipoint runs to CDPs
- AGES unit is designed specifically to take the parallel data from each GPC and convert it to serial for more efficient multipoint distribution



CAU Interfaces – Internal – High-Speed Serial



CAU Interfaces – Internal – High-Speed Serial

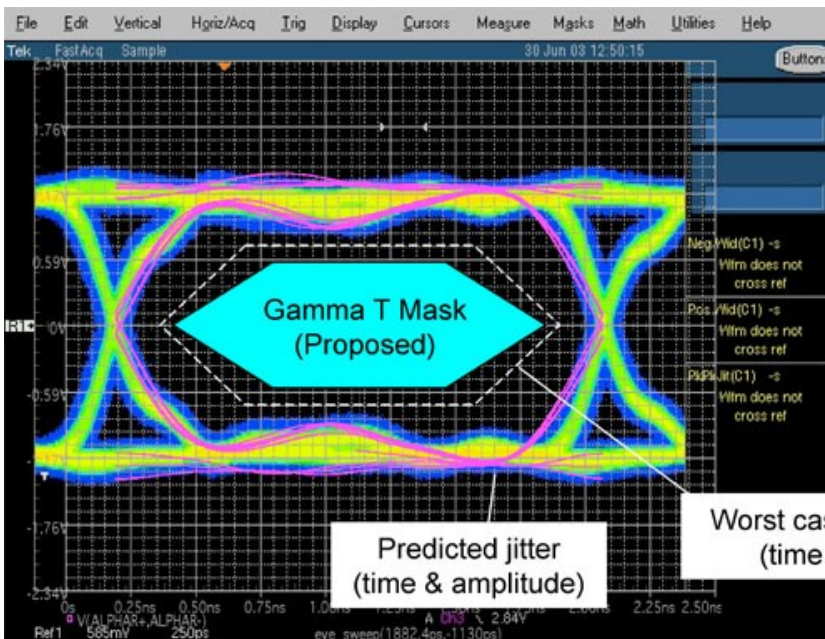
High-Speed Serial Link Design

- Point-to-point from each AGES to each CDP
- Uses COTS Fibre Channel transceiver components
- 1E-19 Bit Error Rate (BER) allocation keeps link errors below 10% of intrinsic CAU hardware failure rate
- Native Fibre Channel spec 1E-12 BER requires 1E-7 BER improvement for use in CAU

- Reed-Solomon code corrects any one character in error (1 to 10 bits in error) per 10 character data packet on serial link
- Assuming random distribution of bits in error, design produces 4.5E-21 BER
 - Correction code offers 4.5E-9 improvement factor over the spec'd 1E-12 interface BER
- Lab & Model evaluation of CAU implementation indicates that UNCORRECTED link meets 1E-19 requirement (see at left and below)

High-Speed Serial Link Model vs. Actual

- Model predictions in Pink
- Remaining trace is measured data
- Outer mask is worst-case noise prediction
- Inner mask is exclusion zone for 1E-19 BER without correction code – uncorrected physical design exceeds CAU system requirements !
- Reed-Solomon ECC improves link BER by 4.5E-16 factor: System BER < 4.5E-35 !
 - Link MTBF = 1.2E24 hours = 1.3E20 years
 - System 15-Link MTBF = 8.8E18 years
 - (Age of Universe is 1.4E10 years...)
- Conclusion: CAU High-Speed Serial Interface is ~immune to noise, thermal & jitter effects



The Rest of the Story...

- Preceding analysis is valid for the superposition of all known thermal & electrical noise contributions to Bit Error Rate (BER), but...
- Recent radiation testing of COTS Fibre Channel Interface chipset revealed a failure mode that does NOT map to the design assumptions on the previous page !
- Inadequate fidelity of initial COTS component test allowed the escape, caught (late) in system-level test
 - In addition to expected bit inversions, we occasionally see single MISSING or EXTRA bits, which cause loss of correct data sync until the next sync character (channel resyncs only between whole message packets)
 - Causes ALL data characters within a data packet after the initial error to be garbled, which sometimes exceeds the error-correction capability of the FPGA-based custom Reed Solomon (RS) error correction scheme
- Since links are ~redundant at the system level, we prefer to lose a link rather than accept bad data
- Fix (actually a statistical mitigation, not a fix) is a design tweak to the FPGAs on either end of the link:
 - Transmitter - send less data, more idle (sync) characters, by eliminating “unimportant” GPC data
 - Receiver – DO NOT fail the link in response to garbled sync characters that are bracketed by good sync characters
 - Receiver - deterministically FAIL the link, rather than attempt to correct detected sync errors and “codeword violations” (morphing of data characters into control characters)
- Result is a 5X improvement in radiation tolerance, and no known way to induce xfer of erroneous data
 - Link reliability still meets top-level system requirements, but is now somewhat lower than “age of the universe”
- Predict one serial link radiation upset every 2560 days
 - Was one upset every 482 days prior to design tweak
- “Do-Over” (big redesign) would perhaps interleave individual data and sync characters, isolating each erroneous data character from other data characters, preserving the RS error correction capability
 - Cost, schedule and (perhaps) performance prohibitive, not required for adequate radiation tolerance

Lessons Heeded ✓ Lessons Learned □

- ✓ Test non-pedigree components as early as possible
- Test non-pedigree components in a manner that is as high-fidelity as possible vs. your intended design application
- Conduct rigorous comparison between your test pass / fail criteria and any assumptions you make about component behavior, both specified and unspecified
- ✓ DO NOT assume that all logic features & functions within a component have similar radiation sensitivity
- ✓ Exercise all the component features you intend to use, at realistic duty cycles, during component test
- Iterate component test (spiral development!) as design application detail is revealed or modified
- ✓ Confirm component test results (and extrapolations!) via system-level test
- ❖ Downside – all this is expensive and takes a long time, but it's a bargain compared to a failed project

CAU Project Status & Accomplishments

■ Software

- Ten major software builds complete
- Data Management
- GPC commanding & state tracking
- 1553 & DK bus management
- Keyboard input
- 120+ new displays
- Shuttle Abort Flight Management (SAFM)

■ Hardware

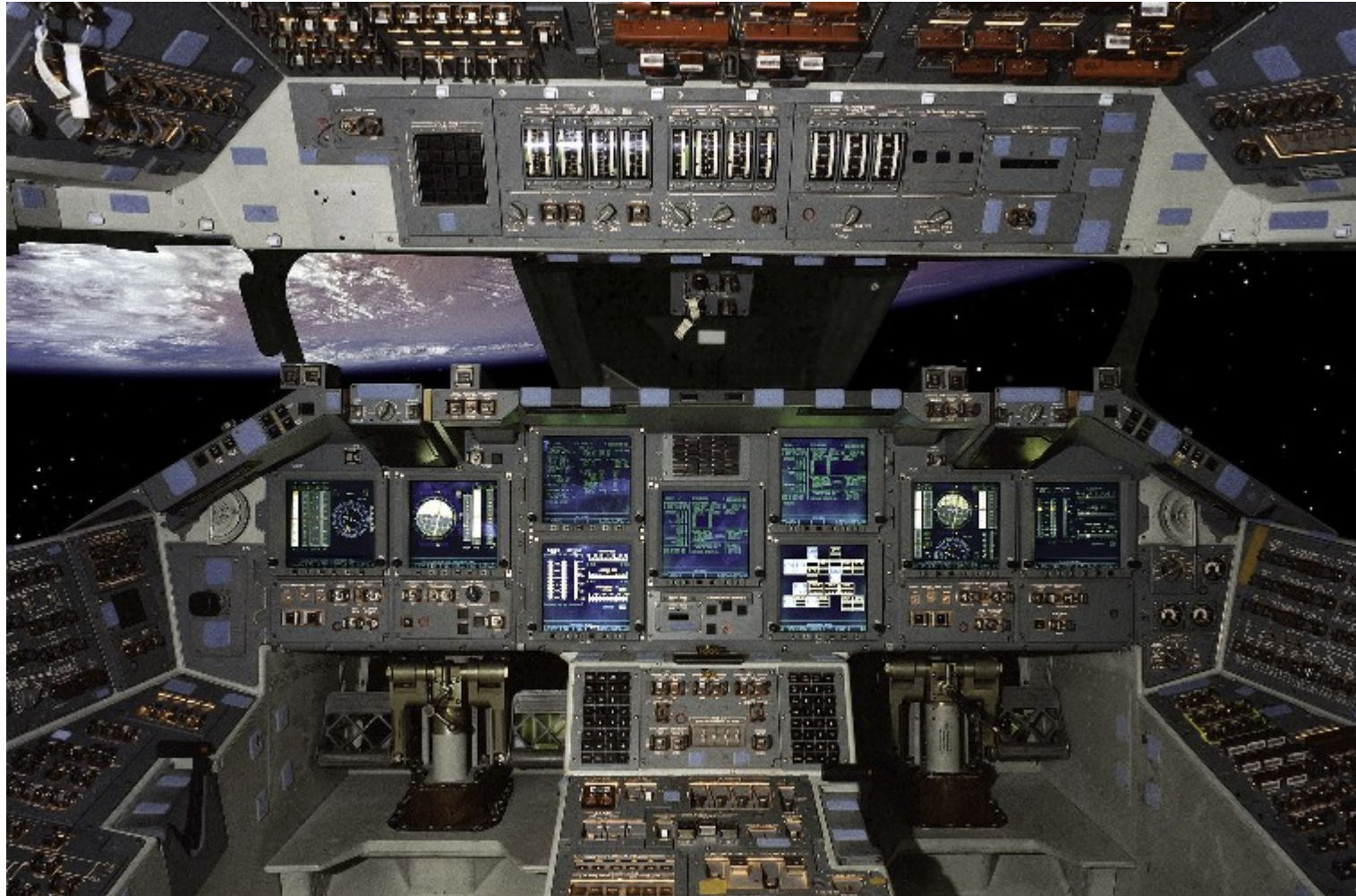
- Mature Flight-Like Hardware installed in numerous NASA facilities
- Flight Hardware Production ramping up
- Vehicle Modification Kits Complete, ready to support Vehicle Installation

- Full System is being “flown” in the Shuttle Mission Simulator (SMS) by Astronaut crews, for human factors evaluation purposes, with great results

- Strong Cost & Schedule posture for On-Time, On-Budget Completion



Backup Charts



Hardware-Based Data Pollution Prevention

- Data Pollution = ANY erroneous transfer of data from one unit to another
- AGES
 - Inhibits outputs during AGES and GPC power transients
 - Validates clocks and control signal sequences of every GPC memory transaction
- CDP
 - Hardware disable of all external and critical internal interfaces at power on / off and reset
 - Dual bus transmitter disable controls, per each 1553 channel and MIA channel
 - Independent dissimilar software actions required to enable external interfaces
 - Independent dissimilar software actions required to invoke Built In Test Equipment (BITE) logic
 - Robust error detection / correction on internal interfaces and memories
 - Robust bus energy detection on MIA interfaces to preclude dual-transmitter bus collisions
 - Synchronization of DK Bus transmitter *cutoff* to GPCs upon error, to prevent mixed perception of I/O error signature among redundant GPCs due to time-slivering
 - Comprehensive detection and status of errors (critical and non-critical) on internal interfaces and memories, for software mitigation, annunciation or downlist as required

Software-Based Data Pollution Prevention

1. Failed CDPs purge any pending GPC commands
2. Commands are only sent from the "Prime" CDP (usually this means only from the CDP with MDU focus)
3. Don't respond to invalid GPC DK Bus Polls
4. Don't command to GPC bus polls which had transmission errors
5. In addition to CDP-detected errors, use GPC parameters ("Fail Indicator DEUX GPCY") to determine if a DK Bus is failed
6. Do not command on a failed DK Bus (CDP-detected or GPC-detected)
7. Do not command to a failed GPC
8. Do not command to a GPC if that GPC's Major Function can't be determined by CAU "GPC State ID" process
9. Reject user commands targeted for a GPC Memory Configuration which does not exist
10. Reject user commands targeted for a GPC Memory Configuration to which the CDP does not have a DK connection
11. Reject user commands targeted for GPC Software OPS 0 if GNC, Sys Mgt, Payload modes all exist
12. Reject user commands during Primary Avionics System Software (PASS) Ops Transitions and Major Mode boundaries
13. Purge latent user commands during PASS Ops Transitions and Major Mode boundaries
 - 12 & 13 satisfy legacy GPC Flight Software OPS / User Notes
14. Sniff Backup Flight Software (BFS) GPC memory to verify commands targeted for BFS arrive correctly.
15. "Bus Busy" detection on the MIO (hardware & software) prevents dual responding
16. Detect Dual GPC bus commanders and annunciate to crew, but do not respond to GPCs
17. Disable DK Bus if dual CDP responders detected - protects legacy system against bus collisions
18. Perform Dual-Software-Path GPC Command computation in CDP, compare results on rad-tolerant MIO (GPC command path I/O channel hardware inside CDP), discard if not equal
19. Command Key Timer in CDP prevents latent or spurious GPC commands - ensures GPC commands are from REAL (human-initiated, not hardware transient) keystrokes

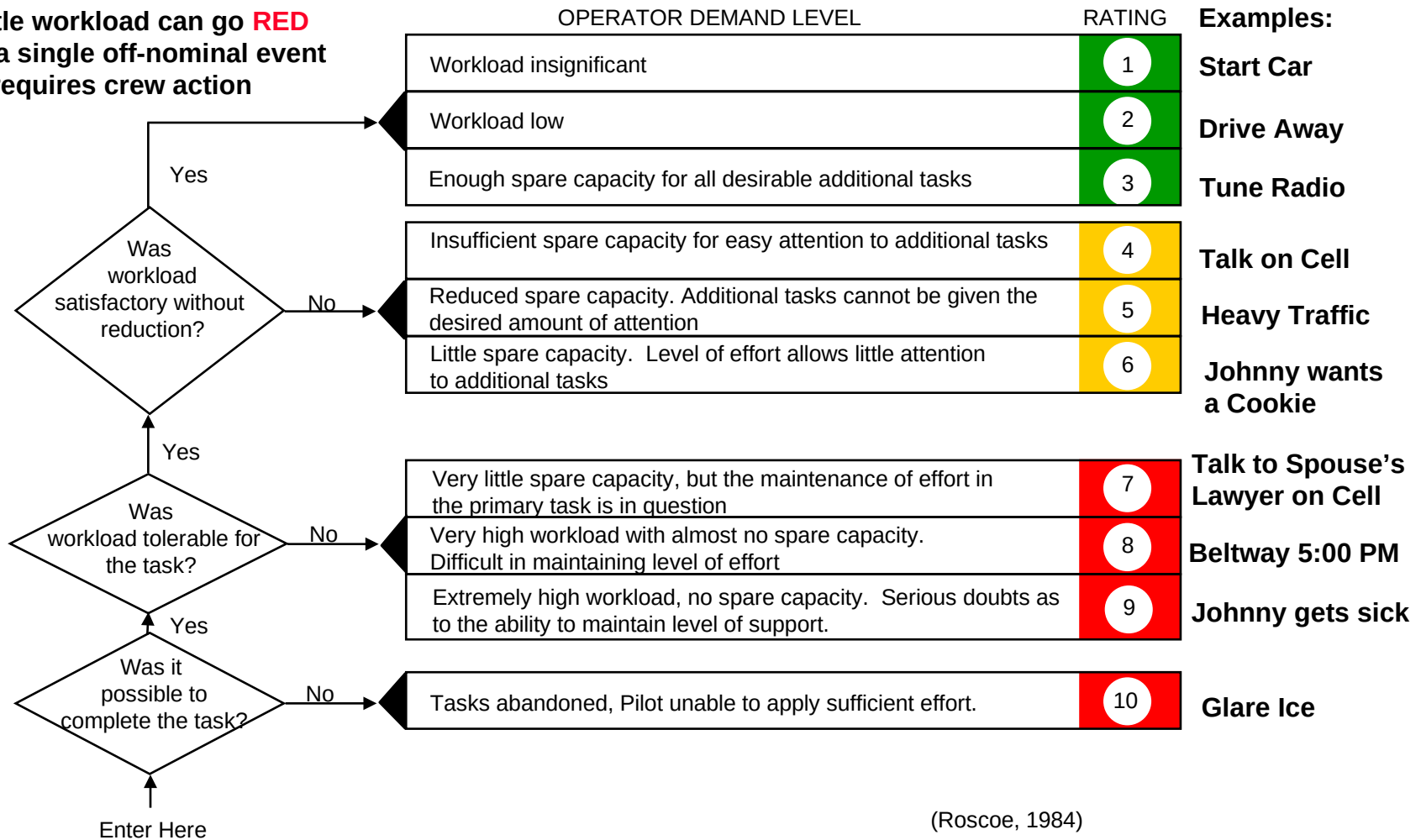
System-Level Data Pollution Prevention



- In addition to all previous Hardware & Software techniques for preventing erroneous results from single units, do the following to prevent system-level errors:
 - Within a single CDP, Compare & Vote critical redundant data from redundant GPCs (when available) @ 25 Hz, to detect otherwise undetectable interface, storage or processing errors
 - Auto-Inhibit (fail) minority external data source, select next available redundant data source
 - Across multiple CDPs, Compare & Vote critical CAU System Configuration parameters (data bus commander & responder assignments, keyboard & display assignments) @ 25 Hz, to detect divergence between CDPs
 - Auto-Inhibit (fail) minority CDP, reassign Displays to other working CDPs
 - Manual intervention required if no minority CDP (rare multiple failure scenario)

Bedford Workload Scale

Shuttle workload can go **RED** with a single off-nominal event that requires crew action



Shuttle Cockpit is a Complex Work Environment

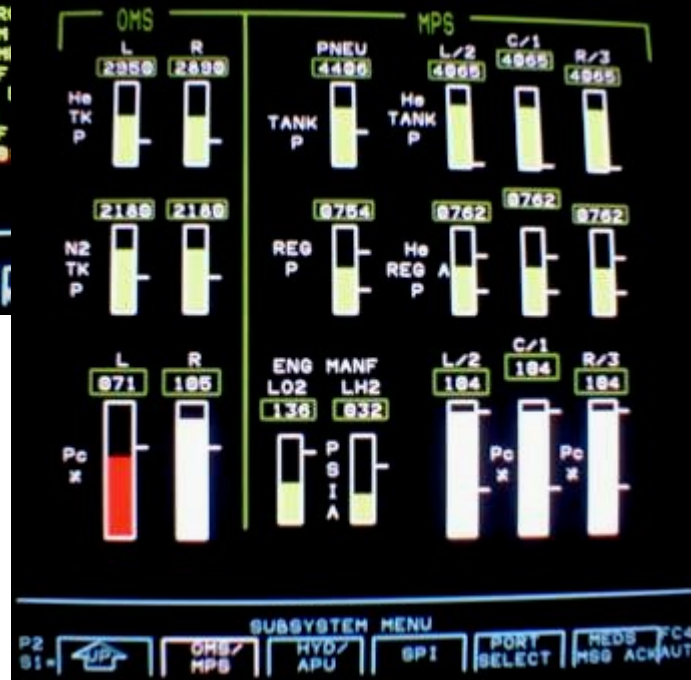
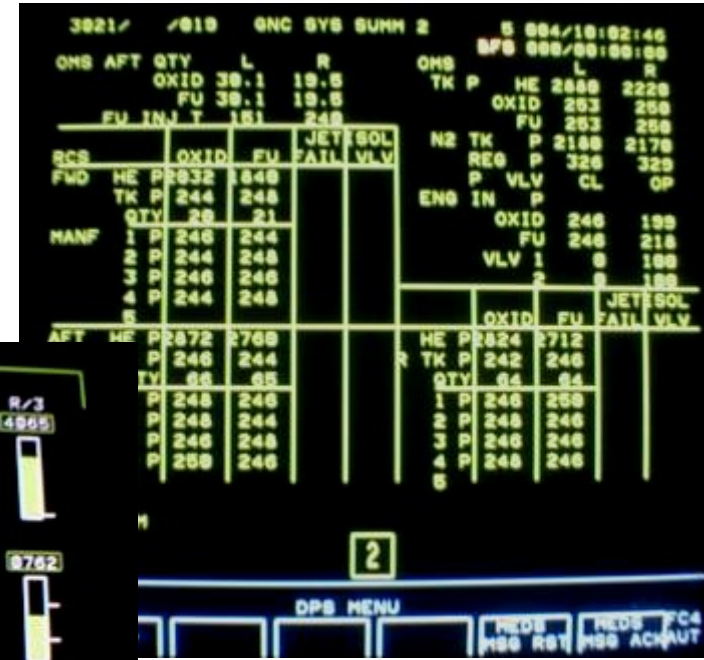


- 100+ time / safety critical dynamic flight procedures
 - Aborts to KSC, East Coast, Spain, Africa, Orbit
- ~1000 on orbit procedures
 - Systems, Payloads, Mission Objectives
- On orbit in-flight maintenance procedures designed in real-time
 - Problem diagnosis and repair / recovery
- Pre-CAU - Signature Recognition required for almost every procedure
 - Obscure problems are recognized by specific 'Christmas Tree' warning light patterns
- Pre-CAU - Rote memorization required in display navigation and problem diagnosis
 - Backed up by hundreds of pages of printed manuals, carried each mission

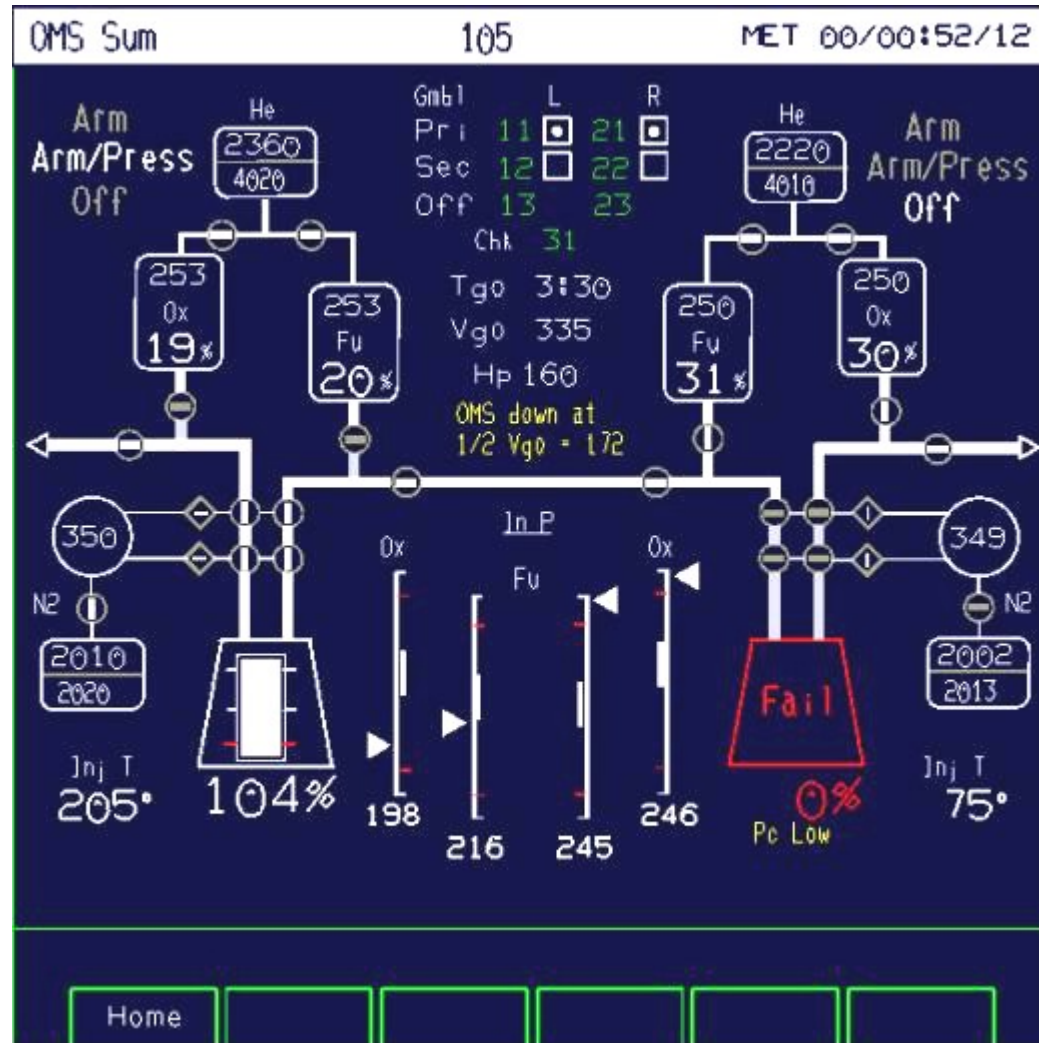
Legacy vs. CAU Display Quality

- The following charts show examples of legacy displays vs. new CAU displays
- Each pair of charts shows the same fault scenario or emergency procedure
- Observe that fault conditions are often obscured on the legacy displays, requiring the crew to perform pattern recognition vs. memorized display appearance
- Conversely, observe that CAU displays highlight fault conditions in a more logical, more easily recognizable manner

Legacy Displays to support OMS Burn Task



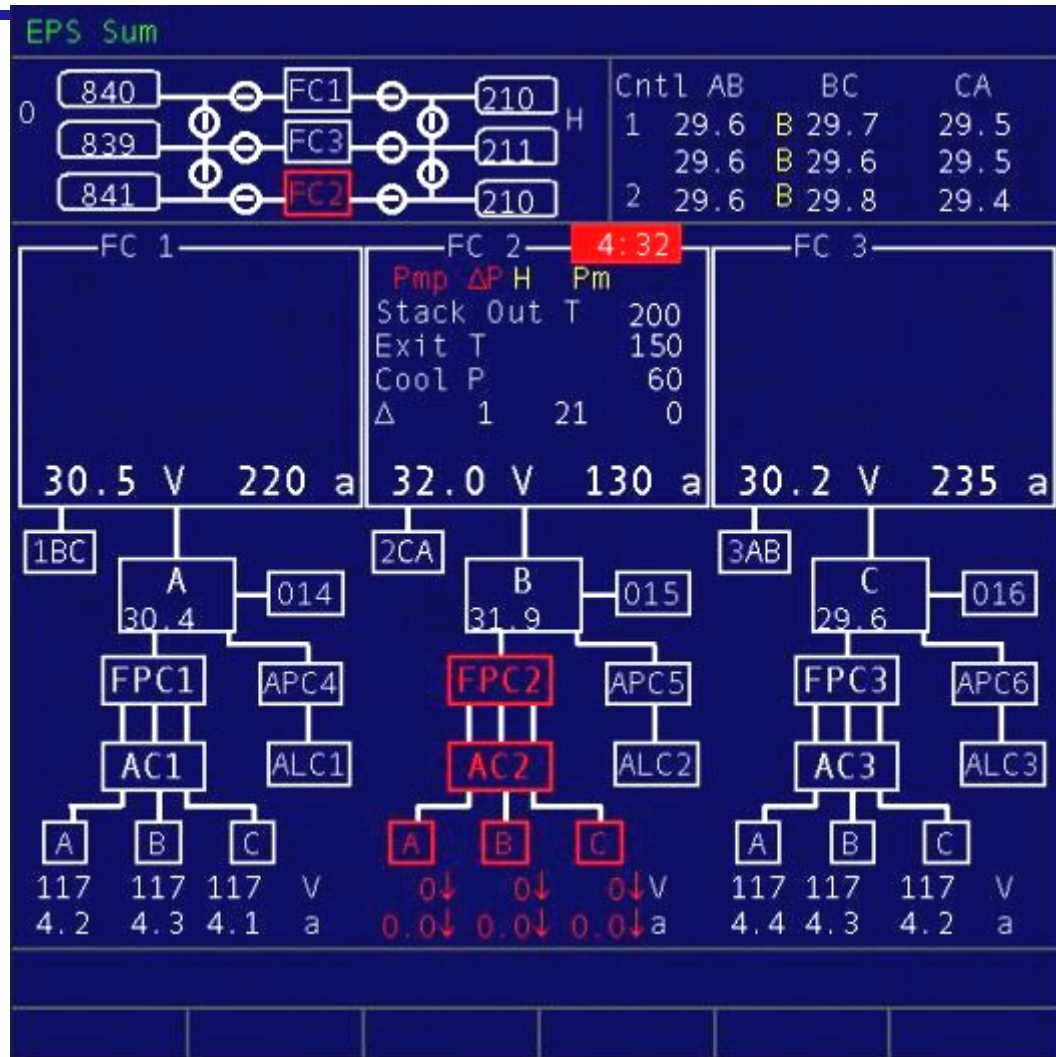
CAU Display to support OMS Burn Task



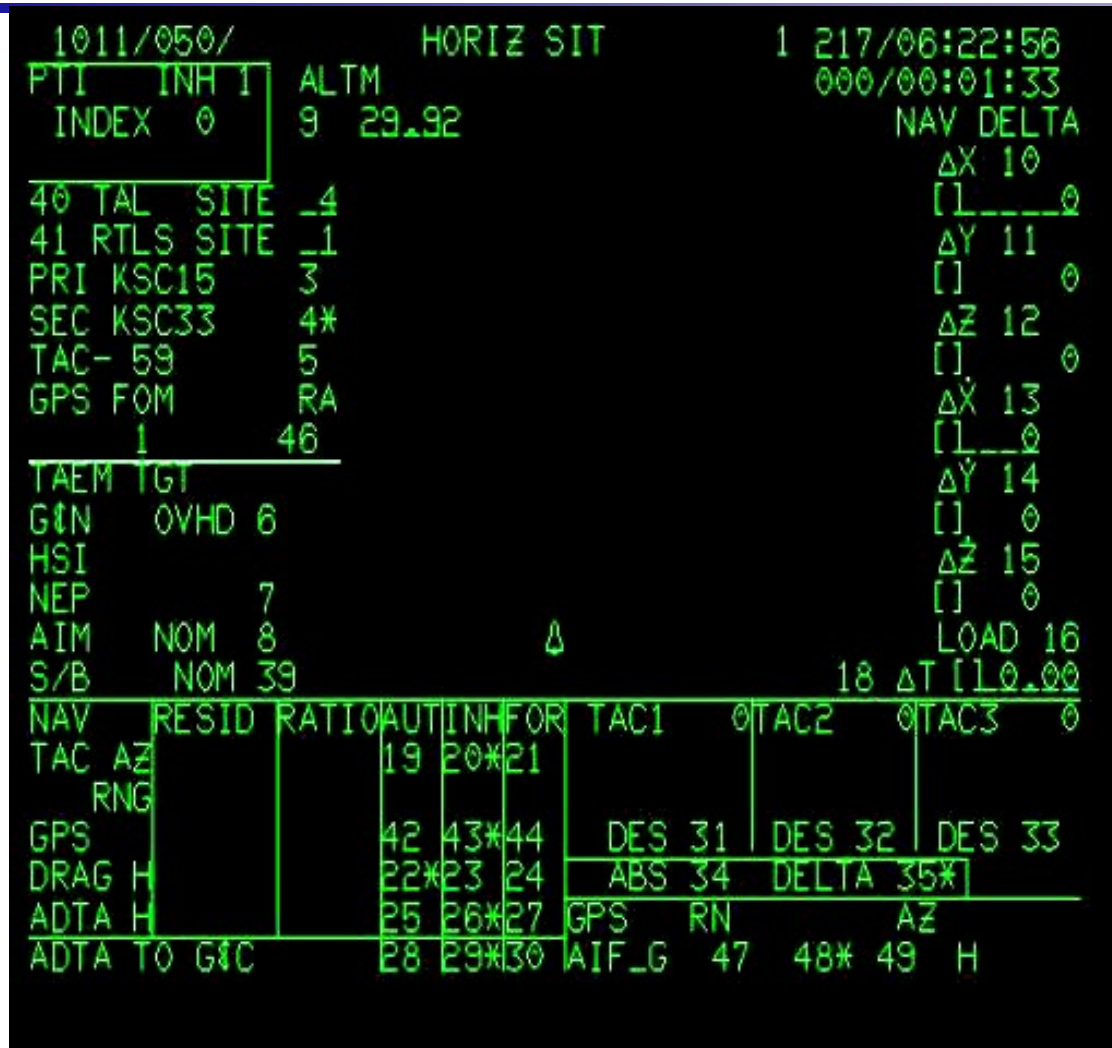
Legacy Electrical Monitoring Displays



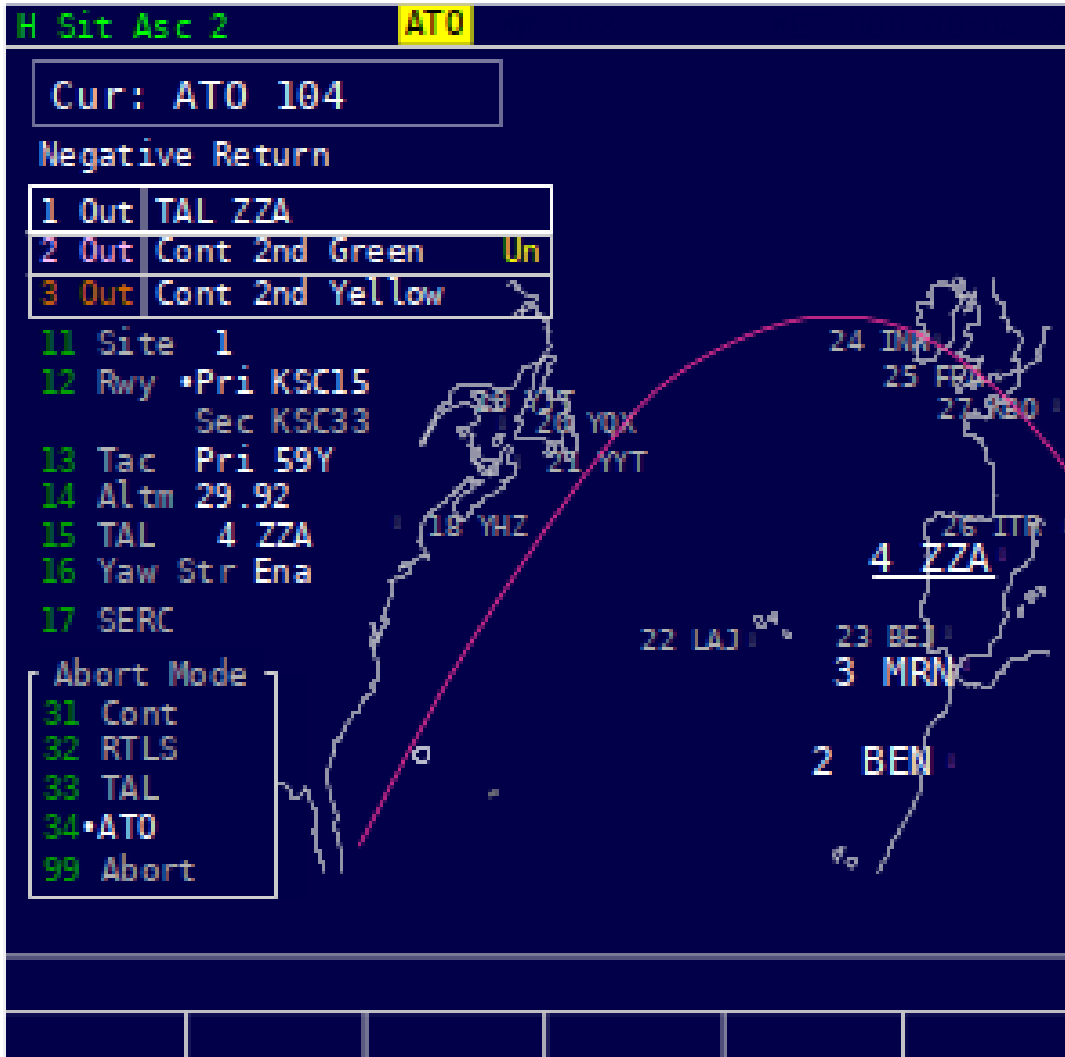
CAU Electrical System Summary Display



Legacy Ascent Horizontal Situation Display



CAU Ascent Horizontal Situation with SAFM



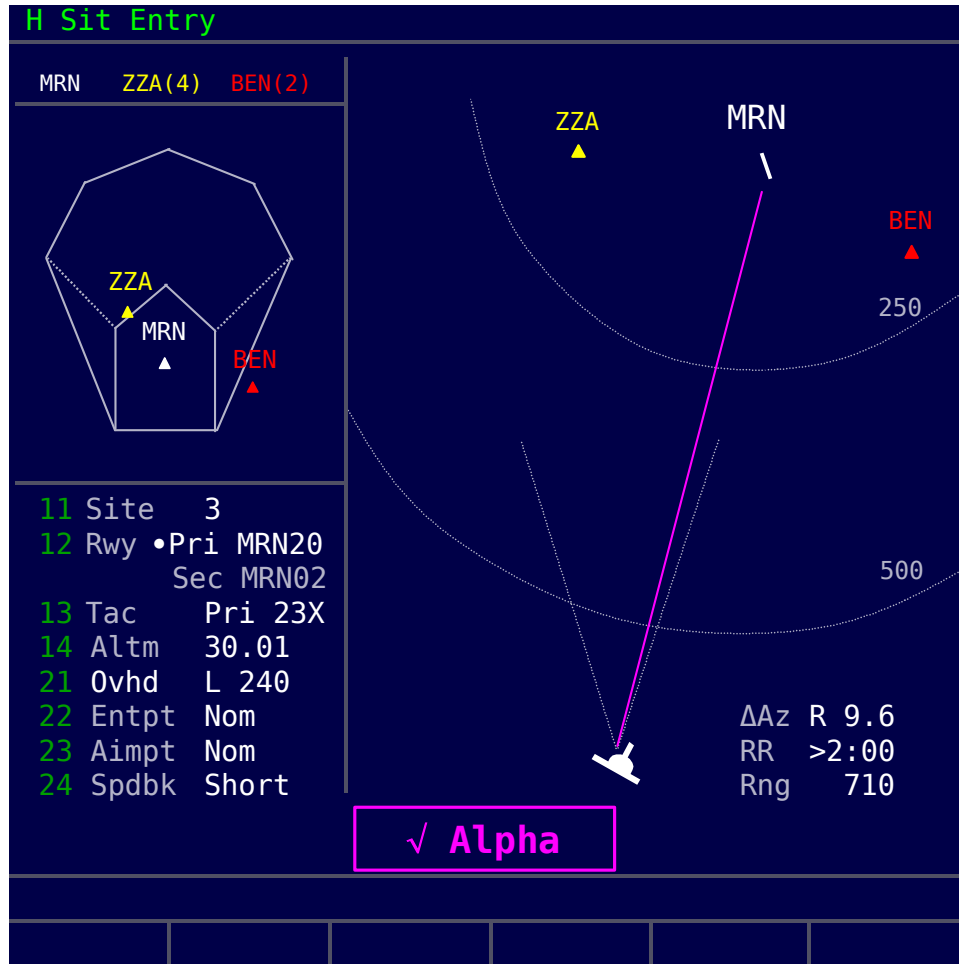
Ascent Horizontal Situation Display 2 with 1 Engine Out, and ATO Abort Executed.

Legacy Entry Horizontal Situation Display

```

3041/050/          HORIZ SIT          2 010/20:00:41
PTI INH 1          ALTM                000/00:16:27
INDEX 0           9 29.92              NAV DELTA
                                     ΔX 10
                                     [ ] ____ 0
41 LAND SITE  _1          ΔY 11
PRI KSC15      3*         [ ] ____ 0
SEC KSC33      4          ΔZ 12
TAC- 59        5          [ ] ____ 0
GPS FOM        RA        ΔX 13
  1            46         [ ] ____ 0
TAEM TGT       ΔY 14
G&N L OVHD 6    °         [ ] ____ 0
HSI L          °         ΔZ 15
NEP            7    °         [ ] ____ 0
AIM NOM 8      1.4 Δ     LOAD 16
S/B NOM 39     18 ΔT [ ] ____ 00
NAV RESID RATIO AUT INH FOR TAC1- 59 TAC2- 59 TAC3- 59
TAC AZ          19 20*21      M M M
RNG             M M M
GPS + 1.19V0.4 42 43*44     DES 31 DES 32 DES 33
DRAG H+ 947 0.0 22*23 24    ABS 34 DELTA 35*
ADTA H         25 26*27     GPS RN- 0.1 AZ+ 0.01
ADTA TO G&C    28 29*30    AIF_G 47 48* 49 H193.0
    
```


CAU Entry Horizontal Situation Display with SAFM



Summary – The CAU Safety Payback

- Decisions and actions are more timely and more accurate
- CAU provides improved crew interface for display navigation and vehicle command and control
 - Execute commands from any display via the existing keyboards
 - Consolidate information from / commanding to multiple subsystems on single display
 - Fewer keystrokes, less rote memorization, and better encoding of display parameters
 - New mobile scratchpad and improved keyboard
 - Generate multi-color graphics and logical information & command groupings on any display format
- CAU provides task-oriented displays
 - Tailored to the phase of operation
 - Utilize data from multiple sources and embedded logic in critical system and flight displays (data becomes information)
 - Provide root cause analysis for the Data Processing subsystem and Electrical subsystem
- CAU provides trajectory information, now available at all times
- CAU expands the avionics processing power and capacity for future implementation of display applications and logic
- CAU separates display generation software and new applications from the GPCs
- Enabling Requirements drove the CAU Architecture & Design