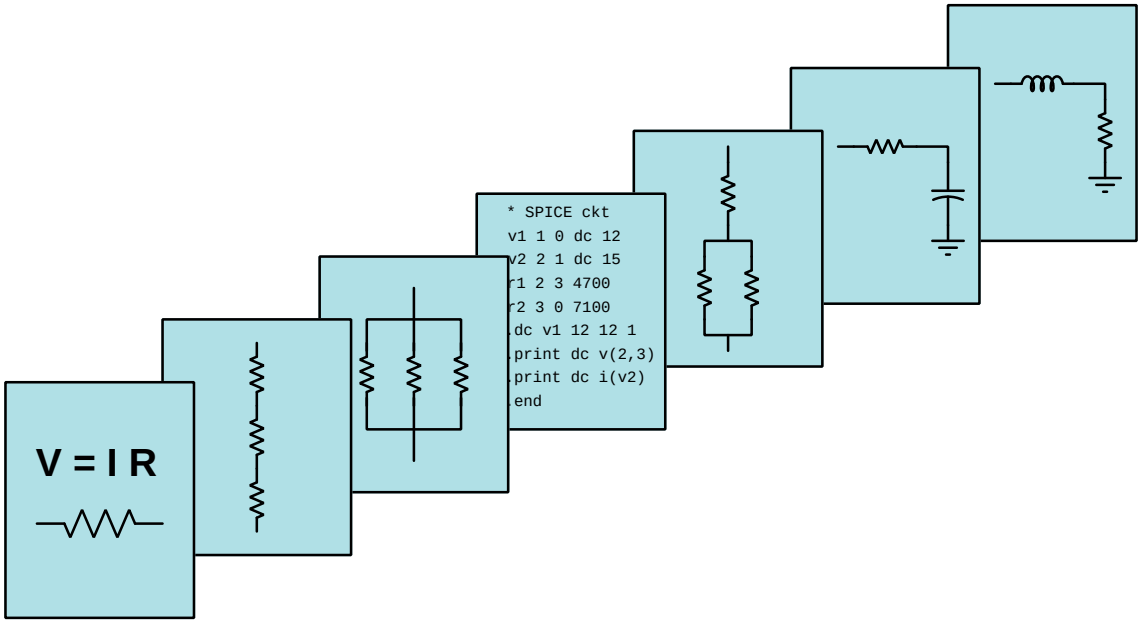
Modular Electronics Learning (ModEL) project



SPICE Modeling of Amplifier Circuits

Last update = 6 September 2024

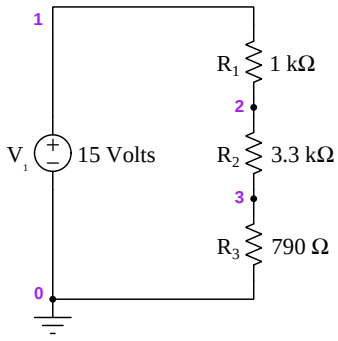
Contents

Chapter 1

What is SPICE?

SPICE is a general-purpose computer simulator for electronic circuits, with several "freeware" versions available for academic use. Although its text-based user interface may seem clumsy and archaic at first, it is quite powerful, and also neatly side-steps the many problems students tend to experience with graphic-entry ("WYSIWYG")[1] circuit simulators.

Circuits are described to SPICE in the form of a *netlist*, which is a text-based code listing of each component within the circuit, the "nodes" connecting them to each other, and the types of analyses requested of SPICE to perform on that circuit. A simple three-resistor DC circuit is shown in schematic form below, along with the netlist you would write and input to SPICE instructing it to analyze this circuit for a single source voltage value of 15 Volts and displaying the voltage drop across each resistor as well as the current through the voltage source:




```
* SPICE netlist for a series DC circuit
v1 1 0 dc 15
r1 1 2 1000
r2 2 3 3300
r3 3 0 790
.dc v1 15 15 1
.print dc v(1,2) v(2,3) v(3) i(v1)
.end
```

The purpose of this document is to give a general introduction to the use of SPICE, and also to showcase a "gallery" of examples where SPICE is used to perform analyses on circuits containing semiconductor components. This gallery will not only help new users of SPICE learn how to format netlists and interpret analyses, but they also serve as an extensive bank of practice problems for new students of electricity and electronics to use as they build and sharpen their circuit analysis skills.

This last point deserves some elaboration. The study of electricity and electronics, like all scientific studies, is aided by the solution of practice problems. Problem-solving is a skill like any

[1] "WYSIWYG" is an acronym meaning *What You See Is What You Get*.

other, and practice helps to build an arsenal of tools useful to any new problems you may encounter. Having answers provided for these problems allows students to check their work and to self-identify any misconceptions or bad problem-solving habits.

Traditional textbooks provide banks of practice problems for students to solve, and while these are useful, the availability of computer simulation software take this concept one enormous step further. Not only may the sample simulations given in this learning module serve as practice problems for students, but they will also serve as templates for creating one's own practice problems, so you will never be wanting for more practice opportunities. Like all computer simulations, SPICE rigorously applies known laws and principles of physics to predict how specific systems will behave, and as such it never makes mistakes[2].

SPICE has played a pivotal role in my own self-education on the topic of circuits, being an excellent tool to check my own analytical skills and to explore the properties of certain devices (e.g. transistors, transmission lines, transformers) with relative ease. The ultimate goal of any scientific education is to equip the student with mental tools to solve problems and to continue their own learning. SPICE is a software tool that can aid in the development of these mental tools, and should be used as such.

[2]Some simulations can and do miss certain details if they are not set up properly, but this is not the same kind of error as a human is prone to committing, and it is precisely this difference between computers and humans that makes computer simulations useful learning tools. Simply put, the computer will not repeat *your* mistakes.

Chapter 2

Using SPICE

SPICE is computer software designed to simulate the behavior of electric circuits. It was developed in the early days of digital computing when the dominant user interface was the *command prompt*, and the most common user file format was plain "ASCII" text. Graphic, mouse- or touchscreen-driven interfaces simply did not exist at that time except for prototype systems or highly specialized applications. Most general-purpose computing of that era occurred through the use of a keyboard and a monochrome text-based monitor, or worse yet in the form of punched paper cards and teletyped output.

This is why SPICE usage seems to resemble text-based code programming. The user (that means *you*) enters a description of the circuit to be analyzed and the analysis/display methods preferred by means of typed text, then the SPICE program is run and the output is viewed again in text form.

This may all seem terribly anachronistic in the 21st century, but there are some decided advantages to using SPICE with this legacy interface:

- These legacy versions of SPICE are free to use. No license fees, nothing.
- The relatively small (by modern standards) SPICE software runs very fast on modern computers.
- Circuits that are challenging to graphically draw are easy to "code"
- Errors resulting from the computer's incorrect interpretation[1] of a diagram are eliminated
- Learning to use SPICE in this manner is an excellent orientation to simple programming

The first step in setting up SPICE to analyze a circuit is to describe that circuit using SPICE's own language, and to type this description into a plain-text file on your computer. This file is often referred to as a *deck*, with each line of text in that file called a *card*. Taken together, those lines of text (a.k.a. *cards*) comprise a *netlist* describing the circuit and the intended analysis for SPICE. The

[1] I have struggled multiple times to get a WYSIWYG circuit analyzer program to simply analyze what I have drawn, due to "hidden" wire connections, or intended wire connections that don't exist – all "bugs" in the software stemming from the non-trivial challenge of getting a computer to recognize and correctly interpret a hand-made diagram. SPICE, with its "netlist" input and clear node-labeling protocol, neatly eliminates this whole problem.

anachronistic terms "card" and "deck" harken back to the days of punched-card input for computer systems, where each separate instruction for SPICE was a series of punched holes on its own paper card, the collection of cards representing one circuit being a "deck of cards" that would be fed into the card reader one at a time[2].

Once you have typed the netlist and saved it as a text file (a.k.a. *deck*) to your computer, you are ready to run a SPICE analysis on it. This is done by typing the word `spice` on a command-line interface[3] followed by a less-than symbol (<) and then followed by the name of the text file "deck", and finally terminated by pressing the Enter key. Here is an example, showing a screenshot of a SPICE analysis about to happen on a "deck" file named `test.cir` just prior to pressing the Enter key:

After entering this command, SPICE performs its analysis and by default dumps a report as plain text to the same command-line terminal. If you desire to save SPICE's text output to another plain-text file for posterity, or to be able to paste that analysis into another document, you may "redirect" SPICE to send its plain-text analysis to another file of your choosing by using the greater-than symbol (>) in the command. Here is an example showing how to instruct SPICE to read the contents of `test.cir` and place all the analysis text into another file named `test.out`:

```
spice < test.cir > test.out
```

[2]Interestingly, legacy versions of SPICE do not care what order these "cards" appear in the "deck" with the exception of the first line (the Title) and the last line (the `.end`) statement.

[3]Microsoft Windows operating systems provide a general-purpose command line interface terminal named `cmd`. Unix-based systems such as Apple's OS X and Linux typically offer a variety of terminal programs suitable for this purpose.

2.1 Summary of steps

To summarize, using SPICE in this legacy format requires the use of a *text editor* program (such as "Notepad" on Microsoft Windows operating systems) to write the netlist, and a command-line interface on your computer to invoke SPICE to perform its analysis. The sequence of steps may be listed:

1. Invoke a text editor program and type the netlist (instructions) describing the circuit and the type of analysis you wish SPICE to perform
2. Save this netlist as a plain-text file to your computer
3. Type `spice` < *deck_filename* on the command-line interface and then press Enter
4. View the analysis in the command-line interface

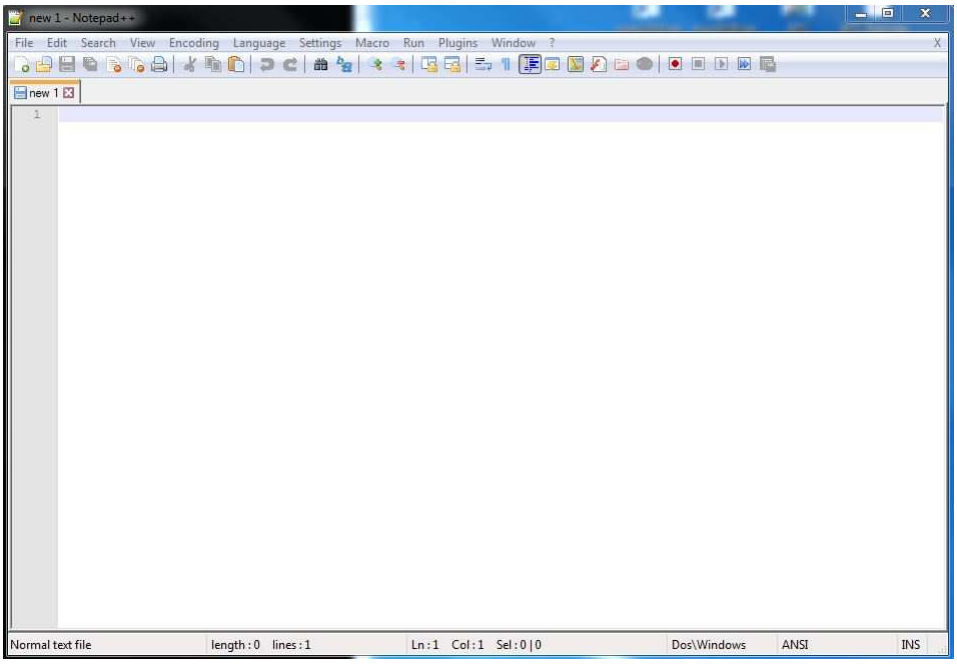
Most of SPICE's "learning curve" is in becoming familiar with the syntax of the netlist: exactly which letters, numbers, and sequences must be entered in order to properly describe the circuit and the type(s) of analysis desired. A few cardinal rules must be obeyed when creating or editing netlists:

- The first line (card) of the netlist is the Title. It cannot be omitted.
- The last line (card) of the netlist is the `.end` command. It cannot be omitted.
- Each and every unique connection point in the circuit must be assigned a number called a *node*. This is how you describe the "shape" of the circuit to SPICE: by describing which nodes each component connects to. Components sharing common node numbers are electrically common to each other; components with differing node numbers are electrically distinct from each other. There *must* be a node 0, and this is the "Ground" node of the circuit.

2.2 Demonstration on Microsoft Windows

Here I will demonstrate this four-step process as a series of screenshots from a computer running SPICE version 2G6 on the Microsoft Windows version 7 operating system.

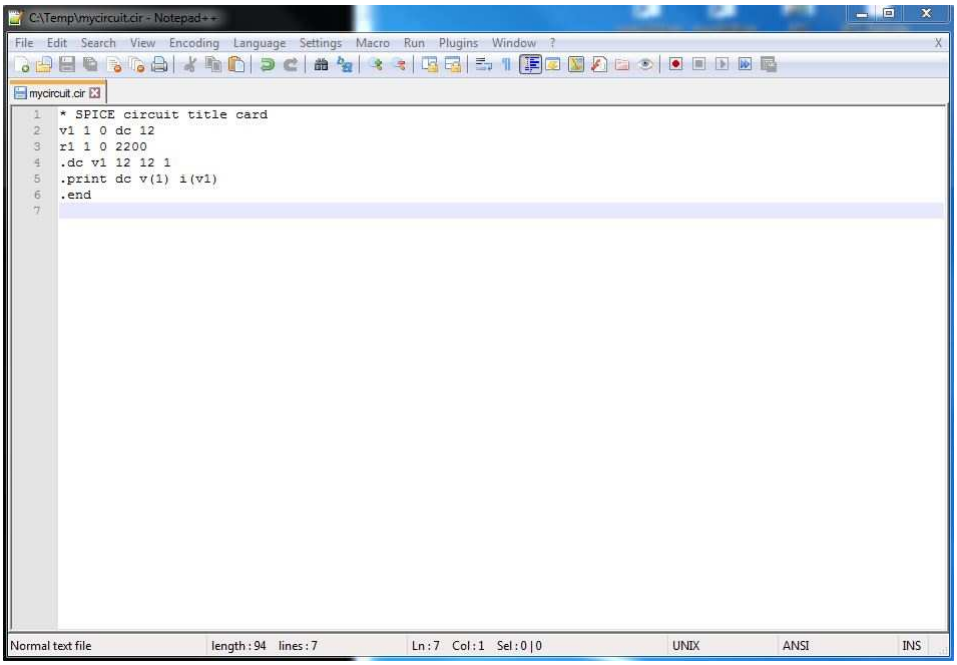
2.2.1 Invoking a text editor



Here, the screenshot shows an empty file, ready for me to type text. *Text editors* are similar to *word processors* except they lack provision for neatly formatting the text (e.g. no font selections, no paragraph formatting, etc.). Their sole purpose is to facilitate the creation and editing of plain-text files.

Text editors are the go-to application for practically all text-based computer programming. *Many* different text editors exist, each with their own features, and computer programmers tend to develop a fondness for one particular editor that best suits their programming needs. A "stock" text editor comes with every version of Microsoft Windows called `notepad`, but this editor is extremely limited in its capabilities, and I do not recommend it. The editor shown here (`notepad++`) is *vastly* superior and highly recommended.

2.2.2 Saving the deck



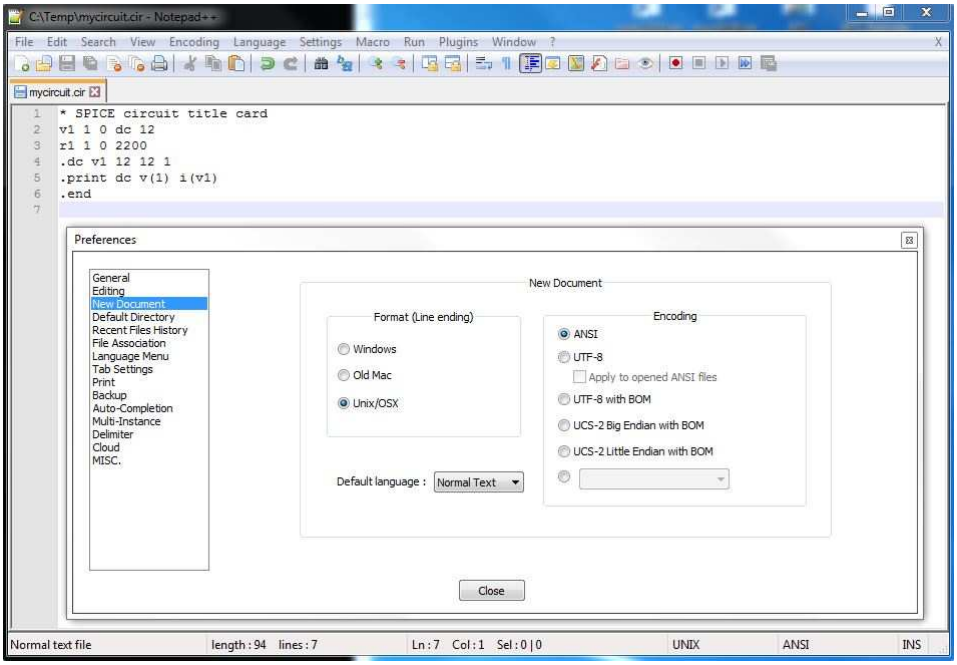
Here, I have chosen the filename `mycircuit.cir` for the deck. Note that you do not have to end every deck filename with the suffix "`.cir`" – this is simply my personal choice. Any filename consistent with the naming conventions of your computer's filesystem and containing no space characters is permissible. We avoid space characters because command-line interfaces typically interpret spaces as delimiting characters designed to separate commands and filenames from each other. If you must have a "space" in your filename, use an underscore character or a dash (_ or -). For example, `my-circuit` is acceptable, but `my circuit` is not.

Here is a line-by-line (a.k.a. *card-by-card*) interpretation of the netlist:

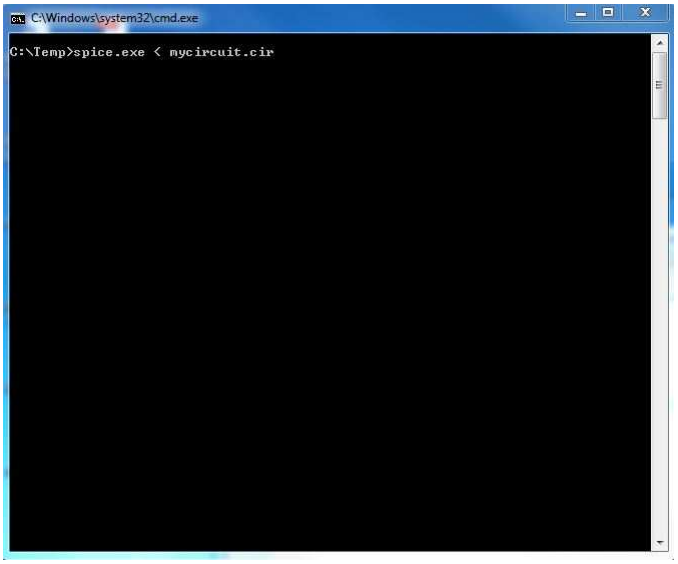
`* SPICE circuit title card` *This is the arbitrary "title" line*
`v1 1 0 dc 12` *Defines a 12 Volt DC voltage source named "v1" between nodes 1 and 0*
`r1 1 0 2200` *Defines a 2200 Ohm resistor between nodes 1 and 0*
`.dc v1 12 12 1` *Requests a DC "sweep" analysis from 12 Volts to 12 Volts on source "v1"*
`.print dc v(1) i(v1)` *Measures the voltage at node 1 and current through source "v1"*
`.end` *Tells SPICE to stop*

Note how components are "connected" to each other in the netlist by common node (connection-point) numbers. This is how SPICE is able to "picture" circuits without the use of graphical images. Each electrically distinct point in a circuit is given a unique number, and different components specified by the points they're connected to.

An idiosyncrasy of SPICE version 2G6 is that it must receive its "deck" file in Unix text format rather than Windows text format. Thankfully, `notepad++` provides a means to select which text format the deck file will be written in, as shown in this screenshot of the "Preferences" dialog window:



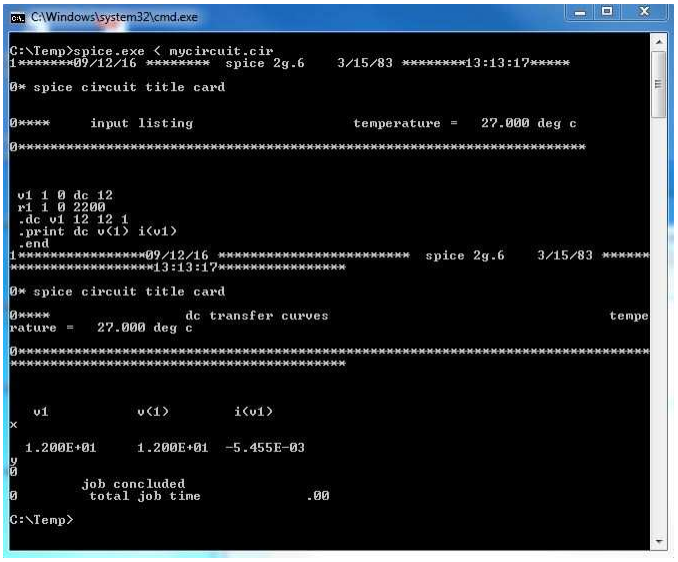
2.2.3 Invoking SPICE



This screenshot shows the command-line interface terminal (not the text editor), with the command ready to enter. This terminal may be access on any Windows operating system by invoking the `cmd` command.

Note that the exact command being entered here is `spice.exe < mycircuit.cir` because the SPICE executable file installed on this computer is named `spice.exe` rather than just `spice`.

2.2.4 Viewing the SPICE analysis



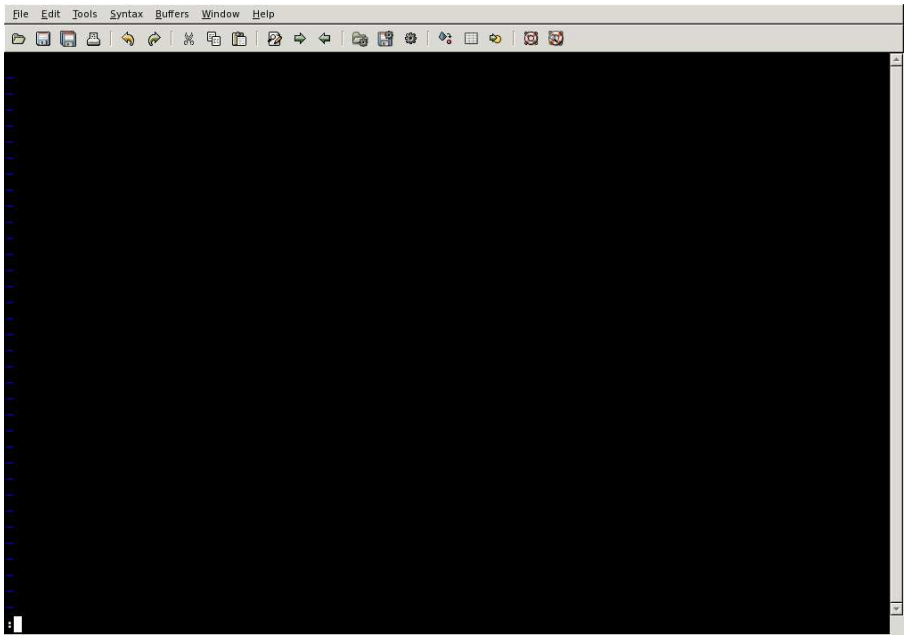
As you can see, SPICE is a very "chatty" program that displays a fair amount of extraneous text on the screen following an analysis. Ignoring all the headings and labels, you can see in this display a reiteration of the original netlist (deck) followed by the requested measurements of `v(1)` (i.e. voltage between node 1 and ground, which is node 0) and `i(v1)` (current through source `v1`).

This concludes a *very* brief orientation on using SPICE. For more information, I refer you to the following sections on SPICE component descriptions and analysis descriptions, as well as to the "Gallery" chapter which shows you tested SPICE netlists and output results so you may learn by example.

2.3 Demonstration on Linux or CygWin

Now, I will show you this same four-step process using SPICE version 2G6 running under the Linux operating system. The steps shown here are virtually identical within the "CygWin" emulator which adds a Unix-like command line environment to any Microsoft Windows operating system.

2.3.1 Invoking a text editor



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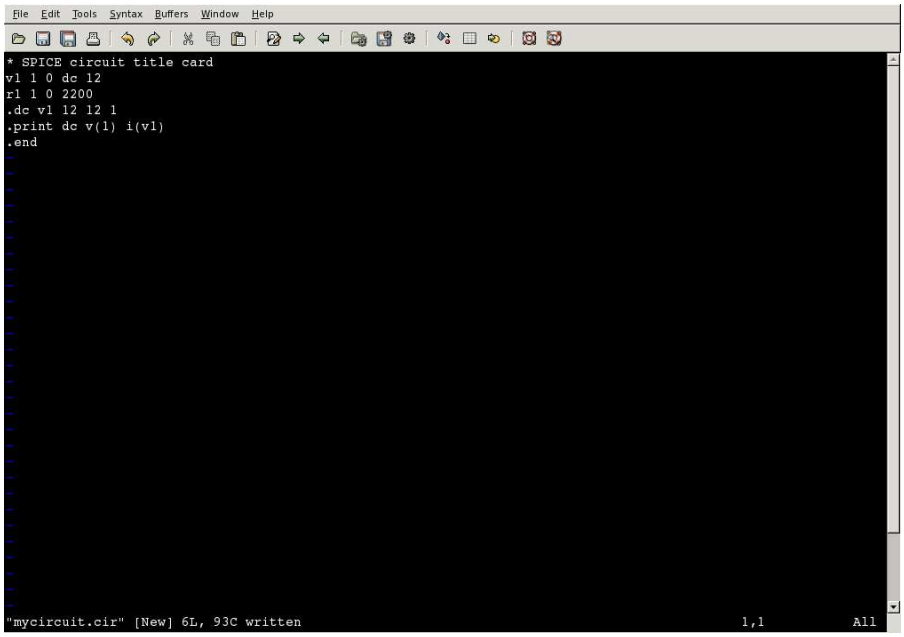
Text editors are the go-to application for practically all text-based computer programming. *Many* different text editors exist, each with their own features, and computer programmers tend to develop a fondness for one particular editor that best suits their programming needs. I personally prefer `gvim` (or `vim` in the CygWin emulator) and loathe Microsoft `notepad`, but text editors tend to be a highly personal choice.

2.3.2 Saving the deck



Here, I have chosen the filename `mycircuit.cir` for the deck. Note that you do not have to end every deck filename with the suffix "`.cir`" – this is simply my personal choice. Any filename consistent with the naming conventions of your computer's filesystem and containing no space characters is permissible. We avoid space characters because command-line interfaces typically interpret spaces as delimiting characters designed to separate commands and filenames from each other. If you must have a "space" in your filename, use an underscore character or a dash (_ or -). For example, `my-circuit` is acceptable, but `my circuit` is not.

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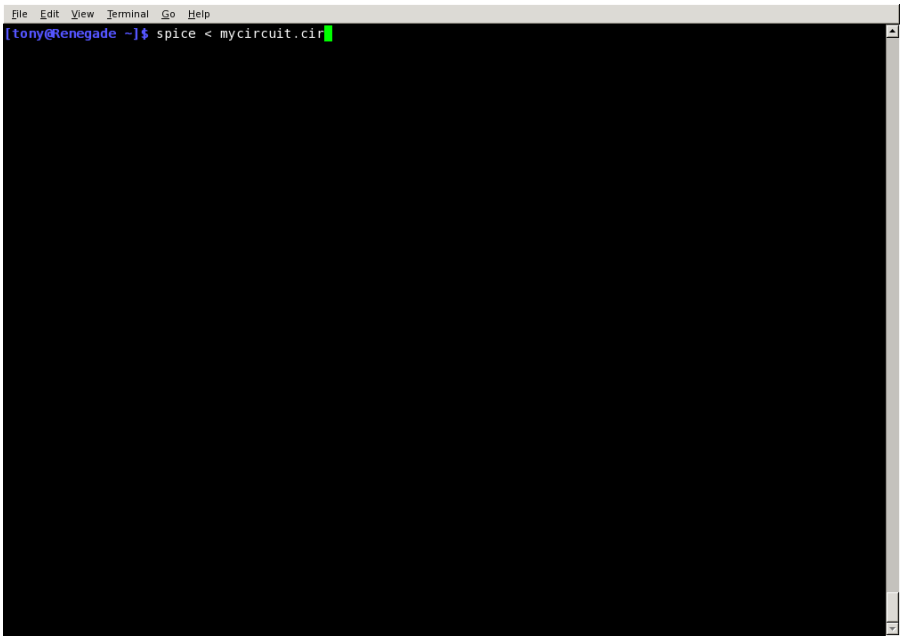
`.end` *Tells SPICE to stop*

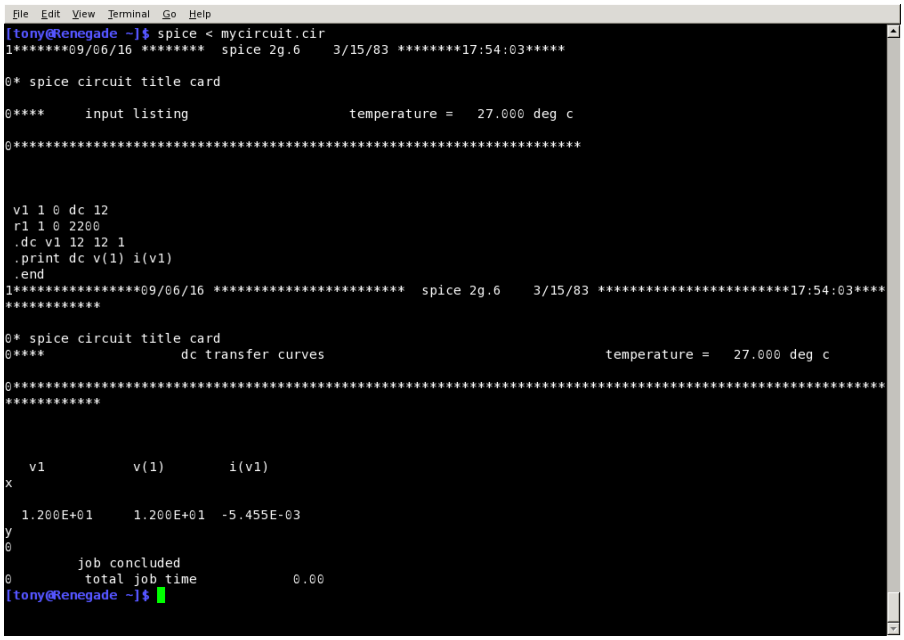
Note how components are "connected" to each other in the netlist by common node (connection-point) numbers. This is how SPICE is able to "picture" circuits with no graphics. Each and every electrically distinct point in a circuit is given a unique number, component placement being specified by these numbered connection points.

2.3.3 Invoking SPICE



This screenshot shows the command-line interface terminal (not the text editor), with the command ready to enter.

2.3.4 Viewing the SPICE analysis



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This concludes a *very* brief orientation on using SPICE. For more information, I refer you to the following sections on SPICE component descriptions and analysis descriptions, as well as to the "Gallery" chapter which shows you tested SPICE netlists and output results so you may learn by example.

2.4 Demonstration of NGSPICE interactive mode

A more modern (yet still free) version of SPICE is NGSPICE which provides all the old command-line functionality of legacy SPICE versions, plus a window-based *interactive* mode where you may call for certain analyses of a circuit without editing the netlist (deck file). This interactive display window contains a command-entry field as well as a display showing the results of those commands. The procedure for doing this, which I have tested on NGSPICE version 26 on a computer running the Microsoft Windows 7 operating system, is as follows:

1. Create the netlist using your favorite text editor and save it under a convenient filename in a convenient location. I will arbitrarily choose the filename `test.cir` for this demonstration.

2. Start the interactive version of NGSPICE and then enter the command `source test.cir` to instruct it to read the contents of that netlist file. Alternatively, instruct the Windows operating system to associate all `*.cir` files with NGSPICE by right-clicking on the file's icon and choosing the "Open with..." option, selecting `ngspice.exe` as the application you *always* wish to use for opening any `.cir` files. From then on, all netlist files ending in `.cir` will appear as icons bearing the NGSPICE logo, and double-clicking on it will start NGSPICE and automatically run the `source` instruction. *You should be able to skip this filename-association step for all future uses of NGSPICE.*

3. (Optional) – Type `listing` and press Enter to execute the "listing" command. NGSPICE will print the netlist in its display window, letting you verify that NGSPICE has loaded your intended netlist.

4. Enter the `run` command.

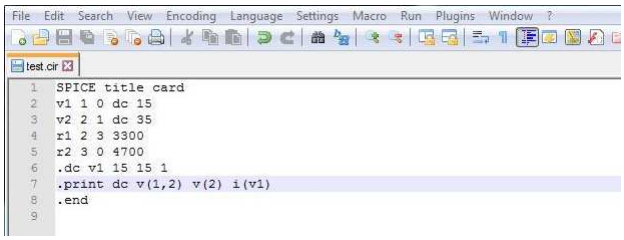
5. Enter various display commands such as `print` and `plot`. If you choose to plot results using the `plot` command, for example if you are testing a circuit's response over a range of time, or of source values swept over a specified interval, NGSPICE will open up an additional graphic window showing the results in color. When in doubt, `print all` and `plot all` are good display commands to try.

If you decide to alter the circuit after having run an analysis, simply close down NGSPICE, edit the netlist file using your text editor (re-saving that file), and then re-open NGSPICE by double-clicking on the netlist file icon again. Then, just issue the `run` command followed by any display commands you wish.

A very nice feature of this interactive mode is the ability to recall past commands without the need to re-type them. Simply press the "up" and down "arrow" keys to recall all past typed commands from history buffer, then press Enter to re-issue that command. This will save you much time and potential for keystroke errors!

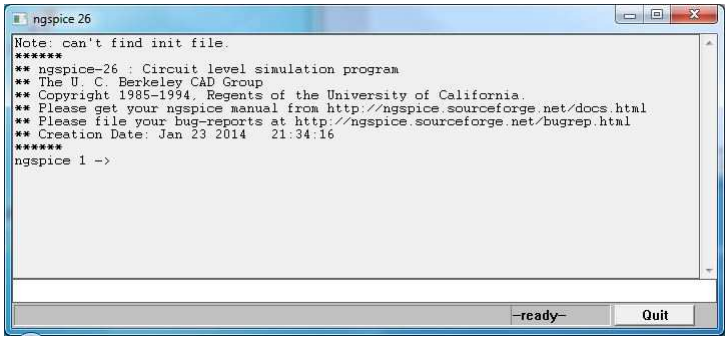
2.4.1 Creating the netlist

To begin our demonstration, we will first create a netlist using a text editor. In this case, the editor happens to be `notepad++` which is much more capable than the stock `notepad` that comes with Microsoft Windows. After writing the netlist, it will be saved under the filename `test.cir`:



2.4.2 Starting NGSPICE

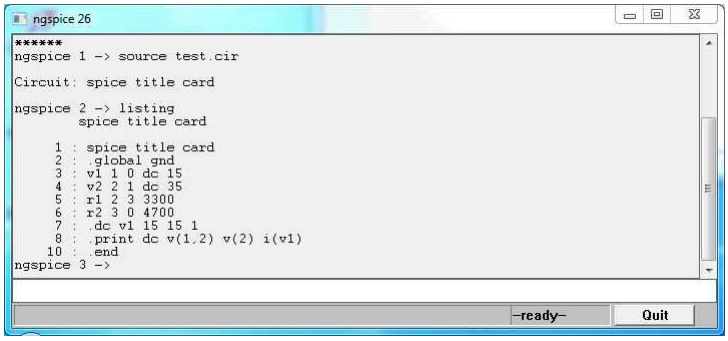
When NGSPICE is started with no command-line arguments (or simply started by double-clicking on the `ngspice.exe` filename), you will see this interactive window appear on your computer's screen. Commands are typed into the rectangular field at the bottom of the window, and after pressing Enter you will see the results of that command displayed in the upper portion of the window:



Please note that if you take the time to associate `.cir` files with NGSPICE in Microsoft Windows, this step (as well as the "Loading the netlist" step and "Verifying the loaded netlist" step) will be performed automatically for you whenever you double-click on the netlist file icon. You will know you have been successful in setting up this association if all files with filenames ending in `.cir` appear with the NGSPICE logo in their Windows icons.

2.4.3 Verifying the loaded netlist

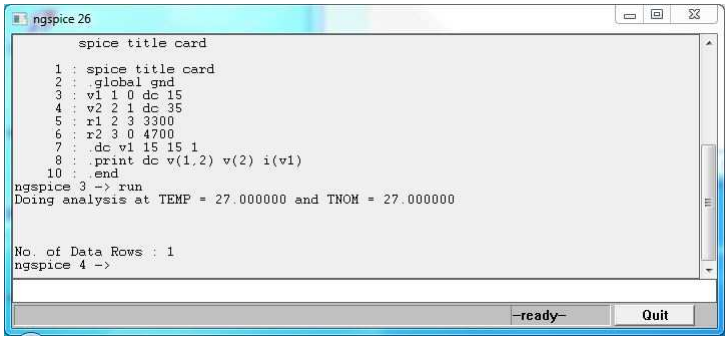
Now we will verify the successful loading of our netlist by issuing the `listing` command. Our netlist now appears in the display window:



This step is optional, but is a good habit. If you approach SPICE as a learning tool, using it to run simulated experiments on virtual circuits to help you master certain electrical concepts, you will find yourself making many changes to your netlists and re-running analyses on those revised circuits. The `listing` step gives you opportunity to verify each time that your edited netlist has been loaded into NGSPICE and is ready for analysis. It also shows, as in this case, if NGSPICE inserted any statements of its own (e.g. `.global gnd`).

2.4.4 Running the analysis

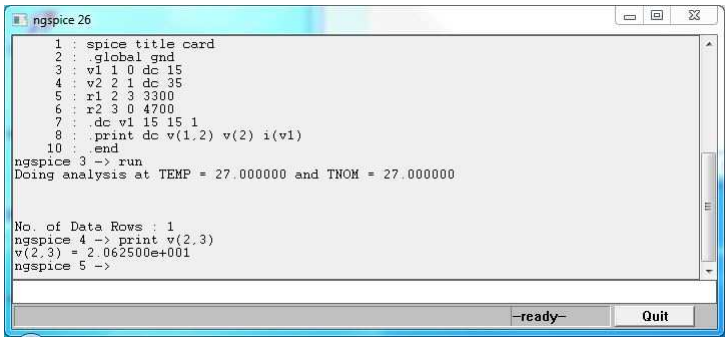
Before we may request any displayed results from NGSPICE, we must issue the `run` command:



An interesting feature of NGSPICE is that it ignores the `print` command within the netlist. Running the simulation merely performs the calculations, but provides no automatic output of results. In the "interactive" version of NGSPICE, it waits for you to enter specific commands before actually displaying any results to the screen. Even with `.print` or `.plot` instructions (cards) contained in the netlist, NGSPICE's interactive mode demands you type the display command yourself after it has "run" the simulation. To print the voltage between nodes 1 and 2, for example, you would enter the command `print v(1,2)`. NGSPICE relies on the analysis option in the netlist to discern whether this is a DC or AC analysis.

2.4.5 Printing a voltage

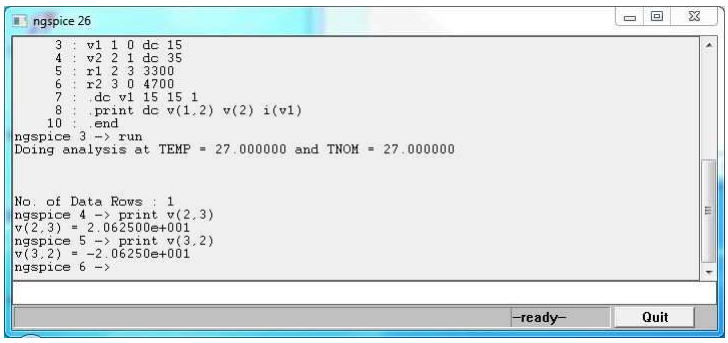
Now we are ready to make `print` or `plot` requests of NGSPICE. Here we request NGSPICE to print the voltage between nodes 2 and 3 with the `print v(2,3)` command:



Please note how NGSPICE does not require a preceding period symbol with the `print` command when it is typed at the interactive command line, nor does it require we specify `dc` analysis as part of the `print` command! In fact we could have omitted the entire `.print` card in the netlist, as NGSPICE's interactive mode only follows output instructions typed at the command line.

Note also how NGSPICE defaults to scientific notation, in this case the voltage displayed as `2.062500e+001` which means 2.062500×10^{1} Volts, or 20.62500 Volts.

If we issue the `print` command with the node numbers swapped, NGSPICE displays the DC voltage as though measuring with a DC voltmeter with the red test lead on node 3 and black test lead on node 2, showing a negative value instead of positive:



If we wish to see more than one voltage reported, we may specify this at the interactive command line in exactly the same manner as we would have specified within the netlist. For example, issuing the command `print v(1,2) v(2) i(v1)` would result in NGSPICE printing the voltage between nodes 1 and 2, followed by the voltage between nodes 2 and 0, followed by the current through voltage source v1. Alternatively, we can type `print all` in the NGSPICE command line and receive a report of all voltages (with reference to node 0 which is ground) rather than just the voltage(s) we specify.

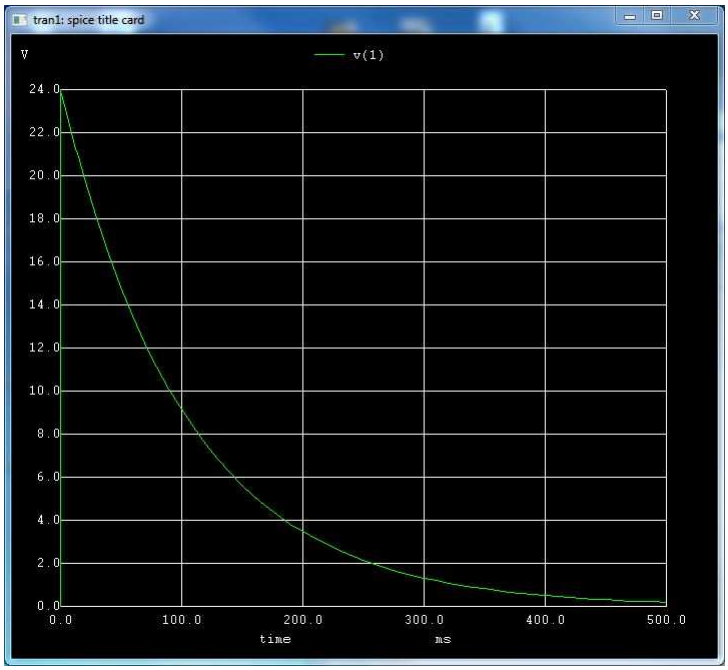
2.4.6 Plotting graphs using NGSPICE

Now we will explore the graphic plotting capabilities of NGSPICE. This is much more advanced than the text-based plots of legacy SPICE versions such as 2G6. Let's begin our example with the following netlist:

```
SPICE title card
c1 1 0 47e-6 ic=24
r1 1 0 2200
.tran 10m 500m uic
.plot tran v(1)
.end
```

This particular netlist defines a simple capacitor-resistor circuit with the 47 μF capacitor precharged to 24 Volts. The `.tran` card calls for a time-domain analysis from $t = 0$ to $t = 500$ milliseconds, in 10 millisecond steps, using the initial condition specified in the capacitor's card.

Once having loaded this netlist into NGSPICE and issuing the `run` command, we may type `plot v(1)` and get the following output in its own window. As with the previous (DC) analysis, there is no need to specify the analysis type in the `plot` instruction (i.e. `plot v(1)` rather than `plot tran v(1)`) because NGSPICE takes its analysis cue from the `.tran` card in the netlist. In fact, the `.plot tran v(1)` card in the netlist is entirely ignored (and could have been omitted!) when using NGSPICE in interactive mode:



As with the `print` command, we may issue a `plot all` instruction at the command line which

will prompt NGSPICE to plot *all* variables in the simulation. This may make for a cluttered result when done with complex circuits containing many nodes, but in simple cases such as this example it may be more convenient to simply enter `plot all` rather than specify each of the desired variables one by one.

2.4.7 Issuing multiple commands in a single line

A very convenient feature of NGSPICE's interactive command line is its support for multiple commands in a single typed line. This is useful if you wish to edit the netlist and re-run the simulation without re-starting NGSPICE. Instead of typing in `source test.cir` followed by `run` followed by any specific analysis commands such as `print` and/or `plot` commands, it is possible to type all these commands on a single line in the interactive window (separated by semicolons), after which the entire string of commands may be repeated by pressing the "up" arrow key followed by the "Enter" key.

Consider for example the following sequence of commands, typically entered one command at a time in the NGSPICE interactive environment to read, execute, and finally plot data from a netlist file named `test.cir`:

```
source test.cir

run

plot v(2) v(4,3)
```

These three commands may alternatively be entered at once on a single line, then recalled with a single press of the "up" arrow key, thus conserving many keystrokes and shortening the test/development cycle:

```
source test.cir ; run ; plot v(2) v(4,3)
```

2.5 Idiosyncrasies of SPICE

SPICE, particularly early versions such as 2G6, is intolerant of certain omissions and circuit topologies. Some of them are listed here.

2.5.1 Beginning and ending cards

Every SPICE deck must begin with a "title" line of plain text. I typically insert a comment (a line beginning with a `*` character) in the first line, but a comment is not strictly necessary. The deck cannot begin with a component or analysis description.

Similarly, every SPICE deck must finish with an `.end` card to instruct the program to stop its analysis. There should be no lines past the `.end` card, not even blank lines! Similarly, the `.end` line should not be terminated with either a linefeed nor a carriage return character; i.e. do *not* press the Enter key when typing in this last line! SPICE version 2G6 will still process the deck properly with a terminated `.end` card, but it generates an annoying *missing .end card* statement anyway.

2.5.2 Node zero

Every SPICE deck must contain reference to node zero (0). Node zero is not just the default "ground" reference point in a circuit, it is a *necessary* point of reference in order for SPICE to perform its mathematical analyses of the circuit. Furthermore, every other node in the circuit must have some DC path to node 0 (ground) or else SPICE will refuse to analyze the circuit, even if the specified analysis is not DC.

2.5.3 Current measurement

Early versions of SPICE lacked the ability to print or plot values for current through any component but a voltage source. Therefore, if you need to display the calculated current at any point in a circuit being analyzed by a legacy version of SPICE, you must insert special "dummy" voltage sources (set to zero volts each) in the circuit, and then instruct the `.print` or `.plot` analysis statements to display the current through those "dummy" sources.

Alternatively, you may insert low-valued "shunt" resistors in series with the point of interest through which you wish to measure current, and then have SPICE measure the voltage(s) across the resistor(s), just the same as you might do for any real circuit where you lack an ammeter suitable for measuring current. So long as these shunt resistor values are considerably less than the other resistances through which you need to measure current, their impact on the circuit will be negligible. Shunt resistor values of 1 Ω are common for many practical current-measurement applications in the milliAmpere range. For greater currents, shunt resistances of 1 mΩ or even 1 $\mu\Omega$ may be used.

Interestingly, the mathematical sign of the calculated current is negative when the voltage source in question is actually functioning as a source (i.e. conventional current flow out the + terminal and in the − terminal). In order to display a positive current value, current must be entering the voltage source's + terminal and exiting the − terminal, like a load.

2.5.4 Open and short circuits

The fundamental problem with open or shorted circuits is that either condition creates an *undefined* mathematical quantity that SPICE cannot compute. Opens create a condition of infinite (undefined) resistance. Shorts create a condition of zero resistance, which leads to infinite (undefined) current.

Since the insertion of a "short" or an "open" condition may be very useful for simulating a failed component, a common strategy in SPICE modeling is to use a resistor having a very low resistance (short) or a very high resistance (open). For example, a resistance with a value of `1e-9` Ohms is a short for all practical purposes. Similarly, a resistance with a value of `1e9` Ohms is tantamount to an open for most applications.

2.5.5 Multiple sources

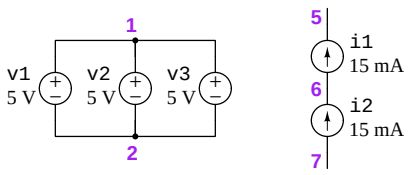
Multiple voltage and/or current sources are permitted in SPICE, but only in certain configurations. Connecting multiple voltage sources in parallel creates a *voltage source loop* error which will cause the analysis to abort, and connecting multiple current sources in series creates a *no dc path to ground* error that is similarly fatal, regardless of source values.

The problem may be understood by considering the internal impedance of each source, and how that impedance "appears" from the perspective of any other source(s). Ideal voltage sources have zero internal impedance, which is why SPICE balks at parallel-connected voltage sources: from the perspective of one voltage source, any other paralleled voltage source appears to be a direct short-circuit. Ideal current sources have infinite internal impedance, which is why SPICE balks at series-connected current sources: from the perspective of one current source, any others connected in series appear to create an open-circuit condition.

It is permissible, however, to connect multiple voltage sources in series with each other. Likewise, multiple current sources connected in parallel are also permissible.

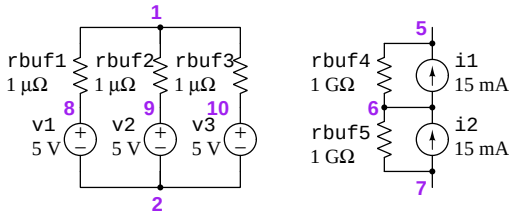
If paralleled voltage sources and/or series-connected current sources are necessary for your circuit design, you may "break up" the offending configuration by inserting *buffer components*. For example, inserting resistors of extremely low value in series with each voltage source before paralleling them will allow the analysis to proceed. A resistor of extremely high value inserted in parallel with a current source will provide the dc path around the other current source that SPICE is looking for, similarly allowing the analysis to proceed.

Impermissible source connections




```
v1 1 2 dc 5
v2 1 2 dc 5
v3 1 2 dc 5
*
i1 6 5 dc 15e-3
i2 7 6 dc 15e-3
```

Permissible source connections




```
v1 8 2 dc 5
v2 9 2 dc 5
v3 10 2 dc 5
rbuf1 1 8 1e-6
rbuf2 1 9 1e-6
rbuf3 1 10 1e-6
*
i1 6 5 dc 15e-3
i2 7 6 dc 15e-3
rbuf4 5 6 1e9
rbuf5 6 7 1e9
```

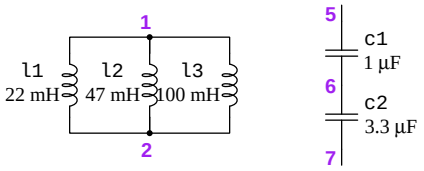
2.5.6 Multiple inductors/capacitors

Similar problems arise when connecting multiple inductors directly in parallel with each other, or multiple capacitors directly in series with each other. SPICE views an inductor as being a short (zero resistance) under DC conditions, and a capacitor as being an open (infinite resistance) under DC conditions. As with multiple sources, the problem may be understood by considering the DC resistance of each component as seen from the other components. Parallel-connected inductors are problematic because any attempt to analyze the behavior of one inductor is thwarted by the apparent short-circuit formed by the other inductor(s); series-connected capacitors are problematic because any attempt to analyze the behavior of one capacitor is thwarted by the apparent open-circuit formed by the other capacitor(s).

Likewise, SPICE cannot tolerate any voltage source being connected in parallel with any inductor, nor any current source being connected in series with any capacitor.

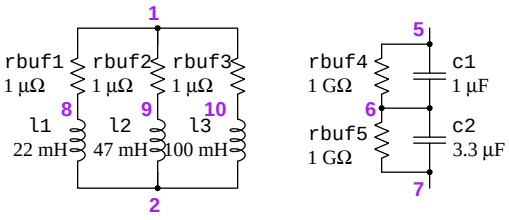
If any of these offending configurations are necessary for your circuit design, you may skirt the problem by inserting buffer components as previously described:

Impermissible inductor/capacitor connections




```
l1 1 2 22e-3
l2 1 2 47e-3
l3 1 2 100e-3
*
c1 5 6 1e-6
c2 6 7 3.3e-6
```

Permissible inductor/capacitor connections




```
l1 8 2 22e-3
l2 9 2 47e-3
l3 10 2 100e-3
rbuf1 1 8 1e-6
rbuf2 1 9 1e-6
rbuf3 1 10 1e-6
*
c1 5 6 1e-6
c2 6 7 3.3e-6
rbuf4 5 6 1e9
rbuf5 6 7 1e9
```

Chapter 3

SPICE component descriptions

To review, here are some of the "cardinal rules" for writing SPICE netlists:

- The first line (card) of the netlist is the Title. It cannot be omitted.
- The last line (card) of the netlist is the `.end` command. It cannot be omitted.
- Each and every unique connection point in the circuit must be assigned a number called a *node*. This is how you describe the "shape" of the circuit to SPICE: by describing which nodes each component connects to. Components sharing common node numbers are connected to each other. There *must* be a node 0, and this is the "Ground" node of the circuit.
- Comment lines (cards) must begin with an asterisk symbol (`*`). These are lines of text inserted into the netlist strictly for the benefit of human readers. SPICE skips over them.

Note that SPICE is case-insensitive. Any instances of capitalization in the following SPICE examples are included solely for clarity and readability, and do not matter when entered into a SPICE netlist.

3.1 Independent voltage sources

General format for DC and AC analyses:

[**V***name*] [+node_ID] [−node_ID] [DC/AC *voltage*] [AC *voltage phaseangle*]

The first node specified is always the positive (+) terminal of the voltage source, while the second node is always the negative (−) terminal.

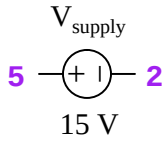
3.1.1 Example: DC source

- Name = *supply*
- Polarity = *+ on node 5 and − on node 2*
- Value = *15 Volts DC*

SPICE element description

```
Vsupply 5 2 dc 15
```

Schematic representation



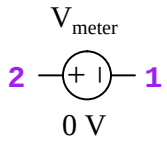
3.1.2 Example: "Dummy" source

- Name = *meter*
- Polarity = *+ on node 2 and − on node 1*
- Value = *0 Volts*

SPICE element description

```
Vmeter 2 1 0
```

Schematic representation



"Dummy" voltage sources are useful in SPICE netlists, to serve as points of measurement for current. Legacy versions of SPICE could not display a calculated current value for any element other than a voltage source, so a "dummy" voltage source with a value of 0 Volts served the purpose quite well.

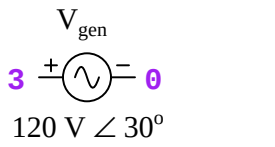
3.1.3 Example: AC source

- Name = *gen*
- Polarity = *+ on node 3 and − on node 0*
- Value = *120 Volts ∠ 30* degrees

SPICE element description

```
Vgen 3 0 ac 120 30
```

Schematic representation



AC sources specified in this manner are assumed to be sinusoidal in waveform with a constant magnitude and phase shift, and the analysis performed by SPICE will be in the frequency domain.

In addition to steady-state DC and AC sources, SPICE also supports multiple types of time-dependent sources, useful for simulating waveforms and pulse trains in the time domain.

General format for time-domain analyses:

[**V***name*] [+node_ID] [−node_ID] [*waveform_type*] ([*option1 option2*] [*option3* $\cdots$])

The first node specified is always the positive (+) terminal of the voltage source, while the second node is always the negative (−) terminal. Five different waveform types are supported, each with their own options. The waveform types are Sinusoidal (`sin`), Pulse (`pulse`), Exponential (`exp`), Piecewise Linear (`pwl`), and Frequency-Modulated Sinusoidal (`sffm`).

No provision for phase angle exists for AC time-domain sources. Instead, one must make creative use of the start delay time option. A positive start delay time means that the waveform's start becomes delayed, representing a negative phase shift angle. Conversely, a negative start delay time means the waveform has an "early" start, or a positive phase shift angle. Unfortunately, SPICE version 2G6 does not support negative start delay time values.

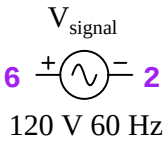
3.1.4 Example: Sinusoidal source

- Name = *signal*
- Polarity = *+ on node 6 and − on node 2*
- Wave type = *sinusoidal*
- DC offset = *10 Volts*
- Peak amplitude = *120 Volts*
- Frequency = *60 Hz*
- Start delay = *8 milliseconds*
- Damping factor = *0 seconds*$^{-1}$ (i.e. an undamped waveform)

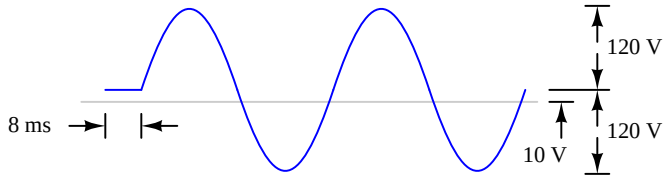
SPICE element description

```
Vsignal 6 2 sin(10 120 60 8m 0)
```

Schematic representation



Waveform



As opposed to a simple AC voltage sources which is assumed to be sinusoidal in waveform and constant in magnitude (i.e. no growth or decay over time), this source is explicitly sinusoidal, and the analysis performed by SPICE will be in the time domain.

Note that the damping factor assumes a decaying signal with a positive value. In order to generate an exponentially growing waveform you will need to use a *negative* value for the damping factor. In other words, the damping factor is equal to $-\sigma$.

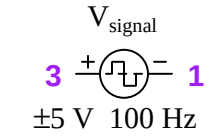
3.1.5 Example: Pulse source

- Name = *signal*
- Polarity = *+ on node 3 and − on node 1*
- Wave type = *pulse*
- Initial value = −5 *Volts*
- Pulsed value = 5 *Volts*
- Start delay = *3 milliseconds*
- Rise time = *1 millisecond*
- Fall time = *2 millisecond*
- Pulse width = *5 milliseconds*
- Period = *10 milliseconds*

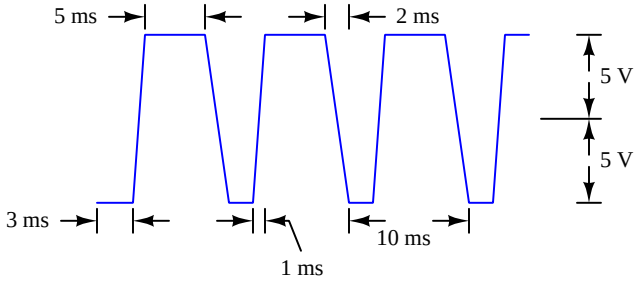
SPICE element description

```
Vsignal 3 1 pulse (-5 5 3m 1m 2m 5m 10m)
```

Schematic representation



Waveform



Like other time-dependent sources, a `pulse` source requires analysis in the time domain using the `.tran` analysis option.

3.2 Independent current sources

General format for DC and AC analyses:

[**I***name*] [sink_node_ID] [source_node_ID] [DC/AC *current*] [AC *current phaseangle*]

The first node specified is always the terminal where current (conventional flow) enters the current source, while the second node is always the terminal where current exits the source.

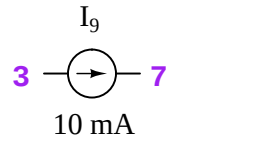
3.2.1 Example: DC source

- Name = *9*
- Polarity = *current enters node 3 and exits node 7*
- Value = *10 milliAmperes*

SPICE element description

```
I9 3 7 dc 10e-3
```

Schematic representation



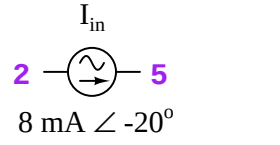
3.2.2 Example: AC source

- Name = *in*
- Polarity = *current enters node 2 and exits node 5*
- Value = *8 milliAmperes ∠ -20* degrees

SPICE element description

```
Iin 2 5 ac 8m -20
```

Schematic representation



3.3 Resistors

General format:

[**R***name*] [node_ID] [node_ID] [*value*]

As with all SPICE elements, resistor values may be specified using plain decimal notation, power-of-ten notation, or metric-prefix notation as alternatively shown in the example.

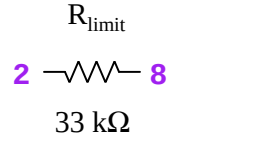
3.3.1 Example

- Name = *limit*
- Nodes = *connected between nodes 2 and 8*
- Value = *33 kilo-Ohms* Ω

SPICE element description

```
Rlimit 2 8 33000
(or)
Rlimit 2 8 33e3
(or)
Rlimit 2 8 33k
```

Schematic representation



3.4 Capacitors

General format:

[**C***name*] [+node_ID] [−node_ID] [*value*] [**IC=** *initial_voltage*]

An important caveat when using capacitors in a SPICE netlist is that SPICE cannot tolerate multiple capacitors connected directly in series. If your circuit design requires this configuration, you will need to insert a "buffer" component (e.g. a resistor with an extremely high resistance value) in parallel with one or more of the capacitors so that the offending components are no longer directly in series with each other.

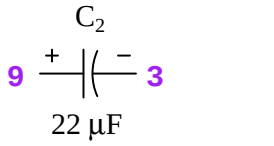
3.4.1 Example: Capacitor with initial charge

- Name = *2*
- Polarity = *+ on node 9 and − on node 3, initially charged to 3.5 Volts*
- Value = *22 micro-Farads*

SPICE element description

```
C2 9 3 22e-6 ic=3.5
```

Schematic representation



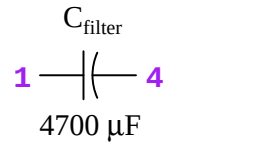
3.4.2 Example: Uncharged capacitor

- Name = *filter*
- Nodes = *connected between nodes 1 and 4, no initial voltage*
- Value = *4700 micro-Farads*

SPICE element description

```
Cfilter 1 4 4700e-6
```

Schematic representation



3.5 Inductors

General format:

[**L***name*] [sink_node_ID] [source_node_ID] [*value*] [**IC=** *initial_current*]

An important caveat when using inductors in a SPICE netlist is that SPICE cannot tolerate multiple inductors connected directly in parallel, nor can it abide any voltage source connected directly in parallel with an inductor. If your circuit design requires either of these configurations, you will need to insert a "buffer" component (e.g. a resistor with a negligible resistance value) between the inductors or inductor/voltage source so that the offending components are no longer directly in parallel with each other.

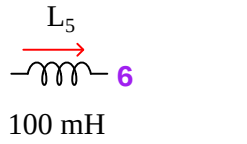
3.5.1 Example: Inductor with initial charge

- Name = *5*
- Polarity = *current enters node 2 and exits node 6, initially carrying 25 milliAmperes*
- Value = *100 milliHenrys*

SPICE element description

```
L5 2 6 100e-3 ic=25e-3
```

Schematic representation



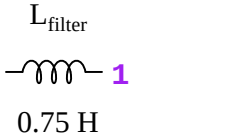
3.5.2 Example: Uncharged inductor

- Name = *filter*
- Nodes = *connected between nodes 8 and 1, no initial current*
- Value = *0.75 Henrys*

SPICE element description

```
Lfilter 8 1 0.75
```

Schematic representation



3.6 Transformers

Transformers do not exist as independent entities in SPICE. Instead, one must specify the windings of a transformer as separate inductors, then specify a *coupling* factor k magnetically linking those inductors. The relationship between mutual inductance (M), k, and the two inductor values (L_1 and L_2) are given by the formula $M = k\sqrt{L_1 L_2}$.

General format:

[**K***name*] [**L***name_1*] [**L***name_2*] [*value*]

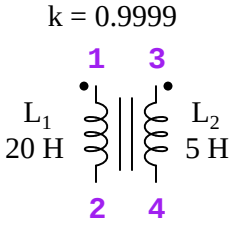
3.6.1 Example: 2:1 ratio step-down transformer

- Name = *xfmr1*
- Nodes = *primary inductor L1 connected between nodes 1 and 2, secondary inductor L2 connected between nodes 3 and 4*
- Value = *0.9999*

SPICE element description

```
L1 1 2 20
L2 3 4 5
Kxfmr1 L1 L2 0.9999
```

Schematic representation



Note how the ratio of primary to secondary inductance is equal to the square of the turns ratio, because inductance is proportional to the square of the winding turns. Thus, in order to achieve a 2:1 turns ratio, we need a 4:1 inductance ratio.

3.7 Transmission lines

Transmission lines are four-terminal devices, much like dependent sources. Rather than specifying a physical length for the transmission line, we may *either* specify delay time (i.e. the time it takes for the signal to propagate along the entire length of the line) *or* the signal frequency and corresponding electrical length of the line (in units of wavelengths). These two methods of specifying line length are exclusive to each other. If using the frequency option, the electrical line length defaults to 0.25 ($\frac{\lambda}{4}$) unless specified otherwise.

General format:

[**T***name*] [node_ID] [node_ID] [node_ID] [node_ID] [**Z0=** *characteristic impedance*] [**TD=** *delay time*] [**F=** *frequency* and **NL=** *electrical length*]

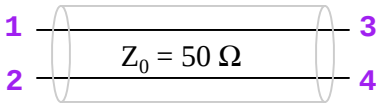
3.7.1 Example: 50-Ohm transmission line with 10 nanosecond delay

- Name = *cable*
- Nodes = *one end of cable has nodes 1 and 2, other end of cable has nodes 3 and 4*
- Delay = *10e-9 seconds*

SPICE element description

```
Tcable 1 2 3 4 z0=50 td=10e-9
```

Schematic representation



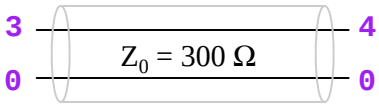
3.7.2 Example: half-wavelength (at 35 MHz) 300-Ohm transmission line

- Name = *feedline*
- Nodes = *one end of cable has nodes 3 and 0, other end of cable has nodes 4 and 0*
- Frequency = *35 MHz*
- Electrical length = *0.5 wavelengths*

SPICE element description

```
Tcable 3 0 4 0 z0=300 f=35e6 nl=0.5
```

Schematic representation



3.8 Linear dependent sources

While independent sources output a prescribed voltage or current, dependent sources output a voltage or current as a function of some other voltage or current signal in the circuit. While there is no real-world equivalent component for a dependent source, dependent sources are useful for modeling a variety of phenomena and are often used as portions of a SPICE model for some real-world component.

SPICE offers dependent sources in four different types:

- Voltage-controlled voltage source (`E`)
- Voltage-controlled current source (`G`)
- Current-controlled voltage source (`H`)
- Current-controlled current source (`F`)

Voltage-controlled sources (types `E` and `G`) have four nodes specified in their SPICE card: two nodes for the input terminals of the controlling voltage, and two nodes for the output terminals. Current-controlled sources (types `H` and `F`) only specify the two output terminal nodes, the controlling current being specified by the name of some independent voltage source used as a current sensor.

General formats:

[**E***name*] [+output_node_ID] [−output_node_ID] [+input_node_ID] [−input_node_ID] [*gain*]

[**G***name*] [sink_node_ID] [source_node_ID] [+input_node_ID] [−input_node_ID] [*gain*]

[**H***name*] [+output_node_ID] [−output_node_ID] [**V***name*] [*gain*]

[**F***name*] [sink_node_ID] [source_node_ID] [**V***name*] [*gain*]

In each case, the *gain* value is the ratio of output to input, regardless of units (e.g. Volts output per Volt input for a type `E` source; Amperes output per Volt input for a type `G` source, etc.).

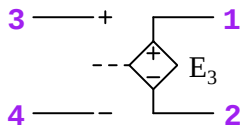
3.8.1 Example: voltage-controlled voltage source

- Name = *3*
- Polarity = *input on nodes 3 (+) and 4 (−) ; output on nodes 1 (+) and 2 (−)*
- Gain = *0.5 Volts output per Volt input*

Spice element description

```
E3 1 2 3 4 0.5
```

Schematic representation



$V_{out} = (0.5)(V_{in})$

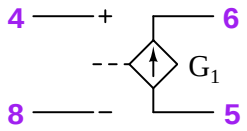
3.8.2 Example: voltage-controlled current source

- Name = *1*
- Polarity = *input on nodes 4 (+) and 8 (−) ; output current enters node 5 and exits node 6*
- Gain = *2.3 Amperes output per Volt input*

Spice element description

```
G1 5 6 4 8 2.3
```

Schematic representation



$I_{out} = (2.3)(V_{in})$

3.9 Nonlinear dependent sources

While independent sources output a prescribed voltage or current, dependent sources output a voltage or current as a function of some other voltage or current signal in the circuit. A *nonlinear* source is able to implement a mathematical function relating one or more inputs to its output. While there is no real-world equivalent component for a dependent source, dependent sources are useful for modeling a variety of phenomena and are often used as portions of a SPICE model for some real-world component.

Note: these sources are not available in legacy versions of SPICE, but are supported in NGSPICE.

General format:

[**B***name*] [+output_node_ID] [−output_node_ID] [i= *expression*] [v= *expression*]

Supported mathematical functions include the arithmetic basic operations of addition (`+`), subtraction (`-`), multiplication (`*`), division (`/`), and powers (`^`) as well as many other functions. Exponential (`exp`) and logarithmic (both `ln` and `log`), trigonometric , hyperbolic, and other functions are supported too.

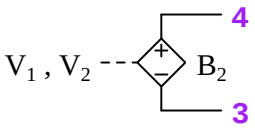
3.9.1 Example: multiplier

- Name = *2*
- Polarity = *output on nodes 4 (+) and 3 (−)*
- Function = *voltage v(1) times voltage v(2)*

Spice element description

```
B2 4 3 v=(v(1)*v(2))
```

Schematic representation



$V_{out} = (V_1)(V_2)$

3.10 Diodes

Semiconductor diodes, like other semiconductor components in SPICE, must be accompanied by a `.model` card somewhere in the netlist specifying the model name and parameters.

General format:

[**D***name*] [anode_node_ID] [cathode_node_ID] [*model_name*] [**IC=** *initial_voltage*]
[**.MODEL**] [*model_name*] [D] [**Parameter1=** *value*] [**Parameter2=** *value*] [$\cdots$]

The following is a list of parameters, any of which may be included in the `.model` card:

- IS = Reverse saturation current (default = 1×10^{-14} Amperes)
- N = Emission coefficient (default = 1)
- RS = Ohmic resistance (default = 0 Ohms)
- TT = Transit time (default = 0 seconds)
- CJO = Zero-bias junction capacitance (default = 0 Farads)
- VJ = Junction potential (default = 1 Volt)
- M = Grading coefficient (default = 0.5)
- EG = Activation energy (default = 1.11 electron-Volts, representing Silicon)
- BV = Breakdown voltage (default = infinite Volts)
- IBV = Current at breakdown voltage (default = 1×10^{-3} Amperes)

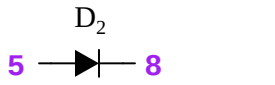
3.10.1 Example: Generic diode

- Name = *2*
- Polarity = *anode on node 5 and cathode on node 8*
- Model = *acme*, generic diode

SPICE element description

```
D2 5 8 acme
.MODEL acme d
```

Schematic representation



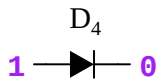
3.10.2 Example: 1N4001

- Name = *4*
- Polarity = *anode on node 1 and cathode on node 0*
- Model = *1N4001* rectifying diode

SPICE element description

```
D4 1 0 1N4001
.MODEL 1N4001 d
+ IS=1.2e-8 RS=0.04
+ N=1.83 EG=0.6
+ BV=50 IBV=5e-8
+ CJO=1e-11 VJ=0.65
+ M=0.5 TT=1e-9
```

Schematic representation



3.11 Bipolar Junction Transistors (BJTs)

BJTs, like other semiconductor components in SPICE, must be accompanied by a `.model` card somewhere in the netlist specifying the model name and parameters. This is where the type of BJT (NPN or PNP) is specified.

General format:

[**Q***name*] [collector_node_ID] [base_node_ID] [emitter_node_ID] [*model_name*]
[**.MODEL**] [*model_name*] [NPN *or* PNP] [**Parameter1=** *value*] [**Parameter2=** *value*] [$\cdots$]

The following is a list of parameters, any of which may be included in the `.model` card:

- IS = Reverse saturation current (default = 1×10^{-14} Amperes)
- BF = Forward current gain (default = 100)
- BR = Reverse current gain (default = 1)
- NF = Forward emission coefficient (default = 1)
- NR = Reverse emission coefficient (default = 1)
- VAF = Forward Early voltage (default = infinite Volts)
- VAR = Reverse Early voltage (default = infinite Volts)
- RC = Collector ohmic resistance (default = 0 Ohms)
- RB = Base ohmic resistance (default = 0 Ohms)
- RE = Emitter ohmic resistance (default = 0 Ohms)
- TF = Forward transit time (default = 0 seconds)
- TR = Reverse transit time (default = 0 seconds)
- CJE = Zero-bias B-E junction capacitance (default = 0 Farads)
- CJC = Zero-bias B-C junction capacitance (default = 0 Farads)
- VJE = B-E junction potential (default = 0.75 Volt)
- VJC = B-C junction potential (default = 0.75 Volt)
- MJE = B-E grading coefficient (default = 0.33)
- MJC = B-C grading coefficient (default = 0.33)

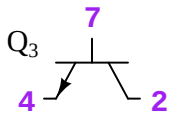
3.11.1 Example: Generic NPN transistor

- Name = *3*
- Terminals = *collector on node 2 and base on node 7 and emitter on node 4*
- Model = *mynpn*, generic NPN

SPICE element description

```
Q3 2 7 4 mynpn
.MODEL mynpn npn
```

Schematic representation



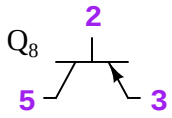
3.11.2 Example: 2N2907

- Name = *8*
- Terminals = *collector on node 5 and base on node 2 and emitter on node 3*
- Model = *2N2907* small-signal PNP

SPICE element description

```
Q8 5 2 3 2N2907
.MODEL 2N2907 pnp
+ IS=3e-12 BF=395
+ NF=1.15 VAF=42
+ VJE=0.69 VJC=0.41
```

Schematic representation



3.12 Junction Field-Effect Transistors (JFETs)

JFETs, like other semiconductor components in SPICE, must be accompanied by a `.model` card somewhere in the netlist specifying the model name and parameters. The channel type is specified in the `.model` card: NJF for N-channel and PJF for P-channel.

General format:

[**J***name*] [drain_node_ID] [gate_node_ID] [source_node_ID] [*model_name*]
[**.MODEL**] [*model_name*] [NJF *or* PJF] [**Parameter1=** *value*] [**Parameter2=** *value*] [$\cdots$]

The following is a list of parameters, any of which may be included in the `.model` card:

- VTO = Threshold pinch-off voltage (default = -2.0 Volts)
- BETA = Transconductance (default = 10^{-4} A/V^2)
- LAMBDA = Channel length modulation (default = 0 V^{-1})
- RD = Drain ohmic resistance (default = 0 Ohms)
- RS = Source ohmic resistance (default = 0 Ohms)
- CGS = Zero-bias G-S junction capacitance (default = 0 Farads)
- CGD = Zero-bias G-D junction capacitance (default = 0 Farads)
- IS = Gate junction saturation current (default = 1×10^{-14} Amperes)
- PB = Gate junction potential (default = 1.0 Volt)

The mathematical sign of the threshold pinch-off voltage (`VTO`) is important. Since JFETs are normally-on devices, and the gate-channel PN junction must be reverse-biased in order to turn the transistor off, the value for `VTO` is negative. Interestingly, this negative sign is true regardless of channel type (i.e. N-channel or P-channel) although the actual polarity necessary for reverse-biasing that junction is different for the two channel types.

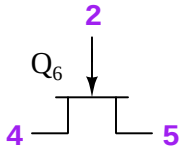
3.12.1 Example: Generic N-channel JFET

- Name = *6*
- Terminals = *drain on node 4 and gate on node 2 and source on node 5*
- Model = *nchannel*, generic NJF

SPICE element description

```
J6 4 2 5 nchannel
.MODEL nchannel njf
```

Schematic representation



3.13 Metal-Oxide Field-Effect Transistors (MOSFETs)

MOSFETs, like other semiconductor components in SPICE, must be accompanied by a `.model` card somewhere in the netlist specifying the model name and parameters. The channel type is specified in the `.model` card: NMOS for N-channel and PMOS for P-channel.

General format:

[**M***name*] [drain_node_ID] [gate_node_ID] [source_node_ID] [bulk_node_ID] [*model_name*]

[**.MODEL**] [*model_name*] [NMOS *or* PMOS] [**Parameter1=** *value*] [**Parameter2=** *value*] [$\cdots$]

Note: the "bulk" terminal describes the semiconductor substrate upon which the MOSFET is built, and is optional. The following is a list of parameters, any of which may be included in the `.model` card:

- VTO = Threshold pinch-off voltage (default = 0 Volts)
- KP = Transconductance (default = 2×10^{-5} A/V^2)
- GAMMA = Bulk threshold (default = 0 V$^{\frac{1}{2}}$)
- LAMBDA = Channel length modulation (default = 0 V^{-1})
- RD = Drain ohmic resistance (default = 0 Ohms)
- RS = Source ohmic resistance (default = 0 Ohms)
- RSH = Drain and source diffusion sheet resistance (default = 0 Ohms)
- CBD = Zero-bias B-D junction capacitance (default = 0 Farads)
- CBS = Zero-bias B-S junction capacitance (default = 0 Farads)
- CJ = Zero-bias bulk junction bottom capacitance (default = 0 Farads)
- MJ = Bulk junction grading coefficient (default = 0.5)
- CJSW = Zero-bias bulk junction sidewall capacitance (default = 0 Farads)
- MJSW = Bulk junction sidewall grading coefficient (default = 0.33)
- IS = Bulk junction saturation current (default = 1×10^{-14} Amperes)
- PB = Bulk junction potential (default = 1.0 Volt)
- CGDO = G-D overlap capacitance per unit channel width (default = 0 Farads/meter)
- CGSO = G-S overlap capacitance per unit channel width (default = 0 Farads/meter)

- CGBO = G-B overlap capacitance per unit channel width (default = 0 Farads/meter)
- TOX = Oxide thickness (default = infinite meters)
- LD = Lateral diffusion (default = 0 meters)

The same device card is used for enhancement-mode as well as depletion-mode MOSFETs, the only difference being the value assigned to the threshold pinch-off voltage (`VTO`). Enhancement-mode MOSFETs are normally-off devices and thus are "pinched off" at zero gate voltage, requiring `VTO` to be a positive value for NMOS devices and a negative value for PMOS devices. Depletion-mode MOSFETs are normally-on devices and need a "reverse-bias" gate voltage to turn off, requiring `VTO` to be a negative value for NMOS devices and a positive value for PMOS devices.

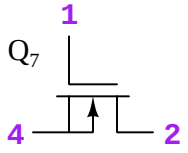
3.13.1 Example: Generic N-channel depletion-type MOSFET

- Name = *7*
- Terminals = *drain on node 2 and gate on node 1 and source on node 4 (bulk connected to source)*
- Model = *ndmos*, generic depletion-type NMOS

SPICE element description

```
M7 2 1 4 4 ndmos
.MODEL ndmos VTO=-3
```

Schematic representation



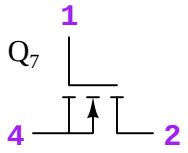
3.13.2 Example: Generic N-channel enhancement-type MOSFET

- Name = *7*
- Terminals = *drain on node 2 and gate on node 1 and source on node 4 (bulk connected to source)*
- Model = *nemos*, generic enhancement-type NMOS

SPICE element description

```
M7 2 1 4 4 nemos
.MODEL nemos VTO=2
```

Schematic representation



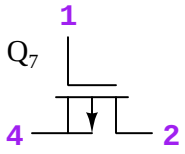
3.13.3 Example: Generic P-channel depletion-type MOSFET

- Name = *7*
- Terminals = *drain on node 2 and gate on node 1 and source on node 4 (bulk connected to source)*
- Model = *pdmos*, generic depletion-type PMOS

SPICE element description

```
M7 2 1 4 4 pdmos
.MODEL pdmos VTO=3
```

Schematic representation



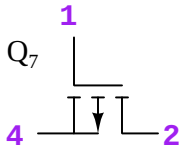
3.13.4 Example: Generic P-channel enhancement-type MOSFET

- Name = *7*
- Terminals = *drain on node 2 and gate on node 1 and source on node 4 (bulk connected to source)*
- Model = *pemos*, generic enhancement-type PMOS

SPICE element description

```
M7 2 1 4 4 pemos
.MODEL pemos VTO=-2
```

Schematic representation



3.14 Subcircuits

Computer programming languages provide the means to perform *subroutines*, which consist of collections of code (instructions) separate from the main body of the program, but which may be "called" from the main program as many times as needed. This is used in applications where a particular algorithm or set of instructions must be repeatedly executed: rather than have those instructions appear repeated throughout the program, they are entered as a subroutine and that subroutine is called by name as many times as necessary.

SPICE has the ability to do the equivalent when simulating electric circuits. A collection of components that would otherwise need to be repeatedly entered in the netlist can be defined once as a *subcircuit*, and then that subcircuit may be called by name as often as desired elsewhere in the netlist. Subcircuits are useful when the overall circuit is comprised of multiple identical sub-networks, because it makes the netlist shorter and easier to understand to a human reader.

[**X**] [*subcircuit_name*] [node_1] [node_2] [$\cdots$]

[**.SUBCKT***name*] [node_1] [node_2] $\cdots$]

All node numbers with the exception of node 0 used within the `.SUBCKT` card are "local" to that card and may be re-used for other purposes elsewhere in the netlist.

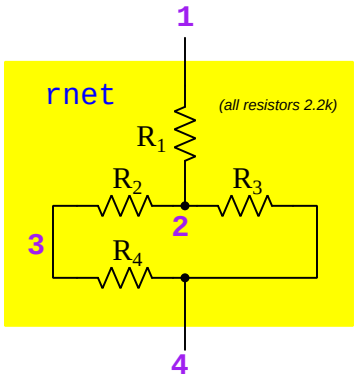
3.14.1 Example: resistor subnetwork

- Name = *rnet*
- Terminals = *first node is upper, second is lower*

SPICE subcircuit description

```
.SUBCKT rnet 1 4
R1 1 2 2200
R2 2 3 2200
R3 2 4 2200
R4 3 4 2200
.ENDS rnet
```

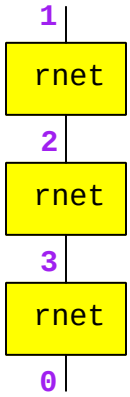
Schematic representation



SPICE subcircuit usage

```
X1 1 2 rnet
X2 2 3 rnet
X3 3 0 rnet
```

Schematic representation



3.14.2 Example: solar cell array

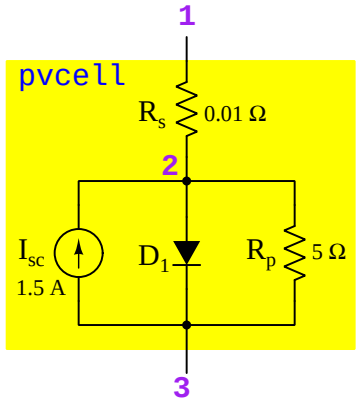
The simulation of a solar cell array is an excellent use of both subcircuits and semiconductor models in SPICE. Each individual solar cell outputs about the same amount of voltage as the forward drop of a silicon rectifying diode, because a solar cell *is* a silicon PN junction. The larger the cell's junction contact area, the greater its short-circuit current capacity. We may simulate each cell's short-circuit (maximum) current using a current source (I_{sc}) and its PN-junction characteristics using a diode element (D_1) with added resistors representing substrate and inter-cell connection resistances:

- Name = *pvcell*
- Terminals = *first node is positive, second is negative*

SPICE subcircuit description

```
.SUBCKT pvcell 1 3
RS 1 2 0.01
ISC 3 2 1.5
D1 2 3 pnjunc
RP 2 3 5
.MODEL pnjunc d
.ENDS pvcell
```

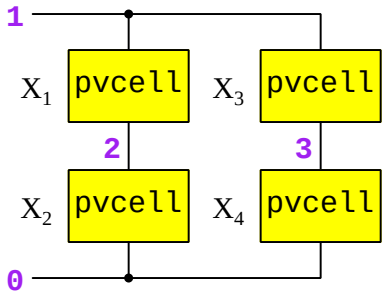
Schematic representation



SPICE subcircuit usage

```
X1 1 2 pvcell
X2 2 0 pvcell
X3 1 3 pvcell
X4 3 0 pvcell
```

Schematic representation



Chapter 4

SPICE analysis descriptions

To review, here are some of the "cardinal rules" for writing SPICE netlists:

- The first line (card) of the netlist is the Title. It cannot be omitted.
- The last line (card) of the netlist is the `.end` command. It cannot be omitted.
- Each and every unique connection point in the circuit must be assigned a number called a *node*. This is how you describe the "shape" of the circuit to SPICE: by describing which nodes each component connect to. Component terminals sharing common node numbers are electrically common (i.e. directly connected to each other). There *must* be a node 0, and this is the "Ground" node of the circuit.
- Comment lines (cards) must begin with an asterisk symbol (`*`). These are lines of text inserted into the netlist strictly for the benefit of human readers. SPICE skips over them.

Note that SPICE is case-insensitive. Any instances of capital letters in the following SPICE analysis descriptions are included solely for clarity and readability.

4.1 DC voltage/current "sweep" analysis

General format:

[**.dc**] [*source_name*] [*start_value*] [*end_value*] [*increment*]

The starting and ending values for the sweep will override any static values specified in the source's line (card).

4.1.1 Example: sweep of voltage source

- Source = *voltage source "v1"*
- Starting value = *2 Volts*
- Ending value = *12 Volts*
- Increment value = *5 Volts*

SPICE analysis description: `.dc v1 2 12 5`

4.1.2 Example: sweep of voltage and current sources

- Source1 = *voltage source "vce"*

  Starting value = *0 Volts*

  Ending value = *20 Volts*

  Increment value = *0.5 Volt*

- Source2 = *current source "ib"*

  Starting value = *0 milliAmperes*

  Ending value = *0.6 milliAmperes*

  Increment value = *0.1 milliAmperes*

SPICE analysis description: `.dc vce 0 20 0.5 ib 0 0.6e-3 0.1e-3`

Multi-source sweeps are useful when plotting "families" of characteristic curves for semiconductor devices, where each curve plotted is at a different controlling signal value. In the example shown, V_{CE} is swept from 0 to 20 Volts at an I_B value of 0 milliAmperes, then swept again from 0 to 20 Volts at I_B = 0.1 mA, then swept again from 0 to 20 Volts at I_B = 0.2 mA, etc.

4.2 AC frequency "sweep" analysis

General format:

[**.ac**] [*linearity*] [*points*] [*start_frequency*] [*end_frequency*]

4.2.1 Example: linear frequency sweep

- Linearity type = *linear*
- Number of points = *100*
- Starting frequency = *400 Hz*
- Ending frequency = *900 Hz*

SPICE analysis description: `.ac lin 100 400 900`

4.2.2 Example: decade logarithmic frequency sweep

- Linearity type = *decade*
- Number of points = *5 per decade*
- Starting frequency = *1 kHz*
- Ending frequency = *100 kHz*

SPICE analysis description: `.ac dec 5 1k 100k`

4.2.3 Example: octave logarithmic frequency sweep

- Linearity type = *octave*
- Number of points = *12 per octave*
- Starting frequency = *440 Hz*
- Ending frequency = *3.52 kHz*

SPICE analysis description: `.ac oct 12 440 3.52e3`

Note: this particular analysis covers four octaves of the frequencies of the equal-tempered Western musical scale, beginning with 440 Hz (concert tuning pitch "A").

4.3 Transient analysis

General format:

[**.tran**] [*interval_time*] [*end_time*] [*start_time*] [**uic**] [*end_frequency*]

This instructs SPICE to perform a time-domain analysis of the circuit, from time $t = 0$ to the specified end time, over intervals of specified length. The starting time is used only for analyses where the printed or plotted results do not begin at $t = 0$; if unspecified it is assumed that the starting time is zero. The `UIC` parameter is optional, instructing SPICE to honor any initial conditions (`IC=`) specified in the component descriptions.

4.3.1 Example: using initial conditions, beginning at time $t = 0$

- Time interval = *10 milliseconds*
- Ending time = *500 milliseconds*

SPICE analysis description: `.tran 10m 500m uic`

4.3.2 Example: using initial conditions, beginning at non-zero time

- Time interval = *30 microseconds*
- Ending time = *200 microseconds*
- Print/plot starting time = *100 microseconds*

SPICE analysis description: `.tran 30u 200u 100u uic`

4.4 Fourier analysis

General format:

[**.four**] [*fundamental_frequency*] [*variable*] [*variable*] [*variable* $\cdots$]

Fourier analysis provides a printed-text summary of the first ten harmonic frequencies of the specified variable(s). This analysis must always be used in conjunction with a *transient* (`.tran`) analysis in the same netlist, since the Fourier transform takes a time-domain function (i.e. transient data in SPICE) and converts it into a frequency-domain function.

4.4.1 Example: analysis of 60 Hz waveform

- Fundamental frequency = *60 Hz*
- Variable = *Voltage between nodes 3 and 1*

SPICE analysis description: `.four 60 v(3,1)`

4.5 Display option: print

General format:

[**.print**] [*analysis_type*] [*variable*] [*variable*] [*variable* $\cdots$]

In order for this display option to function, the netlist (deck) must also contain an analysis line (card).

4.5.1 Example: printing a DC analysis

- Analysis type = *DC* (netlist must contain a `.dc` analysis line)
- First variable = *Voltage between node 4 and Ground*
- Second variable = *Voltage between nodes 6 and 3*
- Third variable = *Current through voltage source "vsupply"*

SPICE analysis description: `.print dc v(4) v(6,3) i(vsupply)`

4.5.2 Example: printing an AC analysis

- Analysis type = *AC* (netlist must contain an `.ac` analysis line)
- First variable = *Voltage magnitude between node 4 and Ground*
- Second variable = *Voltage phase angle between node 4 and Ground*
- Third variable = *Current magnitude through voltage source "vsupply"*
- Fourth variable = *Current phase angle through voltage source "vsupply"*

SPICE analysis description: `.print ac vm(4) vp(4) im(vsupply) ip(vsupply)`

Note that SPICE version 2 defaults to *degrees* as the unit for phase angles, while SPICE version 3 defaults to *radians*. If degrees are desired while running newer versions of SPICE, you may include the following cards in the netlist deck to control units:

```
.control
set units=degrees
.endc
```

4.6 Display option: plot

General format:

[**.plot**] [*analysis_type*] [*variable*] [*variable*] [*variable* $\cdots$]

The `.plot` display accepts all the same parameters as the `.print` display, but instead of merely printing a list of numbers it plots a graph of the variables over the domain of the analysis type. In order for this display option to function, the netlist (deck) must also contain an analysis line (card).

Since the purpose of the `.plot` display is to produce a *graph*, the analysis line really needs to "sweep" over multiple points.

4.6.1 Example: plotting a DC analysis

- Analysis type = *DC* (netlist must contain a `.dc` analysis line)
- First variable = *Voltage between nodes 4 and 1*

SPICE analysis description: `.plot dc v(4,1)`

4.6.2 Example: plotting an AC analysis

- Analysis type = *AC* (netlist must contain an `.ac` analysis line)
- First variable = *Voltage magnitude between nodes 4 and 1*
- Second variable = *Voltage phase angle between nodes 4 and 1*

SPICE analysis description: `.plot ac vm(4,1) vp(4,1)`

Note that SPICE version 2 defaults to *degrees* as the unit for phase angles, while SPICE version 3 defaults to *radians*. If degrees are desired while running newer versions of SPICE, you may include the following cards in the netlist deck to control units:

```
.control
set units=degrees
.endc
```

It is important to note that an AC plot is in the frequency domain; that is to say, the x axis of the plot will represent frequency while the y axis will represent the variable(s) specified in the `.plot` line. This is useful for generating Bode plots. An AC analysis will *not* plot waveforms as a function of time. That feature is delivered by `plot` only when the netlist specifies a *transient* analysis rather than an *AC* analysis.

4.6.3 Example: plotting a transient analysis

- Analysis type = *transient* (netlist must contain a `.tran` analysis line)
- First variable = *Voltage between nodes 7 and 3*

SPICE analysis description: `.plot tran v(7,3)`

This plot will show the waveform as a function of time, with the plot's x axis expressed in units of time.

4.6.4 Example: plotting parametric functions

- Analysis type = *transient* (netlist must contain a `.tran` analysis line)
- First variable = *Voltage between nodes 1 and 0*
- First variable = *Voltage between nodes 5 and 8*

SPICE analysis description: `.plot tran v(1) vs v(5,8)`

Not all versions of SPICE support the "versus" option, but in those that do, this is useful for plotting one circuit parameter against another, rather than plot circuit parameter(s) over time. Use this option to create Lissajous figures, plotting one sinusoidal voltage against another at different frequencies and/or phase shifts.

4.7 Display option: width

General format:

[**.width**] [**out=** *characters*]

When SPICE outputs plain-text to the computer terminal, it assumes a 120-character display width, which is fitting for legacy teletype machines, but actually exceeds the standard electronic terminal display width of 80 characters. For this reason, especially when using the `.plot` output option, it is advisable to also use the `.width` option set to 80 characters to limit the width of the text display.

4.7.1 Example

- Display width = *80 characters*

SPICE analysis description: `.width out=80`

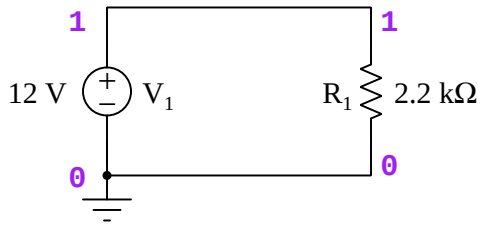
Chapter 5

Primitive circuit examples

"Primitive" circuits consist of the minimum number of components to demonstrate a concept. In most cases they consist of one source and one load directly connected together. They are presented here as a form of "Hello World" example to show how SPICE netlists and analyses are formatted.

5.1 DC voltage source with .op analysis

Circuit schematic diagram (with node numbers listed). Note how the voltage source and the resistor are connected between the same pair of nodes: 1 and 0. This tells SPICE they are parallel to each other, because the upper terminals of each component are electrically common (node 1) and the lower terminals of each component are also electrically common (node 0). Note also how ground is defined in SPICE as node number *zero*, which must be included in every netlist:



SPICE netlist:

```
* SPICE circuit
v1 1 0 dc 12
r1 1 0 2200
.op
.end
```

SPICE version 2G6 analysis (edited for brevity):

```
node   voltage
 (1)   12.0000

   voltage source currents

   name       current
   v1       -5.455E-03

   total power dissipation   6.55E-02  watts
```

Just to show you what the raw output of SPICE version 2G6 looks like for this analysis, here it is in all its unedited glory (note that I had to shorten some of the lines that exceeded the page width):

```
1*******09/02/16 ********  spice 2g.6    3/15/83 ********12:04:38*****

0* spice circuit

0****     input listing                    temperature =   27.000 deg c

0******************************************************************************



 v1 1 0 dc 12
 r1 1 0 2200
 .op
 .end
1******09/02/16 *********  spice 2g.6 3/15/83 ********12:04:38**********

0* spice circuit
0****  small signal bias solution           temperature =   27.000 deg c

0******************************************************************************


  node   voltage


 (  1)   12.0000



     voltage source currents

     name       current


     v1       -5.455E-03


     total power dissipation   6.55E-02  watts
0
         job concluded
0         total job time            0.00
```

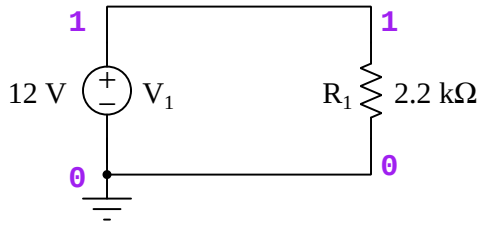
NGSPICE version 26 is more verbose than the legacy SPICE version 2G6 running the "Operating Point" (`.op`) analysis, requiring more than a page to display:

```
Circuit: * spice circuit

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000


No. of Data Rows : 1
Node                                  Voltage
----                                  -------
-----------
V(1)                              1.200000e+01

Source Current
-------------

v1#branch                         -5.45455e-03

 Resistor models (Simple linear resistor)
      model                       R

        rsh                       0
     narrow                       0
      short                       0
        tc1                       0
        tc2                       0
       defw                   1e-05
          l                   1e-05
         kf                       0
         af                       0
          r                       0
     bv_max                   1e+99

 Resistor: Simple linear resistor
     device                      r1
      model                       R
 resistance                    2200
         ac                    2200
      dtemp                       0
     bv_max                   1e+99
      noisy                       1
          i              0.00545455
          p               0.0654545

 Vsource: Independent voltage source
```

```
     device                    v1
         dc                    12
      acmag                     0
      pulse         -
       sine         -
        sin         -
        exp         -
        pwl         -
       sffm         -
         am         -
    trnoise         -
   trrandom         -
          i           -0.00545455
          p             0.0654545

CPU time since last call: 0.032 seconds.

Total CPU time: 0.032 seconds.

Total DRAM available = 489.546875 MB.
DRAM currently available = 152.234375 MB.
Total ngspice program size = 2.191406 MB.
Resident set size = 593.000 kB.
Shared ngspice pages = 464.000 kB.
Text (code) pages = 1.087891 MB.
Stack = 0 bytes.
Library pages = 164.000 kB.
```

5.2 DC voltage source with single-point .dc sweep analysis

Circuit schematic diagram (with node numbers listed). Note how ground is defined in SPICE as node number *zero*. In this example we will maintain the voltage source at a constant value of 12 Volts DC. The "sweep" analysis is intended to cover a specified range of voltage values, but we are exploiting that analysis option here to perform an analysis at only a single voltage value:



SPICE netlist:

```
* SPICE circuit
v1 1 0 dc 12
r1 1 0 2200
.dc v1 12 12 1
.print dc v(1) i(v1)
.end
```

SPICE version 2G6 analysis (edited for brevity):

```
   v1            v(1)         i(v1)
 1.200E+01     1.200E+01  -5.455E-03
```

SPICE version 2G6 is slightly less verbose when performing the `.dc` analysis than when performing the `.op` analysis. Here is the "raw" output of SPICE version 2G6 for your perusal:

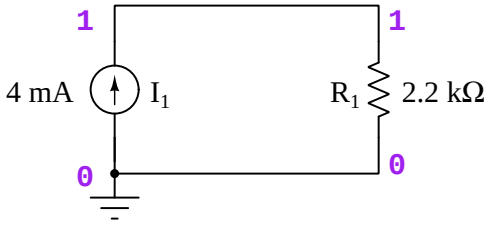
```
1*******09/02/16 ********  spice 2g.6    3/15/83 ********12:22:56*****

0* spice circuit

0****     input listing                    temperature =   27.000 deg c

0******************************************************************************



 v1 1 0 dc 12
 r1 1 0 2200
 .dc v1 12 12 1
 .print dc v(1) i(v1)
 .end
1******09/02/16 *********  spice 2g.6  3/15/83 *********12:22:56********

0* spice circuit
0****    dc transfer curves      temperature =   27.000 deg c

0******************************************************************************



   v1            v(1)        i(v1)
x

  1.200E+01     1.200E+01  -5.455E-03
y
0
         job concluded
0         total job time            0.00
```

NGSPICE version 26 is substantially less verbose when performing the `.dc` analysis. Here is the "raw" output of NGSPICE version 26 for your perusal:

```
Circuit: * spice circuit

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000


No. of Data Rows : 1
                          * spice circuit
                          DC transfer characteristic  Fri Sep  2 12:28:41  2016
--------------------------------------------------------------------------------
Index   v-sweep         v(1)            v1#branch
--------------------------------------------------------------------------------
0       1.200000e+01    1.200000e+01    -5.45455e-03

CPU time since last call: 0.032 seconds.

Total CPU time: 0.032 seconds.

Total DRAM available = 489.546875 MB.
DRAM currently available = 152.128906 MB.
Total ngspice program size = 2.191406 MB.
Resident set size = 595.000 kB.
Shared ngspice pages = 466.000 kB.
Text (code) pages = 1.087891 MB.
Stack = 0 bytes.
Library pages = 164.000 kB.
```

5.3 DC current source with single-point .dc sweep analysis

Circuit schematic diagram (with node numbers listed). Note how ground is defined in SPICE as node number *zero*. In this example we will maintain the current source at a constant value of 4 milliAmperes DC. The "sweep" analysis is intended to cover a specified range of current values, but we are exploiting that analysis option here to perform an analysis at only a single current value:



SPICE netlist:

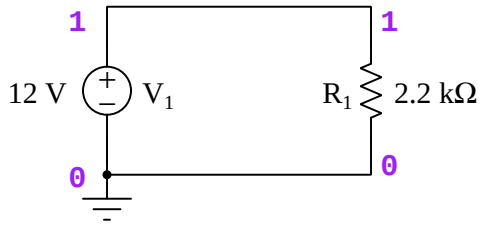
```
* SPICE circuit
i1 0 1 dc 4e-3
r1 1 0 2200
.dc i1 4e-3 4e-3 1
.print dc v(1)
.end
```

SPICE version 2G6 analysis (edited for brevity):

```
   i1            v(1)
 4.000E-03     8.800E+00
```

5.4 DC voltage source with multi-point .dc sweep analysis

Circuit schematic diagram (with node numbers listed). Note how ground is defined in SPICE as node number *zero*. In this example we will "sweep" the voltage source from 2 to 12 Volts DC in increments of 1 Volt:



First, showing the "printed" output option:

SPICE netlist:

```
* SPICE circuit
v1 1 0 dc 12
r1 1 0 2200
.dc v1 2 12 1
.print dc v(1) i(v1)
.end
```

SPICE version 2G6 analysis (edited for brevity):

```
 v1           v(1)         i(v1)
2.000E+00     2.000E+00  -9.091E-04
3.000E+00     3.000E+00  -1.364E-03
4.000E+00     4.000E+00  -1.818E-03
5.000E+00     5.000E+00  -2.273E-03
6.000E+00     6.000E+00  -2.727E-03
7.000E+00     7.000E+00  -3.182E-03
8.000E+00     8.000E+00  -3.636E-03
9.000E+00     9.000E+00  -4.091E-03
1.000E+01     1.000E+01  -4.545E-03
1.100E+01     1.100E+01  -5.000E-03
1.200E+01     1.200E+01  -5.455E-03
```

Next, showing the "plotted" output option[1]:

SPICE netlist:

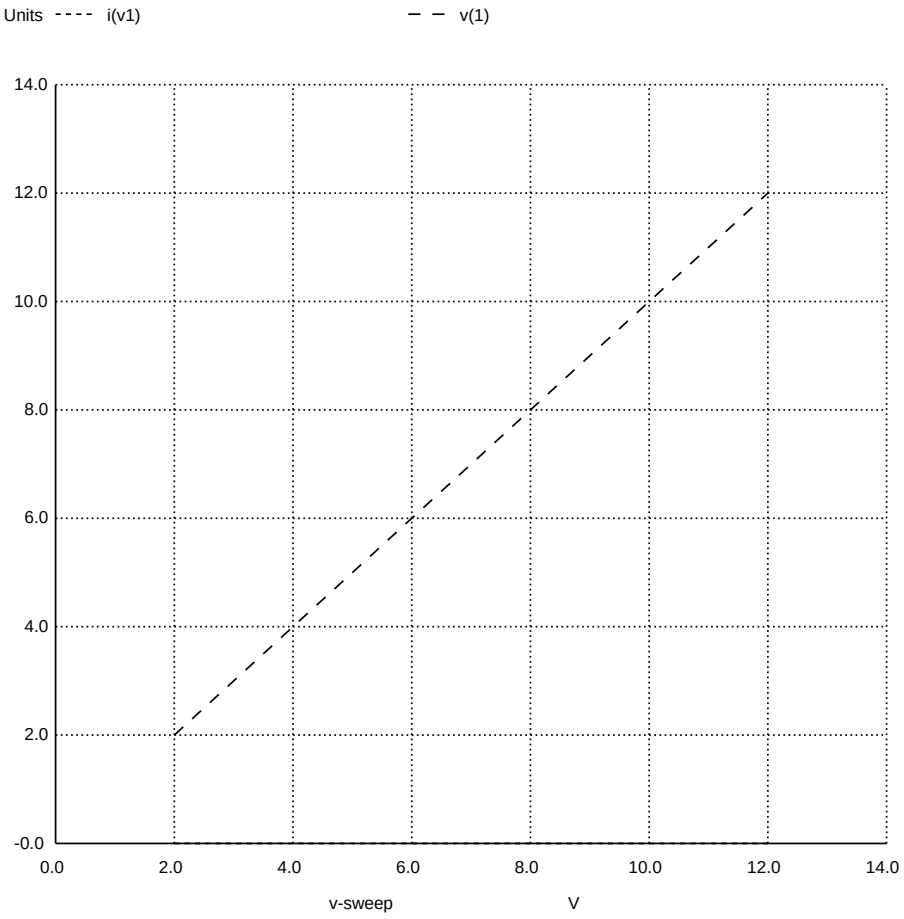
```
* SPICE circuit
v1 1 0 dc 12
r1 1 0 2200
.dc v1 2 12 1
.plot dc v(1) i(v1)
.width out=80
.end
```

SPICE version 2G6 analysis (edited for brevity):

```
legend:
 *: v(1)
 +: i(v1)

   v1          v(1)

(*)------------  0.000E+00     5.000E+00     1.000E+01     1.500E+01  2.000E+01
                 - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(+)------------ -6.000E-03    -4.000E-03    -2.000E-03     0.000E+00  2.000E-03
                 - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
 2.000E+00  2.000E+00 .     *       .             .       +     .            .
 3.000E+00  3.000E+00 .       *     .             .   +         .            .
 4.000E+00  4.000E+00 .          *  .             .+            .            .
 5.000E+00  5.000E+00 .             *           + .             .            .
 6.000E+00  6.000E+00 .             .  *     +    .             .            .
 7.000E+00  7.000E+00 .             .     x       .             .            .
 8.000E+00  8.000E+00 .             .  +    *     .             .            .
 9.000E+00  9.000E+00 .            +.          *  .             .            .
 1.000E+01  1.000E+01 .         +   .             *             .            .
 1.100E+01  1.100E+01 .      +      .             .  *          .            .
 1.200E+01  1.200E+01 .   +         .             .     *       .            .
                 - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
```

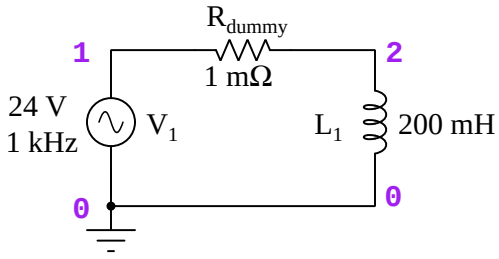
[1]SPICE assumes a 120-character width display, and so to fit the text output on a standard terminal the `.width` option must be invoked to set the display width at 80 characters

NGSPICE version 26 analysis (using window-based interactive mode on Linux/X-Windows):



5.5 AC voltage source with single-point .ac sweep analysis

Circuit schematic diagram (with node numbers listed). Note how the series connection between the "dummy" resistor and the inductor is specified by three nodes: 1, 2, and 0. The resistor connects between nodes 1 and 2, while the inductor connects between nodes 2 and 0. The one node common to both components (node 2) makes those two components share a common connection. Note as always how ground is defined in SPICE as node number *zero*. In this example we will "sweep" the source frequency from 1 kHz to 1 kHz with just one interval. The "dummy" resistance of 1 milli-Ohm is necessary in order to avoid a direct "loop" between the voltage source and the inductor, which SPICE cannot abide:



SPICE netlist:

```
* SPICE circuit
v1 1 0 ac 24
rdummy 1 2 1m
l1 2 0 200m
.ac lin 1 1k 1k
.print ac vm(1) vp(1) im(v1) ip(v1)
.end
```

SPICE version 2G6 analysis (edited for brevity):

```
    freq        vm(1)        vp(1)        im(v1)       ip(v1)
1.000E+03    2.400E+01    0.000E+00    1.910E-02    9.000E+01
```

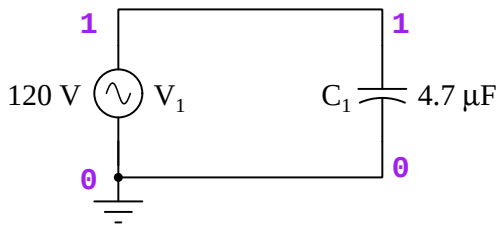
Early versions of SPICE such as 2G6 assumed phase angle unit of degrees, but many later versions assume *radians* when displaying phase angles. In order to specifically instruct modern versions of SPICE to display angles in degrees, the following "control" cards must be added to the netlist:

```
.control
set units=degrees
.endc
```

These cards may be added to the netlist "deck" anywhere between the first line (`* SPICE circuit`) and the last (`.end`).

5.6 AC voltage source with multi-point .ac sweep analysis

Circuit schematic diagram (with node numbers listed). Note how ground is defined in SPICE as node number *zero*. In this example we will "sweep" the source frequency from 60 Hz to 6 kHz on a decade logarithmic scale with 5 points per decade:



First, showing the "printed" output option:

SPICE netlist:

```
* SPICE circuit
v1 1 0 ac 120
c1 1 0 4.7u
.ac dec 5 60 6k
.print ac vm(1) vp(1) im(v1) ip(v1)
.end
```

SPICE version 2G6 analysis (edited for brevity):

```
    freq        vm(1)        vp(1)        im(v1)       ip(v1)
  6.000E+01     1.200E+02    0.000E+00    2.126E-01   -9.000E+01
  9.509E+01     1.200E+02    0.000E+00    3.370E-01   -9.000E+01
  1.507E+02     1.200E+02    0.000E+00    5.341E-01   -9.000E+01
  2.389E+02     1.200E+02    0.000E+00    8.465E-01   -9.000E+01
  3.786E+02     1.200E+02    0.000E+00    1.342E+00   -9.000E+01
  6.000E+02     1.200E+02    0.000E+00    2.126E+00   -9.000E+01
  9.509E+02     1.200E+02    0.000E+00    3.370E+00   -9.000E+01
  1.507E+03     1.200E+02    0.000E+00    5.341E+00   -9.000E+01
  2.389E+03     1.200E+02    0.000E+00    8.465E+00   -9.000E+01
  3.786E+03     1.200E+02    0.000E+00    1.342E+01   -9.000E+01
  6.000E+03     1.200E+02    0.000E+00    2.126E+01   -9.000E+01
```

Next, showing the "plotted" output option[2]:

SPICE netlist:

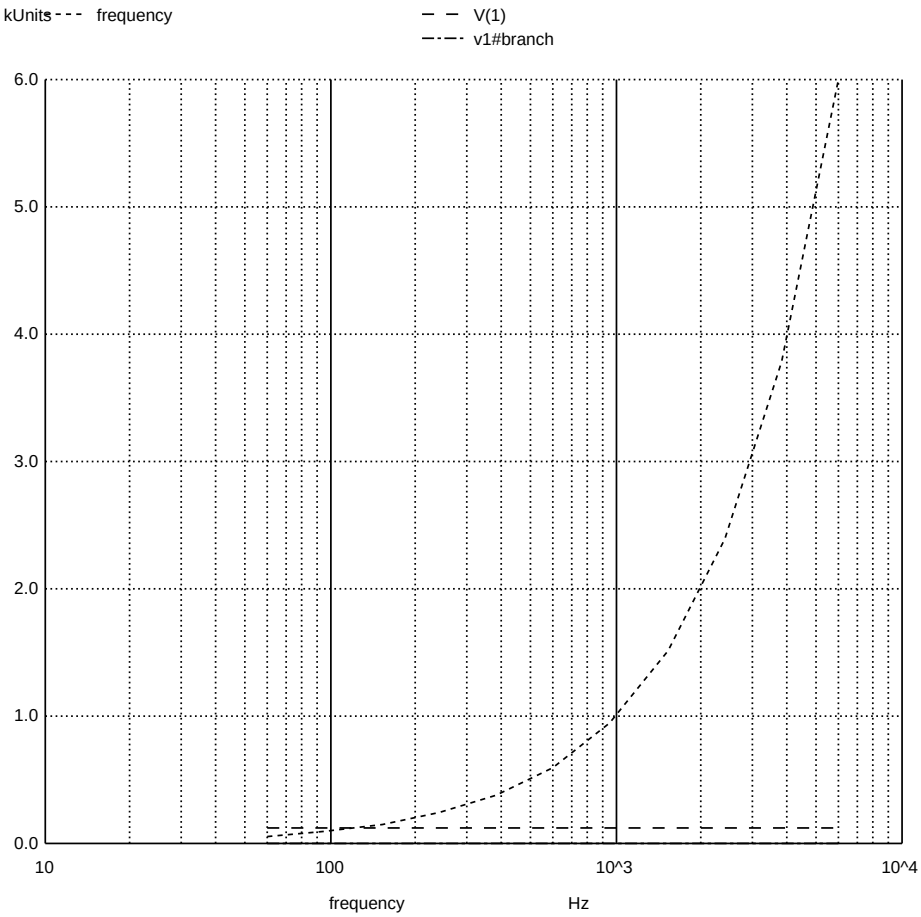
```
* SPICE circuit
v1 1 0 ac 120
c1 1 0 4.7u
.ac dec 5 60 6k
.plot ac vm(1) vp(1) im(v1) ip(v1)
.width out=80
.end
```

[2]SPICE assumes a 120-character width display, and so to fit the text output on a standard terminal the `.width` option must be invoked to set the display width at 80 characters

SPICE version 2G6 analysis (edited for brevity):

```
legend:
 *: vm(1)
 +: vp(1)
 =: im(v1)
 $: ip(v1)

     freq      vm(1)
(*)------------  1.000E+01     1.000E+02     1.000E+03     1.000E+04  1.000E+05
                 - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(+)------------ -1.000E-12    -5.000E-13     0.000E+00     5.000E-13  1.000E-12
                 - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(=)------------  1.000E-01     1.000E+00     1.000E+01     1.000E+02  1.000E+03
                 - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
($)------------ -1.500E+02    -1.000E+02    -5.000E+01     0.000E+00  5.000E+01
                 - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
 6.000E+01  1.200E+02 .    =        .* $          +             .             .
 9.509E+01  1.200E+02 .      =      .* $          +             .             .
 1.507E+02  1.200E+02 .         =   .* $          +             .             .
 2.389E+02  1.200E+02 .            =.* $          +             .             .
 3.786E+02  1.200E+02 .             .*=$          +             .             .
 6.000E+02  1.200E+02 .             .* $ =        +             .             .
 9.509E+02  1.200E+02 .             .* $   =      +             .             .
 1.507E+03  1.200E+02 .             .* $      =   +             .             .
 2.389E+03  1.200E+02 .             .* $         =+             .             .
 3.786E+03  1.200E+02 .             .* $          + =           .             .
 6.000E+03  1.200E+02 .             .* $          +    =        .             .
                 - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
```

NGSPICE version 26 analysis (using window-based interactive mode on Linux/X-Windows):



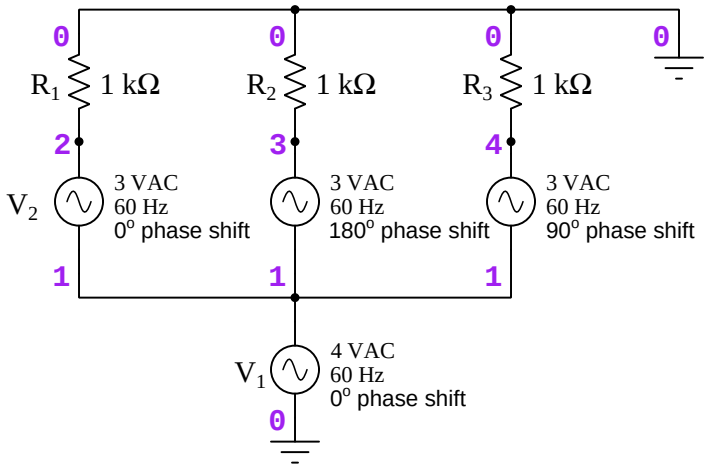
It should be noted that early versions of SPICE such as 2G6 assumed phase angle unit of degrees, but many later versions assume *radians* when displaying phase angles. In order to specifically instruct modern versions of SPICE to display angles in degrees, the following "control" cards must be added to the netlist:

```
.control
set units=degrees
.endc
```

These cards may be added to the netlist "deck" anywhere between the first line (`* SPICE circuit`) and the last (`.end`).

5.7 Additive AC voltage sources with single-point .ac sweep analysis

Circuit schematic diagram (with node numbers listed). Note the use of node numbers to specify the circuit's shape. Node 0 is the ground point, while nodes shared between different components specify direct connections between those components (i.e. all identically-numbered nodes are electrically common to each other). Nodes with different numbers are electrically distinct from each other:



SPICE netlist:

```
* SPICE circuit
v1 1 0 ac 4 0
v2 2 1 ac 3 0
v3 3 1 ac 3 180
v4 4 1 ac 3 90
r1 2 0 1k
r2 3 0 1k
r3 4 0 1k
.ac lin 1 60 60
.print ac vm(2) vm(3) vm(4)
.print ac vp(2) vp(3) vp(4)
.end
```

SPICE version 2G6 analysis (edited for brevity):

```
    freq        vm(2)       vm(3)       vm(4)
6.000E+01     7.000E+00   1.000E+00   5.000E+00

    freq        vp(2)       vp(3)       vp(4)
6.000E+01     0.000E+00   2.105E-14   3.687E+01
```

The voltage at node 2 (with respect to ground, 0) is the simple sum of 4 Volts and 3 Volts because V_1 and V_2 are perfectly in sync with each other, analogous to a pair of DC voltage sources connected in series with polarities additive. This also explains the zero phase shift of node 2's voltage: the sum of those two sources is in-phase with our reference source V_1 (at 0 degrees phase angle).

The voltage at node 3 is only 1 Volt (the difference between 4 Volts and 3 Volts) because V_1 and V_3 are perfectly *opposed* to one another, analogous to a pair of DC voltage sources connected in series with polarities subtractive. The phase shift of this voltage is practically zero, the only reason for the miniscule non-zero phase result being imperfections in SPICE's AC analysis.

The voltage at node 4 has no DC analogue because here the two sources V_1 and V_4 are neither directly in sync with each other nor perfectly opposed to each other – instead, these two sources are 90 degrees out of phase with each other. Their phasor sum is 5 Volts for the same reason that a right triangle with opposite and adjacent side lengths of 4 and 3 will have a hypotenuse length of 5. Note that the phase angle of this voltage is neither 0 degrees nor 90 degrees, but instead is 36.87 degrees: the same angle one would expect between the 4-length and 5-length sides of a right triangle (i.e. $\cos^{-1}\left(\frac{4}{5}\right) = 36.87^o$).

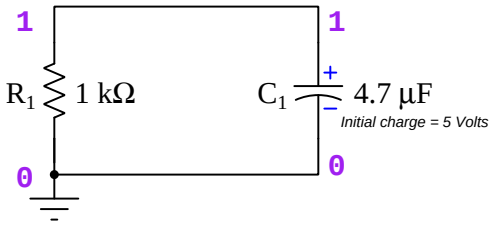
It should be noted that early versions of SPICE such as 2G6 assumed phase angle unit of degrees, but many later versions assume *radians* when displaying phase angles. In order to specifically instruct modern versions of SPICE to display angles in degrees, the following "control" cards must be added to the netlist:

```
.control
set units=degrees
.endc
```

These cards may be added to the netlist "deck" anywhere between the first line (`* SPICE circuit`) and the last (`.end`).

5.8 Transient analysis of discharging RC circuit

Circuit schematic diagram (with node numbers listed). Note how ground is defined in SPICE as node number *zero*. In this example we will pre-charge the capacitor to 5 Volts and analyze its discharge over time. The time-span for analysis is from $t = 0$ to $t = 250$ milliseconds, in 10 millisecond intervals:



First, showing the "printed" output option:

SPICE netlist:

```
* SPICE circuit
r1 1 0 1k
c1 1 0 47u ic=5
.tran 10m 250m uic
.print tran v(1)
.end
```

SPICE version 2G6 analysis (edited for brevity):

```
   time       v(1)
0.000E+00     5.000E+00
1.000E-02     4.046E+00
2.000E-02     3.270E+00
3.000E-02     2.643E+00
4.000E-02     2.136E+00
5.000E-02     1.726E+00
6.000E-02     1.395E+00
7.000E-02     1.127E+00
8.000E-02     9.112E-01
9.000E-02     7.364E-01
1.000E-01     5.951E-01
1.100E-01     4.810E-01
1.200E-01     3.887E-01
1.300E-01     3.142E-01
1.400E-01     2.539E-01
1.500E-01     2.052E-01
1.600E-01     1.658E-01
1.700E-01     1.340E-01
1.800E-01     1.083E-01
1.900E-01     8.754E-02
2.000E-01     7.075E-02
2.100E-01     5.718E-02
2.200E-01     4.621E-02
2.300E-01     3.735E-02
2.400E-01     3.018E-02
2.500E-01     2.437E-02
```

Next, showing the "plotted" output option[3]:

SPICE netlist:

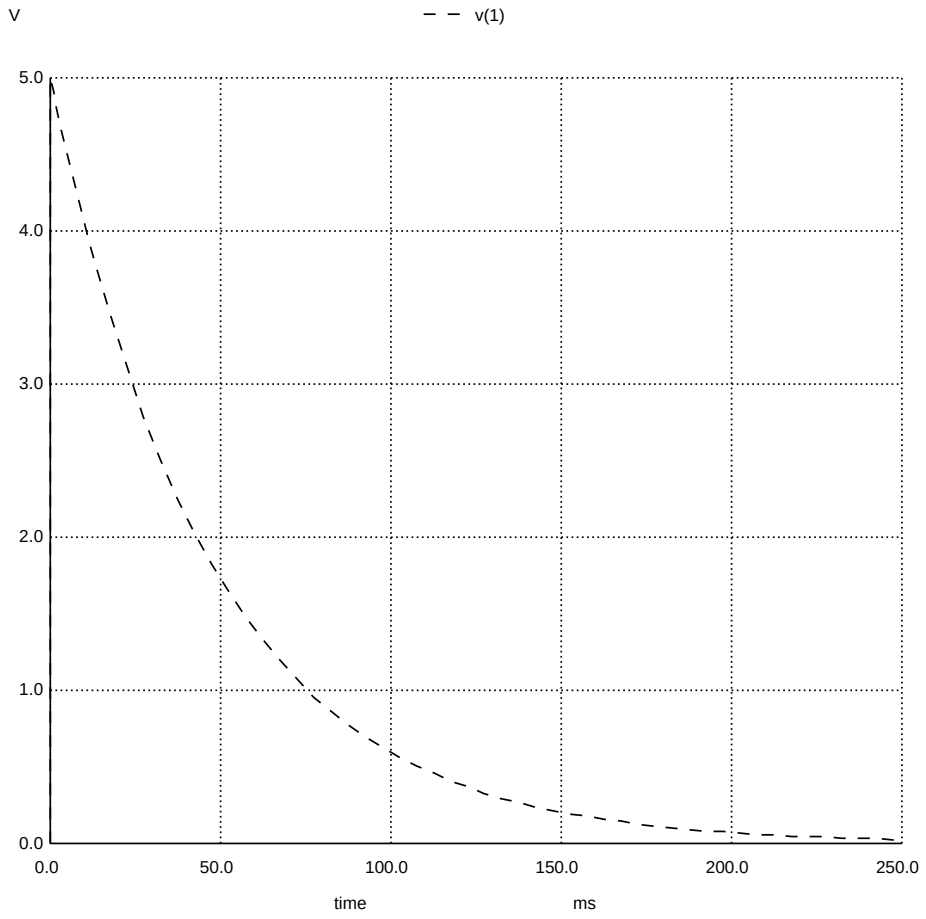
```
* SPICE circuit
r1 1 0 1k
c1 1 0 47u ic=5
.tran 10m 250m uic
.plot tran v(1)
.width out=80
.end
```

[3]SPICE assumes a 120-character width display, and so to fit the text output on a standard terminal the `.width` option must be invoked to set the display width at 80 characters

SPICE version 2G6 analysis (edited for brevity):

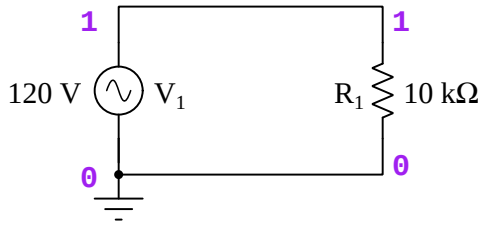
```
    time      v(1)
                0.000E+00     2.000E+00     4.000E+00     6.000E+00  8.000E+00
                - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
0.000E+00  5.000E+00 .             .             .      *      .             .
1.000E-02  4.046E+00 .             .             *             .             .
2.000E-02  3.270E+00 .             .        *    .             .             .
3.000E-02  2.643E+00 .             .   *         .             .             .
4.000E-02  2.136E+00 .             .*            .             .             .
5.000E-02  1.726E+00 .           * .             .             .             .
6.000E-02  1.395E+00 .         *   .             .             .             .
7.000E-02  1.127E+00 .       *     .             .             .             .
8.000E-02  9.112E-01 .     *       .             .             .             .
9.000E-02  7.364E-01 .    *        .             .             .             .
1.000E-01  5.951E-01 .   *         .             .             .             .
1.100E-01  4.810E-01 .  *          .             .             .             .
1.200E-01  3.887E-01 .  *          .             .             .             .
1.300E-01  3.142E-01 . *           .             .             .             .
1.400E-01  2.539E-01 . *           .             .             .             .
1.500E-01  2.052E-01 .*            .             .             .             .
1.600E-01  1.658E-01 .*            .             .             .             .
1.700E-01  1.340E-01 .*            .             .             .             .
1.800E-01  1.083E-01 .*            .             .             .             .
1.900E-01  8.754E-02 .*            .             .             .             .
2.000E-01  7.075E-02 *             .             .             .             .
2.100E-01  5.718E-02 *             .             .             .             .
2.200E-01  4.621E-02 *             .             .             .             .
2.300E-01  3.735E-02 *             .             .             .             .
2.400E-01  3.018E-02 *             .             .             .             .
2.500E-01  2.437E-02 *             .             .             .             .
                - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
```

NGSPICE version 26 analysis (using window-based interactive mode on Linux/X-Windows):



5.9 Transient analysis of a steady sinusoidal voltage source

Circuit schematic diagram (with node numbers listed). Note how ground is defined in SPICE as node number *zero*. In this example we will define a voltage source with a sinusoidal waveform, no DC offset, 120 Volt peak amplitude, 60 Hz frequency, no start delay, and no decay (i.e. an undamped waveform). The time-span for analysis is from $t = 0$ to $t = 34$ milliseconds, in 1 millisecond intervals:



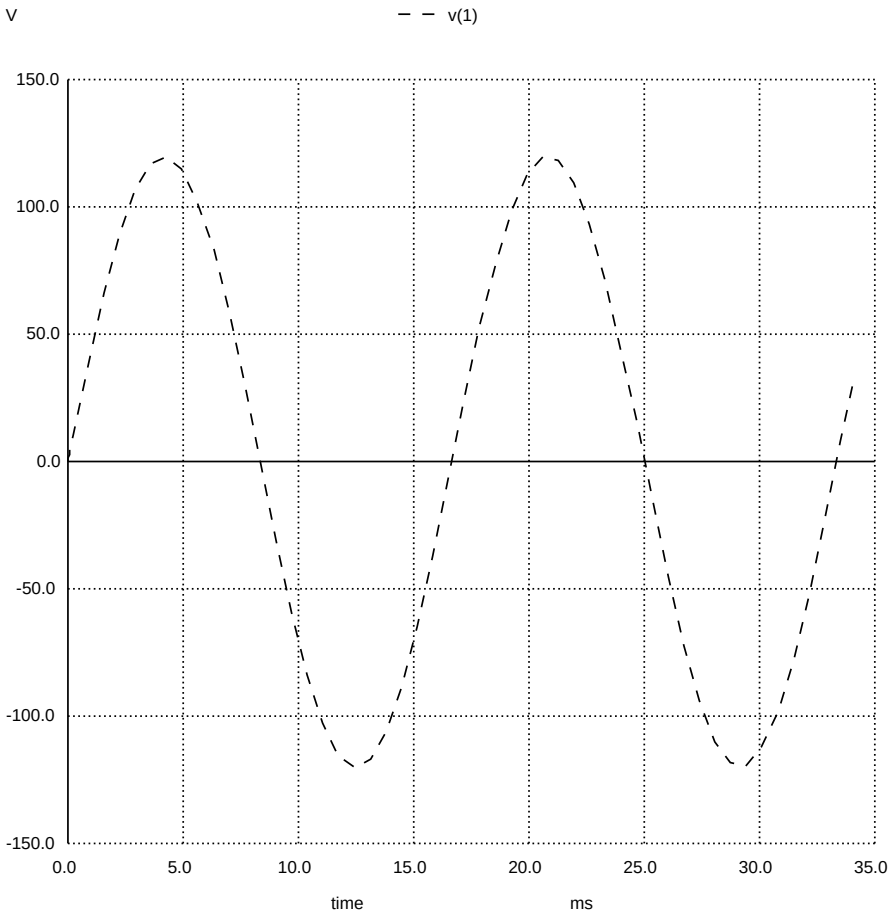
SPICE netlist:

```
* SPICE circuit
v1 1 0 sin (0 120 60 0 0)
r1 1 0 10e3
.tran 1m 34m
.plot tran v(1)
.width out=80
.end
```

SPICE version 2G6 analysis (edited for brevity):

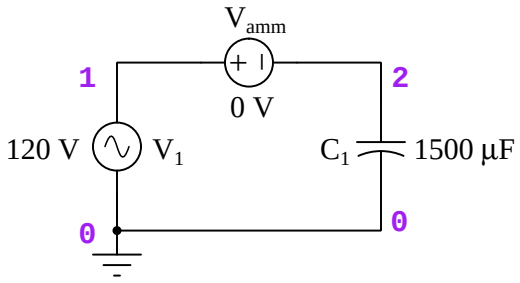
```
    time      v(1)
               -2.000E+02    -1.000E+02     0.000E+00     1.000E+02  2.000E+02
                    - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
0.000E+00  0.000E+00 .              .              *              .             .
1.000E-03  4.387E+01 .              .              .     *        .             .
2.000E-03  8.104E+01 .              .              .          *   .             .
3.000E-03  1.071E+02 .              .              .             .*             .
4.000E-03  1.181E+02 .              .              .             .  *           .
5.000E-03  1.125E+02 .              .              .             . *            .
6.000E-03  9.108E+01 .              .              .            *.              .
7.000E-03  5.690E+01 .              .              .       *     .              .
8.000E-03  1.473E+01 .              .              . *           .              .
9.000E-03 -2.951E+01 .              .         *    .             .              .
1.000E-02 -6.961E+01 .              .   *          .             .              .
1.100E-02 -9.993E+01 .              *              .             .              .
1.200E-02 -1.162E+02 .            * .              .             .              .
1.300E-02 -1.162E+02 .            * .              .             .              .
1.400E-02 -9.982E+01 .              *              .             .              .
1.500E-02 -6.945E+01 .              .   *          .             .              .
1.600E-02 -2.933E+01 .              .         *    .             .              .
1.700E-02  1.492E+01 .              .              . *           .              .
1.800E-02  5.707E+01 .              .              .       *     .              .
1.900E-02  9.120E+01 .              .              .            *.              .
2.000E-02  1.125E+02 .              .              .             . *            .
2.100E-02  1.180E+02 .              .              .             .  *           .
2.200E-02  1.070E+02 .              .              .             .*             .
2.300E-02  8.091E+01 .              .              .          *  .              .
2.400E-02  4.346E+01 .              .              .     *        .              .
2.500E-02 -9.465E-02 .              .              *             .              .
2.600E-02 -4.363E+01 .              .        *     .             .              .
2.700E-02 -8.104E+01 .              .  *           .             .              .
2.800E-02 -1.071E+02 .            *.               .             .              .
2.900E-02 -1.181E+02 .          *  .               .             .              .
3.000E-02 -1.125E+02 .           * .               .             .              .
3.100E-02 -9.108E+01 .             .*              .             .              .
3.200E-02 -5.690E+01 .              .     *        .             .              .
3.300E-02 -1.473E+01 .              .           * .             .              .
3.400E-02  2.951E+01 .              .             .   *         .              .
                    - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
```

NGSPICE version 26 analysis (using window-based interactive mode on Linux/X-Windows):



5.10 Transient analysis of a sinusoidal capacitive circuit

Circuit schematic diagram (with node numbers listed). Note how ground is defined in SPICE as node number *zero*. In this example we will define a voltage source with a sinusoidal waveform, no DC offset, 120 Volt peak amplitude, 60 Hz frequency, no start delay, and no decay (i.e. an undamped waveform). The time-span for analysis is from $t = 0$ to $t = 30$ milliseconds, in 1 millisecond intervals:



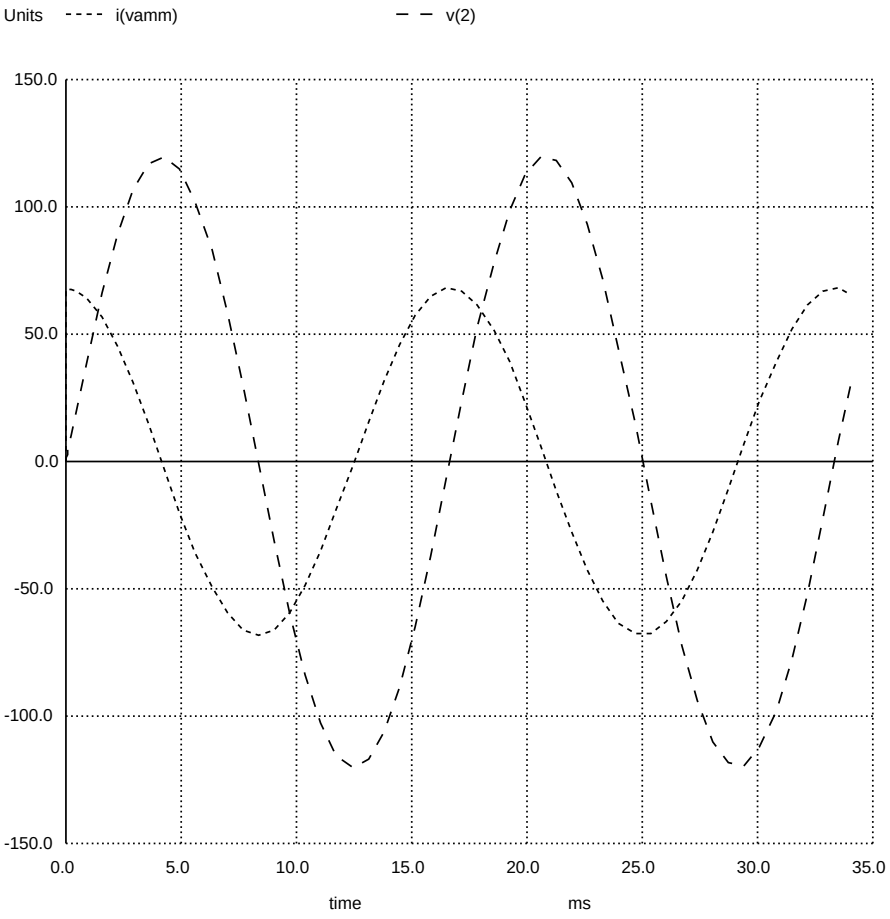
SPICE netlist:

```
* SPICE circuit
v1 1 0 sin (0 120 60 0 0)
c1 2 0 1500u
vamm 1 2 0
.tran 1m 30m
.plot tran v(1) i(vamm)
.width out=80
.end
```

SPICE version 2G6 analysis (edited for brevity):

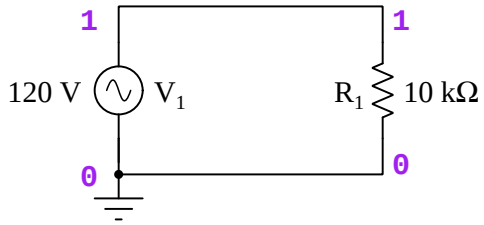
```
legend:
 *: v(1)
 +: i(vamm)

     time      v(1)

(*)------------ -2.000E+02    -1.000E+02     0.000E+00     1.000E+02  2.000E+02
                - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(+)------------ -1.000E+02    -5.000E+01     0.000E+00     5.000E+01  1.000E+02
                - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
 0.000E+00  0.000E+00 .             .             x             .            .
 1.000E-03  4.390E+01 .             .             .     *       .   +        .
 2.000E-03  8.203E+01 .             .             .          *  +            .
 3.000E-03  1.080E+02 .             .             .       +     .*           .
 4.000E-03  1.190E+02 .             .             .+            .  *         .
 5.000E-03  1.140E+02 .             .       +     .             . *          .
 6.000E-03  9.197E+01 .             . +           .            *.            .
 7.000E-03  5.747E+01 .          +  .             .       *     .            .
 8.000E-03  1.503E+01 .        +    .             . *           .            .
 9.000E-03 -2.971E+01 .         +   .         *   .             .            .
 1.000E-02 -7.010E+01 .            +.   *         .             .            .
 1.100E-02 -1.012E+02 .            *   +         .             .            .
 1.200E-02 -1.173E+02 .          * .         +   .             .            .
 1.300E-02 -1.172E+02 .          * .             .   +         .            .
 1.400E-02 -1.012E+02 .            *             .         +   .            .
 1.500E-02 -7.015E+01 .            .   *         .             .+           .
 1.600E-02 -2.967E+01 .            .         *   .             .   +        .
 1.700E-02  1.501E+01 .            .             . *           .    +       .
 1.800E-02  5.753E+01 .            .             .       *     .  +         .
 1.900E-02  9.189E+01 .            .             .          +*.            .
 2.000E-02  1.140E+02 .            .             .     +       . *          .
 2.100E-02  1.191E+02 .            .           +.              .  *         .
 2.200E-02  1.079E+02 .            .     +       .             .*           .
 2.300E-02  8.205E+01 .            +             .         *   .            .
 2.400E-02  4.393E+01 .         +  .             .     *       .            .
 2.500E-02  1.243E-02 .        +   .             *             .            .
 2.600E-02 -4.411E+01 .         +  .       *     .             .            .
 2.700E-02 -8.174E+01 .            +  *          .             .            .
 2.800E-02 -1.079E+02 .           *.     +       .             .            .
 2.900E-02 -1.196E+02 .          *  .           +.             .            .
 3.000E-02 -1.141E+02 .          * .             .     +       .            .
                - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
```

NGSPICE version 26 analysis (using window-based interactive mode on Linux/X-Windows):



5.11 Transient analysis of a damped, offset sinusoidal voltage source

Circuit schematic diagram (with node numbers listed). Note how ground is defined in SPICE as node number *zero*. In this example we will define a voltage source with a sinusoidal waveform, an 80 Volt DC offset, 120 Volt peak amplitude, 60 Hz frequency, no start delay, and a damping factor of 40 s^{-1}. The time-span for analysis is from $t = 0$ to $t = 34$ milliseconds, in 1 millisecond intervals:



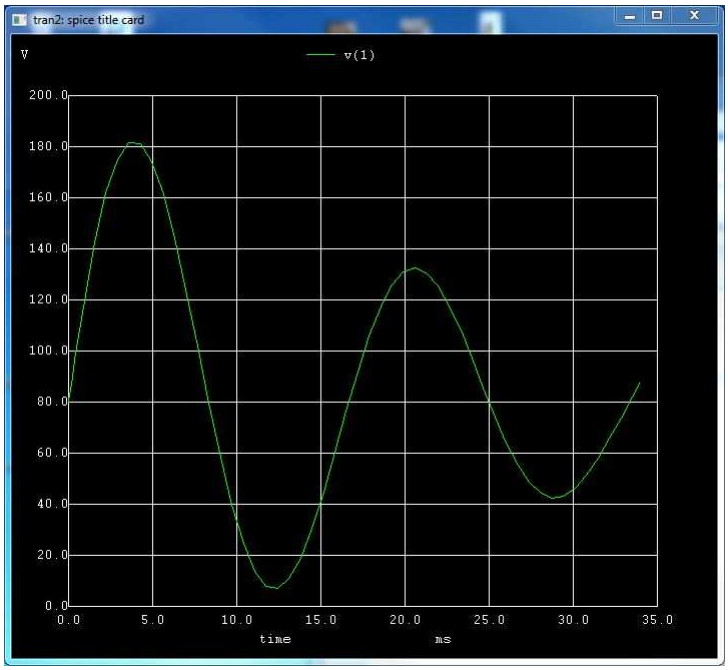
SPICE netlist:

```
* SPICE circuit
v1 1 0 sin (80 120 60 0 40)
r1 1 0 10e3
.tran 1m 34m
.plot tran v(1)
.width out=80
.end
```

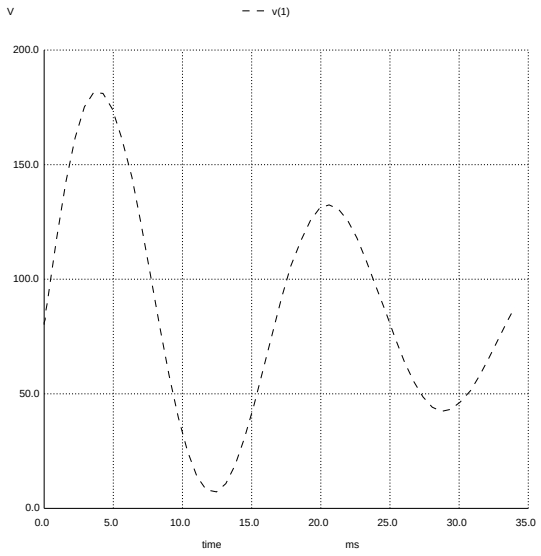
SPICE version 2G6 analysis (edited for brevity):

```
    time      v(1)
                0.000E+00     5.000E+01     1.000E+02     1.500E+02  2.000E+02
                - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
0.000E+00  8.000E+01 .             .       *     .             .            .
1.000E-03  1.221E+02 .             .             .     *       .            .
2.000E-03  1.552E+02 .             .             .             .*           .
3.000E-03  1.759E+02 .             .             .             .      *     .
4.000E-03  1.812E+02 .             .             .             .        *   .
5.000E-03  1.733E+02 .             .             .             .      *     .
6.000E-03  1.522E+02 .             .             .             .*           .
7.000E-03  1.237E+02 .             .             .      *      .            .
8.000E-03  9.098E+01 .             .          *  .             .            .
9.000E-03  5.922E+01 .             .  *          .             .            .
1.000E-02  3.321E+01 .        *    .             .             .            .
1.100E-02  1.497E+01 .   *         .             .             .            .
1.200E-02  7.632E+00 . *           .             .             .            .
1.300E-02  1.023E+01 .  *          .             .             .            .
1.400E-02  2.246E+01 .     *       .             .             .            .
1.500E-02  4.146E+01 .           * .             .             .            .
1.600E-02  6.426E+01 .             .   *         .             .            .
1.700E-02  8.750E+01 .             .         *   .             .            .
1.800E-02  1.079E+02 .             .             . *           .            .
1.900E-02  1.229E+02 .             .             .     *       .            .
2.000E-02  1.311E+02 .             .             .        *    .            .
2.100E-02  1.313E+02 .             .             .        *    .            .
2.200E-02  1.250E+02 .             .             .      *      .            .
2.300E-02  1.125E+02 .             .             .   *         .            .
2.400E-02  9.691E+01 .             .            *.             .            .
2.500E-02  8.008E+01 .             .       *     .             .            .
2.600E-02  6.442E+01 .             .   *         .             .            .
2.700E-02  5.238E+01 .             .*            .             .            .
2.800E-02  4.469E+01 .           *.              .             .            .
2.900E-02  4.274E+01 .           * .             .             .            .
3.000E-02  4.577E+01 .            *.             .             .            .
3.100E-02  5.339E+01 .             .*            .             .            .
3.200E-02  6.399E+01 .             .   *         .             .            .
3.300E-02  7.596E+01 .             .      *      .             .            .
3.400E-02  8.766E+01 .             .          *  .             .            .
                - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
```

NGSPICE version 26 analysis (using window-based interactive mode on Microsoft Windows 7):

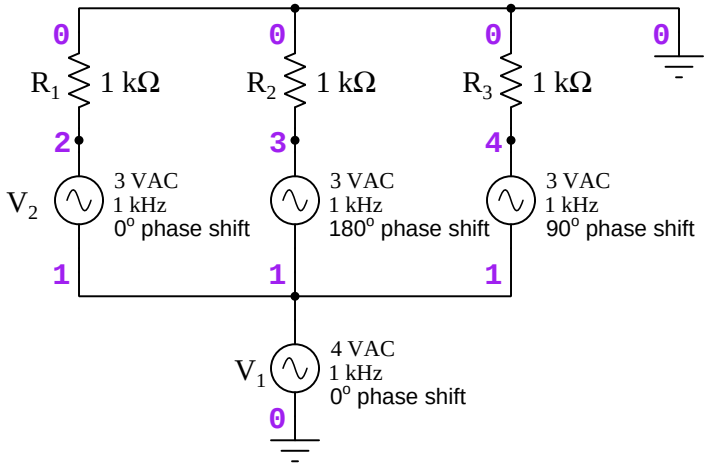


NGSPICE version 26 analysis (using window-based interactive mode on Linux/X-Windows):



5.12 Additive AC voltage sources with transient analysis

Circuit schematic diagram (with node numbers listed):



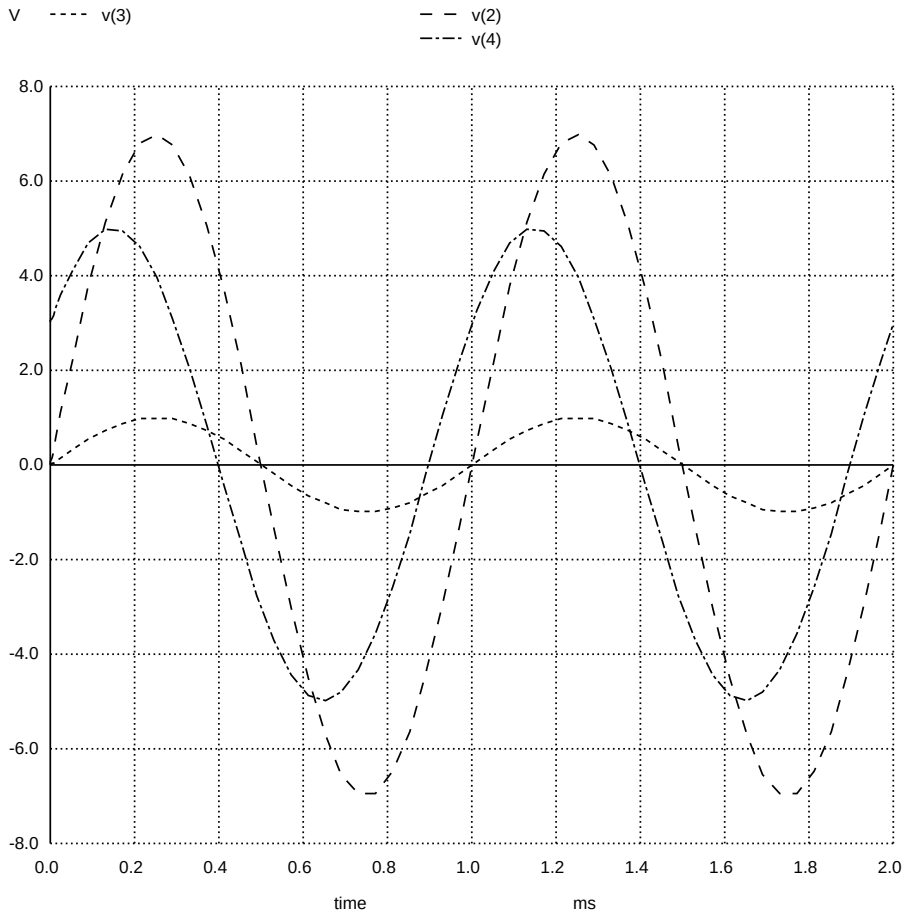
SPICE netlist:

```
* SPICE circuit
v1 1 0 sin (0 4 1k 0 0)
v2 2 1 sin (0 3 1k 0 0)
v3 3 1 sin (0 3 1k -0.5m 0)
v4 4 1 sin (0 3 1k -0.25m 0)
r1 2 0 1k
r2 3 0 1k
r3 4 0 1k
.tran 0.05m 4m
.plot tran v(1) v(2,1) v(3,1) v(4,1)
.plot tran v(2) v(3) v(4)
.end
```

Here, the phase shift of each sinusoidal voltage source must be specified in terms of *start delay time*. A 1000 Hertz waveform has a period of 1 millisecond, and therefore 180 degrees of phase shift is equivalent to a start delay of 0.5 milliseconds (i.e. one-half of the 360^o period) and 90 degrees of phase shift is equivalent to a start delay of 0.25 milliseconds (i.e. one-quarter of the 360^o period). The start delay times are shown here as negative quantities because we want the phase shifts to be *leading* (e.g. the V_3 sinusoidal source with a start delay of -0.5 milliseconds is already at its 180 degree mark by the time our reference source V_1 begins at 0 degrees.).

An important note here is that SPICE version 2G6 does not handle negative start delay time values, but NGSPICE version 26 does. For this reason, a SPICE version 2G6 analysis is omitted.

NGSPICE version 26 analysis (using window-based interactive mode on Linux/X-Windows):



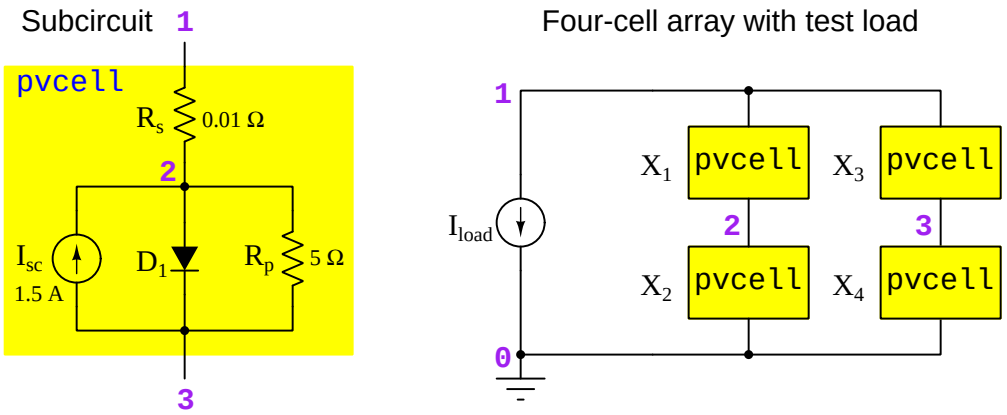
The voltage at node 2 (with respect to ground, 0) is the simple sum of 4 Volts and 3 Volts because V_1 and V_2 are perfectly in sync with each other, analogous to a pair of DC voltage sources connected in series with polarities additive. The voltage at node 3 is only 1 Volt (the difference between 4 Volts and 3 Volts) because V_1 and V_3 are perfectly *opposed* to one another, analogous to a pair of DC voltage sources connected in series with polarities subtractive.

The voltage at node 4 has no DC analogue because here the two sources V_1 and V_4 are neither directly in sync with each other nor perfectly opposed to each other – instead, these two sources are 90 degrees out of phase with each other. Their phasor sum is 5 Volts for the same reason that a right triangle with opposite and adjacent side lengths of 4 and 3 will have a hypotenuse length of 5.

Note how the voltage at node 4 does not peak at the same times as the voltages at nodes 2 or 3 because its phase shift is not 0 degrees as with the others.

5.13 Solar cell array simulation

This simulation uses both subcircuits and semiconductor models to represent a solar (photovoltaic) panel comprised of four individual cells. Each cell is modeled by the `pvcell` subcircuit, while the four-cell series-parallel array calls on that subcircuit four times. In order to plot the array's voltage-current characteristic curve, we use an external current source as a controlled load (I_{load}) and "sweep" the load current from zero to the full short-circuit rating of the array. In this case, with four cells connected in series-parallel fashion we would expect an open-circuit voltage approximately equal to two diode forward voltage drops and a short-circuit current approximately equal to two cells' parallel-total current:



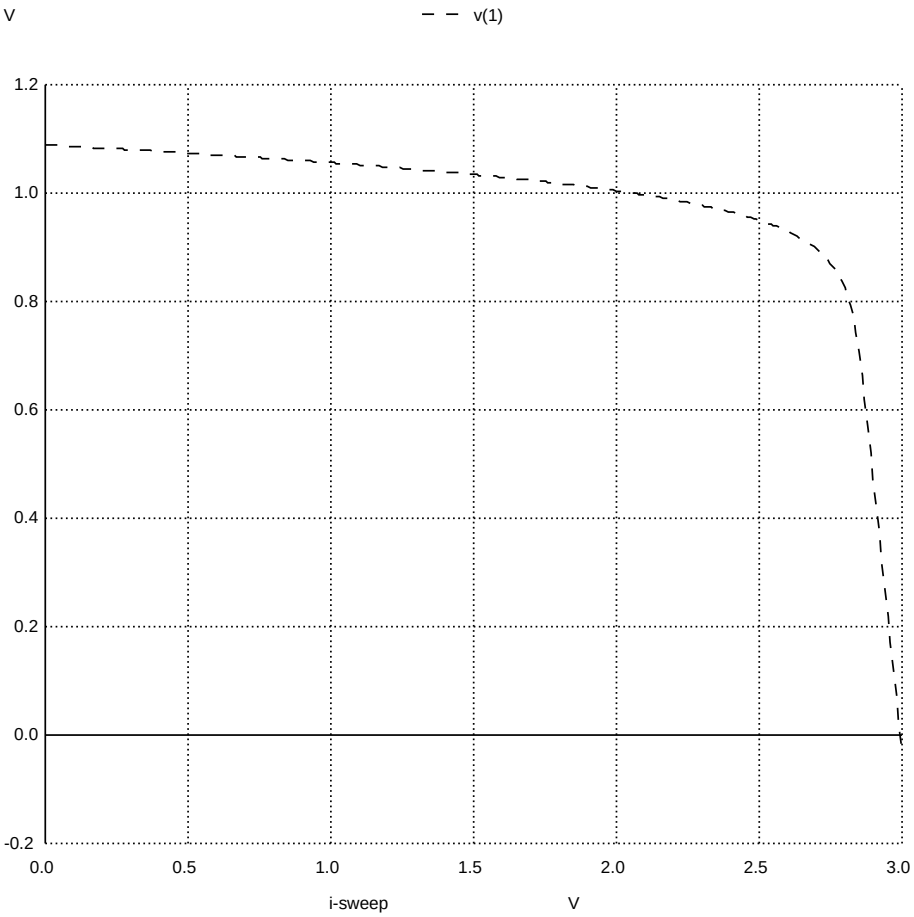
SPICE netlist:[4]

```
* SPICE circuit
x1 1 2 pvcell
x2 2 0 pvcell
x3 1 3 pvcell
x4 3 0 pvcell
iload 1 0
.subckt pvcell 1 3
rs 1 2 0.01
isc 3 2 1.5
d1 2 3 pnjunc
rp 2 3 5
.model pnjunc d is=1e-9 vj=0.65
.ends pvcell
.dc iload 0 3 0.01
.plot dc v(1)
```

[4] `.plot dc` statement intended to display the array's voltage as a function of load current.

```
.end
```

NGSPICE version 26 analysis (using window-based interactive mode on Linux/X-Windows):



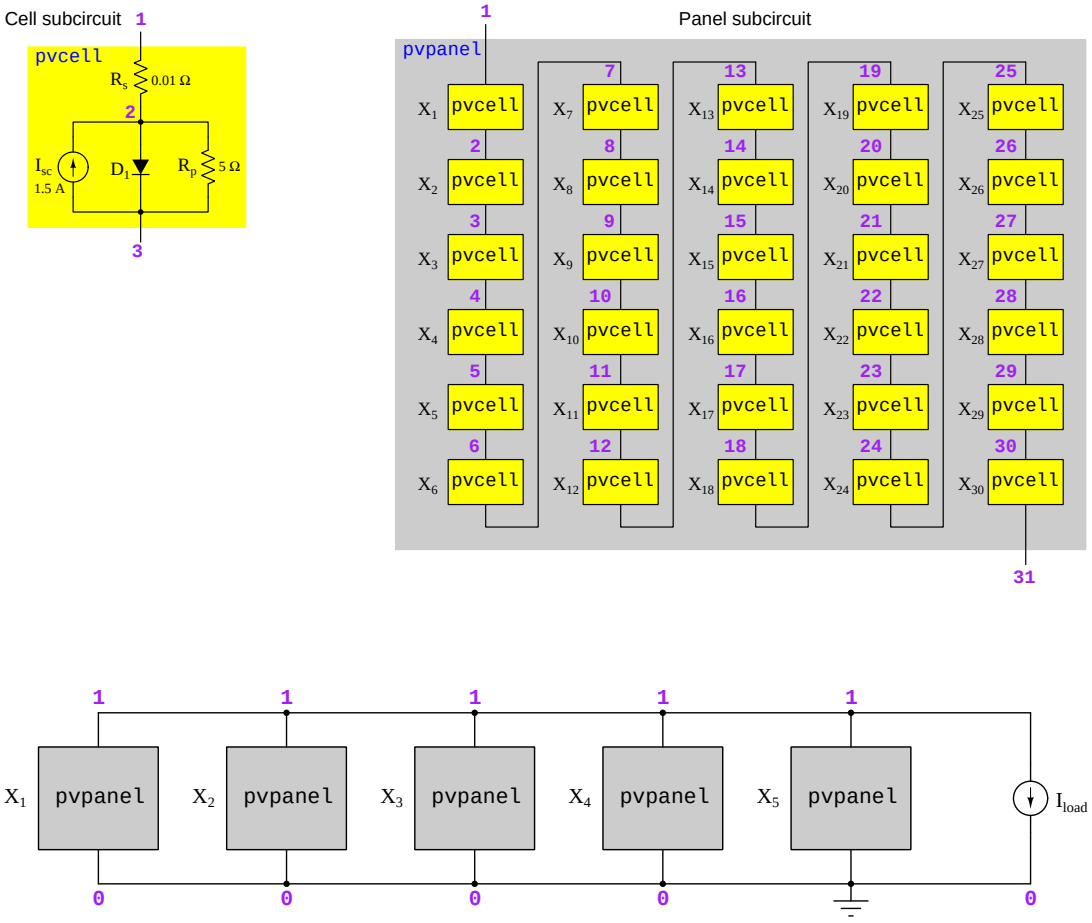
In this analysis we see the open-circuit condition represented at the far left of the graph (maximum voltage, zero current) and the short-circuit condition represented at the far right (zero voltage[5], maximum current).

The amount of open-circuit voltage for each cell is primarily a function of the cell subcircuit's diode model (`vj` parameter defining its nominal forward-voltage drop, and `is` parameter defining its saturation current). The amount of short-circuit current for each cell is primarily a function of the cell's current source (I_{sc}). The slope of the voltage-current curve toward the right-hand side is primarily a function of the cell's internal parallel resistance (R_p).

[5] We actually see the voltage dip slightly below zero at a load current of 3 Amperes, because at this point I_{load} is actually behaving as a *source* rather than a load. This demonstrates that the array's short-circuit capability is actually slightly less than 3 Amperes.

5.14 Solar panel array simulation

This simulation uses nested subcircuits, the lowest-level subcircuit representing a single solar (photovoltaic) cell and the next-level subcircuit representing a single panel comprised of 30 of those cells. The top-level simulation uses five of those panels in parallel to power a test load.



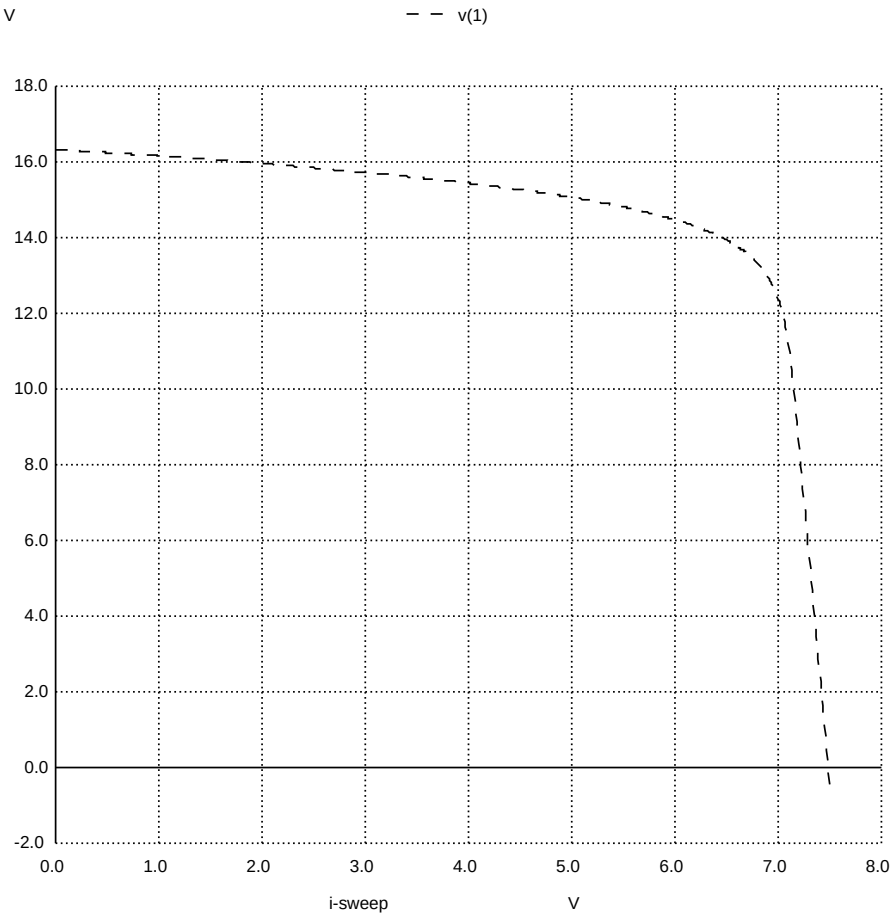
SPICE netlist:[6]

```
* SPICE circuit
x1 1 0 pvpanel
x2 1 0 pvpanel
x3 1 0 pvpanel
x4 1 0 pvpanel
x5 1 0 pvpanel
iload 1 0
*
* Panel subcircuit
.subckt pvpanel 1 31
x1 1 2 pvcell
x2 2 3 pvcell
x3 3 4 pvcell
x4 4 5 pvcell
x5 5 6 pvcell
x6 6 7 pvcell
x7 7 8 pvcell
x8 8 9 pvcell
x9 9 10 pvcell
x10 10 11 pvcell
x11 11 12 pvcell
x12 12 13 pvcell
x13 13 14 pvcell
x14 14 15 pvcell
x15 15 16 pvcell
x16 16 17 pvcell
x17 17 18 pvcell
x18 18 19 pvcell
x19 19 20 pvcell
x20 20 21 pvcell
x21 21 22 pvcell
x22 22 23 pvcell
x23 23 24 pvcell
x24 24 25 pvcell
x25 25 26 pvcell
x26 26 27 pvcell
x27 27 28 pvcell
x28 28 29 pvcell
x29 29 30 pvcell
```

[6] `.plot dc` statement intended to display the array's voltage as a function of load current. Also note the addition comments (`*`) inserted to visually separate and clearly label the subcircuits, so as to distinguish them from the rest of the netlist code.

```
x30 30 31 pvcell
.ends pvpanel
*
* Cell subcircuit
.subckt pvcell 1 3
rs 1 2 0.01
Isc 3 2 1.5
d1 2 3 pnjunc
rp 2 3 5
.model pnjunc d is=1e-9 vj=0.65
.ends pvcell
*
.dc iload 0 7.5 0.01
.plot dc v(1)
.end
```

NGSPICE version 26 analysis (using window-based interactive mode on Linux/X-Windows):



In this analysis we see the open-circuit condition represented at the far left of the graph (maximum voltage, zero current) and the short-circuit condition represented at the far right (zero voltage[7], maximum current).

The amount of open-circuit voltage for each cell is primarily a function of the cell subcircuit's diode model (`vj` parameter defining its nominal forward-voltage drop, and `is` parameter defining its saturation current). The amount of short-circuit current for each cell is primarily a function of the cell's current source (I_{sc}). The slope of the voltage-current curve toward the right-hand side is primarily a function of the cell's internal parallel resistance (R_p).

One of the tremendous advantages of using subcircuits in SPICE netlists is also seen when using

[7] We actually see the voltage dip slightly below zero at a load current of 7.5 Amperes, because at this point I_{load} is actually behaving as a *source* rather than a load. This demonstrates that the array's short-circuit capability is actually slightly less than 7.5 Amperes.

subroutines in a computer programming language: by relegating the specific details of each solar cell to its own sub-set of the code, we may very easily make adjustments to that sub-set and watch the effects of those adjustments on the larger system. Imagine if we had to build a SPICE netlist without subcircuits, representing all 150 current sources, 150 diodes, 150 series resistors, and 150 parallel resistors! Not only would the netlist be enormous, but it would also be extremely tedious to alter any parameter(s) common to every cell.

Chapter 6

Gallery

All SPICE netlists showcased in this "Gallery" have been tested on two different versions of SPICE: SPICE version 2G6, and a modern variant of SPICE called NGSPICE (version 26 or newer). In most cases only one of these SPICE versions is used to generate the output.

When an analysis has been noted as "edited for brevity" it means that I have deleted unnecessary blank lines, unnecessary spaces, unnecessary characters, and all the statistical information typically output by SPICE in order to maximize the readability of the SPICE text output. This editing is especially important for those who wish to use the Gallery examples as practice problems (with answers provided by SPICE) for developing manual circuit analysis skills and do not care about the particulars of SPICE.

6.1 Using gallery examples for practice

Perhaps the most obvious use of the example netlists and analyses presented in this "Gallery" chapter is to learn how to write well-formed netlists for SPICE, and how to interpret the output generated by SPICE simulations. In other words, you may use these examples to help you learn how to use SPICE as a circuit simulation tool specific types of circuits.

However, this is not the only use of these examples. Students in quantitative fields of study such as electricity and electronics benefit from having sets of worked example problems to hone and test their burgeoning analytical skills. Textbooks commonly contain practice problems, followed by answers (at least for *some* of these problems!) located in an appendix against which students may self-check their own results. The SPICE example analyses presented in this "Gallery" chapter may serve as the same: sample problems complete with their own answer keys. Even more, once the basic syntax and netlist format of SPICE is mastered, students may use SPICE to generate answer keys for circuit problems of their own making, thus freeing them from the limitations of their textbooks' problem sets.

Here are some suggestions for using the Gallery examples as practice problems:

1. Take the given information presented in the circuit schematic diagrams (also in the corresponding SPICE netlists) and use your analytical skills to calculate those same voltages and/or currents that SPICE is tasked with computing. When you think you have a complete analysis, turn to the SPICE analysis to check if your answers match.

2. Take the circuit schematic diagram and the results of the SPICE analysis as given parameters, and then use your analytical skills to "work backwards" to one or more of the specified component values in the SPICE netlist. For example, taking the schematic diagram and component voltage drops, and then calculating source voltage/current from that.

3. Modify component values within a SPICE netlist and re-run the analysis to make a new quantitative problem with different given conditions.

4. Use SPICE to predict the effects of *qualitative* changes by either increasing or decreasing any one component's value and re-running the simulation, challenging yourself beforehand to predict all the effects of that qualitative change before letting SPICE tell you what will happen.

5. Use SPICE to predict the effects of *component faults* (e.g. opens and shorts) by altering resistance values to become very large (open) or very small (short), or by inserting high resistances in series with a component to simulate an "open" fault and low resistances in parallel to simulate a "short" fault. As with qualitative component value changes, you will challenging yourself beforehand to predict all the effects of that fault before letting SPICE tell you what will happen.

6.2 BJT amplifiers

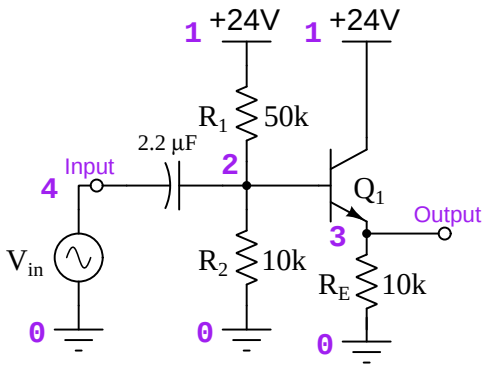
INCOMPLETE!

6.2.1 Common-collector amplifier

In this analysis we will use a sinusoidal input signal set to 60 Hz and a voltage divider network (R_1 and R_2) to properly bias the transistor so that it will be conducting with no input.

The transistor model used in this SPICE netlist is minimal, specifying only which type of BJT it is: in this case, *NPN*. The input signal coupling capacitor is pre-charged to 4 Volts (the same as the voltage divider bias network) in order to avoid the damped response typical of an un-charged coupling capacitor gradually charging to the bias voltage.

Circuit schematic diagram (with node numbers listed):



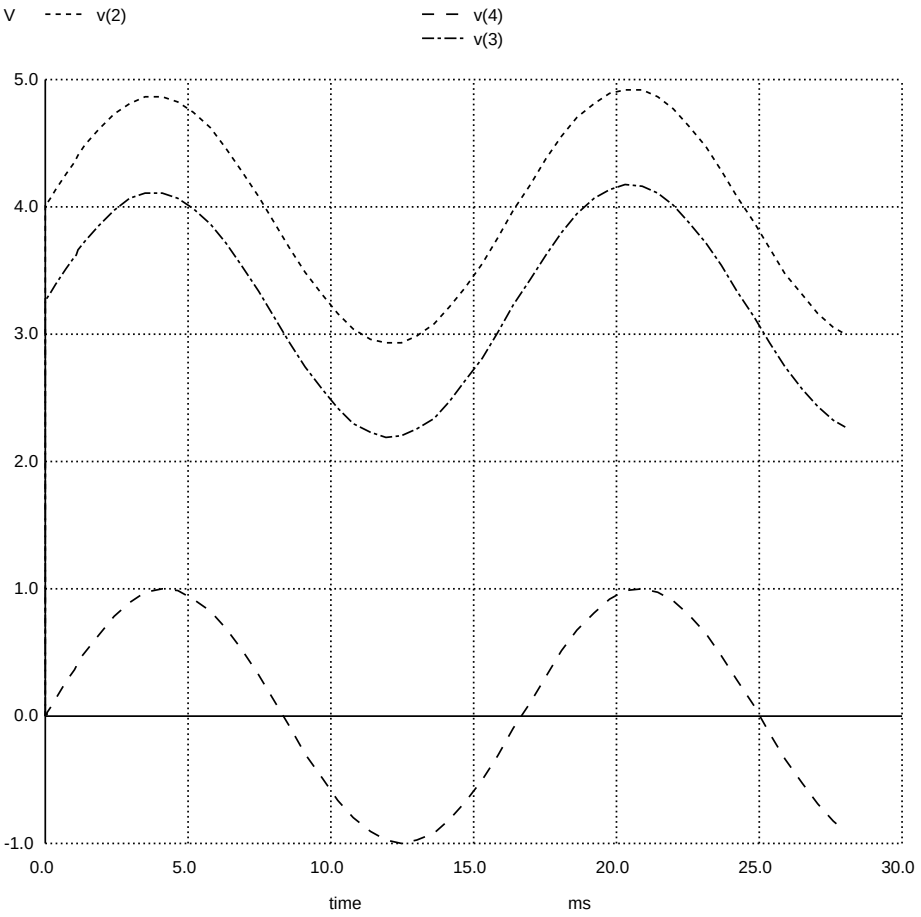
SPICE netlist:

```
* SPICE circuit
vsup 1 0 dc 24
vin 4 0 sin (0 1 60 0 0)
r1 1 2 50000
r2 2 0 10000
re 3 0 10e3
c1 2 4 2.2e-6 ic=4
q1 1 2 3 qmod
.model qmod npn
.tran 1m 28m uic
.plot tran v(4) v(2) v(3)
.width out=80
.end
```

SPICE version 2G6 analysis (edited for brevity):

```
legend:
 *: v(4)
 +: v(2)
 =: v(3)

     time      v(4)
(*)------------ -1.000E+00    -5.000E-01     0.000E+00     5.000E-01  1.000E+00
                - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(+=)-----------  2.000E+00     3.000E+00     4.000E+00     5.000E+00  6.000E+00
                - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
 0.000E+00  9.409E-09 .              .   =         x             .             .
 1.000E-03  3.661E-01 .              .       =     .    +    *   .             .
 2.000E-03  6.813E-01 .              .           = .        +    .    *        .
 3.000E-03  9.034E-01 .              .             .=         +  .          *  .
 4.000E-03  9.954E-01 .              .             . =          + .            *
 5.000E-03  9.462E-01 .              .             =          +  .           * .
 6.000E-03  7.663E-01 .              .          =  .       +     .      *      .
 7.000E-03  4.800E-01 .              .      =      .  +          *.             .
 8.000E-03  1.253E-01 .              . =         + .   *          .             .
 9.000E-03 -2.479E-01 .          =  .      x      .              .             .
 1.000E-02 -5.846E-01 .      =    * .  +          .              .             .
 1.100E-02 -8.399E-01 .   x         +             .              .             .
 1.200E-02 -9.795E-01 .* =         +.             .              .             .
 1.300E-02 -9.809E-01 .* =          +             .              .             .
 1.400E-02 -8.405E-01 .   * =       . +           .              .             .
 1.500E-02 -5.845E-01 .         = * .      +      .              .             .
 1.600E-02 -2.477E-01 .             .=     *   +  .              .             .
 1.700E-02  1.250E-01 .             .     =       .  +*          .             .
 1.800E-02  4.806E-01 .             .          =  .      +     *.             .
 1.900E-02  7.667E-01 .             .             =          +  .      *      .
 2.000E-02  9.458E-01 .             .             . =          +.           * .
 2.100E-02  9.942E-01 .             .             . =          +.             *
 2.200E-02  9.047E-01 .             .             =          +  .          *  .
 2.300E-02  6.819E-01 .             .          =  .      +      .    *        .
 2.400E-02  3.661E-01 .             .     =       . +       *   .             .
 2.500E-02  9.933E-05 .             .=         +  *             .             .
 2.600E-02 -3.670E-01 .         =   .   * +       .              .             .
 2.700E-02 -6.837E-01 .     =  *    . +           .              .             .
 2.800E-02 -9.048E-01 .  *=         +             .              .             .
                - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
```

NGSPICE version 26 analysis (using window-based interactive mode on Linux/X-Windows):



As you can see in this plot, the voltage at node 2 (with respect to ground, node 0) is biased from the input signal by +4 Volts, by virtue of the R_1/R_2 resistor network. This bias voltage is critically important for full-wave (Class A) operation of the amplifier. If not for this bias, the transistor would be completely cut off during most of the input waveform's cycle, amplifying only the upper-most positive peak of input signal (`v(5)`).

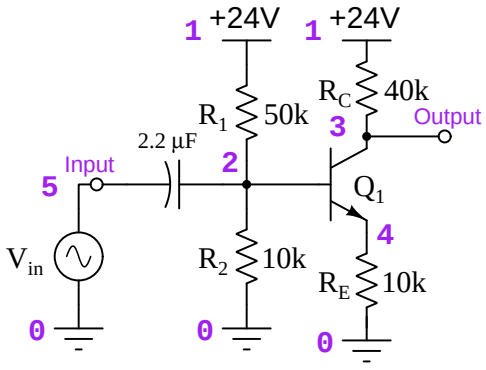
Also evident in this plot is the fact that the voltage gain of this amplifier circuit is nearly unity (1): the output waveform `v(3)` is only a bit smaller in amplitude than the input waveform `v(4)`. The offset between the collector and base voltages (both with respect to ground) is due to the constant voltage drop of the forward-biased base-emitter junction, in this case 0.6 Volts as assumed in SPICE's default BJT model.

6.2.2 Common-emitter amplifier

In this analysis we will use a sinusoidal input signal set to 60 Hz, a voltage divider network (R_1 and R_2) to properly bias the transistor so that it will be conducting with no input, and a collector/emitter resistor pair sized for a voltage gain of approximately 4.

The transistor model used in this SPICE netlist is minimal, specifying only which type of BJT it is: in this case, *NPN*. The input signal coupling capacitor is pre-charged to 4 Volts (the same as the voltage divider bias network) in order to avoid the damped response typical of an un-charged coupling capacitor gradually charging to the bias voltage.

Circuit schematic diagram (with node numbers listed):



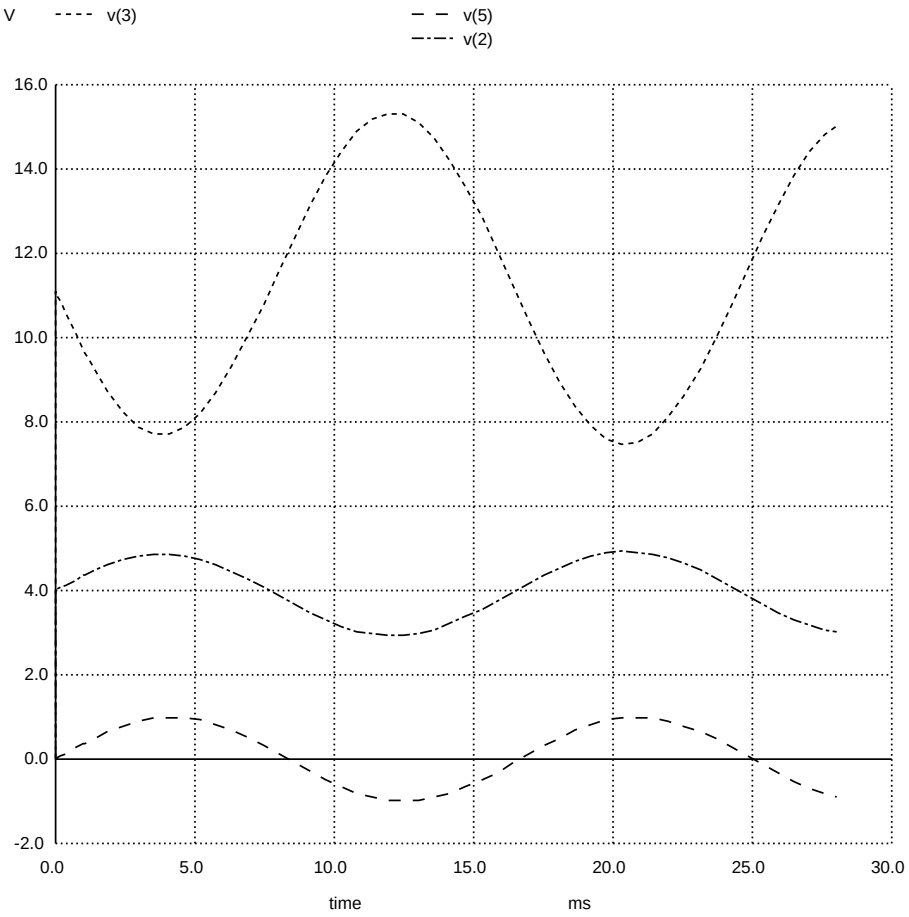
SPICE netlist:

```
* SPICE circuit
vsup 1 0 dc 24
vin 5 0 sin (0 1 60 0 0)
r1 1 2 50000
r2 2 0 10000
rc 1 3 40e3
re 4 0 10e3
c1 2 5 2.2e-6 ic=4
q1 3 2 4 qmod
.model qmod npn
.tran 1m 28m uic
.plot tran v(5) v(2) v(3)
.width out=80
.end
```

SPICE version 2G6 analysis (edited for brevity):

```
legend:
 *: v(5)
 +: v(2)
 =: v(3)

     time      v(5)
(*)------------ -1.000E+00    -5.000E-01     0.000E+00     5.000E-01  1.000E+00
                - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(+)------------  2.000E+00     3.000E+00     4.000E+00     5.000E+00  6.000E+00
                - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(=)------------  5.000E+00     1.000E+01     1.500E+01     2.000E+01  2.500E+01
                - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
 0.000E+00  9.409E-09 .             .  =          x             .            .
 1.000E-03  3.661E-01 .            =.             .    +    *   .            .
 2.000E-03  6.813E-01 .         =   .             .        +    .    *       .
 3.000E-03  9.034E-01 .       =     .             .          +  .          *  .
 4.000E-03  9.954E-01 .       =     .             .            + .            *
 5.000E-03  9.462E-01 .        =    .             .          +  .          * .
 6.000E-03  7.663E-01 .          =  .             .       +     .      *      .
 7.000E-03  4.800E-01 .             =             .  +         *.             .
 8.000E-03  1.253E-01 .             .   =       + .   *         .             .
 9.000E-03 -2.479E-01 .             .      x=     .             .             .
 1.000E-02 -5.846E-01 .           * .  +        = .             .             .
 1.100E-02 -8.399E-01 .   *         +            =             .             .
 1.200E-02 -9.795E-01 .*          +.             .=            .             .
 1.300E-02 -9.809E-01 .*          +              =             .             .
 1.400E-02 -8.405E-01 .   *         . +         = .             .             .
 1.500E-02 -5.845E-01 .           * .      + =    .             .             .
 1.600E-02 -2.477E-01 .             .    = *   +  .             .             .
 1.700E-02  1.250E-01 .             .=            .  +*         .             .
 1.800E-02  4.806E-01 .          =  .             .      +     *.             .
 1.900E-02  7.667E-01 .        =    .             .          +  .      *      .
 2.000E-02  9.458E-01 .      =      .             .            +.           * .
 2.100E-02  9.942E-01 .      =      .             .            +.             *
 2.200E-02  9.047E-01 .        =    .             .          +  .          *  .
 2.300E-02  6.819E-01 .           = .             .      +      .    *        .
 2.400E-02  3.661E-01 .             .=            . +       *   .             .
 2.500E-02  9.933E-05 .             .    =     +  *             .             .
 2.600E-02 -3.670E-01 .             .   * +  =    .             .             .
 2.700E-02 -6.837E-01 .        *    . +         = .             .             .
 2.800E-02 -9.048E-01 .  *          +            =             .             .
                - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
```

NGSPICE version 26 analysis (using window-based interactive mode on Linux/X-Windows):



As you can see in this plot, the voltage at node 2 (with respect to ground, node 0) is biased from the input signal by +4 Volts, by virtue of the R_1/R_2 resistor network. This bias voltage is critically important for full-wave (Class A) operation of the amplifier. If not for this bias, the transistor would be completely cut off during most of the input waveform's cycle, amplifying only the upper-most positive peak of input signal (`v(5)`).

Also evident in this plot is the fact that the voltage gain of this amplifier circuit is nearly four (4) as set by the 40 kΩ / 10 kΩ collector/emitter resistor ratio: the output waveform `v(3)` is only a bit smaller in amplitude than four times the input waveform `v(5)`.

6.2.3 Common-base amplifier

INCOMPLETE!
Circuit schematic diagram (with node numbers listed):
SPICE netlist:

```
* SPICE circuit
???
.end
```

SPICE version 2G6 analysis (edited for brevity):

```
???
```

NGSPICE version 26 analysis (using window-based interactive mode on Linux/X-Windows):

6.3 JFET amplifiers

INCOMPLETE!

6.3.1 Common-drain amplifier

INCOMPLETE!
Circuit schematic diagram (with node numbers listed):
SPICE netlist:

```
* SPICE circuit
???
.end
```

SPICE version 2G6 analysis (edited for brevity):

```
???
```

NGSPICE version 26 analysis (using window-based interactive mode on Linux/X-Windows):

6.3.2 Common-gate amplifier

INCOMPLETE!
Circuit schematic diagram (with node numbers listed):
SPICE netlist:

```
* SPICE circuit
???
.end
```

SPICE version 2G6 analysis (edited for brevity):

```
???
```

NGSPICE version 26 analysis (using window-based interactive mode on Linux/X-Windows):

6.4 Operational amplifiers

One of the idealized components offered in SPICE is a *voltage-controlled voltage source*, which serves well to model the behavior of an ideal differential-voltage input amplifier. This particular SPICE component, identified by the label `E`, is specified by its two input terminals, two output terminals, and voltage gain value. The general format for this component is shown below:

[**E***name*] [+output_node_ID] [−output_node_ID] [+input_node_ID] [−input_node_ID] [*gain*]

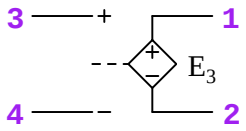
An example of a voltage-controlled voltage source is shown below:

- Name = *3*
- Polarity = *input on nodes 3 (+) and 4 (−) ; output on nodes 1 (+) and 2 (−)*
- Gain = *0.5 Volts output per Volt input*

Spice element description

```
E3 1 2 3 4 0.5
```

Schematic representation



$V_{out} = (0.5)(V_{in})$

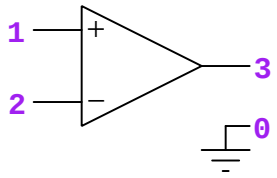
Operational amplifiers, of course, have extremely high differential voltage gains. An example of a voltage-controlled voltage source being used to model an opamp is shown below:

- Name = *opamp*
- Polarity = *input on nodes 1 (+) and 2 (−) ; output on nodes 3 with reference to ground (0)*
- Gain = 1×10^6

Spice element description

```
Eopamp 3 0 1 2 1e6
```

Schematic representation

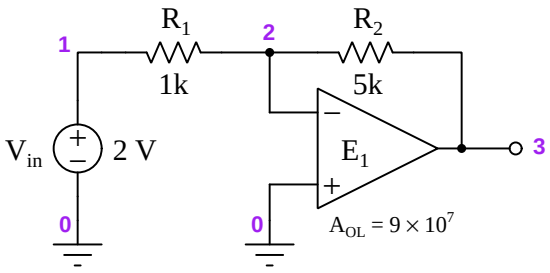


$V_{out} = (1 \times 10^6)(V_{in})$

6.4.1 Inverting amplifier

In this analysis we will test the operation of a simple inverting opamp amplifier circuit using a DC voltage source:

Circuit schematic diagram (with node numbers listed):



SPICE netlist:

```
* SPICE circuit
vin 1 0
r1 1 2 1000
r2 2 3 5000
e1 3 0 0 2 9e7
.dc vin 2 2 1
.print dc v(2) v(3)
.width out=80
.end
```

NGSPICE version 26 analysis (using batch mode on Linux console):

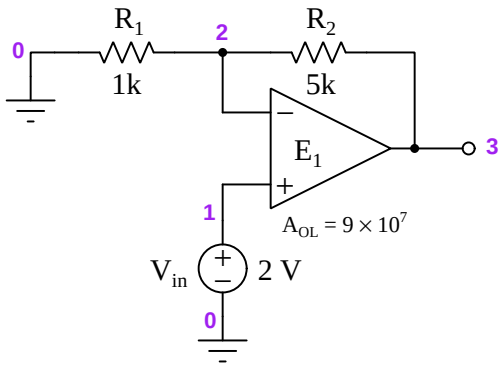
```
--------------------------------------------------
Index   v-sweep         v(2)            v(3)
--------------------------------------------------
0       2.000000e+00    1.11111e-07    -1.00000e+01
```

With an R_2/R_1 ratio of 5:1, this inverting amplifier circuit should have a gain of -5 ($-\frac{R_2}{R_1}$). This is proven by the fact it outputs -10 Volts for a V_{in} value of 2 Volts. Node 2 is the "virtual ground" point within this circuit, with negligible potential compared to the real ground (node 0).

6.4.2 Noninverting amplifier

In this analysis we will test the operation of a simple noninverting opamp amplifier circuit using a DC voltage source:

Circuit schematic diagram (with node numbers listed):



SPICE netlist:

```
* SPICE circuit
vin 1 0
r1 2 0 1000
r2 2 3 5000
e1 3 0 1 2 9e7
.dc vin 2 2 1
.print dc v(2) v(3)
.width out=80
.end
```

NGSPICE version 26 analysis (using batch mode on Linux console):

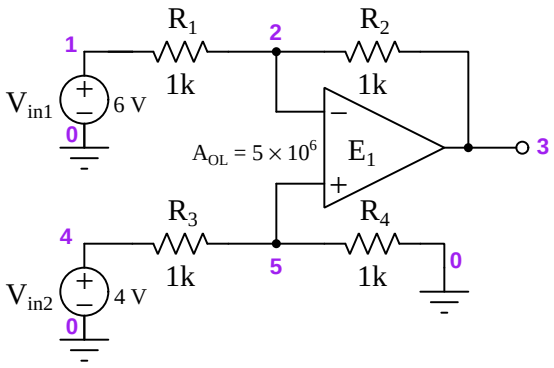
```
--------------------------------------------------
Index   v-sweep         v(2)            v(3)
--------------------------------------------------
0       2.000000e+00    2.000000e+00    1.200000e+01
```

With an R_2/R_1 ratio of 5:1, this inverting amplifier circuit should have a gain of 6 ($\frac{R_2}{R_1} + 1$). This is proven by the fact it outputs 12 Volts for a V_{in} value of 2 Volts. The voltage measured at node 2 with respect to ground matches V_{in} with negligible error.

6.4.3 Subtracting amplifier

In this analysis we will test the operation of a simple subtractor (or differential amplifier with a voltage gain of one) using a DC voltage source:

Circuit schematic diagram (with node numbers listed):



SPICE netlist:

```
* SPICE circuit
vin1 1 0
vin2 4 0 dc 4
r1 1 2 1000
r2 2 3 1000
r3 4 5 1000
r4 5 0 1000
e1 3 0 5 2 5e6
.dc vin1 6 6 1
.print dc v(2,5) v(3)
.width out=80
.end
```

NGSPICE version 26 analysis (using batch mode on Linux console):

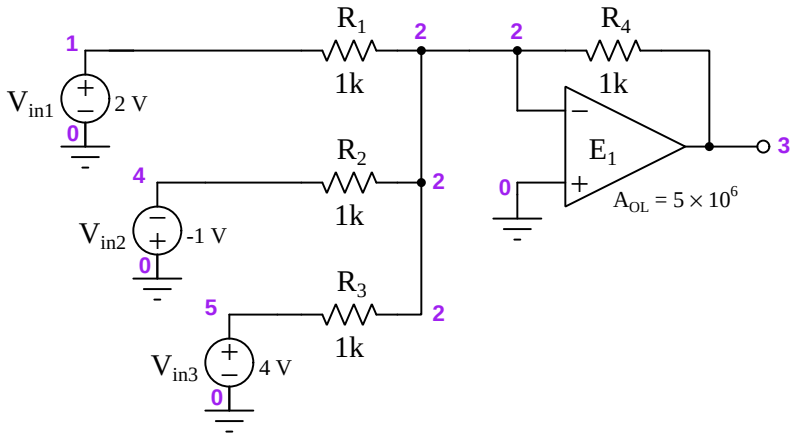
```
--------------------------------------------------------------------------------
Index   v-sweep         v(2)-v(5)       v(3)
--------------------------------------------------------------------------------
0       6.000000e+00    3.999998e-07   -2.00000e+00
```

With equal-valued resistors throughout, this subtracting amplifier circuit should have a voltage gain of 1. This is proven by the fact it outputs -2 Volts given 4 Volts at the noninverting input and 6 Volts at the inverting input. The voltage measured between nodes 2 and 5 is negligible due to the action of negative feedback.

6.4.4 Inverting summer

In this analysis we will test the operation of an inverting summer using three DC voltage sources:

Circuit schematic diagram (with node numbers listed):



SPICE netlist:

```
* SPICE circuit
vin1 1 0
vin2 0 4 dc 1
vin3 5 0 dc 4
r1 1 2 1000
r2 4 2 1000
r3 5 2 1000
r4 2 3 1000
e1 3 0 0 2 5e6
.dc vin1 2 2 1
.print dc v(2) v(3)
.width out=80
.end
```

NGSPICE version 26 analysis (using batch mode on Linux console):

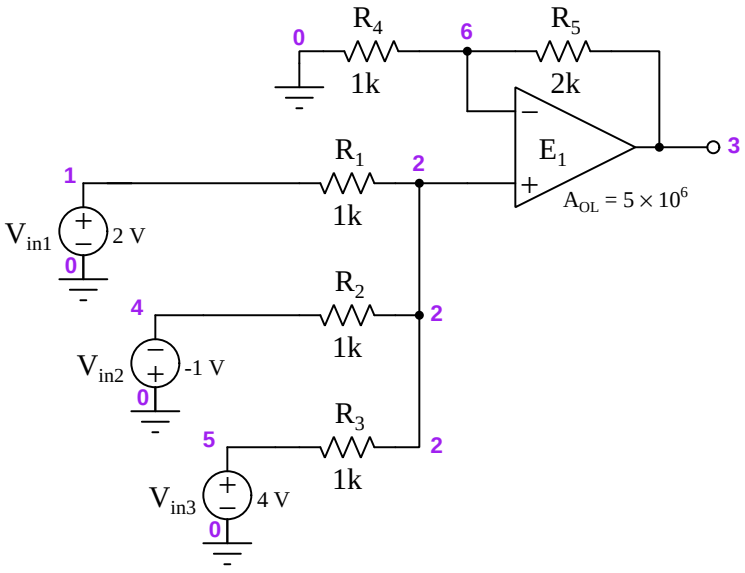
```
--------------------------------------------------------------------------------
Index   v-sweep         v(2)            v(3)
--------------------------------------------------------------------------------
0       2.000000e+00    9.999992e-07    -5.00000e+00
```

With equal-valued resistors throughout, this inverting summer circuit should have a voltage gain of -1. This is proven by the fact it outputs -5 Volts given the three input signals of $+2$ Volts, -1 Volt, and $+4$ Volts. The voltage measured between nodes 2 and 5 is negligible due to the action of negative feedback.

6.4.5 Non-inverting summer

In this analysis we will test the operation of a non-inverting summer using three DC voltage sources:

Circuit schematic diagram (with node numbers listed):



SPICE netlist:

```
* SPICE circuit
vin1 1 0
vin2 0 4 dc 1
vin3 5 0 dc 4
r1 1 2 1000
r2 4 2 1000
r3 5 2 1000
r4 6 0 1000
r5 3 6 2000
e1 3 0 2 6 5e6
.dc vin1 2 2 1
.print dc v(2) v(3)
.width out=80
.end
```

NGSPICE version 26 analysis (using batch mode on Linux console):

```
--------------------------------------------------------------------------------
Index   v-sweep         v(2)            v(3)
--------------------------------------------------------------------------------
0       2.000000e+00    1.666667e+00    4.999997e+00
```

With R_5 having twice the resistance of R_4, this non-inverting circuit should have a voltage gain of 3, which is what we need to take the passive averager network's voltage (between node 2 and ground) and convert that into a sum. This is proven by the fact it outputs +5 Volts given the three input signals of +2 Volts, −1 Volt, and +4 Volts. The voltage measured between nodes 2 and 0 shows the average of +2, −1, and +4 Volts.

Appendix A

Problem-Solving Strategies

The ability to solve complex problems is arguably one of the most valuable skills one can possess, and this skill is particularly important in any science-based discipline.

- Study principles, not procedures. Don't be satisfied with merely knowing how to compute solutions – learn *why* those solutions work.
- Identify what it is you need to solve, identify all relevant data, identify all units of measurement, identify any general principles or formulae linking the given information to the solution, and then identify any "missing pieces" to a solution. Annotate all diagrams with this data.
- Sketch a diagram to help visualize the problem. When building a real system, always devise a plan for that system and analyze its function *before* constructing it.
- Follow the units of measurement and meaning of every calculation. If you are ever performing mathematical calculations as part of a problem-solving procedure, and you find yourself unable to apply each and every intermediate result to some aspect of the problem, it means you don't understand what you are doing. Properly done, every mathematical result should have practical meaning for the problem, and not just be an abstract number. You should be able to identify the proper units of measurement for each and every calculated result, and show where that result fits into the problem.
- Perform "thought experiments" to explore the effects of different conditions for theoretical problems. When troubleshooting real systems, perform *diagnostic tests* rather than visually inspecting for faults, the best diagnostic test being the one giving you the most information about the nature and/or location of the fault with the fewest steps.
- Simplify the problem until the solution becomes obvious, and then use that obvious case as a model to follow in solving the more complex version of the problem.
- Check for exceptions to see if your solution is incorrect or incomplete. A good solution will work for *all* known conditions and criteria. A good example of this is the process of testing scientific hypotheses: the task of a scientist is not to find support for a new idea, but rather to *challenge* that new idea to see if it holds up under a battery of tests. The philosophical

principle of *reductio ad absurdum* (i.e. disproving a general idea by finding a specific case where it fails) is useful here.

- Work "backward" from a hypothetical solution to a new set of given conditions.
- Add quantities to problems that are qualitative in nature, because sometimes a little math helps illuminate the scenario.
- Sketch graphs illustrating how variables relate to each other. These may be quantitative (i.e. with realistic number values) or qualitative (i.e. simply showing increases and decreases).
- Treat quantitative problems as qualitative in order to discern the relative magnitudes and/or directions of change of the relevant variables. For example, try determining what happens if a certain variable were to increase or decrease before attempting to precisely calculate quantities: how will each of the dependent variables respond, by increasing, decreasing, or remaining the same as before?
- Consider limiting cases. This works especially well for qualitative problems where you need to determine which direction a variable will change. Take the given condition and magnify that condition to an extreme degree as a way of simplifying the direction of the system's response.
- Check your work. This means regularly testing your conclusions to see if they make sense. This does *not* mean repeating the same steps originally used to obtain the conclusion(s), but rather to use some other means to check validity. Simply repeating procedures often leads to *repeating the same errors* if any were made, which is why alternative paths are better.

Appendix B

Instructional philosophy

"The unexamined circuit is not worth energizing" – Socrates (if he had taught electricity)

These learning modules, although useful for self-study, were designed to be used in a formal learning environment where a subject-matter expert challenges students to digest the content and exercise their critical thinking abilities in the answering of questions and in the construction and testing of working circuits.

The following principles inform the instructional and assessment philosophies embodied in these learning modules:

- The first goal of education is to enhance clear and independent thought, in order that every student reach their fullest potential in a highly complex and inter-dependent world. Robust reasoning is *always* more important than particulars of any subject matter, because its application is universal.
- Literacy is fundamental to independent learning and thought because text continues to be the most efficient way to communicate complex ideas over space and time. Those who cannot read with ease are limited in their ability to acquire knowledge and perspective.
- Articulate communication is fundamental to work that is complex and interdisciplinary.
- Faulty assumptions and poor reasoning are best corrected through challenge, not presentation. The rhetorical technique of *reductio ad absurdum* (disproving an assertion by exposing an absurdity) works well to discipline student's minds, not only to correct the problem at hand but also to learn how to detect and correct future errors.
- Important principles should be repeatedly explored and widely applied throughout a course of study, not only to reinforce their importance and help ensure their mastery, but also to showcase the interconnectedness and utility of knowledge.

These learning modules were expressly designed to be used in an "inverted" teaching environment[1] where students first read the introductory and tutorial chapters on their own, then individually attempt to answer the questions and construct working circuits according to the experiment and project guidelines. The instructor never lectures, but instead meets regularly with each individual student to review their progress, answer questions, identify misconceptions, and challenge the student to new depths of understanding through further questioning. Regular meetings between instructor and student should resemble a Socratic[2] dialogue, where questions serve as scalpels to dissect topics and expose assumptions. The student passes each module only after consistently demonstrating their ability to logically analyze and correctly apply all major concepts in each question or project/experiment. The instructor must be vigilant in probing each student's understanding to ensure they are truly *reasoning* and not just *memorizing*. This is why "Challenge" points appear throughout, as prompts for students to think deeper about topics and as starting points for instructor queries. Sometimes these challenge points require additional knowledge that hasn't been covered in the series to answer in full. This is okay, as the major purpose of the Challenges is to stimulate analysis and synthesis on the part of each student.

The instructor must possess enough mastery of the subject matter and awareness of students' reasoning to generate their own follow-up questions to practically any student response. Even completely correct answers given by the student should be challenged by the instructor for the purpose of having students practice articulating their thoughts and defending their reasoning. Conceptual errors committed by the student should be exposed and corrected not by direct instruction, but rather by reducing the errors to an absurdity[3] through well-chosen questions and thought experiments posed by the instructor. Becoming proficient at this style of instruction requires time and dedication, but the positive effects on critical thinking for both student and instructor are spectacular.

An inspection of these learning modules reveals certain unique characteristics. One of these is a bias toward thorough explanations in the tutorial chapters. Without a live instructor to explain concepts and applications to students, the text itself must fulfill this role. This philosophy results in lengthier explanations than what you might typically find in a textbook, each step of the reasoning process fully explained, including footnotes addressing common questions and concerns students raise while learning these concepts. Each tutorial seeks to not only explain each major concept in sufficient detail, but also to explain the logic of each concept and how each may be developed

[1] In a traditional teaching environment, students first encounter new information via *lecture* from an expert, and then independently apply that information via *homework*. In an "inverted" course of study, students first encounter new information via *homework*, and then independently apply that information under the scrutiny of an expert. The expert's role in lecture is to simply *explain*, but the expert's role in an inverted session is to *challenge*, *critique*, and if necessary *explain* where gaps in understanding still exist.

[2] Socrates is a figure in ancient Greek philosophy famous for his unflinching style of questioning. Although he authored no texts, he appears as a character in Plato's many writings. The essence of Socratic philosophy is to leave no question unexamined and no point of view unchallenged. While purists may argue a topic such as electric circuits is too narrow for a true Socratic-style dialogue, I would argue that the essential thought processes involved with scientific reasoning on *any* topic are not far removed from the Socratic ideal, and that students of electricity and electronics would do very well to challenge assumptions, pose thought experiments, identify fallacies, and otherwise employ the arsenal of critical thinking skills modeled by Socrates.

[3] This rhetorical technique is known by the Latin phrase *reductio ad absurdum*. The concept is to expose errors by counter-example, since only one solid counter-example is necessary to disprove a universal claim. As an example of this, consider the common misconception among beginning students of electricity that voltage cannot exist without current. One way to apply *reductio ad absurdum* to this statement is to ask how much current passes through a fully-charged battery connected to nothing (i.e. a clear example of voltage existing without current).

from "first principles". Again, this reflects the goal of developing clear and independent thought in students' minds, by showing how clear and logical thought was used to forge each concept. Students benefit from witnessing a model of clear thinking in action, and these tutorials strive to be just that.

Another characteristic of these learning modules is a lack of step-by-step instructions in the Project and Experiment chapters. Unlike many modern workbooks and laboratory guides where step-by-step instructions are prescribed for each experiment, these modules take the approach that students must learn to closely read the tutorials and apply their own reasoning to identify the appropriate experimental steps. Sometimes these steps are plainly declared in the text, just not as a set of enumerated points. At other times certain steps are implied, an example being assumed competence in test equipment use where the student should not need to be told *again* how to use their multimeter because that was thoroughly explained in previous lessons. In some circumstances no steps are given at all, leaving the entire procedure up to the student.

This lack of prescription is not a flaw, but rather a feature. Close reading and clear thinking are foundational principles of this learning series, and in keeping with this philosophy all activities are designed to *require* those behaviors. Some students may find the lack of prescription frustrating, because it demands more from them than what their previous educational experiences required. This frustration should be interpreted as an unfamiliarity with autonomous thinking, a problem which must be corrected if the student is ever to become a self-directed learner and effective problem-solver. Ultimately, the need for students to read closely and think clearly is more important both in the near-term and far-term than any specific facet of the subject matter at hand. If a student takes longer than expected to complete a module because they are forced to outline, digest, and reason on their own, so be it. The future gains enjoyed by developing this mental discipline will be well worth the additional effort and delay.

Another feature of these learning modules is that they do not treat topics in isolation. Rather, important concepts are introduced early in the series, and appear repeatedly as stepping-stones toward other concepts in subsequent modules. This helps to avoid the "compartmentalization" of knowledge, demonstrating the inter-connectedness of concepts and simultaneously reinforcing them. Each module is fairly complete in itself, reserving the beginning of its tutorial to a review of foundational concepts.

This methodology of assigning text-based modules to students for digestion and then using Socratic dialogue to assess progress and hone students' thinking was developed over a period of several years by the author with his Electronics and Instrumentation students at the two-year college level. While decidedly unconventional and sometimes even unsettling for students accustomed to a more passive lecture environment, this instructional philosophy has proven its ability to convey conceptual mastery, foster careful analysis, and enhance employability so much better than lecture that the author refuses to ever teach by lecture again.

Problems which often go undiagnosed in a lecture environment are laid bare in this "inverted" format where students must articulate and logically defend their reasoning. This, too, may be unsettling for students accustomed to lecture sessions where the instructor cannot tell for sure who comprehends and who does not, and this vulnerability necessitates sensitivity on the part of the "inverted" session instructor in order that students never feel discouraged by having their errors exposed. *Everyone* makes mistakes from time to time, and learning is a lifelong process! Part of the instructor's job is to build a culture of learning among the students where errors are not seen as shameful, but rather as opportunities for progress.

To this end, instructors managing courses based on these modules should adhere to the following principles:

- Student questions are always welcome and demand thorough, honest answers. The only type of question an instructor should refuse to answer is one the student should be able to easily answer on their own. Remember, *the fundamental goal of education is for each student to learn to think clearly and independently.* This requires hard work on the part of the student, which no instructor should ever circumvent. Anything done to bypass the student's responsibility to do that hard work ultimately limits that student's potential and thereby does real harm.

- It is not only permissible, but encouraged, to answer a student's question by asking questions in return, these follow-up questions designed to guide the student to reach a correct answer through their own reasoning.

- All student answers demand to be challenged by the instructor and/or by other students. This includes both correct and incorrect answers – the goal is to practice the articulation and defense of one's own reasoning.

- No reading assignment is deemed complete unless and until the student demonstrates their ability to accurately summarize the major points in their own terms. Recitation of the original text is unacceptable. This is why every module contains an "Outline and reflections" question as well as a "Foundational concepts" question in the Conceptual reasoning section, to prompt reflective reading.

- No assigned question is deemed answered unless and until the student demonstrates their ability to consistently and correctly apply the concepts to *variations* of that question. This is why module questions typically contain multiple "Challenges" suggesting different applications of the concept(s) as well as variations on the same theme(s). Instructors are encouraged to devise as many of their own "Challenges" as they are able, in order to have a multitude of ways ready to probe students' understanding.

- No assigned experiment or project is deemed complete unless and until the student demonstrates the task in action. If this cannot be done "live" before the instructor, video-recordings showing the demonstration are acceptable. All relevant safety precautions must be followed, all test equipment must be used correctly, and the student must be able to properly explain all results. The student must also successfully answer all Challenges presented by the instructor for that experiment or project.

Students learning from these modules would do well to abide by the following principles:

- No text should be considered fully and adequately read unless and until you can express every idea *in your own words, using your own examples.*
- You should always articulate your thoughts as you read the text, noting points of agreement, confusion, and epiphanies. Feel free to print the text on paper and then write your notes in the margins. Alternatively, keep a journal for your own reflections as you read. This is truly a helpful tool when digesting complicated concepts.
- Never take the easy path of highlighting or underlining important text. Instead, *summarize* and/or *comment* on the text using your own words. This actively engages your mind, allowing you to more clearly perceive points of confusion or misunderstanding on your own.
- A very helpful strategy when learning new concepts is to place yourself in the role of a teacher, if only as a mental exercise. Either explain what you have recently learned to someone else, or at least *imagine* yourself explaining what you have learned to someone else. The simple act of having to articulate new knowledge and skill forces you to take on a different perspective, and will help reveal weaknesses in your understanding.
- Perform each and every mathematical calculation and thought experiment shown in the text on your own, referring back to the text to see that your results agree. This may seem trivial and unnecessary, but it is critically important to ensuring you actually understand what is presented, especially when the concepts at hand are complicated and easy to misunderstand. Apply this same strategy to become proficient in the use of *circuit simulation software*, checking to see if your simulated results agree with the results shown in the text.
- Above all, recognize that learning is hard work, and that a certain level of frustration is unavoidable. There are times when you will struggle to grasp some of these concepts, and that struggle is a natural thing. Take heart that it will yield with persistent and varied[4] effort, and never give up!

Students interested in using these modules for self-study will also find them beneficial, although the onus of responsibility for thoroughly reading and answering questions will of course lie with that individual alone. If a qualified instructor is not available to challenge students, a workable alternative is for students to form study groups where they challenge[5] one another.

To high standards of education,

Tony R. Kuphaldt

[4] As the old saying goes, "Insanity is trying the same thing over and over again, expecting different results." If you find yourself stumped by something in the text, you should attempt a different approach. Alter the thought experiment, change the mathematical parameters, do whatever you can to see the problem in a slightly different light, and then the solution will often present itself more readily.

[5] Avoid the temptation to simply share answers with study partners, as this is really counter-productive to learning. Always bear in mind that the answer to any question is far less important in the long run than the method(s) used to obtain that answer. The goal of education is to empower one's life through the improvement of clear and independent thought, literacy, expression, and various practical skills.

Appendix C

Tools used

I am indebted to the developers of many open-source software applications in the creation of these learning modules. The following is a list of these applications with some commentary on each.

You will notice a theme common to many of these applications: a bias toward *code*. Although I am by no means an expert programmer in any computer language, I understand and appreciate the flexibility offered by code-based applications where the user (you) enters commands into a plain ASCII text file, which the software then reads and processes to create the final output. Code-based computer applications are by their very nature *extensible*, while WYSIWYG (What You See Is What You Get) applications are generally limited to whatever user interface the developer makes for you.

The `GNU/Linux` computer operating system

> There is so much to be said about Linus Torvalds' `Linux` and Richard Stallman's `GNU` project. First, to credit just these two individuals is to fail to do justice to the *mob* of passionate volunteers who contributed to make this amazing software a reality. I first learned of `Linux` back in 1996, and have been using this operating system on my personal computers almost exclusively since then. It is *free*, it is completely *configurable*, and it permits the continued use of highly efficient `Unix` applications and scripting languages (e.g. shell scripts, Makefiles, `sed`, `awk`) developed over many decades. `Linux` not only provided me with a powerful computing platform, but its open design served to inspire my life's work of creating open-source educational resources.

Bram Moolenaar's `Vim` text editor

> Writing code for any code-based computer application requires a *text editor*, which may be thought of as a word processor strictly limited to outputting plain-ASCII text files. Many good text editors exist, and one's choice of text editor seems to be a deeply personal matter within the programming world. I prefer `Vim` because it operates very similarly to `vi` which is ubiquitous on `Unix`/`Linux` operating systems, and because it may be entirely operated via keyboard (i.e. no mouse required) which makes it fast to use.

Donald Knuth's TEX typesetting system

Developed in the late 1970's and early 1980's by computer scientist extraordinaire Donald Knuth to typeset his multi-volume magnum opus *The Art of Computer Programming*, this software allows the production of formatted text for screen-viewing or paper printing, all by writing plain-text code to describe how the formatted text is supposed to appear. TEX is not just a markup language for documents, but it is also a Turing-complete programming language in and of itself, allowing useful algorithms to be created to control the production of documents. Simply put, TEX *is a programmer's approach to word processing*. Since TEX is controlled by code written in a plain-text file, this means anyone may read that plain-text file to see exactly how the document was created. This openness afforded by the code-based nature of TEX makes it relatively easy to learn how other people have created their own TEX documents. By contrast, examining a beautiful document created in a conventional WYSIWYG word processor such as Microsoft `Word` suggests nothing to the reader about *how* that document was created, or what the user might do to create something similar. As Mr. Knuth himself once quipped, conventional word processing applications should be called WYSIAYG (What You See Is *All* You Get).

Leslie Lamport's LATEX extensions to TEX

Like all true programming languages, TEX is inherently extensible. So, years after the release of TEX to the public, Leslie Lamport decided to create a massive extension allowing easier compilation of book-length documents. The result was LATEX, which is the markup language used to create all ModEL module documents. You could say that TEX is to LATEX as `C` is to `C++`. This means it is permissible to use any and all TEX commands within LATEX source code, and it all still works. Some of the features offered by LATEX that would be challenging to implement in TEX include automatic index and table-of-content creation.

Tim Edwards' `Xcircuit` drafting program

This wonderful program is what I use to create all the schematic diagrams and illustrations (but not photographic images or mathematical plots) throughout the ModEL project. It natively outputs PostScript format which is a true vector graphic format (this is why the images do not pixellate when you zoom in for a closer view), and it is so simple to use that I have never had to read the manual! Object libraries are easy to create for `Xcircuit`, being plain-text files using PostScript programming conventions. Over the years I have collected a large set of object libraries useful for drawing electrical and electronic schematics, pictorial diagrams, and other technical illustrations.

`Gimp` graphic image manipulation program

Essentially an open-source clone of Adobe's `PhotoShop`, I use `Gimp` to resize, crop, and convert file formats for all of the photographic images appearing in the ModEL modules. Although `Gimp` does offer its own scripting language (called `Script-Fu`), I have never had occasion to use it. Thus, my utilization of `Gimp` to merely crop, resize, and convert graphic images is akin to using a sword to slice bread.

`SPICE` circuit simulation program

`SPICE` is to circuit analysis as TEX is to document creation: it is a form of markup language designed to describe a certain object to be processed in plain-ASCII text. When the plain-text "source file" is compiled by the software, it outputs the final result. More modern circuit analysis tools certainly exist, but I prefer `SPICE` for the following reasons: it is *free*, it is *fast*, it is *reliable*, and it is a fantastic tool for *teaching* students of electricity and electronics how to write simple code. I happen to use rather old versions of `SPICE`, version 2g6 being my "go to" application when I only require text-based output. `NGSPICE` (version 26), which is based on Berkeley `SPICE` version 3f5, is used when I require graphical output for such things as time-domain waveforms and Bode plots. In all `SPICE` example netlists I strive to use coding conventions compatible with all `SPICE` versions.

Andrew D. Hwang's `ePiX` mathematical visualization programming library

This amazing project is a `C++` library you may link to any `C/C++` code for the purpose of generating PostScript graphic images of mathematical functions. As a completely free and open-source project, it does all the plotting I would otherwise use a Computer Algebra System (CAS) such as `Mathematica` or `Maple` to do. It should be said that `ePiX` is *not* a Computer Algebra System like `Mathematica` or `Maple`, but merely a mathematical *visualization* tool. In other words, it won't determine integrals for you (you'll have to implement that in your own `C/C++` code!), but it can graph the results, and it does so beautifully. What I really admire about `ePiX` is that it is a `C++` programming library, which means it builds on the existing power and toolset available with that programming language. Mr. Hwang could have probably developed his own stand-alone application for mathematical plotting, but by creating a `C++` library to do the same thing he accomplished something much greater.

`gnuplot` mathematical visualization software

Another open-source tool for mathematical visualization is `gnuplot`. Interestingly, this tool is *not* part of Richard Stallman's GNU project, its name being a coincidence. For this reason the authors prefer "gnu" *not* be capitalized at all to avoid confusion. This is a much "lighter-weight" alternative to a spreadsheet for plotting tabular data, and the fact that it easily outputs directly to an X11 console or a file in a number of different graphical formats (including PostScript) is very helpful. I typically set my `gnuplot` output format to default (X11 on my Linux PC) for quick viewing while I'm developing a visualization, then switch to PostScript file export once the visual is ready to include in the document(s) I'm writing. As with my use of `Gimp` to do rudimentary image editing, my use of `gnuplot` only scratches the surface of its capabilities, but the important points are that it's *free* and that it *works well*.

`Python` programming language

Both Python and C++ find extensive use in these modules as instructional aids and exercises, but I'm listing Python here as a *tool* for myself because I use it almost daily as a *calculator*. If you open a Python interpreter console and type `from math import *` you can type mathematical expressions and have it return results just as you would on a hand calculator. Complex-number (i.e. *phasor*) arithmetic is similarly supported if you include the complex-math library (`from cmath import *`). Examples of this are shown in the Programming References chapter (if included) in each module. Of course, being a fully-featured programming language, Python also supports conditionals, loops, and other structures useful for calculation of quantities. Also, running in a console environment where all entries and returned values show as text in a chronologically-ordered list makes it easy to copy-and-paste those calculations to document exactly how they were performed.

Appendix D

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Appendix E

References

Vladimirescu, Andrei, *The Spice Book*, John Wiley & Sons, New York, 1994.

Appendix F

Version history

This is a list showing all significant additions, corrections, and other edits made to this learning module. Each entry is referenced by calendar date in reverse chronological order (newest version first), which appears on the front cover of every learning module for easy reference. Any contributors to this open-source document are listed here as well.

6 September 2024 – re-named the "Introduction" chapter to be called "What is SPICE?", so that later I may add an "Introduction" chapter more aligned with other modules' Introduction chapters.

2 November 2023 – added more opamp example circuits (subtractor and summers).

1 November 2021 – fixed netlist errors in operational amplifier simulations, where I had the inverting and non-inverting nodes swapped (!).

17 December 2020 – uncommented "using SPICE" lines so that this chapter would exist in the document.

12 February 2020 – added some operational amplifier examples to the Gallery chapter.

7 April 2019 – added introductory section to the Gallery chapter discussing the use of SPICE as a tool for generating answers for practice problem sets.

October 2018 – document first published.

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